SDS 930 Examiner Automatic Instruction Diagnostics
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This archive contains the files needed to run the SDS 930 Examiner Automatic Instruction Diagnostics as modified by Mark Emmer, marke@SNOBOL4.com

The original source was meant to be assembled with the Meta-Symbol assembler under the Monarch tape O/S. It was designed to run on a 4K system, was loaded at location 2 by a non-standard bootstrap loader and just fit in the ending address 7777B.

To use the standard SIMH bootstrap in locations 2-11B, this code was moved up to location 12B and it runs over the 4K boundary to 10001B despite removing a few unused storage cells. It works with the SIMH SDS 940 boot command. The 940 emulation runs the diagnostics in Normal (SDS 930) mode.

The source was edited for ARPAS compatibility:

1. HLT requires an operand (typically 0)
2. No PAGE directive
3. Octal constants require a B suffix
4. No PZE pseudo-op to get a 0 placeholder.
5. '7' used as a label, not allowed
6. CLR in 930 assembler in CLAB in ARPAS
7. Remove the ORG so it's relocatable
8. EOM 20001B (REO) is being relocated by NARP. Needs to be EOM =20001B
9. L0 is hardcoded considering a ORG 3 start address, not 12B. 77 needs to be changed by adding 7B to it. Or using address of first test minus 11 decimal.

240 source lines were missing from the original tape file. Code from ADC7 through SKG1 was manually entered from book listing.

The interrupt enable and disable instructions IET and IDT are defined incorrectly in ARPAS, requiring a patched ARPAS to get it to assemble properly.

The modified source file was assembled using the ARPAS assembler under the SDS 940 Berkeley TSS simulation, loaded in DDT at offset 12B, then memory from 12B to 10001B was saved as a memory Save file. The Save and assembler listing files were transferred back to the host (Windows 10) system via simulated paper tape, then converted to mag tape boot and ASCII text files using tools created by Mark Emmer.

The code corresponds to the version in 900097A_ExaminerDiagnosticVol1_Sep64.pdf, beginning at PDF page 87, entitled 930 Instruction Diagnostic Loader. The memory addresses won't match because of the above changes.

Examiner is now a SIMH mag tape bootstrap file, boot_diag.tap. The SIMH command file boot_diag.mt0 will boot the diagnostic in file boot_diag.tap and stop the simulator at

location 12B, the first location of the program.

Run the program with this command:

sds boot_diag.mt0

Once loaded and stopped at the location 12B breakpoint, type ‘cont’ to begin execution, or ‘step’ to step through the machine instructions in the diagnostic.

The program loops continuously if it passes all tests and produces no output messages. The simulator can be interrupted by typing control-E.

break 121 inserts a program breakpoint at the completion of the test loop.

The console breakpoint switches can be used to control diagnostic behavior:

BPT1 - On error, repeat the test. Do not advance to the next test.
BPT2 - Don't halt on error
BPT3 - Halt between tests

Breakpoint switches can be set with the SIMH command:

dep bptn x

where n is 1, 2, 3, or 4 and x is 0 or 1.

Each test is controlled by a table of values, those entities set before the test instruction is executed, and their expected values after execution. The value pairs in each table are in this order: A, B, X, Memory, and finally two values to set/reset overflow before the test, and the expected overflow value after the test.

The various halt locations are:

57B - A register error
65B - B register error
73B - X register error
101B - Memory error
106B - Overflow error (should be set)
114B - No overflow error (should not be set)

For halts at 57B-101B, register A contains the actual result, register B contains the expected result. Examine registers in simh with:

ex a-x or ex p-x to see the program counter as well.

For all test halts, register X+1 points to the offending instruction and test table. See the listing file for details of the test and expected result values.

A problematic shift instruction at label LSH12 that appears as LCY* MEMORY. MEMORY is cleverly constructed to produce a shift count of 777B. Some versions of the simulator erroneously treat cyclic shift counts as modulo 48. The diagnostic runs correctly once sds_cpu.c shift instructions are changed to use:

```
  if (sc > 48)
    sc=48
```

for all shifts. This correct interpretation is based on the SDS logic diagrams and equations.

SDS documentation manual 900097A_ExaminerDiagnosticVol1_Sep64 is available at:
HYPERLINK "https://bitsavers.org/pdf/sds/9xx/diagnostic/900097A_ExaminerDiagnosticVol1_Sep64.pdf"https://bitsavers.org/pdf/sds/9xx/diagnostic/900097A_ExaminerDiagnosticVol1_Sep64.pdf
(PDF pages 87-223, manual pages 237-372, Automatic Instruction Test)

Files in the zip archive:

boot_diag.mt0	SIMH command file to boot from mag tape unit 0
boot_diag.tap	Diag mag tape boot file
DIAG2.asm	ARPAS source
Ldiag2.txt	Diag listing output:
Readme.doc	this file
SDS.exe	SIMH SDS940 simulator V4.0-0 Current with cyclic shift instructions fixed