SYSTEMASTER

User Manual

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I. PRODUCT DESCRIPTION

The SYSTEMASTER is a microcomputer on a board. It incorporates most of the features required in a small computing system including a CPU, 64k bytes of RAM, serial and parallel I/O, and a floppy disk controller.

On board is a Z80A CPU which operates at 4 MHz for high-speed, efficient processing of information. The Z80A provides the capability to support many sophisticated applications. The interrupt structure of the Z80A is particularly important for systems which perform multiple tasks concurrently. The SYSTEMASTER utilizes the structured interrupt system of the Z80A in all of its I/O capabilities.

The on-board memory of SYSTEMASTER can provide up to 8k bytes of storage in EPROM/ROM and 64k bytes of RAM. The standard SYSTEMASTER is set up for 2k bytes of EPROM (to be used for on-board initialization routines) and 64k bytes of RAM. Options are available allowing the RAM to be bank switched.

Providing two independent serial ports, the Z80A SIO provides RS232C-compatible serial ports which can be operated under interrupt control. Both serial ports include full handshaking for connection to external devices as a printer, CRT terminal, or MODEM.

Also on board is a counter-timer chip which provides software-settable clocks for both serial ports and a real time clock. The real time clock is used by the software to provide timekeeping functions. It normally functions under interrupt control requiring a minimum of overhead. This real time clock can be used by software for any time-related functions, such as time dating of files, a stop watch or timing loops for external operations.

The Z80A PIO provides two parallel ports. One of these two ports is bidirectional with 8 data and 4 handshake lines. Normally this port is configured as a printer output, but because it is under software control, it can be reconfigured by the user to be a device input or a truly bidirectional port. The second parallel port has 8 data lines available which can be set independently to be input or output lines.

Using the NEC 765AC FDC and Zilog Z80 DMA ICs, SYSTEMASTER provides single- and double-density data storage on both mini- and maxi-floppy disk drives providing capabilities which minimize the overhead burden on the CPU and software. Use of the DMA controller allows the CPU to be available at all times for interrupts, a very important feature when the board is used in a multi-user or real time enviroment.

Some additional capabilities are: single- and double-density data transfer under software control; performance of simultaneous seek operations on all drives connected to the system; IBM compatible formatting for ease of information exchange with controllers using similar operating system software; compatibility with both single- and double-sided drives; ANSI standard 50 pin disk drive connector; automatic reading of sequential sectors on a diskette; automatic reading of both tracks of a two-sided diskette; automatic error-checking detected via CRC; under software control, possible selection of sector size to be 128, 256, 512, or 1,024 bytes.

The floppy disk control section of SYSTEMASTER also incorporates a field proven phase-locked oscillator (PLO) which is used to stabilize the separated information and clock for precise data recovery.

A reset-jump circuit on SYSTEMASTER makes the CPU jump to the EPROM software on board whenever the system reset button is activated. This is useful for systems which do not have a front panel. For systems with a front panel, reset-jump will override the functions of the front panel. Also, incorporated as part of the reset-jump circuit, a power-on-clear function is included which automatically generates a reset when power is first applied.

SYSTEMASTER can be used as a cost effective stand-alone microcomputer board or as the basis for a high-performance multi-user multi-processing system.

II. SPECIFICATIONS

Central processor: Z80A CPU - 4 MHz operation.

Memory: 64k bytes dynamic RAM, bank selectable. Uses eight 64k x 1 devices, 200nS (or faster), 128 cycle refresh.

Serial: Z80A SIO - 2 RS-232C, independent operation. Speeds from 110 to 19200 baud.

Timer: Z80A CTC - 4 channels, 2 used for serial ports, 2 used for real-time clock.

Parallel: Z80A PIO - 1 bidirectional port with 4 handshake lines, 1 port with 8 independent input or output lines.

Floppy disk controller: NEC uPD 765AC, single- or double-density and single- or double-sided operation, mini- or maxi-drives, ANSI standard 50 pin connector, IBM compatible format.

DMA: Z80A DMA controller handles floppy disk transfers

Disk data transfer rates:

Single density	5-1/4" - 125k bits/sec	8" - 250k bits/sec
Double density	5-1/4" - 250k bits/sec	8" - 500k bits/sec

EPROM/ROM: 2716, 2732, 2764, 2316, 2332, 2364; up to 8k bytes total.

S-100 Bus: Bus pins used by the SYSTEMASTER are shown on the next page. Note the definition of pin 66 as the RFSH* signal from the Z80 CPU. Also note that PHANTOM* is an option and requires modification to the standard board.

Note: SYSTEMASTER does not provide 8080-type I/O addressing; only the lower 8 address lines contain the I/O address.

Dimensions: 5.05" x 10.0", excluding edge connector.

Power requirements: +8v @ 2.0 amp, +16v @ 50mA, -16v @ 50mA.

Workmanship conforms to the requirements of MIL-STD-454.

Forced air cooling is required.

S-100 BUS Connections

Pin #	Function	Pin #	Function
1	+8V	51	+8V
2	+16V	52	-16V
3	XRDY	53	GND
4		54	SLAVE CLR*
5		55	
6		56	
7		57	
8		58	sXTRQ*
9		59	
10		60	
11		61	
12	NMI*	62	
13		63	
14		64	
15		65	
16		66	RFSH*
17		67	PHANTOM* (optional)
18	SDSB*	68	MWRT
19	CDSB*	69	
20	GND	70	GND
21		71	
22	ADSB*	72	RDY
23	DODSB*	73	INT*
24	Ø	74	HOLD*
25	pSTVAL*	75	RESET*
26	pHLDA	76	pSYNC
27		77	pWR*
28		78	pDBIN
29	A5	79	A0
30	A4	80	A1
31	A3	81	A2
32	A15	82	A6
33	A12	83	A7
34	A9	84	A8
35	DO1	85	A13
36	DO0	86	A14
37	A10	87	A11
38	DO4	88	DO2
39	DO5	89	DO3
40	DO6	90	DO7
41	DI2	91	DI4
42	DI3	92	DI5
43	DI7	93	DI6
44	sM1	94	DI1
45	sOUT	95	DI0
46	sINP	96	sINP
47	sMEMR	97	sWO*
48	sHLTA	98	
49	CLOCK	99	POC*
50	GND	100	GND

III. INSTALLATION

Upon receipt of SYSTEMASTER, check the shipping package for signs of abuse which may indicate possible damage. Check the board physically to look for any parts which may have been damaged during shipping. If any diskettes were shipped with SYSTEMASTER, check the diskettes for signs of damage which might be any bending or signs of a sharp object placed against the diskettes. Diskettes are quite fragile and any warping of the surface of the diskette will render it inoperative. Notify the shipper of any damage.

SYSTEMASTER is ready for immediate use upon receipt. It requires only that the peripherals which will be used with it be connected to the appropriate female connector which will then plug into the headers along the top of the board. For the particular connections required, see the section entitled "Peripheral Connections".

SYSTEMASTER need only be plugged into a standard S-100 bus for power and it will be functional, able to utilize the peripherals connected to it with the memory on board. The SYSTEMASTER needs to be in a well ventilated area due to the high density of IC's on board. Ideally, the board should be mounted vertically in a stream of air which will be moving across the face of the board. Whatever the mounting position, forced-air cooling is mandatory. Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable, as this may cause the cable to separate from its crimp connection causing intermittent problems.

For serial console devices, SIO B is the primary port. With the standard software, SIO B can determine the baud rate of a carriage return and thus set the appropriate speed automatically after a reset. The serial speed must be a standard value between 110 and 19200 baud. Note: Up to eight carraige returns are required for a terminal operating at 110 baud. Also, SIO B requires the handshake lines of the RS-232-C interface before it will function. See "Serial Ports" for further information.

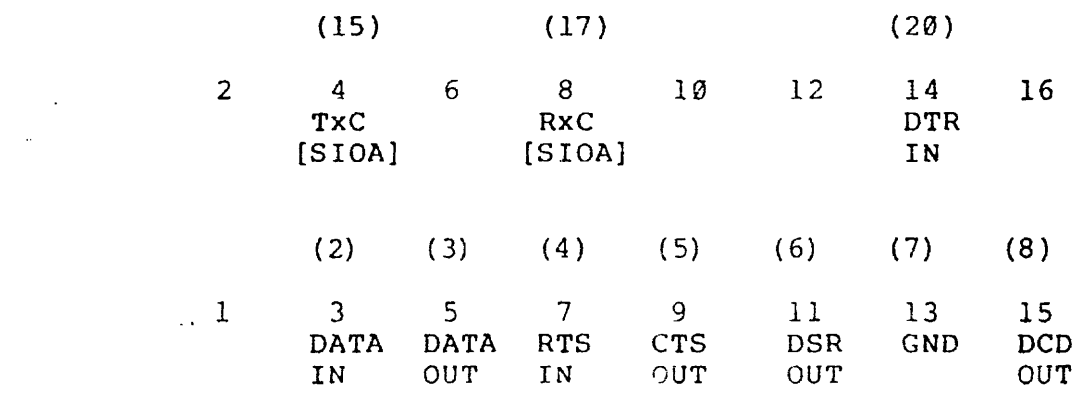
Once the system has been brought up the console port speed may, as an option, be statically set to allow the system to boot fully on RESET. This can be done by running the utility CONSYS.COM on the system disk.

Some versions of SYSTEMASTER, upon request, do not have RAM on board. If no RAM is provided, it must be supplied by the user before the SYSTEMASTER will function. Care must be exercised in choosing the right RAM device for use on the board. See the SYSTEMASTER specifications for further information.

3.1 Peripheral Connections

Serial Ports

SIO A and SIO-B



EIA pins are shown in parentheses.

These are the connections going into channels A and B of the SIO chip. In this configuration, each channel appears as a data communication device and will connect to a terminal or a printer.

IN and OUT refer to data direction with respect to the SYSTEMASTER. Data from an external device is IN to SYSTEMASTER, and data to an external device is OUT.

The signals TxC and RxC are clock inputs for synchronous communications. They are provided on serial port A only. If these inputs are to be used then jumper E22 to E23, and E25 to E26. These modifications connect the clock inputs of the SIO to the externally supplied clock on the EIA connector.

CTS (Clear To Send) and DSR (Data Set Ready) are outputs to the external device and are at +12V when the SIO channel is ready to function. RTS (Request To Send) and DTR (Data Terminal Ready) are inputs which must be at +12V for the SIO channel to function if the Auto Enables option is activated through software. This option is normally enabled in the standard SYSTEMASTER software.

Either channel can be crimp-connected to a 25-pin RS-232 connector by aligning pin 1 of the cable from the SYSTEMASTER connector with pin 1 of the 25 pin RS-232 connector. In this configuration, the channel connects directly to a terminal or printer.

NOTE: If the terminal or printer does not provide the necessary handshake lines, EIA pins 4, 5, and 20 should be jumpered together. This ensures that the required handshake signals to the SIO port are provided. The connections can be made on the serial cable or at the SIO connector on the SYSTEMASTER. At the SIO connector this requires that pins7, 9, and 14 be jumpered.

An alternative to providing a hardware handshake is to disable the "Auto Enables Option" on the SIO. This can be accomplished by altering the initialization software.

EIA Serial Data Transfer Protocol

Prior to sending or receiving data, the four handshake lines should be active. However, the SIO will allow control of its receive and transmit functions independently. If the "Auto Enables" function of the SIO channel is enabled (standard), the SIO will not send data until DTR is active. (This function is labelled "CTS" on the SIO chip.) This is handy for buffered printers which need to stop receiving data until the buffer is printed. By pulling DTR inactive, the printer will stop the flow of data from the SIO. When it is ready to receive more data, it reactivates DTR. Similarly, if "Auto Enables" is enabled, the SIO will not accept information until RTS is active. (This function is labelled "DCD" on the SIO chip.) This is primarily used with a communications link where, if signal conditions deteriorate, the data may be garbled.

In summary, the handshake lines provide a convenient means of controlling the flow of information in a serial channel. If any line is pulled inactive, transfer ceases.

RS-232-C Voltage Levels

A logic high (a binary ONE), or marking condition, is any voltage less than -3 volts to a minimum of -25 volts. A logic low (a binary ZERO), or spacing condition, is any voltage greater than +3 volts to a maximum of +25 volts. Any level between -3 and +3 volts is undefined. This is called the transition region. The maximum transition time between bit cells is four per cent of the basic clock period. The maximum voltage rate of change (slew rate) is 30 volts/uSec. Thus the maximum RS-232-C transmission speed, based on voltage swings of -12 to +12 volts, is 50,000 baud.

Serial Data Timing

Prior to transmitting data the signal line is held high, or marking. It goes low (spacing) to indicate the start of a character. The bits representing the character are then sent Least Significant Bit first, then a parity bit (if used), and finally 2 stop bits. The stop bits indicate the end of the character and are always logic ONEs. The standard SYSTEMASTER is set up for 8 data bits, no parity, and 2 stop bits.

The value of each character bit is held for the entire length of each bit cell. The length in time of each bit cell is the basic clock period, equal to the reciprocal of the baud rate. Thus for 9600 baud, each bit cell is 104 uSec long (.0001041 Sec=1/9600).

MODEM Connections

If connection to a MODEM is desired then the following connections must be made:

SYSTEMASTER Pin #	EIA Pin #	Direction	Function
5	2	OUT	Data to MODEM
3	3	IN	Data to SYSTEMASTER
11	4	OUT	RTS (Request To Send)
14	5	IN	CTS (Clear To Send)
7	6	IN	DSR (Data Set Ready)
13	7	--	Signal Ground
9	20	OUT	DTR (Data Terminal Ready)

IN refers to data sent to SYSTEMASTER, and OUT refers to data sent to the MODEM.

Parallel Ports

PIO A

2	4	6	8	10	12	14	16
RESET*		+5	GND	B STB	B RDY	A STB	A RDY
1	3	5	7	9	11	13	15
D7	D6	D5	D4	D3	D2	D1	DØ

PIO B

2	4	6	8	10
GND		D1	D2	DØ
1	3	5	7	9
D3	D4	D7	D6	D5

These are the connections into the PIO chip. The PIO chip has two parallel ports, A and B. As configured, PIO A may be used as an input, output, bidirectional or control port with four handshake lines. PIO B is the same except that it does not have bidirectional capabilties or handshake lines.

The signals are:

DØ - D7	8 data lines
A STB	Strobe input pulse from a device. Depending on the mode of operation, it means: 1. Output mode: Positive edge of this strobe is issued by the device to acknowledge the receipt of data made available by PIO A. 2. Input mode: The strobe is issued by the device to load data from the device into PIO A. 3. Bidirectional mode: Same as 1, except output data are present only while A STB is low. 4. Control mode: The strobe is inhibited internally.
A RDY	Ready output to a device. Depending on the mode of operation, it means: 1. Output mode: Indicates that the data bus is stable for transfer to the device. 2. Input mode: When active, it indicates that PIO A is ready to accept data from the device. 3. Bidirectional mode: Same as 1. 4. Control mode: Always in a low state.

RESET* The active-low reset line on the SYSTEMASTER. This can be used to reset a hard disk connected to PIO A.

B STB Used when PIO A is in the bidirectional mode; strobes data from the device into PIO A.

B RDY Used when PIO A is in the bidirectional mode; it goes high to indicate that PIO A is ready for data from the device.

The software supplied by Teletek allows PIO A to be set up as an input port or an output port. PIO B is set up in the control mode with all eight data lines available individually as input or output lines.

Parallel Printer Connection

A Centronics type parallel printer may be connected to PIOA on the SYSTEMASTER board. The following table lists the pin connections required to make a cable that will interface this type of printer.

SYSTEMASTER		Printer	
Pin #	Function	Pin #	Function
1	D7	1	DATA STB*
15	DØ	2	D1
13	D1	3	D2
11	D2	4	D3
9	D3	5	D4
7	D4	6	D5
5	D5	7	D6
3	D6	8	D7
14	ASTB	1Ø	ACK*

NOTE: The SYSTEMASTER provides a software strobe to the printer using data bit 7 from PIOA. Therefore data bit 8 on the printer is not connected. On most printers this bit controls special print modes and should be jumpered to ground to enable normal printing. Also remember that there are no drivers on the PIO signal lines therefore the cable length must be kept short (less than five feet depending upon your printer termination).

Floppy Disk Drive

Ground Pin #	Signal Pin #	Input - I Output - O	Description
1	2	O	Above track 43
3	4	-	Not used
5	6	-	Not used
7	8	O	Above track 43
9	10	I	Dual sided
11	12	-	Not used
13	14	O	Head 1
15	16	-	Not used
17	18	O	Head load
19	20	I	Index
21	22	I	Ready
23	24	-	Not used
25	26	O	Drive select 0
27	28	O	Drive select 1
29	30	O	Drive select 2
31	32	O	Drive select 3
33	34	O	Direction
35	36	O	Step pulse
37	38	O	Write data
39	40	O	Write gate
41	42	I	Track 00
43	44	I	Write protected
45	46	I	Read data, composite
47	48	-	Not used
49	50	O	Motor control

Input/Output are referenced to SYSTEMASTER. Input is a signal from the disk drive to SYSTEMASTER, and output is a signal to the disk drive.

More detailed information regarding floppy disk drive interfacing is available in appendix B. Please refer to that section of the manual when installing disk drives on the SYSTEMASTER.

3.2 Options

Write Compensation

To help compensate for the shifting of data bits during the read process of the floppy disk drive, the write data bits are compensated. This is particularly critical for double-density operation. Different drives require different amounts of write compensation. The symptoms of too much or not enough write compensation are as follows: 1. Too much write compensation shows up as read errors (usually CRC) in the outer tracks (Ø-42); 2. Not enough write compensation shows up as read errors in the inner tracks (43-76).

SYSTEMASTER provides selectable compensation for both 5 1/4" and 8" drives in the following combinations:

Jumper			Compensation	
PØ	P1	P2	5 1/4"	8"
1	1	1	None	None
Ø	1	1	None	125 nSec
1	Ø	1	None	250 nSec
Ø	Ø	1	250 nSec	125 nSec
1	1	Ø	250 nSec	250 nSec
Ø	1	Ø	500 nSec	125 nSec
1	Ø	Ø	500 nSec	250 nSec
Ø	Ø	Ø	Illegal, no write data output	

A 1 indicates the jumper is in place, while a Ø indicates the option pins are open.

Compensation is automatically switched as the on-board drive size control is switched from 5 1/4" to 8" drives.

Compensation depends on the recommendations of the drive manufacturer. Both 5 1/4" and 8" drives usually require 250 nSec compensation.

Track 43 Selectable Compensation

In addition to the above options, SYSTEMASTER provides one more: if the P3 jumper is in place, the compensation for tracks Ø-42 will be one step less than that in the above table. At track 43 and higher, write compensation will be equal to the table value. This option is provided because most drives require more compensation on the inner tracks where the recording density is higher. For 5 1/4" drives which do not have more than 42 tracks, select compensation one step greater than that required.

For example, assume an 8" drive which requires 250 nSec compensation, and a 5 1/4" drive with 40 tracks which requires 250 nSec compensation. Option jumper P3 is in place:

Select P0=1, P1=0, P2=0

At Tracks 0-42, 5 1/4" compensation is 250 nSec, and 8" compensation is 125 nSec. For tracks 43 and above, the 8" drive will have 250 nSec compensated data.

Extended Head Load

The uPD-765AC floppy disk controller has a maximum head unload time of 240 mSec. In some applications this will cause an undue amount of head loading and unloading. To increase this head unload time and reduce the number of head load actions, a 74LS123 monostable can be wired into the head drive circuit. With the addition of a 6 volt capacitor, the head unload time is extended. This increases the life of the media and the heads where there would normally be a great deal of head load activity. The following table gives the effective head load time for several different capacitor values:

Capacitor (uF)	Head Load Time (sec)
10	0.5
30	1.4
50	2.3
70	3.2
90	4.1
110	5.0
130	5.9
150	6.8
170	7.7
190	8.6
210	9.5
230	10.4
250	11.3

The time values are approximate (normally resistor values are $\pm$ 10% and capacitor values $\pm$ 20%) and are derived from the following equation:

HLT = (45 * C)/(1E03), where C is in microFarads.

To enable the head load option, jumper option pin E-19 to E-20 and install the desired capacitor value at location C-12. If this option is not desired then pin E-19 should be connected to E-18.

Wait State Generator

The wait-state generator can generate a wait-state during all memory accesses, M1 accesses, or only when the on-board ROM is accessed. The choice of wait-state generation is dictated by the requirements of the system. For the standard SYSTEMASTER, one wait state is generated for every access to the on-board ROM. With a faster ROM (less than 360 nSec access time), the wait state is not needed. The following wait-state options are available:

Option	Jumper
No wait state	E1 open
On-board ROM only	E1 to E4
All memory	E1 to E3
All memory, M1 only	E1 to E2

NOTE: if the RDY or XRDY input of the S-100 bus is low, this will be gated into the CPU wait input causing the CPU to wait until RDY and XRDY are released to an inactive high state.

CAUTION: An extended wait state will cause a loss of refresh to the dynamic RAMs on the SYSTEMASTER.

CTC Timing

The trigger inputs to CTC channels 0 through 2 connect to a 1.2288 MHz source. Thus all standard baud rates from 150 to 76,800 can be generated by programming the CTC for the counter mode, with a time constant between 1 and 256 (0). The SIO divider is set for 16 or 32 as necessary. For baud rates that are non-standard or below 150, use the CTC in the timer mode with a divide by 16 prescaler, and the SIO divider set for 16 or 32.

To summarize:

Baud rate 300 to 76,800- SIO divider set to 16, CTC in the counter mode, time constant set from 1 to 256.

Baud rate 150- SIO divider set to 32, CTC in the counter mode, time constant set to 256.

Baud rates less than 150:

(CTC in the timer mode, prescaler set to 16)

Baud Rate	SIO divider	Time Constant	Error
45	32	174	0.22%
60	32	130	0.16%
75	16	208	0.16%
110	16	142	0.04%

Real Time Clock

Channels 2 and 3 of the CTC are chained together to provide a 1-second interrupt real-time clock. Channel 2 is programmed in the timer mode, pre-scaler set to 256, and time constant set to 125. Channel 3 is set to the counter mode, time constant set to 125, and interrupt enabled. For a multi-user operating system which requires a fast clock interrupt, enable the interrupt for channel 2 also. The interrupt routine for channel 2 can count down to provide periods which are integral multiples of the 8 millisecond interrupt.

The standard system software stores the time and date in system RAM in six consecutive bytes: SEC,MIN,HOUR,YEAR,DAY, and MONTH. The CPU is interrupted every second and the time is updated. The date is also updated if necessary, but leap years and turn of the century occurances are not accounted for. All of the values are kept in binary.

The user may set or read the time and date by accessing these six bytes of data. The following code in a user program will return the address of SEC in the HL register:

```
LD   C,12       ;select function 12
CALL 40H        ;call BIOS function handler
```

Note that the clock is not initialized on reset. It is up to the user's software to set the time and date, and until they are set they should be considered invalid.

EPROM/RAM Options

The on-board ROM socket (U41) can accommodate 24 or 28-pin EPROMs or ROMs occupying 2k, 4k, or 8k bytes of memory space. This ROM can originate at 0000H, E000H, F000H, or F800H depending on the setting of the option jumpers on LA-5:

ROM Memory Space Options

ROM	Origin	End	Space	Jumpers
2316,2716	0000H	07FFH	2k	E14 to E16, E15 to E17
2332,2732	0000H	0FFFH	4k	E14 to E16, G to E17
2364,2764	0000H	1FFFH	8k	G to E16, G to E17
2316,2716	F800H	FFFFH	2k	E14 to E16, E15 to E17
2332,2732	F000H	FFFFH	4k	E14 to E16, E13 to E17
2364,2764	E000H	FFFFH	8k	E13 to E16, E13 to E17

The type of ROM used determines the socket and jumpers used at the socket:

ROM	Size	Socket	Jumpers
2316	2k	24 pin	E5 to E8, E6 to E1Ø, E7 to E12
2332	4k	24	E5 to E11, E6 to E1Ø, E7 to E12
2364	8k	24	E5 to E9, E6 to E12, E7 to E11
2716	2k	24	E5 to E8, E6 to E1Ø, E7 to E12
2732	4k	24	E5 to E11 E6 to E1Ø, E7 to E12
2764	8k	28	E5 to E11, E6 to E1Ø, E7 to E12

The chip select options for the 2316 and 2332 must be specified as follows for the above jumper connections:

2316	Pin 18 active low
	Pin 2Ø active low
	Pin 21 active high
2332	Pin 18 active low
	Pin 2Ø active low

NOTE: when the 24-pin 2364 is used, underlying RAM cannot be written when the ROM is enabled.

Except for the 24-pin 2364, when the ROM is enabled, either during reset-jump or otherwise, the underlying RAM can be written to but not read. Memory other than that occupied by the ROM can be accessed normally. Thus on reset the ROM monitor could copy itself into RAM then disable the ROM and continue execution from RAM.

RAM Select

SYSTEMASTER contains 64k bytes of RAM. This RAM is partitioned into a fixed and a selectable block. The selectable block can be disabled allowing CPU access to additional external memory. The fixed block is always resident in the CPU memory space. This combination of fixed and selectable memory accommodates such multi-user operating systems as MP/M from Digital Research, which requires a fixed block of RAM for the operating system.

The size of the fixed block of RAM can be varied by option jumpers AJ-1, 2, and 3:

Fixed Block Size	Range	Jumpers	
32k	8000H-FFFFH	AJ-1	Open
		AJ-2	Open
		AJ-3	Open
16k	C000H-FFFFH	AJ-1	Open
		AJ-2	Open
		AJ-3	Connected
8k	E000H-FFFFH	AJ-1	Open
		AJ-2	Connected
		AJ-3	Connected
4k	F000H-FFFFH	AJ-1	Connected
		AJ-2	Connected
		AJ-3	Connected

The selectable block of RAM occupies the memory space from 0000H up to the fixed block of RAM. The selectable block is enabled when /RAMEN islow. (/RAMEN is bit 7 of the control register.) When disabled, the selectable block of RAM is not affected by memory accesses in its memory space.

NOTE: The on-board RAM cannot be accessed by off-board temporary bus masters.

IV. THEORY OF OPERATION

SYSTEMASTER is a single-board computer for the S-100 bus. It contains 2k- 8k bytes of ROM, 64k bytes of RAM, a flexible-disk controller, two parallel ports, two serial ports, a DMA controller, a CTC, and a CPU. With appropriate software, SYSTEMASTER comprises a complete stand-alone single-user computer. The following discussion details the operation of the various functional areas of SYSTEMASTER. Please refer to Appendix A for the board layout and schematics when reading the following information.

Central Processor Operations

The heart of SYSTEMASTER is a 4 MHz Z80A CPU. It provides the intelligence to operate the on-board support chips and to provide the information interchange to the S-100 bus. Connections to the bus are made through tri-state buffers and control logic to provide the correct timing signals and status signals to operate other boards within the microcomputer.

The 4MHz clock for the CPU is derived from a 16MHz oscillator (U16) and a counter IC (U39). This circuit also provides clock signals to the disk controller section and a 2MHz signal for the S-100 bus.

The SYSTEMASTER CPU is configured in interrupt mode 2. In this mode, a requesting device generates an interrupt and when that interrupt is acknowledged, the CPU expects the device to place an 8 bit address vector on the data lines. The CPU then adds this 8 bit vector with another 8 bit register internal to the CPU to form a 16 bit absolute memory address. This address points to a 2 byte location in memory which contains the absolute address of the desired subroutine to service the interrupt.

In the case of the Z80A DMA, SIO, PIO and CTC, the necessary interrupt vectors are loaded to internal registers during initialization. For the case of the floppy controller IC, the interrupt vector is simply composed of that vector formed by the pull-up resistors on the data lines, an FE. The Z80 support IC's normally begin on an even memory location because bit 0 is always low during their interrupt response.

When a device external to the CPU requests an interrupt, the external device must provide an interrupt vector on the data bus when interrupt acknowledge status line goes active high. The Z80A support IC's are series connected to provide priority interrupts. The last device in the chain, namely the PIO, provides an interrupt enable signal for external devices. When this line is high, interrupts are enabled for external requests. When this line is low, external devices must be prevented from generating a response to an interrupt acknowledge signal. The vector that external devices place on the bus, when combined with the internal high order vector of the CPU, must point to a location in memory which provides the absolute address of the subroutine used for servicing that particular interrupt. Following is the on board interrupt daisy chain in order of priority:

1. DMA
2. SIO
3. CTC
4. PIO

DMA Controller

SYSTEMASTER incorporates a DMA controller to provide efficient, transparent flexible-disk data transfer without requiring CPU intervention. Interrupts can be enabled during DMA operations. Prior to a series of DMA data transfers the DMA controller must be set up as necessary for the particular operation desired. No CPU intervention is required during a DMA transfer process. At the completion of the series of data transfers the DMA controller will interrupt the CPU. At this time, the CPU performs any operations necessary to terminate the data transfer.

The sequence of operations should be: set up the DMA controller for the # of bytes to transfer (the sector size) and the starting memory address for the transfer, and finally send the read or write command to the 765. When the DMA controller interrupts the CPU at the end of the data transfer, the interrupt routine must immediately issue a terminal count to the 765 by doing an input from port 14H. The DMA controller accesses port 10H to transfer data to or from the 765. This port connects to the DACK (DMA acknowledge) pin of the 765.

The DMA controller is a single-channel device which can execute only one series of operations at a time. Although it is connected to the uPD765 flexible-disk controller, when the uPD765 is idle the DMA controller can perform block moves of data between memory and I/O devices. This is done by reprogramming the control registers of the DMA controller with the appropriate information and forcing the transfer through the use of a special software command.

Dynamic RAM Control

Logic Array LA-1 (U15) controls the access to the on-board dynamic RAM. A RAM cycle is started by M1* going low, or by MREQ* active low in conjunction with RD*, WR*, or RFSH*. If the RAM-select options match RAMEN* and the option address jumpers, MSTRT* goes low. Both sections of U-19, a dual J-K flip-flop, are clocked active by the action of MSTRT*. One section of U19 activates the RAS* line of the dynamic RAM ICs. RAS* clocks the lower 8 bits of the memory address into the RAM ICs. The second section of U19 sends a positive pulse into the delay line, U-47. The 20% tap of the delay line resets this section of U-19 to terminate the positive pulse, and in addition clocks one section of U-54. The output of U-54 causes the address multiplexers, U-42 and U-43, to select the upper 8 bits of the memory address.

When the positive pulse in the delay line reaches the 40% tap it clocks the remaining section of U-54, which generates a CAS* signal to complete the RAM access. After the RAM access time has elapsed, data lines are stable at the RAM outputs. When the positive pulse in the delay line reaches the 100% tap, the first section of U-19 is cleared which resets the RAS* signal. This allows the RAM RAS circuit to pre-charge in preparation for the next memory access.

As long as CAS* is low, the RAM outputs are stable. When the CPU terminates the memory request, LA-1 resets U-54 which returns the address multiplexers to the low-order address lines and resets the CAS* signal.

A memory write operation does not begin until WR* from the CPU is active. This ensures that the R/WR* line to the RAM ICs is active when the RAM ICs are accessed. This precaution allows the DATA IN and DATA OUT lines of the RAM ICs to be connected together, simplifying the memory circuitry.

A refresh operation begins when RFSH* and MREQ* from the CPU are both active low. A normal memory cycle is started, but the address multiplexer and CAS* circuits are held idle. The CPU outputs a refresh address during this time to refresh one of 128 consecutive locations in the RAM necessary to retain data. Because the CPU supplies the refresh address the only RAM devices that can be used are those that are compatible with a 128 cycle refresh.

NOTE: An extended RESET* or Wait State condition will cause a loss of refresh in the on board dynamic RAM.

Wait State Generator

The wait-state generator functions by holding the CPU wait input low until one clock cycle after MREQ* from the CPU is active. U-53, a J-K flip-flop, has its "K" input connected to MREQ* from the CPU. The inverted state of MREQ* connects to the "J" input. Initially, prior to a memory cycle, MREQ* is high causing U-53 to clock its "Q" output low. The "Q" output of U53 is gated with the desired condition (active M1*, ROM*, or all memory accesses). The resulting signal is gated with MREQ* and connected to the wait input of the CPU.

If the current CPU cycle meets the desired conditions the wait input of the CPU is held low. On the next negative edge of the CPU clock, because MREQ* is low and the "J" input of U-53 is now high, the "Q" output of U-53 will go high. This in turn releases the wait input of the CPU allowing completion of the cycle. U-53 resets itself at the end of the memory cycle when MREQ* again goes inactive.

ROM-I/O Decoder

U-26, a logic array (LA-5), provides the logic necessary to access the on-board ROM, select I/O, and control the RAM data buffer. When the CPU accesses memory, LA-5 decodes the address and option lines to determine if the on-board ROM is being accessed. If the CPU is accessing ROM, the RAM data buffer is held inactive, otherwise it is enabled if LA-1 has determined that on-board memory is to be accessed.

During an I/O operation, if the CPU address is less than 20H, the on-board I/O decoder is selected. If M1* is active at the same time as IORQ*, an interrupt acknowledge cycle is in process and neither ROM, RAM nor I/O is selected.

On-board Control Register

U-13, an octal D-type flip-flop, provides control for several areas of SYSTEMASTER. The output lines of U-13 are:

Bit	Name	Function
7	RAMEN*	When low, enables the selectable block of on-board RAM.
6	ROMEN*	With JMP*, controls the on-board ROM
5	JMP*	With ROMEN*, controls the on-board ROM
4	MOT*	When low, turns on the flexible-disk drive spindle motor
3	FL8*	When low, allows 8" flexible-disk data transfers. When high, 5 1/4" flexible-disk data transfers are enabled.
0-2	-	Not presently used

All these bits are reset low when a reset pulse occurs. The control register bits are set simultaneously by a CPU output to port 1CH. The outputs follow the inputs directly.

Reset-Jump

After a reset operation SYSTEMASTER begins execution of the instructions in the ROM to initialize the system. Because the ROM may reside at 0000H or a higher memory address, special circuitry enables the ROM independent of its actual location.

The outputs of U-13, the on-board control register, are cleared by a reset pulse. Therefore, outputs JMP* and ROMEN* are low. This combination causes LA-5, the ROM-I/O decoder, to enable the ROM for any CPU memory access. If the ROM options are set for a ROM location at E000H, F000H, or F800H, the first instruction in the ROM should be an absolute jump to the ROM location plus three. For example, a SYSTEMASTER set up for a 2716 has the ROM options set for an address of F800H. The first instruction in the ROM is a jump to F803H. This sets the CPU program counter to the actual ROM address space.

While JMP* and ROMEN* are both active RAM cannot be accessed. After the CPU begins executing the ROM in the correct address space, RAM can be enabled by setting JMP* high if the ROM occupies high address space (F000H or higher), or setting ROMEN* high if the ROM occupies memory starting at 0000H. If the RAMEN* signal is active low then both ROM and RAM can be accessed at this time. In order to disable ROM both signals JMP* and ROMEN* should be inactive.

NOTE: If ROM is addressed at 0000H, ROMEN* is high, and JMP* is low, then RAMEN* must be low to enable ROM.

To summarize:

RAMEN*	ROMEN*	JMP*	Result
X	0	0	ROM enabled, RAM disabled
0	0	1	F000 ROM enabled, RAM enabled
0	1	0	0000 ROM enabled, RAM enabled
0	1	1	ROM disabled, RAM enabled
1	0	1	F000 ROM enabled, RAM disabled
1	1	X	ROM and RAM disabled

(0 - low, 1 - high, X - don't care)

Parallel Ports

The parallel ports consist primarily of the Z80A PIO. Port A is used as an 8 bit input, output or bidirectional port. The four handshaking lines of the PIO are used with port A. Normally, port A is configured as an output for such parallel items as a printer. Under software control, port A can be configured as an input or as a bidirectional port where input data and output data as well as direction are controlled by the four handshaking lines.

Port B of the PIO is used in a bit control mode. This port is normally used to provide individual control lines for interfacing to parallel devices such as hard disk drives.

Serial Ports

The Z80A SIO is used to generate two entirely independent serial ports. Both serial ports incorporate all the handshaking lines required by an RS232C data interconnection device. Each channel of the SIO is driven by an independent section of the CTC. This means that baud rates for the two channels can be independently selected. In fact, the baud rates may range anywhere from 45 baud up to 19200 baud. These frequencies are determined during initialization of the CTC. The data lines to and from the SIO channels are buffered by RS-232-C level translators. These buffers are also inherently protected from short circuits on the external lines.

Both serial ports will interconnect with terminal equipment (printer, CRT terminal, etc) using standard insulation-displacement connectors. Connection to a MODEM requires transposition of all six serial lines as required by the MODEM (see "Peripheral Connections"). When connecting to a synchronous MODEM, which provides the receive and transmit clocks, the clock inputs to SIO A must be connected to the MODEM:

SIO A clocks	Jumper
Internal, CTC	E22 to E21, E25 to E24
From MODEM	E22 to E23, E25 to E26

The transmit and receive clocks for SIO A are provided by CTC channel 0. Those for SIO B are provided by CTC channel 1.

Floppy Disk Controller Operation

The heart of the flexible-disk controller is the NEC uPD765AC. Capable of single- and double-density, single- and double-sided 5 1/4" and 8" data recording, the 765 provides a flexible, reliable disk controller for SYSTEMASTER. Circuitry on board SYSTEMASTER supports the 765 in stabilizing the read data from the disk drive, compensating data written to the disk drive, and buffering status signals to and from the disk drive. The following discussion details the circuitry surrounding the 765.

To reduce the number of its pins the 765 multiplexes dual signals on four of its control lines. Pin 39 of the 765 selects the seek mode when high and the data read-write mode when low. One section of U-56, an inverting buffer, inverts the signal from pin 39 to enable the appropriate drivers when the 765 is in its seek mode. When in the seek mode, the 765 positions the disk drive head over the desired track on the diskette. In this mode, the 765 looks at the dual-sided and track Ø signals and outputs drive control signals to the direction and step lines. In the read-write mode, these four function lines become write-protect, write-fault, low-current (track greater than 42), and write-fault reset. The 765 also has two drive-select outputs. U-49, a dual decoder, decodes USØ and US1 from the 765 to develop four drive select signals.

The 765 generates an interrupt request to the CPU when it detects an error or completes an operation. The 765 interrupt output on pin 18 is active high, thus it is inverted by U-57 and activates the output of U-7, a tri-state buffer. U-7 pulls down the CPU interrupt request line. When the CPU acknowledges the interrupt, LA-4 will pull down data line Ø if no other interrupts are active on SYSTEMASTER. Because the other data lines to the CPU have resistor pull ups to +5 volts, the CPU sees FEH on its data bus and will execute the absolute address stored at FEH in the interrupt table. The data input buffer from the S-1ØØ bus is held inactive by LA-4 during the interrupt acknowledge operation when the 765 interrupt line is active.

The read data from the disk drive may vary in frequency due to disk drive rotation speed variations. To maintain reliable read data, a phase-locked loop oscillator follows the frequency of the read data and provides a stabilized read clock for the 765. The action of the phase-lock loop is such that the read data pulses will occur in the center of the high or low portion of the read data clock sent to the 765. This provides the maximum margin for error in disk read operations.

Disk Data Encoding

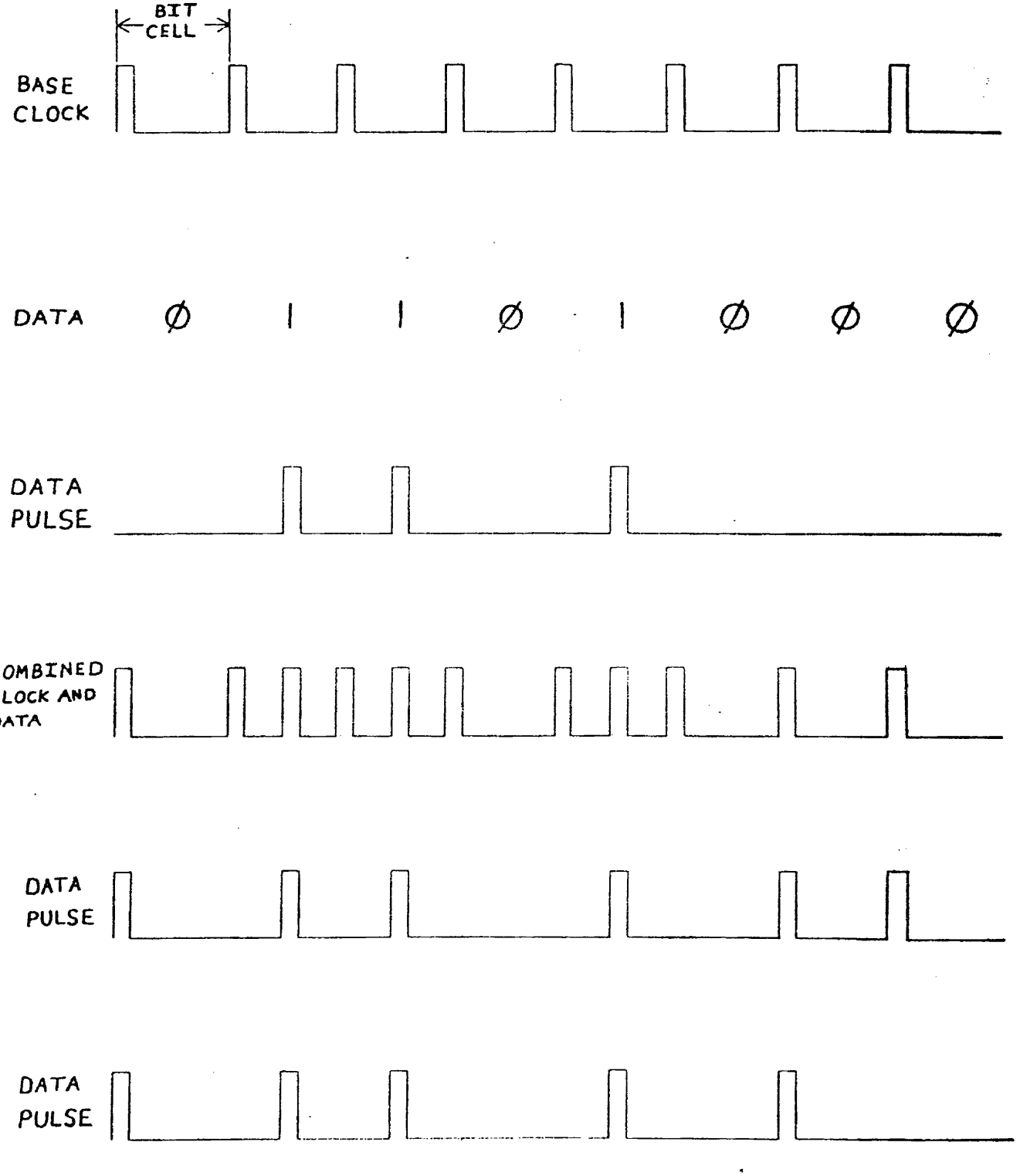
Physically, double density disk drives do not differ significantly from their single density counterparts. Improvements in double density record and playback heads and changes in mechanics often provide less expensive and more durable drives. These changes are minor compared to the differences in reading and writing functions. Figure 1 reviews encoding methods used in single and double density. The standard recording formats are FM (for frequency modulation), MFM (for modified frequency modulation-double density), and MMFM (for modified modified frequency modulation) which is a refinement of MFM. Line 1 of Figure 1 indicates the basic clock frequency which designates the bit cell in which information will be passed. The next line illustrates a sample of information; the line following shows the pulses which generate that information in a single- density FM format. Notice that information actually sent to and received from the drive is a combination of the basic clock frequency and data pulses. Refer to the next line which is MFM.

Here, only the data pulses will be sent to the drive and their orientation within the bit cell determines the value of that particular data pulse (a 1 or a Ø). Every Ø is represented by a data pulse that coincides with the basic clock frequency. Every 1 is represented by a pulse that occurs midway between two clock pulses. Thus, when the data pulse occurs in the middle of a bit cell, it is a 1; when it occurs in the beginning of a bit cell, it is a Ø. Look at the next line which represents MMFM.

This is a slight refinement of MFM; in this instance the data pulses once again represent 1's and Ø's via their placement within the bit cell. However, the rules change slightly. If the preceding data pulse was a Ø and the present datum is a Ø, then the data pulse will occur. If the last data pulse was a 1 and the present datum is a Ø, the present data pulse does not appear. If the last data pulse was a 1 and the present datum is a 1, that data pulse appears. Every time there is a 1, a data pulse will appear in the middle of a bit cell. But whether or not a Ø data pulse occurs depends on the preceding datum. Note that the density of data pulses for MFM is almost exactly one-half the density of data pulses for FM. Thus, for the same density of pulses on the diskette, MFM will record twice as much information as FM. MMFM has slightly less dense data pulses than MFM, but its complexity of encoding and decoding outweighs the slight advantage it might enjoy due to slightly less density.

The basic clock frequency for FM encoding is 250 KHz for an 8-inch diskette. When we delete the clock and leave only the data pulses in MFM, that clock rate changes to 500 KHz. The MFM data transfer rate is twice as fast as FM. The density and the speed are both doubled, which means that twice as much information can be stored in the same physical space and manipulated twice as fast.

FIGURE 1 FLOPPY DISK DATA ENCODING



S-100 Bus Interface

The signals generated by SYSTEMASTER are compatible with the proposed IEEE-696 standard. U-14, a logic array (LA-4) transforms the Z-80 family status signals to those of the S-100 bus. In addition, U-14 controls the data input bus driver, U-12, to prevent conflicts with on-board I/O and memory devices. If a conflict could occur, SYSTEMASTER ignores the off-board device.

SYSTEMASTER generates the S-100 standard memory write strobe by the logical equation: MWRT= pWR AND /SOUT.

In addition to the standard S-100 signals, SYSTEMASTER brings the Z-80 CPU refresh signal to pin 66 of the bus for those memory boards which need this signal.

U-5, a dual monostable, generates the pSYNC and pSTVAL* signals. Whenever the CPU activates a status line (M1, MREQ, or IORQ), U-14 outputs an active-low signal to trigger U-5A. The output of U-5A appears on the bus as pSYNC and also triggers U-5B. U-5B generates a pSTVAL* signal whose active edge occurs after status is valid, and during the pSYNC pulse.

Power-On Clear

SYSTEMASTER generates a reset pulse when power is applied to automatically initialize the system. Thus during the start-up operation operator intervention is not required. To develop the power-on reset pulse, circuitry on-board SYSTEMASTER detects the first application of power: Capacitor C-26 is initially discharged. C-26 holds the plus input of U-17 (a dual comparator) low, which causes the output of U-17 to be low. The output of U-17 enables two drivers of U-6, a hex inverting bus driver, which pull RESET* and SLAVE CLR* low on the S-100 bus. In addition, the output of U-17 is buffered by U-18 to drive POC* low. When C-26 charges above the level on the minus input pin of U-17, the output of U-17 goes high. RESET* and SLAVE CLR* are released and pulled high by resistors connected to +5 volts, and POC* goes high. At this time the CPU on board SYSTEMASTER begins execution of the instructions in the on-board ROM. When power is turned off, diode D-1 discharges C-26 quickly to provide a reset action if power is shortly reapplied. (Such a sequence can occur during a temporary power outage.)

SYSTEMASTER Port Assignments

Port	Device	Function
ØØH	SIO	A-Data
Ø1	"	A-Control
Ø2	"	B-Data
Ø3	"	B-Control
Ø4	PIO	A-Data
Ø5	"	A-Control
Ø6	"	B-Data
Ø7	"	B-Control
Ø8	CTC	Channel Ø, SIO-A baud rate
Ø9	"	Channel 1, SIO-B baud rate
ØA	"	Channel 2, Real-time clock
ØB	"	Channel 3, Real-time clock-connects to the output of Channel 2.
ØC	765	Status register
ØD	"	Data
ØE-ØF	"	Not used
1Ø	DACK	DMA acknowledge to 765
11-13	"	Not used
14	TC	Terminal count to 765
15-17	"	Not used
18	DMA	DMA processor control registers
19-1B	"	Not used
1C	CONT	On-board control register
1D-1F	"	Not used

V. IN CASE OF TROUBLE

If the SYSTEMASTER does not respond the first time it's connected, relax. Due to its complexity, there are many areas that may have inadvertently been overlooked. Take time to read the "Peripheral Connections" section. The following trouble-shooting guide lists the major functional areas of the SYSTEMASTER and some typical problems associated with each. Suggested solutions are offered for each. But remember: it is highly recommended that the entire manual be read.

TROUBLESHOOTING GUIDE

Once the SYSTEMASTER board has been plugged into your mainframe, a disk drive cable attached to the 50 pin connector on-board, and the system console cable connected, then the typical boot procedure should be as follows:

a) Insert the SYSTEMASTER CP/M disk supplied by Teletek into drive A: and RESET the system.

b) A disk access should take place.

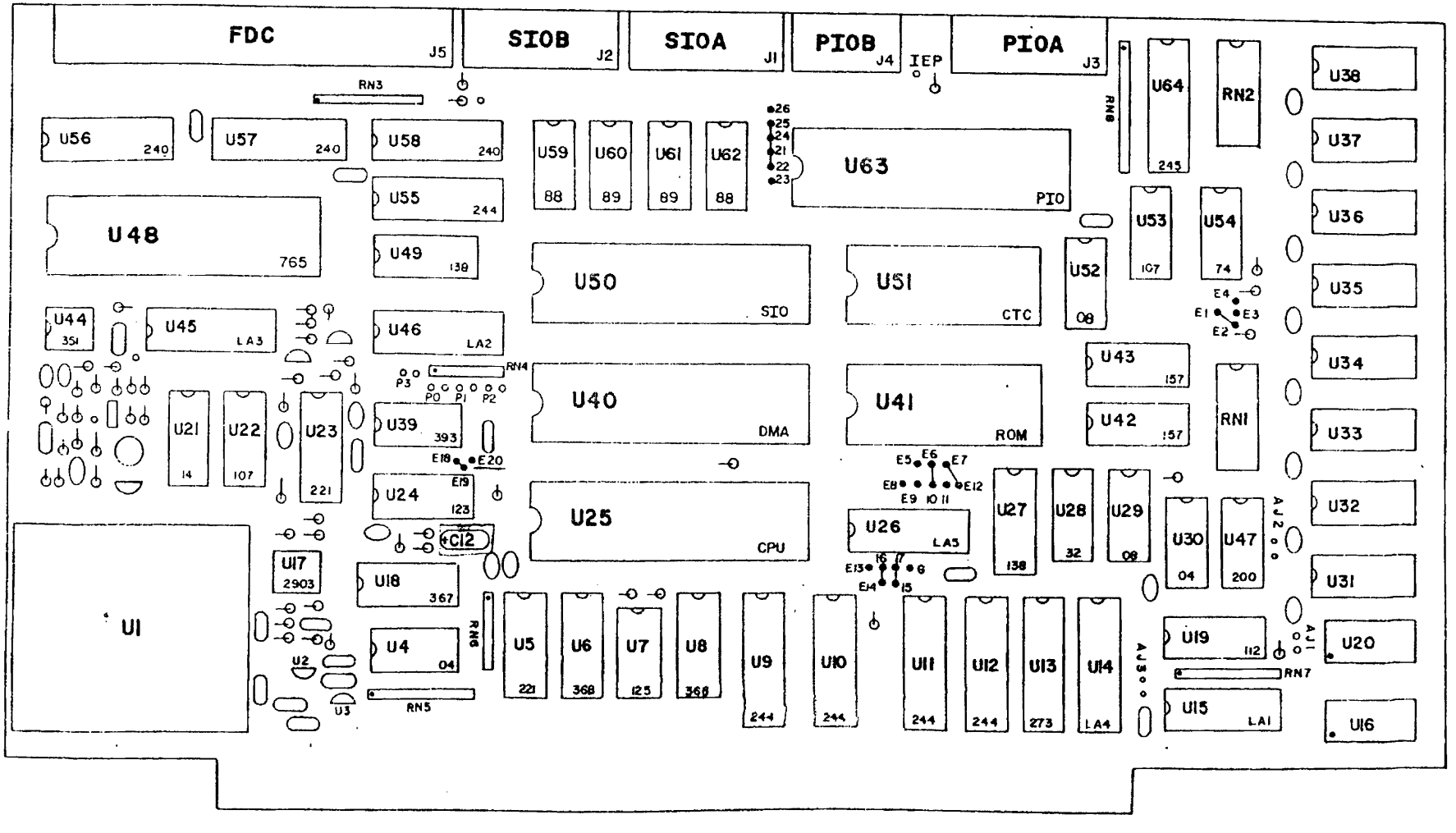
c) The system will then wait for you to enter a series of carraige returns (up to eight may be required) so that the baud rate of your console device can be determined. (This procedure can be bypassed by choosing the static option for SIOB when running the CONSYS.COM utility.)

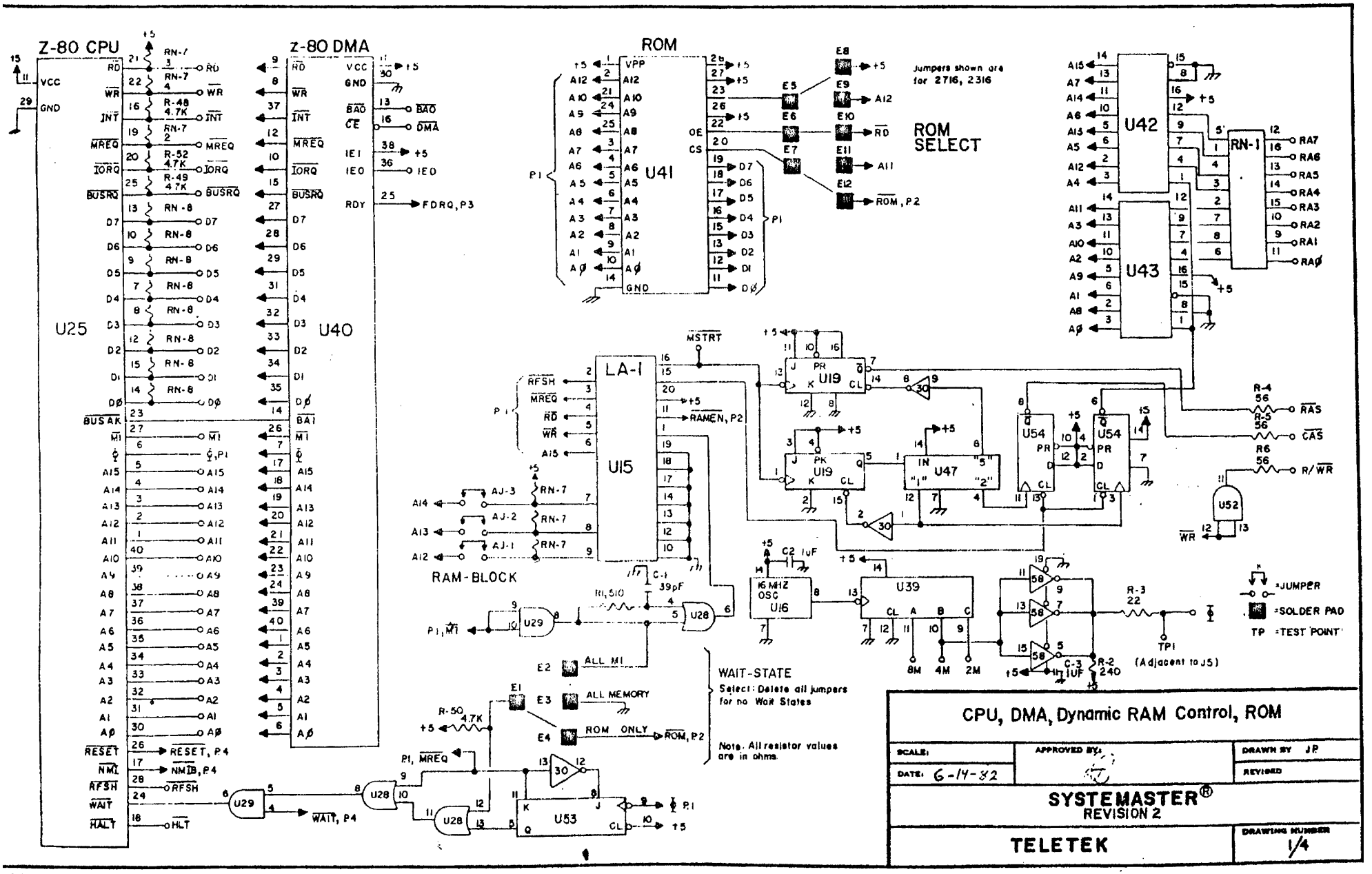
d) Once the console port speed has been successfully determined a sign-on message will appear on your console followed by a CP/M prompt.

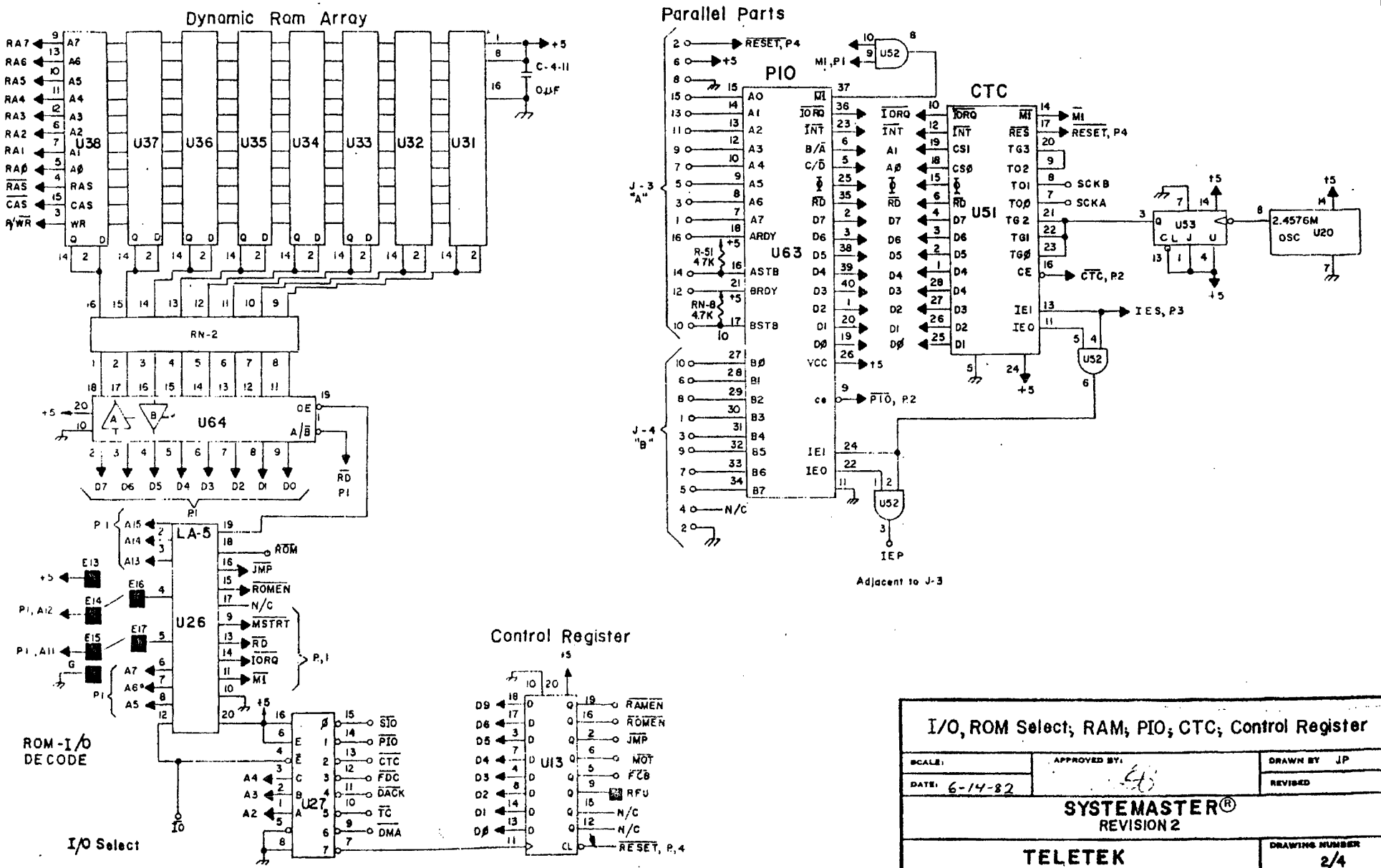
SYMPTOM	POSSIBLE CAUSES
There is no disk access on RESET.	1) Missing power and ground, check +5V supply. Make sure your mainframe provides ground on pins 20 and 70 of the S-100 bus. 2) Check that the 50-pin drive cable is connected correctly. 3) Verify that the drives are configured as recommended in the drive appendix of this manual.
Disk access occurs but nothing appears on the terminal upon entering many carraige returns.	1) Make sure the terminal is connected to SIOB, the port next to the disk drive cable. 2) Verify that the terminal cable is connected correctly and that the terminal provides hardware handshake. If not, then follow the suggestions given in the "Peripheral Connections" section for the serial ports. 3) Check the + and -12V supply.
List device does not function.	1) Verify that the BIOS has been configured correctly for your list device by running the CONSYS.COM utility. Make sure the correct protocols and port speeds are selected for your printer. Remember that the system must be rebooted before any changes that are made will take effect. 2) For a parallel printer verify the cable connection to PIOA (see "Peripheral Connections"). Also remember that the PIO is a MOS device and is not capable of driving long cables without adding an external driver adapter.
Board dies after a short period of operatioin.	1) Check the cooling ability of your mainframe. If the temperature of the +5V regulator is high enough it will shut down. Forced airflow across the face of the board is required. Also verify that the supply voltages are not more than are required by the S-100 standard. Any excess voltage will cause the regulator to operate at a higher temperature than is necessary.

TELETEK SYSTEMASTER®

Board Layout




Z-80 CPU
U25
Z-80 DMA
U40
ROM
U41
Jumpers shown are for 2716, 2316
ROM SELECT
U42
U43
RN-1
LA-1
U15
RAM-BLOCK
WAIT-STATE
Select: Delete all jumpers for no Wait States
Note. All resistor values are in ohms
16 MHZ OSC U16
U39
U47
U53
U54
U52
U19
U29
U28
=JUMPER
=SOLDER PAD
TP =TEST POINT
TP1 (Adjacent to J5)
CPU, DMA, Dynamic RAM Control, ROM
SCALE:
APPROVED BY:
DRAWN BY JP
DATE: 6-14-82
REVISED
SYSTEMASTER®
REVISION 2
TELETEK
DRAWING NUMBER
1/4



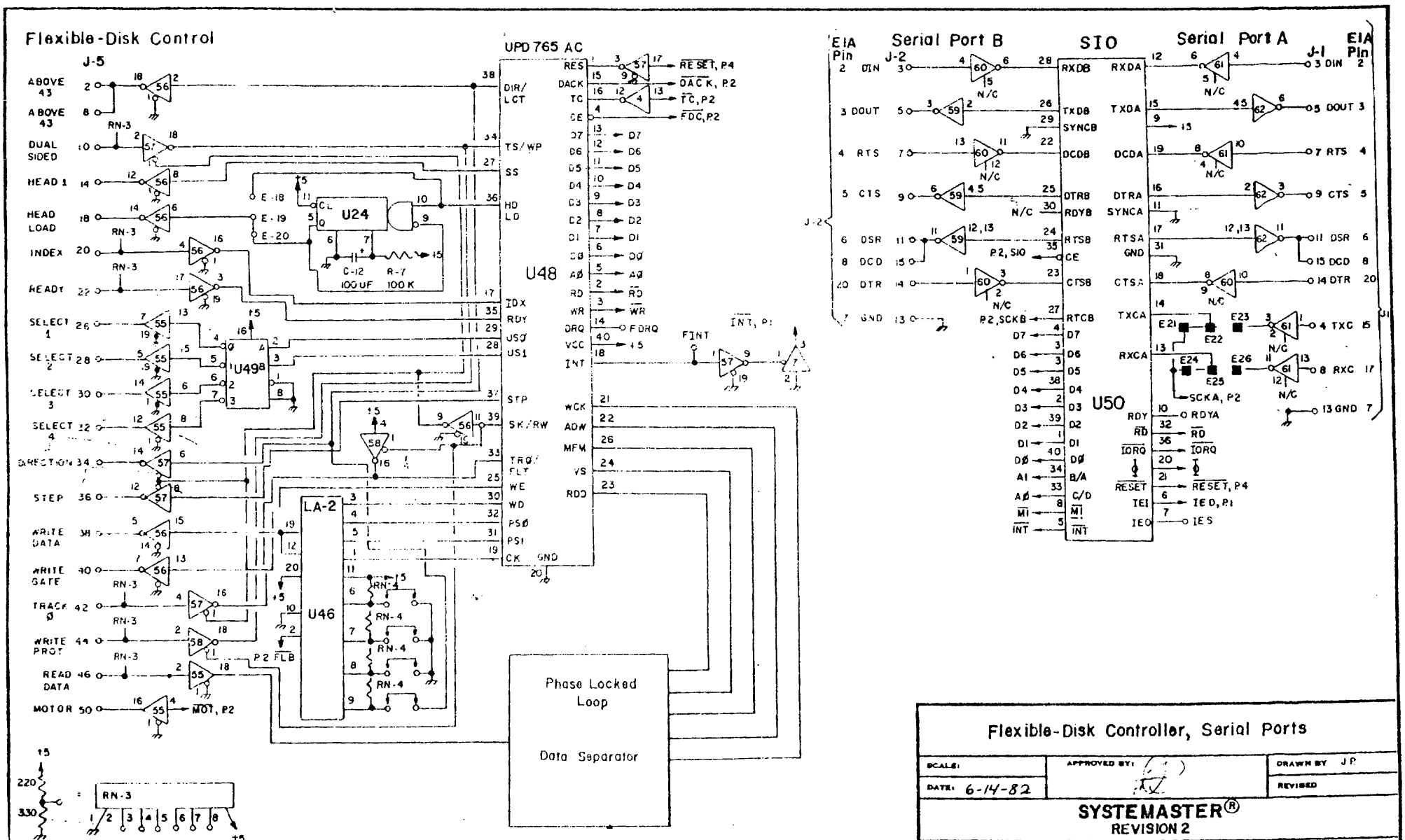
I/O, ROM Select; RAM; PIO; CTC; Control Register

SCALE:	APPROVED BY:	DRAWN BY JP
DATE: 6-14-82		REVISED

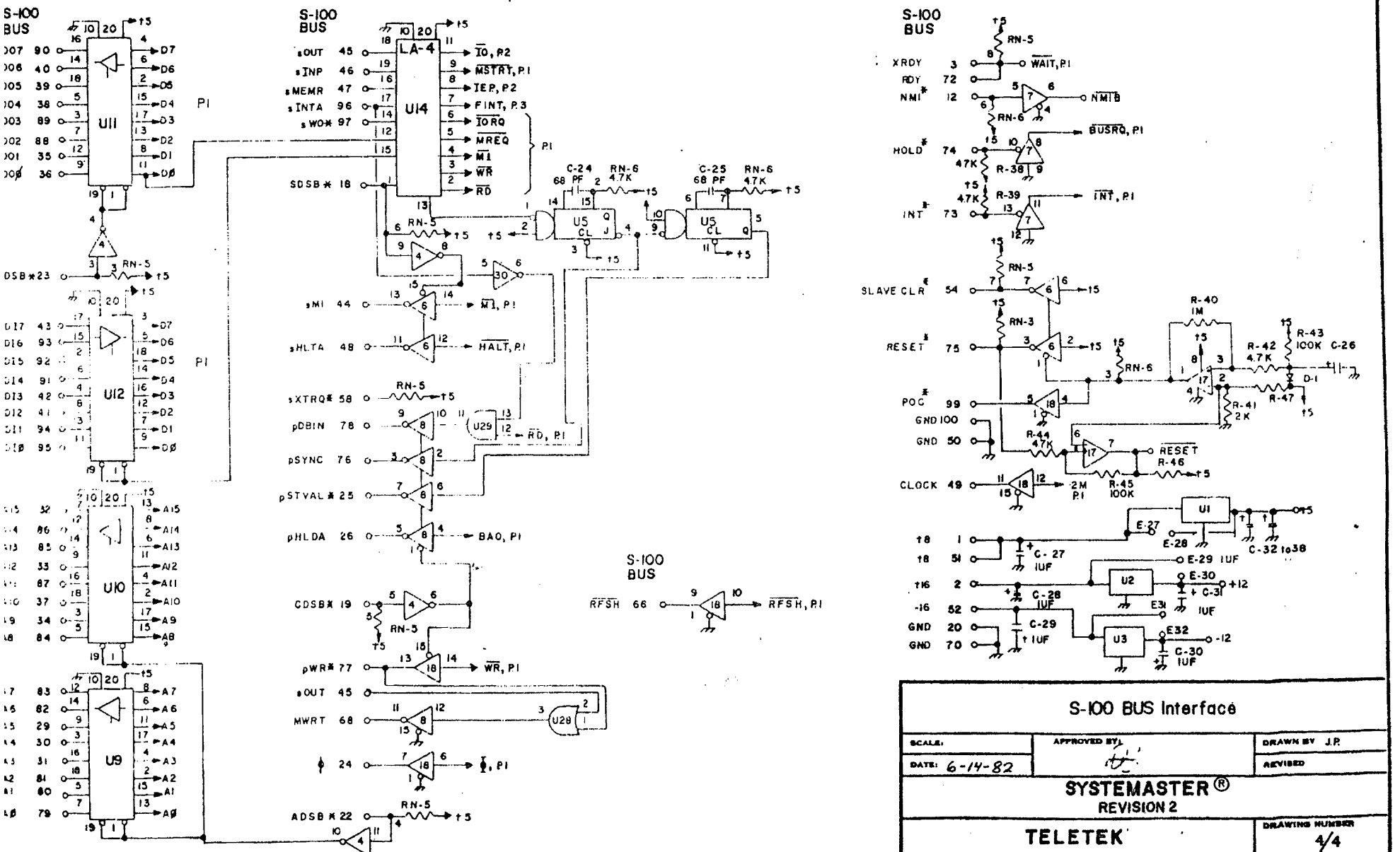
SYSTEMASTER® REVISION 2

TELETEK

DRAWING NUMBER 2/4



Flexible-Disk Controller, Serial Ports		
SCALE:	APPROVED BY:	DRAWN BY J.P.
DATE: 6-14-82		REVISED
SYSTEMASTER® REVISION 2		
TELETEK		DRAWING NUMBER 3/4



S-100 BUS Interface

SCALE:	APPROVED BY:	DRAWN BY J.P.
DATE: 6-14-82		REVISED

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DRAWING NUMBER 4/4

APPENDIX B

SYSTEMASTER DRIVE INTERFACING

In controlling a disk drive from SYSTEMASTER, proper connections must be made to the disk drive in order for it to be operational. The drive options must be configured as outlined in the appropriate manufacturer's section following this introduction. Particularly important is the fact that the uPD-765 continuously polls all drives in the system to keep track of their status. With some drives this will interfere with their seek function (positioning of the head). Thus, most drives will have a stepper motor enable option, or simultanious seek option, that powers the stepper motor continuously, rather than just when the drive is selected. If the drive won't read initially, check for this option.

Drive interfacing deals with the proper connection of functional signals and the satisfying of electrical and mechanical requirements.

To help ease the shock of transition from the interchanging of various disk drives to other host controllers, a standard known as ANSI was developed which standardized the means of intercommunication between disk drive and host controller by specifying power requirements and voltage levels, edge connector and cable specifications, and specific pin numbers of the connector to particular functional signals.

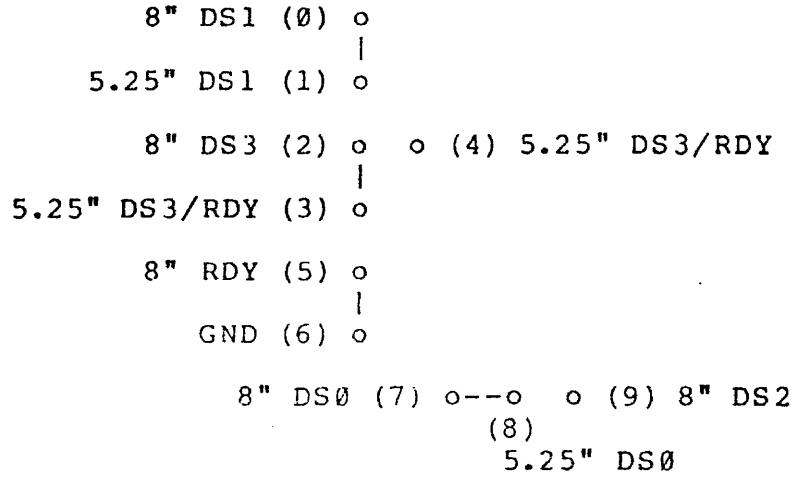
ANSI Standards

Functional signals assigned to specific pin numbers of the connector are shown on the next page for a 5.25-inch disk drive and an 8-inch disk drive.

Mini-Floppy Drives

Use of mini-floppy drives requires the use of a special 50 to 34 pin adapter board. The following is a diagram of this board and its options.

Eight inch to five and a quarter inch drive p.c. adaptor board:



Options:

1) Pad 0 to 1 - 8" drive select 1 connected to 5.25" drive select 1.

2) Pad 1 to 2 - 8" drive select 2 connected to 5.25" drive select 1.

3) Pad 2 to 3 - 8" drive select 3 connected to 5.25" pin 6. Normally this pin is drive select 3 for 5.25" drives but is the READY signal for Micropolis drives.

4) Pad 2 to 4 - 8" drive select 3 connected to 5.25" pin 34. This pin is drive select 3 for Micropolis drives or READY for Pertec drives.

5) Pad 5 to 3 - 8" READY connected to 5.25" pin 6. This pin is the READY pin for Micropolis drives.

6) Pad 5 to 6 - 8" READY connected to GROUND. Since most 5.25" drives do not provide a READY signal it is neccessary to ground this line.

7) Pad 7 to 8 - 8" drive select 0 connected to 5.25" drive select 0.

8) Pad 9 to 8 - 8" drive select 2 connected to 5.25" drive select 0.

Electrical

1. Multi Drop Bus: Multiple drives may be connected to the same host controller as shown in Figure 1. Only one drive is logically connected to the interface at a time.

2. Voltage Levels (as measured at the driver)

Logical true	Active low	+0V to +0.4V
Logical false	Active high	+2.4V to +5.5V

3. Termination: Signal lines shall be terminated by one of two resistive networks. Either the signal line will have a pull-up resistor of 150 ohms or it will have a pull-up resistor of 220 ohms in addition to a 330 ohm resistor connecting the signal to ground.

4. Signal Drivers: The signal drivers should have open collector output stages capable of sinking a minimum of 40mA at logical true (low) level, with maximum voltage of 0.4V as measured at the driver output.

5. Signal Receivers: The signal receivers should not unduly load the multi drop bus and should not require more than 40uA current from the driver at input high (2.4V) nor supply more than 1.6mA to a current sink at input low (0.4V) level.

Interconnecting Cable

Conductor Size

Copper- AWG #30 or larger for solid conductor
AWG #28 or larger for stranded conductor

Non-copper- Sufficient size as to yield a dc resistance not to exceed 110 Ohms per 1000 ft. per conductor.

Stray capacitance- Capacitance between one wire in a cable and all others in the cable with all others connected to ground shall not exceed 40pF/ft. and the value shall be reasonably uniform over the length of the cable.

Mutual pair capacitance- Capacitance between one wire of the pair to the other shall not exceed 20pF/ft. and the value should be reasonably uniform over the length of the cable.

ANSI Standard for 5.25 Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Not assigned (Head load)
4	3	In use control
6	5	Drive select 3 (Ready)
8	7	Index/sector
10	9	Drive select 0
12	11	Drive select 1
14	13	Drive select 2
16	15	Motor on
18	17	Direction select
20	19	Step
22	21	Composite write data
24	23	Write gate
26	25	Track 0
28	27	Write protected
30	29	Composite read data
32	31	Side one select
34	33	Disk change (Drive select 3)

ANSI Standard for 8-Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Head current switch
4	3	Not assigned
6	5	Not assigned
8	7	Drive busy
10	9	Two-sided
12	11	Disk change
14	13	Side one select
16	15	In use control
18	17	Head load
20	19	Index
22	21	Drive ready
24	23	Sector
26	25	Drive select 0
28	27	Drive select 1
30	29	Drive select 2
32	31	Drive select 3
34	33	Direction select
36	35	Step
38	37	Composite write data
40	39	Write gate
42	41	Track 0
44	43	Write protected
46	45	Composite read data
48	47	Separated read data
50	49	Separated read clock

Tandon TM100 Disk Drive

Required configuration:

1.	MX	Open
2.	HS	Jumper
3.	HM	Open
3.	NDS0-NDS3	Select appropriate drive address

Install the termination network 2F in the last drive only.

Eacn drive requires +12 volts at 0.9A and +5 volts at 0.6A.

Required Pre-write Compensation: none.

Snugart 850/851 Disk Drive

Required configuration:

(Shunts with * next to them are on shunt block at IC location 4E)

1.	X *	Shunt intact
2.	DC	Open
3.	D	Open
4.	C	Jumper
5.	I *	Shunt intact
6.	R *	Shunt intact
7.	S *	Shunt intact
8.	DS1-4	Select appropriate drive address
9.	HL *	Shunt open
10.	DS	Open
11.	RI } IN ETCH —	Trace intact
12.	RR }	Trace intact
13.	Y	Open
14.	Z *	Shunt intact
15.	850	Jumper
16.	851	Open
17.	A *	Shunt intact
18.	B *	Shunt open
19.	1B, 2B, 3B, 4B	Open
20.	2S	Jumper
21.	WP } IN ETCH	Trace intact
22.	NP }	Open
23.	S1	Open
24.	S2	Jumper
25.	S3	Open
26.	DL	Jumper
27.	M	Jumper
28.	TS	Open
29.	FS	~~Jumper~~ OPEN
30.	IWI	Jumper
31.	RS	Jumper
32.	RM	Open
33.	HLL	Open
34.	IT	Jumper
35.	HI	Open
36.	FM	Open
37.	~~MF~~ FM	Jumper
38.	~~MF~~ M²FM	Open
39.	~~Eo.~~ LOG	OPEN IC5E

WE SUGGEST BENDING THE PINS ON THE SHUNT BLOCK AT 4E TO OPEN THEM INSTEAD OF CUTTING THE SHUNT THROUGH.

Install the termination network ~~IC2F~~ in the last drive only.

Each drive requires +24 volts at 1.0A and +5 volts at 1.1A.

Required Pre-write Compensation: 250 ns.

Shugart 800/801 Disk Drive

Required drive configuration:

1.	X	Jumper
2.	DC	Open
3.	D	Open
4.	C	Jumper
5.	I	Trace intact
6.	R	Trace intact
7.	S	Trace intact
8.	DS1-4	Select appropriate drive address
9.	T1, 3, 4, 5, 6	Jumper on last drive in system
10.	T2	Jumper
11.	HL	Open
12.	DS	Open
13.	RI	Trace intact
14.	RR	Trace intact
15.	Y	Open
16.	Z	Jumper
17.	800	Jumper
18.	801	Open
19.	A	Jumper
20.	B	Open

Each drive requires 24 volts at 1.7A, +5 volts at 1.0A, and -5 volts at 0.07A. Note: Many power supplies for floppy drives do not have the required current capability for 2 or more Shugart drives.

Required Pre-write compensation: 250 ns.

Qume DT-8 Disk Drive

Required drive configuration:

1.	A	Jumper
2.	B	Open
3.	X	Jumper
4.	Z	Jumper
5.	HL	Open
6.	R	Jumper
7.	I	Jumper
8.	RI	Trace intact
9.	RR	Trace intact
10.	C	Jumper
11.	D	Open
12.	DC	Open
13.	2S	Jumper
14.	DS	Open
15.	Y	Open
16.	DL	Open
17.	WP	Trace intact
18.	NP	Open
19.	S2	Trace intact
20.	S1, S3	Open
21.	DS1-4	Select appropriate drive address
22.	B1, 2, 3, 4	Open

Install 2 resistor terminator modules into the last drive in the daisy chain.

Each drive requires 24 volts at 0.9A and 5 volts at 1.1A.

Required Pre-write Compensation: none.