AMD Geode™ CS5536 Companion Device Silicon Revision B1 Specification Update

1.0 Scope

This document discusses known issues of silicon revision B1 of the AMD Geode™ CS5536 companion device.

Table 1-1 provides a summary of the issues. A detailed description of each issue, its impact, and a recommended resolution/fix follow.

The silicon revision number, B1, is printed on the chip (top-side of PBGA in the seventh line of the part marking).

Software Readable IDs for Rev B1

- CS5536 Silicon Revision:
  — MSR 51700017h[7:0] = 03h
  — PCI Index 08h[15:0] = 03h
  — Test Controller Instruction 8FFFFAh = 03h

- Device (Module) Revisions:
  — GLIU: MSR 51010000h[7:0] = 01h
  — GLPCI_SB: MSR 51000000h[7:0] = 01h
  — ACC: MSR 51500000h[7:0] = 01h
  — ATAC: MSR 51300000h[7:0] = 01h
  — USBC: MSR 51200000h[7:0] = 02h
  — DD: MSR 51400000h[7:0] = 02h
  — GLCP: MSR 51700000h[7:0] = 01h

Note: This is revision D of the document. The change from revision C (also dated March 2006) is the document was made non confidential.

Table 1-1. Issue Summary

Issue#[1]	Description
1	PIT deviation from industry standard operation
2	Debug port hangs system if used
3	Incorrect operation of PIT count mode 3 value load
4	Restrictions on AEOI bit use in the PIC
5	DMA rotating mode does not rotate correctly
6	PMC Sleep_Clock control disable side effect
7	GLIU data compare cannot generate a hit
8	GLIU Error MSR unexpected address flag failure
9	8237 software DMA memory write from LPC fails
10	I/O cycles with address 10000h or higher hangs the system
11	LBARs allow specification of an I/O base at 10000h or higher
12	PIC fails if processed interrupt still high when clock goes off
14	ACC PRD may prefetch incorrectly
16	Main GLIU clock domain does not awaken when statistics counter generates an ASMI
17	Byte accesses to ACPI PM1_STS and PM1_EN (ACPI I/O Offset 00h and 02h)
18	WORD and BYTE writes to PMC registers may corrupt other PMC register writes
20	PIC does not support Polling mode
21	Automatic clock gating for UART clock domain does not work in CEIR mode
30	Resume from STALL/CLEAR_FEATURE HALT
31	USB device zero length packet when FIFO full
35	If RxFIFO is not empty, clearing endpoint NAK bits not possible

Table 1-1. Issue Summary (Continued)

Issue#[1]	Description
36	Write to GPIO High Bank Feature Bit registers failed after suspend
38	SMBus hold time too short
40	Missing LOWBAT_FLAG after abnormal standby
41	Normal work delay does not work if only WORK_AUX is deasserted during standby
42	Sleep_X is not deasserted if delay is larger than PM_SED delay
43	LPC Aborts on Long_Sync or Ready_Sync for I/O writes and reads
44	USB Device interrupt status issue
45	Retry counter does not distinguish between accesses
46	High V_{BAT} current
47	UDMA Mode 5 stability issues
48	USB over current condition results in deadlock
49	PMS I/O Offset 54h[0] status does not work
51	High speed DC levels too high
52	USB test mode
53	Abnormal work delay is only active if register is locked
54	Malfunction of squelch and chirp detection logic
55	Stability Issues during USB On-the-Go Host Negotiation Protocol
56	Stability Issues upon USB EHC Port Suspend in S0
57	USB Serial Short Detect Status flag is set after power on
58	USB Device mode remote wakeup fails in high speed

1.   Issue numbers may not be sequential since issues are omitted when resolved.

2.0   Issues

1.   PIT deviation from industry standard operation

Description: *The Indispensable PC Hardware Book* says: "If you output a counter latch command and later a read-back command to determine the counting mode, without having read the counter value before, then the PIT first supplies the status byte with the first IN instructions, and only afterwards the byte(s) that indicate the counter value". Effectively, a read-back command should cancel an uncompleted counter latch command.

For the PIT in the CS5536 companion device, this 'cancellation' does not happen. The PIT first supplies the counter value.

Implications: The issue only occurs with a 'questionable' programming sequence under which a new command is issued before completing the current command. Therefore, the negative effects of this deviation are negligible.

Resolution: Do not issue a read-back command until the previous latch command has completed.

2.   Debug port hangs system if used

Description: The GeodeLink™ Interface Unit (GLIU) incorporates a debug port that allows internal GeodeLink traffic to be copied to an external port so it can be viewed. The GLIU uses a special packet type to indicate debug. The debug port should detect this packet type and always forward it to the LPC bus. The debug port detects the packet type but hangs.

Implications: Since there is no 'internal only' GeodeLink traffic in the CS5536 companion device, the loss of this feature is minimal. All CS5536 internal traffic exits or enters the CS5536 via the PCI bus. Hence, all internal traffic is also external.

Resolution: None. Do not use the debug port.

3.   Incorrect operation of PIT count mode 3 value load

Description: A new count value should not affect the current counting. However, the new count value is immediately loaded without finishing the counting process of the original count value.

Implications: Software that relies on this operation will not operate properly.

Resolution: None. Avoid reliance on this property of the PIT.

4.   Restrictions on AEOI bit use in the PIC

Description: Upon receiving the first interrupt acknowledge pulse, the priority encoder should transfer the highest priority bit from the IRR to the ISR (PIC I/O Port 020h) and clear the corresponding bit in the IRR. However, the XPIC (Extended PIC) does not clear the IRR bit until one clock after the second interrupt acknowledge pulse. When the PIC performs an auto end of interrupt (AUTO_EOI) (PIC I/O Port 021h[1]), this causes two interrupts to be sent to the CPU instead of one.

Implications: When AUTO_EOI (PIC I/O Port 021h[1]) is enabled in the master PIC, the master PIC automatically issues a non-specific EOI command on the rising edge of the last interrupt acknowledge pulse. The AEOI bit can only be enabled on the master PIC. AEOI should only be enabled when a nested multilevel interrupt structure is not needed.

PCs need a nested multilevel interrupt structure. DOS uses non-specific EOIs. Microsoft® Windows®, Linux, BeOS, and FreeBSD all use specific EOIs.

This feature is not used on PCs.

Resolution: None.

5.   DMA rotating mode does not rotate correctly

Description: There are four transfer channels/requests. Given a case where each request arrives one clock cycle later with respect to the previous request, the transfers should be performed in the same order as the incoming requests. With rotating priority, the most recent channel to be serviced becomes the lowest priority, with the priorities of the other channels rotated accordingly. This design is supposed to prevent any one channel from monopolizing the system. However, the priorities do not always rotate as expected.

Implications: The transfers on multiple channels do complete successfully. However, the sequence of the transfers do not rotate correctly. Since legacy devices using such techniques are so slow compared to existing system speeds, and since there are so few multiple legacy DMA operations, there is no significant impact of incorrect rotation.

Resolution: None.

6. PMC Sleep Clock control disable side effect

Description: The use of SLEEP_X, SLEEP_Y, and SLP_CLK _EN# (ball C2, J3, A1, respectively) is optional and subject to optional delays. All of these options are specified as independent. However, if any option is desired, the Sleep Clock option must be enabled.

Implications: Operation may not be as expected if the Sleep Clock option is not properly enabled.

Resolution: If the Sleep Clock option is not desired and if one or more of the other options above are desired, then disable the Sleep Clock option at the GPIO but enable it in PMS I/O Offset 10h[30]). A disable at the GPIO has the same system effect as a disable in the PMC. Thus always enable Sleep Clock at the appropriate PMC register and then enable/disable actual use via the GPIO controls.

7. GLIU data compare cannot generate a hit

Description: The GLIU contains a debug feature that generates a signal if a specified data pattern is detected in a data packet passing through it. This signal is passed to the GLCP as an "error" for debug. The detection operation does not work.

Implications: The detection operation is designed to support debug efforts only, and hence, this failure has no operational impact. The operation is controlled by the following registers:
GLIU_DA_COMPARE_VAL_LO,
GLIU_DA_COMPARE_VAL_HI,
GLIU_DA_COMPARE_MASK_LO,
and GLIU_DA_COMPARE_MASK_HI
(MSR 510100D0h-510100D3h). Due to this issue, these registers should be left in there default state and not written.

Resolution: None.

8. GLIU Error MSR unexpected address flag failure

Description: When the GLIU receives an MSR packet request with an address that does not match an implemented register, this is considered an "Unexpected Address Error". If the "Unexpected Address" mask bit in GLIU_GLD_MSR_ERROR is in the enabled state (MSR 51010003h[1] = 0) and such an error occurs, then two actions should happen: 1) the "Unexpected Address" flag (MSR 51010003h[33]) should become active; 2) the "Exception" flag in the response packet should be set. However, neither of these actions occur.

Implications: No functional impact. This is a rare failure that only occurs in debug (i.e., does not occur in an operational system).

Resolution: None.

9. 8237 software DMA memory write from LPC fails

Description: The 8237 DMA Controller contains a legacy feature called "Software DMA". This is a diagnostic feature designed to generate memory access cycles. The actual data moved with the DMA is a "don't care", specifically, software DMA has no operational use. Conceptually, the combinations supported are "don't care" data from the UART or LPC bus written to memory and "don't care" data read from memory to the UART or LPC bus. However, the LPC bus "don't care" data written to memory combination does not work. Under the failing combination, the LPC controller issues a DMA acknowledge to the LPC bus. However, since no device actually asked for a DMA, no device responds. The LPC controller then aborts the DMA request and does not write to memory. The overall software DMA operation will complete but no "don't care" data is written to memory.

Implications: No operational impact.

Resolution: Do not use the failing combination in diagnostic tests.

10. I/O cycles with address 10000h or higher hangs the system

Description: Any I/O address 10000h or higher on the PCI bus should not be claimed by the CS5536 companion device. Assuming no other PCI device made a claim, such an address would master abort. Such an address can be generated by an x86 processor by performing a 16-bit access to FFFFh, which will increment to 10000h.

However, the CS5536 claims addresses at or above 10000h. These default to the Diverse Device, which hangs for such addresses.

Implications: Operationally, there is no impact because no "normal" software would make such an access. This issue is likely only to occur under new software code that is not fully debugged.

Resolution: Do not generate PCI I/O cycles with addresses at or above 10000h.

11. LBARs allow an I/O base at 10000h or higher

Description: The ATA-5 Controller (ATAC) and Diverse Device (DD) allow I/O Local Base Address Register (LBAR) values at 10000h or higher. Such addresses are illegal under an x86 system. Such settings should not be used.

Implications: Operationally, LBAR values of 10000h or higher are not used by the BIOS or operating system. The fact that an LBAR can be set to an illegal value has no operational impact.

Resolution: Do not use LBAR values of 10000h or higher.

12. PIC fails if processed interrupt still high when clock goes off

Description: This issue applies when a PIC interrupt input is configured for "edge" operation and the interrupt source remains high long after the interrupt has been serviced. For example, PIT Timer 0 is connected to PIC Interrupt 0. This timer is used as a continuously running interval or periodic timer. The timer is normally programmed to produce a square wave signal with at least a 50% high duty cycle and frequency less than 250 Hz. The low-to-high edge of this signal generates the periodic interrupt. This means the interrupt source remains high hundreds of ms after the interrupting edge. This is more than enough time for the interrupt to be generated and serviced. By itself, this is not a problem.

The DD features automatic hardware clock gating on the Local bus clock. If there is no other activity in the DD, the Local bus clock automatically turns off after a given interrupt has been generated and serviced. If the interrupt source of an edge-configured PIC input remains high after the clock goes off, the PIC can not return to an Idle state. The Idle state is associated with the interrupt input being low. From Idle, any low-to-high edge produces a new interrupt. Because the PIC can not return to Idle, any new low-to-high edges are not recognized as interrupts. Since the interrupt is used to turn the clock back on, the clock never comes back on. Thus, the system potentially hangs due to the lack of an interrupt.

Unrelated activity elsewhere in the DD could turn on the Local bus clock while the interrupt source is low and allow the PIC to return to Idle. However, if a source, such as in the PIT for example, goes low and then back high while the clock is off, the PIC will not recover even if the Local bus clock comes back on due to an unrelated activity. A PIC edge-configured input can only return to Idle if the clock is currently on or goes on while the source input is low.

Implications: Interrupts may be missed. If an interrupt is missed, then the system may hang or exhibit other unexpected behavior.

Resolution: Do not turn on automatic clock gating for the DD Local bus.

14. ACC PRD may prefetch incorrectly

Description: The recommended setting for ACC_GLD_MSR_CONFIG (MSR 51500001h) is 00000000_0008F000h. This setting allows the ACC master to determine the GA prefetch setting when it does a Physical Region Descriptor (PRD) access. The master requests a prefetch value of two (010 binary) for PRD requests. This is a prefetch of eight bytes. If the PRD table is 8-byte aligned in main memory, this is OK. If not aligned, this setting results in the first four bytes of the next PRD to be prefetched. This could introduce an error.

Implications: The error "exposure" of this issue is as follows:

1) Audio playback (memory read): None. The data fetches cause the prefetch to be discarded.

2) Audio record (memory write):
a) 8-byte aligned PRD tables. None. GA prefetches just the right amount of data.
b) 4-byte aligned PRD tables. GA will prefetch first four bytes of next PRD. This is a hazard only if the software is changing the next PRD entry associated with the current PRD entry.

Note that any new audio operation involves a write to the native registers. Any I/O write discards all prefetched data unconditionally.

Resolution: Insure PRD table changes being made on the fly are at least two tables ahead of the current PRD.

16. Main GLIU clock domain does not awaken when statistics counter generates an ASMI

Description: When the GLIU statistics counters are in use, they generate ASMIs under certain conditions. These counter functions work correctly. The primary GLIU logic and these counters operate on different clock domains and hence have separate controls in GLIU_GLD_MSR_PM (MSR 51010004h). They are domains zero and one respectively. If hardware clock gating is enabled for domain zero and a statistics counter generates an ASMI, the domain zero clock should wakeup to pass on the ASMI, but it does not.

Implications: If the statistics counters are used in a mode that generates an ASMI, then any given ASMI could be lost if hardware clock gating is enabled for domain zero.

Resolution: If the statistics counters are used in a mode that generates an ASMI, then leave hardware clock gating off for domain zero.

17. **Byte accesses to ACPI PM1_STS and PM1_EN (ACPI I/O Offset 00h and 02h)**

    Description: Byte reads and writes to ACPI registers, PM1_EN and PM1_STS, do not complete. The current implementation supports only WORD and DWORD reads/writes to PM1_EN and PM1_STS.

    Nature of the failure: PM1_STS is located at ACPI I/O Offset 00h and PM1_EN is located at ACPI I/O Offset 02h from DIVIL_LBAR_ACPI (MSR 5140000Eh). They are located on a 32-bit bus so PM1_STS is associated with lanes 1 and 0 while PM1_EN is associated with lanes 3 and 2.

    The following access rules apply:
    1) PM1_STS access requires byte lanes 1 and 0 to be active. If only one lane is active, the access will hang.

    2) PM1_EN access requires byte lanes 3 and 2 to be active. If only one lane is active, the access will hang.

    3) Alternatively, if any 3 or 4 lanes are active, PM1_STS and PM1_EN will be accessed simultaneously as 32-bit operation. If read, both registers are read. If write, only the register(s) associated with (1 and 0) and/or (3 and 2) will be written. Regardless, the access will not hang.

    4) Address bits[1:0] are "don't care" with regards to the PMC.

    5) Any BYTE, WORD, or DWORD access to ACPI I/O Offset 04h hits reserved space and will not hang.

    Any access disregarding the rules above will hang.

    Implications: The PM1_STS and PM1_EN registers are 16 bits, so there is no "natural" need for byte access. However, the ACPI specification allows it. Therefore, byte access is possible but has not been observed in application software.

    Resolution: Do not use byte access to these registers. Alternatively, use AMD BIOS that traps bytes and performs the intended function via system management emulation software.

18. **WORD and BYTE writes to PMC registers may corrupt other PMC register writes**

    Description: The PMC operational clock is different and slower than the DD Local bus clock. A shadow register technique is used to hold write data from DD I/O space temporarily before it is moved to the operational space. The shadow register is updated based on the byte enables associated with the 32-bit write. However, when the operational register is updated with the shadow register contents, the byte lane information is not used. As a result, the register is updated at 32-bit granularity irrespective of the write size.

Additionally, the shadow register for the inactive byte lane retains the previous write data. Thus, a corruption to a future write is possible. There are two categories of corruption: local and cross. Local corruption can only occur to the same register on a future write. Cross corruption can occur to an unrelated register. All the PMC registers are listed below by category.

Local	Address
PM1_STS	ACPI I/O Offset 00h
PM1_EN	ACPI I/O Offset 02h
GPE0_STS	ACPI I/O Offset 18h
GPE0_EN	ACPI I/O Offset 1Ch
PM_WKD	PMS I/O Offset 30h
PM_WKXD	PMS I/O Offset 34h
PM_RD	PMS I/O Offset 38h
PM_WKXA	PMS I/O Offset 3Ch
PM_FSD	PMS I/O Offset 40h
PM_TSD	PMS I/O Offset 44h
PM_PSD	PMS I/O Offset 48h
PM_NWKD	PMS I/O Offset 4Ch
PM_AWKD	PMS I/O Offset 50h
PM_SSC	PMS I/O Offset 54h

Cross	Address
PM1_CNT	ACPI I/O Offset 08h
PM2_CNT	ACPI I/O Offset 0Ch
PM_TMR	ACPI I/O Offset 10h
PM_SSD	PMS I/O Offset 00h
PM_SCXA	PMS I/O Offset 04h
PM_SCYA	PMS I/O Offset 08h
PM_SODA	PMS I/O Offset 0Ch
PM_SCLK	PMS I/O Offset 10h
PM_SED	PMS I/O Offset 14h
PM_SCXD	PMS I/O Offset 18h
PM_SCYD	PMS I/O Offset 1Ch
PM_SIDD	PMS I/O Offset 20h

Implications: The ACPI specification allows WORD and BYTE accesses to the ACPI defined registers PM1_STS, PM1_EN, PM1_CNT, and PM2_CNT. However, byte accesses result in the register corruption described above. The ACPI specification allows DWORD, WORD, and BYTE accesses to ACPI defined registers GPE0_STS and GPE0_EN. However, WORD and BYTE accesses result in the register corruption described above. For the proprietary non-ACPI registers, the CS5536 companion device specification restricts accesses to DWORD only.

Resolution: An SMI I/O trap can be setup for the ACPI defined registers. This trap can control accesses to the specified registers and prevent an incorrectly sized access.

20. PIC does not support Polling mode

Description: The standard 8259 PIC (Program-mable Interrupt Controller) has a Polling mode that is not supported by the CS5536 companion device. Specifically, the OCW3 bit 2 (I/O port 20h/A0h[2]) is marked reserved, indicating that the Polling mode is not supported.

Implications: This mode is not normally used in x86 systems.

Resolution: None.

21. Automatic clock gating for UART clock domain does not work in CEIR mode

Description: In CEIR mode with clock gating on (i.e., MSR 51400004h[15:14] and [13:12] = 01), the UART clock becomes inactive when the RX_FIFO is empty and the incoming data is a long stream of 1s even though the RXACT bit (UART I/O Offset 07h[5]) is set. This affects both UART1 and UART2.

Implications: CEIR mode will not work correctly with clock gating enabled.

Resolution: Do not turn on automatic clock gating for these domains. Device power will therefore be slightly higher than nominal. Note that wakeup from this device is still possible even with clock gating disabled.

30 Resume from STALL/CLEAR_FEATURE HALT

Description: When the remote host sends a CLEAR_FEATURE ENDPOINT_HALT to a stalled endpoint, software is not notified like it should be, and that endpoint is silently set to NAK all subsequent requests.

Implications: Once this occurs, communication with the remote host is prevented, software cannot react and properly re-initialize that endpoint.

Resolution: The device driver should poll the S-bit (bit 0) in the EPINCTRL_x and EPOUTCTRL_x registers to look for the stall.

31 USB device zero length packet when FIFO full

Description: The device driver is not notified when writing a zero length packet to a full TxFIFO.

Implications: The packet is not transmitted and the device driver is not informed. This would most likely lead to data corruption with the remote host.

Resolution: The device driver must ensure never to write to a full TxFIFO.

35 If RxFIFO is not empty, clearing endpoint NAK bits not possible

Description: When the UDC device driver writes to CNAK (bit 8) in the endpoint control registers (EPOUTCRTL_x and EPINCTRL_x), the device controller should stop NAKing regardless of FIFO contents. It is the UDC device driver's responsibility to ensure that no overflows occur. However, CNAK only prevents the NAKing when the FIFO is empty.

Implications: Permanent NAKing on all endpoints can happen.

Resolution: The UDC device driver can set the NAK bits for every endpoint after receipt of any packet, resulting in serialized processing of packets. In this manner, the device driver can always know the contents of the FIFO.

36 Write to GPIO High Bank Feature Bit registers failed after Suspend

Description: Atomic write transactions to the atomic GPIO High Bank Feature Bit registers should only affect the bits selected by the atomic write transaction. However, after Suspend, an atomic write transaction to any of the atomic GPIO High Bank Feature Bit registers will affect the selected bit correctly, but will clear all non-selected bits of the accessed register.

Implications: Unexpected behavior results after Suspend if these registers are written.

Resolution: After Suspend, an atomic write transaction to any of the atomic GPIO High Bank Feature Bit registers must be executed as a Read-Modify-Write transaction to all bits of the register.

38 SMBus hold time too short

Description: SMB Specification v2.0 requires a minimal data hold time, T_HD:DAT, of 300 nanoseconds. For the CS5536 companion device, the minimum data hold time, T_HD:DAT, is 280 nanoseconds.

Implications: None expected.

Resolution: None.

40   Missing LOWBAT_FLAG after abnormal standby

Description: If LOW_BAT# is asserted in Normal or Re-start Standby state, the system is caused to enter a Faulted Standby state, but the status bit (LOWBAT_FLAG) in the PM_SSC register (PMS I/O Offset 54h[5]) fails to be set.

Implications: After exit from Standby, the previous occurrence of a low-battery condition cannot be detected via the LOWBAT_FLAG bit (PMS I/O Offset 54h[5]).

Resolution: None.

41   Normal work delay does not work if only WORK_AUX is deasserted during standby

Description: If the Standby state is entered normally and PMS I/O Offset 30h[30] is cleared, the Working state can be entered again immediately, without waiting for NWKD_DELAY (PMS I/O Offset 4Ch[19:0]) number of 32 kHz clock edges.

Implications: No functional issues are expected.

Resolution: Do no rely on NWKD_DELAY.

42   Sleep_X is not deasserted if delay is larger than PM_SED delay

Description: When the system is transitioning out of the Sleep state, the PM_SCXD, PM_SCYD, and PM_IN_SLPCTL registers' (PMS I/O Offset 18h, 1Ch, and 20h[29:0]) delay counters are reset upon the de-assertion of SUSPA#. In consequence of the premature counter reset, the respective control signals SLEEP_X and SLEEP_Y are not de-asserted and the PCI/IDE input signals are not re-enabled.

Implications: When the system is transitioning out of the Sleep state, the external circuitry controlled by SLEEP_X and SLEEP_Y remains in the Sleep state and the PCI and IDE input signalling remains non-functional.

Resolution: Program the PM_SCXD, PM_SCYD, and PM_IN_SLPCTL delay counters (PMS I/O Offset 18h, 1Ch, and 20h[29:0]) to values less than the value of the PM_SED delay counter (PMS I/O Offset 14h[29:0]).

43   LPC Aborts on Long_Sync or Ready_Sync for I/O writes and reads

Description: Under random conditions the CS5536 companion device's LPC controller may abort a transaction when it observes only two consecutive clocks without a defined (non-reserved) SYNC pattern after the turn-around phase.

Implications: This behavior has only been observed with LPC-to-ISA bridges, which may drive defined (non-reserved) SYNC patterns not earlier than the third clock after the turn-around phase. In that case, write transactions are discarded and read transactions return a value of all ones.

Resolution: A Programmable Logic Device (PLD) can be programmed and connected to the LPC bus in a way that works around the above mentioned issue. See the *AMD Geode™ CS5535/CS5536 Companion Devices LPC-to-ISA Bridge* (publication #33329) application note.

44   USB Device interrupt status issue

Description: When DMA is in progress, and an IN token is received, the interrupt service routine clears the IN Token bit in the Endpoint Status register (UDC Memory Offset 0004h-0084h[6]). Additional IN tokens will get a negative acknowledge and should not set the IN Token bit. If the TXFIFO is empty when the additional IN token is received, a negative acknowledge is sent, but the IN Token bit in the EPINSTS register is incorrectly set.

Implications: The current data packet may be mixed with the next one.

Resolution: The interrupt service routine should check the TDC bit (bit 10) in the EPINSTS register. If TDC is set, the IN Token bit must be cleared and ignored.

45   Retry counter does not distinguish between accesses

Description: The Retry Transaction Limit (RTL) bit (GLPCI MSR 51000010h[51:49]) determines the number of retries the master should attempt for a given transaction. The implementation counts not only its own retries but also any other retry on the PCI bus.

Implications: The master may stop retrying earlier than expected.

Resolution: Program a higher value for MSR 51000010h[51:49] or disable this functionality by programming to 0.

46   High V_{BAT} current

Description: On a very small number of devices, higher than expected current (greater than 200 µA) can occur on V_{BAT} when the battery is first installed. Once V_{CORE_VSB} is applied, then the V_{BAT} current returns to normal.

Implications: If V_{CORE_VSB} is not applied to the device immediately after V_{BAT} is applied, then the battery drains faster than expected.

Resolution: Do not install the battery until just before V_{CORE_VSB} is to be applied to the system. Use a jumper to disable the battery from V_{BAT} until V_{CORE_VSB} power is applied. Applying V_{CORE_VSB} always returns V_{BAT} current back to the expected range.

47   UDMA Mode 5 stability issues

Description: When two IDE devices are used and when both devices are mounted in trays, timing problems have been observed when in UDMA Mode 5.

Implications: The occasional timing failures result in CRC errors, which result in performance degradation.

Resolution: Drop back to UDMA Mode 4 for safer operation or change system configuration to reduce errors.

48   USB over current condition results in deadlock

Description: When host driver software writes 0 to the Port Reset bit (EHC Memory Offset 54h-60h[8]) while a USB over current event exists, the host controller does not clear this bit in response. In this situation the host controller does not identify the successful termination of the bus reset due to the existing over current event.

Implications: Host driver software polls the Port Reset bit looking for it to be cleared to 0 by the host controller. Since the bit never clears, the driver hangs.

Resolution: System firmware should disable over current reporting by writing 0h to the OCR bits (UOC Memory Offset 00h[13:10]).

49   PMS I/O Offset 54h[0] status does not work

Description: PMS I/O Offset 54h[0] is not reliably set after the system transitions out of the power off state.

Implications: System software can not use PMS I/O Offset 54h[0] in order to determine whether the system has transitioned out of the power off state.

Resolution: After the system transitions out of the power off state, PMS I/O Offset 54h[12:1] are cleared to zero. System software should use this setting in order to determine whether the system has transitioned out of the power off state.

51   High speed DC levels too high

Description: In high speed mode, the CS5536 may drive the USB data lines up to 450 mV. The specification states the max voltage to be 440 mV.

Implications: No functional impact has been observed. However, driving an output voltage of greater than 440 mV does not comply with the USB 2.0 electrical specification. A waiver may be required if the B1 revision of the CS5536 does not pass the USB High Speed Logo specification.

Resolution: AMD has received a waiver for USB logo certification for revision B1. The high DC levels have no impact to USB 2.0 functionality. End product USB logo certifications will be obtainable via the USB 2.0 certification as well as the waiver for revision B1.

52   USB test mode

Description: USB electrical compliance test software has been observed to set bits [19:16] of the Port Status and Control registers (PORTSC_x) to 2h before setting EHC Memory Offset 10h[0] to 0, and then waits for EHC Memory Offset 14h[12] to be cleared by the host controller. When programmed in this order, the host controller asserts 15K ohm pulldowns on both USB signals, instead of driving SE0 to those signals.

Implications: The USB electrical compliance test software will fail.

Resolution: Attach a high speed termination to the USB port under test. This can be achieved by either connecting a passive high speed termination or connect a USB peripheral in high speed mode. Once in TEST_SE0 test mode, the high speed termination can be removed.

53   Abnormal work delay is only active if register is locked

Description: If the Standby state is entered abnormally and PMS I/O Offset 50h[31] is cleared, the Working state can be entered again immediately without waiting for AWKD_DELAY (bits [19:0]) number of 32 KHz clock edges to pass.

Implication: No failure of the system function is expected.

Resolution: Lock the Abnormal Work Delay register (PMS I/O Offset 50h) after initialization.

54   Malfunction of squelch and chirp detection logic

Description: Under the following conditions a USB high speed peripheral device may sporadically become associated with the USB Open Host Controller.

– Upon connect, the peripheral device termination drives the D+ line above 100 mV.
– During peripheral device chirp, the D+ line is impacted by cross-talk from the rising edge on the D- line in a way that the differential high speed receiver in the USB host detects a J-state.

When both of these conditions occur together the peripheral device can be recognized as a full speed device and become associated with the USB Open Host Controller.

Implication: Only the full speed traffic capabilities of the high speed peripheral device are used.

Resolution: Either run the device at full speed or disconnect and reconnect the USB peripheral device.

55   Stability Issues during USB On-the-Go Host Negotiation Protocol

Description: Under very sporadic conditions, when the CS5536 acts as host in a USB On-the-Go (OTG) session and the peripheral device initiates the Host Negotiation Protocol, the CS5536 fails to disconnect its pull-down resistors from the USB data signals, USBx_DATPOS and USBx_DATNEG. The Host Negotiation Protocol fails to complete.

Implication: The USB OTG session fails and the USB port hangs. The only workaround is to reset and reinitialize the USB EHC host controller.

Resolution: Since resetting the port under this condition is not a practical solution for normal operation, USB OTG is not considered to be supported on the CS5536 B1 version of silicon. However, since both USB Host and USB Device modes operate correctly, another option is to use cable select to achieve desired port operation.

56   Stability Issues upon USB EHC Port Suspend in S0

Description: Under very sporadic conditions, when a USB EHC host port is transferred into USB Port Suspend state, the CS5536 fails to disconnect its pull-down resistors from the USB data signals, USBx_DATPOS and USBx_DATNEG. This condition applies to a scenario when the operating system transfers a USB EHC port into the USB Suspend state, since e.g., a USB high speed hub is attached to this port without any device connected. Unplug-

ging the last device from the HUB will trigger a USB port suspend while the system is in ACPI S0 state.

Implication: The USB EHC port fails to enter the USB Suspend state and the USB port hangs.

Resolution: When this situation occurs the USB EHC host controller must be reset and reinitialized. This situation may be prevented by avoiding system setups that allow system software to transfer a USB EHC port into USB Port Suspend state while the system is in ACPI S0 state.

57   USB Serial Short Detect Status flag is set after power on

Description: After reset, in conjunction with cycling the power supply, the value of MSR Address 51200005h[36] may be 1.

Implication: A false serial short condition may be detected.

Resolution: System software must clear this bit by writing 1 to MSR Address 51200005h[36] when transferring the system out of ACPI state G3, S3, S4, or S5.

58   USB Device mode remote wakeup fails in high speed

Description: When the USB device controller is configured as a USB high speed device and is in the USB suspend state, setting DEVCTRL[RES] (UDC Memory Offset 0404h[0]) causes the USB device controller to drive a USB high speed K-state on the USB bus instead of a USB full speed K-state.

Implication: The USB host controller at the other end of the cable may not properly resume.

Resolution: Configure the USB device controller as a USB full speed device when USB remote wake-up capability is required.

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