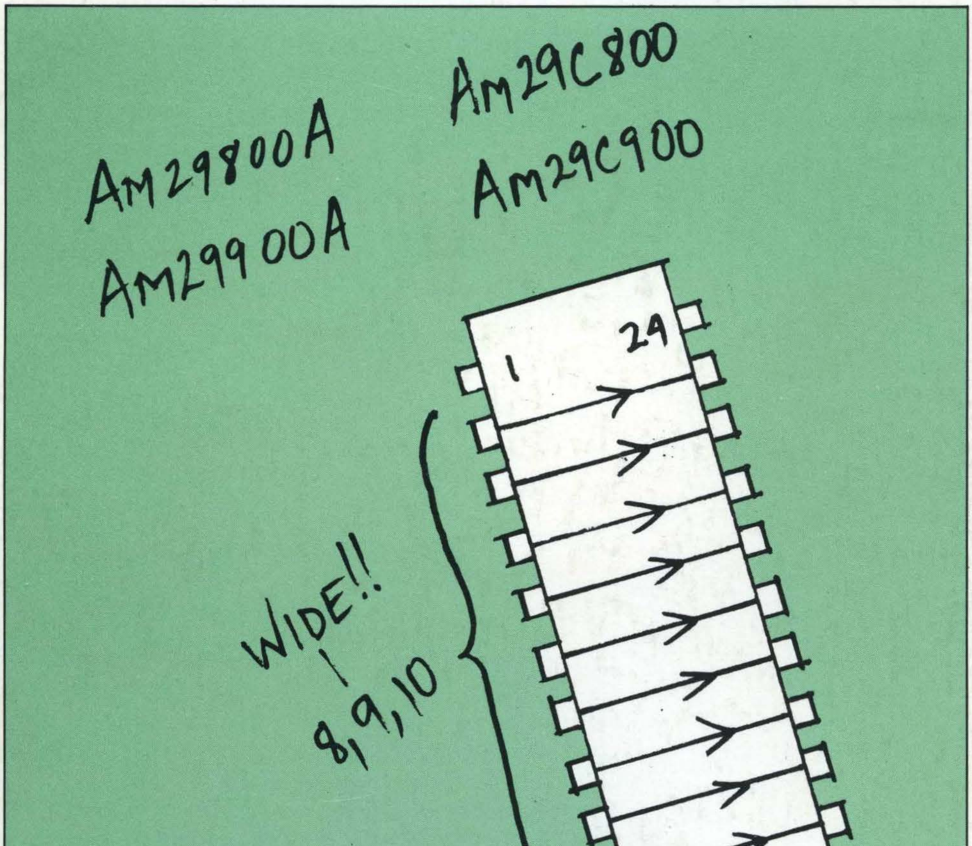
Bus Interface Products

1988 Data Book

Advanced Micro Devices



1988 Data Book Bus Interface Products AMD

Advanced Micro Devices

Bus Interface Products
Data Book

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"Increasing integration and performance on the system level now require corresponding improvements in bus interface. AMD's Am29C800 and Am29800A families meet this challenge, offering the designer innovative solutions to his interface needs. We are confident that you will find these devices suitable for your most demanding applications."

Fred J. Roeder
Vice-President and Managing Director
Logic Products Division

CONTENTS

NUMERICAL DEVICE INDEX

INTRODUCTION

This document contains product specifications for two series of high-performance bus interface devices — the CMOS Am29C800 Family and the Bipolar Am29800A Family. Together these families provide interface solutions for many system applications, offering a variety of interface functions in 8-, 9-, and 10-bit data paths.

The Am29C800 High-Performance CMOS Bus Interface Family provides bipolar-compatible speed performance at a fraction of the static power consumption. This series consists of CMOS registers, latches, buffers, transceivers, parity transceivers, and pipeline registers, all of which are pin-for-pin compatible with their bipolar Am29800A counterparts. Produced with AMD's exclusive CS-11 CMOS process, the Am29C800s feature 24-mA output drive current over the commercial and military operating ranges. In addition, the DC and AC electrical parameters are specified in accordance with the most current recommendations of the JEDEC JC40.2 committee, which is preparing a standard for FCT-compatible CMOS specifications.

The Am29800A High-Performance Bipolar Bus Interface Family is a performance upgrade of AMD's industry-standard Am29800 Family. The new Am29800As offer higher speed and lower power consumption than their predecessors, while maintaining an output drive current of 48 mA (commercial) and 32 mA (military). Am29800A functions include registers, latches, buffers, transceivers, parity transceivers, and pipeline registers, all of which are pin-for-pin compatible with the Am29800s, as well as the Am29C800s. The Am29800As are produced with AMD's patented IMOX bipolar process, which provides the speed and drive capability necessary for today's high-performance systems.

The Am29C800s and the Am29800As are available in a wide variety of package options, including 24-pin slim plastic and ceramic DIPs, 24-pin ceramic flatpacks, and 28-pin plastic leaded and ceramic leadless chip carriers. 24-pin plastic small outline packages are planned as future offerings; physical dimensions for each of these package types can be found in the Package Outline section at the end of this data book.

For selected members of the Am29C800 and Am29800A Families, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. This pinout is achieved by rotating the die 90 degrees inside the DIP package. The bipolar (Am29800A) devices with this "rotated" pinout will be designated Am29900A, and the CMOS (Am29C800) devices with this pinout will be called Am29C900. For specific pinouts and ordering part numbers, see the individual data sheets.

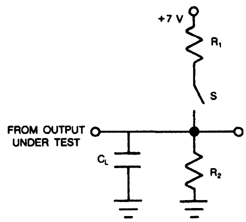
Information common to each of the devices in the Am29C800 and Am29800A families, such as test circuits, waveforms, propagation delay graphs, ESD data, and capacitance data appears at the beginning of the data book. Individual data sheets follow.

For more information, please contact the nearest AMD sales office or representative.

Am29C800/Am29800A GENERAL PRODUCT INFORMATION

SWITCHING TEST CIRCUIT

THREE-STATE OUTPUTS



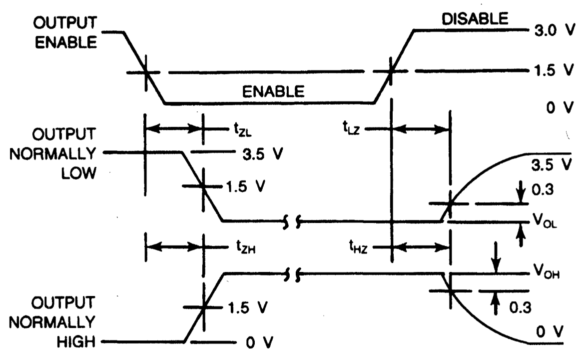
TC002682

SWITCH POSITIONS FOR PARAMETER TESTING

Parameter	S Position
t_{PLH}	OPEN
t_{PHL}	OPEN
t_{HZ}	OPEN
t_{ZH}	OPEN
t_{LZ}	CLOSED
t_{ZL}	CLOSED

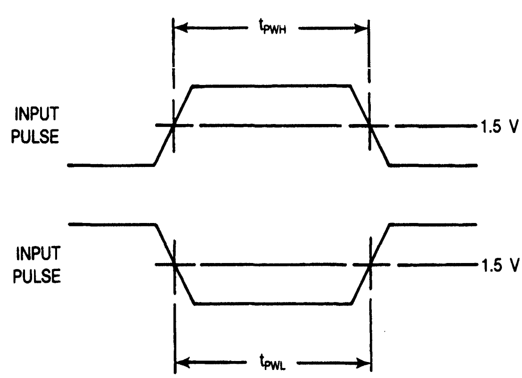
Note: Switch is closed for tests on open-collector and open-drain outputs.

SWITCHING TEST WAVEFORMS



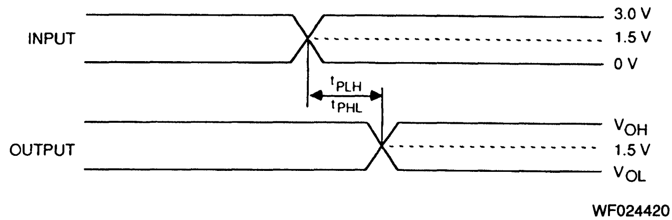
WF001414

Enable and Disable Times



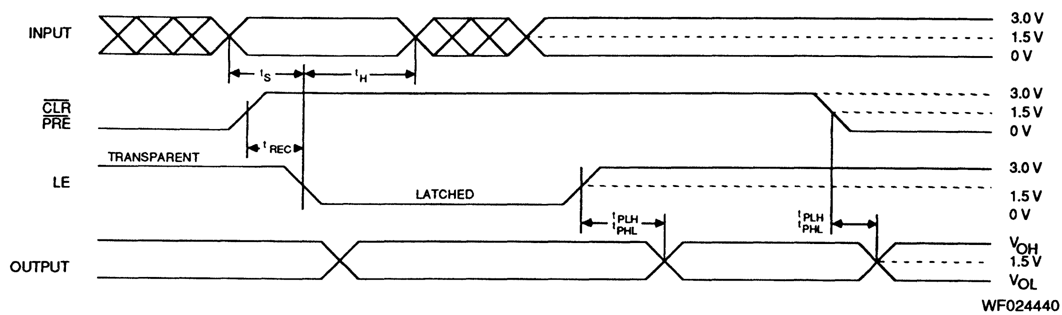
WF001271

Pulse Width



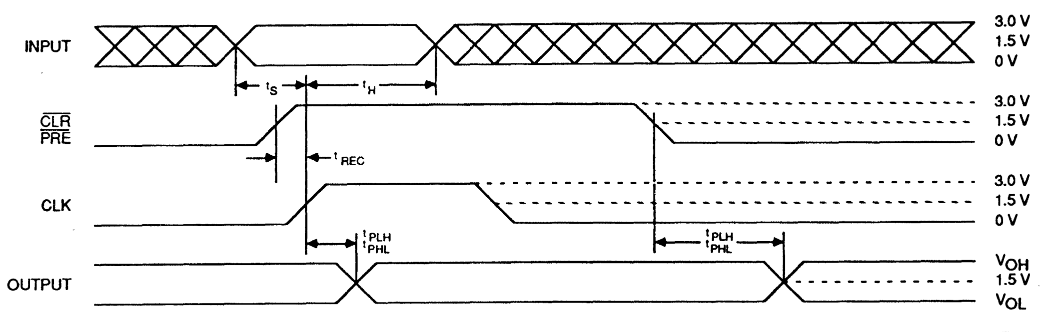
Propagation Delay for Buffers, Transceivers, and Latches in the Transparent Mode

(Am29827A, Am29828A, Am29861A, Am29863A, Am29841A, Am29843A, Am29845A, Am29833A, Am29853A, Am29855A, Am29C827, Am29C828, Am29C861, Am29C863, Am29C841, Am29C843, Am29C833, Am29C853, Am29C855)



Switching Parameters for Circuits with Latches

(Am29841A, Am29843A, Am29845A, Am29853A, Am29855A Am29C841, Am29C843, Am29C853, Am29C855)



Switching Parameters for Circuits with Registers

(Am29821A, Am29823A, Am29825A, Am29833A Am29C821, Am29C823, Am29C833)

TEST PHILOSOPHY AND METHODS

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data sheet reconciliations that follow.

Capacitive Loading for AC Testing

Automatic test equipment (ATE) and its associated hardware has stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays into the high-impedance state, and are usually specified at a load capacitance of 5.0 pF. In these cases, the ATE test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical ATE is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances, even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data sheet loads, may be used during production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of devices near threshold frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" HIGH and LOW levels are used for other tests. Generally, this means that function and AC testing are performed at "hard" input levels.

AC Testing

Some AC parameters cannot be measured accurately on automatic testers because of tester limitations. In these cases, the parameter in question is tested by correlating the tester data to bench data.

Certain AC tests are guaranteed by correlating to other tests that have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

When performing I_{SC} tests on devices containing latches or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements, which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result is identical to the $V_{OUT} = 0$, $V_{CC} = $ Max. case.

Am29800 TYPICAL CAPACITANCE VALUES

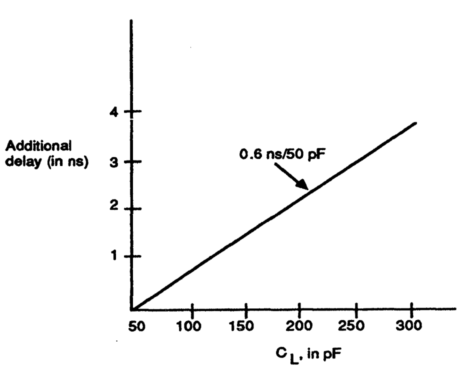
The following table shows typical zero bias capacitance values for ceramic packages.

Device Family	Output to GND	Output to V_{CC}	Input to GND	Input to V_{CC}
Am29C800	10 pF	10 pF	5 pF	5 pF
Am29800A	15 pF	15 pF	10 pF	10 pF

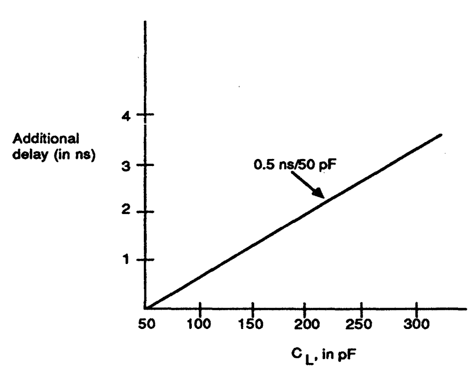
TYPICAL SWITCHING SPEEDS vs. LOAD CAPACITANCE

AC delays in the Am29800 data sheets are specified for unloaded outputs only. The following graphs show the typical effects of increased capacitive loads on propagation delays. Note that these graphs display typical derating, over the entire V_{CC} and temperature range.

Am29C800



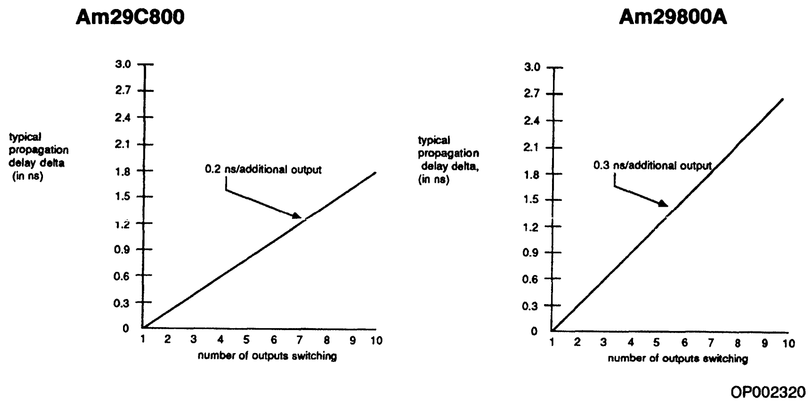
Am29800A



OP002500

TYPICAL SWITCHING SPEEDS vs. NUMBER OF OUTPUTS SWITCHING

Some degradation of propagation delay is normally experienced when several outputs switch simultaneously. By industry convention, data sheet limits are specified for only one output switching. To assist the system designer, we offer the following graphs to estimate speed degradation in the Am29800 Family.



Note that these graphs are to be used as design guidelines and should not be used to generate specification limits.

The measurements for deriving this graph were done on a carefully built AC jig in a noise-free environment. All outputs were loaded according to data sheet specifications, and in the case of buffers and transceivers, all inputs were switched simultaneously from the same signal source.

It is important to note that conditions external to the device can also contribute to the speed degradation. For example, inductance of PC board traces, inefficient GROUND and V_{CC} planes, and inadequate bypassing can cause significant GROUND and V_{CC} bounce which will in turn degrade AC delay when several bits are switched simultaneously. In the case of buffers and transceivers, input signal skew will cause a sustained disturbance of internal threshold due to a protracted GROUND bounce within the device. This can result in further degradation of AC delays. These conditions are application-specific. Therefore, if the system designer sees speed degradation much in excess of the guidelines given, a closer look should be taken at board layout and the application.

ESD PROTECTION

All Am29C800 and Am29800A devices are protected from ESD damage up to 2000 V.

SIMULTANEOUS SWITCHING CONSIDERATIONS

High current drive, short propagation delays, and fast logic level transitions at the output are the characteristics of TTL-compatible high-speed bus interface circuits, such as those in the Am29C800 and Am29800A family of products. When they are used in high-performance systems, simultaneous switching of several outputs is a common occurence. During such switching, noise is generated due to rapid changes in the drive currents (di/dt) and their interaction with the parasitic inductance (L) of the bonding wires and package leads associated with the V_{CC}, GROUND, and output terminals. This section describes the nature of this noise, its impact on circuit behavior, and the measures that can be taken by the IC vendor and the system designer to minimize the effects of this noise.

Description of the Problem

The problem is best described with reference to a simplified first-order equivalent circuit of the output of a high-speed bus interface device. Switches S1 and S2 represent active pull-up and pull-down structures. L1, L2, and L3 represent the parasitic lumped inductances associated with the V_{CC}, GROUND, and output terminals of the device. The output switches are designed to carry high currents so that fast TTL logic level transitions can occur at the output in the presence of heavy capacitance loading.

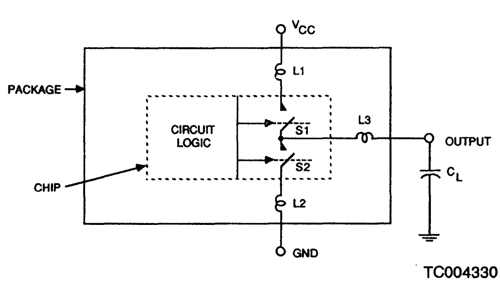


Figure 1. Equivalent Circuit of Bus Interface Output

During the switching of an output, rapid changes occur in the current levels in the V_{CC}, GROUND, and output leads due to the load charging current and the "overlap" current through switches S1 and S2 if these switches turn on simultaneously for a short time. The resulting di/dt and its interaction with L1 and L2 disturb the static voltage levels at the device V_{CC} and GROUND pads. This superimposed noise at the internal power supply nodes is commonly referred to as the "V_{CC} and GROUND BOUNCE." Since the magnitude of this noise is a function of di/dt, it is higher when several outputs switch simultaneously.

As an example, consider a 24-lead ceramic DIP package with a GND pin (pin #12) inductance of 15 nH. A di/dt of 50 mA/ns caused by simultaneous switching of multiple outputs will result in a GROUND bounce of 15 x 50 = 750 mV magnitude. Note that parasitic effects external to the package are ignored in this calculation.

Effects of Ground and V_{CC} Bounce

The total magnitude of the V_{CC} and GROUND noise caused by di/dt and parasitic inductances is a function of circuit configuration, package characteristics, and PC board layout external to the device. Depending on the magnitude of the bounce, one or more of the following effects may occur in a system environment:

1. When several outputs are switching simultaneously, the static logic level of an unswitched output may be disturbed, and may cross the input logic recognition level (V_{IH} or V_{IL}) of the circuits connected to that output.
2. Non-monotonic transitions may occur at the switched outputs due to violation of noise immunity within the circuit.
3. Circuits with storage elements, such as latches and flip-flops, may experience loss of data due to false clocking or latching of erroneous data.
4. A protracted disturbance of voltage levels at internal nodes may cause significant degradation of propagation delays when several outputs are switched simultaneously.

System Design Considerations

The following guidelines will help the system designer minimize the adverse effects of V_{CC} and GROUND bounce when using high-speed interface devices in a high-performance system.

1. GROUND and V_{CC} planes must be used to minimize parasitic effects. Wire-wrap boards will exacerbate the noise problem.
2. Use of sockets or device carriers must be avoided since these will add to the parasitic inductance and increase power supply noise.
3. It is recommended that each device be bypassed directly at the power pins with a high-frequency bypass capacitor in addition to the normal bypassing scheme.
4. Simultaneous switching of several control lines coincident with the switching of multiple outputs should be avoided.
5. Use of a package type that has lower pin parasitics will help minimize the effects of power supply and ground noise. AMD offers surface mount devices (in PLCC, LCC, and SO) and "rotated-die" devices (Am29C900, Am29900A) which reduce the lead inductance associated with the V_{CC} and GND pins.
6. If possible, system timing can be adjusted to allow for settling time before reading the data on the bus.
7. External series damping resistors can be used on the outputs that are subjected to simultaneous switching. This will slow down the transition times and reduce di/dt effects.
8. By reducing the loading on the circuits that drive sensitive control lines such as CLOCK, CLEAR, PRESET, and LATCH ENABLE, noise immunity can be improved at these inputs.

Summary

Package lead inductance and other parasitics contribute to the noise induced in high-speed, high-drive integrated circuits. This noise gets worse if multiple outputs are switched simultaneously and can cause performance degradation. The system designer should be aware of the problems associated with high-speed switching and should carefully evaluate the application and system considerations.

Am29C800 POWER DISSIPATION CONSIDERATIONS

Introduction

CMOS bus interface devices (8, 9, and 10 bits wide) are rapidly invading the arena previously dominated by bipolar devices. This is because CMOS technology has made sufficient progress to provide an alternative to bipolar in terms of both high-speed and high-drive. In addition, at low data rates, CMOS devices offer much lower power dissipation when compared with their bipolar counterparts. However, there are some overzealous claims made with regard to this "power advantage." Statements such as "stingy CMOS consumes negligible power when driving high-speed buses" are too general and can be misleading. This report explains the basics of switching in CMOS circuits and provides guidelines for calculating power dissipation in CMOS parallel interface circuits.

Definition of Terms

$I_{CC(Q)}$ – Quiescent power supply current

$I_{CC(T)}$ – Power supply current component per input at TTL HIGH level

$I_{CC(D)}$ – Dynamic power supply current expressed in μA/MHz/bit

f – Equivalent toggle frequency at the output

C_L – Load capacitance per output

C_i – Lumped equivalent circuit capacitance per bit

Power Supply Current Components

A CMOS circuit operating in a TTL environment has three power supply current (I_{CC}) components. The total I_{CC}, when multiplied by V_{CC}, will determine the total power dissipated in the device.

The first component is the quiescent current $I_{CC(Q)}$. This is the leakage current through the device when all inputs are tied to either V_{CC} rail or GND, and all outputs are open (no load). This current is typically in the microamps region, and represents STAND-BY (or quiescent) power dissipation. Its contribution to the total power dissipation is insignificant at high data rates.

The second component is $I_{CC(T)}$, the current in TTL-compatible input stages. Because of the difference in threshold for N-channel and P-channel devices, each input stage offers a DC path from V_{CC} to GND. This I_{CC} component is a function of input voltage applied. Figure 2 shows a typical $I_{CC(T)}$ characteristic as a function of V_{IN}.

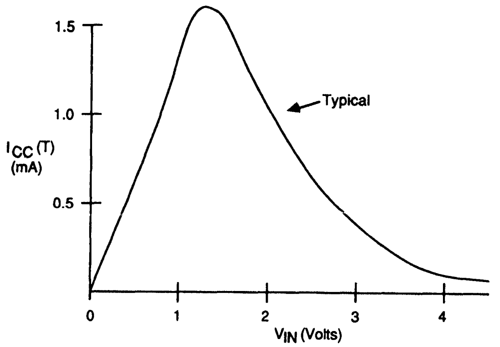


Figure 2. Typical $I_{CC(T)}$ as a Function of V_{IN}

Considering "realistic" worst-case conditions, $I_{CC(T)}$ is normally specified at $V_{IN} = 3.4$ V. Its value is given on a per input basis. To determine the total $I_{CC(T)}$ per device, one needs to know the number of inputs and the duty cycle for those inputs in HIGH state.

Note that the $I_{CC(T)}$ component applies to CMOS circuits operating in a TTL environment and driven by bipolar TTL circuits. In an all-CMOS environment, the driving signals (input signals) to such interface circuits will be close to V_{CC} rail or GND. In such cases $I_{CC(T)}$ is not applicable.

The third component is the dynamic power supply current — $I_{CC(D)}$. This current represents the power dissipated in the device in order to charge and discharge internal node capacitances in the device as well as any external load connected to the outputs. This component is a function of operating frequency and load capacitance, and dominates the total I_{CC} at high data rates. Therefore it is discussed in further detail in the following sections.

Back to Basics

Consider a simple buffer gate. Figure 3-1 shows the lumped equivalent capacitance of the circuit internal to the device. This capacitance C_i is charged rail-to-rail at frequency f. When the gate has load C_L at the output as shown in Figure 3-2, this load is also charged rail-to-rail.

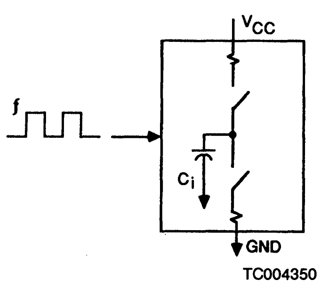


Figure 3-1. Unloaded Buffer

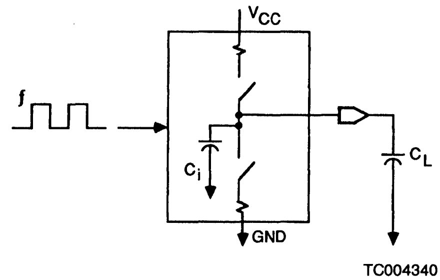


Figure 3-2. Buffer with Load C_L

Basic theory leads us to the equation $P = f\,CV_{CC}^2$ where P is the dynamic power dissipation in the gate. Since $P = IV_{CC}$ where I is the average current in the V_{CC} line, we get:

$$I = f\,CV_{CC} \quad \text{- - - - - - - (1)}$$

Equation (1) shows that there is a linear relationship between I and frequency. By obtaining values of I for different values of f, one can derive a normalized expression for current I per MHz. For the unloaded case, this equation is:

$$I_{CC(D)} = C_i\ V_{CC}\ \mu A/MHz/bit \quad \text{- - - - - (2)}$$

where V_{CC} is in volts and C_i is in pF. Equation (2) enables us to obtain the value of C_i per bit if $I_{CC(D)}$ is known at a given V_{CC}. For example, if $I_{CC(D)} = 200\ \mu A/MHz/bit$ at $V_{CC} = 5$ V, then:

$$C_i = 200/5 = 40\ pF/bit$$

If the output has a load C_L, it is effectively added to C_i, and $I_{CC(D)}$ will be higher as a result (see equation 2). If C_i is estimated, $I_{CC(D)}$ for a loaded case can be computed by using the formula:

$$I_{CC(D)}\ @\ C_L = I_{CC(D)}\ \frac{C_L + C_i}{C_i}$$

For the example just given,

$$I_{CC(D)}\ @\ 50\ pF = 200\ \frac{50 + 40}{40} = 450\ \mu A/MHz/bit$$

$$I_{CC(D)}\ @\ 300\ pF = 200\ \frac{300 + 40}{40} = 1.7\ mA/MHz/bit$$

To get a good feel for the numbers, consider a 10-bit buffer, with 300-pF load on each output, running at an "average" 5 MHz rate. The dynamic I_{CC} component will be:

$$I_{CC(D)} = 10\ \text{bits} \times 1.7\ mA/bit \times 5\ MHz = 85\ mA$$

The term "average" rate used in the example above needs some explanation. Since the dynamic I_{CC} is attributed to signal transitions, its value is highest when all outputs have a 1010... pattern at the data rate. However, such a pattern on a continuous basis is not realistic because it does not contain any information, except, of course, in a clock driver application. Therefore, to obtain a "realistic" worst-case $I_{CC(D)}$, one needs to estimate an average rate based on expected number of transitions. This average rate is lower than the data rate.

Total Power Supply Current (An Example)

For any given condition, the total I_{CC} is given by:

$$I_{CC}\ (\text{total}) = I_{CC(Q)} + I_{CC(T)} + I_{CC(D)}$$

Consider the following specification for the 10-bit buffer used in the last example:

$I_{CC(Q)}$		=	150 μA
$I_{CC(T)}$	— Data Inputs	=	1.5 mA/input @ 3.4 V
	— Control Inputs	=	3.0 mA/input @ 3.4 V
$I_{CC(D)}$	— Unloaded	=	0.2 mA/MHz/bit

To find the total I_{CC} at a data rate of 10 MHz (50% duty cycle) when all outputs have 50-pF load:

1. $I_{CC(Q)} = 0.15$ mA

2. $I_{CC(T)} = 10$ bits x 1.5 mA per bit x 0.5 = 7.5 mA*

* Control inputs (such as $\overline{OE}$) are assumed to be at logic LOW; therefore their contribution to $I_{CC(T)}$ is ignored.

3. $I_{CC(D)}$ @ 50 pF $= 0.2\ \dfrac{50 + 40}{40} = 0.45$ mA/MHz

(see example shown earlier)

Therefore:

$I_{CC(D)}$ for the device = 10 bits x 0.45 per bit x 10 MHz = 45 mA

Total $I_{CC} = 0.15 + 7.5 + 45 = 52.65$ mA

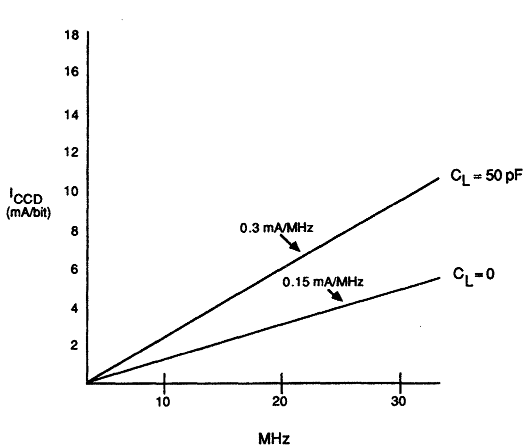
Summary

A system designer needs to consider all components of power supply current, and calculate the total I_{CC} based on the frequency of operation and loading. This is particularly important if CMOS parallel interface devices are used in high-speed bus applications.

Am29C800 TYPICAL I_{CCD} vs. FREQUENCY PLOTS

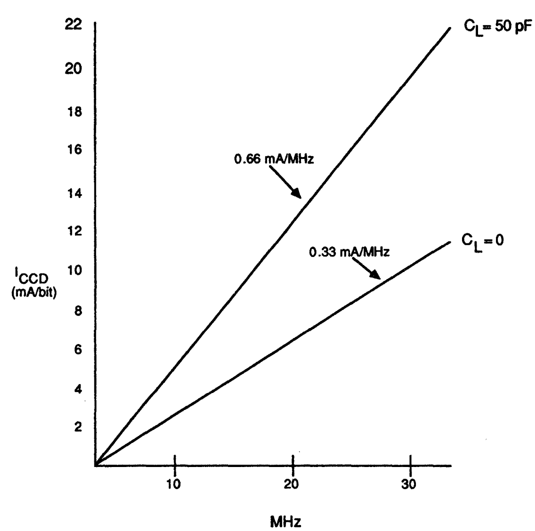
For CMOS devices, I_{CC} is very dependent on the frequency of operation. The graphs below show the increase in dynamic I_{CC} as frequency increases. These graphs represent typical performance over the V_{CC} and temperature operating ranges and are not included in production testing.

Am29C821/Am29C823
Am29C841/Am29C843
Am29C827/Am29C828



OP002470

Am29C861/Am29C863
Am29C833/Am29C853/Am29C855



OP002480

Am29C821/Am29C823
Am29C921/Am29C923

High-Performance CMOS Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y propagation delay = 8 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- I_{OL} = 24 mA, Commercial and Military
- Extra-wide (9- and 10-bit) data paths
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

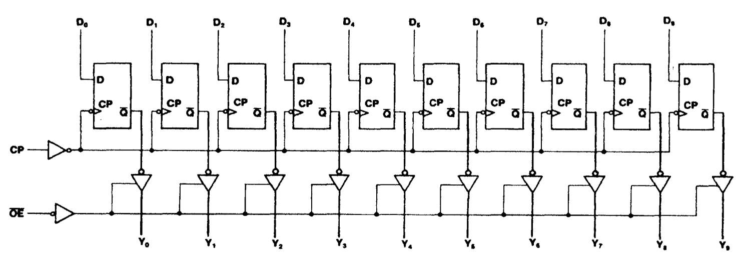
The Am29C821 and Am29C823 CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800 registers are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 8 ns, as well as an output current drive of 24 mA.

The Am29C821 is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823 is a 9-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821 and Am29C823 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS registers with this pinout are the Am29C921 and Am29C923; their pinouts are shown later in this data sheet.

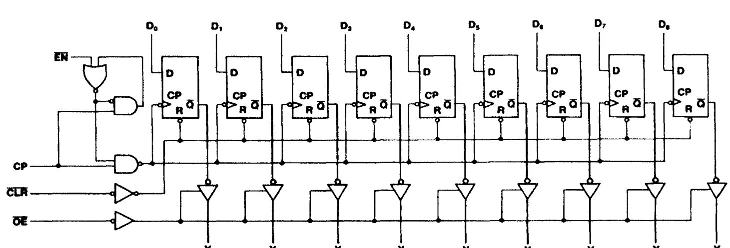
BLOCK DIAGRAMS

Am29C821



BD005471

Am29C823



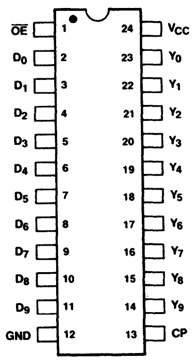
BD005481

Publication # 07135 Rev. C Amendment /0
Issue Date: January 1988

CONNECTION DIAGRAMS
Top View

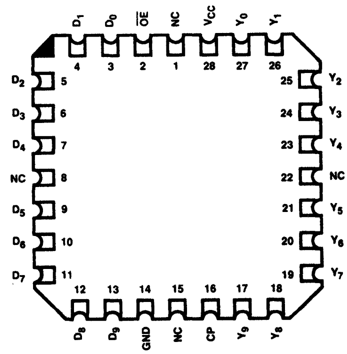
Am29C821

DIPs*



CD001360

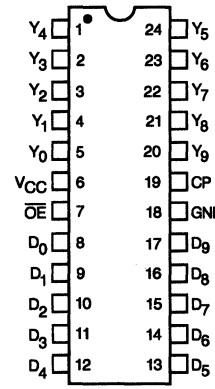
LCC**



CD001370

Am29C921

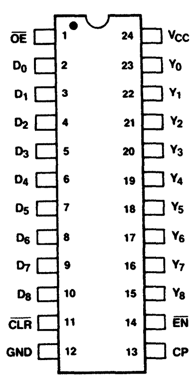
DIPs



CD010716

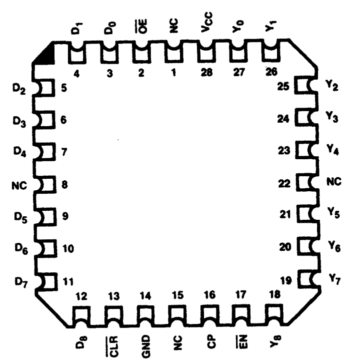
Am29C823

DIPs*



CD001220

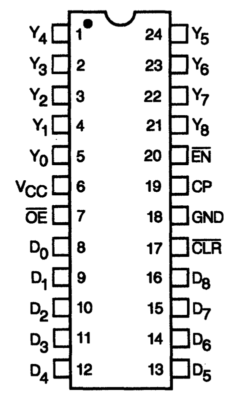
LCC**



CD001230

Am29C923

DIPs

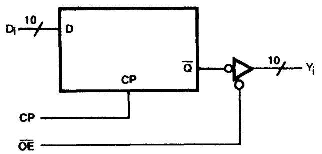


CD010717

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

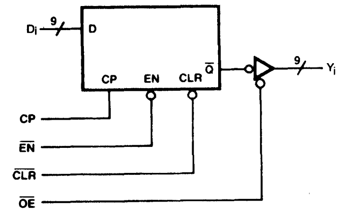
LOGIC SYMBOLS

Am29C821



LS000452

Am29C823



LS000432

FUNCTION TABLES

Am29C821

Inputs			Internal	Outputs	Function
$\overline{OE}$	D_i	CP	$\overline{Q_i}$	Y_i	
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Am29C823

Inputs					Internal	Outputs	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q_i}$	Y_i	
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C821 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commericial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C821 CMOS 10-Bit Register
Am29C823 CMOS 9-Bit Register
Am29C921 CMOS 10-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29C923 CMOS 9-Bit Register (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C821	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C823	
AM29C921	PC, PCB, DC, DCB, DE
AM29C923	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C821 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C821 CMOS 10-Bit Register
Am29C921 CMOS 10-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29C823 CMOS 9-Bit Register
Am29C923 CMOS 9-Bit Register (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C821	/BLA, /BKA, /B3A
AM29C823	
AM29C921	/BLA
AM29C923	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C821/Am29C823

D_i Data Input (Input)
D_i are the register data inputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

Y_i Data Outputs (Output)
Y_i are the three-state outputs.

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is present at the Y_i outputs.

Am29C823 only:

$\overline{EN}$ $\overline{\text{Clock Enable}}$ (Input, Active LOW)
When $\overline{EN}$ is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of the data or clock input transitions.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the $\overline{Q}_i$ outputs are HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Output Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output .... +50 mA
Out of Output .... −50 mA
DC Input Diode Current: Into Input .... +20 mA
Out of Input .... −20 mA
DC Output Current per Pin: I_{Sink} .... +48 mA (2 x I_{OL})
I_{Source} .... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	μA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{CLR}$, CP, $\overline{EN}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency $\leq$ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITHCING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)				12		14	ns
t_{PHL}					12		14	ns
t_S	Data to CP Setup Time			4		6		ns
t_H	Data to CP Hold Time			2		3		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			4		6		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		6		ns
t_H	Enable ($\overline{EN}$) Hold Time		$C_L = 50$ pF	2		3		ns
t_{PHL}	Propagation Delay, Clear to Y_i		$R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$		13		15	ns
t_{REC}	Clear ($\overline{CLR}$ ↑) to CP Setup Time			4		6		ns
t_{PWH}	Clock Pulse Width	HIGH		7		11		ns
t_{PWL}		LOW		7		11		ns
t_{PWL}	Clear Pulse Width	LOW		7		11		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i				12		14	ns
t_{ZL}					12		14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i				12		14	ns
t_{LZ}					12		14	ns

*See Test Circuit and Waveforms.

Am29C827/Am29C828
Am29C927/Am29C928

High-Performance CMOS Bus Buffers

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS buffers and inverters
  - D-Y delay = 7 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- I_{OL} = 24 mA, Commercial and Military
- 200-mV typical hysteresis on data input ports
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

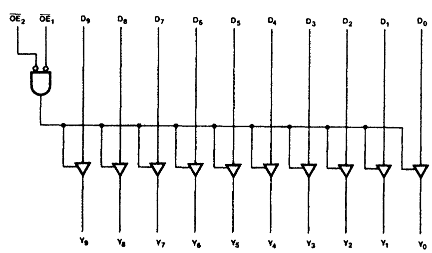
GENERAL DESCRIPTION

The Am29C827 and Am29C828 CMOS Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature 10-bit wide data paths and NORed output enables for maximum control flexibility. The Am29C827 has non-inverting outputs, while the Am29C828 has inverting outputs. Each device has data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C827 and Am29C828 are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 7 ns, as well as an output current drive of 24 mA.

The Am29C827 and Am29C828 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS buffers with this pinout are the Am29C927 and Am29C928; their pinouts are shown later in this data sheet.

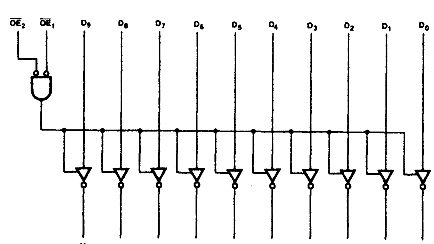
BLOCK DIAGRAMS

Am29C827 (Noninverting)



BD001092

Am29C828 (Inverting)



BD001093

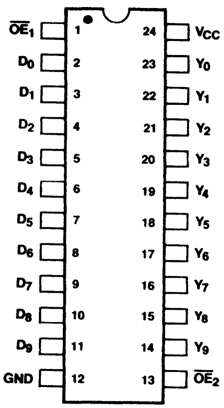
Publication #	Rev.	Amendment
05308	C	/0

Issue Date: **January 1988**

CONNECTION DIAGRAMS
Top View

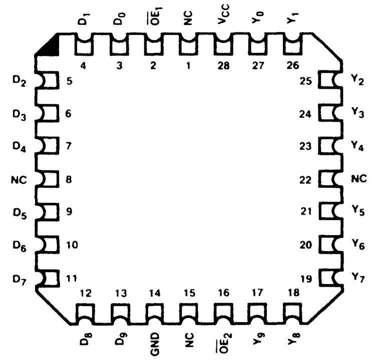
Am29C827/Am29C828

DIPs*



CD001170

LCC**

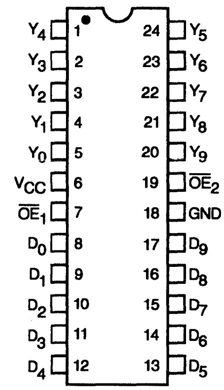


CD001393

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

Am29C927/ Am29C928

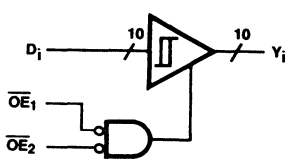
DIPs



CD010718

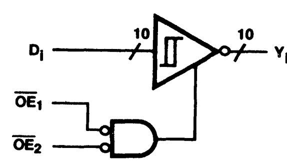
LOGIC SYMBOLS

Am29C827



LS000391

Am29C828



LS000393

FUNCTION TABLES

Am29C827

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

Am29C828

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = Hi-Z

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C827 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C827 CMOS 10-Bit Noninverting Buffer
Am29C828 CMOS 10-Bit Inverting Buffer
Am29C927 CMOS 10-Bit Noninverting Buffer (Center-V_{CC}-and-GND Pinout)
Am29C928 CMOS 10-Bit Inverting Buffer (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C827	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C828	
AM29C927	PC, PCB, DC, DCB, DE
AM29C928	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C827 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am27C827 CMOS 10-Bit Noninverting Buffer
Am29C828 CMOS 10-Bit Inverting Buffer
Am29C927 CMOS 10-Bit Noninverting Buffer (Center-V_{CC}-and-GND Pinout)
Am29C928 CMOS 10-Bit Inverting Buffer (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C827	/BLA, /BKA, /B3A
AM29C828	/BLA, /BKA, /B3A
AM29C927	/BLA
AM29C928	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$\overline{OE}_i$ Output Enables (Input, Active LOW)
When $\overline{OE}_1$ and $\overline{OE}_2$ are both LOW, the outputs are enabled. When either one or both are HIGH, the outputs are in the Hi-Z state.

D_i Data Inputs (Input)
D_i are the 10-bit data inputs.

Y_i Data Output (Output)
Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Output Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output .... +50 mA
Out of Output .... −50 mA
DC Input Diode Current: Into Input .... +20 mA
Out of Input .... −20 mA
DC Output Current per Pin:
I_{SINK} .... +48 mA (2 x I_{OL})
I_{SOURCE} .... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	μA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}_1$, $\overline{OE}_2$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i) Am29C827 (Noninverting)	$C_L = 50$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$		10		12	ns
t_{PHL}				10		12	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29C828 (Inverting)			10		12	ns
t_{PHL}				10		12	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i			13		15	ns
t_{ZL}				13		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i			13		15	ns
t_{LZ}				13		15	ns

*See Test Circuit and Waveforms.

Am29C833/Am29C853/Am29C855
Am29C933/Am29C953/Am29C955

High-Performance CMOS Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 6 ns typical
  - R-Parity delay = 9 ns typical
- Error flag with open-drain output
- Generates odd parity for all-zero protection
- Low standby power
- Am29C855 adds new functionality
- 200-mV typical input hysteresis on input data ports
- I_{OL} = 24 mA, Commercial and Military
- JEDEC FCT-compatible specs
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

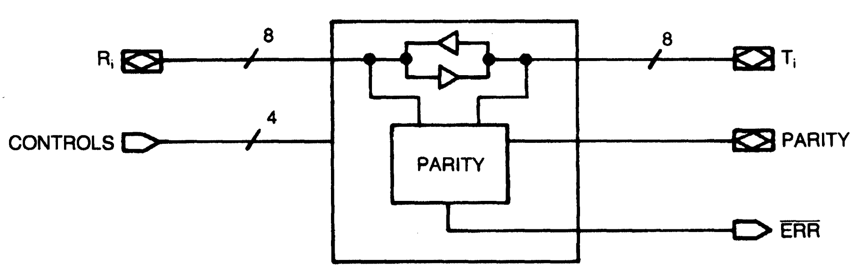
The Am29C833, Am29C853, and Am29C855 are high-performance CMOS parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with the $\overline{ERR}$ flag showing the results of the parity test. Each of these devices is produced with AMD's exclusive CS-11 CMOS process, and features a typical propagation delay of 6 ns, as well as an output current drive of 24 mA.

In the Am29C833, the error flag is clocked and stored in a register which is read at the open-drain $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29C853, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29C853 and Am29C833, parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port. The Am29C855, a variation of the Am29C853, is designed so that when both output enables are HIGH, the $\overline{ERR}$ pin retains its current state.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29C833, Am29C853, and Am29C855 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS parity transceivers with this pinout are the Am29C933, Am29C953, and Am29C955; their pinouts are shown later in this data sheet.

SIMPLIFIED BLOCK DIAGRAM

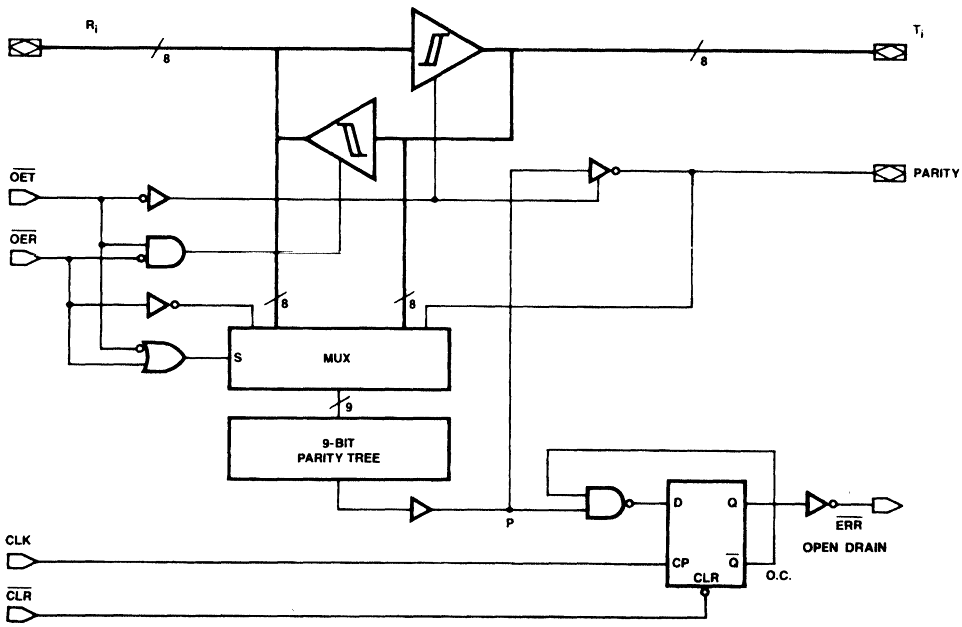


BD005541

Publication # 07323 Rev. B Amendment /0
Issue Date: January 1988

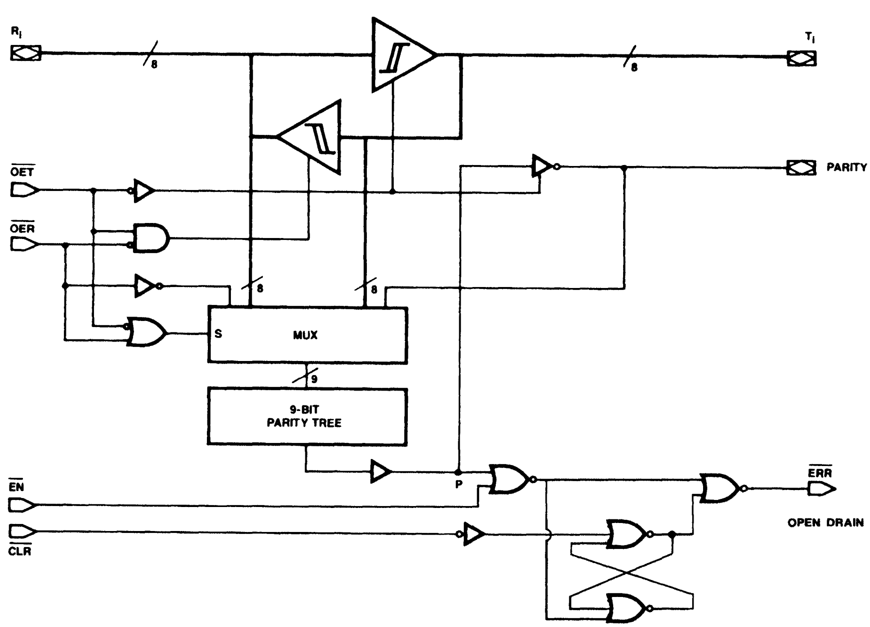
BLOCK DIAGRAMS*

Am29C833



BD001044

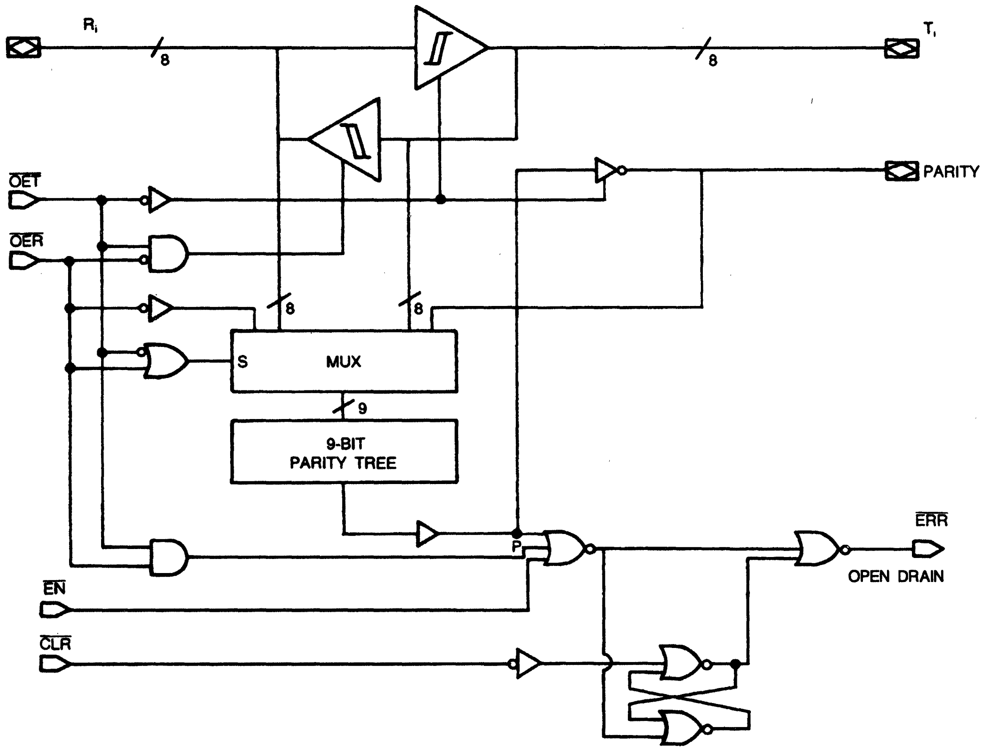
Am29C853



BD001035

BLOCK DIAGRAMS (Cont'd.)

Am29C855

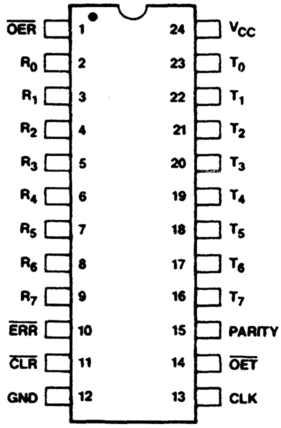


BD005562

CONNECTION DIAGRAMS
Top View

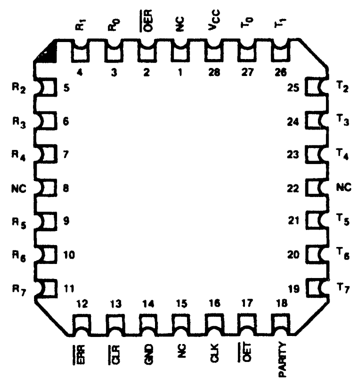
Am29C833

DIPs*



CD001120

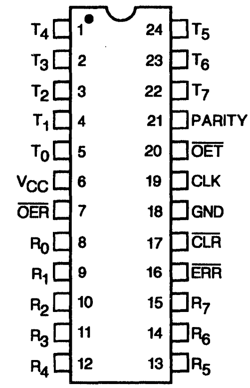
LCC**



CD001398

Am29C933

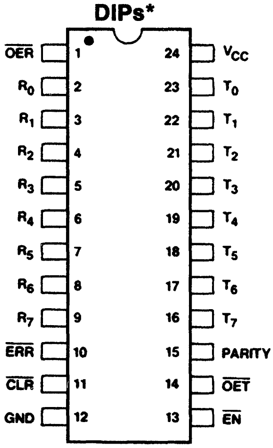
DIPs



CD010714

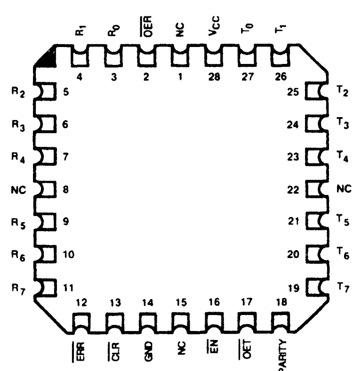
Am29C853/Am29C855

DIPs*



CD001130

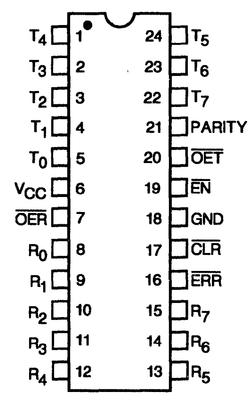
LCC**



CD001399

Am29C953/Am29C955

DIPs



CD010715

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

FUNCTION TABLES

Am29C833 (Register Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition of Clock
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE

Error Flag Output

Am29C833

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FUNCTION TABLES (Cont'd.)

Am29C853 (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

Am29C855 (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = HIGH
L = LOW
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE
Error Flag Output

Am29C853/Am29C855

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's Capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C833 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C833 CMOS Parity Bus Transceiver — Register Option
Am29C853 CMOS Parity Bus Transceiver — Latch Option
Am29C855 CMOS Parity Bus Transceiver — Latch Option
Am29C933 CMOS Parity Bus Transceiver — Register Option (Center-V_{CC}-and-GND Pinout)
Am29C953 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)
Am29C955 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C833	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C853	
AM29C855	
AM29C933	PC, PCB, DC, DCB, DE
AM29C953	
AM29C955	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C833 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C833 CMOS Parity Bus Transceiver — Register Option
Am29C853 CMOS Parity Bus Transceiver — Latch Option
Am29C855 CMOS Parity Bus Transceiver — Latch Option
Am29C933 CMOS Parity Bus Transceiver — Register Option (Center-V_{CC}-and-GND Pinout)
Am29C953 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)
Am29C955 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C833	/BLA, /BKA, /B3A
AM29C853	
AM29C855	
AM29C933	/BLA
AM29C953	
AM29C955	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C833/Am29C853/Am29C855

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i Receive Port (Input/Output, Three-State)
R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output, Three-State)
T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity Parity Flag (Input/Output, Three-State)
In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29C833 Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK Clock (Input, Positive Edge-Triggered)
This pin is the clock input for the Error Flag register.

Am29C853/Am29C855 Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared. In the Am29C855, the error flag will retain its previous state when $\overline{OET}$ and $\overline{OER}$ are HIGH.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW and $\overline{EN}$ is HIGH, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$ Latch Enable (Input, Active LOW)
This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Output Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output .... +50 mA
Out of Output .... −50 mA
DC Input Diode Current: Into Input .... +20 mA
Out of Input .... −20 mA
DC Output Current per Pin: I_{SINK} .... +48 mA (2 x I_{OL})
I_{SOURCE} ..... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage .... +4.5 V to +5.5 V
Military (M) Devices
Temperature (T_A) .... −55 to +125°C
Supply Voltage .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage (Note 2)	Am29C853 Am29C855	All Inputs	2.0		V
			Am29C833	$\overline{CLR}$	3.0		V
				Remaining Inputs	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0.0 V			−10	µA
			V_{IN} = 0.4 V			−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 2.7 V			5	µA
			V_{IN} = 5.5 V			10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V			15	µA
			V_{OUT} = 5.5 V			20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V			−15	µA
			V_{OUT} = 0.0 V			−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_0 = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	µA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	R_i, T_i, Parity		3.0	mA/Bit
				$\overline{CLR}$, $\overline{EN}$, $\overline{OET}$, $\overline{OER}$		1.5	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)				400	µA/Bit/MHz

Notes: 1. n = number outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		$C_L = 50$ pF, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$		15		18	ns
t_{PHL}					15		18	ns
t_{PLH}	Propagation Delay R_i to Parity				19		23	ns
t_{PHL}					19		23	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity				15		18	ns
t_{ZL}					15		18	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity				15		18	ns
t_{LZ}					15		18	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			18		21		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		2		ns
t_{REC}	Clear ($\overline{CLR}$ ⌐) to CLK Setup Time (Note 2)			15		18		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		6		9		ns
t_{PWL}		LOW		6		9		ns
t_{PWL}	Clear Pulse Width	LOW		6		9		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				15		18	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				20		23	ns
t_{PLH}	Propagation-Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29C853/854				29		33	ns
t_{PHL}					25		28	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				22		25	ns
t_{PHL}					22		25	ns

*See test circuit and waveforms.

Notes: 1. For Am29C853/Am29C855, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833.

Am29C841/Am29C843
Am29C941/Am29C943

High-Performance CMOS Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - D-Y propagation delay = 7 ns typical
- Low standby power
- I_{OL} = 24 mA, Commercial and Military
- JEDEC FCT-compatible specs
- Extra-wide (9- and 10-bit) data paths
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

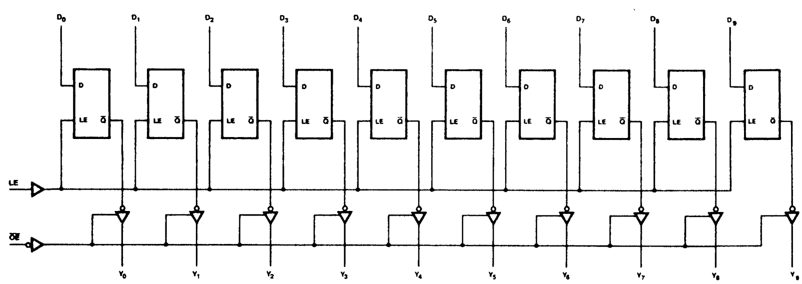
The Am29C841 and Am29C843 CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800 latches are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 7 ns, as well as an output current drive of 24 mA.

The Am29C841 is a buffered, 10-bit version of the popular '373 function. The Am29C843 is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C841 and Am29C843 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS latches with this pinout are the Am29C941 and Am29C943; their pinouts are shown later in this data sheet.

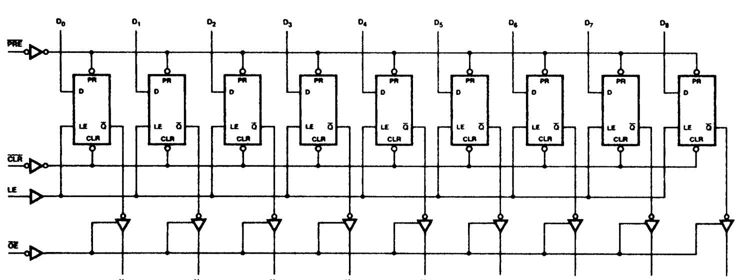
BLOCK DIAGRAMS

Am29C841



BD001054

Am29C843



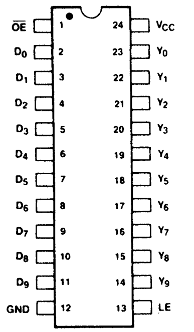
BD001055

Publication #	Rev.	Amendment
07137	C	/0
Issue Date: January 1988		

CONNECTION DIAGRAMS
Top View

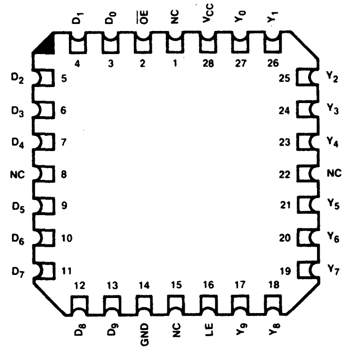
Am29C841

DIPs*



CD001380

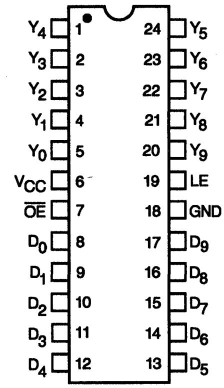
LCC**



CD001390

Am29C941

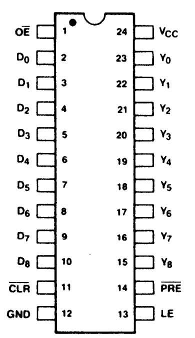
DIPs



CD010712

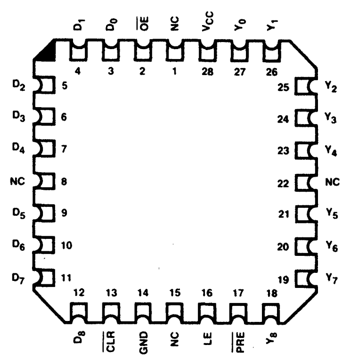
Am29C843

DIPs*



CD001400

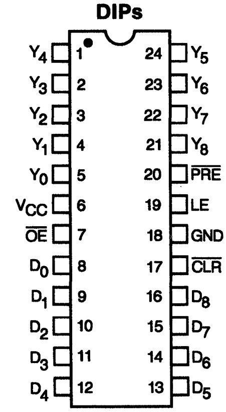
LCC**



CD001410

Am29C943

DIPs

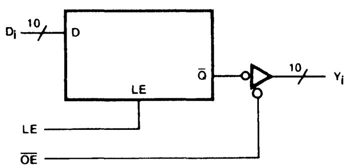


CD010713

*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

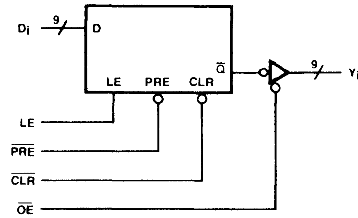
LOGIC SYMBOLS

Am29C841



LS000463

Am29C843



LS000473

FUNCTION TABLES

Am29C841

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C841 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C841 CMOS 10-Bit Latch
Am29C843 CMOS 9-Bit Latch
Am29C941 CMOS 10-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29C943 CMOS 9-Bit Latch (Center-V_{CC}-and-GND Pinout)

<table>
<tr><th colspan="2">Valid Combinations</th></tr>
<tr><td>AM29C841</td><td rowspan="2">PC, PCB, DC, DCB, DE, SC, JC, LC</td></tr>
<tr><td>AM29C843</td></tr>
<tr><td>AM29C941</td><td rowspan="2">PC, PCB, DC, DCB, DE</td></tr>
<tr><td>AM29C943</td></tr>
</table>

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C841 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C841 CMOS 10-Bit Latch
Am29C843 CMOS 9-Bit Latch
Am29C941 CMOS 10-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29C943 CMOS 9-Bit Latch (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C841	/BLA, /BKA, /B3A
AM29C843	
AM29C941	/BLA
AM29C943	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C841/Am29C843

D_i Data Inputs (Input)
D_i are the latch data inputs.

Y_i Data Outputs (Output)
Y_i are the three state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedance state.

Am29C843 Only

$\overline{PRE}$ $\overline{\text{Preset}}$ (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Output Voltage...................... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage..................... −0.5 V to +V_{CC} + 0.5 V
DC Output Diode Current: Into Output.............. +50 mA
Out of Output .... −50 mA
DC Input Diode Current: Into Input.................. +20 mA
Out of Input .... −20 mA
DC Output Current per Pin: I_{SINK}.......... +48 mA (2 x I_{OL})
I_{SOURCE}..... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A)................................. 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A)............................ −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	μA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{PRE}$, $\overline{CLR}$, LE		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency $\leqslant$ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		11		14	ns
t_{PHL}					11		14	ns
t_S	Data to LE Setup Time			3		3		ns
t_H	Data to LE Hold Time			4		4		ns
t_{PLH}	Latch Enable (LE) to Y_i				12		14	ns
t_{PHL}					12		14	ns
t_{PLH}	Propagation Delay, Preset to Y_i				13		15	ns
t_{PHL}					13		15	ns
t_{REC}	Preset ($\overline{PRE}$ ↑) to LE Setup Time			4		4		ns
t_{PLH}	Propagation Delay, Clear to Y_i				12		14	ns
t_{PHL}					12		14	ns
t_{REC}	Clear ($\overline{CLR}$ ↑) to LE Setup Time			3		3		ns
t_{PWH}	LE Pulse Width	HIGH		6		9		ns
t_{PWL}	Preset Pulse Width	LOW		8		12		ns
t_{PWL}	Clear Pulse Width	LOW		8		12		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i				12		14	ns
t_{ZL}					12		14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i				12		14	ns
t_{LZ}					12		14	ns

*See Test Circuit and Waveforms.

Am29C861/Am29C863
Am29C961/Am29C963

High-Performance CMOS Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 7 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- I_{OL} = 24 mA, Commercial and Military
- 200-mV typical hysteresis on data input ports
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

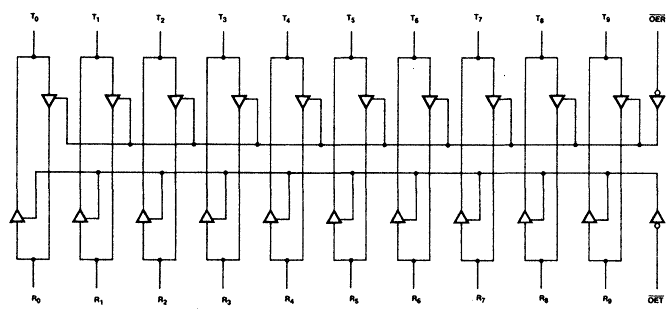
GENERAL DESCRIPTION

The Am29C861 and Am29C863 CMOS Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29C861 is a 10-bit bidirectional transceiver; the Am29C863 is a 9-bit transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C861 and Am29C863 are produced with AMD's exclusive CS-11 CMOS process, and features a typical propagation delay of 7 ns, as well as an output current drive of 24 mA.

The Am29C861 and Am29C863 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS transceivers with this pinout are the Am29C961 and Am29C963; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS

Am29C861



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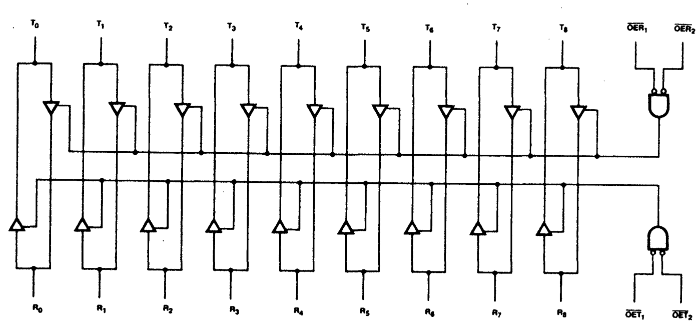
Am29C863



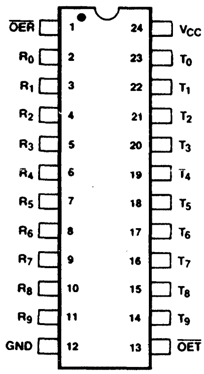
BD001070

Publication # 07324 Rev. C Amendment /0
Issue Date: January 1988

CONNECTION DIAGRAMS
Top View

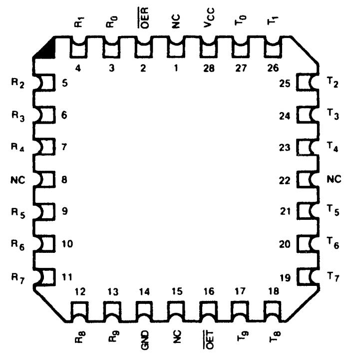
Am29C861

DIPs*



CD001150

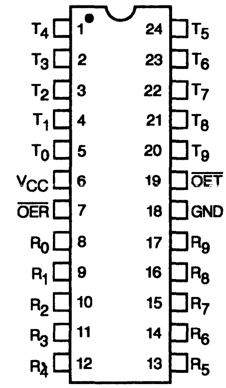
LCC**



CD010810

Am29C961

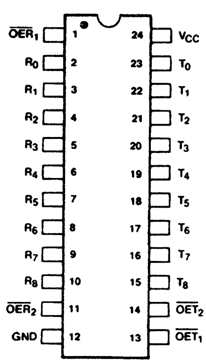
DIPs



CD010710

Am29C863

DIPs*



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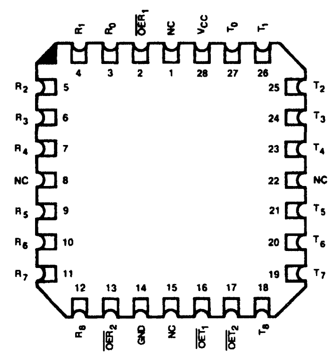
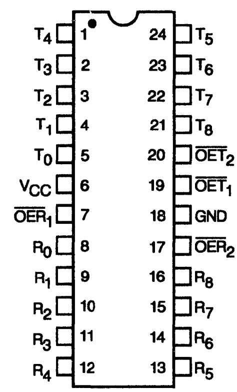
LCC**



CD001397

Am29C963

DIPs



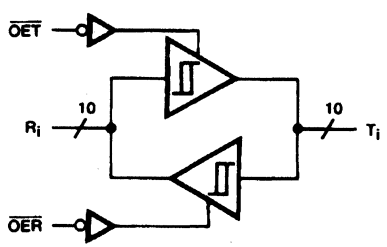
CD010711

*Also available in 24-Pin Flatpack and Small Outline Package; pinout identical to DIPs.

**Also available in 28-Pin PLCC; pinout identical to LCC.

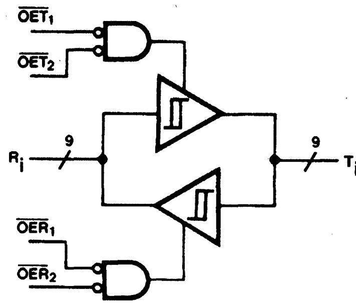
LOGIC SYMBOLS

Am29C861



LS000372

Am29C863



LS000382

FUNCTION TABLES

Am29C861

Inputs				Outputs		Function
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29C863

Inputs						Outputs		Function
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_i	T_i	R_i	T_i	
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C861 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C861 CMOS 10-Bit Transceiver
Am29C863 CMOS 9-Bit Transceiver
Am29C961 CMOS 10-Bit Transceiver (Center-V_{CC}-and-GND Pinout)
Am29C963 CMOS 9-Bit Transceiver (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C861	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C863	
AM29C961	PC, PCB, DC, DCB, DE
AM29C963	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C861 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C861 CMOS 10-Bit Transeiver
Am29C863 CMOS 9-Bit Transceiver
Am29C961 CMOS 10-Bit Transceiver (Center-V_{CC}-and-GND Pinout)
Am29C963 CMOS 9-Bit Transceiver (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C861	/BLA, /BKA, /B3A
AM29C863	
AM29C961	/BLA
AM29C963	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C861

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_i Receive Port (Input/Output)
R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29C863

$\overline{OER}_i$ Output Enables-Receive (Input, Active LOW)
When both $\overline{OER}_1$ and $\overline{OER}_2$ are LOW while $\overline{OET}_1$ or $\overline{OET}_2$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}_i$ Output Enables-Transmit (Input, Active LOW)
When both $\overline{OET}_1$ and $\overline{OET}_2$ are LOW while $\overline{OER}_1$ or $\overline{OER}_2$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_i Receive Port (Input/Output)
R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Output Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output .... +50 mA
Out of Output .... −50 mA
DC Input Diode Current: Into Input .... +20 mA
Out of Input .... −20 mA
DC Output Current per Pin: I_{SINK} .... +48 mA (2 x I_{OL})
I_{SOURCE} ..... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0.0 V			−10	μA
			V_{IN} = 0.4 V			−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 2.7 V			5	μA
			V_{IN} = 5.5 V			10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V			15	μA
			V_{OUT} = 5.5 V			20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V			−15	μA
			V_{OUT} = 0.0 V			−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_0 = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	μA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OER_1}$, $\overline{OER_2}$, $\overline{OET_1}$, $\overline{OET_2}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)				400	μA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861A/Am29863A (Non-inverting)	$C_L = 50$ pF, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$		10		12	ns
t_{PHL}				10		12	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			14		16	ns
t_{ZL}				14		16	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			14		16	ns
t_{LZ}				14		16	ns

*See Test Circuit and Waveforms.

Am29C818

CMOS Pipeline Register with SSR™ Diagnostics

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed noninverting 8-bit parallel register for any data path or pipelining application
- WCS (Writable Control Store) pipeline register
  - Load WCS from serial register
  - Read WCS via serial scan
- Alternate sourced as SN74ACT818
- High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- Low standby power

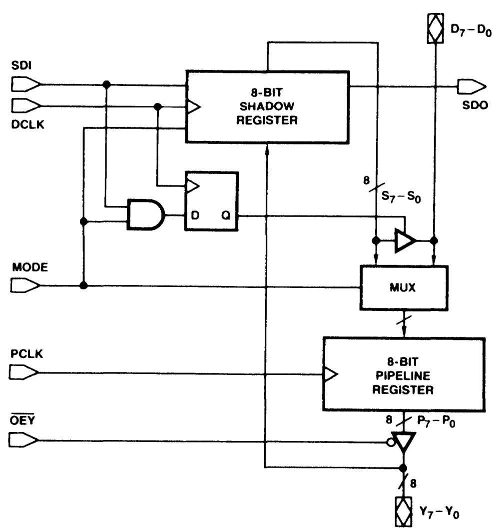
GENERAL DESCRIPTION

The Am29C818 is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for *normal* system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a shift register. In the serial shift mode, SDI is shifted into the '0' location of the Shadow register and the contents of '7' location appear at the SDO output. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29C818 Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM



BD001020

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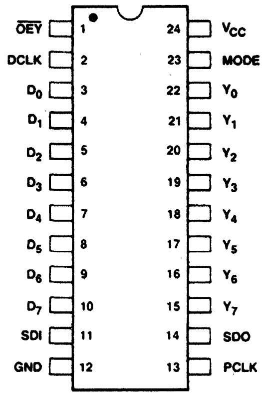
Publication #	Rev.	Amendment
09323	B	/0

Issue Date: **January 1988**

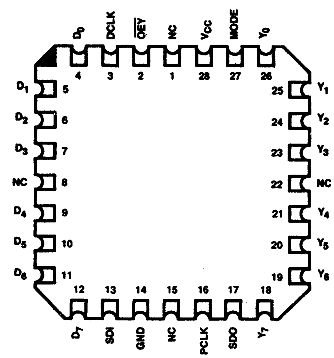
CONNECTION DIAGRAMS
Top View

DIPs*



CD001102

LCC**



CD001160

*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.

**Also available in 28-Pin PLCC; pinout identical to LCC.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C818 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)
S = 24-Pin Plastic Small Outline Package (SO 024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C818
CMOS Pipeline Register with SSR Diagnostics

Valid Combinations	
AM29C818	PC, PCB, DC, DCB, DE, SC, JC, LC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C818 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C818
CMOS Pipeline Register with SSR Diagnostics

Valid Combinations	
AM29C818	/BLA, /BKA, /B3A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$D_0 - D_7$ Parallel Data Inputs (Input/Output)
Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK Diagnostics Clock (Input)
Diagnostics/WCS clock for loading shadow register (serial or parallel modes — see Function Table).

MODE Mode Control (Input)
Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$ Y-Port Output Enable (Input: Active LOW)
Active LOW output enable for Y-port.

PCLK Pipeline Register Clock (Input)
Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI Serial Data Input (Input)
Input to shadow register (see Function Table).

SDO Serial Data Input (Output)
Output from shadow register.

$Y_0 - Y_7$ Parallel Data Outputs (Input/Output)
Data outputs from the pipeline register and parallel inputs to the shadow register.

FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no setup or hold times are violated, this simultaneous operation is legal.

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_0 \leftarrow SDI$	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	SDI	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	X	SDI	Hold*	NA	Hold Shadow Register; $D_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

FUNCTION TABLE DEFINITIONS

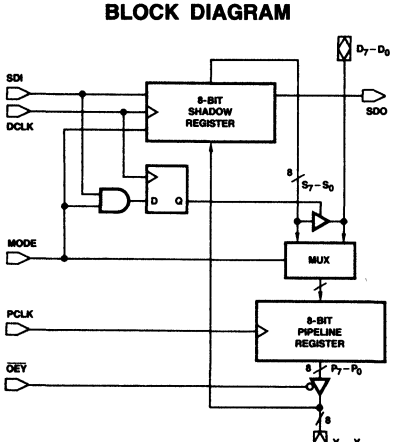
INPUTS

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition

OUTPUTS

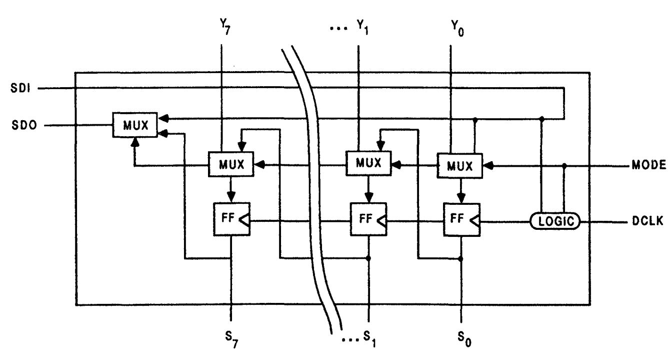
$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable output is not a function of the specified input combinations.

BLOCK DIAGRAM



BD001020

SHADOW REGISTER



BD006770

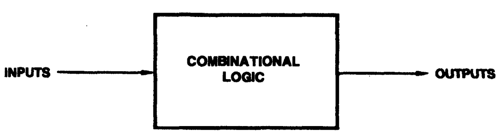
An Introduction to Serial Shadow Register (SSR) Diagnostics

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals - address, data, control and status - to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.



DF000071

Figure 1. Combinational Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

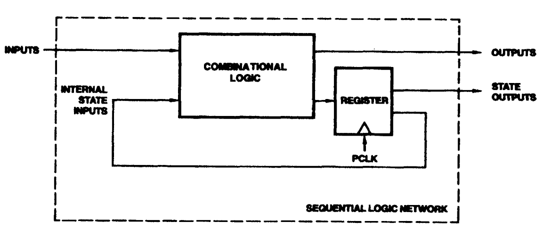


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Figure 2. Sequential Network

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.

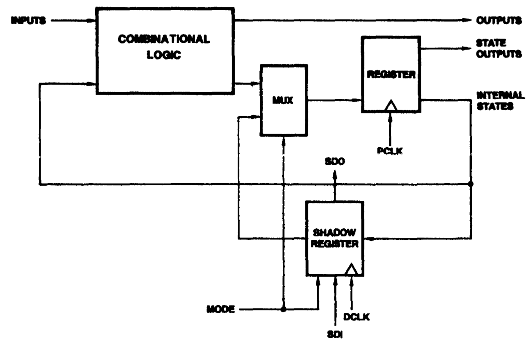

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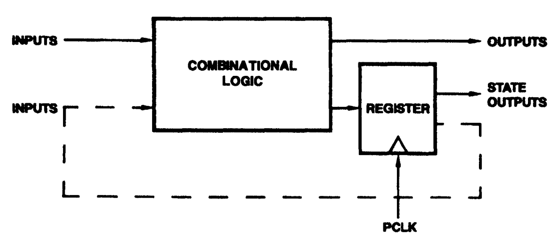
Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.



DF000051

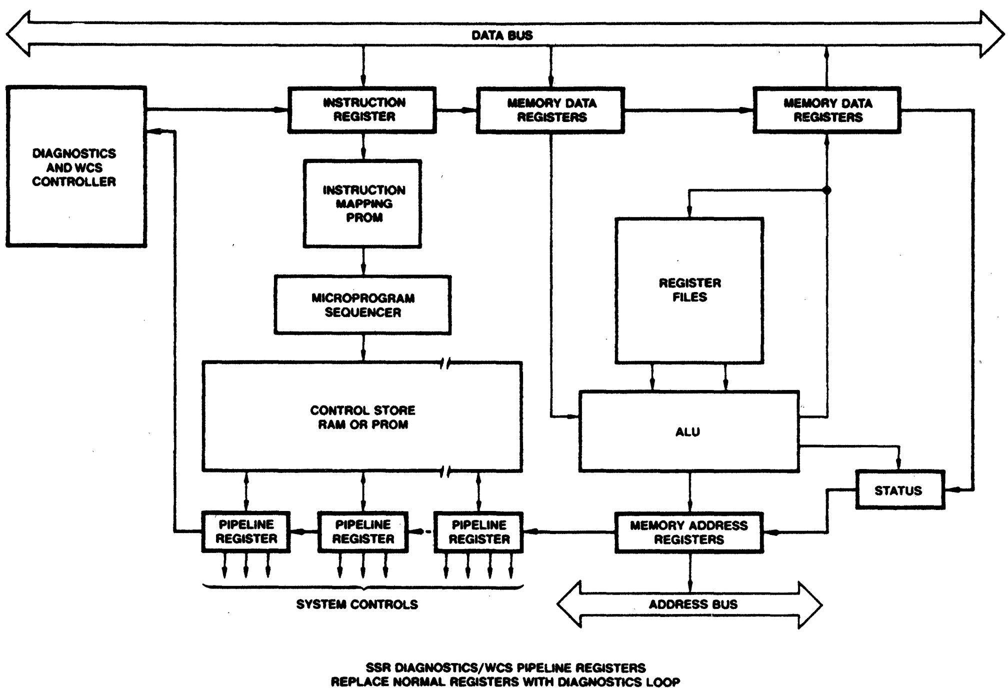
Figure 4. SSR Diagnostics Logical Path

A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29C818.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29C818's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.



DF000030

Figure 5. Typical System Configuration

Use of the Am29C818 Pipeline Register in Writable Control Store (WCS) Designs

The Am29C818 SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29C818 supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29C818. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinational network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.

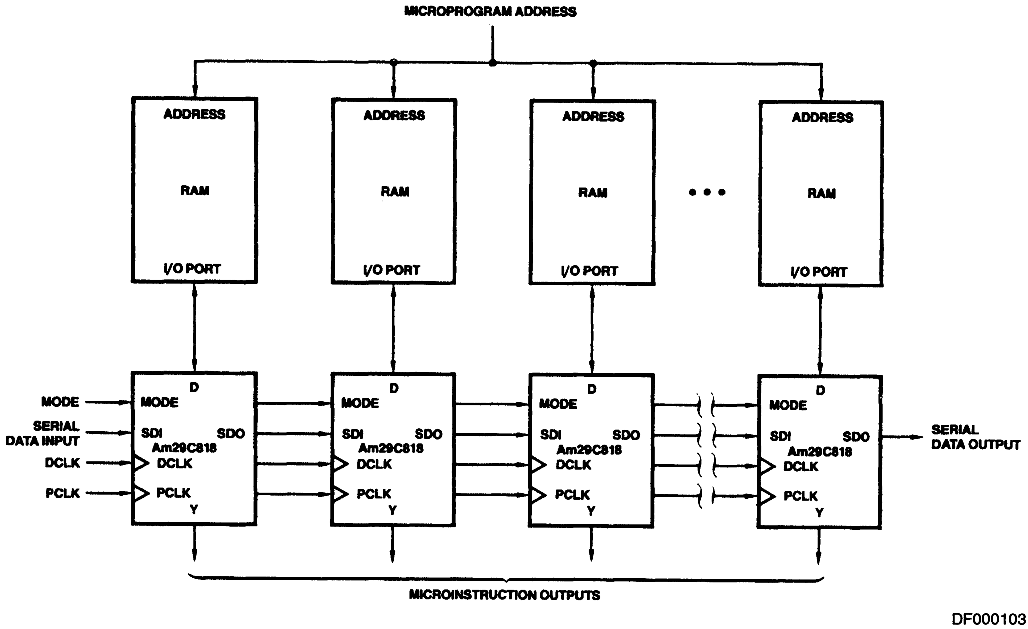


Figure 6. Am29C818-Based WCS Application

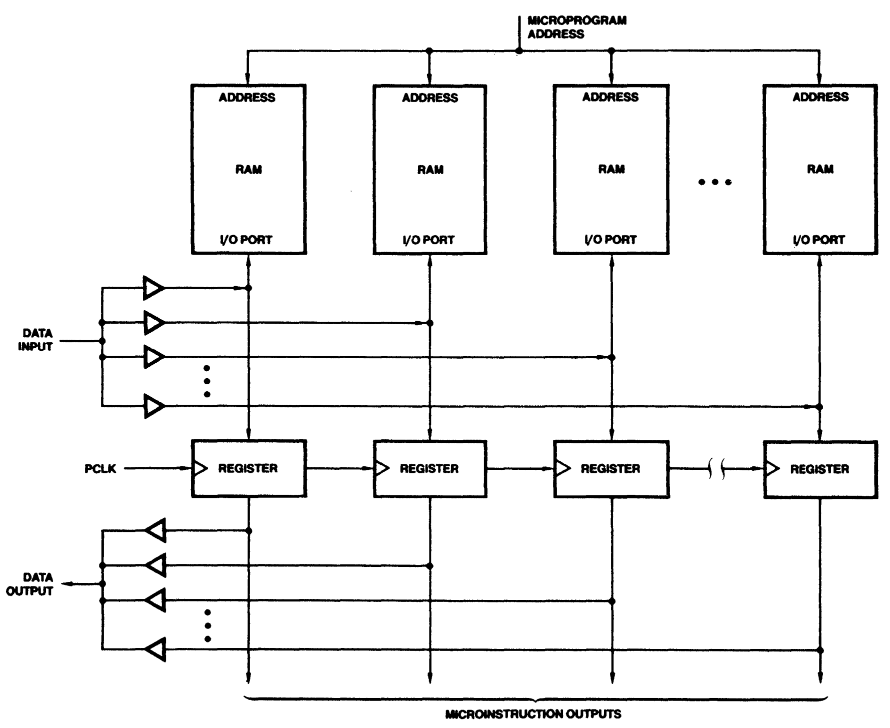


Figure 7. WCS Application without Am29C818s

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....−65°C to +150°C
Supply Voltage to Ground Potential
Continuous ....−0.5 V to +7.0 V
DC Output Voltage.....................−0.5 V to V_{CC} +0.5 V
DC Input Voltage.......................−0.5 V to V_{CC} +0.5 V
DC Output Diode Current: Into Output.............. +50 mA
Out of Output ....−50 mA
DC Input Diode Current: Into Input .... +20 mA
Out of Input ....−20 mA
DC Output Current per Pin: I_{SINK}..........+48 mA (2 x I_{OL})
I_{SOURCE}.....−30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A).................................0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A)............................−55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	μA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	μA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 2.4 V			15	μA
			V_O = V_{CC}			20	
I_{OZL}		V_{CC} = 5.5 V	V_O = 0.4 V			−15	μA
			V_O = GND			−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL			μA
				COM'L			
I_{CCT}			V_{IN} = 3.4 V				mA/Bit
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)					μA/ MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ⩽ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH} and t_{PHL}	PCLK → Y_X	See Test Output Load Conditions		12		14	ns
	MODE → SDO			12		14	ns
	SDI → SDO			12		14	ns
	DCLK → SDO			12		14	ns
t_S	D_X → PCLK		4		6		ns
	MODE → PCLK		6		8		ns
	Y_X → DCLK		6		8		ns
	MODE → DCLK		6		8		ns
	SDI → DCLK		6		8		ns
	DCLK → PCLK		20		20		ns
	PCLK → DCLK		20		20		ns
t_H	D_X → PCLK		2		2		ns
	MODE → PCLK		2		2		ns
	Y_X → DCLK		2		2		ns
	MODE → DCLK		2		2		ns
	SDI → DCLK		2		2		ns
t_{LZ}	$\overline{OEY}$ → Y_X			12		14	ns
	DCLK → D_X			14		16	ns
t_{HZ}	$\overline{OEY}$ → Y_X			12		14	ns
	DCLK → D_X			14		16	ns
t_{ZL}	$\overline{OEY}$ → Y_X			14		16	ns
	DCLK → D_X			18		20	ns
t_{ZH}	$\overline{OEY}$ → Y_X			14		16	ns
	DCLK → D_X			18		20	ns
t_{PW}	PCLK (HIGH and LOW)		8		10		ns
	DCLK (HIGH and LOW)		8		10		ns

Am29821A/Am29823A/Am29825A
Am29921A/Am29923A/Am29925A

High-Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y $t_{PD} = 6$ ns typical
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL}: 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29821, Am29823, & Am29825
- Am29900A DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

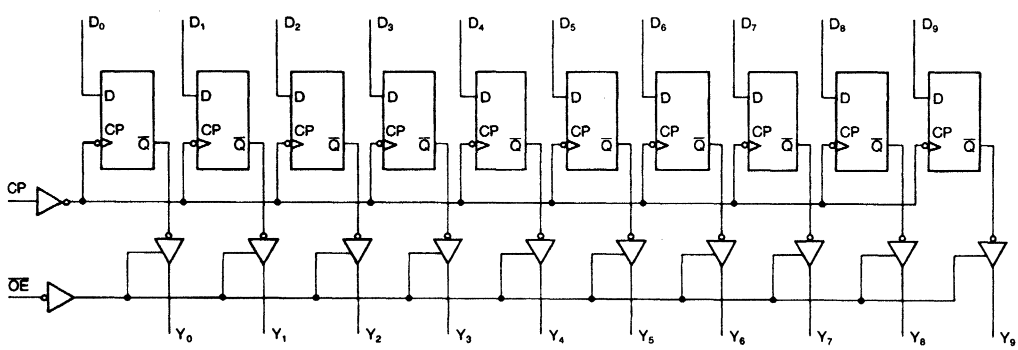
The Am29821A, Am29823A, and Am29825A Buffered Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for address/data paths or buses carrying parity. The Am29800A registers are produced with AMD's exclusive IMOX* bipolar process, and feature typical propagation delays of 6 ns, as well as high-capacitive drive capability.

The Am29821A is a buffered, 10-bit version of the popular '374/'534 functions. The Am29823A is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The Am29825A, an 8-bit buffered register, has all the 9-bit controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multi-user control of the interface; e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The device is ideal for use as an output port requiring high I_{OL}/I_{OH}.

The Am29800A registers are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for registers with this pinout are the Am29921A, Am29923A, and Am29925A; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS**

Am29821A



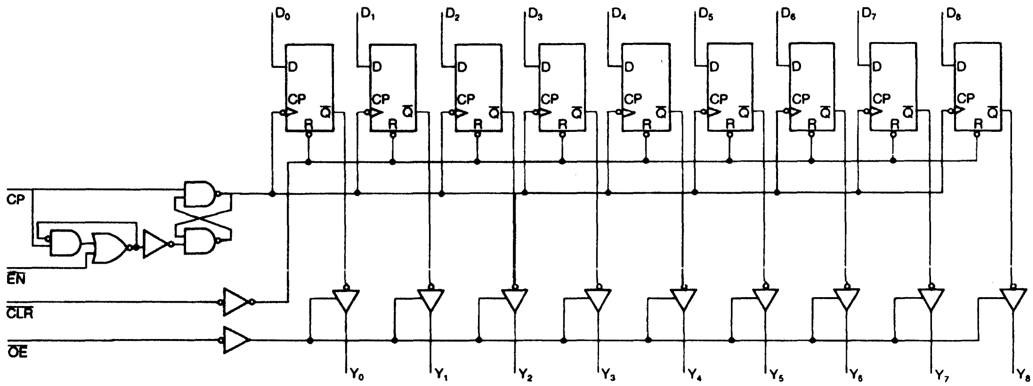
BD005501

*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following page for additional Block Diagrams.

Publication # 07138 Rev. C Amendment /0
Issue Date: January 1988

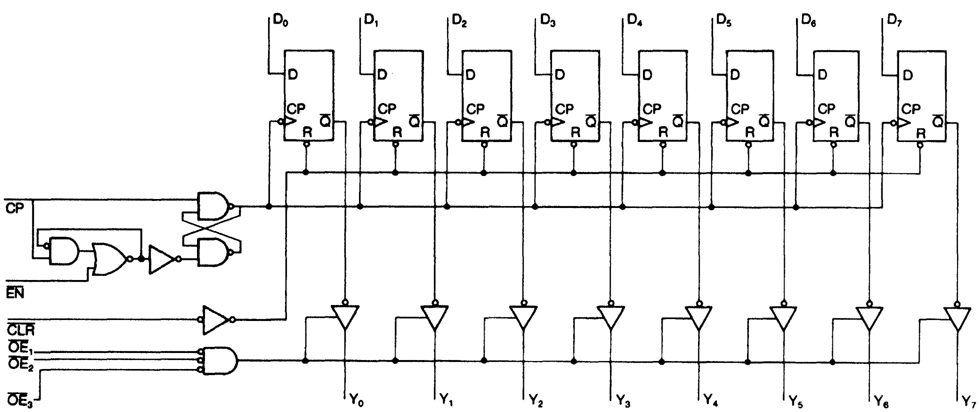
BLOCK DIAGRAMS (Cont'd.)

Am29823A



BD005512

Am29825A

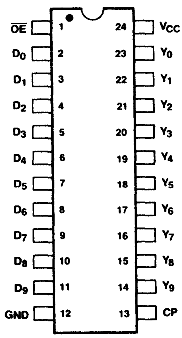


BD005522

CONNECTION DIAGRAMS
Top View

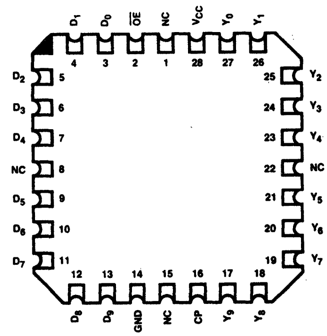
Am29821A

DIPs*



CD001360

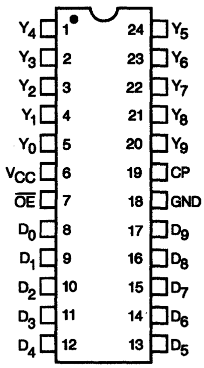
LCC**



CD001370

Am29921A

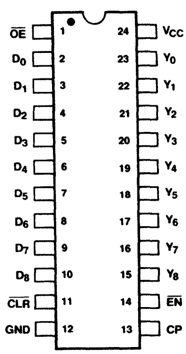
DIPs



CD010719

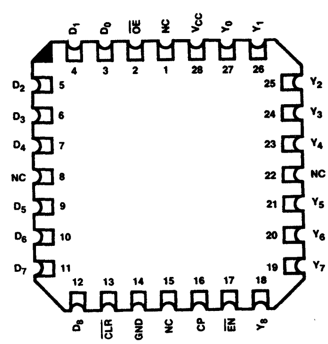
Am29823A

DIPs*



CD001220

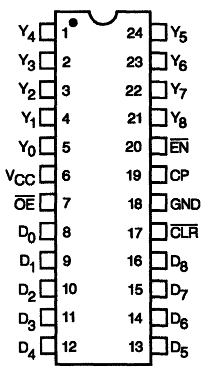
LCC**



CD001230

Am29923A

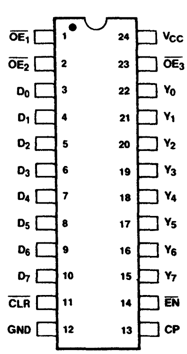
DIPs



CD010720

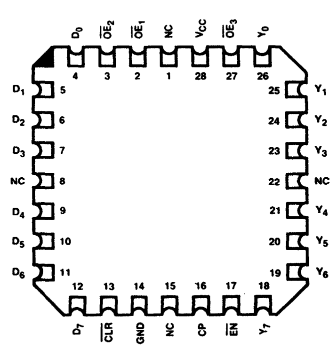
Am29825A

DIPs*



CD001200

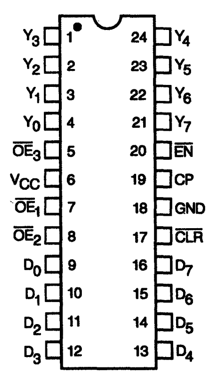
LCC**



CD001210

Am29925A

DIPs

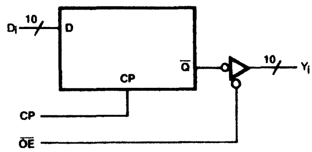


CD010721

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

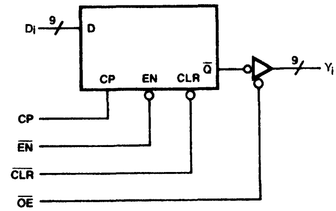
LOGIC SYMBOLS

Am29821A



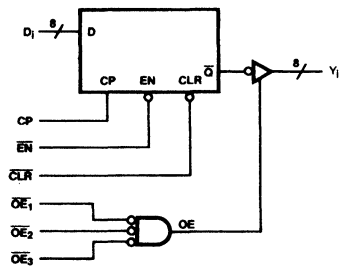
LS000453

Am29823A



LS000432

Am29825A



LS000422

FUNCTION TABLES

Am29821A

Inputs			Internal	Outputs	Function
$\overline{OE}$	D_i	CP	$\overline{Q}_i$	Y_i	
H H	L H	↑ ↑	H L	Z Z	Hi-Z
L L	L H	↑ ↑	H L	L H	Load

H = HIGH
L = LOW

↑ = LOW-to-HIGH Transition
Z = High Impedance

FUNCTION TABLES (Cont'd.)

Am29823A

Inputs					Internal	Outputs	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q_i}$	Y_i	
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

Am29825A

Inputs					Internal	Outputs	Function
OE*	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q_i}$	Y_i	
L	H	L	L	↑	H	Z	Hi-Z
L	H	L	H	↑	L	Z	
L	L	X	X	X	H	Z	Clear
H	L	X	X	X	H	L	
L	H	H	X	X	NC	Z	Hold
H	H	H	X	X	NC	NC	
L	H	L	L	↑	H	Z	Load
L	H	L	H	↑	L	Z	
H	H	L	L	↑	H	L	
H	H	L	H	↑	L	H	

*OE is an Active-HIGH internal signal produced as follows:

$\overline{OE_1}$	$\overline{OE_2}$	$\overline{OE_3}$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29821A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29821A 10-Bit Register
Am29823A 9-Bit Register
Am29825A 8-Bit Register
Am29921A 10-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29923A 9-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29925A 8-Bit Register (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29821A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29823A	
AM29825A	
AM29921A	PC, PCB, DC, DCB, DE
AM29923A	
AM29925A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29821A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29821A 10-Bit Register
Am29823A 9-Bit Register
Am29825A 8-Bit Register
Am29921A 10-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29923A 9-Bit Register (Center-V_{CC}-and-GND Pinout)
Am29925A 8-Bit Register (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29821A	/BLA, /BKA, /B3A
AM29823A	
AM29825A	
AM29921A	/BLA
AM29923A	
AM29925A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_i Data Input (Input)
D_i are the register data inputs.

Y_i Data Outputs (Output)
Y_i are the three-state data outputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on LOW-to-HIGH transitions.

Am29821A Only

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is transferred to the Y_i outputs.

Am29823A Only

$\overline{EN}$ $\overline{\text{Clock Enable}}$ (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are put in the high-impedance state. When $\overline{OE}$ is LOW, the register data is passed to the Y_i outputs.

Am29825A Only

$\overline{EN}$ $\overline{\text{Clock Enable}}$ (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and all $\overline{OE}_i$ are LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ $\overline{\text{Output Enables}}$ (Input, Active LOW)
When $\overline{OE}_1$, $\overline{OE}_2$, and $\overline{OE}_3$ are all LOW, register data is passed to the Y_i outputs. If any or all $\overline{OE}_i$ are HIGH, the Y_i outputs are put in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
  Power Applied .... −55 to +125°C
Supply Voltage to Ground Potential
  Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
  for High Output State .... −0.5 V to 5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
DC Output Current, into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_A) .... 0 to +70°C
  Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V
Military (M) and Extended Commercial (E) Devices
  Temperature (T_C) .... −55 to +125°C
  Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		Volts
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	Volts
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−500	μA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	μA
I_{OZL}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 0.4 V		−50	μA
I_{OZH}			V_O = 2.7 V		50	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current (Note 3)	Am29821A/Am29921A	Outputs LOW		100	mA
			Outputs HIGH		88	
			Outputs Hi-Z		97	
		Am29823A/Am29823A	Outputs LOW		100	mA
			Outputs HIGH		88	
			Outputs Hi-Z		96	
		Am29825A/Am29925A	Outputs LOW		94	mA
			Outputs HIGH		84	
			Outputs Hi-Z		92	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.
3. Clock input, CP, is HIGH after clocking in data. Parameter tested with V_{CC} = Max. and outputs unloaded.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)			3.5	8	3.5	9	ns
t_{PHL}				3.5	10	3.5	11.5	ns
t_S	Data to $\overline{CP}$ Setup Time			4		5		ns
t_H	Data to $\overline{CP}$ Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			6		7		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		5		ns
t_H	Enable ($\overline{EN}$) Hold Time		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2		2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				14		15	
t_{REC}	Clear ($\overline{CLR}$ ↑) to CP Setup Time			6		8		ns
t_{PWH}	Clock Pulse Width	HIGH		7		8		ns
t_{PWL}		LOW		7		8		ns
t_{PWL}	Clear Pulse Width	LOW		6		7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i				11		12	ns
t_{ZL}					12		13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i				8		9	ns
t_{LZ}					8		9	ns

*See Test Circuit and Waveforms.

Am29827A/Am29828A

High-Performance Buffers

DISTINCTIVE CHARACTERISTICS

- High-speed buffers and inverters
  - t_{PD} = 5.0 ns Typical
- 200-mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and power-down
- I_{OL}: 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29827/Am29828

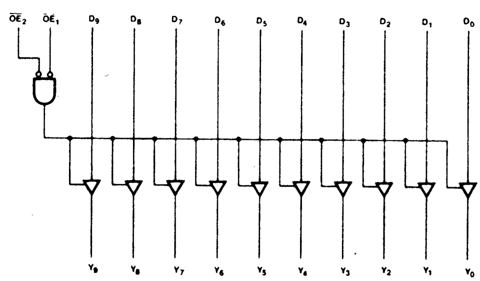
GENERAL DESCRIPTION

The Am29827A and Am29828A Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature a 10-bit wide data path and NORed output enables for maximum control flexibility. The Am29827A has non-inverting outputs, while the Am29828A has inverting outputs. Each device features data inputs with 200-mV minimum input hysteresis to provide improved noise immunity. The Am29827A and Am29828A are produced with AMD's proprietary IMOX* bipolar process, and feature typical propagation delays of 5 ns. Package options include DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

Each member of the Am29800A/Am29900A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both inputs and outputs.

BLOCK DIAGRAMS

Am29827A



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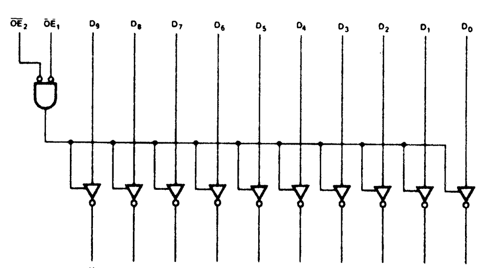
Am29828A



BD001093

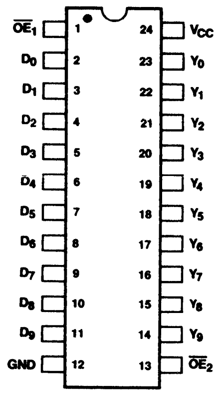
Publication #	Rev.	Amendment
07139	C	/0

Issue Date: **January 1988**

CONNECTION DIAGRAMS
Top View

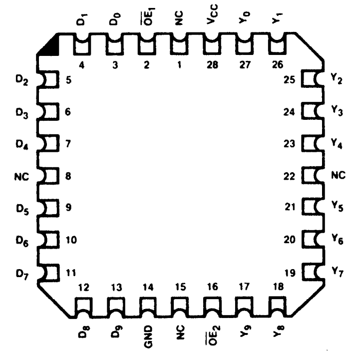
Am29827A/Am29828A

DIPs*



CD001170

LCC**

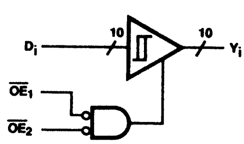


CD001393

*Also available in 24-Pin Flatpack and Small Outline Package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

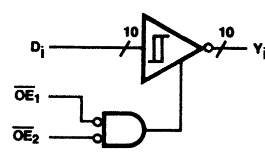
LOGIC SYMBOLS

Am29827A



LS000391

Am29828A



LS000392

FUNCTION TABLES

Am29827A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

Am29828A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29827A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29827A 10-Bit Buffers (Noninverting)
Am29828A 10-Bit Buffers (Inverting)

Valid Combinations	
AM29827A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**

b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29827A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29827A 10-Bit Buffer (Non-inverting)
Am29828A 10-Bit Buffer (Inverting)

Valid Combinations	
AM29827A	/BLA, /BKA, /B3A
AM29828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$\overline{OE_i}$ Output Enables (Input, Active LOW)
When both Output Enables are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are Hi-Z.

D_i Data Inputs (Input)
D_i are the 10-bit data inputs.

Y_i Data Outputs (Output)
Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State .... −0.5 V to +5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
Output Current, into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	V
			COM'L, I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)	COM'L		0.8	V
			MIL		0.7	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
V_{HYST}	Input Hysteresis			200		mV
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	μA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V			−50	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current	V_{CC} = 5.5 V, Outputs Unloaded	Outputs LOW		80	mA
			Outputs HIGH		55	mA
			Outputs Hi-Z		70	mA

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Data (D_i) to Output (Y_i) Am29827A (Noninverting)	$C_L = 50$ pF, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$		8		9	ns
t_{PHL}				8		9	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828A (Inverting)			7		8	ns
t_{PHL}				9		10	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i			11		12	ns
t_{ZL}				12		13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i			10		10	ns
t_{LZ}				10		10	ns

*See Test Circuit and Waveforms.

Am29833A/Am29853A/Am29855A

Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceivers for processor organized devices
  - T-R delay = 6 ns typical
  - R_i-Parity delay = 9 ns typical
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- 200-mV minimum input hysteresis (Commercial) on input data ports
- High drive capability:
  - 48 mA Commercial I_{OL}
  - 32 mA Military I_{OL}
- Higher speed, lower power versions of the Am29833 & Am29853
- Am29855A adds new functionality

GENERAL DESCRIPTION

The Am29833A, Am29853A, and Am29855A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an $\overline{ERR}$ flag showing the result of the parity test.

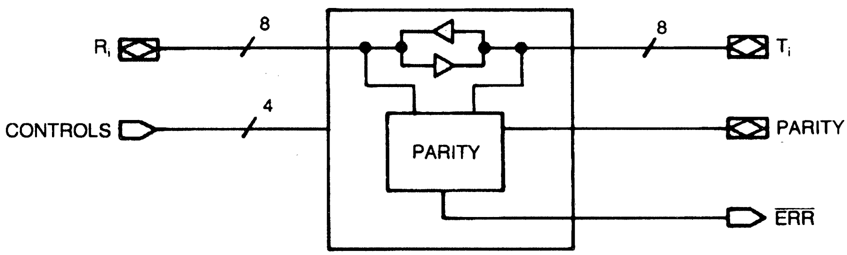
In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29853A and Am29833A, the parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port. The Am29855A, a variation of the Am29853A, is designed so that when both output enables are HIGH, the $\overline{ERR}$ pin retains its current state.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

Each of these devices is produced with AMD's proprietary IMOX* bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability. Package option s include DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

SIMPLIFIED BLOCK DIAGRAM

Parity Transceivers



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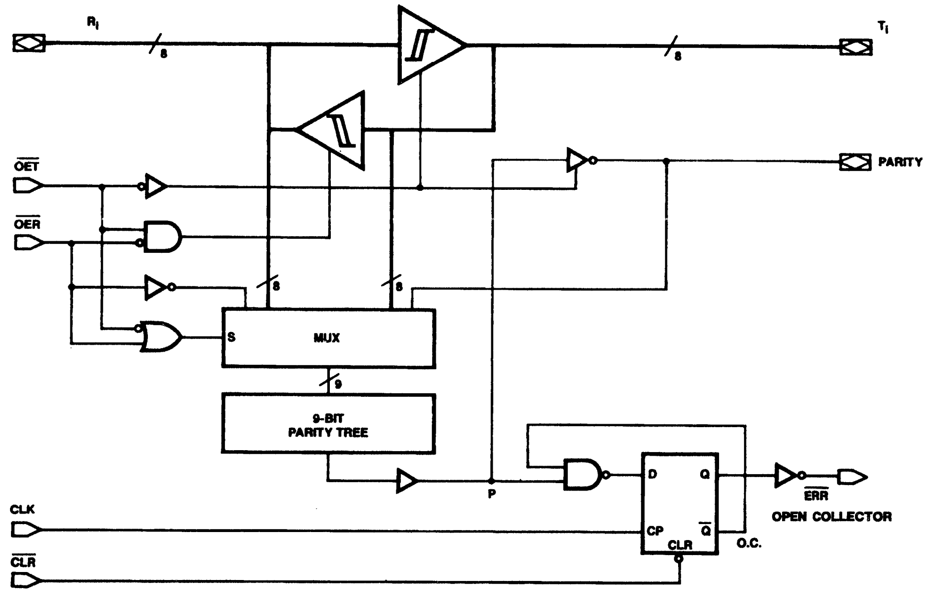
*IMOX is a trademark of Advanced Micro Devices, Inc.

Publication # 07140 Rev. C Amendment /0
Issue Date: January 1988

BLOCK DIAGRAMS*

Am29833A



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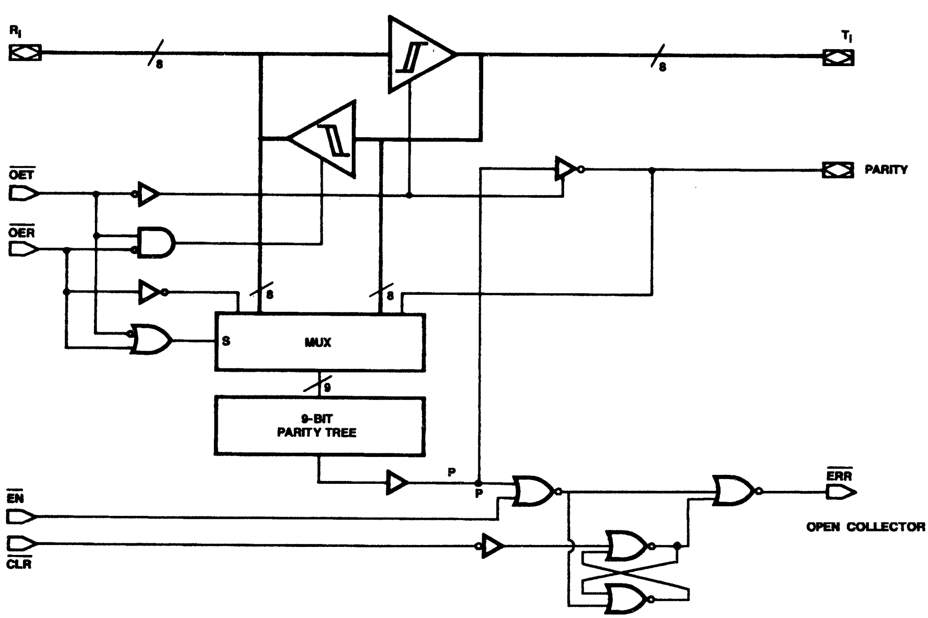
Am29853A



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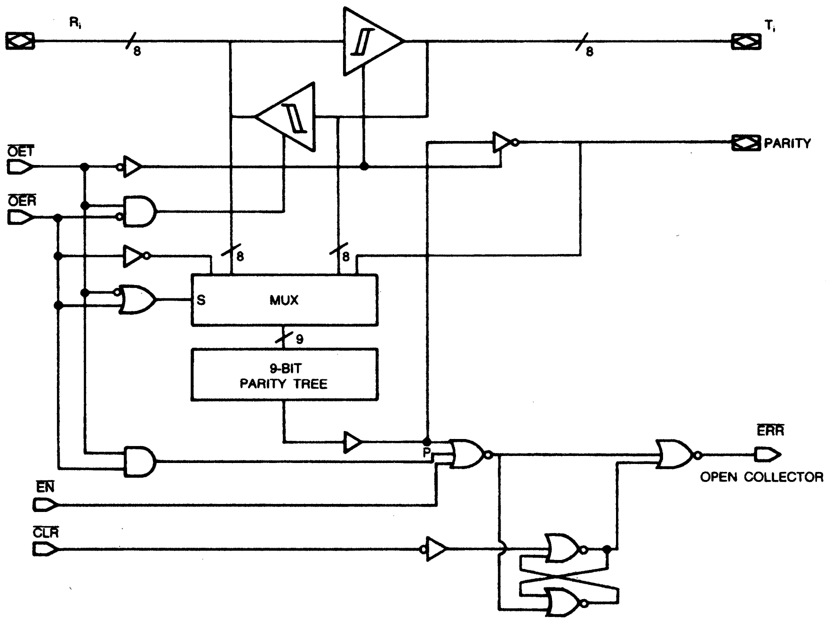
*See following page for additional Block Diagrams.

BLOCK DIAGRAMS (Cont'd.)

Am29855A

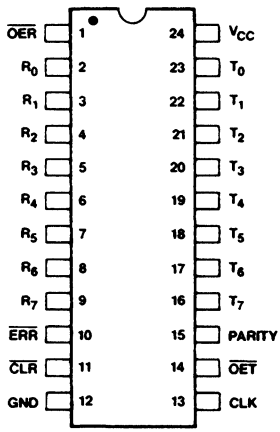


BD005560

CONNECTION DIAGRAMS
Top View

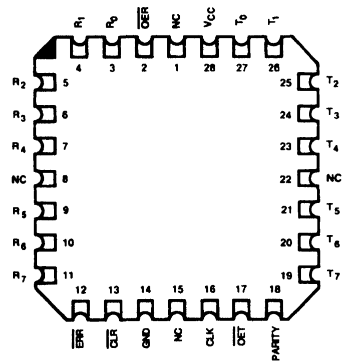
Am29833

DIPs*



CD001120

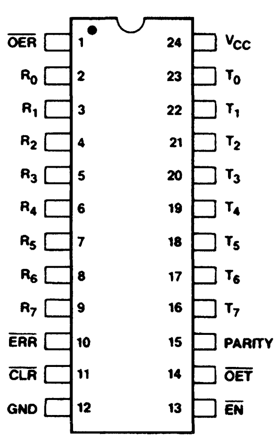
LCC**



CD001398

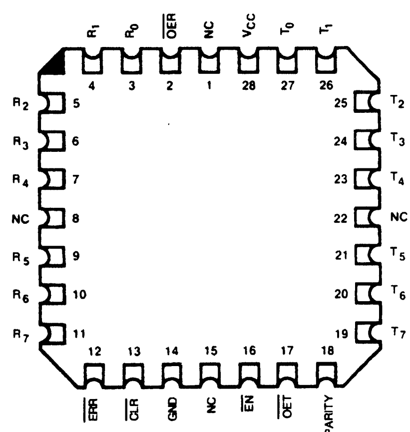
Am29853/Am29855

DIPs*



CD001130

LCC**



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*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

FUNCTION TABLES

Am29833A (Register Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Recieve path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	Parity logic defaults to transmit mode.
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition of Clock
X = Don't Care

Z = High Impedance
NA = Not Applicable
* = Store the Error State of the Last Receive Cycle

ODD = Odd Number
Even = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE

Error Flag Output

Am29833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample
H	↑	X	L	L	(1's
H	↑	L	X	L	Capture)
L	X	X	X	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FUNCTION TABLES (Cont'd.)

Am29853A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

Am29855A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
X = Don't Care

Z = High impedance
NA = Not applicable
* = Store the Error state of the last Receive cycle

Odd = Odd number
Even = Even number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE
Error Flag Output

Am29853A/Am29855A

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L L	L L	L H	X X	L H	Pass
L L L	H H H	L X H	X L H	L L H	Sample (1's Capture)
H	L	X	X	H	Clear
H H	H H	X X	L H	L H	Store

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29833A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Military (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29833A Parity Transceiver, Register Option
Am29853A Parity Transceiver, Latch Option
Am29855A Parity Transceiver, Latch Option (New Functionality)

Valid Combinations	
AM29833A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29853A	
AM29855A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29833A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29833A Parity Transceiver, Register Option
Am29853A Parity Transceiver, Latch Option
Am29855A Parity Transceiver, Latch Option (New Functionality)

Valid Combinations	
AM29833A	/BLA, /BKA, /B3A
AM29853A	
AM29855A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29833A, Am29853A/Am29855A

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i Receive Port (Input/Output, Three-State)
R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output, Three-State)
T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity Parity Flag (Input/Output, Three-State)
In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29833A Only

$\overline{ERR}$ Error Flag (Output, Open Collector)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK Clock (Input, Positive Edge-Triggered)
This pin is the clock input for the Error Flag register.

Am29853A/Am29855A Only

$\overline{ERR}$ Error Flag (Output, Open Collector)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared. In the Am29855A, the error flag will retain its previous state when $\overline{OET}$ and $\overline{OER}$ are HIGH.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW and $\overline{EN}$ is HIGH, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$ Latch Enable (Input, Active LOW)
This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Output
for High Output State .... −0.5 V to +5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
DC Output Current, into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15 mA	2.4		V
				I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	$\overline{ERR}$	I_{OL} = 48 mA		0.5	V
			All Other Outputs	I_{OL} = 32 mA MIL		0.5	
				I_{OL} = 48 mA COM'L		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)		COM'L		0.8	V
				MIL		0.7	
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i			COM'L	200		mV
				MIL	150		
I_{ZL}	I/O Port LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V				−550	μA
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V				−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V V_{IN} = 5.5 V				100	μA
I_{ZH}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				100	μA
I_{ZI}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				150	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0.0 V (Note 2)			−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V				100	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5 V Outputs Unloaded		Ouputs LOW		180	mA
				Outputs HIGH		155	
				Outputs Hi-Z		170	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		$C_L = 50$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$		10		14	ns
t_{PHL}					10		14	ns
t_{PLH}	Propagation Delay R_i to Parity				15		20	ns
t_{PHL}					15		20	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity			12		16		ns
t_{ZL}					12		16	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity			12		16		ns
t_{LZ}					12		16	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			12		16		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		0		ns
t_{REC}	Clear ($\overline{CLR}$ ↑) to CLK Setup Time (Note 2)			15		20		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		7		9.5		ns
t_{PWL}		LOW		7		9.5		ns
t_{PWL}	Clear Pulse Width	LOW		7		9.5		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				12		16	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				16		20	ns
t_{PLH}	Propagation-Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29853A/Am29855A				22		25	ns
t_{PHL}					18		20	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				15		20	ns
t_{PHL}					15		20	ns

*See test circuit and waveforms.

Notes: 1. For Am29853A/Am29855A, replace CLK with $\overline{EN}$.
2. Not applicable to Am29853A/Am29855A.

Am29841A/Am29843A/Am29845A
Am29941A/Am29943A/Am29945A

High-Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - transparent $t_{PD} = 5.0$ ns typical
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL}: 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29841, Am29843, and Am29845
- Am29900A DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

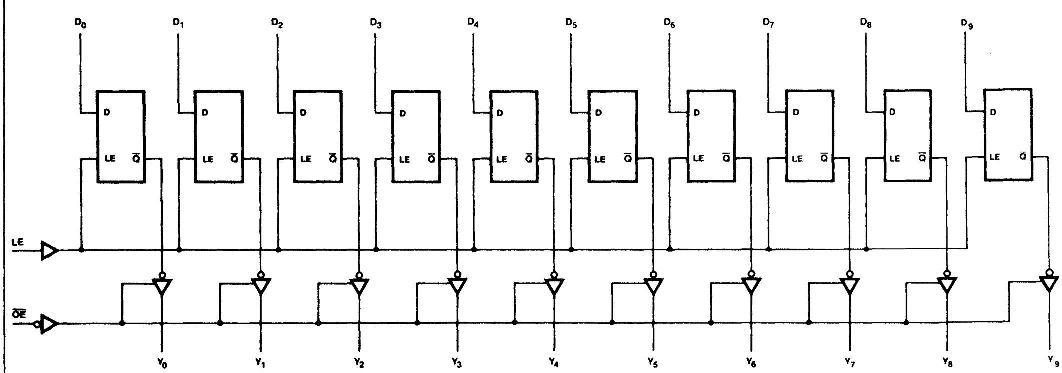
The Am29841A, Am29843A, and Am29845A Buffered Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29800A latches are produced with AMD's exclusive IMOX* bipolar process, and feature typical propagation delays of 5 ns, as well as high-capacitive drive capability.

The Am29841A is a buffered, 10-bit version of the popular '373 function. The Am29843A is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The Am29845A, an 8-bit buffered latch, has all the 9-bit controls, plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$), to allow multi-user control of the interface; e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The device is ideal for use as an output port requiring high I_{OL}/I_{OH}.

The Am29800A latches are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for latches with this pinout are the Am29941A, Am29943A, and Am29945A; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS**

Am29841A



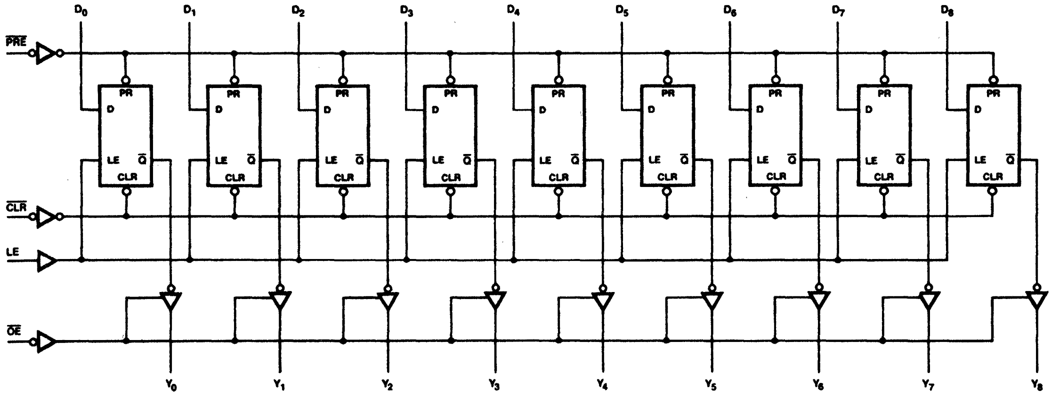
BD001056

*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following pages for additional Block Diagrams.

Publication # 07141 Rev. C Amendment /0
Issue Date: January 1988

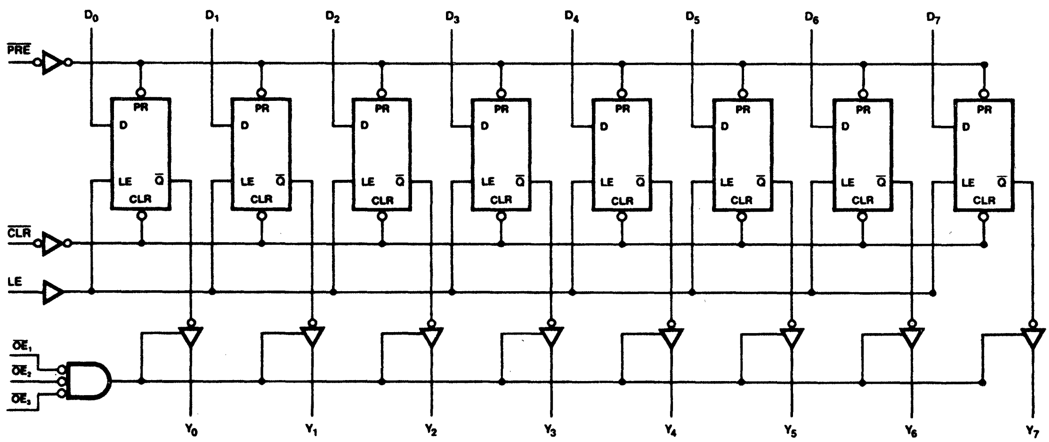
BLOCK DIAGRAMS (Cont'd.)

Am29843A



BD001057

Am29845A

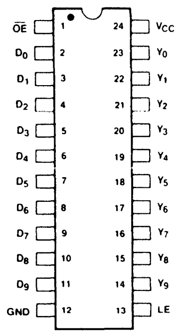


BD001058

CONNECTION DIAGRAMS
Top View

Am29841A

DIPs*



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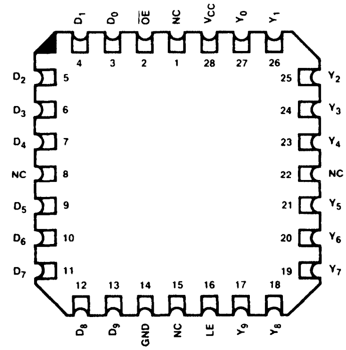
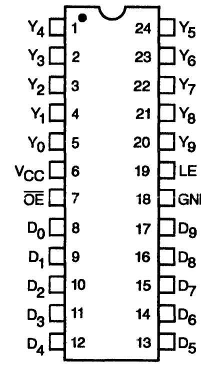
LCC**



CD001390

Am29941A

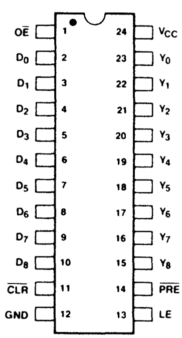
DIPs



CD010722

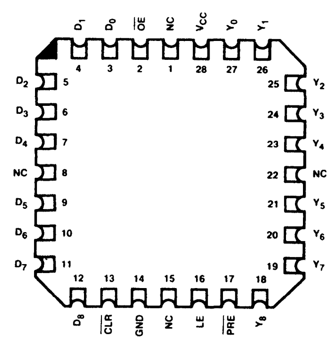
Am29843A

DIPs*



CD001400

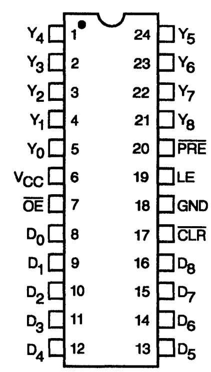
LCC**



CD001410

Am29943A

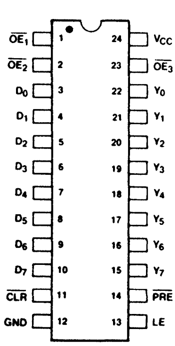
DIPs



CD010723

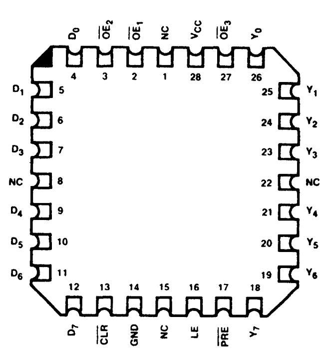
Am29845A

DIPs*



CD001340

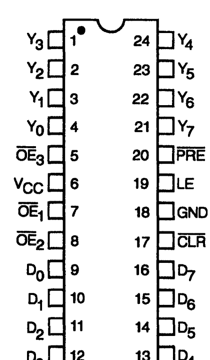
LCC**



CD001350

Am29945A

DIPs

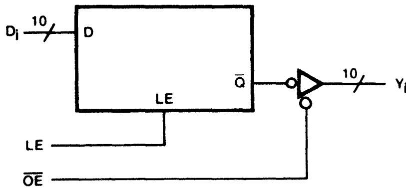


CD010724

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

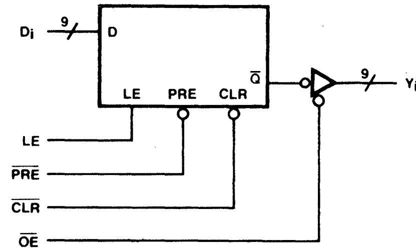
LOGIC SYMBOLS

Am29841A



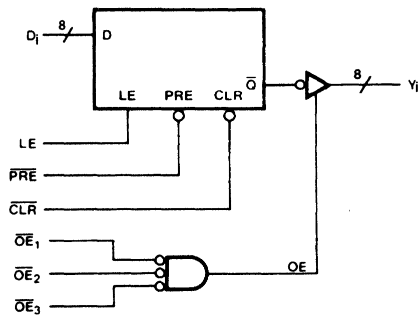
LS000463

Am29843A



LS000473

Am2985A



LS000443

FUNCTION TABLES

Am29841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance

FUNCTION TABLES (Cont'd.)

Am29843A

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	H	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

Am29845A

OE*	Inputs				Internal	Outputs	Function
	$\overline{CLR}$	$\overline{PRE}$	LE	D_i	$\overline{Q}_i$	Y_i	
L	H	H	X	X	X	Z	Hi-Z
L	H	H	H	L	H	Z	Hi-Z
L	H	H	H	H	L	Z	Hi-Z
L	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	H	H	L	H	L	Transparent
H	H	H	H	H	L	H	Transparent
H	H	H	L	X	NC	NC	Latched
H	H	L	X	X	L	H	Preset
H	L	H	X	X	H	L	Clear
H	L	L	X	X	L	H	Preset
L	L	H	L	X	H	Z	Latched (Hi-Z)
L	H	L	L	X	L	Z	Latched (Hi-Z)

*OE is an Active HIGH internal signal produced as follows:

$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH
L = LOW
NC = No Change
Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29841A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29841A 10-Bit Latch
Am29843A 9-Bit Latch
Am29845A 8-Bit Latch
Am29941A 10-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29943A 9-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29945A 8-Bit Latch (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29841A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29843A	
AM29845A	
AM29941A	PC, PCB, DC, DCB, DE
AM29943A	
AM29945A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29841A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29841A 10-Bit Latch
Am29843A 9-Bit Latch
Am29845A 8-Bit Latch
Am29941A 10-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29943A 9-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29945A 8-Bit Latch (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29841A	/BLA, /BKA, /B3A
AM29843A	
AM29845A	
AM29941A	/BLA
AM29943A	
AM29945A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_i Data Inputs (Input)
D_i are the latch data inputs.

Y_i Data Outputs (Output)
Y_i are the three-state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

Am29841A

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high-impedance state.

Am29843A

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high-impedance state.

$\overline{PRE}$ $\overline{\text{Preset}}$ (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

Am29845A

$\overline{OE_i}$ $\overline{\text{Output Enables}}$ (Input, Active LOW)
When $\overline{OE_1}$, $\overline{OE_2}$, and $\overline{OE_3}$ are all LOW, the latch data is passed to the Y_i outputs. If any or all $\overline{OE_i}$ are HIGH, the Y_i outputs are put in a high impedance state.

$\overline{PRE}$ $\overline{\text{Preset}}$ (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if all $\overline{OE_i}$ are LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ $\overline{\text{Clear}}$ (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the Y_i outputs are LOW if all $\overline{OE_i}$ are LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State .... −0.5 V to +5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
DC Output Current, into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		Volts
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	Volts
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 5.5 V, I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	μA
I_{OZL}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 0.4 V		−50	μA
I_{OZH}			V_O = 2.7 V		50	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current	V_{CC} = 5.5 V Outputs Unloaded	Outputs LOW		97	mA
			Outputs HIGH		70	
			Outputs Hi-Z		81	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)			7		8.5	ns
t_{PHL}				9		10	ns
t_S	Data to LE Setup Time		2.5		3.5		ns
t_H	Data to LE Hold Time		2.5		3.5		ns
t_{PLH}	Latch Enable (LE) to Y_i			12		13	ns
t_{PHL}				12		13	ns
t_{PLH}	Propagation Delay, Preset to Y_i	$C_L = 50$ pF		12		14	ns
t_{PHL}		$R_1 = 500\ \Omega$		12		14	ns
t_{REC}	Preset ($\overline{PRE}$ ↑) to LE Setup Time	$R_2 = 500\ \Omega$	4		5		ns
t_{PLH}	Propagation Delay, Clear to Y_i			13		14	ns
t_{PHL}				13		14	ns
t_{REC}	Clear ($\overline{CLR}$ ↑) to LE Setup Time		7		8		ns
t_{PWH}	LE Pulse Width HIGH		4		5		ns
t_{PWL}	Preset Pulse Width LOW		5		7		ns
t_{PWL}	Clear Pulse Width LOW		4		5		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i			10.5		13.5	ns
t_{ZL}				11.5		14.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i			8		10	ns
t_{LZ}				8		10	ns

*See Test Circuit and Waveforms.

Am29861A/Am29863A

High-Performance Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed symmetrical bidirectional transceivers
  - t_{PD} = 5 ns typical
- 200-mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down
- I_{OL}: 48 mA Commercial I_{OL}, 32 mA Military
- Higher speed, lower power versions of the Am29861 and Am29863

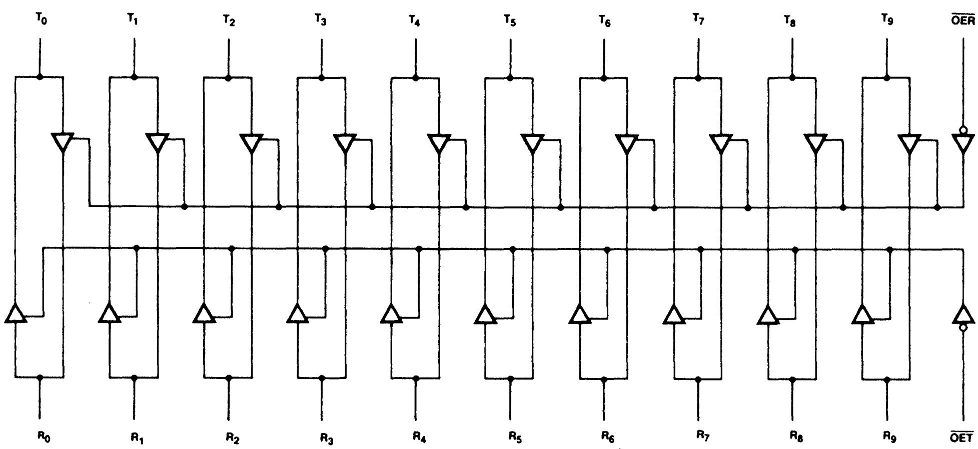
GENERAL DESCRIPTION

The Am29861A and Am29863A Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29861A is a 10-bit bidirectional transceiver; the Am29863A is a 9-bit bidirectional transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV minimum input hysteresis to provide improved noise immunity. The Am29861A and Am29863A are produced with AMD's proprietary IMOX* bipolar process, and feature typical propagation delays of 5 ns. Package options include DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

Each member of the Am29800A/Am29900A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both the inputs and outputs.

BLOCK DIAGRAMS**

Am29861A



BD001060

*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following page for additional Block Diagram.

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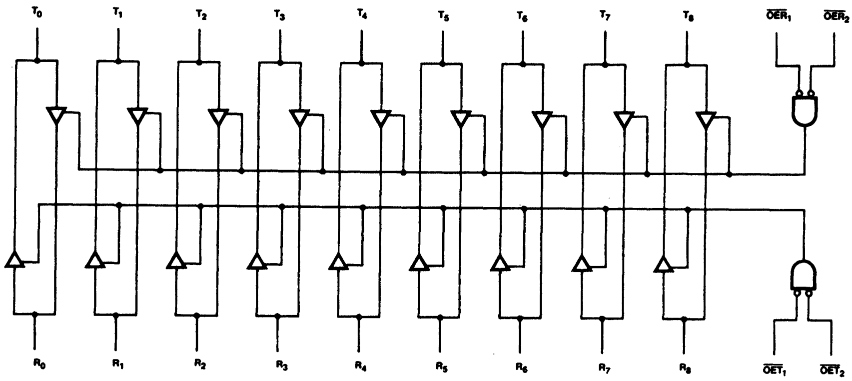
Issue Date: January 1988

BLOCK DIAGRAMS (Cont'd.)

Am29863A

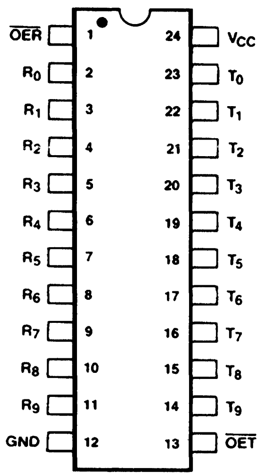


BD001070

CONNECTION DIAGRAMS
Top View

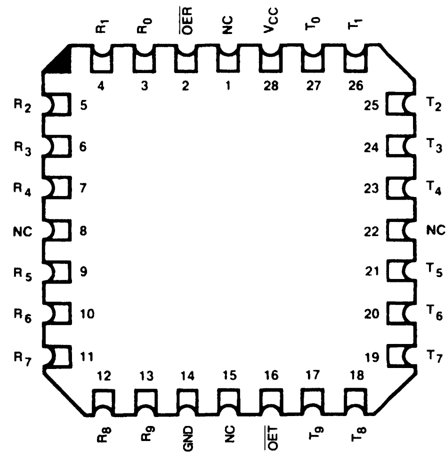
Am29861A

DIPs*



CD001150

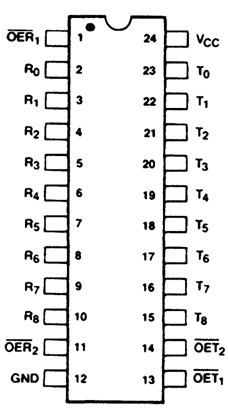
LCC**



CD001391

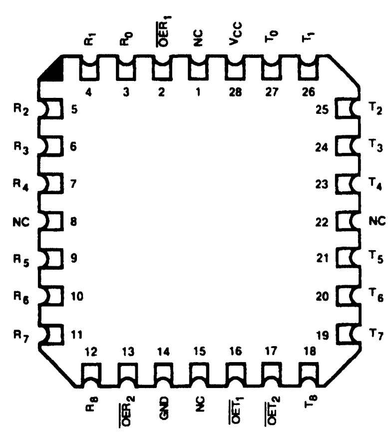
Am29863A

DIPs*



CD001140

LCC**



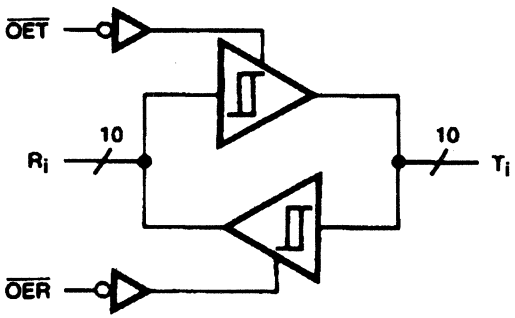
CD001397

*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.

**Also available in 28-Pin PLCC; pinout identical to LCC.

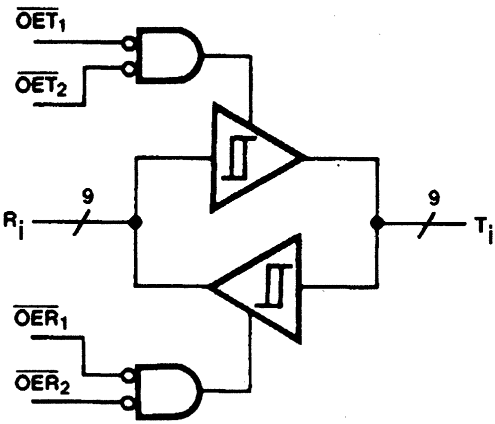
LOGIC SYMBOLS

Am29861A



LS000372

Am29863A



LS000382

FUNCTION TABLES

Am29861A

Inputs				Outputs		Function
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29863A

Inputs						Outputs		Function
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_i	T_i	R_i	T_i	
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29861A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29861A 10-Bit Transceiver
Am29863A 9-Bit Transceiver

Valid Combinations	
AM29861A	PC, PCB, DC, DCB,
AM29863A	DE, SC, JC, LC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29861A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29861A 10-Bit Transceiver
Am29863A 9-Bit Transceiver

Valid Combinations	
AM29861A	/BLA, /BKA, /B3A
AM29863A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29861A

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_i Receive Port (Input/Output)
R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29863A

$\overline{OER_i}$ Output Enables-Receive (Input, Active LOW)
When both $\overline{OER_1}$ and $\overline{OER_2}$ are LOW while $\overline{OET_1}$ or $\overline{OET_2}$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET_i}$ Output Enables-Transmit (Input, Active LOW)
When both $\overline{OET_1}$ and $\overline{OET_2}$ are LOW while $\overline{OER_1}$ or $\overline{OER_2}$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_i Receive Port (Input/Output)
R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Output
for High Output State .... −0.5 V to +5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
DC Output Current, Into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	V
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)	COM'L		0.8	V
			MIL		0.7	
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
V_{HYST}	Input Hysteresis			200		mV
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	μA
I_{ZL}	I/O Port LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−550	μA
I_{ZH}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			100	μA
I_{ZI}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			150	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current	V_{CC} = 5.5 V, Outputs Unloaded	Outputs LOW		140	mA
			Outputs HIGH		115	
			Outputs Hi-Z		130	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Paremeter Description	Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861A/Am29863A	$C_L = 50$ pF, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$		8		9	ns
t_{PHL}				8		9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			11		12	ns
t_{ZL}				12		13	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			10		10	ns
t_{LZ}				10		10	ns

*See Test Circuit and Waveforms.

Am29818A

Pipeline Register with SSR™ Diagnostics
Higher Speed Version of Am29818

DISTINCTIVE CHARACTERISTICS

- High-speed noninverting 8-bit parallel register for any data path or pipelining application
- WCS (Writable Control Store) pipeline register
  - Load WCS from serial register
  - Read WCS via serial scan
- Alternate sourced as SN54/74S818
- High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- Speed comparable with that of 'AS374 register

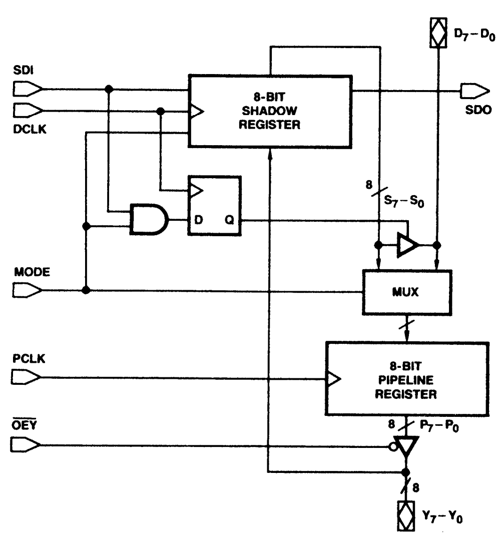
GENERAL DESCRIPTION

The Am29818A is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for *normal* system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a shift register. In the serial shift mode, SDI is shifted into the '0' location of the Shadow register and the contents of '7' location appear at the SDO output. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29818A Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM

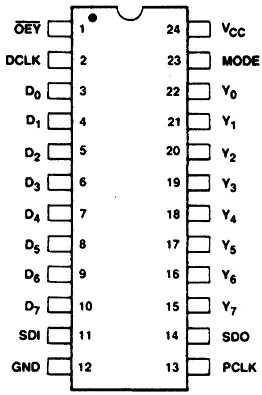


BD001020

Publication # 08611 Rev. C Amendment /0
Issue Date: January 1988

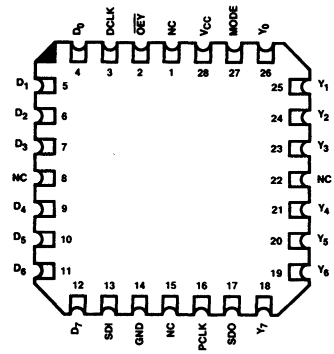
CONNECTION DIAGRAMS
Top View

DIPs*



CD001102

LCC**



CD001160

*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29818A P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29818A
Pipeline Register with SSR Diagnostics
(Higher Speed Version of Am29818 & Am29818-1)

Valid Combinations	
AM29818A	PC, PCB, DC, DCB, DE, SC, JC, LC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29818A /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29818A
Pipeline Register with SSR Diagnostics
(Higher Speed Version of Am29818 & Am29818-1)

Valid Combinations	
AM29818A	/BLA, /BKA, /B3A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$D_0 - D_7$ Parallel Data Inputs (Input/Output)
Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK Diagnostics Clock (Input)
Diagnostics/WCS clock for loading shadow register (serial or parallel modes — see Function Table).

MODE Mode Control (Input)
Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$ Y-Port Output Enable (Input; Active LOW)
Active-LOW output enable for Y-port.

PCLK Pipeline Register Clock (Input)
Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI Serial Data Input (Input)
Input to shadow register (see Function Table).

SDO Serial Data Output (Output)
Output from shadow register.

$Y_0 - Y_7$ Parallel Data Outputs (Input/Output)
Data outputs from the pipeline register and parallel inputs to the shadow register.

FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no set-up or hold times are violated, this simultaneous operation is legal.

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_0 \leftarrow SDI$	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	SDI	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	X	SDI	Hold*	NA	Hold Shadow Register; $D_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

FUNCTION TABLE DEFINITIONS

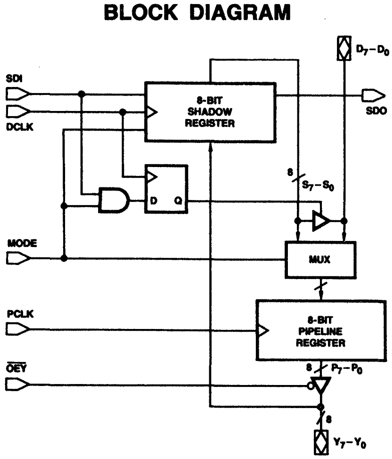
INPUTS

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition

OUTPUTS

$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable output is not a function of the specified input combinations.

BLOCK DIAGRAM



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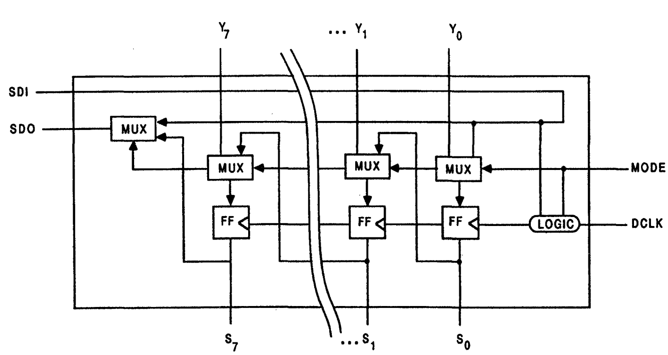
SHADOW REGISTER



BD006770

An Introduction to Serial Shadow Register (SSR) Diagnostics

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals - address, data, control and status - to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.

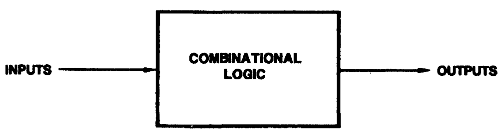


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Figure 1. Combinational Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

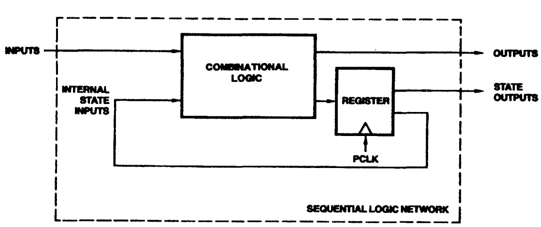

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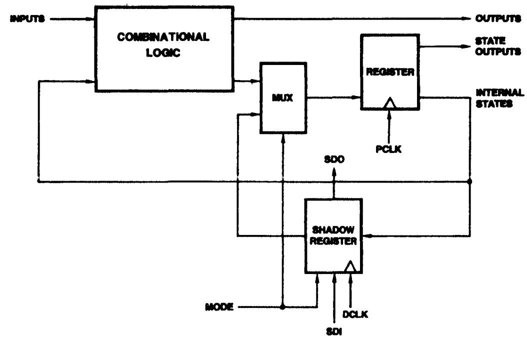
Figure 2. Sequential Network

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.



DF000041

Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

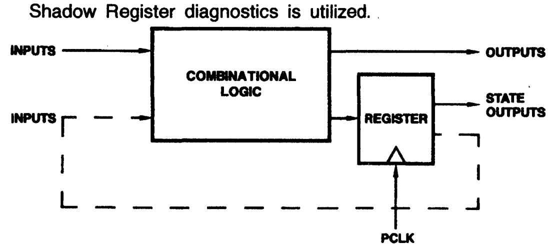


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Figure 4. SSR Diagnostics Logical Path

A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29818A.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818A's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

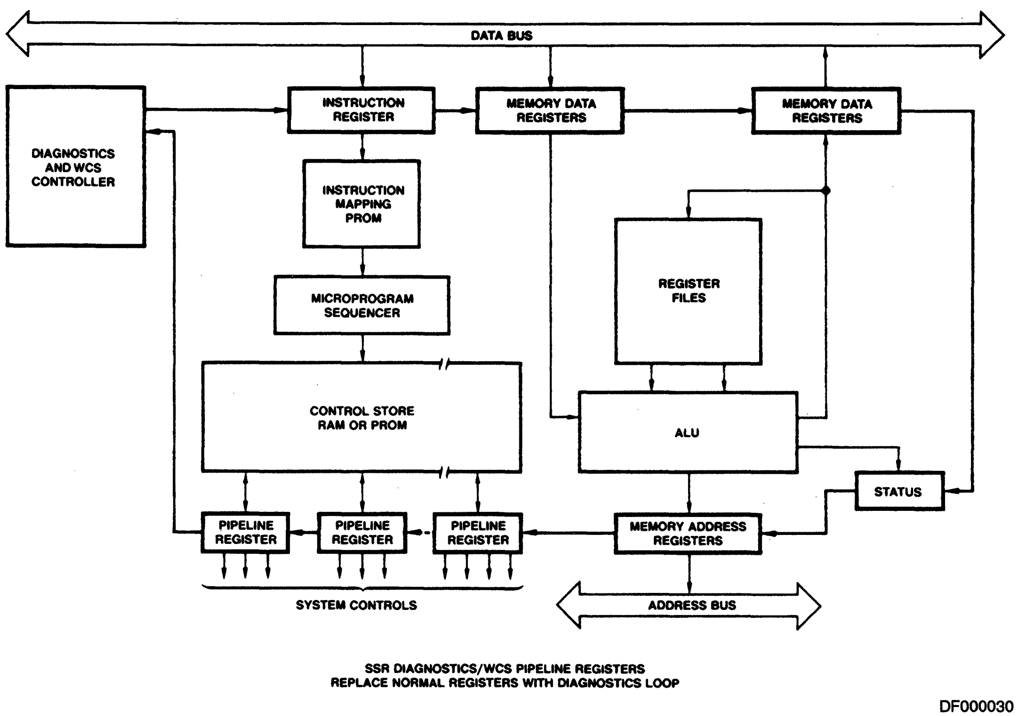


Figure 5. Typical System Configuration

Use of the Am29818A Pipeline Register in Writable Control Store (WCS) Designs

The Am29818A SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29818A supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29818A. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinational network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.

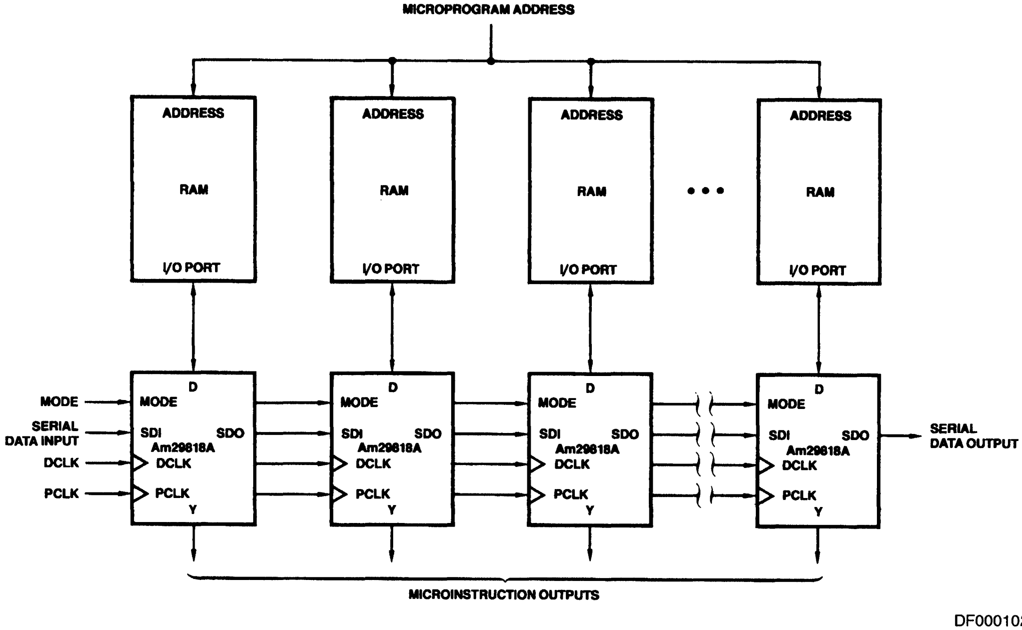


Figure 6. Am29818A-Based WCS Application

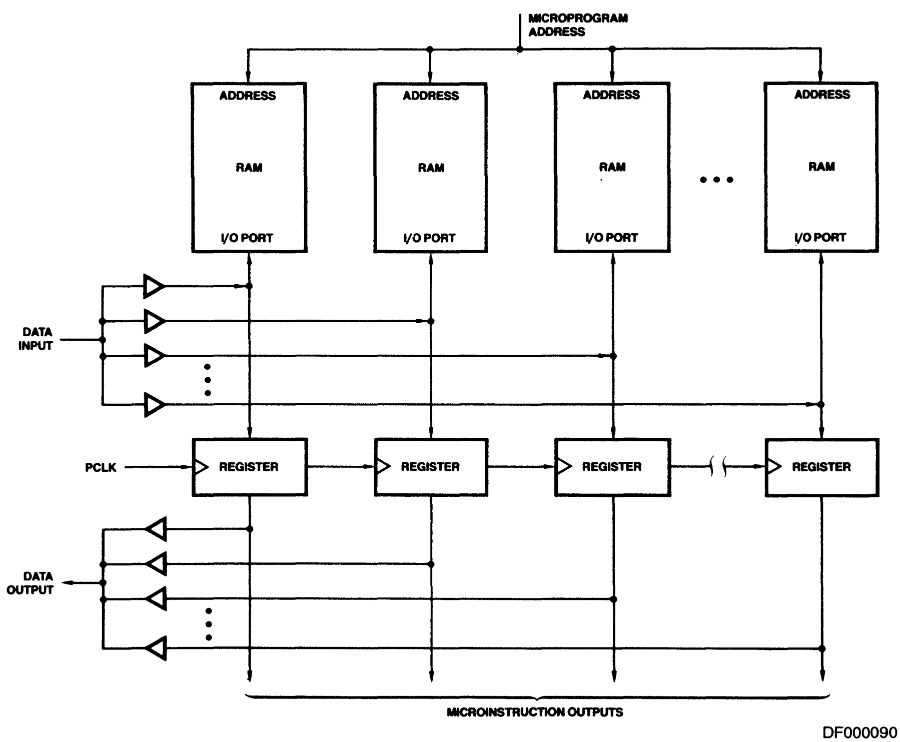


Figure 7. WCS Application without Am29818As

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature with
Power Applied .... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State .... −0.5 V to +5.5 V
DC Input Voltage .... −1.5 V to +6.0 V
DC Output Current, into Outputs .... 100 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0°C to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

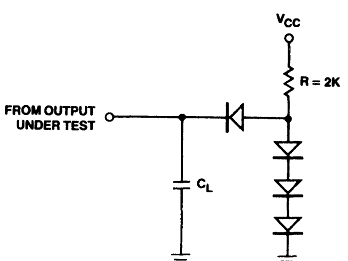
Parameter Symbol	Parameter Description	Test Conditions (Note 1)				Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	$Y_0 - Y_7$: I_{OH} = −6 mA $D_0 - D_7$, SDO: I_{OH} = −1 mA			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	$Y_0 - Y_7$		I_{OL} = 24 mA			0.5
			$D_0 - D_7$,	COM'L	I_{OL} = 8 mA		0.5	V
			SDO	MIL	I_{OL} = 4 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)				2.0		
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.5 V					−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.4 V					50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V					1.0	mA
I_O	Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 0.5 V				−250	μA
			V_O = 2.4 V				100	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V (Note 2)	$Y_0 - Y_7$			−30	−100	mA
			$D_0 - D_7$, SDO			−15	−50	
I_{OFF}	Bus Leakage	V_{CC} = 0 V, V_{OUT} = 2.9 V					100	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5 V	Outputs Hi-Z				145	mA

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

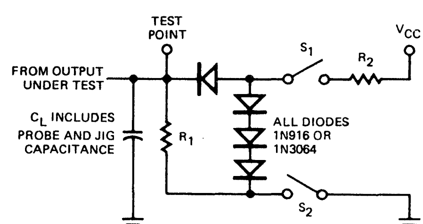
Parameter Symbol	Paramter Description	Test Conditions	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH} and t_{PHL}	PCLK→Y_X	See Test Output Load Conditions Below C_L = 50 pF		9		12	ns
	MODE→SDO			16		18	ns
	SDI→SDO			15		18	ns
	DCLK→SDO			25		30	ns
t_S	D_X→PCLK		4		6		ns
	MODE→PCLK		15		15		ns
	Y_X→DCLK		5		5		ns
	MODE→DCLK		12		12		ns
	SDI→DCLK		10		12		ns
	DCLK→PCLK		15		15		ns
	DCLK→DCLK		40		45		ns
t_H	D_X→PCLK		2		2		ns
	MODE→PCLK		0		0		ns
	Y_X→DCLK		5		5		ns
	MODE→DCLK		2		5		ns
	SDI→DCLK		0		0		ns
t_{LZ}	$\overline{OEY}$→Y_X			15		20	ns
	DCLK→D_X			45		45	ns
t_{HZ}	$\overline{OEY}$→Y_X			25		30	ns
	DCLK→D_X			80		90	ns
t_{ZL}	$\overline{OEY}$→Y_X			15		20	ns
	DCLK→D_X			25		35	ns
t_{ZH}	$\overline{OEY}$→Y_X			15		20	ns
	DCLK→D_X			25		30	ns
t_{PW}	PCLK (HIGH and LOW)		10		15		ns
	DCLK (HIGH and LOW)		15		25		ns

SWITCHING TEST CIRCUITS



TC000330

SDO Output



TC000340

Three-State Outputs

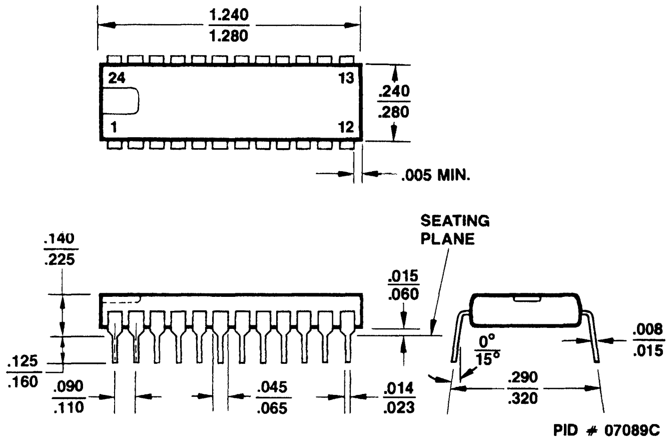
Pin	R_1	R_2
$Y_0 - Y_7$	1K	280
D_{0-7}	5K	2K

Am29C800/Am29800A DEVICE GATE COUNTS

Part Number	Equivalent Number of Gates
Am29C800 Family	
Am29C818	303
Am29C821	90
Am29C823	96
Am29C827	60
Am29C828	55
Am29C833	139
Am29C841	73
Am29C843	69
Am29C853	135
Am29C855	135
Am29C861	105
Am29C863	98
Am29800A Family	
Am29818A	147
Am29821A	72
Am29823A	72
Am29825A	68
Am29827A	30
Am29828A	40
Am29833A	88
Am29841A	62
Am29843A	58
Am29845A	54
Am29853A	84
Am29855A	85
Am29861A	55
Am29863A	52

PACKAGE OUTLINES*

PD3024



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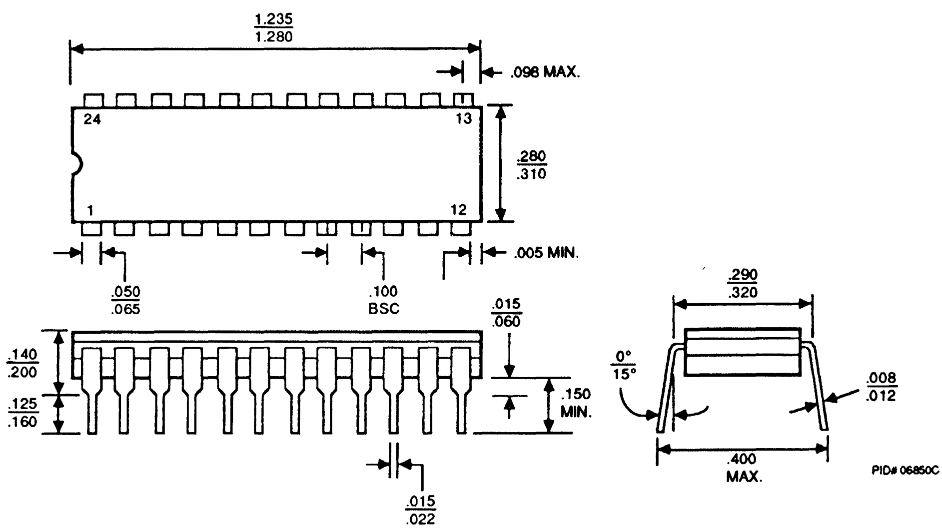
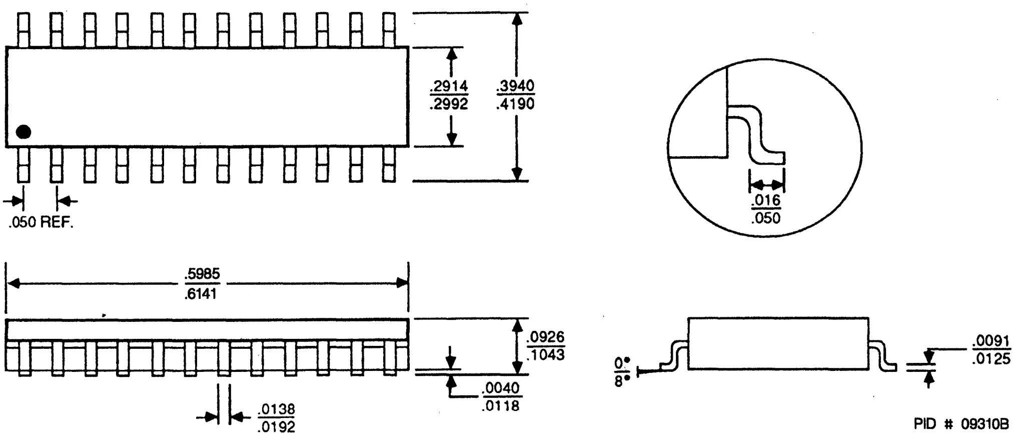


*For reference only.

PACKAGE OUTLINES (Cont'd.)

SO 024



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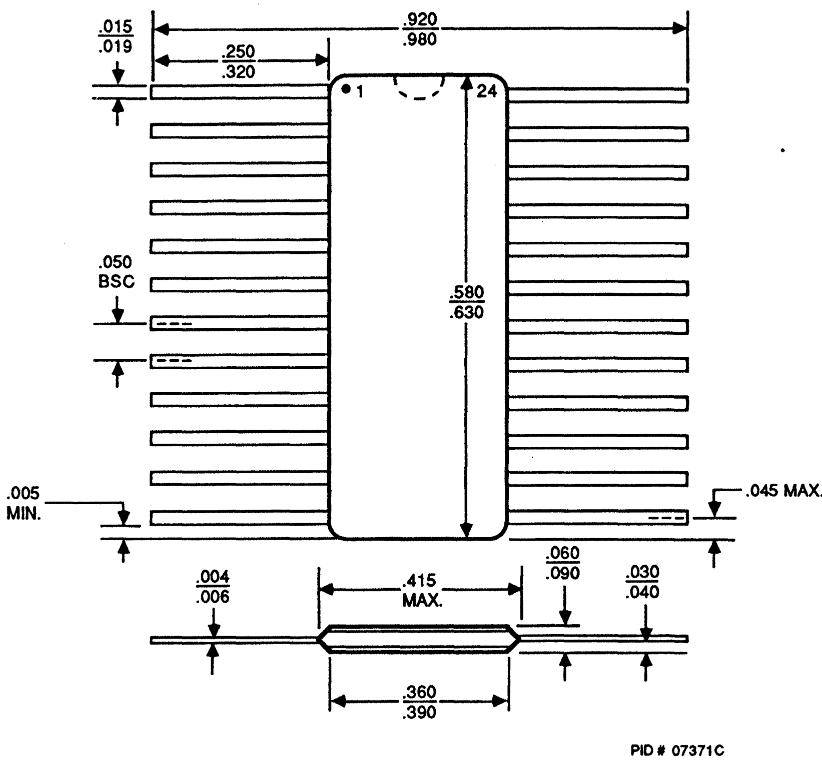

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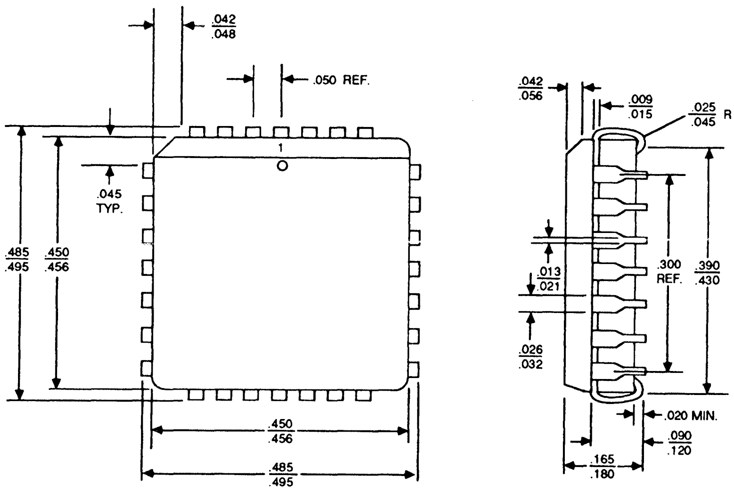
PL 028



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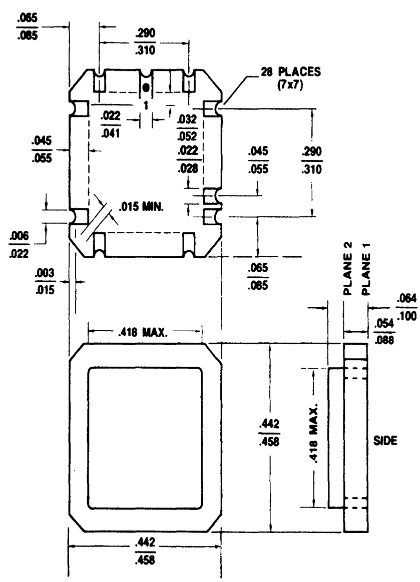

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