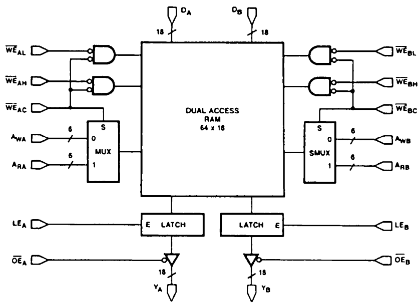
Am29C334

CMOS Four-Port Dual-Access Register File

DISTINCTIVE CHARACTERISTICS

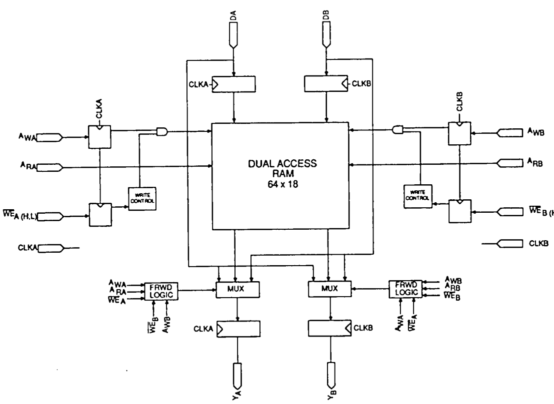
- **64 x 18 Bit Wide Register File**
  The Am29C334 is a 64 x 18-bit, dual-access RAM with two read ports and two write ports.
- **Pipelined Data Path**
  The Am29C334 can be configured to support either a non-pipelined data path (similar to the Am29334) or a pipelined data path.
- **Cascadable**
  The Am29C334 is cascadable to support either wider word widths, deeper register files, or both.
- **Built in Forwarding Logic**
  The Am29C334 provides simultaneous read/write access to the same address for double pipelined systems.
- **Byte Parity Storage**
  Width of 18 bits facilitates byte parity storage for each port and provides consistency with the Am29C332 32-bit ALU.
- **Byte Write Capability**
  Individual byte-write enables allow byte or full word write.

BLOCK DIAGRAMS



BD003022

Non-Pipelined Mode



BD007020

Pipelined Mode

Am29C334

Advanced Micro Devices

Publication #	Rev.	Amendment
08786	B	/0

Issue Date: **August 1987**

GENERAL DESCRIPTION

The Am29C334 is a 64-word by 18-bit dual-access RAM with two read ports and two write ports. Two independent, simultaneous accesses are possible and each access can be either a read or a write. It is designed to be used in a system that requires as many as two reads and two writes in a single cycle. The device can be configured to support either a non-pipelined data path or a pipelined data path.

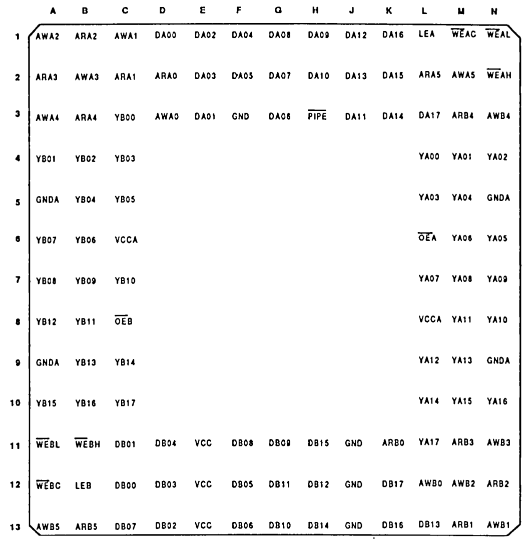
The Am29C334 is also fully compatible with the bipolar Am29334. When the device is connected to the pinout specified for the Am29334, it will appear as a 64-word by 18-bit array without support for pipelined operation. The pipelined operation of the Am29C334 is made possible because of the availability of unused power pins not required by the CMOS part. The pipelined operation is disabled by attaching the $\overline{\text{PIPE}}$ pin to V_{CC}.

RELATED AMD PRODUCTS

Part No.	Description
Am29C323	CMOS 32-Bit Parallel Multiplier
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	64 x 18 Four-Port Dual-Access Register File
Am29337	16-Bit Bounds Checker
Am29338	128 x 9 Byte Queue

CONNECTION DIAGRAM

120 Lead PGA*



CD010320

*Pins facing up.

TABLE OF INTERCONNECTIONS

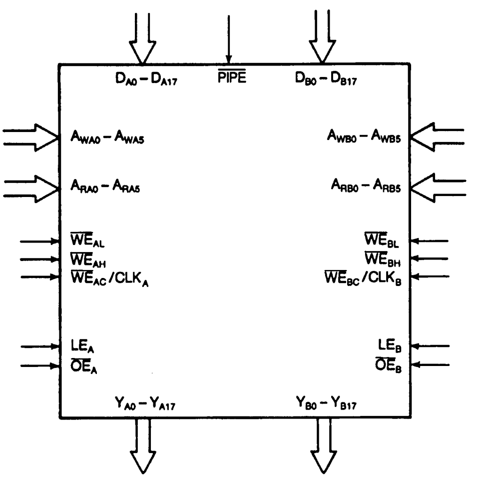
(Sorted by Pin Name)

PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.
			D_{A03}	E02	65	D_{B16}	K13	93	Y_{A05}	N06	21
			D_{A04}	F01	6	D_{B17}	K12	33	Y_{A06}	M06	81
			D_{A05}	F02	66	GND	F03	8	Y_{A07}	L07	22
			D_{A06}	G03	7	GND	J11	37	Y_{A08}	M07	82
A_{RA0}	D02	63	D_{A07}	G02	67	GND	J12	38	Y_{A09}	N07	24
A_{RA1}	C02	62	D_{A08}	G01	9	GND	J13	39	Y_{A10}	N08	84
A_{RA2}	B01	61	D_{A09}	H01	69	GNDA	N05	20	Y_{A11}	M08	25
A_{RA3}	A02	120	D_{A10}	H02	10	GNDA	N09	26	Y_{A12}	L09	85
A_{RA4}	B03	119	D_{A11}	J03	70	GNDA	A09	50	Y_{A13}	M09	86
A_{RA5}	L02	74	D_{A12}	J01	11	GNDA	A05	56	Y_{A14}	L10	27
A_{RB0}	K11	92	D_{A13}	J02	71	LE_A	L01	14	Y_{A15}	M10	87
A_{RB1}	M13	91	D_{A14}	K03	12	LE_B	B12	45	Y_{A16}	N10	28
A_{RB2}	N12	90	D_{A15}	K02	72	$\overline{OE}_A$	L06	23	Y_{A17}	L11	88
A_{RB3}	M11	89	D_{A16}	K01	13	$\overline{OE}_B$	C08	53	Y_{B00}	C03	118
A_{RB4}	M03	77	D_{A17}	L03	73	$\overline{PIPE}$	H03	68	Y_{B01}	A04	58
A_{RB5}	B13	105	D_{B00}	C12	104	V_{CC}	E11	97	Y_{B02}	B04	117
A_{WA0}	D03	3	D_{B01}	C11	44	V_{CC}	E12	98	Y_{B03}	C04	57
A_{WA1}	C01	2	D_{B02}	D13	103	V_{CC}	E13	99	Y_{B04}	B05	116
A_{WA2}	A01	1	D_{B03}	D12	43	V_{CCA}	L08	83	Y_{B05}	C05	115
A_{WA3}	B02	60	D_{B04}	D11	102	V_{CCA}	C06	113	Y_{B06}	B06	55
A_{WA4}	A03	59	D_{B05}	F12	42	$\overline{WE}_{AC}/CLK_A$	M01	75	Y_{B07}	A06	114
A_{WA5}	M02	15	D_{B06}	F13	101	$\overline{WE}_{AH}$	N02	76	Y_{B08}	A07	54
A_{WB0}	L12	32	D_{B07}	C13	41	$\overline{WE}_{AL}$	N01	16	Y_{B09}	B07	112
A_{WB1}	N13	31	D_{B08}	F11	100	$\overline{WE}_{BC}/CLK_B$	A12	106	Y_{B10}	C07	52
A_{WB2}	M12	30	D_{B09}	G11	40	$\overline{WE}_{BH}$	B11	107	Y_{B11}	B08	111
A_{WB3}	N11	29	D_{B10}	G13	96	$\overline{WE}_{BL}$	A11	47	Y_{B12}	A08	51
A_{WB4}	N03	17	D_{B11}	G12	36	Y_{A00}	L04	18	Y_{B13}	B09	110
A_{WB5}	A13	46	D_{B12}	H12	95	Y_{A01}	M04	78	Y_{B14}	C09	109
D_{A00}	D01	4	D_{B13}	L13	35	Y_{A02}	N04	19	Y_{B15}	A10	49
D_{A01}	E03	64	D_{B14}	H13	94	Y_{A03}	L05	79	Y_{B16}	B10	108
D_{A02}	E01	5	D_{B15}	H11	34	Y_{A04}	M05	80	Y_{B17}	C10	48

TABLE OF INTERCONNECTIONS (Cont'd.)
(Sorted by Pin No.)

PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.
			C05	Y_{B05}	115	H02	D_{A10}	10	M05	Y_{A04}	80
			C06	V_{CCA}	113	H03	$\overline{PIPE}$	68	M06	Y_{A06}	81
			C07	Y_{B10}	52	H11	D_{B15}	34	M07	Y_{A08}	82
			C08	$\overline{OE}_B$	53	H12	D_{B12}	95	M08	Y_{A11}	25
A01	A_{WA2}	1	C09	Y_{B14}	109	H13	D_{B14}	94	M09	Y_{A13}	86
A02	A_{RA3}	120	C10	Y_{B17}	48	J01	D_{A12}	11	M10	Y_{A15}	87
A03	A_{WA4}	59	C11	D_{B01}	44	J02	D_{A13}	71	M11	A_{RB3}	89
A04	Y_{B01}	58	C12	D_{B00}	104	J03	D_{A11}	70	M12	A_{WB2}	30
A05	GNDA	56	C13	D_{B07}	41	J11	GND	37	M13	A_{RB1}	91
A06	Y_{B07}	114	D01	D_{A00}	4	J12	GND	38	N01	$\overline{WE}_{AL}$	16
A07	Y_{B08}	54	D02	A_{RA0}	63	J13	GND	39	N02	$\overline{WE}_{AH}$	76
A08	Y_{B12}	51	D03	A_{WA0}	3	K01	D_{A16}	13	N03	A_{WB4}	17
A09	GNDA	50	D11	D_{B04}	102	K02	D_{A15}	72	N04	Y_{A02}	19
A10	Y_{B15}	49	D12	D_{B03}	43	K03	D_{A14}	12	N05	GNDA	20
A11	$\overline{WE}_{BL}$	47	D13	D_{B02}	103	K11	A_{RB0}	92	N06	Y_{A05}	21
A12	$\overline{WE}_{BC}/CLK_B$	106	E01	D_{A02}	5	K12	D_{B17}	33	N07	Y_{A09}	24
A13	A_{WB5}	46	E02	D_{A03}	65	K13	D_{B16}	93	N08	Y_{A10}	84
B01	A_{RA2}	61	E03	D_{A01}	64	L01	LE_A	14	N09	GNDA	26
B02	A_{WA3}	60	E11	V_{CC}	97	L02	A_{RA5}	74	N10	Y_{A16}	28
B03	A_{RA4}	119	E12	V_{CC}	98	L03	D_{A17}	73	N11	A_{WB3}	29
B04	Y_{B02}	117	E13	V_{CC}	99	L04	Y_{A00}	18	N12	A_{RB2}	90
B05	Y_{B04}	116	F01	D_{A04}	6	L05	Y_{A03}	79	N13	A_{WB1}	31
B06	Y_{B06}	55	F02	D_{A05}	66	L06	$\overline{OE}_A$	23			
B07	Y_{B09}	112	F03	GND	8	L07	Y_{A07}	22			
B08	Y_{B11}	111	F11	D_{B08}	100	L08	V_{CCA}	83			
B09	Y_{B13}	110	F12	D_{B05}	42	L09	Y_{A12}	85			
B10	Y_{B16}	108	F13	D_{B06}	101	L10	Y_{A14}	27			
B11	$\overline{WE}_{BH}$	107	G01	D_{A08}	9	L11	Y_{A17}	88			
B12	LE_B	45	G02	D_{A07}	67	L12	$A_{W\ B0}$	32			
B13	A_{RB5}	105	G03	D_{A06}	7	L13	$D_{\ B13}$	35			
C01	A_{WA1}	2	G11	D_{B09}	40	M01	$\overline{WE}_{AC}/CLK_A$	75			
C02	A_{RA1}	62	G12	D_{B11}	36	M02	$A_{W\ A5}$	15			
C03	Y_{B00}	118	G13	D_{B10}	96	M03	A_{RB4}	77			
C04	Y_{B03}	57	H01	D_{A09}	69	M04	Y_{A01}	78			

LOGIC SYMBOL



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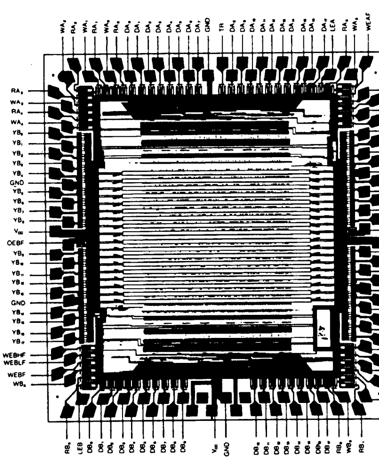
METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C334 -1 G C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
G = 120-Lead Pin Grid Array without Heatsink (CGX120)

b. SPEED OPTION
-1 = Speed Select

a. DEVICE NUMBER/DESCRIPTION
Am29C334
CMOS Four-Port Dual-Access Register File

Valid Combinations	
AM29C334	GC, GCB
AM29C334-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C334 /B Z C

e. LEAD FINISH
C = Gold

d. PACKAGE TYPE
Z = 120-Lead Pin Grid Array without Heatsink (CGX120)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C334
CMOS Four-Port Dual-Access Register File

Valid Combinations	
AM29C334	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_{RA0} - A_{RA5} Read Address A-Side (Input)
The 6-bit read address input selects one of the 64 memory locations for output to the Y_A Data Latch.

A_{RB0} - A_{RB5} Read Address B-Side (Input)
The 6-bit read address input selects one of the 64 memory locations for output to the Y_B Data Latch.

A_{WA0} - A_{WA5} Write Address A-Side (Input)
The 6-bit write address input selects one of the 64 memory locations for writing new data from the D_A input.

A_{WB0} - A_{WB5} Write Address B-Side (Input)
The 6-bit write address input selects one of the 64 memory locations for writing new data from the D_B input.

D_{A0} - D_{A17} Data A-Side (Input)
New data is written into memory from this input, as selected by the A_{WA} address input.

D_{B0} - D_{B17} Data B-Side (Input)
New data is written into memory from this input, as selected by the A_{WB} address input.

GND, V_{CC} Power
Power supply for the internal logic (0, 5 V).

GNDA, V_{CCA} Power
Power supply for the output drivers (0, 5 V).

LE_A Y_A Data Latch Enable (Input, Active HIGH)
The LE_A input controls the latch for the Y_A output port. When LE_A is HIGH, the latch is open (transparent) and data from the RAM, as selected by the A_{RA} address inputs, is passed to the Y_A output. When LE_A is LOW, the latch is closed and it retains the last data read from the RAM. LE_A is disabled in the pipelined mode.

LE_B Y_B Data Latch Enable (Input, Active HIGH)
The LE_B input controls the latch for the Y_B output port. When LE_B is HIGH, the latch is open (transparent), and data from the RAM, as selected by the A_{RB} address inputs, is passed to the Y_B output. When LE_B is LOW, the latch is closed and it retains the last data read from the RAM. LE_A is disabled in the pipelined mode.

$\overline{OE}_A$ Y_A Output Enable (Input, Active LOW)
When $\overline{OE}_A$ is LOW, data in the Y_A Data Latch is driven on the Y_A output. When $\overline{OE}_A$ is HIGH, Y_A output is in the high-impedance (off) state.

$\overline{OE}_B$ Y_B Output Enable (Input, Active LOW)
When $\overline{OE}_B$ is LOW, data in the Y_B Data Latch is driven on the Y_B outputs. When $\overline{OE}_B$ is HIGH, Y_B output is in the high-impedance (off) state.

$\overline{PIPE}$ Pipeline Enable (Input, Active LOW)
When $\overline{PIPE}$ is LOW, the input and output registers are enabled, allowing for pipelined operation. When HIGH, these registers are made transparent.

$\overline{WE}_{AC}$/CLK_A Write Enable A-Side Common (Input, Active LOW)
When $\overline{WE}_{AC}$ is LOW together with $\overline{WE}_{AH}$ or $\overline{WE}_{AL}$, new data is written into the location selected by the AW_A address. When $\overline{WE}_{AC}$ is HIGH, no data is written into the RAM through the A port. $\overline{WE}_{AC}$ acts as a clock input in the pipeline mode for the A side.

$\overline{WE}_{BC}$/CLK_B Write Enable B-Side Common (Input, Active LOW)
When $\overline{WE}_{BC}$ is LOW together with $\overline{WE}_{BH}$ or $\overline{WE}_{BL}$, new data is written into the location selected by the AW_B address. When $\overline{WE}_{BC}$ is HIGH, no data is written into the RAM through the B port. $\overline{WE}_{BC}$ acts as a clock input in the pipeline mode for the B side.

$\overline{WE}_{AH}$ High-Byte Write Enable A-Side (Input, Active LOW)
When $\overline{WE}_{AH}$ is LOW together with $\overline{WE}_{AC}$, new data is written into the high byte of the location selected by the AW_A address input. When $\overline{WE}_{AH}$ is HIGH, no data is written into the high byte.

$\overline{WE}_{BH}$ High-Byte Write Enable B-Side (Input, Active LOW)
When $\overline{WE}_{BH}$ is LOW together with $\overline{WE}_{BC}$, new data is written into the high byte of the location selected by the AW_B address input. When $\overline{WE}_{BH}$ is HIGH, no data is written into the high byte.

$\overline{WE}_{AL}$ Low-Byte Write Enable A-Side (Input, Active LOW)
When $\overline{WE}_{AL}$ is LOW together with $\overline{WE}_{AC}$, new data is written into the low byte of the location selected by the AW_A address input. When $\overline{WE}_{AL}$ is HIGH, no data is written into the low byte.

$\overline{WE}_{BL}$ Low-Byte Write Enable B-Side (Input, Active LOW)
When $\overline{WE}_{BL}$ is LOW together with $\overline{WE}_{BC}$, new data is written into the low byte of the location selected by the AW_B address input. When $\overline{WE}_{BL}$ is HIGH, no data is written into the low byte.

Y_{A0} - Y_{A17} Data Latch (Outputs, Three-State)
The 18-bit Y_A Data Latch outputs.

Y_{B0} - Y_{B17} Data Latch (Outputs, Three-State)
The 18-bit Y_B Data Latch outputs.

FUNCTIONAL DESCRIPTION

The heart of the Am29C334 is a high-speed 64-word by 18-bit dual RAM cell array. Six write enables permit the RAM word to be written in one or both of its 9-bit bytes. Data to be written is presented to each side of the RAM array through the two data ports (D_A and D_B).

The remainder of the logic surrounding the RAM array supports pipelining the RAM access and providing a forwarding path for data around the RAM. This forwarding path is needed to eliminate the latency cycle associated with consecutive write/read accesses to the same memory location in a pipelined system.

Pipelining of the RAM is controlled by the $\overline{PIPE}$ pin. When not asserted (i.e., in non-pipelined mode) the registers on the inputs (write ports $D_{A/B}$, write addresses $A_{WA/B}$, and write enables $\overline{WE}_{AC/BC}$) are made fully transparent, while the registers at the outputs (the read ports $Y_{A/B}$) are turned into latches, controlled by the latch enables $LE_{A/B}$.

In either mode of operation, each side of the RAM is controlled by its individual control signals. This means that the two sides of the RAM can operate at different clock rates to one another. In the pipelined mode, these clock rates must have a known relationship between each other.

In the non-pipelined mode, there is no need for a relationship between the clock rates. Two special cases of operation arise because of this. The first is where the location written to by one side is being read from the other side. In this case, known as A-to-B transparency, the value read is the value being written. The second occurs when two writes to the same location occur at the same time. In this case the value written can not be defined, but the operation is not harmful to the device.

The transparency mode (A-A or B-B) during a write ($\overline{WE}_A$ = LOW) allows the data in (D_A) to not only be written into memory, but also to appear at the output (Y_A) when the output latch (LE_A) is HIGH and the output enable control ($\overline{OE}_A$) is LOW.

Extensions to Four Read Ports and Two Write Ports

A RAM with four read ports and two write ports can be made by using two dual-access RAMs and connecting each of the write ports, write addresses, and write enables in parallel for the two devices. Figure 2 details this in a non-pipelined mode.

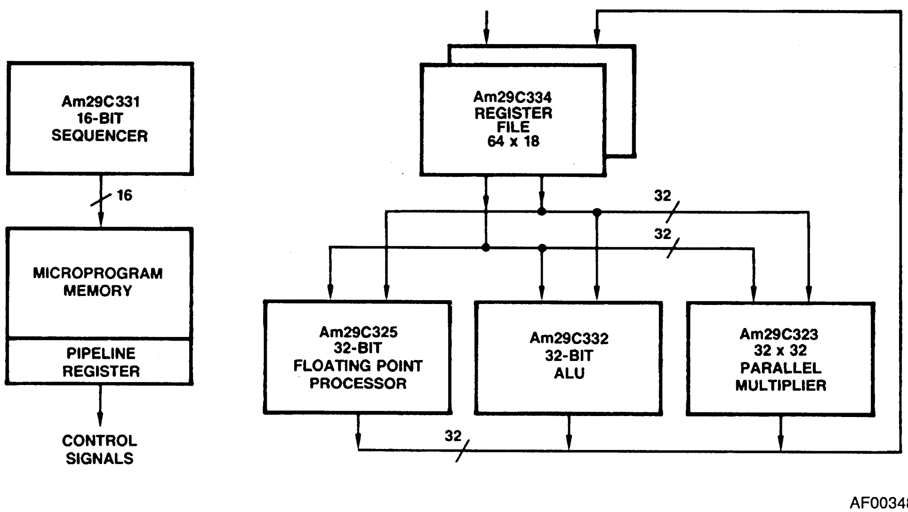


Figure 1. Am29C300 CMOS Family High-Performance System Block Diagram

32 Word x 36 Bit Single-Access RAM

It is possible to convert the 64 word x 18 bit dual-access RAM into a 32 word x 36 bit single-access RAM. This is performed by storing the upper half of the 36 bits in the upper half of the 64 words and addressing these from the A side, and storing the lower half of the 36 bits in the lower half of the 64 words and addressing these from the B side. This arrangement does not change the capacity of the RAM, but the dual access is lost (see Figure 4).

Operational Modes

The Am29C334 may be configured in a non-pipelined mode or in a pipelined mode by controlling the $\overline{PIPE}$ pin. This mode is selected via hardwiring the pin to either LOW or HIGH. This option should not be changed during operation.

Non-Pipelined Data Path

In non-pipelined mode ($\overline{PIPE}$ = 1), the Am29C334 is a flow-through device; data is read out, used, and written back all in the same cycle. In this mode all the registers are made transparent except the registers at the two read ports that are configured as latches. The read port latches are controlled individually by the LE_A and LE_B, so that they are transparent when the latch enables are HIGH and retain the data when the latch enables are LOW. The "forwarding logic" incorporated to support the pipelined mode of operation is also disabled in this mode of operation (specifically, the address comparators are disabled).

In the non-pipelined mode of operation it is possible to simultaneously read two ports, read one port and write to the other, or write to two ports, concurrently. The read and write addresses are internally multiplexed on each side. The selection of the read and write addresses is controlled by the exclusive-OR of the $\overline{PIPE}$ pin and $\overline{WE}_{AC/BC}$. Normally, the $\overline{WE}_{AC/BC}$ are connected to the system clock. With $\overline{PIPE}$ deasserted, the read address will be selected in the high part of the clock cycle ($\overline{WE}_{AC/BC} = 1$) and the write address selected only in the low part. Byte selection for writing on either ports is controlled by the $\overline{WE}_{H/L}$ pins.

Two interesting cases arise as a result of the dual access capability. The first occurs if a location is written into by one side while it is being read out by the other side. In this case, known as A-to-B transparency, the data being written will appear on the read port after the $Transparency_{AB}$ time (if other read access time parameters are met). The second case of interest occurs if both sides write to the same location at the same time. The value written as a result of this operation cannot be defined.

Pipelined Data Path

The Am29C334 can be configured in a pipelined system by asserting the $\overline{PIPE}$ signal ($\overline{PIPE} = 0$) and adding an additional external register in the write address and the write control path on both A and B ports as shown in Figure 3. The registers on each side are controlled by separate clocks that are supplied over the $\overline{WE}_{AC}$ and $\overline{WE}_{BC}$ pins.

Typically, in a pipelined system a read - modify - write would span three cycles. In the second half of the first cycle, a read of the operand(s) is performed and the data is clocked into the output registers at the end of the cycle. In the second cycle, the operation is performed on the operands and the result is clocked into the data register on the write port at the end of the second cycle. In the first half of the third cycle, the data is written to the register file. Therefore, in any cycle, a pipelined system is writing the result of instruction n (in the first half), executing instruction n + 1, and reading the operands needed in instruction n + 2. In any case, a write operation followed by a read operation is performed in the RAM in a cycle.

A special case arises if the data to be written by the previous instruction is needed in the next instruction as an operand. Due to the pipeline register being at its write port, the location is not written into until the next cycle, and hence only the previous value is available in the current cycle. To overcome this problem, "forwarding logic" is included as shown in the block diagram. This logic consists of three elements: an address comparator, an AND gate, and a three-to-one multiplexer, as shown. If the read address of the current instruction is the same as the write address of the previous instruction, and if the result is to be written, then the data to be written is forwarded by the forwarding multiplexer to the output registers. Since there are two write ports, forwarding paths on both ports are provided. As each write port has byte write capability, the forwarding is further broken into the upper and lower bytes.

Since each side has its own $\overline{WE}_C$/CLK control, it is possible to clock each side of the chip differently. However, if the part is used at different frequencies, the forwarding cannot be guaranteed unless the addresses compared are held valid long enough to allow for a comparison to be made and the results of the forwarding setup on the output register.

As mentioned earlier, it is necessary to use an external write address and write control registers in a pipelined system. These registers have not been included for two reasons. First, it is possible for the user to abort the writing before it fills the internal pipe. This situation may arise in cases such as in "traps." Second, by providing an external write address register it provides the flexibility of obtaining the write address from several sources by using an external multiplexer.

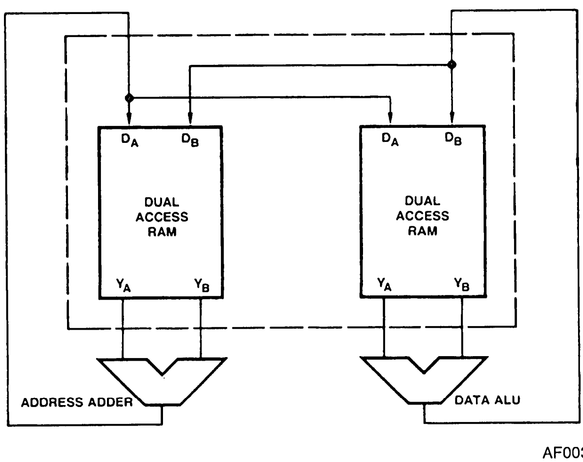


Figure 2. RAM with Four Read Ports and Two Write Ports for Non-pipelined Mode

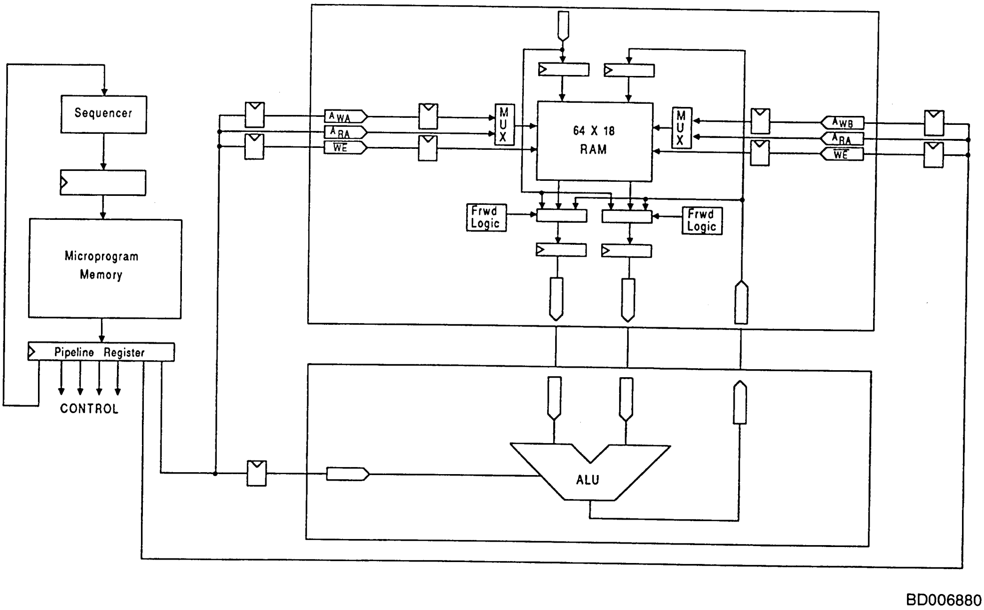


Figure 3. System Diagram With the Am29C334 in a Double Pipelined Data Path

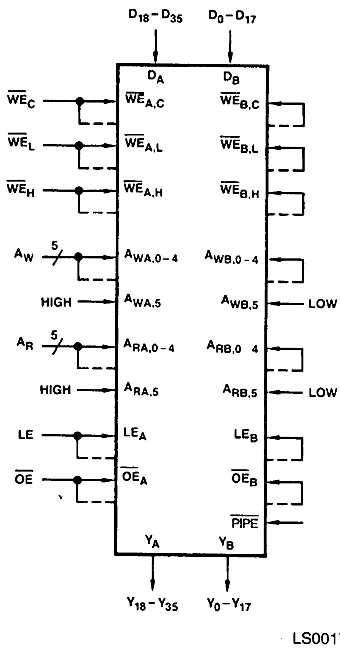


Figure 4. 32 x 36 RAM (Single Access) Using 64 x 18 Dual-Access RAM

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Temperature Under Bias – T_C .... −55 to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.3 to +7.0 V
DC Voltage Applied to Outputs
for HIGH Output State .... −0.3 V to $+V_{CC}+0.3$ V
DC Input Voltage .... −0.3 V to $+V_{CC}+0.3$ V
DC Output Current, Into LOW Outputs .... 30 mA
DC Input Current .... −10 mA to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage .... +4.75 to +5.25 V

Military* (M) Devices
Temperature (T_A) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* Military product 100% tested at T_A = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -4$ mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 8$ mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage (Note 2)		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage (Note 2)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = 0.5 V			−10	μA
I_{IH}	Input HIGH Current	V_{CC} = Max. $V_{IN} = V_{CC} - 0.5$ V			10	μA
I_{OZH}	Off State (High-Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V		10	μA
I_{OZL}			V_O = 0.5 V		−10	
I_{CC}	Static Power Supply Current	$V_{IN} = V_{CC}$ or GND V_{CC} = Max I_O = 0 μA	T_A = −55 to 125°C		80	mA
			T_A = 0 to +70°C		70	mA
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = 5.0 V T_A = 25°C No Load		900 pF Typical		

Notes: 1. V_{CC} conditions shown as Min. or Max. refer to the commercial (±5%) V_{CC} limits.
2. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. C_{PD} determines the no-load dynamic current consumption:
I_{CC} (Total) = I_{CC} (Static) + C_{PD} V_{CC} f, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency. This specification is not tested.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

NON-PIPELINED MODE (Note 1)

No.	Parameter	Description	Test Conditions	29C334		29C334-1		29C334-2		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Access Time	A_{RA} or A_{RB} to Y_A or Y_B	LE_A or LE_B = H		32		26		21	ns
2	Access Time	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to Y_A or Y_B	LE_A or LE_B = H		30		25		20	ns
3	Turn-On Time	$\overline{OE}_A$ or $\overline{OE}_B$ $\downarrow$ to Y_A or Y_B Active		0	20	0	16	0	16	ns
4	Turn-Off Time (Note 2)	$\overline{OE}_A$ or $\overline{OE}_B$ $\uparrow$ to Y_A or Y_B = High Impedance		0	20	0	16	0	16	ns
5	Enable Time	LE_A or LE_B $\uparrow$ to Y_A or Y_B		0	16	0	14	0	14	ns
6	Transparency	$\overline{WE}_A$ or $\overline{WE}_B$ $\downarrow$ to Y_A or Y_B	LE_A or LE_B = H		39		33		27	ns
7	Transparency	D_A or D_B to Y_A or Y_B	LE_A or LE_B = H, $\overline{WE}_A$ or $\overline{WE}_B$ = L		39		33		27	ns
8	Write Recovery Time	A_{RA} or A_{RB} to $\overline{WE}_{AC}$ or $\overline{WE}_{BC}$			(2)-(1)		(2)-(1)		(2)-(1)	ns
9	Data Setup Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B$ $\uparrow$		15		13		13		ns
10	Data Hold Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B$ $\uparrow$		0		0		0		ns
11	Address Setup Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B$ $\downarrow$		2		2		2		ns
12	Address Hold Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B$ $\uparrow$		1		1		1		ns
13	Address Setup Time	A_{RA} or A_{RB} to LE_A or LE_B $\downarrow$		20		17		17		ns
14	Address Hold Time	A_{RA} or A_{RB} to LE_A or LE_B $\downarrow$		1		1		1		ns
15	Latch Close Before Write	LE_A or LE_B to $\overline{WE}_A$ or $\overline{WE}_B$ $\downarrow$		0		0		0		ns
16	Read Before Latch Close	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to LE_A or LE_B $\downarrow$		20		16		16		ns
17	Write Pulse Width	$\overline{WE}_A$ or $\overline{WE}_B$ (LOW)		20		16		16		ns
18	Latch Data Capture Pulse Width	LE_A or LE_B (HIGH)		14		12		12		ns

Notes: See notes following Military table.

SWITCHING CHARACTERISTICS over **MILITARY** operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

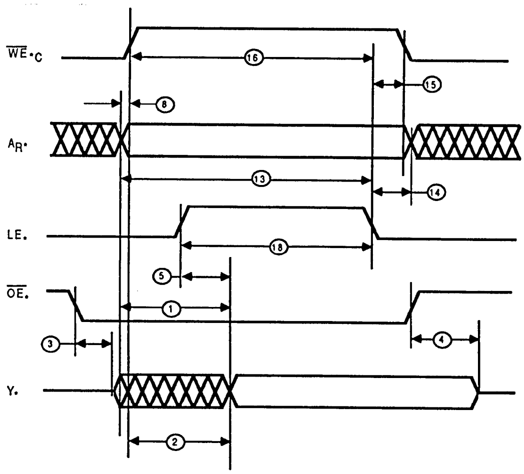
NON-PIPELINED MODE (Note 1)

No.	Parameter	Description	Test Conditions	29C334 Min.	29C334 Max.	Unit
1	Access Time	A_{RA} or A_{RB} to Y_A or Y_B	LE_A or LE_B = H		40	ns
2	Access Time	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to Y_A or Y_B	LE_A or LE_B = H	0	37	ns
3	Turn-On Time	$\overline{OE}_A$ or $\overline{OE}_B$ ↓ to Y_A or Y_B Active		0	16	ns
4	Turn-Off Time (Note 2)	$\overline{OE}_A$ or $\overline{OE}_B$ ↑ to Y_A or Y_B = High Impedance		0	25	ns
5	Enable Time	LE_A or LE_B ↑ to Y_A or Y_B		0	21	ns
6	Transparency	$\overline{WE}_A$ or $\overline{WE}_B$ ↓ to Y_A or Y_B	LE_A or LE_B = H	0	47	ns
7	Transparency	D_A or D_B to Y_A or Y_B	LE_A or LE_B = H, $\overline{WE}_A$ or $\overline{WE}_B$ = L		47	ns
8	Write Recovery Time	A_{RA} or A_{RB} to $\overline{WE}_{AC}$ or $\overline{WE}_{BC}$			(2)-(1)	ns
9	Data Setup Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B$ ↑		19		ns
10	Data Hold Time	D_A or D_B to $\overline{WE}_A$ or $\overline{WE}_B$ ↑		2		ns
11	Address Setup Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B$ ↓		4		ns
12	Address Hold Time	A_{WA} or A_{WB} to $\overline{WE}_A$ or $\overline{WE}_B$ ↑		2		ns
13	Address Setup Time	A_{RA} or A_{RB} to LE_A or LE_B ↓		23		ns
14	Address Hold Time	A_{RA} or A_{RB} to LE_A or LE_B ↓		1		ns
15	Latch Close Before Write	LE_A or LE_B to $\overline{WE}_A$ or $\overline{WE}_B$ ↓		0		ns
16	Read Before Latch Close	$\overline{WE}_{AC}$ or $\overline{WE}_{BC}$ to LE_A or LE_B ↓		24		ns
17	Write Pulse Width	$\overline{WE}_A$ or $\overline{WE}_B$ (LOW)		23		
18	Latch Data Capture Pulse Width	LE_A or LE_B (HIGH)		17		ns

Notes: 1. $\overline{WE}_A = \overline{WE}_{AC} + \overline{WE}_{AL/H}$
$\overline{WE}_B = \overline{WE}_{BC} + \overline{WE}_{BL/H}$
2. Y_A and Y_B are tested independently.
3. Minimum delays are not tested.

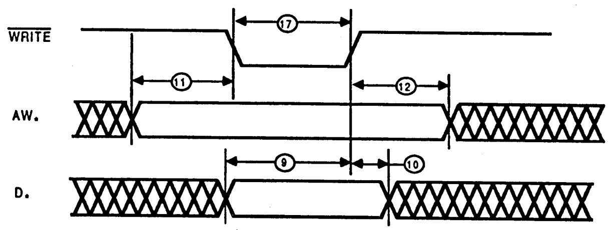
SWITCHING WAVEFORMS

NON-PIPELINED MODE



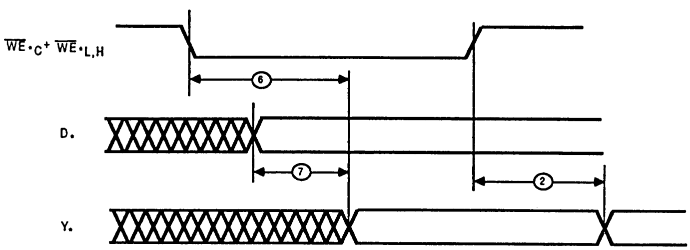
WF023330

Read Function (* means A or B)



WF023340

Write Function (* means A or B)



WF023320

Transparency

NOTE: LE* = HIGH
OE* = LOW
* means A or B

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cont'd.)

PIPELINED MODE

No.	Parameter	Description	29C334		29C334-1		29C334-2		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
19	Write Data Setup Time	D_A or D_B to CLK_A or CLK_B ↑	15		13		13		ns
20	Write Data Hold Time	D_A or D_B to CLK_A or CLK_B ↑	1		1		1		ns
21	Write Address Setup Time	A_{WA} or A_{WB} to CLK_A or CLK_B ↑	23		20		20		ns
22	Write Address Hold Time	A_{WA} or A_{WB} to CLK_A or CLK_B ↑	0		0		0		ns
23	Write Enable Setup Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B ↑	20		16		16		ns
24	Write Enable Hold Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B ↑	0		0		0		ns
25	Read Address Setup Time	A_{RA} or A_{RB} to CLK_A or CLK_B ↑	24		20		20		ns
26	Read Address Hold Time	A_{RA} or A_{RB} to CLK_A or CLK_B ↑	0		0		0		ns
27	Minimum Clock Cycle	CLK_A or CLK_B (LOW)	50		40		40		ns
28	Minimum Clock Pulse	CLK_A or CLK_B (HIGH)	17		14		14		ns
29	Minimum Clock Pulse	CLK_A or CLK_B (LOW)	17		14		14		ns
30	Clock to Y	Y_A or Y_B to CLK_A or CLK_B	14		12		10		ns

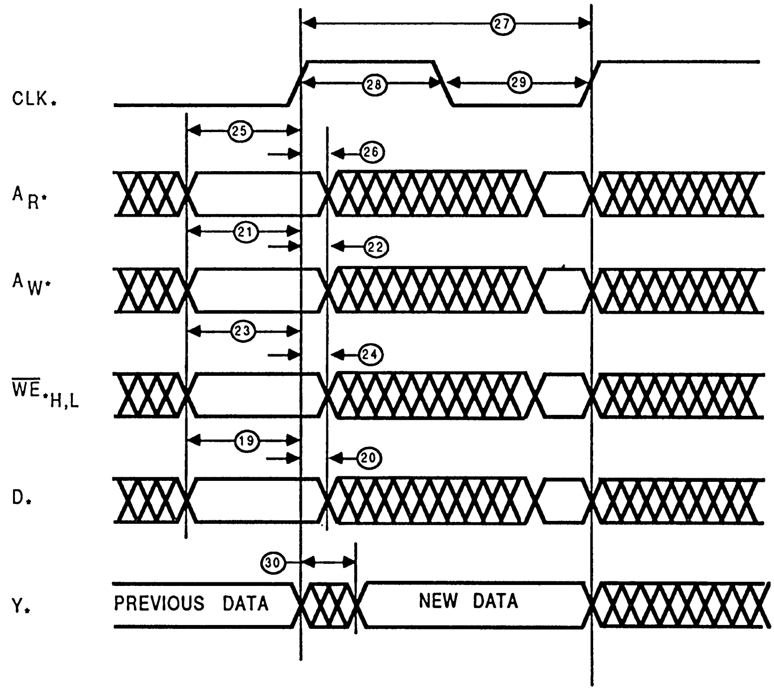
SWITCHING CHARACTERISTICS over MILITARY operating range (Cont'd.)

PIPELINED MODE

No.	Parameter	Description	29C334 Min.	29C334 Max.	Unit
19	Write Data Setup Time	D_A or D_B to CLK_A or CLK_B ↑	19		ns
20	Write Data Hold Time	D_A or D_B to CLK_A or CLK_B ↑	2		ns
21	Write Address Setup Time	A_{WA} or A_{WB} to CLK_A or CLK_B ↑	27		ns
22	Write Address Hold Time	A_{WA} or A_{WB} to CLK_A or CLK_B ↑	2		ns
23	Write Enable Setup Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B ↑	23		ns
24	Write Enable Hold Time	$\overline{WE}_H$ or $\overline{WE}_L$ to CLK_A or CLK_B ↑	2		ns
25	Read Address Setup Time	A_{RA} or A_{RB} to CLK_A or CLK_B ↑	28		ns
26	Read Address Hold Time	A_{RA} or A_{RB} to CLK_A or CLK_B ↑	0		ns
27	Minimum Clock Cycle	CLK_A or CLK_B (LOW)	55		ns
28	Minimum Clock Pulse	CLK_A or CLK_B (HIGH)	20		ns
29	Minimum Clock Pulse	CLK_A or CLK_B (LOW)	20		ns
30	Clock to Y	Y_A or Y_B to CLK_A or CLK_B	18		ns

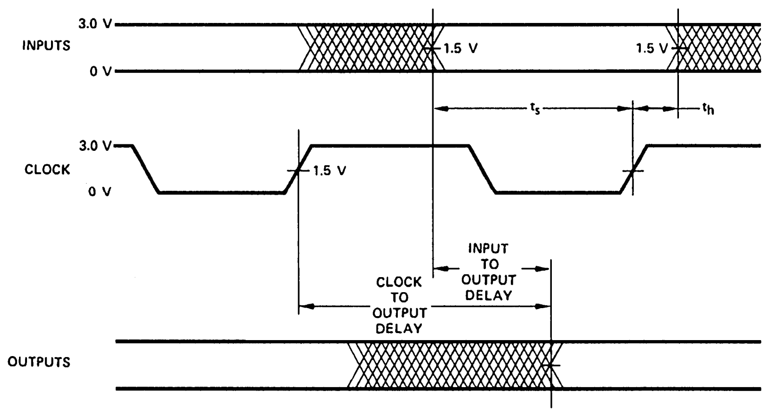
SWITCHING WAVEFORMS (Cont'd.)

PIPELINED MODE



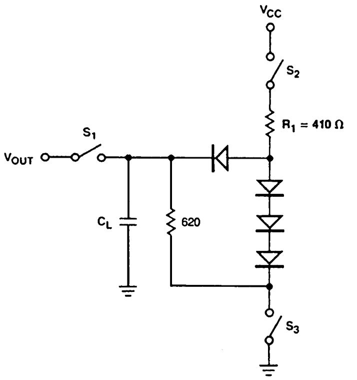
WF023310

* means A or B



WFR02990

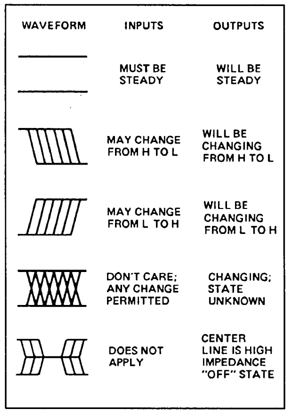
SWITCHING TEST CIRCUIT



TC003424

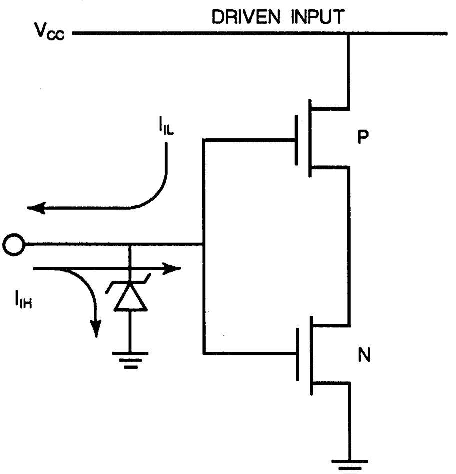
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during functions tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test. S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = TBD for output disable tests.

KEY TO SWITCHING WAVEFORMS



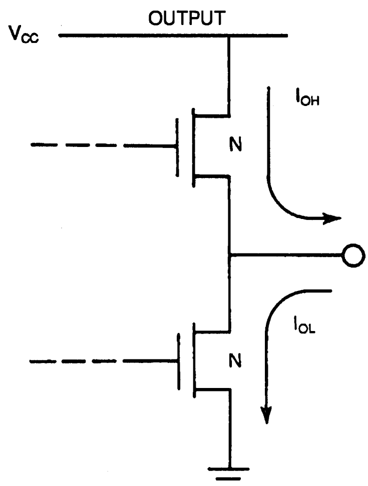
KS000010

INPUT/OUTPUT CIRCUIT DIAGRAMS



IC000861

$C_I \approx 5.0$ pF, all inputs

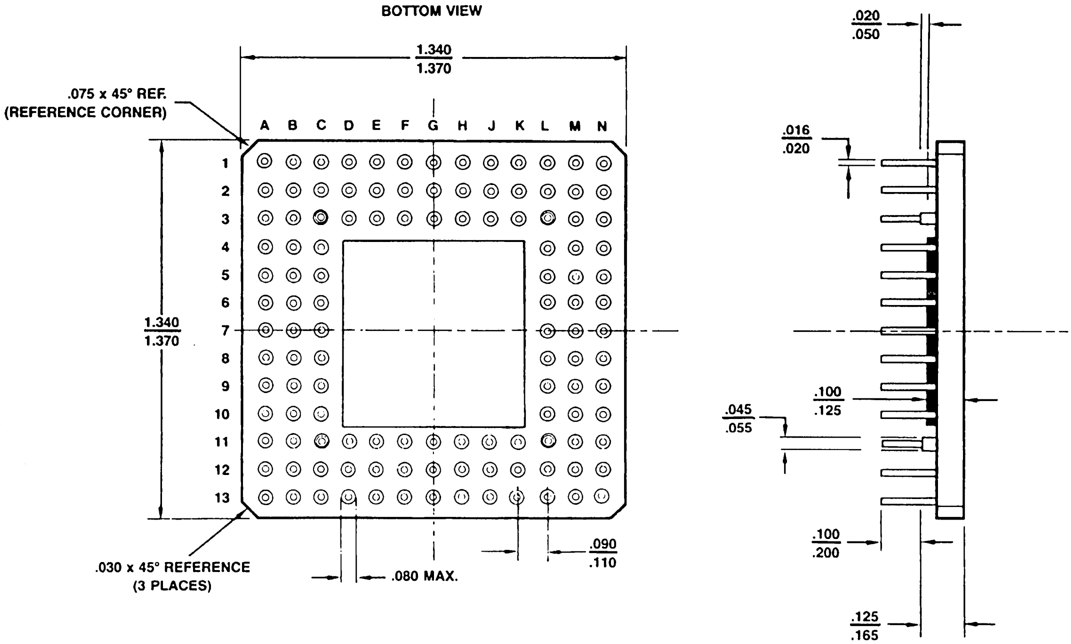


IC000870

$C_O \approx 5.0$ pF, all outputs

PHYSICAL DIMENSIONS*

CGX120



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* For reference only.

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Printed in U.S.A. AIS-WCP-13.5M-9/87-0