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ER_R4B1
Product Advisory

October 15, 1998

Rage 128 Rev A13 Errata & Branding

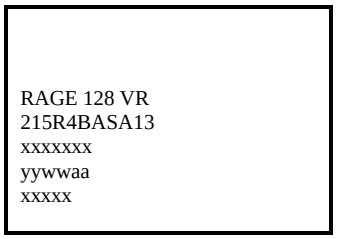
The RAGE 128 VR and RAGE 128 GL represent ATI's latest high performance 128-bit graphics and multimedia accelerators. The RAGE 128 VR supports a 64-bit memory interface, while the RAGE 128 GL supports a 128-bit memory interface. Devices at the A13 revision level are engineering samples, and are provided for evaluation only. The A13 is not a production part. Note that the A13 revision level is extracted from the last three digits of the ATI part number. This product advisory describes the errata and the branding information for the A13 revision. The errata applies equally to the VR and GL variants of the RAGE 128.

#	Errata Description	Workaround and Implications	Fix Schedule
1	Screen corruption may be visible due to a write operation failure in the pixel cache. This is due to a sensitivity within the pixel cache resulting from potential Pchan/Nchan transistor mismatches (process variations).	This sensitivity in the A13 is reduced by decreasing the operating frequency and/or increasing the core voltage. However, some A13 samples do function properly at nominal voltages and up to 80-90MHz engine clock.	The pixel cache errata has been fixed in the Rage128 A21 by decreasing the size of the Nchan transistors of the storage cells to make them switch properly.
2	Cross allocation of resources between different requestors (i.e., host/2d/3d/…) within the pixel cache can result in deadlocks and hangs.	Temporary software workarounds have been implemented to do various checking and purging/flushing of the pixel cache in order to avoid potential deadlocks. Some of these software workarounds have an impact on performance.	Deadlock conditions have been isolated, and the pixel cache control logic has been fixed in the Rage128 A21.
3	Low Vil threshold voltage on AGP and GPIO pads. Depending on the amount of noise and ground bounce in the system, artifacts can occur on the overlay/tvout (GPIO) interface. Corrupt data/operation on the AGP/PCI interface could potentially result in a hang.	By temporarily increasing the core voltage from 2.5 to 2.8v with A13, Vil is increased which in turn reduces sensitivity to ground bounce at the chip IO level.	The Vil for the AGP/PCI and GPIO pads has been re-adjusted in the Rage128 A21 to provide a higher noise immunity.
4	The DP_WRITE_MASK function/register affects the Z-plane. This can cause a failure in one of the OpenGL CDRS conformance tests.	Workaround under investigation	This has been fixed in the Rage128 A21. DP_WRITE _MASK does not affect the Z plane.

5	The Rage 128 requires a 128 MB of memory aperture which needs to be allocated by the system. In some cases, the system can not allocate this amount of aperture (which is actually due to errors within the system bios).	Reducing the aperture requirement of the system to 64 MB (option available through the CMOS settings of some systems) or by getting a system bios upgrade are possible workarounds.	The Rage 128 memory aperture requirement visible to the system has been reduced to 64 MB in the Rage128 A21
6	In 33MHz PCI implementations, the PCI 66MHz capability bit is set to 1. This should not cause any problems. However, according to the PCI spec, it may result in a warning being issued by the system.	No workaround - this errata should not cause any problems.	This has been fixed in the Rage 128 A21
7	The nandtree IO test structure does not work properly. This is due to the fact that the PU control pins of the IO pads require a higher than standard drive strength in order to be driven and switched properly.	By temporarily increasing the core supply voltage (around 3v) and decreasing the IO supply voltage (around 2v) the nandtree IO test structure can be made to work (this is not a practical workaround, it just proves the failure mechanism).	This has been fixed in the Rage 128 A21 by implementing buffers with appropriate strength to drive the IO pads PU ctrl pins.
8	An inefficiency in the A13 memory arbitration/sequencing logic has been identified.	There are no bugs or failures caused by this errata.	The implementation of this logic has been corrected in the Rage128 A21 in order to optimize the memory bandwidth utilization and therefore further improve performance.

Branding Summary for Revision A13

RAGE 128 VR
272 BGA package



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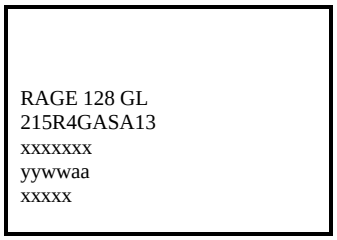
RAGE 128 GL
328 BGA package



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Document Revision History
The document revisions are tracked by the last digit in the document number. As modifications are made, the trailing digit is incremented. The listing below identifies the document number, date of release, and the changes made.

ER_R4B1 October 15, 1998, Initial release of the A13 errata and branding advisory.

Please contact your field applications engineer or technical representative if you have any questions about this advisory.