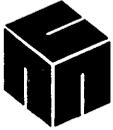




**C-CUBE MICROSYSTEMS**

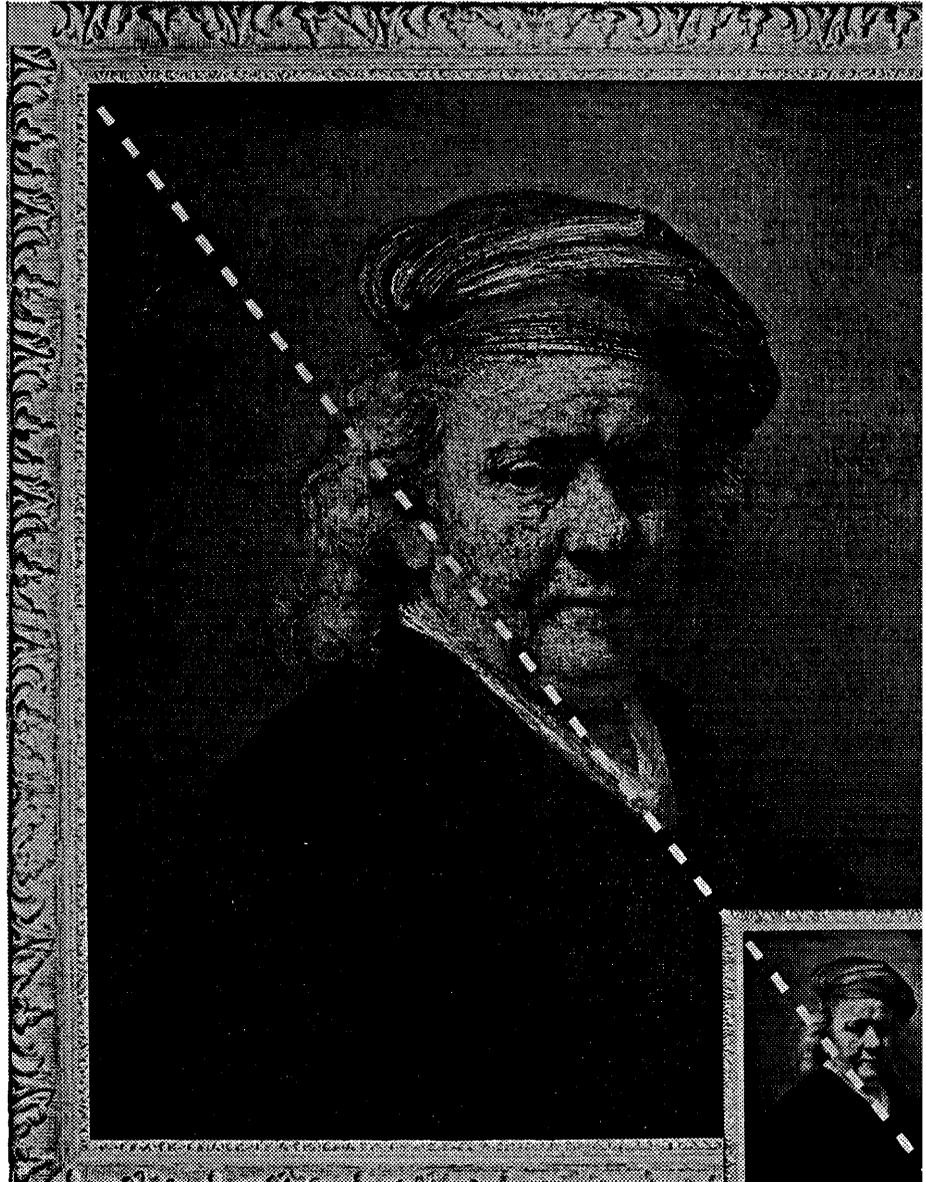
**C-CUBE  
JPEG STILL IMAGE (SI-1)  
BOARD DESIGN  
TECHNICAL MANUAL**





**C-CUBE MICROSYSTEMS**

**C-CUBE  
JPEG STILL IMAGE (SI-1)  
BOARD DESIGN  
TECHNICAL MANUAL**



**This document is preliminary. The specifications contained herein are derived from functional specifications and performance estimates, and have not been verified against production parts.**

**C-Cube Microsystems reserves the right to change any products described herein at any time and without notice. C-Cube Microsystems assumes no responsibility or liability arising from the use of the products described herein, except as expressly agreed to in writing by C-Cube Microsystems. The use and purchase of this product does not convey a licence under any patent rights, copyrights, trademark rights, or any other intellectual property rights of C-Cube Microsystems.**

**Trademark Acknowledgment:**

**C-Cube Still Image Board, C-Cube SI-1 Board, C-Cube Still Image Utility, and C-Cube CL550, are trademarks of C-Cube Microsystems. The corporate logo is a registered trademark of C-Cube Microsystems.**

**IBM and PC AT are trademarks of International Business Machines.**

**80386 and 80486 are registered trademarks of Intel Corp.**

**Windows is a trademark of Microsoft Corporation.**

**© C-Cube Microsystems 1992**

**All rights reserved**

**C-Cube Microsystems  
1778 McCarthy Boulevard  
Milpitas, CA 95035  
Telephone (408) 944-6300  
Fax (408) 944-6314**

# Preface

This application note provides detailed information about the C-Cube JPEG Still Image (SI-1) board design. It includes a complete technical description of the design including bus and chip timing, state machine state diagrams, schematics, PAL Equations, and a sample bill of materials.

This manual is intended for:

- System designers and managers who are evaluating the CL550 for possible use in a system
- Designers and hardware engineers who are designing a system based on the CL550
- Designers and hardware engineers who wish to produce a clone of the SI-1 board design
- Programmers and software engineers who are writing application programs that interact with the CL550 and SI-1 board

---

**Audience**

---

---

## **Organization**

---

This application note is divided into three chapters, and includes three appendices:

- Chapter 1: Introduction
- Chapter 2: Theory of Operation
- Chapter 3: Hardware Description
- Appendices
  - Appendix A: Schematics
  - Appendix B: PAL Equations
  - Appendix C: Bill of Materials

The JPEG standard is described in detail in *JPEG Still Picture Compression Algorithm*, October 15, 1991. This document is available from the C-Cube Microsystems Marketing Department.

Detailed information on the installation and operation of the SI-1 board and its associated software is available in the “*Still Image (SI-1) Board Users Manual*” (C-Cube Publication # 92-1502-001). This document is available from the C-Cube Microsystems Marketing Department.

Detailed information on the JPEG File Interchange Format (JFIF) is provided in “*JPEG File Interchange Format Version 1.01*”. This document is available from the C-Cube Microsystems Marketing Department.

Detailed information on JPEG Device Independent Bitmap file formats can be found in “*JPEG DIB File Formats*”. This document is available from the C-Cube Microsystems Marketing Department.

Detailed information on the CL550 Compression Processor is provided in the *C-Cube CL550 JPEG Image Compression Processor Data Book* (C-Cube Publication #90-1150-203). This document is available from the C-Cube Microsystems Marketing Department.

Detailed information on Microsoft defined Windows file structures can be found in the *Microsoft Windows Software Development Kit Programmers Reference. Volume 3: Messages, Structures and Macros*.

Detailed information on Windows graphics function calls can be found in the *Microsoft Windows Software Development Kit Programmers Reference. Volume 2: Functions*.

**Notice:**

*At the time that this application note was written, the JPEG Still Frame Board had not yet gone through comprehensive compatibility testing. Although it is believed that the design is sound, minor changes to the P.C. bus timing may occur if incompatible computers are found. If problems are encountered, contact C-Cube technical support for the latest information and PAL equations.*

# Table of Contents

## Section I. General Information

### Chapter 1 Introduction

- 1.1 Design Kit Options 1-2
- 1.2 Additional Information 1-2

### Chapter 2 Theory of Operation

- Theory of Operation 2-1

### Chapter 3 Configuration and Installation

- 3.1 Address Decoder 3-2
- 3.2 Clock Generation 3-4
- 3.3 Host Bus Interface 3-5
- 3.4 Pixel Bus Interface 3-13

## Section II. Appendices

### Appendix A Schematics

- Schematics A-1

### Appendix B PAL Equations

- PAL Equations B-1

### Appendix C Bill of Materials

- Bill Of Materials C-1

# Figures and Tables

<b>Figure 2-1</b>	<b>Detailed Block Diagram</b>	<b>2-3</b>
<b>Figure 3-1</b>	<b>Clock Generator Timing Diagram</b>	<b>3-4</b>
<b>Figure 3-2</b>	<b>START- State Diagram</b>	<b>3-5</b>
<b>Figure 3-3</b>	<b>Host Bus Register Write Timing</b>	<b>3-7</b>
<b>Figure 3-4</b>	<b>Host Bus Register Read Timing</b>	<b>3-10</b>
<b>Figure 3-5</b>	<b>Toggle State Machine State Diagram</b>	<b>3-14</b>
<b>Figure 3-6</b>	<b>STALL- Operation: Compression</b>	<b>3-15</b>
<b>Figure 3-7</b>	<b>STALL- Operation: Decompression</b>	<b>3-15</b>
<b>Figure 3-8</b>	<b>STALL- Handshake Operation For Compression</b>	<b>3-17</b>
<b>Figure 3-9</b>	<b>STALL- Handshake Operation For Decompression</b>	<b>3-20</b>
<b>Table 3-1</b>	<b>Base Address Jumper Positions</b>	<b>3-3</b>
<b>Table C-1</b>	<b>JPEG Still Image Board Bill of Materials</b>	<b>C-2</b>

# Chapter 1

## Introduction

This application note describes the design of the C-Cube JPEG Still Image (SI-1) board. The SI-1 board is designed for use in an IBM PC or PC clone based on the Industry Standard Architecture (ISA) bus. It contains a C-Cube CL550 JPEG compression processor which is mapped into the PC's I/O space.

This purpose of this application note is to provide the hardware designer enough information to either clone this design directly, or use this design as a starting point for a more complex JPEG compression processor board design.

This application note is divided into three chapters and three appendices:

1. Introduction: Introduction and additional information
2. Hardware Theory of Operation: Block level description of the circuitry on the board
3. Hardware Description: Detailed description of the hardware blocks, state diagrams and timing diagrams
4. Appendices

---

### 1.1 Design Kit Options

---

To make it easier for you to reproduce boards based on this design, C-Cube offers two design kits:

1. **Development Kit:** A complete kit of information for either the hardware designer who is going to design a board similar to the SI-1 or the software designer who is going to write CL550 drivers. This kit includes:
  - A tested, working reference board
  - A copy of the SI-1 Users Guide
  - A copy of the SI-1 Product Brief
  - The Microsoft Windows based JPEG Still Image Utility
  - Source code for the Windows based JPEG Still Image Utility
  - Some sample compressed images for testing and demonstration purposes
  - A copy of the CL550 Monitor/Debugger (runs under DOS)
  - A copy of the SI-1 application note (this note)
2. **Manufacturing Kit:** A complete kit of information for the hardware designer who wishes to produce copies of the SI-1 board. This kit includes everything listed in the Development Kit above plus:
  - Gerber photoplot files and fabrication drawings for producing the SI-1 printed circuit board.

Pricing and delivery information on these design packages is available from your local C-Cube sales representative. There is a list of these sales representatives at the end of this note.

---

### 1.2 Additional Information

---

For additional information on the SI-1 board and JPEG compression in general, refer to the following documents:

- JPEG Still Image Board Users Manual, C-Cube P/N 92-1502-001
- CL550 Databook, C-Cube part number 90-2250-203
- JPEG Still Picture Compression Algorithm, Baseline Process (available from C-Cube marketing, C-cube P/N 90-3503-001)

# **Chapter 2**

## **Theory of Operation**

**This chapter describes the theory of operation of the JPEG Still Image Board (SI-1) at the block diagram level. It shows the block diagram of the board, and describes the path the data uses in both compression and decompression modes.**

**The purpose of this chapter is to give the user a basic overview of the operation of the JPEG Still Image Board. Understanding what each section does will aid in understanding the detailed technical description in the next chapter.**

The JPEG Still Image Board, or SI-1 board, is a JPEG compression/decompression accelerator card that uses the C-Cube CL550 JPEG compression processor. The CL550 is the heart of the SI-1 board, and all compression and decompression operations take place within the processor itself. The other 14 integrated circuits on the board simply connect the CL550 to the ISA (IBM PC AT) bus and provide status and control signals.

The SI-1 compression board design has a single 10-MHz CL550 processor, two sets of bus transceivers and latches, control logic and clock circuitry. Figure 2-1 shows a block diagram of the board. This board design uses the CL550 in the still-frame mode. In this mode, the host (PC) processor reads and writes data to and from the CL550 processor, but the CL550 is not connected to a display device. The strip buffer is also not used.

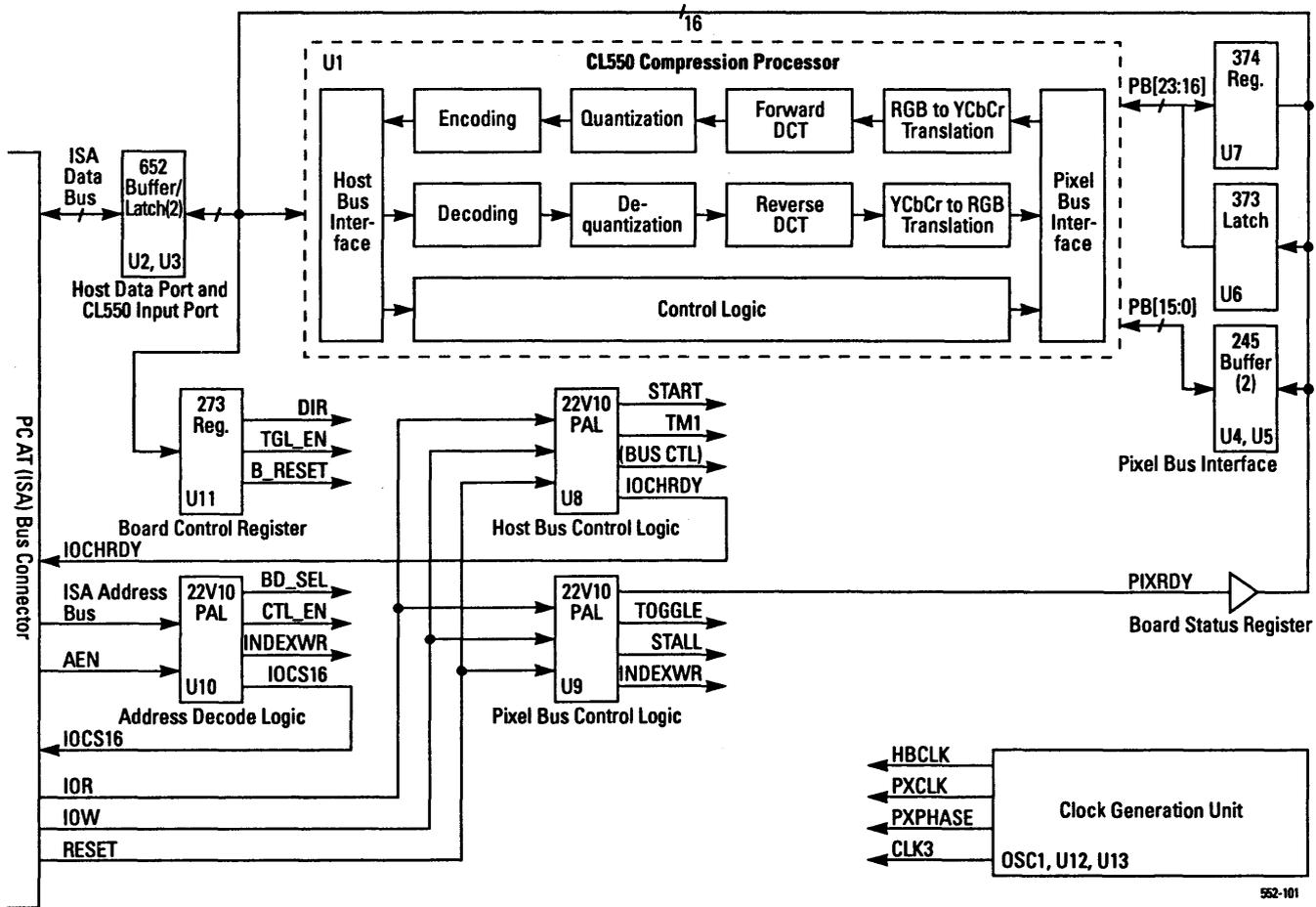
Data can be transferred in any of the following modes:

- From a disk file to a disk file
- From a disk file to memory
- From memory to a disk file
- From memory to memory

The CL550 decompression processor has two buses. The 16-bit Host bus is used for programming the CL550 during the initialization process and for loading and unloading JPEG compressed data during operation. The 24-bit Pixel bus is used to transfer uncompressed pictures to and from the processor. Both buses are connected to the 16-bit ISA Data bus.

When the CL550 is compressing or decompressing 24 bit RGB data, the 24-bit Pixel bus expects data reads and writes to be 24 bits wide, but the ISA bus only supports 16-bit transfers. To overcome this bus width mismatch, latches have been added to store the extra eight bits of data.

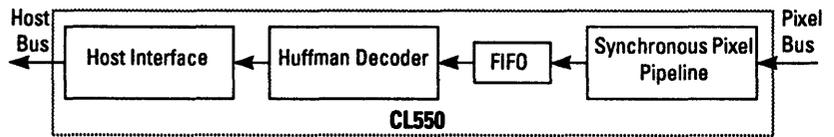
When the pixel port is read, the lower 16 bits of the Pixel bus, PD[15:0], are enabled onto the ISA data bus, and the upper eight bits of the Pixel bus, PD[32:16], are stored in latch U7. The host processor accesses the upper eight bits by reading the pixel port a second time. Logic in the PALs automatically enables the latched data onto the ISA Data bus.



**Figure 2-1 Detailed Block Diagram**

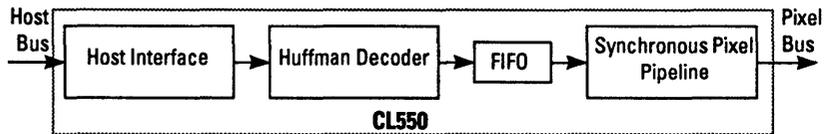
When the Pixel port is written, the host processor must make two sequential writes. The first write stores the upper eight bits of pixel data into latch U6. When the second write is made, a reassembled 24-bit word made up of eight bits from the latch and 16 bits from the host data bus is strobed into the CL550 Pixel port.

During compression operations, uncompressed pixel data is written to the Pixel port, and compressed data is read from the host-bus data port as shown in Figure 2-2.



**Figure 2-2 Compression Data Flow**

During decompression operations, compressed data is written to the host-bus data port, and uncompressed data is read from the Pixel port as shown in Figure 2-3.



**Figure 2-3 Decompression Data Flow**

The remaining logic on the board is the clock generation circuit and some control logic for decoding the board address and controlling the bus buffers.

# Chapter 3

## Hardware Description

This chapter presents a detailed description of the various components of the JPEG Still Image (SI-1) board, using the schematic and PAL equations as references. The schematics are located in Appendix A of this document, and the PAL equations are located in Appendix B.

The purpose of this chapter is to give the designer a thorough understanding of the design of the SI-1 board. The purpose of every integrated circuit on the board is discussed, and the timing of the ISA bus interface signals is described in detail. The state machines implemented in the PALs are described and state maps are provided.

The four sections of this chapter are:

- Section 3.1, Address Decoder
- Section 3.2, Clock Generation
- Section 3.3, Host Bus Interface
- Section 3.4, Pixel Bus Interface

---

**3.1**  
**Address Decoder**

---

The SI-1 board is mapped into eight locations in the PC's I/O address space. Four I/O ports are used to configure and communicate with the board. The address of these ports is determined by taking the base address of the board and adding an offset value for the specific port being addressed:

**CL550 Host Data Port**

**Base + 0**

The host processor uses this 16 bit read/write port to pass data to and from the CL550s registers. The data to be passed includes programming and status information, and JPEG compressed data.

**CL550 Index Register**

**Base + 2**

This 16-bit write-only register stores the address of the CL550 register being addressed. To access a CL550 register, the program must first load the CL550 register index value into this port.

**Control / Status Register**

**Base + 4**

This I/O location functions as the Control register during an I/O write, and the Status register during an I/O read. The Control / Status register is 8-bits wide, but only three bits are used in the control register, and one bit in the status register. They are:

- **Control Bit 0: Direction.** The host processor writes a 0 to this bit to configure the board for compression, and a 1 to configure the board for decompression.
- **Control Bit 1: Toggle Enable.** The host processor sets this bit to a 1 to enable the CL550 to transfer 24-bit pixel data.
- **Control Bit 7: Reset.** The host processor sets this bit to a 1 to force the CL550 into a hardware reset condition, and sets it to a 0 to release the reset. A reset is performed immediately after power-up and each time the operating mode is changed.
- **Status Bit 0: Pixel Port Status.** The host processor monitors this bit to determine the status of the CL550s Pixel Port. When the Pixel Port Status bit is a 1, the CL550 is ready to input or output data.

Unused bit should be set to 0 when writing the register, and will return indeterminate data when reading the register.

**Pixel Port****Base + 6**

The host uses this 16-bit read/write port to transfer pixel data to and from the CL550. When the board is configured for 24-bit pixel mode (Toggle Enable set to 1), two accesses are required to transfer a pixel. The first access will read or write the high byte (bits 23-16) of the pixel bus using the lower 8 bits of the data bus. The second access will read or write the lower word (bits 15 - 0) of the pixel bus.

The base address of the board is set using three jumpers. Table 3-1 lists the allowable base address configurations for the board.

**Table 3-1 Base Address Jumper Positions**

JP1	JP2	JP3	Base Address (Hex)
2-3	2-3	2-3	0x0300 <sup>1</sup>
1-2	2-3	2-3	0x0320
2-3	1-2	2-3	0x0340
1-2	1-2	2-3	0x0360
2-3	2-3	1-2	0x0380
1-2	2-3	1-2	0x03A0
2-3	1-2	1-2	0x03C0
1-2	1-2	1-2	0x03E0

1. Default Configuration

The address decoder, shown on Page 4 of the schematic, consists of two parts. NOR gates U14A and U14B detect that the upper six bits of the address bus are zero. Address decoder PAL U10 decodes nine of the lower ten bits and compares the results to the base address select jumpers. If the addresses match, then the board select signal (BD\_SEL-) is generated. Note that to save logic, the least significant bit of the address is not decoded.

The signal CTL\_WR- (also called CTL\_EN-) is generated whenever the host processor accesses address Base + 2. It is used to strobe the contents of the host data bus into the Board Control Register U11. IOCS16- is generated whenever the host processor accesses any port on the SI-1 board. This signal indicates to the ISA bus that a 16-bit wide transfer is in process.

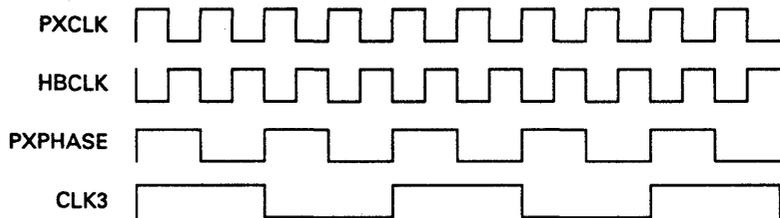
---

**3.2**  
**Clock Generation**

---

The SI-1 board contains its own clock generation circuitry. This circuit is shown on Page 5 of the schematic. Crystal oscillator OSC1 generates a 10MHz symmetrical square wave that is buffered by U12A and U12B. U13A and U13B divide the clock by four giving 5MHz and 2.5MHz outputs.

The buffered oscillator signal PXCLK is used as the CL550 Pixel Clock. The 5MHz output drives the CL550 PXPULSE clock signal and the 2.5MHz output drives the CL550 CLK3 clock signal. HBCLK is the inverse of the Pixel clock signal PXCLK and is used to clock the PALS and to synchronize host bus transfers. Figure 3-1 shows the timing diagram for this circuit and shows the relationships between the four outputs.

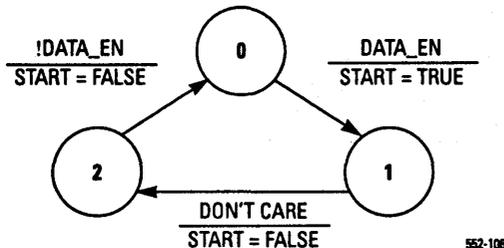


**Figure 3-1** Clock Generator Timing Diagram

### 3.3 Host Bus Interface

The host bus interface, shown on Page 3 of the schematic, is designed to support CL550 slave mode transfers only. The data bus interface consists of two 74LS652 Octal bus transceiver/registers (U2 and U3) which act as both the index port and the host data port. A PAL controls these buffers during a transfer. When a slave mode transfer is performed, the host processor must first write the address of the register being accessed into the index port. In a separate operation, it must perform a read or write of the data port. At the time of the data port read or write, logic in the HBUSCTL PAL U8 (Schematic Page 4) generates the signals necessary to complete a slave mode transfer.

Control logic for the host bus interface resides in the HBUSCTL PAL, U8. Equations for this PAL, in ABEL format, are listed in Appendix B. All of the logic within the PAL is combinatorial except the logic that generates the START- signal. This output is controlled by a two bit state machine. The state diagram for the generation of START- is shown in Figure 3-2.



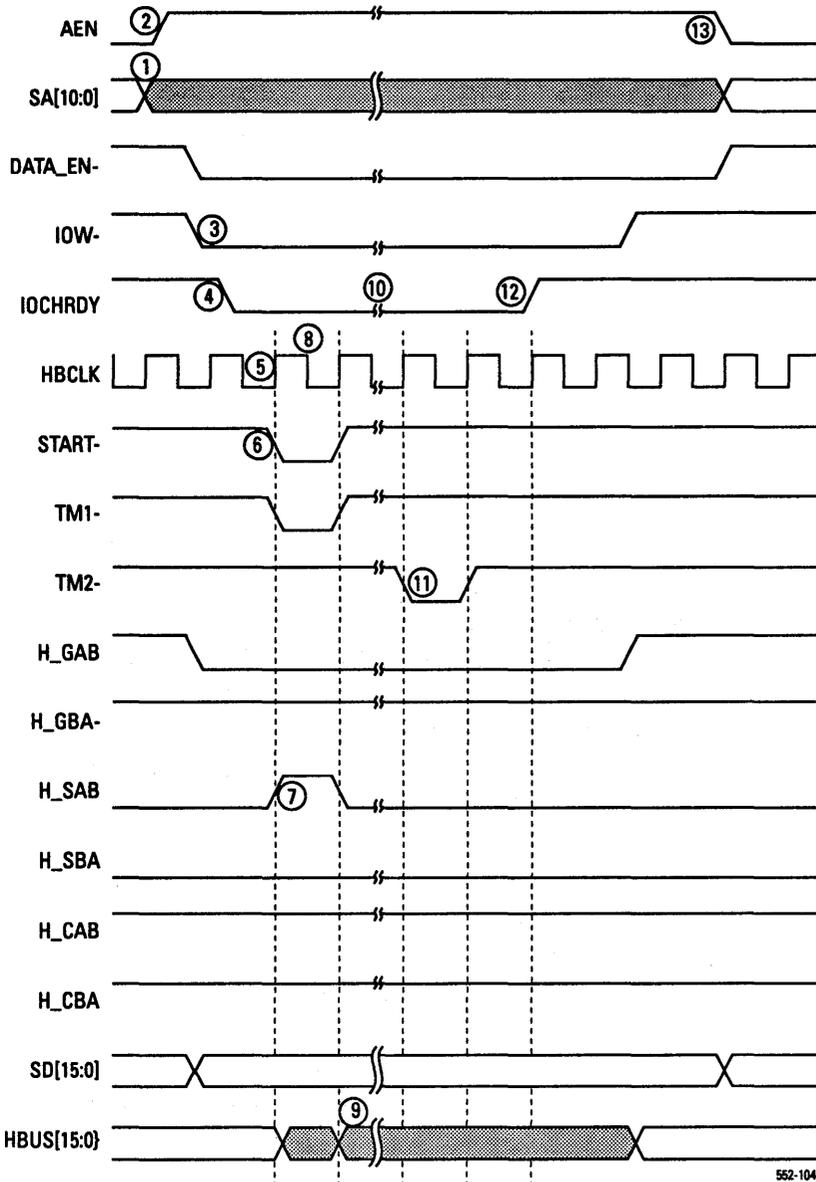
**Figure 3-2** START- State Diagram

The control logic for the Host bus adds ISA bus wait states whenever necessary. Accessing the CODEC register incorrectly or at the wrong time can result in generation of a number of wait states that exceeds the ISA bus maximum allowable wait state specification. As a worst-case condition, the CL550 could simply never return an acknowledge (TM2-) which would cause the ISA bus to hang. There is no timeout mechanism in this design. Proper usage of the CODEC register is described in the CL550 databook, and examples of correct procedures

for accessing the CODEC register are given in the driver code examples.

This information is provided to help you understand the sequence of events taking place:

- The 74S652 “A” bus pins are connected to the ISA data bus signals.
- The 74S652 “B” bus pins are connected to the CL550 host bus port.
- The signal H\_GAB enables the ISA data bus signals onto the CL550 host bus (PC write to CL550).
- The signal H\_GBA enables the CL550 host bus signals onto the ISA data bus (PC read from CL550).
- The signal H\_SAB enables the 74S652 latched data (previously written by the host processor into the Index register) onto the CL550 host bus.
- The signal H\_SBA enables the 74S652 latched data (the stored output of the CL550) onto the ISA data bus.
- The signal H\_CAB clocks the contents of the ISA data bus into the 74S652 “A” registers (Index register).
- The signal H\_CBA clocks the output of the CL550 into the 74S652 “B” register.



562-104

Figure 3-3 Host Bus Register Write Timing

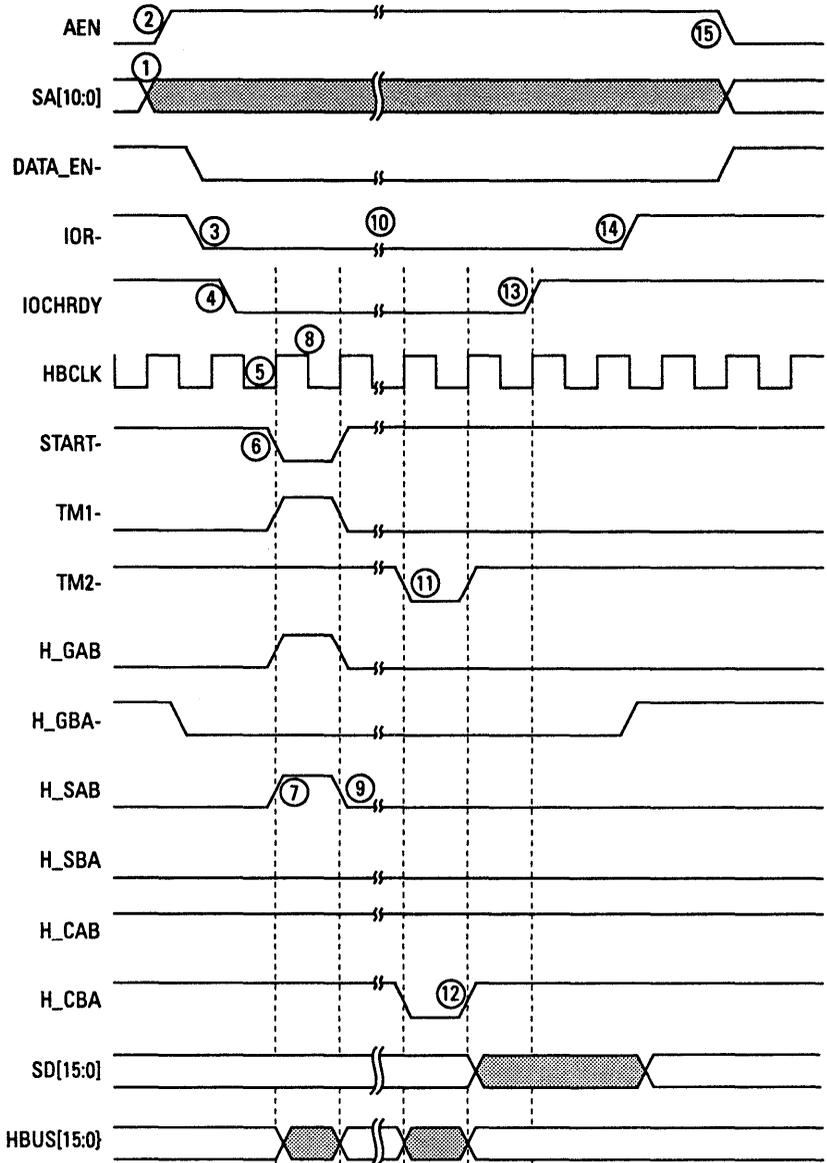
### 3.3.1 Host Bus Register Write Timing

Figure 3-3 shows the sequence of events when the ISA host processor writes to a CL550 register. The circled numbers in the figure refer to the steps in the text below.

1. The processor on the ISA bus initiates the transfer by outputting the address of the CL550 host data port (Base + 0) on the address bus, SA[10:0].
2. The processor on the ISA bus asserts the Address Enable (AEN) signal to qualify the address.
3. The processor on the ISA bus asserts the I/O Write (IOW-) signal to indicate to the SI-1 board that an I/O write operation is in progress.
4. The HBUSCTL PAL on the SI-1 board responds by immediately asserting the ISA bus signal IOCHRDY- signal. This indicates to the host CPU that at least one wait state will be inserted.
5. All operations before this point have been asynchronous. Operations between the vertical dotted lines are synchronized to the HBCLK signal.
6. The HBUSCTL PAL asserts the START- signal and the TM1- signal to tell the CL550 that a write operation is in progress.
7. The HBUSCTL PAL asserts the H\_SAB signal. This signal enables the address of the CL550 register being written (the contents of the Index register) onto the host bus. (The Index register contents were written previously by the ISA host processor.)
8. The CL550 samples START- and TM1- and the register address on the host data bus on the falling edge of HBCLK. The CL550 internal write cycle begins at this point.
9. The HBUSCTL PAL releases H\_SAB which enables the contents of the ISA data bus onto the host bus.
10. For any CL550 register other than the CODEC, there is always one clock period (wait state) between START and TM2. Accesses to the CODEC can encounter from zero to several (70 Pixel clock time) wait states.
11. When the CL550 is ready to accept the data, it asserts the acknowledge signal, TM2-. This completes the CL550 write cycle.

12. The HBUSCTL PAL releases IOCHRHY to tell the ISA bus that the data has been accepted.
13. The processor on the ISA bus releases IOW-, AEN and the data and address buses to end the ISA Bus write cycle.

# Host Bus Interface



552-105

**Figure 3-4 Host Bus Register Read Timing**

### 3.3.2 Host Bus Register Read Timing

Figure 3-4 shows the sequence of events when the ISA host processor reads from a CL550 register. The circled numbers in the figure refer to the steps in the text below.

1. The processor on the ISA bus initiates the transfer by outputting the address of the CL550 host data port (Base + 0) on the address bus, SA[10:0].
2. The processor on the ISA bus asserts the Address Enable (AEN) signal to qualify the address.
3. The processor on the ISA bus asserts the I/O Read (IOR-) signal to indicate that a read operation is in progress.
4. The HBUSCTL PAL in the SI-1 responds by immediately asserting the ISA bus signal IOCHRDY- signal. This indicates that at least one wait state will be inserted.
5. All operations before this point have been asynchronous. Operations after this point are synchronized to the HBCLK signal.
6. The HBUSCTL PAL asserts the START- signal and deasserts the TM1- signal to tell the CL550 that a read operation is in progress.
7. The HBUSCTL PAL asserts the H\_SAB and H\_GAB signals. This enables the address of the CL550 register being addressed (the contents of the Index register) onto the host bus. (The index register was written previously by the ISA host processor)
8. The CL550 samples START- and TM1- and the register address on the host data bus on the falling edge of HBCLK. The CL550 internal read cycle begins at this point.
9. The HBUSCTL PAL releases H\_SAB and H\_GAB which three-states the host bus.
10. For registers other than the CODEC, there is always one clock period (wait state) between START and TM2. Accesses to the CODEC can encounter from zero to several (70 Pixel clock time) wait states.
11. The CL550 outputs the data on HBUS[15:0] and asserts the acknowledge signal, TM2-. This completes the CL550 read cycle.
12. The HBUSCTL PAL asserts and releases H\_CBA. Data from the CL550 is stored in the LS652 registers on the rising edge of

H\_CBA. Because H\_GBA is asserted, it immediately becomes visible on SD[15:0].

13. The HBUSCTL PAL releases IOCHRHY to tell the ISA bus that the data is available.
14. The ISA bus releases IOR-. This causes H\_GBA to be released, and the data on SD[15:0] to become invalid.
15. The ISA bus releases AEN and the data and address buses to end the ISA bus read cycle.

The CL550 Pixel port is a 24-bit wide data port used to transfer pixel data to and from the CL550 processor. During compression operations, it is used as a write-only port to input uncompressed image data. During decompression operations, it is used as a read-only port to output decompressed image data.

Video formats grayscale, YCbCr 4:2:2 and CMYK use only 16 of the 24 pixel port data lines. All the remaining formats use all 24 pixel port data lines. Bit one in the SI-1's Control register (TGL\_EN) sets the 16-bit transfer mode when it is LOW and 24-bit transfer mode when it is HIGH.

The pixel port on the SI-1 board, shown on Pages 3 and 4 of the schematic, consists of two transceivers (U4 and U5) and two latches (U6 and U7) that connect the 24-bit Pixel data bus to the 16-bit ISA computer data bus. The latches are used to store the upper 8 bits of the 24-bit bus in the 24-bit mode. U7 is used to store the upper eight bits when reading data from the Pixel port, and U6 is used to store the upper eight bits when writing data to the Pixel port. The PBUSCTL PAL (22V10 U9) controls these buffers and latches during read and write operations.

Sixteen-bit pixel data can be transferred using a single I/O read or write. 24-bit pixel data reads and writes always require two I/O accesses. To write a 24-bit pixel, the host must first write the upper 8 bits of the pixel. This byte is temporarily stored in latch U6. On the second write the host writes the lower 16 bits of the pixel. As the lower word is being written, logic in the PBUSCTL PAL enables the byte stored in latch U6 onto Pixel bus bits PD[23:16], and enables the word currently on the host data bus onto Pixel bus bits PD[15:0]. The reassembled 24-bit word is then written into the CL550.

Twenty-four-bit pixel port reads also require two accesses. During the first read, the lower 16 bits of the pixel bus, PXDAT[15:0], are output on the ISA data bus, and the upper 8 bits, PXDAT[23:16], are stored in a latch (U7). The second read enables the latched data onto the 8 least significant bits of the ISA computer data bus.

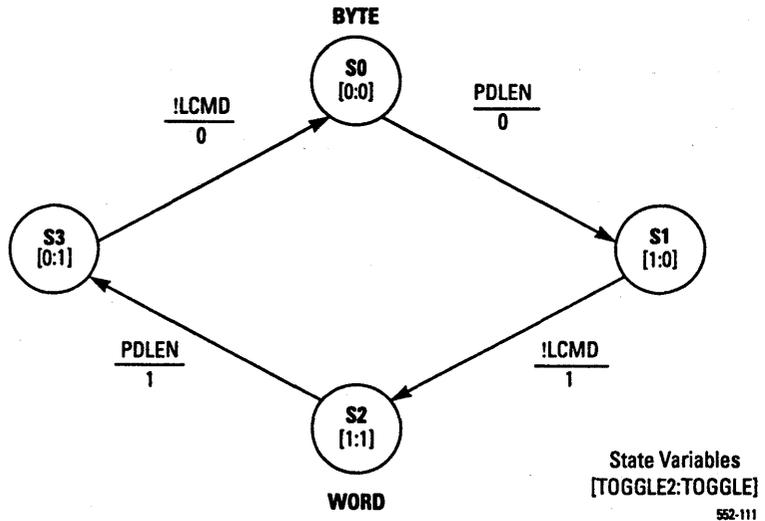
The Toggle state machine in the Pixel bus control PAL generates the signals necessary to perform 24-bit accesses. The state diagram for this PAL is shown in Figure 3-5. Immediately following a reset, the state machine is always in the WORD state. If a compression is the first op-

---

## 3.4 Pixel Bus Interface

---

eration to be performed after a reset, the state must be changed to the BYTE state by performing a dummy read of the Pixel port.



**Figure 3-5 Toggle State Machine State Diagram**

One of the more important components of the pixel bus interface is the hardware handshake mechanism for controlling the CL550 STALL- input. The CL550 can manipulate data much faster than the ISA bus is capable of transferring it. The STALL- line is used to hold the CL550 until the ISA bus can complete the transfer.

Figure 3-6 and Figure 3-7 show the operation of the STALL state machine during a compression operation and a decompression operation respectively. Generation of the STALL- signal is complex because during 24-bit operations the CL550 must be stalled until both the low word and the high byte have been transferred.

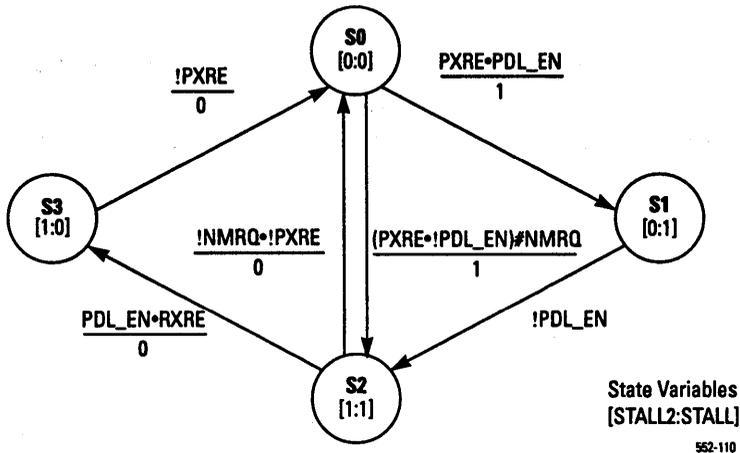


Figure 3-6 STALL- Operation: Compression

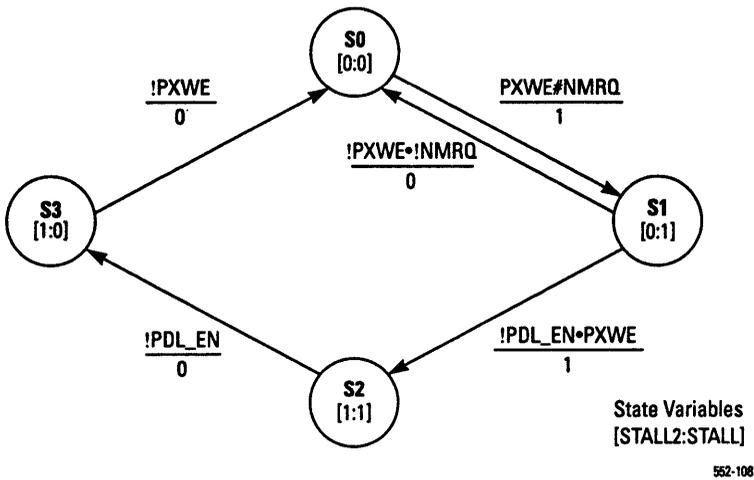
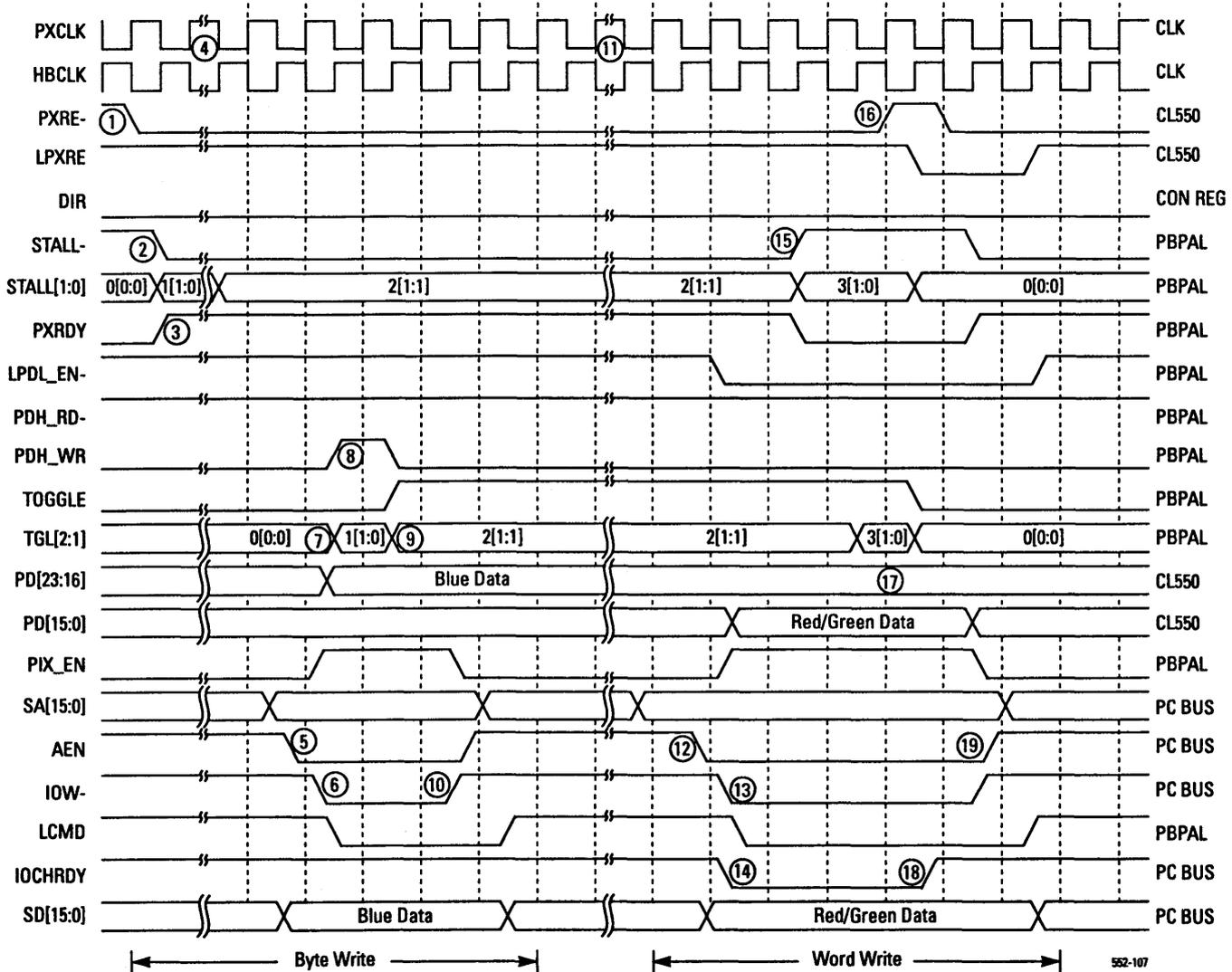


Figure 3-7 STALL- Operation: Decompression

## Pixel Bus Interface

The following background information is given to help you understand the examples.

- The CL550 clocks on the rising edge of PXCLK, but the PALS clock on the rising edge of HBCLK. This means that signals generated in the PALS will appear to transition in the center of the PXCLK cycle.
- The CL550 expects the pixel data to be presented on the following pins:
  - PD [23:16] = Blue Pixel Data
  - PD [15:8] = Green Pixel Data
  - PD [7:0] = Red Pixel Data
- A CL550 Pixel read cycle is a Host bus write cycle and a CL550 Pixel write cycle is a Host bus read cycle.



**Figure 3-8 STALL- Handshake Operation For Compression**

### 3.4.1 Pixel Bus Compression Timing

Figure 3-8 shows the timing diagram for a typical pixel write cycle during a compression operation. The numbers in the diagram refer to the steps listed below.

1. The transfer begins when the CL550 requests a 24-bit wide pixel. It asserts PXRE- to begin the request.
2. The pixel bus PAL immediately causes the CL550 STALL- signal to be asserted, putting the CL550 into a wait state. During compression operations, the stall signal must remain asserted until the host processor has written both the upper byte and the lower word of data.
3. The pixel bus PAL asserts the PXRDY signal. This signal is connected to Bit 0 in the status register (Pixel Port Status). The host must determine that the CL550 is ready to input data by polling the PXRDY bit and transferring data when it becomes valid. (PXRDY only needs to be checked for the first pixel. For all subsequent pixels, it is guaranteed to be ready again before the next pixel write.)
4. The pixel bus PAL holds the CL550 stalled while waiting for the host processor to supply the first byte of data.
5. When the host processor is ready to provide the requested data, it begins the write operation by outputting the address of the SI-1 pixel port and asserting the Address Enable (AEN) signal.
6. The processor indicates to the CL550 that a write operation is going to take place by asserting I/O Write (IOW-).
7. The Toggle State Machine recognizes the valid write condition and changes state.
8. The combination of the assertion of IOW- and state 1 from the Toggle state machine causes the signal PDH\_WR to be asserted by the pixel bus PAL. This signal enables the contents of the lower eight bits of the data bus (SD 7:0) into the High Byte Pixel Latch (PX23:16). This is typically Blue pixel data.
9. On the next HCLK rising edge, the Toggle state machine increments again. This causes the PDH\_WR signal to be deasserted and the TOGGLE signal to be asserted. The pixel data is latched

into the High Byte Pixel Latch (U6) on the falling edge of PDH\_WR.

10. The host processor releases IOW-, AEN, and the address and data buses. This completes the write of the High Byte Pixel Latch.
11. The CL550 remains stalled until the host processor is able to provide the lower word of data.
12. When the host processor is ready to provide the lower word, it begins the write operation by outputting the address of the CL550 pixel port and asserting Address Enable (AEN).
13. The host processor asserts IOW- to indicate to the CL550 that it is going to write the second word.
14. The Host Bus Interface PAL pulls IOCHRDY low. This forces the host bus to hold the data on the data bus until the CL550 has accepted it by adding ISA bus wait states.
15. The Pixel Bus PAL releases Stall. This allows the CL550 to complete the “read a 24-bit pixel” operation. To re-assemble the 24-bit word, the upper eight bits (Blue data) are read from the High Byte Pixel Latch, and the lower 16 bits (Red/Green data) are read directly from the Host data bus.
16. The CL550 acknowledges that it has read the data by deasserting the PXRE- signal.
17. Pixel data is sampled on the same clock edge that deasserted the PXRE- signal.
18. The Host Bus Interface PAL releases IOCHRDY as soon as it sees PXRE- deasserted. This allows the host CPU to finish the write cycle.
19. The Host CPU finishes the write cycle by releasing IOW-, AEN, and the address and data buses. This completes the write of a 24-bit pixel.



### 3.4.2 Pixel Bus Decompression Timing

Figure 3-9 shows the timing diagram for a typical pixel read cycle during a decompression operation. The numbers in the diagram refer to the steps listed below.

1. A Decompression pixel write cycle begins when the CL550 has a 24 bit pixel ready to be transferred to the host computer. The CL550 asserts PXWE- to start the transfer. The CL550 data bus is already valid at this point.
2. On the next leading edge of HBCLK, the pixel bus PAL asserts the PXRDY signal. This signal is connected to Bit 0 in the status register (Pixel Port Status). The host must determine that the CL550 is ready to output data by polling the PXRDY bit and transferring data when it becomes valid. (Note: PXRDY needs to be polled on the first pixel of every group of eight pixels during the first eight lines of the frame. After the first eight lines, PXRDY only needs to be checked once for the remainder of the frame.)
3. The pixel bus PAL also causes the CL550 STALL- signal to be asserted, putting the CL550 into a wait state. The STALL- signal will remain asserted only until the host processor has read the lower word of pixel data. During decompression operations there is no need to stall the CL550 until the upper byte is read because the upper byte of pixel data is stored in an external latch.
4. The pixel bus PAL generates CL550 wait states while waiting for the host processor to read the first byte of data. The CL550 can be stalled indefinitely with no loss of data.
5. When the host processor is ready to accept the data, it begins the read operation by outputting the address of the SI-1 pixel port and asserting the Address Enable (AEN) signal.
6. The processor indicates to the CL550 that a read operation is taking place by asserting I/O Read (IOR-).
7. The Toggle State Machine recognizes a valid read condition and changes state.
8. The combination of the assertion of IOR- and state 01 from the

Toggle state machine causes the signal PDL\_EN to be asserted by the pixel bus PAL. PDL\_EN enables the contents of the pixel data bus, PD[15:0], onto the host bus, SD[15:0]. This is typically Red/Green pixel data.

9. The host processor releases IOR-, AEN, and the address and data buses. This completes the read of the lower 16-bits of the Pixel data bus.
10. The Pixel Bus PAL releases the STALL- signal. This allows the CL550 to continue the decompression operation.
11. When the CL550 sees the STALL- signal released, it completes the bus cycle by releasing PXWE-. The rising edge of PXWE- is used to strobe the contents of the upper 8 bits of the pixel bus into the high byte pixel latch.
12. The pixel bus PAL recognizes that the transfer is complete and increments the Toggle state machine. This causes the TOGGLE line to change from the word state (HIGH) to the byte state (LOW).
13. One PXCLK cycle after the PXWE- was released, the CL550 has the next 24-bit pixel ready to be stored. The host processor has not yet read the high byte at this point and is not ready to accept the data.
14. The Pixel bus PAL causes the CL550 stall signal to be asserted until the host processor is able to accept the data. The new pixel cannot be read until the high byte of the last pixel has been retrieved from the latch.
15. The host processor begins the read of the pixel high byte by outputting the address of the SI-1 pixel port and asserting the address enable (AEN) signal.
16. The processor indicates to the CL550 that a read operation is taking place by asserting I/O Read (IOR-).
17. The Pixel bus PAL asserts the PDH\_RD- signal to enable the output of the Pixel high-byte latch (Blue Data) onto lower eight bits of the host data bus.
18. The Toggle State Machine recognizes a valid read condition and changes state.

19. The host processor releases IOW-, AEN, and the address and data buses. This completes the read of the Pixel high byte latch.
20. The signal PXRDY is valid because the next 24-bit pixel is ready to be read.

**Pixel Bus Interface**

# Appendix A

## Schematics

This appendix contains the schematics for the JPEG Still Image Board. The schematics were drawn using the ORCAD Schematic Capture program. The source files for the schematics are located on the diskette entitled:

**JPEG Still Frame Board  
Schematics and PAL Equations  
Hardware Rev. A  
Part # 83-5003-003**

This diskette is included with the JPEG Still Image Board manufacturing kit.

# PC550

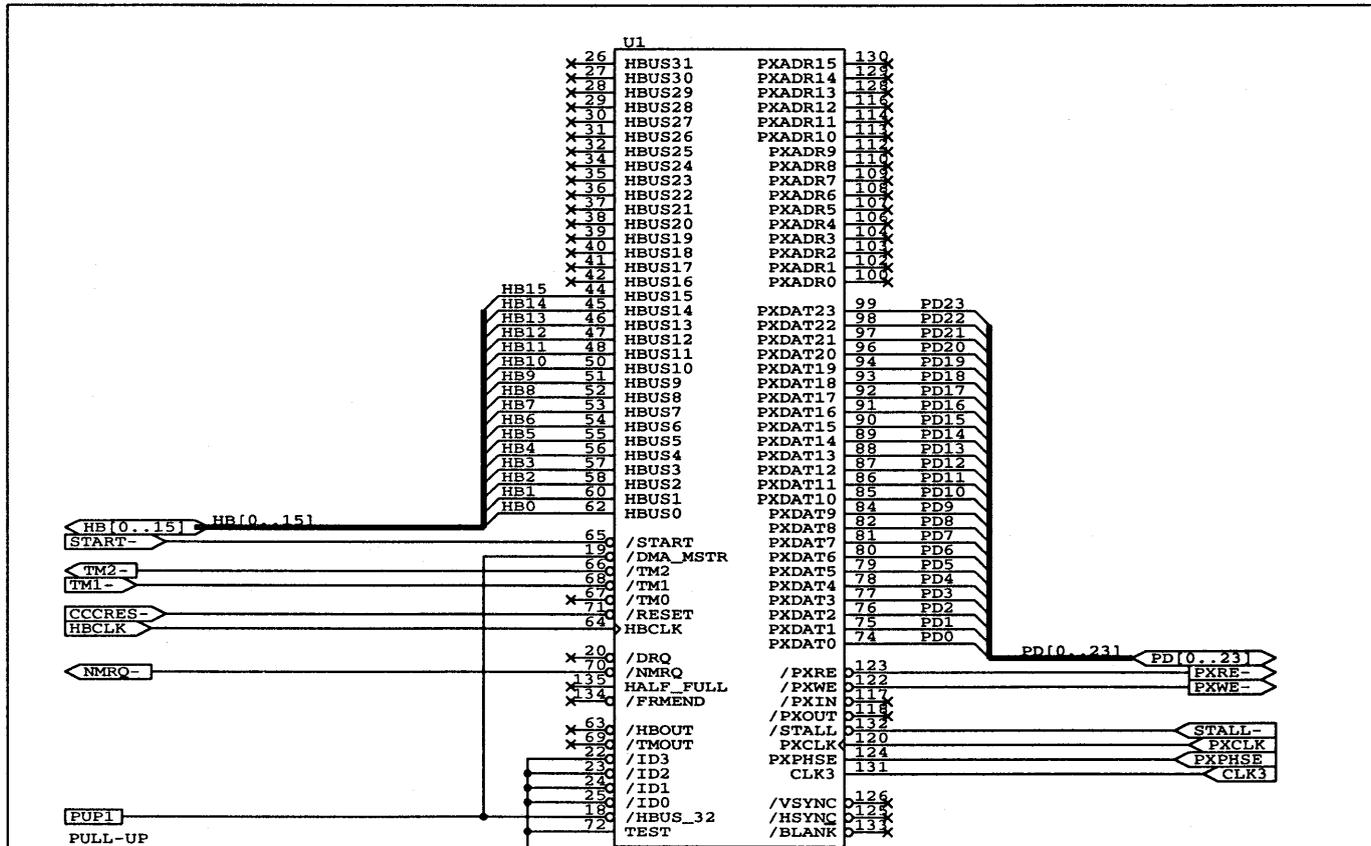
|LINK  
|CL550.SCH  
|BUSBUFFS.SCH  
|CONTROL.SCH  
|CLOCKS.SCH  
|ISA\_BUS.SCH

C-CUBE MICROSYSTEMS  
1778 McCarthy Blvd.  
Milpitas, CA 95035 USA  
Tel: (408) 944-6300  
FAX: (408) 944-6314

Title  
PC550 JPEG Compression Card for AT

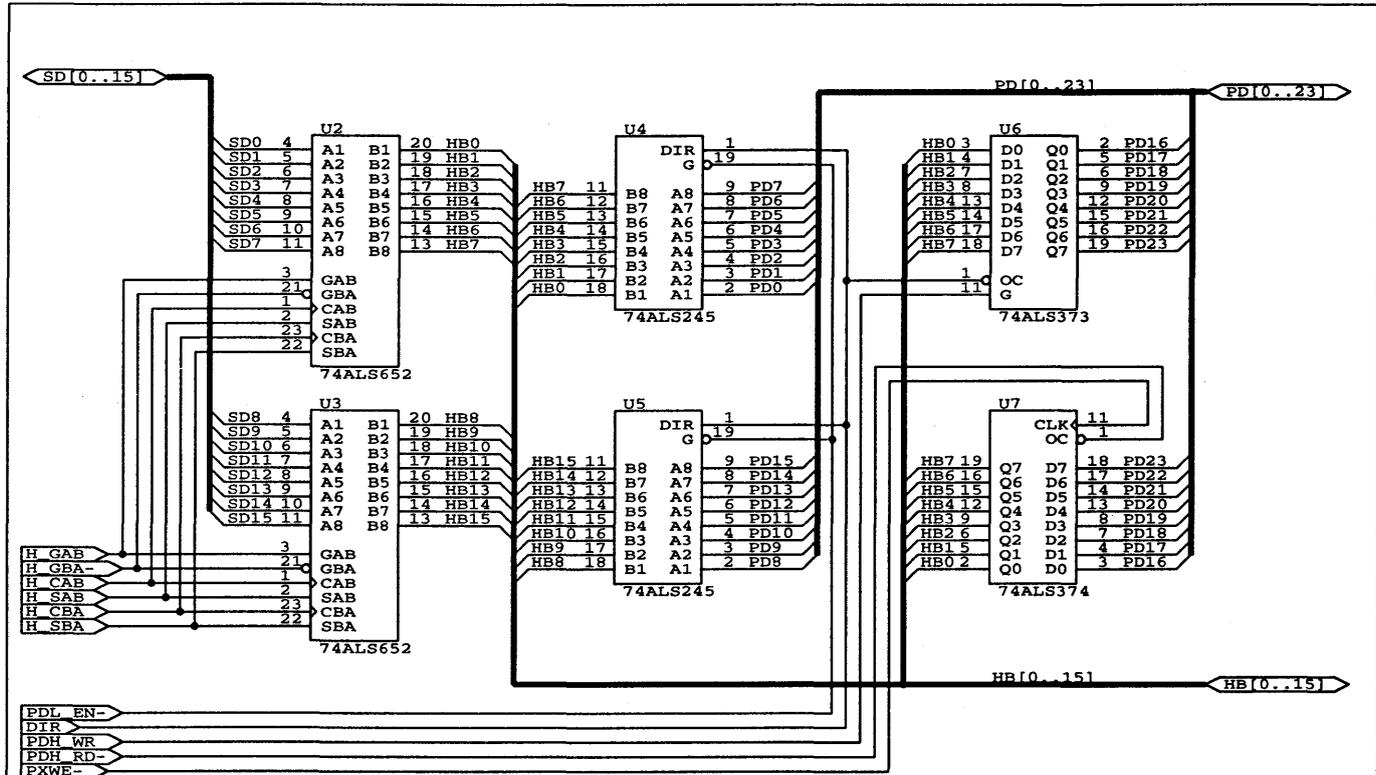
Size	Document Number	REV
A		A

Date: March 31, 1992 Sheet 1 of 6

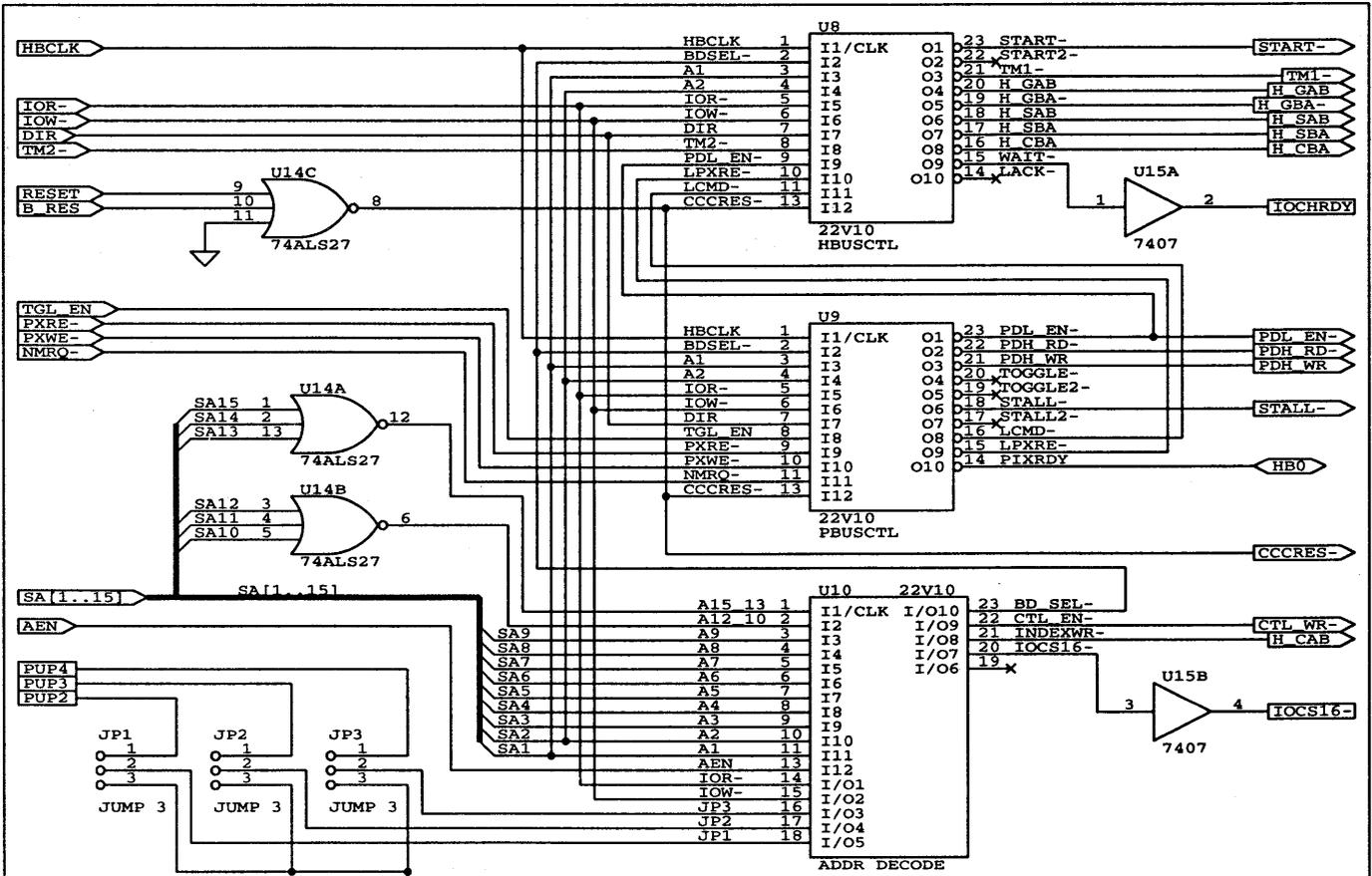


C-CUBE MICROSYSTEMS  
 1778 McCarthy Blvd.  
 Milpitas, CA 95035 USA

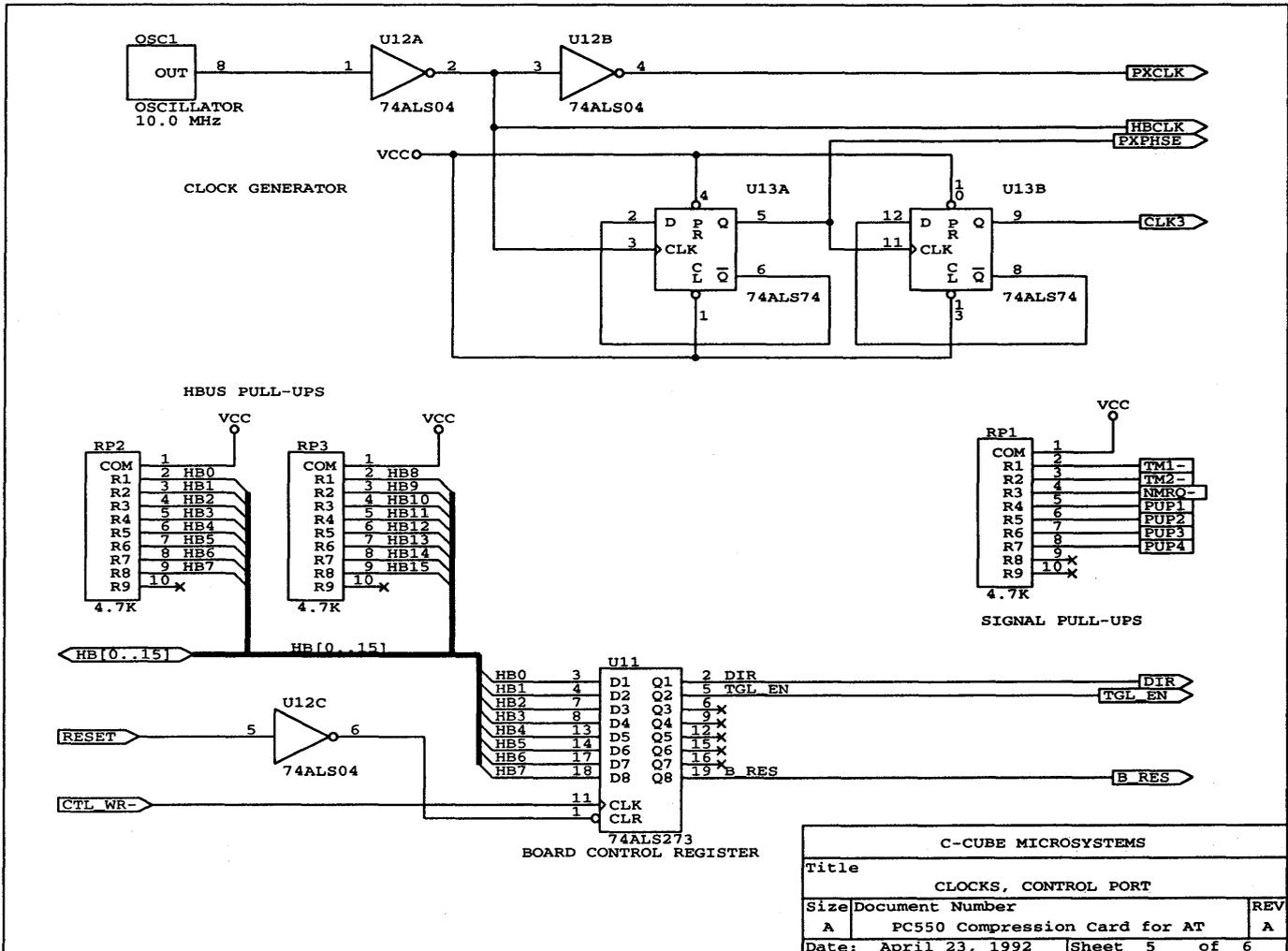
Title		
PC550 STILL IMAGE COMPRESSION CARD		
Size	Document Number	REV
A	CL550 JPEG PROCESSOR	A
Date:	April 23, 1992	Sheet 2 of 6

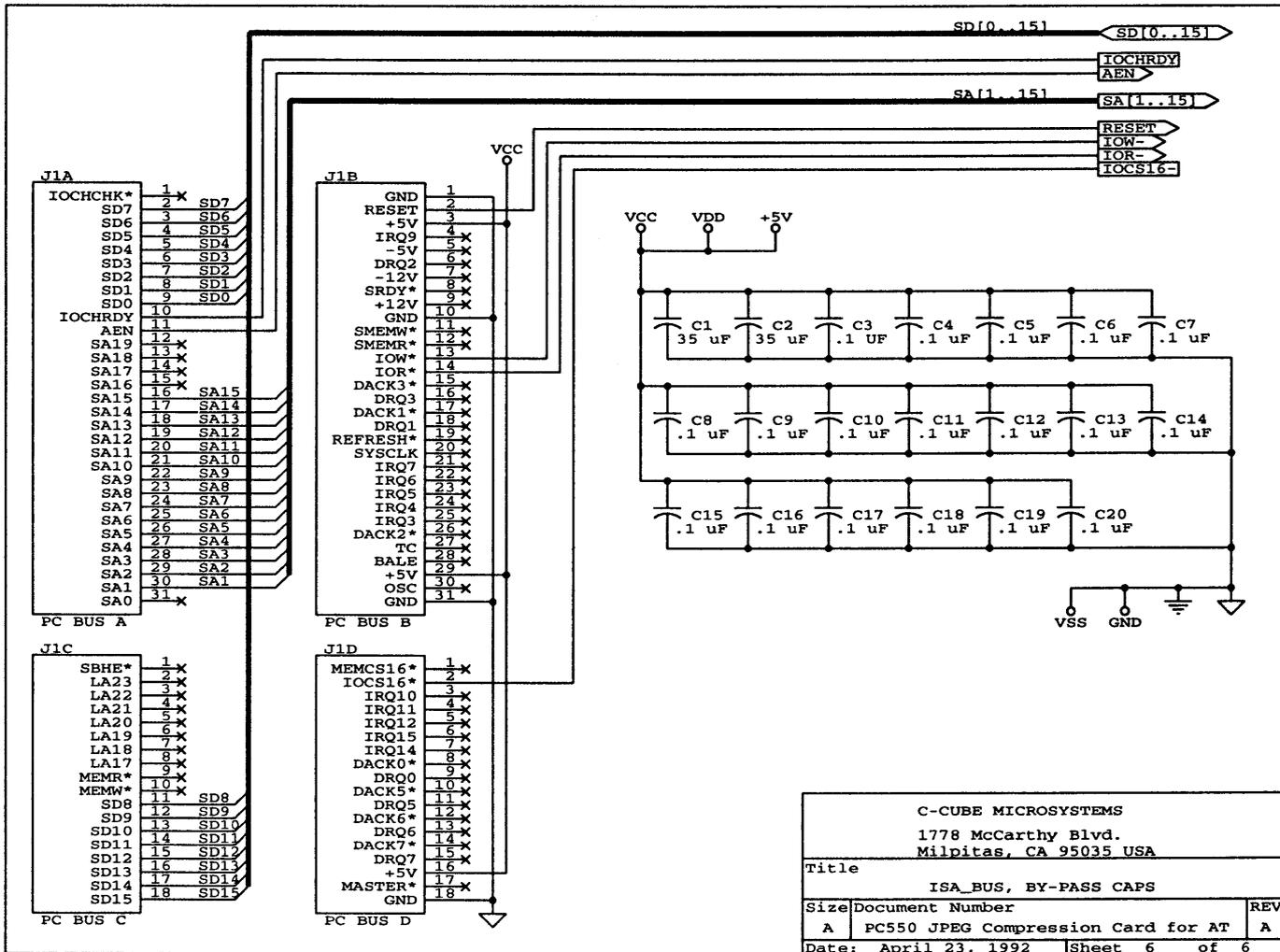


C-CUBE MICROSYSTEMS 1778 McCarthy Blvd. Milpitas, CA 95035 USA		
Title BUS BUFFERS		
Size	Document Number	REV
A	PC550 Compression Card for AT	A
Date:	April 23, 1992	Sheet 3 of 6



C-CUBE MICROSYSTEMS		
Title		
CONTROL LOGIC		
Size	Document Number	REV
A	PC550-ST STILL-IMAGE COMPRESSOR	
Date:	April 23, 1992	Sheet 4 of 6





C-CUBE MICROSYSTEMS		
1778 McCarthy Blvd.		
Milpitas, CA 95035 USA		
Title		
ISA_BUS, BY-PASS CAPS		
Size	Document Number	REV
A	PC550 JPEG Compression Card for AT	A
Date:	April 23, 1992	Sheet 6 of 6



# **Appendix B**

## **PAL Equations**

This appendix contains the source equations for the PAL devices used in the design of the JPEG Still Image Board. The equations are written to be compiled using DATA I/O's ABEL program. The source files for the PALs are located on the diskette entitled:

**JPEG Still Frame Board**  
**Schematics and PAL Equations**  
**Hardware Rev. A**  
**Part # 83-5003-003**

This diskette is included with the JPEG Still Image Board manufacturing kit.

## Address Decoder PAL Equations

---

### **B.1** **Address Decoder** **PAL Equations**

---

```
module _addrdec;
title 'Address Decoder PAL
PC550 Still-Image Compression Card for AT
```

```
Revision A1, April 1992
```

```
C-Cube Microsystems, 1778 McCarthy Blvd, Milpitas CA 95035, U.S.A.
Tel: (408) 944-6300 FAX: (408) 944-6314';
```

```
declarations
```

```
addrdec device 'p22v10';
```

```
"inputs
```

```
A15_13 pin 1;
A12_10 pin 2;
A9      pin 3;
A8      pin 4;
A7      pin 5;
A6      pin 6;
A5      pin 7;
A4      pin 8;
A3      pin 9;
A2      pin 10;
A1      pin 11;
AEN     pin 13;
!IOR    pin 14;
!IOW    pin 15;
JP3     pin 16;
JP2     pin 17;
JP1     pin 18;
```

```
"outputs
```

```
!BDSEL pin 23; !BDSEL istype 'com,neg';
!CTL_WR pin 22; !CTL_WR istype 'com,neg';
!INDEX pin 21; !INDEX istype 'com,neg';
!IOCS16 pin 20; !IOCS16 istype 'com,neg';
```

```
"logic declarations
```

```

CMD = IOR # IOW;
HIGH_A = A15_13 & A12_10;
BASE1 = HIGH_A & A9 & A8 & !A7 & !A6 & !A5 & !A4 & !A3; "0x300-307
BASE2 = HIGH_A & A9 & A8 & !A7 & !A6 & A5 & !A4 & !A3; "0x320-327
BASE3 = HIGH_A & A9 & A8 & !A7 & A6 & !A5 & !A4 & !A3; "0x340-347
BASE4 = HIGH_A & A9 & A8 & !A7 & A6 & A5 & !A4 & !A3; "0x360-367
BASE5 = HIGH_A & A9 & A8 & A7 & !A6 & !A5 & !A4 & !A3; "0x380-387
BASE6 = HIGH_A & A9 & A8 & A7 & !A6 & A5 & !A4 & !A3; "0x3A0-3A7
BASE7 = HIGH_A & A9 & A8 & A7 & A6 & !A5 & !A4 & !A3; "0x3C0-3C7
BASE8 = HIGH_A & A9 & A8 & A7 & A6 & A5 & !A4 & !A3; "0x3E0-3E7

```

```
equations
```

```
"BDSEL enables read/write transfers to the PC550 board
```

```

BDSEL = (!JP3 & !JP2 & !JP1 & !AEN & BASE1)
# (!JP3 & !JP2 & JP1 & !AEN & BASE2)
# (!JP3 & JP2 & !JP1 & !AEN & BASE3)
# (!JP3 & JP2 & JP1 & !AEN & BASE4)
# (JP3 & !JP2 & !JP1 & !AEN & BASE5)
# (JP3 & !JP2 & JP1 & !AEN & BASE6)
# (JP3 & JP2 & !JP1 & !AEN & BASE7)
# (JP3 & JP2 & JP1 & !AEN & BASE8);

```

```
"CTL_WR enables a write to the PC550 Control Register
```

```
CTL_WR = BDSEL & A2 & !A1 & IOW;
```

```
"INDEX enables a write to the PC550 Index Register
```

```
INDEX = BDSEL & !A2 & A1 & IOW;
```

```
"IOCS16 drives the IOCS16 line of the ISA bus during CMD
```

```
IOCS16 = BDSEL & CMD;
```

```
end_addrdec
```

---

### **B.2** **HBUS Controller** **PAL Equations**

---

```
module _hbusctl;  
title 'HBUS-to-ISA Bus Control Logic  
PC550 Still-Image Compression Card for AT and Compatibles
```

```
Revision A, September 17, 1992
```

```
C-Cube Microsystems, 1778 McCarthy Blvd., Milpitas, CA 95035, USA.  
Tel: (408) 944-6300 FAX: (408) 944-6314 ';
```

```
declarations  
hbusctl device 'p22v10';  
*inputs  
HBCLK pin 1;  
!BDSEL pin 2;  
A1 pin 3;  
A2 pin 4;  
!IOR pin 5;  
!IOW pin 6;  
DIR pin 7;  
!TM2 pin 8;  
!PDL_EN pin 9;  
!LPXRE pin 10;  
!LCMD pin 11;  
!CCCRE pin 13;  
*outputs  
!START pin 23; !START istype 'reg,neg';  
!START2 pin 22; !START2 istype 'reg,neg';  
!TM1 pin 21; !TM1 istype 'com,neg';  
H_GAB pin 20; H_GAB istype 'com,pos';  
!H_GBA pin 19; !H_GBA istype 'com,neg';  
H_SAB pin 18; H_SAB istype 'com,pos';  
H_SBA pin 17; H_SBA istype 'com,pos';  
!H_CBA pin 16; !H_CBA istype 'com,neg';  
!WAIT pin 15; !WAIT istype 'com,neg';  
!LACK pin 14; !LACK istype 'reg,neg';  
  
*intermediate expressions  
CMD = IOW # IOR;  
DATA_EN = BDSEL & !A2 & !A1;  
INDEX_EN = BDSEL & !A2 & A1 & IOW;  
CTL_STS = BDSEL & A2 & !A1;  
PIX_EN = BDSEL & A2 & A1;
```

```

equations
*/START AND /START2 FORM A STATE MACHINE WHICH PULSES START WHEN
DATA_EN = 1

START := !START & !START2 & DATA_EN & LCMD & !CCCRE;
START2 := (START & !CCCRE) # (START2 & LCMD & !CCCRE);

*/TM1 IS EQUAL TO IOW BUT IS HI-Z WHEN START IS FALSE
TM1 = IOW;
TM1.OE = START;

"H_GAB contols the '652-to-HBUS drivers.
H_GAB = (DATA_EN & IOW)
# (DATA_EN & IOR & START)
# (PIX_EN & IOW)
# (CTL_STS & IOW);

*/H_GBA controls the '652-to-ISA bus drivers.
H_GBA = (DATA_EN & IOR)
# (PIX_EN & IOR)
# (CTL_STS & IOR);

"H_SAB places the latched CL550 index value on HBUS
H_SAB = (IOW & START)
# (IOR & START);

"H_SBA is used to pass latched CL550 register read data to ISA bus
H_SBA = DATA_EN & IOR;

"H_CBA is used to latch read data from the CL550 during TM2
H_CBA = TM2 & IOR;

"WAIT drives the IOCHRDY line.
"On host accesses, WAIT is driven until TM2 is returned from the
550. On pixel WORD writes, WAIT is driven until the rising edge of
PXRE. On pixel BYTE read or writes, WAIT is driven until 1 clock
past LCMD. On pixel reads, WAIT is driven until LCMD is asserted. On
CTL port writes, wait is driven until 1 HCLK past LCMD. On INDEX
port writes, wait is driven until 1 HCLK past LCMD."

WAIT = (DATA_EN & CMD & !LACK) "CL550 Host r/w
# (!DIR & PDL_EN & IOW & !LPXRE) "PIXEL WORD WRITE
# (!DIR & PIX_EN & !PDL_EN & IOW & !LPXRE) "PIXEL BYTE WRITE
# (PIX_EN & IOR & !LPXRE); "PIXEL READ

"LACK is true on TM2 (ACK) active and is latched through CMD ac-
tive.
LACK := TM2 # (LCMD & LACK);
end _hbusctl;
?

```

## Pixel Bus Controller PAL Equations

---

### **B.3** **Pixel Bus Controller** **PAL Equations**

---

```
module _pbusctl;  
title 'PXDAT-to-HBUS Interface Control Logic  
PC550 Still-Image Compression Card for AT
```

Revision A, September 17, 1992

C-Cube Microsystems, 1778 McCarthy Blvd., Milpitas, CA 95035, USA  
Tel: (408) 944-6300 FAX: (408) 944-6314 ';

```
declarations
```

```
pbusctl device 'p22v10';
```

```
"inputs
```

```
HBCLK   pin 1;  
!BDSEL  pin 2;  
A1      pin 3;  
A2      pin 4;  
!IOR    pin 5;  
!IOW    pin 6;  
DIR     pin 7;  
TGL_EN  pin 8;  
!PXRE   pin 9;  
!PXWE   pin 10;  
!NMRQ   pin 11;  
!CCCREs pin 13;
```

```
"outputs
```

```
!PDL_EN pin 23; !PDL_EN istype 'reg,neg';  
!PDH_RD pin 22; !PDH_RD istype 'com,neg';  
PDH_WR pin 21;  PDH_WR istype 'com,pos';  
!TGL1 pin 20;  !TGL1 istype 'reg,neg';  
!TGL2 pin 19;  !TGL2 istype 'reg,neg';  
!STALL pin 18; !STALL istype 'reg,neg';  
!STALL2 pin 17; !STALL2 istype 'reg,neg';  
!LCMD pin 16;  !LCMD istype 'reg,neg';  
!LPXRE pin 15; !LPXRE istype 'reg,neg';  
PIXRDY pin 14; PIXRDY istype 'com,pos';
```

```
"logic declarations
```

```
CMD = IOR # IOW;  
DATA_EN = BDSEL & !A1 & !A2;  
INDEX_EN = BDSEL & A1 & !A2 & IOW;  
STS_EN = BDSEL & !A1 & A2 & IOR;  
CTL_EN = BDSEL & !A1 & A2 & IOW;  
PIX_EN = BDSEL & A1 & A2;  
LPIX_EN = PIX_EN & CMD & LCMD;  
LPDL_EN = PDL_EN & LCMD;  
PDH_EN = PIX_EN & !TGL1 & CMD;  
IRESET = CCCRES;
```

equations

"PDL\_EN opens the 16-bit transceivers connected to PXDAT[0..15]  
 "The x-cvrs open only for writes in compress and reads in decom-  
 press

```
PDL_EN = ( PIX_EN & TGL1 & IOW & !DIR )
# ( PIX_EN & TGL1 & IOR & DIR );
```

"PDH\_RD enables the 8-bit read latch from PXDAT[16..23]  
 PDH\_RD = PDH\_EN & IOR & DIR; "decompress only

"PDH\_WR enables the 8-bit write latch to PXDAT[16..23]  
 PDH\_WR = PDH\_EN & LCMD & !LPXRE & !DIR; "compress only

"These state equations control the pixel port toggle for 24/32-bit  
 modes.

"When toggle mode is entered, the initial state will point to the  
 WORD

"port (TGL1=1, TGL2=1). In compression, BYTE-WORD input of data is  
 "required, so a dummy read to the pixel port will toggle to the  
 BYTE latch.

"For decompression, WORD-BYTE access of data is required (reading  
 the word

"latches the byte).

```
TGL1 := (!TGL_EN
# (TGL_EN & TGL2 & !LCMD)
# (TGL_EN & TGL1 & LCMD) ) & !CCRES;
```

```
TGL2 := !TGL_EN
# (TGL_EN & TGL2 & !LPIX_EN)
# (TGL_EN & !TGL1 & LPIX_EN)
# CCRES;
```

## Pixel Bus Controller PAL Equations

\*State equations for STALL in compression (!DIR) and decompression (DIR).

```
STALL := (!DIR & !IRESET & !STALL2 & STALL)
# (!DIR & !IRESET & !STALL2 & PXRE)
# (!DIR & !IRESET & STALL & PXRE & !LPDL_EN)
# (!DIR & !IRESET & !STALL2 & !STALL & NMRQ)
# (!DIR & !IRESET & STALL & !PXRE & NMRQ)
# (DIR & !IRESET & STALL & STALL2 & LPDL_EN)
# (DIR & !IRESET & !STALL2 & PXWE)
# (DIR & !IRESET & !STALL2 & !PXWE & NMRQ);
```

```
STALL2 := (!DIR & !IRESET & !STALL2 & NMRQ)
# (!DIR & !IRESET & STALL2 & STALL & NMRQ)
# (!DIR & !IRESET & STALL2 & PXRE)
# (!DIR & !IRESET & PXRE & !LPDL_EN)
# (!DIR & !IRESET & !STALL2 & STALL & !PXRE & LPDL_EN)
# (DIR & !IRESET & STALL & STALL2)
# (DIR & !IRESET & STALL & PXWE & LPDL_EN)
# (DIR & !IRESET & STALL2 & PXWE);
```

\*LCMD is a synchronized CMD line for use in all state machines.

```
LCMD := (DATA_EN # PIX_EN) & CMD;
```

\*/LPXRE is used in compression WORD writes to hold WAIT until PXRE goes high. /LPXRE is used in compression BYTE writes hold wait for 1 clock past LCMD. /LPXRE is used in all pixel READs to hold WAIT for 1 HCLK past LCMD\*

```
LPXRE := (!DIR & LPDL_EN & !PXRE) *PIXEL WORD WRITE
# (!DIR & LPDL_EN & LPXRE) *PIXEL WORD WRITE
# (!DIR & PDH_EN & IOW & LCMD) *Pixel BYTE write
# (PIX_EN & IOR & LCMD); *pixel READ (byte or word)
```

\*PIXRDY is a status bit which is read at IObase+4 (Pixel Port Ready)

```
PIXRDY = (!DIR & PXRE & STALL )
# (DIR & PXWE & STALL);
```

```
PIXRDY.OE = STS_EN & IOR;
```

```
end _pbusctl;
```

?

# **Appendix C**

## **Bill of Materials**

This appendix contains the Bill of Materials for the JPEG Still Image Board. All of the Integrated Circuits except the CL550-10 are expected to be in low-cost standard DIP packages.

The PAL devices need to be programmed to the equations listed in Appendix B before being loaded onto the board. To facilitate this, sockets are listed for these three devices only.

This Bill of Materials is for the board assembly only. It does not include items which are normally on the top level Bill of Material such as manuals, software diskettes, and packing materials.

**Table C-1 JPEG Still Frame Board Bill of Materials**

Item	Qty	Reference	Part Number	Description
1	1	U1	CL550Q	CL550-10 MQUAD JPEG Compression Processor
2	2	U2,U3	74ALS652	Octal Transceivers/Latches, Through Hole
3	2	U4,U5	74ALS245	Octal Transceivers, Through Hole
4	1	U6	74ALS373	Octal D-Type Transparent Latches, Through Hole
5	1	U7	74ALS374	Octal D-Type Edge-Triggered Flip-Flops, Through Hole
6	1	U8	HBUS Control	PAL22V10-15 Programmable Logic Device, Socketed
7	1	U9	PBUS Control	PAL22V10-15 Programmable Logic Device, Socketed
8	1	U10	ADDR Decode	PAL22V10-15 Programmable Logic Device, Socketed
9	1	U11	74ALS273	Octal D-Type Flip-Flops with Clear, Through Hole
10	1	U12	74ALS04	Hex Inverters, Through Hole
11	1	U13	74ALS74	Dual D-Type Flip-Flops with Preset, Clear, Through Hole
12	1	U14	74ALS27	Triple 3-Input NOR Gates, Through Hole
13	1	U15	7407	Hex Open-Collector Drivers, Through Hole
14	1	OSC1	Oscillator	TTL Oscillator, 10.0 MHz
15	3	JP1,JP2,JP3	JUMP 3	3-post Pin Jumpers
16	2	C2,C1	35 uF	Capacitor, Through Hole, Tantalum, 20V
17	18	C3,C4,C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15,C16, C17,C18,C19,C20	.1 UF	Capacitor, Through Hole, Ceramic, 20V
18	3	U8, U9, U10	DIP-24	24-pin DIP Low Insertion Force socket
19	3	JP1, JP2, JP3	SHUNT-2	Jumper Shunts
20	3	RP1,RP2,RP3	4.7K	SIP res pack, 10 pin, 9 res, 5%
21	1	B1	PCB mounting bracket,	GLOBE G35
22	2	S1,S2	Philips Head Screw	4-40 X 3/16
23	1			Printed Circuit Board

# Customer Feedback

C-Cube Microsystems is always working to improve the quality of our documentation. If you have comments or suggestions on this document, please copy the following page, note your comments, and send it to us. You can also send us marked-up copies of pages in this document with your comments. Our address is:

C-Cube Microsystems  
1778 McCarthy Boulevard  
Milpitas, CA 95035

phone: (408) 944-6300

fax: (408) 944-6314

Attn: Technical Publications

**Customer Comments**

Document \_\_\_\_\_

Date \_\_\_\_\_

Please rate this document according to these criteria:

	Excellent	Good	Fair	Poor
Completeness:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ease of use:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Accuracy:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

List any errors by page number. Include a marked-up copy of the page.

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

How can we improve this document?

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Please complete this information:

Name \_\_\_\_\_ Title \_\_\_\_\_

Company \_\_\_\_\_

Phone \_\_\_\_\_ Fax \_\_\_\_\_

Department \_\_\_\_\_ Mail Stop \_\_\_\_\_

Street \_\_\_\_\_

City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

Country \_\_\_\_\_

Thanks for helping us make our documentation better!

# North American Representatives

## United States

---

### Alabama

Montgomery Marketing  
1910 Sparkman Avenue  
Huntsville, AL 35816  
phone: 205-830-0498  
fax: 205-837-7049

### Arizona

C-Cube Microsystems

### Arkansas

TL Marketing  
14850 Quorum Dr., Suite 100  
Dallas, TX 75240  
phone: 214-490-9300  
fax: 214-960-6075

### California

#### *Bay Area*

Norcomp  
3350 Scott Blvd.  
Santa Clara, CA 95054  
phone: 408-727-7707  
fax: 408-986-1947

#### *Sacramento Area*

Norcomp  
2140 Professional Drive, #200  
Roseville, CA 95661  
phone: 916-782-8070  
fax: 916-782-8073

#### *Southern California*

Bager Electronics  
17220 Newhope Street, Suite 209  
Fountain Valley, CA 92708  
phone: 714-957-3367  
fax: 714-546-2654

### Colorado

Promotech Sales, Inc.  
2901 S. Colorado Blvd.  
Denver, CO 80222  
phone: 303-692-8484  
fax: 303-692-8416

### Connecticut

C-Cube Microsystems

### Delaware

Omega  
2655 Interplex Drive Suite 104  
Trevose, PA 19053  
phone: 215-244-4000  
fax: 215-244-4104

### District of Columbia

C-Cube Microsystems

### Florida

#### *Northern*

Semtronic Associates  
657 Maitland Avenue  
Altamonte Springs, FL 32701  
phone: 407-831-8233  
fax: 407-831-2844

#### *Western*

Semtronic Associates  
1467 S. Missouri Avenue  
Clearwater, FL 34616  
phone: 813-461-4675  
fax: 813-442-2234

#### *Southern*

Semtronic Associates  
3471 NW 55th Street  
Ft. Lauderdale, FL 33309  
phone: 305-731-2484  
fax: 305-731-1019

### Georgia

Montgomery Marketing  
3000 Northwoods Parkway #110  
Norcross, GA 30071  
phone: 404-447-6124  
fax: 404-447-0422

### Hawaii

Bager Electronics  
17220 Newhope Street, Suite 209  
Fountain Valley, CA 92708  
phone: 714-957-3367  
fax: 714-546-2654

### Idaho

#### *Eastern*

Anderson Associates  
270 South Main #108  
Bountiful, UT 84010  
phone: 801-292-8991  
fax: 801-298-1503

#### *Western*

Thorson Company Northwest  
12340 N.E. 8th Street  
Bellevue, WA 98005  
phone: 206-455-9180  
fax: 206-455-9185

### Illinois

#### *Northern*

Beta Technology Sales, Inc.  
1009 Hawthorn Drive  
Itasca, IL 60143  
phone: 708-250-9586  
fax: 708-250-9592

#### *Southern*

C-Cube Microsystems

**Indiana**

C-Cube Microsystems

**Iowa**

Cahill, Schmitz & Howe  
4905 Lakeside Dr. N.E., Suite 100  
Cedar Rapids, IA 52402  
phone: 319-377-8219  
fax: 319-377-0958

**Kansas**

C-Cube Microsystems

**Kentucky**

C-Cube Microsystems

**Louisiana**

TL Marketing  
14850 Quorum Dr., Suite 100  
Dallas, TX 75240  
phone: 214-490-9300  
fax: 214-960-6075

**Maine**

Procomp Associates  
1049 East Street  
Tewksbury, MA 01876  
phone: 508-858-0100  
fax: 508-858-0110

**Maryland**

C-Cube Microsystems

**Massachusetts**

Procomp Associates  
1049 East Street  
Tewksbury, MA 01876  
phone: 508-858-0100  
fax: 508-858-0110

**Michigan**

C-Cube Microsystems

**Minnesota**

Cahill, Schmitz & Cahill, Inc.  
315 N. Pierce Street  
St. Paul, MN 55104  
phone: 612-646-7217  
fax: 612-646-4484

**Mississippi**

Montgomery Marketing  
1910 Sparkman Avenue  
Huntsville, AL 35816  
phone: 205-830-0498  
fax: 205-837-7049

**Missouri**

C-Cube Microsystems

**Montana**

Promotech Sales, Inc.  
2901 S. Colorado Blvd.  
Denver, CO 80222  
phone: 303-692-8484  
fax: 303-692-8416

**Nebraska**

C-Cube Microsystems

**Nevada**

*Excluding Clark County*  
Norcomp  
2140 Professional Drive, #200  
Roseville, CA 95661  
phone: 916-782-8070  
fax: 916-782-8073

**Clark County**

Bager Electronics  
6324 Variel, Suite 314  
Woodland Hills, CA 91367  
phone: 818-712-0011  
fax: 818-712-0160

**New Hampshire**

Procomp Associates  
1049 East Street  
Tewksbury, MA 01876  
phone: 508-858-0100  
fax: 508-858-0110

**New Jersey**

*Northern*  
Parallax  
734 Walt Whitman Road  
Melville, NY 11747  
phone: 516-351-1000  
fax: 516-351-1606

**Southern**

Omega  
2655 Interplex Drive Suite 104  
Trevose, PA 19053  
phone: 215-244-4000  
fax: 215-244-4104

**New Mexico**

C-Cube Microsystems

**New York**

*Metro*  
Parallax  
734 Walt Whitman Road  
Melville, NY 11747  
phone: 516-351-1000  
fax: 516-351-1606

**Upstate**

Empire Technical Associates  
29 Fennell Street, Suite A  
Skaneateles, NY 13152  
phone: 315-685-5703  
fax: 315-685-5979

**Eastern**

Empire Technical Associates  
349 W. Commercial Street  
Suite 2920  
East Rochester, NY 14445  
phone: 716-381-8500  
fax: 716-381-0911

**North Carolina**

Montgomery Marketing  
1200 Trinity Road  
Raleigh, NC 27607  
phone: 919-851-0010  
fax: 919-851-6620

**North Dakota**

Cahill, Schmitz & Cahill, Inc.  
315 N. Pierce Street  
St. Paul, MN 55104  
phone: 612-646-7217  
fax: 612-646-4484

**Ohio**

C-Cube Microsystems

**Oklahoma**

TL Marketing  
14850 Quorum Dr., Suite 100  
Dallas, TX 75240  
phone: 214-490-9300  
fax: 214-960-6075

**Oregon**

Thorson Company Northwest  
9600 S.W. Oak Street #320  
Portland, OR 97223  
phone: 503-293-9001  
fax: 503-293-9007

**Pennsylvania**

Omega  
2655 Interplex Drive Suite 104  
Trevoise, PA 19053  
phone: 215-244-4000  
fax: 215-244-4104

**Rhode Island**

Procomp Associates  
1049 East Street  
Tewksbury, MA 01876  
phone: 508-858-0100  
fax: 508-858-0110

**South Carolina**

Montgomery Marketing  
1200 Trinity Road  
Raleigh, NC 27607  
phone: 919-851-0010  
fax: 919-851-6620

**South Dakota**

Cahill, Schmitz & Cahill, Inc.  
315 N. Pierce Street  
St. Paul, MN 55104  
phone: 612-646-7217  
fax: 612-646-4484

**Tennessee**

Montgomery Marketing  
3000 Northwoods Parkway #110  
Norcross, GA 30071  
phone: 404-447-6124  
fax: 404-447-0422

**Texas**

*Northern*  
TL Marketing  
14850 Quorum Dr., Suite 100  
Dallas, TX 75240  
phone: 214-490-9300  
fax: 214-960-6075

*Central*

TL Marketing  
12015 Park 35 Circle, Suite 224  
Austin, TX 78753  
phone: 512-837-7272  
fax: 512-837-6886

*Eastern*

TL Marketing  
14343 Tory Chase Blvd. Suite I  
Houston, TX 77014  
phone: 713-587-8100  
fax: 713-580-7517

**Utah**

Anderson Associates  
270 South Main #108  
Bountiful, UT 84010  
phone: 801-292-8991  
fax: 801-298-1503

**Vermont**

Procomp Associates  
1049 East Street  
Tewksbury, MA 01876  
phone: 508-858-0100  
fax: 508-858-0110

**Virginia**

C-Cube Microsystems

**Washington**

Thorson Company Northwest  
12340 N.E. 8th Street  
Bellevue, WA 98005  
phone: 206-455-9180  
fax: 206-455-9185

**West Virginia**

C-Cube Microsystems

**Wisconsin***Western*

Cahill, Schmitz & Cahill, Inc.  
315 N. Pierce Street  
St. Paul, MN 55104  
phone: 612-646-7217  
fax: 612-646-4484

*Eastern*

Beta Technology Sales, Inc.  
9401 W. Beloit Road, Suite 409  
Milwaukee, WI 53227  
phone: 414-543-6609  
fax: 414-543-9288

**Wyoming**

C-Cube Microsystems

## **Canada**

---

### **British Columbia**

**Thorson Company Northwest**  
12340 N.E. 8th Street  
Bellevue, WA 98005  
phone: 206-455-9180  
fax: 206-455-9185

### **Alberta**

**Thorson Company Northwest**  
12340 N.E. 8th Street  
Bellevue, WA 98005  
phone: 206-455-9180  
fax: 206-455-9185

### **Saskatchewan**

**Electrosource**  
230 Galaxy Blvd.  
Rexdale, ONT  
Canada M9W 5R8  
phone: 416-675-4490  
fax: 416-675-6871

### **Ontario**

**Electrosource**  
230 Galaxy Blvd.  
Rexdale, ONT  
Canada M9W 5R8  
phone: 416-675-4490  
fax: 416-675-6871

**Electrosource**  
340 March Road, Suite 503  
Kanata, ONT  
Canada  
K2K 2E4  
phone: 613-592-3214  
fax: 613-592-4256

### **Quebec**

**Electrosource**  
6600 Trans Canada Highway,  
Suite 420  
Pointe Claire, Quebec  
H9R 4S2  
phone: 514-630-7486  
fax: 514-630-7421

# International Representatives and Distributors

## Pacific

---

Kubota C-Cube Inc.  
Yokohama Business Park  
East Tower, 12th Floor  
134 Goudo-cho, Hodogaya-ku  
Yokohama-city  
Japan, 240  
phone: (81) 45-336-6550  
fax: (81) 45-336-6551

MEMEC Asia Pacific  
(Rep/Dist.)  
4th Floor Myungdang Bldg.  
152-62 Samsung-Dong  
Kangnam-Ku  
Seoul  
Korea  
phone: (82) 2 563-5277  
fax: (82) 2 563-5279

MEMEC Asia Pacific(Rep)  
14F-1, 171 Section 58  
Min Sheng East Road  
Hai Hwa Building  
Taipei  
Taiwan  
phone: (886) 2 760 2028  
fax: (886) 2 765-1488

Jung Tai Electronic Co. Ltd.  
(Dist.)  
47 Park Ave. II, Suite 104  
Science-Based Industrial Park  
Hsinchu  
Taiwan 30077, R.O.C.  
phone: (886) 2 762 8102  
fax: (886) 2 762-3259

ALLY, Inc. (Dist.)  
7F, 18, Alley 1 Lane 768, Sec. 4  
Pa Teh Rd., Taipei, Taiwan,  
R.O.C.  
phone: (886) 2 788-6270  
fax: (886) 2 786-3550

MEMEC Asia Pacific (Rep)  
10 Anson Rd., #14 -02, Int'l Plaza  
Singapore 0207, Singapore  
phone: (65) 222-4962  
fax: (65) 222-4939

Serial System Marketing  
(Rep/Dist.)  
11 Jalan Mesin  
Standard Industrial Bldg, #06-00  
Singapore 1336  
phone: (65) 280-0200  
fax: (65) 286-6723

MEMEC Asia Pacific  
(Rep/Dist.)  
Unit No 2520-2525  
Tower 1  
Metroplaza  
Hing Fong Road  
Kwai Fong, N.T.,  
Hong Kong  
phone: (852) 410-2780  
fax: (852) 418-1600

ZATEK Components Pty Ltd.  
(Rep/Dist.)  
Suite 8, 1059 Victoria Rd.  
West Ryde 2114  
Sydney, Australia  
phone: (61) 2-874-0122  
fax: (61) 2-874-6171

## Europe

---

NEWTEK (Rep/Dist.)  
8, rue de l'Estere  
SILIC 583  
94663 Rungis Cedex  
France  
phone: (33) 1-46.87.22.00  
fax: (33) 1-46.87.80.49

Kudos Thame Ltd. (Rep/Dist.)  
55 Suttons Park, London Rd.  
Reading, BERKS RG6 1AZ  
United Kingdom  
phone: (44) 734-351010  
fax: (44) 734-351030

Metronik GmbH (Rep/Dist.)  
Leonhardsweg 2  
8025 Unterhaching  
Germany  
phone: (49) 89-61108-0  
fax: (49) 89-6116858

