65550/554

HiQVideo™ Series
Mode Support
(Including Video Capture/Playback)

Application Note
Revision 1.4

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P R E L I M I N A R Y

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Revision History

Revision	Date	By	Comment
0.1	3/16/95	DJ/st	Draft - Internal Review
1.0	4/19/95	ST	Official Release
1.1	6/30/95	BU/lc	Added 85Hz modes and 1024 x 768 (56Hz) to Table 1-1; clarified 554 DRAM options.
1.2	9/6/95	DJ/lc	Merged “Mode Support with Video Overlay”; added miscellaneous additional modes; clarified mode support restrictions and notes, including analysis of DRAM-C bandwidth limitations; revised analysis of STN-DD panel support considerations; deleted references to 65552; removed 65554 from 32-bit modes.
1.3	1/4/96	SP/lc	Removed confidential markings.
1.4	2/16/96	SP/lc	Added numbered sections. Changed table numbers. Updated display memory size requirements.

Table of Contents

List of Tables

HiQVideo™ Series Mode Support

1.0 Introduction

Several key factors determine which Super VGA graphics modes the HiQVideo ™ controllers (65550/65554) can support:

- Display memory size requirements
- Dot clock requirement (display pixel rate)
- Memory bandwidth requirement (bytes per pixel, pixel rate, and bandwidth available to CPU)
- DRAM "C" memory bandwidth when using an external DD buffer with an STN-DD panel
- For simultaneous CRT and panel operation, compatibility between panel timing requirem ents and CRT requirements.

This Application Note summarizes the mode support capabilities of the 65550/65554 VGA Controllers and explains how to derive the summary tables. The tables in section three show the mode support without video overlay. The tables in section 4 show mode support with video overlay.

General note: The tables in this application note are designed to provide a representative list of the most memory bandwidth intensive modes, not necessarily a complete list of all modes that the VGA BIOS can support. Refer to BIOS documentation for more information about VGA BIOS mode support.

2.0 Specific Notes for the Mode Support Tables

The tables specify the minimum MCLK frequency needed to support each mode. Higher MCLK frequencies require faster DRAMs. Refer to the specific notes below for a list of choices.

The 65550 a 32-bit (64-bit on the 65554) wide memory interface, plus an optional 16-bit wide DRAM "C" interface to support an external STN-DD buffer.

STN-DD panels require additional buffering compared to TFT panels and CRT displays. STN-DD panels usually are divided into upper and lower half-panels, which must be refreshed simultaneously. A "DD" buffer allows pixels to be read from display memory in a single-scan manner while refreshing the STN-DD panel in a dual-drive ("DD") manner. The DD buffer can either be embedded in the main display memory in an off-screen area or located in a separate external DD buffer memory. This external DD buffer memory is also known as DRAM "C". In either case, the DD buffer can be either full-frame or half-frame.

With a half-frame DD buffer, the refresh rate of the STN-DD panel (FLM frequency) is double the refresh rate of the CRT. This doubling effect is also referred to as frame acceleration. In all of the STN-DD mode listed, frame acceleration can be used to achieve a panel refresh rate twice as high as the specified refresh rate, except in cases where frame acceleration is already assumed to be enabled. See note (P) below. Frame acceleration and STN-DD buffering are discussed further in a later section of this Application Note.

All the DD buffer sizes shown in the tables are full-frame. With frame acceleration enabled, the DD buffer size is half the value shown. Also, the video capture buffer size shown in the tables is for double buffering. With single buffering, the buffer size will be half the amount shown in the tables.

The tables use the following symbols **:**

40 MHz	Mode can be supported without restrictions if MCLK is 40 MHz. 60 ns EDO DRAM (or faster) is required.
33 MHz	Mode can be supported without restrictions if MCLK is 33 MHz. 70 ns EDO DRAM (or faster) is required.
28 MHz	Mode can be supported without restrictions if MCLK is 28 MHz. 60 ns standard DRAM (or 70 ns EDO) is required.
25 MHz	Mode can be supported without restrictions if MCLK is 25 MHz. 70 ns standard or EDO DRAM is required.
20 MHz	Mode can be supported without restrictions if MCLK is 20 MHz. 70 ns standard or EDO DRAM should be used. Somewhat slower DRAM may be usable, also (TBD).
xx (y)	Mode can be supported with MCLK equal to "xx" MHz with the corresponding DRAM listed above. The restriction indicated by (y) below also applies. For example, “40(B)” indicates the mode requires a 40MHz MCLK and restriction (B) below applies. Similarly, “40(BD)” means both restrictions (B) and (D) apply.
(B)	Mode slightly exceeds the computed bandwidth of the main display memory and/or the external DD buffer (DRAM "C"), if applicable. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.
(D)	Mode can be supported at 5V but not 3.3V, because of the DCLK limit (80 MHz max. at 3.3V, 110 MHz max. at 5V).
(E)	Simultaneous CRT and panel operation requires an external DD buffer because of main memory bandwidth or size limitations. Panel-only operation can be supported with either an embedded or external DD buffer (see "P" below). This note does not apply to TFT panels, which do not require a DD buffer.
(P)	Panel only. Graphics raster registers and DCLK must be programmed for half the specified refresh rate, and frame acceleration must be enabled to achieve the specified panel FLM frequency. Memory bandwidth limitations prevent simultaneous operation with a CRT.
(H)	The driver will compensate for short horizontal blanking time to optimize vertical interpolation. (This note applies only when using video capture and playback.)
(S)	Video capture must be single buffered instead of double buffered to remain within the memory size limit. (This note applies only when using video capture and playback.)
N(M)	Mode cannot be supported because it exceeds the bandwidth limit of the main display memory and/or the external DD buffer (DRAM "C"), if applicable.
N(Z)	Mode cannot be supported because it exceeds the memory size limit.
N(K)	Mode cannot be supported because it exceeds the DC LK limit at both 3.3V and 5V.

3.0 CRT and TFT Support without Video Overlay

Table 3-1: CRT/TFT Mode Support

Resolution and Color Depth	Screen Refresh	Horiz. Freq.	Dot Clock	Display Memory +Cursor/Popup	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	37.5 KHz	31.5 MHz	300 KB + 4.2 KB	20 MHz	20 MHz
640 x 480 x 8 bpp	85 Hz	43.3 KHz	36 MHz	300 KB + 4.2 KB	20 MHz	20 MHz
640 x 480 x 16 bpp	75 Hz	37.5 KHz	31.5 MHz	600 KB + 4.2 KB	25 MHz	20 MHz
640 x 480 x 16 bpp	85 Hz	43.3 KHz	36 MHz	600 KB + 4.2 KB	28 MHz	20 MHz
640 x 480 x 24 bpp	60 Hz	31.5 KHz	25.175 MHz	900 KB + 4.2 KB	28 MHz	20 MHz
640 x 480 x 24 bpp	75 Hz	37.5 KHz	31.5 MHz	900 KB + 4.2 KB	40 MHz	20 MHz
640 x 480 x 24 bpp	85 Hz	43.3 KHz	36 MHz	900 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 8 bpp	60 Hz	37.9 KHz	40 MHz	469 KB + 4.2 KB	20 MHz	20 MHz
800 x 600 x 8 bpp	75 Hz	46.9 KHz	49.5 MHz	469 KB + 4.2 KB	20 MHz	20 MHz
800 x 600 x 8 bpp	85 Hz	53.7 KHz	56.25 MHz	469 KB + 4.2 KB	25 MHz	20 MHz
800 x 600 x 16 bpp	56 Hz	35.1 KHz	36 MHz	938 KB + 4.2 KB	28 MHz	20 MHz
800 x 600 x 16 bpp	60 Hz	37.9 KHz	40 MHz	938 KB + 4.2 KB	33 MHz	20 MHz
800 x 600 x 16 bpp	75 Hz	46.9 KHz	49.5 MHz	938 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 16 bpp	85 Hz	53.7 KHz	56.25 MHz	938 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 24 bpp	56 Hz	35.1 KHz	36 MHz	1406 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	1406 KB + 4.2 KB	40(B)	25 MHz
800 x 600 x 24 bpp	75 Hz	46.9 KHz	49.5 MHz	1406 KB + 4.2 KB	N(M)	28 MHz
800 x 600 x 24 bpp	85 Hz	53.7 KHz	56.25 MHz	1406 KB + 4.2 KB	N(M)	33 MHz
1024 x 768 x 8 bpp	60 Hz	48.4 KHz	65 MHz	768 KB + 4.2 KB	25 MHz	20 MHz
1024 x 768 x 8 bpp	75 Hz	60.0 KHz	78.75 MHz	768 KB + 4.2 KB	28 MHz	20 MHz
1024 x 768 x 8 bpp	85 Hz	68.7 KHz	94.5 MHz	768 KB + 4.2 KB	40(D)	20(D)
1024 x 768 x 16 bpp	56 Hz	45.2 KHz	60.7 MHz	1536 KB + 4.2 KB	40(B)	25 MHz
1024 x 768 x 16 bpp	60 Hz	48.4 KHz	65 MHz	1536 KB + 4.2 KB	N(M)	25 MHz
1024 x 768 x 16 bpp	75 Hz	60.0 KHz	78.75 MHz	1536 KB + 4.2 KB	N(M)	28 MHz
1024 x 768 x 16 bpp	85 Hz	68.7 KHz	94.5 MHz	1536 KB + 4.2 KB	N(M)	40(D)
1024 x 768 x 24 bpp	75 Hz	60.0 KHz	78.75 MHz	2304 KB + 4.2 KB	N(ZM)	40(B)
1024 x 768 x 24 bpp	85 Hz	68.7 KHz	94.5 MHz	2304 KB + 4.2 KB	N(ZM)	N(M)
1280 x 1024 x 8 bpp	43 Hz*	47 KHz	78.75 MHz	1280 KB + 4.2 KB	28 MHz	20 MHz
1280 x 1024 x 8 bpp	60 Hz	64 KHz	108 MHz	1280 KB + 4.2 KB	40(D)	20(D)
1280 x 1024 x 8 bpp	85 Hz	91.2 KHz	157.5 MHz	1280 KB + 4.2 KB	N(KM)	N(K)
1280 x 1024 x 16 bpp	43 Hz*	47 KHz	78.75 MHz	2560 KB + 4.2 KB	N(ZM)	28 MHz
1280 x 1024 x 16 bpp	60 Hz	64 KHz	108 MHz	2560 KB + 4.2 KB	N(ZM)	40(D)
1280 x 1024 x 24 bpp	43 Hz*	47 KHz	78.75 MHz	3840 KB + 4.2 KB	N(ZM)	40(B)
1280 x 1024 x 24 bpp	60 Hz	64 KHz	108 MHz	3840 KB + 4.2 KB	N(ZM)	N(M)

* 43 Hz modes are interlaced. Interlacing is supported for CRT only. Except for interlacing, Table 3-1 applies to TFT panels as well as CRT displays, including simultaneous CRT and TFT operation.

3.1 640 x 480 STN-DD Support without Video Overlay

Table 3-2: 640 x 480 STN DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300 KB + 120 KB + 4.2 KB	25 MHz	20 MHz
640 x 480 x 16 bpp	75 Hz	600 KB + 120 KB + 4.2 KB	40 MHz	20 MHz
640 x 480 x 16 bpp	85 Hz	600 KB + 120 KB + 4.2 KB	40 MHz	20 MHz
640 x 480 x 24 bpp	75 Hz	900 KB + 120 KB + 4.2 KB	40(B)	25 MHz
800 x 600 x 8 bpp	75 Hz	469 KB + 120 KB + 4.2 KB	25 MHz	20 MHz
800 x 600 x 16 bpp	75 Hz	938 KB + 120 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 24 bpp	75 Hz	1406 KB + 120 KB + 4.2 KB	40(B)	25 MHz
1024 x 768 x 8 bpp	75 Hz	768 KB + 120 KB + 4.2 KB	25 MHz	20 MHz
1024 x 768 x 16 bpp	75 Hz	1536 KB + 120 KB + 4.2 KB	40 MHz	20 MHz
1024 x 768 x 24 bpp	75 Hz	2304 KB + 120 KB + 4.2 KB	N(Z)	25 MHz
1280 x 1024 x 8 bpp	75 Hz	1280 KB + 120 KB + 4.2 KB	25 MHz	20 MHz
1280 x 1024 x 16 bpp	75 Hz	2560 KB + 120 KB + 4.2 KB	N(Z)	20 MHz
1280 x 1024 x 24 bpp	75 Hz	3840 KB + 120 KB + 4.2 KB	N(Z)	25 MHz

Table 3-3: 640 x 480 STN DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300 KB + 37.5 KB + 4.2 KB	20 MHz	20 MHz
640 x 480 x 16 bpp	75 Hz	600 KB + 37.5 KB + 4.2 KB	28 MHz	20 MHz
640 x 480 x 24 bpp	75 Hz	900 KB + 37.5 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 8 bpp	75 Hz	469 KB + 37.5 KB + 4.2 KB	20 MHz	20 MHz
800 x 600 x 16 bpp	75 Hz	938 KB + 37.5 KB + 4.2 KB	28 MHz	20 MHz
800 x 600 x 24 bpp	75 Hz	1406 KB + 37.5 KB + 4.2 KB	40 MHz	20 MHz
1024 x 768 x 8 bpp	75 Hz	768 KB + 37.5 KB + 4.2 KB	20 MHz	20 MHz
1024 x 768 x 16 bpp	75 Hz	1536 KB + 37.5 KB + 4.2 KB	28 MHz	20 MHz
1024 x 768 x 24 bpp	75 Hz	2304 KB + 37.5 KB + 4.2 KB	N(Z)	20 MHz
1280 x 1024 x 8 bpp	75 Hz	1280 KB + 37.5 KB + 4.2 KB	20 MHz	20 MHz
1280 x 1024 x 16 bpp	75 Hz	2560 KB + 37.5 KB + 4.2 KB	N(Z)	20 MHz
1280 x 1024 x 24 bpp	75 Hz	3840 KB + 37.5 KB + 4.2 KB	N(Z)	20 MHz

3.2 800 x 600 STN-DD Support Without Video Overlay

Table 3-4: 800 x 600 STN DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300 KB + 120 KB + 4.2 KB	28 MHz	20 MHz
640 x 480 x 16 bpp	75 Hz	600 KB + 120 KB + 4.2 KB	40(B)	25 MHz
640 x 480 x 24 bpp	75 Hz	900 KB + 120 KB + 4.2 KB	40(EB)	28 MHz
800 x 600 x 8 bpp	75 Hz	469 KB + 188 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 8 bpp	80 Hz	469 KB + 188 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 8 bpp	85 Hz	469 KB + 188 KB + 4.2 KB	40 MHz	20 MHz
800 x 600 x 16 bpp	75 Hz	938 KB + 188 KB + 4.2 KB	40(E)	28 MHz
800 x 600 x 16 bpp	80 Hz	938 KB + 188 KB + 4.2 KB	40(E)	28 MHz
800 x 600 x 16 bpp	85 Hz	938 KB + 188 KB + 4.2 KB	40(E)	33 MHz
800 x 600 x 24 bpp	75 Hz	1406 KB + 188 KB + 4.2 KB	40(P)	40 MHz
800 x 600 x 24 bpp	85 Hz	1406 KB + 188 KB + 4.2 KB	40(P)	40 MHz
1024 x 768 x 8 bpp	75 Hz	768 KB + 188 KB + 4.2 KB	40 MHz	20 MHz
1024 x 768 x 16 bpp	75 Hz	1536 KB + 188 KB + 4.2 KB	40(E)	28 MHz
1024 x 768 x 24 bpp	75 Hz	2304 KB + 188 KB + 4.2 KB	N(Z)	40 MHz
1280 x 1024 x 8 bpp	75 Hz	1280 KB + 188 KB + 4.2 KB	40 MHz	20 MHz
1280 x 1024 x 16 bpp	75 Hz	2560 KB + 188 KB + 4.2 KB	N(Z)	28 MHz
1280 x 1024 x 24 bpp	75 Hz	3840 KB + 188 KB + 4.2 KB	N(Z)	40 MHz

Table 3-5: 800 x 600 STN DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300 KB + 37.5 KB + 4.2 KB	20 MHz	20 MHz
640 x 480 x 16 bpp	75 Hz	600 KB + 37.5 KB + 4.2 KB	33 MHz	20 MHz
640 x 480 x 24 bpp	75 Hz	900 KB + 37.5 KB + 4.2 KB	40(EB)	25 MHz
800 x 600 x 8 bpp	75 Hz	469 KB + 58.6 KB + 4.2 KB	25 MHz	20 MHz
800 x 600 x 16 bpp	75 Hz	938 KB + 58.6 KB + 4.2 KB	40(B)	25 MHz
800 x 600 x 24 bpp	75 Hz	1406 KB + 58.6 KB + 4.2 KB	33(P)	33 MHz
1024 x 768 x 8 bpp	75 Hz	768 KB + 58.6 KB + 4.2 KB	25 MHz	20 MHz
1024 x 768 x 16 bpp	75 Hz	1536 KB + 58.6 KB + 4.2 KB	40(B)	25 MHz
1024 x 768 x 24 bpp	75 Hz	2304 KB + 58.6 KB + 4.2 KB	N(Z)	33 MHz
1280 x 1024 x 8 bpp	75 Hz	1280 KB + 58.6 KB + 4.2 KB	25 MHz	20 MHz
1280 x 1024 x 16 bpp	75 Hz	2560 KB + 58.6 KB + 4.2 KB	N(Z)	25 MHz
1280 x 1024 x 24 bpp	75 Hz	3840 KB + 58.6 KB + 4.2 KB	N(Z)	33 MHz

3.3 1024 x 768 STN-DD Support without Video Overlay

Table 3-6: 1024 x 768 STN DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	70 Hz	300 KB + 120 KB + 4.2 KB	40 MHz	20 MHz
640 x 480 x 16 bpp	70 Hz	600 KB + 120 KB + 4.2 KB	40(E)	25 MHz
640 x 480 x 24 bpp	70 Hz	900 KB + 120 KB + 4.2 KB	40(P)	40 MHz
800 x 600 x 8 bpp	70 Hz	469 KB + 188 KB + 4.2 KB	40(B)	25 MHz
800 x 600 x 16 bpp	70 Hz	938 KB + 188 KB + 4.2 KB	40(EB)	33 MHz
800 x 600 x 24 bpp	70 Hz	1406 KB + 188 KB + 4.2 KB	40(PB)	40(B)
1024 x 768 x 8 bpp	70 Hz	768 KB + 307 KB + 4.2 KB	28(P)	28 MHz
1024 x 768 x 16 bpp	70 Hz	1536 KB + 307 KB + 4.2 KB	40(P)	40 MHz
1024 x 768 x 24 bpp	70 Hz	2304 KB + 307 KB + 4.2 KB	N(Z)	28(P)
1280 x 1024 x 8 bpp	70 Hz	1280 KB + 307 KB + 4.2 KB	28(P)	28 MHz
1280 x 1024 x 16 bpp	70 Hz	2560 KB + 307 KB + 4.2 KB	N(Z)	40 MHz
1280 x 1024 x 24 bpp	70 Hz	3840 KB + 307 KB + 4.2 KB	N(Z)	28(P)

Table 3-7: 1024 x 768 STN DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Misc.	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	70 Hz	300 KB + 37.5 KB + 4.2 KB	25 MHz	20 MHz
640 x 480 x 16 bpp	70 Hz	600 KB + 37.5 KB + 4.2 KB	40 MHz	20 MHz
640 x 480 x 24 bpp	70 Hz	900 KB + 37.5 KB + 4.2 KB	28(P)	28 MHz
800 x 600 x 8 bpp	70 Hz	469 KB + 58.6 KB + 4.2 KB	28 MHz	20 MHz
800 x 600 x 16 bpp	70 Hz	938 KB + 58.6 KB + 4.2 KB	40(EB)	25 MHz
800 x 600 x 24 bpp	70 Hz	1406 KB + 58.6 KB + 4.2 KB	40(P)	40 MHz
1024 x 768 x 8 bpp	70 Hz	768 KB + 96 KB + 4.2 KB	40 MHz	20 MHz
1024 x 768 x 16 bpp	70 Hz	1536 KB + 96 KB + 4.2 KB	33(P)	33 MHz
1024 x 768 x 24 bpp	70 Hz	2304 KB + 96 KB + 4.2 KB	N(Z)	40(B)
1280 x 1024 x 8 bpp	70 Hz	1280 KB + 96 KB + 4.2 KB	40 MHz	20 MHz
1280 x 1024 x 16 bpp	70 Hz	2560 KB + 96 KB + 4.2 KB	N(Z)	33 MHz
1280 x 1024 x 24 bpp	70 Hz	3840 KB + 96 KB + 4.2 KB	N(Z)	40(B)

Note: 1024 x 768 STN-DD panels are not yet readily available.
The tables above are for future reference only.

4.0 CRT and TFT Support with Video Overlay

Table 4-1: CRT/TFT Mode Support with Video Overlay

Resolution and Color Depth	Screen Refresh	Horiz. Freq.	Dot Clock	Display Memory + Cursor + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	37.5 KHz	31.5 MHz	300KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 16 bpp	75 Hz	37.5 KHz	31.5 MHz	600KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 24 bpp	60 Hz	31.5 KHz	25.175 MHz	900KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 24 bpp	75 Hz	37.5 KHz	31.5 MHz	900KB + 4.2KB + 300KB	40MHz	20MHz
800 x 600 x 8 bpp	60 Hz	37.9 KHz	40 MHz	469KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 8 bpp	75 Hz	46.9 KHz	49.5 MHz	469KB + 4.2KB + 300KB	40MHz	25MHz
800 x 600 x 16 bpp	56 Hz	35.1 KHz	36 MHz	938KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 16 bpp	60 Hz	37.9 KHz	40 MHz	938KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 16 bpp	75 Hz	46.9 KHz	49.5 MHz	938KB + 4.2KB + 300KB	40MHz	25MHz
800 x 600 x 24 bpp	56 Hz	35.1 KHz	36 MHz	1406KB + 4.2KB + 300KB	40(B)	25MHz
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	1406KB + 4.2KB + 300KB	N(M)	25MHz
800 x 600 x 24 bpp	75 Hz	46.9 KHz	49.5 MHz	1406KB + 4.2KB + 300KB	N(M)	33MHz
1024 x 768 x 8 bpp	60 Hz	48.4 KHz	65 MHz	768KB + 4.2KB + 300KB	40(H)	25MHz
1024 x 768 x 8 bpp	75 Hz	60.0 KHz	78.75 MHz	768KB + 4.2KB+ 300KB	40(H)	33MHz
1024 x 768 x 16 bpp	60 Hz	48.4 KHz	65 MHz	1536KB + 4.2KB + 300KB	N(M)	25MHz
1024 x 768 x 16 bpp	75 Hz	60.0 KHz	78.75 MHz	1536KB + 4.2KB + 300KB	N(M)	33MHz
1024 x 768 x 24 bpp	75 Hz	60.0 KHz	78.75 MHz	2304KB + 4.2KB + 300KB	N(Z)	40(B)
1280 x 1024 x 8bpp	43 Hz*	47 KHz	78.75 MHz	1280 KB + 4.2 KB + 300KB	40(H)	25MHz
1280 x 1024 x 8bpp	60 Hz	64 KHz	108 MHz	1280 KB + 4.2 KB + 300KB	N(M)	33(D)
1280 x 1024 x 16bpp	43 Hz*	47 KHz	78.75 MHz	2560 KB + 4.2 KB + 300KB	N(Z)	33MHz
1280 x 1024 x 16bpp	60 Hz	64 KHz	108 MHz	2560 KB + 4.2 KB + 300KB	N(Z)	40(D)
1280 x 1024 x 24bpp	43 Hz*	47 KHz	78.75 MHz	3840 KB + 4.2 KB + 300KB	N(Z)	40(SB)
1280 x 1024 x 24bpp	60 Hz	64 KHz	108 MHz	3840 KB + 4.2 KB + 300KB	N(Z)	N(M)

* 43 Hz modes are interlaced. Interlacing is supported for CRT only. Except for interlacing, Table 4-1 applies to TFT panels as well as CRT displays, including simultaneous CRT and TFT operation.

4.1 640 x 480 STN-DD Support with Video Overlay

Table 4-2: 640 x 480 STN-DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300KB + 120KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 16 bpp	75 Hz	600KB + 120KB + 4.2KB + 300KB	40MHz	20MHz
640 x 480 x 24 bpp	75 Hz	900KB + 120KB + 4.2KB + 300KB	33(P)	25MHz
800 x 600 x 8 bpp	75 Hz	469KB + 120KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 16 bpp	75 Hz	938KB + 120KB + 4.2KB + 300KB	40MHz	20MHz
800 x 600 x 24 bpp	75 Hz	1406KB + 120KB + 4.2KB + 300KB	33(P)	25MHz
1024 x 768 x 8 bpp	75 Hz	768KB + 120KB + 4.2KB + 300KB	33MHz	20MHz
1024 x 768 x 16 bpp	75 Hz	1536KB + 120KB + 4.2KB + 300KB	40MHz	20MHz
1024 x 768 x 24 bpp	75 Hz	2304KB + 120KB + 4.2KB + 300KB	N(Z)	25MHz
1280 x 1024 x 8 bpp	75 Hz	1280KB + 120KB + 4.2KB + 300KB	33MHz	20MHz
1280 x 1024 x 16 bpp	75 Hz	2560KB + 120KB + 4.2KB + 300KB	N(Z)	20MHz
1280 x 1024 x 24 bpp	75 Hz	3840KB + 120KB + 4.2KB + 300KB	N(Z)	N(Z)

Table 4-3: 640 x 480 STN-DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 16 bpp	75 Hz	600KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
640 x 480 x 24 bpp	75 Hz	900KB + 37.5KB + 4.2KB + 300KB	40(B)	25MHz
800 x 600 x 8 bpp	75 Hz	469KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 16 bpp	75 Hz	938KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
800 x 600 x 24 bpp	75 Hz	1406KB + 37.5KB + 4.2KB + 300KB	40(B)	25MHz
1024 x 768 x 8 bpp	75 Hz	768KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
1024 x 768 x 16 bpp	75 Hz	1536KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
1024 x 768 x 24 bpp	75 Hz	2304KB + 37.5KB + 4.2KB + 300KB	N(Z)	25MHz
1280 x 1024 x 8 bpp	75 Hz	1280KB + 37.5KB + 4.2KB + 300KB	33MHz	20MHz
1280 x 1024 x 16 bpp	75 Hz	2560KB + 37.5KB + 4.2KB + 300KB	N(Z)	20MHz
1280 x 1024 x 24 bpp	75 Hz	3840KB + 37.5KB + 4.2KB + 300KB	N(Z)	N(Z)

4.2 800 x 600 STN-DD Support with Video Overlay

Table 4-4: 800 x 600 STN-DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300KB + 120KB + 4.2KB + 300KB	40MHz	25MHz
640 x 480 x 16 bpp	75 Hz	600KB + 120KB + 4.2KB + 300KB	40(P)	25MHz
640 x 480 x 24 bpp	75 Hz	900KB + 120KB + 4.2KB + 300KB	40(P)	33MHz
800 x 600 x 8 bpp	75 Hz	469KB + 188KB + 4.2KB + 300KB	40MHz	25MHz
800 x 600 x 16 bpp	75 Hz	938KB + 188KB + 4.2KB + 300KB	40(P)	33MHz
800 x 600 x 24 bpp	75 Hz	1406KB + 188KB + 4.2KB + 300KB	40(P)	40MHz
1024 x 768 x 8 bpp	75 Hz	768KB + 188KB + 4.2KB + 300KB	40MHz	25MHz
1024 x 768 x 16 bpp	75 Hz	1536KB + 188KB + 4.2KB + 300KB	40(P)	33MHz
1024 x 768 x 24 bpp	75 Hz	2304KB + 188KB + 4.2KB + 300KB	N(Z)	40MHz
1280 x 1024 x 8 bpp	75 Hz	1280KB + 188KB + 4.2KB + 300KB	40MHz	25MHz
1280 x 1024 x 16 bpp	75 Hz	2560KB + 188KB + 4.2KB + 300KB	N(Z)	33MHz
1280 x 1024 x 24 bpp	75 Hz	3840KB + 188KB + 4.2KB + 300KB	N(Z)	N(Z)

Table 4-5: 800 x 600 STN-DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	75 Hz	300KB + 37.5KB + 4.2KB + 300KB	40MHz	25MHz
640 x 480 x 16 bpp	75 Hz	600KB + 37.5KB + 4.2KB + 300KB	40MHz	25MHz
640 x 480 x 24 bpp	75 Hz	900KB + 37.5KB + 4.2KB + 300KB	40(P)	28MHz
800 x 600 x 8 bpp	75 Hz	469KB + 58.6KB + 4.2KB + 300KB	40MHz	25MHz
800 x 600 x 16 bpp	75 Hz	938KB + 58.6KB + 4.2KB + 300KB	40(B)	25MHz
800 x 600 x 24 bpp	75 Hz	1406KB + 58.6KB + 4.2KB + 300KB	40(P)	33MHz
1024 x 768 x 8 bpp	75 Hz	768KB + 58.6KB + 4.2KB + 300KB	40MHz	25MHz
1024 x 768 x 16 bpp	75 Hz	1536KB + 58.6KB + 4.2KB + 300KB	40(B)	25MHz
1024 x 768 x 24 bpp	75 Hz	2304KB + 58.6KB + 4.2KB + 300KB	N(Z)	33MHz
1280 x 1024 x 8 bpp	75 Hz	1280KB + 58.6KB + 4.2KB + 300KB	40MHz	25MHz
1280 x 1024 x 16 bpp	75 Hz	2560KB + 58.6KB + 4.2KB + 300KB	N(Z)	25MHz
1280 x 1024 x 24 bpp	75 Hz	3840KB + 58.6KB + 4.2KB + 300KB	N(Z)	N(Z)

4.3 1024 x 768 STN-DD Support with Video Overlay

Table 4-6: 1024 x 768 STN-DD Color Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	70 Hz	300KB + 120KB + 4.2KB + 300KB	40(HB)	33MHz
640 x 480 x 16 bpp	70 Hz	600KB + 120KB + 4.2KB + 300KB	40(P)	33MHz
640 x 480 x 24 bpp	70 Hz	900KB + 120KB + 4.2KB + 300KB	40(P)	40MHz
800 x 600 x 8 bpp	70 Hz	469KB + 188KB + 4.2KB + 300KB	40(P)	33MHz
800 x 600 x 16 bpp	70 Hz	938KB + 188KB + 4.2KB + 300KB	40(P)	40MHz
800 x 600 x 24 bpp	70 Hz	1406KB + 188KB + 4.2KB + 300KB	N(M)	40(B)
1024 x 768 x 8 bpp	70 Hz	768KB + 307KB + 4.2KB + 300KB	40(P)	33MHz
1024 x 768 x 16 bpp	70 Hz	1536KB + 307KB + 4.2KB + 300KB	N(M)	40(B)
1024 x 768 x 24 bpp	70 Hz	2304KB + 307KB + 4.2KB + 300KB	N(Z)	33(P)
1280 x 1024 x 8 bpp	70 Hz	1280KB + 307KB + 4.2KB + 300KB	40(P)	33MHz
1280 x 1024 x 16 bpp	70 Hz	2560KB + 307KB + 4.2KB + 300KB	N(Z)	40(B)
1280 x 1024 x 24 bpp	70 Hz	3840KB + 307KB + 4.2KB + 300KB	N(Z)	N(Z)

Table 4-7: 1024 x 768 STN-DD Monochrome Panel Support

Resolution in Display Memory	Screen Refresh	Display Memory + STN Buffer + Miscellaneous + Video Capture	65550 32-Bit	65554 64-Bit
640 x 480 x 8 bpp	70 Hz	300KB + 37.5KB + 4.2KB + 300KB	40(H)	33MHz
640 x 480 x 16 bpp	70 Hz	600KB + 37.5KB + 4.2KB + 300KB	40(PH)	33MHz
640 x 480 x 24 bpp	70 Hz	900KB + 37.5KB + 4.2KB + 300KB	40(PH)	33MHz
800 x 600 x 8 bpp	70 Hz	469KB + 58.6KB + 4.2KB + 300KB	40(H)	33MHz
800 x 600 x 16 bpp	70 Hz	938KB + 58.6KB + 4.2KB + 300KB	40(PH)	33MHz
800 x 600 x 24 bpp	70 Hz	1406KB + 58.6KB + 4.2KB + 300KB	40(PHB)	40MHz
1024 x 768 x 8 bpp	70 Hz	768KB + 96KB + 4.2KB + 300KB	40(HB)	33MHz
1024 x 768 x 16 bpp	70 Hz	1536KB + 96KB + 4.2KB + 300KB	40(PH)	33MHz
1024 x 768 x 24 bpp	70 Hz	2304KB + 96KB + 4.2KB + 300KB	N(Z)	33(P)
1280 x 1024 x 8 bpp	70 Hz	1280KB + 96KB + 4.2KB + 300KB	40(HB)	33MHz
1280 x 1024 x 16 bpp	70 Hz	2560KB + 96KB + 4.2KB + 300KB	N(Z)	33MHz
1280 x 1024 x 24 bpp	70 Hz	3840KB + 96KB + 4.2KB + 300KB	N(Z)	33(PS)

Note: 1024 x 768 STN-DD panels are not yet readily available.
The above tables are for future reference only.

5.0 Display Memory Size Requirements

The following figures show the display memory configurations for the 65550 and 65554.

32-bit Memory Bus (65550/65554)

1MB	256Kx16	256Kx16
1MB*	128Kx32	
	128Kx32	
1MB	256Kx32	
2MB	256Kx16	256Kx16
	256Kx16	256Kx16
2MB	256Kx32	
	256Kx32	
2MB	512Kx32	

64-bit Memory Bus (65554 Only)

1MB*	128Kx32		128Kx32	
2MB*	256Kx16	256Kx16	256Kx16	256Kx16
2MB*	128Kx32		128Kx32	
	128Kx32		128Kx32	
2MB*	256Kx32		256Kx32	
4MB*	256Kx16	256Kx16	256Kx16	256Kx16
	256Kx16	256Kx16	256Kx16	256Kx16
4MB*	256Kx32		256Kx32	
	256Kx32		256Kx32	
4MB*	512Kx32		512Kx32	

*65554 Only. Not available on 65550.

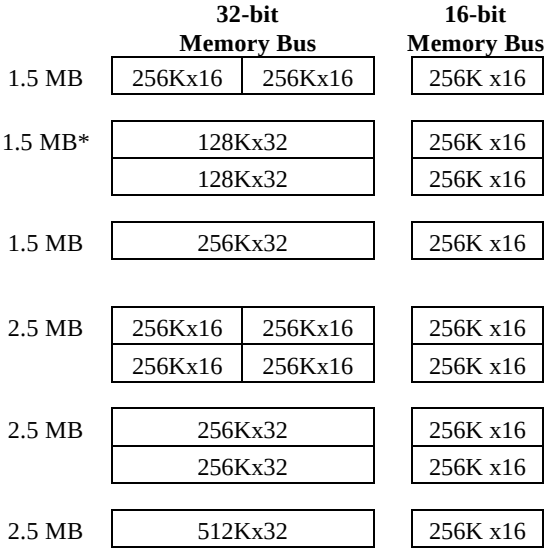
Figure 1: Display Memory Configurations

Notes:

- 1KB = 1024 bytes, 1MB = 1024KB
- The 32-bit wide memory configurations have the same performance on the 65554 as on the 65550.
- The 64-bit wide memory configurations have double the memory bandwidth of the 32-bit wide configurations.

5.1 External STN-DD Buffer

The following figure shows the display memory configurations using an external STN-DD buffer.



*65554 Only. Not available on 65550

Figure 2: Display Memory Configurations with an STN-DD Buffer

Notes:

- All of the 32-bit configurations allow an additional 256K x 16 device to be used for an external 16-bit wide STN-DD buffer, as shown above.
- Because of pin sharing on the 65550, video capture/playback precludes an external STN-DD buffer.
- Unlike the 65550, the 65554 supports both video capture/playback and an external STN-DD buffer at the same time.

The total required display memory size is the sum of the following:

- Number of pixels to be stored in display memory, mul tiplied by the number of bytes per pixel (1 byte for 8 bpp, 2 bytes for 16 bpp, 3 bytes for 24 bpp).

  Example: 1024 x 768 x 24 bpp = 2304 KB

  This exceeds the 2 MB limit for the 65550, but is within the 4 MB size limit for the 65554.

- For Color STN-DD panels, add 0.4 byte per pixel for DD buffering (3 bits per pixel, packed as 10 pixels per DWORD). For monochrome STN-DD panels, add 0.125 byte per pixel (1 bit per pixel packed 32 pixels per DWORD).

  Example: 800 x 600 x 0.4 byte/pixel = 192,000 bytes needed for full frame buffer for color STN-DD panel, or 96,000 bytes (93.75 KB) for half-frame DD buffer.

  STN-DD panels require buffering because the panel needs the upper and lower halves refreshed simultaneously. These panels also need Frame Rate Control (FRC) to achieve more colors than the panel itself supports directly. The buffer can be either full frame or half-frame, and can reside either in main display memory (off-screen area) or in a separate "C" DRAM. The main tradeoffs are as follows:

  Full Frame Buffer vs Half Frame Buffer
  - Half-frame DD buffer uses half as much memory as a full frame DD buffer.
  - Half-frame DD buffer requires panel pixel rate to be double the CRT pixel rate when using simultaneous CRT and panel display mode. This effect is known as “Frame Acceleration.”
  - In simultaneous operation, if the CRT refresh rate is relatively slow, such as 60 Hz, the panel can run at 120 Hz refresh (FLM frequency) to achieve optimum panel display quality. However, if the CRT refresh is very fast, such as 85 Hz, the panel can run at 85 Hz instead of 170 Hz if 170 Hz exceeds the limitations of the panel.
  - For panel-only operation with a half-frame DD buffer, the pixel rate imposed on the display memory is half the panel pixel rate. This means higher resolution modes can be supported at any given panel refresh rate (FLM frequency) than on a CRT at the same refresh rate (VSYNC frequency).

  External DD buffer
  - Eliminates any added burden on display memory bandwidth for buffer a ccesses.
  - May allow finer granularity in total memory, e.g., 1.5 MB total instead of 2 MB total.
  - On the 550 only, precludes use of the multi-media video port (due to shared pin functions).
  - Usable only for panel buffering.

  DD Buffer Embedded in Main Display Memory (off-screen area)
  - Allows DRAM "C" pins to remain available for the multimedia video port.
  - Imposes extra burden on display memory bandwidth due to buffer reads and writes.
  - The remaining off-screen display memory spa ce is highly usable by software drivers for improving overall graphics performance.

- Cursor and popup require 2 KB each (e.g., 128 x 128 x 1 bpp), 4 KB total.

- Up to 200 bytes of additional memory (64 pixels x 24 bpp) may also be needed in connection with bit blitting.

- A multi-media video capture buffer, if used, typically needs 320 x 240 x 16 bpp = 150 KB. If double-buffering is selected (programmable option), multiply by two.

6.0 Display Memory Bandwidth Consumption

The 65550 and 65554 typically access memory in bursts of one RAS-CAS cycle followed by a series of back-to-back CAS-only cycles. The CAS-only cycles require only one MCLK cycle per access. Thus, for an MCLK frequency of 40 MHz, the burst bandwidth is 160 MB/sec for 32-bit wide memory, 320 MB/sec for 64-bit wide memory, and 80 MB/sec for 16-bit wide DRAM "C". After allowing for RAS overhead and CPU accesses, the maximum memory bandwidths usable for graphics refresh are approximately as follows (40 MHz MCLK):

- 32-bit wide display memory, 65550 or 65554 — 112 MB/sec
- 64-bit wide display memory, 65554 only — 224 MB/sec
- 16-bit wide DRAM "C" — 64 MB/sec

These bandwidth limits scale proportionally downward for lower MCLK frequencies. (1 MB/sec = 1,000,000 bytes per second.)

Memory bandwidth is usually most critical during the horizontal active time, e.g., while displaying a horizontal scan line on the display. To determine if there is sufficient bandwidth for a given graphics mode, the following factors must be considered:

(1) Display pixel rate. For example, 1024 x 768 x 24 bpp @ 75 Hz requires a pixel rate of 78.75 MHz. The resulting bandwidth requirement is 78.75 MHz x 3 bytes/pixel = 236.25 MB/sec. This is too fast for the 65550, and exceeds the 64-bit wide 65554 memory bandwidth by about 5%.

(2) STN-DD buffer overhead. If the panel is an STN-DD type, there is additional bandwidth burden for DD buffer access. Color STN-DD panels require an average of 1.0 bytes of access per pixel (0.4 byte read, 0.4 byte write, and 0.2 byte to allow for added RAS overhead due to shorter bursts). Monochrome STN-DD panels require an average of 0.3 bytes of access per pixel (0.125 byte write, 0.125 byte read, and 0.05 byte to allow for added RAS overhead). Neither the graphics color depth (e.g., 16 bpp or 24 bpp), nor frame acceleration affects the DD buffer overhead. Frame acceleration doubles the panel refresh rate without any increase in memory bandwidth usage. The DD buffer overhead is also the same for both the embedded and external DD buffers. If using an embedded buffer, add the DD buffer bandwidth burden to the display pixel rate. The DRAM "C" bandwidth limit does not apply. If using an external DD buffer, compare the DD buffer bandwidth requirement to the DRAM "C" bandwidth limit. This case does not add to the display pixel rate.

(3) Video capture pixel rate. The capture rate is typically 6.2 Mpps with 16 bpp (YUV). The effective bandwidth burden is 12.4 MB/sec, which must be added to the display pixel rate if video capture/playback is enabled.

(4) Video playback burden. This burden is usually negligible because each video playback line is loaded into an internal FIFO during horizontal blanking. There is no burden on memory bandwidth during the horizontal active interval unless the blanking interval is too short to allow a complete FIFO fill. It is probably not feasible to provide a simple guideline for the short-blanking cases, but the mode support tables account for them. The calculation involves estimating the number of playback bytes that can be fetched during horizontal blanking, and the number of remaining bytes (if any) that need to be fetched during the horizontal active interval. The calculations are best performed using a spreadsheet program or equivalent.

The following page shows an example of the display memory bandwidth usage with both 32-bit and 64-bit memory.

Example: 800 x 600 x 8 bpp @ 85 Hz on a color STN-DD panel, with 320 x 240 video capture/playback.

The corresponding graphics pixel rate is 56.250 MHz, and the horizontal frequency is 53.674 KHz. Graphics bandwidth is 56.25 MB/sec. DD buffer overhead is also 56.25 MB/sec. Video capture overhead is 12.4 MB/sec.

With 32-bit wide memory and an external DD buffer, the display memory bandwidth needed is 56.25 + 12.4 = 68.65 MB/sec. The DRAM "C" bandwidth is 56.25 MB/sec. Both bandwidth requirements are within the capabilities of the 65550 and 65554. The display memory bandwidth utilization is 68.65 ÷ 112 = 61% (if MCLK is 40 MHz). DRAM "C" bandwidth utilization is 56.25 ÷ 64 = 88%. A more precise calculation for video playback overhead shows that approximately 556 bytes of video playback data can be fetched and loaded into the FIFO during the 4.4 µs horizontal blanking interval, leaving only 84 additional bytes to fetch during the horizontal active interval. The added 84 bytes increase the bandwidth usage by only 6%, still well within the capabilities of the 65550 and 65554.

With 64-bit memory, the total bandwidth requirement is 56.25 + 56.25 + 12.4 = 124.9 MB/sec. This also is within the capabilities of the 65554, and there is no video playback burden in this case because of the doubled memory bandwidth. The display memory bandwidth utilization is 124.9 ÷ 224 = 56%.

It is possible for the image resolution in display memory to be larger or smaller than the physical resolution of the CRT and panel. The image resolution in display memory does not affect panel and CRT timing. If the resolution in display memory is greater than the physical resolution of the panel and CRT, panning is used on both the CRT and the panel to display a smaller region taken from the total image. If the image size is smaller, the image is displayed on both the CRT and panel using centering and stretching to achieve optimum image appearance and positioning. Panel and CRT timing remain consistent with their physical requirements even though the displayed image is smaller.

Panning has no effect on display memory bandwidth, but stretching may have a slight beneficial effect. Horizontal stretching involves replication and optional averaging of consecutive pixels. The affected pixels are read from display memory only once. The 65550 and 65554 perform the replication as needed without re-reading the pixel data. As a result, the total number of pixels read from display memory for any particular horizontal scan line is determined by the image resolution in display memory, which may be less horizontally than the stretched image size shown on the CRT and panel. The mode support tables include this effect. The 65550 and 65554 are capable of the following horizontal stretch factors: 8:9, 8:10, 8:12, or 8:16. Examples:

640 dots can stretch to 800 (for 800-dot panel) using 8:10.

640 dots can stretch to 960 (for 1024-dot panel) using 8:12.

640 dots can stretch to 1280 (for 1280-dot panel) using 8:16.

800 dots can stretch to 1000 (for 1024-dot panel) using 8:10.

800 dots can stretch to 1200 (for 1280-dot panel) using 8:12.

1024 dots can stretch to 1280 (for 1280-dot panel) using 8:10.

7.0 STN-DD Comparisons and Tradeoffs

STN-DD panels typically have characteristics similar to the following:

- The panel is divided equally into upper and lower regions, which must be refreshed simultaneously.
- Color STN-DD panels have three bits per pixel (red, green, blue), allowing up to 8 colors to be displayed (including black). The 65550 and 65554 can modulate the R, G, B data over multiple frames (up to 16 frames) to expand the perceived color space into roughly 16 levels per primary color, 4096 colors total. This is approximately equivalent to 12 bpp. The RGB modulation is referred to as Frame Rate Control (FRC).
- The data width to the panel is typically 16 bits, allowing 16 pixels to be sent to the panel with every three data transfers. A shift clock (SHFCLK) marks the data transfers.
- Monochrome STN-DD panels have one bit per pixel and transfer 16 pixels in ea ch 16-bit data word. Some monochrome panels may have only an 8-bit wide data bus and transfer 8 pixels per SHFCLK.
- A latch pulse (LP) signal indicates the start of each horizontal scan. The panel scans two lines for each LP -- one line in the upper half of the panel and one line in the lower half.
- A first line marker (FLM) signal indicates the start of the frame.

The 65550 and 65554 use a DD buffer to allow the system to read pixels from display memory in a single-scan manner, while refreshing the STN-DD panel in a dual-drive (DD) manner. The DD buffer also facilitates the Frame Rate Control process (FRC) for expanding the perceived color depth from 8 to about 4096 colors.

Full-frame DD buffer operation. For every two pixels read out of display memory and sent to the CRT, two pixels are read from the DD buffer and sent to the panel. During the same interval, the two pixels sent to the CRT are subjected to FRC calculation and written into the DD buffer. There are a total of two DD buffer reads and two DD buffer writes for every two CRT pixels. The panel pixel rate is the same as the CRT pixel rate.

Half-frame DD buffer operation. Unlike the full-frame buffer, as each pixel is read from display memory and sent to the CRT, the same pixel is subjected to FRC calculation and sent to the panel. The pixel is processed for additional FRC and written into the DD buffer. During the same interval, a second pixel is read from the DD buffer and sent to the panel. There is a total of one DD buffer read and one DD buffer write for every CRT pixel. This is the same ratio of DD buffer accesses per CRT pixel as with a full-frame buffer, but two pixels instead of one are sent to the panel for each pixel sent to the CRT. The panel pixel rate and frame rate are double the CRT rates, which is also referred to as Frame Acceleration.

Note that the pixel relationships described above are short-term averages. There is actually extensive FIFO buffering to smooth out the cycle-by-cycle memory accesses.

Table 7-1 illustrates the timing relationships between CRT and panel, with and without frame acceleration.

Table 7-1: Timing Relationship Examples

640 x 480 @ 60 Hz	CRT	STN-DD Color with Frame Acceleration
Vertical refresh rate	60 Hz	120 Hz (FLM)
Horizontal rate	31.5 KHz	31.5 KHz (LP)
Pixel clock	25.175 MHz	9.44 MHz (SHFCLK)
Pixel rate	25.175 Mpps	50.35 Mpps
Horizontal blanking factor	1.25	1.25
Vertical blanking factor	1.09	1.09
Combined blanking factor	1.37	1.37

640 x 480 @ 85 Hz	CRT	STN-DD Color no Frame Acceleration
Vertical refresh rate	85 Hz	85 Hz (FLM)
Horizontal rate	43.269 KHz	21.635 KHz (LP)
Pixel clock	36 MHz	6.75 MHz (SHFCLK)
Pixel rate	36 Mpps	36 Mpps
Horizontal blanking factor	1.30	1.30
Vertical blanking factor	1.06	1.06
Combined blanking factor	1.38	1.38

800 x 600 @ 60 Hz	CRT	STN-DD Color with Frame Acceleration
Vertical refresh rate	60 Hz	120 Hz (FLM)
Horizontal rate	37.9 KHz	37.9 KHz (LP)
Pixel clock	40 MHz	15 MHz (SHFCLK)
Pixel rate	40 Mpps	80 Mpps
Horizontal blanking factor	1.32	1.32
Vertical blanking factor	1.05	1.05
Combined blanking factor	1.39	1.39

800 x 600 @ 85 Hz	CRT	STN-DD Color no Frame Acceleration
Vertical refresh rate	85 Hz	85 Hz (FLM)
Horizontal rate	53.674 KHz	26.837 KHz (LP)
Pixel clock	56.25 MHz	10.55 MHz (SHFCLK)
Pixel rate	56.25 Mpps	56.25 Mpps
Horizontal blanking factor	1.31	1.31
Vertical blanking factor	1.05	1.05
Combined blanking factor	1.38	1.38

Note that the LP rate without frame acceleration is half the CRT horizontal frequency. This is because the panel scans two horizontal lines for each LP pulse. Frame acceleration doubles the LP rate, making it the same as the CRT horizontal frequency.

STN-DD panels often need 100 Hz to 120 Hz refresh for best display quality, particularly with 16-frame FRC. In general, frame acceleration should be used for panels with slower CRT refresh rates. For higher CRT refresh rates, the resulting 2X panel refresh rate may be too fast for the panel. In that case, frame acceleration can be disabled, resulting in equal panel and CRT refresh rates.

For a given CRT refresh rate, the required display memory bandwidth usage is the same with, or without, frame acceleration. The number of display memory and DD buffer accesses per CRT pixel is exactly the same in both cases.

In panel only operation, the system can significantly reduce (as compared to simultaneous operation) the required display memory bandwidth by using frame acceleration, a reduced panel refresh rate, and reduced blinking factors. This may allow additional high-performance graphics mode support in panel-only operation but not in simultaneous operation, as long as the reduced panel refresh rate can provide acceptable display quality. For example, instead of running the panel at 120 Hz refresh (FLM frequency) in simultaneous operation with a CRT, running at 90 Hz (FLM) may allow additional mode support for panel-only operation. The corresponding CRT refresh rate would be 45 Hz, almost certainly too slow for acceptable CRT display quality, but 90 Hz panel refresh rate may still be adequate for acceptable panel display quality. Reducing the overall blanking factor from 1.37 to around 1.04 can significantly reduce memory bandwidth usage, and allow the panel to operate with reduced blanking times. 120 Hz panel refresh (60 Hz CRT equivalent) with 1.37 combined blanking requires a pixel rate of 25.175 Mpps for 640 x 480 resolution. With 1.04 blanking instead of 1.37, the pixel rate could be reduced to 19.1 Mpps, or about 76% of the bandwidth needed for 1.37, without reducing the frame refresh rate.

8.0 Video Capture and Playback

Video capture and playback operate as follows:

- Off-screen display memory stores incoming video information in a “Video Capture Buffer”. This method of sharing the main display memory is also known as a “Shared Frame Buffer.”
- The Video Capture Buffer can use double buffering to allow assembly of complete video frames before the video playback mechanism attempts to display the video information on the screen. This prevents parts of different incoming frames from appearing in the same output frame.
- Incoming video information has its own timing synchronization, completely independent from the graphics engine that is controlling the display screen.
- Typically, “color keying” specifies where on the screen the video overlay information should appear. One or more colors are designated as the “key”, and a window containing the “key” color is created using the normal Windows mechanisms. Under control of the software driver, the 65550/65554 creates a separate window overlaying the video playback information. With color keying enabled, video playback information appears wherever the playback window and color key window overlap, and video playback information does not appear anywhere else on the screen. The video overlay driver aligns the playback window with the color key window. If a popup or part of another graphics window overlaps part or all of the color key window, the video playback information is automatically suppressed in the overlap area since the color key is no longer visible.
- Video information can be scaled down during capture to occupy only the amount of display memory actually needed to support the desired playback window resolution. Video information can also be enlarged (“zoomed”) on playback to fill a larger window area without requiring a larger capture buffer or higher capture resolution. When enlarging (zooming) the video overlay image, vertical interpolation can be used to improve the quality of the zooming. Vertical interpolation is a programmable option.
- Video capture information typically consists of 16 bits per pixel, encoded in YUV 4:2:2 format, with 320 x 240 total resolution (NTSC). The effective pixel rate is approximately 6.2 Mpps. The 65550 can also accept 640 x 480 resolution for video capture, but the 65550 normally will be programmed to compress this to 320 x 240 before storing the information into the video capture buffer. Video information is stored exactly as received (i.e., YUV 4:2:2.). Conversion to RGB occurs when the video information is subsequently read out of the capture buffer for display on the screen.
- The 6.2 Mpps pixel rate for video capture is based on compressing an incoming 640-pixel line to 320 pixels. The incoming uncompressed pixel rate is typically 12.2727MHz, but only one pixel is captured in the buffer for every two pixels received. With conservative round off, the effective capture rate is 6.2 Mpps.
- The full color range of YUV 4:2:2 is available on playback, regardl ess of the graphics color depth. Although YUV 4:2:2 requires only 16 bpp, it provides color depth equivalent to approximately 22 or 24 bpp RGB. If the display device is capable of 24 bpp RGB color depth, the full color depth will be utilized in the video playback window even if the rest of the screen is operating in a graphics color depth of 16 bpp or 8 bpp or less. Since VGA CRT monitors use an analog RGB interface, the full 24-bit RGB color depth is available in the RGB signals generated by the 65550 and 65554 for video playback, and will appear on the monitor if the monitor is capable of displaying that many colors.
- The video capture buffer requires 150KB (320 x 240 x 2 ÷ 1024) of off-screen display memory. Double buffering requires of 300KB of memory.
- If enabled, the vertical interpolation mentioned above requires an entire video overlay line to be read out of the video capture buffer and stored in an on-chip FIFO during the horizontal blanking interval. This is necessary to average the new line with the previous line before attempting to display the newly computed line. If a complete video overlay line is not obtained before the end of horizontal blanking, the FIFO fill process continues during the horizontal active interval. The video overlay image does not become corrupted as long as the FIFO is completely filled before the start of video overlay display. If vertical interpolation is disabled, the FIFO need not be completely filled before the start of video overlay display.

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Title: HiQVideo™ Series Mode Support
(Including Video Capture/Playback)

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