

FEATURES

- Single-chip PCMCIA host adapter
- Direct connection to PCI bus
- Direct connection of two PCMCIA sockets
- Compliant with PCI 2.0
- Compliant with PCMCIA 2.1 and JEIDA 4.1
- 82365SL-compatible register set, ExCA™-compatible
- Automatic Low-power Dynamic mode for lowest power consumption
- Programmable Suspend mode
- Five programmable memory windows per socket
- Two programmable I/O windows per socket
- Programmable card access cycle timing
- 8- or 16-bit PCMCIA card support
- ATA disk interface support
- Automatic flash memory timing support
- 3.3V, 5V, or mixed 3.3/5V operation
- Supports PCMCIA low-voltage card specification
- Multiple CL-PD6729s can be used on the PCI bus without external hardware
- 208-pin PQFP

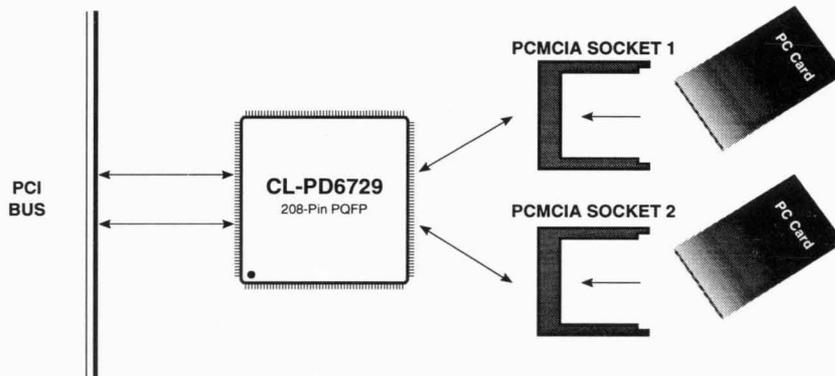
PCI-to-PCMCIA Host Adapter

OVERVIEW

The CL-PD6729 is a single-chip PCMCIA host adapter solution capable of controlling two fully independent PCMCIA sockets. The chip is fully PCMCIA-2.1 and JEIDA-4.1 compliant and is optimized for use in notebook and handheld computers where reduced form factor and low power consumption are critical design objectives. With the CL-PD6729, a complete dual-socket PCMCIA solution with power-control logic can occupy less than 2 square inches (excluding connectors).

The CL-PD6729 chip employs energy-efficient, mixed-voltage technology that can reduce system power consumption by over 50 percent. The chip also provides a Suspend mode, which stops the internal clock, and an automatic Low-power Dynamic mode, which stops transactions on the PCMCIA bus, stops internal clock distribution, and turns off much of the internal circuitry. *(cont.)*

System Block Diagram



OVERVIEW (cont.)

PC applications typically access PCMCIA cards through the socket/card-services software interface. To assure full compatibility with existing socket/card-services software and PC-card applications, the register set in the CL-PD6729 is a superset of the Intel® 82365SL register set.

The chip provides fully buffered PCMCIA interfaces, meaning that no external logic is required for buffering signals to/from the interface, and power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

Notebook Computer Design Priorities

- Small Form Factor
- Minimum Power Consumption
- High Performance
- Compatibility

Supporting Features

- Single-chip solution
- No external buffers for host or socket interfacing
- Efficient board layout
- Automatic Low-power Dynamic mode
- Suspend mode
- Mixed-voltage operation
- Write FIFO
- Programmable timing supports more cards, faster reads and writes
- Compliant with PCMCIA 2.1 and JEIDA 4.1
- Compliant with PCI 2.0
- 82365SL A-step register-compatible, ExCA™-compatible

Host Adapter Form Factor

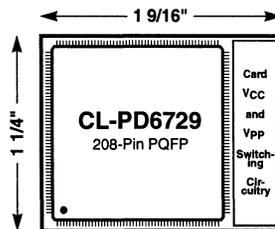


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1. GENERAL CONVENTIONS

The following general conventions apply to this document.

Bits within words and words within various memory spaces are generally numbered with a 0 (zero) as the least-significant bit or word. For example, the least-significant bit of a byte is bit 0, while the most-significant bit is bit 7.

In addition, number ranges for bit fields and words are presented with the most-significant value first. Thus, when discussing a bit field within a register, the bit number of the most-significant bit is written first, followed by a hyphen (-) and then the bit number of the least-significant bit; as in, bits 7-0.

In this document, the names of the CL-PD6729 internal registers are bold-faced. For example, **Chip Revision** and **Power Control** are register names. The names of bit fields are written with initial upper-case letters. For example, Card Power On and Battery Voltage Detect are bit field names.

Numbers and Units

The unit *Kbyte* designates 1024 bytes (2^{10}). The unit *Mbyte* designates 1,048,576 bytes (2^{20}). The unit *Gbyte* designates 1,073,741,824 bytes (2^{30}). The unit *Hz* designates hertz. The unit *KHz* designates 1000 hertz. The unit *MHz* designates 1,000,000 Hz. The unit *ms* designates millisecond. The unit μ s designates microsecond. The unit *ns* designates nanosecond. The unit *mA* designates milliampere. The unit *V* immediately following a number designates volt.

Hexadecimal numbers are presented with all letters in uppercase and a lowercase *h* appended. For example, *14h* and *03CAh* are hexadecimal numbers.

Binary numbers have the letter *b* appended to them or are enclosed in single quotation marks. For example, *11b* and '11' are binary numbers.

Numbers not indicated by an *h* or *b* are decimal.

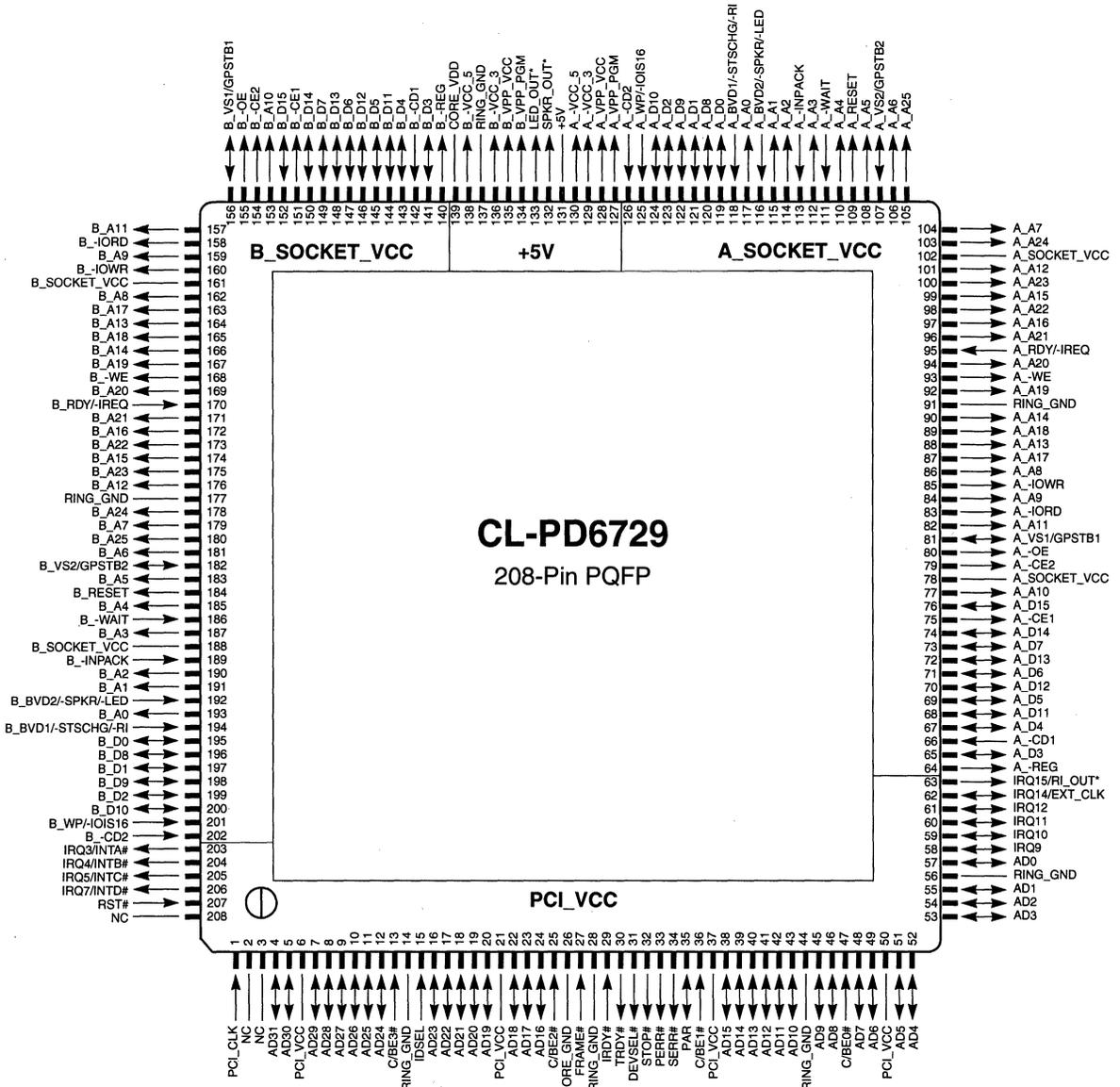
In addition, a capital letter *X* is used within numbers to indicate digits ignored by the CL-PD6729 within the current context. For example, *101XX01b* is a binary number with bits 3-2 ignored.

2. PIN INFORMATION

The CL-PD6729 device is packaged in a 208-pin plastic quad flat pack (PQFP) component package. The interface pins can be divided into four groups:

- PCI bus interface pins
- PCMCIA socket interface pins (two sets)
- Power control and general interface pins
- Power, ground, and no-connect pins

Refer to Figure 2-1 for the CL-PD6729 pin diagram. The pin assignments for the groups of interface pins are shown in Table 2-1 through Table 2-4.

2.1 Pin Diagram

Figure 2-1. CL-PD6729 Pin Diagram

2.2 Pin Description Conventions

The following conventions apply to the pin description tables in Section 2.3:

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PCMCIA bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6729.
- Pins marked with a dagger (†) in the pin description tables can be switched between CMOS and TTL input levels when CORE_VDD is powered at 5 volts. All other pins use CMOS input levels when CORE_VDD is powered at 5 volts and TTL input levels when powered at 3.3 volts.
- A pin name ending in bracketed digits separated by a colon [n:n] indicates a multi-pin bus.
- The pin number (Pin Number) column indicates the package pin that carries the listed signal. Note that multi-pin buses are listed with the first pin number corresponding to the most-significant bit of the bus. For example, pin numbers 4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-55, and 57 associated with PCI Bus Address Input and Data Input/Output pins AD[31:0] indicate that:
 - AD[31] is pin 4
 - AD[1] is pin 55
 - AD[0] is pin 57
- The quantity (Qty.) column indicates the number of pins used (per socket where applicable).
- The I/O-type code (I/O) column indicates the input and output configurations of the pins on the CL-PD6729. The possible types are defined below.
- The power-type code (Pwr.) column indicates the output drive power source for an output pin or the pull-up power source for an input pin on the CL-PD6729. The possible types are defined below.

I/O Type	Description
I	Input pin
I-PU	Input pin with an internal pull-up resistor
O	Constant-driven, output pin
I/O	Input/output pin
OD	Open-drain output pin
TO	Three-state output pin
TO-PU	Three-state output pin with internal pull-up resistor
PW	Power or ground pin

Power Type	Output or Pull-up Power Source
1	+5V: powered from a 5-volt power supply (in most systems, see description of +5V pin in Table 2-4)
2	A_SOCKET_VCC: powered from the Socket A V _{CC} supply connecting to PCMCIA pins 17 and 51 of Socket A
3	B_SOCKET_VCC: powered from the Socket B V _{CC} supply connecting to PCMCIA pins 17 and 51 of Socket B
4	PCI_VCC: powered from the PCI bus power supply
5	CORE_VDD: powered from the lowest available logic supply, which in most systems is 3.3 volts

NOTE: All pin inputs are referenced to CORE_VDD, independently of their output supply voltage.

- The drive-type (Drive) column describes the output drive-type of the pin (see DC specifications in Chapter 13 for more information). Note that the drive type listed for an input-only (I) pin is not applicable (-).

2.3 Pin Descriptions

Table 2-1. PCI Bus Interface Pins

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
AD[31:0]	PCI Bus Address Inputs / Data Input/Outputs: These pins connect to PCI bus signals AD[31:0].	4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-55, 57	32	I/O	4	PCI Spec.
C/BE[3:0]#	PCI Bus Command / Byte Enables: The command signalling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	13, 25, 36, 47	4	I	-	-
FRAME#	Cycle Frame: This input indicates to the CL-PD6729 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is at its final phase.	27	1	I	-	-
IRDY#	Initiator Ready: This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	1	I	-	-
TRDY#	Target Ready: This output indicates the CL-PD6729's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.	30	1	TO	4	PCI Spec.
STOP#	Stop: This output indicates the current target is requesting the master to stop the current transaction.	32	1	TO	4	PCI Spec.
IDSEL	Initialization Device Select: This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. The CL-PD6729 must be connected to its own unique IDSEL line (from the PCI bus arbiter or one of the high-order AD bus pins).	15	1	I	-	-
DEVSEL#	Device Select: The CL-PD6729 drives this output active (low) when it has decoded the PCI address as one that it is programmed to support, thereby acting as the target for the current PCI cycle.	31	1	TO	4	PCI Spec.
PERR#	Parity Error: The CL-PD6729 drives this output active (low) if it detects a data parity error during a write phase.	33	1	TO	4	PCI Spec.
SERR#	System Error: This output is pulsed by the CL-PD6729 to indicate an address parity error.	34	1	OD	4	PCI Spec.

Table 2-1. PCI Bus Interface Pins (cont.)

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
PAR	Parity: This pin is sampled the clock cycle after completion of each corresponding address or write data phase. For read operations this pin is driven from the cycle after TRDY# is asserted until the cycle after completion of each data phase. It ensures even parity across AD[31:0] and C/BE[3:0]#.	35	1	I/O	4	PCI Spec.
PCI_CLK	PCI Clock: This input provides timing for all transactions on the PCI bus to and from the CL-PD6729. All PCI bus interface signals described in this table (Table 2-1), except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of PCI_CLK; and all CL-PD6729 PCI bus interface timing parameters are defined with respect to this edge. This input can be operated at frequencies from 0 to 33 MHz. Note that the PCMCIA socket interface cannot operate at more than 25 MHz; a Timer Clock Divide bit is provided (Misc Control 2 register bit 4).	1	1	I	-	-
RST#	Device Reset: This input is used to initialize all registers and internal logic to their reset states and place most CL-PD6729 pins in a high-impedance state.	207	1	I	-	-
IRQ15/ RI_OUT*	Interrupt Request 15 / Ring Indicate Out: This output can be used either as an interrupt output (usually the system's IRQ15 interrupt line), or if Misc Control 2 register bit 7 is a '1', as a ring indicate output from a socket's BVD1/-STSCHG/-RI input.	63	1	TO	4	2 mA
IRQ14/ EXT_CLK	Interrupt Request 14 / External Clock: This pin can be used either as an interrupt output (usually the system's IRQ14 interrupt line), or if Misc Control 2 register bit 0 is a '1', as an alternate external clock input that will provide the internal clock to the CL-PD6729 for PCMCIA cycle timing when the PCI bus is not active.	62	1	I/O	4	2 mA
IRQ[12:9]	Interrupt Request: These outputs indicate programmable interrupt requests generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect these pins to the corresponding signal name in the system. These pins are also used as a 4-bit-wide data bus for general-purpose external I/O logic. They are used with the VS1/GPSTB1 and VS2/GPSTB2 pins to carry 8 bits of data to/from External Data register at index 2Fh, extended index 0Ah.	61-58	4	I/O	4	2 mA

Table 2-1. PCI Bus Interface Pins (cont.)

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
IRQ3/INTA#	Interrupt Request 3 / PCI Bus Interrupt A: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ3 signal or to the PCI bus INTA# signal.	203	1	TO	4	PCI Spec.
IRQ4/INTB#	Interrupt Request 4 / PCI Bus Interrupt B: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ4 signal or to the PCI bus INTB# signal.	204	1	TO	4	PCI Spec.
IRQ5/INTC#	Interrupt Request 5 / PCI Bus Interrupt C: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ5 signal or to the PCI bus INTC# signal.	205	1	TO	4	PCI Spec.
IRQ7/INTD#	Interrupt Request 7 / PCI Bus Interrupt D: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ7 signal or to the PCI bus INTD# signal.	206	1	TO	4	PCI Spec.
PCI_VCC	PCI Bus V_{CC}: These pins can be connected to either a 3.3- or 5-volt power supply. The PCI bus interface pin outputs listed in this table (Table 2-1) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6729 pin groups.	6, 21, 37, 50	4	PW	—	—

Table 2-2. Socket Interface Pins

Pin Name ¹	Description ²	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
-REG	Register Access: In Memory Card Interface mode, this output chooses between attribute and common memory. In I/O Card Interface mode, this signal is active (low). In ATA mode this signal is always high.	64	140	1	TO	2 or 3	2 mA
A[25:0]	PCMCIA socket address outputs.	105, 103, 100, 98, 96, 94, 92, 89, 87, 97, 99, 90, 88, 101, 82, 77, 84, 86, 104, 106, 108, 110, 112, 114, 115, 117	180, 178, 175, 173, 171, 169, 167, 165, 163, 172, 174, 166, 164, 176, 157, 153, 159, 162, 179, 181, 183, 185, 187, 190, 191, 193	26	TO	2 or 3	2 mA
D[15:0] †	PCMCIA socket data I/O pins.	76, 74, 72, 70, 68, 124, 122, 120, 73, 71, 69, 67, 65, 123, 121, 119	152, 150, 148, 146, 144, 200, 198, 196, 149, 147, 145, 143, 141, 199, 197, 195	16	I/O	2 or 3	2 mA
-OE	Output Enable: This output goes active (low) to indicate a memory read from the PCMCIA socket to the CL-PD6729.	80	155	1	TO	2 or 3	2 mA
-WE	Write Enable: This output goes active (low) to indicate a memory write from the CL-PD6729 to the PCMCIA socket.	93	168	1	TO	2 or 3	2 mA
-IORD	I/O Read: This output goes active (low) for I/O reads from the socket to the CL-PD6729.	83	158	1	TO	2 or 3	2 mA
-IOWR	I/O Write: This output goes active (low) for I/O writes from the CL-PD6729 to the socket.	85	160	1	TO	2 or 3	2 mA
WP-/IOIS16 †	Write Protect / I/O Is 16-Bit: In Memory Card Interface mode, this input is interpreted as the status of the write protect switch on the PCMCIA card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PCMCIA card.	125	201	1	I	-	-

¹ To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

² When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

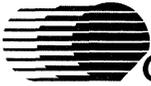


Table 2-2. Socket Interface Pins (cont.)

Pin Name ¹	Description ²	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
-INPACK †	Input Acknowledge: The -INPACK function is not applicable in PCI bus environments. However, for compatibility with other Cirrus Logic products, this pin should be connected to the PCMCIA socket's -INPACK pin.	113	189	1	I-PU	2 or 3	-
RDY/-IREQ †	Ready / Interrupt Request: In Memory Card Interface mode, this input indicates to the CL-PD6729 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request.	95	170	1	I-PU	2 or 3	-
-WAIT †	Wait: This input indicates a request by the card to the CL-PD6729 to halt the cycle in progress until this signal is deactivated.	111	186	1	I-PU	2 or 3	-
-CD[2:1]	Card Detect: These inputs indicate to the CL-PD6729 the presence of a card in the socket. They are internally pulled high to the voltage of the +5V power pin.	126, 66	202, 142	2	I-PU	1	-
-CE[2:1]	Card Enable: These outputs are driven low by the CL-PD6729 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes.	79, 75	154, 151	2	TO	2 or 3	2 mA
RESET	Card Reset: This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled.	109	184	1	TO	2 or 3	2 mA
BVD2/-SPKR/ -LED †	Battery Voltage Detect 2 / Speaker / LED: In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input.	116	192	1	I-PU	2 or 3	-

¹ To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

² When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

Table 2–2. Socket Interface Pins (cont.)

Pin Name ¹	Description ²	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
BVD1/ -STSCHG/-RI †	Battery Voltage Detect 1 / Status Change / Ring Indicate: In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the CL-PD6729 that the card's internal status has changed. If bit 7 of the Interrupt and General Control register is set to a '1', this pin serves as the ring indicate input for wakeup-on-ring system power management support.	118	194	1	I-PU	2 or 3	–
VS2/GPSTB2	Voltage Sense 2 / General-Purpose Strobe 2: This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin connects to PCMCIA socket pin 57. This pin can also be used as a general-purpose strobe to control read and write capabilities of IRQ[12:9] when they are used as general-purpose I/O. See Section 3.1.10 for more information.	107	182	1	I/O	1	2 mA
VS1/GPSTB1	Voltage Sense 1 / General-Purpose Strobe 1: This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin connects to PCMCIA socket pin 43. This pin can also be used as a general-purpose strobe to control read and write capabilities of IRQ[12:9] when they are used as general-purpose I/O. See Section 3.1.10 for more information.	81	156	1	I/O	1	2 mA
SOCKET_VCC	This pin can be connected to either a 3.3- or 5-volt power supply. The socket interface outputs (listed in this table, Table 2–2) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6729 pin groups. Connect these pins to the V _{CC} supply of the socket (pins 17 and 51 of the respective PCMCIA socket).	78, 102	161, 188	2	PW	–	–

¹ To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

² When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

Table 2-3. Power Control and General Interface Pins

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
VPP_VCC	This active-high output controls the socket V _{CC} supply to the socket's V _{PP1} and V _{PP2} pins. The active-high level of this output is mutually exclusive with that of VPP_PGM.	128	135	1	O	1	12 mA
VPP_PGM	This active-high output controls the programming voltage supply to the socket's V _{PP1} and V _{PP2} pins. The active-high level of this output is mutually exclusive with that of VPP_VCC.	127	134	1	O	1	12 mA
-VCC_3	This active-low output controls the 3.3-volt supply to the socket's V _{CC} pins. The active-low level of this output is mutually exclusive with that of -VCC_5.	129	136	1	O	1	12 mA
-VCC_5	This active-low output controls the 5-volt supply to the socket's V _{CC} pins. The active-low level of this output is mutually exclusive with that of -VCC_3.	130	138	1	O	1	12 mA
SPKR_OUT*	Speaker Output: This output can be used as a digital output to a speaker to allow a system to support PCMCIA card fax/modem/voice and audio sound output. This output is enabled by setting the socket's Misc Control 1 register bit 4 to a '1' (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-LED to this pin).	132		1	TO-PU	4	12 mA
LED_OUT*	LED Output: This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. The Extension Control 1 register bit 2 must be set to a '1' to enable this output (to reflect any activity on BVD2/-SPKR/-LED), and a socket's ATA Control register bit 1 must be set to a '1' to allow the level of the BVD2/-SPKR/-LED pin to reflect disk activity.	133		1	O	4	12 mA

Table 2-4. Power, Ground, and No-Connect Pins

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
+5V	This pin is connected to the system's 5-volt power supply, unless 5 volts is not available. In systems where 5 volts is not available, this pin is connected to the system's 3.3-volt supply.	131	1	PW	-	-
CORE_VDD	This pin provides power to the core circuitry of the CL-PD6729. It can be connected to either a 3.3- or 5-volt power supply, independent of the operating voltage of other interfaces. For power conservation on a system with a 3.3-volt supply available, this pin should be connected to the 3.3-volt supply even if there is no intention of operating other interfaces on the device at less than 5 volts.	139	1	PW	-	-
CORE_GND	All CL-PD6729 ground lines should be connected to system ground.	26	1	PW	-	-
RING_GND	All CL-PD6729 ground lines should be connected to system ground.	14, 28, 44, 56, 91, 137, 177	7	PW	-	-
NC	These pins are Reserved for future expansion and can be left unconnected. Pin 2 is an output, and pins 3 and 208 are inputs.	2, 3, 208	3	-	-	-

Table 2-5. Pin Usage Summary

Pin Group	Pin Quantity
PCI bus interface pins	63
Socket interface pins	122
Power control and general interface pins	10
Power, ground, and no-connect pins	13
Total:	208

3. INTRODUCTION TO THE CL-PD6729

3.1 System Architecture

This section describes PCMCIA basics, windowing, socket power management features, interrupts, device power management, write FIFO usage, bus sizing, programmable PCMCIA timing, and ATA mode operation.

3.1.1 PCMCIA Basics

PCMCIA is an abbreviation for Personal Computer Memory Card International Association. PCMCIA 2.1¹ is a standard for using memory and I/O devices as insertable, exchangeable peripherals for PCs (personal computers) and handheld computers.

For simpler end-user and vendor implementation of the standard, systems employing PCMCIA 2.1 should also be backward-compatible with industry-standard PC addressing.

For PCMCIA memory-type cards, the memory information must be mapped into the system memory address space. This is accomplished with a 'windowing' technique that is similar to expanded memory schemes already used in PC systems (for example, LIM 4.0 memory manager).

PCMCIA cards can have *attribute* and *common* memory. Attribute memory is used to indicate to host software the capabilities of the PCMCIA card, and it allows host software to change the configuration of the card. Common memory can be used by host software for any purpose (such as flash file system, system memory, and floppy emulation).

PCMCIA I/O-type cards, such as modems, should also be directly addressable, as if the cards were I/O devices plugged into the PCI bus. For example, it would be highly desirable to have a PCMCIA modem accessible to standard communications software as if it were at a COM port. For COM1, this would require that the modem be accessed at system I/O address 3F8h–3FFh. The method of mapping a PCMCIA I/O address into anticipated areas of PCI I/O space is done similarly to memory windowing.

PCMCIA I/O-type cards usually have interrupts that need to be serviced by host software. For the example of a modem card accessed as if at COM1, software would expect the modem to generate interrupts on the IRQ4 line. To be sure all interrupts are routed as expected, the CL-PD6729 can steer the interrupt from the PCMCIA card to one of the four PCI-bus-defined interrupts or to one of several standard PC interrupts (see Section 3.1.3 and the **Interrupt and General Control** register).

3.1.2 CL-PD6729 Windowing Capabilities

For full compatibility with existing software, and to ensure compatibility with future memory cards and software, the CL-PD6729 provides five programmable memory windows per socket and two programmable I/O windows per socket. These windows can be used by an inserted PCMCIA card to access PCI memory and I/O space.

Having five memory windows per socket allows a memory-type card to be accessed through four memory windows programmed for common memory access, (allowing PC-type expanded-memory-style management), leaving the fifth memory window available to be programmed to access the card's attribute memory without disrupting the common memory in use.

¹ The CL-PD6729 is backward-compatible with PCMCIA standards 1.0, 2.0, and 2.01. The CL-PD6729 is also compatible with JEIDA 4.1 and its earlier standards corresponding with the PCMCIA standards above.

Each memory window has several programming options, including:

Memory Window Option	Description
Enable	Each of the five memory windows can be individually enabled. Disabled windows are not responded to.
Start Address	This is the start address of the memory window within the selected 16-Mbyte page of PCI memory. The start address can be programmed to reside on any 4-Kbyte boundary within the programmed page of PCI memory.
End Address	This is the end address of the memory window within the selected 16-Mbyte page of PCI memory. The end address can be programmed to reside on any 4-Kbyte boundary within the programmed page of PCI memory. Only memory accesses between the start and end address are responded to.
Offset Address	The offset address is added to the PCI address to determine the address for accessing the PCMCIA card. This allows the addresses in the PCMCIA address space to be different from the PCI address space.
Upper Address	The upper memory address specifies a 16-Mbyte page of PCI memory.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.
Register Access Setting	The -REG pin can be enabled on a per-window basis so that any of the windows can be used for accessing attribute memory.
Write Protect	If the window is programmed to be write-protected, then writes to the memory window are ignored (reads are still performed normally).

Each I/O window also has several programming options, including:

I/O Window Option	Description
Enable	Each of the two I/O windows can be individually enabled.
Start Address	The start address of the window is programmable on single-byte boundaries from 0 to 64 Kbytes.
End Address	The end address of the window is also programmable on single-byte boundaries from 0 to 64 Kbytes.
Offset Address	The offset address is added to the PCI address to determine the address for accessing the PCMCIA card.
Auto Size	The size of accesses can be set automatically, based on the PCMCIA -IOIS16 signal.
Data Size	The size of accesses can be set manually to either 8 or 16 bits, overriding the Auto Size option.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.

CAUTION: The windows of the CL-PD6729 should never be allowed to overlap with each other or the other devices in the system. This would cause signal collisions, resulting in erratic behavior.

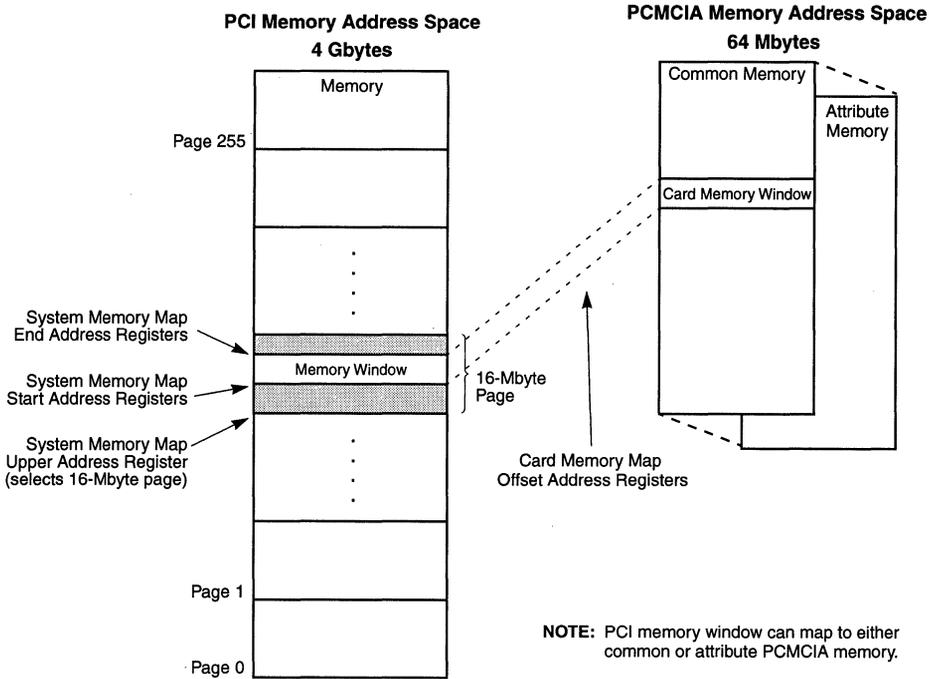


Figure 3-1. Memory Window Organization

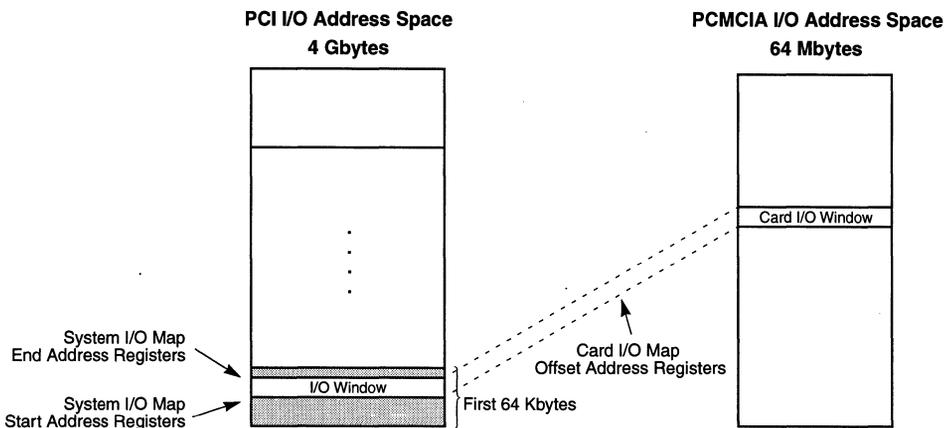


Figure 3-2. I/O Window Organization

3.1.3 Interrupts

In a PC-compatible system with a PCI bus, there usually are two types of interrupts in use:

- Four PCI-defined, active-low, open-drain, shared interrupt lines INTA# through INTD#
- A number of ISA-architecture-defined, active-high, totem-pole IRQ output interrupts

The CL-PD6729 provides ten interrupt pins that are individually programmable to work as either PCI-type 'INT#' open-drain interrupts or ISA-type 'IRQ' totem-pole output interrupts. Bits 3 and 4 of the **Extension Control 1** register select PCI-bus or ISA-architecture-compatible interrupt programming.

The CL-PD6729 interrupt pins are labeled with names suggesting their mapping in a PCI-bus-based, ISA-architecture-compatible system, though there are no hard requirements specifying the exact mapping. Typically, all ten interrupt pins should be connected to system interrupt signals to allow maximum flexibility in programming interrupt routing from the CL-PD6729.

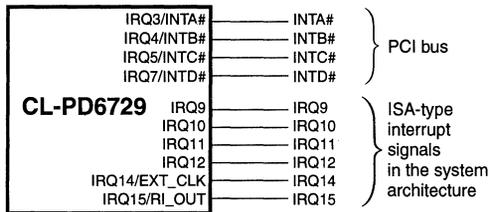


Figure 3–3. A Common Mapping of CL-PD6729 Interrupt Pins to System Interrupt Signals

3.1.3.1 Classes of Interrupts

The CL-PD6729 supports two classes of interrupts:

- Socket or card interrupts initiated by the PCMCIA card activating its RDY/-IREQ signal
- Management interrupts triggered by changes in PCMCIA card status

There are four card-status-change conditions that can be programmed to cause management interrupts:

- Card insertion or removal
- Battery warning indicator (BVD2) change on a memory-type card
- Battery dead indicator (BVD1) or I/O-type card status change (STSCHG)
- Ready (RDY) status change on a memory-type card

Either class of interrupts can be routed to any of the ten interrupt pins on the CL-PD6729.

3.1.3.2 Connection of Interrupt Pins Programmed as PCI-Bus INT# Signals

Pins programmed as INT#-type interrupts can be connected to the correspondingly named signals on the PCI bus.

If the management interrupt is being routed to a pin connected to a PCI-bus INT# signal, bit 4 of the **Extension Control 1** register should be set to a '1'. If the card interrupt is being routed to a pin connected to a PCI-bus INT# signal, bit 3 of the **Extension Control 1** register should be set to a '1'.

Although four of the ten CL-PD6729 interrupt pins are labeled as INTA# through INTD#, any of the ten interrupt pins can be used as PCI-type INT# signals.

3.1.3.3 Connection of Interrupt Pins Programmed as ISA-Architecture-Compatible IRQ Signals

IRQ-type interrupts in PC-compatible systems are not generally shared by hardware. Therefore, each device in the system using IRQ-type interrupts must have a unique interrupt line. Additionally, many software applications assume that certain I/O devices use specific IRQ signals. To allow PCMCIA cards with differing I/O functionalities to be connected to appropriate non-conflicting IRQ locations, the CL-PD6729 can steer the interrupt signal from a PCMCIA card to any one of the ten different hardware interrupt lines.

For some I/O-type cards, software is written so that IRQ interrupts can be shared. The CL-PD6729 contains unique logic that allows IRQ-type interrupts to be shared under software control. This is accomplished by programming the CL-PD6729 to alternately pulse and then three-state the desired interrupt pin, which has been programmed as an IRQ-type output. This unique IRQ interrupt sharing technique can be controlled through software so that systems incapable of IRQ sharing have no loss of functionality.

3.1.3.4 Alternate Functions of Interrupt Pins

The CL-PD6729 has two dual-function interrupt pins: IRQ14/EXT_CLK and IRQ15/RI_OUT*. In their default modes, these pins indicate interrupt requests IRQ14 and IRQ15.

IRQ14/EXT_CLK can alternately be configured as an external clock input (EXT_CLK). When configured in External Clock mode by programming **Misc Control 2** register bit 0 to a '1', IRQ14/EXT_CLK acts as a clock input, bringing in an external clock that drives the CL-PD6729 circuitry whenever the PCI bus is inactive.

Similarly, IRQ15/RI_OUT* can alternately be configured to function as a ring indicator output (RI_OUT*) to an 80360-type chip set's -RI input. When configured in Ring Indicate mode by programming **Misc Control 2** register bit 7 to a '1', outputs from a PCMCIA I/O card's -STSCHG pin¹ are passed through to the IRQ15/RI_OUT* pin of the CL-PD6729.

¹ **Interrupt and General Control** register bits 5 and 7 must be set to '1's for a socket interface to accept an -RI input.

3.1.4 CL-PD6729 Power Management

To provide the longest possible battery life, the CL-PD6729 provides many power management features, including Low-power Dynamic mode, Suspend mode, and control of PCMCIA socket power.

Low-power Dynamic mode is transparent to the PCI bus. After reset, the CL-PD6729 is configured for Low-power Dynamic mode. This mode can be turned off by setting **Misc Control 2** register, bit 1 to a '0'. When in Low-power Dynamic mode, periods of inactivity (no activity on the PCMCIA bus and system accesses to chip registers or inserted cards are no longer being performed) cause the CL-PD6729 to enter a low-power state where the clock is turned off to most of the chip and the PCMCIA address and data lines are set to a static value. V_{CC} and V_{PP} power to the card is left unchanged. When there is activity present on the PCMCIA bus, or the system accesses CL-PD6729 registers, or PCMCIA cards are inserted or removed from the socket, the CL-PD6729 enters its active state, services the transaction, and then returns to its low-power state.

A Suspend mode can also be programmed. The CL-PD6729 Suspend mode is the chip's lowest power mode. The CL-PD6729 is put into Suspend mode by setting the **Misc Control 2** register, bit 2 to a '1'. In Suspend mode, all the internal clocks are turned off, and only read/write access to the PCI-Configuration registers, read/write access of the **Index** register, and write access to the **Misc Control 2** register is supported. All accesses to the PCMCIA cards are ignored when in Suspend mode. V_{CC} and V_{PP} power to the card is left unchanged (the system power management software is responsible for turning off power to the socket and entering Suspend mode). Interrupts are passed through to the processor when in Suspend mode. To exit Suspend mode, the **Misc Control 2** register bit 2 must be reset to a '0'.

The CL-PD6729 power can be further managed by controlling socket power as outlined in Section 3.1.5. Socket power can be turned on and off through software or automatically when cards are inserted or removed. The CL-PD6729 provides six pins per socket for controlling external logic to switch V_{CC} and V_{PP} voltages on and off and for sensing a card's operating voltage range. Cards can be turned off when they are not in use.

Table 3–1. CL-PD6729 Power-Management Modes

Mode Name	RST# Level	Misc Control 2 Register		Functionality	Typical Power Consumption (PCI_VCC = 5.0V, CORE_VDD = 3.3V, +5V = 5.0V)
		Suspend Mode (Bit 2)	Low-Power Dynamic Mode (Bit 1)		
Low-power Dynamic (default)	High	0	1	Full functionality	tbd
Normal	High	0	0	Full functionality	tbd
Suspend (software-controlled)	High	1	–	8-bit access to Misc Control 2 register. No other register access. No card in socket(s).	tbd
Reset	Low	–	–	No register access. No card in socket(s). System bus signals disabled.	tbd

3.1.5 Socket Power Management Features

Card Removal

When a card is removed from a socket, the CL-PD6729 by default automatically disables the V_{CC} and V_{PP} supplies to the socket. If **Extension Control 1** register bit 1 is a '0', card power is prevented from being automatically disabled when a card is removed. The CL-PD6729 can also be configured to have management interrupts notify software of card removal.

Card Insertion

At reset, and whenever there is no card in a socket, power to the socket is off. When a card is detected (card detect input pins, -CD1 and -CD2, to the CL-PD6729 become asserted low), two independent actions can be programmed to occur.

If the CL-PD6729 has been set for automatic power-on (**Power Control** register bits 4 and 5 are both '1's), the CL-PD6729 automatically enables the socket V_{CC} supply (and, if so programmed, V_{PP} supply).

If the CL-PD6729 has been programmed to cause management interrupts for card-detection events,

assertion of -CD1 and -CD2 to the CL-PD6729 causes a management interrupt to be generated to inform system software that a card was inserted. In the case of manual power detection (**Power Control** register bits 5 is a '0'), system software can then determine the card's operating voltage range and then power-up the socket and initialize the card, or if programmed for automatic power-on (**Power Control** register bits 5 is a '1' and **Extension Control 1** register bit 1 is a '1'), simply initialize the card.

3.1.6 Write FIFO

To increase performance when writing to PCMCIA cards, two, independent, four-word-deep write FIFOs are used. Writes to PCMCIA cards will complete without wait states until the FIFO is full. Register states should not be changed when the write FIFO is not empty.

3.1.7 Bus Sizing

The CL-PD6729 operates in 32-bit mode. All PCI transactions are 32-bit, even when supporting 8-bit-only or 16-bit PCMCIA cards.

3.1.8 Programmable PCMCIA Timing

The Setup, Command, and Recovery time for the PCMCIA bus is programmable (see Chapter 11). The CL-PD6729 can be programmed to match the timing requirements of any PCMCIA card. There are two sets of timing registers, Timer Set 0 and Timer Set 1, that can be selected on a per-window basis for both I/O and memory windows.

By setting one of the timing sets for a Recovery time equal to flash memory programming time and utilizing the write FIFO, algorithms can be created to relieve system software of the necessity of doing timing loops, and thus allow for flash programming in the background.

3.1.9 ATA Mode Operation

The CL-PD6729 supports direct connection to AT-attached-interface hard drives. ATA drives use an interface very similar to the IDE interface found on many popular portable computers. In this mode, the address and data conflict with the floppy drive is handled automatically. See Chapter 12 for more information.

3.1.10 VS/GPSTB

The pins VS1/GPSTB1 and VS2/GBSTB2 can be used to determine the voltage capabilities of an inserted card. The status of these pins, for both

sockets, are indicated by bits 3:0 of the **External Data** register at extended index 0Ah of index 6Fh (this is true even though registers 40h-7Fh are generally for Socket B only).

The CL-PD6729 supports a general-purpose 8-bit-wide read port and a general-purpose 8-bit-wide write port. This I/O port uses the IRQ[12:9] lines from the CL-PD6729. These ports are accessible by programming bits 3 or 4 in the **Extended Control 2** register at extended index 0Bh. This enables the VS1/GPSTB1 and VS2/GPSTB2 to be used as controls for the ports, allowing side-band signals to the PCMCIA sockets. The **External Data** register at extended index 0Ah of index 2Fh holds the data. Refer to application note AN-PD4 for more information.

3.2 Host Access to Registers

The CL-PD6729 registers are accessed through an 8-bit indexing mechanism. An index register scheme allows a large number of internal registers to be accessed by the CPU using only two I/O addresses.

The **Index** register (see Chapter 6) is used to specify which of the internal registers the CPU will access next. The value in the **Index** register is called the Register Index and is the number that specifies a unique internal register. The **Data** register is used by the CPU to read and write the internal register specified by the **Index** register.

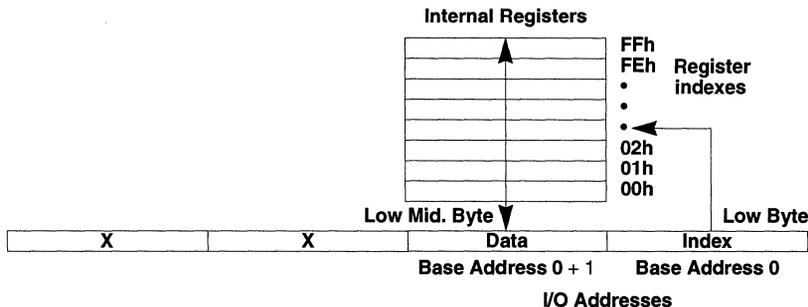


Figure 3-4. Indexed 8-Bit Register Structure

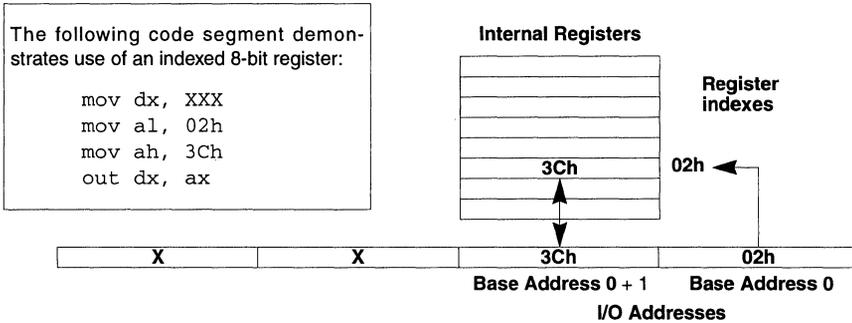


Figure 3-5. Indexed 8-Bit Register Example

The CL-PD6729 has Extension registers that add to the functionality of the 82365SL-compatible register set. Within the Extension registers is an **Extended Index** register and **Extended Data** register that provide access to more registers. The registers accessed through **Extended Index** and **Extended Data** are thus double indexed. The example below shows how to access the **Extension Control 1** register, one of the double-indexed registers.

```

;Write to Extension Control 1 register example
;Constants section
Extended_Index    EQU 2Eh
Index_Reg         EQU 2Fh
Ext_Cntrl_1      EQU 03h
Base_IO_Address   EQU XXX
;The base I/O address for the CL-PD6729
;should be obtained through PCI BIOS.
;Code section
mov dx, Base_IO_Address
mov al, Extended_Index
mov ah, Ext_Cntrl_1
out dx, ax
        
```

```

mov al, Index_Reg
mov ah, user_data ;Desired data to be
out dx, ax        ;written to
                  ;extended index 3
        
```

;Read from Extension Control 1 register example

```

;Code section
mov dx, Base_IO_Address
mov al, Extended_Index
mov ah, Ext_Cntrl_1
out dx, ax
mov al, Index_Reg
out dx, al
inc dx ;al has extended
in al, dx ;index 3 data
        
```

3.3 Power-On Setup

Following RST#-activated reset, the CL-PD6729 must be configured by host initialization or BIOS software. The application of the RST# signal on power-up causes initialization of all the CL-PD6729 register bits and fields to their reset values.

4. REGISTER DESCRIPTION CONVENTIONS

Register Headings

The description of each register starts with a header containing the following information:

Header Field	Description
Register Name	This indicates the register name.
Offset	This is added to the base address to generate the total effective address. This field is for PCI-Configuration registers only.
Register Per	This indicates whether the register affects both sockets, marked <i>chip</i> , or an individual socket, marked <i>socket</i> . If <i>socket</i> is indicated, there are two registers being described, each with a separate Index value (one for each socket, A and B). ^a
Index ^a	This is the Index value through which an internal register in an indexed register set is accessed.
Register Compatibility Type	This indicates whether the register is 82365SL-compatible, marked <i>365</i> or a register extension, marked <i>ext</i> .

^a When the register is socket-specific, the Index value given in the register heading is for Socket A only. For the Socket B register, add 40h to the Index value of the Socket A register.

Special Function Bits

Following is a description of bits with special functions:

Bit Type	Description
<i>Reserved</i>	These bits are Reserved and should not be changed.
<i>Compatibility Bit</i>	These bits have no function on the CL-PD6729 but are included for compatibility with the 82365SL register set.
<i>0 or 1</i>	These read-only bits are forced to either a '0' or '1' at reset and cannot be changed.
<i>Scratchpad Bit</i>	These read/write bits are available for use as bits of memory.

Bit Naming Conventions

The following keywords are used within bit and field names:

Keyword	Description
Enable	Indicates that the function described in the rest of the bit name is active when the bit is a '1'.
Disable	Indicates that the function described in the rest of the bit name is active when the bit is a '0'.
Mode	Indicates that the function of the bit alters the interpretation of the values in other registers.
Input	Indicates a bit or field that is read from a pin.
Output	Indicates a bit or field that is driven to a pin.
Select	Indicates that the bit or field selects between multiple alternatives. Fields that contain <i>Select</i> in their names have an indirect mapping between the value of the field and the effect.
Status	Indicates one of two types of bits: either Read-only bits used by the CL-PD6729 to report information to the system or bits set by the CL-PD6729 in response to an event, and can also be cleared by the system. The system cannot directly cause a Status bit to become a '1'.
Value	Indicates that the bit or field value is used as a number.

Bit Descriptions

When used to describe an action taken by the host system, the phrase "the system *sets* a bit" is the same as stating "the system writes the appropriate register with a '1' (one) in the bit".

Similarly, the phrase "the system *resets* a bit" or "the system *clears* a bit" is the same as stating "the system writes the appropriate register with a '0' (zero) in the bit".

5. PCI-CONFIGURATION REGISTERS

These registers occupy offsets 00–3Fh. They control basic PCI bus functionality. PCMCIA Operation registers are accessed through the **Base Address 0** register. The registers in this section apply to the entire chip; they are not specific to either socket.

CAUTION: If bits indicated as read only (R:) are to be written to, they should be written to a '0'.

5.1 Vendor ID and Device ID

Configuration Register Name: Vendor ID and Device ID							
Offset: 00h							
							Register Per: chip
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Device ID (high) Device ID (high) R:00010001							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Byte 2 Device ID (low) Device ID (low) R:00000000							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Byte 1 Vendor ID (high) Vendor ID (high) R:00010000							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0 Vendor ID (low) Vendor ID (low) R:00010011							

Bits 15-0: Vendor ID

This read-only field is the vendor identification assigned to Cirrus Logic by the PCI Special Interest Group. This field always reads back 1013h.

Bits 31-16: Device ID

This read-only field is the device identification assigned to this device by Cirrus Logic. This field always reads back 1100h for the CL-PD6729. (Revision number identification for the CL-PD6729 part itself is indicated by the Revision ID field in the **Revision ID and Class Code** register at offset 08h.)

5.2 Command and Status

Configuration Register Name: Command and Status								
Offset: 04h								
Register Per: chip								
Byte 3 Status (high)	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
	Address/Data Parity Error Detected RW:0	System Error (SERR#) Generated RW:0	Reserved R:XXX			DEVSEL# Timing R:01		Master Data Parity Error Reported R:0
Byte 2 Status (low)	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
	Reserved R:XXXXXXXX							
Byte 1 Command (high)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	Reserved R:XXXXXXXX							System Error (SERR#) Enable RW:0
Byte 0 Command (low)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Wait Cycle Enable R:1	Parity Error Check/Report Enable RW:0	Reserved R:XXXX			PCI Memory Space Enable RW:0	PCI I/O Space Enable RW:0	

Bit 0: PCI I/O Space Enable

0	The I/O space for the CL-PD6729 is disabled. Any reads or writes to the I/O space will be ignored. This applies to both the I/O registers of the CL-PD6729 itself, as well as any I/O windows that might have been enabled to the PCMCIA sockets.
1	The I/O space for the CL-PD6729 is enabled and will respond to reads and writes to the I/O address range defined in Base Address 0 register as well as any I/O window addresses.

Bit 1: PCI Memory Space Enable

This bit must be set or the CL-PD6729 will not respond to memory transactions.

0	The memory space for the CL-PD6729 is disabled. Any reads or writes to the CL-PD6729 memory space will be ignored.
1	The memory space for the CL-PD6729 is enabled, allowing memory window access.

Bit 6: Parity Error Check/Report Enable

This bit enables all parity-reporting-related circuitry, except for bit 31 of this register.

0	Parity checking and reporting in the CL-PD6729 disabled.
1	Parity checking and reporting in the CL-PD6729 is enabled.

Bit 7: Wait Cycle Enable

This bit always reads a '1', indicating that the CL-PD6729 employs address stepping.

Bit 8: System Error (SERR#) Enable

This bit enables the CL-PD6729's reporting of system errors by assertion of the SERR# pin when address parity errors occur. Bit 6 must also be set to a '1' to allow detecting of conditions that allow SERR# activation. See also description of bit 30.

0	Activation of SERR# on address parity error is disabled.
1	SERR# is activated whenever an address parity error is internally detected (slave mode).

Bit 24: Master Data Parity Error Reported

This bit is Reserved and will always read a '0'.

Bits 26-25: DEVSEL# Timing

This field always reads back '01', identifying the CL-PD6729 as a medium-speed device.

Bit 30: System Error (SERR#) Generated

This bit is set whenever the CL-PD6729 asserts SERR# because of internal detection of a PCI address parity error. Bit 8 of this register must be set before system errors can be reported, and bit 6 must be set to allow address parity errors to be detected. The CL-PD6729 only asserts SERR# if address parity errors occur. No other chip or system actions will cause SERR# to be driven active.

0	SERR# was not asserted by this device.
1	SERR# was asserted by this device, indicating a PCI address parity error.

Bit 31: Address/Data Parity Error Detected

This bit indicates whether a parity error was detected, independently of whether bit 6 of this register is a '1'.

0	No data parity errors detected.
1	Address or data parity error detected.



5.3 Revision ID and Class Code

Configuration Register Name: Revision ID and Class Code							
Offset: 08h							
Register Per: chip							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Class Code (high)				Class Code (high)			
R:00000110							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Byte 2 Class Code (mid.)				Class Code (mid.)			
R:00000101							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Byte 1 Class Code (low)				Class Code (low)			
R:00000000							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0 Revision ID				Revision ID			
R:nnnnnnn ^a							

^a This read-only value depends on the revision level of the CL-PD6729.

Bits 7-0: Revision ID

This read-only field identifies the revision level of the CL-PD6729 chip.

Bits 31-8: Class Code

This field always reads back 060500h, identifying the CL-PD6729 as a PCI-to-PCMCIA bridge device.

5.4 Cache Line Size, Latency Timer, Header Type, and BIST

Configuration Register Name: Cache Line Size, Latency Timer, Header Type, and BIST								
Offset: 0Ch								
Register Per: chip								
Byte 3 BIST	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
	Reserved R:XXXXXXXX							
Byte 2 Header Type	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
	Header Type R:10000000							
Byte 1 Latency Timer	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	Reserved R:XXXXXXXX							
Byte 0 Cache Line Size	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved R:XXXXXXXX							

Bits 23-16: Header Type

This field always reads back 80h, specifying that the CL-PD6729 is a multi-function device and that it uses the standard layout for configuration bytes 10h-3Fh.

5.5 Base Address 0

Configuration Register Name: Base Address 0								Register Per: chip	
Offset: 10h									
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 16
I/O Base Address (high)									
RW:00000000									
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 8
I/O Base Address (high mid.)									
RW:00000000									
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 0
I/O Base Address (low mid.)									
RW:00000000									
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
I/O Base Address (low)						Reserved	I/O Space Indicator		
RW:000000						R:0	R:1		

This is the PCI I/O address space base address for the Operation registers.

Bit 0: I/O Space Indicator

This bit always reads back a '1', indicating that this base address register defines a PCI I/O space.

Bits 31-2: I/O Base Address

This field specifies the I/O-mapped register space of the CL-PD6729. All bits in this field are readable and writable because only the lower 2 bytes are required for Operation register access and the PCI bus's minimum I/O base address granularity is 4 bytes. The Operation registers can be accessed only after these bits are set to a non-zero value.

5.6 Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat

Configuration Register Name: Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat							
Offset: 3Ch							
Register Per: chip							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Max_Lat Max_Lat R:00000000							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Byte 2 Min_Gnt Reserved R:XXXXXXXX							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Byte 1 Interrupt Pin Interrupt Pin R:00000000							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0 Interrupt Line Interrupt Line RW:00000000							

Bits 7-0: Interrupt Line

For other than PCMCIA-controller-type PCI devices, this field indicates interrupt line routing. Although this register is read/write for PCI compatibility, no interrupt line routing is controlled by this register on the CL-PD6729. Because the CL-PD6729 must dynamically configure interrupt usage, the actual routing to the appropriate interrupt line is made by writing to interrupt-type-specific interrupt control bit settings in the Operation registers (see the **Interrupt and General Control** register).

Bits 15-8: Interrupt Pin

For other than PCMCIA-controller-type PCI devices, this read-only field indicates which interrupt pin the device uses. Because the CL-PD6729 must dynamically configure interrupt usage, the actual connection of interrupt pins is defined by interrupt control bit settings in the Operation registers (see the **Management Interrupt Configuration** register). This field always reads back 00h.

Bits 31-24: Max_Lat

This field indicates the maximum time that can occur between PCI bus accesses to the CL-PD6729 while still efficiently performing transfers to or from PCMCIA cards. The value programmed is in 250-ns increments, based on full-speed PCI_CLK operation. This field always reads back 00h, indicating that there are no major latency requirements.

6. OPERATION REGISTERS

The CL-PD6729's internal Device Control, Window Mapping, Extension, and Timing registers are accessed through a pair of Operation registers — an **Index** register and a **Data** register.

The **Index** register is accessed at the address programmed in the **Base Address 0** register, and the **Data** register (see page 35) is accessed by adding 1 to the address programmed in **Base Address 0**.

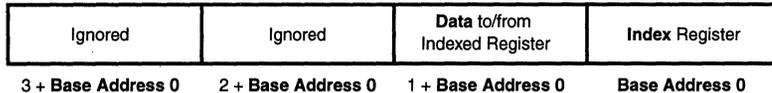


Figure 6–1. Operation Registers as PCI Double-Word I/O Space at Base Address 0 Register (programmed at offset 10h)

6.1 Index

<i>Register Name: Index</i>							<i>Register Per: chip</i>
<i>Index: n/a</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
<i>Reserved</i>	Socket Index	Register Index					
RW:0	RW:0	RW:000000					

Bits 5-0: Register Index

These bits determine which of the 64 possible socket-specific registers will be accessed when the **Data** register is next accessed by the processor. Note that some values of the Register Index field are reserved, see Table 6–1.

Bit 6: Socket Index

This bit determines which set of socket-specific registers is currently selected. When this bit is a '0', a Socket A register is selected; when this bit is a '1', a Socket B register is selected.

The **Index** register value determines which internal register should be accessed (read or written) in response to each CPU access of the **Data** register. Each of the two possible PCMCIA sockets is allocated 64 of the 256 locations in the internal register index space.

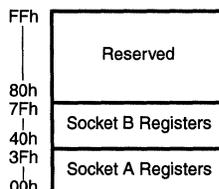


Figure 6–2. Socket/Register Index Space

When viewed as a 7-bit value, the contents of this register completely specify a single internal-register byte. For example, when the value of this register is in the range 00h–3Fh, a Socket A register is selected (Socket Index bit is a '0'), and when the value of this register is in the range 40h–7Fh, a Socket B register is selected (Socket Index bit is a '1').

The internal register that is accessed when the CPU reads or writes the **Data** register is determined by the current value of the **Index** register, as follows:

Table 6–1. Index Registers

0EFF5

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B		
Chip Revision	00h ^a		Chapter 7: Device Control	36
Interface Status	01h	41h		37
Power Control	02h	42h		39
Interrupt and General Control	03h	43h		41
Card Status Change	04h	44h		43
Management Interrupt Configuration	05h	45h		44
Mapping Enable	06h	46h		46
I/O Window Control	07h	47h	Chapter 8: I/O Window Mapping	48
System I/O Map 0 Start Address Low	08h	48h		49
System I/O Map 0 Start Address High	09h	49h		49
System I/O Map 0 End Address Low	0Ah	4Ah		50
System I/O Map 0 End Address High	0Bh	4Bh		50
System I/O Map 1 Start Address Low	0Ch	4Ch		49
System I/O Map 1 Start Address High	0Dh	4Dh		49
System I/O Map 1 End Address Low	0Eh	4Eh		50
System I/O Map 1 End Address High	0Fh	4Fh		50
System Memory Map 0 Start Address Low	10h	50h		Chapter 9: Memory Window Mapping
System Memory Map 0 Start Address High	11h	51h	53	
System Memory Map 0 End Address Low	12h	52h	53	
System Memory Map 0 End Address High	13h	53h	54	
Card Memory Map 0 Offset Address Low	14h	54h	55	
Card Memory Map 0 Offset Address High	15h	55h	55	
Misc Control 1	16h	56h	Chapter 10: Extension	57
FIFO Control	17h	57h		59
System Memory Map 1 Start Address Low	18h	58h	Chapter 9: Memory Window Mapping	52
System Memory Map 1 Start Address High	19h	59h		53
System Memory Map 1 End Address Low	1Ah	5Ah		53
System Memory Map 1 End Address High	1Bh	5Bh		54
Card Memory Map 1 Offset Address Low	1Ch	5Ch		55
Card Memory Map 1 Offset Address High	1Dh	5Dh		55
Misc Control 2	1Eh ^a		Chapter 10: Extension	60
Chip Information	1Fh ^a			61
System Memory Map 2 Start Address Low	20h	60h	Chapter 9: Memory Window Mapping	52
System Memory Map 2 Start Address High	21h	61h		53
System Memory Map 2 End Address Low	22h	62h		53

Table 6-1. Index Registers (cont.)

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B		
System Memory Map 2 End Address High	23h	63h	Chapter 9: Memory Window Mapping	54
Card Memory Map 2 Offset Address Low	24h	64h		55
Card Memory Map 2 Offset Address High	25h	65h		55
ATA Control	26h	66h	Chapter 10: Extension	62
<i>Scratchpad</i>	27h	67h	–	–
System Memory Map 3 Start Address Low	28h	68h	Chapter 9: Memory Window Mapping	49
System Memory Map 3 Start Address High	29h	69h		53
System Memory Map 3 End Address Low	2Ah	6Ah		53
System Memory Map 3 End Address High	2Bh	6Bh		54
Card Memory Map 3 Offset Address Low	2Ch	6Ch		55
Card Memory Map 3 Offset Address High	2Dh	6Dh		55
Extended Index:	2Eh	6Eh		63
<i>Scratchpad</i>	Extended index 00h		–	
<i>Reserved</i>	Extended index 01h		–	
<i>Reserved</i>	Extended index 02h		–	
Extension Control 1	Extended index 03h		64	
<i>Reserved</i>	Extended index 04h		–	
System Memory Map 0 Upper Address	Extended index 05h		65	
System Memory Map 1, Upper Address	Extended index 06h		65	
System Memory Map 2 Upper Address	Extended index 07h		65	
System Memory Map 3 Upper Address	Extended index 08h		65	
System Memory Map 4 Upper Address	Extended index 09h		65	
External Data	Extended index 0Ah		65	
Extension Control 2	Extended index 0Bh		66	
Extended Data	2Fh	6Fh	Chapter 10: Extension	63
System Memory Map 4 Start Address Low	30h	70h	Chapter 9: Memory Window Mapping	49
System Memory Map 4 Start Address High	31h	71h		53
System Memory Map 4 End Address Low	32h	72h		53
System Memory Map 4 End Address High	33h	73h		54
Card Memory Map 4 Offset Address Low	34h	74h		55
Card Memory Map 4 Offset Address High	35h	75h		55
Card I/O Map 0 Offset Address Low	36h	76h		51
Card I/O Map 0 Offset Address High	37h	77h	Chapter 8: I/O Window Mapping	51
Card I/O Map 1 Offset Address Low	38h	78h		51
Card I/O Map 1 Offset Address High	39h	79h		51
Setup Timing 0	3Ah	7Ah	Chapter 11: Timing	67
Command Timing 0	3Bh	7Bh		68
Recovery Timing 0	3Ch	7Ch		69
Setup Timing 1	3Dh	7Dh		67
Command Timing 1	3Eh	7Eh		68
Recovery Timing 1	3Fh	7Fh		69
<i>Reserved</i>	80h–FFh			–

^a This register affects both sockets (it is not specific to either socket).

6.2 Data

Register Name: Data						Register Per: chip	
Index: n/a						Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data							

The **Data** register is accessed at **Base Address 0 + 1**. This register indicates the contents of the register at the Socket/Register Index selected by the **Index** register.

Index

[2E] ← 0x03 (ADDR EXT 1 REG)

[2F] ← 0x18 (INIT OK)

[03] ← 0x63 (STEER TO PLS "A")

EEFC = INDEX

ECFD = DATA

7. DEVICE CONTROL REGISTERS

7.1 Chip Revision

Register Name: Chip Revision				Register Per: chip			
Index: 00h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interface ID		0	0	Revision			
R:10		R:0	R:0	R:0010 ^a			

^a Value for the current stepping only.

Bits 3-0: Revision

This field indicates the CL-PD6729's compatibility with the 82365SL A-step.

Bits 7-6: Interface ID

00	I/O only.
01	Memory only.
10	Memory and I/O.
11	Reserved.

These bits identify what type of interface this controller supports. The CL-PD6729 supports both memory and I/O interface PCMCIA cards.

7.2 Interface Status

Register Name: Interface Status						Register Per: socket	
Index: 01h						Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5 RDY	Bit 4 WP	Bit 3 -CD2	Bit 2 -CD1	Bit 1 BVD2	Bit 0 BVD1
1	Card Power On	Ready/Busy*	Write Protect	Card Detect		Battery Voltage Detect	
R:1 ^a	R:0	R ^b	R ^c	R ^d		R ^e	

- ^a Bit 7 always reads a '1' on the CL-PD6729.
- ^b Bit 5 indicates the value of the RDY/-IREQ pin (see page 12).
- ^c Bit 4 indicates the value of the WP/-IOIS16 pin (see page 11).
- ^d Bits 3-2 indicate the inversion of the values of the -CD1 and -CD2 pins (see page 12).
- ^e Bits 1-0 indicate the values of the BVD1/-STSCHG/-RI and BVD2/-SPKR/-LED pins (see page 12).

Bits 1-0: Battery Voltage Detect

BVD2 Level	BVD1 Level	Bit 1	Bit 0	PCMCIA Interpretation
Low	Low	0	0	Card data lost
Low	High	0	1	Battery low warning
High	Low	1	0	Card data lost
High	High	1	1	Battery/data okay

In Memory Card Interface mode, these bits are used by PCMCIA support software and firmware to indicate the remaining capacity of the battery in battery-backed cards. In I/O Card Interface mode, bit 0 indicates the state of the BVD1/-STSCHG/-RI pin (see page 13). Bit 1 status is not valid in I/O Card Interface mode.

Bits 3-2: Card Detect

-CD2 Level	-CD1 Level	Bit 3	Bit 2	Card Detect Status
High	High	0	0	Either no card or card is not fully inserted
High	Low	0	1	Card is not fully inserted
Low	High	1	0	Card is not fully inserted
Low	Low	1	1	Card is fully inserted

These bits indicate the state of the -CD1 and -CD2 pins (see page 12).

Bit 4: Write Protect

0	Card is not write protected.
1	Card is write protected.

In Memory Card Interface mode, this bit indicates the state of the WP/-IOIS16 pin (see page 11) on the card. This bit is not valid in I/O Card Interface mode.

Bit 5: Ready/Busy*

0	Card is not ready.
1	Card is ready.

In Memory Card Interface mode, this bit indicates the state of the RDY/-IREQ pin (see page 12) on the card. This bit is not valid in I/O Card Interface mode.

Bit 6: Card Power On

0	Power to the card is not on.
1	Power to the card is on.

This status bit indicates whether power to the card is on. Refer to the Table 7-1 for more details.

7.3 Power Control

Register Name: Power Control				Register Per: socket			
Index: 02h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Card Enable	Compatibility Bit	Auto-Power	V _{CC} Power	Compatibility Bits		V _{pp1} Power	
RW:0	RW:0	RW:0	RW:0	RW:00		RW:00	

Table 7-1. Enabling of Socket Power Controls

RST# Level	Both -CD1 and -CD2 are Active (Low)	Power Control Register		Interface Status Register (see page 37)	-VCC_3 and -VCC_5 Levels	VPP_PGM and VPP_VCC Levels
		V _{CC} Power (Bit 4)	Auto-Power (Bit 5)	Card Power On (Bit 6)		
Low	X	X	X	0	Inactive (high)	Inactive (low)
High	X	0	X	0	Inactive (high)	Inactive (low)
High	X	1	0	1	Activated per Misc Control 1 register, bit 1	Activated per Power Control register, bits 1 and 0
High	No	1	1	0	Inactive (high)	Inactive (low)
High	Yes	1	1	1	Activated per Misc Control 1 register, bit 1	Activated per Power Control register, bits 1 and 0

Table 7-2. Enabling of Output Signals to Socket

RST# Level	Both -CD1 and -CD2 are Active (Low)	Power Control Register		CL-PD6729 Output Signals to Socket
		V _{CC} Power (Bit 4)	Card Enable (Bit 7)	
Low	X	X	X	High impedance
High	No	X	X	High impedance
High	Yes	0	0	High impedance
High	Yes	0	1	Enabled
High	Yes	1	0	High impedance
High	Yes	1	1	Enabled

Bits 1-0: V_{PP1} Power

Bit 1	Bit 0	VPP_PGM	VPP_VCC	PCMCIA Intended Socket Function
0	0	Inactive (low)	Inactive (low)	Zero volts to PCMCIA socket V _{PP1} pin
0	1	Inactive (low)	Active (high) ^a	Selected card V _{CC} to PCMCIA socket V _{PP1} pin
1	0	Active (high) ^a	Inactive (low)	+12V to PCMCIA socket V _{PP1} pin
1	1	Inactive (low)	Inactive (low)	Zero volts to PCMCIA socket V _{PP1} pin

^a Under conditions where V_{PP1} power is activated. See Table 7-1.

These bits control the power to the V_{PP1} pin of the PCMCIA card.

Bit 4: V_{CC} Power

0	Power is not applied to the card: the -VCC_3 and -VCC_5 socket power control pins are inactive (high).
1	Power is applied to the card: if bit 5 is a '0', or bit 5 is a '1' and -CD2 and -CD1 are active low, then the selected -VCC_3 or -VCC_5 socket power control pin is active (low).

Depending on the value of bit 5 below, setting this bit to a '1' applies power to the card. The V_{CC} 3.3V bit (see page 57) determines whether 3.3V or 5V power is applied. Note that this bit is reset to a '0' when a card is removed from the socket unless the auto-power-off feature is disabled by setting **Extension Control 1** register bit 1 to a '1'; a write is required to reactivate power to the card.

Bit 5: Auto-Power

0	V _{CC} and V _{PP1} power control signals are activated independent of the socket's -CD2 and -CD1 input levels.
1	V _{CC} and V _{PP1} power control signals are only activated if the socket's -CD2 and -CD1 inputs are both active (low).

When this bit is set to a '1', the CL-PD6729 allows power to the card to be turned on and off automatically with the insertion and removal of a PCMCIA card.

Bit 7: Card Enable

0	Outputs to card socket are not enabled and are floating.
1	Outputs to card socket are enabled if -CD1 and -CD2 are active low and bit 4 is a '1'.

When this bit is a '1', the outputs to the PCMCIA card are enabled if a card is present and card power is being supplied. The pins affected include -CE2, -CE1, -IORD, -IOWR, -OE, -REG, RESET, A[25:0], D[15:0], and -WE.

7.4 Interrupt and General Control

Register Name: Interrupt and General Control				Register Per: socket			
Index: 03h				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Ring Indicate Enable	Card Reset*	Card Is I/O	Manage Int Enable		IRQ Level		
RW:0	RW:0	RW:0	RW:0		RW:0000		

Bits 3-0: IRQ Level

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ3 (INTA#)
0100	IRQ4 (INTB#)
0101	IRQ5 (INTC#)
0110	Reserved
0111	IRQ7 (INTD#)
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14 (This output can alternately be used as external clock input.)
1111	IRQ15 (This output can alternately be used as ring indicate output.)

These bits determine which IRQ will occur when the card causes an interrupt through the RDY/-IREQ pin on the PCMCIA socket.

Bit 4: Manage Int Enable

0	Management IRQ (see page 45) specifies management interrupt bits.
1	Reserved.

This bit was created to determine how management interrupts occur on ISA-based systems. It is included for software compatibility. Because there is no -INTR pin on the PCI bus, setting this bit to a '1' would cause management interrupts not to occur.

Bit 5: Card Is I/O

0	Sets Memory Card Interface mode. The card socket is configured to support memory-only-type cards. All dual-function socket interface pins are defined to perform memory-only-type interface functions.
1	Sets I/O Card Interface mode. The card socket is configured to support combined I/O-and-memory-type cards. All dual-function socket interface pins are defined to perform all I/O and basic memory type interface functions.

This bit determines how dual-function socket interface pins will be used. For more information on specific pins, refer to Table 2-2 in Chapter 2.

Bit 6: Card Reset*

0	The RESET signal to the card socket is set active (high for normal, low for ATA mode).
1	The RESET signal to the card socket is set inactive (low for normal, high for ATA mode).

This bit determines whether the RESET signal (see page 12) to the card is active or inactive. When the Card Enable bit (see page 40) is a '0', the RESET signal to the card is high impedance. See Chapter 10 for further description of ATA mode functions.

Bit 7: Ring Indicate Enable

0	BVD1/-STSCHG/-RI pin is status change function.
1	BVD1/-STSCHG/-RI pin is ring indicate input pin from card.

In I/O Card Interface mode, this bit determines whether the -STSCHG input pin is used to activate the IRQ15 pin in conjunction with the IRQ15 Is RI Out bit (**Misc Control 2** bit 7, see page 60). This bit is not valid in Memory Card Interface mode.

7.5 Card Status Change

Register Name: Card Status Change				Register Per: socket			
Index: 04h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	Card Detect Change	Ready Change	Battery Warning Change	Battery Dead Or Status Change
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

This register indicates the source of a management interrupt generated by the CL-PD6729.

NOTE: The corresponding bit in the **Management Interrupt Configuration** register must be set to a '1' to enable each specific status change detection.

Bit 0: Battery Dead Or Status Change

0	A transition (from high to low in Memory Card Interface mode or either high to low or low to high in I/O Card Interface mode) on the BVD1/-STSCHG/-RI pin has not occurred since this register was last read.
1	A transition on the BVD1/-STSCHG/-RI pin has occurred.

In Memory Card Interface mode, this bit is set to a '1' when the BVD1/-STSCHG/-RI pin (see page 13) changes from high to low, indicating a battery dead condition. In I/O Card Interface mode, this bit is set to a '1' when the BVD1/-STSCHG/-RI pin changes from either high to low or low to high. In I/O Card Interface mode, the function of this bit is not affected by bit 7 of the **Interrupt and General Control** register. This bit is reset to a '0' whenever this register is read.

Bit 1: Battery Warning Change

0	A transition (from high to low) on the BVD2/-SPKR/-LED pin has not occurred since this register was last read.
1	A transition on the BVD2/-SPKR/-LED pin has occurred.

In Memory Card Interface mode, this bit is set to a '1' when the BVD2/-SPKR/-LED pin changes from high to low, indicating a battery warning. This bit is not valid in I/O Card Interface mode. This bit is reset to a '0' whenever this register is read.

Bit 2: Ready Change

0	A transition on the RDY/-IREQ pin has not occurred since this register was last read.
1	A transition on the RDY/-IREQ pin has occurred.

In Memory Card Interface mode, this bit is a '1' when a change has occurred on the RDY/-IREQ pin (see page 12). In I/O Card Interface mode, this bit always reads a '0'. This bit is reset to a '0' whenever this register is read.

Bit 3: Card Detect Change

0	A transition on neither the -CD1 nor the -CD2 pin has occurred since this register was last read.
1	A transition on either the -CD1 or the -CD2 pin or both has occurred.

This bit is set to a '1' when a change has occurred on the -CD1 or -CD2 pin (see page 12). This bit is reset to a '0' whenever this register is read.

7.6 Management Interrupt Configuration

Register Name: Management Interrupt Configuration							Register Per: socket
Index: 05h							Register Compatibility Type: 365
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Management IRQ				Card Detect Enable	Ready Enable	Battery Warning Enable	Battery Dead Or Status Change Enable
RW:0000				RW:0	RW:0	RW:0	RW:0

This register controls which status changes cause management interrupts as well as at which pin the management interrupts will appear.

Bit 0: Battery Dead Or Status Change Enable

0	Battery Dead Or Status Change management interrupt disabled.
1	If Battery Dead Or Status Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Battery Dead Or Status Change bit (see page 43) is a '1'. This allows management interrupts to be generated on changes in level of the BVD1/-STSCHG/-RI pin.

Bit 1: Battery Warning Enable

0	Battery Warning Change management interrupt disabled.
1	If Battery Warning Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Battery Warning Change bit (see page 43) is a '1'. This allows management interrupts to be generated on changes in level of the BVD2/-SPKR/-LED pin. This bit is not valid in I/O Card Interface mode.

Bit 2: Ready Enable

0	Ready Change management interrupt disabled.
1	If Ready Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Ready Change bit (see page 43) is a '1'. This allows management interrupts to be generated on changes in level of the RDY/-IREQ pin.

Bit 3: Card Detect Enable

0	Card Detect Change management interrupt disabled.
1	If Card Detect Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Card Detect Change bit (see page 43) is a '1'. This allows management interrupts to be generated on changes in level of the -CD1 and -CD2 pins.

Bits 7-4: Management IRQ

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ3 (INTA#)
0100	IRQ4 (INTB#)
0101	IRQ5 (INTC#)
0110	Reserved
0111	IRQ7 (INTD#)
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14 (This output can alternately be used as external clock input.)
1111	IRQ15 (This output can alternately be used as ring indicate output.)

These bits determine which interrupt pin will be used for card status change management interrupts.

7.7 Mapping Enable

<i>Register Name: Mapping Enable</i>						<i>Register Per: socket</i>	
<i>Index: 06h</i>						<i>Register Compatibility Type: 365</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
I/O Map 1 Enable	I/O Map 0 Enable	Compatibility Bit	Memory Map 4 Enable	Memory Map 3 Enable	Memory Map 2 Enable	Memory Map 1 Enable	Memory Map 0 Enable
RW:0	RW:0	R:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: Memory Map 0 Enable

0	Memory Window Mapping registers for Memory Window 0 disabled.
1	Memory Window Mapping registers for Memory Window 0 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 0 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 1: Memory Map 1 Enable

0	Memory Window Mapping registers for Memory Window 1 disabled.
1	Memory Window Mapping registers for Memory Window 1 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 1 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 2: Memory Map 2 Enable

0	Memory Window Mapping registers for Memory Window 2 disabled.
1	Memory Window Mapping registers for Memory Window 2 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 2 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 3: Memory Map 3 Enable

0	Memory Window Mapping registers for Memory Window 3 disabled.
1	Memory Window Mapping registers for Memory Window 3 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 3 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 4: Memory Map 4 Enable

0	Memory Window Mapping registers for Memory Window 4 disabled.
1	Memory Window Mapping registers for Memory Window 4 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 4 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 6: I/O Map 0 Enable

0	I/O Window Mapping registers for I/O Window 0 disabled.
1	I/O Window Mapping registers for I/O Window 0 enabled.

When this bit is a '1', the I/O Window Mapping registers for I/O Window 0 are enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

Bit 7: I/O Map 1 Enable

0	I/O Window Mapping registers for I/O Window 1 disabled.
1	I/O Window Mapping registers for I/O Window 1 enabled.

When this bit is a '1', the I/O Window Mapping registers for I/O Window 1 are enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

8. I/O WINDOW MAPPING REGISTERS

CAUTION: Be sure that the I/O windows do not map to the **Base Address 0** register programmed at offset 10h.

8.1 I/O Window Control

Register Name: I/O Window Control							Register Per: socket	
Index: 07h							Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Timing Register Select 1	Compatibility Bit	Auto-Size I/O Window 1	I/O Window 1 Size	Timing Register Select 0	Compatibility Bit	Auto-Size I/O Window 0	I/O Window 0 Size	
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	

Bit 0: I/O Window 0 Size

0	8-bit data path to I/O Window 0.
1	16-bit data path to I/O Window 0.

When bit 1 if this register is a '0', this bit determines the width of the data path for I/O Window 0 accesses to the card. When bit 1 is a '1', this bit is ignored.

Bit 1: Auto-Size I/O Window 0

0	I/O Window 0 Size (see bit 0 of this register) determines the data path for I/O Window 0 accesses.
1	The data path to I/O Window 0 is determined by the -IOIS16 level returned by the card.

This bit controls the method that the width of the data path for I/O Window 0 accesses to the card is determined. Note that when this bit is a '1', the -IOIS16 signal (see page 11) determines the width of the data path to the card.

Bit 3: Timing Register Select 0

0	Accesses made with timing specified in Timer Set 0 registers.
1	Accesses made with timing specified in Timer Set 1 registers.

This bit determines the access timing specification (see Chapter 11) for I/O Window 0.

Bit 4: I/O Window 1 Size

0	8-bit data path to I/O Window 1.
1	16-bit data path to I/O Window 1.

When bit 5 of this register is a '0', this bit determines the width of the data path for I/O Window 1 accesses to the card. When bit 5 is a '1', this bit is ignored.

Bit 5: Auto-Size I/O Window 1

0	I/O Window 1 Size (see bit 4 of this register) determines the data path for I/O Window 1 accesses.
1	The data path to I/O Window 1 will be determined based on -IOIS16 returned by the card.

This bit controls the method that the width of the data path for I/O Window 1 accesses to the card is determined. Note that when this bit is a '1', the -IOIS16 signal (see page 11) determines the width of the data path to the card. This bit must be set to a '1' for correct ATA mode operation (see Chapter 12).

Bit 7: Timing Register Select 1

0	Accesses made with timing specified in Timer Set 0.
1	Accesses made with timing specified in Timer Set 1.

This bit determines the access timing specification (see Chapter 11) for I/O Window 1.

8.2 System I/O Map 0-1 Start Address Low

<i>Register Name:</i> System I/O Map 0-1 Start Address Low						<i>Register Per:</i> socket	
<i>Index:</i> 08h, 0Ch						<i>Register Compatibility Type:</i> 365	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Start Address 7-0							
RW:00000000							

There are two separate System I/O Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map Start Address Low
08h	System I/O Map 0 Start Address Low
0Ch	System I/O Map 1 Start Address Low

Bits 7-0: Start Address 7-0

This register contains the least-significant byte of the address that specifies where in the I/O space the corresponding I/O map will begin. I/O accesses that are equal or above this address and equal or below the corresponding System I/O Map End Address will be mapped into the I/O space of the corresponding PCMCIA card.

The most-significant byte is located in the **System I/O Map 0-1 Start Address High** register.

8.3 System I/O Map 0-1 Start Address High

<i>Register Name:</i> System I/O Map 0-1 Start Address High						<i>Register Per:</i> socket	
<i>Index:</i> 09h, 0Dh						<i>Register Compatibility Type:</i> 365	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Start Address 15-8							
RW:00000000							

There are two separate System I/O Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map Start Address High
09h	System I/O Map 0 Start Address High
0Dh	System I/O Map 1 Start Address High

Bits 15-8: Start Address 15-8

This register contains the most-significant byte of the Start Address. See the description of the Start Address field associated with bits 7-0 of the **System I/O Map 0-1 Start Address Low** register.

8.4 System I/O Map 0-1 End Address Low

<i>Register Name: System I/O Map 0-1 End Address Low</i>						<i>Register Per: socket</i>	
<i>Index: 0Ah, 0Eh</i>						<i>Register Compatibility Type: 365</i>	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
End Address 7-0							
RW:00000000							

There are two separate System I/O Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map End Address Low
0Ah	System I/O Map 0 End Address Low
0Eh	System I/O Map 1 End Address Low

Bits 7-0: End Address 7-0

This register contains the least-significant byte of the address that specifies where in the I/O space the corresponding I/O map will end. I/O accesses that are equal or below this address and equal or above the corresponding System I/O Map Start Address will be mapped into the I/O space of the corresponding PCMCIA card.

The most-significant byte is located in the **System I/O Map 0-1 End Address High** register.

8.5 System I/O Map 0-1 End Address High

<i>Register Name: System I/O Map 0-1 End Address High</i>						<i>Register Per: socket</i>	
<i>Index: 0Bh, 0Fh</i>						<i>Register Compatibility Type: 365</i>	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
End Address 15-8							
RW:00000000							

There are two separate System I/O Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map End Address High
0Bh	System I/O Map 0 End Address High
0Fh	System I/O Map 1 End Address High

Bits 15-8: End Address 15-8

This register contains the most-significant byte of the End Address. See the description of the End Address field associated with bits 7-0 of the **System I/O Map 0-1 End Address Low** register.

8.6 Card I/O Map 0-1 Offset Address Low

Register Name: Card I/O Map 0-1 Offset Address Low							Register Per: socket
Index: 36h, 38h							Register Compatibility Type: ext.
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Offset Address 7-1							0 ^a
RW:0000000							RW:0

^a This bit must be programmed to '0'.

There are two separate Card I/O Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card I/O Map Offset Address Low
36h	Card I/O Map 0 Offset Address Low
38h	Card I/O Map 1 Offset Address Low

Bits 7-1: Offset Address 7-1

This register contains the least-significant byte of the quantity that will be added to the system I/O address that determines where in the PCMCIA card's I/O map the I/O access will occur.

The most-significant byte is located in the **Card I/O Map 0-1 Offset Address High** register.

8.7 Card I/O Map 0-1 Offset Address High

Register Name: Card I/O Map 0-1 Offset Address High							Register Per: socket
Index: 37h, 39h							Register Compatibility Type: ext.
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Offset Address 15-8							
RW:00000000							

There are two separate Card I/O Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card I/O Map Offset Address High
37h	Card I/O Map 0 Offset Address High
39h	Card I/O Map 1 Offset Address High

Bits 15-8: Offset Address 15-8

This register contains the most-significant byte of the Offset Address. See the description of the End Address field associated with bits 7-1 of the **Card I/O Map 0-1 Offset Address Low** register.

9. MEMORY WINDOW MAPPING REGISTERS

The following information about the memory map windows is important:

- The memory window mapping registers determine where in the PCI memory space and PC card memory space accesses will occur. There are five memory windows that can be used independently.
- The memory windows are enabled and disabled using the **Mapping Enable** register (see page 46).
- To specify where in the PCI space a memory window is mapped, start and end addresses are specified. A memory window is selected whenever the appropriate Memory Map Enable bit (see page 46) is set and the following conditions are true:
 - The PCI address is greater than or equal to the appropriate **System Memory Map Start Address** register (see page 52).
 - The PCI address is less than or equal to the appropriate **System Memory Map End Address** register (see page 53).
 - The **System Memory Map Upper Address** register (see page 65) is equal to the upper PCI address.
- Start and end addresses are specified with PCI Address bits 31-12. This sets the minimum size of a memory window to 4K bytes. Memory windows are specified in the PCI memory address space.
- To ensure proper operation, none of the memory windows can overlap in the PCI address space.

9.1 System Memory Map 0-4 Start Address Low

<i>Register Name:</i> System Memory Map 0-4 Start Address Low						<i>Register Per:</i> socket	
<i>Index:</i> 10h, 18h, 20h, 28h, 30h						<i>Register Compatibility Type:</i> 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Start Address 19-12 RW:00000000							

There are five separate System Memory Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map Start Address Low
10h	System Memory Map 0 Start Address Low
18h	System Memory Map 1 Start Address Low
20h	System Memory Map 2 Start Address Low
28h	System Memory Map 3 Start Address Low
30h	System Memory Map 4 Start Address Low

Bits 7-0: Start Address 19-12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will begin. Memory accesses that are equal or above this address and equal or below the corresponding System Memory Map End Address will be mapped into the memory space of the corresponding PCMCIA card.

The most-significant four bits are located in the **System Memory Map 0-4 Start Address High** register.

9.2 System Memory Map 0-4 Start Address High

<i>Register Name: System Memory Map 0-4 Start Address High</i>						<i>Register Per: socket</i>	
<i>Index: 11h, 19h, 21h, 29h, 31h</i>						<i>Register Compatibility Type: 365</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Window Data Size	Compatibility Bit	Scratchpad Bits		Start Address 23-20			
RW:0	RW:0	RW:00		RW:0000			

There are five separate System Memory Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map Start Address High
11h	System Memory Map 0 Start Address High
19h	System Memory Map 1 Start Address High
21h	System Memory Map 2 Start Address High
29h	System Memory Map 3 Start Address High
31h	System Memory Map 4 Start Address High

Bits 3-0: Start Address 23-20

This field contains the most-significant four bits of the Start Address. See the description of the Start Address field associated with bits 7-0 of the **System Memory Map 0-4 Start Address Low** register.

Bit 7: Window Data Size

0	8-bit data path to the card.
1	16-bit data path to the card.

This bit determines the data path size to the card.

9.3 System Memory Map 0-4 End Address Low

<i>Register Name: System Memory Map 0-4 End Address Low</i>						<i>Register Per: socket</i>	
<i>Index: 12h, 1Ah, 22h, 2Ah, 32h</i>						<i>Register Compatibility Type: 365</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
End Address 19-12							
RW:00000000							

There are five separate System Memory Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map End Address Low
12h	System Memory Map 0 End Address Low
1Ah	System Memory Map 1 End Address Low
22h	System Memory Map 2 End Address Low
2Ah	System Memory Map 3 End Address Low
32h	System Memory Map 4 End Address Low

Bits 7-0: End Address 19-12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will end. Memory accesses that are equal or below this address and equal or above the corresponding System Memory Map Start Address will be mapped into the memory space of the corresponding PCMCIA card.

The most-significant four bits are located in the **System Memory Map 0-4 End Address High** register.

9.4 System Memory Map 0-4 End Address High

<i>Register Name: System Memory Map 0-4 End Address High</i>				<i>Register Per: socket</i>			
<i>Index: 13h, 1Bh, 23h, 2Bh, 33h</i>				<i>Register Compatibility Type: 365</i>			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Card Timer Select		Scratchpad Bits		End Address 23-20			
RW:00		RW:00		RW:0000			

There are five separate System Memory Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map End Address High
13h	System Memory Map 0 End Address High
1Bh	System Memory Map 1 End Address High
23h	System Memory Map 2 End Address High
2Bh	System Memory Map 3 End Address High
33h	System Memory Map 4 End Address High

Bits 3-0: End Address 23-20

This field contains the most-significant four bits of the End Address. See the description of the End Address field associated with bits 7-0 of the **System Memory Map 0-4 End Address Low** register. Note that the upper memory addresses are stored in the **System Memory Map Upper Address** register.

Bits 7-6: Card Timer Select

00	Selects Timer Set 0.
01	Selects Timer Set 1.
10	Selects Timer Set 1.
11	Selects Timer Set 1.

This field selects the timer set. Timer Set 0 and 1 reset to values compatible with standard PCI and three-wait-state cycles (see page 67).

9.5 Card Memory Map 0-4 Offset Address Low

<i>Register Name: Card Memory Map 0-4 Offset Address Low</i>						<i>Register Per: socket</i>	
<i>Index: 14h, 1Ch, 24h, 2Ch, 34h</i>						<i>Register Compatibility Type: 365</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Offset Address 19-12							
RW:00000000							

There are five separate Card Memory Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card Memory Map Offset address Low
14h	Card Memory Map 0 Offset Address Low
1Ch	Card Memory Map 1 Offset Address Low
24h	Card Memory Map 2 Offset Address Low
2Ch	Card Memory Map 3 Offset Address Low
34h	Card Memory Map 4 Offset Address Low

Bits 7-0: Offset Address 19-12

This register contains the least-significant byte of the quantity that will be added to the system memory address that determines where in the PCMCIA card's memory map the memory access will occur.

The most-significant six bits are located in the **Card Memory Map 0-4 Offset Address High** register.

9.6 Card Memory Map 0-4 Offset Address High

<i>Register Name: Card Memory Map 0-4 Offset Address High</i>						<i>Register Per: socket</i>	
<i>Index: 15h, 1Dh, 25h, 2Dh, 35h</i>						<i>Register Compatibility Type: 365</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Write Protect	REG Setting	Offset Address 25-20					
RW:0	RW:0	RW:000000					

There are five separate Card Memory Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Memory Map Address Offset High
15h	Card Memory Map 0 Offset Address High
1Dh	Card Memory Map 1 Offset Address High
25h	Card Memory Map 2 Offset Address High
2Dh	Card Memory Map 3 Offset Address High
35h	Card Memory Map 4 Offset Address High

Bits 5-0: Offset Address 25-20

This field contains the most-significant six bits of the Offset Address. See the description of the Offset Address field associated with bits 7-0 of the **Card Memory Map 0-4 Offset Address Low** register.

Bit 6: REG Setting

0	-REG (see page 11) is not active for accesses made through this window.
1	-REG is active for accesses made through this window.

This bit determines whether -REG (see page 11) is active for accesses made through this window. Card Information Structure (CIS) memory is accessed by setting this bit to a '1'.

Bit 7: Write Protect

0	Writes to the card through this window are allowed.
1	Writes to the card through this window are inhibited.

This bit determines whether writes to the card through this window are allowed.

10. EXTENSION REGISTERS

10.1 Misc Control 1

Register Name: Misc Control 1						Register Per: socket	
Index: 16h						Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Inpack Enable	Scratchpad Bits		Speaker Enable	Pulse System IRQ	Pulse Management Interrupt	V _{CC} 3.3V	Reserved
RW:0	RW:00		RW:0	RW:0	RW:0	RW:0	R:0

Bit 1: V_{CC} 3.3V

0	-VCC_5 activated when card power is to be applied.
1	-VCC_3 activated when card power is to be applied.

This bit determines which output pin is used to enable V_{CC} power to the socket when card power is applied; this bit is used in conjunction with bits 5-4 of the **Power Control** register (see page 39).

Bit 2: Pulse Management Interrupt

0	Interrupts are passed to the IRQ[XX] pin as level-sensitive.
1	When an interrupt occurs, the IRQ[XX] pin is driven with the pulse train shown in Figure 10-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] pin (see page 9). Note that a clock must be present on PCI_CLK or IRQ14/EXT_CLK for pulsed interrupts to work. Refer to Section 13.3.2 for more information on interrupt timing.

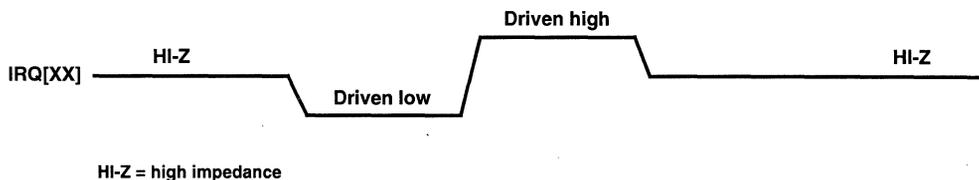


Figure 10-1. Pulse Mode Interrupts

Bit 3: Pulse System IRQ

0	Interrupts are passed to the IRQ[XX] pin as level-sensitive.
1	When an interrupt occurs, the IRQ[XX] pin is driven with the pulse train shown in Figure 10-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] pins (see page 9).

Bit 4: Speaker Enable

0	SPKR_OUT* is three-stated.
1	SPKR_OUT* is driven from the XOR of -SPKR from each enabled socket.

This bit determines whether the card -SPKR pin will drive SPCR_OUT* (see page 14).

Bit 7: Inpack Enable

0	-INPACK pin (see page 12) ignored.
1	-INPACK pin used to control data bus drivers during I/O read from the socket.

The -INPACK function is not applicable in PCI bus environments. This bit is provided for compatibility with other Cirrus Logic products.



10.2 FIFO Control

Register Name: FIFO Control				Register Per: socket			
Index: 17h				Register Compatibility Type: ext.			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO Status / Flush FIFO		Scratchpad Bits					
RW:1		RW:0000000					

Bit 7: FIFO Status / Flush FIFO

Value	I/O Read	I/O Write
0	FIFO not empty	No operation occurs (default at reset)
1	FIFO empty	Flush the FIFO

This bit controls FIFO operation and reports FIFO status. When this bit is set to a '1' during write operations, all data in the FIFO is lost. During read operations, when this bit is a '1', the FIFO is empty. During read operations when this bit is a '0', the FIFO has valid data.

This bit is used to ensure the FIFO is empty before changing any registers; registers should not be modified while the write FIFO is not empty.

FIFO contents will be lost whenever any of the following occur:

- RST# pin (see page 9) is a '0'.
- The card is removed.
- V_{CC} Power bit (see page 40) is programmed to a '0'.

10.3 Misc Control 2

Register Name: Misc Control 2							Register Per: chip
Index: 1Eh							Register Compatibility Type: ext.
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ15/ RI_OUT* Is RI Out	Reserved		Timer Clock Divide	5V Core	Suspend Mode	Low-Power Dynamic Mode	External Clock Enable
RW:0	RW:00		RW:0	RW:0	RW:0	RW:1	RW:0

Bit 0: External Clock Enable

0	External clock is disabled.
1	IRQ14/EXT_CLK pin will be used as an external clock whenever the PCI bus is not doing a transfer.

This bit determines whether the external clock option is enabled. When set to a '1', the clock supplied to IRQ14/EXT_CLK will be used as the internal clock. This feature facilitates PCMCIA cycle timing when the PCI bus clock is stopped to conserve power.

Bit 1: Low-Power Dynamic Mode

0	Clock runs always.
1	Normal operation, stop clock when possible.

This bit determines whether Low-power Dynamic mode is enabled.

Bit 2: Suspend Mode

0	Normal operation.
1	Stop internal clock, enable all Low-power modes, and disable socket access.

This bit enables Suspend mode.

Bit 3: 5V Core

0	Normal operation: use when CORE_VDD pin is connected to 3.3 volts.
1	Selects input thresholds for use when 5.0 volts is connected to the CL-PD6729 CORE_VDD pin.

This bit selects input threshold circuits. This bit must be set to a '1' when the CORE_VDD pin is connected to 5.0 volts to allow TTL-compatible input thresholds to the card socket.

Bit 4: Timer Clock Divide

0	Normal socket interface timing.
1	Timer clocks used for socket interface timing operate at half-frequency.

This bit allows the PCMCIA socket interface to operate at half the PCI_CLK or EXT_CLK frequency. This bit should be set to '1' whenever PCI_CLK or EXT_CLK is run faster than 25 MHz.

Bit 7: IRQ15/RI_OUT* Is RI Out

0	Normal IRQ15 operation on the IRQ15/RI_OUT* pin.
1	IRQ15/RI_OUT* is connected to ring indicate pin on the system logic.

This bit determines the function of the IRQ15/RI_OUT* pin. When this bit is set to a '1', IRQ15/RI_OUT* can be used to trigger restoration of system activity when a high-to-low change is detected on the BVD1/-STSCHG/-RI pin.

10.4 Chip Information

Register Name: Chip Information						Register Per: chip	
Index: 1Fh						Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cirrus Logic Host-Adapter Identification		Dual/Single Socket	CL-PD6729 Revision Level			Reserved	
R:11		R:1	R:nnnn ^a			R:0	

^a This read-only value depends on the revision level of the CL-PD6729 chip.

Bits 4-1: CL-PD6729 Revision Level

This field identifies the revision of the controller. Contact Cirrus Logic for more information on revision levels for the CL-PD6729.

Bit 5: Dual/Single Socket

0	Chip identified as a single-socket controller.
1	Chip identified as a dual-socket controller.

This bit specifies that the CL-PD6729 supports two sockets.

Bits 7-6: Cirrus Logic Host-Adapter Identification

00	Second read after I/O write to this register.
11	First read after I/O write to this register.

This field identifies a Cirrus Logic host-adapter device. After chip reset or doing an I/O write to this register, the first read of this register will return a 11b. On the next read, this field will be 00b. This pattern of toggling data on subsequent reads can be used by software to determine presence of a Cirrus Logic host adapter in a system or to determine occurrence of a device reset.

10.5 ATA Control

Register Name: ATA Control							Register Per: socket
Index: 26h							Register Compatibility Type: ext.
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A25/CSEL	A24/M/S*	A23/VU	A22	A21	Scratchpad Bit	Speaker Is LED Input	ATA Mode
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: ATA Mode

0	Normal operation.
1	Configures the socket interface to handle ATA-type disk drives.

This bit reconfigures the particular socket as an ATA drive interface. Refer to Table 12–1 on page 70 for PCMCIA socket pin definitions in ATA mode.

Bit 1: Speaker Is LED Input

0	Normal operation.
1	The PCMCIA -SPKR pin will be used to drive IRQ12 if Drive LED Enable (see page 59) is set.

This bit changes the function of the BVD2/-SPKR/-LED pin (see page 12) from digital speaker input to disk status LED input. When in I/O Card Interface mode or ATA mode, setting this bit to a '1' reconfigures the BVD2/-SPKR/-LED input pin to serve as a -LED input from the socket.

NOTE: This bit should be set to a '0' if in Memory Card Interface mode.

Bit 3: A21

In ATA mode, the value in this bit is applied to the ATA A21 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 4: A22

In ATA mode, the value in this bit is applied to the ATA A22 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 5: A23/VU

In ATA mode, the value in this bit is applied to the ATA A23 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 6: A24/M/S*

In ATA mode, the value in this bit is applied to the ATA A24 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 7: A25/CSEL

In ATA mode, the value in this bit is applied to the ATA A25 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

10.6 Extended Index

Register Name: Extended Index							Register Per: socket	
Index: 2Eh							Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Extended Index								
RW:00000000								

This register controls which of the following registers at index 2Fh can be accessed:

Register Name at Index 2Fh	Extended Index
Scratchpad	00h
Reserved	01h
Reserved	02h
Extension Control 1	03h
Reserved	04h
System Memory Map 0 Upper Address	05h
System Memory Map 1 Upper Address	06h
System Memory Map 2 Upper Address	07h
System Memory Map 3 Upper Address	08h
System Memory Map 4 Upper Address	09h
External Data	0Ah
Extension Control 2	0Bh

For information on how to access these registers, see Section 3.2.

10.7 Extended Data

Register Name: Extended Data							Register Per: socket	
Index: 2Fh							Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Extended Data								

The data in this register allows the registers indicated by the **Extended Index** register to be read and written. The value of this register is the value of the register selected by the **Extended Index** register.

10.7.1 Extension Control 1

Register Name: Extension Control 1				Register Per: socket			
Index: 2Fh		Extended Index: 03h		Register Compatibility Type: ext.			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Pull-Up Control	Invert Management IRQ Output	Invert Card IRQ Output	LED Activity Enable	Auto Power Clear	V _{CC} Power Lock
RW:00		RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: V_{CC} Power Lock

0	The V _{CC} Power bit (bit 4 of Power Control register) is not locked.
1	The V _{CC} Power bit (bit 4 of Power Control register) cannot be changed by software.

This bit can be used to prevent card drivers from overriding the Socket Services' task of controlling power to the card, thus preventing situations where cards are powered incorrectly.

Bit 1: Auto Power Clear

0	The V _{CC} Power bit (bit 4 of Power Control register) is reset to '0' when the card is removed.
1	The V _{CC} Power bit (bit 4 of Power Control register) is not affected by card removal.

Bit 2: LED Activity Enable

0	LED activity disabled.
1	LED activity enabled.

This bit allows the LED_OUT* pin to reflect any activity in the card. Whenever PCMCIA cycles are in process to or from a card in either socket, LED_OUT* will be active low.

Bit 3: Invert Card IRQ Output

0	The card IRQ is active-high.
1	The card IRQ is active-low and open-drain.

This bit changes the active-high, ISA-type card IRQ level to an active-low, open-collector output that complies with PCI bus requirements.

Bit 4: Invert Management IRQ Output

0	The management IRQ is active-high.
1	The management IRQ is active-low and open-drain.

This bit changes the active-high, ISA-type management IRQ level to an active-low, open-collector output that complies with PCI bus requirements.

Bit 5: Pull-Up Control

0	Pull-ups on VS2, VS1, CD2, and CD1 are in use.
1	Pull-ups on VS2, VS1, CD2, and CD1 are turned off.

This bit turns off the pull-ups on VS2, VS1, CD2, and CD1. Turning off these pull-ups can be used in addition to Suspend mode to even further reduce power when cards are inserted but no card accessibility is required. Even though power may or may not still be applied, all pull-ups and their associated inputs will be disabled.

NOTE: Setting GPSTB I/O Write* or GPSTB I/O Read* bit to '1' forces the VS2 and VS1 pull-ups to be turned off for that socket (see Section 10.7.5 and Section 10.7.6), independent of the setting of Pull-Up Control bit.

Note that insertion or removal of a card cannot be determined when this bit is set to a '1'. Also, when a card is already in the socket, a card detect interrupt will be generated when this bit is changed from a '0' to '1'.

10.7.2 System Memory Map 0-4 Upper Address

Register Name: System Memory Map 0-4						Register Per: socket	
Upper Address						Register Compatibility Type: ext.	
Index: 2Fh				Extended Index: 05h-09h			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Upper Address							
RW:00000000							

These bits are used in comparing PCI Address bits 31-24 for each memory window (0-4). These bits are used in conjunction with the **System Memory Map 0-4 Start Address** and **System Memory Map 0-4 End Address** registers.

10.7.3 External Data (Index 2Fh¹)

Register Name: External Data						Register Per: socket	
Index: 2Fh						Register Compatibility Type: ext.	
Extended Index: 0Ah							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
External Data (Phase 2 IRQ12)	External Data (Phase 2 IRQ11)	External Data (Phase 2 IRQ10)	External Data (Phase 2 IRQ9)	External Data (Phase 1 IRQ12)	External Data (Phase 1 IRQ11)	External Data (Phase 1 IRQ10)	External Data (Phase 1 IRQ9)
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bits 7-0: External Data

These bits hold data for I/O reads and writes. This register is updated and accessed according to the setting of bits 3 and 4 of **Extension Control 2** register.

10.7.4 External Data (Index 6Fh¹)

Register Name: External Data						Register Per: socket	
Index: 6Fh						Register Compatibility Type: ext.	
Extended Index: 0Ah							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Socket B VS2 Input	Socket B VS1 Input	Socket A VS2 Input	Socket A VS1 Input
RW:0000				R:0	R:0	R:0	R:0

Bits 3-0: Socket A/B VS1/VS2 Input

These bits indicate the values of the four voltage sense pins (two for each socket). These values are used to determine the operating voltage capabilities of an inserted card.

¹ **External Data** register (extended index 0Ah) functionality varies depending on if index 2Fh or 6Fh is accessed.

10.7.5 Extension Control 2 (Index 2Fh¹)

<i>Register Name: Extension Control 2</i>				<i>Register Per: socket</i>			
<i>Index: 2Fh</i>				<i>Extended Index: 0Bh</i>		<i>Register Compatibility Type: ext.</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
<i>Reserved</i>			<i>GPSTB I/O Write*</i>	<i>Reserved</i>			
<i>RW:000</i>			<i>RW:0</i>	<i>RW:0000</i>			

Bit 4: GPSTB I/O Write*

0	A_VS1/GPSTB1 and A_VS2/GPSTB2 pins (socket A) are used as voltage sense.
1	A_VS1/GPSTB1 and A_VS2/GPSTB2 pins are used to strobe I/O writes on IRQ[12:9].

Note that setting this bit forces the pull-ups on A_VS1/GPSTB1 and A_VS2/GPSTB2 to be off, independent of the setting of the Pull-Up Control bit (index 2Fh, extended index 03h, bit 5).

10.7.6 Extension Control 2 (Index 6Fh¹)

<i>Register Name: Extension Control 2</i>				<i>Register Per: socket</i>			
<i>Index: 6Fh</i>				<i>Extended Index: 0Bh</i>		<i>Register Compatibility Type: ext.</i>	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
<i>Reserved</i>			<i>GPSTB I/O Read*</i>	<i>Reserved</i>			
<i>RW:0000</i>			<i>RW:0</i>	<i>RW:000</i>			

Bit 3: GPSTB I/O Read*

0	B_VS1/GPSTB1 and B_VS2/GPSTB2 pins (socket B) are used as voltage sense.
1	B_VS1/GPSTB1 and B_VS2/GPSTB2 pins are used to strobe I/O reads on IRQ[12:9].

Note that setting this bit forces the pull-ups on B_VS1/GPSTB1 and B_VS2/GPSTB2 to be off, independent of the setting of the Pull-Up Control bit (index 6Fh, extended index 03h, bit 5).

¹ Extension Control 2 register (extended index 0Bh) functionality varies depending on if index 2Fh or 6Fh is accessed.

11. TIMING REGISTERS

The following information about the timing registers is important:

- All timing registers take effect immediately and should only be changed when the FIFO is empty (see the **FIFO Control** register on page 59).
- Selection of Timer Set 0 or Timer Set 1 register sets is controlled by **I/O Window Control**, bits 3 and 7 (see page 48).

11.1 Setup Timing 0-1

Register Name: Setup Timing 0-1						Register Per: socket	
Index: 3Ah, 3Dh						Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Setup Prescalar Select		Setup Multiplier Value					
RW:00		RW:000001					

There are two separate Setup Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Setup Timing
3Ah	Setup Timing 0
3Dh	Setup Timing 1

The Setup Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) setup time will be, in terms of the number of internal clock cycles.

The overall command setup timing length S is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command setup timing length according to the following formula:

$$S = (N_{pres} \times N_{val}) + 1$$

The value of S , representing the number of clock cycles¹ for command setup, is then multiplied by the clock period to determine the actual command setup time (see Section 13.3.3 for further discussion).

Bits 5-0: Setup Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length of setup time before a command becomes active.

Bits 7-6: Setup Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Setup Multiplier Value (bits 5-0) to control the length of setup time before a command becomes active.

¹ The internal clock period is the same as PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '0', and it is double the PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '1'.

11.2 Command Timing 0-1

Register Name: Command Timing 0-1				Register Per: socket			
Index: 3Bh, 3Eh				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command Prescalar Select		Command Multiplier Value					
RW:00		RW:000101/010100 ^a					

^a Timing set 0 (index 3Bh) resets to 05h for socket timing equal to 250-ns PCMCIA card timing. Timing set 1 (3Eh) resets to 14h for socket timings equal to 600-ns PCMCIA card timing.

There are two separate Command Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Command Timing
3Bh	Command Timing 0
3Eh	Command Timing 1

The Command Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) active time will be, in terms of the number of internal clock cycles.

The overall command timing length C is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command timing length according to the following formula:

$$C = (N_{pres} \times N_{val}) + 1$$

The value of C , representing the number of clock cycles¹ for a command, is then multiplied by the clock period to determine the actual command active time (see Section 13.3.3 for further discussion).

Bits 5-0: Command Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length that a command is active.

Bits 7-6: Command Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Command Multiplier Value (bits 5-0) to control the length that a command is active.

¹ The internal clock period is the same as PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '0', and it is double the PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '1'.

11.3 Recovery Timing 0-1

Register Name: Recovery Timing 0-1						Register Per: socket	
Index: 3Ch, 3Fh						Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Recovery Prescalar Select		Recovery Multiplier Value					
RW:00		RW:000000					

There are two separate Recover Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Recovery Timing
3Ch	Recovery Timing 0
3Fh	Recovery Timing 1

The Recovery Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) recovery time will be, in terms of the number of internal clock cycles.

The overall command recovery timing length R is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command recovery timing length according to the following formula:

$$R = (N_{pres} \times N_{val}) + 1$$

The value of R, representing the number of clock cycles¹ for command recovery, is then multiplied by the clock period to determine the actual command recovery time (see Section 13.3.3 for further discussion).

Bits 5-0: Recovery Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length of recovery time after a command is active.

Bits 7-6: Recovery Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Recovery Multiplier Value (bits 5-0) to control the length of recovery time after a command is active.

¹ The internal clock period is the same as PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '0', and it is double the PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '1'.

12. ATA MODE OPERATION

The CL-PD6729 card interfaces can be dynamically configured to support a PCMCIA-compatible ATA disk interface (commonly known as 'IDE') instead of the standard PCMCIA card interface. Disk drives that can be made mechanically-compatible with PCMCIA card dimensions can thus operate through the socket using the ATA electrical interface.

Configuring a socket to support ATA operation changes the function of certain card socket signals to support the needs of the ATA disk interface. Table 12-1 lists each interface pin and its function when a CL-PD6729 card socket is operating in ATA mode.

All register functions of the CL-PD6729 are available in ATA mode, including socket power control, interface signal disabling, and card window control. No memory operations are allowed in ATA mode.

Table 12-1. ATA Pin Cross-Reference

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
1	Ground	Ground
2	D3	D3
3	D4	D4
4	D5	D5
5	D6	D6
6	D7	D7
7	-CE1	CS0*
8	A10	n/c
9	-OE	Always low
10	A11	n/c
11	A9	CS1*
12	A8	n/c
13	A13	n/c
14	A14	n/c
15	-WE	n/c
16	-IREQ	IREQ
17	VCC	VCC
18	VPP1	n/c
19	A16	n/c
20	A15	n/c
21	A12	n/c

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
35	Ground	Ground
36	-CD1	-CD1
37	D11	D11
38	D12	D12
39	D13	D13
40	D14	D14
41	D15	D15
42	-CE2	CS1*
43	VS1	VS1
44	-IORD	-IORD
45	-IOWR	-IOWR
46	A17	n/c
47	A18	n/c
48	A19	n/c
49	A20	n/c
50	A21	n/c
51	VCC	VCC
52	VPP2	n/c
53	A22	n/c
54	A23	VU
55	A24	M/S*

Table 12-1. ATA Pin Cross-Reference (cont.)

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
22	A7	n/c
23	A6	n/c
24	A5	n/c
25	A4	n/c
26	A3	n/c
27	A2	A2
28	A1	A1
29	A0	A0
30	D0	D0
31	D1	D1
32	D2	D2
33	-IOIS16	-IOIS16
34	Ground	Ground

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
56	A25	CSEL
57	VS2	VS2
58	RESET	RESET*
59	-WAIT	IOCHRDY
60	-INPACK	DREQ ^a
61	-REG	DACK* ^a
62	-SPKR	LED*
63	-STSCHG	PDIAG* ^a
64	D8	D8
65	D9	D9
66	D10	D10
67	-CD2	-CD2
68	Ground	Ground

^a Not supported by the CL-PD6729.

13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Description	Absolute Maximum Rating ^a
Ambient temperature under bias	0°C to 70°C
Storage temperature	-65°C to 150°C
Voltage on any pin (with respect to ground)	-0.3 volts to 0.3 volts greater than voltage of the +5V pin, respective to ground
Operating power dissipation	500 mW
Power dissipation during Suspend mode	10 mW
Power supply voltage	7 volts
Injection current (latch up)	25 mA

^a Stresses above those listed may cause permanent damage to system components. These are stress ratings only; functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect system reliability.

13.2 DC Specifications

Table 13-1. General DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
C _{IN}	Input capacitance		10.0	pF	
C _{OUT}	Output capacitance		10.0	pF	
I _{IL}	Input leakage	-10.0	10.0	μA	0 < V _{IN} < respective V _{CC} supply pin
I _{PU}	Internal pull-up current	-30	-400	μA	

Table 13–2. PCMCIA Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
SOCKET_VCC _{5V}	Power supply voltage	4.5	5.5	V	Normal operation
SOCKET_VCC _{3V}		3.0	3.6	V	
V _{IH}	Input high voltage	2.0		V	V _{DD} core voltage = 3.0V, Misc Control 2 register, bit 3 = '0'
		2.0		V	V _{DD} core voltage = 4.5V, Misc Control 2 register, bit 3 = '1'
V _{IL}	Input low voltage		0.8	V	V _{DD} core voltage = 3.6V, Misc Control 2 register, bit 3 = '0'
			0.8	V	V _{DD} core voltage = 5.5V, Misc Control 2 register, bit 3 = '1'
V _{IHC}	Input high voltage CMOS	0.7 V _{DD}		V	V _{DD} core voltage = 4.5V, Misc Control 2 register, bit 3 = '0'
V _{ILC}	Input low voltage CMOS		0.2 V _{DD}	V	V _{DD} core voltage = 5.5V, Misc Control 2 register, bit 3 = '0'
V _{OH}	Output high voltage	2.4		V	At rated I _{OH} , respective SOCKET_VCC = 3.0V
V _{OHC}	Output high voltage CMOS	SOCKET_VCC – 0.5		V	At rated I _{OHC} , respective SOCKET_VCC = 3.0V
V _{OL}	Output low voltage		0.4	V	At rated I _{OL}
I _{OH}	Output high current	–2		mA	Respective SOCKET_VCC = 3.0V, V _{OH} = 2.4V
I _{OHC}	Output high current CMOS	–1		mA	Respective SOCKET_VCC = 3.0V, V _{OHC} = SOCKET_VCC – 0.5V
I _{OL}	Output low current	2		mA	Respective SOCKET_VCC = 3.0V, V _{OL} = 0.4V

Table 13–3. PCI Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
PCI_VCC _{5V}	Power supply voltage	4.5	5.5	V	Normal operation
PCI_VCC _{3V}		3.0	3.6	V	
V _{IH} ^a	Input high voltage	2.0		V	V _{DD} core voltage = 3.0V
V _{IL} ^a	Input low voltage		0.8	V	V _{DD} core voltage = 3.6V
V _{IHC} ^a	Input high voltage CMOS	0.7 V _{DD} ^b		V	V _{DD} core voltage = 4.5V
V _{ILC} ^a	Input low voltage CMOS		0.2 V _{DD} ^b	V	V _{DD} core voltage = 5.5V
V _{OH}	Output high voltage	2.4		V	At rated I _{OH} , PCI_VCC = 3.0V
V _{OHC}	Output high voltage CMOS	PCI_VCC – 0.5		V	At rated I _{OHC} , PCI_VCC = 3.0V
V _{OL}	Output low voltage		0.5	V	At rated I _{OL}
I _{OH}	Output current high	–5		mA	PCI_VCC = 3.0V, V _{OH} = 2.4V
I _{OHC}	Output current high CMOS	–1		mA	PCI_VCC = 3.0V, V _{OHC} = PCI_VCC – 0.5V
I _{OL}	Output current low	16		mA	PCI_VCC = 3.0V, V _{OL} = 0.5V

^a When CORE_VDD is 3.3V, input thresholds are TTL-compatible; when CORE_VDD is 5V, input thresholds are CMOS-compatible.

^b The value of the input threshold level is dependent on the voltage applied to the CORE_VDD pin of the CL-PD6729.

Table 13-4. Power Control Interface (+5V Powered) DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
+5V	+5V supply voltage	Highest $V_{CC} - 0.3$	5.5	V	
V_{IH}	Input high voltage	2.0		V	+5V pin voltage = 4.5V
V_{IL}	Input low voltage		0.8	V	+5V pin voltage = 5.5V
V_{OH}	Output high voltage	2.4		V	+5V pin voltage = 4.5V, $I_{OH} = -5$ mA
V_{OHC}	Output high voltage CMOS	+5V volt- age - 0.5		V	+5V pin voltage = 4.5V, $I_{OH} = -1$ mA
V_{OL}	Output low voltage		0.4	V	
I_{OH}	Output current high	-5		mA	Respective +5V pin voltage = 4.5V, $V_{OH} = 2.4$ V
I_{OHC}	Output current high CMOS	-1		mA	Respective +5V pin voltage = 4.5V, $V_{OHC} = +5$ V pin voltage - 0.5V
I_{OL}	Output current low	16		mA	Respective +5V pin voltage = 4.5V, $V_{OL} = 0.4$ V

Table 13–5. Operating Current Specifications (3.3V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$I_{CC_{tot}(1)}$	Power supply current, operating	tbd	tbd	tbd	mA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P _{DISS} = < 85 mW
$I_{CC_{tot}(2)}$	Power supply current, Suspend mode (Misc Control 2, bit 2 = '1')		tbd		μA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P _{DISS} = < 2 mW
$I_{CC_{tot}(3)}$	Power supply current, RST# active, no clocks		tbd		μA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P _{DISS} = < 1 mW

Table 13–6. Operating Current Specifications (5.0V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$I_{CC_{tot}(1)}$	Power supply current, operating	tbd	tbd	tbd	mA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$I_{CC_{tot}(2)}$	Power supply current, Suspend mode (Misc Control 2, bit 2 = '1')		tbd		μA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$I_{CC_{tot}(3)}$	Power supply current, RST# active, no clocks		tbd		μA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V.

13.3 AC Timing Specifications

This section includes system timing requirements for the CL-PD6729. Unless otherwise specified, timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0°C to 70°C, and V_{CC} varying from 3.0V to 3.6V or 4.5V to 5.5V DC. The PCI bus speed is 33 MHz unless otherwise specified. Note the following conventions:

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PCMCIA bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6729.

Additionally, the following statements are true for all timing information:

- All timings assume a load of 50 pF.
- TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

Table 13–7. Index of AC Timing Specifications

Title	Page Number
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13.3.1 PCI Bus Timing
Table 13–8. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL#

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t ₁	FRAME# setup to PCI_CLK	7	–	7	–	ns
t ₂	AD[31:0] (address) setup to PCI_CLK	7	–	7	–	ns
t ₃	AD[31:0] (address) hold from PCI_CLK	0	–	0	–	ns
t ₄	AD[31:0] (data) setup to PCI_CLK	7	–	7	–	ns
t ₅	AD[31:0] (data) active to HI-Z from PCI_CLK	0	28	0	28	ns
t ₆	C/BE[3:0]# (bus command) setup to PCI_CLK	7	–	7	–	ns
t ₇	C/BE[3:0]# (bus command) hold from PCI_CLK	0	–	0	–	ns
t ₈	C/BE[3:0]# (byte enable) setup to PCI_CLK	7	–	7	–	ns
t ₉	DEVSEL# delay from PCI_CLK	–	11	–	11	ns
t ₁₀	DEVSEL# high before HI-Z	1	–	1	–	PCI_CLK

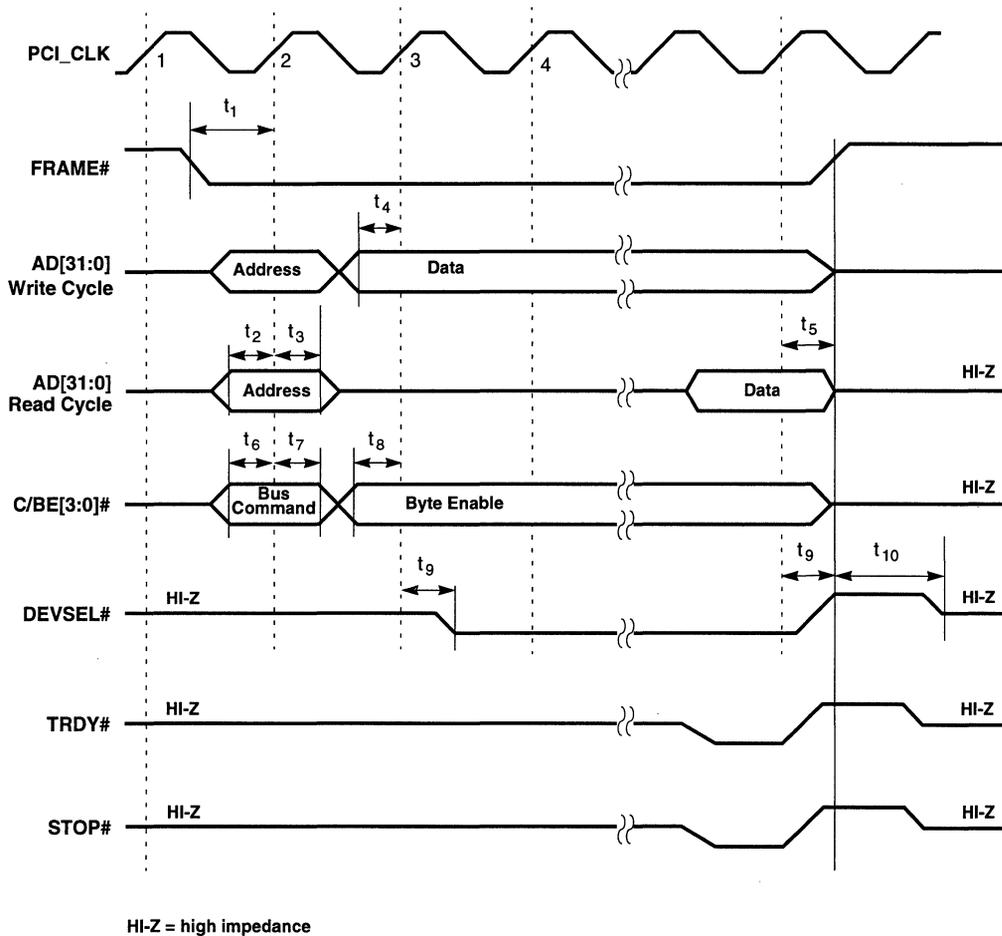


Figure 13-1. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL# (PCI™ Bus)

Table 13–9. TRDY# and STOP# Delay

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t_1	TRDY# active delay from PCI_CLK	–	11	–	11	ns
t_2	TRDY# inactive delay from PCI_CLK	–	11	–	11	ns
t_3	TRDY# high before HI-Z	1	–	1	–	PCI_CLK
t_4	STOP# active delay from PCI_CLK	–	11	–	11	ns
t_5	STOP# inactive delay from PCI_CLK	–	11	–	11	ns
t_6	STOP# high before HI-Z	1	–	1	–	PCI_CLK

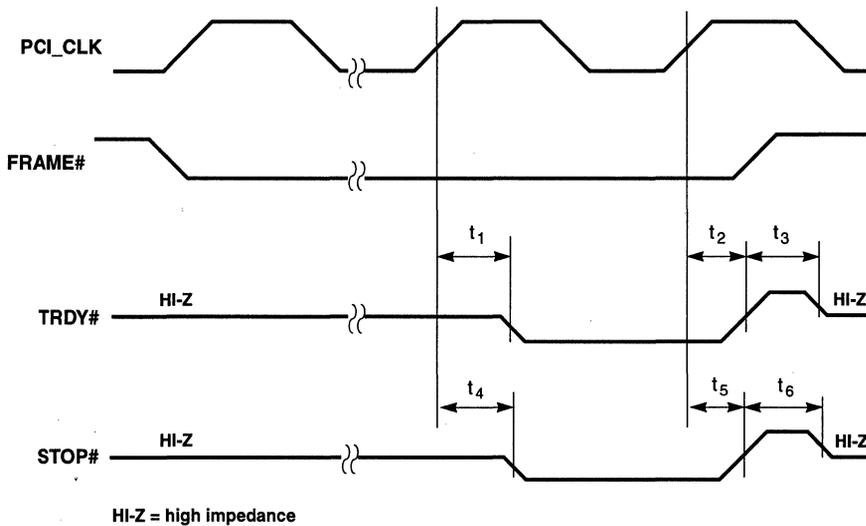

Figure 13–2. TRDY# and STOP# Delay (PCI™ Bus)

Table 13–10. IDSEL Timing in a Configuration Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to PCI_CLK	7	–	ns
t_2	IDSEL hold from PCI_CLK	0	–	ns

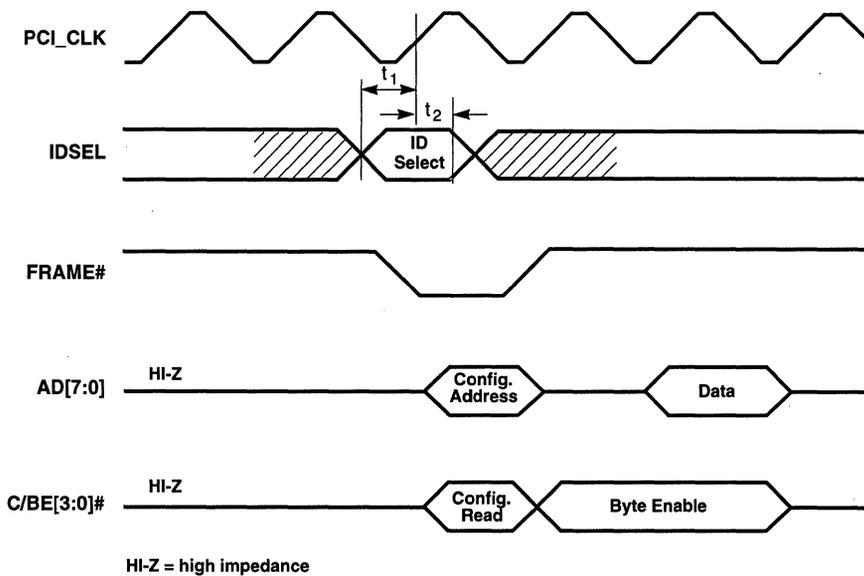
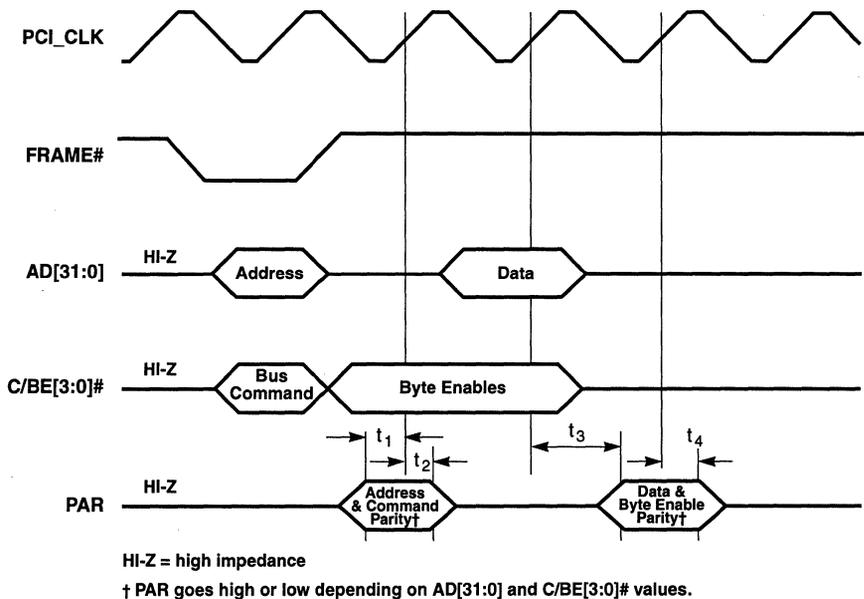


Figure 13–3. IDSEL Timing in a Configuration Cycle (PCI™ Bus)

Table 13–11. PAR Timing

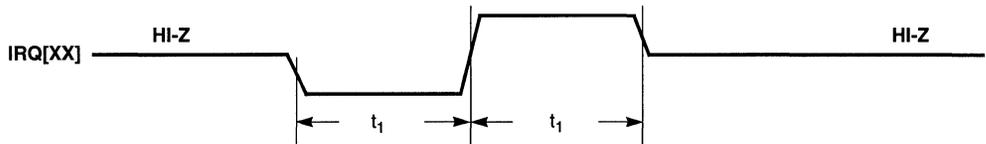
Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup to PCI_CLK (input to CL-PD6729)	7	–	ns
t_2	PAR hold from PCI_CLK (input to CL-PD6729)	0	–	ns
t_3	PAR valid delay from PCI_CLK (output from CL-PD6729)	–	11	ns
t_4	PAR hold from PCI_CLK (output from CL-PD6729)	0	–	ns


Figure 13–4. PAR Timing (PCI™ Bus)

13.3.2 System Interrupt Timing

Table 13–12. Pulse Mode Interrupt Timing

Symbol	Parameter	MIN	MAX	Units
t_1	IRQ[XX] low or high	4	4	PCI_CLK



HI-Z = high impedance

NOTE: Each time indicated is 4 PCI clocks or 4 external clocks, independent of setting of the Timer Clock Divide bit.

Figure 13–5. Pulse Mode Interrupt Timing

13.3.3 PCMCIA Bus Timing Calculations

Calculations for minimum PCMCIA cycle Setup, Command, and Recovery timings are made by first calculating factors derived from the applicable timer set's timing registers and then by applying the factor to an equation relating it to the internal clock period.

The PCMCIA cycle timing factors, in terms of the number of internal clocks¹, are calculated as follows:

$$S = (N_{pres} \times N_{val}) + 1$$

$$C = (N_{pres} \times N_{val}) + 1$$

$$R = (N_{pres} \times N_{val}) + 1$$

N_{pres} and N_{val} are the specific selected prescaler and multiplier value from the timer set's Setup, Command, and Recovery Timing registers (see Chapter 11 for description of these registers).

From this, a PCMCIA cycle's Setup, Command, and Recovery time for the selected timer set are calculated as follows:

$$\text{Minimum Setup time} = (S \times T_{cp}) - 10 \text{ ns}$$

$$\text{Minimum Command time} = (C \times T_{cp}) - 10 \text{ ns}$$

$$\text{Minimum Recovery time} = (R \times T_{cp}) - 10 \text{ ns}$$

T_{cp} is the period of the internal clock.

If PCI_CLK is selected (**Misc Control 2** register bit 0 is a '0') and operates at 25 MHz, and the clock input is not being divided (**Misc Control 2** register bit 4 is a '0'), then:

$$T_{cp} = 40 \text{ ns}$$

The timing diagrams that follow were derived for a CL-PD6729 using the PCI clock at 25 MHz. The examples are for the default values of the Timing registers for Timer Set 0, as follows:

Timing Register Name (Timer Set 0)	Index	Value (Default)	Resultant N_{pres}	Resultant N_{val}
Setup Timing 0	3Ah	01h	1	1
Command Timing 0	3Bh	05h	1	8
Recovery Timing 0	3Ch	00h	1	0

Thus the minimum times for the default values are as follows:

$$\text{Minimum Setup time} = (S \times T_{cp}) - 10 \text{ ns} = \{[(1 \times 1) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{70 \text{ ns}}$$

$$\text{Minimum Command time} = (C \times T_{cp}) - 10 \text{ ns} = \{[(1 \times 5) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{230 \text{ ns}}$$

$$\text{Minimum Recovery time} = (R \times T_{cp}) - 10 \text{ ns} = \{[(1 \times 0) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{30 \text{ ns}}$$

¹ The internal clock period is the same as PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '0', and it is double the PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '1'.

13.3.4 PCMCIA Bus Timing

Table 13-13. Memory Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG, -CE[2:1], Address, and Write Data setup to Command active ¹	$(S \times Tcp) - 10$		ns
t_2	Command pulse width ²	$(C \times Tcp) - 10$		ns
t_3	Address hold and Write Data valid from Command inactive ³	$(R \times Tcp) - 10$		ns
t_4	-WAIT active from Command active		$(C - 2)Tcp - 10$	ns
t_5	Command hold from -WAIT inactive	$2 Tcp$		ns
t_6	Data setup before -OE inactive	$(2 Tcp) + 10$		ns
t_7	Data hold after -OE inactive	0		ns
t_8	Data valid from -WAIT inactive	$Tcp + 10$		ns

¹ The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. $S = (N_{pres} \times N_{val} + 1)$, see page 84.

² The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. $C = (N_{pres} \times N_{val} + 1)$, see page 84.

³ The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. $R = (N_{pres} \times N_{val} + 1)$, see page 84.

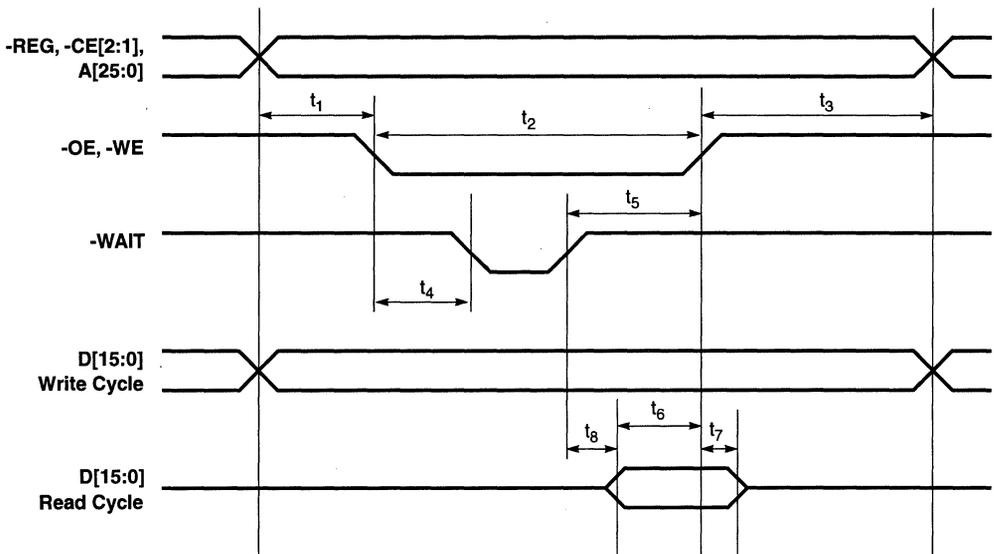


Figure 13-6. Memory Read/Write Timing

Table 13–14. Word I/O Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active ¹	$(S \times T_{cp}) - 10$		ns
t_2	Command pulse width ²	$(C \times T_{cp}) - 10$		ns
t_3	Address hold and Write Data valid from Command inactive ³	$(R \times T_{cp}) - 10$		ns
t_{ref}	Card -IOIS16 delay from valid Address (PCMCIA card specification)		35	ns
t_4	-IOIS16 setup time before Command end	$(3 T_{cp}) + 10$		ns
t_5	-CE2 delay from -IOIS16 active ⁴	$T_{cp} - 10$		ns
t_6	Data setup before -IOR inactive	$(2 T_{cp}) + 10$		ns
t_7	Data hold after -IOR inactive	0		ns

¹ The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. $S = (N_{pres} \times N_{val} + 1)$, see page 84.

² The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. $C = (N_{pres} \times N_{val} + 1)$, see page 84.

³ The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. $R = (N_{pres} \times N_{val} + 1)$, see page 84.

⁴ -IOIS16 must go low within $3T_{cp} + 10$ ns of the cycle beginning or -IOIS16 will be ignored and -CE will not be activated.

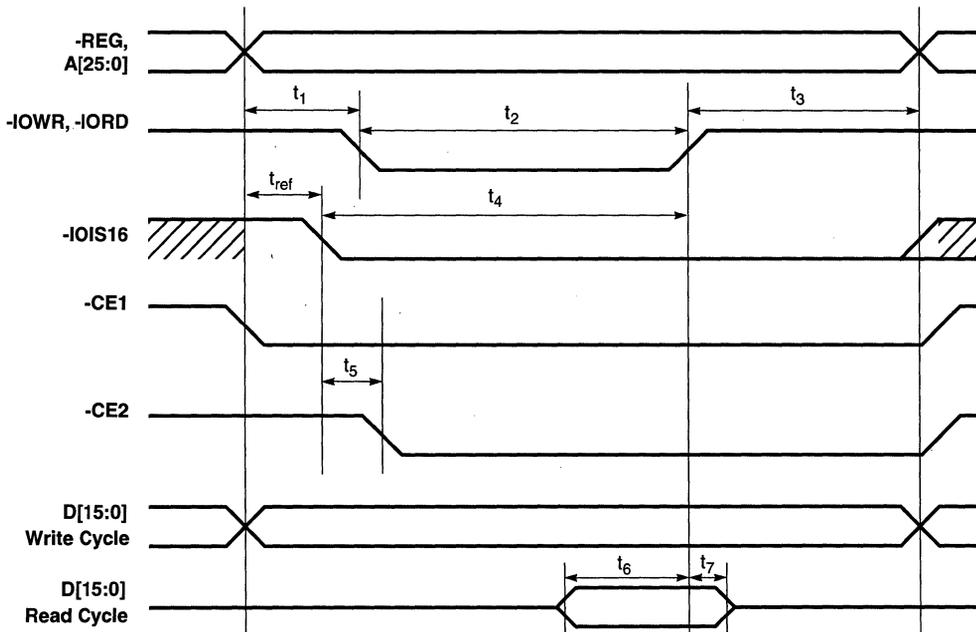

Figure 13–7. Word I/O Read/Write Timing

Table 13–15. PCMCIA Read/Write Timing when System is 8-Bit

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active ¹	$(S \times T_{cp}) - 10$		ns
t_2	Command pulse width ²	$(C \times T_{cp}) - 10$		ns
t_3	Address hold from Command inactive ³	$(R \times T_{cp}) - 10$		ns
t_4	Data setup before Command inactive	$(2 T_{cp}) + 10$		ns
t_5	Data hold after command inactive	0		ns

¹ The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. $S = (N_{pres} \times N_{val} + 1)$, see page 84.

² The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. $C = (N_{pres} \times N_{val} + 1)$, see page 84.

³ The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. $R = (N_{pres} \times N_{val} + 1)$, see page 84.

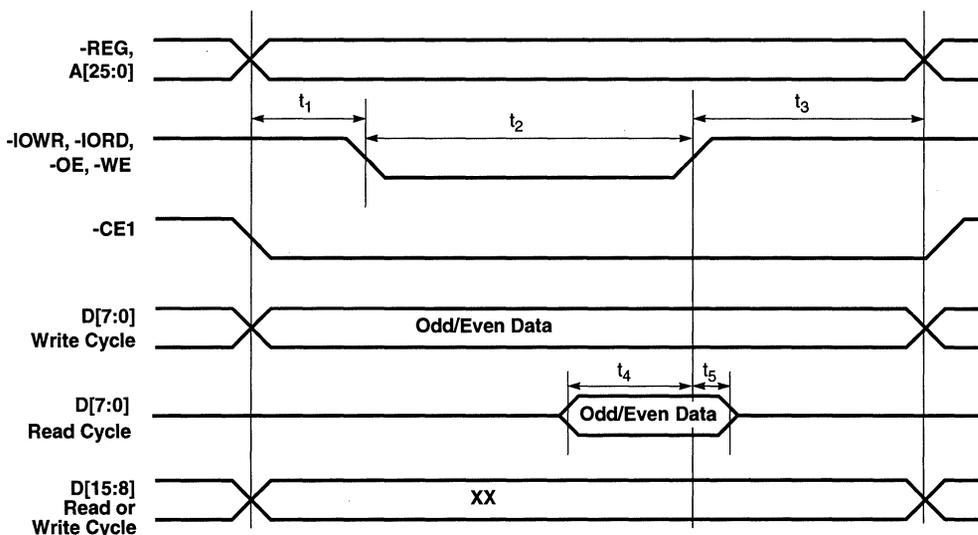


Figure 13–8. PCMCIA Read/Write Timing when System is 8 Bit (SBHE Tied High)

Table 13–16. Normal Byte Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address setup to Command active ¹	$(S \times T_{cp}) - 10$		ns
t_2	Command pulse width ²	$(C \times T_{cp}) - 10$		ns
t_3	Address hold from Command inactive ³	$(R \times T_{cp}) - 10$		ns

¹ The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. $S = (N_{pres} \times N_{val} + 1)$, see page 84.

² The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. $C = (N_{pres} \times N_{val} + 1)$, see page 84.

³ The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. $R = (N_{pres} \times N_{val} + 1)$, see page 84.

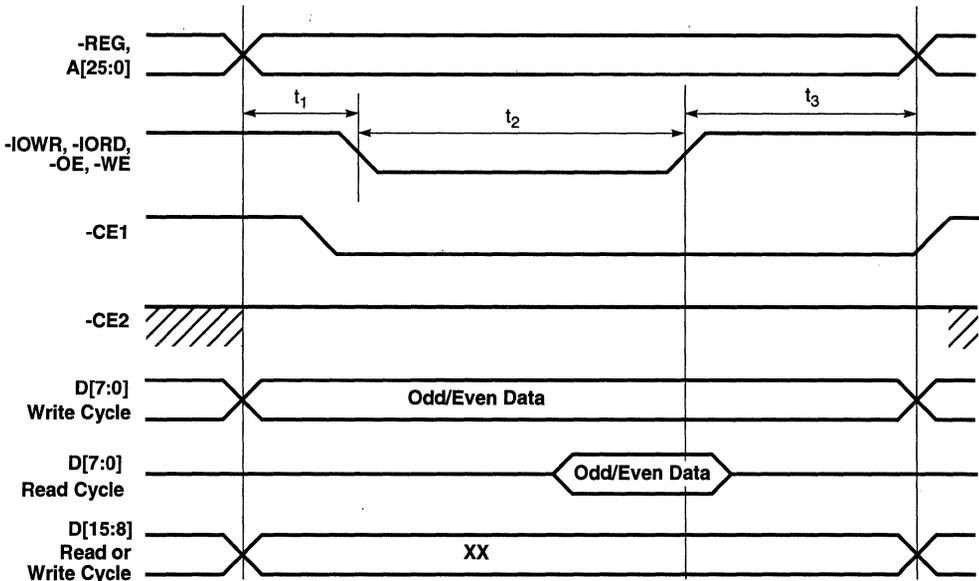

Figure 13–9. Normal Byte Read/Write Timing (that is, all other byte accesses, including odd I/O cycles where -IOIS16 is low)

Table 13–17. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address change to -IOIS16 inactive ⁴		$(3T_{cp}) + 10$	ns
t_2	-IOIS16 inactive to -CE2 inactive		20	ns
t_3	-IOIS16 inactive to -CE1 active		20	ns
t_4	Address setup to Command active ¹	$(S \times T_{cp}) - 10$		ns
t_5	Command pulse width ²	$(C \times T_{cp}) - 10$		ns
t_6	Address hold from Command inactive ³	$(R \times T_{cp}) - 10$		ns

¹ The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. $S = (N_{pres} \times N_{val} + 1)$, see page 84.
² The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. $C = (N_{pres} \times N_{val} + 1)$, see page 84.
³ The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. $R = (N_{pres} \times N_{val} + 1)$, see page 84.
⁴ -IOIS16 level from card must be valid within 3 clocks of an address change to the card.

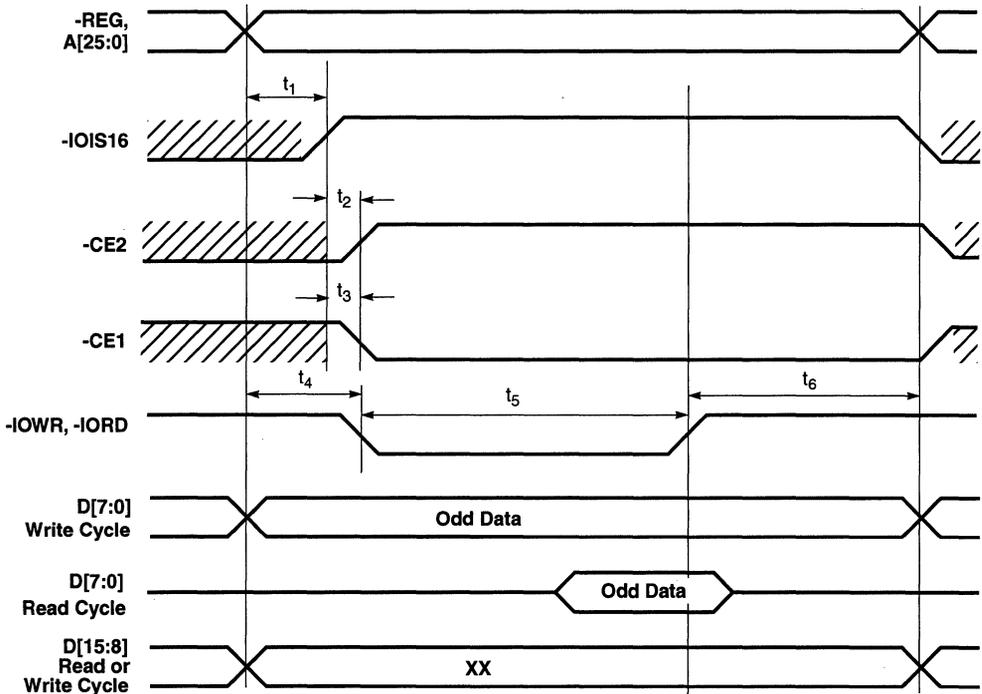
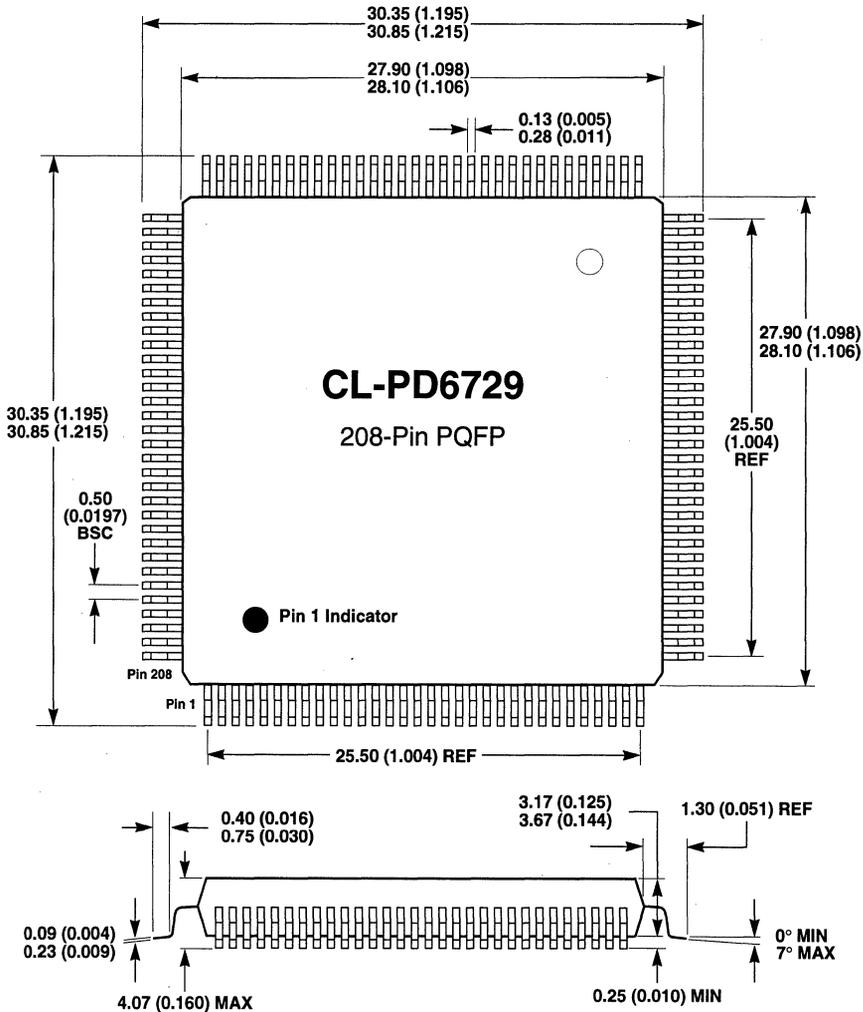


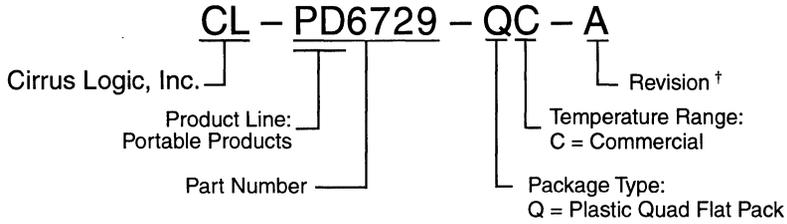
Figure 13–10. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

14. PACKAGE DIMENSIONS

NOTES:

- 1) Dimensions are in millimeters (inches), and the controlling dimension is millimeter.
- 2) Drawing above does not reflect exact package pin count.
- 3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

15. ORDERING INFORMATION

The order number for the part is:



† Contact Cirrus Logic for up-to-date information on revisions.

Notes

Appendix A

Using the Cirrus Logic BBS

Cirrus Logic maintains a BBS (bulletin board service) 24 hours a day for customers to obtain up-to-date files and information. For the CL-PD6729, the BBS gives access to utilities, schematics, and software upgrades.

Cirrus Logic strictly controls access to this BBS. All downloadable files are checked by Cirrus Logic and customers cannot upload files to any publicly downloadable area.

Follow the steps that follow to download files. If you would like access to more restricted files, or would like to exchange files with Cirrus Logic personnel on a regular basis, contact your Cirrus Logic representative to obtain expanded access privileges.

1. Set your communication parameters as follows:

- 8 data bits
- No parity
- 1 stop bit
- Baud rate up to 14,400 bps

2. Dial the Cirrus Logic BBS at (510) 440-9080.

3. When connected, do one of the following:

- Enter your name and password. First-time users can establish an account by entering a name and password and completing the questionnaire.
- Or, follow the instructions to log on as a 'guest'.

4. Select [J] Join Product Area.

5. Select [19] 67XX.

6. Select [F] File Menu.

7. You can now choose among the options for the CL-PD6729.

Many BBS files are compressed in a 'zipped' file format (using PKZIP.EXE version 2.04G). These files have the suffix .ZIP appended to their names. They need to be uncompressed after downloading using PKUNZIP.EXE. If you do not have this 'unzip' utility, you can download it in a self-extracting form from the Cirrus Logic BBS — from any area, download the file called PKZ204G.EXE.

Notes

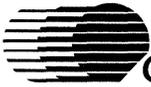
Appendix B

Summary of Register Tables

B.1 PCI-Configuration Registers

Page 25

Configuration Register Name: Vendor ID and Device ID							
Offset: 00h							
Register Per: chip							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Device ID (high)				Device ID (high)			
R:00010001							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Byte 2 Device ID (low)				Device ID (low)			
R:00000000							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Byte 1 Vendor ID (high)				Vendor ID (high)			
R:00010000							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0 Vendor ID (low)				Vendor ID (low)			
R:00010011							



Configuration Register Name: Command and Status							
Offset: 04h							
Register Per: chip							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Status (high)	Address/Data Parity Error Detected	System Error (SERR#) Generated	Reserved		DEVSEL# Timing		Master Data Parity Error Reported
	RW:0	RW:0	R:XXX		R:01		R:0
Byte 2 Status (low)	Reserved						
	R:XXXXXXXX						
Byte 1 Command (high)	Reserved						System Error (SERR#) Enable
	R:XXXXXXXX						RW:0
Byte 0 Command (low)	Wait Cycle Enable	Parity Error Check/Report Enable	Reserved			PCI Memory Space Enable	PCI I/O Space Enable
	R:1	RW:0	R:XXXX			RW:0	RW:0

Configuration Register Name: Revision ID and Class Code							
Offset: 08h							
Register Per: chip							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 Class Code (high)	Class Code (high)						
	R:00000110						
Byte 2 Class Code (mid.)	Class Code (mid.)						
	R:00000101						
Byte 1 Class Code (low)	Class Code (low)						
	R:00000000						
Byte 0 Revision ID	Revision ID						
	R:nnnnnnn ^a						

^a This read-only value depends on the revision level of the CL-PD6729.

Configuration Register Name: Cache Line Size, Latency Timer, Header Type, and BIST								Register Per: chip
Offset: 0Ch								
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	
Reserved								
R:XXXXXXXX								
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
Header Type								
R:10000000								
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
Reserved								
R:XXXXXXXX								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Reserved								
R:XXXXXXXX								

Configuration Register Name: Base Address 0								Register Per: chip
Offset: 10h								
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	
I/O Base Address (high)								
RW:00000000								
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
I/O Base Address (high mid.)								
RW:00000000								
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
I/O Base Address (low mid.)								
RW:00000000								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
I/O Base Address (low)						Reserved	I/O Space Indicator	
RW:000000						R:0	R:1	

Configuration Register Name: Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat								
Offset: 3Ch								
Register Per: chip								
Byte 3 Max_Lat	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Max_Lat								
R:00000000								
Byte 2 Min_Gnt	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved								
R:XXXXXXXX								
Byte 1 Interrupt Pin	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Interrupt Pin								
R:00000000								
Byte 0 Interrupt Line	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt Line								
RW:00000000								

B.2 Operation Registers

Register Name: Index							
Index: n/a							
Register Per: chip							
Register Compatibility Type: 365							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Socket Index	Register Index					
RW:0	RW:0	RW:000000					

Register Name: Data							
Index: n/a							
Register Per: chip							
Register Compatibility Type: 365							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data							

B.2.1 Device Control Registers

Register Name: Chip Revision				Register Per: chip			
Index: 00h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interface ID		0	0	Revision			
R:10		R:0	R:0	R:0010 ^a			

^a Value for the current stepping only.

Register Name: Interface Status				Register Per: socket			
Index: 01h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Card Power On	RDY Ready/Busy*	WP Write Protect	-CD2 Card Detect	-CD1	BVD2 Battery Voltage Detect	BVD1
R:1 ^a	R:0	R ^b	R ^c	R ^d		R ^e	

^a Bit 7 always reads a '1' on the CL-PD6729.

^b Bit 5 indicates the value of the RDY/-IREQ pin (see page 12).

^c Bit 4 indicates the value of the WP/-IOIS16 pin (see page 11).

^d Bits 3-2 indicate the inversion of the values of the -CD1 and -CD2 pins (see page 12).

^e Bits 1-0 indicate the values of the BVD1/-STSCHG/-RI and BVD2/-SPKR/-LED pins (see page 12).

Register Name: Power Control				Register Per: socket			
Index: 02h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Card Enable	Compatibility Bit	Auto-Power	V _{CC} Power	Compatibility Bits		V _{pp1} Power	
RW:0	RW:0	RW:0	RW:0	RW:00		RW:00	

Register Name: Interrupt and General Control				Register Per: socket			
Index: 03h				Register Compatibility Type: 365			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ring Indicate Enable	Card Reset*	Card Is I/O	Manage Int Enable	IRQ Level			
RW:0	RW:0	RW:0	RW:0	RW:0000			

Register Name: Card Status Change				Register Per: socket			
Index: 04h				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
0	0	0	0	Card Detect Change	Ready Change	Battery Warning Change	Battery Dead Or Status Change
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

Register Name: Management Interrupt Configuration				Register Per: socket			
Index: 05h				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Management IRQ				Card Detect Enable	Ready Enable	Battery Warning Enable	Battery Dead Or Status Change Enable
RW:0000				RW:0	RW:0	RW:0	RW:0

Register Name: Mapping Enable				Register Per: socket			
Index: 06h				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
I/O Map 1 Enable	I/O Map 0 Enable	Compatibility Bit	Memory Map 4 Enable	Memory Map 3 Enable	Memory Map 2 Enable	Memory Map 1 Enable	Memory Map 0 Enable
RW:0	RW:0	R:0	RW:0	RW:0	RW:0	RW:0	RW:0

B.2.2 I/O Window Mapping Registers

Register Name: I/O Window Control				Register Per: socket			
Index: 07h				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Timing Register Select 1	Compatibility Bit	Auto-Size I/O Window 1	I/O Window 1 Size	Timing Register Select 0	Compatibility Bit	Auto-Size I/O Window 0	I/O Window 0 Size
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Register Name: System I/O Map 0-1 Start Address Low				Register Per: socket			
Index: 08h, 0Ch				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Start Address 7-0							
RW:00000000							

Register Name: System I/O Map 0-1 Start Address High							Register Per: socket	
Index: 09h, 0Dh							Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Start Address 15-8								
RW:00000000								

Register Name: System I/O Map 0-1 End Address Low							Register Per: socket	
Index: 0Ah, 0Eh							Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
End Address 7-0								
RW:00000000								

Register Name: System I/O Map 0-1 End Address High							Register Per: socket	
Index: 0Bh, 0Fh							Register Compatibility Type: 365	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
End Address 15-8								
RW:00000000								

Register Name: Card I/O Map 0-1 Offset Address Low							Register Per: socket	
Index: 36h, 38h							Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Offset Address 7-1							0 ^a	
RW:00000000							RW:0	

^a This bit must be programmed to '0'

Register Name: Card I/O Map 0-1 Offset Address High							Register Per: socket	
Index: 37h, 39h							Register Compatibility Type: ext.	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Offset Address 15-8								
RW:00000000								

B.2.3 Memory Window Mapping Registers
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Register Name: System Memory Map 0-4 Start Address Low							<i>Register Per: socket</i>
<i>Index: 10h, 18h, 20h, 28h, 30h</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Start Address 19-12							
RW:00000000							

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Register Name: System Memory Map 0-4 Start Address High							<i>Register Per: socket</i>
<i>Index: 11h, 19h, 21h, 29h, 31h</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Window Data Size	Compatibility Bit	Scratchpad Bits		Start Address 23-20			
RW:0	RW:0	RW:00		RW:0000			

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Register Name: System Memory Map 0-4 End Address Low							<i>Register Per: socket</i>
<i>Index: 12h, 1Ah, 22h, 2Ah, 32h</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
End Address 19-12							
RW:00000000							

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Register Name: System Memory Map 0-4 End Address High							<i>Register Per: socket</i>
<i>Index: 13h, 1Bh, 23h, 2Bh, 33h</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Card Timer Select		Scratchpad Bits		End Address 23-20			
RW:00		RW:00		RW:0000			

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Register Name: Card Memory Map 0-4 Offset Address Low							<i>Register Per: socket</i>
<i>Index: 14h, 1Ch, 24h, 2Ch, 34h</i>							<i>Register Compatibility Type: 365</i>
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Offset Address 19-12							
RW:00000000							

Register Name: Card Memory Map 0-4 Offset Address High						<i>Register Per:</i> socket	
Index: 15h, 1Dh, 25h, 2Dh, 35h						<i>Register Compatibility Type:</i> 365	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Write Protect	REG Setting	Offset Address 25-20					
RW:0	RW:0	RW:000000					

B.2.4 Extension Registers

Register Name: Misc Control 1						<i>Register Per:</i> socket	
Index: 16h						<i>Register Compatibility Type:</i> ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Inpack Enable	Scratchpad Bits		Speaker Enable	Pulse System IRQ	Pulse Management Interrupt	V _{CC} 3.3V	Reserved
RW:0	RW:00		RW:0	RW:0	RW:0	RW:0	R:0

Register Name: FIFO Control						<i>Register Per:</i> socket	
Index: 17h						<i>Register Compatibility Type:</i> ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
FIFO Status / Flush FIFO	Scratchpad Bits						
RW:1	RW:0000000						

Register Name: Misc Control 2						<i>Register Per:</i> chip	
Index: 1Eh						<i>Register Compatibility Type:</i> ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
IRQ15/ RI_OUT* Is RI Out	Reserved		Timer Clock Divide	5V Core	Suspend Mode	Low-Power Dynamic Mode	External Clock Enable
RW:0	RW:00		RW:0	RW:0	RW:0	RW:1	RW:0

Register Name: Chip Information						<i>Register Per:</i> chip	
Index: 1Fh						<i>Register Compatibility Type:</i> ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Cirrus Logic Host-Adapter Identification	Dual/Single Socket		CL-PD6729 Revision Level			Reserved	
R:11	R:1		R:nnnn ^a			R:0	

^a This read-only value depends on the revision level of the CL-PD6729 chip.

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Register Name: ATA Control						Register Per: socket	
Index: 26h						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
A25/CSEL	A24/M/S*	A23/VU	A22	A21	Scratchpad Bit	Speaker Is LED Input	ATA Mode
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

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Register Name: Extended Index						Register Per: socket	
Index: 2Eh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Extended Index							
RW:00000000							

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Register Name: Extended Data						Register Per: socket	
Index: 2Fh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Extended Data							

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Register Name: Extension Control 1						Register Per: socket	
Index: 2Fh						Register Compatibility Type: ext.	
Extended Index: 03h							
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Reserved		Pull-Up Control	Invert Management IRQ Output	Invert Card IRQ Output	LED Activity Enable	Auto Power Clear	V _{CC} Power Lock
RW:00		RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

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Register Name: System Memory Map 0-4						Register Per: socket	
Upper Address						Register Compatibility Type: ext.	
Index: 2Fh						Extended Index: 05h-09h	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Upper Address							
RW:00000000							

Register Name: External Data (Index 2Fh)				Extended Index: 0Ah		Register Per: socket	
Index: 2Fh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
External Data (Phase 2 IRQ12)	External Data (Phase 2 IRQ11)	External Data (Phase 2 IRQ10)	External Data (Phase 2 IRQ9)	External Data (Phase 1 IRQ12)	External Data (Phase 1 IRQ11)	External Data (Phase 1 IRQ10)	External Data (Phase 1 IRQ9)
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Register Name: External Data (Index 6Fh)				Extended Index: 0Ah		Register Per: socket	
Index: 6Fh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
	Reserved			Socket B VS2 Input	Socket B VS1 Input	Socket A VS2 Input	Socket A VS1 Input
	RW:0000			R:0	R:0	R:0	R:0

Register Name: Extension Control 2 (Index 2Fh)				Extended Index: 0Bh		Register Per: socket	
Index: 2Fh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
	Reserved		GPSTB I/O Write*		Reserved		
	RW:000		RW:0		RW:0000		

Register Name: Extension Control 2 (Index 6Fh)				Extended Index: 0Bh		Register Per: socket	
Index: 6Fh						Register Compatibility Type: ext.	
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
	Reserved			GPSTB I/O Read*	Reserved		
	RW:0000			RW:0	RW:000		

B.2.5 Timing Registers
Page 67

Register Name: Setup Timing 0-1				Register Per: socket			
Index: 3Ah, 3Dh				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Setup Prescalar Select		Setup Multiplier Value					
RW:00		RW:000001					

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Register Name: Command Timing 0-1				Register Per: socket			
Index: 3Bh, 3Eh				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Command Prescalar Select		Command Multiplier Value					
RW:00		RW:000101/010100 ^a					

^a Timing set 0 (index 3Bh) resets to 05h for socket timing equal to 250-ns PCMCIA card timing. Timing set 1 (3Eh) resets to 14h for socket timings equal to 600-ns PCMCIA card timing.

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Register Name: Recovery Timing 0-1				Register Per: socket			
Index: 3Ch, 3Fh				Register Compatibility Type: 365			
<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
Recovery Prescalar Select		Recovery Multiplier Value					
RW:00		RW:000000					

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