



# KEYBOARD ENCODER 99 KEYS, 4 MODES

# EA 2000

SEPTEMBER 1975

EA 2000 - KEYBOARD ENCODER - 99 KEYS - 4 MODES

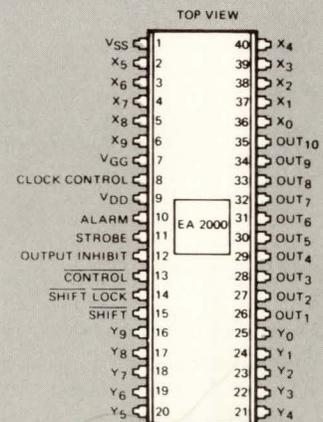
## GENERAL DESCRIPTION

The EA 2000 is a monolithic keyboard encoder utilizing MOS P-channel integrated circuit technology. The EA 2000 encodes 99 keys, with four modes per key, allowing 396 different key codes. Each key code contains 10 parallel output bits. N-key rollover is provided together with automatic key bounce suppression, alarm signal for detection of simultaneous key depression, data ready strobe, electronic shift lock, and output inhibit features. The Shift Control and Output Inhibit inputs are all TTL compatible. All outputs are TTL compatible. Standard +5V and -12V supplies are used. Custom programming of the encoder matrix (4000 bits) is accomplished by the alteration of one mask used in the fabrication of the device. An internal clock generator is built into the device.

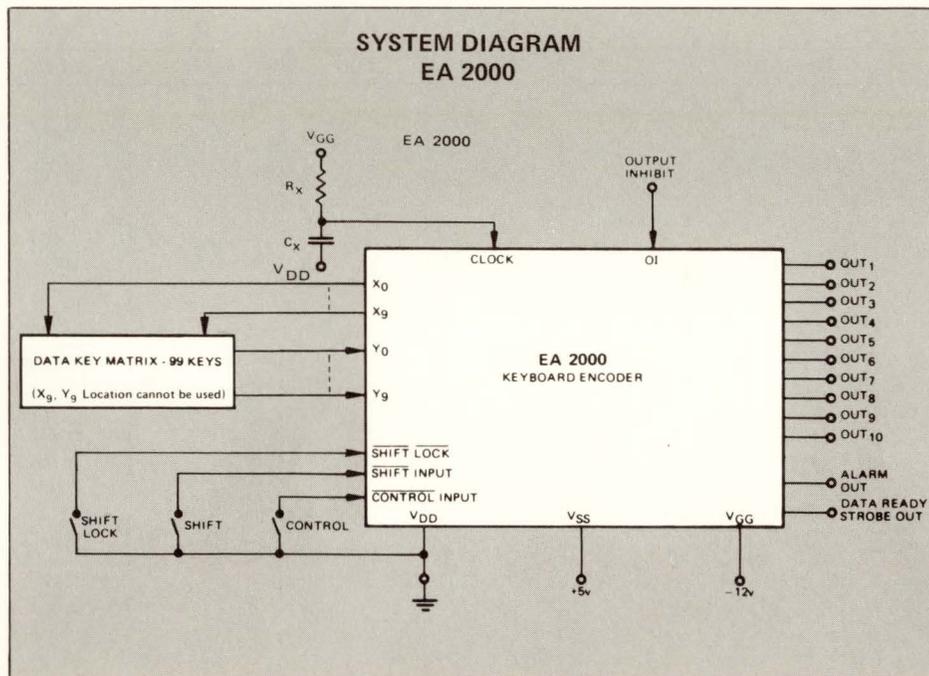
## FEATURES

- 99 KEY, FOUR MODE OPERATION
- FULLY PROGRAMMABLE 10 BIT OUTPUT WORDS
- N-KEY ROLLOVER
- ERROR DETECTION FOR SIMULTANEOUS KEY DEPRESSIONS
- AUTOMATIC KEY BOUNCE PROTECTION
- ELECTRONIC SHIFT LOCK
- INTERNAL CLOCK GENERATOR
- TTL COMPATIBLE - 3-STATE OUTPUTS

## CONNECTION DIAGRAM 40 LEAD DIP



## SYSTEM DIAGRAM EA 2000



## ORDERING INFORMATION

	Temp. Range	Package
EA20XXCD	0°C to +70°C	Hermetic 40 Pin DIP
EA20XXCP	0°C to +70°C	Molded 40 Pin DIP

Custom bit patterns require a unique bit pattern number (XX) assigned by Electronic Arrays.

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# electronic arrays, inc.

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**ABSOLUTE MAXIMUM RATINGS**

V <sub>DD</sub> Supply Voltage (Relative to V <sub>SS</sub> )	+0.5V to -20V	Stresses more severe than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
V <sub>GG</sub> Supply Voltage (Relative to V <sub>SS</sub> )	+0.5V to -20V	
Operating Temperature Range (Ambient)	0°C to +70°C	
Storage Temperature	-65°C to +150°C	

**STANDARD TEST CONDITIONS**

The characteristics below apply for the following standard test conditions unless otherwise noted. All voltages are referenced with respect to GND. Positive current is defined as flowing into the referenced pin.

$$+4.75V \leq V_{SS} \leq +5.25V$$

$$0^\circ C \leq T_A \leq +70^\circ C$$

$$-11.4V \geq V_{GG} \geq -12.6V$$

$$\text{Output Load} = 1 \text{ TTL Load}$$

$$V_{DD} = \text{GND}$$

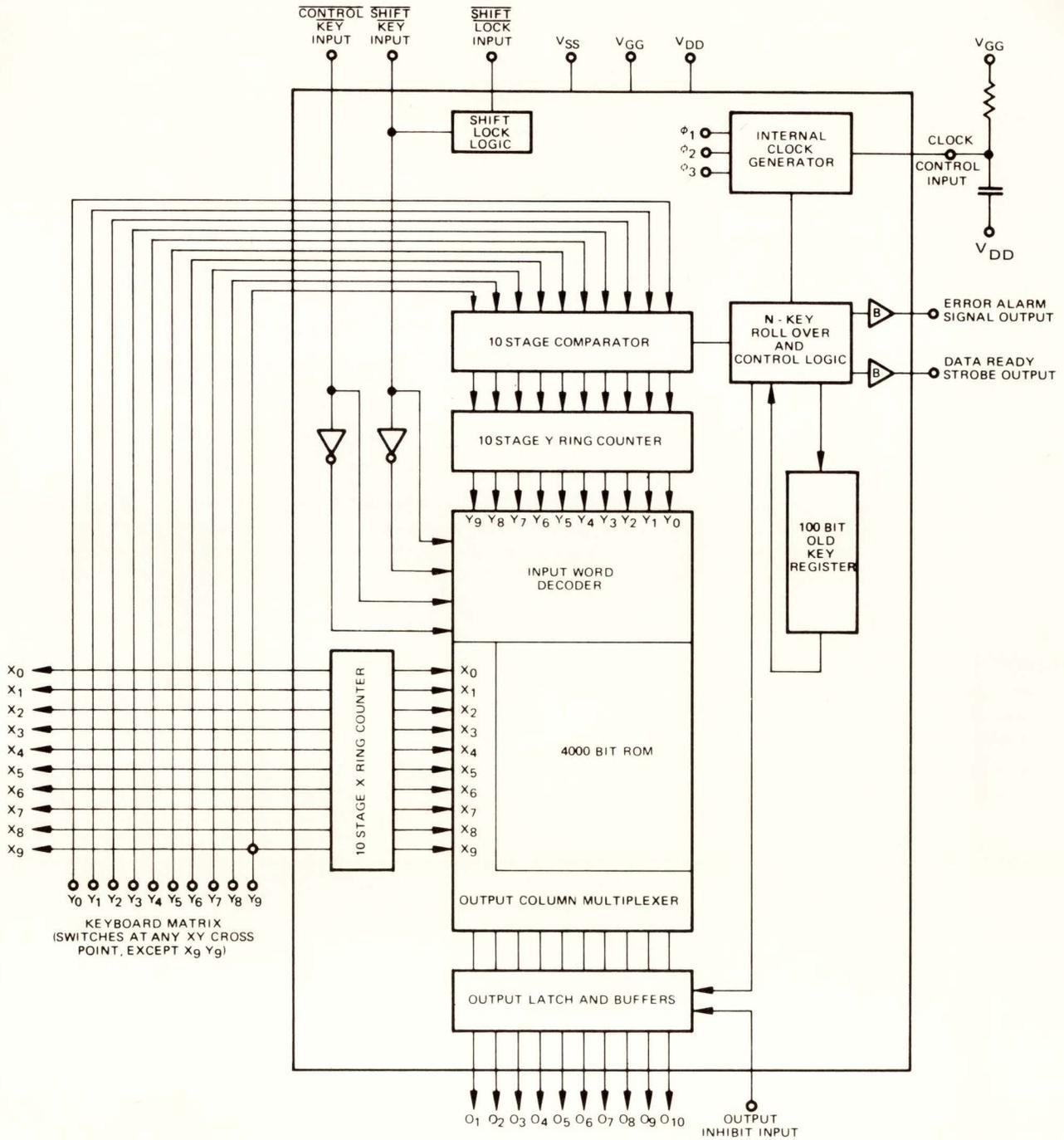
**ELECTRICAL DRIVE REQUIREMENTS**

Parameter	Condition	Min.	Typ.	Max.	Units
Clock Frequency (Internal)	Under specified RC conditions(Note1)	40		125	KHz
Clock Frequency (External)	(Note 2)	80		250	KHz
<b>INPUT LEVELS</b> (Control, Shift, Shift Lock, and Output Inhibit)					
Logic "1"		2.8		V <sub>SS</sub> +0.3	Volts
Logic "0"				+0.8	Volts
<b>ALLOWABLE KEYSWITCH LOAD</b>					
Series Contact Resistance				500	Ohms
Stray Capacitance	(Note 3)			200	pF
Forward Diode Voltage Drop				0.8	Volts

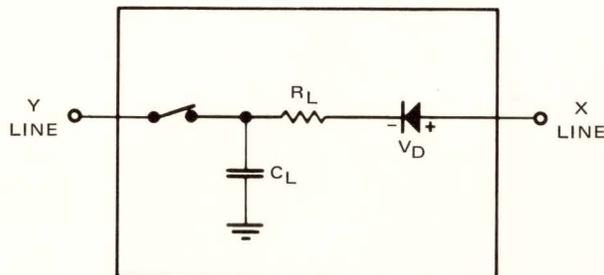
**ELECTRICAL CHARACTERISTICS**

Parameter	Condition	Min.	Typ.	Max.	Units
<b>DATA OUTPUTS</b>					
Logic "0" Level	I = 1.6mA			0.4	Volts
Logic "1" Level	I = -100μA	4.0			Volts
<b>INPUT CAPACITANCE</b> (Control, Shift, Shift Lock, and Output Inhibit)					
	0 volt bias			5.0	pF
<b>INPUT RESISTANCE</b> (Control, Shift, Shift Lock, and Output Inhibit)					
	T <sub>A</sub> = +25°C	3.0		10	Kohms
<b>POWER SUPPLY CURRENT</b>					
I <sub>SS</sub> (note 4)	T <sub>A</sub> = +25°C		19	24	mA
I <sub>GG</sub>	T <sub>A</sub> = +25°C		19	24	mA
<b>OUTPUT CAPACITANCE</b>					
				15	pF
<b>OUTPUT LEAKAGE</b>					
	Disabled V <sub>O</sub> = V <sub>SS</sub>			10	μA

- NOTES:**
- For the internal frequency to fall within the spec range of 40 to 125 KHz use R<sub>x</sub> = 180 Kohms and C<sub>x</sub> = 33 pF. These values also assume a 2 pF stray capacitance. For other frequency, resistor, capacitor combinations see operating characteristic graph.
  - Due to a divider network in the internal clock, the external clock frequency at pin 8 is twice the required internal clock frequency.
  - Keyswitch capacitance is defined as the total capacitance between any X or Y line and ground.
  - Input and output interface current not included. Each TTL compatible input adds 1.75 mA maximum to I<sub>SS</sub>.



KEY SWITCH PARAMETER:



- R<sub>L</sub> max = 500 Ω
- C<sub>L</sub> max = 200 pF
- V<sub>D</sub> max = 0.8 V

## 1. KEYBOARD SCANNING

The EA 2000 automatically scans a 99-key keyboard, generating continuous sequential outputs on the X outputs and detecting key closures on the Y inputs.

The scanning circuitry consists of a 10-stage X ring counter, a 10-stage Y ring counter, and a 10-bit word comparator as shown in the block diagram.

Only one stage of a ring counter can be in the "one" state at any point in time. A "one" in the Y ring counter is shifted one position with each clock period. Every 10th clock period the Y ring counter generates a clock enable signal which gates the clock to the X ring counter. Thus, the Y ring counter controls the clocking to the X ring counter. The clock rate of the Y ring counter is ten times the clock rate of the X ring counter and a complete cycle of the X and Y ring counters requires 100 clock periods. The single ended outputs of the X ring counter drive the 10 rows of the key matrix. The Y ring counter outputs feed a 10-stage comparator which compares each Y ring counter output with a Y (column) line from the key matrix. The key matrix is limited to 99 keys since internal control logic is being reset at the time the 100th key is being scanned.

When a key is depressed, an X output line drives a Y line to a logic one. The word comparator generates a "one" level when the Y ring counter output and the Y line are both a logic one.

A load capacitance of 200 pF can be driven by the X lines. Also, a diode and a series resistance of 500 ohms can be placed between the X and Y lines. When a key is depressed, the Y line switches to a logic one which is a minimum voltage of +3 volts.

## 2. KEY VERIFICATION

A key depression will be considered verified after it is detected three times by the scanning matrix. When a key is detected the first time, an internal flip-flop will be set. If the key is again detected on the third scan cycle, an output code will be generated and will be available at the Output pins. At the beginning of the fourth scan cycle, Data Ready Strobe will become true (logic 1) indicating that valid data is available. This verification technique automatically accomplishes key bounce protection. A key will not be recognized unless it is detected through these successive scan cycles. Key bounce protection can be adjusted indirectly by modifying the clock frequency.

## 3. ENCODING ROM

The output code for each key depression is stored in 4000 bit ROM which is permanently programmed during the manufacture of the encoder. This ROM program is established by the user and transmitted to Electronic Arrays using either truth tables, paper tape or punched cards.

The 4000 bit ROM provides the user with complete flexibility for each of the 10-bit output words for each key depression and mode. The EA 2000 does not use logic to generate any codes. Therefore, output data words are completely programmable with no restrictions.

## 4. ALARM SIGNAL

The Alarm output or error signal will become true whenever two new keys are detected as being closed during a single scan cycle. A new key is defined as one for which valid data (indicated by a Data Ready Strobe) has not been outputted. The Alarm signal is reset or cleared by the occurrence of any of the following conditions:

- a. The first end-of-scan after all keys have been released.
- b. If one new key is detected after the alarm condition is cleared, but before the Alarm signal is cleared, the Alarm will clear at the beginning of the next scan cycle.
- c. If an old key is still depressed (not one which caused the alarm condition), and one new key is detected after the alarm condition is cleared but before the Alarm is cleared, the Alarm signal will clear at the end-of-scan of the following cycle (one scan cycle before strobe).

## 5. ELECTRONIC SHIFT LOCK

The shift lock input will provide for sustained operation of the keyboard in the shift mode. Shift lock is enabled by applying an external logic "0" to the shift lock input pin. Reset of the shift lock operation occurs when a shift signal is applied. The shift lock lead will directly drive a transistor buffer which will provide current for an indicator lamp.

## 6. DATA READY SIGNAL

When a new key depression is verified and its output code has been generated, the Data Ready Strobe will switch to a logic 1 state at the beginning of the following scan cycle. The Data Ready Strobe then remains in the logic 1 state and is reset either the first time a new key is scanned, or the first end-of-scan after all keys are detected as released.

## 7. TTL INTERFACE

The Keyboard Encoder outputs will drive TTL directly without external resistors. The control, output inhibit, shift, and shift lock inputs have internal pull-up resistors so that no external resistors are required for direct TTL compatibility on these inputs.

**8. N-KEY ROLLOVER**

The unique logic design of the EA 2000 provides N-Key rollover characteristics without requiring either diodes at each key location or pulse output key switches.

Certain patterns of three key closures can simulate a fourth (ghost) key closure. When three keys are depressed, one which shares a common X line with the second key and a common Y line with the third key, a conductive path is created between the Y line of the second key and the X line of the third key which will be detected as a fourth key closure. This obviously can always be avoided by using a blocking diode in series with each key. The EA 2000 key validation logic, however, accomplishes this without requiring the diode. When the third key closure creates the ghost key condition, the EA 2000 will detect two key closures (the third key and the ghost) and the Alarm signal will go HIGH. Once the Alarm signal is HIGH, the Data Ready Strobe is inhibited, and the EA 2000 does not indicate that valid data is available. Following clearing of this condition, the Alarm signal will be reset as described in Section 4.

**9. INTERNAL CLOCK**

An internal clock performs all the timing for the EA 2000 Keyboard Encoder. The frequency of the clock is controlled by two external components, resistor  $R_X$  and capacitor  $C_X$ .

The clock is forced into oscillation as power is applied to the Keyboard Encoder. Capacitor  $C_X$  charges through resistor  $R_X$  towards the  $V_{GG}$  voltage. When the voltage across the capacitor exceeds an internal reference voltage, the capacitor is discharged and the cycle is repeated. Two charging cycles for the capacitor required to form one clock cycle. For each clock cycle, the clock generates three phase internal clocks  $\phi_1$ ,  $\phi_2$ , and  $\phi_3$ , which drive the ring counters and a static shift register.

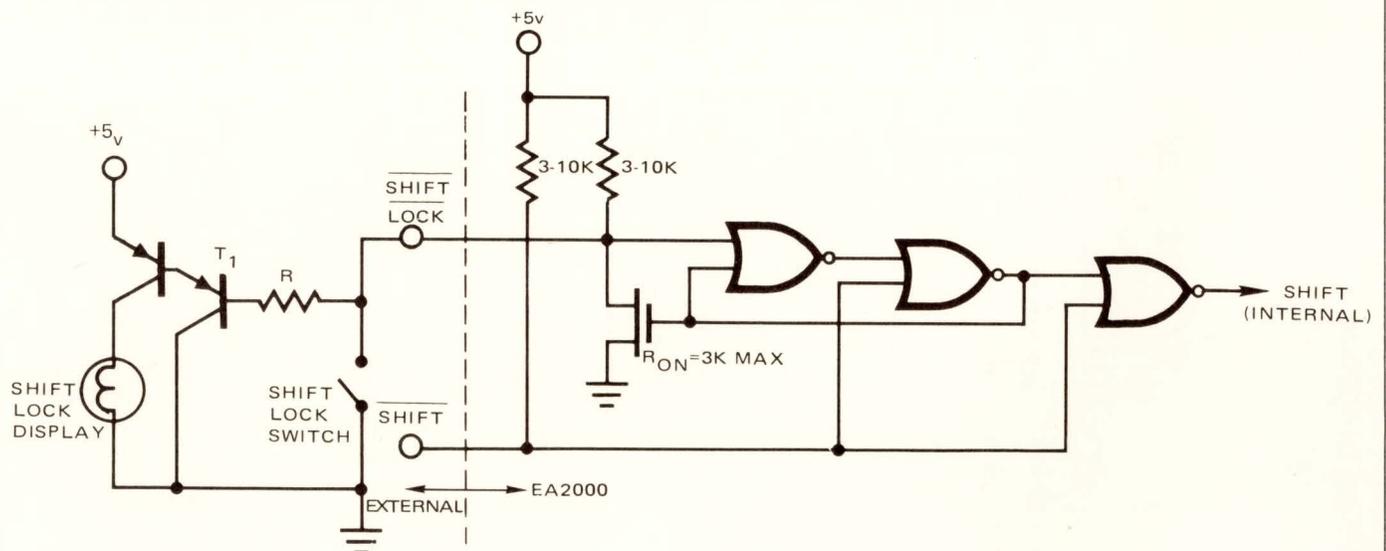
Additional features of the internal clock are as follows:

- a. The tolerance of the frequency of oscillation is established by the tolerance of the external RC components. The recommended values to stay within limits of 80 to 125 KHz are  $R_X = 180$  Kohms,  $C_X = 33$  pF, plus 2 pF stray wiring capacitance. The combined RC network must be maintained within  $\pm 12\%$  tolerance such as a 2% resistor and a 10% capacitor. Other frequency, resistor, capacitor values can be determined from the operating characteristic graph.
- b. The internal clock frequency can be varied from 40 KHz to 125 KHz which results in scan rates of 2.5 msec and 0.8 msec respectively.
- c. If necessary, an external clock can be used to drive the internal clock under special conditions. Special testing is required, consult factory.

**SHIFT LOCK CIRCUIT**

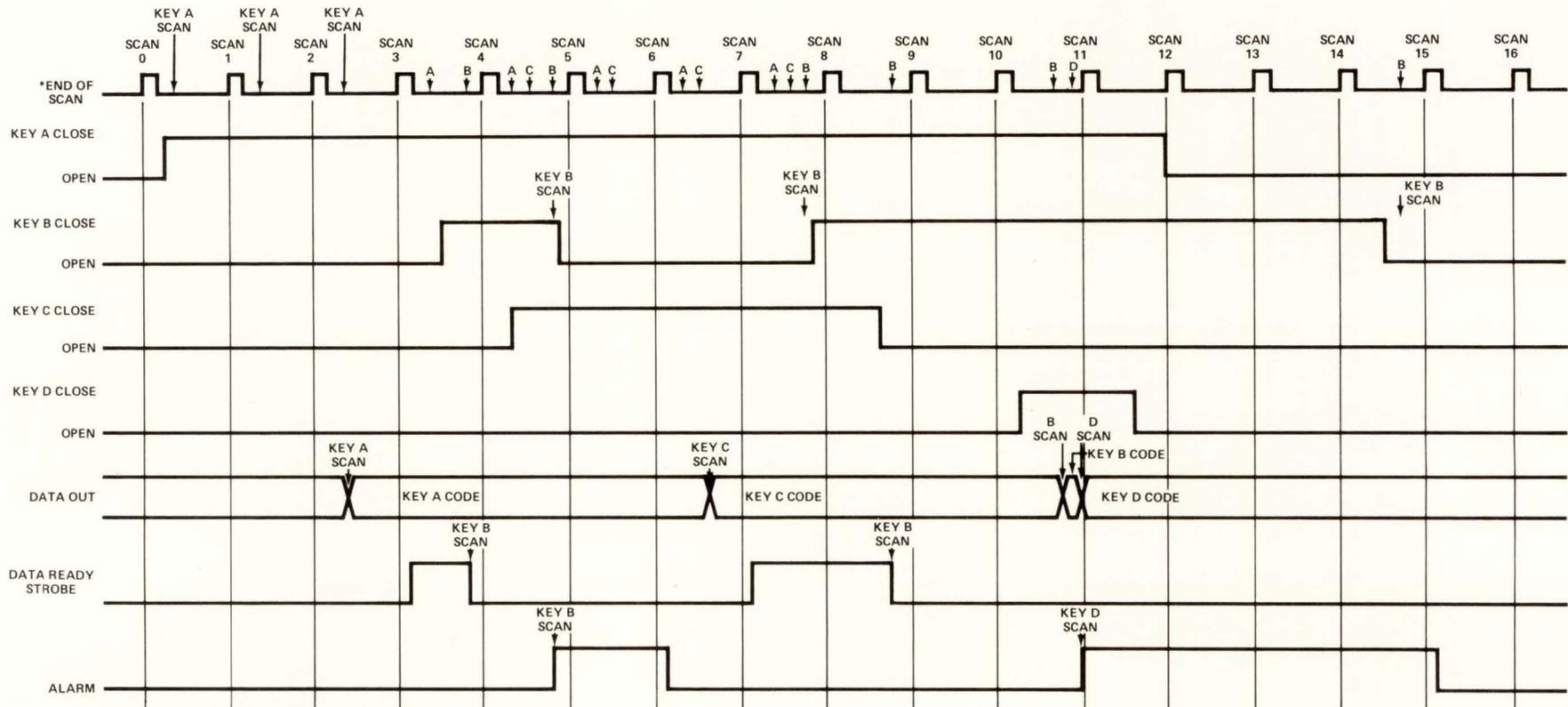
Shown below is the internal logic used inside the EA 2000 to accomplish shift lock. The shift input performs the dual function of inverting the internal shift signal, and resetting the shift lock flip-flop.

The shift lock display circuit shown on the SHIFT LOCK input can be used to display the state of this input. The internal circuitry can provide a max of 100  $\mu$ A of base current (negative) to the  $T_1$  transistor without impairing the internal voltage divider network. Exact external circuit design is the responsibility of the user.



# TIMING DIAGRAM

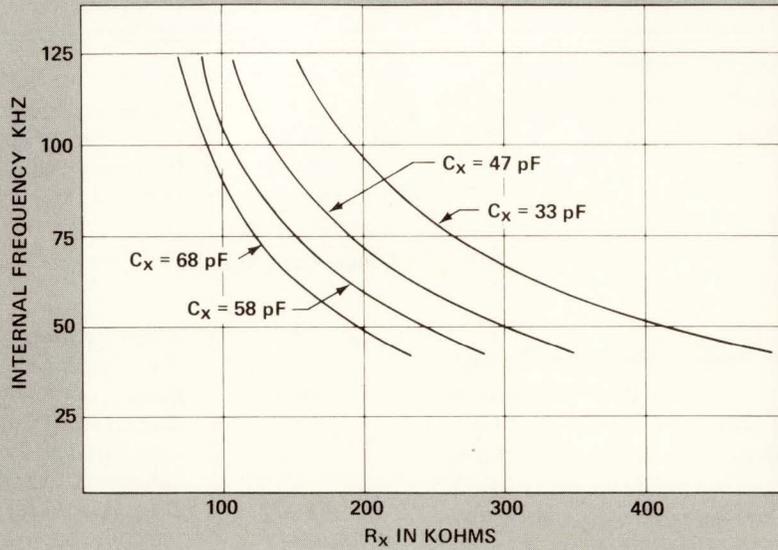
EA 2000



\*DENOTES SIGNAL INTERNAL TO EA 2000.

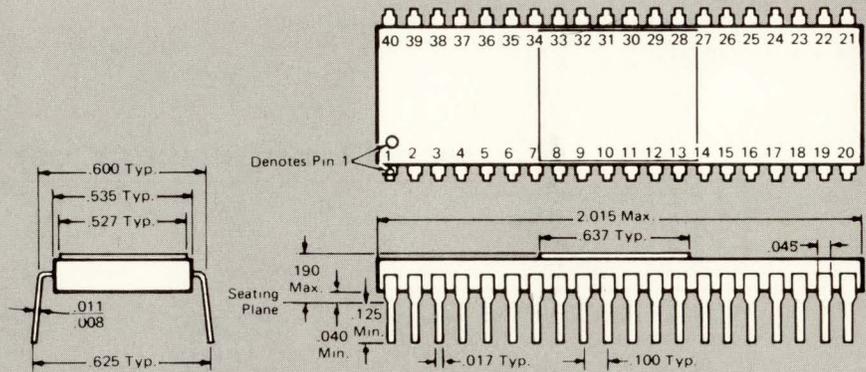
1. End of scan is signal internal to the EA2000.
2. At a clock frequency of 100 KHz, each scan cycle is 1 msec in duration. During each scan cycle all 99 key locations are scanned.
3. If all keys are released, the data ready strobe returns to a logic "0" state, but the data output lines maintain the code of the last depressed key. If this condition is not desirable, the output inhibit can be used to float the data outputs.
4. At power up, the encoder outputs will assume an arbitrary key code until a key is depressed and detected. However, the data ready strobe will come on in the "zero" state.



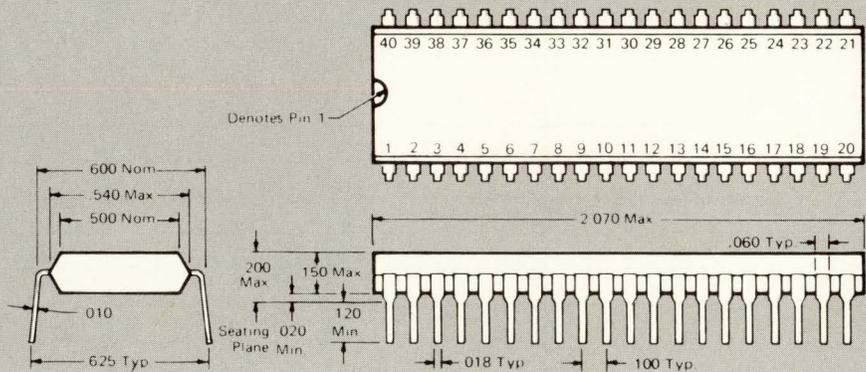


PHYSICAL DIMENSIONS

40 LEAD HERMETIC DIP



40 LEAD SILICONE DIP



EA RESERVES THE RIGHT TO MAKE CHANGES IN THESE SPECIFICATIONS AT ANY TIME AND WITHOUT NOTICE

