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EXAR

TIMER DATA BOOK

First in Quality... First in Service • Custom, Semi-custom and Standard IC's

Introduction

This Data Book contains a complete summary of technical information covering Exar's entire line of monolithic IC timer products. In addition, several design and applications articles are also included, along with a review of fundamentals of IC timing circuits. To help the designer to choose the right timer circuit for his application, a convenient cross-reference chart is also included which shows the key features of each of the products discussed, in terms of different classes of applications.

EXPERIENCE AND PRODUCTS

Exar's innovativeness, product quality and responsiveness to customer needs have been the key to its success. Exar today offers a broad line of linear and interface circuits. In the field of standard linear IC products, Exar has extended its circuit technological leadership into the areas of communications and control circuits. Today Exar has one of the most complete lines of IC oscillators, timing circuits and phase-locked loops in the industry. Exar also manufactures a large family of telecommunication circuits such as tone decoders, compandors, modulators, PCM repeaters and FSK Modem Circuits. In the field of industrial control circuits, Exar manufactures a broad line of quad and dual operational amplifiers,voltage regulators, radio-control and servo driver IC's, and power control circuits.

Exar's experience and expertise in the area of bipolar IC technology extends both into custom and standard IC products. In the area of custom IC's, Exar has designed, developed, and manufactured a wide range of full-custom monolithic circuits, particularly for applications in the areas of telecommunications, consumer electronics, and industrial controls.

In addition to the full-custom capability, Exar also offers a unique semi-custom IC development capability for low to medium-volume custom circuits. This semi-custom program, is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks at a small fraction of the cost of a full-custom development program.

EXCELLENCE IN ENGINEERING

Exar quality starts in Engineering where highly qualified people are backed up with the advanced instruments and facilities needed for design and manufacture of custom, semi-custom and standard integrated circuits. Exar's engineering and facilities are geared to handle all three classes of IC design: (1) semi-custom design programs using Exar's bipolar and I^2L master chips; (2) full-custom IC design; (3) development and high-volume production of standard products.

Some of the challenging and complex development programs successfully completed by Exar include analog compandors and PCM repeaters for telecommunication, electronic fuel-injection, anti-skid braking systems and voltage regulators for automotive electronics, digital voltmeter circuits, 40-MHz frequency synthesizers, high-current and high-voltage display and relay driver ICs, and many others.

NEW TECHNOLOGIES

Through company sponsored research and development activities, Exar constantly stays abreast of all technology areas related to changing customer needs and requirements. Exar has recently completed development efforts in Integrated Injection Logic (I^2L) technology, which offers unique advantages in the area of low-power, high-density logic arrays. Exar has a complete design engineering group dedicated to this new technology, and is currently supplying over twenty different custom and semi-custom I^2L products.

FIRST IN QUALITY

From incoming inspection of all materials to the final test of the finished goods, Exar performs sample testing of each lot to ensure that every product meets Exar's high quality standards. Exar's manufacturing process is inspected or tested in accordance with its own stringent Quality Assurance Program, which is in compliance with MIL-Q-9858A. Additional special screening and testing can be negotiated to meet individual customer requirements.

Throughout the wafer fab and assembly process, the latest scientific instruments, such as scanning electron microscopes, are used for inspection, and modern automated equipment is used for wafer probe, AC, DC, and functional testing. Environmental and burn-in testing of finished products is also done in-house. For special environmental or high reliability burn-in tests outside testing laboratories are used to complement Exar's own extensive in-house facilities.

FIRST IN SERVICE

Exar has the ability and flexibility to serve the customer in a variety of ways from wafer fabrication to full parametric selection of assembled units for individual customer requirements. Special marking, special packaging and military screening are only a few of the service options available from Exar. We are certain that Exar's service is flexible enough to satisfy 99% of your needs. The company has a large staff of Applications Engineers to assist the customer in the use of the product and to handle any request, large or small.

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Fundamentals of IC Timers

Monolithic timing circuits or *timers* find a wide variety of applications in both linear and digital signal processing. In a large number of industrial control or test sequencing applications, these circuits provide direct and economical replacement for mechanical or electro-mechanical timing devices.

Monolithic timers generate precise timing pulses, or time delays whose length or repetition rate is determined by an external timing resistor, R, and a timing capacitor, C. The timing interval is proportional to the external (RC) product, and can be varied from micro-seconds to minutes, days or months, by the choice of the external R and C. Integrated circuit timers can be classified into two categories, based on their principle of operation:

1. **One-Shot or Single-Cycle Timers**: These timer IC's operate by charging an external capacitor with a current set by an external resistor. Upon triggering, the charging cycle happens only *once* during the timing interval. The total timing interval, T, is the time duration necessary for the voltage across the capacitor to reach a threshold value.
2. **Multiple-Cycle or Timer/Counters**: These timer circuits charge and discharge the external timing capacitor, not once, but a *multiple number of times* during the timing interval. The number of times the capacitor is charged and discharged is set by means of a pre-set count, N, stored in a binary counter included on the chip. Thus, the resulting time interval is proportional to N times the external (RC) product.

Both the one-shot and the timer/counter type IC's can be operated in either their monostable or free-running (i.e., self-triggering) mode. They can also be used for sequential timing, clock generation, as well as for pulse-position or pulse-width modulation, as outlined in Table I.

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Missing-Pulse Detection
Sweep Generation
Pulse Counting
Clock Generation

TABLE 1. Typicial Applications of Monolithic Times

ONE - SHOT OR SINGLE - CYCLE TIMERS

One-shot or single-cycle timers operate by charging a timing capacitor through an external resistor or a current source. The simplest form of the one-shot type timer is the "exponential-ramp generator" circuit shown in Figure 1. Normally all the components except the R and the C shown in the Figure are internal to the IC, and the switch S_1 is a grounded-emitter NPN transistor included in the IC chip.

The operation of the circuit can be briefly explained as follows: In the rest, or reset condition, the switch S_1 is closed; and the voltage across the capacitor is clamped to ground. The timing cycle is initiated by applying an external trigger pulse to "set" the flip-flop and to open the switch S_1 across the timing capacitor. The voltage across the capacitor rises exponentially toward the supply voltage, V_{CC}, with a time-constant of RC. When this voltage level reaches an internally set threshold voltage, V_{REF}, the voltage comparator changes state, resets the flip-flops, closes the switch S_1, and ends the timing cycle. The output is taken from either the Q or $\bar{Q}$ terminal of the flip-flop and corresponds to a timing pulse of duration T, where:

$$T = RC \ln \left[\frac{V_{CC}}{V_{CC} - V_{REF}}\right] \tag{1}$$

Normally, the internal threshold voltage, V_{REF}, is generated from the supply voltage by means of a resistor divider as shown in Figure 1. Then, V_{REF} is equal to a fraction of the supply voltage:

$$V_{REF} = V_{CC}\left[\frac{R_2}{R_1 + R_2}\right] \tag{2}$$

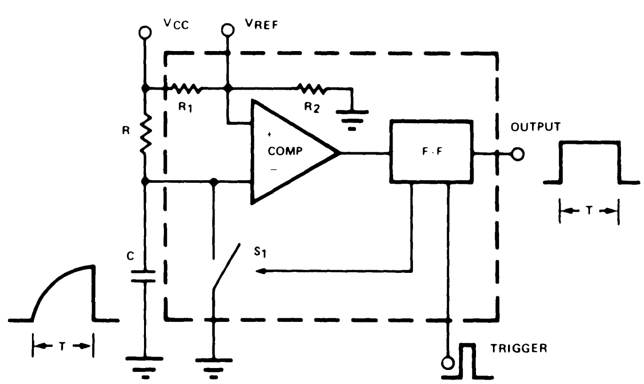


Figure 1. Exponential-Ramp Type Timing Circuit

and the basic timing equation becomes independent of the supply voltage:

$$T = RC \ln \left[1 + \frac{R_2}{R_1} \right] \qquad (3)$$

Since the resistors R_1 and R_2 are inside the IC, their ratio is set by the design of the IC, and is normally accurate to within ± 1%. Thus, virtually all the accuracy of the timing interval is determined by the external R and C.

An alternate approach to the design of one-shot timers is the "linear-ramp generator" circuit, shown in Figure 2. This circuit operates on a principle similar to that of the basic exponential timer, except the timing capacitor C is now charged *linearly* with a constant current, I, and generates a linear-ramp waveform with a constant slope of (I/C). The constant-current is in turn controlled by an external control voltage, V_C, applied to the current source. The total timing interval, T, is the time necessary for the voltage across C to rise from ground to V_{REF}, at a constant slope of (I/C), or:

$$T = (V_{REF})(C/I) \qquad (4)$$

Normally, V_{REF} and V_C (and consequently I) would be derived from V_{CC} by means of resistor-dividers; therefore, they would be both proportional to V_{CC}. Thus, the effects of supply voltage variations cancel, and the basic timing equation for the linear-ramp type timer circuit of Figure 2 becomes

$$T = \alpha\ RC$$

where α is a constant of proportionality set by the internal resistor-dividers within the IC, and R and C are the external timing components.

The exponential-ramp type timing circuit of Figure 1 is inherently simpler and more accurate than the linear-ramp type circuit. However, the latter has the advantage of providing a linear voltage across the capacitor which is proportional to the *elapsed-time* during the timing cycle and can be used as a "linear sweep" or time-base signal for oscilloscope or X-Y recorder displays.

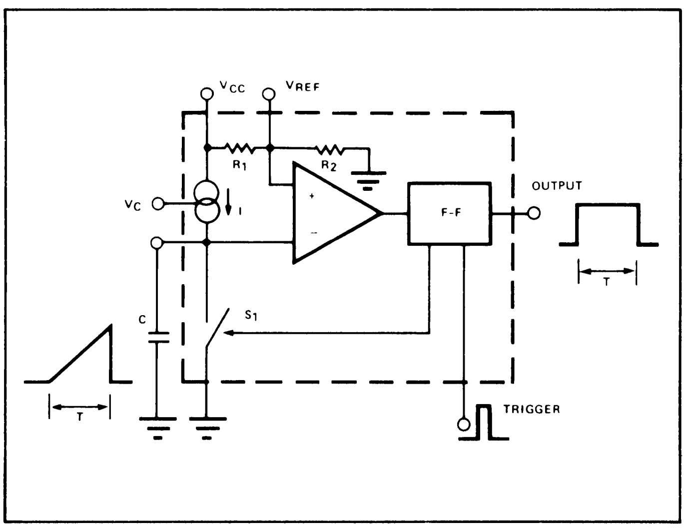


Figure 2. Block Diagram of a Linear-Ramp Type Timer Circuit.

Normally, the internal threshold reference, V_{REF}, of one-shot IC's is available as a package terminal and can be modulated by an external input signal. This permits the user to modulate or vary the timing interval by means of an external control signal. This feature can also be used for generating pulse-width modulated (PWM), or pulse-position modulated (PPM) signals, or allows the timer circuit to be used as a voltage-controlled oscillator.

PRACTICAL LIMITATIONS OF ONE-SHOT TIMERS

The accurate timing intervals which can be obtained from commercially available one-shot type timer IC's are limited to the range of several micro-seconds to several minutes. For generating very short timing pulses (in the few micro-second range) the internal time delays associated with the switching speeds of the comparator, the flip-flop and the discharge transistor (i.e., the switch S_1) may contribute additional timing errors. Similarly, for long time delays (in the several minute range) which require large values of R and C, the input bias current of the comparator, and the leakage currents associated with the timing capacitor, or the internal discharge transistor, may limit the timing accuracy of the circuit.

In general, for timing applications requiring time delays in excess of several minutes, the multiple-cycle or timer/counter type timer circuits provide a more economical and practical solution than the one-shot type IC timers.

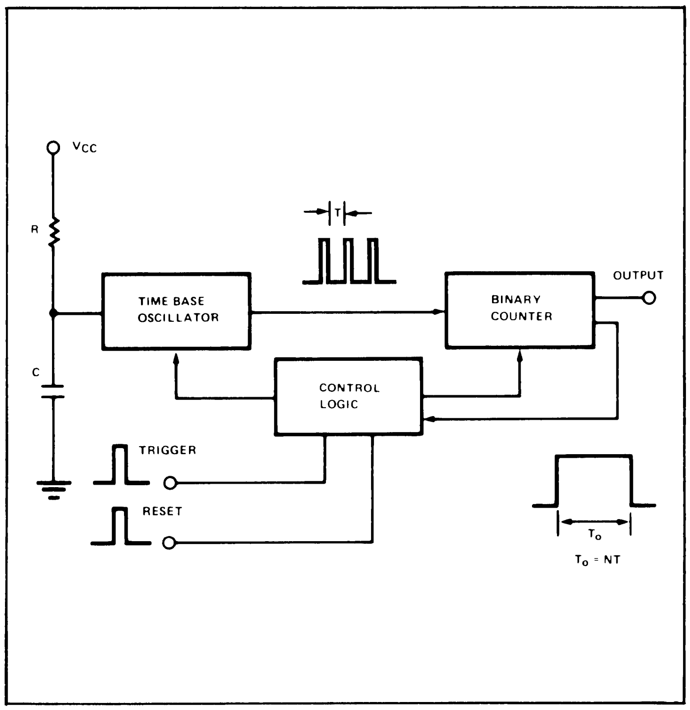


Figure 3. Simplified Block Diagram of a Timer/Counter.

TIMER/COUNTER CIRCUITS

The timer/counter, or multiple-cycle timing circuits use the combination of a time-base oscillator and a binary counter to generate the desired time delay. Figure 3 shows a simplified block diagram of a timer/counter IC, which is made up of three basic blocks: (1) a time-base oscillator; (2) a binary counter; and (3) a control flip-flop.

With reference to the simplified block diagram of Figure 3, the principle of operation of a timer/counter can be explained as follows: when the circuit is at rest, or reset condition, the time-base oscillator is disabled, and the counter is reset to zero. Once the circuit is triggered, the time-base oscillator is activated and produces a series of timing pulses whose repetion rate is proportional to external timing resistor R, and the capacitor C. These timing pulses are then counted by the binary counter; and when a pre-programmed count is reached, the binary-counter resets the control flip-flops, stops the time-base oscillator and ends the timing cycle. The total timing interval, T_0, is then proportional to N times the (RC) product, where N is the pre-programmed count.

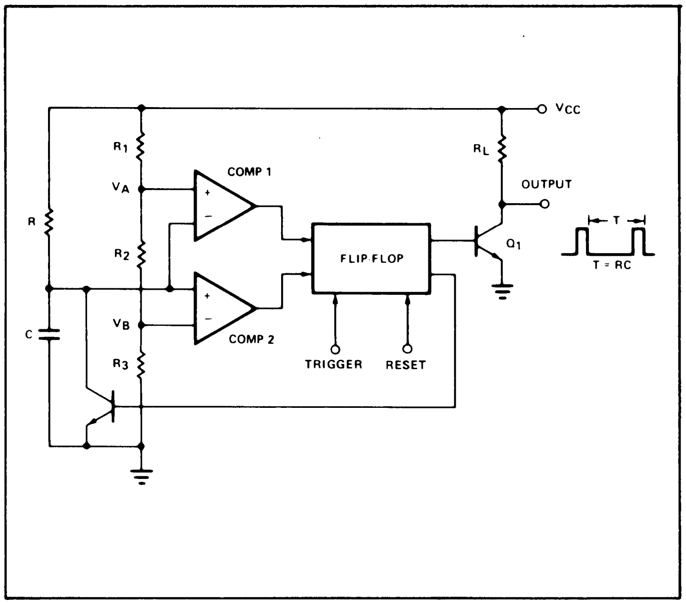


Figure 4. Simplified Schematic of a Time-Base Oscillator Circuit

Time-Base Oscillator: The time-base oscillator used in most of the timer/counter IC's is derived from the simple exponential-ramp type timer circuit. Figure 4 shows the simplified circuit diagram of such an oscillator. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, and the transistor Q_1 is "off", the external capacitor C is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor Q_1 to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_B, the comparator #2 changes state, resets the flip-flop and turns Q_1 "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_A, comparator #1 changes state and sets the flip-flop again, and discharges C back to the lower threshold level, V_B. In this manner, the circuit continues to oscillate, with the voltage level across C exponentially rising to V_A, then rapidly decaying to V_B, and then repeating its cycle. The output of the circuit is a sequence of narrow pulses, with a repetition rate T, given as:

$$T = RC \ln \left[1 + \frac{R_2}{R_1} \right] \qquad (6)$$

where R_1 and R_2 are the internal bias resistors setting up the threshold levels V_A and V_B. The train of output pulses coming out of the time-base oscillator are counted by the binary counter; and when a given count, N, is reached, the control flip-flop is latched in its reset condition until the next trigger input to the circuit.

In most timer/counter designs, it is convenient to set the ratio of resistors R_1 and R_2 such that:

$$\frac{(R_1 + R_2)}{R_1} = e = 2.718\ldots \qquad (7)$$

where "e" is the base of the natural logorithm. This makes the period of the time-base oscillator directly equal to 1.0 RC and simplifies the selection of external R or C values for a given timer setting.

UNIQUE FEATURES OF TIMER/COUNTERS

The combination of a stable time-base oscillator and a programmable binary counter on the same IC chip offer some unique application and performance features. Some of these are outlined below:

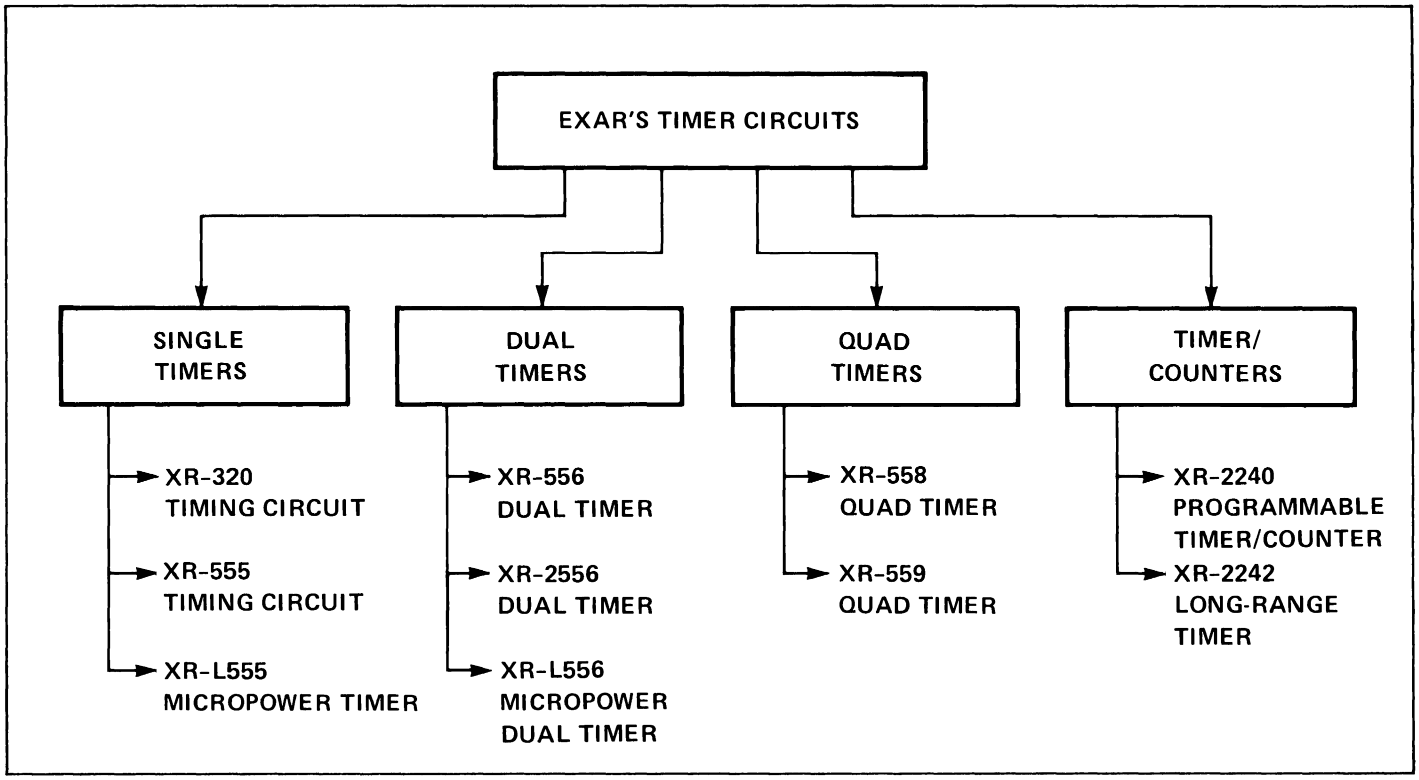
Generating Long Delays with Small Capacitors: For a given time delay setting, the timer/counter would require a timing capacitor, C, that is N times smaller than that needed for the "one-shot" type timer, where N is the count programmed into the binary counter. Since large-value, low-leakage capacitors are quite expensive, this technique may provide substantial cost savings for generating long time delays in excess of several minutes.

Generating Ultra-Long Delays by Cascading: When cascading two timer/counters, one cascades the counter stages of both timers. Since the second timer/ counter further divides down the counter output of the first timer, the total available count is increased *geometrically*, rather than arithmetically. For example, if one timer/counter gives a time delay of NRC, two such timer/counters cascaded will produce a time delay of N^2 RC where N is the count setting of the binary counter. Thus, a cascade of two timer/counter IC's, each with an 8-bit binary counter, can produce a time delay in excess of 32,000 RC.

Generating Multiple Delays From Same RC Setting: By using a programmable binary counter, whose total count can be programmed between a minimum count of 1, to a maximum count of N, one can obtain N different time intervals from the same external RC setting.

Easy to Set or Calibrate: Although timer/counters are normally used for generating long time delays or intervals, their accuracy characteristics are only determined by the characteristics of the time-base oscillator. The counter section does not affect the over-all timing accuracy. Thus, time setting or calibration for long interval timing can be done quickly, without waiting for the entire timing cycle, by setting the accuracy of the time-base oscillator.

Overview of Exar's Timer Products



Exar offers the widest selection of monolithic timers in the IC industry. These products cover both the conventional one-shot type timers, as well as the timer/counter circuits. Table I, gives a summary of the *nine* different families of IC timer products manufactured by Exar.

XR-320 MONOLITHIC TIMING CIRCUIT

The XR-320 is a one-shot or single-cycle type timer, operating on the "linear-ramp generation" principle. Figure 1 shows the functional block diagram of the monolithic chip in terms of its 14-pin circuit package. The XR-320 can be triggered with either positive- or negative-going trigger pulses and produces both positive and negative polarity outputs. The timing period of the circuit is set by an external resistor, R, and capacitor, C, and is equal to 2.0 (RC).

A unique feature of the XR-320, compared to other one-shot timer IC's, is that it uses an on-chip constant-current source to charge the external timing capacitor. Thus, it produces a linear-ramp waveform across the external capacitor (pin 3) which can be used as "linear sweep" for X-Y recorders or oscilloscope displays.

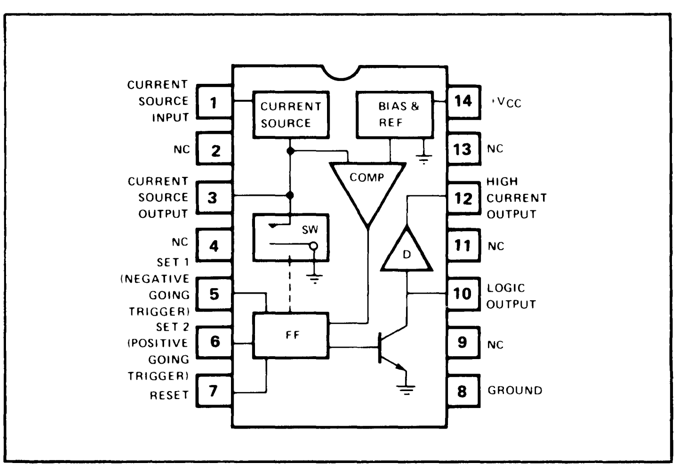


Figure 1. Functional Diagram of XR-320 Monolithic Timing Circuit.

XR-555 TIMER CIRCUIT

The XR-555 timer IC operates on the "exponential-ramp principle" and produces time delays of 1.1 RC, as set by the external timing resistor and capacitor. It is a direct, pin-for-pin replacement for the popular SE/NE-555 timer circuit.

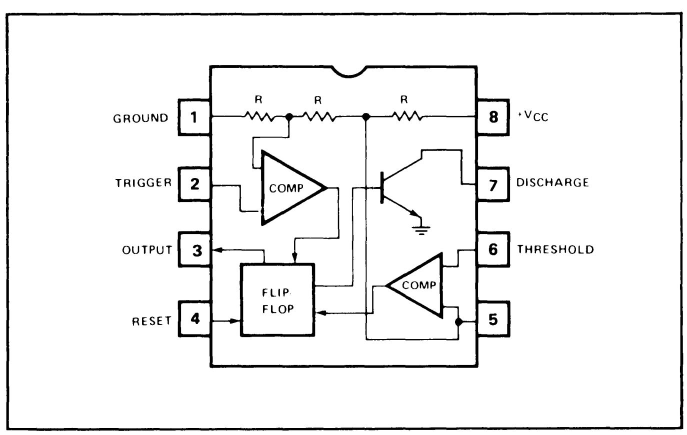


Figure 2. Block Diagram of XR-555 Timer Circuit.

A functional block diagram of the XR-555 timer is shown in Figure 2, in terms of its 8-pin circuit package. The circuit is activated by a negative-going trigger input applied to pin 2; and produces a positive-going output pulse. Its output can source or sink up to 200 mA of load current. The circuit can also be used as an oscillator by operating it in its free-running (i.e., self-triggering) mode. The output duty cycle and the frequency can be externally adjusted or modulated.

XR-556 DUAL TIMER

The XR-556 dual timing circuit contains *two* independent 555-type timers on a single monolithic chip. It is a direct, pin-for-pin replacement for SE/NE-556 dual timer IC.

As shown in Figure 3, both timer sections common power supply and ground lines; however, their control and output terminals are completely independent. Each output of XR-556 can source or sink up to 150 mA of load current. The matching and tracking characteristics between each timer section of a dual timer IC are normally superior to those available from two separate timer packages.

The XR-556 dual timer is particularly well-suited to those timing applications which require a multiplicity of timing functions. Some examples of such applications are sequential timing, pulse-width modulation, delayed timing and tone-burst generation.

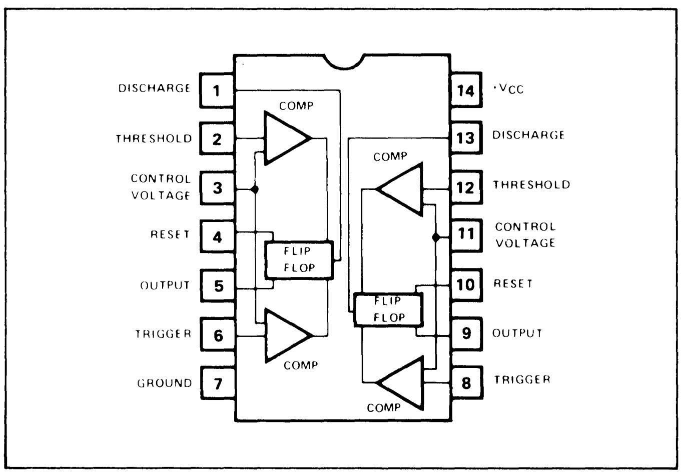


Figure 3. Functional Diagram of XR-556 Dual Timer.

XR-2556 DUAL TIMER

The XR-2556 is a modified version of the basic XR-556 dual timer. It offers higher current output capability (up to 200 mA) than the conventional 556-type dual timer. The package and pin configuration of the XR-2556 is given in Figure 4.

XR-L555 MICROPOWER TIMER

The XR-L555 is *the micropower version* of the popular 555-type timer expecially designed for applications requiring very low power dissipation. It is directly pin compatible with the basic 555-timer. However, it exhibits 1/15th the power dissipation and can operate down to 2.7 volts, without sacrificing such key features as timing accuracy and frequency stability.

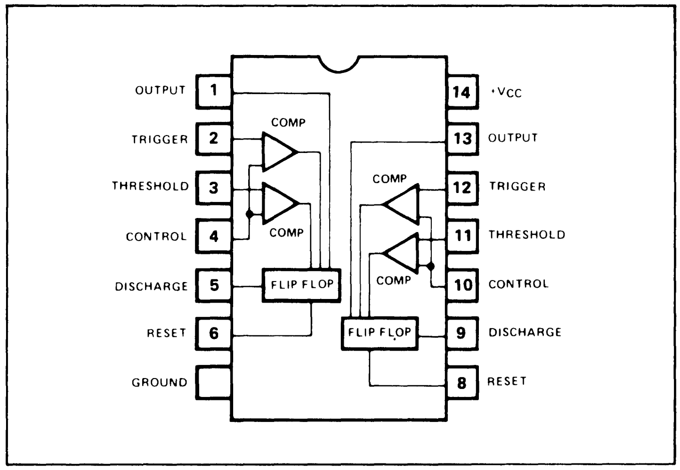


Figure 4. Functional Diagram of XR-2556 Dual Timer.

Figure 5 shows the functional block diagram of the XR-L555. The circuit output can source up to 50 mA of load current or drive TTL circuits. Because of its temperature stability and low-voltage operation capability, the XR-L555 is ideally suited as a micropower clock oscillator or VCO for low-power CMOS systems. It can operate up to 1500 hours with only two 300 mA-Hour NiCd batteries.

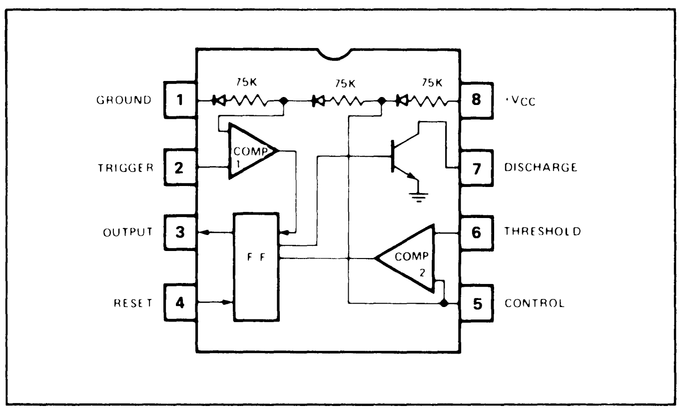


Figure 5. Package Diagram of XR-L555 Micropower Timer.

XR-L556 MICROPOWER DUAL TIMER

The XR-L556 is the *micropower version* of the popular 556-type dual timer. It is especially designed for applications requiring multiple timing functions with very low power dissipation. It is the dual-timer version of Exar's XR-L555 micropower timer, and is directly pin-compatible with the basic 556-type dual timer circuits. The circuit exhibits 1/15th the power dissipation of conventional dual-timer circuits and can operate down to 2.5 Volts.

Each micropower timer section of the XR-L556 have independent trigger and reset controls, and each output can source up to 50mA of load current, or drive TTL circuits. The functional block diagram of the XR-L556 micropower dual timer is identical to that of XR-556.

XR-558/XR-559 QUAD TIMERS

The XR-558 and the XR-559 quad timer IC's contain *four* independent timer sections on a monolithic chip. The time delay associated with each timer section is set by an external resistor and a capacitor combination, and is equal to 1.0 RC. These quad timers provide a direct, pin-for-pin replacement for the SE/NE 558 and the SE/NE 559 quad timer IC's.

Figure 6 shows the block diagram of the XR-558 or the XR-559 quad timers. Both IC's have identical internal circuitry, except for the outputs: the XR-558 has open-collector type outputs designed for current-sinking; the XR-559 has Darlington emitter-follower outputs, designed for current-sourcing. All of the timer outputs are normally at a "low" state, and go to "high" state during timing cycle. All of the four timer sections share common "reset" and "modulation" controls, but have independent triggers. Each timer section is edge-triggered; thus they can be cascaded, without coupling capacitors, to provide sequential timing..

The quad timer circuits are particularly useful for system applications requiring a multiplicity of timing functions. In such applications, they can provide significant cost or board-space savings over single-timer circuits.

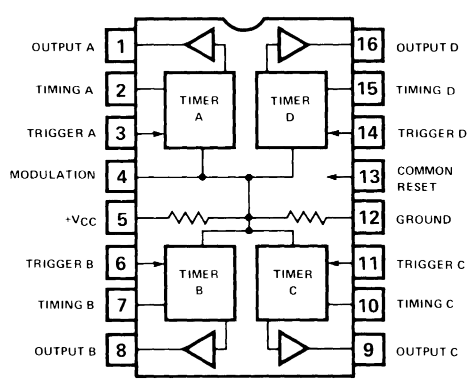


Figure 6. Functional Block Diagram of the XR-558 or the XR-559 Quad Timer Circuits.

XR-2240 PROGRAMMABLE TIMER/COUNTER

The XR-2240 programmable timer/counter circuit contains an internal time-base oscillator, a control flip-flop and a programmable 8-bit binary counter, as shown in Figure 7.

When triggered, the time-base oscillator generates timing pulses with a repetition rate equal to the external RC product, set by the resistor and the capacitor externally connected to the timing terminal. These output pulses are counted by the binary-counter, and when a given count, N, is reached, the circuit resets itself and completes its timing cycle. The programming of the binary-counter is done by selectively shorting one or more of the counter outputs to a common pull-up resistor. In this manner, the circuit can generate a time delay, T_O, where T_O can be programmed to be any integer value from 1.0 RC to 255 RC.

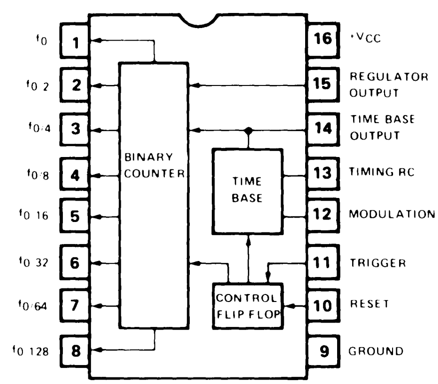


Figure 7. Functional Block Diagram of XR-2240 Timer/Counter.

XR-2242 LONG-RANGE TIMER

The XR-2242 is a timer/counter IC specifically designed for generating ultra-long time delays, from milliseconds to hours or days. Its block diagram is shown in Figure 8, in terms of the circuit package.

The circuit is basically a simplified version of the XR-2240 programmable timer/counter, without its programming capability. When triggered, the circuit produces an output timing pulse of 128 RC duration for a given R-C network connected to its timing terminal. Two such circuits can be cascaded to generate time delays in excess of 32,000 RC.

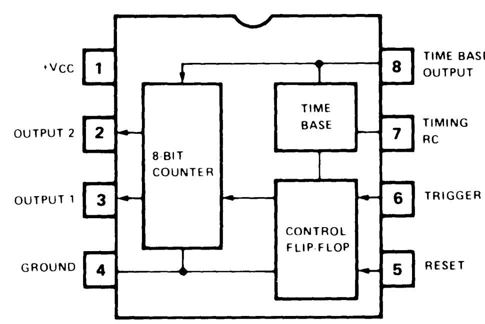


Figure 8. Package Diagram of XR-2242 Long-Range Timer.

Performance Feature	XR-320	XR-555	XR-556	XR-L555	XR-L556	XR-2556	XR-558	XR-559	XR-2240	XR-2242
Output Polarity During Timing Cycle										
High	√	√	√	√	√	√	√	√		
Low	√								√	√
Output Drive Capability										
High Current (⩾100 mA)	√	√	√			√	√	√		
Current Sourcing	√	√	√	√	√	√		√		
Current Sinking	√	√	√			√	√		√	√
Complementary Outputs	√									
Open-Collector Outputs	√						√		√	√
Trigger Characteristics										
Positive-Going	√								√	√
Negative-Going	√	√	√	√	√	√	√	√		
Edge-Triggered							√	√		
Level-Triggered	√	√	√	√	√	√			√	√
Reset Characteristics										
Positive-Going									√	√
Negative-Going	√	√	√	√	√	√	√	√		
Low Voltage Operation ($V_{CC} \leqslant 3V$)				√	√					
Modulation Capability		√	√	√	√	√	√	√		
Adjustable Duty Cycle		√	√	√	√	√			√	
Digital Programming Capability									√	

Table 1. Summary of Performance Features of Exar's Timer IC Products

Choosing the Right IC Timer

Because of its versatility, the monolithic IC timer offers a very wide range of applications in circuit or system design. However, during the design phase, once the "paper design" is accomplished, the user is faced with the key question: which IC timer is the best choice for a given application? If the performance characteristics and the limitations of the timer IC is not carefully considered, the total system performance may be degraded; similarly, if the timing function is overspecified with an excessive amount of "overkill", particularly with regards to its stability and accuracy requirements, then the system cost will increase unnecessarily.

The key selection criteria in choosing the right timer for the job is finding the monolithic IC which will result in the lowest system cost (including the external components) for a given performance requirement.

A very large majority of applications for IC timers can be classified into one of the four categories listed below:

- Interval or Event Timing
- Pulse Generation and Shaping
- Oscillation or Clock-Generation
- Ramp Generation

These categories of applications are discussed in more detail in the following sections, with the particular emphasis on "choosing the right IC timer" for the particular application.

INTERVAL OR EVENT TIMING

In such an application one uses the IC timer either to control the *time interval* between events, or the *duration* of an event. A typical example of such application would be to control the opening or closing of an electromechanical relay or sequencing of indicator lights.

General Purpose Timing: Most timing applications fall within the time interval range of a few microseconds to several minutes. For such applications the basic one-shot timer, such as the XR-555, is often the best choice, based on its low cost and versatility.

Low-Power Timing: Many timing applications involving battery-operated or portable equipment, require a low-power timer which can perform the general purpose timing functions with a minimum amount of power dissipation. The XR-L555 Micropower Timer IC, which operates with less than 1 mW of power dissipation and with supply voltages as low as 2.7 volts, is especially designed for such applications.

Long Interval Timing: For timing applications requiring interval timing in the minutes, hours, or days range, the timer/counter IC's present the most economical approach, since they can produce long time delays using a small value capacitor. For such an application the low-cost XR-2242 Long Range Timer, which operates on the timer/counter principle, is the most cost-effective circuit.

Sequential Timing: Many timing applications require *sequencing* of timing functions, i.e., one timer completes its operation and initiates the next timer, and so on. Since these applications require a multiplicity of timer circuits, they are best served by dual-timer IC's, such as the XR-556 or the XR-2556.

Delayed Timing: Certain timing applications require that the start of the timing pulse be delayed by a specific time from the occurance of the trigger. This can be easily accomplished by using a dual-timer, such as the XR-556, where one section of the dual-timer can be used to set the initial "delay" subsequent to the trigger; and the second section can be used to generate the actual timing pulse.

Event Counting: In such an application, one needs to keep an accurate count of "events" which are normally a series of incoming pulses. This function can be easily performed with a programmable timer/counter IC, such as the XR-2240, where the binary counter section can be programmed to count a given number of input pulses and stop the count, and/or reset the circuit when the programmed count is reached. In the case of the XR-2240, the existing count in the counters is displayed in an 8-bit parallel binary-format.

Digitally-Programmed Timing: Some timing applications may require that the timing interval be digitally programmable, without switching additional precision resistors and capacitors into the circuit. Such a function can be easily achieved by using a programmable timer/counter, such as the XR-2240, where output duration can be programmed from 1.0 RC to 255 RC, in 1 RC increments, where R and C are the external timing components.

PULSE GENERATION AND SHAPING

A popular class of applications for the one-shot type timers is pulse shaping or stretching. Some specific examples of such applications and the recommended types of IC timers for each are given below.

Pulse Stretching: In such an application the IC timer is operated in its monostable mode and is triggered by an input series of pulses, whose repetition period is *longer* than the timing period of the IC. The output from the timer will then have the same repetition rate as the input pulse train, except that each output pulse will now have a uniform duration or length, as set by the RC time constant of the timer. The two IC's best suited to this application are the XR-555 and the XR-320. The XR-555 has the advantage of low unit price, whereas the XR-320 has the advantage of being able to trigger on *either* positive- or negative-going edge of the input pulses.

Delayed-Pulse Generation: In this application it is necessary to convert the input pulse train to a different pulse sequence which has the *same* repetition rate but a *different* duration and a *different* phase. This function can be accomplished with a dual-timer circuit, such as the XR-556 or the XR-2556, where the first timer which is triggered by the input signal, sets the phase difference or "delay" between the input and the output pulse sequence; and the second timer which is triggered at the trailing-edge of the first one, sets the output pulse-width.

Pulse Blanking: In this application it is necessary to selectively "interrupt" or "blank-out" a pulse train. Such an application can be performed using a dual-timer IC, such as the XR-556, where one section of the timer can be operated as a "pulse-stretcher" triggered by the input pulse train; and the second timer section can be triggered by a separate timing signal and serve as an enable/disable control for the first timer, thus interrupting or "blanking" its output during its timing interval.

Pulse-Width Modulation: In certain timing applications it is necessary to modulate the pulse-width of an output pulse sequence, without affecting its repetition rate. Such a requirement can be met by a one-shot timer, such as the XR-555, operating in its monostable mode and being triggered by a fixed-frequency input pulse-train. The width of the output pulses from the timer IC can be modified without affecting the repetition rate, by simply applying a control-voltage to the modulation terminal of XR-555 (see Fig. 27 on page 29).

Pulse-Position Modulation: This application requires the generation of a pulse sequence whose pulse-width is constant (and usually very narrow) and, whose repetition rate is modulated. Such a function can be easily implemented using a dual-timer IC, such as the XR-556, where the second timer generates the narrow output pulses when triggered by the output of the first timer. The first timer section is then operated in its free-running (i.e., astable) mode and its frequency is then externally modulated by applying a control-voltage to its modulation terminal.

OSCILLATION OR CLOCK-GENERATION

IC Timers can be operated in their free-running or "self-triggering" mode, to generate periodic timing pulses. Since the output pulse-width or the frequency can be controlled by the choice of external resistors and capacitors. These circuits make excellent low-cost clock oscillators, for a number of digital systems. Some of these applications are outlined below.

Clock Generator: In such applications, the IC is used to generate a fixed-frequency output waveform with nearly 50% duty cycle. The XR-555 timer, whose output duty-cycle can be controlled by the choice of two external resistors, is ideally suited for such an application, for clock frequencies up to 300 kHz.

High-Current Oscillator: Certain oscillator applications require that the circuit output should be able to source or sink high load currents ($\geqslant$ 100 mA) in order to drive electromechanical relays or capacitive loads. The XR-555 Timer IC, which can provide up to 200 mA of current drive, is well suited for such applications.

Micropower Oscillator: Battery operated or remote-controlled instruments often require a low-power clock oscillator. The XR-L555 Micropower Timer, which operates with less than 1 mW of power drain, is the recommended choice for such applications, since it dissipates 1/15th the power of the conventional 555-type timer.

Voltage-Controlled Oscillator: Voltage-controlled oscillator (VCO) circuits find a wide range of applications in phase-locked loop systems. The XR-555 (or its low-power/low-voltage version of the XR-L555) which has a separate modulation terminal (pin 5) can be used as a VCO by applying the proper control voltage to its modulation terminal and operating the IC in its self-triggering mode.

Low-Voltage Oscillator: Low threshold CMOS logic circuits normally require stable clock oscillators which can operate with a single 3 volt power supply. The XR-L555 Micropower Timer which can operate with supply voltages as low as 2.7 volts is particularly suited for such applications.

Ultra-Low Frequency Oscillator: Certain battery operated or remote-controlled equipment require a stable ultra-low frequency clock oscillator, whose frequency can be as low as one cycle per day. The XR-2242 Long-Range Timer circuit which produces a square-wave output with a period of 256 RC, when operating in its free-running mode, is a very cost-effective replacement for such an oscillator.

Digitally-Programmed Oscillator: In certain applications it may be necessary to program the frequency of an oscillator by means of a binary control signal, without switching additional resistors or capacitors into the circuit. The XR-2240 Programmable Timer/Counter, when operating in its delayed-trigger mode (see Exar Application Note AN-07) can be used in such an application to generate an output frequency whose period is equal to (N + 1)RC, where N is the binary count which can be digitally programmed by an external 8-bit binary signal, to be any integer between 1 and 255.

Binary Pattern Generator: In certain test instrumentation design, it is necessary to generate a pseudorandom binary data pattern, which would then repeat itself periodically. The XR-2240 Programmable Timer/Counter which provides eight separate "open-collector" outputs, can perform such a function by selective shorting of one or more of its outputs to a common pull-up resistor (see Fig. 22 on page 36).

Tone-Burst Generator: Some instrumentation applications require the generation of a certain tone or frequency signal, at periodic intervals. This function can be accomplished using a dual-timer IC, such as the XR-556 or the XR-2556, where one of the timer sections would operate as a keyed oscillator which is turned "on" and "off" by the other timer section. The output of the first timer section will then be a "tone-burst", which will be present only during the timing cycle of the second timer (see Fig. 22 on page 28).

RAMP GENERATION

In a number of timing applications, it is necessary to generate an analog voltage which is proportional to the time elapsed during the timing cycle. This function is particularly useful for generating linear sweep voltage for oscilloscope or X-Y recorder display applications and it can be accomplished either *linearly* or *digitally*, as described below.

Linear Ramp Generator: A linear ramp can be obtained by charging a timing capacitor with a constant-current source. Since the XR-320 Timer IC operates on such a principle, it is ideally suited for this application. Upon triggering, the XR-320 produces a positive-going ramp at its current-source output (pin 3). This ramp starts from the ground level and rises up to a voltage level approximately equal to 80% of the supply voltage, during the timing interval (see Figures 4 and 5, on page 14. Since the current-source output at pin 3 is a high impedance terminal, the sweep or linear ramp signal at this point should be buffered by a high impedance op amp connected as a voltage follower.

Digital Ramp Generator: In certain applications, a digitally generated "staircase" voltage is preferred over a linear ramp signal. Such a digital ramp signal can be generated using the XR-2240 Programmable Timer/Counter, along with an external resistor ladder and a current-summing op amp, as shown in Figure 26 on page 43. The digital ramp signal is particularly useful for analog-to-digital conversion or digital sample-and-hold applications (see Figures 27 and 28 on page 43).

MAJOR APPLICATION	RECOMMENDED TIMER CIRCUIT									
	XR-320	XR-555	XR-L555	XR-556	XR-L556	XR-2556	XR-558	XR-559	XR-2240	XR-2242
Interval Timing										
Short Interval (microseconds to seconds)	√	√	√	√	√	√	√	√		
Long Interval (seconds to days)									√	√
Programmable Time Delays									√	
Delayed Timing				√	√	√	√	√		
Pulse Generation/Shaping										
Pulse Shaping	√	√	√	√	√	√	√	√		
Pulse-Position Modulation	√	√	√	√	√	√				
Pulse-Width Modulation	√	√	√	√	√	√				
Pulse-Counting				√	√	√	√	√	√	
Delayed Pulse Generation				√	√	√	√	√		
Oscillation/Clock-Generation										
Clock Generator	√	√	√	√		√				√
High-Current Oscillator	√	√	√	√		√				
Low-Voltage Oscillator			√		√					
Micropower Oscillator			√		√					
Voltage-Controlled Oscillator		√	√	√	√	√			√	
Tone-Burst Generator				√	√	√	√	√		
Ultra-Low Frequency Oscillator									√	√
Programmable Oscillator									√	
Dual Oscillator				√	√	√	√	√		
Ramp Generation										
Linear Ramp Generator	√									
Stair-Case Generator						√				

Table 1. Major Applications of Exar's Timing Circuits

XR-320

Monolithic Timing Circuit

GENERAL DESCRIPTION

The XR-320 monolithic timing circuit is designed for use in instrumentation and digital communications equipment, and for a wide variety of industrial control and special testing applications. In many cases, this circuit provides a monolithic replacement for mechanical or electromechanical timing devices.

The XR-320 timing circuit generates precise timing pulses (or time delays) whose repetition rate (or length) is determined by an external timing resistor, R, and timing capacitor, C. The timing period is exactly equal to 2RC and can be continuously varied from 1 μsec to 1 hour. The circuits can be operated in a monostable or free-running (self-triggering) mode. They can be used for sequential timing and sweep generation, and also for pulse-position and pulse-width modulation.

The XR-320 integrated circuit is comprised of a stable internal bias reference, a precision current source, a voltage comparator, a flip-flop, a timing switch, and a pair of output logic drivers. The high current output at pin 12 can sink or source up to 100 milliamps of current.

FEATURES

Wide Timing Range: 1 μsec to 1 hour
High Accuracy: 1%
Excellent Temperature Stability: 100 ppm/°C
Wide Supply Voltage Range: 4.5V to 18V
Triggering with Positive or Negative-Going Pulses
Programmable
  Resistor Programming: 3 decades
  Capacitor Program: 9 decades
Logic Compatible Outputs
High Current Drive Capability: 100 mA

APPLICATIONS

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Sweep Generation

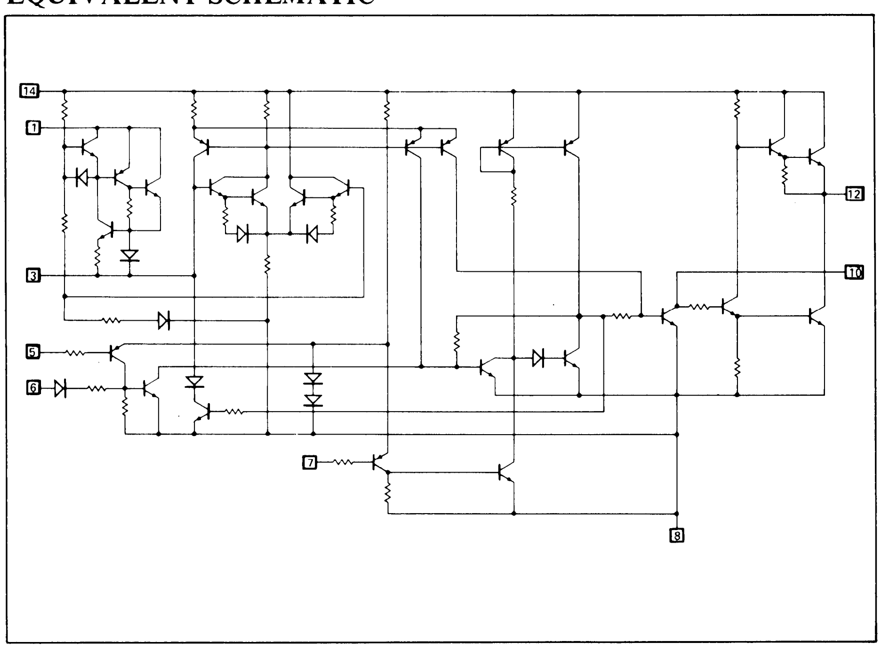
ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Internal Power Dissipation	750 mW
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

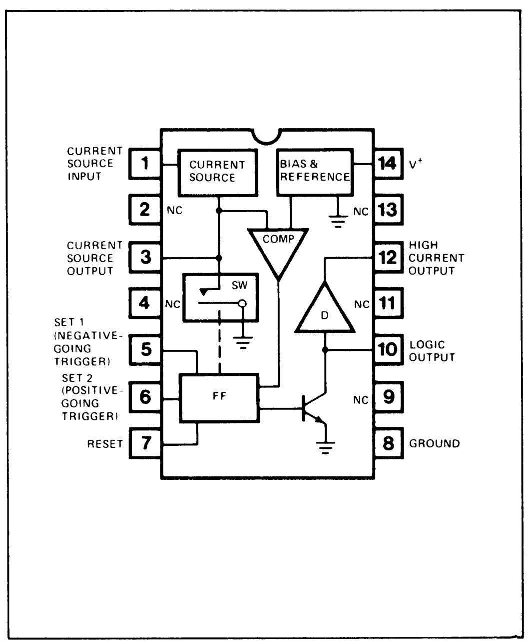
AVAILABLE TYPE

Part Number	Package	Operating Temperature
XR-320P	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V ±5%, Test Circuit of Figure 2, T_A = 25°C, unless otherwise specified.

CHARACTERISTICS	XR-320 MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage	4.5		18	V_{dc}	
Quiescent Supply Current					
V^+ = 5V		2.0	3.5	mA	
V^+ = 12V		6.0	7.0	mA	
V^+ = 18V		10.0	12.5	mA	
Timing Cycle Supply Current					
V^+ = 5V		2.5	4.0	mA	
V^+ = 12V		6.5	8.0	mA	
V^+ = 18V		12.0	14.0	mA	
Timing Accuracy					
V^+ = 5V		1.0	5.0	%	
V^+ = 12V		1.0	5.0	%	
V^+ = 18V		1.0	5.0	%	
Temperature Drift		100		ppm/°C	
Timing vs. Supply Voltage		0.1	0.5	%/V	
Stand-by Voltage (Pin 3)		0.7		V	
Comparator Threshold Voltage (Pin 3)					
V^+ = 5V		2.4		V	
V^+ = 12V	4.5	5.2	6.0	V	
V^+ = 18V		8.4		V	
Current Source Input Voltage (Pin 1)					
V^+ = 5V		4.15		V	
V^+ = 12V	9.0	9.75	10.6	V	
V^+ = 18V		16.15		V	
Trigger Voltage					
Set (Pin 5)		1.0	1.5	V	See Figure 11
Set 2 (Pin 6)	0.5	1.4		V	See Figure 12
Reset (Pin 7)		0.7	1.5	V	
Trigger Current					
Set 1 (Pin 5)		10		μA	
Set 2 (Pin 6)		60		μA	
Reset (Pin 7)		30		μA	
Output 1 (Pin 10) (Normally low)					
"Low" Voltage		0.1		V	
"High" Voltage	4.0	5.0		V	
Rise Time		140		nsec	
Fall Time		50		nsec	
Output 2 (Pin 12) (Normally high)					
"High" Voltage		10.4		V	I_{source} = 100 mA
"Low" Voltage		1.5		V	I_{sink} = 100 mA
Rise Time		100		nsec	
Fall Time		40		nsec	

DEFINITIONS

Timing Accuracy: the timing error solely introduced by the XR-320, defined in per cent as:

$$100 \times \frac{\text{measured timing pulse length} - \text{2 RC based on actual component values}}{\text{2 RC based on actual component values}} \%$$

Timing vs Supply Voltage: the maximum timing drift over the power supply range of 5 to 18 volts referenced to 12 volt operation, defined in per cent per volt as:

$$\frac{100}{15} \times \frac{\text{max. timing pulse length over 5 to 18 volt supply} - \text{min. timing pulse length over 5 to 18 volt supply}}{\text{timing pulse length with 12 volt supply}} \%/V$$

Stand-by Voltage: the voltage between pin 3 and ground in reset condition.

Comparator Threshold Voltage (Pin 3): the voltage at which the internal comparator triggers the flip-flop and the timing capacitor discharges.

Trigger Voltage: the DC voltage level applied to each set or reset terminal which causes the output to change state.

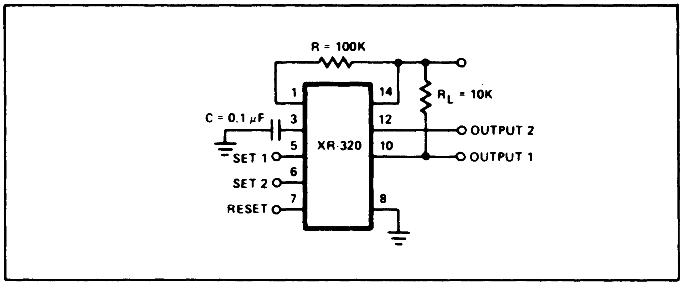


Figure 1. Test Circuit

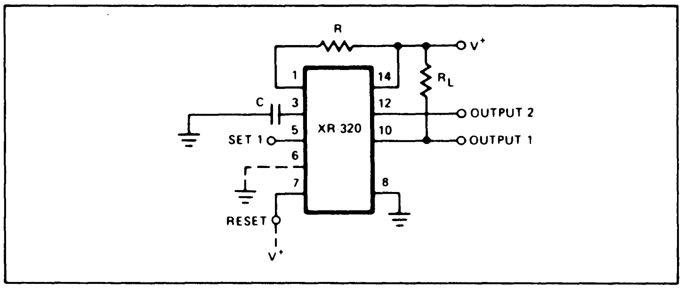


Figure 2. Monostable Operation, Negative Trigger

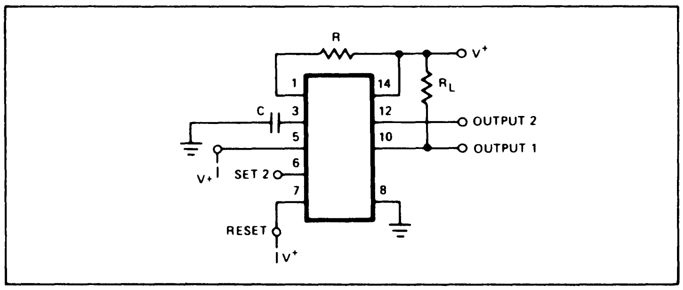


Figure 3. Monostable Operation, Positive Trigger

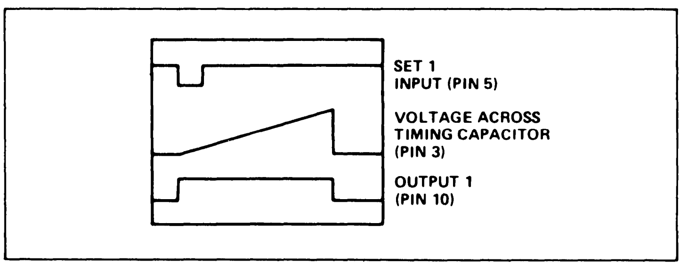


Figure 4. Waveforms for Negative-Going Trigger

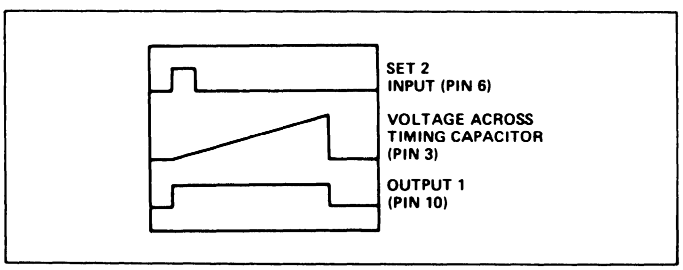


Figure 5. Waveforms for Positive-Going Trigger

OPERATING INSTRUCTIONS

Figures 2 and 3 show typical connections for the XR-320. Only three external components are required for basic operation: the resistor R and capacitor C which determine the time delay (2RC); and an external load resistor, R_L. The circuit provides two independent logic outputs: a medium current output (up to 10 mA) at pin 10, and a high current output (up to 100 mA) at pin 12. The output at pin 10 is of the "bare-collector" type which requires an external pull-up resistor, R_L, connected between this terminal and V^+ for proper circuit operation.

With no trigger pulse applied, the output at pin 10 is in a low state near ground potential; and the output at pin 12 is in a high state, near V^+. The circuit is triggered by the application of a negative-going pulse to pin 5 or a positive-going pulse to pin 6. At that instant, the output levels change state such that pin 10 becomes high and pin 12 low. The outputs will remain in this (switched) state until the delay time, T = 2RC, expires, at which time the outputs will return to their original state. In this mode of operation, the trigger input can be activated repeatedly without further influencing the time cycle, i.e., once the circuit is triggered it becomes immune to subsequent triggering until the entire timing cycle is completed.

For reliable operation, the trigger pulse width must be shorter than the output pulse width. Although many units will function when this rule is not observed, proper operation cannot be guaranteed.

Figure 4 shows the waveforms at various circuit locations for a negative-going trigger applied to pin 5. A similar set of waveforms is displayed in Figure 5 for a positive-going pulse applied to pin 6. The timing cycle can be reset at any time by simply grounding pin 7.

DESCRIPTION OF CIRCUIT CONTROLS

TIMING RESISTOR (PIN 1)

Timing resistor, R, is connected between pin 1 and V^+, pin 14. For maximum timing accuracy, R should be in the range $6\ k\Omega \leq R \leq 1\ M\Omega$. See Figure 6 for the minimum and maximum values for R for various supply voltages.

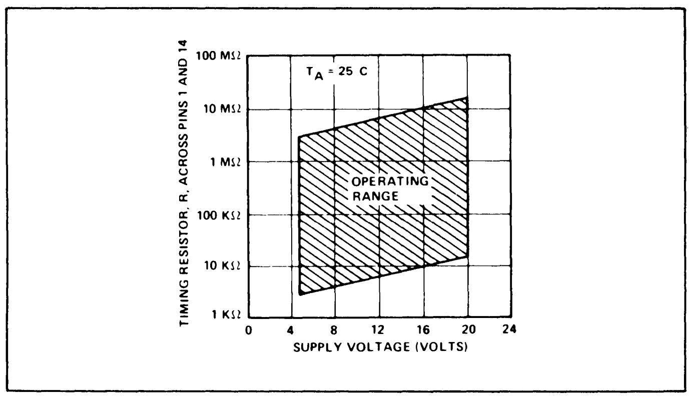


Figure 6. Operating Range as a Function of Timing Resistor and Supply Voltage

TIMING CAPACITOR (PIN 3)

Timing capacitor, C, is connected between pin 3 and ground. The time delay, T, is equal to 2RC in seconds. NOTE: A timing error can result due to the leakage current of the timing capacitor. When a capacitor with a relatively low insulation resistance (e.g. a high-valued electrolytic) is used as the timing capacitor, the resulting delay time will be much longer than 2RC because of the associated leakage current.

SET 1 – NEGATIVE TRIGGER (PIN 5)

A negative-going pulse applied to pin 5 will cause the outputs to change state. Output 1, pin 10, which is normally low will go high, Output 2, pin 12, which is normally high will go low. See Figure 11 for additional details. When not used, pin 5 should be connected to V^+ to avoid false triggering.

SET 2 – POSITIVE TRIGGER (PIN 6)

A positive-going pulse applied to pin 6 will cause the outputs to change state. The normally low output at pin 10 will go high, and the normally high output at pin 12 will go low. See Figure 12 for additional details. When not used, pin 6 should be grounded to avoid false triggering.

RESET (PIN 7)

By grounding or applying a negative pulse to the reset, pin 7, the timing cycle is automatically interrupted and the outputs return to their original state. When the reset function is not in use, it is recommended that it be connected to V^+ to avoid any possibility of false resetting.

ADDITIONAL APPLICATIONS

FREE-RUNNING MODE

By shorting pins 3 and 5, the XR-320 will operate in a "free-running" or self-triggering mode. In this mode of operation, the circuit functions as a stable clock pulse generator with a repetition rate of approximately 1/(2RC). The circuit connection and free-running frequency in this application are shown in Figure 7. Note that one cycle is not precisely equal to 2RC because of capacitor discharge time. Typical waveforms for self-triggered operation are shown in Figure 8.

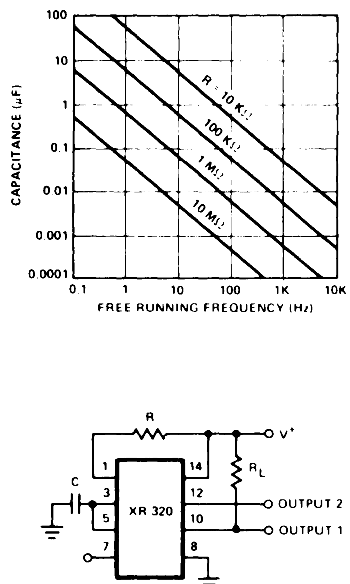


Figure 7. Free-Running Operation

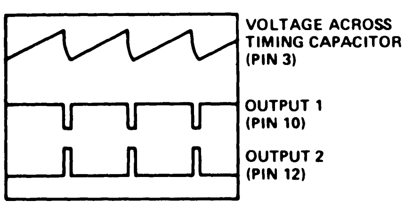


Figure 8. Waveforms for Self-Triggered Operation

SWEEP GENERATION

In self-triggered operation, the waveform across the timing capacitor (at pin 3) is a linear ramp as shown in Figure 8. The waveform at pin 3 can be used as a highly linear sweep voltage with a total nonlinearity of less than 1%.

PULSE-WIDTH MODULATION

For this application, the XR-320 should be connected as shown in Figure 9.

The modulation input is applied to pin 1 through coupling capacitor, C_C. The input signal modulates the current through the timing resistor, R, and, in turn, changes the width of the output timing pulses. The resistor R_M, in series with the signal source, is used to control the amount of modulation for a given input signal level.

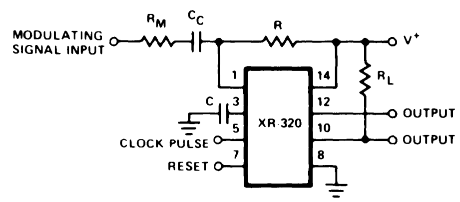


Figure 9. Circuit Connection for Pulse-Width Modulation

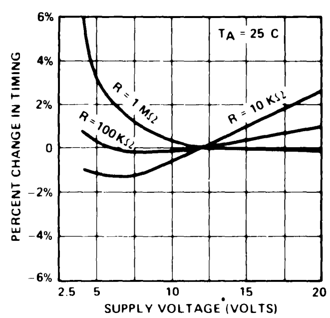


Figure 10. Change in Timing vs. Supply Voltage

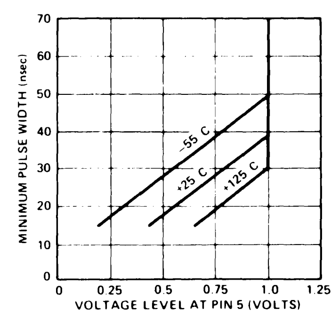


Figure 11. Minimum Pulse Width for Triggering at Pin 5

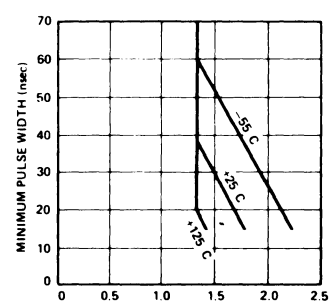


Figure 12. Minimum Pulse Width for Triggering at Pin 6

XR-555
Timing Circuit

GENERAL DESCRIPTION

The XR-555 monolithic timing circuit is a highly stable controller capable of producing accurate timing pulses. It is a direct, pin-for-pin replacement for the SE/NE 555 timer. The circuit contains independent control terminals for triggering or resetting if desired, as shown in the functional block diagram of Figure 1.

In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor (as shown in Figure 2).

The XR-555 may be triggered or reset on falling waveforms. Its output can source or sink up to 200 mA or drive TTL circuits.

FEATURES

- Direct Replacement for SE/NE 555
- Timing from Microseconds Thru Hours
- Operates in Both Monostable and Astable Modes
- High Current Drive Capability (200 mA)
- TTL and DTL Compatible Outputs
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

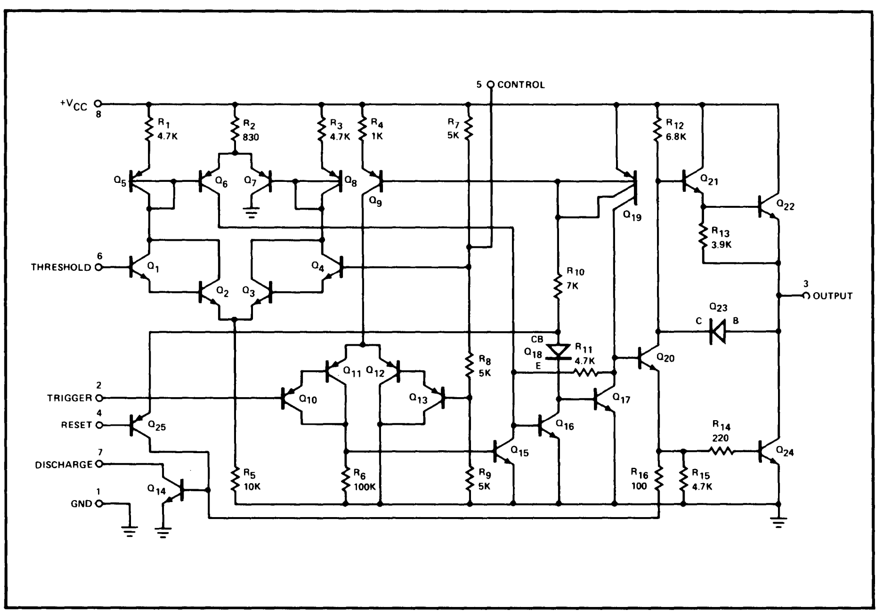
APPLICATIONS

Precision Timing	Missing Pulse Detection
Pulse Generation	Pulse-Width Modulation
Sequential Timing	Frequency Division
Pulse Shaping	Pulse-Position Modulation
Clock Generation	Appliance Timing

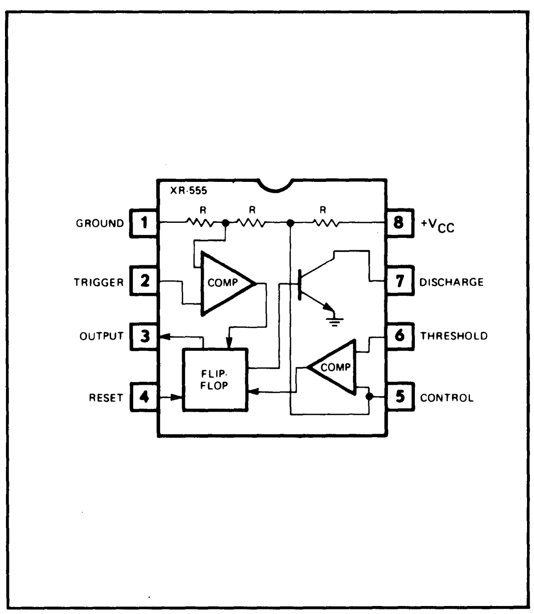
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-555M	Ceramic	−55°C to +125°C
XR-555CM	Ceramic	0°C to +75°C
XR-555CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.)

PARAMETER	XR-555M			XR-555C			UNITS	CONDITION
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	4.5		18	4.5		16	V	
Supply Current								Low State Output (Note 1)
		3	5		3	6	mA	V_{CC} = 5V, $R_L = \infty$
		10	12		10	15	mA	V_{CC} = 15V, $R_L = \infty$
Timing Error (Monostable)								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	2.0		1.0	3.0	%	Note 2, C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	0°C ≤ T_A ≤ 75°C
Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V	
Timing Error (Astable)								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy (Note 2)		1.5			2.25		%	C = 0.1 μF
Drift with Temperature		90			150		ppm/°C	V_{CC} = 15V
Drift with Supply Voltage		0.15			0.3		%/V	
Threshold Voltage	9.4	10.0	10.6	8.8	10.0	11.2	V	V_{CC} = 15V
	2.7	3.33	4.0	2.4	3.33	4.2	V	V_{CC} = 5V
Trigger Voltage	1.45	1.67	1.9		1.67		V	V_{CC} = 5V
	4.8	5.0	5.2		5.0		V	V_{CC} = 15V
Trigger Current		0.5	0.9		0.5	2.0	μA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	Trigger Input High
Reset Current		0.4	1.0		0.4	1.5	mA	
Threshold Current		0.1	0.25		0.1	0.25	μA	(Note 3)
Control Voltage Level	2.7	3.33	4.0	2.4	3.33	4.2	V	V_{CC} = 5V
	9.4	10.0	10.6	8.8	10.0	11.2	V	V_{CC} = 15V
Output Voltage Drop (Low)								V_{CC} = 5V
		0.10	0.25		0.3		V	I_{sink} = 8.0 mA
		0.05	0.2		0.25	0.35	V	I_{sink} = 5.0 mA
								V_{CC} = 15V
		0.1	0.15		0.1	0.25	V	I_{sink} = 10 mA
		0.4	0.5		0.4	0.75	V	I_{sink} = 50 mA
		2.0	2.2		2.0	2.5	V	I_{sink} = 100 mA
		2.5			2.5		V	I_{sink} = 200 mA
Output Voltage Drop (High)								I_{source} = 100 mA
	3.0	3.3		2.75	3.3		V	V_{CC} = 5V
	13	13.3		12.75	13.3		V	V_{CC} = 15V
								I_{source} = 200 mA
		12.5			12.5		V	V_{CC} = 15V
Turn Off Time (Note 4)		0.5	2.0		0.5		μs	V_{RESET} High
Rise Time of Output		100	200		100	300	nsec	
Fall Time of Output		100	200		100	300	nsec	
Discharge Transistor Leakage		20	100		20	100	nA	

Note 1: Supply current when output is high is typically 1.0 mA less.
Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 megohms and for 5V operation, the maximum R_T = 3.4 megohms.
Note 4: Time measured from a positive-going input pulse from 0 to 0.8xV_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

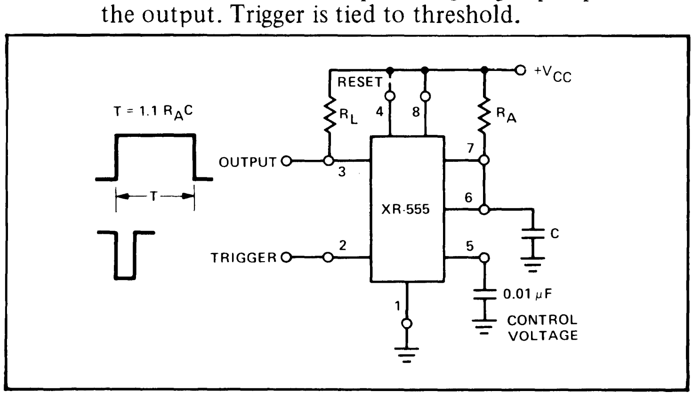


Figure 1. Monostable (One-Shot) Circuit.

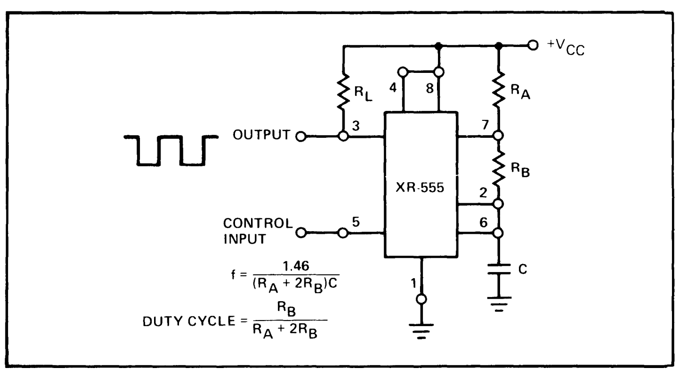


Figure 2. Astable (Free-Running) Circuit.

XR-L555

Micropower Timing Circuit

GENERAL DESCRIPTION

The XR-L555 is a stable micropower controller capable of producing accurate timing pulses. It is a direct replacement for the popular 555-timer for applications requiring very low power dissipation. The XR-L555 has approximately 1/15th the power dissipation of the standard 555-timer and can operate down to 2.7 volts without sacrificing such key features as timing accuracy and frequency stability. At 5-volt operation, typical power dissipation of the XR-L555 is 900 microwatts.

The circuit contains independent control terminals for triggering or resetting if desired, as shown in the functional block diagram (Figure 1). In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor as shown in Figure 2. The XR-L555 is triggered or reset on falling waveforms. Its output can source up to 50 mA or drive TTL circuits.

Because of its temperature stability and low-voltage (2.7V) operation capability, the XR-L555 is ideally suited as a micropower clock oscillator or VCO for low-power CMOS systems. It can operate up to 1500 hours with only two 300 mA-Hr NiCd batteries.

FEATURES

- Pin Compatible with Standard 555 Timer
- Less than 1 mW Power Dissipation (V+ = 5V)
- Timing from Microseconds to Minutes
- Over 1000-Hour Operation with 2 NiCd Batteries
- Low Voltage Operation (V+ = 2.7V)
- Operates in Both Monostable and Astable Modes
- CMOS TTL and DTL Compatible Outputs

APPLICATIONS

- Battery Operated Timing
- Micropower Clock Generator
- Pulse Shaping and Detection
- Micropower PLL Design
- Power-On Reset Controller
- Micropower Oscillator
- Sequential Timing
- Pulse-Width Modulation
- Appliance Timing
- Remote-Control Sequencer

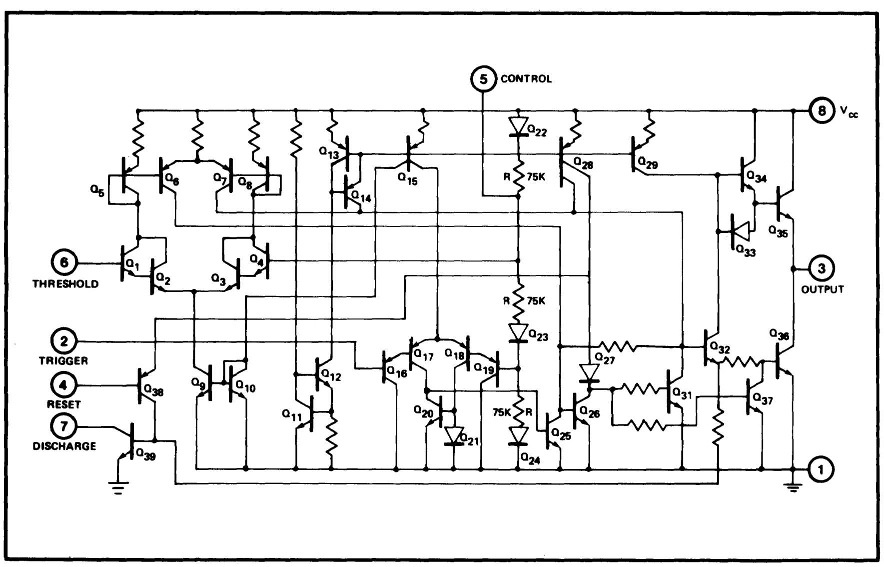
ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

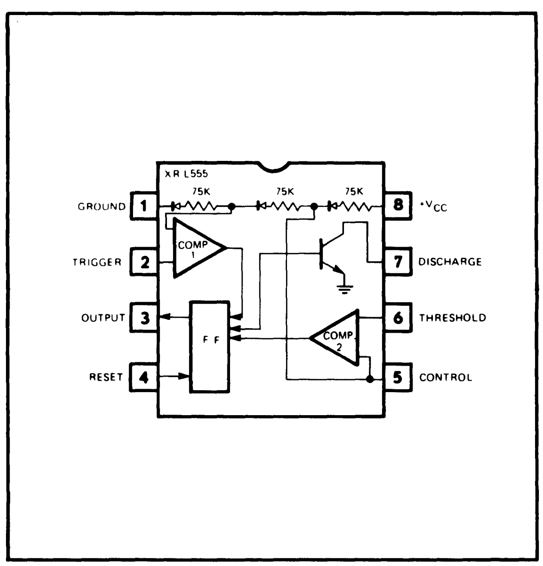
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-L555M	Ceramic	−55°C to +125°C
XR-L555CN	Ceramic	0°C to +75°C
XR-L555CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS – PRELIMINARY

Test Conditions: (T_A = 25°C, V_{CC} = +5V, unless otherwise specified)

PARAMETER	XR-L555M			XR-L555C			UNITS	CONDITION
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	2.7		15	3.0		15	V	
Supply Current		150	300		190	500	μA	Low State Output V_{CC} = 5V, $R_L = \infty$
Timing Error								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	2.0		1.0		%	C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	0°C ≤ T_A ≤ 75°C
Drift with Supply Voltage		0.05			0.05		%/V	
Threshold Voltage		2/3			2/3		x V_{CC}	
Trigger Voltage	1.45	1.67	1.9		1.67		V	V_{CC} = 5V
	4.8	5.0	5.2		5.0		V	V_{CC} = 15V
Trigger Current		0.5			0.5		μA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	
Reset Current		0.1			0.1		mA	
Threshold Current		0.1	0.25		0.1	0.25	μA	
Control Voltage Level	2.90	3.33	3.80	2.60	3.33	4.00	V	V_{CC} = 5V
	9.6	10.0	10.4	9.0	10.0	11.0		V_{CC} = 15V
Output Voltage Drop (Low)		0.1	0.3		0.25	0.35	V	I_{sink} = 1.5 mA
Output Voltage Drop (High)								I_{source} = 10 mA
	3.0	3.3		2.75	3.3		V	V_{CC} = 5V
	13	13.3		12.75	13.3		V	V_{CC} = 15V
								I_{source} = 100 mA
		12.5			12.5		V	V_{CC} = 15V
Rise Time of Output		100			100		nsec	
Fall Time of Output		100			100		nsec	
Discharge Transistor Leakage		0.1			0.1		μA	

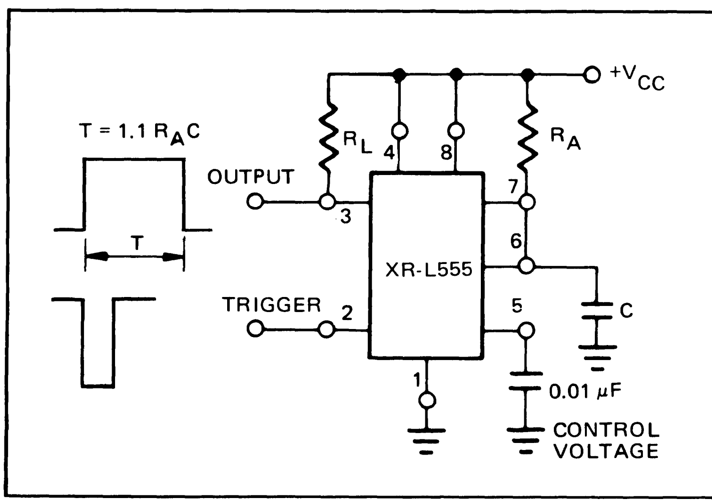


Figure 1. Monostable (One-Shot) Circuit

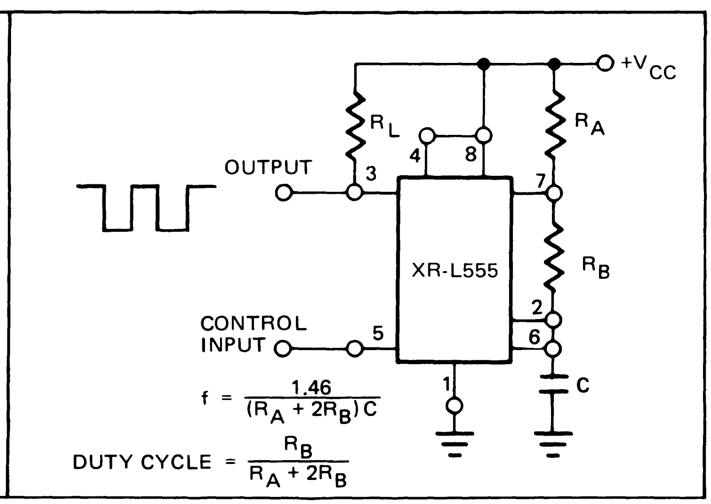


Figure 2. Astable (Free-Running) Circuit

CHARACTERISTIC CURVES

GENERAL CHARACTERISTICS

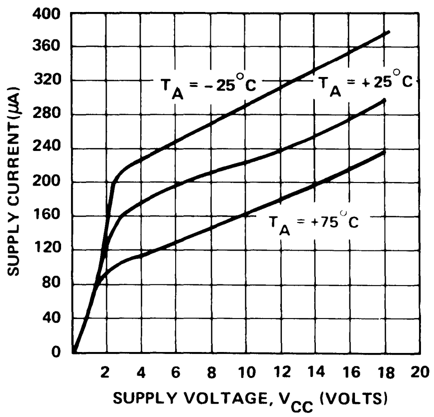


Figure 3. Supply Current as a Function of Supply Voltage

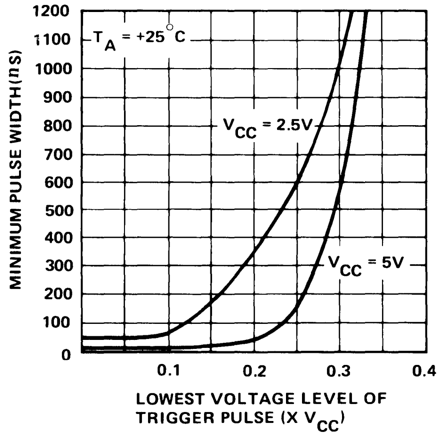


Figure 4. Minimum Pulse-Width Required for Triggering

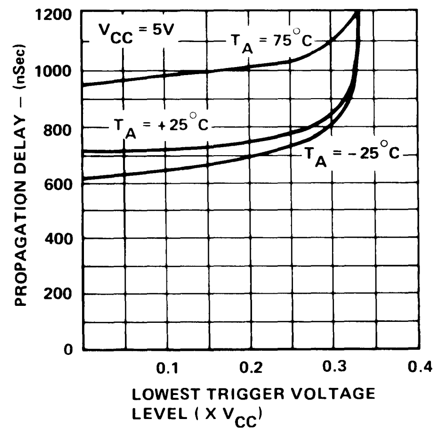


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

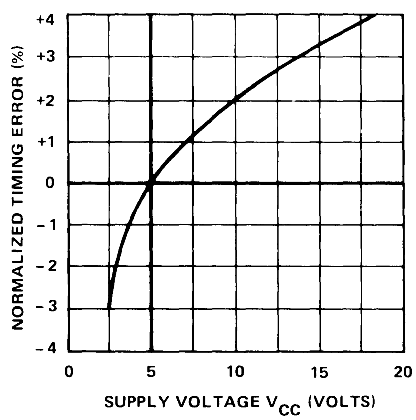


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

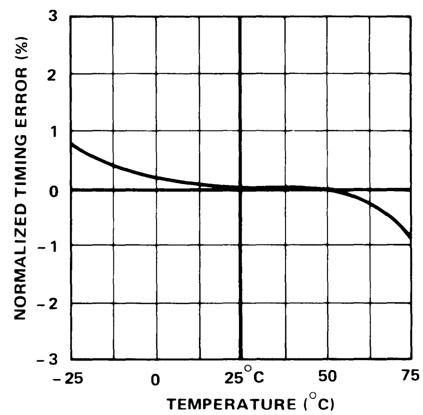


Figure 7. Typical Timing Accuracy as a Function of Temperature
(V_{CC} = 5V, R_A = 100KΩ, C = 0.01μF)

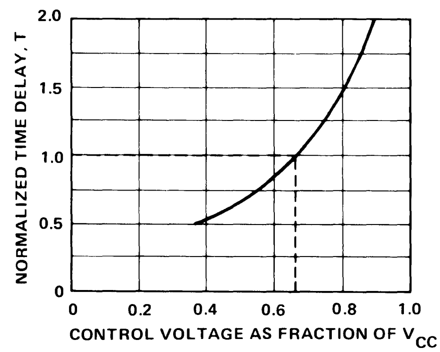


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

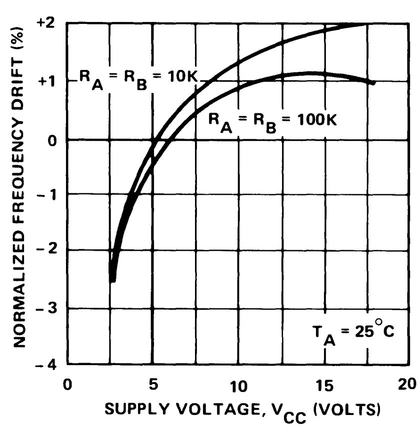


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

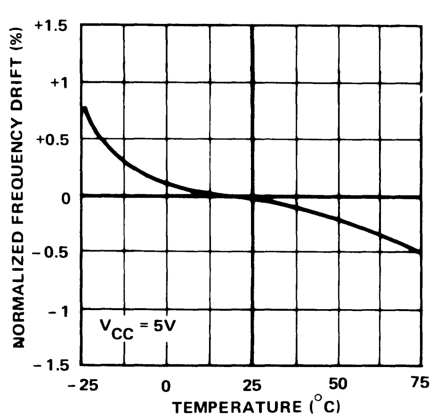


Figure 10. Typical Frequency Stability as a Function of Temperature
(R_A = R_B = 10KΩ, C = 0.1μF)

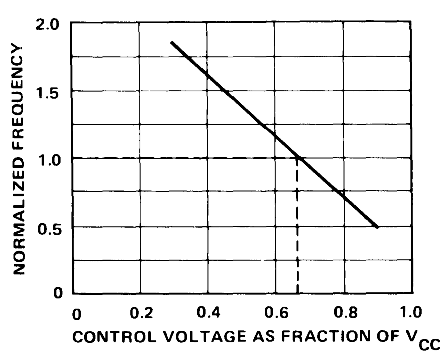


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

FEATURES OF XR-L555

The XR-L555 micropower timer is, in most instances, a direct pin-for-pin replacement for the conventional 555-type timer. However, compared to conventional 555-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 555-timer.

No Supply Current Transients: The conventional 555-timer can produce 300 to 400 mA of supply current spikes during switching. The XR-L555 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L555 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 555-timer. Thus, the XR-L555 can operate safely and reliably with two 1.5V NiCd batteries.

Proven Bipolar Technology: The XR-L555 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

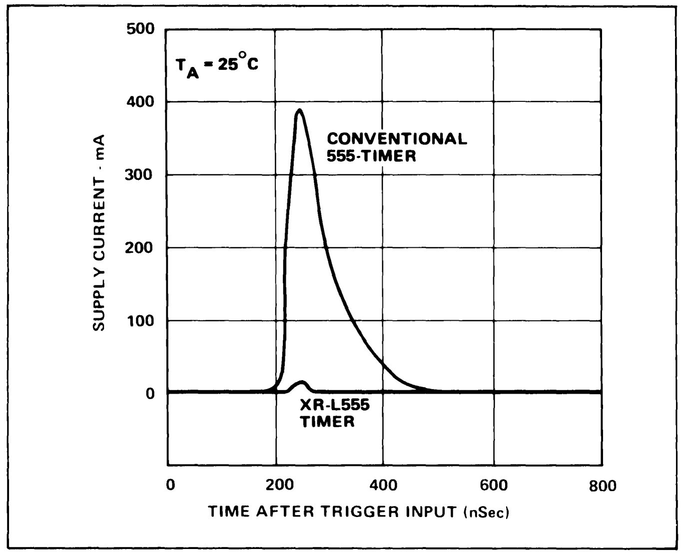


Figure 12. Comparison of Supply Current Transient of Conventional 555-Timer with XR-L555 Micropower Timer

APPLICATIONS INFORMATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation of the XR-L555 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level at pin 2 to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pin 3 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A C$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_A C$$

This time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pin 4). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the parallel combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The oscillations can be keyed "on" and "off" using the reset control. The frequency of oscillation can be readily calculated from the equations in Figure 2 and Figure 14.

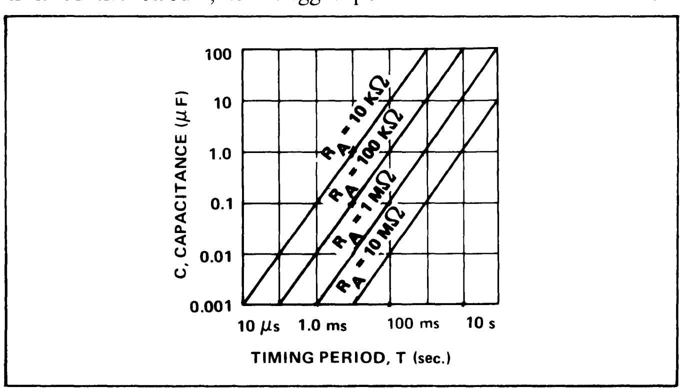


Figure 13. Timing Period, T, as a Function of External R-C Network

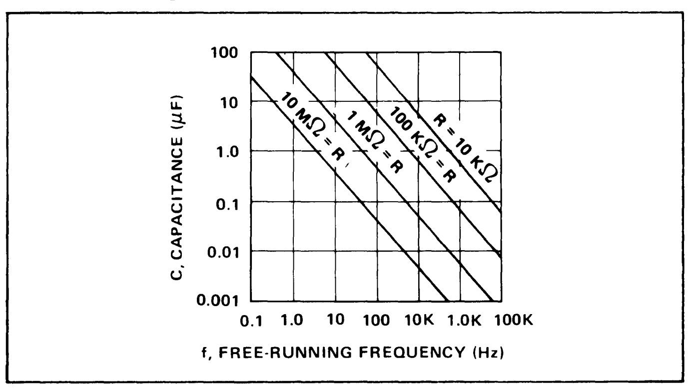


Figure 14. Free Running Frequency as a Function of External Timing Components (Note: $R = R_A + 2R_B$)

XR-556

Dual Timer

GENERAL DESCRIPTION

The XR-556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. It is a direct, pin-for-pin replacement for the SE/NE 556 dual timer. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-556 may be triggered or reset on falling waveforms. Each output can source or sink up to 150 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-556 are superior to those available from two separate timer packages.

FEATURES

Direct Replacement for SE/NE 556
Replaces Two 555-Type Timers
TTL Compatible Pinouts
Timing from Microseconds Thru Hours
Excellent Matching Between Timer Sections
Operates in Both Monostable and Astable Modes
High Current Drive Capability (150 mA each output)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above $T_A = 25°C$	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above $T_A = 25°C$	5 mW/°C
Storage Temperature Range	−65°C to +150°C

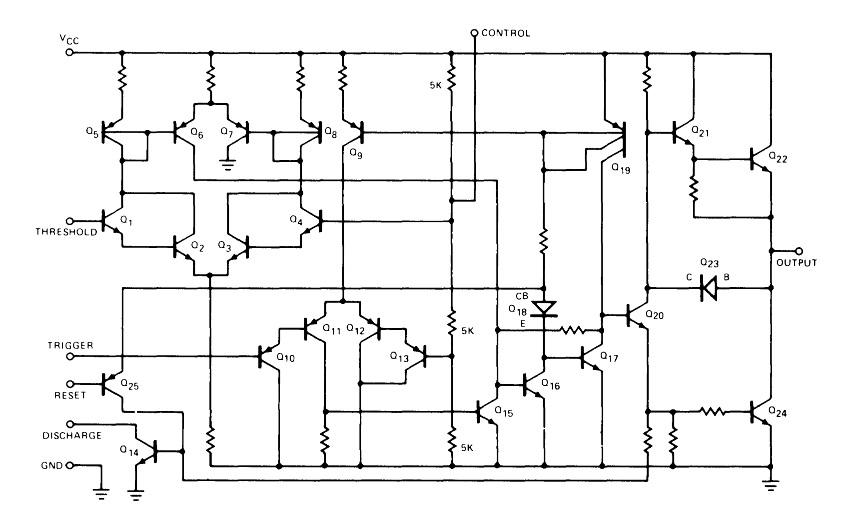
APPLICATIONS

Precision Timing	Missing Pulse Detection
Pulse Generation	Pulse-Width Modulation
Sequential Timing	Frequency Division
Pulse Shaping	Clock Synchronization
Time Delay Generation	Pulse-Position Modulation
Clock Pattern Generation	Appliance Timing

AVAILABLE TYPES

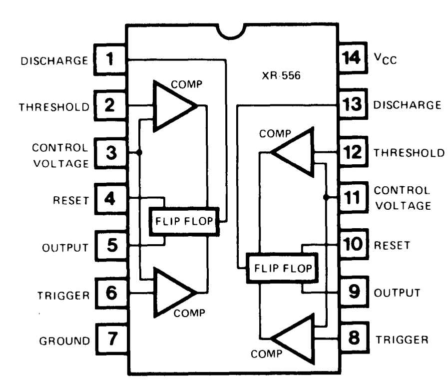
Part Number	Package	Operating Temperature
XR-556M	Ceramic	−55°C to +125°C
XR-556CN	Ceramic	0°C to +75°C
XR-556CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



One Section of XR-556

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: (Each timer section, $T_A = 25^\circ C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified)

PARAMETER	XR-556M			XR-556C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	4.5		18	4.5		16	V	
Supply Current (Each Timer Section)								Low State Output, Note 1
		3	5		3	6	mA	$V_{CC} = 5V$, $R_L = \infty$
		10	11		10	14	mA	$V_{CC} = 15V$, $R_L = \infty$
Total Supply Current (Both Timer Sections)								Low State Output, Note 1
		6	10		6	12	mA	$V_{CC} = 5V$, $R_L = \infty$
		20	22		20	28	mA	$V_{CC} = 15V$, $R_L = \infty$
Timing Error (Monostable)								Timing, R = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	1.5		.75	3	%	Note 2, C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	$0^\circ C \leqslant T_A \leqslant 75^\circ C$
Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V	
Timing Error (Astable)								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy (Note 2)		1.5			2.25		%	C = 0.1 μF
Drift with Temperature		90			150		ppm/°C	$V_{CC} = 15V$
Drift with Supply Voltage		0.15			0.3		%/V	
Threshold Voltage	9.4	10.0	10.6	8.8	10.0	11.2	V	$V_{CC} = 15V$
	2.7	3.33	4.0	2.4	3.33	4.2	V	$V_{CC} = 5V$
Trigger Voltage								
	1.45	1.67	1.9		1.67		V	$V_{CC} = 5V$
	4.8	5.0	5.2	4.5	5.0	5.6	V	$V_{CC} = 15V$
Trigger Current		0.5	0.9		0.5	2	μA	$V_{TRIG} = 0V$
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	V_{TRIG} High
Reset Current		0.4	1		0.4	1.5	mA	$V_{RESET} = 0V$
Threshold Current		0.03	0.1		0.03	0.1	μA	Note 3
Control Voltage Level								
	2.90	3.33	3.80	2.60	3.33	4.00		$V_{CC} = 5V$
	9.6	10.0	10.4	9.0	10.0	11.0		$V_{CC} = 15V$
Output Voltage Drop (Low)								
								$V_{CC} = 5V$
		0.10	0.25		0.3		V	$I_{sink} = 8.0$ mA
		0.05	0.20		0.25	0.35	V	$I_{sink} = 5.0$ mA
								$V_{CC} = 15V$
		0.1	0.15		0.1	0.25	V	$I_{sink} = 10$ mA
		0.4	0.5		0.4	0.75	V	$I_{sink} = 50$ mA
		2.0	2.25		2.0	2.75	V	$I_{sink} = 100$ mA
		2.5			2.5		V	$I_{sink} = 200$ mA
Output Voltage Drop (High)								
								$I_{source} = 100$ mA
	3.0	3.3		2.75	3.3		V	$V_{CC} = 5V$
	13	13.3		12.75	13.3		V	$V_{CC} = 15V$
								$I_{source} = 200$ mA
		12.5			12.5		V	$V_{CC} = 15V$
Rise Time of Output		100	200		100	300	nsec	
Fall Time of Output		100	200		100	300	nsec	
Matching Characteristic								Note 4
Initial Timing Accuracy		0.05	0.1		0.1	0.2	%	
Timing Drift with Temperature		±10			±10		ppm/°C	
Drift with Supply Voltage		0.1	0.2		0.2	0.5	%/V	

Note 1: Supply current when output is high is typically 1.0 mA less.

Note 2: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 10 megohms, and for 5V operation, the maximum R = 3.4 megohms.

Note 4: Matching characteristics refer to the difference between performance characteristics of each timer section.

XR-L556

Micropower Dual Timer

GENERAL DESCRIPTION – PRELIMINARY INFORMATION

The XR-L556 dual timer contains two independent micropower timer sections on a monolithic chip. It is a direct replacement for the conventional 556-type dual timers, for applications requiring very low power dissipation. Each section of the XR-L556 dual timer is equivalent to Exar's XR-L555 micropower timer. The circuit dissipates only 1/15th of the stand-by power of conventional dual timers and can operate down to 2.5 volts without sacrificing such key features as timing accuracy and stability. At 5 volt operation, typical power dissipation of the dual-timer circuit is less than 2 mW; and it can operate in excess of 500 hours with only two 300 mA-Hr NiCd batteries.

The two timer sections of the circuit have separate controls and outputs, but share common supply and ground terminals. Each output can source up to 100 mA of output current or drive TTL circuits.

FEATURES

Replaces two XR-L555 Micropower Timers
Pin Compatible with Standard 556-Type Dual Timer
Less than 1 mW Power Dissipation per Section (V_{CC} = 5V)
Timing from Microseconds to Minutes
Over 500-Hour Operation with 2 NiCd Batteries
Low Voltage Operation (V_{CC} = 2.5V)
Operates in Both Monostable and Astable Modes
CMOS TTL and DTL Compatible Outputs
Introduces No Switching Transients

APPLICATIONS

Battery Operated Timing	Micropower Oscillator
Micropower Clock Generator	Sequential Timing
Pulse Shaping and Detection	Pulse-Width Modulation
Micropower PLL Design	Appliance Timing
Power-On Reset Controller	Remote-Control Sequencer

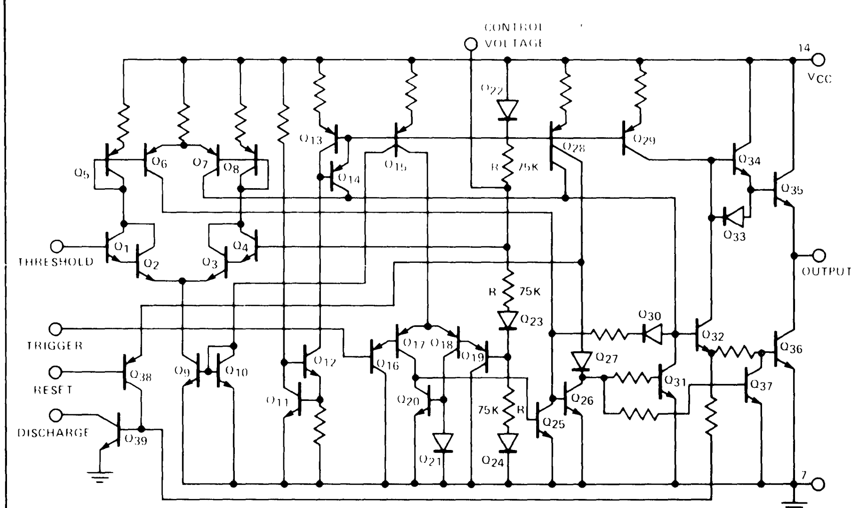
ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

AVAILABLE TYPES

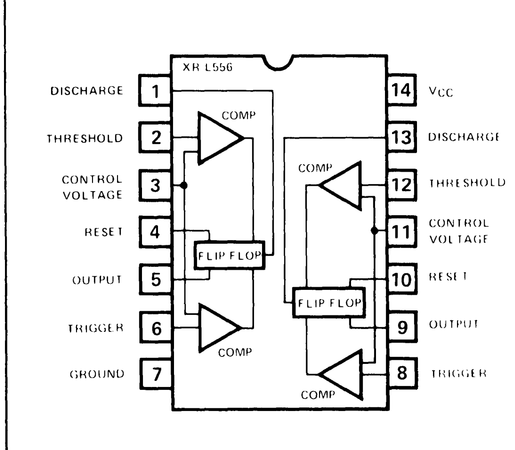
Part Number	Package	Operating Temperature
XR-L556M	Ceramic	-55°C to +125°C
XR-L556CN	Ceramic	0°C to +75°C
XR-L556CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



ONE SECTION OF XR-L556

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS – PRELIMINARY

Test Conditions: ($T_A = 25°C$, $V_{CC} = +5V$, unless otherwise specified)

PARAMETER	XR-L556M			XR-L556C			UNITS	CONDITION
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	2.5		15	2.7		15	V	
Supply Current (Each Timer Section) Total Supply Current (Both Timer Sections)		150 300	300 600		200 400	500 1000	µA µA	Low State Output $V_{CC} = 5V$, $R_L = \infty$
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage		0.5 50 0.5	 200		1.0 50 0.5		% ppm/°C %/V	R_A, R_B = 1 KΩ to 100 KΩ C = 0.1 µF $0°C \leq T_A \leq 75°C$ Monostable Operation
Threshold Voltage		2/3			2/3		x V_{CC}	
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	$V_{CC} = 5V$ $V_{CC} = 15V$
Trigger Current		20			20		nA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	
Reset Current		10			10		µA	
Threshold Current		10	50		20	100	nA	
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0	V V	$V_{CC} = 5V$ $V_{CC} = 15V$
Output Voltage Drop (Low)		0.1	0.3		0.15	0.35	V	$I_{sink} = 1.5$ mA
Output Voltage Drop (High)	 3.0 13 	 3.3 13.3 12.5		 2.75 12.75 	 3.3 13.3 12.5		 V V V	$I_{source} = 10$ mA $V_{CC} = 5V$ $V_{CC} = 15V$ $I_{source} = 100$ mA $V_{CC} = 15V$
Rise Time of Output		200			200		nsec	
Fall Time of Output		100			100		nsec	
Discharge Transistor Leakage		0.1			0.1		µA	

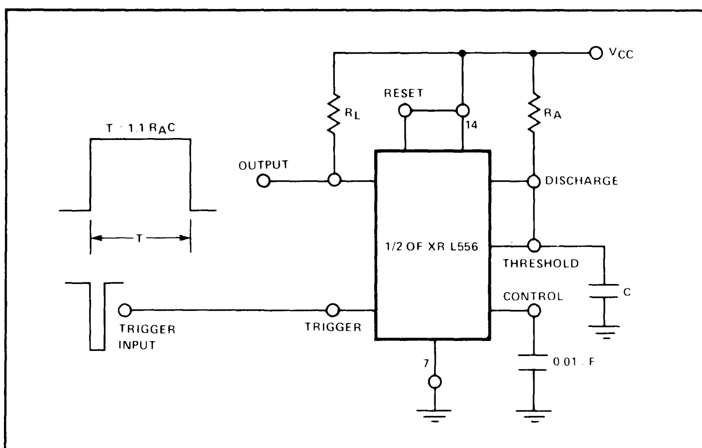


Figure 1. Monostable (One-Shot) Circuit

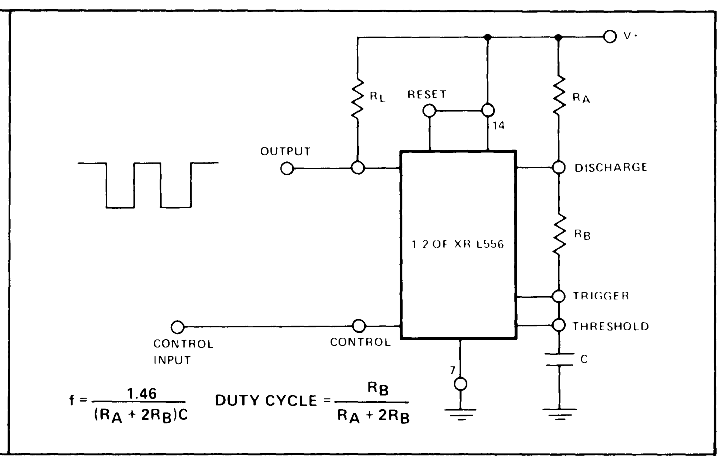


Figure 2. Astable (Free-Running) Circuit

GENERAL CHARACTERISTICS

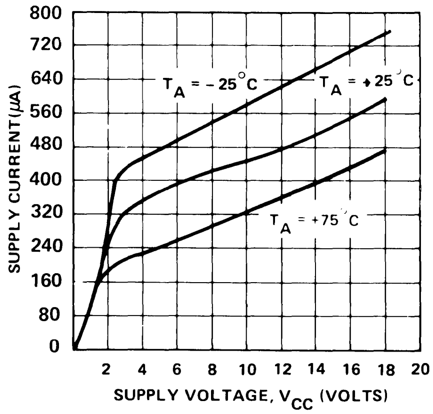


Figure 3. Total Supply Current as a Function of Supply Voltage

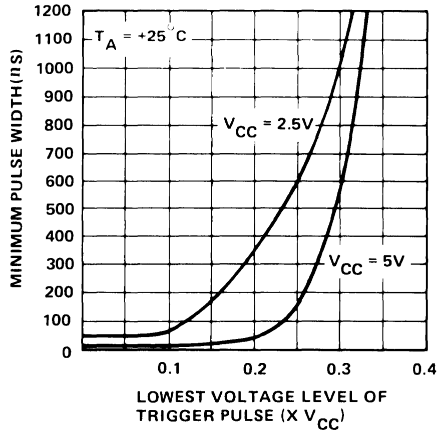


Figure 4. Minimum Pulse-Width Required for Triggering

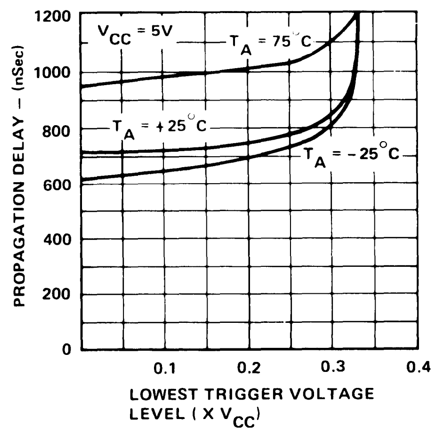


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

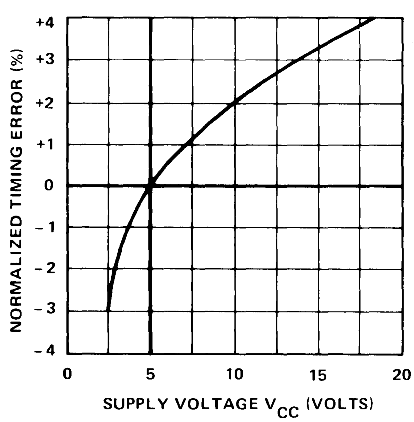


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

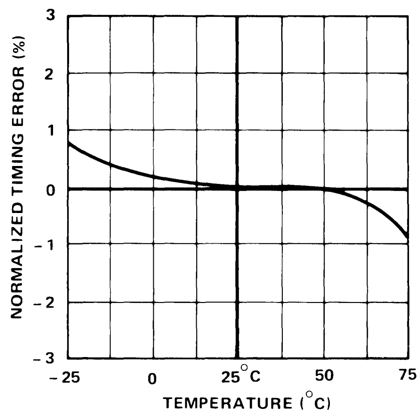


Figure 7. Typical Timing Accuracy as a Function of Temperature (V_{CC} = 5V, R_A = 100KΩ, C = 0.01μF)

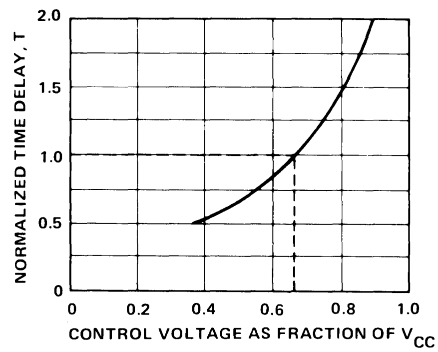


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

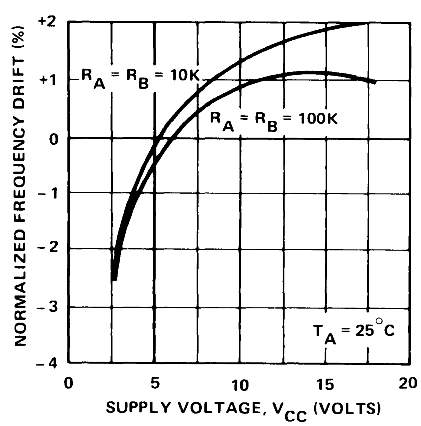


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

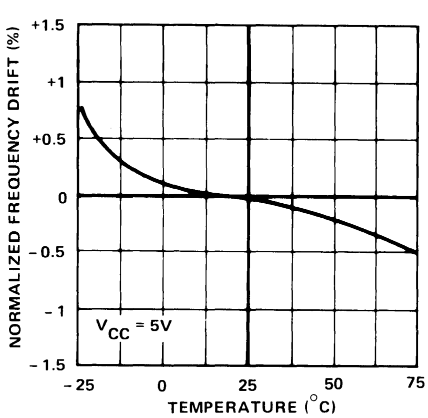


Figure 10. Typical Frequency Stability as a Function of Temperature ($R_A = R_B$ = 10KΩ, C = 0.1μF)

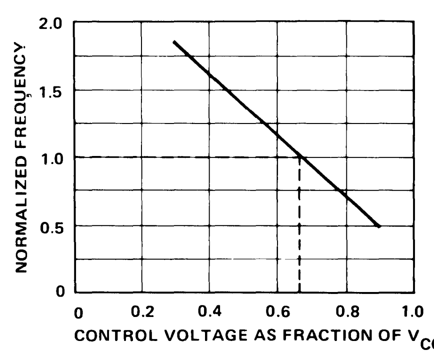


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

FEATURES OF XR-L556

The XR-L556 micropower dual timer is, in most instances, a direct pin-for-pin replacement for the conventional 556-type dual timer. However, compared to conventional 556-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 556-type dual timer.

No Supply Current Transients: The conventional 556-timer can produce 300 to 400 mA of supply current spikes during switching of either one of its timer sections. The XR-L556 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L556 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 556-timer. Thus, the XR-L556 can operate safely and reliably with two 1.5V NiCd batteries.

Proven Bipolar Technology: The XR-L556 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

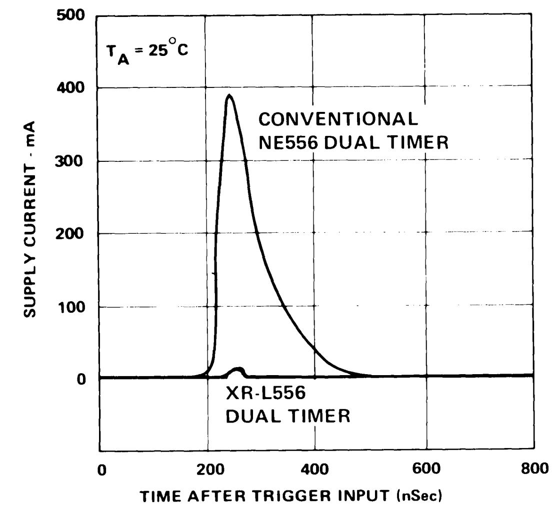


Figure 12. Comparison of Supply Current Transient of Conventional NE556 Dual Timer with XR-L556 Micropower Dual Timer

PRINCIPLE OF OPERATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation of one of the timer sections of the XR-L556 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set, which releases the short circuit across the capacitor and also moves the output level toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_AC$. A comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, the output level moves toward ground and the timing cycle is completed.

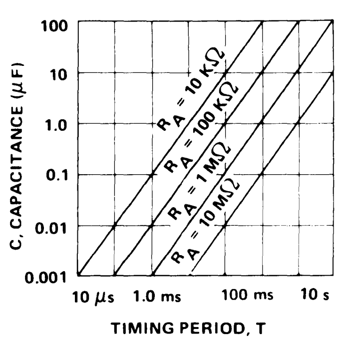


Figure 13. Timing Period, T, as a Function of External R-C Network

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_AC$$

This time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present period has been completed. The timing-cycle can be interrupted by using the reset control. When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the series combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The output level at pin 5 (or 9) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 4 or 10).

The charge time (output high) is given by:

$$t_1 = 0.695\,(R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 = 0.695\,(R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\,(R_A + 1R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \text{ and}$$

may be easily found as shown in Figure 14.

The duty cycle, D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

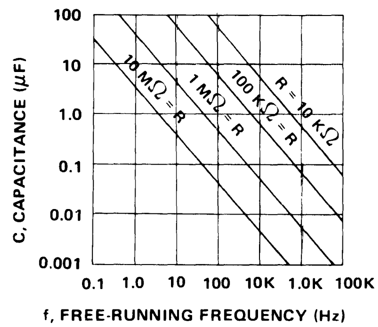


Figure 14. Free Running Frequency as a Function of External Timing Components (Note: $R = R_A + 2R_B$)

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-L556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 15 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\,R_1C_1 \text{ and } T_2 = 1.1\,R_2C_2$$

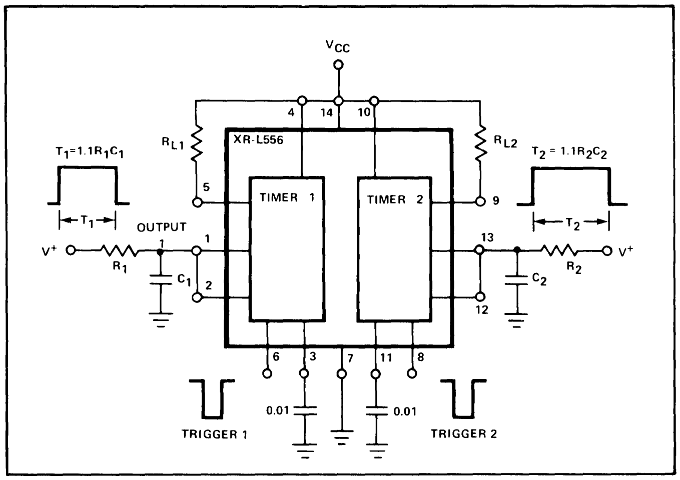


Figure 15. Generation of Two Independent Time Delays

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 16. When Timer 1 is triggered at pin 6, its output at pin 5 goes "high" for a time duration $T_1 = 1.1\,R_1C_1$. At the end of this timing cycle, pin 5 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 5 and 8. Then, the output at pin 9 goes "high" for a time duration $T_2 = 1.1\,R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 6 by a time delay of T_1.

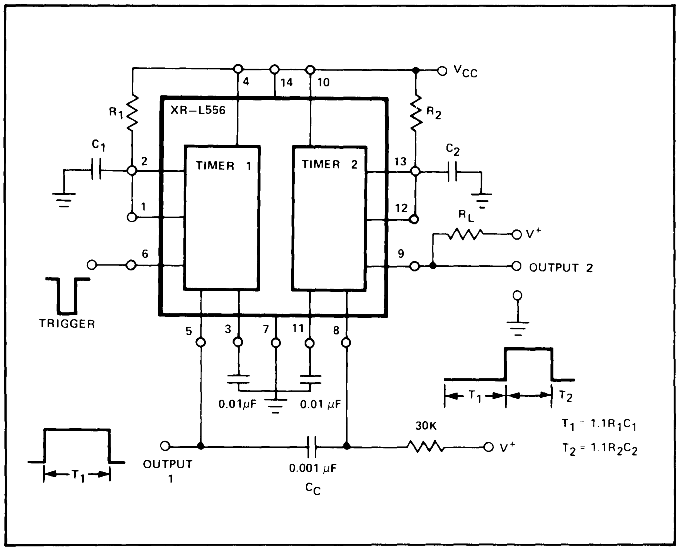


Figure 16. Sequential Timing

KEYED OSCILLATOR

One of the timer sections of the XR-L556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 17. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 10 of Timer 2).

When the circuit is at rest, the logic level at the output of Timer 1 is "low", and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 17.

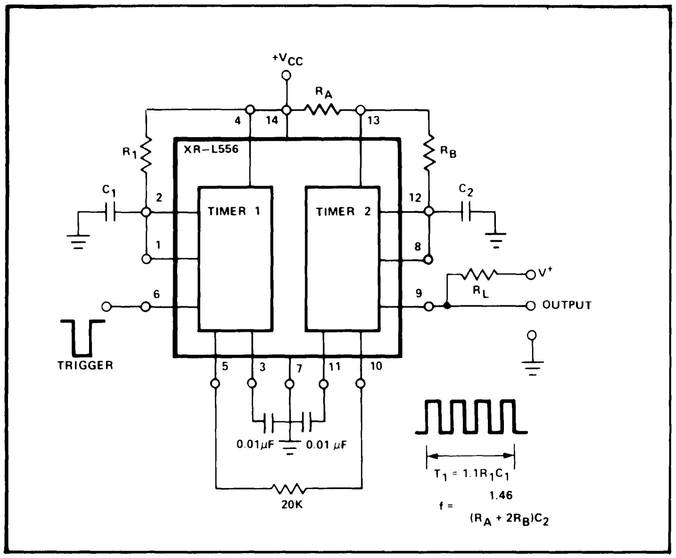


Figure 17. Keyed Oscillator

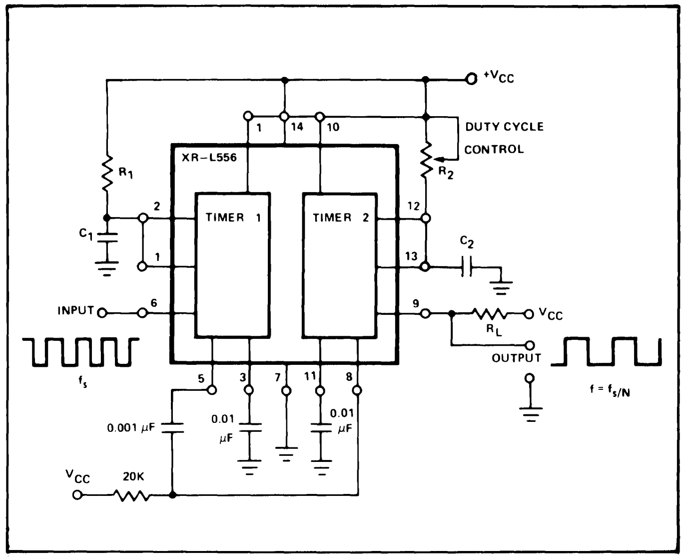


Figure 18. Frequency Divider and Pulse-Shaper

FREQUENCY DIVIDER AND PULSE SHAPER

If the frequency of the input is known, each timer section of the XR-L556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= 1.1 R_1C_1) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than 1.1 R_1C_1 will actually trigger the circuit.

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\frac{T}{Tp} - 1 < N < \frac{T}{Tp}$$

where Tp is the period of the input pulse signal.

Since the two timer sections of the XR-L556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-L556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_s/N_1 \text{ and } f_2 = f_s/N_2$$

where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (1, 2) and (12, 13).

Frequency division can be performed by 1/2 of the XR-L556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 18, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse-shaper.

The output of Timer 1 (pin 5) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 9) can be adjusted from 1% to 99% by varying the value of R_2.

MICROPOWER OSCILLATOR WITH INDEPENDENT FREQUENCY AND DUTY CYCLE ADJUSTMENT

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 19, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 9 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

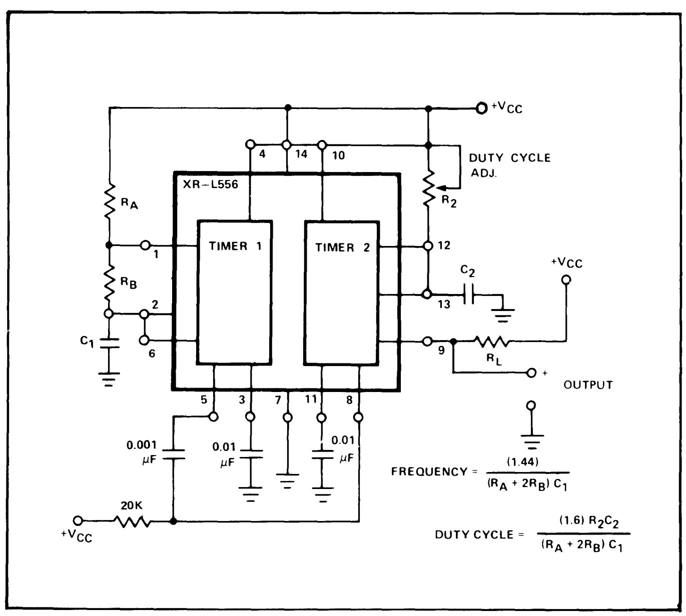


Figure 19. Micropower Oscillator with Fixed Frequency and Variable Duty-Cycle

XR-558/XR-559

Quad Timing Circuits

GENERAL DESCRIPTION – PRELIMINARY INFORMATION

The XR-558 and the XR-559 quad timing circuits contain four independent timer sections on a single monolithic chip. Each of the timer sections on the chip are entirely independent, and each one can produce a time delay from microseconds to minutes, as set by an external R-C network. Each timer has its separate trigger terminal, but all four timers in the IC package share a common reset control.

Both the XR-558 and the XR-559 quad timer circuits are "edge-triggered" devices, so that each timer section can be cascaded, or connected in tandem, with other timer sections, without requiring coupling capacitors.

The XR-558 is designed with open-collector outputs; each output can sink up to 100 mA. The XR-559 is designed with emitter-follower outputs. Each output can source up to 100 mA of load current. The outputs are normally at "low" state, and go to "high" state during the timing interval.

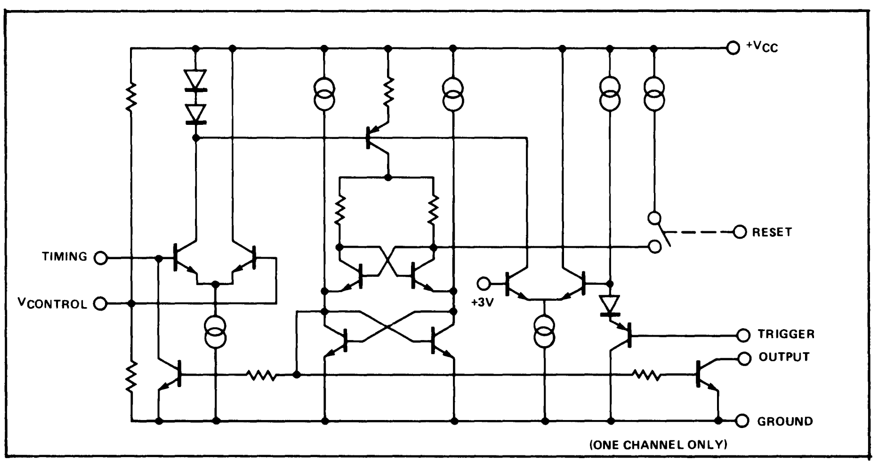
FEATURES

Four Independent Timer Sections
High Current Output Capability
  XR-588: 100 mA sinking capability/output
  XR-559: 100 mA sourcing capability/output
Edge Triggered Controls
Output State Independent of Trigger Condition
Wide Supply Range: 4.5 V to 16 V

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above $T_A = 25°$	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above $T_A = 25°C$	5 mW/°C
Storage Temperature Range	–65°C to +150°C

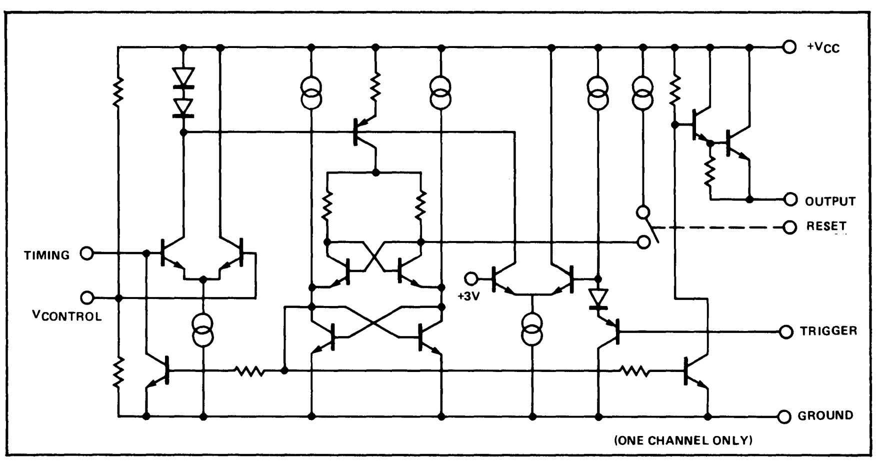
XR-558 EQUIVALENT SCHEMATIC

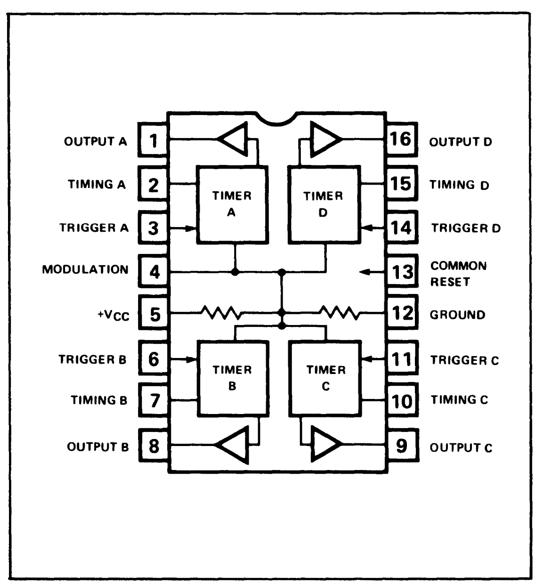


AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-558M	Ceramic	–55°C to +125°C
XR-558 CN	Ceramic	0°C to +75°C
XR-558 CP	Plastic	0°C to +75°C
XR-559 M	Ceramic	–55°C to +125°C
XR-559 CN	Ceramic	0°C to +75°C
XR-559 CP	Plastic	0°C to +75°C

XR-559 EQUIVALENT SCHEMATIC





ELECTRICAL CHARACTERISTICS – PRELIMINARY INFORMATION

Test Conditions: (T_A = 25°C, V_{CC} = +5 V to +15 V, unless otherwise noted.)

PARAMETERS	X558M/XR-559M			XR-558C/XR-559C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	4.5		18	4.5		16	V	
Supply Current								$V_{CC} = V_{RESET}$ = 15V
XR-558 Family		21	32		27	36	mA	Outputs Open
XR-559 Family		9	16		12	18	mA	Outputs Open
Timing Accuracy								R = 2 kΩ to 100 kΩ
Initial Accuracy		1	3		2		%	C = 1 μF
Drift with Temperature		150			150		ppm/°C	
Drift with Supply Voltage		0.1			0.1		%/V	
Trigger Characteristics								See Note: 1
Trigger Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	V_{CC} = 15V
Trigger Current		5	30		10	100	μA	$V_{TRIGGER}$ = 0V
Reset Characteristics								
Reset Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	See Note: 2
Reset Current		50	300		50		μA	
Threshold Characteristics								Measured at Timing Pins
Threshold Voltage		0.63			0.63		X V_{CC}	(Pins 2, 7, 10 or 15)
Threshold Leakage		15			15		nA	
XR-558 Output Characteristics								See Note: 3
Output Voltage		0.1	0.2		0.1	0.4	V	I_L = 10 mA
Output Voltage		0.7	1.5		1.0	2.0	V	I_L = 100 mA
Output Leakage		10			10		nA	Output High Condition
XR-559 Output Characteristics								See Note: 4
Output Voltage	13	13.6		12.5	13.3		V	I_L = 10 mA, V_{CC} = 15V
Output Voltage	12.5	13.3		12.0	13.0		V	I_L = 100 mA, V_{CC} = 15V
Propagation Delay								
XR-558 Family		1.0			1.0		μsec	
XR-559 Family		0.4			0.4		μsec	
Output Rise-time		100			100		nsec	I_L = 100 mA
Output Fall-time		100			100		nsec	I_L = 100 mA

NOTES:

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The XR-558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.
4. The XR-559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

DESCRIPTION OF CIRCUIT OPERATION

The XR-558/559 quad timing circuits are designed to be used in timing applications ranging from few microseconds up several hours. They provide cost-effective alternative to single-timer IC's in applications requiring a multiplicity of timing or sequencing functions.

Each quad-timer circuit contains four independent timer sections, where each section can generate a time delay set by its own resistor and capacitor, external to the IC. All four timing sections can be used simultaneously, or can be interconnected in tandem, for sequential timing applications. For astable operation, two sections of the quad-timer IC can be interconnected to provide an oscillator circuit whose duty-cycle can be adjusted from close to zero, to nearly 100%.

The generalized test and evaluation circuit for both the XR-558 and the XR-559 quad timer circuits is shown in Figure 1. Note that, the only difference between the two circuit types is the structure of the output circuitry.

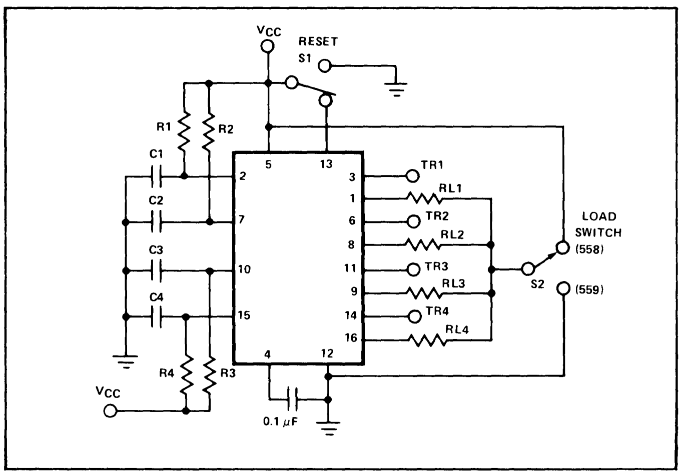


Figure 1. Generalized Test and Evaluation Circuit for XR-558 /XR-559 Quad Timer Circuits

MONOSTABLE OPERATION

In the monostable, or one-shot mode of operation, it is necessary to supply two external components, a resistor and a capacitor, for each section of the timer IC. The timing terminals of those timer-sections not being used can be left open-circuited. The time period is equal to the external RC product. A plot of the timing period, T, as a function of the external R-C combination is shown in Figure 2.

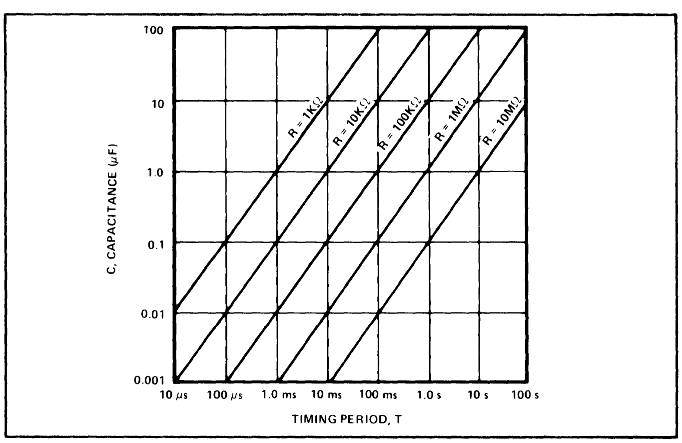


Figure 2. Timing Period, T, as a Function of External R-C Combination (Note: T = 1.0 RC)

ASTABLE OPERATION

For astable, or free-running, operation of the quad timer circuits, it is desirable to cross-couple two of the timer sections on the chip, as shown in Figure 3. In this circuit configuration, the outputs of each section are direct-coupled to the opposite trigger input. Thus, the "high" and "low" half-periods of the output can be set by the external R-C products, as R_1C_1 and R_2C_2, respectively. The frequency of oscillation, and the output duty-cycle are given as:

$$\text{Frequency of Oscillation} = \frac{1}{R_1 C_1 + R_2 C_2}$$

$$\text{Output Duty-Cycle} = \frac{R_2C_2}{R_1C_1 + R_2C_2}$$

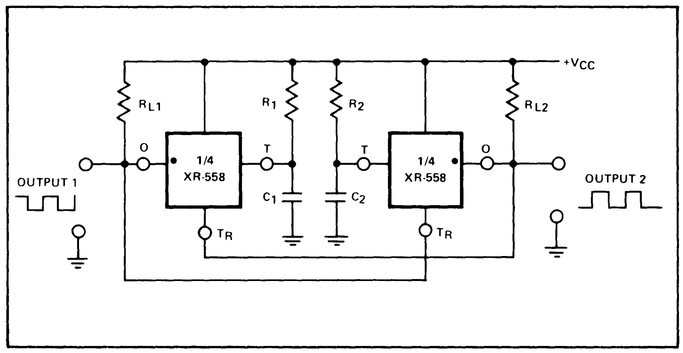


Figure 3. Typical Circuit Connection for Astable Operation Using Two Timer-Sections. (Note: For XR-559, R_{L1} and R_{L2} are Connected from Outputs to Ground.)

The frequency of oscillation can be externally controlled by applying a control-voltage to the control terminal (pin 4). Since the control terminal is common to all the timer sections, the duty cycle of the output waveform is not effected by the modulation voltage; thus the circuit can function as a variable-frequency, fixed duty-cycle oscillator.

The frequency of oscillation increases as the voltage at the control terminal (pin 4) is lowered below its open-circuit value.

OUTPUT STRUCTURE

The XR-558 family of quad timers have "open-collector" NPN-type output stages. Each output can individually sink up to 100 mA of load current. However, with more than one output active, the total current capability is limited by the power-dissipation rating of the IC package (see Absolute Maximum Ratings). In the normal operation of the circuit, each output will require a pull-up resistor to $+V_{CC}$. The output is normally "low" state (i.e. sinking current) when the timer is at reset; and goes to "high" state during the timing cycle.

The XR-559 family of quad timers have Darlington NPN "emitter-follower" type outputs. Each output can source up to 100 mA, during its "high" state. The total amount of output current, available from all outputs, is limited by the package power dissipation rating. For normal operation of the circuit, a pull-down resistor is required from each output to ground. The output of XR-559 is normally low (i.e. at "off-state"), and goes to "high" state when the circuit is triggered.

TRIGGER INPUTS

Each timer section of the quad-timer IC's has its own trigger input. The trigger level is set at nominally +1.5 V, and the trigger input is *edge-triggered* on the falling edge of an input trigger pulse. In other words, for proper triggering, the trigger signal must first go "high" and then go "low". If both the trigger and the reset controls are activated, the reset control overides the trigger input.

RESET INPUT

The reset control (pin 13) is common to all four timer section and resets all of the timer sections simultaneously.

The reset voltage must be brought below 0.8 V to insure reset condition. When reset is activated, all the outputs go to "low" state. While the reset is active, the trigger inputs are inhibited. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

CONTROL VOLTAGE

The control voltage terminal (pin 4) is common to all four timer sections of the XR-558 or the XR-559. This terminal allows the internal threshold voltages of all four timer sections to be modulated, and thus provides the control of the pulse-width or the duty-cycle of the output waveforms. The range of this control voltage is from 0.5 V to $+V_{CC}$ minus 1 Volt. This range provides an over-all timing variation of approximately 50:1. Since the time period of each timer section is proportional to the control voltage, all four timing periods can be simultaneously varied, and their relative ratios remain unchanged over the adjustment range.

APPLICATIONS EXAMPLE

Sequential Timer:

Figure 4 shows a typical application for the quad-timer in sequential timing application. For illustration purposes, the XR-558 is used in the example. Note that, when triggered, the circuit produces four sequential time delays, where the duration of each output is independently controlled by its own R-C time constant. Yet, all four outputs can be modulated over a 50:1 range, and remain proportional over this entire range. Since each timer section is edge-triggered, the sections can be cascaded by direct coupling of respective outputs and trigger inputs.

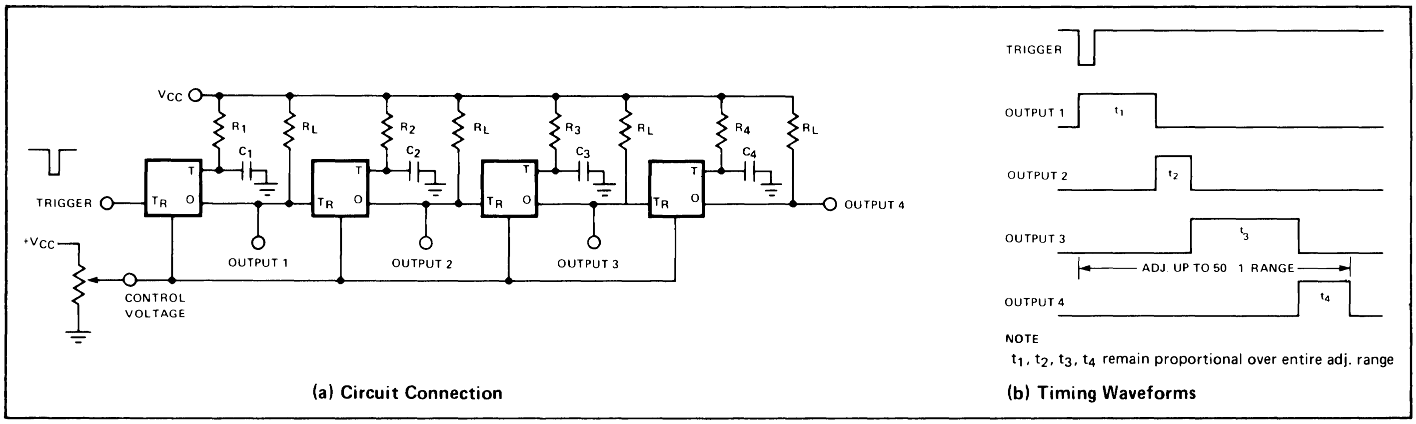


Figure 4. Using the XR-558 as a Four-Stage Sequential Timer with Voltage Control Capability

XR-2556

Dual Timing Circuit

GENERAL DESCRIPTION

The XR-2556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-2556 may be triggered or reset on falling waveforms. Each output can source or sink up to 200 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-2556 are superior to those available from two separate timer packages.

FEATURES

Replaces Two 555-Type Timers
TTL Compatible Pinouts (Gnd – Pin 7, V_{CC} – Pin 14)
Timing from Microseconds Thru Hours
Excellent Matching Between Timer Sections
Operates in Both Monostable and Astable Modes
High Current Drive Capability (200 mA each output)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C
Normally ON and Normally OFF Outputs

APPLICATIONS

Precision Timing	Missing Pulse Detection
Pulse Generation	Pulse-Width Modulation
Sequential Timing	Frequency Division
Pulse Shaping	Clock Synchronization
Time Delay Generation	Pulse-Position Modulation
Clock Pattern Generation	

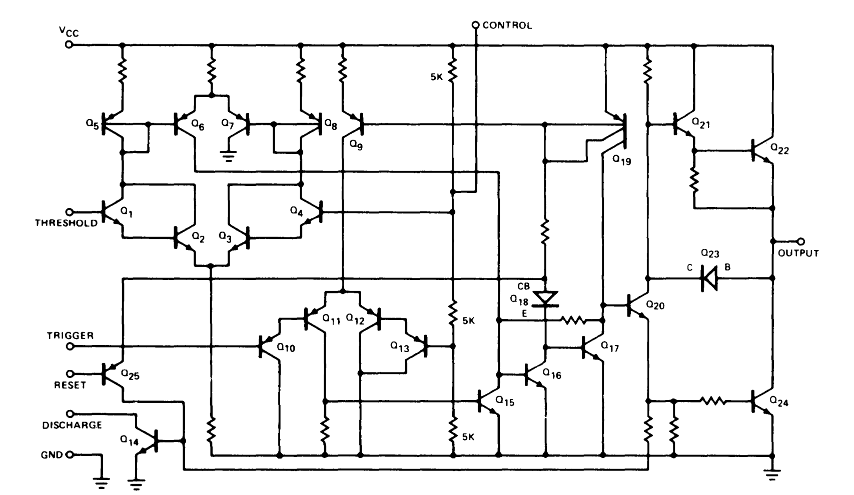
ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	5 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

ORDER INFORMATION

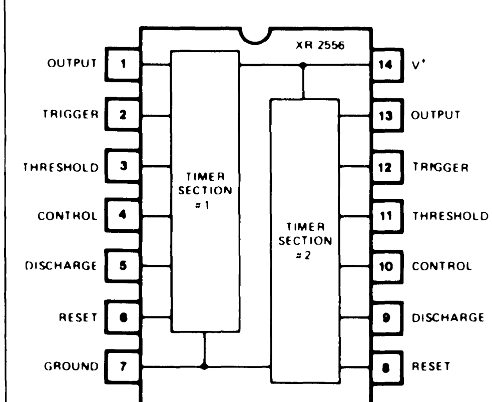
Part Number	Package	Operating Temperature
XR-2556M	Ceramic	–55°C to +125°C
XR-2556CN	Ceramic	0°C to +75°C
XR-2556CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



One section of XR-2556

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	XR-2556M			XR-2556C			UNITS	FIGURE	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Test Conditions: (Each timer section, $T_A = 25°C$, V_{CC} = +5V to +15V, unless otherwise specified)									
Supply Voltage	4.5		18	4.5		16	V	7	
Supply Current (Each Timer Section)								7	Low State Output, Note 1
		3	5		3	6	mA		$V_{CC} = 5V$, $R_L = \infty$
		10	12		10	15	mA		$V_{CC} = 15V$, $R_L = \infty$
Total Supply Current								7	Low State Output
(Both Timer Sections)		6	10		6	12	mA		$V_{CC} = 5V$, $R_L = \infty$
		20	24		20	30	mA		$V_{CC} = 15V$, $R_L = \infty$
Timing Error									R_A, R_B = 1 kΩ to 100 kΩ
Initial Accuracy		0.5	2.0		1.0		%		Note 2, C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	13	
Drift with Supply Voltage		0.05	0.1		0.05		%/V	12	
Threshold Voltage		2/3			2/3		x V_{CC}		
Trigger Voltage									
	1.45	1.67	1.9		1.67		V	6	$V_{CC} = 5V$
	4.8	5.0	5.2		5.0		V		$V_{CC} = 15V$
Trigger Current		0.5			0.5		μA		
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V		
Reset Current		0.1			0.1		mA		
Threshold Current		0.1	0.25		0.1	0.25	μA		Note 3
Control Voltage Level									
	2.90	3.33	3.80	2.60	3.33	4.00			$V_{CC} = 5V$
	9.6	10.0	10.4	9.0	10.0	11.0			$V_{CC} = 15V$
Output Voltage Drop (Low)									
								9	$V_{CC} = 5V$
		0.10	0.25				V		I_{sink} = 8.0 mA
					0.25	0.35	V		I_{sink} = 5.0 mA
								11	$V_{CC} = 15V$
		0.1	0.15		0.1	0.25	V		I_{sink} = 10 mA
		0.4	0.5		0.4	0.75	V		I_{sink} = 50 mA
		2.0	2.2		2.0	2.5	V		I_{sink} = 100 mA
		2.5			2.5		V		I_{sink} = 200 mA
Output Voltage Drop (High)								8	
									I_{source} = 100 mA
	3.0	3.3		2.75	3.3		V		$V_{CC} = 5V$
	13	13.3		12.75	13.3		V		$V_{CC} = 15V$
									I_{source} = 200 mA
		12.5			12.5		V		$V_{CC} = 15V$
Rise Time of Output		100			100		nsec		
Fall Time of Output		100			100		nsec		
Matching Characteristics									Note 4
Initial Timing Accuracy		0.2	0.6		0.2		%		
Timing Drift with Temperature		±10			±10		ppm/°C		

Note 1: Supply current when output is high is typically 1.0 mA less.
Note 2: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 meg-ohms.
Note 4: Matching characteristics refer to the difference between performance characteristics of each timer section.

PRINCIPLE OF OPERATION

Figure 2 is the functional block diagram for each timer section of the XR-2556. These sections share the same V^+ and ground leads, but have independent outputs and control terminals. Therefore, each timer section can operate independently of the other. The timing cycle of each section is determined by an external resistor-capacitor network.

MONOSTABLE (ONE-SHOT) OPERATION

When operating either timer section of the XR-2556 in the monostable mode, a single resistor and a capacitor are used to set the timing cycle. The discharge and threshold terminals are also interconnected in this mode, as shown in Figure 3 .

Referring to Figure 2, monostable operation of the XR-2556 is explained as follows: the external timing capacitor C is held discharged by the internal transistor, T_O. The internal flip-flop is triggered by lowering the trigger levels (pins 2 or 12) to less than 1/3 V_{CC}. The circuit triggers on a *negative-going* slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pins 1 or 13 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal interval resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

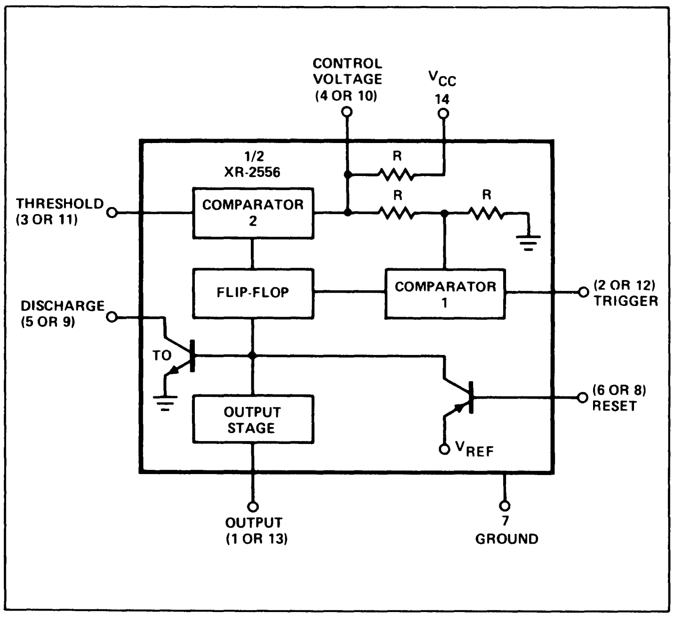


Figure 2. Functional Diagram of One Timer Section

Once the circuit is triggered it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pins 6 or 8). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to V^+ when not used to avoid the possibility of false triggering.

Figure 4 shows the waveforms during the monostable timing cycle. The top waveform is the trigger pulse; the middle is the exponential ramp across the timing capacitor. The bottom waveform is the output logic state (at pins 1 or 13) during the timing cycle. For proper operation of the circuit, the trigger pulse-width must be less than the timing period.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\, R_A C$$

This time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 5 .

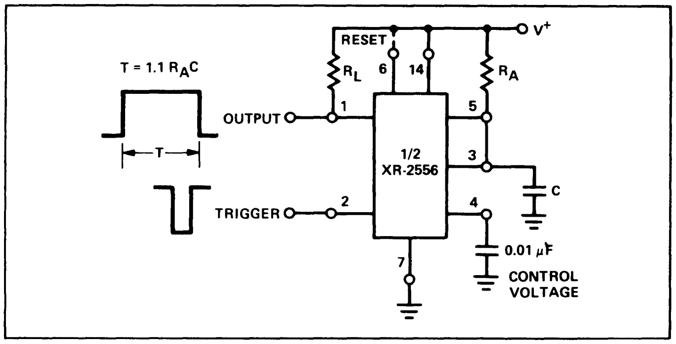


Figure 3. Monostable (One-Shot) Circuit

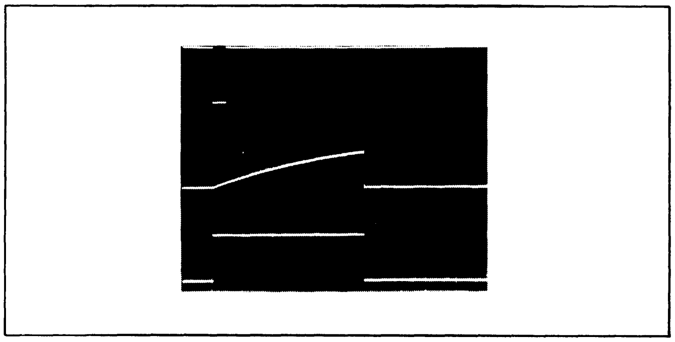


Figure 4. Monostable Waveforms
Top: Trigger Input
Middle: Exponential Ramp across Timing Capacitor
Bottom: Output Logic Level

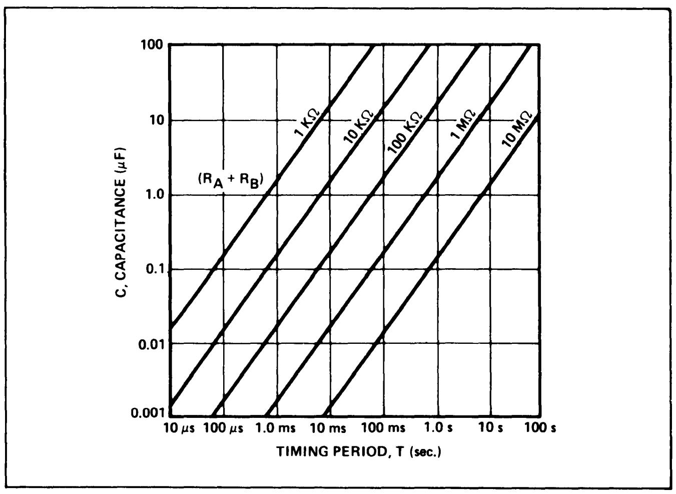


Figure 5. Timing Period, T, as a Function of External R-C Network

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 15. The external capacitor charges to 2/3 V_{CC} through the parallel combination of R_A and R_B, and discharges to 1.3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with the exponential waveform as shown in Figure 16. The output level at pin 1 (or 13) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 6 or 8).

TYPICAL CHARACTERISTICS (Each Timer Section)

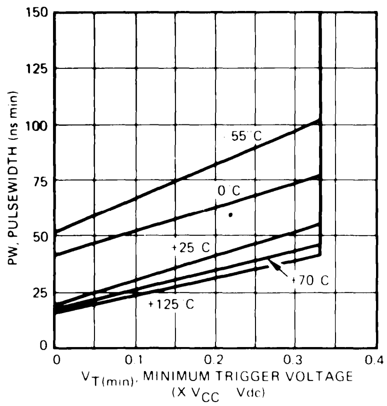


Figure 6. Trigger Pulse Width

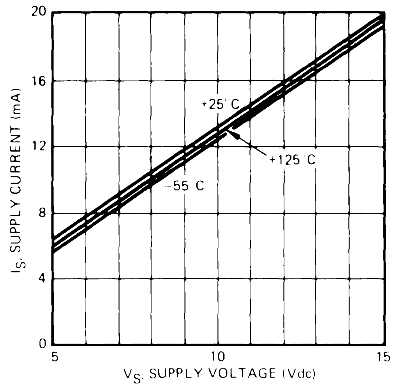


Figure 7. Supply Current (Both Timer Sections)

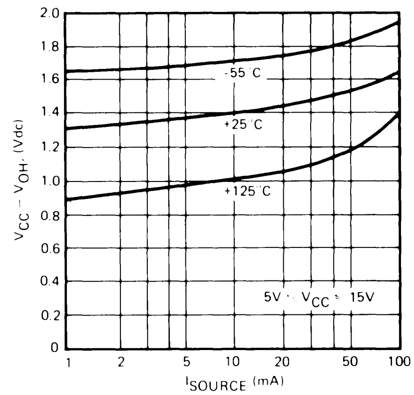


Figure 8. High Output Voltage

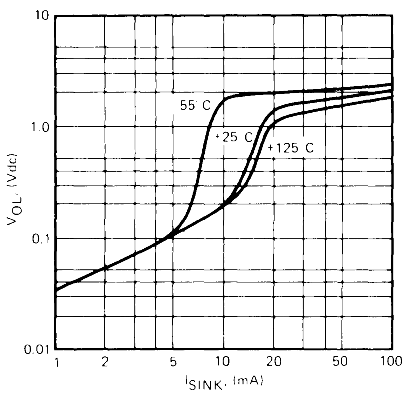


Figure 9. Low Output Voltage V_{CC} = 5.0 Vdc

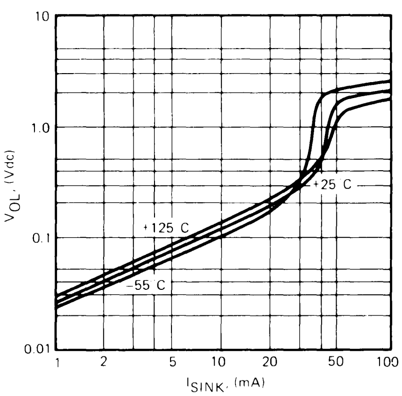


Figure 10. Low Output Voltage V_{CC} = 10 Vdc

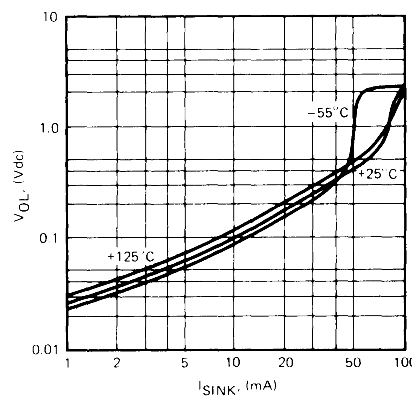


Figure 11. Low Output Voltage V_{CC} = 15 Vdc

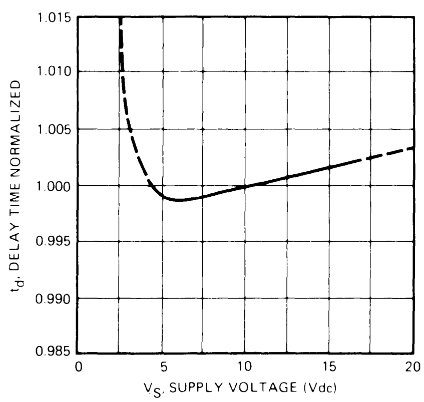


Figure 12. Delay Time vs. Supply Voltage

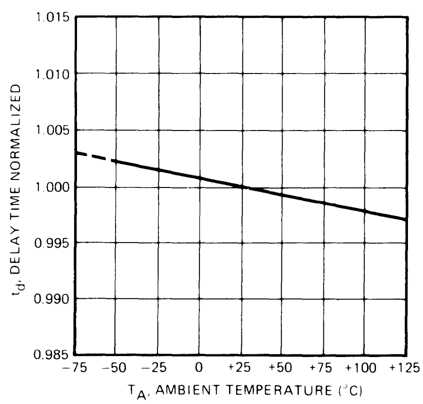


Figure 13. Delay Time vs. Temperature

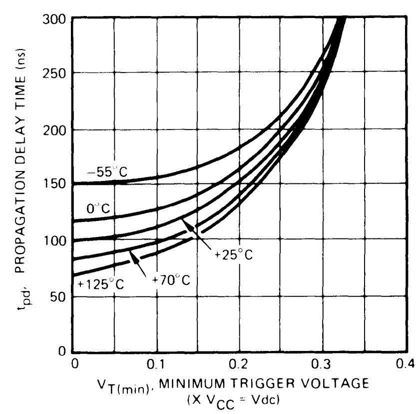


Figure 14. Propagation Delay vs. Trigger Voltage

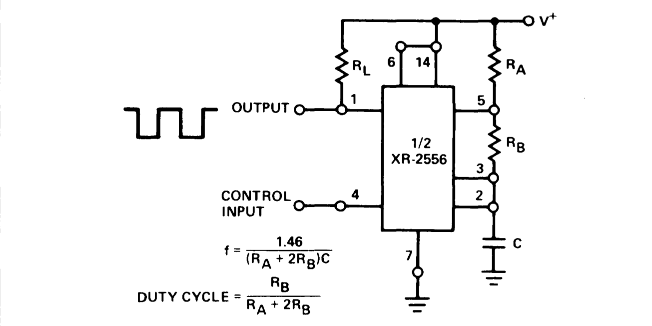


Figure 15. Astable (Free-Running) Circuit

The charge time (output high) is given by:

$$t_1 = 0.695\,(R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 = 0.695\,(R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\,(R_A + 2R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad \text{and}$$

may be easily found as shown in Figure 17.

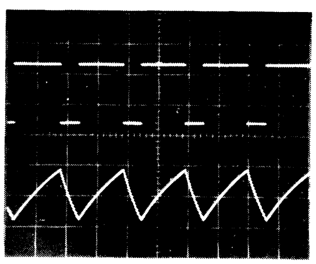


Figure 16. Astable Waveforms
Top: Output Waveform
Bottom: Waveform Across Timing Capacitor

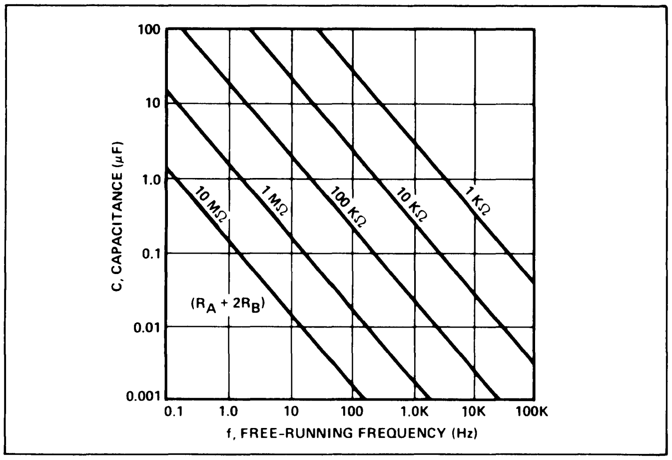


Figure 17. Free Running Frequency as a Function of External Timing Components

The duty cycle, D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

To obtain the maximum duty cycle, R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 5 current) within the maximum rating of the discharge transistor (200 mA).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT (PINS 1 OR 13)

The output logic level is normally in a "low" state, and goes "high" during the timing cycle. Each output of the XR-2556 is a "totem pole" type capable of sinking or sourcing 200 mA of load current (see Figure 18).

TRIGGER (PINS 2 OR 12)

The timing cycle is initiated by lowering the dc level at the trigger terminal below 1/3 V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is completed.

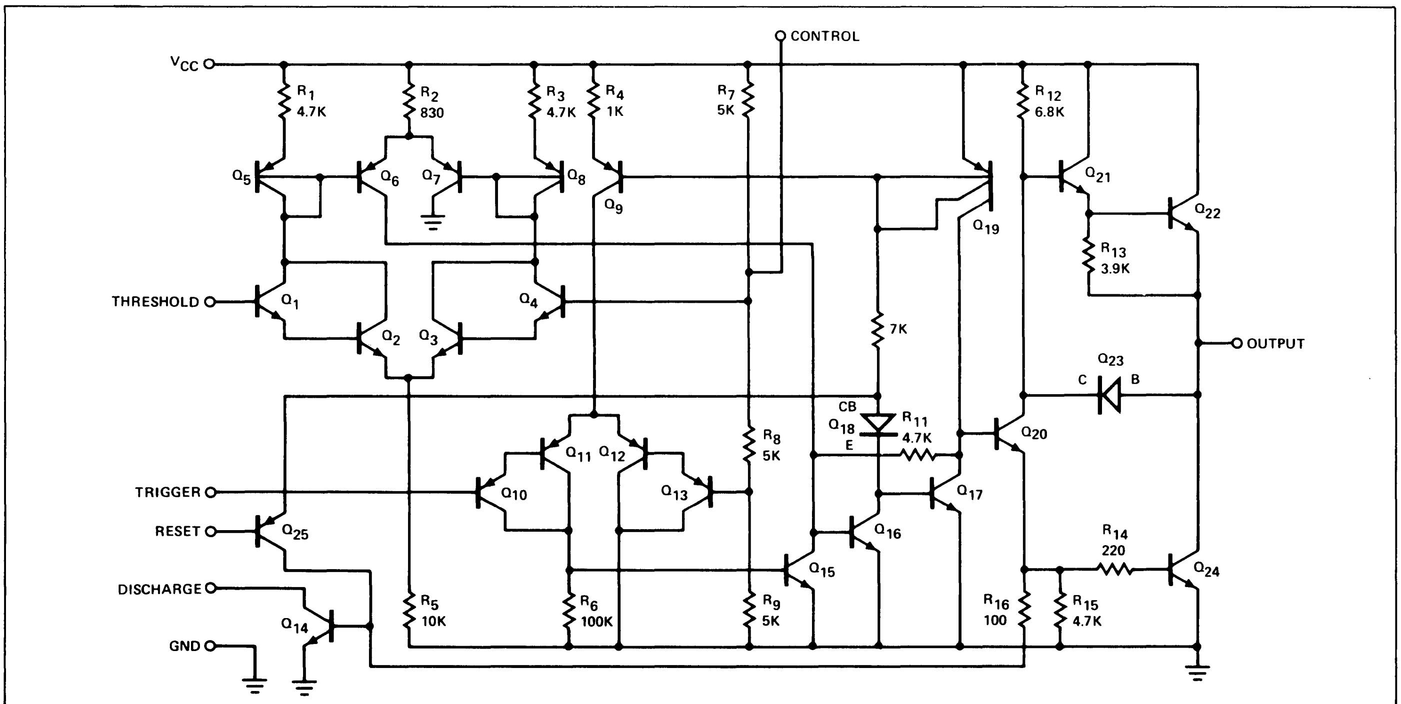


Figure 18. Circuit Schematic – 1/2 of XR-2256

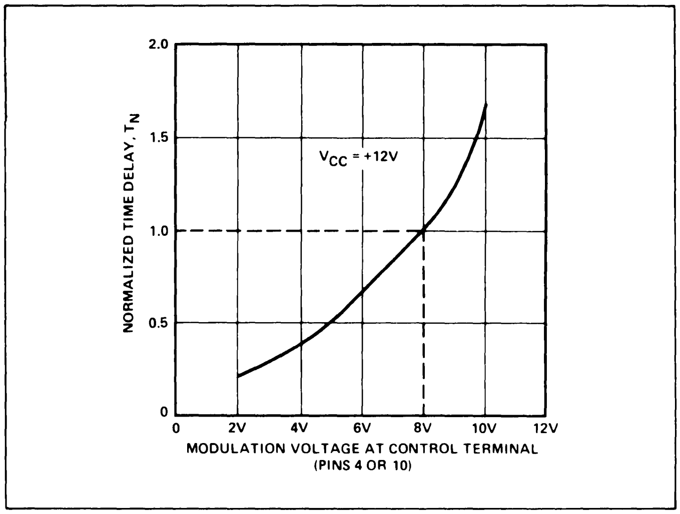


Figure 19. Normalized Time Delay vs. Modulation Voltage

THRESHOLD (PINS 3 OR 11)

The timing cycle is completed when the voltage level at the trigger terminal reaches 2/3 V_{CC}. At this point, Comparator #2 of Figure 2 changes state, resets the internal flip-flop, and initiates the discharge cycle.

CONTROL OR FM (PINS 4 OR 10)

The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 4 or 10. This terminal is internally biased at 2/3 V_{CC}. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. Figure 19 shows the variation of the timing period, T, as a function of dc voltage at the control terminal. When not in use, the control terminals should be ac grounded through 0.01 μF decoupling capacitors.

DISCHARGE (PINS 5 OR 9)

This terminal corresponds to the collector of the discharge transistor, T_O, of Figure 2. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

RESET (PINS 6 OR 8)

The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the reset voltage is applied. When the reset signal is removed, the output remains "low" until re-triggered. When not used, the reset terminals should be connected to V_{CC} in order to avoid any possibility of false triggering. When the timing circuits are operated in the astable mode, the reset terminals can be used for "on" and "off" keying of the oscillations. (See Figure 22).

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-2556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 20 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\ R_1C_1 \text{ and } T_2 = 1.1\ R_2C_2$$

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 21. When Timer 1 is triggered at pin 2, its

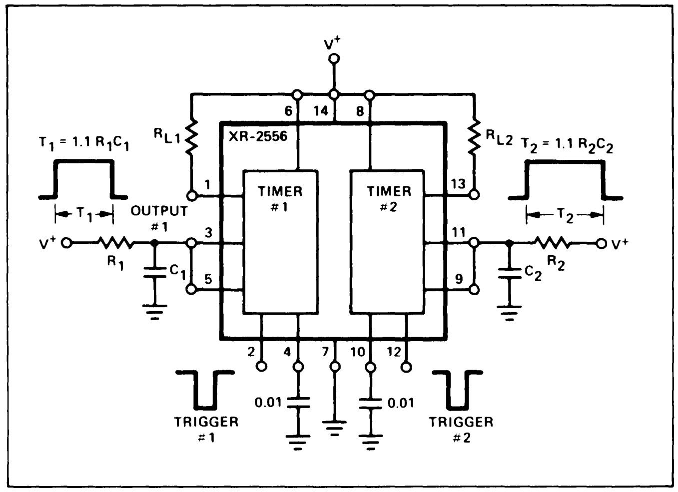


Figure 20. Generation of Two Independent Time Delays

output at pin 1 goes "high" for a time duration $T_1 = 1.1\ R_1C_1$. At the end of this timing cycle, pin 1 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 1 and 12. Then, the output at pin 13 goes "high" for a time duration $T_2 = 1.1\ R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 2 by a time delay of T_1.

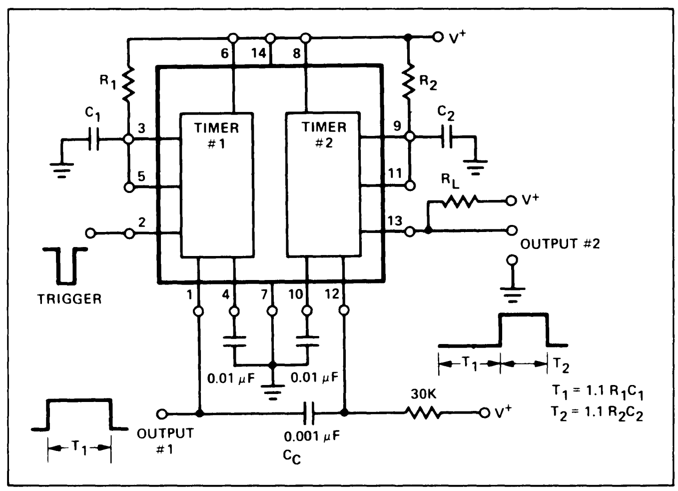


Figure 21. Sequential Timing

KEYED OSCILLATOR

One of the timer sections of the XR-2556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 22. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 8) of Timer 2.

When the circuit is at rest, the logic level at the output of Timer 1 is "low"; and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 22.

FREQUENCY DIVIDER

If the frequency of the input is known, each timer section of the XR-2556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= $1.1\ R_1C_1$) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than $1.1\ R_1C_1$ will actually trigger the circuit.

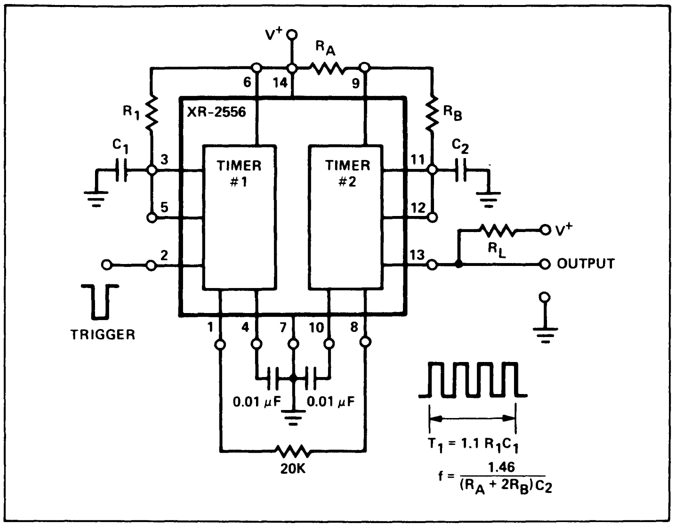


Figure 22. Keyed Oscillator

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\left(\frac{T}{T_P} - 1\right) < N < \frac{T}{T_P}$$

where Tp is the period of the input pulse signal.

Figure 23 shows the circuit waveforms for divide-by-five operation for one of the timer sections of the XR-2556. In this case, the timing period of the circuit is set to be approximately 4.5 times the period of the input pulse.

Since the two timer sections of the XR-2556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-2556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_s/N_1 \text{ and } f_2 = f_s/N_2$$

where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (3, 5) and (9, 11).

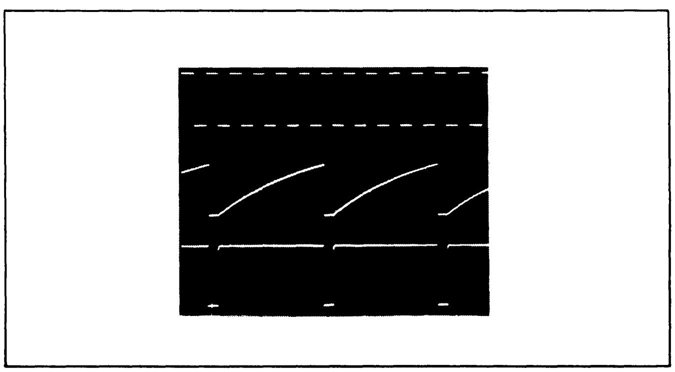


Figure 23. Frequency Divider Waveforms
Top: Input Pulse Train (f = 5 kHz)
Middle: Waveforms Across Timing Capacitor
Bottom: Output Waveform (f = 1 kHz)

FREQUENCY DIVIDER AND PULSE SHAPER

Frequency division can be performed by 1/2 of the XR-2556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 24, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse-shaper.

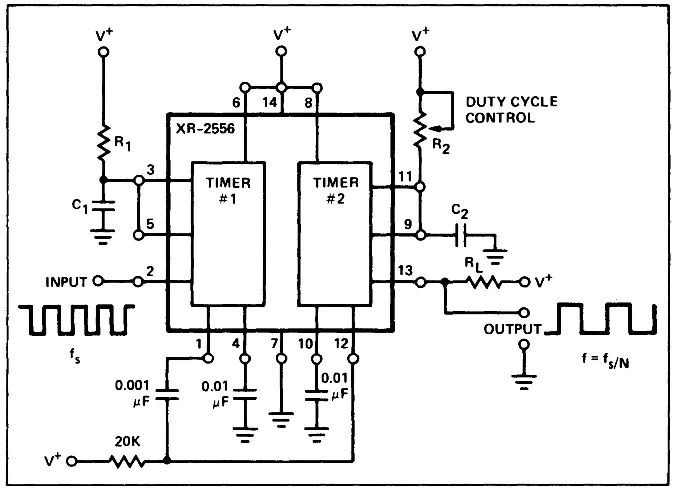


Figure 24. Frequency Divider and Pulse-Shaper

The output of Timer 1 (pin 1) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 13) can be adjusted from 1% to 99% by varying the value of R_2.

Figure 25 shows the circuit waveforms in this application. The top waveform is the input signal of frequency f_s applied to the trigger input (pin 2) of Timer 1. The middle waveform is the output of Timer 1 for divide-by-three operation; and the bottom waveform is the pulse-shaped output obtained from Timer 2 (pin 13).

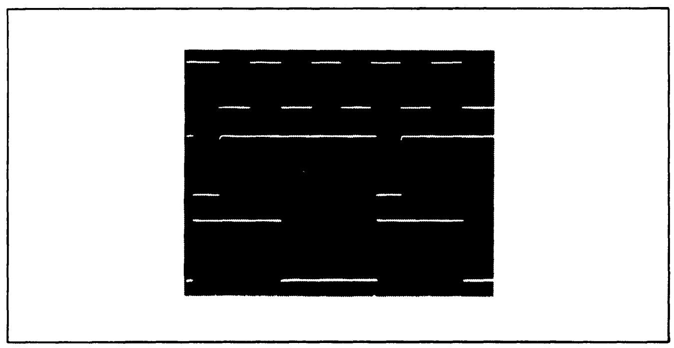


Figure 25. Frequency Divider and Pulse-Shaper Waveforms
Top: Input Signal (f_s = 9 kHz)
Middle: Output at Pin 1 for Divide-by-3
Bottom: Variable Duty Cycle Output at Pin 13

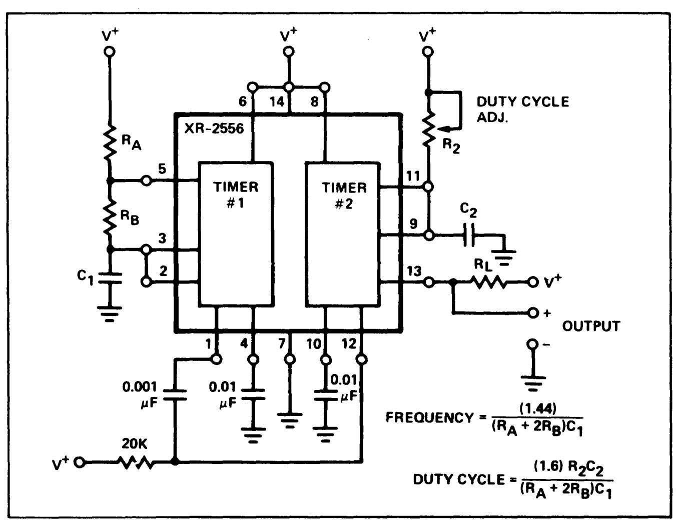


Figure 26. Fixed Frequency Oscillator With Variable Duty Cycle

FIXED-FREQUENCY, VARIABLE DUTY CYCLE OSCILLATOR

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 26, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 13 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

The frequency and the duty cycle of the output waveform are given as:

$$\text{Frequency} = \frac{1.44}{(R_A + 2R_B)C_1}$$

$$\text{Duty Cycle} = \frac{(1.6)\,R_2C_2}{(R_A + 2R_BC_1)}$$

OSCILLATOR WITH SYNCHRONIZED OUTPUTS

The circuit of Figure 26 can also be used as an oscillator with synchronized multiple frequency outputs. Timer 1 generates an output at frequency f_1 at pin 1, as set by resistors R_A, R_B, and C_1. Timer 2 is used as a frequency divider by setting its timing cycle, T_2, to be larger than the period of Timer 1 (see section on frequency division). The resulting output of Timer 2 (pin 13) is at frequency f_2 given as:

$$f_2 = f_1/N$$

where N is the divider ratio set by the external R-C networks as described by Figures 23 and 24.

PULSE-WIDTH MODULATION

For pulse-width modulation, one-half of the XR-2556 is connected as shown in Figure 27. The circuit operates in its monostable mode and is triggered with a continuous pulse train. Output pulses are generated at the same rate as the input pulse train, except the output pulse-width is determined by the timing components R_1 and C_1.

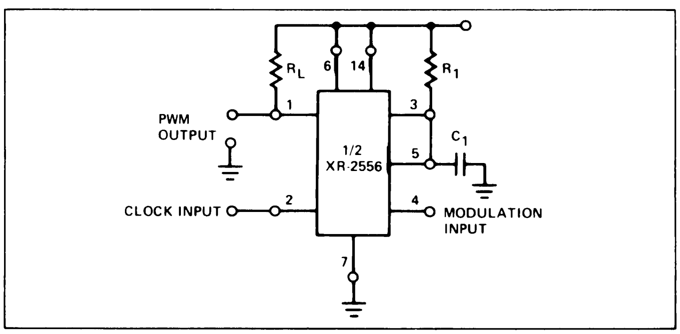


Figure 27. Pulse-Width Modulation

In this mode of operation, the duration of the timing cycle (i.e., the output pulse-width) can be modulated by applying a modulation input to the control voltage terminals (pins 4 or 10). The control characteristics associated with the modulation terminals are depicted in Figure 19. Figure 28 shows the actual circuit waveforms generated in this manner.

When using the XR-2556 for pulse-width modulation, an external clock signal is not necessary, since one section can be operated in its astable mode (see Figure 15) and serve as the clock generator. Figure 29 is the recommended connection for such an application. In this case, Timer 2 is used as the clock generator, and Timer 1 is used as the pulse-width modulator section.

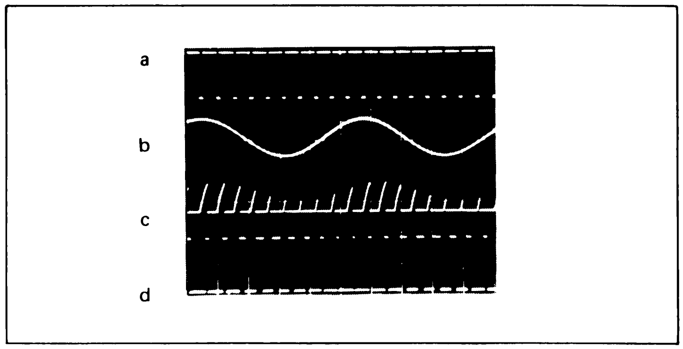


Figure 28. Pulse-Width Modulation Waveforms
a) Clock Input at Pin 2
b) Modulation Input at Pin 4
c) Capacitor Voltage at Pin 3
d) Pulse-Width Modulated Output at Pin 1

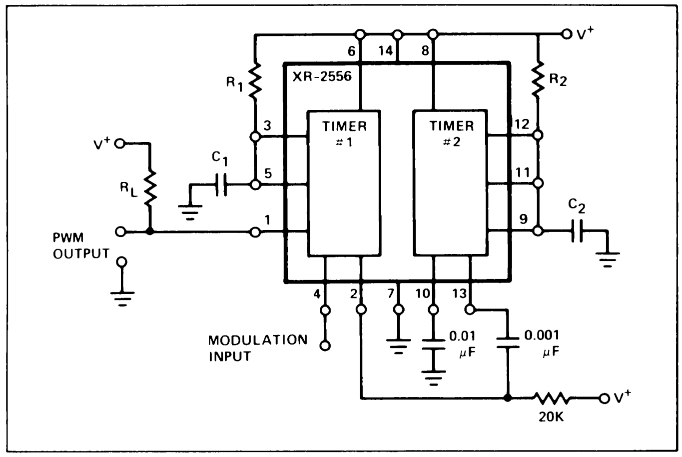


Figure 29. Pulse-Width Modulation With Internal Clock

PULSE-POSITION MODULATION

When a timer section of the XR-2556 is operated in its astable mode (see Figure 15), the period of the output pulse train can be varied by applying a modulation voltage to the corresponding modulation control terminal. In this manner, the repetition rate of the output pulse train can be varied, resulting in a pulse-position modulated output. Typical transfer characteristics between the timing cycle and the modulation voltage are given in Figure 19.

LOGIC "AND" AND "OR" CONNECTION OF OUTPUTS

The individual outputs (pins 1 and 13) of the XR-2556 can be interconnected as shown in Figure 30 to perform logic "or" and "and" functions. Since the output of each timer section is a high-current "totem-pole" type, external diodes are needed to avoid current flow from one output into the other.

Referring to Figure 30(a), the output logic level "P" would read "high" when either one of the outputs at pins 1 or 13 is "high." For Figure 30(b), the output will read "high" only when both outputs at pins 1 and 13 are "high".

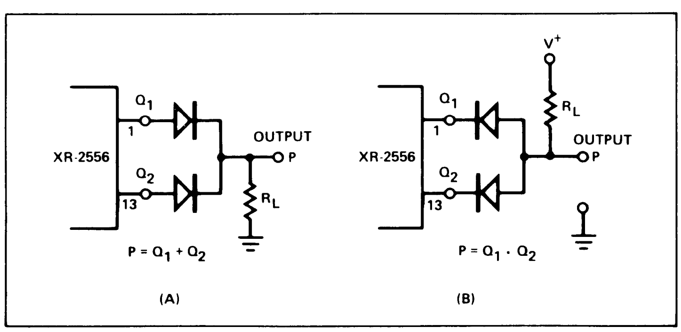


Figure 30. Logic "OR" and "AND"

XR-2240

Programmable Timer/Counter

GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be synchronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and DTL logic levels.

FEATURES

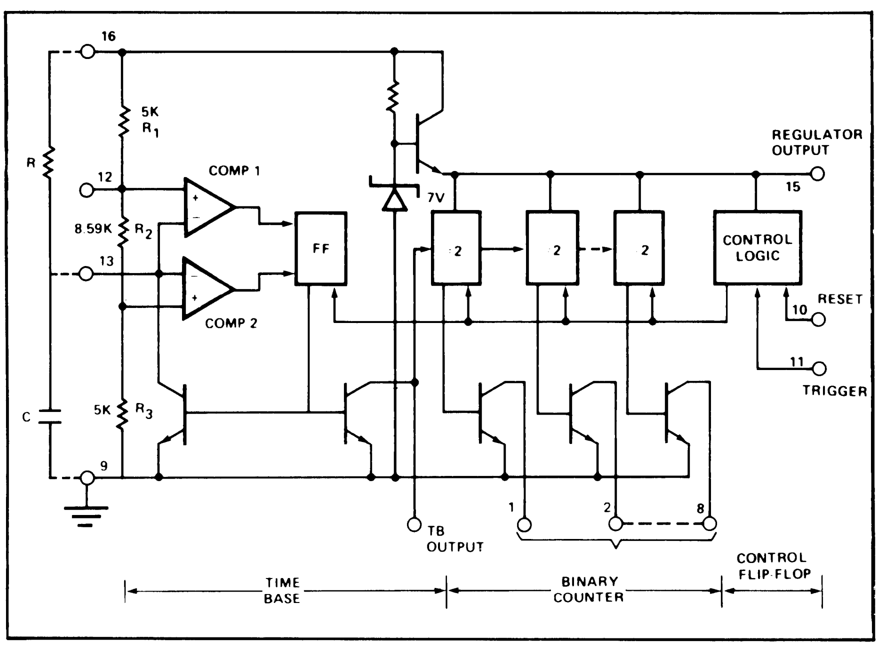
Timing from micro-seconds to days
Programmable delays: 1 RC to 255 RC
Wide supply range: 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2%/V

APPLICATIONS

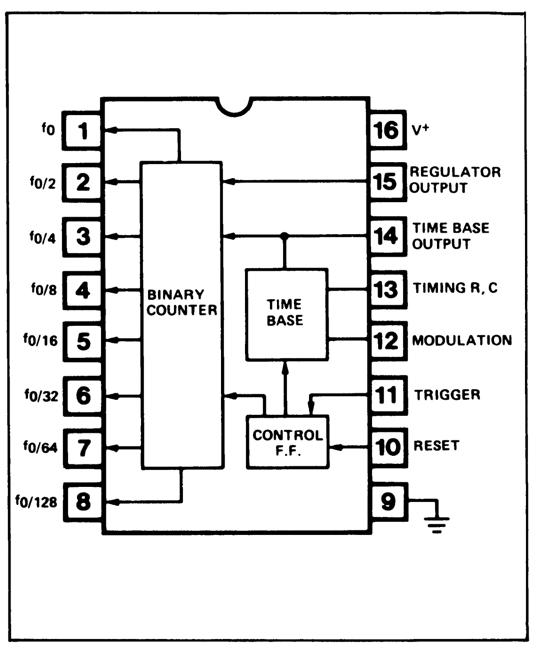
Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5.0 mW/°C
Operating Temperature	
XR-2240M	−55°C to +125°C
XR-2240C	0°C to +75°C
Storage Temperature	−65°C to +150°C



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, R = 10 kΩ, C = 0.1 μF, unless otherwise noted.

PARAMETERS	XR-2240			XR-2240C			UNIT	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Counter Only		1			1.5		mA	See Figure 3
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy *		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \leq T \leq 75°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	R = 1 kΩ, C = 0.007 μF
Modulation Voltage Level								Measured at Pin 12
	3.00	3.50	4.0	2.80	3.50	4.20	V	$V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measures at Pin 11, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time **		1			1		μsec.	
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time **		0.8			0.8		μsec.	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Measured at Pin 14
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

*Timing error solely introduced by XR-2240, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at pin 1.

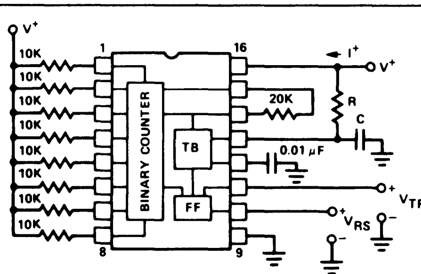


Figure 2. Generalized Test Circuit

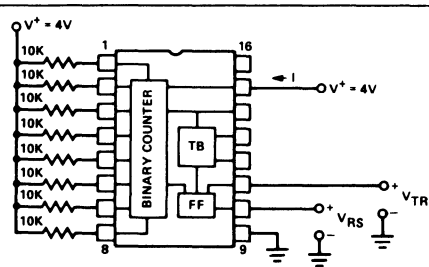


Figure 3. Test Circuit for Low-Power Operation (Time-Base Powered Down)

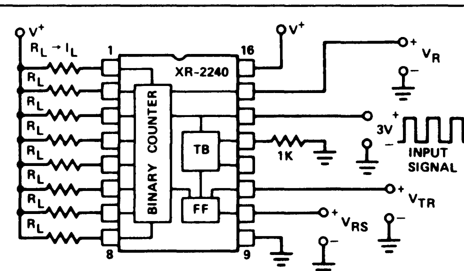


Figure 4. Test Circuit for Counter Section

PRINCIPLE OF OPERATION

The timing cycle for the XR-2240 is initiated by applying a positive-going trigger pulse to pin 11. The trigger input actuates the time-base oscillator, enables the counter section, and sets all the counter outputs to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 10.

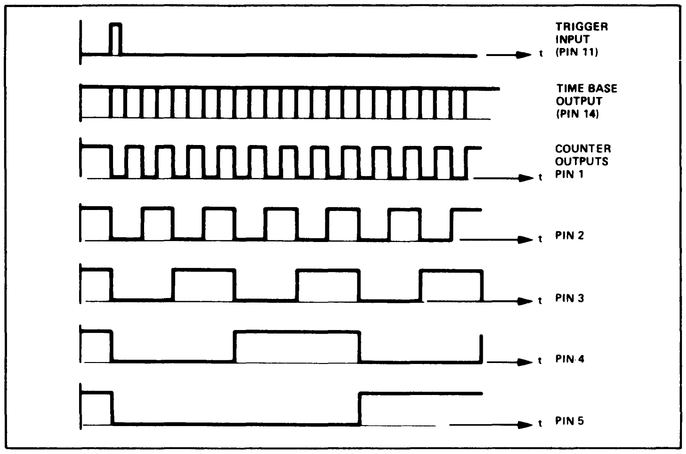


Figure 5. Timing Diagram of Output Waveforms

Figure 5 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is at reset state, both the time-base and the counter sections are disabled and all the counter outputs are at "high" state.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 6, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

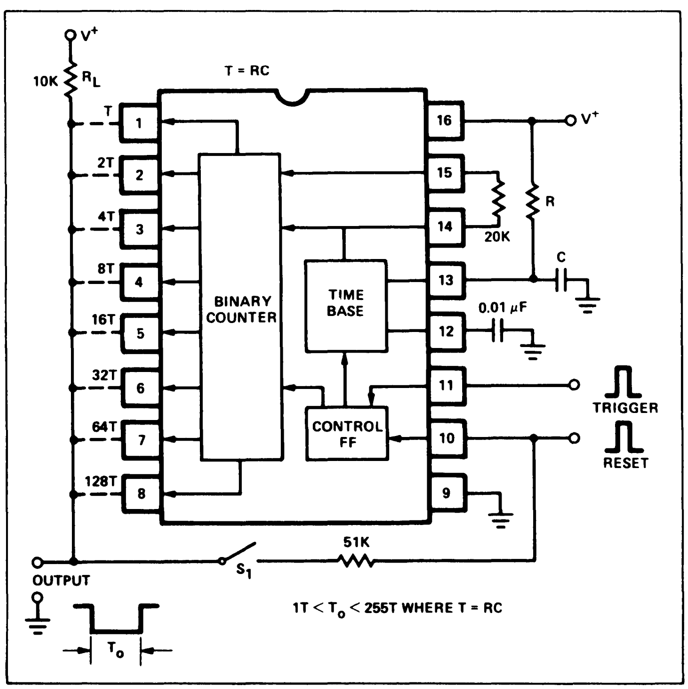


Figure 6. Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

PROGRAMMING CAPABILITY

The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 6. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$, where T = RC.

TRIGGER AND RESET CONDITIONS

When power is applied to the XR-2240 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 5.

The counter outputs can be used individually, or can be connected together in a "wired-or" configuration, as described in the Programming section.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground.

Minimum pulse widths for reset and trigger inputs are shown in Figure 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 13). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 16. Recommended sync pulse widths and amplitudes are also given in the figure.

HARMONIC SYNCHRONIZATION

Time-base can be synchronized with *integer multiples or harmonics* of input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$

$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 17 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

TYPICAL CHARACTERISTICS

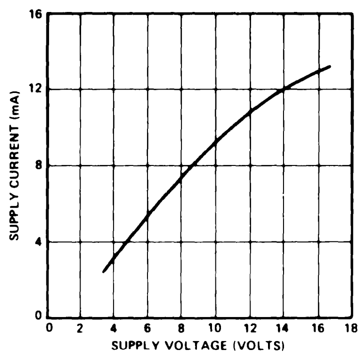


Figure 7. Supply Current vs. Supply Voltage in Reset Condition (Supply Current Under Trigger Condition is ≈0.7 mA less)

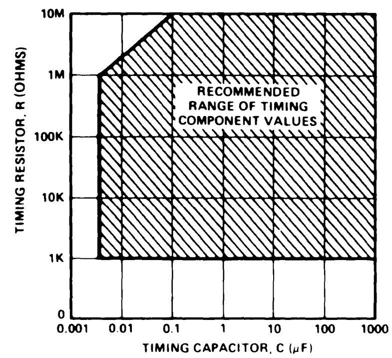


Figure 8. Recommended Range of Timing Component Values

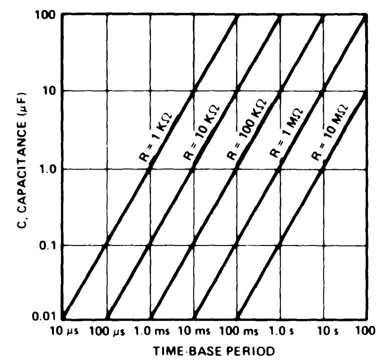


Figure 9. Time-Base Period, T, as a Function of External RC

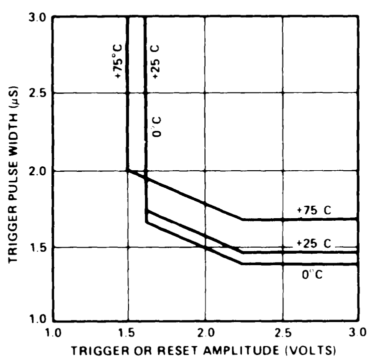


Figure 10. Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

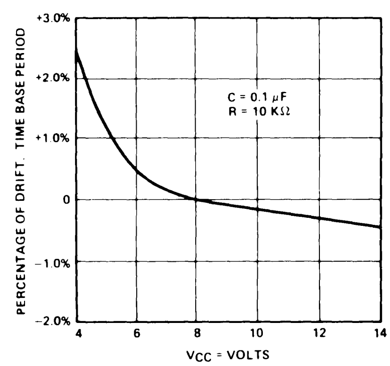


Figure 11. Power Supply Drift

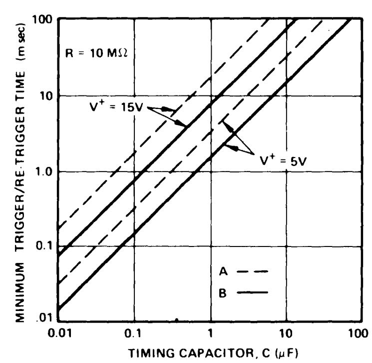


Figure 12.
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

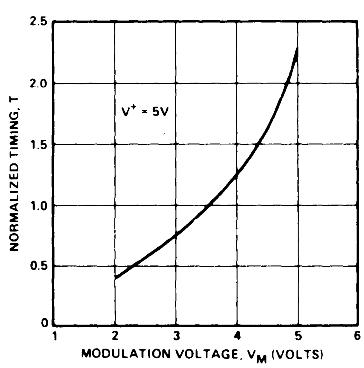


Figure 13. Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12

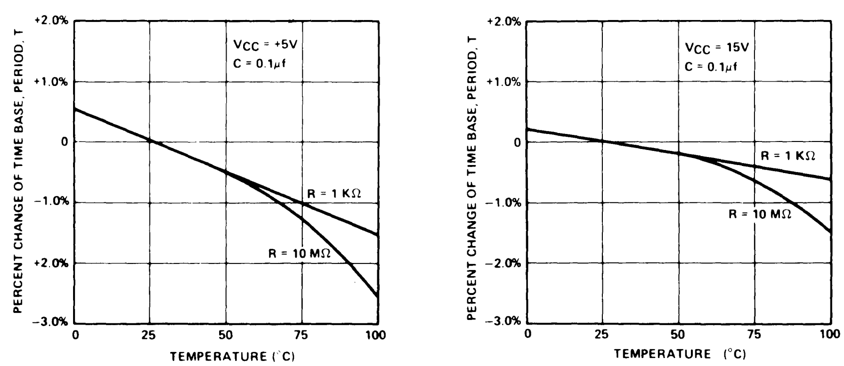


Figure 14. Temperature Drift of Time-Base Period, T

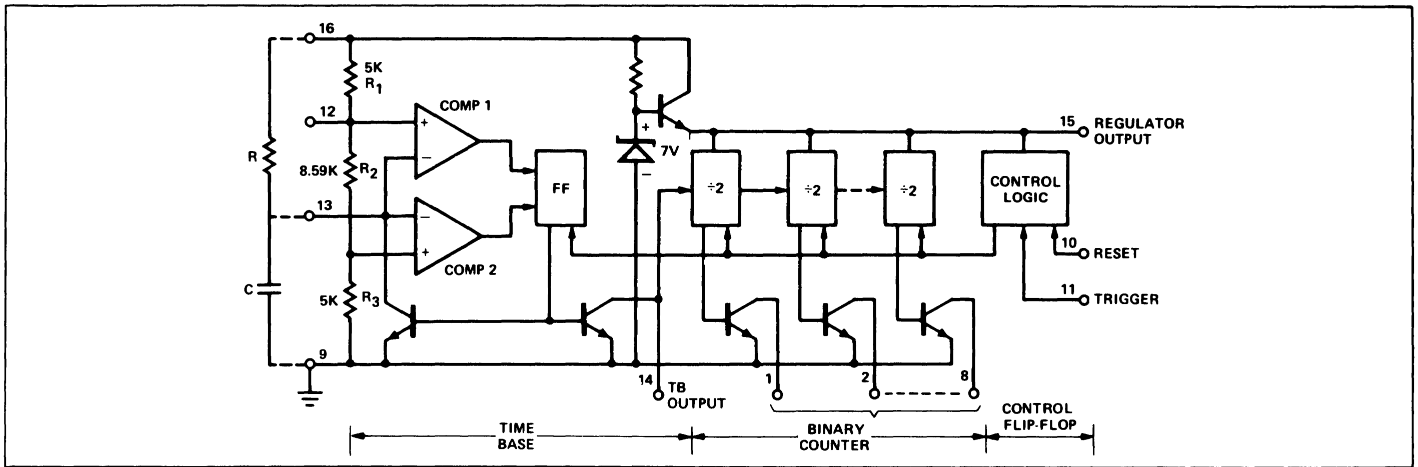


Figure 15. Simplified Circuit Diagram of XR-2240

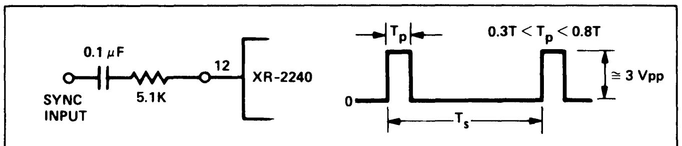


Figure 16. Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

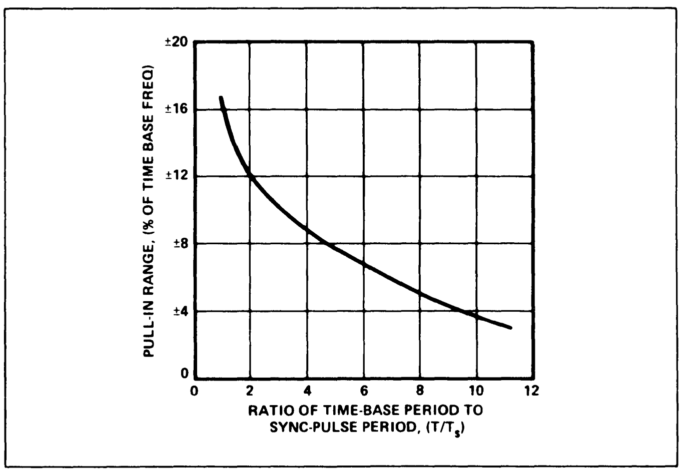


Figure 17. Typical Pull-In Range for Harmonic Synchronization

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage, as shown in Figure 15 and requires a 20 KΩ pull-up resistor to Pin 15 for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 5.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.5 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

Note:
Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

REGULATOR OUTPUT (PIN 15)

This terminal can serve as a V^+ supply to additional XR-2240 circuits when several timer circuits are cascaded (See Figure 20), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V^+ terminal to power-down the internal time-base and reduce power dissipation. The output current shall not exceed 10 mA.

When the internal time-base is used with $V^+ \leq 4.5V$, pin 15 should be shorted to pin 16.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2240 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 18.

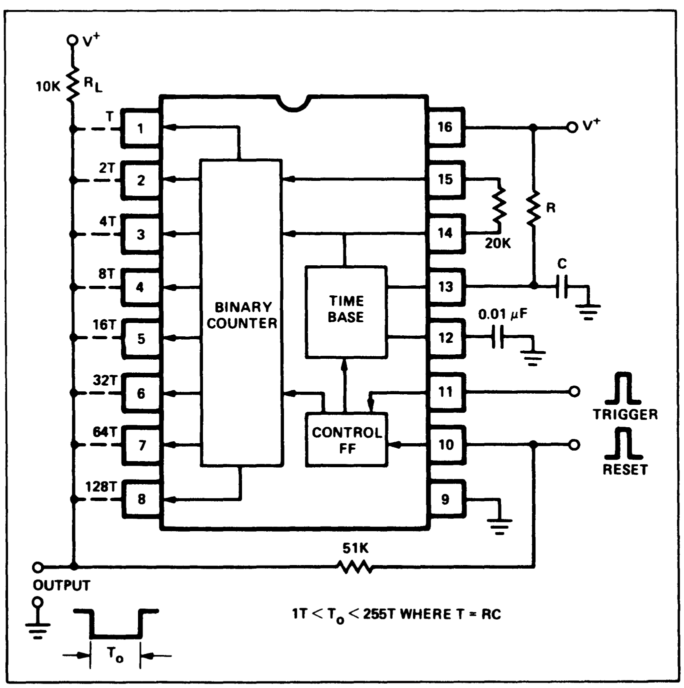


Figure 18. Circuit for Monostable Operation
(T_o = NRC where $1 \leq N \leq 255$)

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_O and then returns to the high state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (See Figure 9). N is an integer in the range of:

$$1 \leq N \leq 255$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described below.

PROGRAMMING OF COUNTER OUTPUTS: The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection where the combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output bus as shown in Figure 18. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$.

ULTRA-LONG DELAY GENERATION

Two XR-2240 units can be cascaded as shown in Figure 19 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output would go to a low state and stay that way for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

PROGRAMMING: Total timing cycle of two cascaded units can be programmed from $T_O = 256RC$ to $T_O = 65{,}536RC$ in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus.

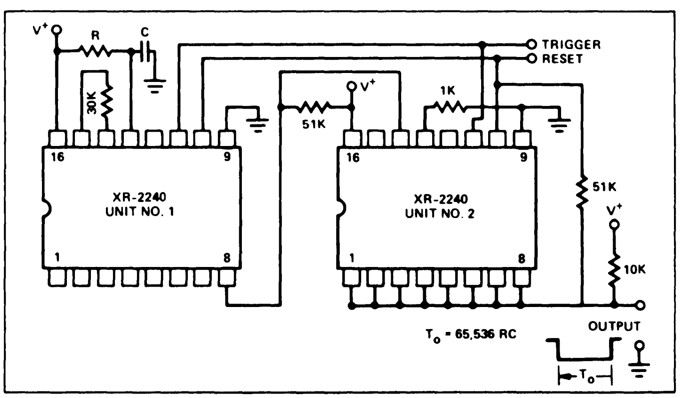


Figure 19. Cascaded Operation for Long Delay Generation

LOW-POWER OPERATION

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 20. In this case, the V^+ terminal (pin 16) of Unit 2 is left open-circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units.

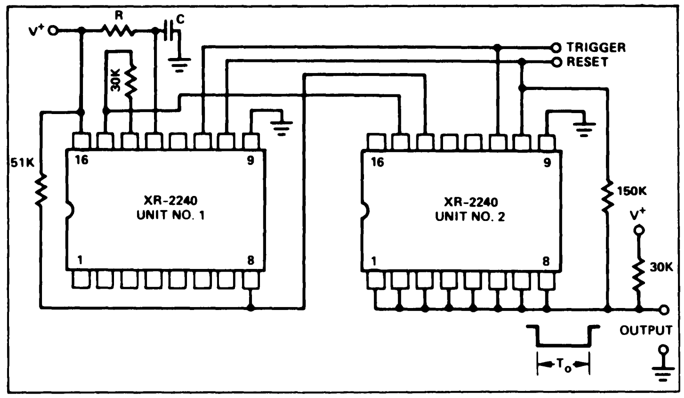


Figure 20. Low-Power Operation of Cascaded Timers

ASTABLE OPERATION

The XR-2240 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 6, with the feedback switch S_1 open.

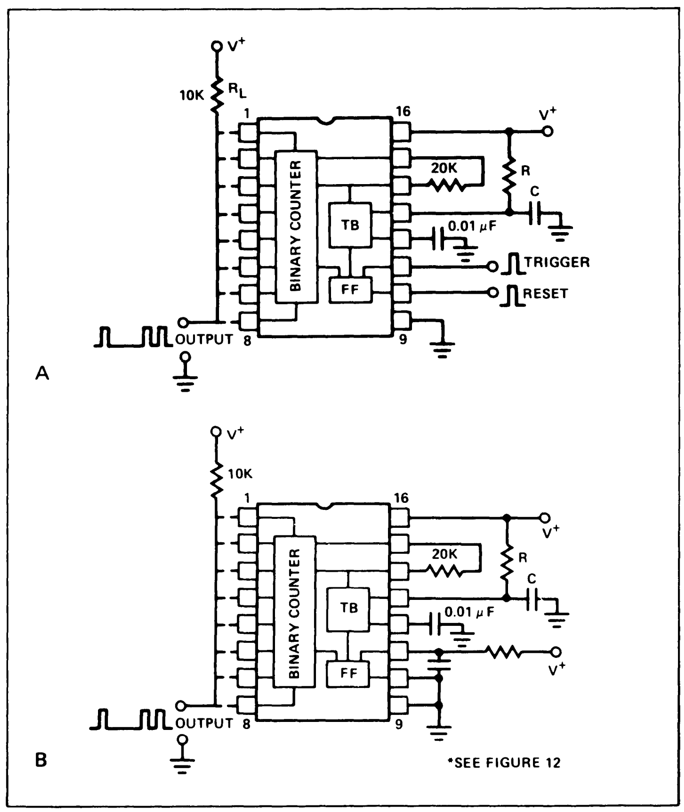


Figure 21. Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

BINARY PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the XR-2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 5 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

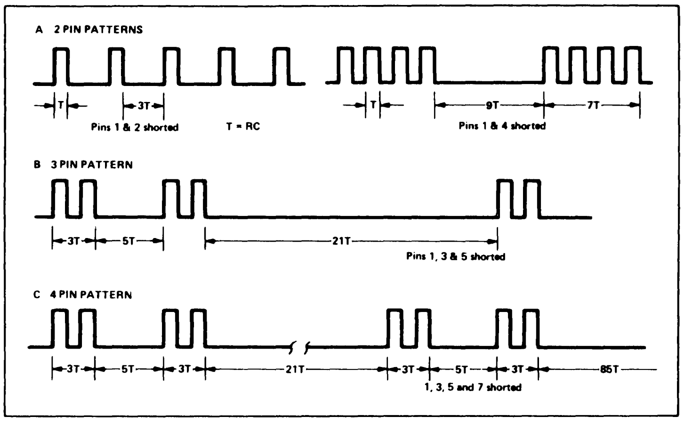


Figure 22. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

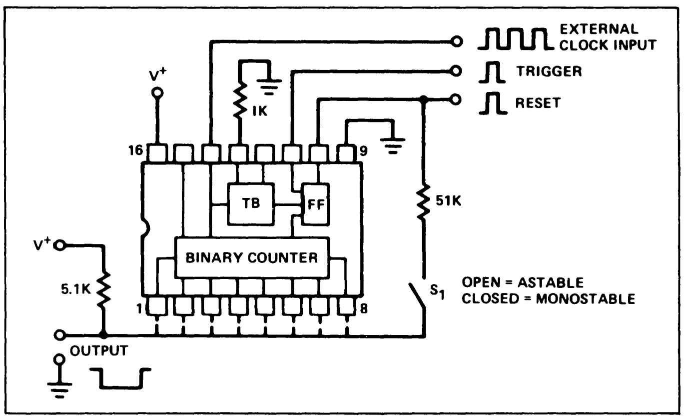


Figure 23. Operation with External Clock

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be $\geq 1\ \mu S$.

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V^+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of XR-2240 can be used to generate 255 discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N+1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 4 are connected together to the output bus, the total count is: N=1+4+8=13; and the period of the output waveform is equal to (N+1) T or 14T. In this manner, 256 different frequencies can be synthesized from a given time-base setting.

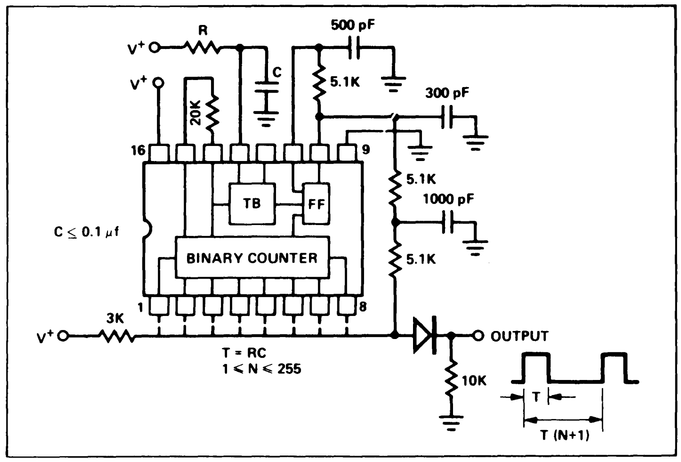


Figure 24. Frequency Synthesis from Internal Time-Base

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 16 and 17 for external sync waveform and harmonic capture range.) If the the time base is synchronized to (m)th harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 25 can produce 1500 separate frequencies from a single fixed reference.

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

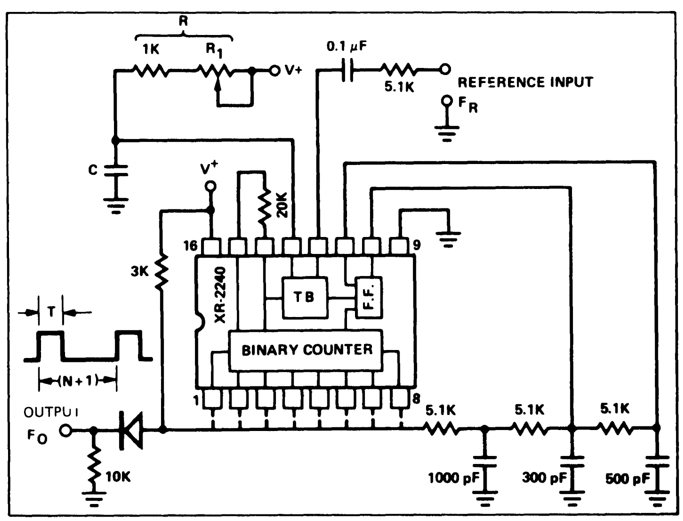


Figure 25. Frequency Synthesis by Harmonic Locking to an External Reference

STAIRCASE GENERATOR

The XR-2240 Timer/Counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator, as shown in Figure 26. Under reset condition, the output is low. When a trigger is applied, the op. amp. output goes to a high state and generates a negative going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14, through a steering diode, as shown in Figure 26. The count is stopped when pin 14 is clamped at a voltage level less than 1.4V.

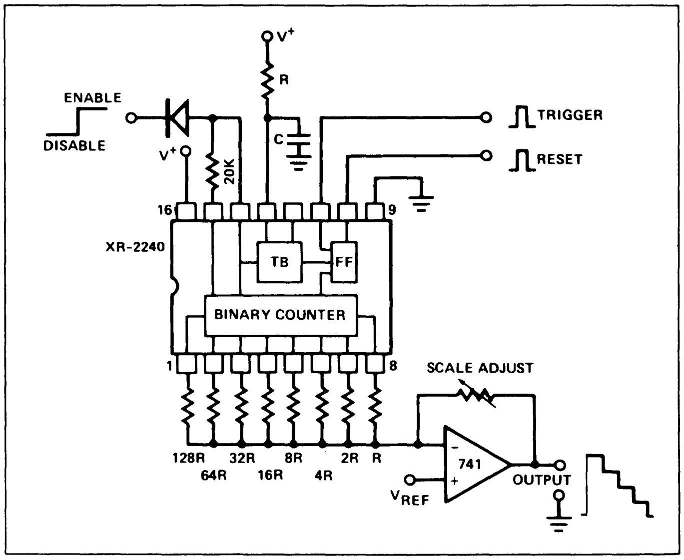


Figure 26. Staircase Generator

DIGITAL SAMPLE/HOLD

Figure 27 shows a digital sample and hold circuit using the XR-2240. The principle of operation of the circuit is similar to the staircase generator described in the previous section. When a "strobe" input is applied, the RC low-pass network between the reset and the trigger inputs of XR-2240 causes the timer to be first reset and then triggered by the same strobe input. This strobe input also sets the output of the bistable latch to a high state and activates the counter.

The circuit generates a staircase voltage at the output of the op. amp. When the level of the staircase reaches that of the analog input to be sampled, comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op. amp. output corresponds to the sampled analog input. Once the input is sampled, it will be held until the next strobe signal. Minimum re-cycle time of the system is ≈ 6 msec.

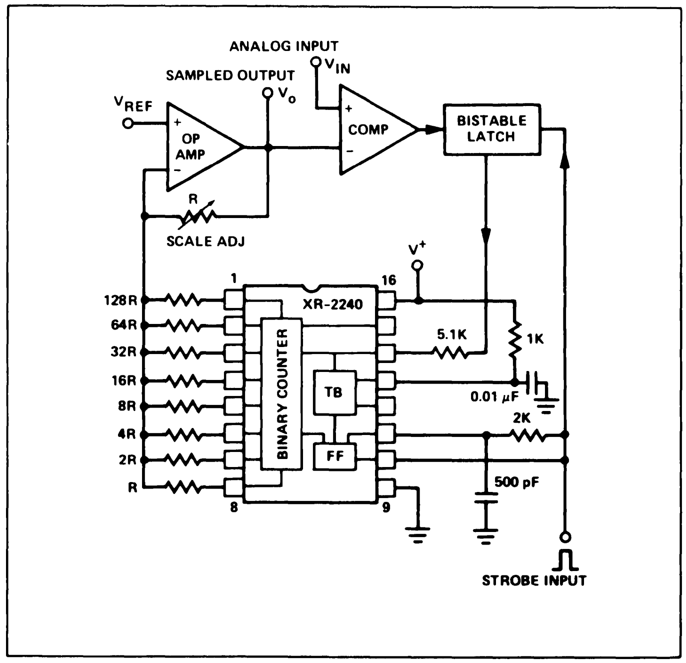


Figure 27. **Digital Sample and Hold Circuit**

ANALOG-TO-DIGITAL CONVERTER

Figure 28 shows a simple 8-bit A/D converter system using the XR-2240. The operation of the circuit is very similar to that described in connection with the digital sample/hold system of Figure 15. In the case of A/D conversion, the digital output is obtained in parallel format from the binary counter outputs, with the output at pin 8 corresponding to the most significant bit (MSB). The re-cycle time of the A/D converter is ≈ 6 msec.

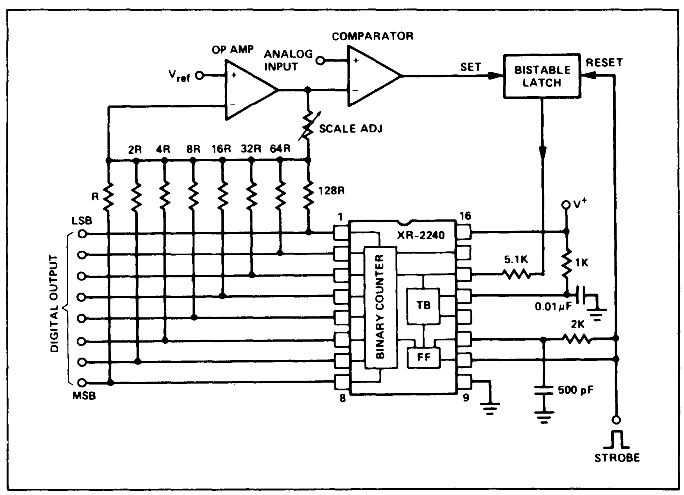


Figure 28. Analog-To-Digital Converter

XR-2242

Long-Range Timer

GENERAL DESCRIPTION

The XR-2242 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 8-bit binary counter and a control flip-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

The timing cycle for the XR-2242 is initiated by applying a positive-going trigger pulse to pin 6. The trigger input actuates the time-base oscillator, enables the counter section, and sets the output to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 5.

In monostable timer applications, the output terminal (pin 3) is connected back to the reset terminal. In this manner, after 128 clock pulses are applied to the circuit, this output goes to "high" state and resets the circuit thus completing the timing cycle. Thus, subsequent to triggering, the output at pin 3 will produce a total timing pulse of 128 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at pin 2 produces a square-wave output with the period of 2 RC.

If the output at pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

FEATURES

Timing from micro-seconds to days
Wide supply range: 4.5V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator

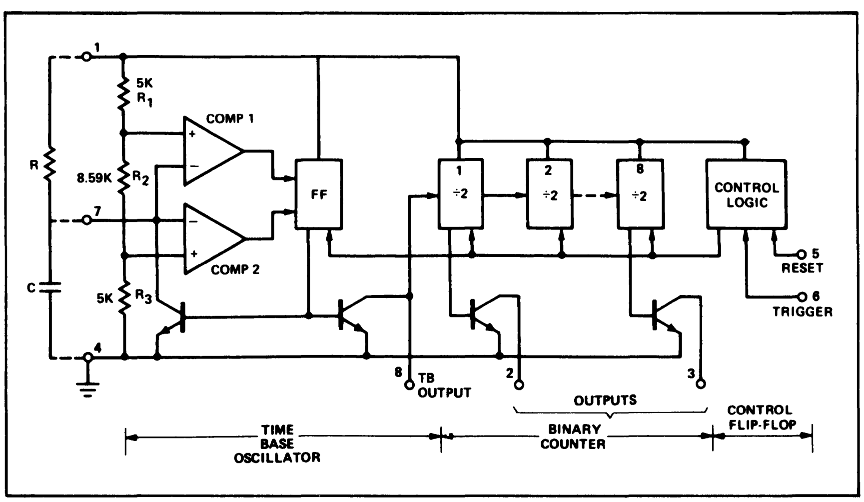
ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2242M	−55°C to +125°C
XR-2242C	0°C to +75°C
Storage	−65°C to +150°C

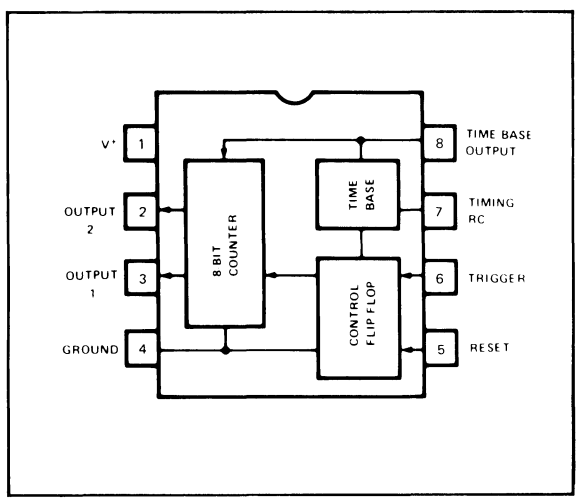
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to + 125°C
XR-2242CN	Ceramic	0°C to +75°C
XR-2242CP	Plastic	0°C to +75°C

SIMPLIFIED SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25^\circ C$, R = 10 kΩ, C = 0.1 μF, unless otherwise noted.

PARAMETERS	XR-2242M			XR-2242C			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
TIME BASE SECTION								See Figure 3
Timing Accuracy *		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0^\circ C \leq T \leq 75^\circ C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts
Max Frequency	100	130			130		kHz	R = 1 kΩ, C = 0.007 μF
Recommended Range of Timing Components								See Figure 5
Timing Resistor, R	0.001		10	0.001		5	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	Low-Leakage Capacitor Required.
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time **		1			1		μsec	
Reset								Measured at Pin 5, $V_{TR} = 0$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time **		0.8			0.8		μsec	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.5	1.0			1.0		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 2 and 3
Rise Time		180			180		nsec.	$R_L = 3K\Omega$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} \leq 15V$

*Timing error solely introduced by XR-2242, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in first stage counter output at pin 2.

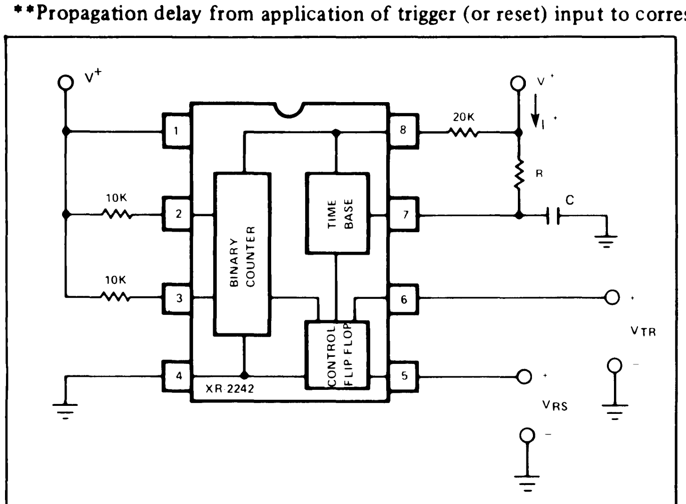


Figure 3. Generalized Test Circuit

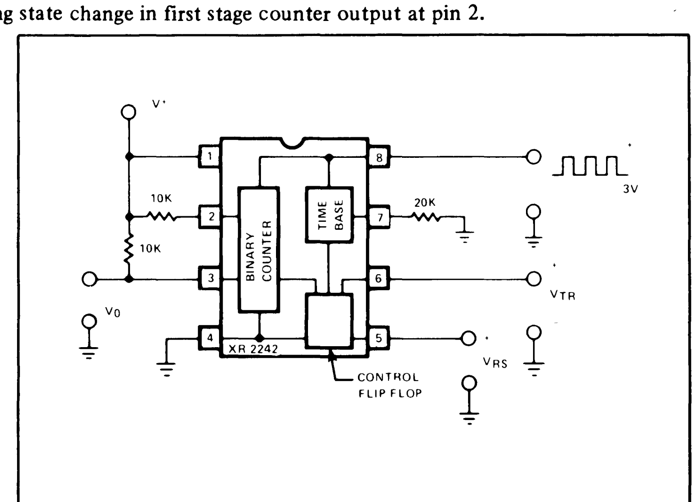
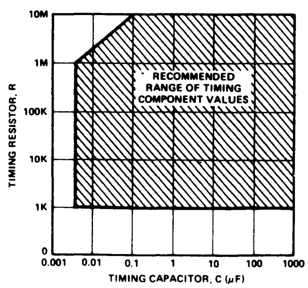


Figure 4. Test for Counter Section



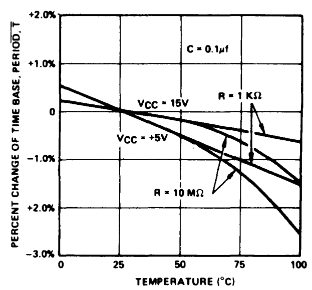


Figure 5. Recommended Range of Timing Component Values

Figure 6. Temperature Drift of Time-Base Period, T

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 2 AND 3)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 1. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 7.

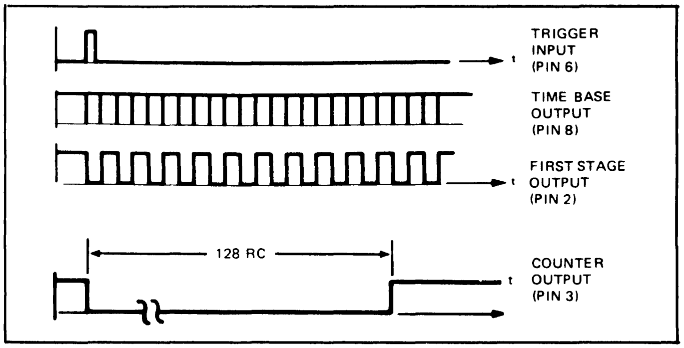


Figure 7. Timing Diagram of Output Waveforms

Basic circuit connection for timing applications is shown in Figure 8. Subsequent to a positive trigger pulse applied to pin 6, the timing output at pin 3 goes to a "low" state and will stay low for a total time duration T_O = 128 RC, where R and C are the timing components connected to pin 7. If the switch S_1 is *open*, then the output at pin 3 would alternately change state every T_O interval of time, and the circuit would operate in its "astable" mode. If the switch S_1 is *closed*, the circuit will reset itself and complete its timing cycle after a time interval of T_O, when the output at pin 3 goes to a "high" state. This corresponds to the "monostable" mode of operation.

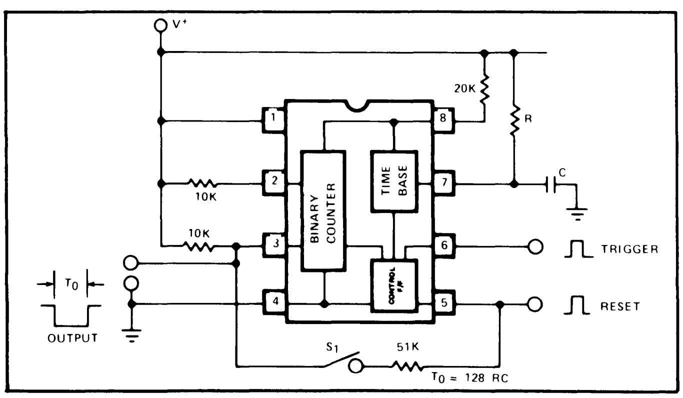


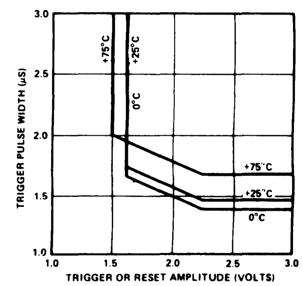
Figure 8. Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

RESET AND TRIGGER INPUTS (PINS 5 AND 6)

The circuit is reset or triggered with positive-going control pulses applied to pins 5 and 6. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs, minimum trigger delay time and minimum re-trigger delay time are shown in Figures 9 and 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Note: In noisy operating environment, 0.01 µF capacitors to ground are recommended from reset and trigger terminals.



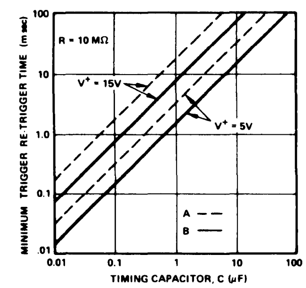


Figure 9. Minimum Trigger and Reset Pulse Widths at Pins 5 and 6

Figure 10. Trigger and Retrigger Delay Time

(A) Minimum Trigger Delay Time Subsequent to Application of Power

(B) Minimum Re-trigger Time, Subsequent to a Reset Input

When power is applied with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

TIMING TERMINAL (PIN 7)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 7 is an exponential ramp with a period T = 1.0 RC.

TIME-BASE OUTPUT (PIN 8)

Time-base output is an open-collector type stage, as shown in Figure 1 and requires a 20 KΩ pull-up resistor to Pin 1 (V^+) for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 7.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses appearing at pin 8. The trigger threshold for the counter section is ≈ +1.5 volts. The counter section can be disabled by clamping the voltage level at pin 8 to ground.

APPLICATIONS INFORMATION

Note: Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 8 may be too narrow to trigger the counter section. This can be corrected by connecting a 500 pF capacitor from pin 8 to ground.

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2242 is used in its monostable or "self-resetting" mode. The circuit connection for this application is shown in Figure 8, with switch S_1 closed.

ASTABLE OPERATION

The XR-2242 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 5) from the counter output (pin 3). Two typical circuit connections for this mode of operation are shown in Figures 11 and 12. In the circuit connection of Figure 11, the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 5, the circuit reverts back to its rest state. The circuit of Figure 11 is essentially the same as that of Figure 8, with the feedback switch S_1 open.

The circuit of Figure 12 is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

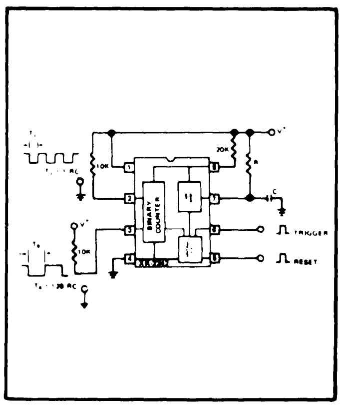


Figure 11. Astable Operation with External Trigger and Reset Controls.

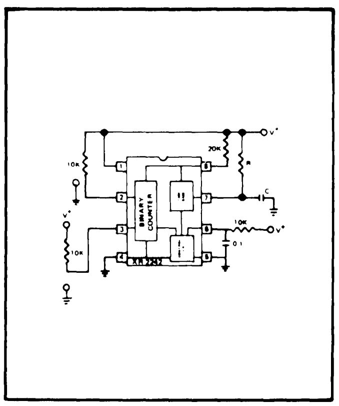


Figure 12. Free-running Operation Self-Triggered When Power Supply is Turned ON.

OPERATION WITH EXTERNAL CLOCK

The XR-2242 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 8. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 7 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be $\geq 1\ \mu S$.

CASCADED OPERATION:

a) Ultra-Long Delay Generation:

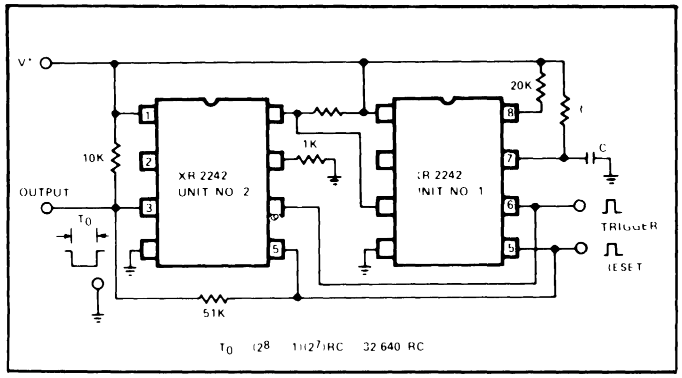


Figure 13. Cascaded Operation of Two XR-2242 Timer Circuits.

Ultra-long time delays, up to one-year duration, can be generated by cascading two XR-2242 timers as shown in Figure 13. In this configuration, the counter section of Unit 2 is cascaded with the counter output of Unit 1, to provide a total count of 32,640 clock cycles before the output (pin 3 of Unit 2) changes state. In the application circuit of Figure 13, the output (pin 3) of Unit 1 is directly connected to the time-base output (pin 8) of Unit 2, through a common pull-up resistor. In this manner, the counter section of Unit 2 is triggered every time the output of Unit 1 makes a *positive-going* transition. The time-base section of Unit 2 is disabled by connecting pin 7 of Unit 2 to ground through a 1 KΩ resistor. The reset and trigger terminals of both units are connected together for common controls.
If an additional XR-2242 were cascaded with Unit 2 of Figure 13, the total available time delay can be extended to (1.065) (10^9) RC. With an external RC = 0.1sec, this would correspond to a time delay of 3.4 years.

b) Sequential Timing:

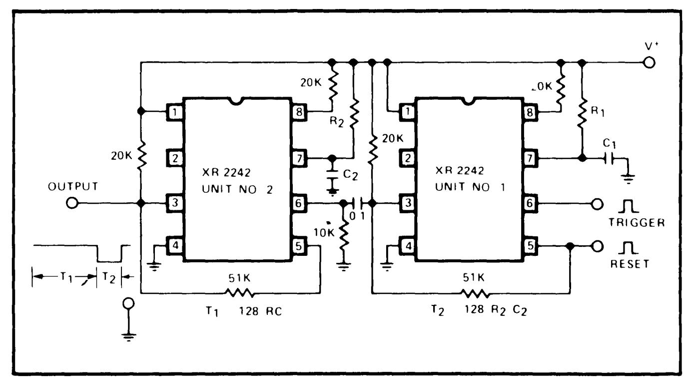


Figure 14. Sequential Timing Using Two XR-2242 Timer Circuits.

Two XR-2242 timers can be cascaded to produce sequential or delayed-timing pulses as shown in Figure 14. In this configuration, the second timer is triggered by the first timer, subsequent to the completion of its timing cycle. Thus, the triggering of Unit 2 is delayed by a time interval, T_1 (= 128 R_1C_1) corresponding to the timing cycle of Unit 1.

The output of Unit 2, which is normally at "high" state will stay high for a duration of T_1 = 128 R_1C_1, subsequent to the application of a trigger pulse; then go to a low state for a duration of T_2 = 128 R_2C_2 corresponding to the timing interval of Unit 2; and finally revert back to its rest state after the comple-of the entire timing sequence.

XR-2243

MICROPOWER LONG-RANGE TIMER

PRINCIPLE OF OPERATION

PRELIMINARY INFORMATION

The XR-2243 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 11-bit binary counter and a control flop-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 1024 RC. If the two circuits are cascaded, a total time delay of $(1024)^2$ or 1,048,576 RC is obtained.

The XR-2243 long range timer was designed for low power operation. Its supply current requires less than 100μA in standby or reset mode. Normal operation requires less than 1mA.

The timing cycle is initiated by applying a positive going pulse to the trigger input, Pin 6. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications, the output terminal (Pin 3) is connected to the reset terminal, Pin 5. In this manner, after 1024 clock pulses are counted, this output goes to "high" state and resets the circuit, thus completing the timing cycle. Therefore, after triggering, the output at Pin 3 will produce a total timing pulse of 1024 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator
Battery Powered Applications

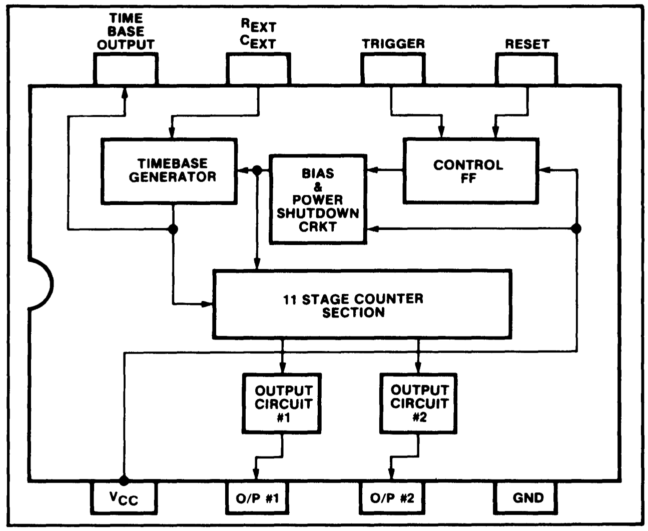


Figure 1: Functional Block Diagram

FEATURES

High Output Current Sink Capability
Timing from Micro-seconds to Days
Wide Supply Range: 2.2V to 15V
TTL and DTL Compatible Outputs
High Accuracy: 0.5%
Excellent Supply Rejection
Monostable and Astable Operation
Mirco Power Consumption–Standby Operation
Low Power Consumption–Normal Operation

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2243CN	Ceramic	0°C to +75°C
XR-2243CP	Plastic	0°C to +75°C

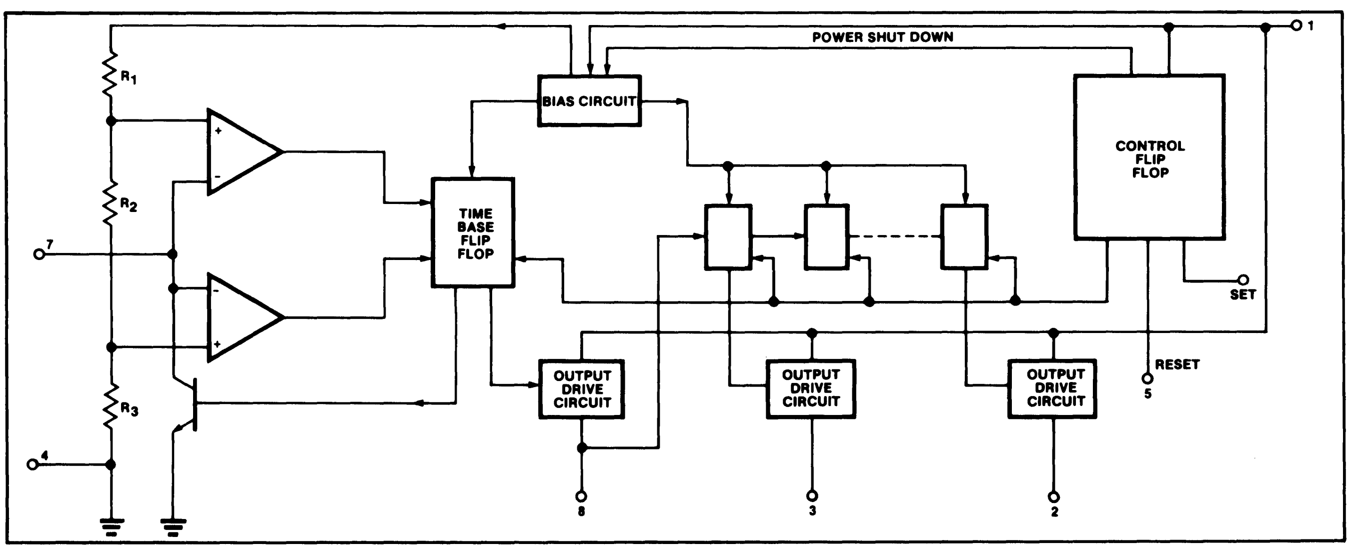


Figure 2: Simplified Circuit Schematic

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, V^+ = 5V, T_A = 25°C, R = 22 kΩ, C = 0.047μf unless otherwise noted.

PARAMETERS	XR-2243C			UNIT	CONDITIONS
	MIN	TYP	MAX		
Supply Voltage	2.7		15	V	
Supply Current					
Standby		45	95	μA	V_{CC} = 2.7V V_{TR} = 0V V_{RS} = 5V
		80	135	μA	V_{CC} = 5V
		250	415	μA	V_{CC} = 15V
Operating		900	1000	μA	V_{CC} = 5V V_{TR} = 5V V_{RS} = 0V
		750	900	μA	V_{CC} = 2.7V
		1250	1500	μA	V_{CC} = 15V
Time Base Section					
Timing Accuracy*		0.5	3	%	V_{CC} = 2.7V V_{TR} = 5V V_{RS} = 0V
Temperature Drift		80	125	ppm/°C	V_{CC} = 5V
		150	225	ppm/°C	V_{CC} = 15V 0°C ≤T_A ≤75°C
		300	650	ppm/°C	V_{CC} = 8V
Supply Drift		0.30	1.0	%/V	
Maximum Frequency	25	35		kHz	
Recommended Range of Timing Components					
Timing Resistor, R	0.005		10	mΩ	
Timing Capacitor, C	0.005		1000	μF	
Trigger/Reset Controls					
Trigger					Measures at Pin 11, V_{RS} = 0
Trigger Threshold		1.4	2.0	V	
Trigger Current		22	30	μA	V_{RS} = 0, V_{TR} = 2V
Impedance		25		kΩ	
Response Time					
Reset					
Reset Threshold		1.4	2.0	V	
Reset Current		22	30	μA	V_{TR} = 0, V_{RS} = 2V
Impedance		25		kΩ	
Response Time					
Counter Section					See Figure 5, V^+ = 5V
Max. Toggle Rate		100	250	kHz	V_{RS} = 0, V_{TR} = 5V Measured at Pin 14
Input:					
Impedance		15		kΩ	
Threshold		1.4		V	
Output:					
Sink Current		10		mA	V_{OL} ≤0.4V
Leakage Current		0.01		μA	V_{OH} ≤15V

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic package	385 mW
Plastic package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2243C	0°C to +75°C
Storage	−65°C to +150°C

PRINCIPLE OF OPERATION

The ultralong time delay micropower timer, in simplest block diagram terms, consists of a timing section followed by a counter section and a control flip-flop. A functional diagram of the circuit including the power shut down is shown in Figure 1.

The main functional portion of the circuit is the time base section. It is a relaxation oscillator whose period of oscillation is determined by the external R and C values. The timing section is followed by an I^2L counter, which consists of eleven binary stages, with high current drive capability output stages from the first and the last. A third subsection of the circuit is the control logic circuit consisting of a flip-flop that is set and reset by Pins 6 and 5, respectively. This section controls the resetting of all counter stages, and starting the timing circuit upon application of a positive-going trigger pulse. The control logic also activates the power shut down circuit when a reset pulse is received, or when the timing cycle is completed. The power shut down circuit turns off the bias line to the time base and I^2L counters to reduce the standby power. A simplified schematic diagram of the circuit is given in Figure 2.

CONTROL FLIP-FLOP

The logic flip-flop circuit controls the timer/counter, as well as the internal power, to reduce standby current consumption to approximately 100μA. Upon command, by a positive-going trigger pulse applied to Pin 6, the control logic circuit will first establish the upper and lower threshold voltages and then setup all internal current sources, biasing the time base and counter sections.

The circuit will automatically reset itself when power is first applied. Once triggered, the circuit is immune to additional trigger pulses until it is reset. A reset pin terminates the timing cycle by resetting the internal logic and shuts off the internal bias circuitry.

TIME BASE OSCILLATOR

The time base oscillator is a simple exponential ramp type timer circuit. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, the discharge transistor is "off", and the external capacitor, C, is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_{th-}, the upper comparator changes state, resets the flip-flop and turns the discharge transistor "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_{th+}, the comparator changes state, sets the flip-flop again, and discharges C back to the lower threshold level, V_{th-}. In this manner, the circuit continues to oscillate with the voltage level across C exponentially rising to V_{th+}, then rapidly decaying to V_{th-} and then repeating this cycle until the timing period ends.

COUNTER SECTION (Pin 8)

The counter consists of eleven stages connected in a "ripple counter" configuration. The operating injector currents are set from a bus of 1.2 volts. This current is supply independent. Pin 8, which is time base o/p, is also the counter section input.

I^2L counters are D-type flip-flops with their $\overline{Q}$ output internally connected to their D input; basically, they form a divide by 2 block. With eleven stages, one could create delays of 1024 RC in a monostable mode of operation. The counters change state on the falling edge of the clock pulses.

When the trigger pulse is applied, the internal power line which is supplying voltage for I^2L circuitry ($I^2L_{V_{CC}}$) is set up first, a Schmitt trigger circuit with a built in delay ensures the application of an internal set pulse, right after the power for the I^2 section is made available. The counters are all set to "1" and are ready to count with the incoming falling edges of clock impulses.

OUTPUT SECTIONS (Pins 2 and 3)

The output sections are designed such that they can handle 10mA load currents @ V_{OL} = 300mV. Both of the transistors in this section are operating in a nonsaturated mode because of the clamping action. This ensures faster operation and also decreases the need of high base drive at full load operation.

The timing cycle for the circuit is initiated by applying a positive-going trigger to the set, or trigger pin, (Pin 6) of the device. The trigger pulse actuates the time base oscillator, enables the counter section, and sets the outputs to "low" state. The time base oscillator generates timing pulses with its period, T = 1RC. These timing or clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to the reset pin (Pin 5).

ASTABLE AND MONOSTABLE MODE

Figure 3 shows the basic connection diagram for astable and monostable modes. When switch S_1 is open, the circuit is in its astable mode of operation. Upon the application of a trigger pulse, the time base oscillator resumes the timing cycles. Until the application of a reset pulse, the circuit will keep on working while generating a square wave at the last stage output, whose frequency is 1/2048 of the time base oscillator frequency. When switch S_1 is closed, the circuit is in its monostable mode of operation, with the last stage being connected to the reset input via an external resistor. This way, when a trigger pulse is applied, and the time base resumes its timing cycle, the last stage output will go low with the first pulse generated by the time base generator, and will stay low for 1024 pulses. With the arrival of the 1024th pulse, the last output will go to a high state since it is coupled to the reset input (see Figure 4). When this stage goes high, the timing cycle is completed.

CASCADED MODE

The cascaded mode of operation allows the generation of ultra-long time delays. When several XR-2243 circuits are cascaded, such that their counter sections are connected in series, the total count available increases geometrically rather than arithmetically. Since one XR-2243 is capable of generating a total of 1024 RC time delay, where R and C are the external timing components, then when two such timers are cascaded, they will produce $(1024)^2$ RC and three will produce $(1024)^3$ RC time delay, and so on. Thus, one can easily achieve time delays in the range of days, months, or years, simply by cascading two or three such counter/timer circuits.

Figure 5 shows the basic connection for cascaded operation. Unit 2's time base is disabled by grounding Pin 7 to ground via 1 kΩ resistor. The last stage output of Unit 1 is connected to the input of the counter section of Unit 2. When the circuit is triggered, Unit 1 will resume generating a frequency whose period T = $R_{ext}C_{ext}$. The output of Unit 1 will change state every 1024 pulses. Since these pulses are supplied to Unit 2, the circuit will stop the timing cycle after 1024 pulses are generated by Unit 1. Therefore, a time delay of $(1024)^2$ RC is generated.

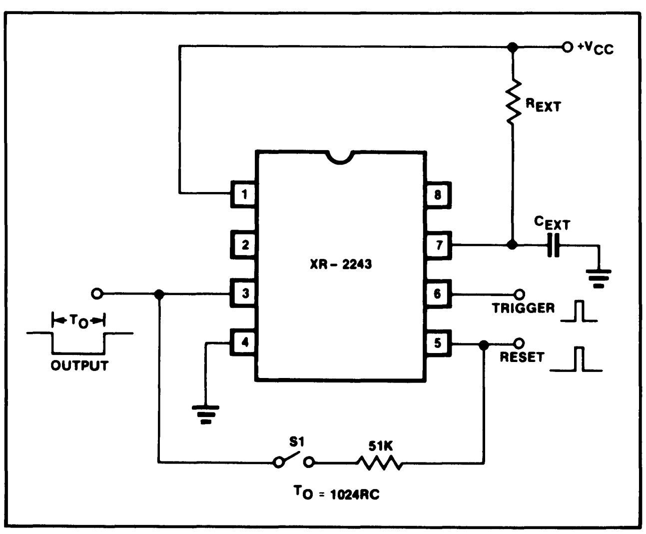


Figure 3: Typical Operation Diagram

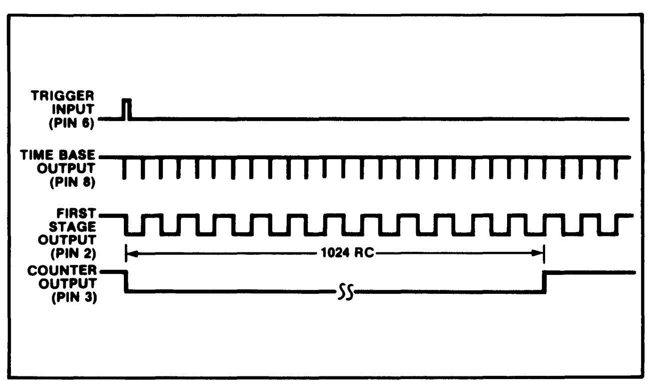


Figure 4: Timing Diagram of Output Waveforms

SEQUENTIAL TIMING APPLICATIONS

Figure 6 shows the basic connections for sequential timing applications. In this mode of operation, Unit 2's trigger input is connected to Unit 1's last output, while each unit's reset input is connected to their last output via external resistors. This way, Unit 1 will generate a time delay 1024 R_1C_1 upon the application of a trigger pulse. Once 1024 R_1C_1 seconds have elapsed, Unit 2 will be triggered, generating in its turn a delay equal to 1024 R_2C_2 seconds; therefore, resulting in an overall time delay of 1024 R_1C_1 + 1024 R_2C_2.

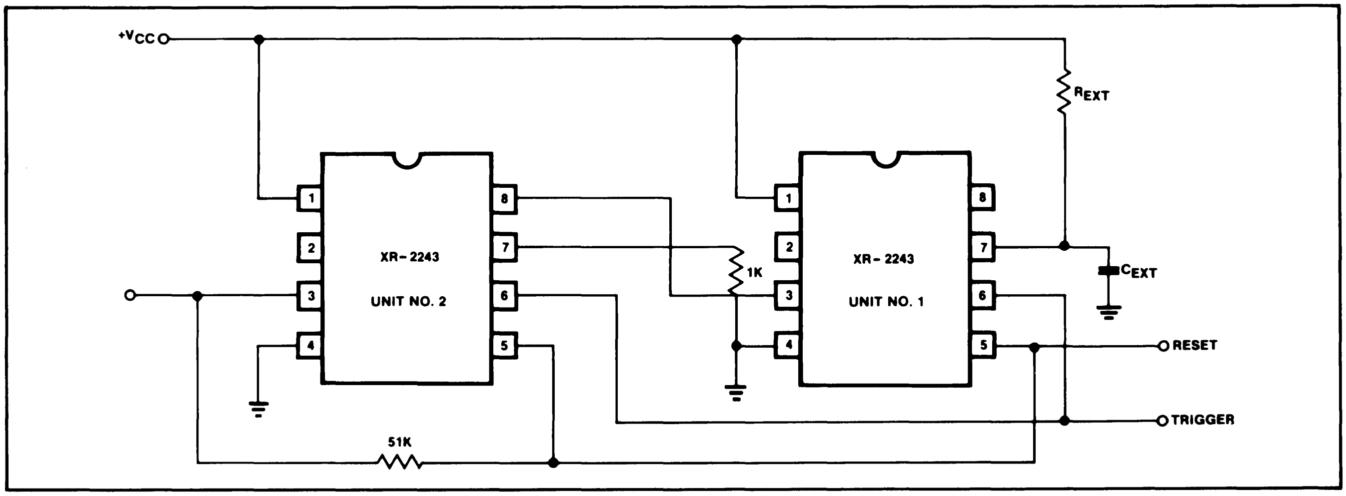


Figure 5: Cascaded Operation of Two XR-2243 Timer Circuits

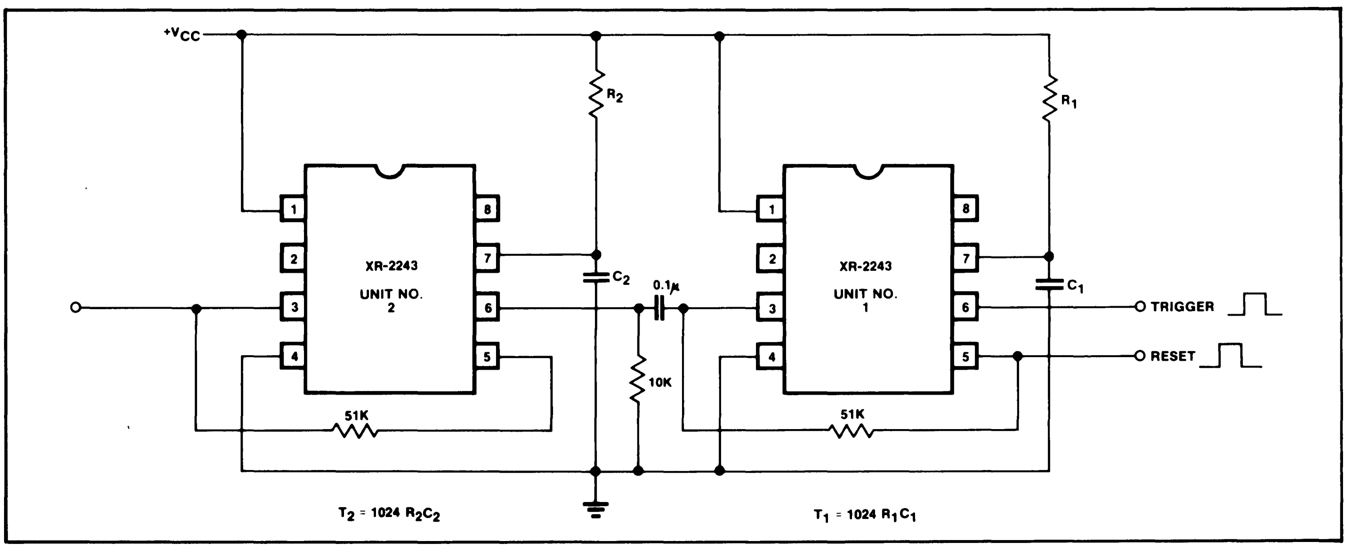


Figure 6: Sequential Timing Using XR-2243 Timer Circuits

Application Note AN-07

Single-Chip Frequency Synthesizer Employing the XR-2240

INTRODUCTION

The XR-2240 monolithic timer/counter contains an 8-bit programmable binary counter and a stable time-base oscillator in a single 16-pin IC package. Although the circuit was originally designed as a long-delay timer capable of generating time delays from microseconds to weeks, it also offers a wide range of other applications beyond simple time-delay generation. One such unique application is its use as a single-chip, frequency synthesizer, where it can generate over 2,500 discrete frequencies from a single reference frequency input.

The operation of the XR-2240 as a frequency synthesizer is possible because of the ability of the circuit to both *multiply* and *divide* the input frequency reference. It can, simultaneously, multiply the input frequency by a factor, "M," and divide it by a factor "N + 1," where both M and N are adjustable integer values. Therefore, the circuit can produce an output frequency, f_O, related to the input reference frequency f_R as:

$$f_O = f_R \frac{M}{1 + N}$$

Figure 1 shows the circuit connection for operating the XR-2240 timer/counter as a self-contained frequency synthesizer. The integer values M and N can be externally adjusted over a broad range:

$$1 \leqslant M \leqslant 10 \qquad 1 \leqslant N \leqslant 255$$

The multiplication factor M is obtained by locking on the harmonics of the input frequency. The division factor N is determined by the pre-programmed count in the binary counter section. The principle of operation of the circuit can be best understood by briefly examining its capabilities for frequency division and multiplication separately.

Frequency Division by (1 + N):

When there is no external reference input, f_R, the time-base oscillator section of the XR-2240 free-runs at its set frequency, f_S ($f_S = 1/RC$), where R and C are the external components at pin 13. The 8-bit binary counter can be programmed to divide the time-base frequency by an integer count, N, and generate an output pulse train whose frequency is:

$$f_O = f_S \frac{1}{1 + N}$$

Frequency Multiplication by "M":

Frequency multiplication is achieved by synchronizing the time-base oscillator with the *harmonics* of the input sync or reference signal. Thus, if the time-base oscillator is made to free-run at "M" times the input frequency, it can be made to synchronize with the "M"th harmonic of the input reference signal. Typical capture range of the circuit is better than ±3%, for values of $1 \leqslant M \leqslant 10$; and since the time-base is accurate to within ±0.5% of the external R-C setting, lock-up does not present a problem for a given harmonic lock setting.

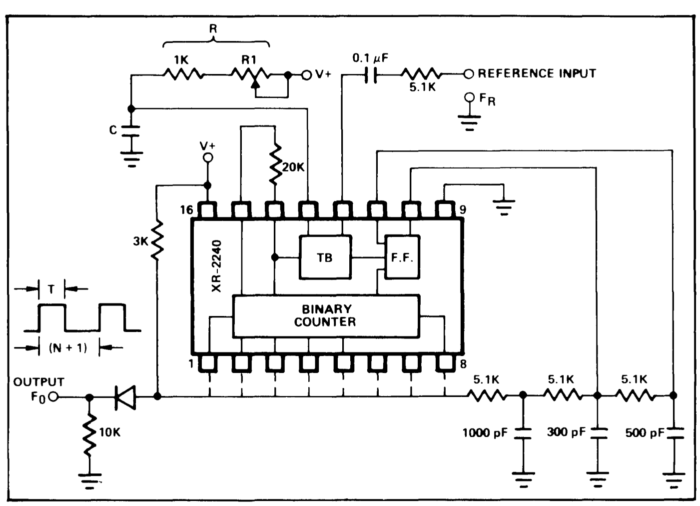


Figure 1.

Circuit Operation:

With reference to Figure 1, the operation of the synthesizer circuit can be briefly explained as follows: The reference input frequency, f_R, is applied to the time-base sync terminal (pin 12) through a 5.1 KΩ series resistance and a coupling capacitor. The recommended waveform for the input frequency, f_R, is a 3 Vpp pulse train with a pulse width in the range of 30% to 80% of the time-base period, T. The multiplication factor M is chosen by the potentiometer R_1 which sets the time-base period T (T = RC). If no external reference is used, then M is automatically equal to 1.

The divider modulus, N, is chosen by shorting various counter outputs to a 3K common pull-up resistor. The output waveform is a pulse train with a fixed pulse width, T = RC, and a period $T_O = (N + 1)RC$.

The external R-C network between the output and the trigger and reset terminals of the XR-2240 is a non-critical delay network which resets and re-triggers the circuit to maintain a periodic output waveform. For the component values shown in Figure 1, the circuit can operate with the timing components R and C in the range of:

$$0.005\ \mu F \leqslant C \leqslant .1\ \mu F;\ 1\ K\Omega \leqslant R \leqslant 1\ M\Omega$$

The XR-2240 is a low-frequency circuit. Therefore, the maximum output frequency is limited to ≈200 kHz, by the frequency capability of the internal time base oscillator.

A particularly useful application of the simple synthesizer circuit of Figure 1 is to generate stable clock frequencies which are synchronized to an external reference, such as the 60 Hz line frequency. For example, one can generate a 100 Hz reference synchronized to 60 Hz line frequency simply by setting M = 5 and N = 2 such that:

$$f_O = f_R \frac{M}{1 + N} = (60) \frac{5}{1 + 2} = 100 \text{ Hz}$$

Application Note AN-15

An Electronic Music Synthesizer Using the XR-2207 and the XR-2240

INTRODUCTION

This application note describes a simple, low-cost "music synthesizer" system made up of two monolithic IC's and a minimum number of external components. The electronic music synthesizer is comprised of the XR-2207 programmable tone generator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 monolithic counter/timer circuit.

PRINCIPLE OF OPERATION

All the active components necessary for the electronic music synthesizer system is contained in the two low-cost monolithic IC's, the XR-2207 variable frequency oscillator and the XR-2240 programmable counter/timer. Figure 1 shows the functional block diagram of the XR-2207 oscillator. This monolithic IC is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and square-wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2240 programmable counter/timer is comprised of an internal time-base oscillator, a control flip-flop and a programmable 8-bit binary counter. Its functional block diagram is shown in Figure 2, in terms of the 16-pin IC package. The eight separate output terminals of the XR-2240 are "open-collector" type outputs which can either be used individually, or can be connected in a "wired-or" configuration.

Figure 3 shows the circuit connection for the electronic music or time synthesizer system using the XR-2207 and the XR-2240. The XR-2207 produces a sequence of tones by oscillating at a frequency set by the external capacitor C_1 and the resistors R_1 through R_6 connected to Pins 4 through 17. These resistors set the frequency or the "pitch" of the output tone sequence. The counter/timer IC generates the pseudo-random pulse patterns by selectively counting down the time-base frequency. The counter outputs of XR-2240 (Pins 1 through 8) then activate the timing resistors R_1 through R_6 of the oscillator IC, which converts the binary pulse patterns to tones. The time-base oscillator frequency of the counter/timer sets the "beat" or the tempo of the music. This setting is done through C_3 and R_0 of Figure 3.

The pulse sequence coming out of the counter/timer IC can be programmed by the choice of counter outputs (Pins 1 through 8 of XR-2240 connected to the programming pins (Pins 4 through 7) of the XR-2207 VCO. The connection of Figure 3 is recommended since it gives a particularly melodic tone sequence at the output.

The pseudo-random pulse pattern out of the counter-timer repeats itself at 8-bit (or 256 count) intervals of the time-base period. Thus, the output tone sequence continues for about 1 to 2 minutes (depending on the "beat") and then repeats itself. The counter/timer resets to zero when the device is turned on; thus, the music, or the tone sequence, always starts from the same point when the synthesizer is turned on.

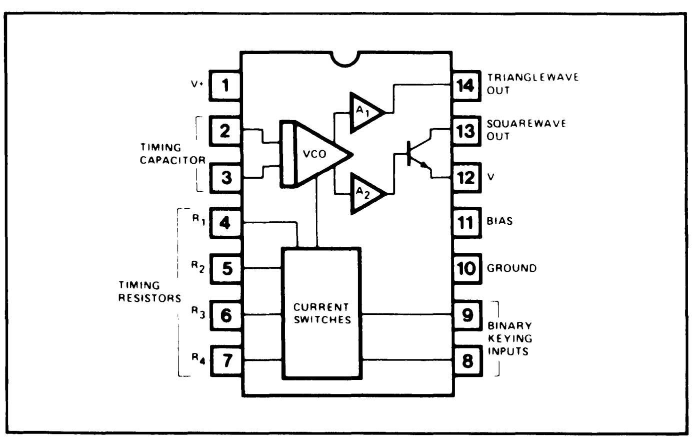


Figure 1. Functional Block Diagram of XR-2207 Oscillator Circuit.

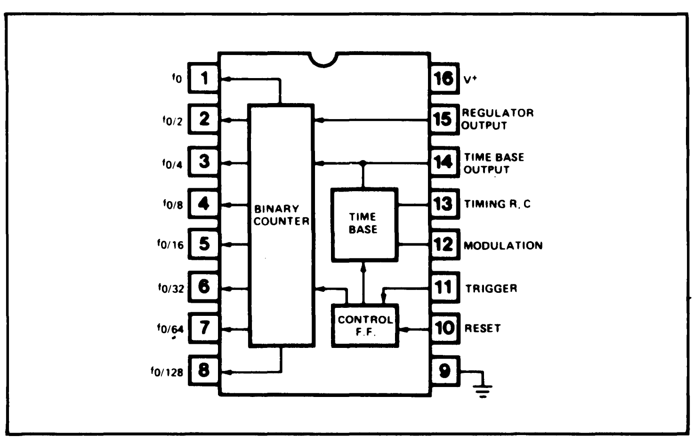


Figure 2. Functional Block Diagram of XR-2240 Counter/Timer.

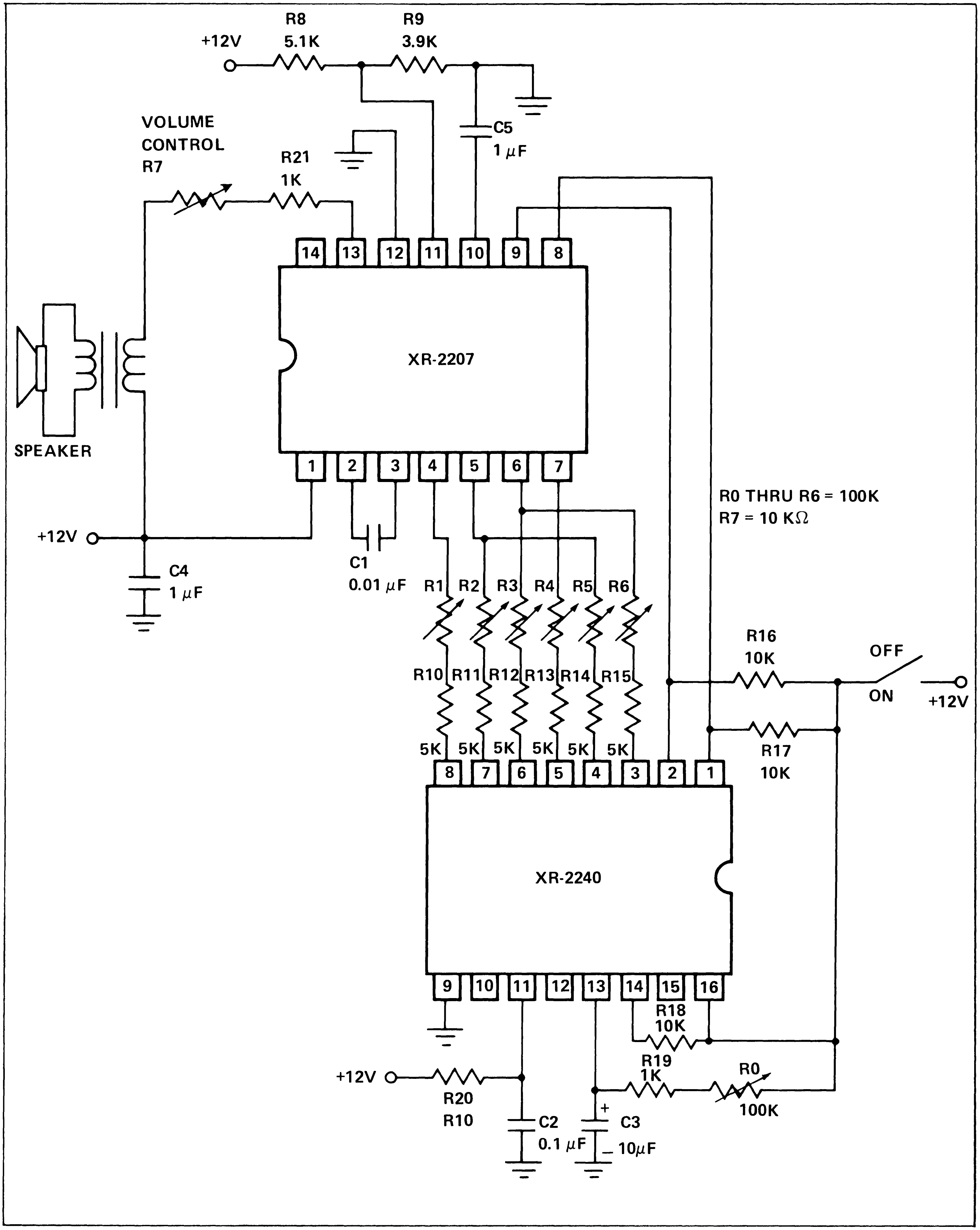
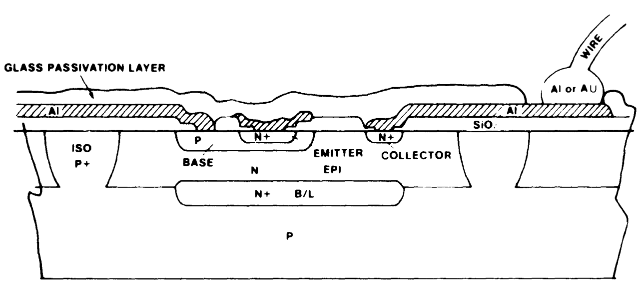


Figure 3. Circuit Connection Diagram for the Music Synthesizer.

Monolithic Chips for Hybrid Assemblies

The major performance characteristics of Exar products are also available in chip form. All chips are 100% electrically tested for guaranteed DC parameters at 25°C; and 100% visually inspected at 30x to 100x magnification using Exar's standard visual inspection criteria or MIL-STD-883, Method 201, depending on the individual customer requirements. Each chip is protected with an inert glass passivation layer over the metal interconnections. The chips are packaged in waffle-pack carriers with an anti-static shield and cushioning strip plated over the active surface to assure protection during shipment. All chips are produced on the same well-proven production lines that produce Exar's standard encapsulated devices. The Quality Assurance testing of dice is provided by normal production testing of packaged devices.



Typical Bipolar Chip Cross Section

FEATURES

DC Parameters Guaranteed at 25°C
100% Visual Inspection
Care in Packaging
100% Stabilization Bake (Wafer Form)
10% LTPD on DC Electrical Parameters

CHIPS IN WAFER FORM

Probed and inked wafers are also available from Exar. The hybrid microcircuit designer can specify either scribed or unscribed wafers and receive a fully tested silicon wafer. Rejected die are clearly marked with an ink dot for easy identification in wafer form.

ELECTRICAL PARAMETERS

Probing the IC chips in die form limits the electrical testing to low level DC parameters at 25°C. These DC parameters are characteristic of those parameters contained on the individual device data sheet and are guaranteed to an LTPD of 10%.

The AC parameters, which are similar to those in the standard Exar device data sheets, have been correlated to selected DC probe parameters and are guaranteed to an LTPD of 20%.

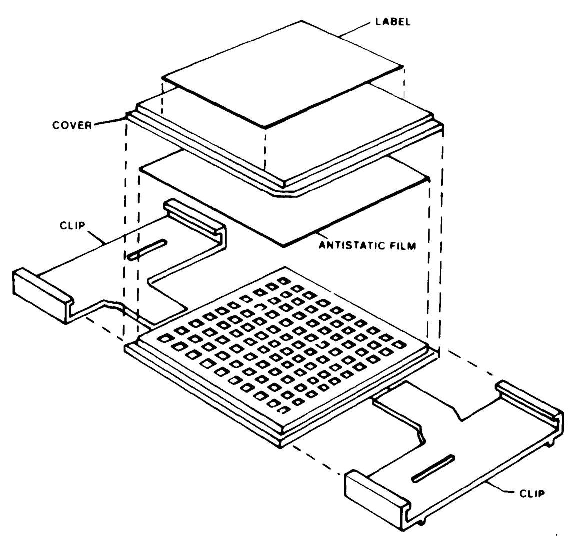
HANDLING PRECAUTIONS AND PACKAGING OPTIONS

Extreme care must be used in the handling of unencapsulated semiconductor chips or dice to avoid damage to the chip surface. Exar offers the following three handling or packaging options for monolithic chips supplied to the customer:

Cavity or Waffle Pack: The dice are placed in individual compartments of the waffle pack (see figure). The plastic snap clips permit inspection and resealing.

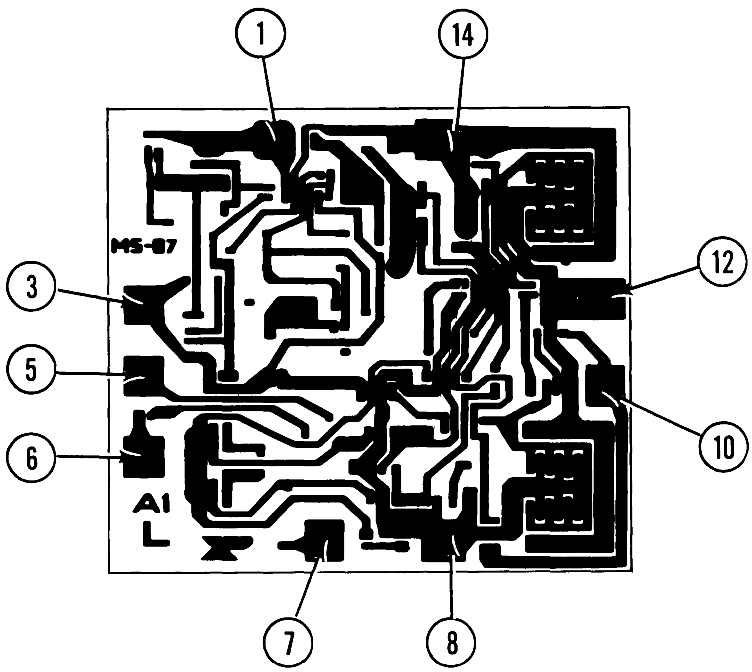
Vial Pack: The vial is filled with inert freon TF and a plastic cap seals the vial. The freon acts as a motion retarder and cleansing agent.

Wafer Pack: The entire wafer is sandwiched between two pieces of mylar and vacuum sealed in a plastic envelope.



Typical Cavity Pack (Waffle Pack)

XR-320 MONOLITHIC TIMING CIRCUIT

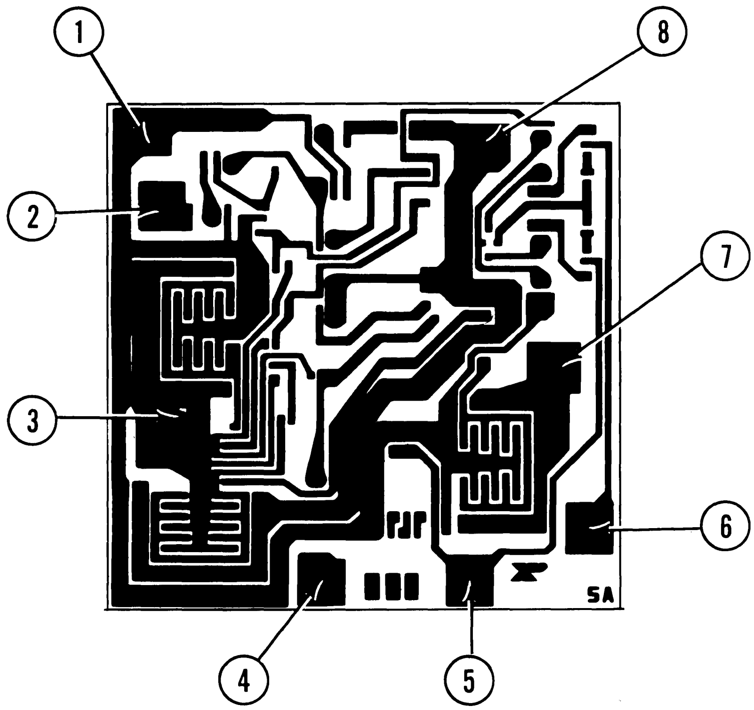


Pad No.*	Pad Function
1	Current Source Input
3	Current Source Output
5	Negative Trigger
6	Positive Trigger
7	Reset
8	Ground
10	Logic Output
12	High Current Output
14	V_{CC}

*Note: Pad numbers also correspond to package pin numbers.

Chip size: 52 mils x 58 mils
(1.32 mm x 1.47 mm)

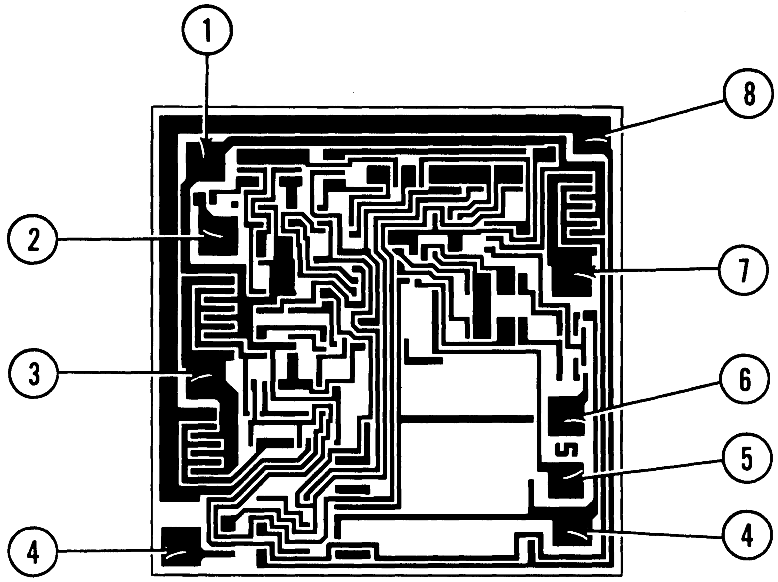
XR-555 TIMING CIRCUIT



Pad No.	Pad Function
1	Ground
2	Trigger
3	Output
4	Reset
5	Control
6	Threshold
7	Discharge
8	V_{CC}

Chip Size: 55 mils x 53 mils
(1.39 mm x 1.34 mm)

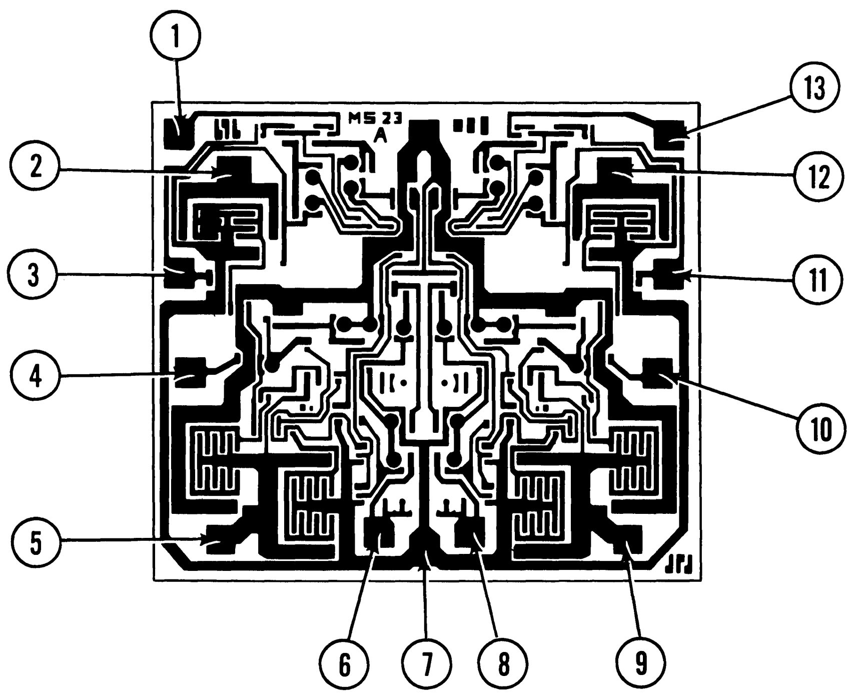
XR-L555 MICROPOWER TIMING CIRCUIT



Pad No.	Pad Function
1	Ground
2	Trigger
3	Output
4	Reset
5	Control
6	Threshold
7	Discharge
8	V_{CC}

Chip Size: 57 x 57 mils
(1.44 mm x 1.44 mm)

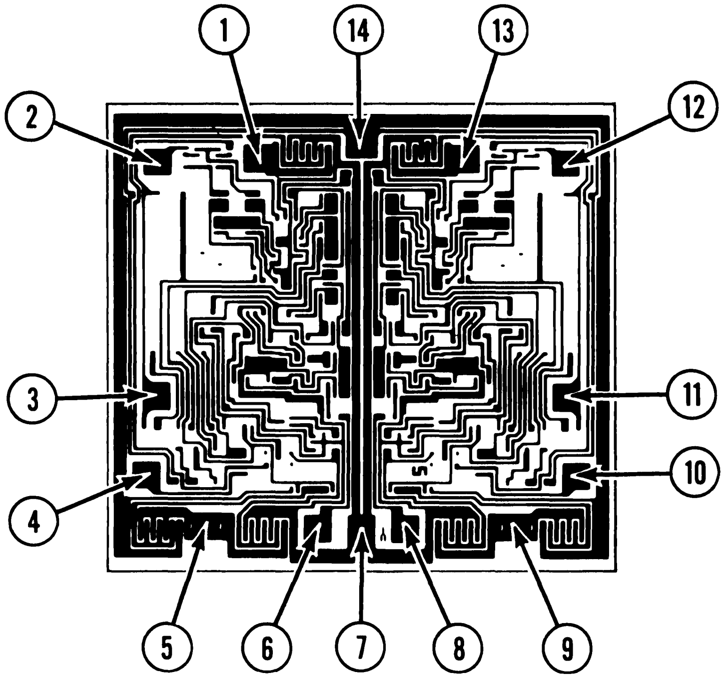
XR-556 DUAL TIMER



Pad No.	Pad Function
1	Discharge 1
2	Threshold 1
3	Control 1
4	Reset 1
5	Output 1
6	Trigger 1
7	Ground
8	Trigger 2
9	Output 2
10	Reset 2
11	Control 2
12	Threshold 2
13	Discharge 2
14	V_{CC}

Chip Size: 66 x 75 mils
(1.67 x 1.90 mm)

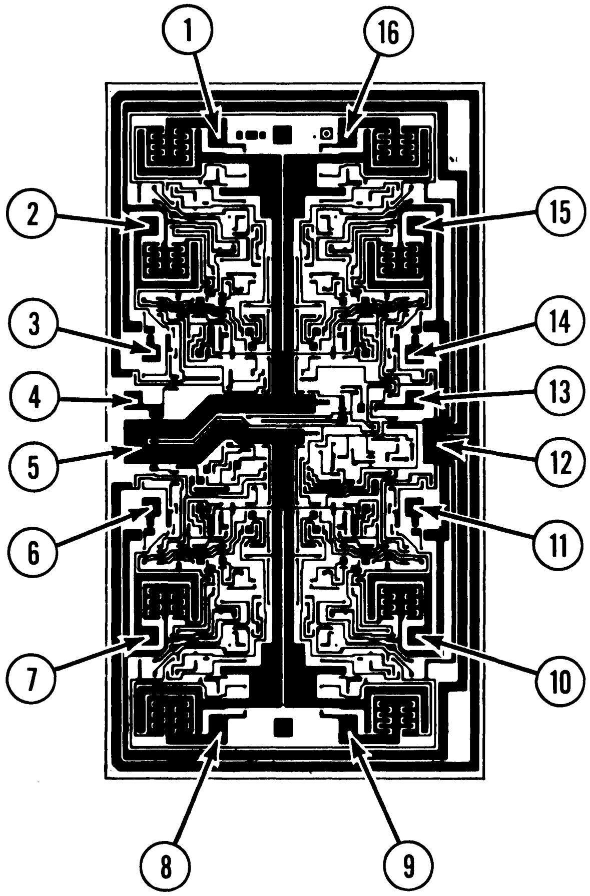
XR-L556 MICROPOWER DUAL TIMER



Pad No.	Pad Function
1	Discharge 1
2	Threshold 1
3	Control 1
4	Reset 1
5	Output 1
6	Trigger 1
7	Ground
8	Trigger 2
9	Output 2
10	Reset 2
11	Control 2
12	Threshold 2
13	Discharge 2
14	V_{CC}

Chip Size: 84 mils x 77 mils
(3.31 mm x 3.03 mm)

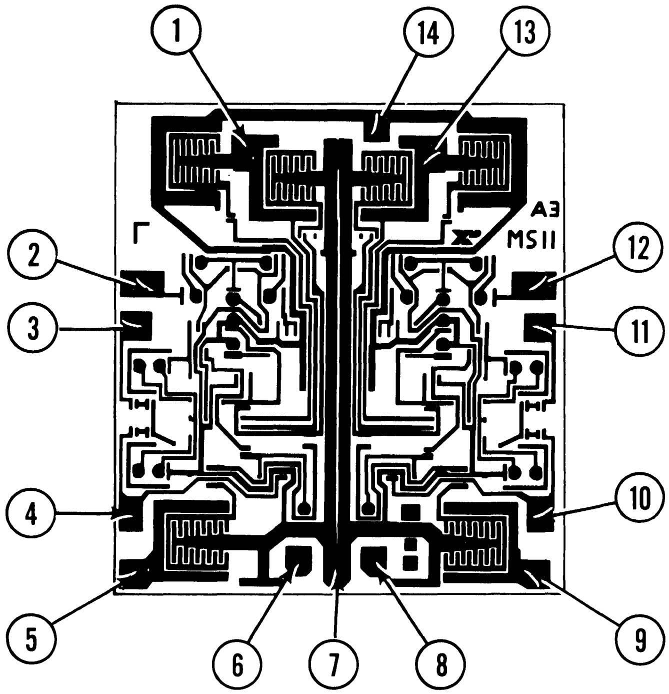
XR-558/XR-559 QUAD TIMING CIRCUITS



Pad No.	Pad Function
1	Output A
2	Timing A
3	Trigger A
4	Modulation
5	V_{CC}
6	Trigger B
7	Timing B
8	Output B
9	Output C
10	Timing C
11	Trigger C
12	Ground
13	Reset
14	Trigger D
15	Timing D
16	Output D

Chip Size: 80 mils x 143 mils
(3.15 mm x 5.63 mm)

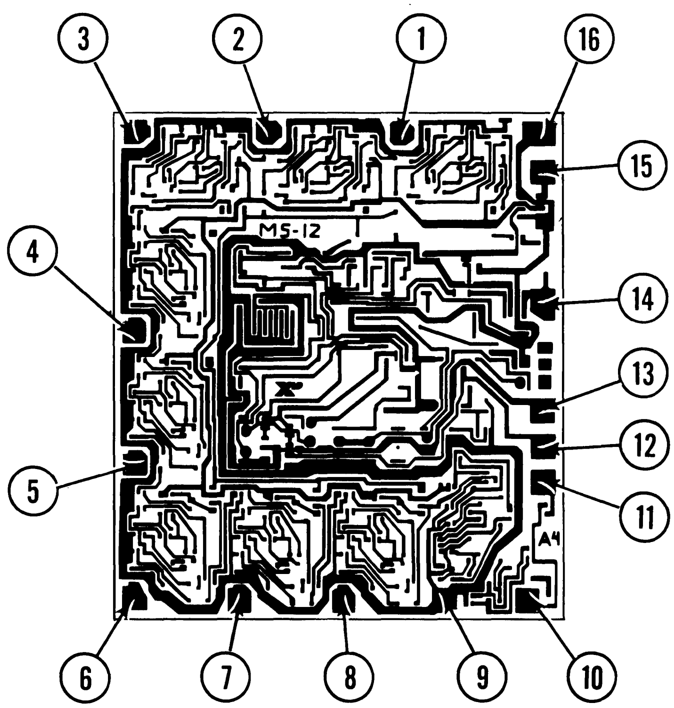
XR-2556 DUAL TIMING CIRCUIT



Pad No.	Pad Function
1	Output 1
2	Trigger 1
3	Threshold 1
4	Control 1
5	Discharge 1
6	Reset 1
7	Ground
8	Reset 2
9	Discharge 2
10	Control 2
11	Threshold 2
12	Trigger 2
13	Output 2
14	V_{CC}

Chip Size: 80 x 87 mils
(2.03 x 2.20 mm)

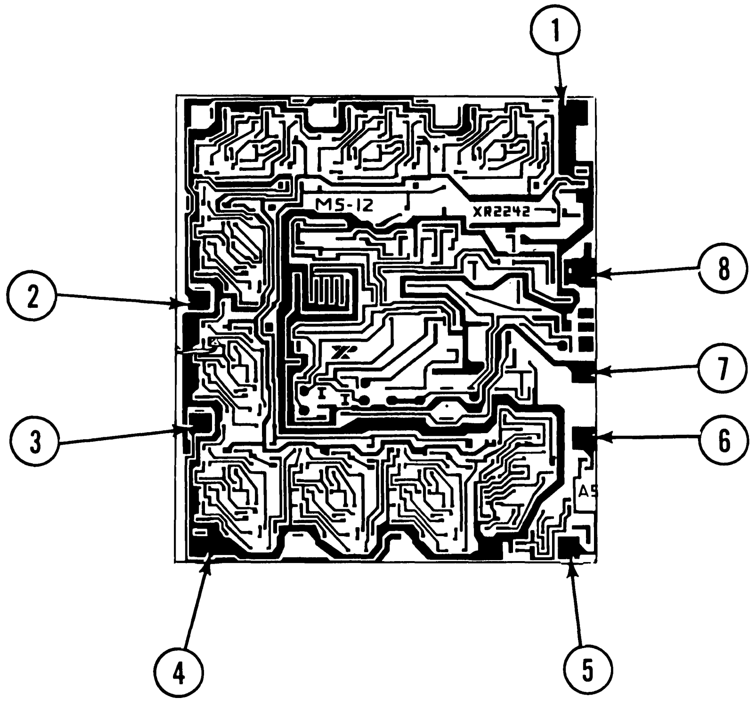
XR-2240 PROGRAMMABLE TIMER/COUNTER



Pad No.	Pad Function
1	Counter Output 1
2	Counter Output 2
3	Counter Output 3
4	Counter Output 4
5	Counter Output 5
6	Counter Output 6
7	Counter Output 7
8	Counter Output 8
9	Ground
10	Reset
11	Trigger
12	Modulation
13	Timing R.C.
14	Time Base Output
15	Regulator Output
16	V_{CC}

Chip Size: 84 mils x 95 mils
(2.13 mm x 2.41 mm)

XR-2242 LONG-RANGE TIMER



Pad No.	Pad Function
1	V_{CC}
2	Output 2
3	Output 1
4	Ground
5	Reset
6	Trigger
7	Timing R.C.
8	Time Base Output

Chip Size: 84 mils x 95 mils
(2.13 mm x 2.41 mm)

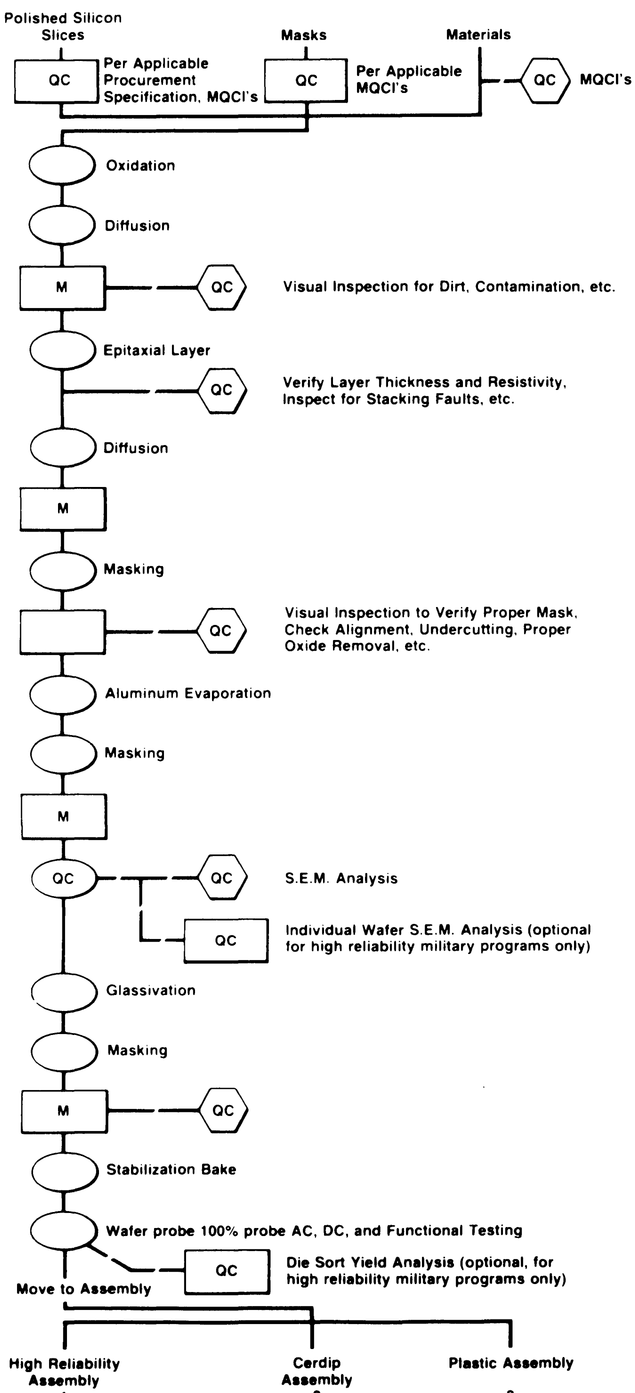
QUALITY ASSURANCE STANDARDS

The quality assurance program at Exar Integrated Systems defines and establishes standards and controls on manufacturing, and audits product quality at critical points during manufacturing. The accompanying Manufacturing/QA process flows illustrate where quality assurance audits, by inspection or test, the manufacturing process. The insertion of these quality assurance points is designed to insure the highest quality standards are maintained on Exar product during its manufacture.

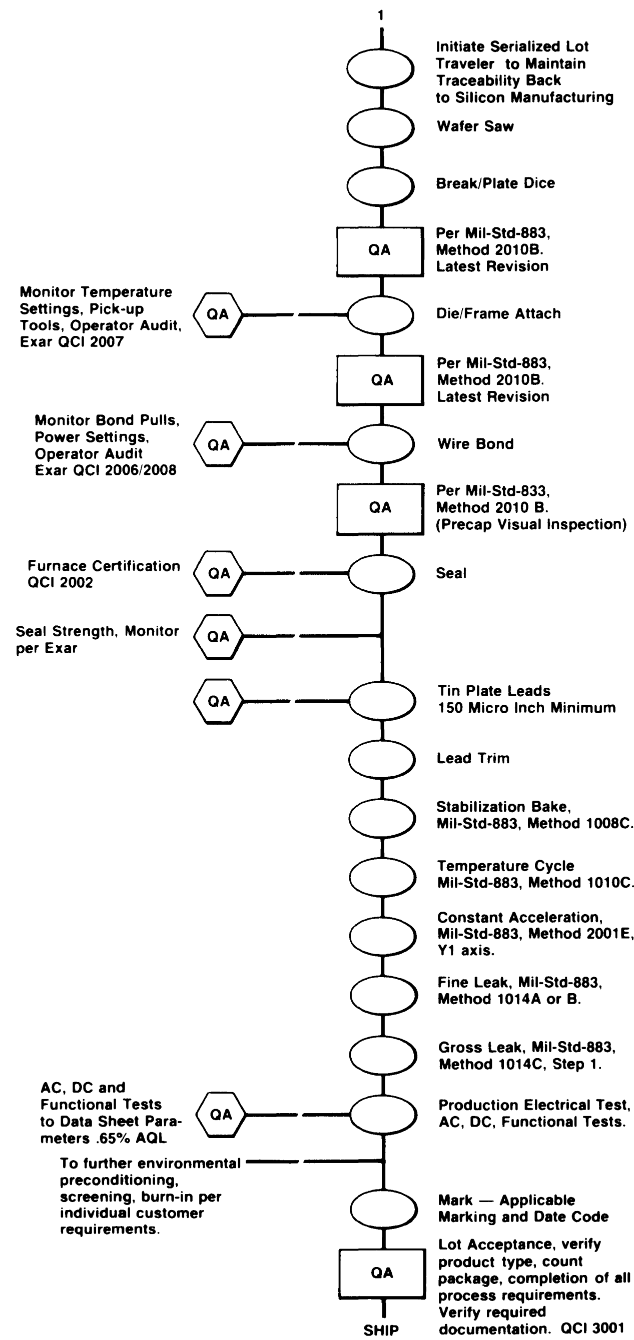
Realizing that these standard Manufacturing/QA process flows do not meet the needs of every customer's specific requirements, Exar quality assurance can negotiate and will screen product to meet any individual customer's specific requirement.

All products ending with the suffix M are fully screened to the requirements of MIL-STD-883, Method 5004, Condition C.

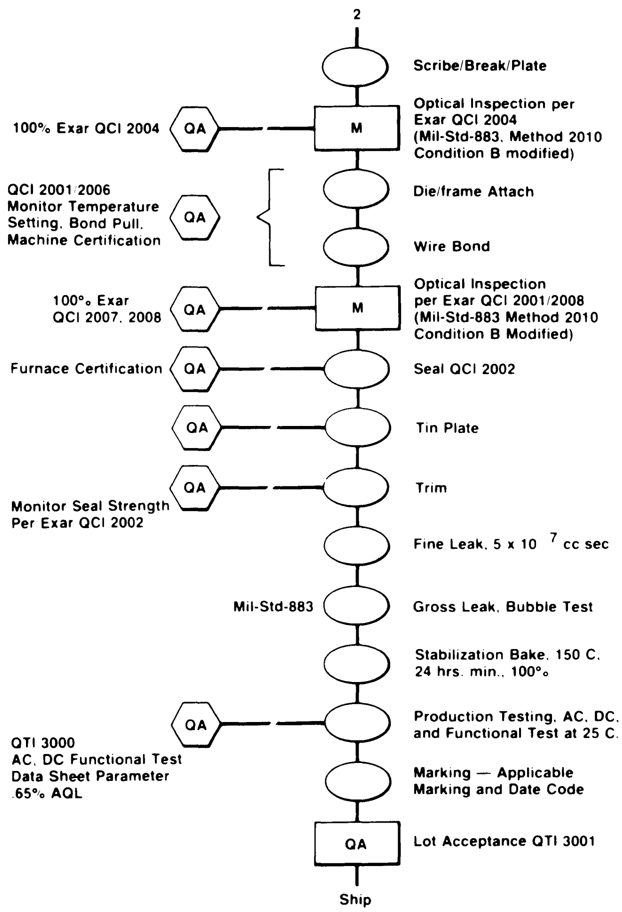
Wafer Fabrication/QA Flow



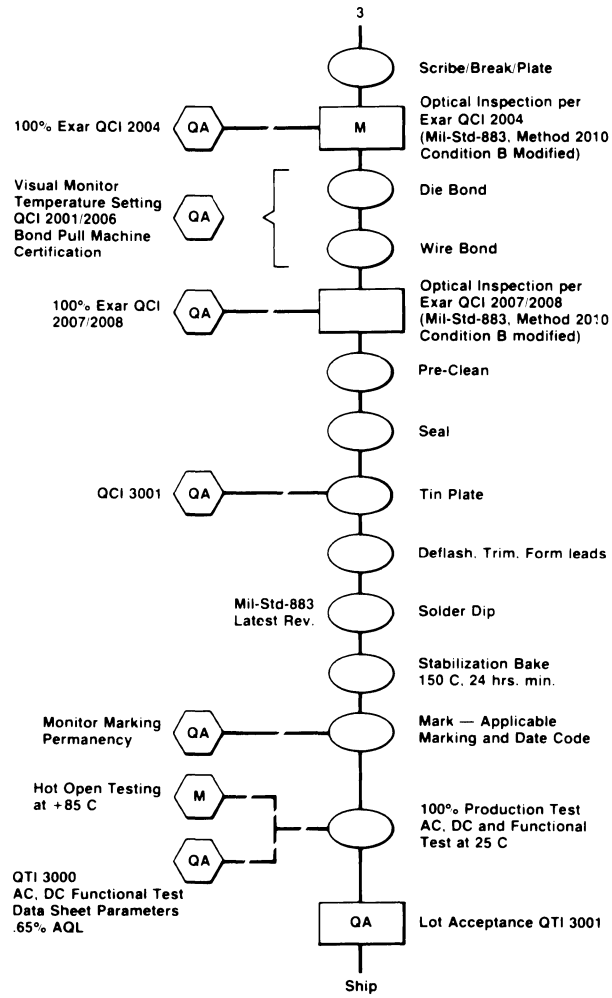
High Reliability Assembly/QA Flow



Cerdip Assembly/QA Flow



Plastic Assembly/QA Flow



PRODUCT ORDERING INFORMATION

Part Identification

XR
Manufacturer's Prefix

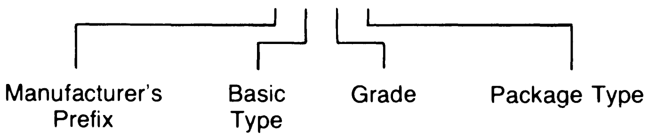
Grade
M = Military
N = Prime Electrical
P = Prime Electrical
C = Commercial
K = Kit

XXXXX
Basic Type (5 spaces)

Package Type
N = Ceramic Dual-in-line
P = Plastic Dual-in-line

Example:

XR-2216 CN



Definition of Symbols:

M = Military Grade Part, Ceramic Package Only. All Military Grades have been processed to MIL-STD-883 Level C, and are guaranteed to operate over military temperture range.
N = Prime Grade Part, Ceramic Package.
P = Prime Grade Part, Plastic Package.
CN = Commercial Grade Part, Ceramic Package.
CP = Commercial Grade Part, Plastic Package.

N, P, CN and CP parts are electrically identical and guaranteed to operate over 0°C to + 75°C range unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts.

For details, consult Exar Sales Headquarters or Sales /Technical Representatives.

Legend:

Surveillance — 100% inspection

Operation — QC = Quality Control, M = Manufacturing

Application Notes

Exar's Applications Engineering Department has prepared a comprehensive set of application notes and information in Exar's products and technologies. A list of these application notes, along with a brief description of their contents, is given below:

AN-01: Stable FSK Modems Featuring the XR-2206, XR-2207 and XR-2211
Design of stable full-duplex FSK modems is described using the XR-2206 or the XR-2207 as the modulator, and the XR-2211 as the demodulator with carrier-detection capability. Complete design examples are given for FSK modems covering mark/space frequencies from a few Hertz to 100 kHz.

AN-02: XR-C240 Monolithic PCM Repeater
The principle of operation of the XR-C240 monolithic regenerative repeater IC is described. Design examples and external connections of the circuit are discussed for applications in T-1 type 1.544 Megabit PCM telephone lines.

AN-03: Active Filter Design with IC Op-Amps
Fundamentals of active filters are discussed, transfer functions and design equations for various classes of high-, low- and band-pass filters are given. Particular design examples are provided for FSK modem filters, using the XR-4202 programmable quad op-amp.

AN-04: XR-C277 Low-Voltage PCM Repeater IC
The design principles and the applications of the XR-C277 low-voltage (6.3 volt) regenerative PCM repeater are described. The monolithic IC contains all the basic functional blocks of a conventional PCM repeater, including the automatic line built-out section. Circuit connection diagrams and application examples are given for operation in 1.544 Megabit T-1 type PCM telephone systems.

AN-05: Tri-State FSK Modem Design Using XR-2206/XR-2211
Design of FSK modems with carrier detection and control capability are discussed. Such a "tri-state" modem uses a third carrier frequency for control functions, in addition to the normal "mark" and "space" frequencies used in conventional "bi-state" FSK systems. This carrier control feature allows each transmitter in a modem system to be automatically interrogated, one at a time, by a control processor, without interference from other modem transmitters within the system.

AN-06: Precision PLL System Using XR-2207/XR-2208
A two-chip versatile phase-locked loop system is described, using the XR-2207 oscillator as the VCO, and the XR-2208 multiplier as the phase detector. The resulting PLL system features 20 ppm/°C temperature stability. Design equations are given to tailor the circuit parameters to specific applications.

AN-07: Single-Chip Frequency Synthesizer Employing the XR-2240 (Reprinted in This Data Book)
The operation of the XR-2240 programmable/counter IC as a frequency synthesizer is described. The circuit can simultaneously multiply an input frequency by an integer modulus M, and divide it by a different modulus N+1. Thus, a wide range of non-integer output frequencies can be produced from a single input reference frequency.

AN-08: Dual-Tone Decoding with XR-567 and XR-2567
Application examples are given for simultaneous or sequential decoding of dual-tone control signals using either two XR-567 PLL tone decoders, or a single XR-2567 dual tone decoder. The examples include high-speed, narrow-band tone detection and Touch-Tone® decoding.

AN-09: Sinusoidal Output from XR-215 Monolithic PLL Circuit
A simple circuit technique is described to convert the VCO output of the XR-215 into a low-distortion sinewave. The external sinewave-shaping circuit is obtained using the XR-C101 monolithic NPN transistor array.

AN-10: XR-C262 High-Performance PCM Repeater
The design principle and the electrical characteristics of the XR-C262 high-performance PCM repeater IC are described. The circuit contains all the active components necessary for a regenerative PCM repeater system and operates with a single 6.8 volt power supply. Circuit connection and application examples are given for its use in 1.5 Megabit or 2 Megabit PCM systems.

AN-11: A Universal Sinewave Converter Using the XR-2208 and XR-2211
A circuit technique is described which can convert *any* periodic waveform into a low-distortion sinewave. The circuit operation is completely independent of input waveform amplitude and frequency as long as the input signal is periodic, and can operate over a frequency range of 1 Hz to over 100 kHz.

AN 12: Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits
A design technique is described for high frequency tone or carrier detection. The two-chip circuit uses either the XR-210 or the XR-215 PLL circuit, in conjunction with the XR-2228 multiplier/detector, and can operate with carrier frequencies up to 20 MHz.

AN-13: Frequency Selective AM Detection Using Monolithic Phase-Locked Loops
Design of frequency selective coherent AM and AM/FM demodulator systems is described using the XR-2228 Multiplier/Detector and the XR-215 or the XR-2212 PLL ICs.

AN-14: A Complete Function Generator System Using the XR-2206
A laboratory quality self-contained function generator system is described, using the XR-2206 waveform generator IC. Complete circuit connection diagram, parts list and assembly instructions are given for a DC to 100 kHz self-contained function generator system with AM/FM capability and triangle, sine and square wave output.

AN-15: An Electronic Music Synthesizer Using the XR-2207 and the XR-2240 (Reprinted in This Data Book)
Design of a simple, low-cost "music synthesizer" system is described. The electronic music synthesizer is comprised of the XR-2207 voltage-controlled oscillator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 counter/timer circuit.

AN-16: Semi-Custom LSI Design with I^2L Gate Arrays
A unique design approach to developing complex LSI systems is described using XR-300 and XR-500 I^2L gate arrays. This technique greatly reduces the design and tooling cost and the prototype fabrication cycle associated with the conventional full-custom IC development cycle; and thus makes custom ICs economically feasible even at low production volumes.

AN-17: XR-C409 Monolithic I^2L Test Circuit
A monolithic test circuit has been developed for evaluation of speed and performance capabilities of Exar's Integrated Injection Logic (I^2L) technology. This test circuit, designated the XR-C409, is intended to familiarize the I^2L user and the system designer with some of the performance features of I^2L such as its frequency capability and power-speed tradeoffs.

Additional Technical Literature Available from Exar

PRODUCT GUIDE:

A complete short-form catalogue of all of Exar's standard and custom products, quality assurance programs and technical capabilities. Key features and applications of each of Exar's products are given, along with their functional block diagrams, package types and operating temperature ranges. Products are grouped according to their applications, and a complete industry-wide cross reference chart is provided.

LINEAR AND DIGITAL SEMI-CUSTOM DESIGN BROCHURE:

This brochure contains a detailed description of Exar's unique bipolar and integrated injection logic (I^2L) semi-custom design technology. Economic advantages of the semi-custom designs are discussed and economic guidelines are given for choosing the most cost-effective solution to a custom IC requirement. In addition, this brochure provides technical information on Exar's Master Chips and IC Design Kits.

APPLICATIONS DATA BOOK:

This book contains a complete and up-to-date set of application notes prepared by Exar's technical staff. These application notes cover a wide range of subjects such as FSK modems, active filters, telecommunication circuits, electronic music synthetics and many more. In each case, specific design examples are given to demonstrate the applications discussed. ($2.95)

FUNCTION GENERATOR DATA BOOK:

This comprehensive data book contains a number of technical articles and application notes on monolithic voltage-controlled oscillators (VCO) and function generator IC products. In addition, the data sheets and technical specifications of Exar's monolithic VCO's and function generators are given. ($2.95)

OPERATIONAL AMPLIFIER DATA BOOK:

This book contains a collection of technical articles on the fundamentals of monolithic IC op amps. Some of the basic op amp circuits are given and the application of IC op amps in active filter design are discussed. The book also contains a complete set of electrical specifications in Exar's bipolar and BIFET op amp products. ($2.95)

PHASE-LOCKED LOOP DATA BOOK:

This data book covers the fundamentals of design and applications of monolithic phase-locked loop (PLL) circuits. A long list of PPL applications are illustrated covering FM demodulation, frequency synthesis, FSK and tone detection. Particular emphasis is given to application of PLL circuits in data interface and communication systems such as FSK modems. This book also contains the data sheets and electrical specifications of all of Exar's PLL products. ($2.95)

TIMER DATA BOOK:

This data book provides a collection of technical articles and application information on monolithic timer IC products. Also included are the data sheets and the detailed specifications of all of Exar's timer circuits, including the programmable timer/counters, micropower and long-delay timers. ($2.95)

TECHNICAL LITERATURE REQUEST:

To obtain the technical literature of interest to you, contact the Exar sales representative nearest you, or write Exar, **Integrated Systems Inc., P.O. Box 62229, Sunnyvale, CA. 94088,** on your company letterhead.

Data Books can also be ordered directly from Exar, at a nominal charge, by completing and sending this request card to Exar, with an appropriate check or money order (include $2.00 for postage and handling). Please make checks payable to **Exar Integrated Systems, Inc.**

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Santa Clara, CA 95051
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El Segundo, CA 90245
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Cedar Rapids, IA 52402
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Lakeville, MN 55044
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Bridgeton, MO 63044
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Quality Components
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Manlius, NY 13104
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Commack, NY 11725
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In NJ: 800-645-5500/1
TWX 510-226-1485

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Raleigh, NC 27619
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TWX 510-928-0513

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Suite 140
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(512) 835-0064

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Carrollton, TX 75006
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TWX 910-860-5158

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Houston, TX 77081
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Salt Lake City, UT 84118
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Bellevue, WA 98007
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TWX 610-492-2540

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Suite 204
Ottawa, Ontario
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