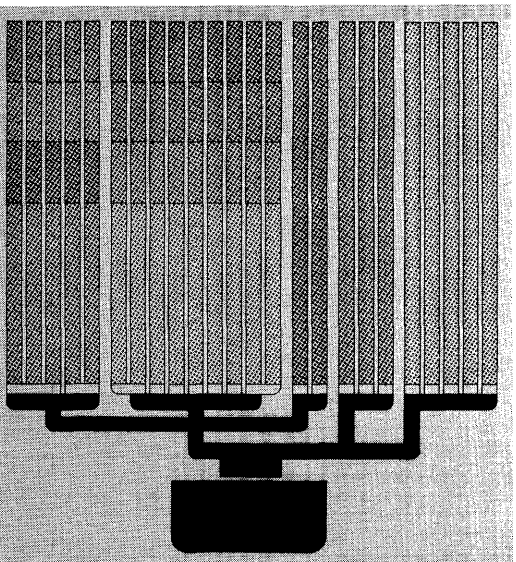

TTL Loading Rules

All devices in the Fairchild TTL family have compatible logic levels. Standard, low power and high speed device, may be mixed in a system to obtain the optimum cost, power, speed combination.

To simplify design calculations the different loading rules of each series have been normalized to one standard set of conditions.

TTL LOADING RULES

All Transistor Transistor Logic integrated circuits are derived from the simple gate schematic shown in Figure 1.

The output is LOW (logic "0") only if both inputs A and B are HIGH (logic "1"). This is defined as a positive logic NAND gate.

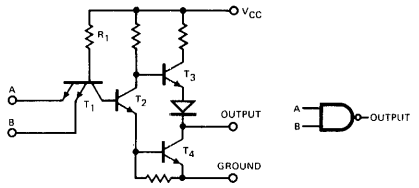

FIGURE 1

Input Characteristics

A low voltage at inputs A or B will cause current to flow out of the forward biased base-emitter diode of the multi-emitter transistor (T_1). When the voltage level at A or B or both is less than 2 $V_{BE(SAT)}$ levels, the current supplied by R_1 will flow out of the LOW input terminal (see Figure 2) keeping transistors T_2 and T_4 turned off. If both inputs A and B are raised to a HIGH voltage level, the base-emitter diodes of the input transistor (T_1) will be reverse biased. The current supplied by R_1 will then flow through the base-collector diode of T_1 (see Figure 3) turning on transistor T_2 and T_4. The HIGH level input voltage source must be capable of supplying leakage current to the reverse biased input transistor. Because of the NPN action of the input device, this leakage current is referred to as inverse beta current. The value of the input LOW current and input HIGH leakage current is dependent on the value of R_1. The value of this resistor is chosen to optimize the specific speed/power performance characteristics of each device.

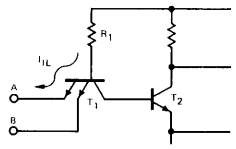

FIGURE 2

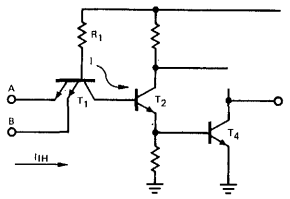

FIGURE 3

Output Characteristics

The fan out or drive capability of a TTL device reflects its ability to sink current in the output LOW (logic "0") state (see Figure 4) and to source or drive current in the output HIGH (logic "1") state (see Figure 5).

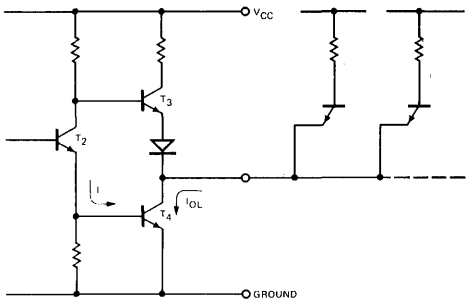

FIGURE 4

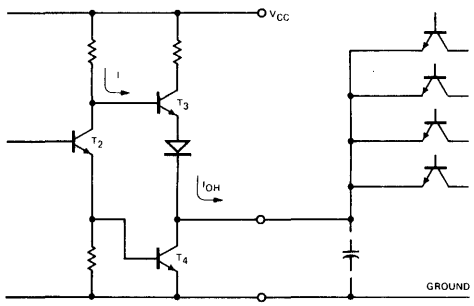

FIGURE 5

In the output LOW state the "phase splitter" transistor T_2 is "on". It supplies base drive to the output pull down transistor (T_4). The amount of base drive required for the pull down transistor is dependent on the worst case beta of the device and the fan out (I_{OL}) sink current requirements of the circuit. The output HIGH drive current (I_{OH}) of the device is supplied from the pull up transistor (T_3). When the phase splitter transistor (T_2) is turned "off", the pull up transistor is turned "on". This presents a low impedance drive source at the output. Although the static I_{OH} requirements of most circuits is less than 0.5 mA, about 35 mA is made available at the instant of LOW to HIGH output transition to charge up the distributed line, board and package capacitances encountered in most system designs. Different types of pull up circuits are used to achieve faster system speeds by minimizing HIGH output impedance and the resulting RC time constant.

Normalized Fan In/Fan Out Rules

In order to simplify designing with Fairchild TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 Unit TTL Load (U.L.) = 40 μA in the HIGH state (logic "1")
= 1.6 mA in the LOW state (logic "0")

Input loading and output drive factors of all products described in this catalog are related to these definitions.

Examples — Input Load

1. A 9N00/7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan in of 1 load.)
2. The 93H72, which has a value of I_{IL} = 3.2 mA and I_{IH} of 80 μA on the CP terminal, is specified as having an input load factor of $\frac{3.2\text{ mA}}{1.6\text{ mA}}$ or 2 U.L.

Examples — Output Drive

1. The output of the 9N00/7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore $\frac{16\text{ mA}}{1.6\text{ mA}}$ = 10 U.L. and the output HIGH drive factor is $\frac{800\ \mu\text{A}}{40\ \mu\text{A}}$ = 20 U.L.

Relative load and drive factors for the basic TTL gate families specified in this catalog are given in Table 1.

Table I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9H00/74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
9L00	0.5 U.L.	0.25 U.L.	10 U.L.	2.5 U.L.
9N00/7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9S00/74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

DC Noise Margin

The loading rules defined above have been determined under test conditions chosen to insure useful worst case noise margin values over the full temperature and supply voltage ranges specified for the Fairchild TTL families.

Noise margin is defined in Figure 6 as the difference between the worst case output logic voltage and the worst case input voltage which guarantees the desired output level.

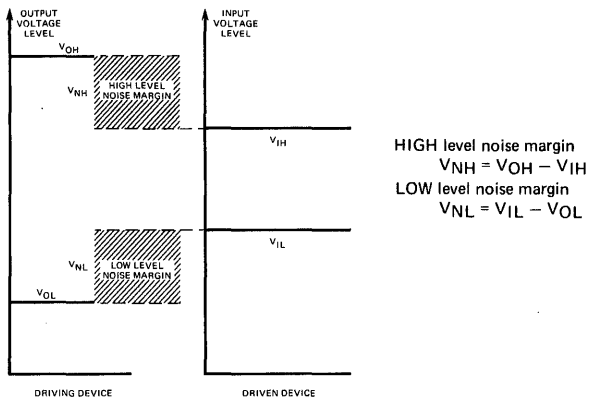

FIGURE 6

Table II below lists the worst case dc logic levels for Fairchild TTL devices.

Table II

PARAMETER	DEFINITION	9300 9N/54, 74 9H/54H, 74H	93L00 9L00	93S00 9S/74S	9S/54S
V_{OH}	Minimum Output Voltage in the HIGH State	2.4 V	2.4 V	2.5 V	2.7 V
V_{OL}	Maximum Output Voltage in the LOW State	0.4 V	0.3 V	0.5 V	0.5 V
V_{IH}	Minimum Voltage Level Which is Guaranteed to be Interpreted as a HIGH at the Input	2.0 V	2.0 V	2.0 V	2.0 V
V_{IL}	Maximum Voltage Level Which is Guaranteed to be Interpreted as a LOW at the Input	0.8 V	0.7 V	0.8 V	0.8 V

Example

1. The worst case guaranteed dc noise margin for a 9300 MSI interfacing with another 9300 MSI is therefore:

$$V_{NH} = 2.4 - 2.0 = 400 \text{ mV}$$
$$V_{NL} = 0.8 - 0.4 = 400 \text{ mV}$$

2. The worst case guaranteed noise margin for a 74S00 gate driving a 7400 gate is therefore:

$$V_{NH} = 2.7 - 2.0 = 700 \text{ mV}$$
$$V_{NL} = 0.8 - 0.5 = 300 \text{ mV}$$

Wired-OR Applications

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull up resistor.

The value of the pull up resistor is determined by considering the fan out of the OR tie and the number of devices in the OR tie. The pull up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan out is not exceeded when only one output is LOW).

Minimum and Maximum Pull Up Values

$$R_X \text{ (Min.)} = \frac{V_{CC} \text{ (max.)} - V_{OL}}{I_{OL} - N_2 I_{IL}}$$

$$R_X \text{ (Max.)} = \frac{V_{CC} \text{ (min.)} - V_{OH}}{N_1 I_{CEX} + N_2 I_{IH}}$$

Where

R_X = External Pull Up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads Being Driven
$I_{CEX}(I_{OH})$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan Out Current of Driving Element
I_{IH} = Input HIGH U.L. (40 μA)
I_{IL} = Input LOW U.L. (1.6 mA)
V_{OL} = Output LOW Voltage Level (0.4 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 9N01/7401 gates driving four other gate or MSI inputs.

$N_1 = 4$
$N_2 = 4$ (U.L.)
$I_{CEX} = 250\ \mu A$
$I_{OL} = 16$ mA
$I_{IH} = 40\ \mu A$
$I_{IL} = 1.6$ mA
$V_{OL} = 0.4$ V
$V_{OH} = 2.4$ V

$$R_X \text{ (min.)} = \frac{5.25 \text{ V} - 0.4 \text{ V}}{16 \text{ mA} - 4(1.6 \text{ mA})} = \frac{4.85 \text{ V}}{9.6 \text{ mA}}$$

$$R_X \geqslant 505\ \Omega$$

$$R_X \text{ (max.)} = \frac{4.75 \text{ V} - 2.4 \text{ V}}{4(0.250 \text{ MA}) + (0.04 \text{ mA})} = \frac{2.35 \text{ V}}{1.16 \text{ mA}}$$

$$R_X \leqslant 2.03\ \text{k}\Omega$$

Unused Inputs

To minimize noise sensitivity and optimize switching times, unused inputs of all TTL circuits should be held between 2.4 V and the absolute maximum 5.5 V. This eliminates the effect of the distributed capacitance associated with the floating input, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to a used input if maximum HIGH level fan out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a HIGH level voltage but adds no loading at a LOW level voltage. The HIGH level fan out for all circuits has been specified at double the LOW level fan out specifically to provide for this method of treating unused inputs.
2. Connect unused inputs to V_{CC} through a 1 kΩ resistor. If a transient exceeding the 5.5 V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1 kΩ resistor.
3. Tie the inputs to the output of an unused gate in the system. The gate must provide a constant HIGH level output.
4. Connect unused inputs to an independent supply voltage in the range of 2.4 V to 3.5 V.