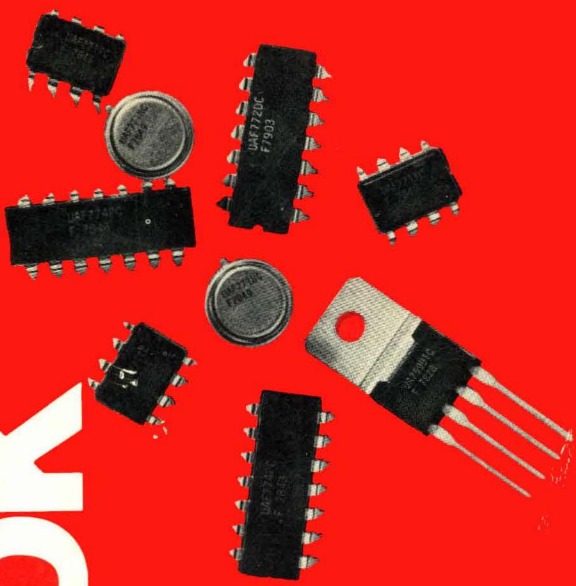
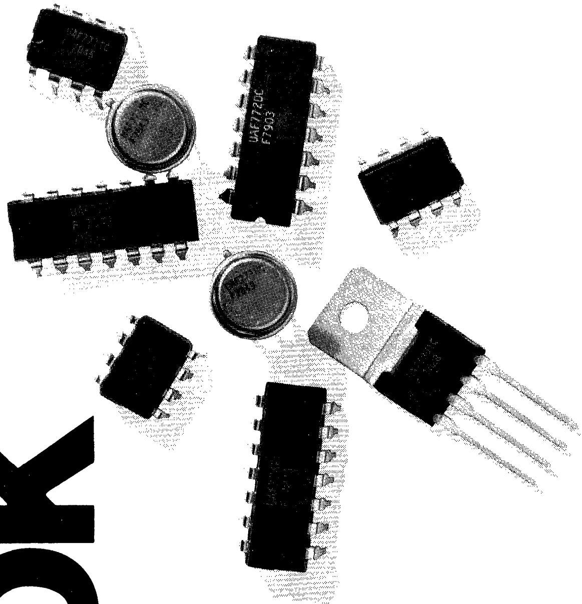
$5.00

LINEAR OP AMP DATA BOOK



FAIRCHILD

LINEAR OP AMP DATA BOOK



FAIRCHILD

INTRODUCTION

The increase in complexity and diversity of Linear Integrated Circuits over the last few years has necessitated a change in format in the Fairchild Linear data books. In this data book we have included our complete line of operational amplifiers and comparators, together with other selected special purpose circuits of primary interest to the industrial market. Other Fairchild Linear data books will cover voltage regulators, consumer, and interface devices.

Fairchild continues to be a pioneer in Linear operational amplifiers. The μA709, μA741, and μA747 are still industry standards a decade after their introduction by Fairchild. These have been followed by many single, dual, and quad devices intended to meet the increasing needs of our customers.

Today Fairchild's state-of-the-art technology is providing devices like the μA714, precision op amp; the μAF771/2/4, the industry's first set of single, dual, and quad BIFET op amps; the μA759 and μA791 power op amps; and the μA7391 and μA7392, precision DC motor speed control circuits.

This data book presents complete technical data on Fairchild's line of industrial linear integrated circuits. To expedite the designer's search for the right devices to meet various system requirements, several helpful aids are provided—selection guides by function, an LIC cross reference identifying competitive devices with their Fairchild direct replacements or nearest equivalents, and a package cross reference for determining equivalent packaging within the industry. For the Hi Rel customer, descriptions of Fairchild's Hi Rel processing and Matrix VI are given in a separate section.

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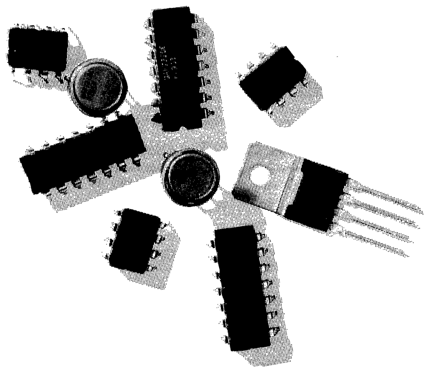

ALPHA-NUMERIC INDEX OF DEVICES

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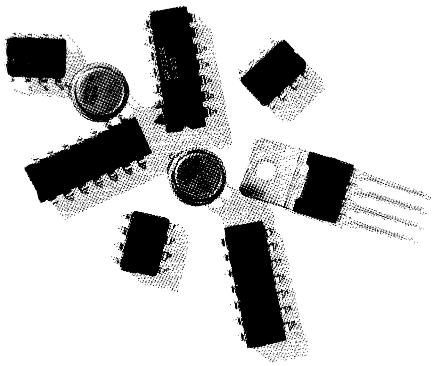


SELECTION GUIDES

VOLTAGE COMPARATOR SELECTION GUIDE

Device No.	Description	Input Bias Current µA (Max) 25 C	Input Offset Current (Max) 25°C	Input Offset Voltage mV - (Max) 25°C	Voltage Gain (Typ)	Supply Voltage V (Typ)	Response Time ns (Typ)	DTL/TTL Fanout	Temperature Range	Package(s)
µAF111	Fet-Input Voltage Comparator	0 05	0.000025	4 0	200K	+36	200	2	M	5S, 6A
µAF311	Fet-Input Voltage Comparator	0 15	0 000075	10	200K	+36	200	2	C	5S, 6A
µA111	Voltage Comparator Strobed Inputs, Single Supply, Low I_B	0 1	0 04	0.7	200K	±15	200	5	M	5S
µA311	Voltage Comparator Strobed Inputs, Single Supply, Low I_B	0 25	0 06	2.0	200K	±15	200	5	C	5S
µA139	Quad Comparator Single Supply, CMRR incl. gnd	0 1	0 025	5.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	M	6A
µA139A	Quad Comparator Single Supply, CMRR incl. gnd	0 1	0 025	2 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	M	6A
µA239	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	5.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
µA239A	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	2 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
µA339	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	5.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A
µA339A	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	2 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A
µA710/C	High Speed Differential Voltage Comparator	20 25	3 0 5 0	2 0/5.0	1 75K	+12, -6	40	1	M, C	5S, 3F, 6A, 9A
µA711/C	Dual High Speed Differential Comparator	75 100	10 15	3 5/5.0	1.5K	+12, -6	40	1	M, C	3F, 5F, 6A, 9A
µA734	Precision Comparator Low Drift -3.5 µV/°C	0 15	0 025 0 05	5 0 3 0	25K	±5 to ±15	200	2	M, C	5N, 6A
µA760	High Speed Differential Comparator	60	7 5	6 0	5K	±4.5 to ±6.5	25	2	M, C	5S, 6A
µA2901	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	7 0	200K	±1 to µ18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
µA3302	Quad Comparator Single Supply, CMRR incl. gnd	0 5	0 1	20 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A

TIMERS

Device Number	Function	Time Delay Hours	Free Running Frequency (kHz)	Output Compatibility	Output Current (mA)	Supply Voltage V (Max)	Timing Error %	Package(s)
μA555	Single Timer	1.0	100	TTL	200	+18	1.0	5S, 6T, 9T, 6A
μA556	Dual Timer	1.0	100	TTL	200	+18	1.0	6A, 9A
μA2240	Programmable Timer-Counter	120	—	TTL	5.0	+18	0.5	7B, 9B

OPERATIONAL AMPLIFIERS SELECTION GUIDE

OPERATIONAL AMPLIFIERS—COMMERCIAL (0°C TO +70°C)[1]

Item	DEVICE NO.	Description	Input Offset Voltage mV (Max)	Input Offset Voltage Drift μV/°C (Max)	Input Offset Current nA (Max)	Input Bias Current nA (Max)
1	μA1458C	High Performance Dual Op Amp	6.0	—	200	500
2	μA301A	General Purpose Op Amp	7.5	30	50	250
3	μA302	Voltage Follower	15	—	—	30
4	μA307	General Purpose Op Amp	7.5	30	50	250
5	μA308	Super Beta Op Amp	7.5	30	1.0	7.0
6	μA308A	Super Beta Op Amp	0.5	5.0	1.0	7.0
7	μA310	Voltage Follower	7.5	—	—	7.0
8	μA318	High Speed Op Amp	10	—	200	500
9	μA324	Quad Op Amp	7.0	—	50	250
10	μA3401	Quad Single Supply Amp	—	—	—	300
11	μA3403	Quad Op Amp	8.0	—	50	-500
12	μA348	Quad Op Amp	6.0	—	50	200
13	μA349	Quad Op Amp (Compensated for $A_V \geq 5$)	6.0	—	50	200
14	μAF355	FET Input Op Amp	10	—	0.05	0.2
15	μAF356	FET Input Op Amp	10	—	0.05	0.2
16	μA4136	Quad Op Amp	6.0	—	200	500
17	μA4558	Dual Op Amp	6.0	—	200	500
18	μA702C	Wide Band dc Amp	5.0	20	2000	7500
19	μA709C	High Performance Op Amp	7.5	—	500	1500
20	μA714C	High Performance Op Amp	0.15	1.8	6.0	7.0
21	μA714E	High Performance Op Amp	0.075	1.3	3.8	4.0
22	μA714L	High Performance Op Amp	0.25	3.0	20	30
23	μA715C	High Speed Op Amp	7.5	—	250	1500

1. Military, automotive and industrial range devices are available.

Common Mode Range V (Min)	Differential Input Voltage V (Max)	Voltage Gain V/V (Min)	Bandwidth $A_V = 1$ MHz (Typ)	Output Current mA (Max)	Slew Rate $A_V = 1$ V/μs (Typ)	Supply Voltage Min V (Typ)	Supply Voltage Max V (Typ)	Supply Current mA (Max)	Compensation Components
±11	±30	20K	1.0	5.5	0.8	±5	±18	2.9	0
±12	±30	25K	1.0	5.0	0.5	±3	±18	3.0	1
±10	—	0.9985	10	1.0	10	±12	±18	5.5	0
±12	±30	25K	1.0	5.0	0.5	±3	±18	3.0	0
±13.5	±1	25K	1.0	1.3	0.3	±5	±18	0.8	1
±13.5	±1	80K	1.0	1.3	0.3	±2	±20	0.8	1
±10	—	0.999	20	1.0	30	±5	±18	5.5	0
±11.5	±15	25K	15	6.0	50	±5	±18	10	0
+13.5, $-V_S$	±32	25K	1.0	13	0.5	+3	+32	2.0	0
—	—	1K	5.0	10	0.6	+5	±9	10	0
+13, $-V_S$	±30	20K	1.0	5.0	0.6	+5	+18	7.0	0
±12	±36	25K	1.0	5.0	0.5	±5	±18	4.5	0
±12	±36	25K	4.0	5.0	2.0	±5	±18	4.5	0
±10	±30	50K	2.5	—	5.0	±5	±18	4.0	0
±10	±30	50K	5.0	—	12	±5	±18	10	0
±12	±30	20K	3.0	5.0	1.0	±5	±18	10	0
±12	±30	20K	3.0	5.0	1.0	±5	±18	5.0	0
-4, +0.5	±5	2K	20	.35	3.5	+6, -3	+14, -7	6.7	2
±8	±5	15K	1.0	5.0	0.3	±9	±18	2.9	0
±13	±30	120K	0.6	5.5	0.17	±3	±22	5.0	0
±13	±30	200K	0.6	10.5	0.17	±3	±22	4.0	0
±13	±30	100K	0.6	5.5	0.17	±3	±18	6.0	0
±10	±15	10K	65	5.0	100	±6	±18	10	3

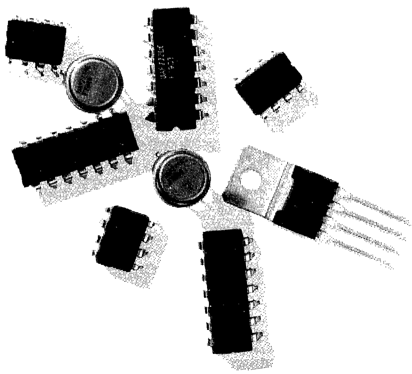
OPERATIONAL AMPLIFIERS SELECTION GUIDE

OPERATIONAL AMPLIFIERS—COMMERCIAL (0°C TO +70° C)[1]

Item	DEVICE NO.	Description	Input Offset Voltage mV (Max)	Input Offset Voltage Drift μV/°C (Max)	Input Offset Current nA (Max)	Input Bias Current nA (Max)
24	μA725C	Instrumentation Op Amp	2.5	—	35	125
25	μA725E	Instrumentation Op Amp	0.5	2.0	5.0	75
26	μA727C	Temperature Controlled Differential Amp	10	1.5	25	75
27	μA730C	Differential Amp	5.0	—	3.0	16
28	μA740E	FET Input Op Amp	100	—	0.3	2.0
29	μA741C	General Purpose Op Amp	6.0	—	200	500
30	μA741E	General Purpose Op Amp	3.0	15	30	80
31	μA747C	Dual General Purpose Op Amp	6.0	—	200	500
32	μA747E	Dual General Purpose Op Amp	3.0	15	30	80
33	μA748C	High Performance Op Amp	6.0	—	200	500
34	μA759	Power Op Amp	6.0	—	50	500
35	μAF771/2/4A	BIFET Op Amp	2.0	—	.05	.10
36	μAF771/2/4B	BIFET Op Amp	5.0	—	.05	.10
37	μAF771/2/4	BIFET Op Amp	10.0	—	.10	.20
38	μAF771/2/4L	BIFET Op Amp	15.0	—	.10	.20
39	μA776C	Multi-Purpose Programmable Op Amp (I_{SET} = 15 μA)	6.0	—	25	50
40	μA776C	Multi-Purpose Programmable Op Amp (I_{SET} = 1.5 μA)	6.0	—	6.0	10
41	μA777C	Precision Op Amp	5.0	—	20	100
42	μA791C	Power Op Amp	6.0	—	200	500
43	μA798C	Dual Op Amp	6.0	—	50	250

1. Military, automotive and industrial range devices are available.

Common Mode Range V (Min)	Differential Input Voltage V (Max)	Voltage Gain V/V (Min)	Bandwidth $A_V = 1$ MHz (Typ)	Output Current mA (Max)	Slew Rate $A_V = 1$ V/µs (Typ)	Supply Voltage Min V (Typ)	Supply Voltage Max V (Typ)	Supply Current mA (Max)	Compensation Components
±13.5	±22	250K	1.0	5.0	.01	±3	±22	3.0	4
±13.5	±22	1000K	1.0	5.0	.01	±3	±22	3.0	4
±12	±15	0.06K	1.0	0.001	—	±9	±18	5.7	2
±3.5	±5	0.1K	1.5	—	—	+6	+14	13	0
±10	±30	25K	1.0	5.0	6.0	±5	±22	8.0	0
±12	±30	20K	1.0	5.0	0.5	±5	±18	2.8	0
±12	±30	50K	1.5	5.0	0.7	±5	±22	3.75	0
±12	±30	25K	1.0	5.0	0.5	±5	±18	5.6	0
±15	30	50K	1.5	5.0	0.7	±5	±18	4.25	0
±12	±30	20K	1.0	5.0	0.5	±5	±18	2.8	1
+13, $-V_S$	±30	25K	1.0	200	0.5	±5	±18	—	0
±11	±30	50K	3.0	5.0	13.0	—	±18	—	0
±11	±30	50K	3.0	5.0	13.0	—	±18	—	0
±11	±30	50K	3.0	5.0	13.0	—	±18	—	0
±11	±30	50K	3.0	5.0	13.0	—	±18	—	0
±10	±30	50K	1.0	2.0	0.8	±1.2	±18	0.19	1
±10	±30	50K	0.2	0.16	0.1	±1.2	±18	0.03	1
±12	±30	25K	1.0	5.0	0.5	±5	±22	2.8	1
±12	±30	20K	1.0	1000	0.5	±5	±18	25	4
+13, $-V_S$	±30	20K	1.0	6.0	0.6	+5	+36	4.0	0



LINEAR INDUSTRY CROSS REFERENCE

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
1458CE	μA1458CHC	
1458CP	μA1458CTC	
1458E	μA1458HC	
1458P	μA1458TC	
1558E	μA1558HM	
3207A		9645
3245	9645/3245	
527		μA760HM
532		μA798TC
536		μA740AHM
556CJ	μA556PC	
709AE	μA709AHM	
709AH	μA709AFM	
709AL	μA709ADM	
709BE	μA709HM	
709BH	μA709FM	
709BL	μA709DM	
709CE	μA709HC	
709CJ	μA709PC	
709CL	μA709DC	
710BE	μA710HM	
710BH	μA710FM	
710BL	μA710DM	
710CE	μA710HC	
710CL	μA710DC	
711BE	μA711HM	
711BH	μA711FM	
711BL	μA711DM	
711CE	μA711HC	
711CJ	μA711PC	
711CL	μA711DC	
723BE	μA723HM	
723BL	μA723DM	
723CE	μA723HC	
723CJ	μA723PC	
723CL	μA723DC	
733DC	μA733DC	
733DM	μA733DM	
733FM	μA733FM	
733HC	μA733HC	
733HM	μA733HM	
741BE	μA741HM	
741BH	μA741FM	
741BL	μA741DM	
741CE	μA741HC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
741CJ	μA741PC	
741CP	μA741TC	
747BE	μA747HM	
747BL	μA747DM	
747CE	μA747HC	
747CJ	μA747PC	
747CL	μA747DC	
748BE	μA748HM	
748BH	μA748FM	
748BL	μA748DM	
748CE	μA748HC	
748CL	μA748DC	
748CP	μA748TC	
75S107		75107APC
75S108		75108APC
75S207		75207PC
75S208		75208PC
75322	9643DC	
75361	9644DC	
75361A		9643DC
75363	9643DC	
75450N	75450APC	
78M05BE	μA78M05HM	
78M05CE	μA78M05HC	
78M06BE	μA78M06HM	
78M06CE	μA78M06HC	
78M08BE	μA78M08HM	
78M08CE	μA78M08HC	
78M12BE	μA78M12HM	
78M12CE	μA78M12HC	
78M15BE	μA78M15HM	
78M15CE	μA78M15HC	
78M20BE	μA78M20HM	
78M20CE	μA78M20HC	
78M24BE	μA78M24HM	
78M24CE	μA78M24HC	
8216	μA8T26A	
8T26A	μA8T26APC	
8T26A	μA8T26ADC	
8T28	μA8T28	
AN217		μA721PC
AM26LS29		9634
AM26LS30		9636A
AM26S10	9640	
AM26S11	9641	
AN559	μA0802	

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA1190	TDA1190Z	
CA1310	μA1310	
CA3004T		μA703HC
CA3005T		μA703HC
CA3006T		μA703HC
CA3008		μA741FM
CA3008A		μA741FM
CA3010		μA741HM
CA3010A		μA741HM
CA3011T		μA753TC
CA3012T		μA753TC
CA3013T		μA753TC
CA3014T		μA753TC
CA3015		μA741HM
CA3015A		μA741HM
CA3016		μA741FM
CA3016		μA741FM
CA3018	μA3018HM	
CA3018A	μA3018HM	
CA3019	μA3019HM	
CA3021T		μA757DC
CA3022T		μA757DC
CA3023T		μA757DC
CA3026	μA3026HM	
CA3028AT		μA703HC
CA3028T		μA703HC
CA3029		μA741TC
CA3029A		μA741TC
CA3030		μA741TC
CA3030A		μA741TC
CA3036	μA3036HM	
CA3037		μA741DM
CA3037A		μA741DM
CA3038		μA741DM
CA3038A		μA741DM
CA3039	μA3039HM	
CA3041E		μA3065PC
CA3024E		μA3065PC
CA3043		μA3065PC
CA3044T		μA3064
CA3045	μA3045DM	
CA3046	μA3046DC	
CA3045	μA3054DC	
CA3058E		μA742DC
CA3059		μA742DC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3064E	μA3064PC	
CA3064T	μA3064HC	
CA3065E	μA3065PC	
CA3070E	μA780PC	
CA3071E	μA781PC	
CA3072E	μA746PC	
CA3075E	μA3075PC	
CA3078AS		μA776DM
CA3078AT		μA776HM
CA3078S		μA776TC
CA3078T		μA776HC
CA3079		μA742DC
CA3085		μA723HC
CA3085A		μA723HC
CA3085AF		μA723DC
CA3085AS		μA723DC
CA3085B		μA723HM
CA3085BF		μA723DM
CA3085BS		μA723DC
CA3085F		μA723DC
CA3085S		μA723DC
CA3086	μA3086DC	
CA3088E		μA720PC
CA3089E	μA3089PC	
CA3090E		μA758PC
CA3123E	μA720PC	
CA3126Q	μA787PC	
CA3134		TDA1190
CA3458S	1458TC	
CA3458T	1458HC	
CA3558S		μA1558HM
CA3558T	1558HM	
CA3741CS	μA741TC	
CA3741CT	μA741HC	
CA3741S		μA741HM
CA3741T	μA741HM	
CA3747CE	μA747PC	
CA3747CF		μA747DC
CA3747CT	μA747HC	
CA3747E	μA747DM	
CA3747F	μA747DM	
CA3747T	μA747HM	
CA3748CS	μA748TC	
CA3748CT	μA748HC	

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3748S		μA748HM
CA3748T	μA748HC	
CA758E	μA758PC	
DAC-08	μA0801	
DAC-08A	μA0801A	
DAC-08C	μA0801C	
DAC-08E	μA0801E	
DS0026	9646/0026	
DS3486		9637A
DS3487		9634
DS3645	9645/3245	
DS3691		9636A
DS3692		9634
DS8834		μA8T26A
DS8835		μA8T26A
DS78LS120		9637A
DS8T26A	μA8T26A	
HA1156	μA1310	
HA11226		μA7300
LA1201		μA721PC
LAS1405	μA78H05KC	
LAS1412	μA78H12KC	
LAS1415	μA78H15KC	
LF111H	μAF111HM	
LF155AH	μAF155AHM	
LF155H	μAF155HM	
LF156AH	μAF156AHM	
LF156H	μAF156HM	
LF157AH	μAF157AHM	
LF157H	μAF157HM	
LF211H	μAF211HM	
LF311H	μAF311HC	
LF347	μAF774	
LF347A	μAF774A	
LF347B	μAF774B	
LF351	μAF771	
LF351A	μAF771A	
LF351B	μAF771B	
LF13741	μAF771L	
LF353	μAF772	
LF353A	μAF772A	
LF353B	μAF772B	
LF355H	μAF355HC	
LF356H	μAF356HC	
LH0002	SH0002	
LH0021CK		μA791KC
LH0021K		μA791KM
LH0021K/883		μA791KMQB
LH0041		μA759HM
LH0061C		μA791KC
LH0061CK		μA791KM
LH0061K		μA791KM
LH101H		μA741HM
LH201H		μA741HM
LH2101AD		μA747ADM
LH740AH		μA740AHM
LM101AD	μA101ADM	
LM101AF	μA101AFM	
LM101AH	μA101AHM	
LM101D	μA101DM	
LM101H	μA101HM	
LM101J	μA101DM	
LM1011		μA7300
LM102H	μA102HM	
LM104H	μA104HM	
LM105H	μA105HM	
LM106F		μA710FM
LM106H		μA710HM
LM107H	μA107HM	
LM108AD	μA108ADM	
LM108AF	μA108AFM	
LM108AH	μA108AHM	
LM108D	μA108DM	
LM108F	μA108FM	
LM108H	μA108HM	
LM109K	μA109KM	
LM110H	μA110HM	
LM111H	μA111HM	
LM114A		μA726
LM117		μA78GKM
LM120H-05		μA79M05HM
LM120H-12		μA79M12HM
LM120H-15		μA79M15HM
LM120K-05		μA7905KM
LM120K-12		μA7912KM
LM121H		μA727HM

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM124D	μA124DM	μA3503DM
LM1303N		μA749PC
LM1304N	μA732PC	
LM1307N	μA767PC	
LM1310	μA1310	
LM139	μA139DM	
LM139A	μA139ADM	
LM148	μA148DM	
LM149	μA149DM	
LM1414J		μA711DC
LM1458H	μA1458HC	
LM1458N	μA1458TC	
LM1488J	μA1488	9616DC
LM1489AJ	μA1489A	9617DC
LM1489J	μA1489	9617DC
LM1496H	μA796HC	
LM1496N	μA796PC	
LM1514J		μA711DM
LM1558H	μA1558HM	
LM160H	μA760HM	
LM1800N	μA758PC	
LM1820N	μA720PC	
LM1829N	μA787PC	
LM1841N	μA2136PC	
LM1850N		μA7390PC
LM198	μAF198	
LM210AF	μA201AFM	
LM201AD	μA201ADM	
LM201AH	μA201AHM	
LM201D	μA201DM	
LM201H	μA201HM	
LM202H	μA202HM	
LM204H	μA204HM	
LM205H	μA205HM	
LM206F		μA710FM
LM206H		μA710HC
LM207H	μA207HM	
LM208AD	μA208ADM	
LM208AF	μA208AFM	
LM208AH	μA208AHM	
LM208D	μA208DM	
LM208F	μA208FM	
LM208H	μA208HM	
LM209K	μA209KM	
LM220H-05		μA79M05HM

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM220H-12		μA79M12HM
LM220H-15		μA79M15HM
LM220K-05		μA7905KM
LM220K-12		μA7912KM
LM220K-15		μA7915KM
LM222N		μA555TC
LM224D	μA224DM	
LM248	μA248DC	
LM249	μA249DC	
LM2901N	μA2901PC	μA775PC
LM2902N	μA2902PC	
LM2904N		μA798TC
LM2905N		μA555TC
LM2907N		μA4151TC
LM2917N		μA7151PC
LM301AD	μA301ADC	
LM301AH	μA301AHC	
LM301AN	μA301ATC	
LM3018AH	μA3018HM	
LM3018H	μA3018HM	
LM3019H	μA3019HM	
LM302H	μA302HC	
LM3026H	μA3026HM	
LM3039H	μA3039HM	
LM304H	μA304HC	
LM3045D	μA3045DM	
LM3046N	μA3046DC	
LM305AH	μA305AHC	
LM305H	μA305HC	
LM3053N	μA753TC	
LM3054N	μA3054DC	
LM306H		μA710HC
LM3064H	μA3064HC	
LM3065N	μA3065PC	
LM307H	μA307HC	
LM307N	μA307TC	
LM3070N	μA780PC	
LM3075N	μA3075PC	
LM308AD	μA308ADC	
LM308AH	μA308AHC	
LM308D	μA308DC	
LM308H	μA308HC	
LM308N	μA308TC	
LM3086N	μA3086DC	
LM309K	μA309KC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM311H	μA311HC	
LM311N	μA311TC	
LM320H-05		μA79M05HC
LM320H-12		μA79M12HC
LM320H-15		μA79M15HC
LM320K-05		μA7905KC
LM320K-12		μA7912KC
LM320K-15		μA7915KC
LM320MP-12		μA79M12AUC
LM320MP-15		μA79M15AUC
LM320MP-5.0		μA79M05AUC
LM320MP-6.0		μA79M06AUC
LM320MP-8.0		μA79M08AUC
LM320T-12		μA7912UC
LM320T-15		μA7915UC
LM320T-18		μA7918UC
LM320T-24		μA7924UC
LM320T-5		μA7905UC
LM320T-6		μA7906UC
LM320T-8		μA7908UC
LM323K	SH323KC	
LM323K	μA78H05KC	
LM324D	μA324DC	μA3403DC
LM324N	μA324PC	μA3403PC
LM339A	μA339ADC	
LM340K-05	μA7805KC	
LM340K-06	μA7806KC	
LM340K-08	μA7808KC	
LM340K-12	μA7812KC	
LM340K-15	μA7815KC	
LM340K-18	μA7818KC	
LM340K-24	μA7824KC	
LM340T-05	μA7805UC	
LM340T-06	μA7806UC	
LM340T-08	μA7808UC	
LM340T-12	μA7812UC	
LM340T-15	μA7815UC	
LM340T-18	μA7818UC	
LM340T-24	μA7824UC	
LM342P-12		μA78C12U1C
LM342P-15		μA78C15U1C
LM342P-18		μA78C18U1C
LM342P-24		μA78C24U1C
LM342P-5.0		
LM342P-6.0		
LM432P-8.0		μA78C08U1C
LM348	μA348DC	
LM349	μA349DC	
LM350N		75453BPC
LM351N	75453BPC	
LM358H	μA798HM	
LM360H	μA760HC	
LM376N	μA376TC	
LM380N		TBA820L
LM381AN		μA739DC
LM381N		μA739PC
LM382N		μA739PC
LM383	TDA2002	
LM386		μA7307
LM387N		μA739PC
LM388N		TBA820L
LM390	μAF398	
LM3905N		μA555TC
LM4250H		μA776HM
LM4250CH		μA776HC
LM4250CN		μA776DC
LM4250H		μA776HM
LM5108AJ	75108ADC	
LM55107AJ	55107ADM	
LM55108AJ	55108ADM	
LM55109J	55109DM	
LM55110J	55110A	
LM5524J	55S24	
LM5528J	5528DM	
LM5534J	55S234DM	
LM555CN	μA555TC	
LM556CN	μA556PC	
LM703LH	μA703HC	
LM709AH	μA709AHM	
LM709CH	μA709HC	
LM709CN	μA709PC	
LM709H	μA709HM	
LM710CH	μA710HC	
LM710CN	μA710PC	
LM710H	μA710HM	
LM711CH	μA711HC	
LM711CN	μA711PC	
LM711H	μA711HM	
LM723CD	μA723DC	
LM723CH	μA723HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM723CN	μA723PC	
LM723D	μA723DM	
LM723H	μA723HM	
LM725AH	μA725AHM	
LM725CH	μA725HC	
LM725H	μA725HM	
LM733CD	μA733DC	
LM733CH	μA733CH	
LM733CN	μA733PC	
LM733D	μA733DM	
LM733H	μA733HM	
LM741CD	μA741DC	
LM741CH	μA741HC	
LM741CN-08	μA741TC	
LM741CN-14	μA741PC	
LM741F	μA741FM	
LM741H	μA741HM	
LM746N	μA746PC	
LM747CD	μA747DC	
LM747CH	μA747HC	
LM747CN	μA747PC	
LM747D	μA747DM	
LM747H	μA747HM	
LM748CH	μA748HC	
LM748CN	μA748TC	
LM748H	μA748HM	
LM75107AJ	75107ADC	
LM75107AN	75107APC	
LM75108AN	75108APC	
LM75109J	75109DC	
LM75109N	75109PC	
LM75110J	75110A	
LM75110N	75110A	
LM75150J	75150DC	
LM75150N	75150PC	9616DC
LM75154J	75154DC	9617DC
LM75154N	75154PC	
LM75207J	75207DC	
LM75207N	75207PC	
LM75208J	75208DC	
LM75208N	75208PC	
LM7524J	75S24	
LM7524N	75S24	
LM7528J	7528DC	
LM7528N	7528PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM75325J	75325DC	
LM75325N	75325PC	
LM7534J	75S234DC	
LM7534N	75S234PC	
LM7535J	7535DC	
LM7535N	7535PC	
LM75450J	75450BDC	
LM75450N	75450BPC	
LM75451N	75451BTC	
LM75452N	75452BTC	
LM75453N	75453BTC	
LM75454N	75454BTC	
M51728		μA7392
MC1303P		μA749PC
MC1304P	μA732PC	
MC1305P		μA732PC
MC1306		μA7307
MC1307P	μA767PC	
MC1310P	μA1310PC	
MC1311P	μA758PC	
MC1312P	μA1312PC	
MC1324P		μA746PC
MC1326P		μA746PC
MC1327		TDA2522
MC1328P		μA746PC
MC1339P		μA749PC
MC1350P		μA757DC
MC1351P		μA3065PC
MC1352P		μA757DC
MC1353P		μA757DC
MC1355P		μA3065PC
MC1357P	μA2136PC	
MC1358P		μA3065PC
MC1364P	μA3064PC	
MC1370P	μA780PC	
MC1371P	μA781PC	
MC1375P	μA3075PC	
MC1391	μA1391TC	
MC1394P	μA1394TC	
MC1398P		μA787PC
MC1408L6	μA0802C	
MC1408L7	μA0802B	
MC1408L8	μA0802A	
MC1410G		μA733HC
MC1411	9665	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC1412	9666	
MC1413	9667	
MC1414L		μA711DC
MC1414P		μA711PC
MC1416	9668	
MC1420G		μA733HC
MC1435G		μA749DHC
MC1435L		μA749DC
MC1437L		μA749DC
MC1437P		μA749PC
MC1438R		μA791KC
MC14443		μA9708
MC14447		μA9708
MC1456CG		μA776HC
MC1456CL		μA776DC
MC1456G		μA776HC
MC1456L		μA776DC
MC1458CG	μA1458CHC	
MC1458CP1	μA1458CTC	
MC1458G	μA1458HC	
MC1458P1	μA1458TC	
MC1496G	μA796HC	
MC1496P	μA796PC	
MC1508L8	μA0802	
MC1510F		μA733FM
MC1510G		μA733HM
MC1514F		μA711FM
MC1514L		μA711DM
MC1520G		μA733HM
MC1535G		μA749HM
MC1535L		μA749DM
MC1537L		μA749DM
MC1550G		μA757DC
MC1556G		μA776HM
MC1556L		μA776DM
MC1558G	μA1558HM	
MC1560G		μA78M00HM
MC1560R		μA7800KM
MC1561G		μA78MGHM
MC1561R		μA78MGHM
MC1563G		μA79MGHM
MC1563R		μA79MGHM
MC1569G		μA78MGHM
MC1569R		μA78GKM
MC1590		μA757DC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC1596G	μA796HM	
MC1709CG	μA709HC	
MC1709CL	μA709DC	
MC1709CP1	μA709TC	
MC1709CP2	μA709PC	
MC1709F	μA709FM	
MC1709G	μA709HM	
MC1709L	μA709DM	
MC1710CG	μA710HC	
MC1710CL	μA710DC	
MC1710CP	μA710PC	
MC1710F	μA710FM	
MC1710G	μA710HM	
MC1710L	μA710DM	
MC1711CG	μA711HC	
MC1711CL	μA711DC	
MC1711CP	μA711PC	
MC1711F	μA711FM	
MC1711G	μA711HM	
MC1711L	μA711DM	
MC1712CG	μA702HC	
MC1712CL	μA702DC	
MC1712F	μA702FM	
MC1712L	μA702DM	
MC1723CG	μA723HC	
MC1723CL	μA723DC	
MC1723G	μA723HM	
MC1723L	μA723DM	
MC1741CG	μA741HC	
MC1741CG	μA747HC	
MC1741CL	μA741DC	
MC1741CP1	μA741TC	
MC1741CP2	μA741PC	
MC1741F	μA741FM	
MC1741G	μA741HM	
MC1741L	μA741DM	
MC1747CL	μA747DC	
MC1747G	μA747HM	
MC1747L	μA747DM	
MC1748CG	μA748HC	
MC1748CP1	μA748TC	
MC1748G	μA748HM	
MC1776CG	μA776HC	
MC1776G	μA776HM	
MC3245	9645/3345	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC3301P	μA3301PC	
MC3302P	μA3302PC	
MC3360		μA7307
MC3401P	μA3401PC	
MC3403L	μA3403DC	
MC3403P	μA3403PC	
MC3425		μA7390TC
MC3430		75107APC
MC3433		75108APC
MC3440		9642DC
MC3441		9642DC
MC3443		9642DC
MC3448A	μA3448A	
MC3456	μA556PC	
MC3476	μA776PC	
MC3486		9637A
MC3487		9634
MC3503L	μA3503DM	
MC75107L	75107ADC	
MC75107P	75107APC	
MC75108L	75108ADC	
MC75108P	75108APC	
MC75109L	75109DC	
MC75109P	75109PC	
MC75110L	75110ADC	
MC75110PC	75110APC	
MC75207L	75207DC	
MC75207P	75207PC	
MC75208L	75208DC	
MC75208P	75208PC	
MC7524L	75S24	
MC7524P	75S24	
MC7528L	7528DC	
MC7528P	7528PC	
MC75325L	75325DC	
MC75325P	75325PC	
MC7534L	755234DC	
MC7534P	755234DC	
MC75365		9645PC
MC75450L	75450BDC	
MC75450P	75450BPC	
MC75451P	75451BTC	
MC75452P	75452BTC	
MC75453P	75453BTC	
MC75454P	75454BTC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC75491P	75491PC	
MC75492P	75492PC	
MC7705CP		μA78M05UC
MC7706CP		μA78M06UC
MC7708CP		μA78M08UC
MC7712CP		μA78M12UC
MC7715CP		μA78M15UC
MC7718CP		μA7818UC
MC7720CP		μA78M20UC
MC7724CP		μA78M24UC
MC7805CK	μA7805KC	
MC7805CP	μA7805UC	
MC7806CK	μA7806KC	
MC7806CP	μA7806UC	
MC7808CK	μA7808KC	
MC7808CP	μA7808UC	
MC7812CK	μA7812KC	
MC7812CP	μA7812UC	
MC7815CK	μA7815KC	
MC7815CP	μA7812UC	
MC7818CK	μA7812KC	
MC7818CP	μA7812UC	
MC7824CK	μA7824KC	
MC7824CP	μA7824UC	
MC7905CK	μA7905KC	
MC7905CP	μA7905UC	
MC7906CK	μA7906KC	
MC7906CP	μA7906UC	
MC7908CK	μA7908KC	
MC7908CP	μA7908UC	
MC7912CK	μA7912KC	
MC7912CP	μA7912UC	
MC7915CK	μA7915KC	
MC7915CP	μA7915UC	
MC7918CK	μA7918KC	
MC7918CP	μA7918UC	
MC7924CK	μA7924KC	
MC7924CP	μA7924UC	
MC8T13L	μA8T13DM	
MC8T13P	μA8T13PC	
MC8T14L	μA8T14DM	
MC8T23P	μA8T23PC	
MC8T24P	μA8T24PC	
MC8T26A	μA8T26A	
MFC4060A		μA78MGT2C

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MFC4062A		µA78MGT2C
MFC4063A		µA78MGT2C
MFC4064A		µA78MGT2C
MFC6030A		µA78MGT2C
MFC6032A		µA78MGT2C
MFC6033A		µA78MGT2C
MFC6034A		µA78MGT2C
MFC8000		µA739PC
MFC8001		µA739PC
MFC8002		µA739PC
MFC8030		µA703HC
MFC8070		µA742DC
MLM101AG	µA101AHM	
MLM104G	µA104HM	
MLM105G	µA105HM	
MLM107G	µA107HM	
MLM109G		µA78M05HM
MLM109K		µA109KM
MLM110G	µA110HM	
MLM201AG	µA201AHM	
MLM204G	µA204HM	
MLM205G	µA205HM	
MLM207G	µA207HM	
MLM209G		µA78M05HM
MLM209K	µA209KM	µA7805KM
MLM210G	µA210HM	
MLM301AG	µA301AHC	
MLM301AP1	µA301ATC	
MLM304G	µA304HC	
MLM305G	µA305HC	
MLM307G	µA307HC	
MLM309G		µA78M05HC
MLM309K	µA309KC	
MLM310G	µA310HC	
MLM311G	µA311HC	
MLM311P1	µA311TC	
ML1408-6L	µA0802CDC	
ML1408-7L	µA0802BDC	
ML1408-8L	µA0802ADC	
ML1508-8L	µA0802DM	
MMH0026	9646/0026	
NE515A	µA733PC	
NE515K		µA733HC
NE521A		75107APC
NE521F		75107ADC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
NE522A		75108APC
NE522F		75108ADC
NE526A		µA760DC
NE526K		µA760HC
NE527K		µA760HC
NE529K		µA760HC
NE536T	µA740HC	µA740HC
NE545		µA7300
NE550A		µA723PC
NE550L		µA723HC
NE555V	µA555TC	
NE556A	µA556PC	
NE556F	µA556DC	
NE592A		µA733PC
NE645		µA7300
N10145	10145A	
N10149	10146	
N5071A	µA781PC	
N5072A	µA746PC	
N5558T	µA1458HC	
N5558V	µA1458TC	
N5570B	µA780PC	
N8T13B	**µA8T13PC**	
N8T13F	**µA8T13DC**	
N8T14B	**µA8T14PC**	
N8T14F	**µA8T14DC**	
N8T15F		9616DC
N8T16F		9627DC
N8T23B	**µA8T23PC**	
N8T23F	**µA8T23DC**	
N8T24B	**µA8T24PC**	
N8T24F	**µA8T24DC**	
N8T26A	µA8T26A	
OP-02		µA741AHM
OP-04		µA741AHM
OP-05		µA714HC
OP-07	µA714HC	
PA239A		µA739PC
RC1488D	µA1488	9616DC
RC1489AD	µA1489A	9617DC
RC1489D	µA1489	9617DC
RC4136D	µA4136DC/DM	
RC4136DB	µA4136PC	
RC4136DP	µA4136PC	
RC4151	µA4151	µA7151

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
RC4152		μA7151
RC4558DN	μA4558TC	
RC4558T	μA4558HC	
RC55109D	55109DM	
RC555DN	μA555TC	
RC556D	μA556DC	
RC556DP	μA556PC	
RC733TF	μA733HC	
RC75107AD	75107ADC	
RC75107AP	75107APC	
RC75108AD	75108ADC	
RC75108ADP	75108APC	
RC75109D	75109DC	
RC75109DP	75109PC	
RC75110D	75110ADC	
RC75150D	75150DC	
RC75154M	75154DC	
RC7524M	75S24DC	
RC7524MP	75S24PC	
RC7528M	7528DC	
RC7528MP	7528PC	
RC75325M	75325DC	
RC75325MP	75325PC	
RC8T13M	μA8T13DC	
RC8T13MP	μA8T13PC	
RC8T14M	μA8T14DC	
RC8T14MP	μA8T14PC	
RC8T23M	μA8T23DC	
RC8T23MP	μA8T23PC	
RC8T24M	μA8T24DC	
RC8T24MP	μA8T24PC	
RC9621D	9621DC	
RC9622D	9622DC	
RM4136D	μA4136DM	
RM55107AD	55107ADM	
RM55108AD	55108ADM	
RM55110D	55110DM	
RM5524M	5524DM	
RM5525M	5525DM	
RM55325M	55325DM	
RM555T	μA555HM	
RM556D	μA556DM	
RM733TF	μA733HM	
RM8T13M	μA8T13DM	
RM8T14M	μA8T14DM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SE515K		μA733HM
SE526A		μA760DM
SE526K		μA760HM
SE527K		μA760HM
SE529A		μA733DM
SE529K		μA760HM
SE536T		μA740HM
SE550L		μA723HM
SE592K		μA733HM
SH76008		TDAA2002
SH76018		TDA2002
SN2660JA		μA776DM
SN52L022L		μA798HM
SN52L044JA		μA3503DM
SN52309LA		μA78M05HM
SN52506J		μA711DM
SN52510L		μA710HM
SN52514J		μA711DM
SN52520J		μA710DM
SN52558L	μA1558HM	
SN52660L		μA776HM
SN52702J	μA702DM	
SN52702L	μA702HM	
SN52709J	μA709DM	
SN52709L	μA709HM	
SN52710J	μA710DM	
SN52710L	μA710HM	
SN52711J	μA711DM	
SN52711L	μA711HM	
SN52723J	μA723DM	
SN52723L	μA723HM	
SN52741J	μA741DM	
SN52741L	μA741HM	
SN52747J	μA747DM	
SN52747L	μA747HM	
SN52748J	μA748DM	
SN52748L	μA748HM	
SN52771J		μA776DM
SN52771L		μA776HM
SN52777J	μA777DM	
SN52777L	μA777HM	
SN52810J		μA710DM
SN52810L		μA710HM
SN52811J		μA711DM
SN52811L		μA711HM

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN52820J		μA711DM
SN529K		μA733HC
SN5510FA		μA833FM
SN5510L		μA733HM
SN55107AL	55107ADM	
SN55107BJ	55107BDM	
SN55108AJ	55108ADM	
SN551088J	55108BDM	
SN55109J	55109DM	
SN5511FA		μA733FM
SN5511L		μA733HM
SN55110J	55110ADM	
SN55112J	55112DM	
SN55114J	9614DM	
SN55114SB	9614FM	
SN55115J	9615DM	
SN55115SB	9615FM	
SN5512L		μA733HM
SN55121J	55121DM	
SN55122J	55122DM	
SN55123J	55123DM	
SN55124J	55124DM	
SN5514L		μA733HM
SN55207J	55207DM	
SN55208J	55208DM	
SN55234J	55S234DM	
SN5524J	55S24DM	
SN55325J	55325DM	
SN55325SB	55325FM	
SN55326SB	55326FM	
SN55327SB	55327FM	
SN55450BJ	55450BDM	
SN55450J	55450DM	
SN55451BL	55451BHM	
SN55451L	55451HM	
SN55452BL	55452BHM	
SN55452L	55452HM	
SN55453BL	55453BHM	
SN55453L	55453HM	
SN55454BL	55454BHM	
SN55454L	55454HM	
SN55460J	55460DM	
SN55461L	55461HM	
SN55462L	55462HM	
SN55463L	55463HM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN55464L	55464HM	
SN71710J	μA710DC	
SN72L022L		μA798HC
SN72L022P		μA798TC
SN72L044JA		μA3403DC
SN72L044N		μA3403PC
SN72301AN	μA301ADC	
SN72301L	μA301AHC	
SN72301P	μA301ATC	
SN72304L	μA104HM	
SN72305AL	μA305AHC	
SN72305L	μA305HC	
SN72307L	μA307HC	
SN72307P	μA307TC	
SN72308AL	μA308AHC	
SN72308AN	μA308ADC	
SN72308L	μA308HC	
SN72308N	μA308DC	
SN72309LA		μA78M05HC
SN72310L	μA310HC	
SN72311L	μA311HC	
SN72311P	μA311TC	
SN72376P	μA376TC	
SN72440J		μA742DC
SN72440N		μA742DC
SN72506J		μA711DC
SN72506N		μA711PC
SN72510J		μA710DC
SN72510L		μA710HC
SN72510N		μA710PC
SN72514J		μA711DC
SN72514N		μA711PC
SN72555P	μA555TC	
SN72556N	μA556PC	
SN72558L	μA1458HC	
SN72558P	μA1458TC	
SN72660JA		μA776DC
SN72660L		μA776HC
SN72660N		μA776DC
SN72660P		μA776TC
SN72702J	μA702DC	
SN72702L	μA702HC	
SN72709J	μA709DC	
SN72709L	μA709HC	
SN72709P	μA709TC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72710L	μA710HC	
SN72710N	μA710PC	
SN72711J	μA711DC	
SN72711L	μA711HC	
SN72711N	μA711PC	
SN72720J		μA710DC
SN72720N		μA710PC
SN72723J	μA723DC	
SN72723L	μA723HC	
SN72723N	μA723PC	
SN72733J	μA733DC	
SN72733L	μA733HC	
SN72733N	μA733PC	
SN72741J	μA741DC	
SN72741L	μA741HC	
SN72741N	μA741PC	
SN72741P	μA741TC	
SN72747J	μA747DC	
SN72747L	μA747HC	
SN72748J	μA748DC	
SN72748L	μA748HC	
SN72748N	μA748DC	
SN72748P	μA748TC	
SN72771J		μA776DC
SN72771L		μA776HC
SN72771N		μA776DC
SN72771P		μA776TC
SN72777J	μA777DC	
SN72777L	μA777HC	
SH72777N	μA777DC	
SN72777P	μA777TC	
SN72810J		μA710DC
SN72810L		μA710HC
SN72810N		μA710PC
SN72811J		μA711DC
SN72811L		μA711HC
SN72811N		μA711PC
SN72820J		μA711DC
SN72820N		μA711PC
SN7496	7496	
SN7497	7497	
SN7510L		μA733HC
SN75107AJ	75107ADC	
SN75107AN	75107APC	
SN75107BJ	75107BDC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN75107BN	75107BPC	
SN75108AJ	75108ADC	
SN75108AN	75108APC	
SN75108BJ	75108BDC	
SN75108BN	75108BPC	
SN75109J	75109DC	
SN75109N	75109PC	
SN7511L		μA733HC
SN7511N		μA733PC
SN75110AJ	75110ADC	
SN75110AJ	75110APC	
SN75110J	75110ADC	
SN75110N	75110APC	
SN75112J	75112DC	
SN75112N	75112PC	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115N	9615PC	
SN7512L		μA733HC
SN7512N		μA733PC
SN75121J	75121DC	
SN75121N	75121PC	
SN75122J	75122DC	
SN75122N	75122PC	
SN75123J	75123DC	
SN75123N	75123PC	
SN75124J	75124DC	
SN75124N	75124PC	
SN75124L		μA733HC
SN7514P		μA733PC
SN75150J	75150DC	9616DC
SN75150P	75150PC	9616DC
SN75152J	9627DC	
SN75154J	75154DC	9617DC
SN75182N		9615DC
SN75183N		9614DC
SN75188J	1488DC	
SN75189AJ	1489ADC	
SN75189J	1489DC	
SN7520	75S20	
SN75207J	75207DC	
SN75207N	75207PC	
SN75208J	75208DC	
SN75208N	75208PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN75224J	75S24DC	
SN75224N	75S24PC	
SN75225J	75225DC	
SN75225N	75225PC	
SN75232J	75232DC	
SN75232N	75232PC	
SN75234J	75S234DC	
SN75234N	75S234PC	
SN75235J	75235DC	
SN75235N	75235PC	
SN75238J	75238DC	
SN75238N	75238PC	
SN7524J	75S24DC	
SN7524N	75S24PC	
SN7528J	7528DC	
SN7528N	7528PC	
SN75325J	75325DC	
SN75325N	75325PC	
SN75326J	75326DC	
SN75236N	75326PC	
SN75327J	75327DC	
SN75327N	75327PC	
SN7534J	75S234DC	
SN7534N	75S234PC	
SN75450BJ	75450BDC	
SN75450BN	75450BPC	
SN75450N	75450BPC	
SN75451BL	75451BHC	
SN75451BP	75451BTC	
SN75451P	75451BTC	
SN75452BL	75452BHC	
SN75452BP	75452BTC	
SN75452P	75452BTC	
SN75453BL	75453BHC	
SN75453BP	75453BTC	
SN75453P	75453BTC	
SN75454BL	75454BHC	
SN75454P	75454BTC	
SN75460J	75460DC	
SN75460N	75460PC	
SN75461L	75461HM	
SN75461L	75462HM	
SN75461P	75461TC	
SN75463P	75463TC	
SN75464L	75464HM	
SN75464P	75464TC	
SN75471L	75471HC	
SN75471P	75471TC	
SN75472L	75472HC	
SN75472P	75472TC	
SN75473L	75473HC	
SN75473P	75473TC	
SN75474L	75474HC	
SN75474P	75474TC	
SN75491N	75491PC	
SN75492N	75492PC	
SN76001N	TBA641A12	
SN76005ND		μA706BPC
SN76024ND		μA706BPC
SN76104N	μA732PC	
SN76105N		μA732PC
SN76111N	μA767PC	
SN76115	μA1310	
SN76116N	μA758PC	
SN76131N	μA739PC	
SN76149N	μA749PC	
SN76227		TDA2522
SN76242N	μA780PC	
SN76243N	μA781PC	
SN76246N	μA746PC	
SN76298N		μA787PC
SN76545		TBA920
SN76565N	μA3064PC	
SN76591P	μA1391TC	
SN76594P	μA1394TC	
SN76600P		μA757PC
SN76635N	μA720PC	
SN76642N		μA2136PC
SN76650N		μA757PC
SN76666N	μA3065PC	
SN76669N	μA2136PC	
SN76675N	μA3075PC	
SN76678P	μA753TC	
SN76689N	μA3089PC	
SSS725AJ		μA725AHM
SSS725BJ		μA725EHM
SSS725EJ		μA725EHC
SSS741CJ		μA741EHC
SSS741J		μA741AHM
SSS747CK		μA747EHC

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SSS747CP		μA747EDC
SSS747K		μA747AHM
SSS747P		μA747ADM
SSS1408A-6	μA0802C	
SSS1408A-7	μA0802B	
SSS1408A-8	μA0802A	
SSS1508A-8	μA0802	
S5558T	μA1558HM	
S5596K	μA796H	
S8T13F	μA8T13DM	
S8T14F	μA8T14DM	
S8T15F		9616DM
S8T16F		9627DM
TA7157	μA1310	
TAA630S	TAA630S	TDA2522
TBA396		TDA2560
TBA510	TBA510	
TBA520	TBA520	TDA2522
TBA530	TBA530	TDA2530
TBA540	TBA540	
TBA560C	TBA560C	TDA2560
TBA570		μA721PC
TBA641A12	TBA641A12	
TBA641B11	TBA641B11	
TBA800	TBA800	
TBA810AS	TBA810AS	
TBA810DS	TBA810DS	
TBA810DAS	TBA810DAS	
TBA810S	TBA810S	
TBA920	TBA920	
TBA920S	TBA920S	
TBA970	TBA970	
TBA990	TBA990	TDA2522
TCA600		μA7392
TCA610		μA7392
TCA900		μA7392
TCA910		μA7392
TCA940		μA783P4C
TDA1170	TDA1170	
TDA1270	TDA1270	
TDA1037		TDA2002
TDA1190	TDA1190	
TDA1190Z	TDA1190Z	
TDA1327		TDA2522
TDA2002	TDA2002	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
TDA2002A	TDA2002A	
TDA2150		TDA2560
TDA2160		TDA2522
TDA2521	TDA2521	
TDA2522	TDA2522	
TDA2530	TDA2530	
TDA2560	TDA2560	
TDA2590	TDA2590	
TDA2610		TDA1190
TL071A	μAF771B	
TL071B	μAF771A	
TL071C	μAF771	
TL072A	μAF772B	
TL072B	μAF772A	
TL072C	μAF772	
TL074A	μAF774B	
TL074B	μAF774A	
TL074C	μAF774	
TL075	μAF774	
TL075A	μAF774B	
TL075B	μAF774A	
TL081A	μAF771B	
TL081B	μAF771A	
TL081C	μAF771L	
TL082A	μAF772B	
TL082B	μAF772A	
TL082C	μAF772L	
TL083	μAF772L	
TL083A	μAF772B	
TL084A	μAF772B	
TL084B	μAF772A	
TL084C	μAF774L	
TL810		μA710HM
TL811		μA711HM
ULN2001A	9665	
ULN2002A	9666	
ULN2003A	9667	
ULN2004A	9668	
ULN2111A		μA2136PC
ULN2113A		μA3065PC
ULN2114A	μA746PC	
ULN2114K	μA746HC	
ULN2120A	μA732PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
ULN2121A		μA767PC
ULN2122A		μA732PC
ULN2124A	μA780PC	
ULN2126A	μA739PC	
ULN2127A	μA781PC	
ULN2128A	μA767PC	
ULN2129A		μA3075PC
ULN2136A	μA2136PC	
ULN2137A	μA720PC	
ULN2165A	μA3065PC	
ULN2209M	μA753TC	
ULN2210A		μA758PC
ULN2224A		μA788PC
ULN2228A		μA788PC
ULN2244A	μA758PC	
ULN2298A		μA787PC
ULX2262A	μA787PC	
ULX2264A	μA3064PC	
ULX2267A	μA3067PC	
ULX2289A	μA3089PC	
YKB2219	μA1310	
μA709CA	μA709PC	
μA709CT	μA709HC	
μA709Q	μA709FM	
μA709T	μA709HM	
μA710CA	μA710HC	
μA710CT	μA710HC	
μA710Q	μA710FM	
μA710T	μA710HM	
μA711CA	μA711PC	
μA711CK	μA711HC	
μA711K	μA711HM	
μA723CA	μA723PC	
μA723CL	μA723HC	
μA723L	μA723HM	
μA733A	μA733DM	
μA733CK	μA733HC	
μA733C1	μA733DC	
μA733K	μA733HM	
μA7330A	μA733PC	
μA7331	μA733DM	
μA740CT	μA740HC	
μA741CA	μA741PC	
μA741CT	μA741HC	
μA741CV	μA741TC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA741T	μA741HM	
μA747CA	μA747PC	
μA747CK	μA747HC	
μA747K	μA747HM	
μA748CA	μA748DC	
μA748CT	μA748HC	
μA748CV	μA748TC	
μA748T	μA748HC	
μA78L02ACLP	μA78L26AWC	
μA78L05ACLP	μA78L05AWC	
μA78L06ACLP	μA78L62AWC	
μA78L08ACLP	μA78L08AWC	
μA78L12ACLP	μA78L12AWC	
μA78L15ACLP	μA78L15AWC	
μA78M05CKC	μA78M05UC	
μA78M05CLA	μA78M05CHC	
μA78M05MLA	μA78M05HM	
μA78M06CKC	μA78M06UC	
μA78M06CLA	μA78M06CHC	
μA78M06MLA	μA78M06HM	
μA78M08CKC	μA78M08UC	
μA78M08CLA	μA78M08CHC	
μA78M08MLA	μA78M08HM	
μA78M12CKC	μA78M12UC	
μA78M12CLA	μA78M12CHC	
μA78M12MLA	μA78M12HM	
μA78M15CKC	μA78M15UC	
μA78M15CLA	μA78M15CHC	
μA78M15MLA	μA78M15HM	
μA78M20CKC	μA78M20CUC	
μA78M20CLA	μA78M20CHC	
μA78M20MLA	μA78M20HM	
μA78M24CKC	μA78M24CUC	
μA78M24CLA	μA78M24CHC	
μA78M24MLA	μA78M24HM	
μA7805CKA	μA7805KC	
μA7805CKC	μA7805UC	
μA7805MKA	μA7805KM	
μA7806CKA	μA7806KC	
μA7806CKC	μA7806UC	
μA7806MKA	μA7806KM	
μA7808CKA	μA7808KC	
μA7808CKC	μA7808UC	
μA7808MKA	μA7808KM	
μA7812CKA	μA7812KC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA7812CKC	μA7812UC	
μA7812MKA	μA7812KM	
μA7815CKA	μA7815KC	
μA7815CKC	μA7815UC	
μA7815MKA	μA7815KM	
μA7818CKC	μA7818UC	
μA7818MKA	μA7818KM	
μA7824CKC	μA7824UC	
μA7824MKA	μA7824KM	
μA7885CKA	μA7885KC	
μA7885CKC	μA7885UC	
μA7885MKA	μA7885KM	
μA79M05CKC	μA79M05AUC	
μA79M05CLA	μA79M05AHC	
μA79M05MLA	μA79M05HM	
μA79M06CKC	μA79M06AUC	
μA79M06CLA	μA79M06AHC	
μA79M06MLA	μA79M06HM	
μA79M08CKC	μA79M08AUC	
μA79M08CLA	μA79M08AHC	
μA79M08MLA	μA79M08HM	
μA79M12CKC	μA79M12AUC	
μA79M12CLA	μA79M12AHC	
μA79M12MLA	μA79M12HM	
μA79M15CLA	μA79M15AHC	
μA79M15MLA	μA79M15HM	
μA79M20CKC	μA79M20AUC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA79M20CLA	μA79M20AHC	
μA79M20MLA	μA79M20HM	
μA79M24CKC	μA79M24AUC	
μA79M24CLA	μA79M24AHC	
μA79M24MLA	μA79M24HM	
μA7905CKA	μA7905KC	
μA7905CKC	μA7905UC	
μA7905MKA	μA7905KM	
μA7906CKA	μA7906KC	
μA7906CKC	μA7906UC	
μA7906MKA	μA7906KM	
μA7908CKA	μA7908KC	
μA7908CKC	μA7908UC	
μA7908MKA	μA7908KM	
μA7912CKA	μA7912KC	
μA7912CKC	μA7912UC	
μA7912MKA	μA7912KM	
μA7915CKA	μA7915KC	
μA7915CKC	μA7915UC	
μA7915MKA	μA7915KM	
μA7918CKA	μA7918KC	
μA7918CKC	μA7918UC	
μA7918MKA	μA7918KM	
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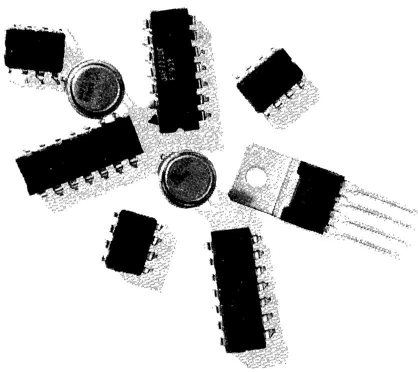
μA7924CKC	μA7924UC	
μA7924MKA	μA7924KM	



QUALITY, RELIABILITY AND HI REL PROCESSING

QUALITY, RELIABILITY AND HI REL PROCESSING

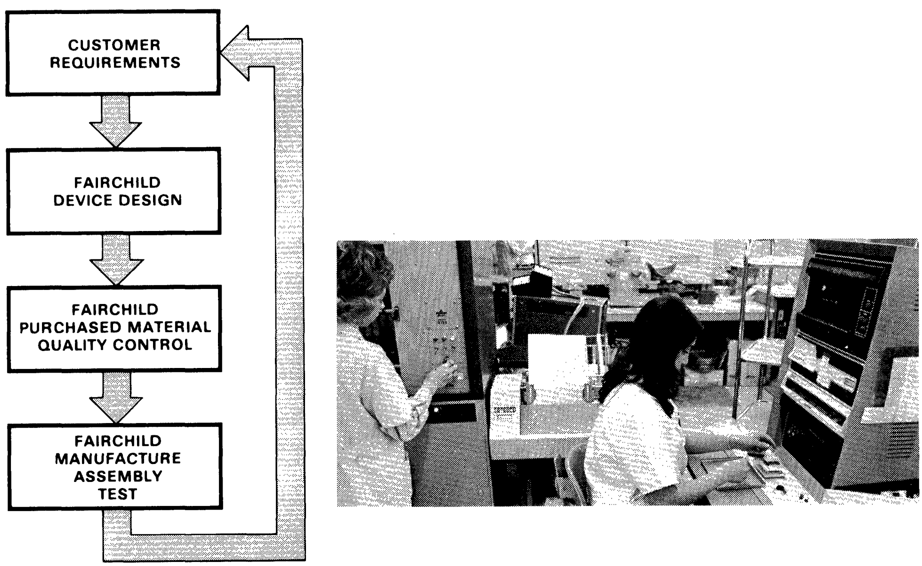
Introduction

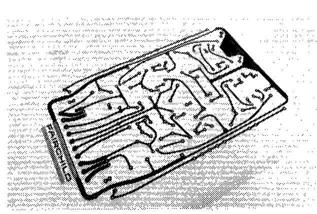
There are three basic ingredients in the manufacture of reliable Linear Circuits. First, the device must be designed with the user's applications and reliability requirements in mind. Secondly, the device must be manufactured with the optimum technology for the application. Thirdly, controls must be established to assure maintenance of the quality/reliability levels established in the design of the device. Consideration is given to the reliability influence of each part of the manufacturing and testing cycle with constant feedback from internal reliability monitoring; customer feedback on the results is a vital factor. The Fairchild reliability concept can be presented as constant feedback system which begins and ends with the customer *(Figure 4-1)*.

Areas of Consideration

Device Applications and Reliability

The reliability cycle begins with the customer. His device application, environment for its usage and end-product reliability requirements are major factors in establishing the quality/reliability levels. The customer is the final judge.





Customer Design Breadboard

Fig. 4-1 Customer Feedback System

Device Design

Inherent component reliability is a function of the product/process design. New Fairchild designs as well as modifications or extensions of existing designs with known performance and reliability characteristics are rigorously evaluated. Three different factors in the manufacture of an IC significantly affect its reliability.

The Silicon Chip — Fairchild's design-technology capability utilizes epitaxial layer to achieve the desired electrical parameter characteristics. The surface influences long-term gain and voltage/leakage stability. The metallization determines mechanical integrity and current distribution.

Chip Assembly — The process and materials used to assemble the chip and package must preserve the inherent reliability of the chip and be inherently reliable to withstand thermal, mechanical and electrical stresses.

The Package — The package must effectively transfer heat from the chip to the outside world and protect the chip during handling and use.

Incoming Quality Control (IQC)

All purchased materials for Fairchild Linear circuits are controlled through central specification control, product engineering, and reliability and quality assurance (R&QA) located in Mountain View. Materials are purchased and inspected per control documents using three IQC methods.

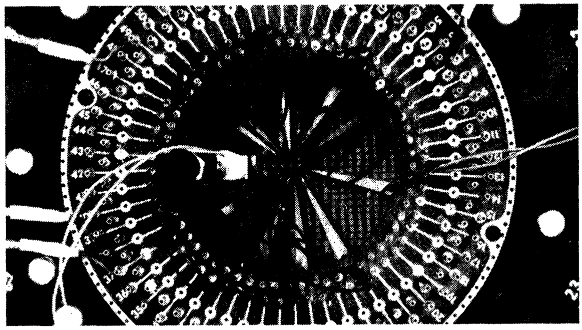
Direct visual and mechanical inspection
Functional testing
Composition analysis utilizing chemical and x-ray techniques from both internal and external sources.

In addition to centralized IQC, each manufacturing facility has a local, fully equipped IQC department. These facilities concentrate on cleanliness, plating quality and functionality. A computer file is made on each vendor's performance and quarterly reports are generated and analyzed.

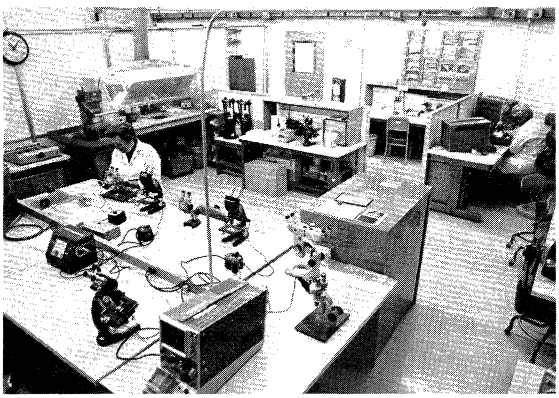
Wafer Manufacture

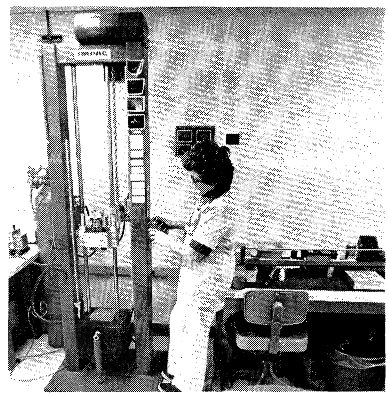
Wafers used to fabricate Fairchild Linear Circuits are made at Fairchild. This includes crystal pulling, slicing, polishing and epitaxial layer growth. Fairchild designs rely on accurate control of thickness and resistivity. All operations have laminar-flow clean-air hoods directly over the work areas. Wafer fabrication is essentially a series of masking and furnace cycles in which geometries are defined and impurities (dopants) introduced to form emitter, base and resistor regions. Daily controls are maintained on furnace temperatures to within $\pm 1°C$. Resistivities (ρ_S) of diffused layers are recorded on every run. Each masking step defines a new portion of the device geometry. A post develop inspection is performed to assure that each wafer has been properly exposed and chemically developed before final etching. When the masking and etching procedures are completed, a final inspection assures that the geometry is properly aligned, etched and cleaned. Following each production masking step, a sample inspection is performed by quality control inspectors to verify correct process implementation.

After masking and diffusion, the metallization process completes wafer manufacture. Fairchild uses electron-beam evaporation techniques to deposit gold and aluminum. Deposits are controlled through utilization of automated process sequencing,which includes an automatic thickness controller. Every run is gated through a first optical (1st opt.) inspection before it leaves the wafer fabrication area. Cleanliness, mask alignment, metal adherence (front and back) and general workmanship are inspected.

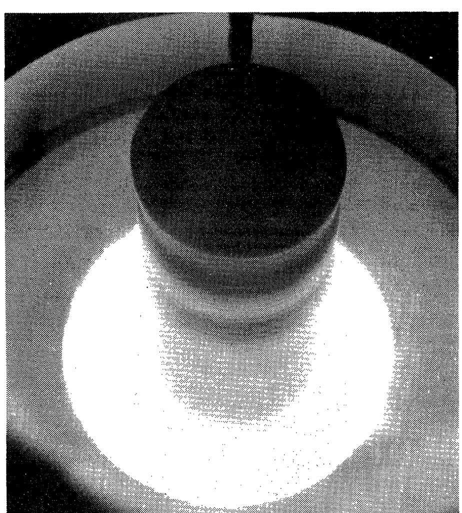


Wafer Probing





IQC Area



Crystal Puller

4

Wafer Testing
Before the wafers are scribed and broken into dice for assembly onto headers or shipment to a customer as probed dice, they are electrically sorted. Each wafer is automatically probed with multiple tests to duplicate or correlate the dice to the final product test requirements. Rejected dice are ink marked and later scrapped. A final quality control gate is performed before the probed wafers can be forwarded to assembly.

Device Assembly
After the wafers are scribed and broken, a second optical (2nd opt.) QC inspection is performed. The dice are inspected for wafer fabrication (handling) damage, as well as for defects which may cause assembly problems or result in latent reliability problems.

Monitors are performed on both assembly equipment and operators. Machines are shut down if defect control limits are exceeded and suspect material is rejected and 100% screened. Key items inspected are die orientation, voids under die, proper bond formation, wirepull strength and cleanliness.

A third optical (3rd opt.) gate is performed prior to final device sealing. If rejected, the lot is 100% screened by production and resubmitted to QC. Accepted lots are sent to the final seal operation, where the packages are monitored for weld strength and hermeticity (except plastic packages).

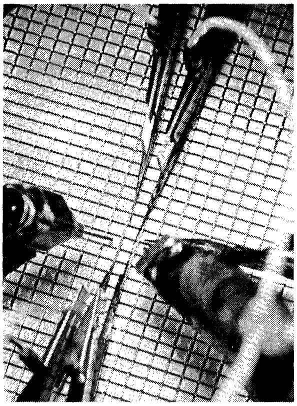
Device Testing
Before shipment, all devices are 100% production tested to the following minimum inspection levels.

Functional dc	0.25% AQL	
25° C dc	0.65% AQL	
25° C ac	1.5% AQL	
Temperature dc	1.5% AQL	
Mechanical/Visual	0.65% AQL	
Marking Performance	15/0 LTPD	
Fine Leak	1.0% AQL	Hermetic Devices Only.
Gross Leak	0.4% AQL	

Customers with special testing requirements are accommodated through an internal specification system. All internal test specifications formatted from customer documents are signed off by QA before they can be issued to the test area.

Device Application
The total reliability effort is completed full-cycle with the customer. Operation in the customer application is the final consideration in device reliability. How each device is handled during system assembly by the customer, heat-sunk (mounted) and cooled during operation, and the amount of overload stresses (due to the system malfunction or misuse) greatly impacts the device reliability. Thus, the customer's specification requirements, the manufacturer's device design, manufacture, test, the actual circuit into which the device is inserted and the equipment containing that circuit in the field all affect the device and reliability.

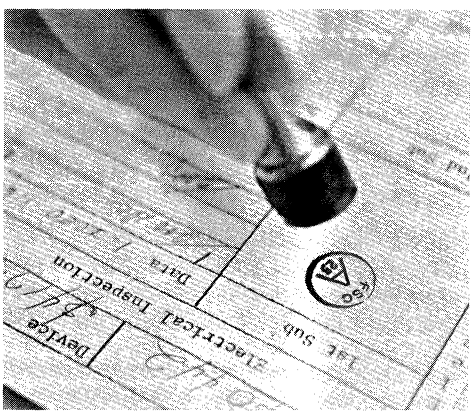
Failure Analysis
Failure analysis results performed by customers and by Fairchild on returned devices provide one of the most important inputs for consideration in Fairchild's total linear reliability concept. Failures generated by line monitors, life tests and field applications are analyzed to provide corrective action in terms of product design, assembly and testing methods. A scanning electron microscope (SEM) and an Auger electron microscope for chemical analysis are available for inspection of materials.



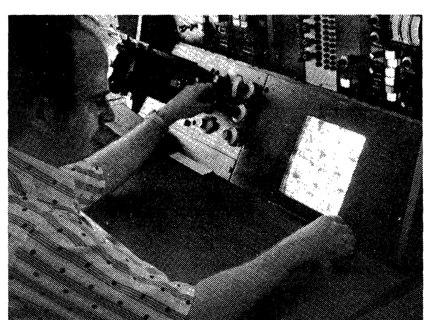
Die Probing

Device Testing

4



IQC Sign-off



Failure Analysis

Reliability Monitor and Control

Line Monitors

Line monitors are used to monitor the production line on a weekly basis. These monitors are designed to provide a constant feedback on product reliability. The following assembly/test monitors are conducted on a routine basis.

Assembly	Test
Package integrity	High-temperature reverse bias
Lead integrity	Intermittent operating life (power cycling)
Die integrity	High-temperature storage
Die-attach integrity	Temperature cycling
Bond integrity	Thermal shock
	Autoclave*
	85% R.H./85° C biased*

*Applied to plastic devices only.

Extended Reliability Tests

In conjunction with the weekly line-monitor program, Fairchild employs an extended reliability test program which is designed to reflect the long-term stability of Fairchild's Linear products. A summary of these reliability tests is shown in *Table 4-1.*

Quality and Reliability Data

Supplemental brochures are published on an annual basis which provide detailed failure rate data. Please contact Fairchild Sales Offices for additional reliability and quality information.

EXTENDED RELIABILITY TESTS	METAL CAN	PLASTIC
High Temperature Operating Life T_A = 150° C Readouts at 0, 168, 500, 1000 Hours	X	X
Temperature Cycling -65° C to +150° C (MIL-STD-883, Method 1010.1, Cond. C) Readouts at 0, 10, 100 Cycles Hermeticity (1 x 10^{-7} - TO-5, 1 x 10^{-6} - TO-3)	X	
Constant Acceleration F = 20K g 1 Min. Ea. 6 Axis (MIL-STD-883, Method 2001)	X	
Impact Shock 1500 g x 5 Blows (MIL-STD-883, Method 2002)	X	
Vibration, Variable Frequency 10 g (MIL-STD-883, Method 2007)	X	
Biased Humidity T_A = 85° C, RH = 85% Readouts at 0, 168, 500, 1000 Hours		X
Thermal Shock -55° C to +125° C Readouts at 0, 10, 100 Cycles MIL-STD-883, Method 1011, Condition C	X	X
Autoclave T_A = 125° C ± 2° C 15 PSI, 24 Hours		X

Table 4-1 Reliability Test Summary

HI REL PROCESSING — MIL-M-38510/MIL STD-883

A unique "company", within Fairchild Linear, is totally dedicated to the processing of high reliability products and to serving the special needs of the HI REL community. It consists of marketing, engineering, production control, manufacturing and quality assurance. Fairchild's HI REL processing facilities are among the most modern and sophisticated in the semiconductor industry. Screening procedures are set up to conform to the most recent version of MIL-STD-883, in conjunction with MIL-M-38510, which establishes standardized requirements for design, material, performance, control and documentation needed to achieve prescribed levels of device quality and reliability.

HI REL Unique II Program

Fairchild's Unique II program fills a longstanding need for a definite and comprehensive program covering HI REL semiconductor products...a program offering users a selection among multi-level screening flows and reliability requirements...a program providing clear and precise definitions on all areas of contractual performance...a program designed to reduce the high costs and delivery delays normally associated with HI REL. The objectives and benefits of the Unique II program for integrated circuits are these:

- Offers a full spectrum of processing options, including full compliance JAN and 883 Classes S, B, and C.
- Offers full compliance with JAN MIL-M-38510 and emphasizes the importance of this program.
- Accommodates the special needs of users' source control and specification control drawings.
- Offers models to aid users in development of source control drawings.
- Takes the mystery out of in-house processing to MIL-STD-883 and to MIL-M-38510 detail specifications. The Unique II program is definitive as to the similarities and differences in these requirements.
- Provides users with alternatives that may be used when JAN slash sheets or QPLs are unavailable, or for programs that demand the highest level of quality and reliability.

4

Fairchild offers a complete processing capability to fulfill requirements ranging from the least demanding to the most complex, including the following:

- Scanning Electron Microscope (SEM) Inspection
- Level A Visual
- Bond Pull and Die Shear Testing
- Read and Record and Δ Drift Parameters
- Particle Impact Noise Detection (Pin-D) Testing
- Group A, B, C and D Qualification Testing.

Standard Unique II processing flows are given on the following pages; special flows will be quoted on an individual basis.

MATRIX VI — COMMERCIAL AND INDUSTRIAL RELIABILITY PROGRAM

Commercial and industrial users increasingly demand optimized quality and reliability for the semiconductor integrated circuits purchased for their systems. Specific factors — increased integrated circuit usage per board, high costs for receiving inspection, pc board and systems repair, and the frequently immeasurable cost associated with field failures — require the user to attain high quality and reliability coupled with total cost. Matrix VI is designed to meet these user requirements.

Fairchild's Matrix VI Program offers a broad spectrum of screens and high technology/high volume integrated circuit products to meet the user's quality and reliability requirements typically associated with the commercial and industrial marketplace. There are two screening options for each package type, each with a separate degree of reliability and cost level. To simplify a cost-effective analysis, reliability factors have been assigned to each screening level. (See following pages.)

It is the goal of Matrix VI to achieve the highest possible reliability consistent with the user's needs and to avoid "over-buying". Cost-effective reliability is the essence of Matrix VI, the most comprehensive program of its kind now offered to the industrial/commercial marketplace.

JAN PART NUMBERING SYSTEM

J M 38510/ 101 01 B G C

JAN DESIGNATOR

Cannot be marked with "J" unless qualified on Part I or Part II of QLP-38510

General Procurement Spec.

REFERS TO DETAIL SPEC

- 101 Op Amps
- 102 Voltage Regulators
- 103 Comparators
- 104 Interface
- 105 733
- 106 Voltage Followers
- 107 3-Terminal Voltage Regulators
- 108 Transistor Arrays
- 109 Timers
- 110 Quad Op Amps

Defines Device Type

PROCESSING LEVEL

- S
- B
- C

PACKAGE TYPE

- A 14-pin 1/4 x 1/4 Flatpak
- B 14-pin 1/4 x 1/8 Flatpak
- C 14-pin 1/4 x 3/4 DIP
- D 14-pin 1/4 x 3/8 Flatpak
- E 16-pin 1/4 x 3/4 DIP
- F 16-pin 1/4 x 3/8 Flatpak
- G 8-pin Can
- H 10-pin 1/4 x 1/4 Flatpak
- I 10-pin Can
- J 24-pin 1/2 x 1 1/4 DIP
- K 24-pin 3/8 x 1/2 Flatpak
- L 24-pin 3/8 x 1/2 Flatpak
- X 3-pin TO-5 Can
- Y 2-pin TO-3 Can
- Z 24-pin 1/4 x 3/8 Flatpak

LEAD FINISH

- A Hot Solder DIP
- B Tin Plate
- C Gold Plate
- X Any of the above

LINEAR JAN GENERIC PART NUMBERS – EXAMPLES

JM38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A	2101	2108	118			
102	723									
103	710	711	106	111	2111					
104	55107	55108	9614	9615	55113	7831	7832	7820	7830	
105	733									
106	102	110	2110							
107	109	78M05	78M12	78M15	78M24	7805	7812	7815	7824	
108	3018	3045								
109	555	556								
110	148	149	4741	4136	124					

Note: Dated material. Please contact Fairchild for latest revisions.

HI REL PROCESS SCREENING REQUIREMENTS

JAN M38510

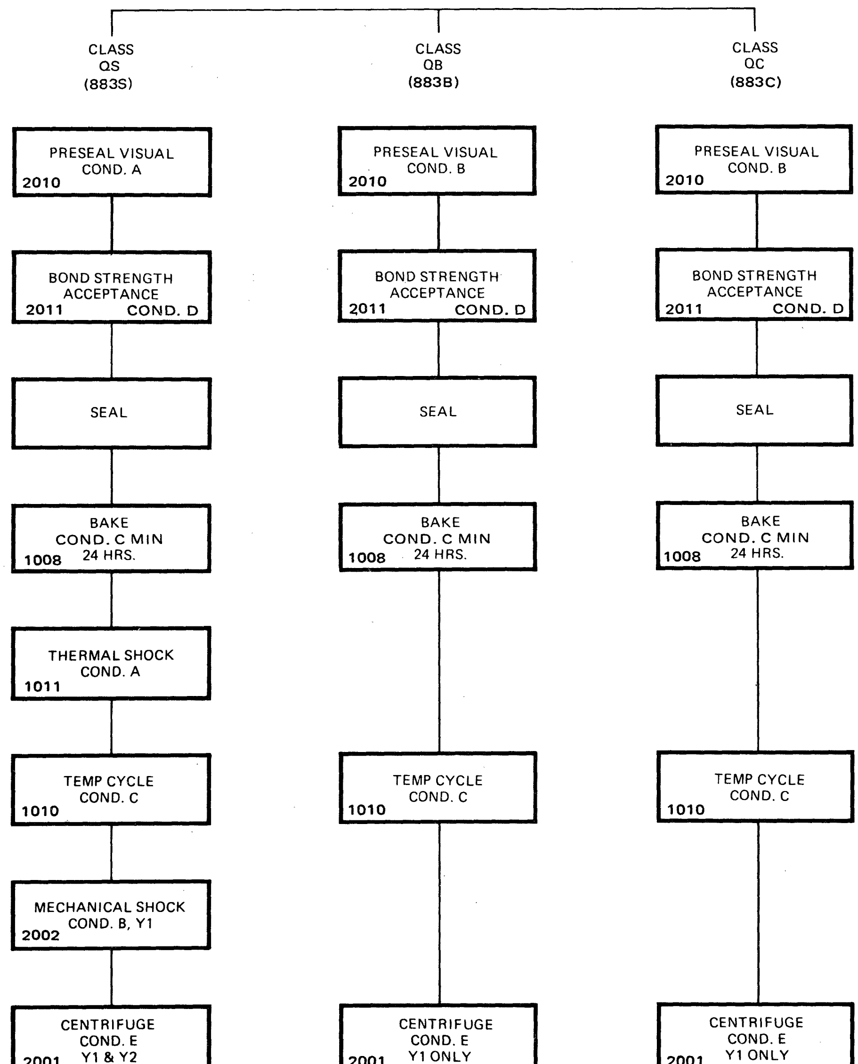
MIL-STD-883B TEST METHODS	DESCRIPTION	CLASS B	CLASS C
Preseal Visual MTD. 2010	Cond. A Maximum Visual Criteria Cond. B. Optimum Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength MTD 2011	Bond strength is monitored on a sample basis three times per shift per machine	BOND STRENGTH COND. D	BOND STRENGTH COND. D
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	BAKE COND. C MIN 24 HRS.	BAKE COND. C MIN 24 HRS.
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001 (Note1)	Cond. E 30000 G's X_1, X_2, Y_1, Y_2	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014 (Note 1)	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C Gross-FC43/Hot 10^{-3} cc/sec or Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C	HERMETICITY COND. A/B COND. C
Pre Burn-in Electrical MTD 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond. C Cond. D, Cond. E, Cond. F	BURN IN* 160 HRS 125°C	
Post Burn-in Electrical MTD 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C dc, 125°C dc, −55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc −55°C dc 25°C ac 10% PDA	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Life Tests Group D: Environmental Tests	QUALITY CONFORMANCE Gp A, B, C and D	QUALITY CONFORMANCE Gp A, B, C and D
External Visual MTD 2009	3X, 10X magnification: Verify dimensions, configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%
RELIABILITY	Figure of Merit	15	2
ORDERING	Part Number	JM38510/ 10101BCB	JM38510/ 10101CCB
	Part Marking	JM38510/ 10101BCB	JM38510/ 10101CCB

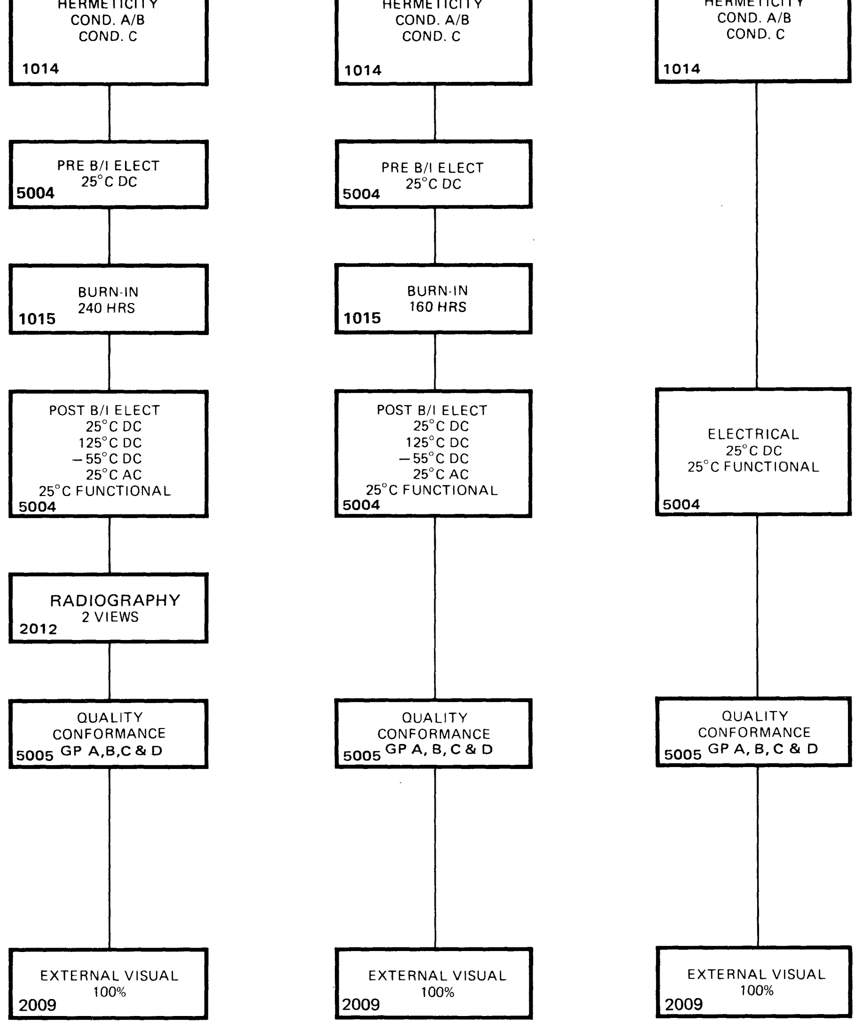
NOTE: RELIABILITY Figure of Merit is the Reliability Improvement Factor from RADC Reliability Notebook, Vol. II, RADC-TR-67-108, Table XII-6, page 419.

1. Not Applicable for TO-3 Cans

*Time Temperature Curve (method 1015) may be used.

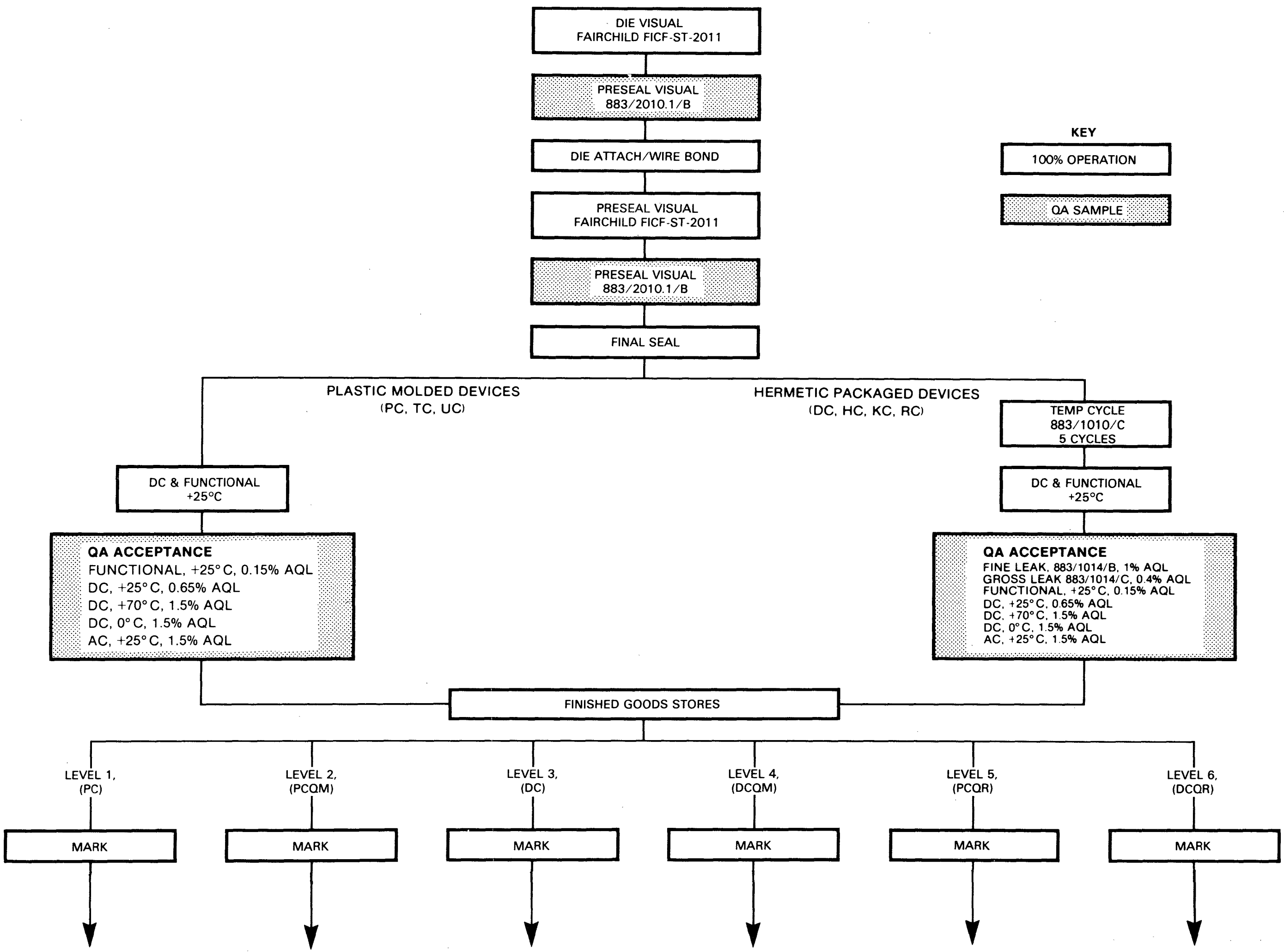
UNIQUE II

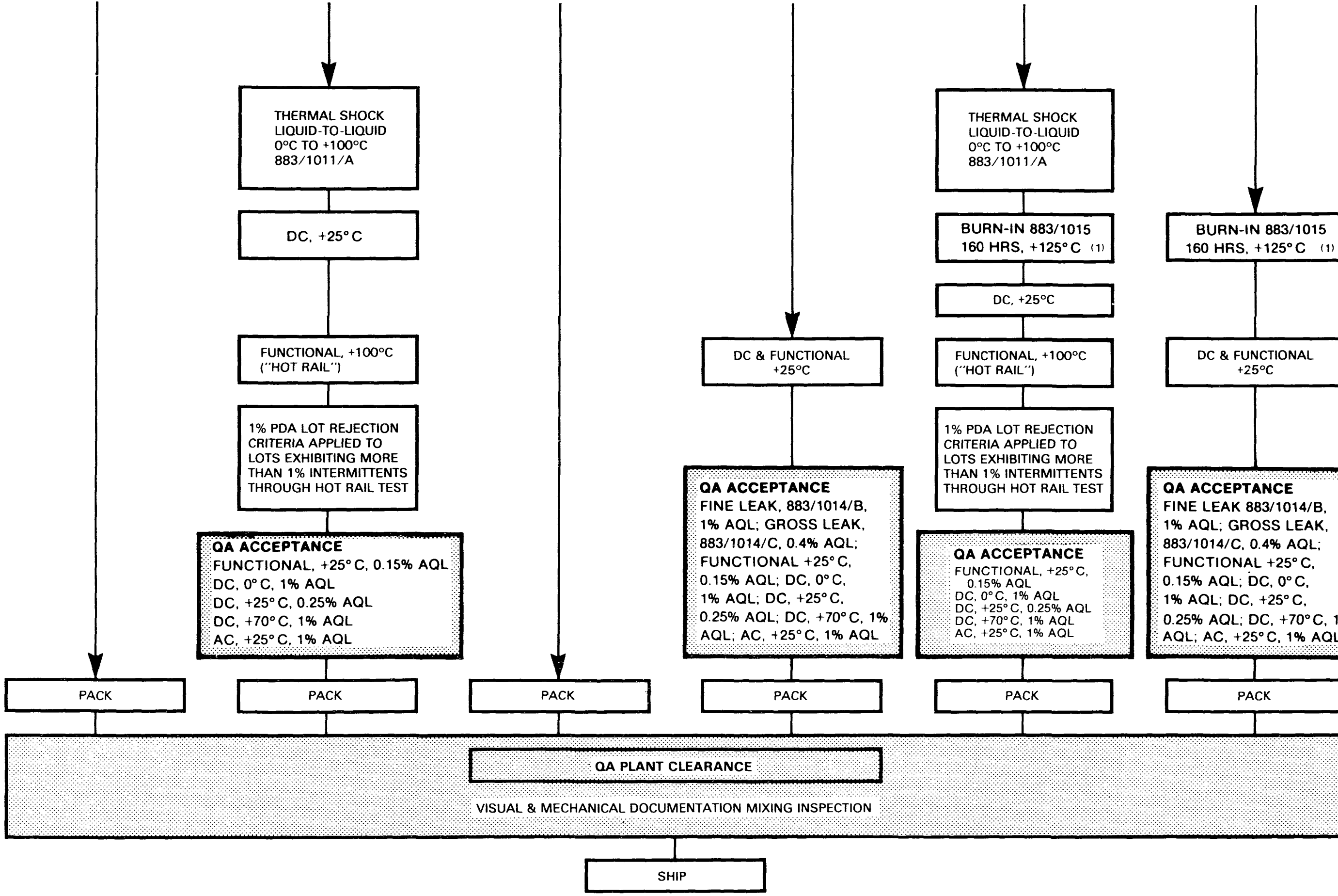

CLASS QS (883S)
CLASS QB (883B)
CLASS QC (883C)
PRESEAL VISUAL COND. A 2010
BOND STRENGTH ACCEPTANCE 2011 COND. D
SEAL
BAKE COND. C MIN 24 HRS. 1008
THERMAL SHOCK COND. A 1011
TEMP CYCLE COND. C 1010
MECHANICAL SHOCK COND. B, Y1 2002
CENTRIFUGE COND. E Y1 & Y2 2001
PRESEAL VISUAL COND. B 2010
BOND STRENGTH ACCEPTANCE 2011 COND. D
SEAL
BAKE COND. C MIN 24 HRS. 1008
TEMP CYCLE COND. C 1010
CENTRIFUGE COND. E Y1 ONLY 2001
PRESEAL VISUAL COND. B 2010
BOND STRENGTH ACCEPTANCE 2011 COND. D
SEAL
BAKE COND. C MIN 24 HRS. 1008
TEMP CYCLE COND. C 1010
CENTRIFUGE COND. E Y1 ONLY 2001



μA741 DMQS　　μA741 DMQB　　μA741 DMQC

MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS

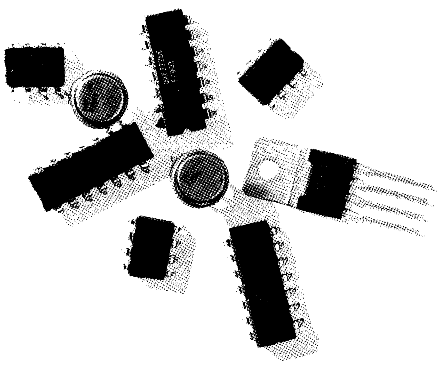




COST EFFECTIVENESS ANALYSIS

RELIABILITY FACTOR = 1X	RELIABILITY FACTOR ≅ 1.4X	RELIABILITY FACTOR ≅ 2X	RELIABILITY FACTOR ≅ 2.3X	RELIABILITY FACTOR ≅ 7.5X – 9X (2)	RELIABILITY FACTOR ≅ 14X
QUALITY GUARANTEE ON FUNCTIONALITY = 0.28% AQL	QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL	QUALITY GUARANTEE ON FUNCTIONALITY = 0.2% AQL	QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL	QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL	QUALITY GUARANTEE ON FUNCTIONALITY = 0.15% AQL
COST SEQUENCE 1	COST SEQUENCE 2	COST SEQUENCE 3	COST SEQUENCE 4	COST SEQUENCE 5	COST SEQUENCE 6

NOTE:
(1) Temperature Accelerated Testing may be used for MIL-STD-883 method 1015 Test Condition F.
(2) Burn-In has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9x. But should the field application be in a less controlled and power on/off application, the reliability would be approximately 7.5X.



OPERATIONAL AMPLIFIERS

OPERATIONAL AMPLIFIERS

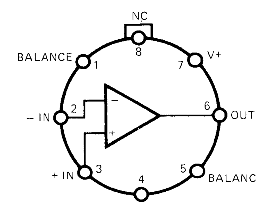
μAF155 • μAF355
LOW-SUPPLY CURRENT
μAF156 • μAF356
WIDEBAND
MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

- **LOW INPUT BIAS CURRENT . . . 30 pA**
- **HIGH INPUT IMPEDANCE . . . 10^{12} Ω**
- **LOW INPUT OFFSET VOLTAGE . . . 2 mV**
- **LOW INPUT OFFSET VOLTAGE TEMPERATURE DRIFT . . . 5 μV/°C**
- **LOW INPUT NOISE CURRENT . . . 0.01 pA/ $\sqrt{Hz}$**
- **HIGH COMMON MODE REJECTION RATIO . . . 100 dB**
- **LARGE DC VOLTAGE GAIN . . . 106 dB**

	μAF155	μAF156	Units
• EXTREMELY FAST SETTLING TIME TO 0.01%	4	1.5	μs
• FAST SLEW RATE	5	15	V/μs
• WIDE GAIN BANDWIDTH (μAF157 AV_{MIN} = 5)	2.5	5	MHz
• LOW INPUT NOISE VOLTAGE	20	12	nV/$\sqrt{Hz}$
• LOW SUPPLY CURRENT	2	5	mA

CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

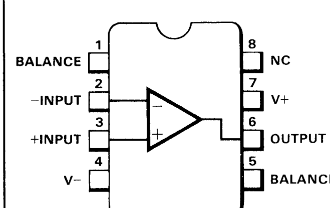


Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μAF155	μAF155HM
μAF355	μAF355HC
μAF156	μAF156HM
μAF356	μAF356HC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE CODE T



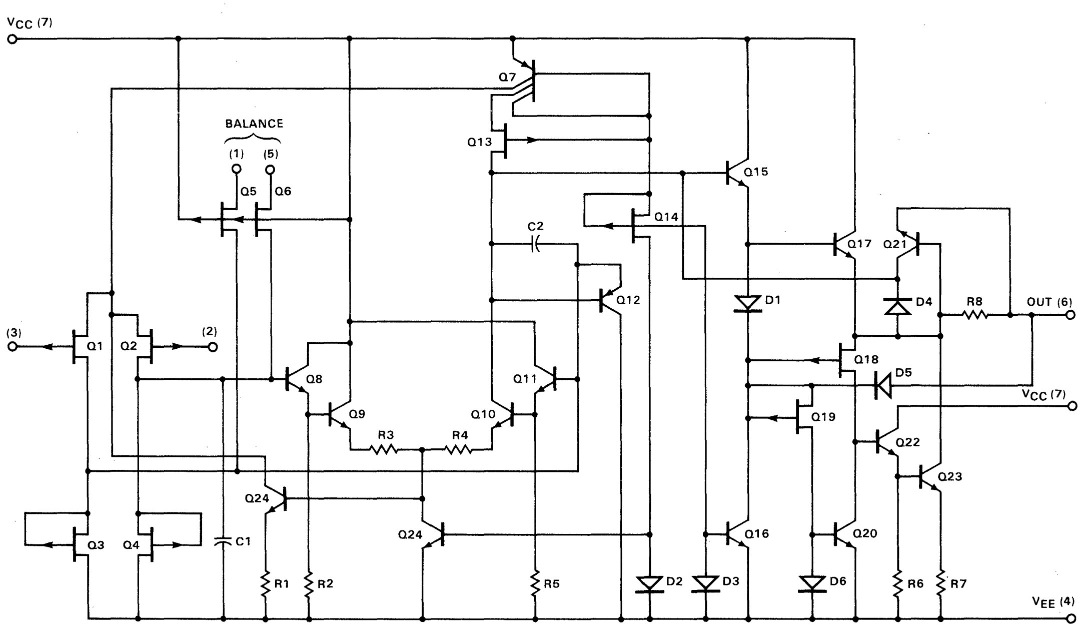
ORDER INFORMATION

TYPE	PART NO.
μAF355	μAF355TC
μAF356	μAF356TC
μAF357	μAF357TC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μAF155, μAF156	±22 V
μAF355, μAF356	±18 V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	
μAF155, μAF156	±40 V
μA355, μA356	±30 V
Input Voltage Range (Note 2)	
μAF155, μAF156	±20 V
μAF355, μAF356	±16 V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
μAF155, μAF156	−55°C to +125°C
μAF355, μAF356	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	300°C
Maximum Junction Temperature, $T_{J(MAX)}$	
μAF155, μAF156	150°C
μAF355, μAF356	100°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: T_A = +25°C unless otherwise noted. (Note 3)

CHARACTERISTICS	CONDITIONS	μAF155, μAF156			μAF355, μAF356			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{OS})	R_S = 50 Ω		3	5		3	10	mV
Average Input Offset Drift	R_S = 50 Ω		5			5		μV/°C
Change in Offset Drift with V_{OS} Adj.	R_S = 50 Ω (Note 6)		1			1		μV/°C/mV
Input Offset Current	T_J = 25°C (Note 4)		3	20		3	50	pA
Input Bias Current	T_J = 25°C (Note 4)		30	100		30	200	pA
Differential Input Resistance and Common Mode Input Resistance	T_J = 25°C		10^{12}			10^{12}		Ω
Large Signal Voltage Gain	V_S = ±15 V, R_L = 2 kΩ V_O = ±10 V	50	200		50	200		V/mV

The following specifications apply for T_C = −55°C to +125°C for μAF155/156
T_C = 0°C to 70°C for μAF355/356

CHARACTERISTICS	CONDITIONS	μAF155, μAF156 MIN	TYP	MAX	μAF355, μAF356 MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 50 Ω			7			13	mV
Input Offset Current				20			2	nA
Input Bias Current				50			8	nA
Large Signal Voltage Gain		25			15			V/mV
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±12	±13		±12	±13		V
Common Mode Voltage Range	V_S = ±15 V	±11	+15.1 −12		±10	±12	+15.1 −12	V
CMRR		85	100		85	100		dB
PSRR		85	100		85	100		dB

The following specifications apply for T_C = +25°C

CHARACTERISTICS	μAF155		μAF355		μAF156		μAF356		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	mA

CHARACTERISTICS	CONDITIONS	μAF155			μAF156			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	V_S = ±15 V, A_V = +1		5			15		V/μs
Gain Bandwidth Product			2.5			5.0		MHz
Setting Time to 0.01% (Note 5)			4			1.5		μs
Equivalent Input Noise	f = 100 Hz		25			15		nV/√Hz
Voltage (e_n)	f = 1 kHz		20			12		nV/√Hz
Equivalent Input Noise	f = 100 Hz		0.01			0.01		pA/√Hz
Current (i_n)	f = 1 kHz		0.01			0.01		pA/√Hz
Input Capacitance (C_{IN})			3			3		pF

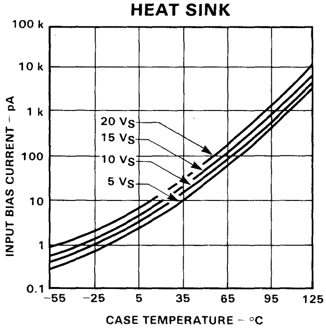
5

NOTES FOR ELECTRICAL CHARACTERISTICS:

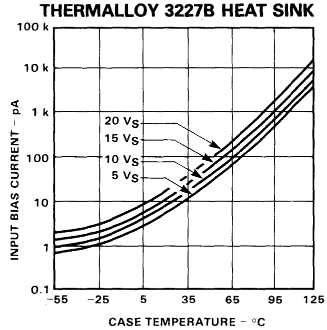
1. For operating at high temperature the package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for ±15 V ⩽ 20 V, unless otherwise stated for the μAF155, μAF156. For the μAF355, μAF356 the temperature specifications are V_S = ±15 V.
4. The input bias currents are junction package currents which approximately double for every 10°C increase in the junction temperature (T_J). Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation (P_D). $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
5. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the μAF155, μAF156. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.10% of its final value from the time a 10 V step input is applied to the inverter.
6. For voltages across the external resistors used in the offset adjust circuitry of greater than a volt (R_{EXT} = 100 k), the Temperature Coefficient of the adjusted input offset voltage changes only a small amount (1 μV/C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.

DC TYPICAL PERFORMANCE CHARACTERISTICS

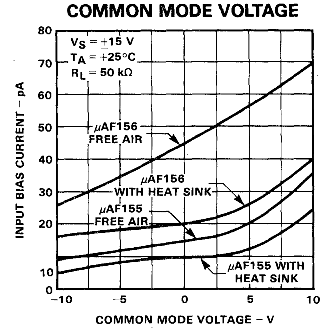
μAF155 INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE WITH THERMALLOY 3227B HEAT SINK



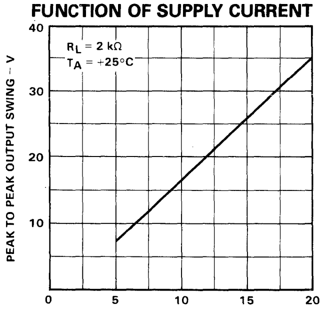
μAF156 INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE WITH THERMALLOY 3227B HEAT SINK



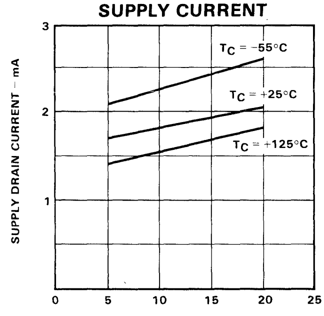
μAF155, μAF156 INPUT BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



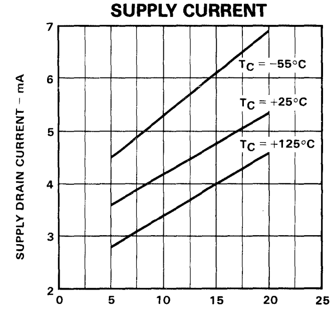
μAF155, μAF156 MAXIMUM VOLTAGE SWING AS A FUNCTION OF SUPPLY CURRENT



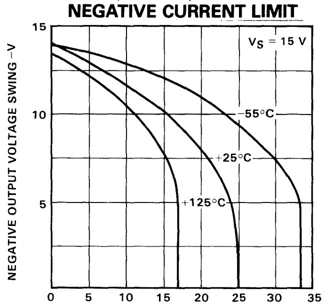
μAF155 SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



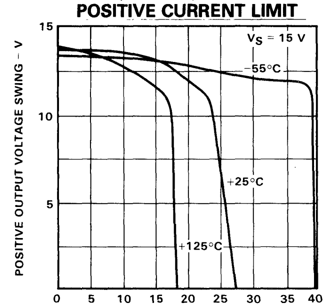
μAF156 SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



μAF155, μAF156 NEGATIVE CURRENT LIMIT

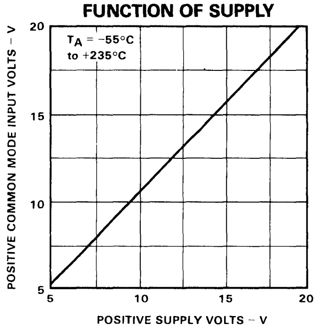


μAF155, μAF156 POSITIVE CURRENT LIMIT

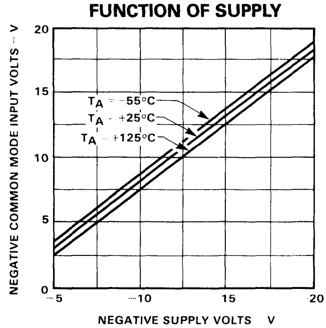


DC TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

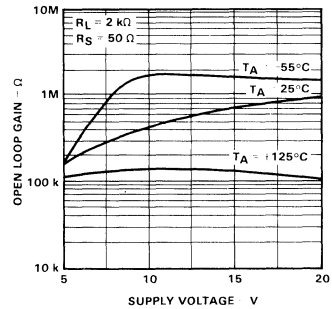
μAF155, μAF156 POSITIVE COMMON MODE INPUT VOLTAGE AS A FUNCTION OF SUPPLY



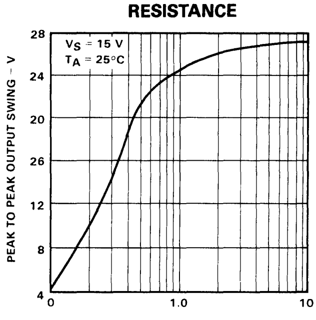
μAF155, μAF156 NEGATIVE COMMON MODE INPUT VOLTAGE AS A FUNCTION OF SUPPLY



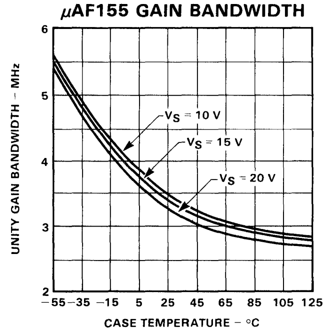
μAF155, μAF156 LOOP GAIN AS A FUNCTION OF SUPPLY VOLTAGE



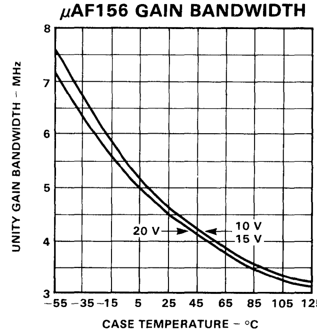
μAF155, μAF156 VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



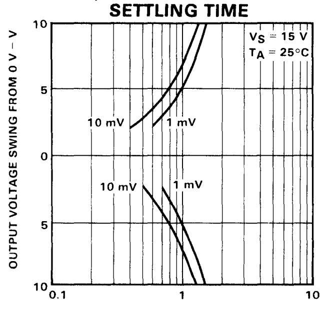
μAF155 GAIN BANDWIDTH



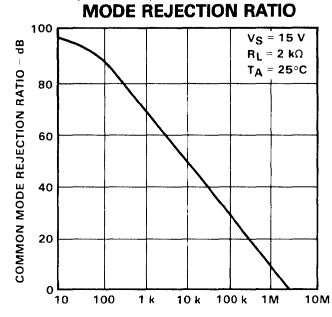
μAF156 GAIN BANDWIDTH



μAF156 INVERTER SETTLING TIME



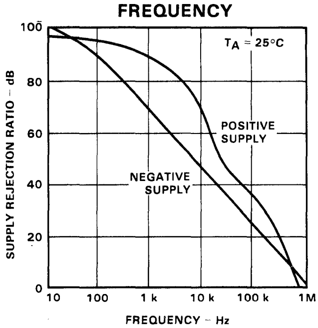
μAF155, μAF156 COMMON MODE REJECTION RATIO



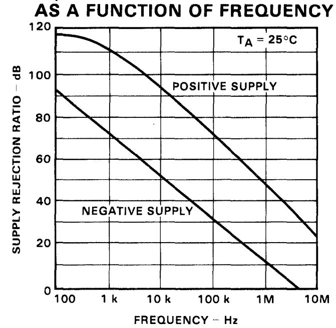
5

DC TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

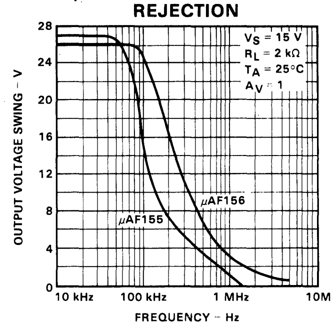
MAXIMUM UNDISTORTED SWING AS A FUNCTION OF FREQUENCY



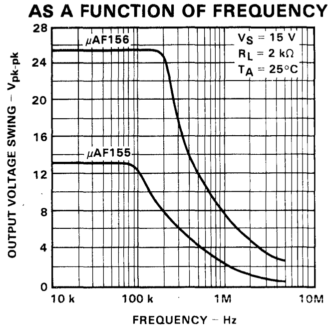
μAF156 SUPPLY REJECTION AS A FUNCTION OF FREQUENCY



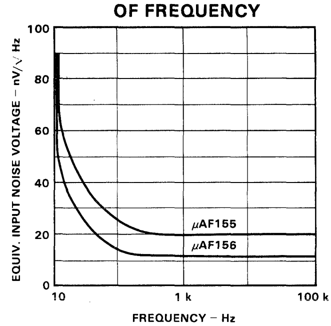
μAF155 POWER SUPPLY REJECTION



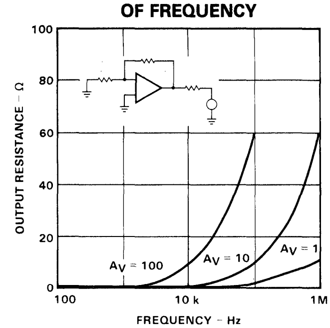
MAXIMUM OUTPUT SWING AS A FUNCTION OF FREQUENCY



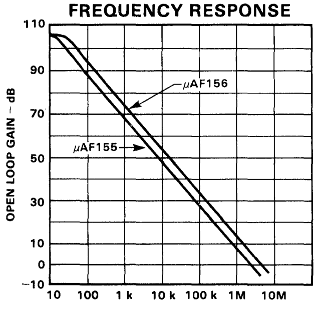
EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



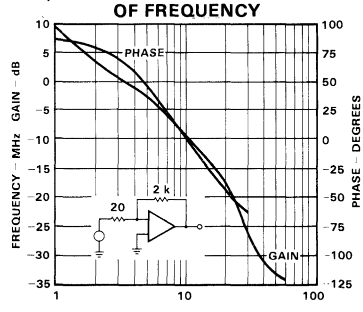
μAF155, μAF156 OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



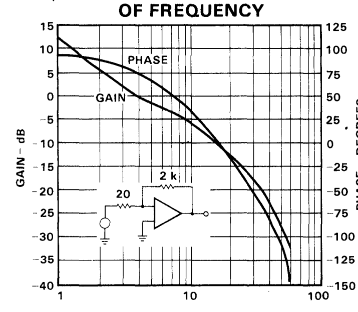
OPEN LOOP FREQUENCY RESPONSE



μAF155 GAIN AS A FUNCTION OF FREQUENCY



μAF156 GAIN AS A FUNCTION OF FREQUENCY



μAF771 SINGLE • μAF772 DUAL μAF774 QUAD BIFET

OPERATIONAL AMPLIFIER FAMILY

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — These monolithic JFET input operational amplifiers incorporate well matched ion implanted JFETS on the same chip with standard bipolar transistors. The key features of these op amps are low input bias currents in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

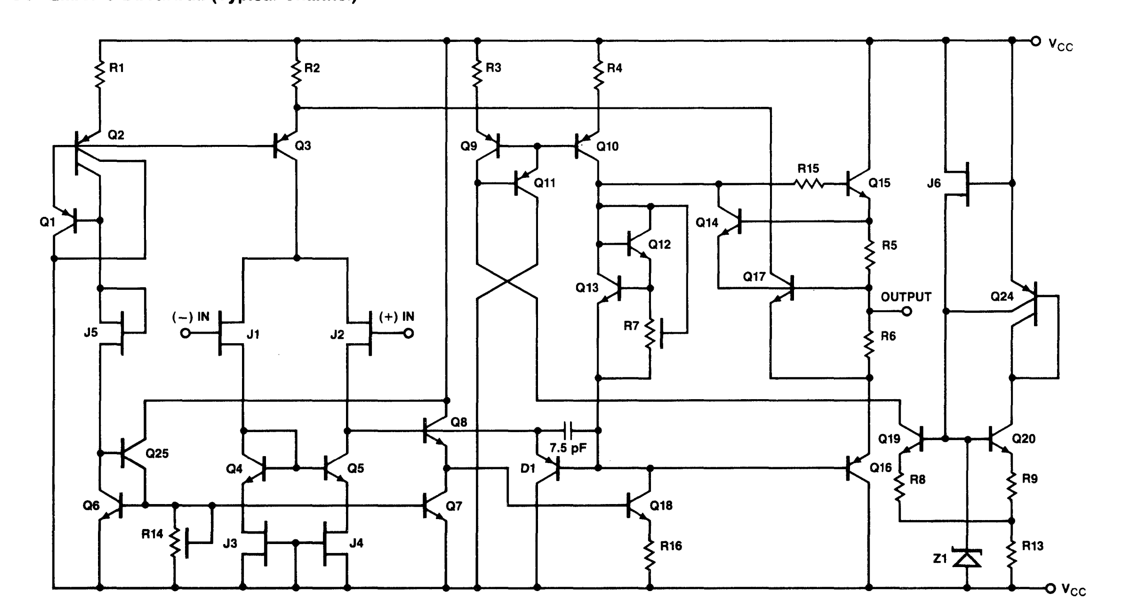
- **LOW INPUT BIAS CURRENT – 200 pA FOR μAF77X**
- **LOW INPUT OFFSET CURRENT – 100 pA FOR μAF77X**
- **HIGH SLEW RATE – 13 V/μs TYPICALLY**
- **WIDE BANDWIDTH – 3.0 MHz TYPICALLY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
DIP Package (9A) (6A)	670 mW
Molded Mini DIP Package (6T) (9T)	310 mW
Hermetic Package (5S)	500 mW
Differential Input Voltage	±30 V
Input Voltage Range (Note 2)	±16 V
Output Short Circuit Duration	continuous
Storage Temperature Range	
(5S) (6A)	−65°C to +150°C
(9A) (9T)	−55°C to +125°C
Operating Temperature Range	
Commercial (μAF77XA, μAF77XB, μAF77X, μAF77XL)	0°C to +70°C
Military (μAF77XAM, μAF77XBM)	−55°C to +125°C
Pin Temperature	
Molded Package (9T, 9A) Soldering 10 s	260°C
Hermetic Package (5S, 6A, 6T) Soldering 60 s	300°C

5

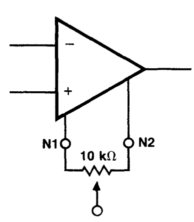
SCHEMATIC DIAGRAM (Typical Channel)



DC ELECTRICAL CHARACTERISTICS — COMMERCIAL GRADE DEVICES

SYMBOL	CHARACTERISTICS	CONDITIONS	μAF77XA			μAF77XB			μAF77X			μAF77XL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The Following Specifications Apply for $V_S = \pm15$ V, $T_A = 25°C$															
V_{OS}	Input Offset Voltage	Note 3 $R_S = 10$ kΩ	–	–	2.0	–	–	5.0	–	–	10.0	–	–	15.0	mV
I_{OS}	Input Offset Current	Notes 3, 4 $T_j = 25°C$	–	–	50	–	–	50	–	–	100	–	–	100	pA
I_B	Input Bias Current	Notes 3, 4 $T_j = 25°C$	–	50	100	–	50	100	–	50	200	–	50	200	pA
R_{IN}	Input Resistance		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V $R_L = 2$ kΩ	50	100	–	50	100	–	50	100	–	50	100	–	V/mV
I_{SC}	Short Circuit Current		–	25	–	–	25	–	–	25	–	–	25	–	mA
I_S	Supply Current	Per Amplifier	–	–	2.8	–	–	2.8	–	–	2.8	–	–	2.8	mA
The Following Specifications Apply for $V_S = \pm15$ V, $0°C \leq T_A \leq 70°C$															
V_{OS}	Input Offset Voltage	Note 3 $R_S = 10$ kΩ	–	–	4.0	–	–	7.0	–	–	13	–	–	20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10$ kΩ	–	10	–	–	10	–	–	10	–	–	10	–	μV/°C
I_{OS}	Input Offset Current	Notes 3, 4	–	–	2.0	–	–	2.0	–	–	4.0	–	–	4.0	nA
I_B	Input Bias Current	Notes 3, 4	–	–	4.0	–	–	4.0	–	–	8.0	–	–	8.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V $R_L = 2$ kΩ	25	–	–	25	–	–	25	–	–	25	–	–	V/mV
V_O	Output Voltage Swing	$R_L = 10$ kΩ	±12	–	–	±12	–	–	±12	–	–	±12	–	–	V
		$R_L = 2$ kΩ	±10	–	–	±10	–	–	±10	–	–	±10	–	–	V
V_{CM}	Input Common Mode Voltage Range		±11	+15 −12	–	±11	+15 −12	–	±11	+15 −12	–	±11	+15 −12	–	V
CMRR	Common Mode Rejection Ratio	$R_S = 10$ kΩ	80	–	–	80	–	–	70	–	–	70	–	–	dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10$ kΩ	80	–	–	80	–	–	70	–	–	70	–	–	dB
I_S	Supply Current	Per Amplifier	–	–	3.0	–	–	3.0	–	–	3.0	–	–	3.0	mA

INPUT OFFSET VOLTAGE NULL CIRCUITS



(μAF771 and μAF772 — 14 pin)

DC ELECTRICAL CHARACTERISTICS — MILITARY GRADE DEVICES

SYMBOL	CHARACTERISTICS	CONDITIONS	μAF77XAM			μAF77XBM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
The Following Specifications Apply for $V_S = \pm15$ V, $T_A = 25°C$									
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$ Note 3	–	–	2.0	–	–	5.0	mV
I_{OS}	Input Offset Current	Notes 3, 4 $T_j = 25°C$	–	–	50	–	–	50	pA
I_B	Input Bias Current	Notes 3, 4 $T_j = 25°C$	–	50	100	–	50	100	pA
R_{IN}	Input Resistance		–	10^{12}	–	–	10^{12}	–	Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = 10$ V, $R_L = 2\ k\Omega$	50	–	–	50	–	–	V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$	±12	–	–	±12	–	–	V
		$R_L = 2\ k\Omega$	±10	–	–	±10	–	–	V
V_{CM}	Input Common Mode Voltage Range		±11	+15 −12	–	±11	+15 −12		V
CMRR	Common Mode Rejection Ratio	$R_S = 10\ k\Omega$	80	–	–	80	–	–	dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10\ k\Omega$	80	–	–	80	–	–	dB
I_S	Supply Current	Per Amplifier	–	–	2.8	–	–	2.8	mA
The Following Specifications Apply for $V_S = \pm15$ V, $-55°C \leq T_A \leq 125°C$									
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$ Note 3	–	–	5.0	–	–	8.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$	–	10	–	–	10	–	μV/°C
I_{OS}	Input Offset Current	Notes 3, 4	–	–	20	–	–	20	nA
I_B	Input Bias Current	Notes 3, 4	–	–	50	–	–	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm10$ V, $R_L = 2k\Omega$	25	–	–	25	–	–	V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$	±12	–	–	±12	–	–	V
		$R_L = 2\ k\Omega$	±10	–	–	±10	–	–	
CMRR	Common Mode Rejection Ratio	$R_S = 10\ k\Omega$	–	80	–	–	80	–	dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10\ k\Omega$	–	80	–	–	80	–	dB
I_S	Supply Current	Per Amplifier	–	–	3.4	–	–	3.4	mA

COMMERCIAL AND MILITARY
AC ELECTRICAL CHARACTERISTICS $V_S = \pm15$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTICS	CONDITIONS	μAF77XA/AM			μAF77XB/BM			μAF77X			μAF77XL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	(Fig. 1)		13			13			13			13		V/μs
GBW	Gain Bandwidth Product	(Fig. 2)		3.0			3.0			3.0			3.0		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\ \Omega$, f = 1000 Hz		16			16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1000 Hz		0.01			0.01			0.01			0.01		$pA/\sqrt{Hz}$

NOTES:
1. Rating applies to ambient temperatures up to 70°C above $T_A = 70°C$. Derate linearly 6.3 mW/°C for the metal can, 5.6 mW/°C for the mini DIP and 8.3 mW/°C for the DIP.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. I_B and I_{OS} are measured at $V_{CM} = 0$.
4. The input bias currents are junction leakage currents which approximately double for every 10°C inrease in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A = \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
5. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

AC CHARACTERISTICS MEASUREMENT INFORMATION

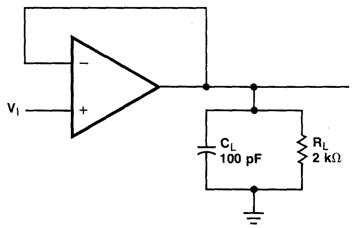


Fig. 1. Unity Gain Amplifier

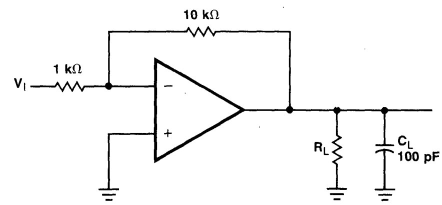


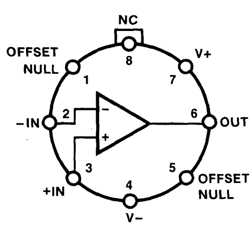
Fig. 2. Gain-of-10 Inverting Amplifier.

CONNECTION DIAGRAMS AND ORDERING INFORMATION

μAF771

8-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE	5B	5S
PACKAGE CODE	H	H



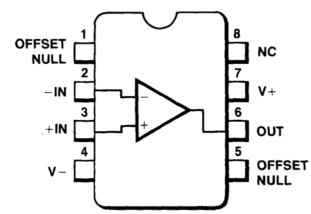
Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μAF771AM	μAF771AHM
μAF771BM	μAF771BHM
μAF771A	μAF771AHC
μAF771B	μAF771BHC
μAF771	μAF771HC
μAF771L	μAF771LHC

8-PIN MINI DIP
(TOP VIEW)

PACKAGE OUTLINES	6T	9T
PACKAGE CODES	R	T



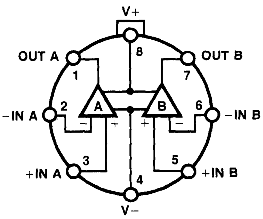
ORDER INFORMATION

TYPE	PART NO.
μAF771AM	μAF771ARM
μAF771BM	μAF771BRM
μAF771A	μAF771ARC
μAF771B	μAF771BRC
μAF771	μAF771RC
μAF771L	μAF771LRC
μAF771A	μAF771ATC
μAF771B	μAF771BTC
μAF771	μAF771TC
μAF771L	μAF771LTC

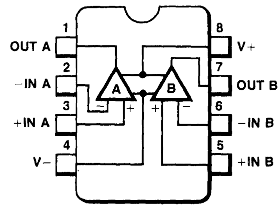
CONNECTION DIAGRAMS AND ORDERING INFORMATION (Cont.)

µAF772

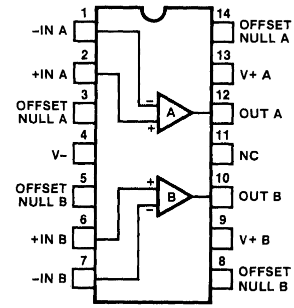
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S 5B
PACKAGE CODE H H



8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES R T



14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION (8-Pin Metal Can)

TYPE	PART NO.
µAF772AM	µAF772AHM
µAF772BM	µAF772BHM
µAF772A	µAF772AHC
µAF772B	µAF772BHC
µAF772	µAF772HC
µAF772L	µAF772LHC

ORDER INFORMATION (8-Pin Mini DIP)

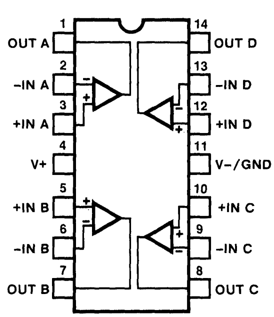
TYPE	PART NO.
µAF772AM	µAF772ARM
µAF772BM	µAF772BRM
µAF772A	µAF772ARC
µAF772B	µAF772BRC
µAF772	µAF772RC
µAF772L	µAF772LRC
µAF772A	µAF772ATC
µAF772B	µAF772BTC
µAF772	µAF772TC
µAF772L	µAF772LTC

ORDER INFORMATION (14-Pin DIP)

TYPE	PART NO.
µAF772AM	µAF772ADM
µAF772BM	µAF772BDM
µAF772A	µAF772ADC
µAF772B	µAF772BDC
µAF772	µAF772DC
µAF772L	µAF772LDC
µAF772A	µAF772APC
µAF772B	µAF772BPC
µAF772	µAF772PC
µAF772L	µAF772LPC

µAF774

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
µAF774AM	µAF774ADM
µAF774BM	µAF774BDM
µAF774A	µAF774ADC
µAF774B	µAF774BDC
µAF774	µAF774DC
µAF774L	µAF774LDC
µAF774A	µAF774APC
µAF774B	µAF774BPC
µAF774	µAF774PC
µAF774L	µAF774LPC

5

μA101 • μA201

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

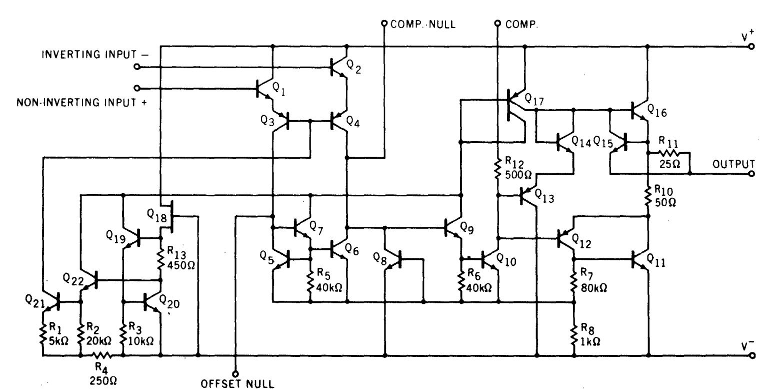
GENERAL DESCRIPTION – The μA101 and μA201 are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The μA101 and μA201 compensate easily with a single external component. High common mode voltage range and absence of "latch-up" make the μA101 and μA201 ideal for use as voltage followers. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA101 and μA201 are short-circuit protected and have the same pin configuration as the popular μA741, μA748 and μA709.

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

ABSOLUTE MAXIMUM RATINGS

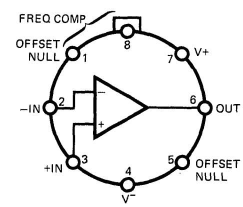
Supply Voltage	±22V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	
Metal Can, DIP	–65°C to +150°C
Operating Temperature Range (Note 3)	
Military (μA101)	–55°C to +125°C
Commercial (μA201)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



Notes on following pages

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

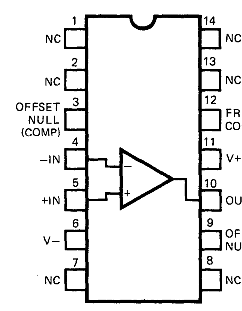


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA101	μA101HM
μA201	μA201HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA101	μA101DM
μA201	μA201DC

*Planar is a patented Fairchild process.

μA101

ELECTRICAL CHARACTERISTICS: $\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1.0	5.0	mV
Input Offset Current			40	200	nA
Input Bias Current			120	500	nA
Input Resistance		300	800		kΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		μV/°C
	$R_S \leq 10\,k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		100	500	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq +125°C$ $-55°C \leq T_A \leq +25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		0.28	1.5	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\,k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB

NOTES
1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the Metal Can and 8.3mW/°C for the DIP.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. The 101 ratings apply to +125°C case temperature or +75°C ambient temperature. The 201 ratings apply to case temperatures up to +70°C.

μA201

ELECTRICAL CHARACTERISTICS: $\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.25	1.5	μA
Input Resistance		100	400		kΩ
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	20	150		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		6.0		μV/°C
	$R_S \leq 10\,k\Omega$		10.0		μV/°C
Input Offset Current	$T_A = 70°C$		50	400	nA
	$T_A = 0°C$		150	750	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$		0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		0.02	0.6	nA/°C
Input Bias Current	$T_A = 0°C$		0.32	2.0	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\,k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB

µA101A • µA201A • µA301A

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The µA101A, µA201A and µA301A are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the µA101A, µA201A, or µA301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "latch-up" coupled with internal short circuit protection make the µA101A, µA201A and µA301A virtually foolproof.

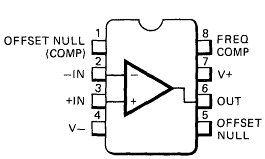
- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (µA101A and µA201A)	±22V
Commercial (µA301A)	±18V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Mini DIP	310 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (µA101A)	−55°C to +125°C
Instrument (µA201A)	−25°C to +85°C
Commercial (µA301A)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Can, DIP and Flatpak (60 s)	300°C
Mini DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

CONNECTION DIAGRAMS

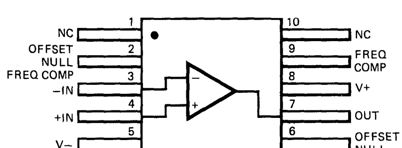
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
µA301A	µA301ATC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

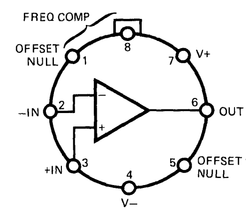


Available on special request.

ORDER INFORMATION

TYPE	PART NO.
µA101A	µA101AFM
µA201A	µ201AFM

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

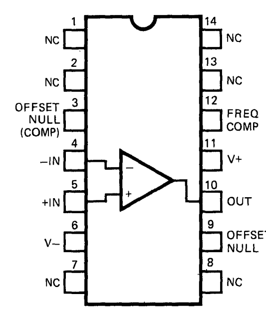


NOTE: Pin Connected to Case.

ORDER INFORMATION

TYPE	PART NO.
µA101A	µA101AHM
µA201A	µA201AHM
µA301A	µA301AHC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
µA101A	µA101ADM
µA201A	µA201ADM
µA301A	µA301ADC

Notes on page 3

*Planar is a patented Fairchild process.

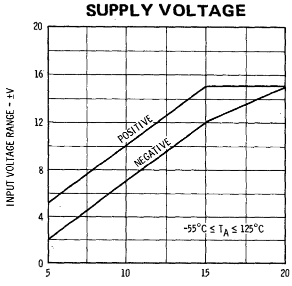
μA101A and μA201A

ELECTRICAL CHARACTERISTICS: $\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified.

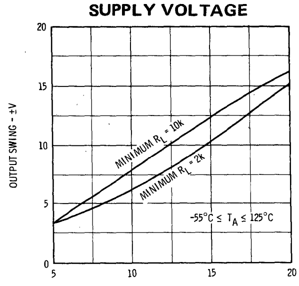
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leq T_A \leq +125°C$: (Note 4)					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq +125°C$		0.01	0.1	nA/°C
	$-55°C \leq T_A \leq +25°C$		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\,k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	80	96		dB

GUARANTEED PERFORMANCE CURVES FOR μA101A AND μA201A

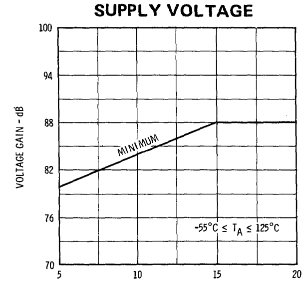
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



µA301A

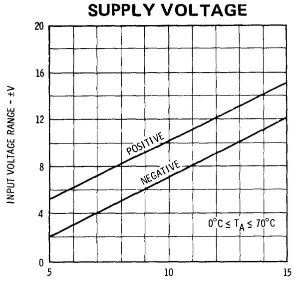
ELECTRICAL CHARACTERISTICS: $\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		2.0	7.5	mV
Input Offset Current			3	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2		MΩ
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	25	160		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	µV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$		0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		0.02	0.6	nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\,k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB

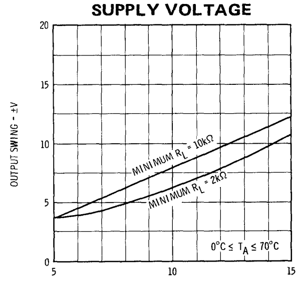
NOTES:
(1) Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. 101A and 201A ratings apply to +125°C case temperature or +75°C ambient temperature. 301A ratings apply for case temperatures to 70°C.
(4) All 201A specifications apply for $-25°C \leq T_A \leq +85°C$ unless otherwise specified.

GUARANTEED PERFORMANCE CURVES FOR µA301A

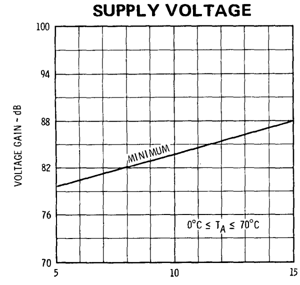
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

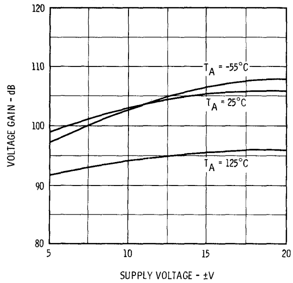


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

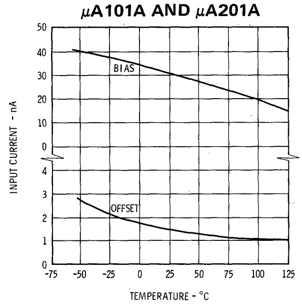


TYPICAL PERFORMANCE CURVES FOR µA101A, µA201A AND µA301A

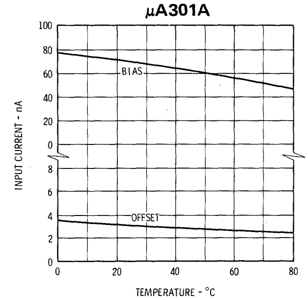
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



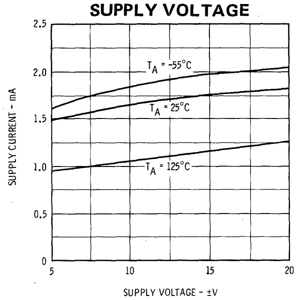
INPUT CURRENT AS A FUNCTION OF TEMPERATURE µA101A AND µA201A



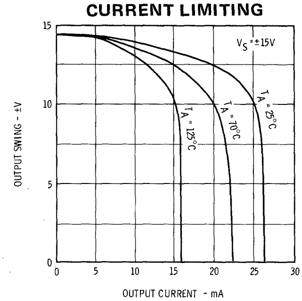
INPUT CURRENT AS A FUNCTION OF TEMPERATURE µA301A



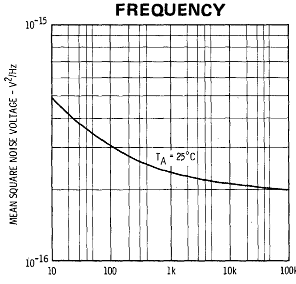
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



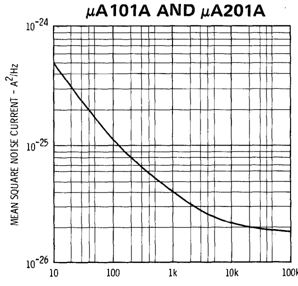
CURRENT LIMITING



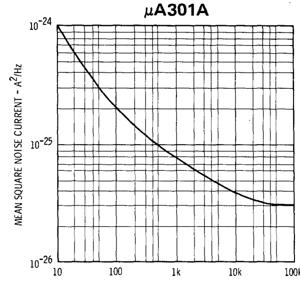
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



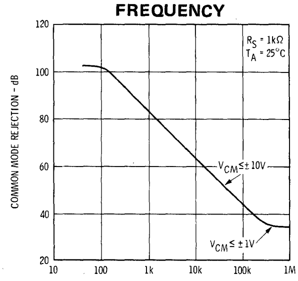
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY µA101A AND µA201A



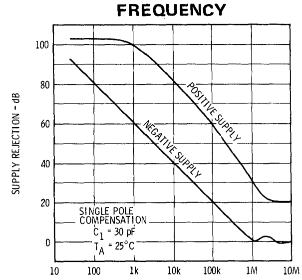
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY µA301A



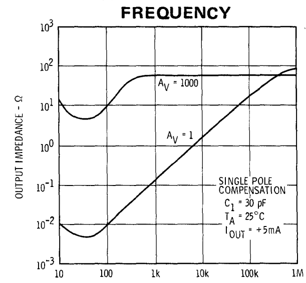
COMMON MODE REJECTION AS A FUNCTION OF FREQUENCY



POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY

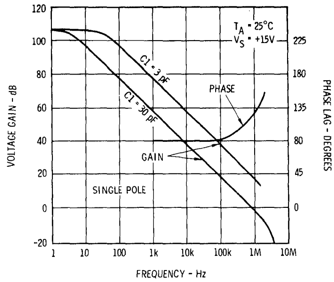


CLOSED LOOP OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

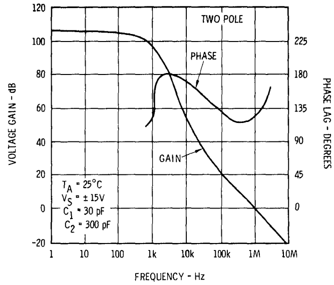


TYPICAL PERFORMANCE CURVES FOR μA101A, μA201A AND μA301A

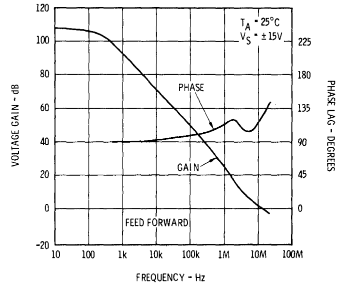
OPEN LOOP FREQUENCY RESPONSE



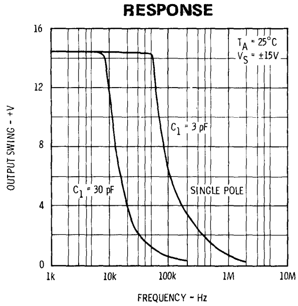
OPEN LOOP FREQUENCY RESPONSE



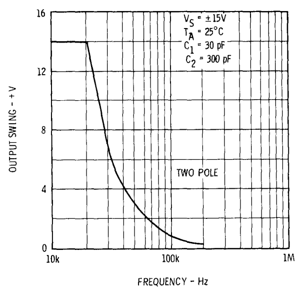
OPEN LOOP FREQUENCY RESPONSE



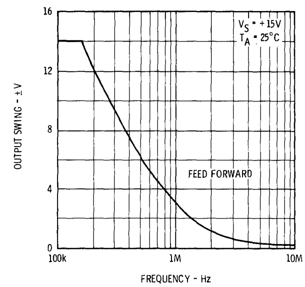
LARGE SIGNAL FREQUENCY RESPONSE



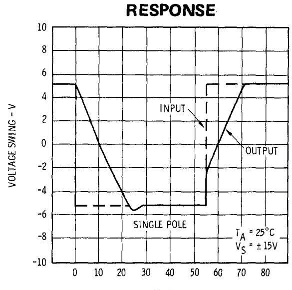
LARGE SIGNAL FREQUENCY RESPONSE



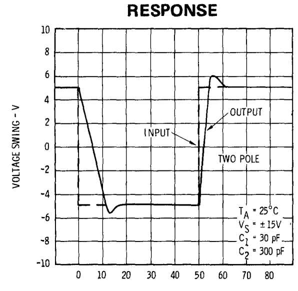
LARGE SIGNAL FREQUENCY RESPONSE



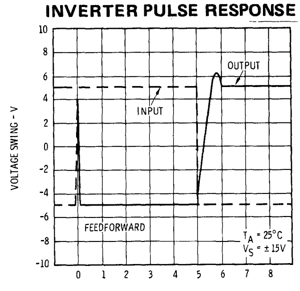
VOLTAGE FOLLOWER PULSE RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



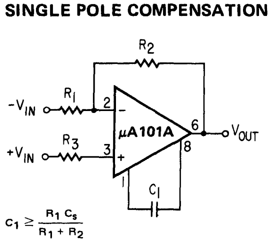
INVERTER PULSE RESPONSE



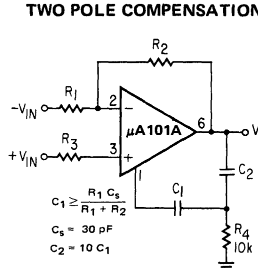
COMPENSATION CIRCUITS

(All pin numbers shown refer to 8-Pin TO-5 package)

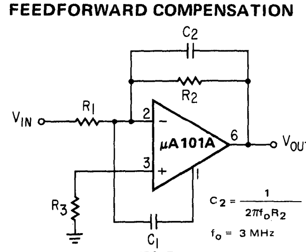
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION



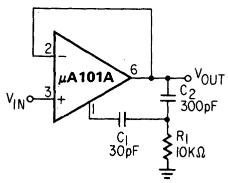
FEEDFORWARD COMPENSATION



TYPICAL APPLICATIONS

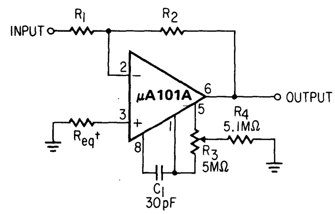
(All pin numbers shown refer to 8-Pin TO-5 package)

FAST VOLTAGE FOLLOWER



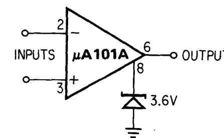
Power Bandwidth: 15 kHz
Slew Rate: 1 V/μs

INVERTING AMPLIFIER WITH BALACING CIRCUIT

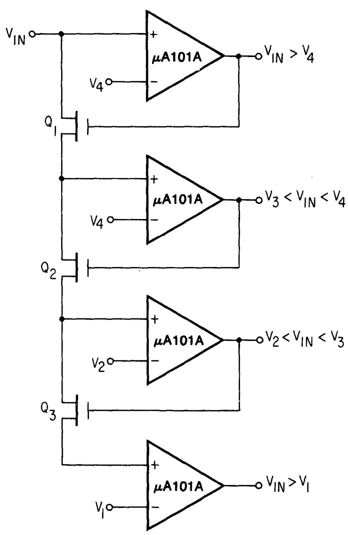


† May be zero or equal to parallel combination of R1 and R2 for minimum offset.

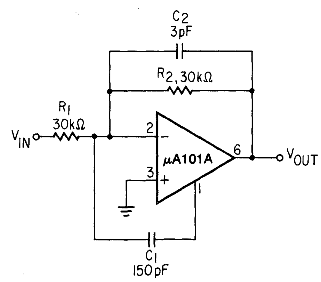
VOLTAGE COMPARATOR FOR DRIVING DTL OR TTL INTEGRATED CIRCUITS



MULTIPLE APERTURE WINDOW DISCRIMINATOR

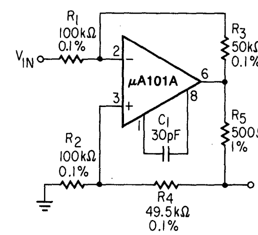


FAST SUMMING AMPLIFIER



Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

BILATERAL CURRENT SOURCE

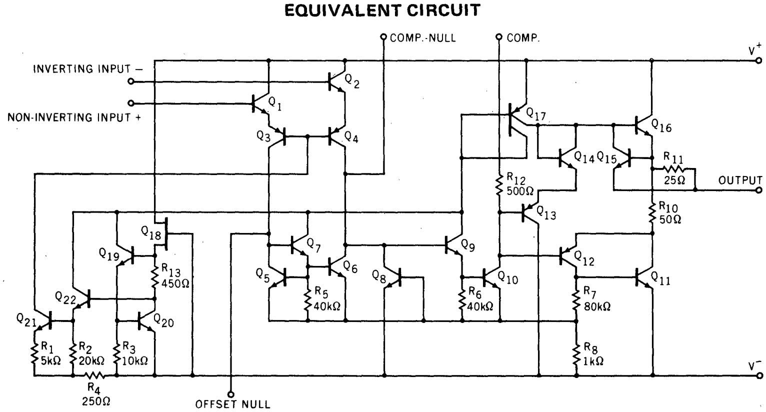


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$$

$R_3 = R_3 + R_5$

$R_1 = R_2$

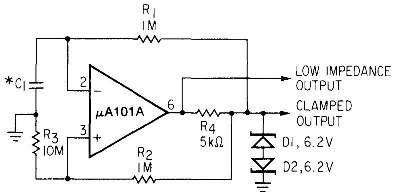
EQUIVALENT CIRCUIT



TYPICAL APPLICATIONS (Cont'd)

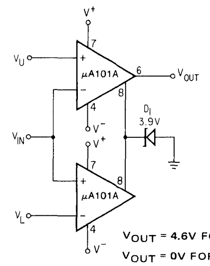
(All pin numbers shown refer to 8-Pin TO-5 package)

LOW FREQUENCY SQUARE WAVE GENERATOR



* Adjust C_1 for frequency

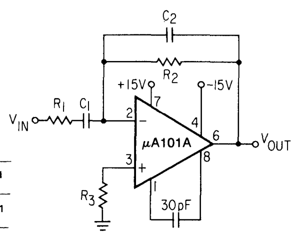
DOUBLE ENDED LIMIT DETECTOR



V_{OUT} = 4.6V FOR $V_L \leq V_{IN} \leq V_U$

V_{OUT} = 0V FOR $V_{IN} < V_L$ OR $V_{IN} < V_U$

PRACTICAL DIFFERENTIATOR

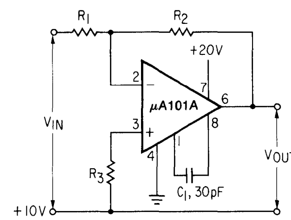


$$f_c = \frac{1}{2\pi R_2 C_1}$$

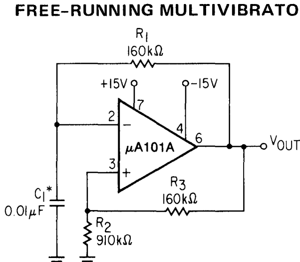
$$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$$

$$f_c < f_h < f_{unity\ gain}$$

CIRCUIT FOR OPERATING WITHOUT A NEGATIVE SUPPLY

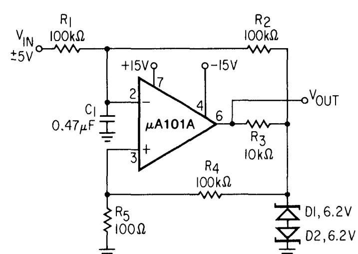


FREE-RUNNING MULTIVIBRATOR

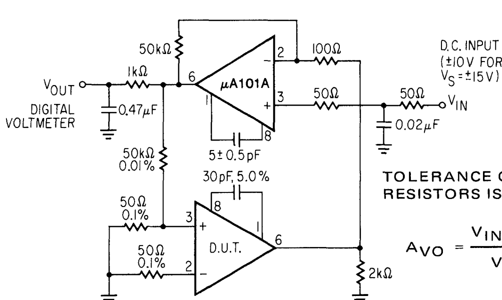


*Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



GAIN TEST CIRCUIT



TOLERANCE OF ALL UNMARKED RESISTORS IS 1%

$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}} = \frac{10 \times 10^3}{V_{OUT}} \text{ FOR } \pm 10\text{V INPUT}$$

μA102 • μA302 • μA110 • μA310

VOLTAGE FOLLOWER OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

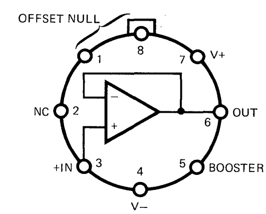
GENERAL DESCRIPTION – The μA102/302 and μA110/310 are monolithic Operational Amplifiers internally connected as unity gain non-inverting amplifiers. They are constructed using the Fairchild Planar* epitaxial process. These circuits are ideal for such applications as fast sample and hold circuits, active filters, or as general purpose buffers. Super-beta transistors are used allowing the devices to operate at very low input currents without sacrificing speed. They may be used interchangeably with the μA101 and the μA741 in voltage follower applications. The μA110/310 are suggested for new designs and are direct replacements for the μA102/302. They feature lower offset voltage, drift, bias current, noise, plus higher speed and a wider operating voltage range.

- HIGH SLEW RATE – 30 V/μs
- LOW INPUT CURRENT
- INTERNALLY COMPENSATED
- PLUG-IN REPLACEMENT FOR BOTH THE μA101 AND μA741 VOLTAGE FOLLOWER APPLICATIONS
- WIDE RANGE OF SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA102, μA110)	−55°C to +125°C
Commercial (μA302, μA310)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C

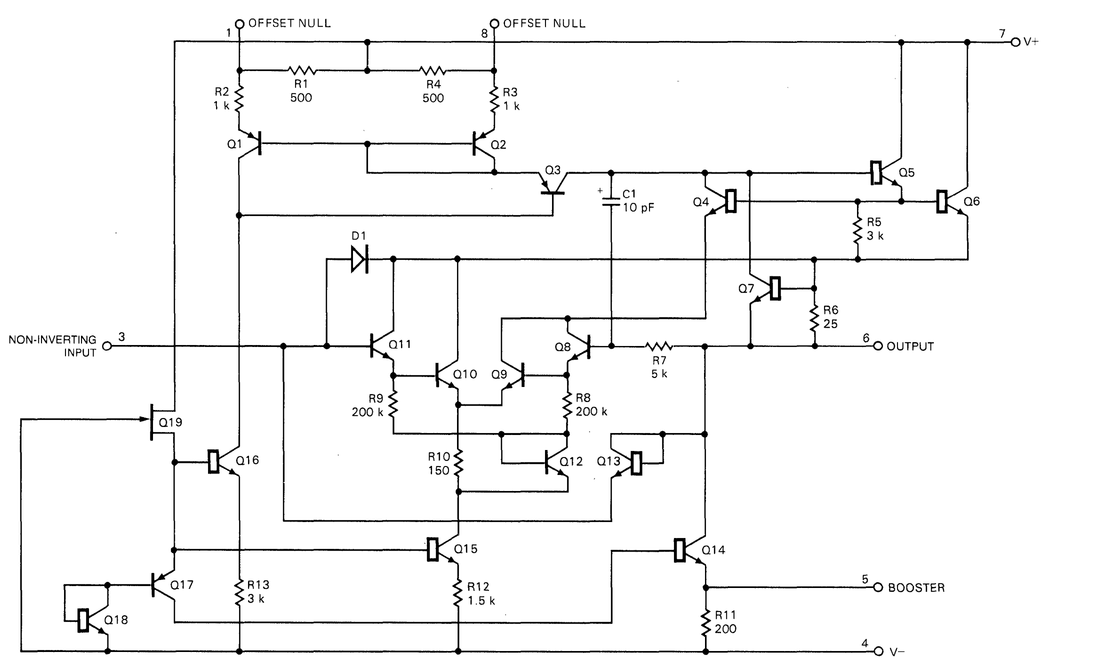
CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA102	μA102HM
μA302	μA302HC
μA110	μA110HM
μA310	μA310HC

EQUIVALENT CIRCUIT



See notes on following pages

*Planar is a patented Fairchild process.

μA102

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$, $C_L \leq 100$ pF, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage			2.0	5.0	mV
Average Temperature Coefficient of Offset Voltage			6.0		μV/°C
Input Current			3.0	10	nA
Input Resistance		10^{10}	10^{12}		Ω
Voltage Gain	$R_L \geq 10$ kΩ	0.999	0.9996		
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq 8$ kΩ	±10	±13		V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance				3.0	pF
Offset Voltage	$-55°C \leq T_A \leq 125°C$			7.5	mV
Input Current	$T_A = 125°C$		3.0	10	nA
	$T_A = -55°C$		30	100	nA
Voltage Gain	$-55°C \leq T_A \leq 125°C$ $R_L \geq 10$ kΩ	0.999			
Output Voltage Swing	$R_L \geq 10$ kΩ	±10			V
Supply Current	$T_A = 125°C$		2.6	4.0	mA

μA302

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$, $C_L \leq 100$ pF, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage			5.0	15	mV
Average Temperature Coefficient of Offset Voltage			20		μV/°C
Input Current			10	30	nA
Input Resistance		10^{9}	10^{12}		Ω
Voltage Gain	$R_L > 8$ kΩ	0.9985	0.9995	1.000	
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq 8$ kΩ	±10			V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance			3.0		pF
Offset Voltage	$0°C \leq T_A \leq 70°C$			20	mV
Input Current	$T_A = 70°C$		3.0	15	nA
	$T_A = 0°C$		20	50	nA

5

μA110

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±18 V, −55°C < T_A ≤ +125°C, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = 25°C		1.5	4.0	mV
Input Bias Current	T_A = 25°C		1.0	3.0	nA
Input Resistance	T_A = 25°C	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15 V V_{OUT} = ±10 V, R_L = 8 kΩ	0.999	0.9999		
Output Resistance	T_A = 25°C		0.75	2.5	Ω
Supply Current	T_A = 25°C		3.9	5.5	mA
Input Offset Voltage				6.0	mV
Offset Voltage Temperature Drift	−55°C ≤ T_A ≤ 85°C		6.0		μV/°C
	T_A = 125°C		12		μV/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V R_L = 10 kΩ	0.999			
Output Voltage Swing (Note 4)	V_S = ±15 V, R_L = 10 kΩ	±10			V
Supply Current	T_A = 125°C		2.0	4.0	mA
Supply Voltage Rejection Ratio	±5 V ≤ V_S ≤ ±18 V	70	80		dB

μA310

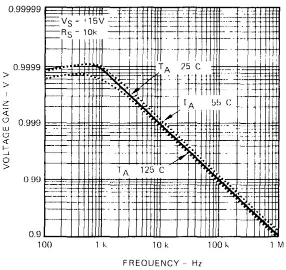
ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±18 V, 0°C ≤ T_A ≤ +70°C, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = 25°C		2.5	7.5	mV
Input Bias Current	T_A = 25°C		2.0	7.0	nA
Input Resistance	T_A = 25°C	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15 V V_{OUT} = ±10 V, R_L = 8 kΩ	0.999	0.9999		
Output Resistance	T_A = 25°C		0.75	2.5	Ω
Supply Current	T_A = 25°C		3.9	5.5	mA
Input Offset Voltage				10	mV
Offset Voltage Temperature Drift			10		μV/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V R_L = 10 kΩ	0.999			
Output Voltage Swing (Note 4)	V_S = ±15 V, R_L = 10 kΩ	±10			V
Supply Voltage Rejection Ratio	±5 V ≤ V_S ≤ ±18 V	70	80		dB

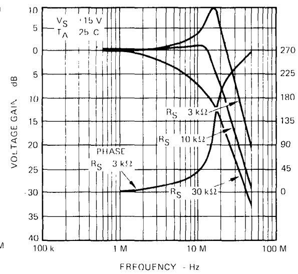
NOTES:
1. Rating applies to ambient temperatures up to +70°C. Above +70°C ambient, derate linearly at 6.3 mW/°C.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. For 102 and 110 continuous short circuit is allowed for case temperature of +125°C and ambient temperature to +70°C. For 302 and 310 continuous short circuit is allowed for case temperature to +70°C and ambient temperature to +55°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.
4. Increased output swing under load can be obtained by connecting an external resistor between the booster and V− terminals (see curve).

TYPICAL PERFORMANCE CURVES FOR μA102 • μA302 • μA110 • μA310

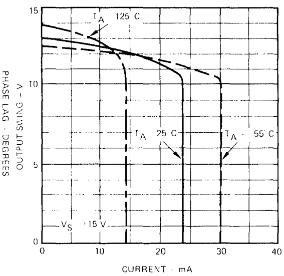
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



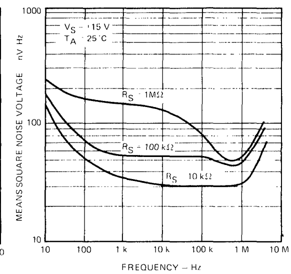
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



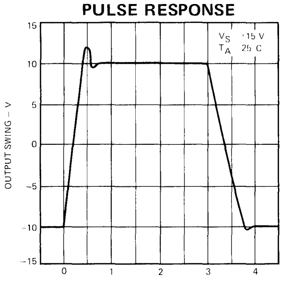
POSITIVE OUTPUT SWING AS A FUNCTION OF CURRENT



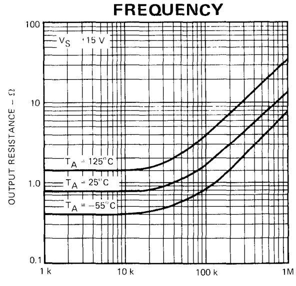
OUTPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



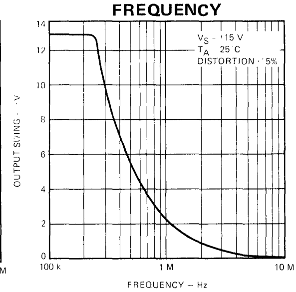
LARGE SIGNAL PULSE RESPONSE



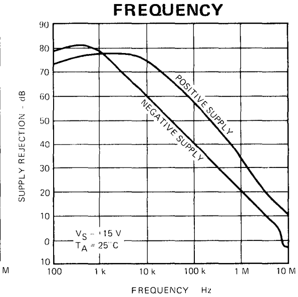
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



LARGE SIGNAL FREQUENCY RESPONSE AS A FUNCTION OF FREQUENCY

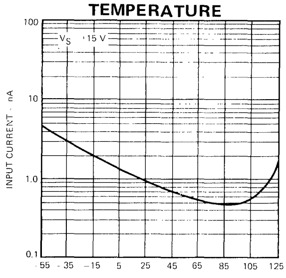


POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY

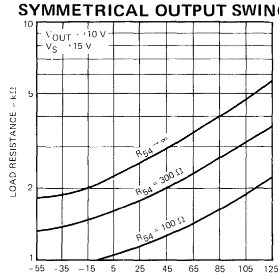


TYPICAL PERFORMANCE CURVES FOR μA102 • μA110

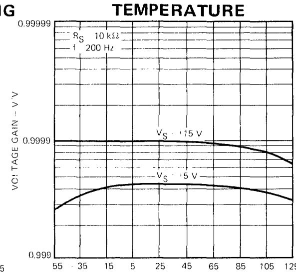
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



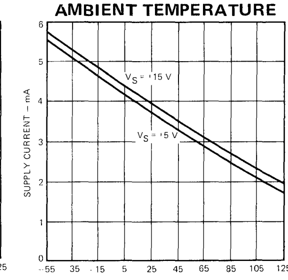
SYMMETRICAL OUTPUT SWING



VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

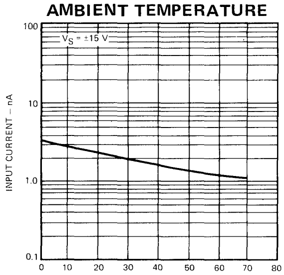


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

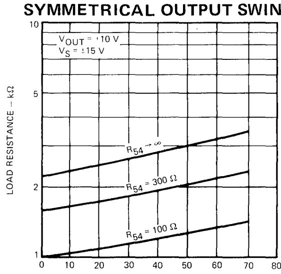


TYPICAL PERFORMANCE CURVES FOR μA302 • μA310

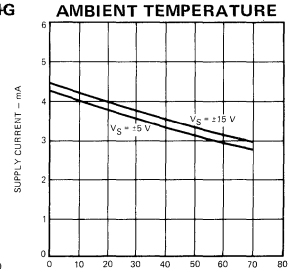
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



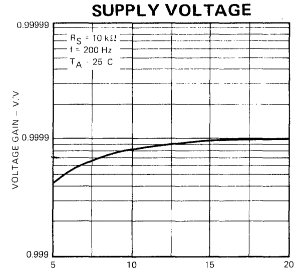
SYMMETRICAL OUTPUT SWING



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

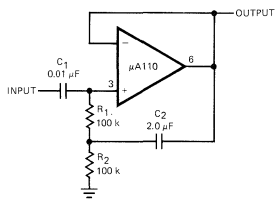


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

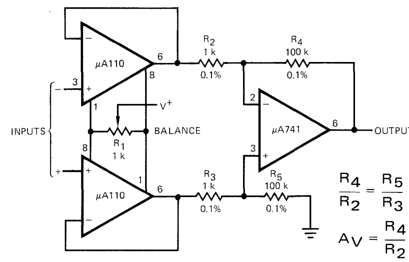


TYPICAL APPLICATIONS

HIGH INPUT IMPEDANCE AC AMPLIFIER



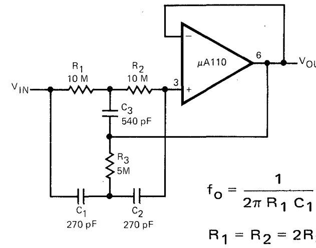
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



$$\frac{R_4}{R_2} = \frac{R_5}{R_3}$$

$$A_V = \frac{R_4}{R_2}$$

HIGH Q NOTCH FILTER

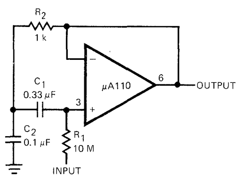


$$f_o = \frac{1}{2\pi R_1 C_1}$$

$$R_1 = R_2 = 2R_3$$

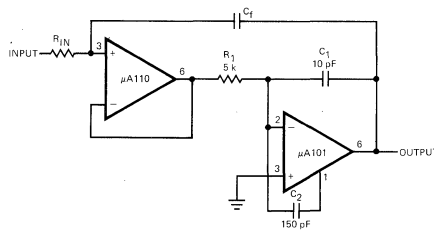
$$C_1 = C_2 = \frac{C_3}{2}$$

BANDPASS FILTER

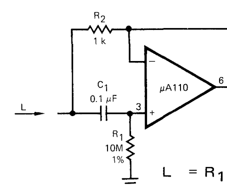


$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

FAST INTEGRATOR WITH LOW INPUT CURRENT



SIMULATED INDUCTOR

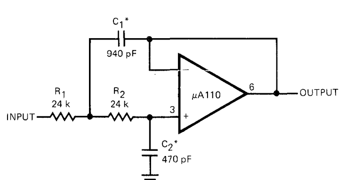


$$L = R_1 R_2 C_1$$

$$R_S = R_2$$

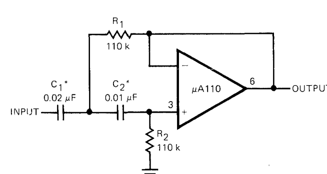
$$R_P = R_1$$

LOW PASS ACTIVE FILTER



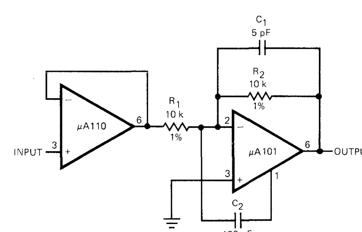
*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

HIGH PASS ACTIVE FILTER

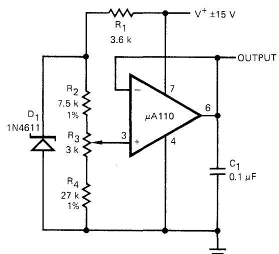


*Values are 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability

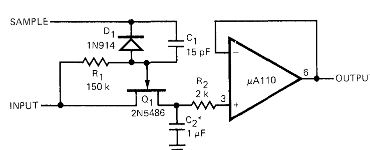
FAST INVERTING AMPLIFIER WITH HIGH INPUT IMPEDANCE



BUFFERED REFERENCE SOURCE

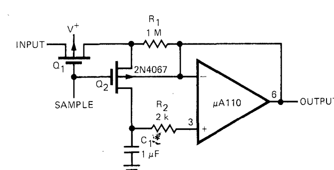


SAMPLE AND HOLD



*Use capacitor with polycarbonate teflon or polyethylene dielectric.

LOW DRIFT SAMPLE AND HOLD**



*Teflon, polyethylene or polycarbonate dielectric capacitor

**Worst case drift less than 3 mV/s

μA107 • μA207 • μA307

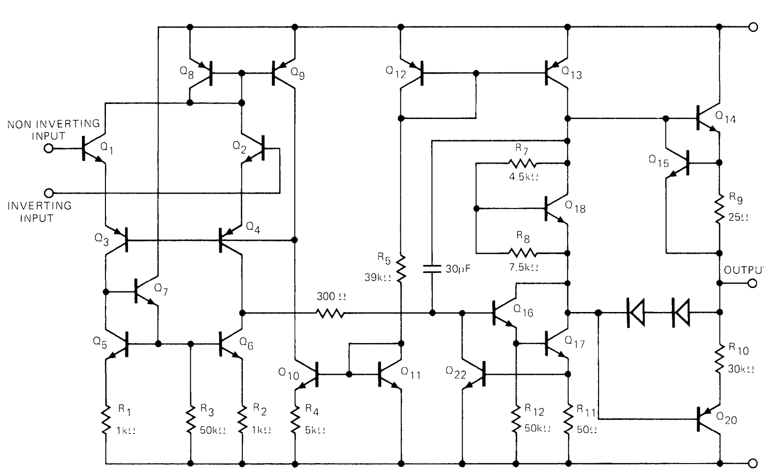
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA107 General Purpose Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. Advanced processing techniques have reduced the 107 input current an order of magnitude below industry standards such as the μA709 while still replacing, pin-for-pin, μA709, μA101, μA101A, and μA741. The μA107, μA207, and μA307 offer better accuracy, internal compensation, and lower noise for high impedance circuit applications while providing features similar to the μA101A. The low input currents allow the device to be used in slow-charge applications such as long period integrators, slow ramps, and sample-and-hold circuits. The μA207 is identical to the μA107 except that the μA207 performance is guaranteed from −25°C to +85°C while the μA107 performance is guaranteed over a −55°C to +125°C temperature range. The μA307 is available in both TO-99 and 8-pin mini DIP packages and is guaranteed over a 0°C to +70C temperature range.

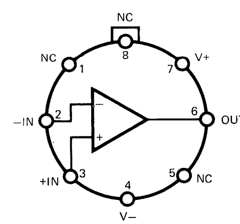
- LOW OFFSET VOLTAGE
- LOW INPUT CURRENT
- LOW OFFSET CURRENT
- GUARANTEED DRIFT CHARACTERISTICS
- GUARANTEED OFFSETS OVER COMMON MODE RANGE

EQUIVALENT CIRCUIT



Pin connections shown are for metal can.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

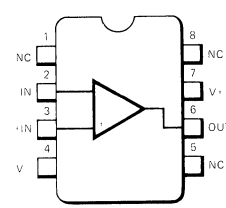


Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA107	μA107HM
μA207	μA207HM
μA307	μA307HC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA307	μA307TC

Dual In-line Package and Flatpak Available By Special Request

*Planar is patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (μA107 and μA207)	±22 V
Commercial (μA307)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA107)	−55°C to +125°C
Instrument (μA207)	−25°C to +85°C
Commercial (μA307)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Can (60 s)	300°C
Mini DIP (10 s)	260°C
Output Short Circuit Duration (μA107 and μA207)	Indefinite
(μA307, Note 3)	Indefinite

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

μA107 and μA207

ELECTRICAL CHARACTERISTICS: $\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ **for μA107 and μA207 unless otherwise specified.**

CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$			0.7	2.0	mV
Input Offset Current				1.5	10	nA
Input Bias Current				30	75	nA
Input Resistance			1.5	4.0		MΩ
Supply Current	$V_S = \pm 20\ V$			1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$		50	160		V/mV
The following applies for $55°C \leq T_A \leq 125°C$ unless otherwise specified						
Input Offset Voltage	$R_S \leq 50\ k\Omega$				3.0	mV
Average Temperature Coefficient of Input Offset Voltage				3.0	15	μV/°C
Input Offset Current					20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$			0.01	0.1	nA/°C
	$-55°C \leq T_A \leq 25°C$			0.02	0.2	nA/°C
Input Bias Current					100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20\ V$			1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$		25			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$	$R_L = 10\ k\Omega$	±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 20\ V$		±15			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		dB

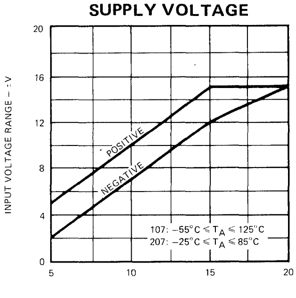
μA307

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±15 V, T_A = 25°C unless otherwise specified.

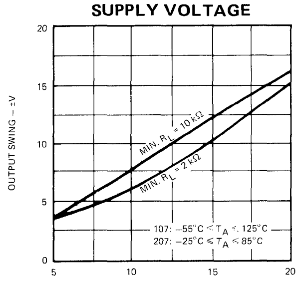
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S ≤ 50 kΩ		2.0	7.5	mV
Input Offset Current			3.0	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2.0		MΩ
Supply Current	V_S = ±15 V		1.8	3.0	mA
Large Signal Voltage Gain	V_S = ±15 V V_{OUT} = ±10 V, R_L ≥ 2 kΩ	25	160		V/mV
The following specifications apply for 0°C ≤ TA ≤ 70°C					
Input Offset Voltage	R_S ≤ 50 kΩ			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ 70°C		0.01	0.3	nA/°C
	0°C ≤ T_A ≤ 25°C		0.02	0.6	nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V R_L ≥ 2 kΩ	15			V/mV
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±12	±14		V
	V_S = ±15 V, R_L = 2 kΩ	± 10	±13		V
Input Voltage Range	V_S = ±15 V	±12			V
Common Mode Rejection Ratio	R_S ≤ 50 kΩ	70	90		dB
Supply Voltage Rejection Ratio	R_S ≤ 50 kΩ	70	96		dB

GUARANTEED PERFORMANCE CURVES FOR μA107 AND μA207

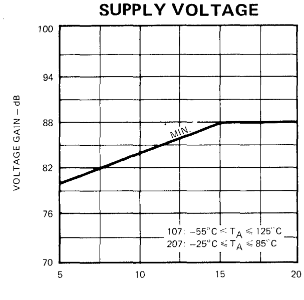
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

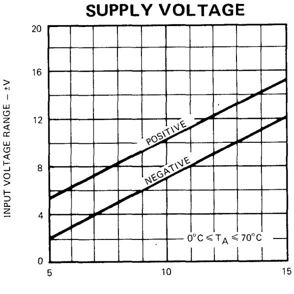


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

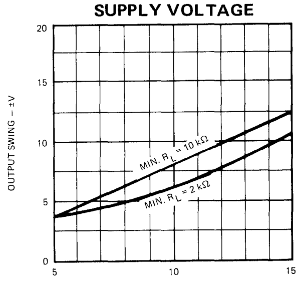


GUARANTEED PERFORMANCE CURVES FOR μA307

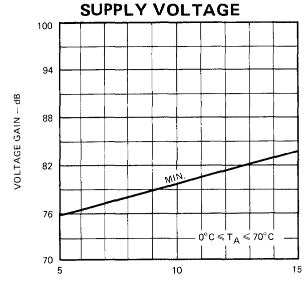
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

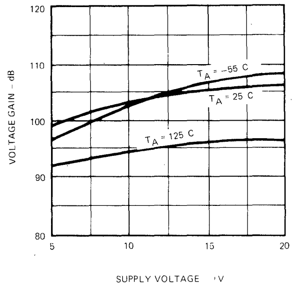


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

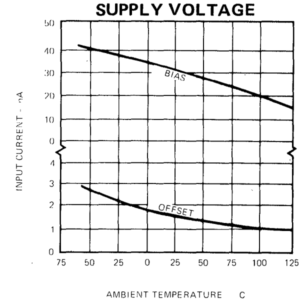


TYPICAL PERFORMANCE CURVES FOR μA107 AND μA207

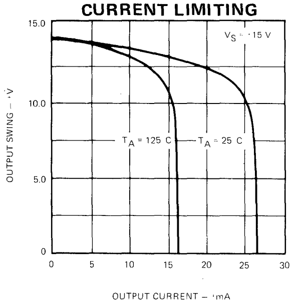
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



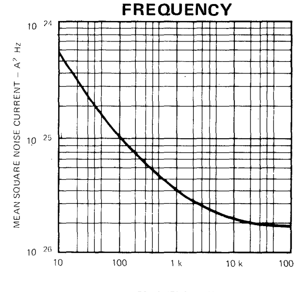
INPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



CURRENT LIMITING

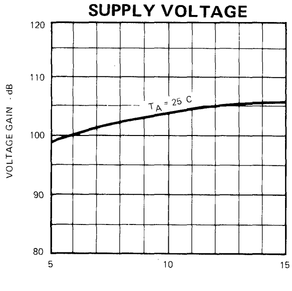


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

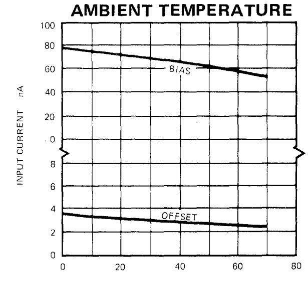


TYPICAL PERFORMANCE CURVES FOR μA307

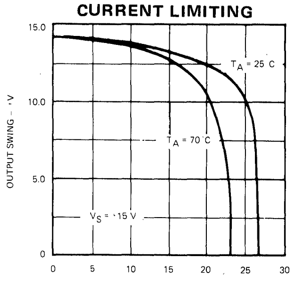
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



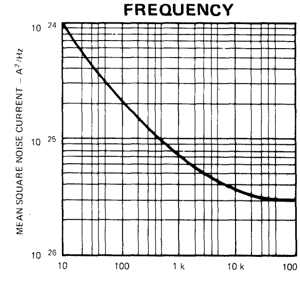
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



CURRENT LIMITING

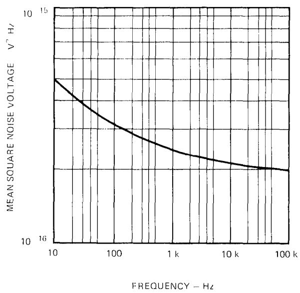


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

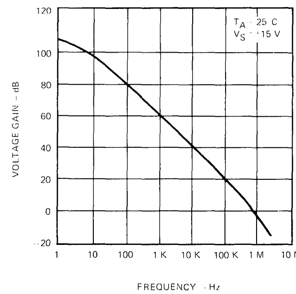


TYPICAL PERFORMANCE CURVES

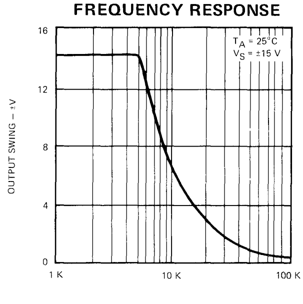
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



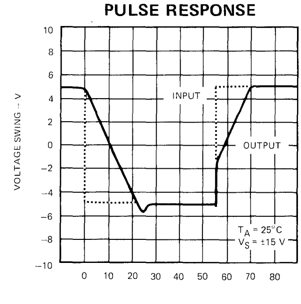
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



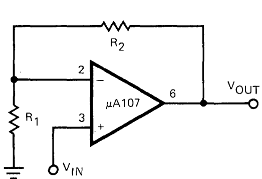
VOLTAGE FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

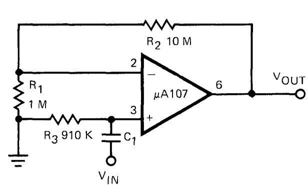
(All pin numbers shown refer to 8-pin TO-5 package)

NON-INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

NON-INVERTING AC AMPLIFIER

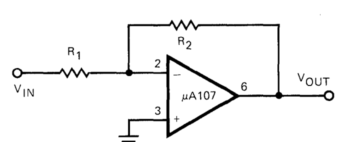


$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

$$R_{IN} = R_3$$

$$R_3 = R_1 R_2$$

INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_2}{R_1} V_{IN}$$

$$R_{IN} = R_1$$

μA108A • μA208A • μA308A
μA108 • μA208 • μA308
SUPER BETA OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

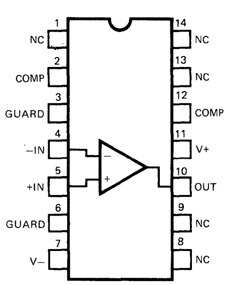
GENERAL DESCRIPTION — The μA108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. High input impedance, low noise, low input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT OFFSET CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT**
- **LOW BIAS CURRENT**
- **OPERATION OVER WIDE SUPPLY RANGE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA108A, μA108, μA208A, μA208	±20 V
μA308A, μA308	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	600 mW
Flatpak	570 mW
Mini DIP	310 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (μA108A, μA108)	-55°C to +125°C
Industrial (μA208A, μA208)	-25°C to +85°C
Commercial (μA308A, μA308)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C
Output Short-Circuit Duration (Note 4)	Indefinite

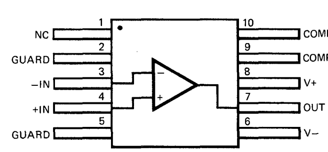
14-PIN DIP**
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108ADM
μA108	μA108DM
μA208A	μA208ADM
μA208	μ208DM
μA308A	μA308ADC
μA308	μA308DC

10-PIN FLATPAK**
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

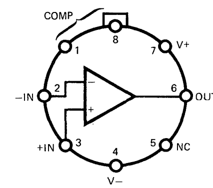


ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AFM
μA108	μA108FM
μA208A	μA208AFM
μA208	μA208FM

** Available on special order

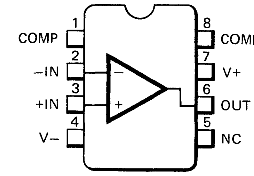
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AHM
μA108	μA108HM
μA208A	μA208AHM
μA208	μA208HM
μA308A	μA308AHC
μA308	μA308HC

CONNECTION DIAGRAMS
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



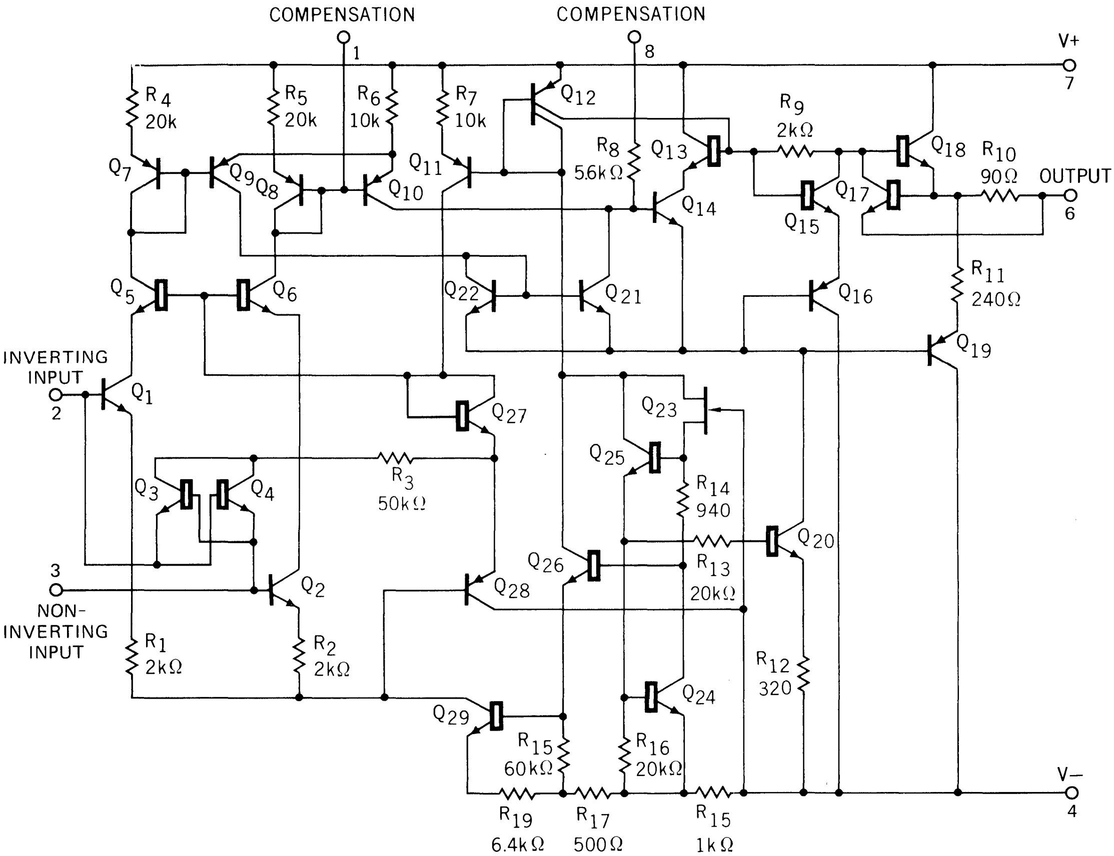
ORDER INFORMATION

TYPE	PART NO.
μA308A	μA308ATC
μA308	μA308TC

See notes on following pages.

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



Pin numbers are for metal can only

μA108A and μA208A

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±20 V, T_A = 25°C, C_C = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	V_S = ±15 V		0.3	0.6	mA
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	80,000	300,000		V/V
The following specifications apply for −55°C ≤ T_A ≤ +125°C (Note 5)					
Input Offset Voltage				1.0	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current			0.8	3.0	nA
Supply Current	T_A = +125°C		0.15	0.4	mA
Input Voltage Range	V_S = ±15 V	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ V_{OUT} = ±10 V	40,000			V/V
Output Voltage Swing	V_S = ±15 V, R_L ≥ 10 kΩ	±13	±14		V

μA308A

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	V_S = ±15 V		0.3	0.8	mA
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	80,000	300,000		V/V
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Offset Voltage				0.73	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	V_S = ±15 V	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	60,000			V/V
Output Voltage Swing	V_S = ±15 V, R_L ≥ 10 kΩ	±13	±14		V

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the mini DIP and 7.1 mW/°C for the flatpak.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
5. For the μA208A/208, all temperature specifications apply over -25°C ≤ T_A ≤ 85°C.

μA108 and μA208

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±20 V, T_A = 25°C, C_C = 30 pF unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.7	2.0	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	V_S = ±15 V		0.3	0.6	mA
Large Signal Voltage Gain	R_L ≥ 10 kΩ, V_{OUT} = ±10 V V_S = ±15 V	50,000	300,000		V/V
The following specifications apply for −55°C ≤ T_A ≤ 125°C (Note 5)					
Input Offset Voltage				3.0	mV
Average Input Offset Voltage Drift			3.0	15	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	T_A = +125°C		0.15	0.4	mA
Input Voltage Range	V_S = ±15 V	±13.5			V
Common Mode Rejection Ratio		85	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±13	±14		V

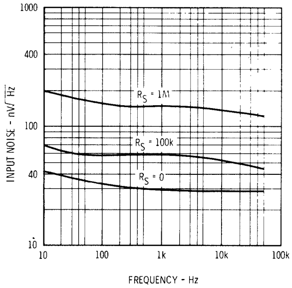
μA308

ELECTRICAL CHARACTERISTICS: ±5.0 V ≤ V_S ≤ ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified.

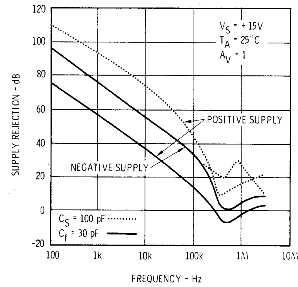
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	V_S = ±15 V		0.3	0.8	mA
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	25,000	300,000		V/V
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Offset Voltage				10	mV
Average Input Offset Voltage Drift			6.0	30	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	V_S = ±15 V	±13.5			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	V_S = ±15 V, R_L ≥ 10 kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±13	±14		V

TYPICAL PERFORMANCE CURVES FOR μA108 SERIES

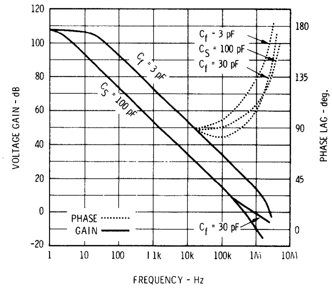
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



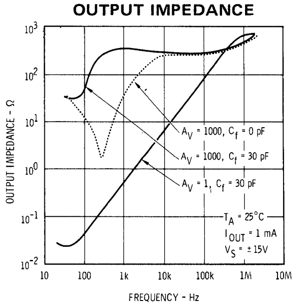
POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY



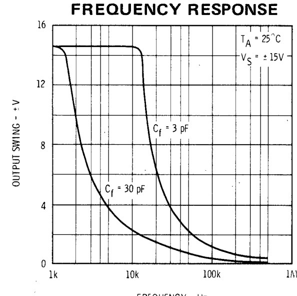
OPEN LOOP FREQUENCY RESPONSE



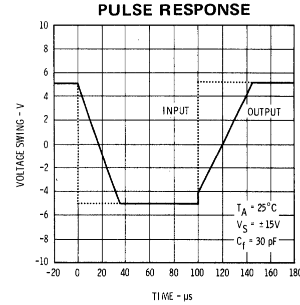
CLOSED LOOP OUTPUT IMPEDANCE



LARGE SIGNAL FREQUENCY RESPONSE

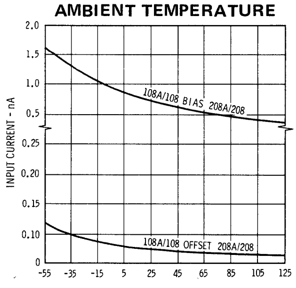


VOLTAGE FOLLOWER PULSE RESPONSE

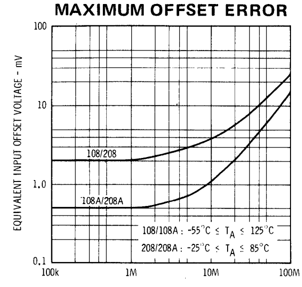


TYPICAL PERFORMANCE CURVES FOR μA108A • μA208A • μA108 • μA208 (Unless Otherwise Specified)

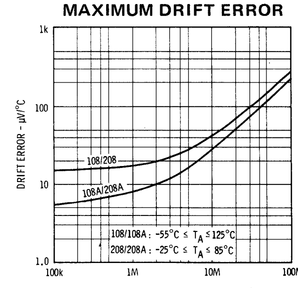
INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



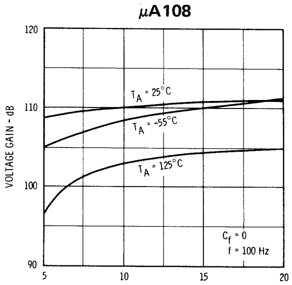
MAXIMUM OFFSET ERROR



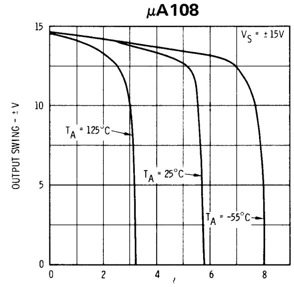
MAXIMUM DRIFT ERROR



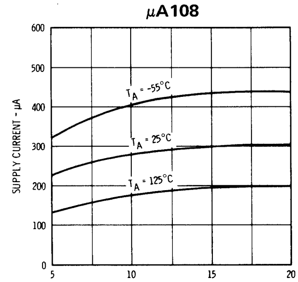
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE μA108



OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT μA108

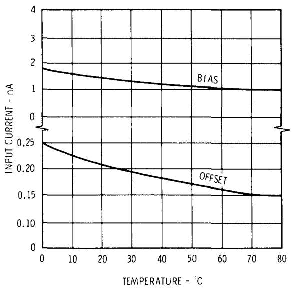


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE μA108

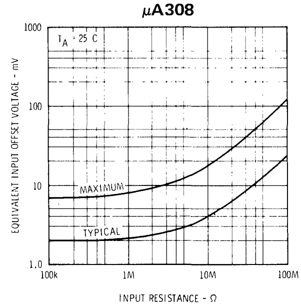


TYPICAL PERFORMANCE CURVES FOR μA308A AND μA308 (Unless Otherwise Specified)

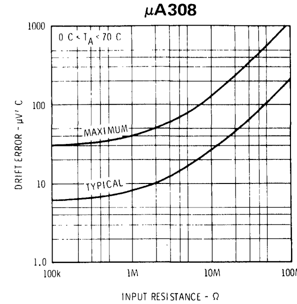
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



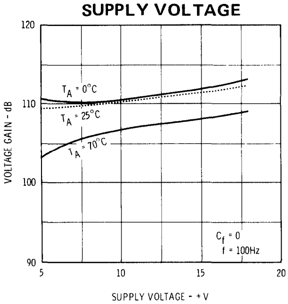
MAXIMUM OFFSET ERROR μA308



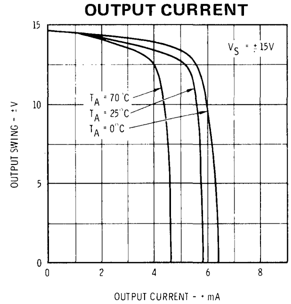
MAXIMUM DRIFT ERROR μA308



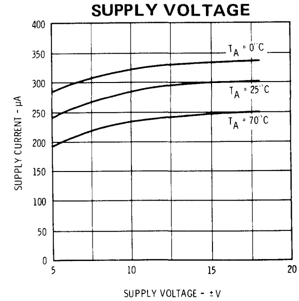
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



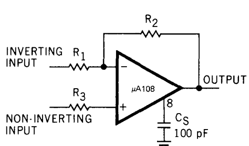
OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT

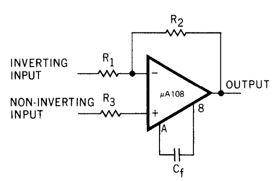


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



STANDARD COMPENSATION CIRCUITS

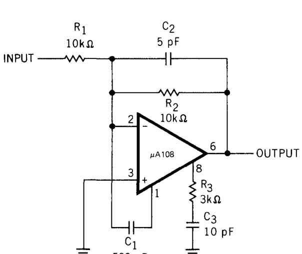




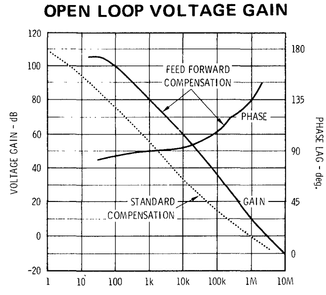
$$C_f \geq 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

FEEDFORWARD COMPENSATION HIGHER SLEW RATES AND WIDER BANDWIDTH

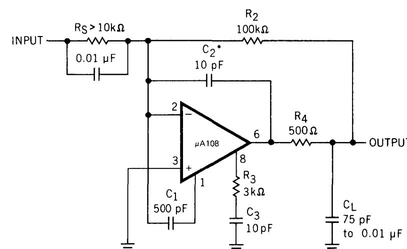
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



$^*C_2 > \frac{5 \times 10^5}{R_2}$ pF

GUARDING

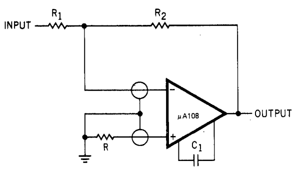
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the μA108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-pin TO-99 package is accomplished by using a 10-pin pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard μA741 and μA101A pin configuration).

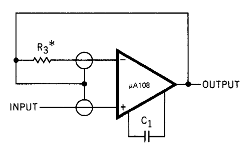
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



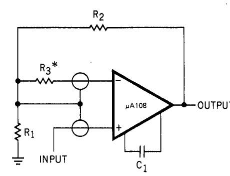
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



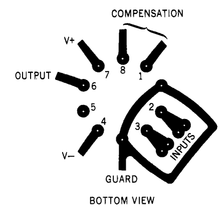
* Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER



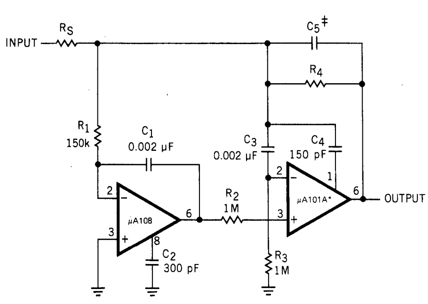
NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO–99 PACKAGE (BOTTOM VIEW)



TYPICAL APPLICATIONS

FAST† SUMMING AMPLIFIER WITH LOW INPUT CURRENT

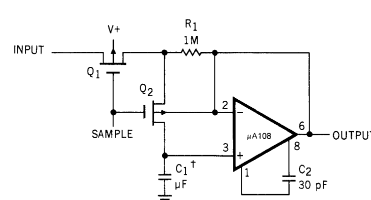


*In addition to increasing speed, the μA101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

$$\ddagger C_5 = \frac{6 \times 10^{-8}}{R_1}$$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s

† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

μA124 • μA224 • μA324 • μA2902

QUAD OPERATIONAL AMPLIFIERS

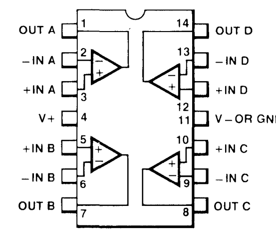
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA124 series of Quad Operational Amplifiers consists of four independent high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar* epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **FOUR INTERNALLY COMPENSATED OPERATIONAL AMPLIFIERS IN A SINGLE PACKAGE**
- **WIDE POWER SUPPLY RANGE: SINGLE OF 3.0 V TO 30 V**
  DUAL SUPPLY OF ±1.5 V to ±16 V
- **POWER DRAIN SUITABLE FOR BATTERY OPERATION**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



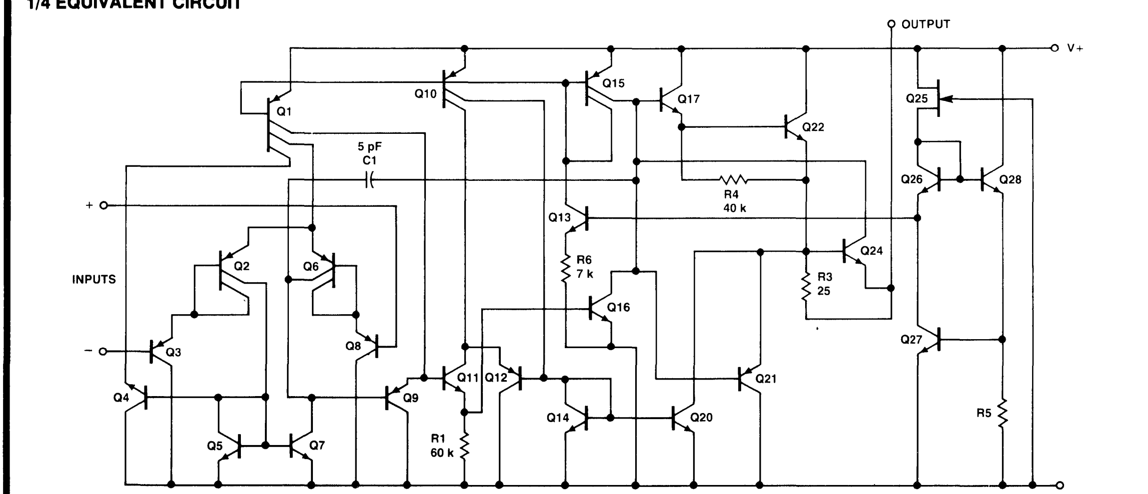
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V–		32
Differential Input Voltage (Note 1)		32
Input Voltage (V–) (Note 1)		–0.3V (V–) to V+
Internal Power Dissipation (Note 2)		670 mW
Operating Temperature Range –	μA124	–55°C to +125°C
	μA224	–25°C to +85°C
	μA324	0°C to +70°C
	μA2902	–40°C to +85°C
Storage Temperature Range		
Molded Package		–55°C to +125°C
Hermetic Package		–65°C to +150°C
Pin Temperature		
Molded Package (Soldering, 10 s)		260°C
Hermetic Package (Soldering, 60 s)		300°C

ORDER INFORMATION

TYPE	PART NO.
μA124	μA124DM
μA224	μA224DM
μA324	μA324DC
μA324	μA324PC
μA2902	μA2902PC

1/4 EQUIVALENT CIRCUIT



μA124 • μA224

ELECTRICAL CHARACTERISTICS: V+ = 5.0 Vdc, T_A = 25°C unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		(Note 5)		2.0	5.0	mV
Input Offset Current				3.0	30	nA
Input Bias Current				−45	−150	nA
Input Common Mode Voltage Range			0		V+ −1.5 V	V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	85		dB
Large Signal Open Loop Voltage Gain		V+ = +15 V, R_L = 2 kΩ	50	100		V/mV
Output Current	Source	$V_{IN}+$ = +1 Vdc, $V_{IN}-$ = 0 V+ = +15 V	20	40		mA
	Sink	$V_{IN}-$ = +1 Vdc $V_{IN}+$ = 0 V+ = +15 Vdc	10	20		mA
	Sink	$V_{IN}-$ = +1 Vdc, $V_{IN}+$ = 0 V_{OUT} = 200 mV	12	50		μA
Power Supply Rejection Ratio			65	100		dB
Channel Separation		f = 1 kHz to 20 kHz		−120		dB
Short Circuit Current		To ground		40	60	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C for μA124 and −25°C to +85°C for μA224						
Input Offset Voltage		(Note 5)			7	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 0		7		μV/°C
Input Offset Current					±100	nA
Average Temperature Coefficient of Input Offset Current				10		pA/°C
Input Bias Current				−40	−300	nA
Large Signal Open Loop Voltage Gain		R_L = 2 kΩ, V+ = +15 V	25			V/mV
Output Voltage Range	V_{OH}	V+ = +30 Vdc, R_L = 2 kΩ	26			V
	V_{OH}	V+ = +30 Vdc, $R_L \geq 10$ kΩ	27	28		V
	V_{OL}	V+ = 5 Vdc, $R_L \leq 10$ kΩ		5	20	mV
Input Common Mode Voltage Range		V+ = +30 Vdc	0		V+ −2.0	V
Output Current	Source	$V_{IN}+$ = +1 V $V_{IN}-$ = 0, V+ = 15 V	10	20		mA
	Sink	$V_{IN}-$ = +1 V $V_{IN}+$ = 0, V+ = 15 V	5	8		mA
Differential Input Voltage					V+	V
Supply Current		R_L = ∞, V_{CC} = 30 V		1.5	3.0	mA
		R_L = ∞, V_{CC} = +5 V		0.7	1.2	mA

NOTES:

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. V_{OUT} = 1.4 Vdc, R_S = 0 Ω with V+ from 5 Vdc to +30 Vdc; and over the full input common mode range (0 to V+ − 2.0 Vdc) except at 25°C, where common mode range is 0 Vdc to V+ − 1.5 Vdc.

μA324

ELECTRICAL CHARACTERISTICS: V+ = 5.0 Vdc, T_A = 25°C unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		(Note 5)		2.0	7.0	mV
Input Offset Current				5.0	50	nA
Input Bias Current				−45	−250	nA
Input Common Mode Voltage Range			0		V+ −1.5 V	V
Common Mode Rejection Ratio		R_S ≤ 10 kΩ	65	70		dB
Large Signal Open Loop Voltage Gain		V+ = +15 V, R_L = 2 kΩ	25	100		V/mV
Output Current	Source	$V_{IN}+$ = +1 Vdc, $V_{IN}-$ = 0, V+ = +15 V	20	40		mA
	Sink	$V_{IN}-$ = +1 Vdc, $V_{IN}+$ = 0, V+ = +15 Vdc	10	20		mA
	Sink	$V_{IN}-$ = +1 Vdc, $V_{IN}+$ = 0, V_{OUT} = 200 mV	12	50		μA
Power Supply Rejection Ratio			65	100		dB
Channel Separation		f = 1 kHz to 20 kHz		−120		dB
Short Circuit Current		To ground		40	60	mA
The following specifications apply for 0°C to +70°C						
Input Offset Voltage		(Note 5)			9	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 0		7		μV/°C
Input Offset Current				±100	±150	nA
Average Temperature Coefficient of Input Offset Current				10		pA/°C
Input Bias Current				−40	−500	nA
Large Signal Open Loop Voltage Gain		R_L = 2 kΩ, V+ = +15 V	15			V/mV
Output Voltage Range	V_{OH}	V+ = +30 Vdc, R_L = 2 kΩ	26			V
	V_{OH}	V+ = +30 Vdc, R_L ≥ 10 kΩ	27	28		V
	V_{OL}	V+ = 5 Vdc, R_L ≤ 10 kΩ		5	20	mV
Input Common Mode Voltage Range		V+ = +30 Vdc	0		V+ −2.0	V
Output Current	Source	$V_{IN}+$ = +1 V, $V_{IN}-$ = 0, V+ = 15 V	10	20		mA
	Sink	$V_{IN}-$ = +1 V, $V_{IN}+$ = 0, V+ = 15 V	5	8		mA
Differential Input Voltage					V+	V
Supply Current		R_L = ∞, V_{CC} = 30 V		1.5	3.0	mA
		R_L = ∞, V_{CC} = +5 V		0.7	1.2	mA

NOTES:
1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. V_{OUT} = 1.4 Vdc, R_S = 0 Ω with V+ from 5 Vdc to +30 Vdc; and over the full input common mode range (0 to V+ − 2.0 Vdc) except at 25°C, where common mode range is 0 Vdc to V+ − 1.5 Vdc.

μA2902

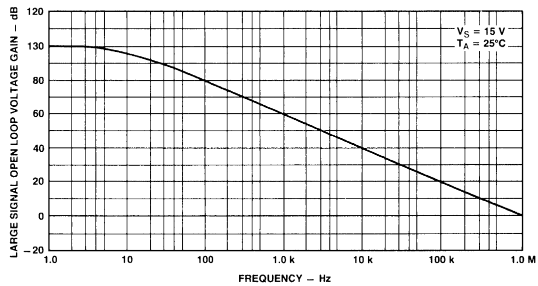
ELECTRICAL CHARACTERISTICS: V+ = 5.0 Vdc, T_A = 25°C unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		(Note 5)		2.0	7.0	mV
Input Offset Current				5.0	50	nA
Input Bias Current				−45	−250	nA
Input Common Mode Voltage Range			0		V+ −1.5 V	V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	50	70		dB
Large Signal Open Loop Voltage Gain		V+ = +15 V, R_L = 2 kΩ		100		V/mV
Output Current	Source	$V_{IN}+$ = +1 Vdc, $V_{IN}-$ = 0 V+ = +15 V	20	40		mA
	Sink	$V_{IN}-$ = +1 Vdc $V_{IN}+$ = 0 V+ = +15 Vdc	10	20		mA
Power Supply Current		$R_L = \infty$			3.0	mA
Power Supply Rejection Ratio			50	100		dB
Short Circuit Current		To ground		40	60	mA
Channel Separation		f = 1 kHz to 20 kHz		−120		dB
The following specifications apply for −40°C to +85°C						
Input Offset Voltage		(Note 5)			10	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 0		7		μV/°C
Input Offset Current				±45	±200	nA
Average Temperature Coefficient of Input Offset Current				10		pA/°C
Input Bias Current				−40	−500	nA
Large Signal Open Loop Voltage Gain		R_L = 2 kΩ, V+ = +15 V	15			V/mV
Output Voltage Range	V_{OH}	V+ = +30 Vdc, R_L = 2 kΩ	22			V
	V_{OH}	V+ = +30 Vdc, $R_L \geq 10$ kΩ	23	24		V
	V_{OL}	V+ = 5 Vdc, $R_L \leq 10$ kΩ		5	100	mV
Input Common Mode Voltage Range		V+ = +30 Vdc	0		V+ −2.0	V
Output Current	Source	$V_{IN}+$ = +1 V $V_{IN}-$ = 0, V+ = 15 V	10	20		mA
	Sink	$V_{IN}-$ = +1 V $V_{IN}+$ = 0, V+ = 15 V	5	8		mA
Differential Input Voltage					V+	V

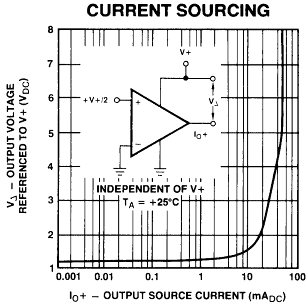
NOTES:
1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. V_{OUT} = 1.4 Vdc, R_S = 0 Ω with V+ from 5 Vdc to +30 Vdc; and over the full input common mode range (0 to V+ − 2.0 Vdc) except at 25°C, where common mode range is 0 Vdc to V+ − 1.5 Vdc.

TYPICAL PERFORMANCE CURVES

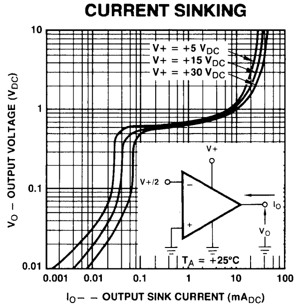
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



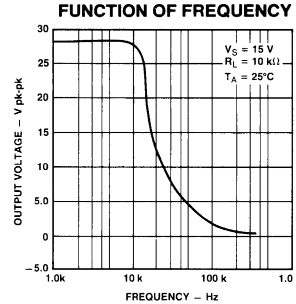
OUTPUT CHARACTERISTICS CURRENT SOURCING



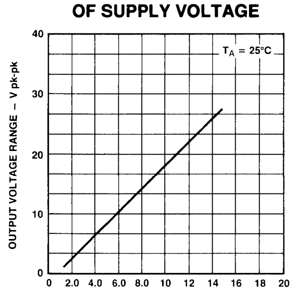
OUTPUT CHARACTERISTICS CURRENT SINKING



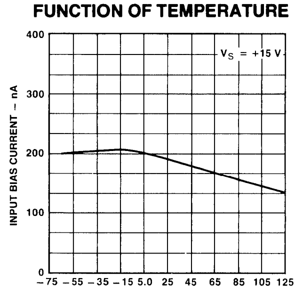
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



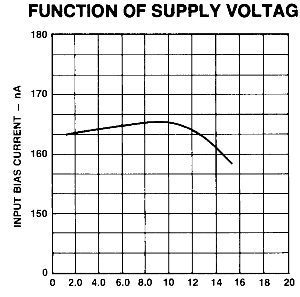
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



5

μA148 • μA248 • μA348
μA149 • μA249 • μA349
QUAD OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

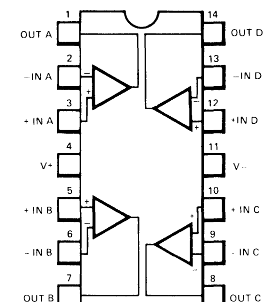
GENERAL DESCRIPTION — The μA148 series is a true quad μA741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar μA741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single μA741 type op amp.

Other features include input offset currents and input bias current which are much less than those of a standard μA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The μA149 series has the same features as the μA148 except that it is decompensated to give a gain bandwidth product of 4 MHz typical at a gain greater than 5.

- **μA741 OP AMP OPERATING CHARACTERISTICS**
- **LOW SUPPLY CURRENT DRAIN**
- **CLASS AB OUTPUT STAGE - NO CROSSOVER DISTORTION**
- **PIN COMPATIBLE WITH THE μA324 & μA3403**
- **LOW INPUT OFFSET VOLTAGE — 1 mV TYP**
- **LOW INPUT OFFSET CURRENT — 4 nA TYP**
- **LOW INPUT BIAS CURRENT — 30 nA TYP**
- **GAIN BANDWIDTH PRODUCT**
  μA148 (UNITY GAIN) — 1.0 MHz TYP
  μA149 (AV>5) — 4 MHz TYP
- **HIGH DEGREE OF ISOLATION BETWEEN AMPLIFIERS — 120 dB**
- **OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA148	μA148DM
μA248	μA248DC
μA248	μA248PC
μA348	μA348DC
μA348	μA348PC
μA149	μA149DM
μA249	μA249DC
μA249	μA249PC
μA349	μA349DC
μA349	μA349PC

ABSOLUTE MAXIMUM RATINGS

		μA148/μA149	μA248/μA249	μA348/μA349
Supply Voltage		±22 V	±18 V	±18 V
Differential Input Voltage		±44 V	±36 V	±36 V
Input Voltage		±22 V	±18 V	±18 V
Output Short Circuit Duration (Note 1)		continuous	continuous	continuous
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{JA}), (Note 2)				
Plastic DIP	P_D	--	--	700 mW
	θ_{JA}	--	--	150°C/W
Ceramic DIP	P_D	670 mW	670 mW	670 mW
	θ_{JA}	100°C/W	100°C/W	100°C/W
Operating Temperature Range		$-55°C<T_A<+125°C$	$-25°C<T_A<+85°C$	$0°C<T_A<+70°C$
Storage Temperature Range		-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Pin Temperature				
Molded Package (Soldering, 10 s)			260°C	260°C
Hermetic Package (Soldering, 60 s)		300°C	300°C	300°C

DC ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted

CHARACTERISTIC	CONDITIONS	μA148/μA149			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	Rs ≤ 10 kΩ		1.0	5.0	mV
Input Offset Current			4	25	nA
Input Bias Current			30	100	nA
Input Resistance		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	3.6	mA
Large Signal Voltage Gain	V_{OUT} = ±10 V, R_L ≥ 2 kΩ	50	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred)		−120		dB
Output Short Circuit Current			25		mA
The following specification apply for −55°C ≤ T_A ≤ +125°C					
Input Offset Voltage	Rs ≤ 10 kΩ			6.0	mV
Input Offset Current				75	nA
Input Bias Current				325	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10 V	25			V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±13		V
	R_L = 2 kΩ	±10	±12		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	Rs ≤ 10 kΩ	70	90		dB
Supply Voltage Rejection	Rs ≤ 10 kΩ	77	96		dB

AC CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted

Small Signal Bandwidth	μA148		1.0		MHz
	μA149		4.0		MHz
Phase Margin	μA148 (Av = 1)		60		degrees
	μA149 (Av = 5)		60		degrees
Slew Rate	μA148 (Av = 1)		0.5		V/μs
	μA149 (Av = 5)		2.0		V/μs

NOTES:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{J\,(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,(MAX)} - T_A)/\theta_{JA}$ or the 25°C $P_{D\,(MAX)}$, whichever is less.
3. μA148, 248, 348 are capable of driving 100 pF capacitive load. μA149, 249, 349 are capable of driving 50 pF capacitive load.

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DC ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25^\circ$C unless otherwise noted

CHARACTERISTIC	CONDITIONS	μA248/μA249			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	Rs ≤ 10 kΩ		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	4.5	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L \geq 2$ kΩ	25	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred)		−120		dB
Output Short Circuit Current			25		mA

The following specification apply for $-25^\circ C \leq T_A \leq 85^\circ C$

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Rs ≤ 10 kΩ			7.5	mV
Input Offset Current				125	nA
Input Bias Current				500	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15			V/mV
Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
	$R_L = 2$ kΩ	±10	±12		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	Rs ≤ 10 kΩ	70	90		dB
Supply Voltage Rejection	Rs ≤ 10 kΩ	77	96		dB

AC CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25^\circ$C unless otherwise noted

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
Small Signal Bandwidth	μA248		1.0		MHz
	μA249		4.0		MHz
Phase Margin	μA248 (Av = 1)		60		degrees
	μA249 (Av = 5)		60		degrees
Slew Rate	μA248 (Av = 1)		0.5		V/μs
	μA249 (Av = 5)		2.0		V/μs

NOTES:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{J\,(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,(MAX)} - T_A)/\theta_{JA}$ or the 25° C $P_{D\,(MAX)}$, whichever is less.
3. μA148, 248, 348 are capable of driving 100 pF capacitive load. μA149, 249, 349 are capable of driving 50 pF capacitive load.

DC ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted

CHARACTERISTIC	CONDITIONS	μA348/μA349			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	Rs≤10 kΩ		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	4.5	mA
Large Signal Voltage Gain	V_{OUT} = ±10 V, R_L≥2 kΩ	25	160		V/mV
Amplifier to Amplifier	f = 1 Hz to 20 kHz (Input Referred)		−120		dB
Output Short Circuit Current			25		mA
The following specification apply for 0°C≤T_A≤70°C					
Input Offset Voltage	Rs≤10 kΩ			7.5	mV
Input Offset Current				100	nA
Input Bias Current				400	nA
Large Signal Voltage Gain	R_L≥2 k , V_{OUT} = ±10 V	15			V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±13		V
	R_L = 2 kΩ	±10	±12		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	Rs≤10 kΩ	70	90		dB
Supply Voltage Rejection	Rs≤10 kΩ	77	96		dB

AC CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted

Small Signal Bandwidth	μA348		1.0		MHz
	μA349		4.0		MHz
Phase Margin	μA348 (Av = 1)		60		degrees
	μA349 (Av = 5)		60		degrees
Slew Rate	μA348 (Av = 1)		0.5		V/μs
	μA349 (Av = 5)		2.0		V/μs

NOTES:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{J\,(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,(MAX)} - T_A)/\theta_{JA}$ or the 25°C $P_{D\,(MAX)}$, whichever is less.
3. μA148, 248, 348 are capable of driving 100 pF capacitive load. μA149, 249, 349 are capable of driving 50 pF capacitive load.

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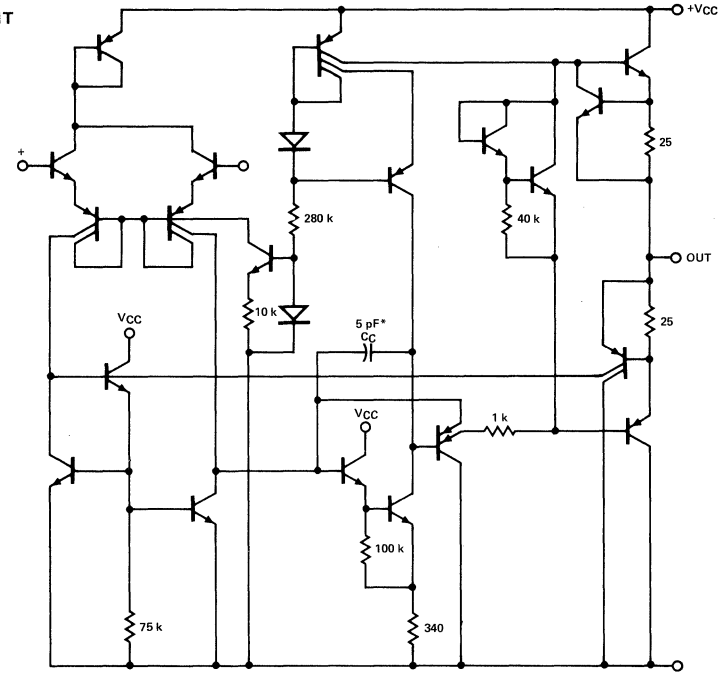
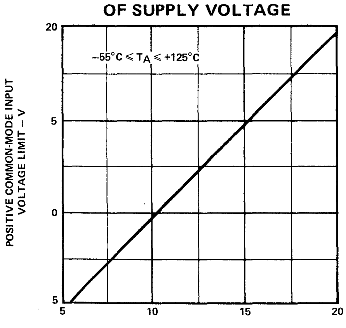
¼ EQUIVALENT CIRCUIT



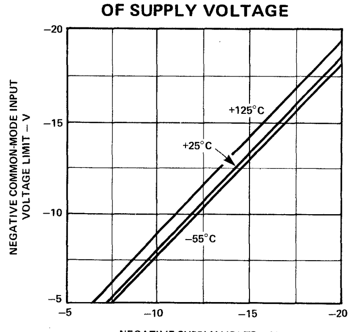
* 1 pF on the μA149

TYPICAL PERFORMANCE CURVES

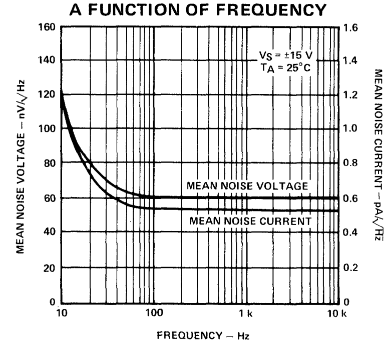
POSITIVE COMMON MODE INPUT VOLTAGE LIMIT AS A FUNCTION OF SUPPLY VOLTAGE



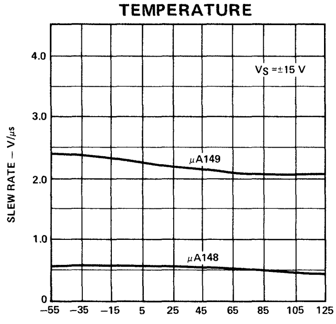
NEGATIVE COMMON MODE INPUT VOLTAGE LIMIT AS A FUNCTION OF SUPPLY VOLTAGE



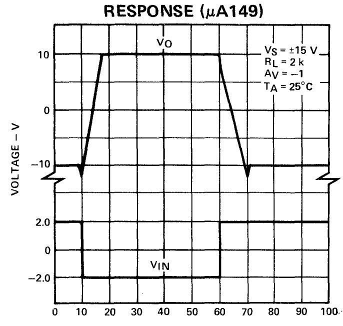
INPUT NOISE VOLTAGE AND NOISE CURRENT AS A FUNCTION OF FREQUENCY



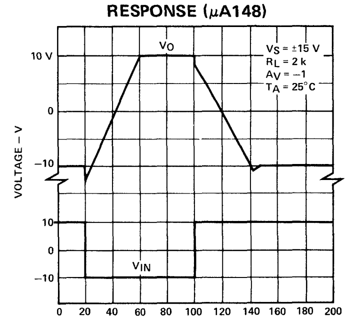
SLEW RATE AS A FUNCTION OF TEMPERATURE



INVERTING LARGE SIGNAL PULSE RESPONSE (μA149)

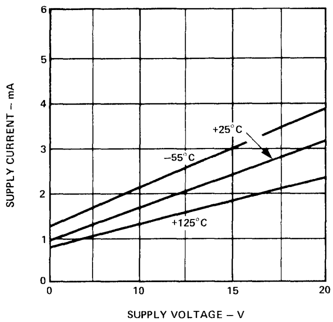


INVERTING LARGE SIGNAL PULSE RESPONSE (μA148)

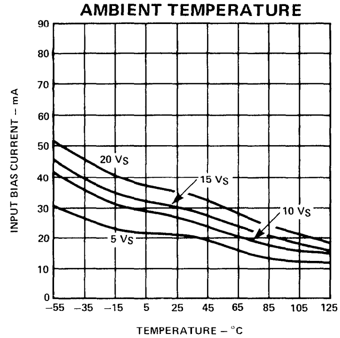


TYPICAL PERFORMANCE CURVES (Cont'd)

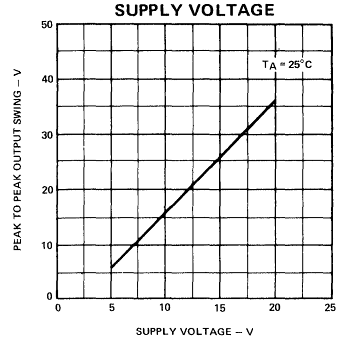
SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



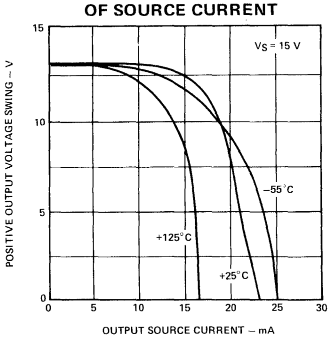
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



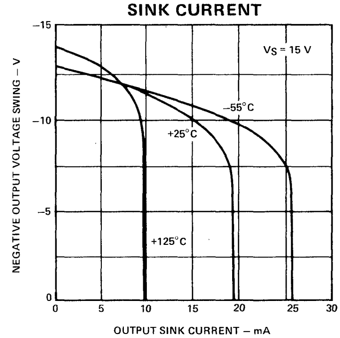
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



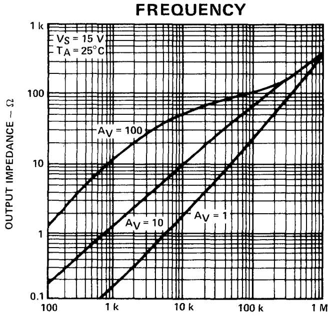
OUTPUT VOLTAGE AS A FUNCTION OF SOURCE CURRENT



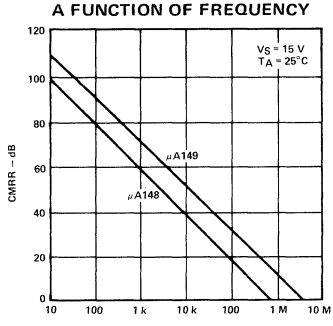
OUTPUT VOLTAGE AS A FUNCTION OF SINK CURRENT



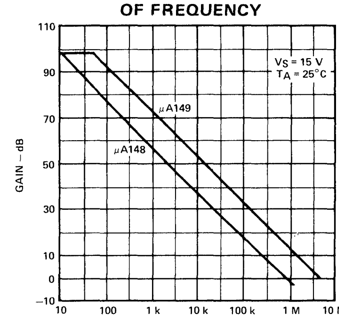
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OPEN LOOP FREQUENCY RESPONSE AS A FUNCTION OF FREQUENCY



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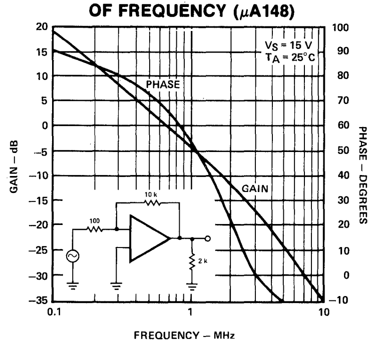
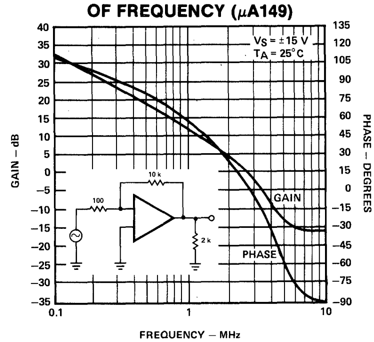
TYPICAL PERFORMANCE CURVES (Cont'd)

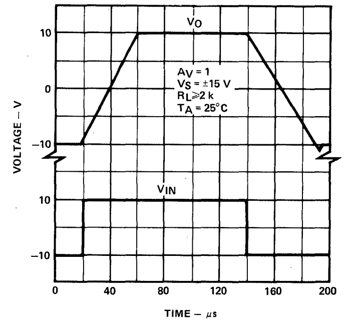
GAIN AS A FUNCTION OF FREQUENCY (μA148)



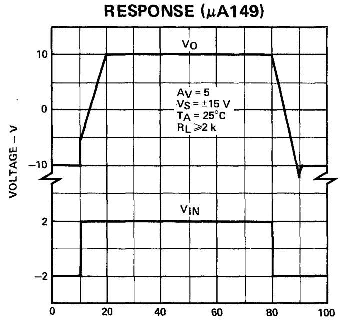
GAIN AS A FUNCTION OF FREQUENCY (μA149)



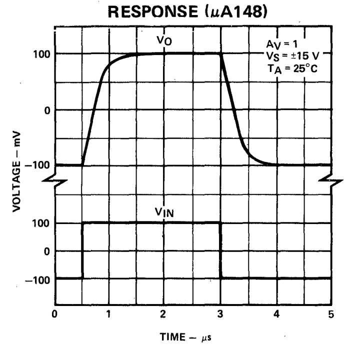
LARGE SIGNAL PULSE RESPONSE (μA148)



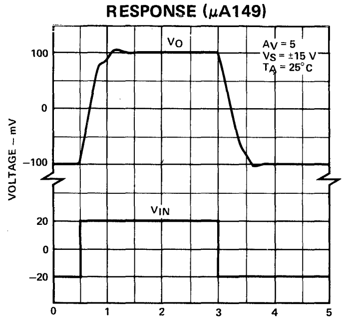
LARGE SIGNAL PULSE RESPONSE (μA149)



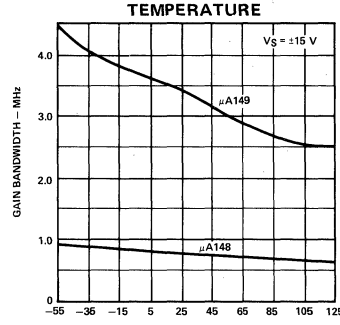
SMALL SIGNAL PULSE RESPONSE (μA148)



SMALL SIGNAL PULSE RESPONSE (μA149)



GAIN BANDWIDTH AS A FUNCTION OF TEMPERATURE



μA318

HIGH-SPEED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

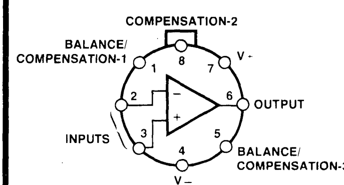
5

ENERAL DESCRIPTION – The μA318 is a precision high-speed operational amplifier esigned for applications requiring wide bandwidth and high slew rate. It features a factor f ten increase in speed over general purpose devices without sacrificing DC performance.

he μA318 has internal unity gain frequency compensation. This simplifies its application nce no external components are necessary for operation. However, unlike most inter-ally compensated amplifiers, external frequency compensation may be added for op-mum performance. For inverting applications, feedforward compensation will boost the ew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be sed with the amplifier for greater stability when maximum bandwidth is not needed. urther, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

he high speed and fast settling time of this op amp makes it useful in A/D converters, scillators, active filters, sample and hold circuits or general purpose amplifiers. This de-ice is easy to apply and offers a better AC performance than industry standards such as e μA709.

CONNECTION DIAGRAM
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

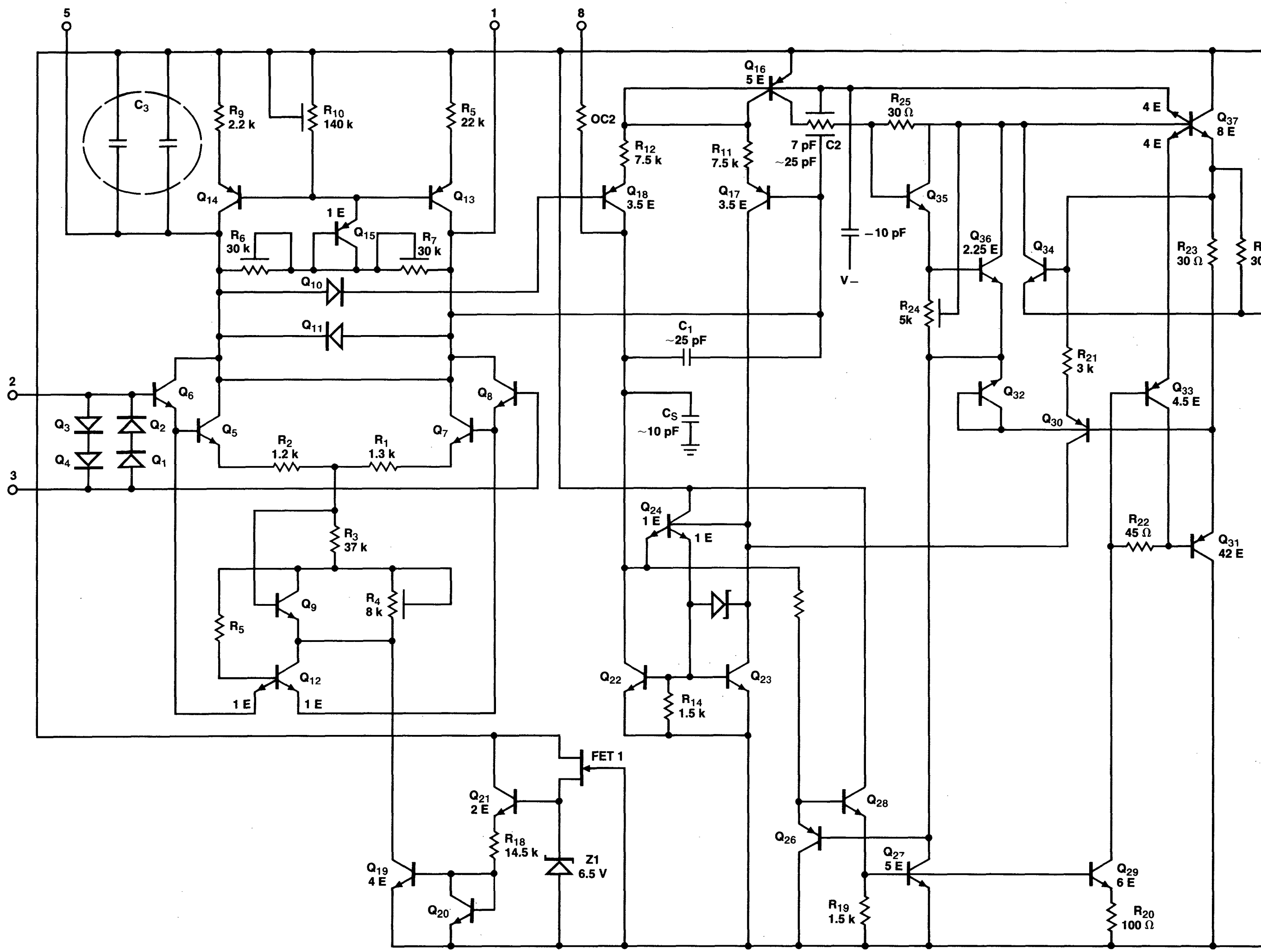
TYPE	PART NO.
μA318	μA318HC

- **15 MHz SMALL SIGNAL BANDWIDTH**
- **GUARANTEED 50 V/μS SLEW RATE**
- **MAXIMUM BIAS CURRENT OF 500 nA**
- **OPERATES FROM SUPPLIES OF ±5 V TO ±20 V**
- **INTERNAL FREQUENCY COMPENSATION**
- **INPUT AND OUTPUT OVERLOAD PROTECTED**
- **PIN COMPATIBLE WITH GENERAL PURPOSE OP AMPS**

BSOLUTE MAXIMUM RATINGS

upply Voltage	±20 V
ower Dissipation (Note 1)	500 mW
ifferential Input Current (Note 2)	±10 mA
put Voltage (Note 3)	±15 V
utput Short-Circuit Duration	Indefinite
perating Temperature Range	0°C to +70°C
torage Temperature Range	−65°C to +150°C
in Temperature (Soldering, 10 s)	300°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: ±5 V ≤ VS ≤ ±20 V, T_A = +25°C

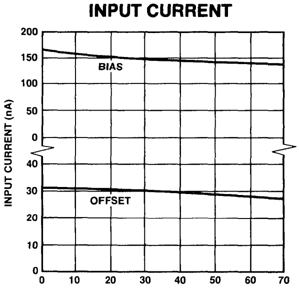
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			4	10	mV
Input Offset Current			30	200	nA
Input Bias Current			150	500	nA
Input Resistance		0.5	3		MΩ
Supply Current			5	10	mA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, R_L ≥ 2 kΩ	25	200		V/mV
Slew Rate	V_S = ±15 V, A_V = 1	50	70		V/μs
Small Signal Bandwidth	V_S = ±15 V		15		MHz
The following specifications apply for 0°C < T_A < +70°C					
Input Offset Voltage				15	mV
Input Offset Current				300	nA
Input Bias Current				750	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, R_L ≥ 2 kΩ	20			V/mV
Output Voltage Swing	V_S = ±15 V, R_L = 2 kΩ	±12	±13		V
Input Voltage Range	V_S = ±15 V	±11.5			V
Common-Mode Rejection Ratio		70	100		dB
Supply Voltage Rejection Ratio		65	80		dB

NOTES:
1. The maximum junction temperature of the μA318 is 150°C for operating at elevated temperatures. The TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

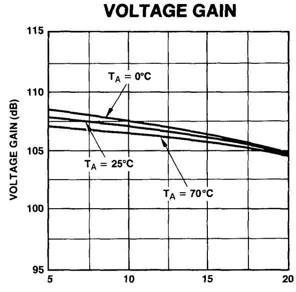
5

TYPICAL PERFORMANCE CHARACTERISTICS

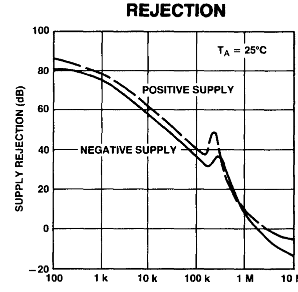
INPUT CURRENT



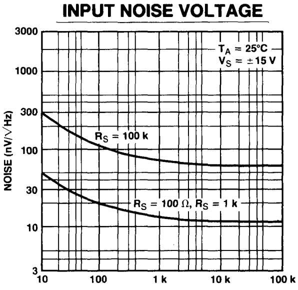
VOLTAGE GAIN



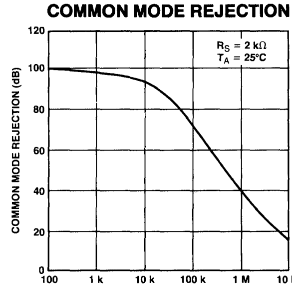
POWER SUPPLY REJECTION



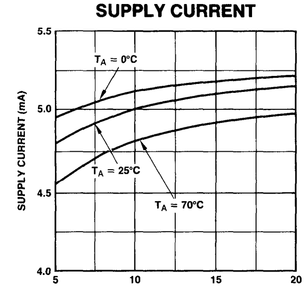
INPUT NOISE VOLTAGE



COMMON MODE REJECTION

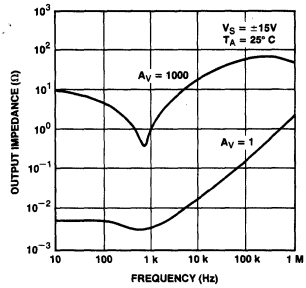


SUPPLY CURRENT

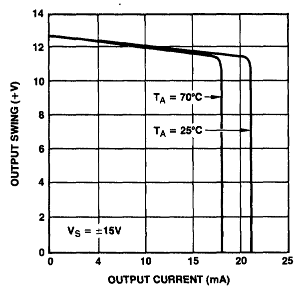


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

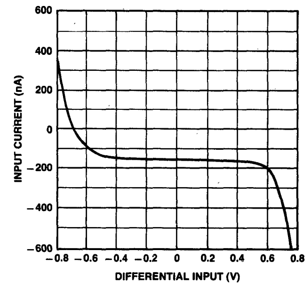
CLOSED LOOP OUTPUT IMPEDANCE



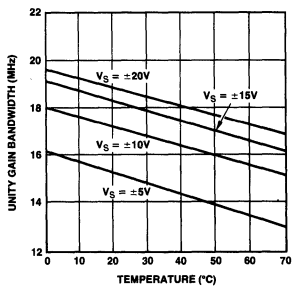
CURRENT LIMITING



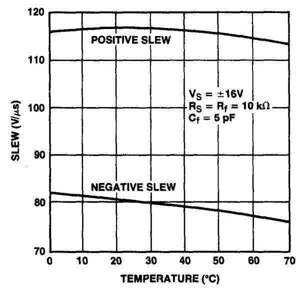
INPUT CURRENT



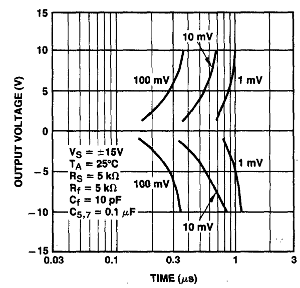
UNIT GAIN BANDWIDTH



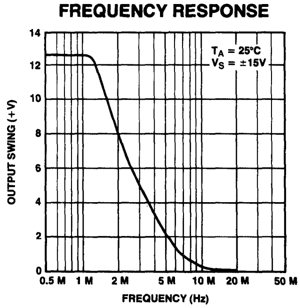
VOLTAGE FOLLOWER SLEW RATE



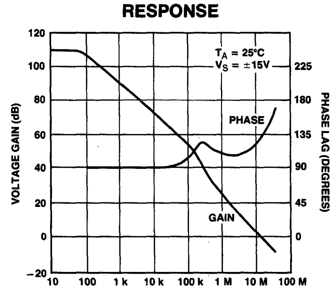
INVERTER SETTLING TIME



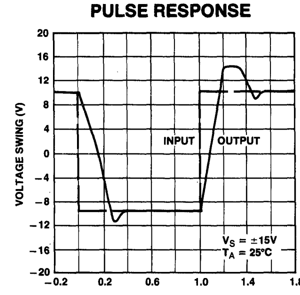
LARGE SIGNAL FREQUENCY RESPONSE



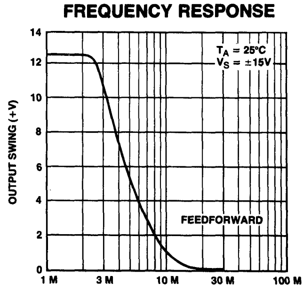
OPEN LOOP FREQUENCY RESPONSE



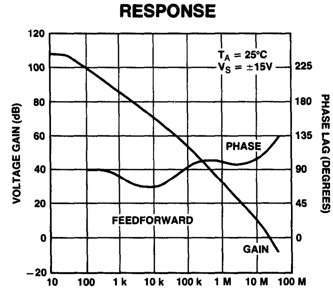
VOLTAGE FOLLOWER PULSE RESPONSE



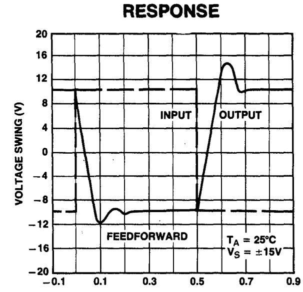
LARGE SIGNAL FREQUENCY RESPONSE



OPEN LOOP FREQUENCY RESPONSE

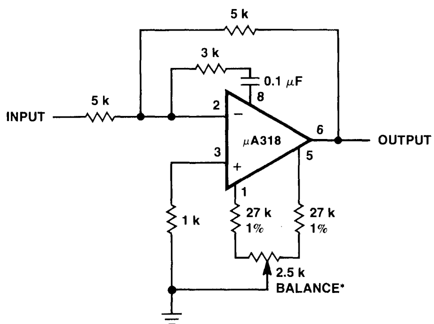


INVERTER PULSE RESPONSE



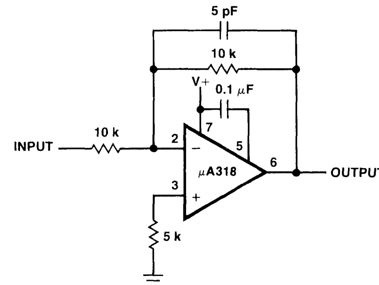
AUXILIARY CIRCUITS

FEEDFORWARD COMPENSATION FOR GREATER INVERTING SLEW RATE†



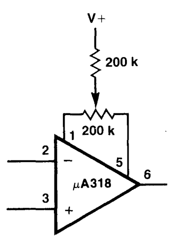
†Slew rate typically 150 V/μs.
*Balance circuit necessary for increased slew.

COMPENSATION FOR MINIMUM SETTLING† TIME

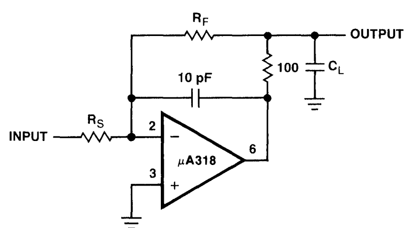


†Slew and settling time to 0.1% for a 10 V step change is 800 ns.

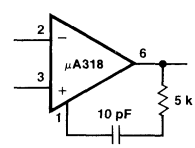
OFFSET BALANCING



ISOLATING LARGE CAPACITIVE LOADS

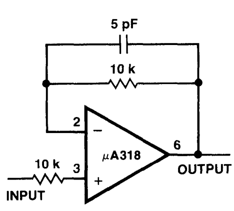


OVERCOMPENSATION

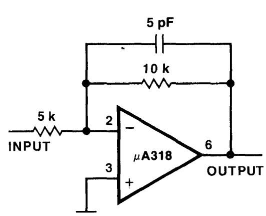


TYPICAL APPLICATIONS

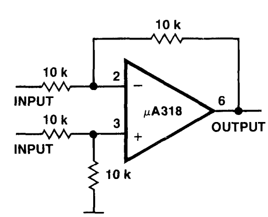
FAST VOLTAGE FOLLOWER



FAST SUMMING AMPLIFIER

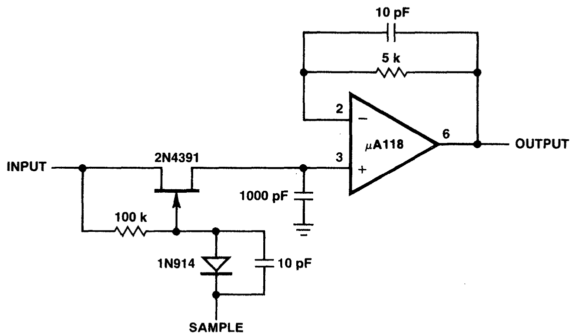


DIFFERENTIAL AMPLIFIER

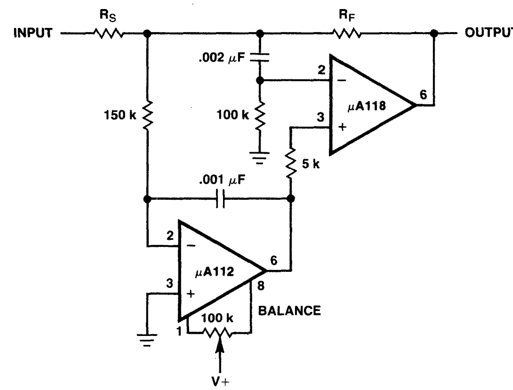


TYPICAL APPLICATIONS (Cont'd.)

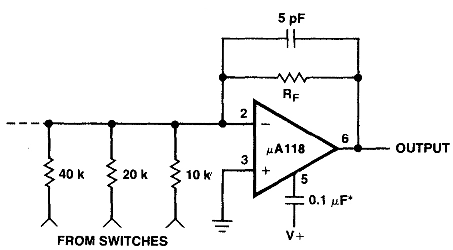
FAST SAMPLE AND HOLD



FAST SUMMING AMPLIFIER WITH LOW INPUT CURRENT

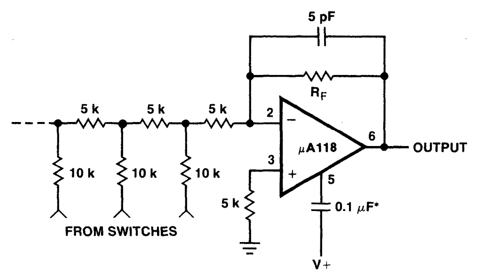


D/A CONVERTER USING BINARY WEIGHTED NETWORK



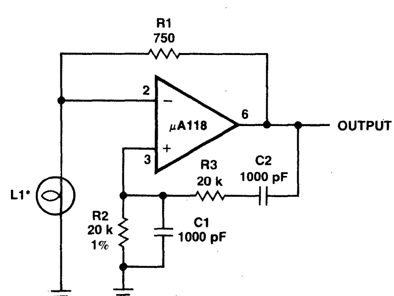
*Optional – Reduces settling time.

D/A CONVERTER USING LADDER NETWORK



*Optional – Reduces settling time.

WEIN BRIDGE SINE WAVE OSCILLATOR



*L1 – 10 V – 14 mA bulb ELDEMA 1869
R1 = R2
C1 = C2

$$f = \frac{1}{2\pi\ R2\ C1}$$

µA702

WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA702 is a monolithic DC Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from dc to 30 MHz.

- **LOW OFFSET VOLTAGE**
- **LOW OFFSET VOLTAGE DRIFT**
- **WIDE BANDWIDTH — 20 MHz TYP**
- **HIGH SLEW RATE — 5 V/µs TYP**

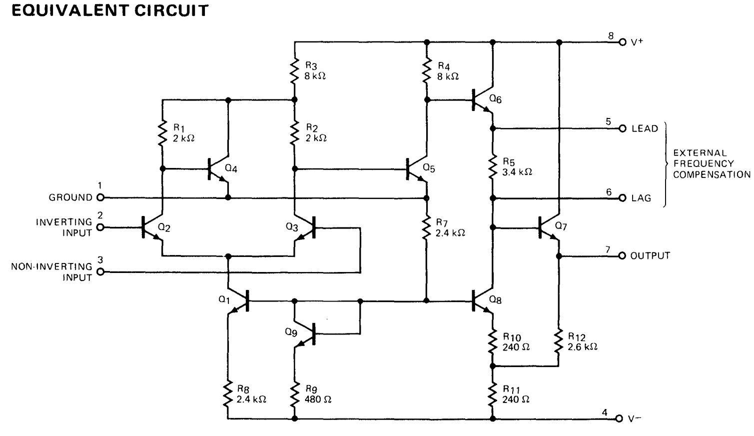
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (µA702)	−55°C to +125°C
Commercial (µA702C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 60 s)	300°C

NOTE

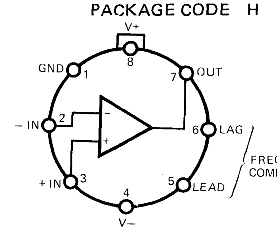
Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP and 7.1 mW/°C for the Flatpak.

EQUIVALENT CIRCUIT



Pin numbers are shown for metal can only.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

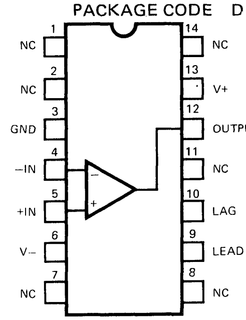


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
µA702	µA702HM
µA702C	µA702HC

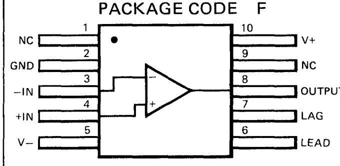
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
µA702	µA702DM
µA702C	µA702DC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
µA702	µA702FM

*Planar is a patented Fairchild process.

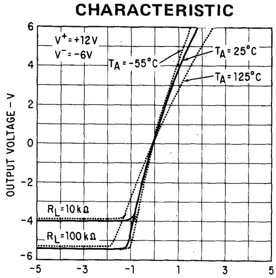
μA702

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$ unless otherwise specified.

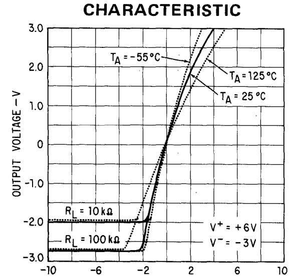
CHARACTERISTICS	CONDITIONS	V+ = 12.0V, V− = −6.0V MIN	TYP	MAX	V+ = 6.0V, V− = −3.0V MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	80	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{OUT} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity-gain) Rise Time	$C_I = 0.01\ \mu F$, $R_I = 20\ \Omega$, $R_L \geq 100\ k\Omega$, $V_{IN} = 10$ mV		25	120				ns
Transient Response (unity-gain) Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain) Rise Time	$C3 = 50$ pF, $R_L \geq 100\ k\Omega$,		10	30				ns
Transient Response (x100 gain) Overshoot	$V_{IN} = 1$ mV		20	40				%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $+125°C$		2.5	10		3.5	15	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $-55°C$		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125°C$		80	500		50	500	nA
	$T_A = -55°C$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $+125°C$		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25°C$ to $-55°C$		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55°C$		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V+ = 12$ V, $V- = -6.0$ V to $V+ = 6.0$ V, $V- = -3.0$ V, $R_S \leq 2\ k\Omega$		75	200		75	200	μV/V
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{OUT} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{OUT} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{OUT} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{OUT} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVE FOR μA702

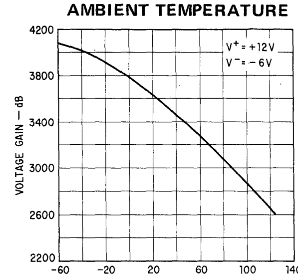
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



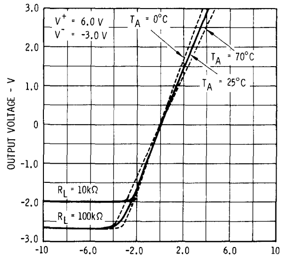
μA702C

ELECTRICAL CHARACTERISTICS: T_A = 25°C unless otherwise specified.

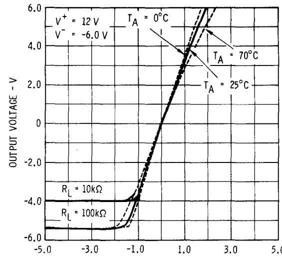
CHARACTERISTICS	CONDITIONS	V+ = 12.0 V, V− = −6.0 V MIN	TYP	MAX	V+ = 6.0 V, V− = −3.0 V MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 2\,k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\,k\Omega$, f ⩽ 1 kHz	70	92		70	92		dB
Large Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{OUT} = \pm 5.0\,V$	2000	3400	6000				
	$R_L \geq 100\,k\Omega$, $V_{OUT} = \pm 2.5\,V$				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{OUT} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity gain) — Rise Time	C1 = 0.01 μF, $R_I = 20\,\Omega$, $R_L \leq 100\,k\Omega$, $V_{IN} = 10\,mV$		25	120				ns
Transient Response (unity gain) — Overshoot	$C_L \leq 100\,pF$		10	50				%
Transient Response (x100 gain) — Rise Time	C3 = 50 pF, $R_L \geq 100\,k\Omega$,		10	30				ns
Transient Response (x100 gain) — Overshoot	$V_{IN} = 1\,mV$		20	40				%
The following specifications apply for 0°C ⩽ T_A ⩽ +70°C:								
Input Offset Voltage	$R_S \leq 2\,k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\,\Omega$, T_A = +70°C to 0°C		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to +70°C		4.0	10		3.0	8.0	nA/°C
	T_A = 25°C to 0°C		6.0	20		5.5	18	nA/°C
Input Bias Current	T_A = 0°C		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\,k\Omega$, f ⩽ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	V+ = 12 V, V− = −6.0 V to V+ = 6.0 V, V− = −3.0 V, $R_S \leq 2\,k\Omega$		90	300		90	300	μV/V
Large Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{OUT} = \pm 5.0\,V$	1500		7000				
	$R_L \geq 100\,k\Omega$, $V_{OUT} = \pm 2.5\,V$				400		1750	
Output Voltage Swing	$R_L \geq 100\,k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\,k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$V_{OUT} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{OUT} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES FOR μA702C

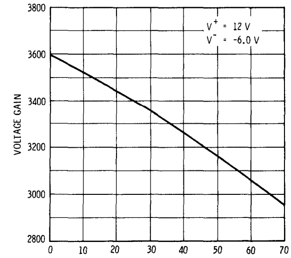
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



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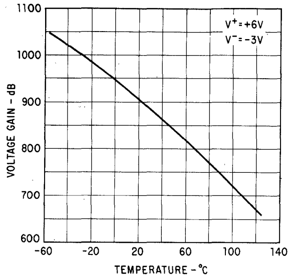
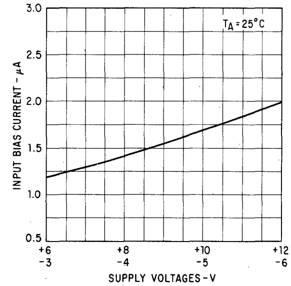
TYPICAL PERFORMANCE CURVES FOR μA702

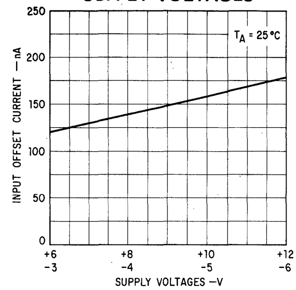
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



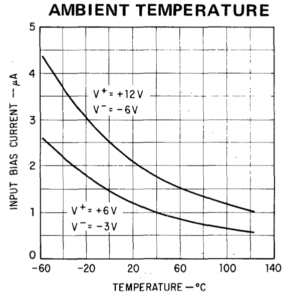
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



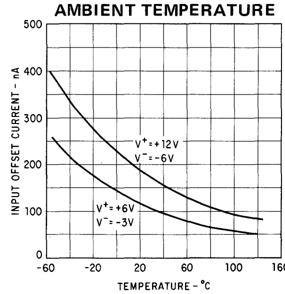
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



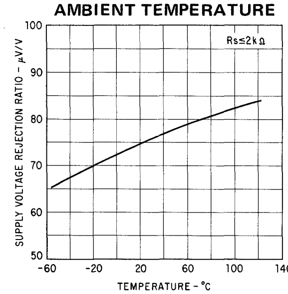
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



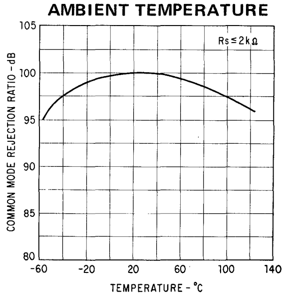
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



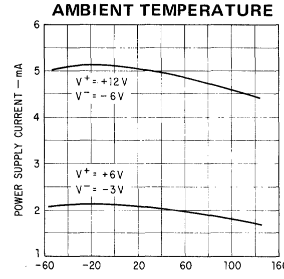
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



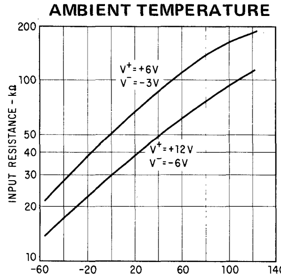
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



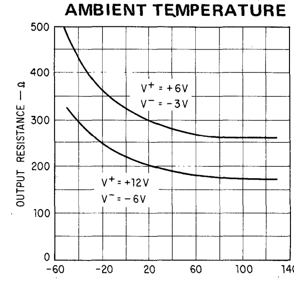
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

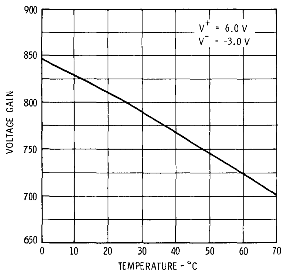


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

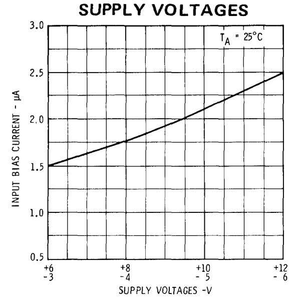


TYPICAL PERFORMANCE CURVES FOR μA702C

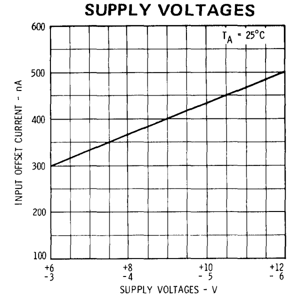
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



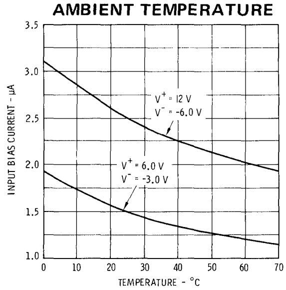
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



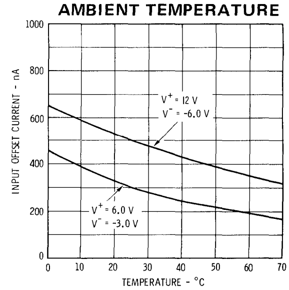
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



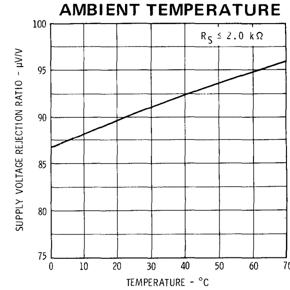
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



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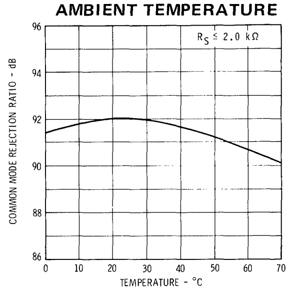
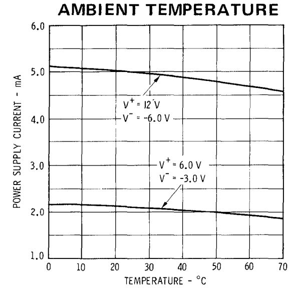
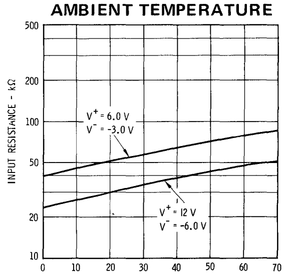
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



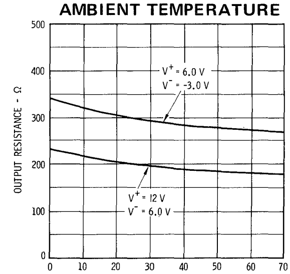
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

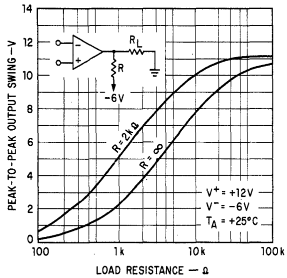


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

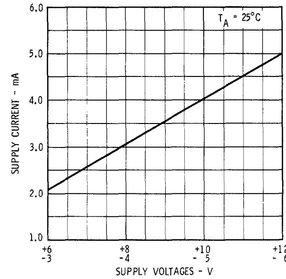


TYPICAL PERFORMANCE CURVES FOR μA702 AND μA702C

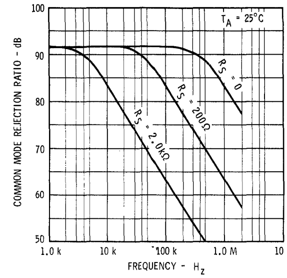
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



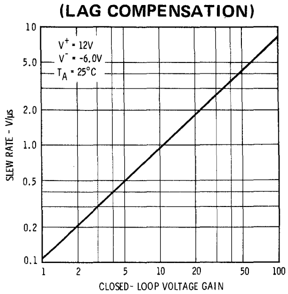
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



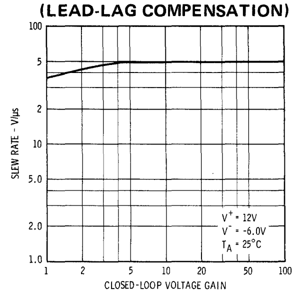
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



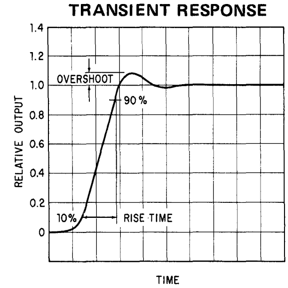
SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LAG COMPENSATION)



SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

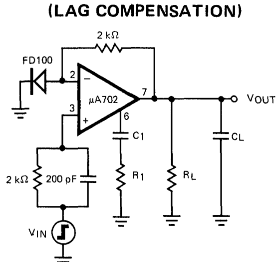


TRANSIENT RESPONSE

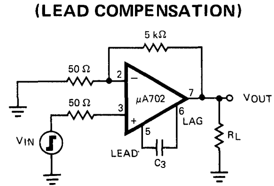


TRANSIENT RESPONSE TEST CIRCUITS

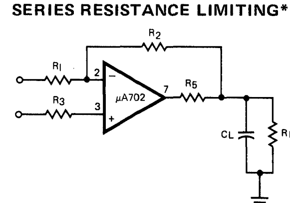
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



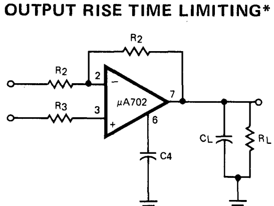
X100 AMPLIFIER (LEAD COMPENSATION)



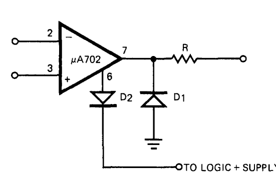
SERIES RESISTANCE LIMITING*



OUTPUT RISE TIME LIMITING*



LOGIC COMPATIBILITY

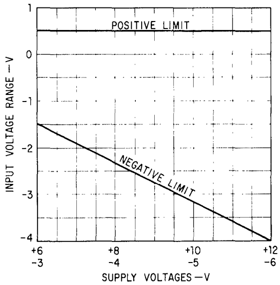


*Peak current limiting with capacitive loads.

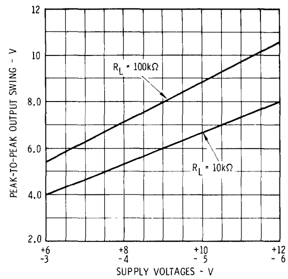
Pin numbers are shown for metal can only.

TYPICAL PERFORMANCE CURVES FOR μA702 AND μA702C

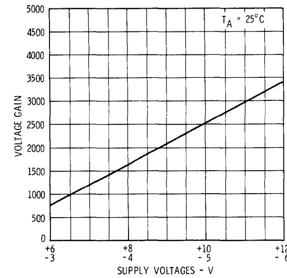
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



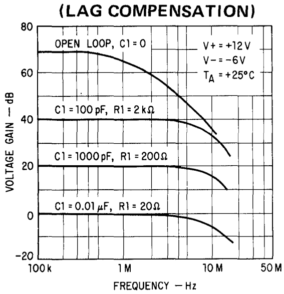
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



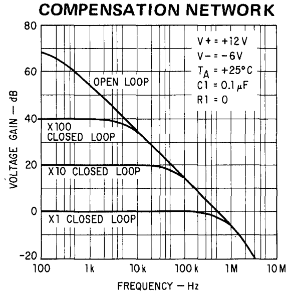
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



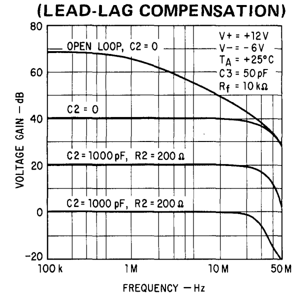
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



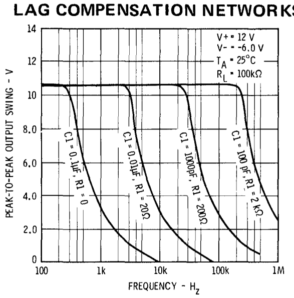
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



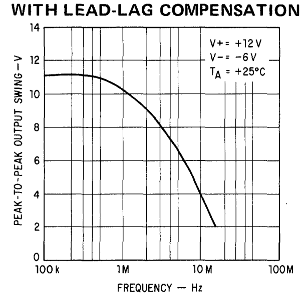
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

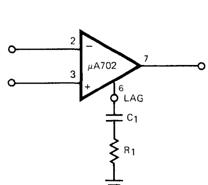


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION

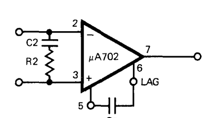


FREQUENCY COMPENSATION CIRCUITS

LAG COMPENSATION



LEAD-LAG COMPENSATION



Pin numbers are shown for metal can only.

µA709
HIGH-PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The µA709 is a monolithic High Gain Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in dc servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

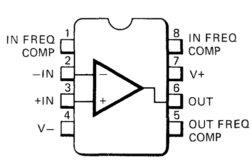
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
Mini DIP	310 mW
DIP	670 mW
Flatpak	570 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Storage Temperature Range	
Metal, Hermetic DIP, and Flatpak	−65°C to +150°C
Molded DIP and Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (µA709A and µA709)	−55°C to +125°C
Commercial (µA709C)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP, and Flatpak (Soldering 60 s)	300°C
Molded DIP and Mini DIP	260°C
Output Short-Circuit Duration	5 s

NOTE:
Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP, 7.1mW/°C for the Flatpak and 5.6mW/°C for the Mini DIP.

CONNECTION DIAGRAMS

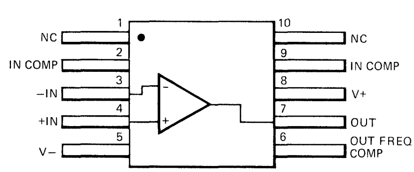
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
µA709C	µA709TC

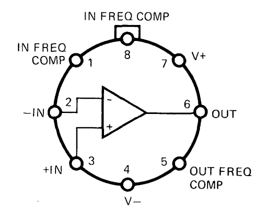
10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
µA709A	µA709AFM
µA709	µA709FM

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

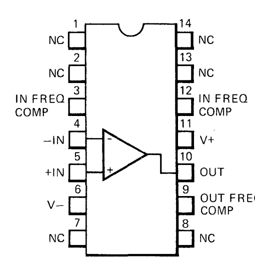


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
µA709A	µA709AHM
µA709	µA709HM
µA709C	µA709HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
µA709A	µA709ADM
µA709	µA709DM
µA709C	µA709DC
µA709C	µA709PC

*Planar is a patented Fairchild process.

μA709A

ELECTRICAL CHARACTERISTICS: T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		0.6	2.0	mV
Input Offset Current				10	50	nA
Input Bias Current				100	200	nA
Input Resistance			350	700		kΩ
Output Resistance				150		Ω
Supply Current		V_S = ±15 V		2.5	3.6	mA
Power Consumption		V_S = ±15 V		75	108	mW
Transient Response		V_S = ±15 V, V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5 nF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω			1.5	μs
	Overshoot	$C_L \leq 100$ pF			30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 10$ kΩ			3.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50Ω, T_A = +25°C to +125°C		1.8	10	μV/°C
		R_S = 50Ω, T_A = +25°C to −55°C		1.8	10	μV/°C
		R_S = 10 kΩ, T_A = +25°C to +125°C		2.0	15	μV/°C
		R_S = 10 kΩ, T_A = +25°C to −55°C		4.8	25	μV/°C
Input Offset Current		T_A = +125°C		3.5	50	nA
		T_A = −55°C		40	250	nA
Average Temperature Coefficient of Input Offset Current		T_A = +25°C to +125°C		0.08	0.5	nA/°C
		T_A = +25°C to −55°C		0.45	2.8	nA/°C
Input Bias Current		T_A = −55°C		300	600	nA
Input Resistance		T_A = −55°C	85	170		kΩ
Input Voltage Range		V_S = ±15 V	±8.0			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	80	110		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		40	100	μV/V
Large Signal Voltage Gain		V_S = ±15 V, $R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000		70,000	V/V
Output Voltage Swing		V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
		V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Supply Current		T_A = +125°C, V_S = ±15 V		2.1	3.0	mA
		T_A = −55°C, V_S = ±15 V		2.7	4.5	mA
Power Consumption		T_A = +125°C, V_S = ±15 V		63	90	mW
		T_A = −55°C, V_S = ±15 V		81	135	mW

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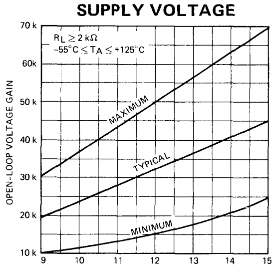
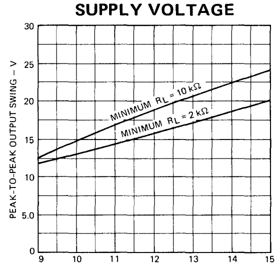
PERFORMANCE CURVES FOR μA709A

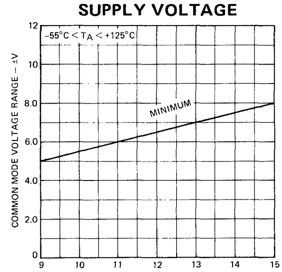
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



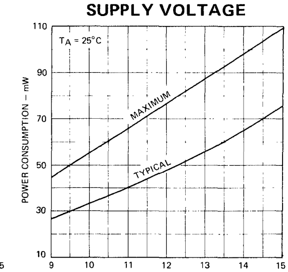
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



μA709

ELECTRICAL CHARACTERISTICS: T_A = +25°C, ±9 V ⩽ V_S ⩽ ±15 V unless otherwise specified.

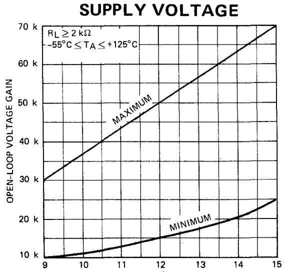
CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				50	200	nA
Input Bias Current				200	500	nA
Input Resistance			150	400		kΩ
Output Resistance				150		Ω
Power Consumption		V_S = ±15 V		80	165	mW
Transient Response	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω		0.3	1.0	
	Overshoot	$C_L \leq 100$ pF		10	30	%

The following specifications apply for −55°C ≤ T_A ≤ +125°C:

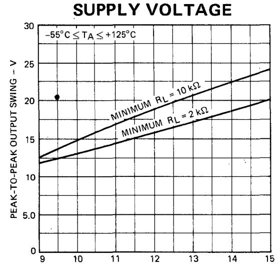
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000	45,000	70,000	V/V
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
	T_A = −55°C		100	500	nA
Input Bias Current	T_A = −55°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

PERFORMANCE CURVES FOR μA709

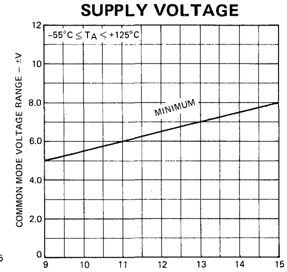
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



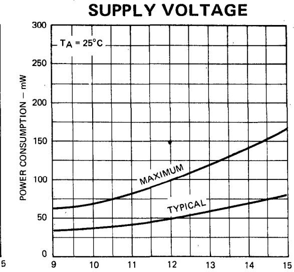
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



μA709C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

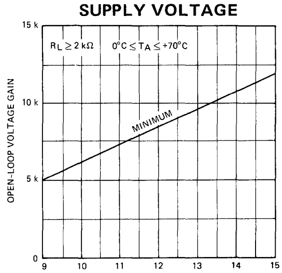
CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ, ±9 V ≤ V_S ≤ ±15 V		2.0	7.5	mV
Input Offset Current				100	500	nA
Input Bias Current				0.3	1.5	μA
Input Resistance			50	250		kΩ
Output Resistance				150		Ω
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000	45,000		V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range			±8.0	±10		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption				80	200	mW
Transient Response	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω $C_L \leq 100$ pF		0.3		μs
	Overshoot			10		%

The following specifications apply for 0°C ≤ T_A ≤ +70°C:

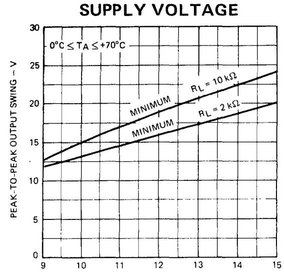
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V ≤ V_S ≤ ±15 V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	12,000			V/V
Input Resistance		35			kΩ

PERFORMANCE CURVES FOR μA709C

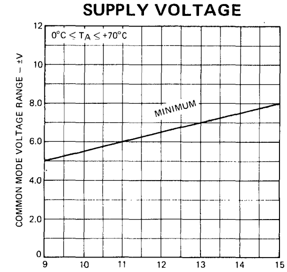
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

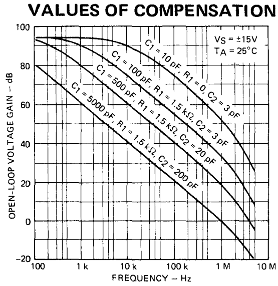


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

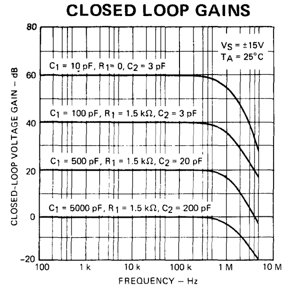


FREQUENCY COMPENSATION CURVES FOR ALL TYPES

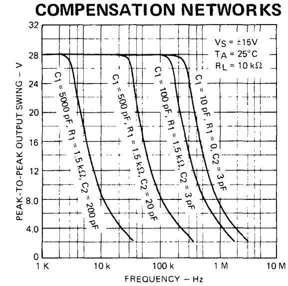
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

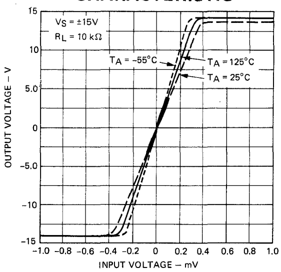


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

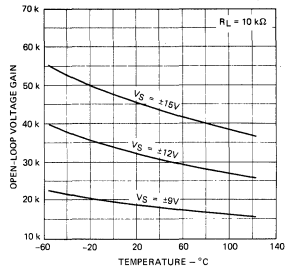


TYPICAL PERFORMANCE CURVES FOR μA709A

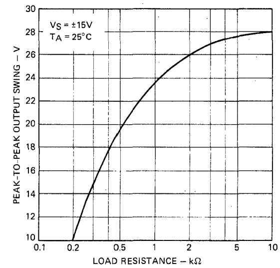
VOLTAGE TRANSFER CHARACTERISTIC



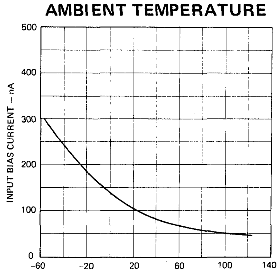
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



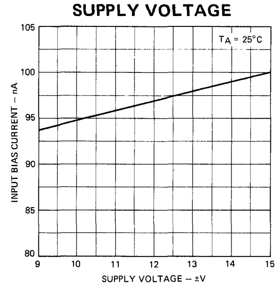
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



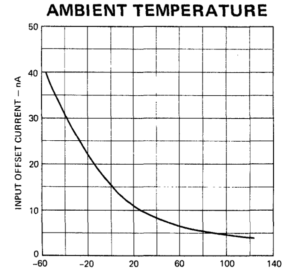
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



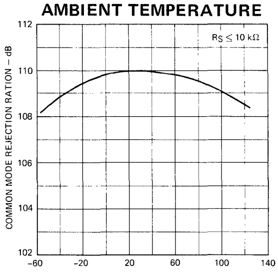
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



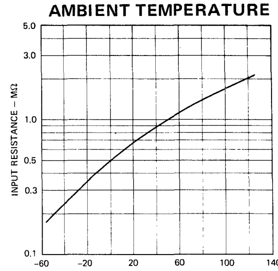
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



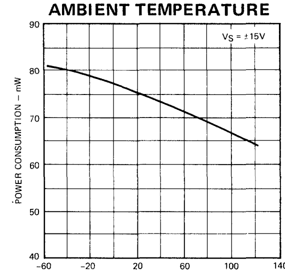
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



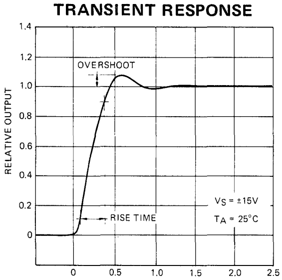
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



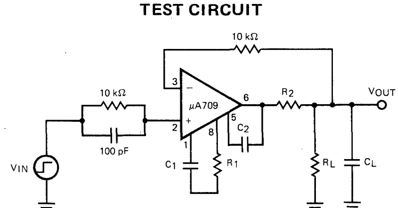
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSIENT RESPONSE

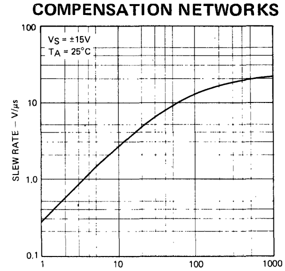


TRANSIENT RESPONSE TEST CIRCUIT



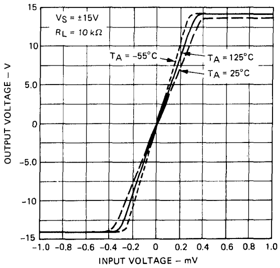
Pin numbers on this and all succeeding circuits apply to metal can or mini DIP package.

SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

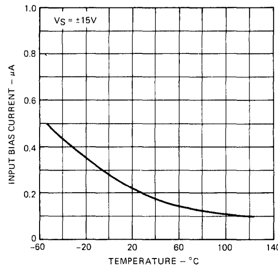


TYPICAL PERFORMANCE CURVES FOR μA709 AND μA709C

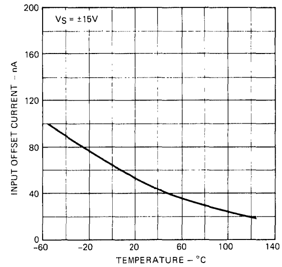
VOLTAGE TRANSFER CHARACTERISTIC



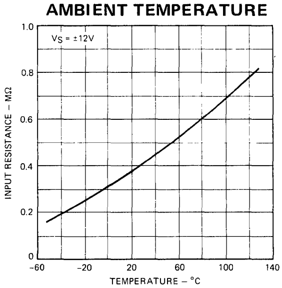
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



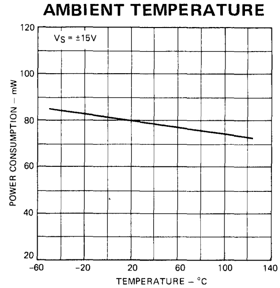
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



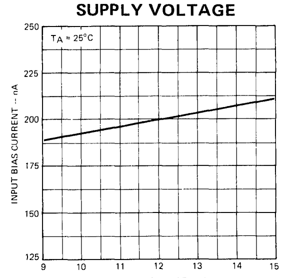
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



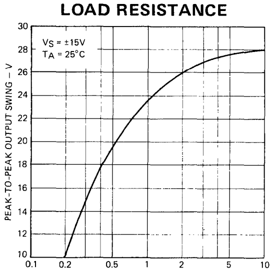
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



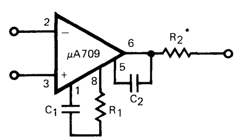
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

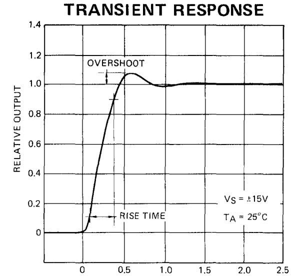


FREQUENCY COMPENSATION CIRCUIT

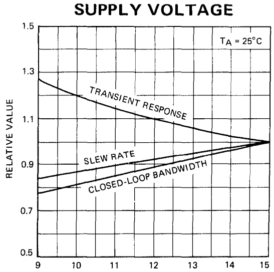


* Use R2 = 50 Ω when the amplifier is operated with capacitive loading.

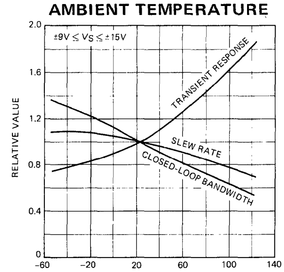
TRANSIENT RESPONSE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



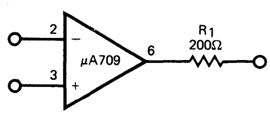
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



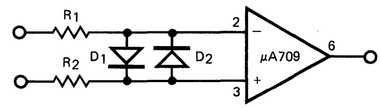
5

PROTECTION CIRCUITS

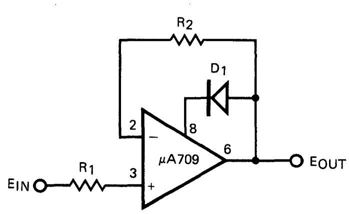
OUTPUT SHORT-CIRCUIT PROTECTION



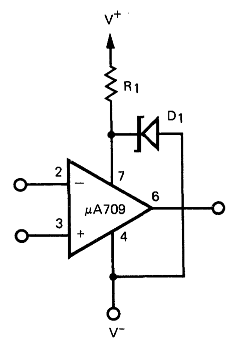
INPUT BREAKDOWN-PROTECTION



LATCH-UP PROTECTION

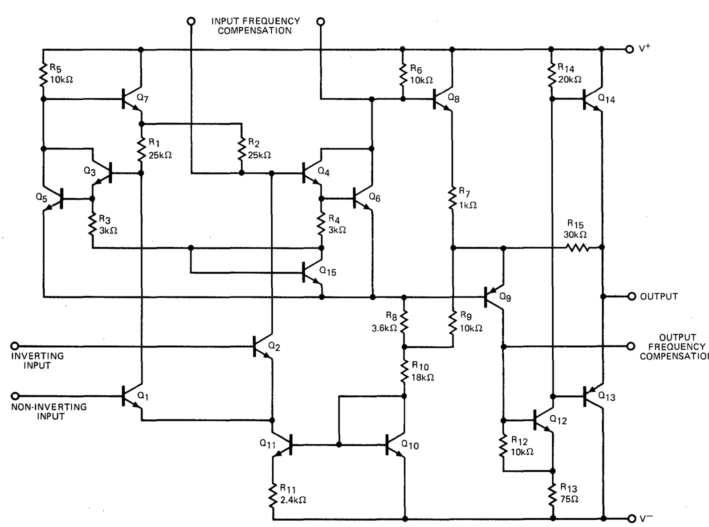


SUPPLY OVERVOLTAGE-PROTECTION



Pin numbers apply to metal can or mini DIP package only.

EQUIVALENT CIRCUIT



μA714

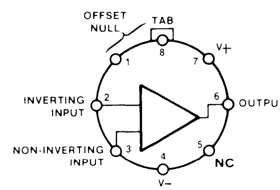
PRECISION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION – The μA714 is a Monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications.

- **LOW OFFSET VOLTAGE . . . 75 μV for μA714**
- **LOW OFFSET VOLTAGE DRIFT . . . 1.3 μV/°C for μA714**
- **LOW BIAS CURRENT . . . ±3.0 nA for μA714**
- **LOW INPUT NOISE CURRENT . . . 0.17 pA/$\sqrt{\text{Hz}}$ @1.0 kHz max**
- **HIGH OPEN LOOP GAIN . . . 500,000 typically**
- **LOW INPUT OFFSET CURRENT . . . 2.8 nA max for μA714**
- **HIGH COMMON MODE REJECTION . . . 110 dB min for μA714**
- **WIDE POWER SUPPLY RANGE . . . ±3.0 TO ±22 V**

CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

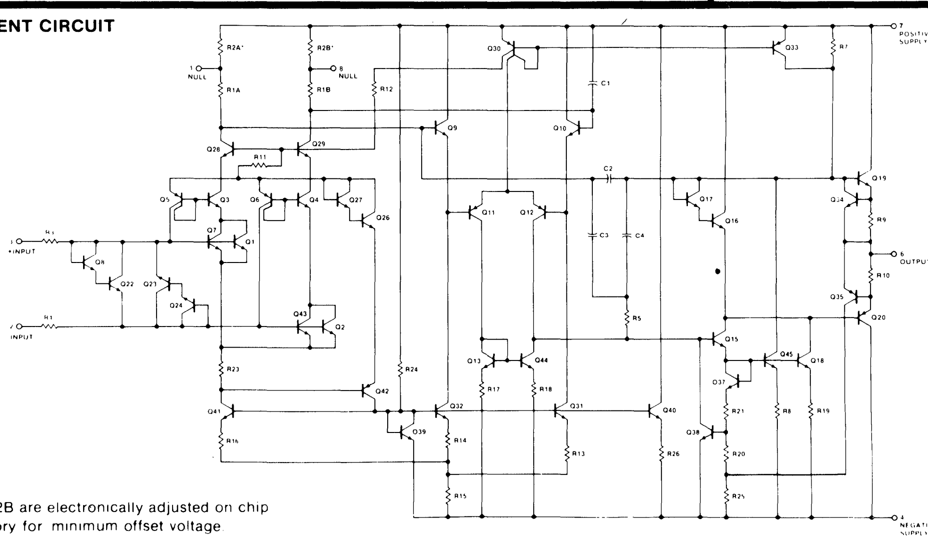
TYPE	PART NO.
714	μA714HM
714E	μA714EHC
714C	μA714HC
714L	μA714LHC

ABSOLUTE MAXIMUM RATINGS

Notes on following pages

	μA714 μA714E, μA714C	μA714L
Supply Voltage	±22 V	±18 V
Internal Power Dissipation (Note 1)		
Metal Can	500 mW	500 mW
Differential Input Voltage	±30 V	±30 V
Input Voltage (Note 2)	±22 V	±18 V
Storage Temperature Range		
Metal Can	−65°C to +150°C	−65°C to +150°C
Operating Temperature Range		
Military	−55°C to +125°C	
Commercial	0°C to +70°C	0°C to +70°C
Pin Temperature		
Metal Can (Soldering, 60 s)	300°C	300°C

EQUIVALENT CIRCUIT



*Note:
R2A and R2B are electronically adjusted on chip at the factory for minimum offset voltage.

ELECTRICAL CHARACTERISTICS μA714

These specifications apply for V_S = ±15 V, T_A = 25°C.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V		30	75	μV
Long Term Input Offset Voltage Stability	Note 4, R_S = 50 Ω, V_{CM} = 0.0V		0.2	1.0	μV/mo.
Input Offset Current	V_{CM} = 0.0 V		0.4	2.8	nA
Input Bias Current	V_{CM} = 0.0 V		±1.0	±3.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 5)		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 5)		10.3	18.0	nV/√Hz
	f_O = 100 Hz (Note 5)		10.0	13.0	
	f_O = 1000 Hz (Note 5)		9.6	11.0	
Input Noise Current	0.1 Hz to 10 Hz (Note 5)		14	30	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 5)		0.32	0.80	pA/√Hz
	f_O = 100 Hz (Note 5)		0.14	0.23	
	f_O = 1000 Hz (Note 5)		0.12	0.17	
Input Resistance – Differential Mode		20	60		MΩ
Input Resistance – Common Mode			200		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ±13 V, R_S = 50 Ω	110	126		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	100	110		dB
Large Signal Voltage Gain	R_L ≥ 2.0 kΩ, V_O = −10 V to +10 V	200	500		V/mV
	R_L ≥ 500 Ω, V_O = −0.5 V to +0.5 V, V_S = ±3.0 V	150	500		
Maximum Output Voltage Swing	R_L ≥ 10 kΩ	±12.5	±13.0		V
	R_L ≥ 2.0 kΩ	±12.0	±12.8		
	R_L ≥ 1.0 kΩ	±10.5	±12.0		
Slewing Rate	R_L ≥ 2.0 kΩ		0.17		V/μs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.6		MHz
Open Loop Output Resistance	V_O = 0 V, I_O = 0 A		60		Ω
Power Consumption	V_O = 0 V		75	120	mW
	V_S = ±3.0 V, V_O = 0 V		4.0	6.0	
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, −55°C ≤ T_A ≤ +125°C.					
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V		60	200	μV
Average Input Offset Voltage Drift					μV/°C
Without External Trim	R_S = 50 Ω, V_{CM} = 0.0 V		0.3	1.3	
With External Trim	Note 5, R_P = 20 kΩ, R_S = 50 Ω		0.3	1.3	
Input Offset Current	V_{CM} = 0.0 V		1.2	5.6	nA
Average Input Offset Current Drift	V_{CM} = 0.0 V		8.0	50	pA/°C
Input Bias Current	V_{CM} = 0.0 V		±2.0	±6.0	nA
Average Input Bias Current Drift	V_{CM} = 0.0 V		13	50	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13 V, R_S = 50 Ω	106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	94	106		dB
Large Signal Voltage Gain	R_L ≥ 2.0 kΩ, V_O = −10 V to +10 V	150	400		V/mV
Maximum Output Voltage Swing	R_L ≥ 2.0 kΩ	±12.0	±12.6		V

NOTES:
1. Ratings applies to ambient temperature to 70°C. Above T_A = 70°C derate linearly 6.3 mW/°C.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. Long term input offset voltage stability refers to the averaged trend of V_{OS} versus time over extended periods after the first 30 days of operation. Parameter is not 100% tested. 90% of the units meet this specification.
5. Parameter is not 100% tested; 90% of the units meet this specification.

ELECTRICAL CHARACTERISTICS μA714E

These specifications apply for $V_S = \pm15$ V, $T_A = 25°C$.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3, $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		30	75	μV
Long Term Input Offset Voltage Stability	Note 4, $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		0.3	1.5	μV/mo.
Input Offset Current	$V_{CM} = 0.0$ V		0.5	3.8	nA
Input Bias Current	$V_{CM} = 0.0$ V		±1.2	±4.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 5)		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	$f_O = 10$ Hz (Note 5) $f_O = 100$ Hz (Note 5) $f_O = 1000$ Hz (Note 5)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	0.1 Hz to 10 Hz (Note 5)		14	30	pA p-p
Input Noise Current Density	$f_O = 10$ Hz (Note 5) $f_O = 100$ Hz (Note 5) $f_O = 1000$ Hz (Note 5)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode		15	50		MΩ
Input Resistance – Common Mode			160		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	$V_{CM} = \pm13$ V, $R_S = 50\ \Omega$	106	123		dB
Power Supply Rejection Ratio	$V_S = \pm3.0$ V to ±18 V, $R_S = 50\ \Omega$	94	107		dB
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = -10$ V to +10 V $R_L \geq 500\ \Omega$, $V_O = -0.5$ V to +0.5 V $V_S = \pm3.0$ V	200 150	500 500		V/mV
Maximum Output Voltage Swing	$R_L \geq 10$ kΩ $R_L \geq 2.0$ kΩ $R_L \geq 1.0$ kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq 2.0$ kΩ		0.17		V/μs
Closed Loop Bandwidth	$A_{VCL} = +1.0$		0.6		MHz
Open Loop Output Resistance	$V_O = 0.0$ V, $I_O = 0.0$ A		60		Ω
Power Consumption	$V_O = 0.0$ V $V_S = \pm3.0$ V, $V_O = 0.0$ V		75 4.0	120 6.0	mW
Offset Adjustment Range	$R_P = 20$ kΩ		±4.0		mV
The following specifications apply for $V_S = \pm15$ V, $0°C \leq T_A \leq +70°C$.					
Input Offset Voltage	Note 3, $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		45	130	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	 $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V Note 5, $R_P = 20$ kΩ, $R_S = 50\ \Omega$		 0.3 0.3	 1.3 1.3	μV/°C
Input Offset Current	$V_{CM} = 0.0$ V		0.9	5.3	nA
Average Input Offset Current Drift	$V_{CM} = 0.0$ V		8.0	35	pA/°C
Input Bias Current	$V_{CM} = 0.0$ V		±1.5	±5.5	nA
Average Input Bias Current Drift	$V_{CM} = 0.0$ V		13	35	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm13$ V, $R_S = 50\ \Omega$	103	123		dB
Power Supply Rejection Ratio	$V_S = \pm3.0$ V to ±18 V, $R_S = 50\ \Omega$	90	104		dB
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = -10$ V to +10 V	180	450		V/mV
Maximum Output Voltage Swing	$R_L \geq 2.0$ kΩ	±12.0	±12.6		V

NOTES:
1. Ratings applies to ambient temperature to 70°C. Above $T_A = 70°C$ derate linearly 6.3 mW/°C.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. Long term input offset voltage stability refers to the averaged trend of V_{OS} versus time over extended periods after the first 30 days of operation. Parameter is not 100% tested. 90% of the units meet this specification.
5. Parameter is not 100% tested; 90% of the units meet this specification.

ELECTRICAL CHARACTERISTICS μA714C

These specifications apply for V_S = ±15 V, T_A = 25°C.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V		60	150	μV
Long Term Input Offset Voltage Stability	Note 4, R_S = 50 Ω, V_{CM} = 0.0V		0.4	2.0	μV/mo.
Input Offset Current	V_{CM} = 0.0 V		0.8	6.0	nA
Input Bias Current	V_{CM} = 0.0 V		±1.8	±7.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 5)		0.38	0.65	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 5)		10.5	20.0	nV/√Hz
	f_O = 100 Hz (Note 5)		10.2	13.5	
	f_O = 1000 Hz (Note 5)		9.8	11.5	
Input Noise Current	0.1 Hz to 10 Hz (Note 5)		15	35	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 5)		0.35	0.90	pA/√Hz
	f_O = 100 Hz (Note 5)		0.15	0.27	
	f_O = 1000 Hz (Note 5)		0.13	0.18	
Input Resistance – Differential Mode		8.0	33		MΩ
Input Resistance – Common Mode			120		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ±13, R_S = 50 Ω	100	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	90	104		dB
Large Signal Voltage Gain	R_L ⩾ 2.0 kΩ, V_O = −10 V to +10 V	120	400		V/mV
	R_L ⩾ 500 Ω, V_O = −0.5 V to +0.5 V, V_S = ±3.0 V	100	400		
Maximum Output Voltage Swing	R_L ⩾ 10 kΩ	±12.0	±13.0		V
	R_L ⩾ 2.0 kΩ	±11.5	±12.8		
	R_L ⩾ 1.0 kΩ		±12.0		
Slewing Rate	R_L ⩾ 2.0 kΩ		0.17		V/μs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.6		MHz
Open Loop Output Resistance	V_O = 0 V, I_O = 0 A		60		Ω
Power Consumption	V_O = 0.0 V		80	150	mW
	V_S = ±3.0 V, V_O = 0.0 V		4.0	8.0	
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ⩽ T_A ⩽ +70°C.					
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V		85	250	μV
Average Input Offset Voltage Drift					
Without External Trim	Note 5, R_S = 50 Ω, V_{CM} = 0.0 V		0.5	1.8	μV/°C
With External Trim	Note 5, R_P = 20 kΩ, R_S = 50Ω		0.4	1.6	
Input Offset Current	V_{CM} = 0.0 V		1.6	8.0	nA
Average Input Offset Current Drift	Note 5, V_{CM} = 0.0 V		12	50	pA/°C
Input Bias Current	V_{CM} = 0.0 V		±2.2	±9.0	nA
Average Input Bias Current Drift	Note 5, V_{CM} = 0.0 V		18	50	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13 V, R_S = 50 Ω	97	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	86	100		dB
Large Signal Voltage Gain	R_L ⩾ 2.0 kΩ, V_O = −10 V to +10 V	100	400		V/mV
Maximum Output Voltage Swing	R_L ⩾ 2.0 kΩ	±11.0	±12.6		V

NOTES:
1. Ratings applies to ambient temperature to 70°C. Above T_A = 70°C derate linearly 6.3 mW/°C.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. Long term input offset voltage stability refers to the averaged trend of V_{OS} versus time over extended periods after the first 30 days of operation. Parameter is not 100% tested. 90% of the units meet this specification.
5. Parameter is not 100% tested; 90% of the units meet this specification.

ELECTRICAL CHARACTERISTICS μA714L

These specifications apply for V_S = ±15 V, T_A = 25°C.

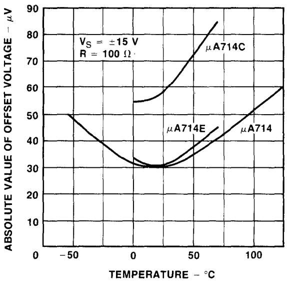
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V		100	250	μV
Long Term Input Offset Voltage Stability	Note 4, R_S = 50 Ω, V_{CM} = 0.0V		0.5	3.0	μV/mo.
Input Offset Current	V_{CM} = 0.0 V		5.0	20	nA
Input Bias Current	V_{CM} = 0.0 V		6.0	±30	nA
Input Noise Voltage Density	f_O = 10 Hz (Note 5)		10.5		
	f_O = 100 Hz (Note 5)		10.2		
	f_O = 1000 Hz (Note 5)		9.8		
Input Noise Current	0.1 Hz to 10 Hz (Note 5)		15		pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 5)		0.35		
	f_O = 100 Hz (Note 5)		0.15		
	f_O = 1000 Hz (Note 5)		0.13		
Input Resistance – Differential Mode		8.0	33		MΩ
Input Resistance – Common Mode			120		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ±13 V, R_S = 50 Ω	100	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	90	104		dB
Large Signal Voltage Gain	R_L ≥ 2.0 kΩ, V_O = −10 V to +10 V	100	300		V/mV
	R_L ≥ 500 Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	50	150		
Maximum Output Voltage Swing	R_L ≥ 10 kΩ	±12.0	±13.0		V
	R_L ≥ 2.0 kΩ	±11.0	±12.8		
	R_L ≥ 1.0 kΩ		±12.0		
Slewing Rate	R_L ≥ 2.0 kΩ		0.17		V/μs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.6		MHz
Open Loop Output Resistance	V_O = 0.0 V, I_O = 0 A		60		Ω
Power Consumption	V_O = 0.0 V		100	180	mW
	V_S = ±3.0 V, V_O = 0.0 V		5.0	12	
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ≤ T_A ≤ +70°C.					
Input Offset Voltage	Note 3, R_S = 50 Ω, V_{CM} = 0.0V			400	μV
Average Input Offset Voltage Drift Without External Trim	Note 5, R_S = 50 Ω, V_{CM} = 0.0 V		1.0	3.0	μV/°C
Input Offset Current	V_{CM} = 0.0 V		8.0	40	nA
Average Input Offset Current Drift	Note 5, V_{CM} = 0.0 V		20	100	pA/°C
Input Bias Current	V_{CM} = 0.0 V		±15	±60	nA
Average Input Bias Current Drift	Note 5, V_{CM} = 0.0 V		35	150	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13 V, R_S = 50 Ω	94	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V, R_S = 50 Ω	83	100		dB
Large Signal Voltage Gain	R_L ≥ 2.0 kΩ, V_O = −10 V to +10 V	80	400		V/mV
Maximum Output Voltage Swing	R_L ≥ 2.0 kΩ	±10.0	±12.6		V

NOTES:
1. Ratings applies to ambient temperature to 70°C. Above T_A = 70°C derate linearly 6.3 mW/°C.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. Long term input offset voltage stability refers to the averaged trend of V_{OS} versus time over extended periods after the first 30 days of operation. Parameter is not 100% tested. 90% of the units meet this specification.
5. Parameter is not 100% tested; 90% of the units meet this specification.

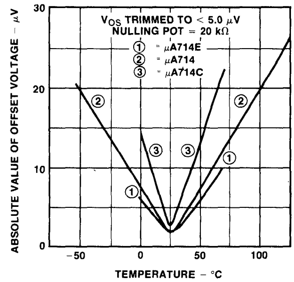
5

TYPICAL PERFORMANCE CURVES

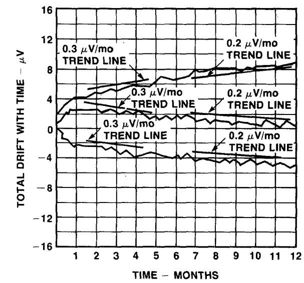
UNTRIMMED OFFSET VOLTAGE VERSUS TEMPERATURE



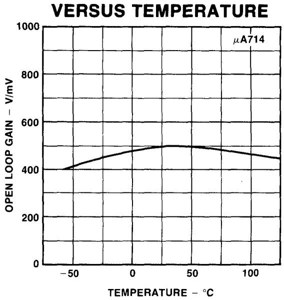
TRIMMED OFFSET VOLTAGE VERSUS TEMPERATURE



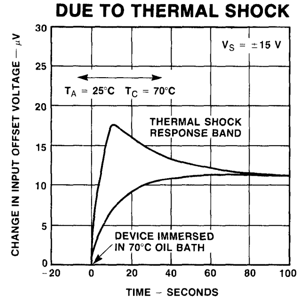
OFFSET VOLTAGE STABILITY VERSUS TIME



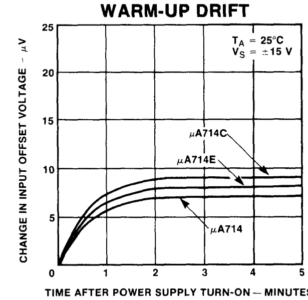
OPEN LOOP GAIN VERSUS TEMPERATURE



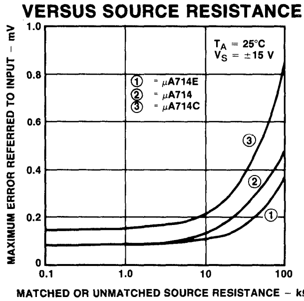
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



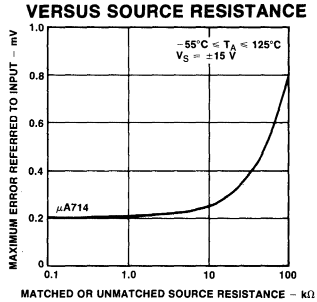
WARM-UP DRIFT



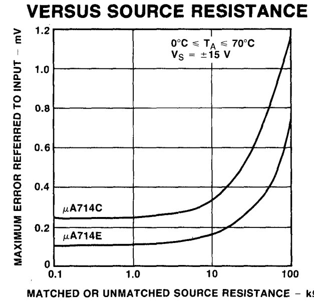
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



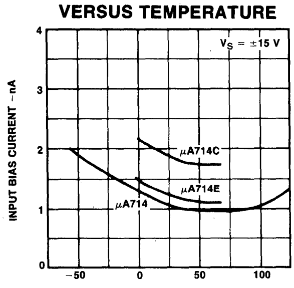
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



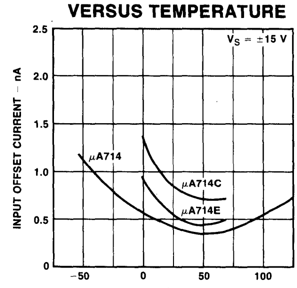
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



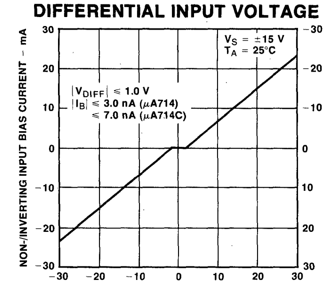
INPUT BIAS CURRENT VERSUS TEMPERATURE



INPUT OFFSET CURRENT VERSUS TEMPERATURE

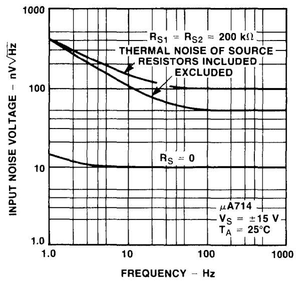


INPUT BIAS CURRENT VERSUS DIFFERENTIAL INPUT VOLTAGE

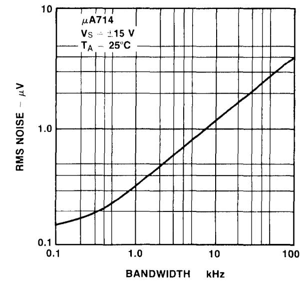


TYPICAL PERFORMANCE CURVES

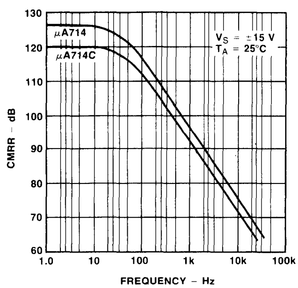
INPUT SPOT NOISE VOLTAGE VERSUS FREQUENCY



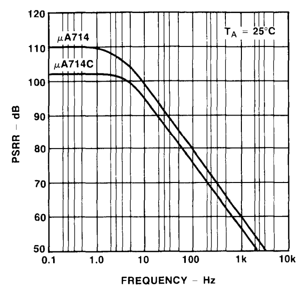
INPUT WIDEBAND NOISE VERSUS BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



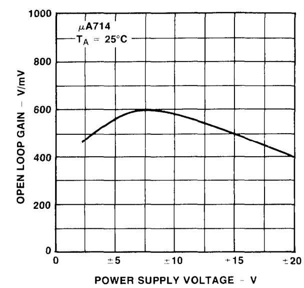
CMRR VERSUS FREQUENCY



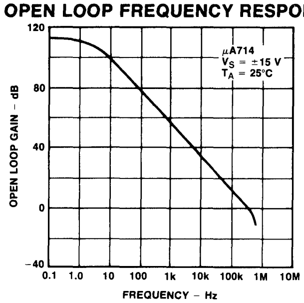
PSRR VERSUS FREQUENCY



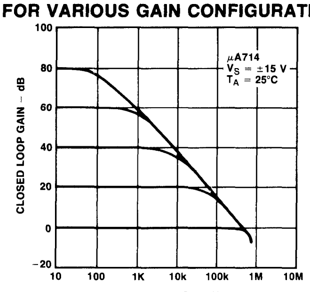
OPEN LOOP GAIN VERSUS POWER SUPPLY VOLTAGE



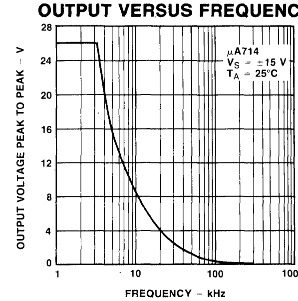
OPEN LOOP FREQUENCY RESPONSE



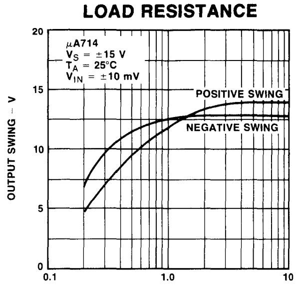
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



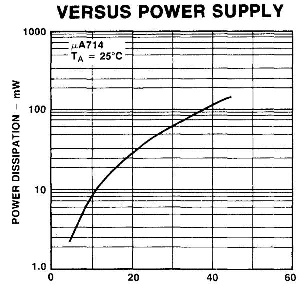
MAXIMUM UNDISTORTED OUTPUT VERSUS FREQUENCY



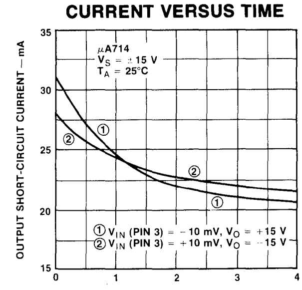
OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



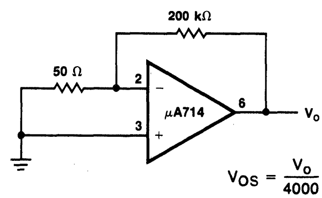
POWER CONSUMPTION VERSUS POWER SUPPLY



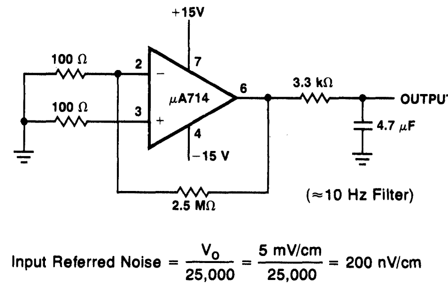
OUTPUT SHORT CIRCUIT CURRENT VERSUS TIME



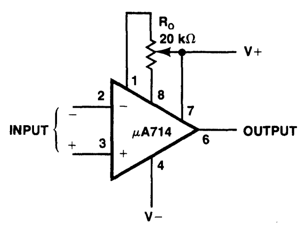
TYPICAL APPLICATIONS



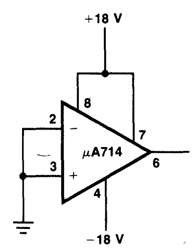
OFFSET VOLTAGE TEST CIRCUIT



LOW FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT

µA715
HIGH-SPEED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

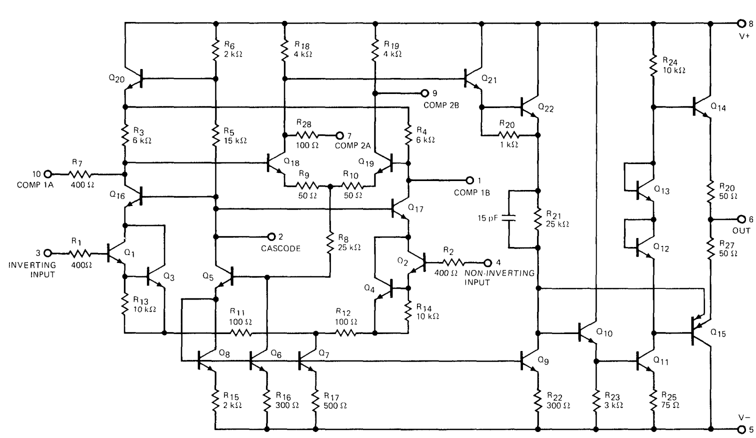
GENERAL DESCRIPTION – The µA715 is a High Speed, High Gain, monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The µA715 features fast settling time, high slew rate, low offsets and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The µA715 is ideally suited for use in A/D and D/A converters, active filters, deflection amplifiers, video amplifiers, phase locked-loops, multiplexed analog gates, precision comparators, sample and holds and general feedback applications requiring dc wide bandwidth operation.

- **HIGH SLEW RATE – 100 V/µs**
- **FAST SETTLING TIME – 800 ns**
- **WIDE BANDWIDTH – 65 MHz**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Operating Temperature Range	
Military (µA715)	−55°C to +125°C
Commercial (µA715C)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	
Metal Can, DIP	300°C

EQUIVALENT CIRCUIT

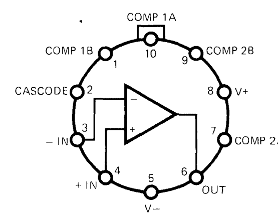


All pin numbers shown refer to 10-pin TO-5 package.

Notes on following pages.

CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5N
PACKAGE CODE H

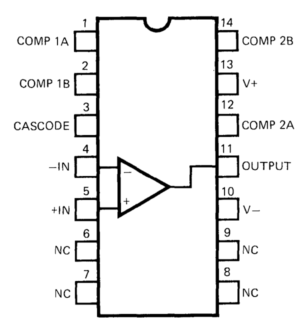


ORDER INFORMATION

TYPE	PART NO.
µA715	µA715HM
µA715C	µA715HC

14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
µA715	µA715DM
µA715C	µA715DC

*Planar is a patented Fairchild process.

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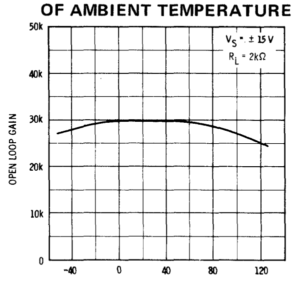
μA715

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

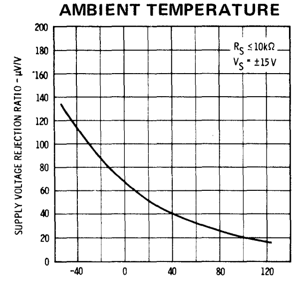
CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	5.0	mV
Input Offset Current				70	250	nA
Input Bias Current				400	750	nA
Input Resistance				1.0		MΩ
Input Voltage Range			±10	±12		V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000	30,000		
Output Resistance				75		Ω
Supply Current				5.5	7.0	mA
Power Consumption				165	210	mW
Settling Time (Unity Gain)		$V_{OUT} = +5$ V		800		ns
Transient Response (Unity Gain)	Rise Time	$V_{IN} = 400$ mV		30	60	ns
	Overshoot			25	40	%
Slew Rate		Av = 100		70		V/μs
Slew Rate		Av = 10		38		V/μs
		Av = 1 (non-inverting)	15	18		V/μs
		Av = 1 (inverting)		100		V/μs
The following apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current		$T_A = +125°C$			250	nA
		$T_A = -55°C$			800	nA
Input Bias Current		$T_A = +125°C$			750	nA
		$T_A = -55°C$			4.0	μA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	74	92		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		45	300	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	10,000			
Output Voltage Swing		$R_L \geq 2$ kΩ	±10	±13		

TYPICAL PERFORMANCE CURVES FOR μA715

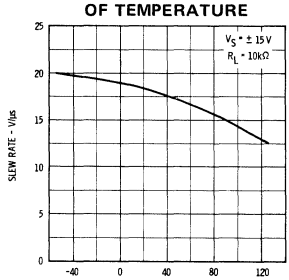
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



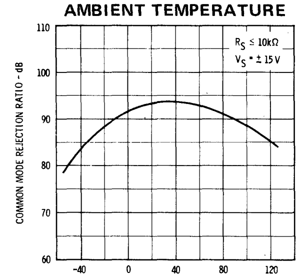
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



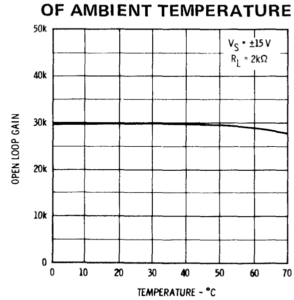
μA715C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

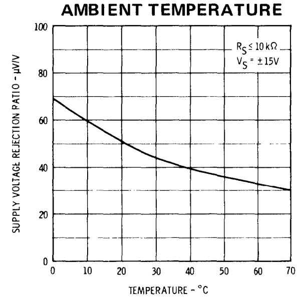
CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leqslant 10\ k\Omega$		2.0	7.5	mV
Input Offset Current				70	250	nA
Input Bias Current				0.4	1.5	μA
Input Resistance				1.0		MΩ
Input Voltage Range			±10	±12		V
Common Mode Rejection Ratio		$R_S \leqslant 10\ k\Omega$	74	92		dB
Supply Voltage Rejection Ratio		$R_S \leqslant 10\ k\Omega$		45	400	μV/V
Large Signal Voltage Gain		$R_L \geqslant 2\ k\Omega$, V_{OUT} = ±10 V	10,000	30,000		
Output Resistance				75		Ω
Supply Current				5.5	10	mA
Power Consumption				165	300	mW
Settling Time (Unity Gain)		V_{OUT} = +5 V		800		ns
Transient Response (Unity Gain)	Rise Time	V_{IN} = 400 mV		30	75	ns
	Overshoot			25	50	%
Slew Rate		A_V = 100		70		V/μs
		A_V = 10		38		V/μs
		A_V = 1 (non-inverting)	10	18		V/μs
		A_V = 1 (inverting)		100		V/μs
The following apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage		$R_S \leqslant 10\ k\Omega$			10	mV
Input Offset Current		T_A = +70°C			250	nA
		T_A = 0°C			750	nA
Input Bias Current		T_A = +70°C			1.5	μA
		T_A = 0°C			7.5	μA
Large Signal Voltage Gain		$R_L \geqslant 2\ k\Omega$, V_{OUT} = ±10 V	8,000			
Output Voltage Swing		$R_L \geqslant 2\ k\Omega$	±10	±13		V

TYPICAL PERFORMANCE CURVES FOR μA715C

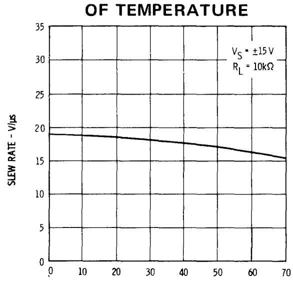
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



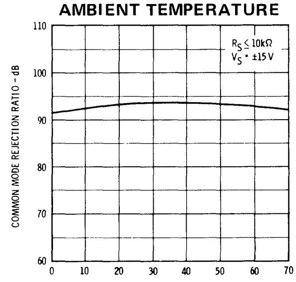
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



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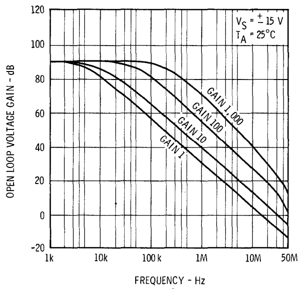
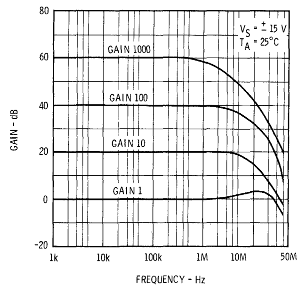
TYPICAL PERFORMANCE CURVES FOR μA715 AND μA715C

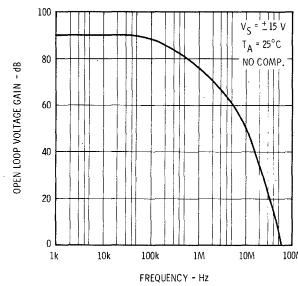
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



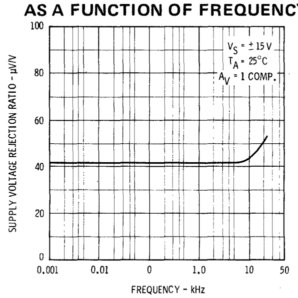
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



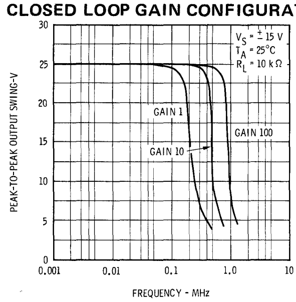
OPEN LOOP GAIN AS A FUNCTION OF FREQUENCY



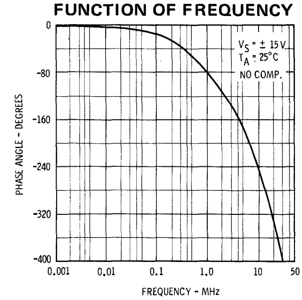
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



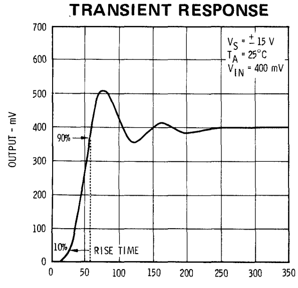
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



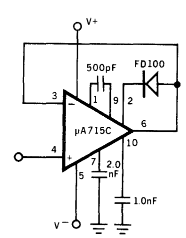
OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER TRANSIENT RESPONSE

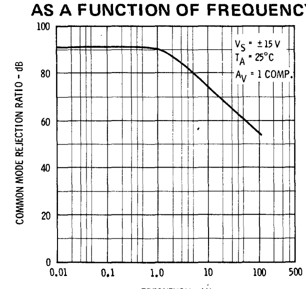


VOLTAGE FOLLOWER



Pin numbers apply to metal can.

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



NOTES

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

LAYOUT INSTRUCTIONS

LAYOUT — The layout should be such that stray capacitance is minimal.

SUPPLIES — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

LATCH-UP — This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive measure.

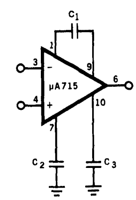
TYPICAL PERFORMANCE CURVES FOR μA715 AND μA715C

NON-INVERTING COMPENSATION COMPONENTS VALUES

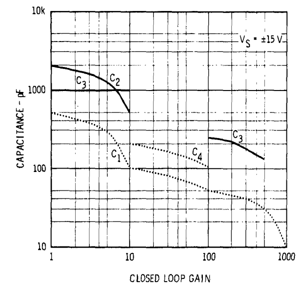
CLOSED LOOP GAIN	C1	C2	C3
1000	10 pF		
100	50 pF		250 pF
10 *	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

*For Gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Pin 7 and 10.

FREQUENCY COMPENSATION CIRCUIT

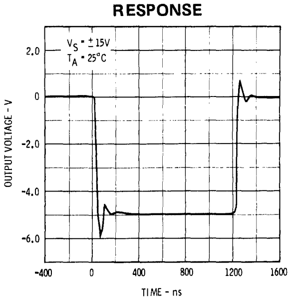


SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN

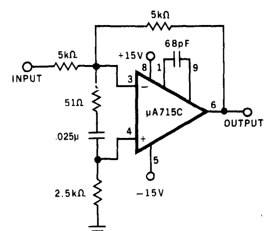


INVERTING UNITY GAIN

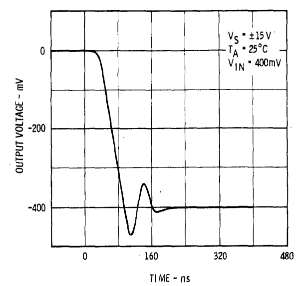
LARGE SIGNAL PULSE RESPONSE



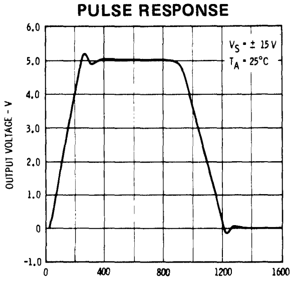
HIGH SLEW RATE CIRCUIT



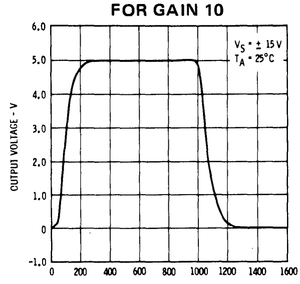
SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



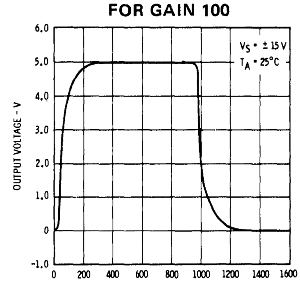
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



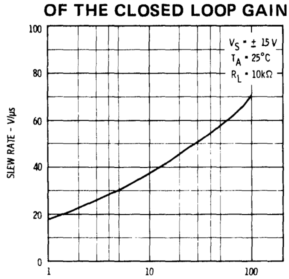
LARGE SIGNAL PULSE RESPONSE FOR GAIN 10



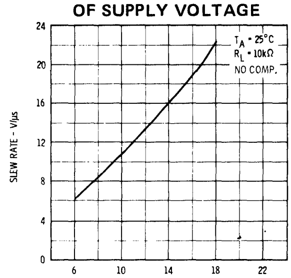
LARGE SIGNAL PULSE RESPONSE FOR GAIN 100



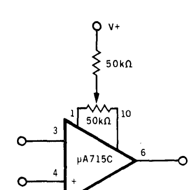
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP GAIN



SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



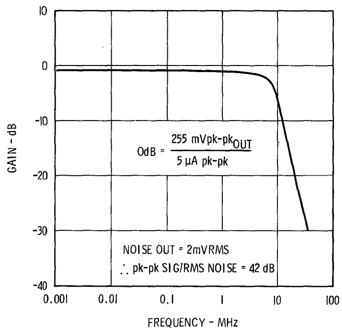
VOLTAGE OFFSET NULL CIRCUIT

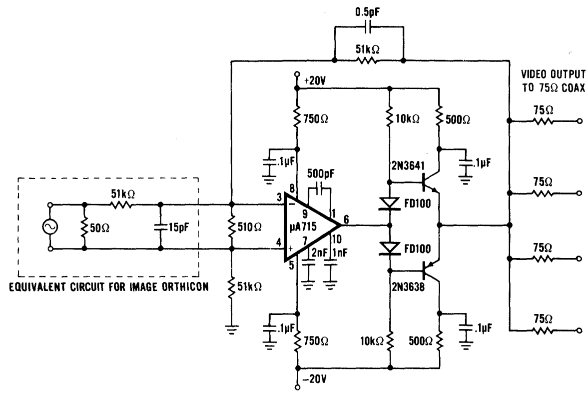


Pin numbers apply to metal can.

TYPICAL APPLICATIONS

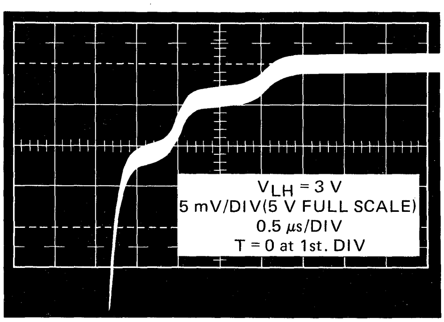
WIDE BAND VIDEO AMPLIFIER WITH 75 Ω COAX CABLE DRIVE CAPABILITY



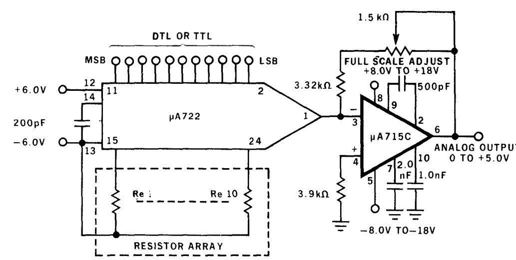


HIGH SPEED 10-BIT DIGITAL TO ANALOG CONVERTER

ANALOG OUTPUT 0 TO +5.0 V



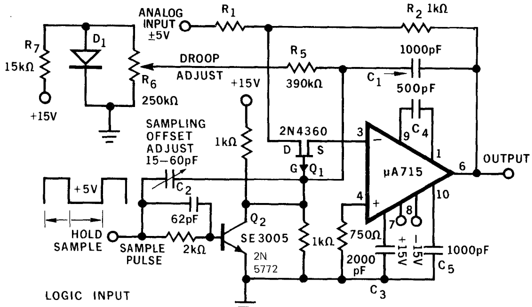
μA722/μA715 op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.



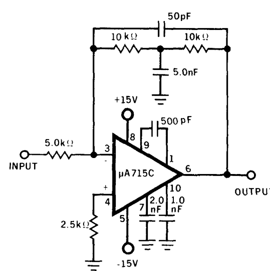
Conversion Rate
6 bits - 300 ns
8 bits - 600 ns
10 bits - 1000 ns

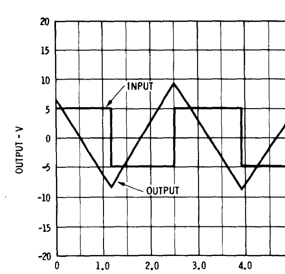
NOTE:
Contact Fairchild for additional information including how to increase conversion speed by clamping LSB's and how to obtain bipolar outputs.

HIGH SPEED SAMPLE AND HOLD



HIGH SPEED INTEGRATOR





μA725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA725 is a monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is pin compatible with the popular μA741 operational amplifier.

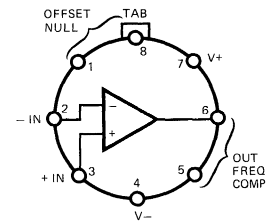
- **LOW INPUT NOISE CURRENT – 0.15 pA/$\sqrt{Hz}$**
- **HIGH OPEN LOOP GAIN – 3,000,000**
- **LOW INPUT OFFSET CURRENT – 2 nA**
- **LOW INPUT VOLTAGE DRIFT – 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION – 120 dB**
- **HIGH INPUT VOLTAGE RANGE – ±14 V**
- **WIDE POWER SUPPLY RANGE – ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Mini Dip	310 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±22 V
Voltage Between Offset Null and V^+	±0.5 V
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini Dip	−55°C to +125°C
Operating Temperature Range	
Military (μA725A, μA725)	−55°C to +125°C
Commercial (μA725E, μA725C)	0°C to +70°C
Pin Temperature	
Metal Can (Soldering, 60 s)	300°C

CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)

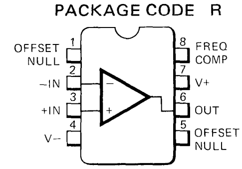
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA725A	μA725AHM
μA725	μA725HM
μA725C	μA725HC
μA725E	μA725EHC

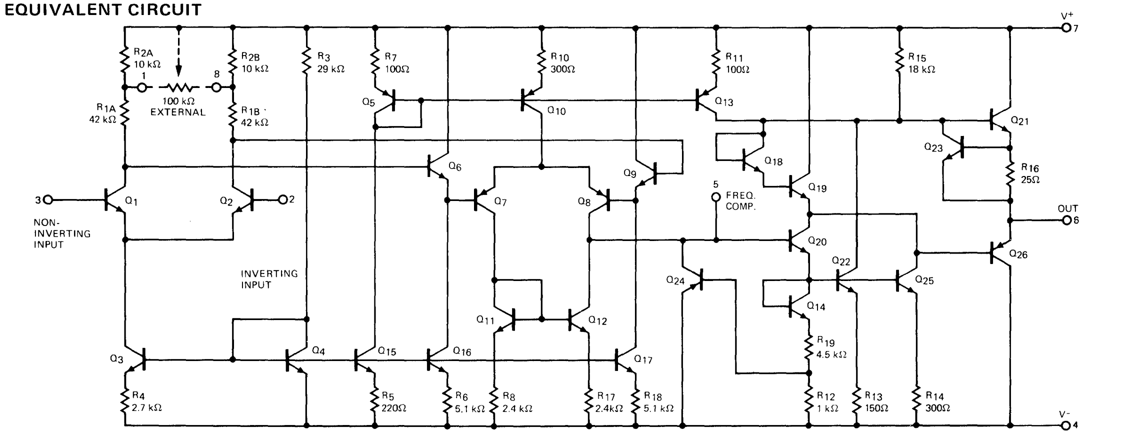
PACKAGE OUTLINE 6T
PACKAGE CODE R



ORDER INFORMATION

TYPE	PART NO.
μA725A	μA725ARM
μA725	μA725RM
μA725C	μA725RC
μA725E	μA725ERC

EQUIVALENT CIRCUIT



Notes on following pages

*Planar is a patented Fairchild process.

μA725A

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

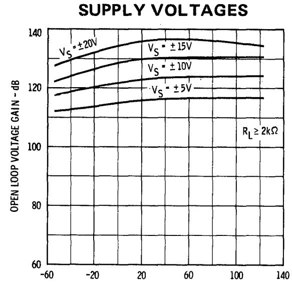
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	f_o = 10 Hz			15	nV/$\sqrt{Hz}$
	f_o = 100 Hz			12	nV/$\sqrt{Hz}$
	f_o = 1 kHz			12	nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz			1.2	pA/$\sqrt{Hz}$
	f_o = 100 Hz			0.6	pA/$\sqrt{Hz}$
	f_o = 1 kHz			0.25	pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω, V_{OUT} = ±0.5 V, V_S = ±3 V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	120	130		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	5.0	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5			V
	$R_L \geq 2$ kΩ	±10			V
Output Resistance			150		Ω
Power Consumption			80	120	mW
	V_S = ±3 V			6.0	mW

The following specifications apply for −55°C ≤ T_A ≤ +125°C unless otherwise specified:

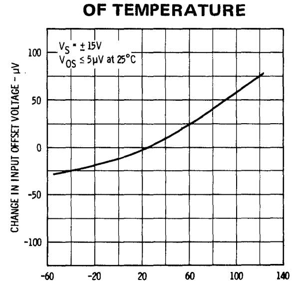
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without External trim)	$R_S \leq 10$ kΩ			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50 Ω			2.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50 Ω		0.6	1.0	μV/°C
Input Offset Current	T_A = +125°C			4.0	nA
	T_A = −55°C		5.0	18	nA
Average Input Offset Current Drift				90	pA/°C
Input Bias Current	T_A = +125°C			70	nA
	T_A = −55°C			180	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = +125°C	1,000,000			V/V
	$R_L \geq 2$ kΩ, T_A = −55°C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			8.0	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES FOR μA725A AND μA725

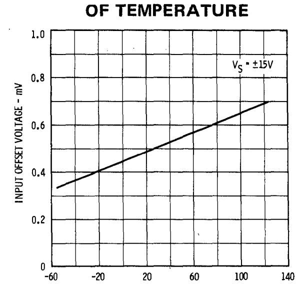
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



μA725

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10\ k\Omega$		0.5	1.0	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	f_o = 10 Hz		15		$nV/\sqrt{Hz}$
	f_o = 100 Hz		9.0		$nV/\sqrt{Hz}$
	f_o = 1 kHz		8.0		$nV/\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		$pA/\sqrt{Hz}$
	f_o = 100 Hz		0.3		$pA/\sqrt{Hz}$
	f_o = 1 kHz		0.15		$pA/\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±13.5		V
	$R_L \geq 2\ k\Omega$	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	105	mW

The following specifications apply for $-55°C \leq T_A \leq +125°C$ unless otherwise specified:

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10\ k\Omega$			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50\Omega$		2.0	5.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50\Omega$		0.6		μV/°C
Input Offset Current	T_A = +125°C		1.2	20	nA
	T_A = −55°C		7.5	40	nA
Average Input Offset Current Drift			35	150	pA/°C
Input Bias Current	T_A = +125°C		20	100	nA
	T_A = −55°C		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, T_A = +125°C	1,000,000			V/V
	$R_L \geq 2\ k\Omega$, T_A = −55°C	250,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	100			dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			20	μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±10			V

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and hermetic mini dip.
2. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

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μA725E

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

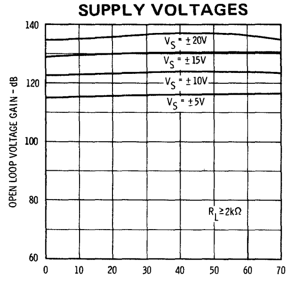
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	f_O = 10 Hz			15	nV/√Hz
	f_O = 100 Hz			12	nV/√Hz
	f_O = 1 kHz			12	nV/√Hz
Input Noise Current	f_O = 10 Hz			1.2	pA/√Hz
	f_O = 100 Hz			0.6	pA/√Hz
	f_O = 1 kHz			0.25	pA/√Hz
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω, V_{OUT} = ±0.5 V, V_S = ±3 V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	120			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	5.0	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5			V
	$R_L \geq 2$ kΩ	±10			V
Output Resistance			150		Ω
Power Consumption			80	150	mW
	V_S = ±3 V			6.0	mW

The following specifications apply for 0°C ≤ T_A ≤ +70°C unless otherwise specified:

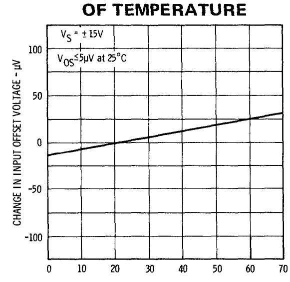
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50 Ω			2.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50 Ω			1.0	μV/°C
Input Offset Current	T_A = +70°C		1.2	4.0	nA
	T_A = 0°C		4.0	18	nA
Average Input Offset Current Drift			10	90	pA/°C
Input Bias Current	T_A = +70°C			70	nA
	T_A = 0°C			180	nA
Large Signal Voltage	$R_L \geq 2$ kΩ, T_A = +70°C	1,000,000			V/V
	$R_L \geq 2$ kΩ, T_A = 0°C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			8.0	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES FOR μA725E AND μA725C

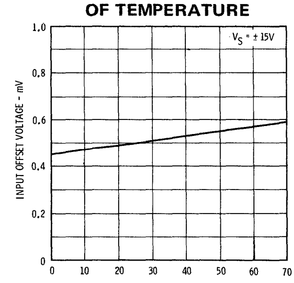
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



μA725C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/ $\sqrt{Hz}$
	f_o = 100 Hz		9.0		nV/ $\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/ $\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/ $\sqrt{Hz}$
	f_o = 100 Hz		0.3		pA/ $\sqrt{Hz}$
	f_o = 1 kHz		0.15		pA/ $\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	250,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW

The following specifications apply for 0°C ≤ T_A ≤ +70°C unless otherwise specified:

Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0		μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
	T_A = +70°C		1.2	35	nA
	T_A = 0°C		4.0	50	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current	T_A = +70°C			125	nA
	T_A = 0°C			250	nA
Large Signal Voltage	$R_L \geq 2$ kΩ, T_A = +70°	125,000			V/V
	$R_L \geq 2$ kΩ, T_A = 0°C	125,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

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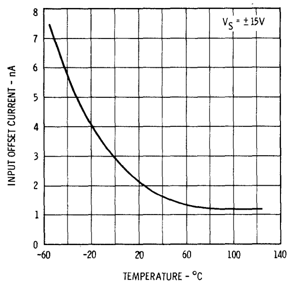
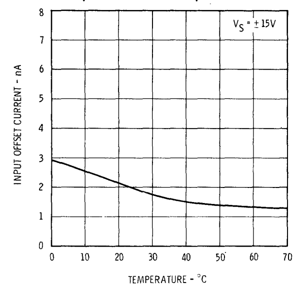
TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

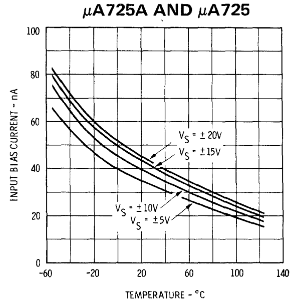
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE μA725A AND μA725



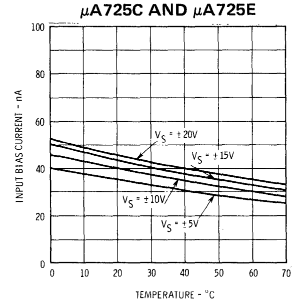
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE μA725C AND μA725E



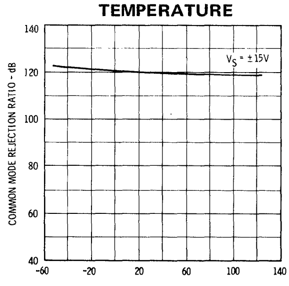
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE μA725A AND μA725



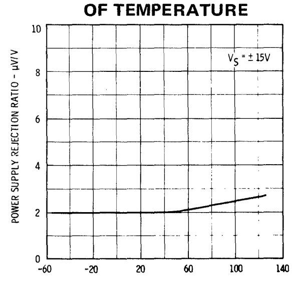
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE μA725C AND μA725E



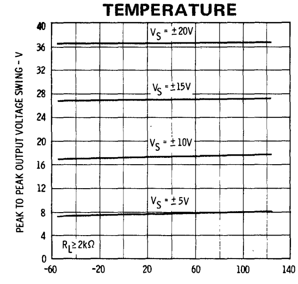
COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



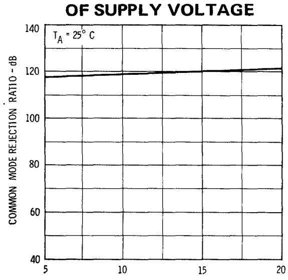
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



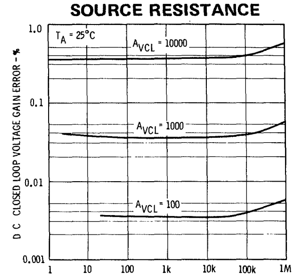
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



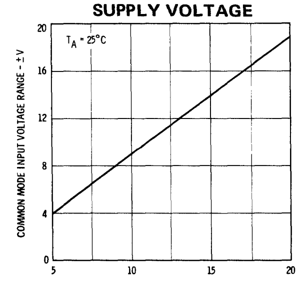
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



DC CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE

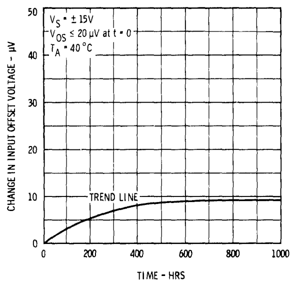


COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

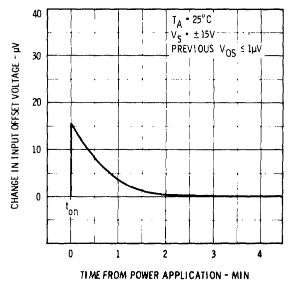


TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

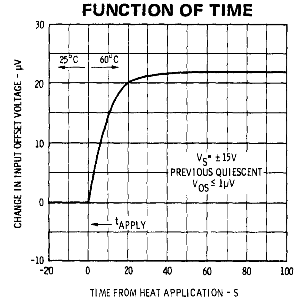
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



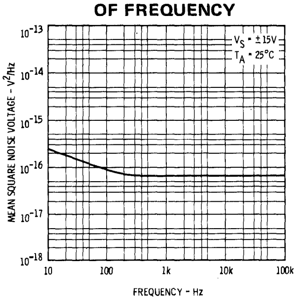
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN ON



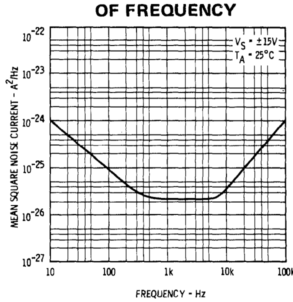
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



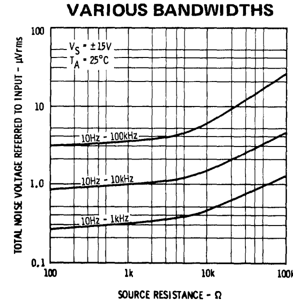
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



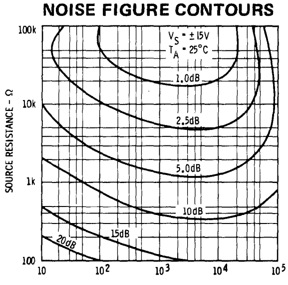
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



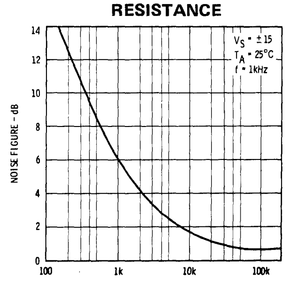
BROAD BAND NOISE FOR VARIOUS BANDWIDTHS



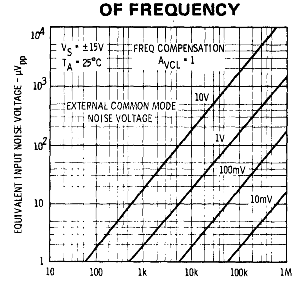
NARROW BAND SPOT NOISE FIGURE CONTOURS



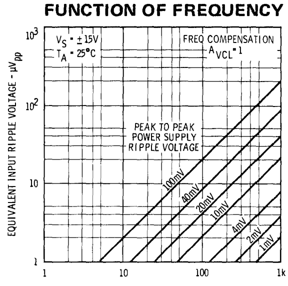
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



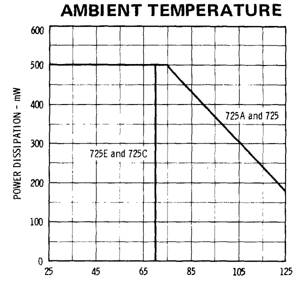
EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY



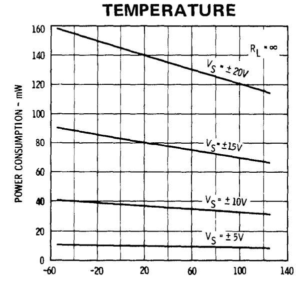
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



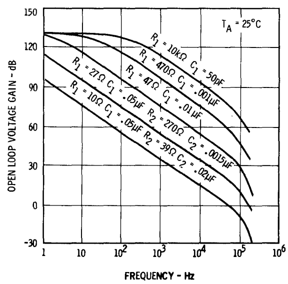
POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE



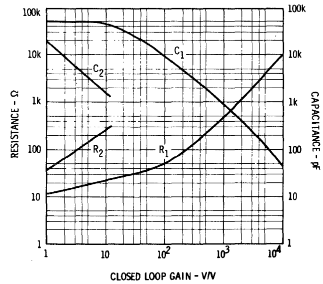
5

TYPICAL PERFORMANCE CURVES FOR ALL TYPES

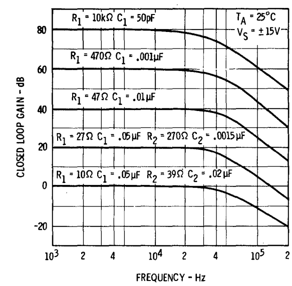
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



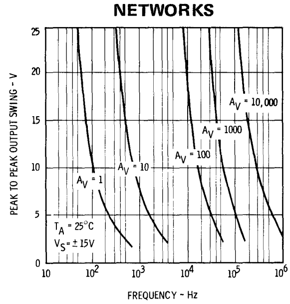
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



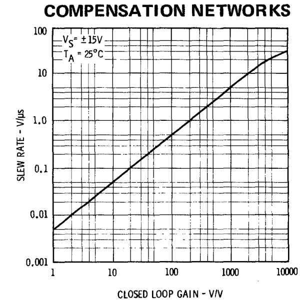
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



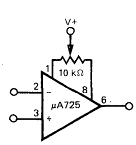
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



SLEW RATE AS A FUNCTION OF CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



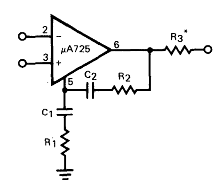
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

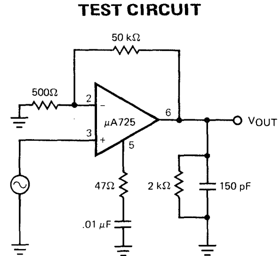
A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	–	–
1,000	470	.001	–	–
100	47	.01	–	–
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



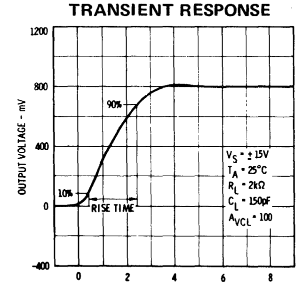
*Use R_3 = 51Ω when the amplifier is operated with capacitive load.

TRANSIENT RESPONSE TEST CIRCUIT



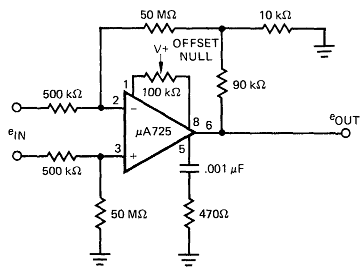
Pin numbers are shown for metal can only.

TRANSIENT RESPONSE



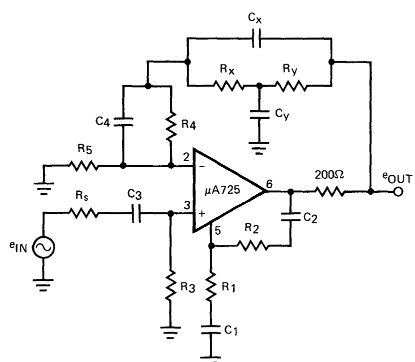
TYPICAL APPLICATIONS

PRECISION AMPLIFIER — A_{VCL} = 1000

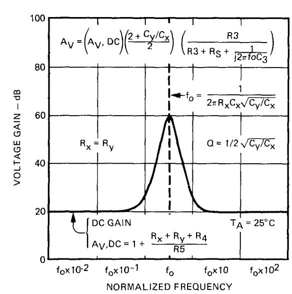


CHARACTERISTICS:
- A_V = 1000 = 60 dB
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for −0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability e_{IN} = 10 μV on V_{CMI} = 1.0 V
- Caution: Minimize Stray Capacitance

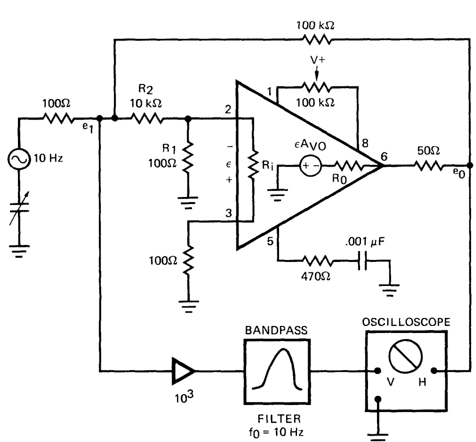
ACTIVE FILTER — BAND PASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE



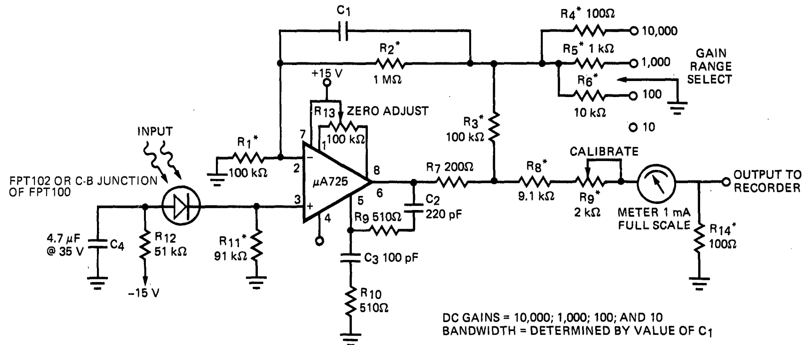
OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



$$A_{VO} \simeq \frac{e0}{e_1}\left(\frac{R2\,Ri + R1\,R_i + R1\,R2}{R1\,R_i}\right) = \frac{e_0}{e_1}\,101$$

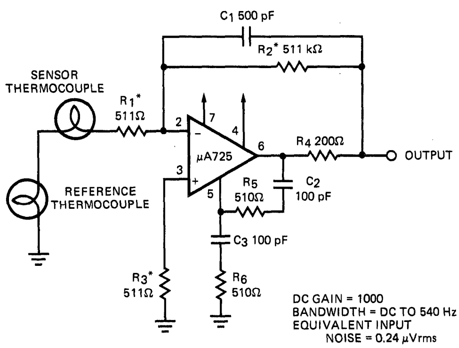
TYPICAL APPLICATIONS (Cont'd)

PHOTODIODE AMPLIFIER



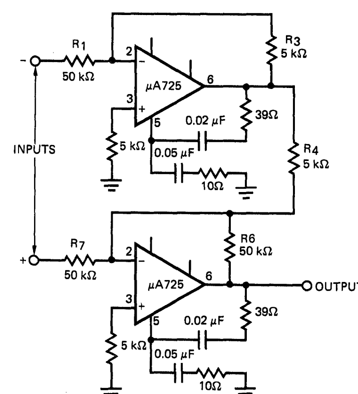
NOTE: *Indicates ±1% metal film resistors recommended for temperature stability.

THERMOCOUPLE AMPLIFIER



NOTE: *Indicates ±1 % metal film resistors recommended for temperature stability.

±100 V COMMON MODE RANGE DIFFERENTIAL AMPLIFIER



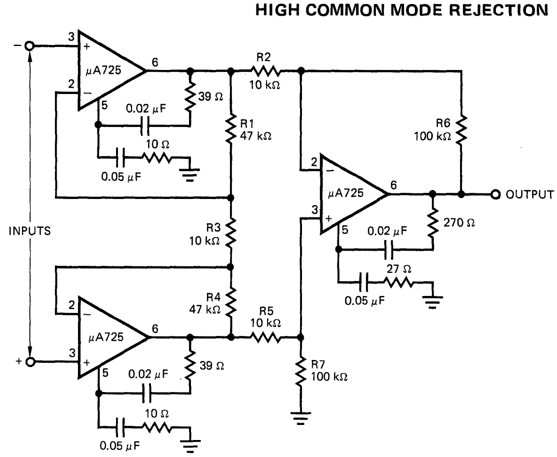
$$\frac{R1}{R6} = \frac{R3}{R4} \text{ for best CMRR}$$

$R3 = R4$

$R1 = R6 = 10\ R3$

$$\text{Gain} = \frac{R6}{R7}$$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$$\frac{R2}{R5} = \frac{R6}{R7} \text{ for best CMR}$$

$R1 = R4$

$R2 = R5$

$$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2\ R1}{R3}\right)$$

μA730

DIFFERENTIAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

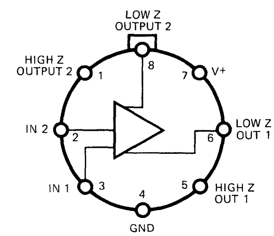
GENERAL DESCRIPTION – The μA730 is a Differential Amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military (μA730)	−55°C to +125°C
Commercial (μA730C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 s)	300°C

NOTE:
1. Rating applies for ambient temperature to +70°C; derate linearly at 6.3 mW/°C for ambient temperatures above +70°C.

CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



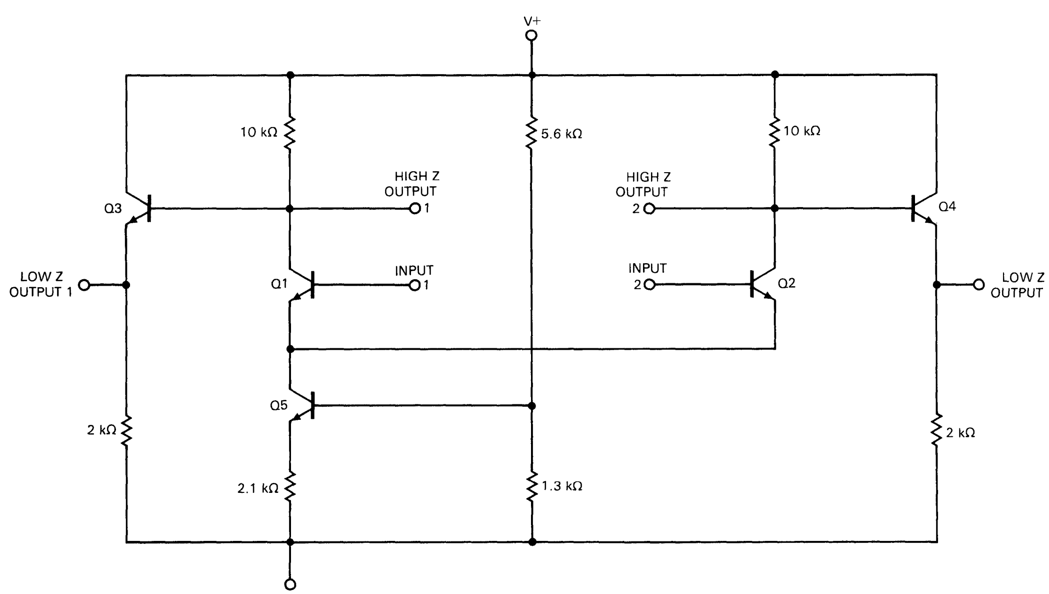
NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA730	μA730HM
μA730C	μA730HC

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



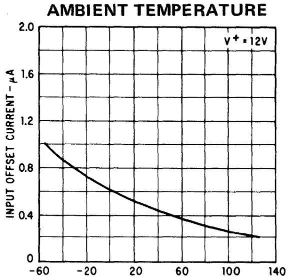
μA730

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, and V_{CM} = 3.5 V unless otherwise specified)

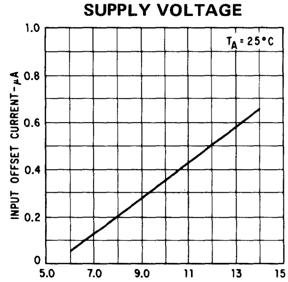
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mV_{pk-pk}
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		V_{pk-pk}
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for −55°C ≤ T_A ≤ 125°C:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	T_A = +125°C		0.2	1.5	μA
	T_A = −55°C		1.0	3.0	μA
Input Bias Current	T_A = −55°C		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ f ≤ 1.0 kHz, +3.5V ≤ V_{CM} ≤ +5.2V	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		V_{pk-pk}
Supply Current	T_A = −55°C		10	15	mA
	T_A = 125°C		8.0	11	mA
Power Consumption	T_A = −55°C		120	180	mW
	T_A = 125°C		96	121	mW

TYPICAL PERFORMANCE CURVES FOR μA730

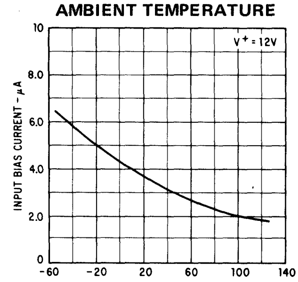
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



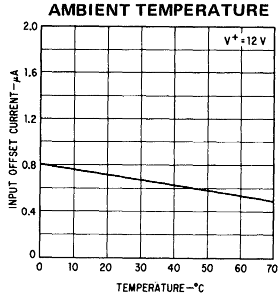
μA730C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, and V_{CM} = 3.5 V unless otherwise specified)

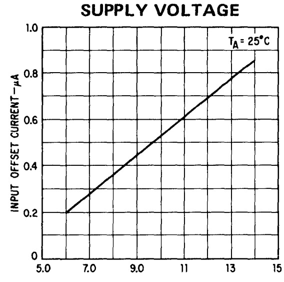
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVp-p
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		V_{pk-pk}
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	T_A = +70°C		0.5	3.0	μA
	T_A = 0°C		0.8	5.0	μA
Input Bias Current	T_A = 0°C		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ f ≤ 1.0 kHz, +3.5V ≤ V_{CM} ≤ +5.2V	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		V_{pk-pk}
Supply Current	T_A = 0°C		10	15	mA
	T_A = +70°C		8.8	13	mA
Power Consumption	T_A = 0°C		120	180	mW
	T_A = +70°C		106	156	mW

TYPICAL PERFORMANCE CURVES FOR μA730C

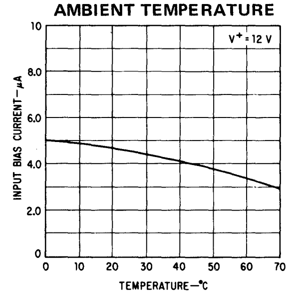
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

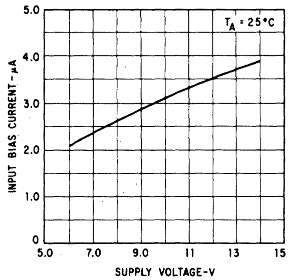


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

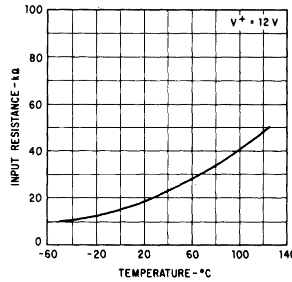


TYPICAL PERFORMANCE CURVES FOR μA730

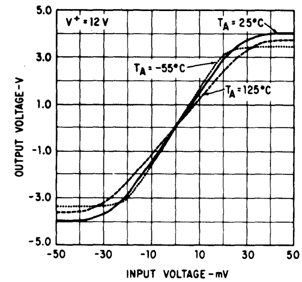
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



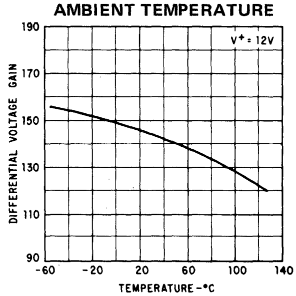
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



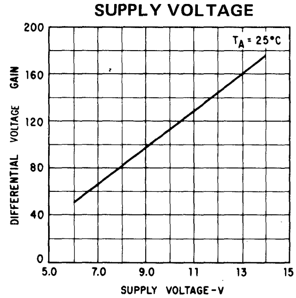
VOLTAGE TRANSFER CHARACTERISTICS



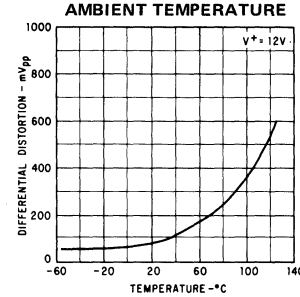
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



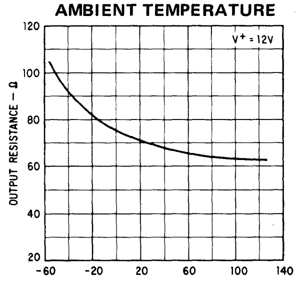
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



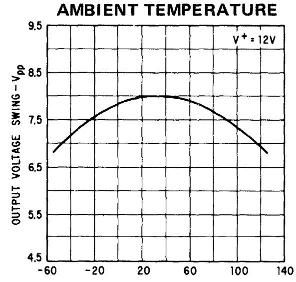
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



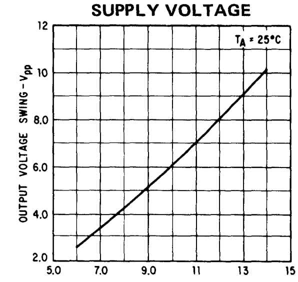
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



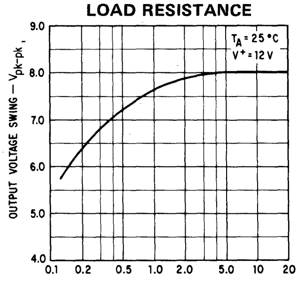
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



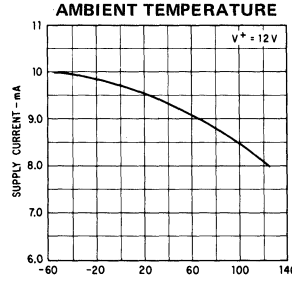
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



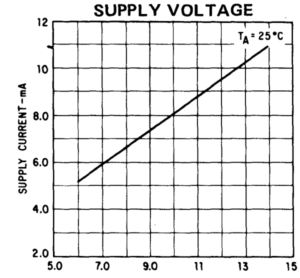
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

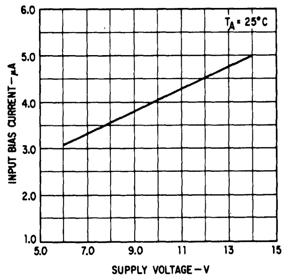


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

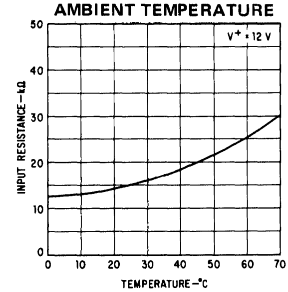


TYPICAL PERFORMANCE CURVES FOR μA730C

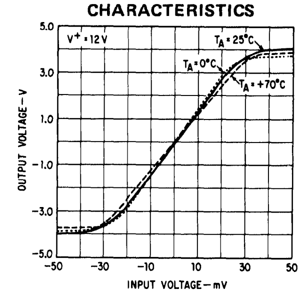
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



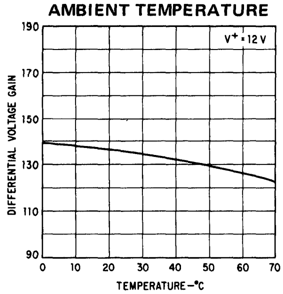
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



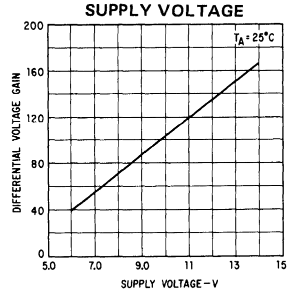
VOLTAGE TRANSFER CHARACTERISTICS



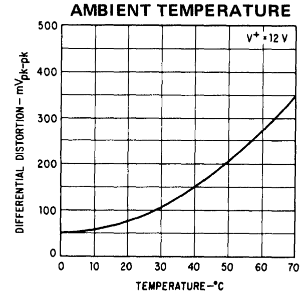
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



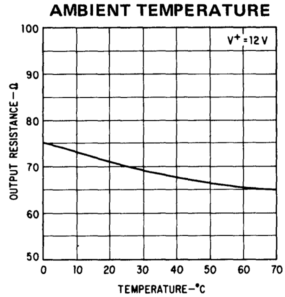
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



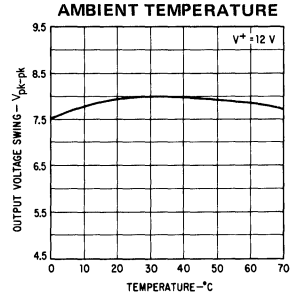
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



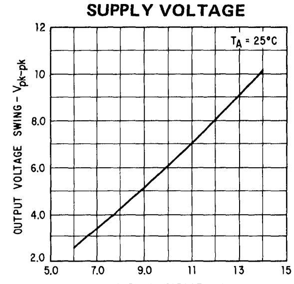
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



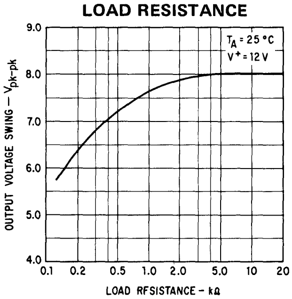
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



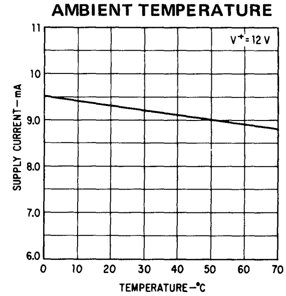
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



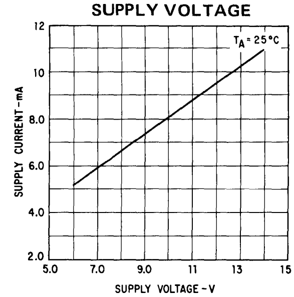
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

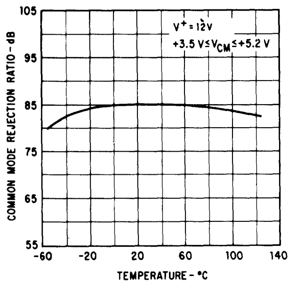


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

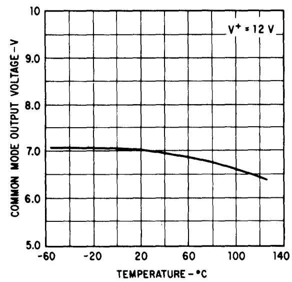


TYPICAL PERFORMANCE CURVES FOR μA730 AND μA730C

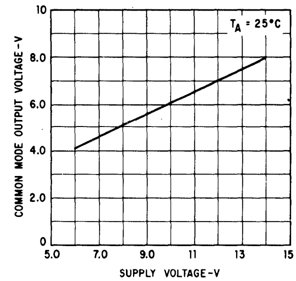
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA739

DUAL LOW-NOISE AUDIO PREAMPLIFIER/OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

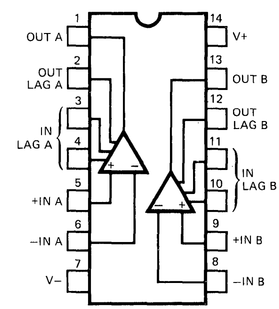
GENERAL DESCRIPTION — The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Hermetic	−65°C to +150°C
Molded	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

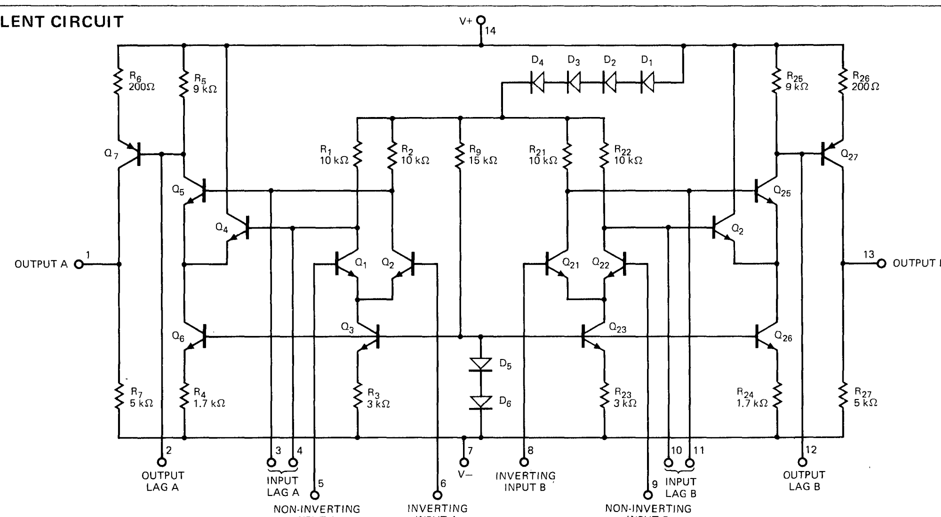
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA739C	**μA739DC**
μA739C	**μA739PC**

EQUIVALENT CIRCUIT



Notes on following page

*Planar is a patented Fairchild process.

μA739C

ELECTRICAL CHARACTERISTICS: V_S = ±15V, R_L = 50 kΩ to Pin 7, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S ≤200Ω		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±5.0V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		–14	–15		V
Output Resistance	f = 1.0kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	R_S ≤10kΩ	70	90		dB
Supply Voltage Rejection Ratio	R_S ≤10kΩ		50		μV/V
Power Consumption	V_{OUT} = 0		270	420	mW
Supply Current	V_{OUT} = 0		9.0	14	mA
Broadband Noise Figure	R_S = 5.0kΩ, BW = 10Hz to 10kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, V_{IN} = ±20mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, V_{IN} = ±20mV		0.3		μs
Slew Rate (unity gain) [See Figure 2]	C_1 = 0.1μF, R_1 = 4.7Ω		1.0		V/μs
Channel Separation (See Figure 3)	R_S ≤10kΩ, f = 10kHz		140		dB
The following specifications apply for V_S = ±4.0V, T_A = 25°C					
Input Offset Voltage	R_S ≤200Ω		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	V_{OUT} = 0		2.5		mA
Power Consumption	V_{OUT} = 0		20		mW
Large Signal Voltage Gain	V_{OUT} = ±1.0V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		–3.6	–4.0		V

NOTES:

1. Rating applies at ambient temperature below 70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

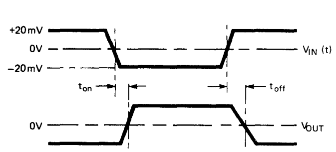


Fig. 1

FREQUENCY RESPONSE TEST CIRCUIT

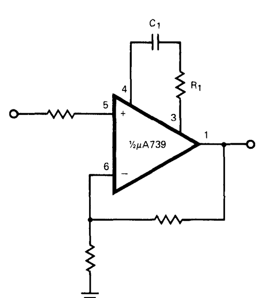


Fig. 2

CHANNEL SEPARATION TEST CIRCUIT

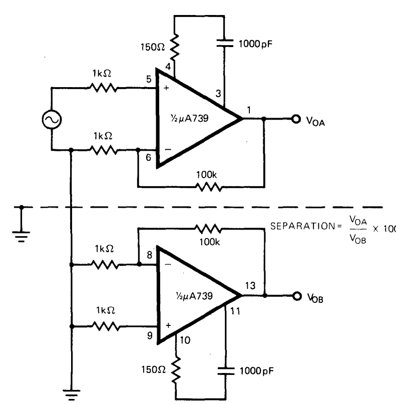
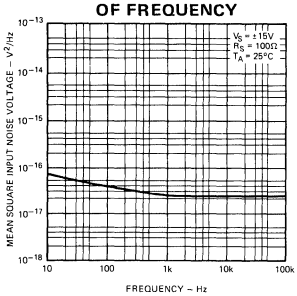


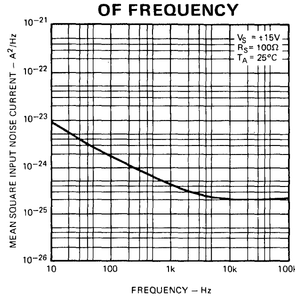
Fig. 3

TYPICAL PERFORMANCE CURVES FOR μA739C

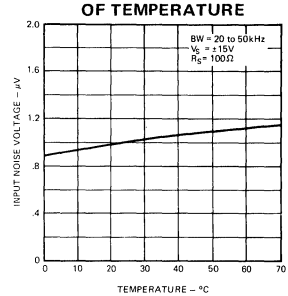
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



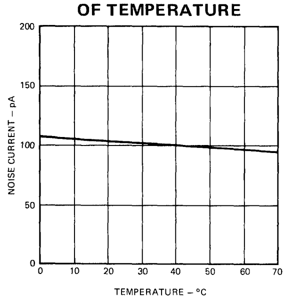
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



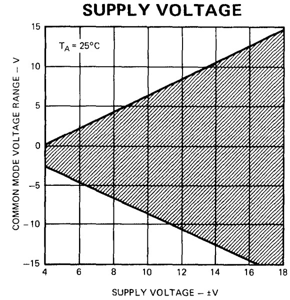
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



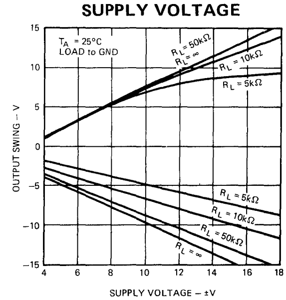
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



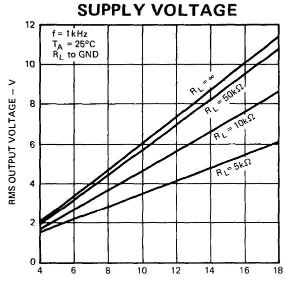
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



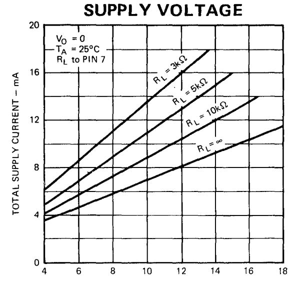
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



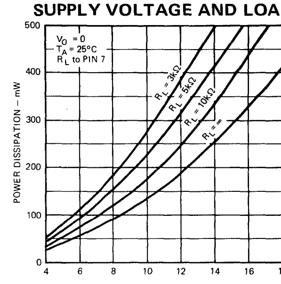
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



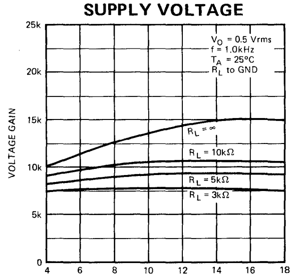
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



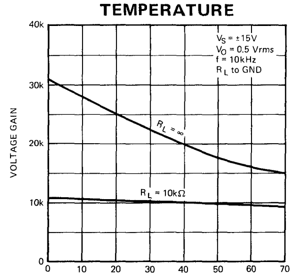
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



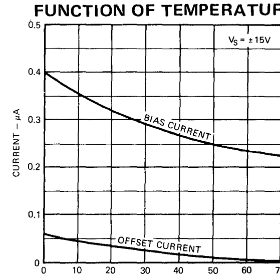
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

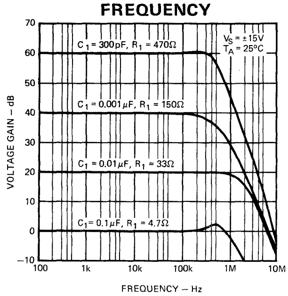


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTION OF TEMPERATURE

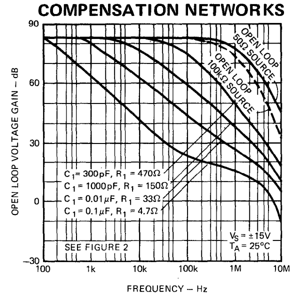


TYPICAL PERFORMANCE CURVES FOR μA739C

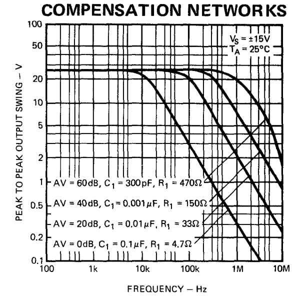
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



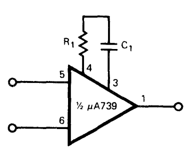
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



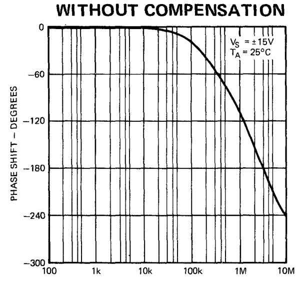
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



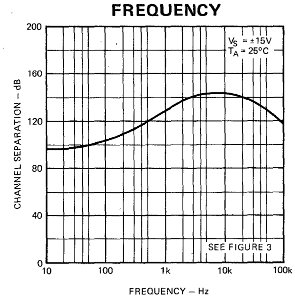
FREQUENCY COMPENSATION NETWORK



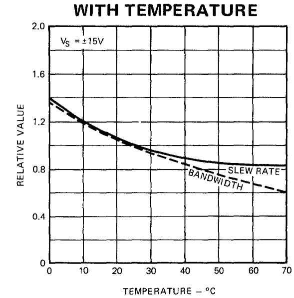
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

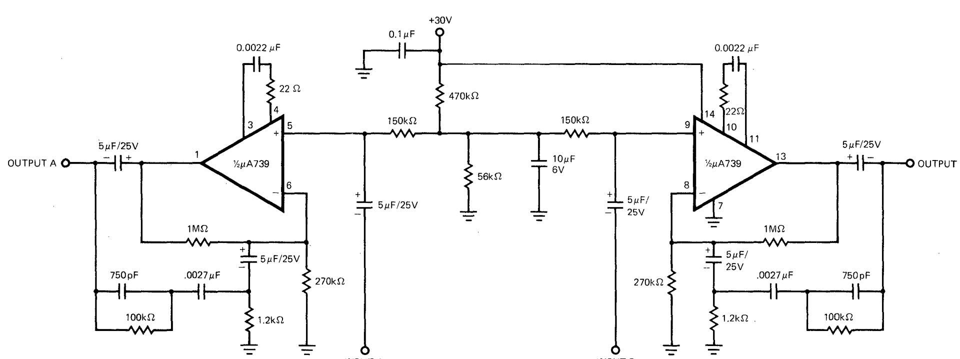


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER – RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40dB at 1kHz, RIAA equalized
Input overload point, 80mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74dB below 10mV
Channel separation @ 1kHz, 80dB

μA740

FET INPUT OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

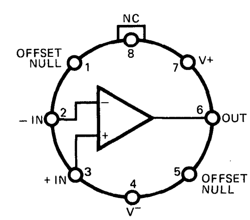
5

GENERAL DESCRIPTION – The μA740 is a high performance monolithic FET Input Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of latch-up make the μA740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample-and-hold circuits, transducer amplifiers, and other general feedback applications. The μA740 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

- **HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **NO LATCH UP**

CONNECTION DIAGRAM

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



NOTE: Pin 4 Connected to Case.

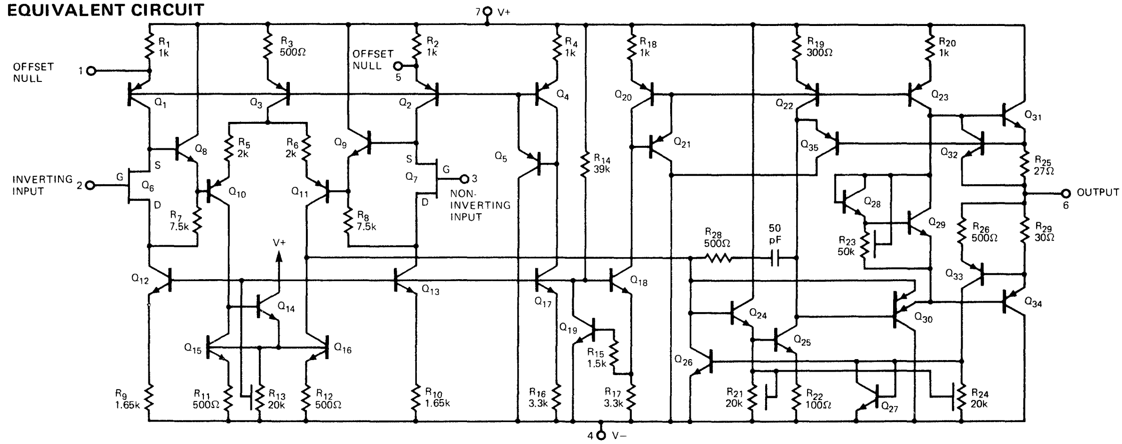
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA740)	−55°C to +125°C
Commercial (μA740C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ORDER INFORMATION

TYPE	PART NO.
μA740	μA740HM
μA740C	μA740HC

EQUIVALENT CIRCUIT



Notes on following pages.

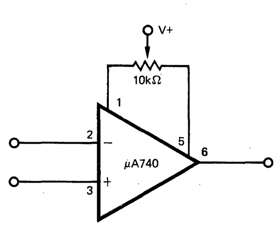
*Planar is a patented Fairchild process.

μA740

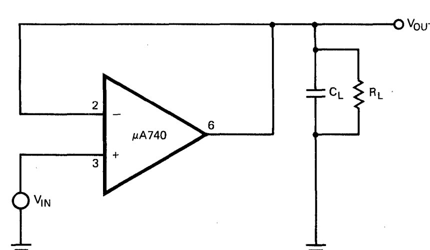
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_C = 25^oC$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 100\,k\Omega$		10	20	mV
Input Offset Current [Note 4]			40	150	pA
Input Current (either input) [Note 4]			100	200	pA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$	50,000	1,000,000		V/V
Output Resistance			75		Ω
Output Short Circuit Current			20		mA
Common Mode Rejection Ratio		64	80		dB
Supply Voltage Rejection Ratio			70	300	μV/V
Supply Current			4.2	5.2	mA
Power Consumption			126	156	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			3.0		MHz
Transient Response (Unity Gain) — Rise Time	$C_L \leqslant 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$		110		ns
Transient Response (Unity Gain) — Overshoot	$C_L \leqslant 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$		10	20	%
The following specifications apply for $T_C = -55^oC$ to $+85^oC$:					
Input Voltage Range		±10		±12	V
Large Signal Voltage Gain	$R_L \geqslant 2\,k\Omega$, $V_{OUT} = \pm 10\,V$	25,000			V/V
Output Voltage Swing	$R_L \geqslant 10k\Omega$	±12	±14		V
	$R_L \geqslant 2k\Omega$	±10	±13		V
Input Offset Voltage	$R_S \leqslant 100k\Omega$		15	30	mV
Input Offset Current	$T_A = -55^oC$		30		pA
	$T_A = +85^oC$		185		pA
Input Current (either input)	$T_A = -55^oC$			200	pA
	$T_A = +85^oC$		2.5	4.0	nA

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



μA740C

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_C = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leqslant 100k\Omega$		30	110	mV
Input Offset Current (Note 4)				60	300	pA
Input Current (either input) [Note 4]				0.1	2.0	nA
Input Resistance				1,000,000		MΩ
Large Signal Voltage Gain		$R_L \geqslant 2k\Omega$, V_{OUT} = ±10V	20,000	1,000,000		V/V
Output Resistance				75		Ω
Output Short Circuit Current				20		mA
Supply Current				4.2	8.0	mA
Power Consumption				126	240	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				1.0		MHz
Transient Response (Unity Gain)	Rise Time	$C_L \leqslant 100pF$, $R_L = 2k\Omega$, V_{IN} = 100mV		300		ns
	Overshoot			10		%
The following specifications apply for $0^oC \leqslant T_A \leqslant +70^oC$:						
Input Voltage Range			±10	±12		V
Common Mode Rejection Ratio			55	80		dB
Supply Voltage Rejection Ratio				70	500	μV/V
Large Signal Voltage Gain		$R_L \geqslant 2k\Omega$, V_{OUT} = ±10V		500,000		V/V
Output Voltage Swing		$R_L \geqslant 10k\Omega$	±12	±14		V
		$R_L \geqslant 2k\Omega$	±10	±13		V
Input Offset Voltage				30		mV
Input Offset Current				60		pA
Input Current (either input)				1.1	10	nA

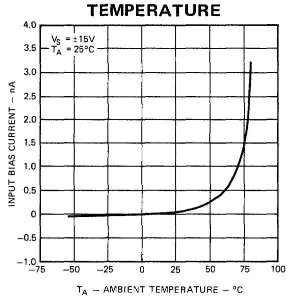
NOTES:

1. Rating applies for ambient temperature to +70°C; derate linearly at 6.3mW/°C for ambient temperatures above +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. Typically doubles for every 10°C increase in ambient temperature.

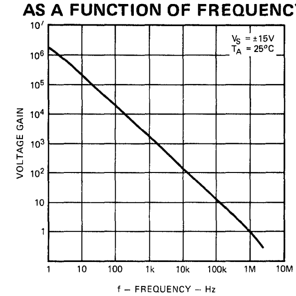
5

TYPICAL PERFORMANCE CURVES FOR μA740 AND μA740C

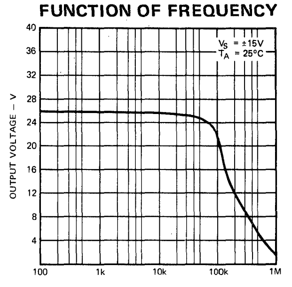
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



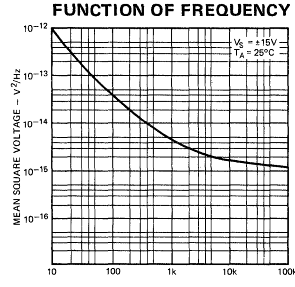
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



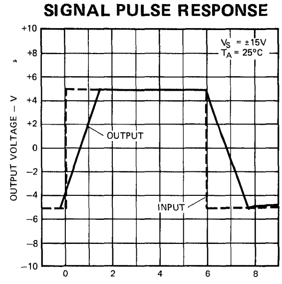
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



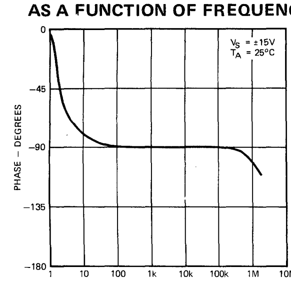
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

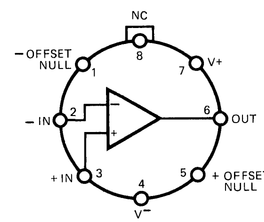
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Hermetic DIP, and Flatpak	−65°C to +150°C
Mini DIP, Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA741A, μA741)	−55°C to +125°C
Commercial (μA741E, μA741C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

CONNECTION DIAGRAMS

8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H

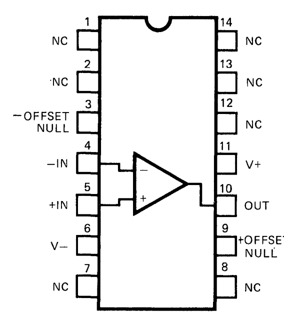


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AHM
μA741	μA741HM
μA741E	μA741EHC
μA741C	μA741HC

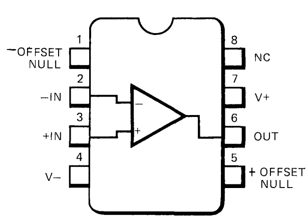
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741ADM
μA741	μA741DM
μA741E	μA741EDC
μA741C	μA741DC
μA741C	μA741PC

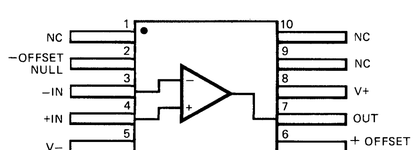
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES R T



ORDER INFORMATION

TYPE	PART NO.
μA741C	μA741TC
μA741C	μA741RC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AFM
μA741	μA741FM

Notes on following pages.

*Planar is a patented Fairchild process.

μA741A

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leqslant 50\Omega$			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift						0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		V_S = +20, −20; V_S = −20, +10V, R_S = 50Ω			15	50	μV/V
Output Short Circuit Current				10	25	40	mA
Power Dissipation		V_S = ±20V			80	150	mW
Input Impedance		V_S = ±20V		1.0	6.0		MΩ
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		50			V/mV
Transient Response	Rise Time				0.25	0.8	μs
(Unity Gain)	Overshoot				6.0	20	%
Bandwidth (Note 4)				.437	1.5		MHz
Slew Rate (Unity Gain)		V_{IN} = ±10V		0.3	0.7		V/μs
The following specifications apply for −55°C ≤ T_A ≤ +125°C							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Common Mode Rejection Ratio		V_S = ±20V, V_{IN} = ±15V, R_S = 50Ω		80	95		dB
Adjustment For Input Offset Voltage		V_S = ±20V		10			mV
Output Short Circuit Current				10		40	mA
Power Dissipation		V_S = ±20V	−55°C			165	mW
			+125°C			135	mW
Input Impedance		V_S = ±20V		0.5			MΩ
Output Voltage Swing		V_S = ±20V,	R_L = 10kΩ	±16			V
			R_L = 2kΩ	±15			V
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		32			V/mV
		V_S = ±5V, R_L = 2kΩ, V_{OUT} = ±2 V		10			V/mV

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

μA741

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°$C unless otherwise specified.

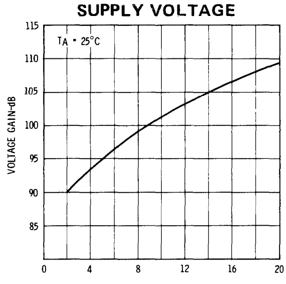
CHARACTERISTICS (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large Signal Voltage Gain	$R_L \geqslant 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain) — Rise time	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leqslant 100$ pF		0.3		μs
Transient Response (Unity Gain) — Overshoot	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leqslant 100$ pF		5.0		%
Slew Rate	$R_L \geqslant 2$ kΩ		0.5		V/μs

The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$:

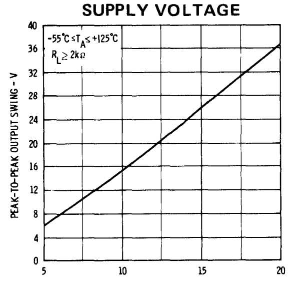
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geqslant 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geqslant 10$ kΩ	±12	±14		V
	$R_L \geqslant 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

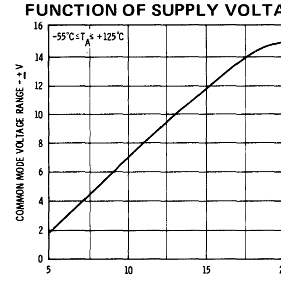
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

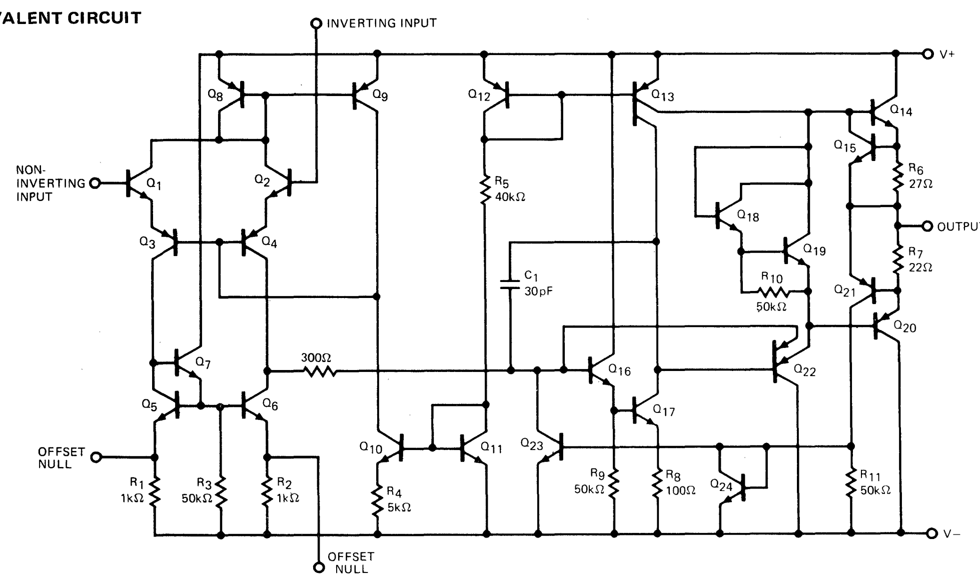


μA741E

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	μV/°C
Input Offset Current			3.0	30	nA
Average Input Offset Current Drift				0.5	nA/°C
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20$; $V_S = +20, -10$V, $R_S = 50\Omega$		15	50	μV/V
Output Short Circuit Current		10	25	40	mA
Power Dissipation	$V_S = \pm 20$V		80	150	mW
Input Impedance	$V_S = \pm 20$V	1.0	6.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 20$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 15$V	50			V/mV
Transient Response (Unity Gain) — Rise Time			0.25	0.8	μs
Transient Response (Unity Gain) — Overshoot			6.0	20	%
Bandwidth (Note 4)		.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{IN} = \pm 10$V	0.3	0.7		V/μs
The following specifications apply for $0°C \leq T_A \leq 70°C$					
Input Offset Voltage				4.0	mV
Input Offset Current				70	nA
Input Bias Current				210	nA
Common Mode Rejection Ratio	$V_S = \pm 20$V, $V_{IN} = \pm 15$V, $R_S = 50\Omega$	80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20$V	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20$V			150	mW
Input Impedance	$V_S = \pm 20$V	0.5			MΩ
Output Voltage Swing	$V_S = \pm 20$V, $R_L = 10k\Omega$	±16			V
Output Voltage Swing	$V_S = \pm 20$V, $R_L = 2k\Omega$	±15			V
Large Signal Voltage Gain	$V_S = \pm 20$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 15$V	32			V/mV
Large Signal Voltage Gain	$V_S = \pm 5$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 2$ V	10			V/mV

EQUIVALENT CIRCUIT



μA741C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geqslant 2$ kΩ, $V_{OUT} = \pm 10$ V	20,000	200,000		
Output Voltage Swing	$R_L \geqslant 10$ kΩ	±12	±14		V
	$R_L \geqslant 2$ kΩ	±10	±13		V
Output Resistance			75		Ω
Output Short Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain) — Rise time	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leqslant 100$ pF		0.3		μs
Transient Response (Unity Gain) — Overshoot			5.0		%
Slew Rate	$R_L \geqslant 2$ kΩ		0.5		V/μs

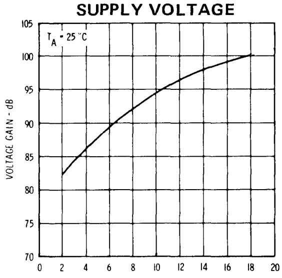
The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large Signal Voltage Gain	$R_L \geqslant 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geqslant 2$ kΩ	±10	±13		V

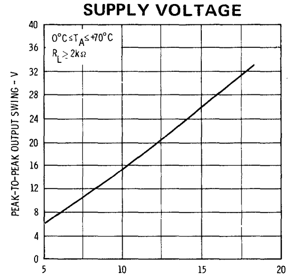
5

TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

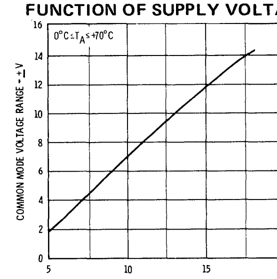
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

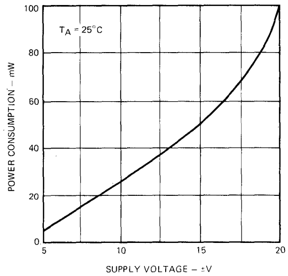


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

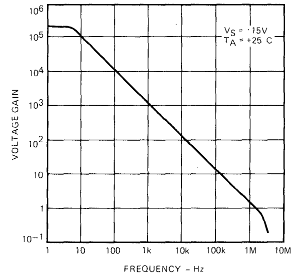


TYPICAL PERFORMANCE CURVES FOR μA741A, μA741, μA741E AND μA741C

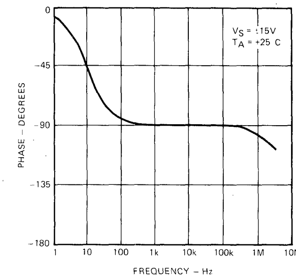
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



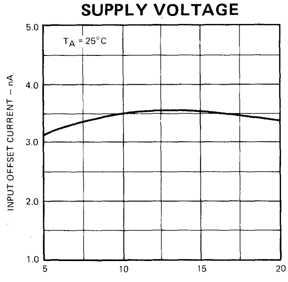
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



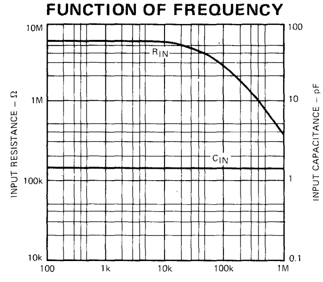
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



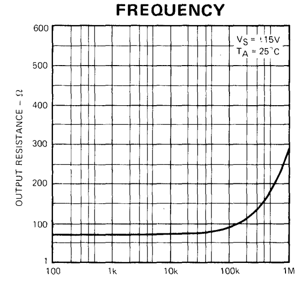
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



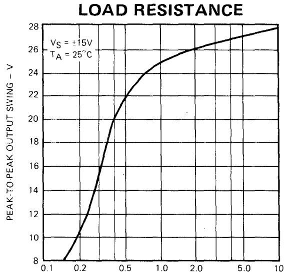
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



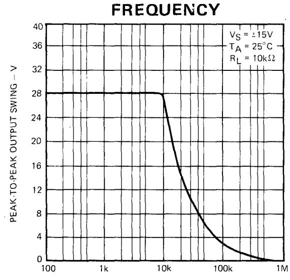
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



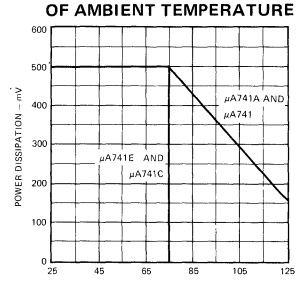
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



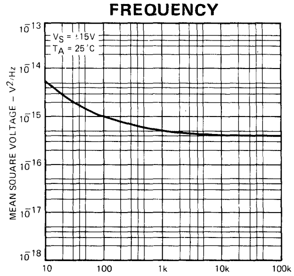
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



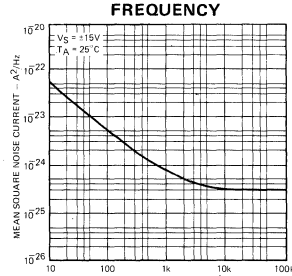
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



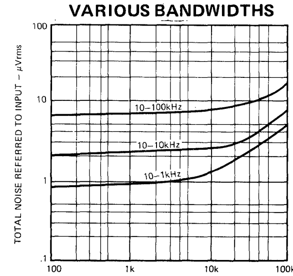
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

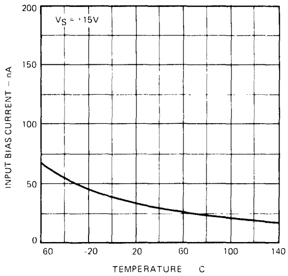


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

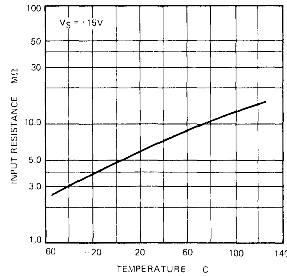


TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

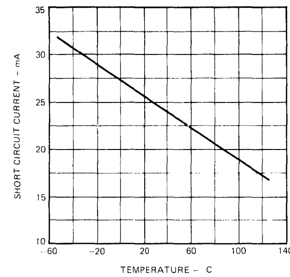
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



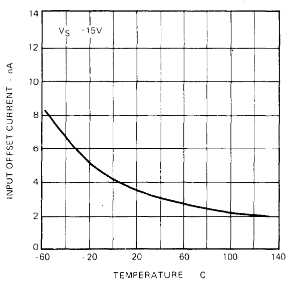
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



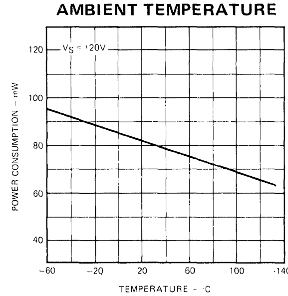
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



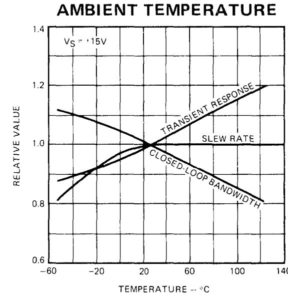
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

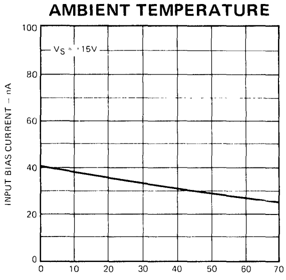


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

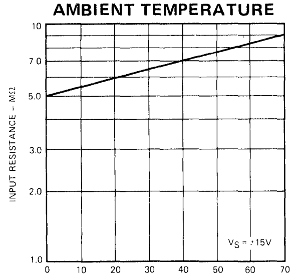


TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

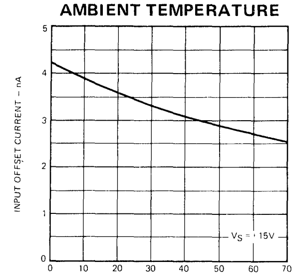
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



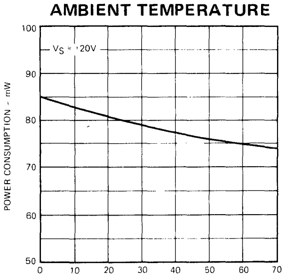
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



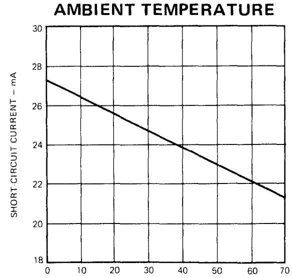
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



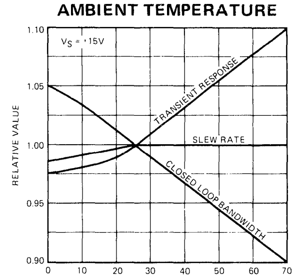
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



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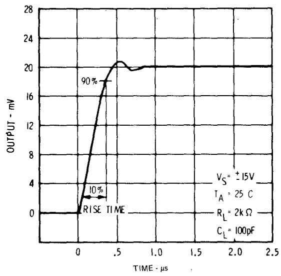
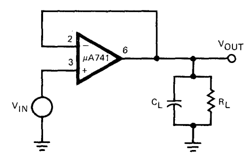
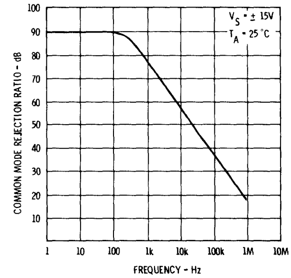
TRANSIENT RESPONSE



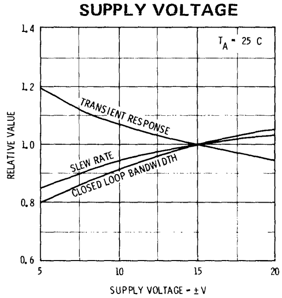
TRANSIENT RESPONSE TEST CIRCUIT



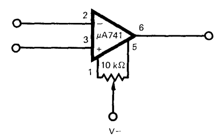
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



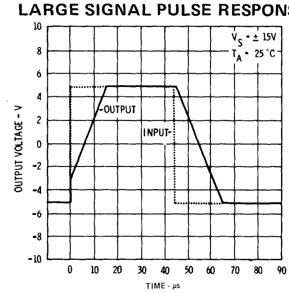
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

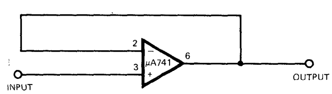


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



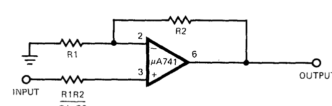
$R_{IN} = 400\ M\Omega$

$C_{IN} = 1\ pF$

$R_{OUT} << 1\ \Omega$

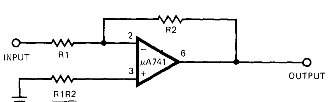
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



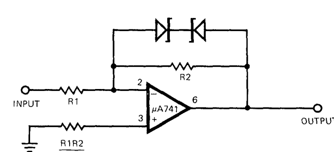
GAIN	R1	R2	B W	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R1	R2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER

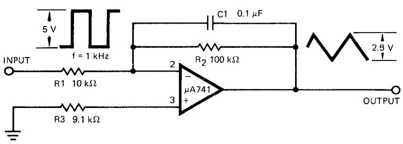


$$\frac{E_{OUT}}{E_{IN}} = \frac{R2}{R1} \text{ if } |E_{OUT}| \leq V_Z + 0.7\ V$$

where V_Z = Zener breakdown voltage

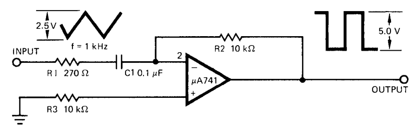
TYPICAL APPLICATIONS (Cont'd)

SIMPLE INTEGRATOR



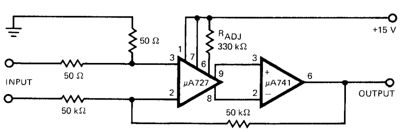
$$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$$

SIMPLE DIFFERENTIATOR



$$E_{OUT} = -R2C\frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

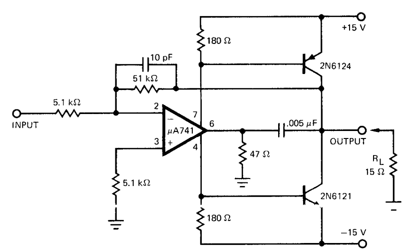


Voltage Gain = 10^3

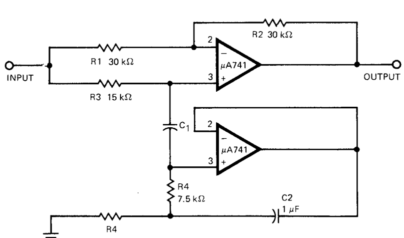
Input Offset Voltage Drift = 0.6 μV/°C

Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER



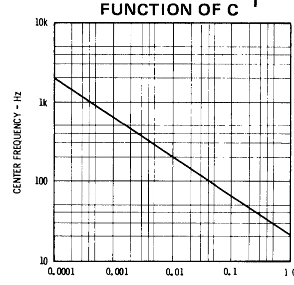
NOTCH FILTER USING THE μA741 AS A GYRATOR



Trim R3 such that

$$\frac{R1}{R2} = \frac{R3}{2\,R4}$$

NOTCH FREQUENCY AS A FUNCTION OF C_1



μA747

DUAL FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

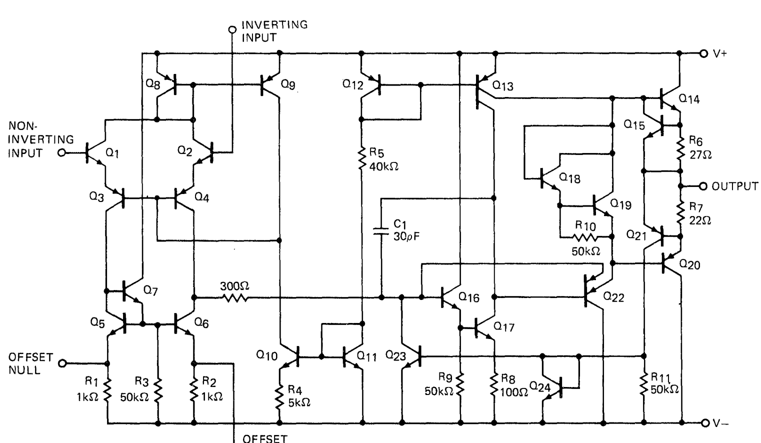
GENERAL DESCRIPTION — The μA747 is a pair of high performance monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

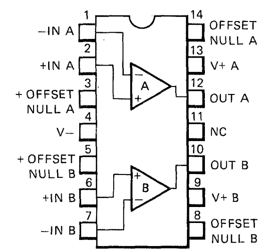
Supply Voltage	
Military (μA747A, μA747, μA747E)	±22 V
Commercial (μA747C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage betweeen Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA747A, μA747)	−55° C to +125°C
Commercial (μA747E, μA747C)	0°C to 70°C
Pin Temperature (Soldering 60 s)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT (1/2 μA747)



Notes on following pages.

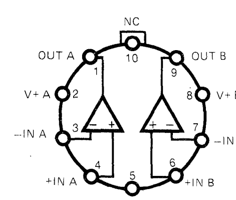
CONNECTION DIAGRAMS
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 7A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA747A	μA747ADM
μA747	μA747DM
μA747E	μA747EDC
μA747C	μA747DC
μA747C	μA747PC
μA747−I	μA747−IDM
μA747−IC	μA747−IDC

10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5N
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA747A	μA747AHM
μA747	μA747HM
μA747E	μA747EHC
μA747C	μA747HC
μA747−I	μA747−IHM
μA747−IC	μA747−IHC

NOTE:
V+A is internally connected to V+B for μA747A, μA747, μA747E, and μA747C. They are not internally connected for μA747-I and μA747-IC.

*Planar is a patented Fairchild process.

μA747A

ELECTRICAL CHARACTERISTICS: ±5 V ≤ V_S ≤ ±20 V, T_A = 25°C unless otherwise specified.

CHARACTERISTICS		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		R_S ≤ 50Ω			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift		T_A = 25°C to +125°C				0.2	nA/°C
		T_A = −55°C to +25°C				0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		V_S = +10 to +20, −20; V_S = +20, −10 to −20 R_S = 50 Ω			15	50	μV/V
Common Mode Rejection Ratio		V_S = ±20 V, V_{IN} = ±15 V R_S = 50 Ω		80	95		dB
Adjustment for Input Offset Voltage		V_S = ±20 V		10			mV
Output Short Circuit Current				10	25	40	mA
Power Dissipation		V_S = ±20 V per Channel			80	150	mW
Input Impedance		V_S = ±20 V		1.0	6		MΩ
Large Signal Voltage Gain		V_S = ±20 V, R_L = 2 kΩ V_{OUT} = ±15 V		50			V/mV
Transient Response (Unity Gain)	Rise Time				0.25	0.8	μs
	Overshoot				6.0	20	%
Bandwidth (Note 4)				0.437	1.5		MHz
Slew Rate (Unity Gain)		V_{IN} = ±10 V		0.3	0.7		V/μs
The following specifications apply for −55°C ≤ T_A ≤ +125°C							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Output Short Circuit Current				10		40	mA
Power Dissipation		V_S = ±20 V	−55°C			165	mW
			+125°C			135	mW
Input Impedance		V_S = ±20 V		0.5			MΩ
Output Voltage Swing		V_S = ±20 V, R_L = 10 kΩ		±16			V
		R_L = 2 kΩ		±15			V
Large Signal Voltage Gain		V_S = ±20 V, R_L = 2 kΩ, V_{OUT} = ±15 V		32			V/mV
		V_S = ± 5 V, R_L = 2 kΩ, V_{OUT} = ± 2 V		10			V/mV
Channel Separation		V_S = ±20 V		100			dB

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW\ (MHz) = \frac{0.35}{RISE\ TIME\ (\mu s)}$

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μA747

ELECTRICAL CHARACTERISTICS: Each Amplifier (V_S = ±15 V, T_A = 25°C unless otherwise specified)

CHARACTERISTICS (see definitions)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	50,000	200,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation				120		dB

The following specifications apply for −55°C ≤ T_A ≤ +125°C.

Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	T_A = +125°C		7.0	200	nA
	T_A = −55°C		85	500	nA
Input Bias Current	T_A = +125°C		0.03	0.5	μA
	T_A = −55°C		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	T_A = +125°C		1.5	2.5	mA
	T_A = −55°C		2.0	3.3	mA
Power Consumption	T_A = +125°C		45	75	mW
	T_A = −55°C		60	100	mW

μA747C

ELECTRICAL CHARACTERISTICS: Each Amplifier (V_S = ±15 V, T_A = 25°C unless otherwise specified)

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		R_S ≤10 kΩ		1.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		R_L ≥2 kΩ, V_{OUT} = ±10 V	25,000	200,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, C_L ≤ 100 pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		R_L ≥2 kΩ		0.5		V/μs
Channel Separation				120		dB

The following specifications apply for 0°C ≤ T_A ≤ +70°C.

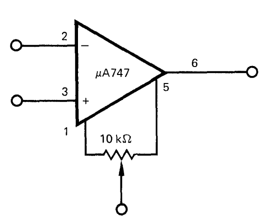
Input Offset Voltage	R_S ≤ 10 kΩ		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	R_S ≤10 kΩ	70	90		dB
Supply Voltage Rejection Ratio	R_S ≤10 kΩ		30	150	μV/V
Large Signal Voltage Gain	R_L ≥2 kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	R_L ≥10 kΩ	±12	±14		V
	R_L ≥2 kΩ	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

μA747E

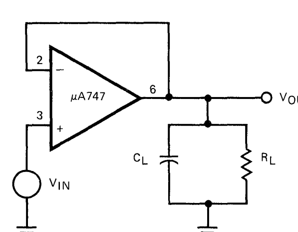
ELECTRICAL CHARACTERISTICS: $\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift					15	μV/°C
Input Offset Current				3	30	nA
Average Input Offset Current Drift		$T_A = 25°C$ to $70°C$ $T_A = 0°C$ to $25°C$			0.2 0.5	nA/°C nA/°C
Input Bias Current				30	80	nA
Power Supply Rejection Ratio		$V_S = +10, -20$; $V_S = +20\ V, -10\ V$ $R_S = 50\ \Omega$		15	50	μV/V
Common Mode Rejection Ratio		$V_S = \pm 20\ V$, $V_{IN} = \pm 15\ V$ $R_S = 50\ \Omega$	80	95		dB
Adjustment for Input Offset Voltage		$V_S = \pm 20\ V$	10			mV
Output Short Circuit Current			10	25	35	mA
Power Dissipation		$V_S = \pm 20\ V$		80	150	mW
Input Impedance		$V_S = \pm 20\ V$	1.0	6		MΩ
Large Signal Voltage Gain		$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15\ V$	50			V/mV
Transient Response (Unity Gain)	Rise Time			0.25	0.8	μs
	Overshoot			6	20	%
Bandwidth (Note 4)			0.437	1.5		MHz
Slew Rate (Unity Gain)		$V_{IN} = \pm 10\ V$	0.3	0.7		V/μs
The following specifications apply for $0°C \leq T_A \leq 70°C$						
Input Offset Voltage					4.0	mV
Input Offset Current					70	nA
Input Bias Current					210	nA
Output Short Circuit Current			10		40	mA
Power Dissipation		$V_S = \pm 20\ V$			165	mW
Input Impedance		$V_S = \pm 20\ V$	0.5			MΩ
Output Voltage Swing		$V_S = \pm 20\ V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±16 ±15			V V
Large Signal Voltage Gain		$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15\ V$	32			V/mV
		$V_S = \pm 5\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 2\ V$	10			V/mV
Channel Separation		$V_S = \pm 20\ V$	100			dB

VOLTAGE OFFSET NULL CIRCUIT

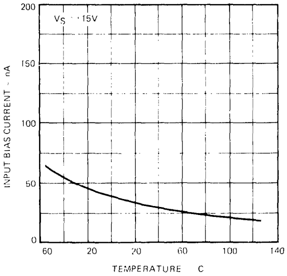


TRANSIENT RESPONSE TEST CIRCUIT

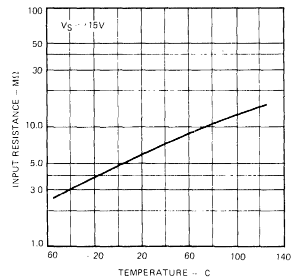


TYPICAL PERFORMANCE CURVES FOR μA747A AND μA747

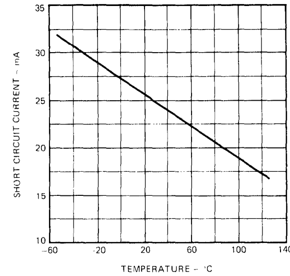
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



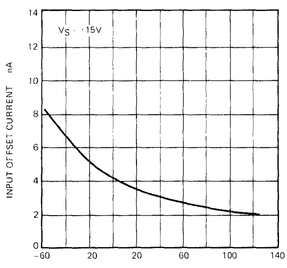
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



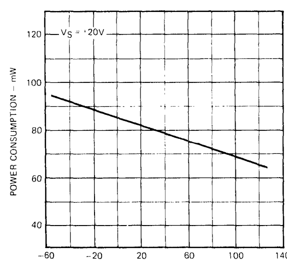
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



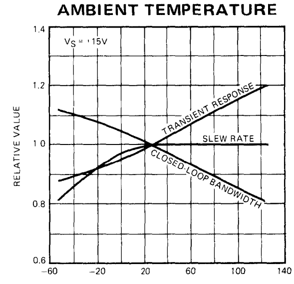
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

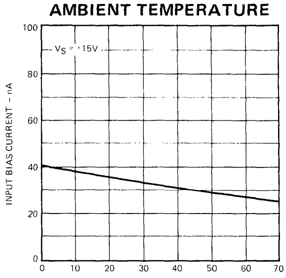


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

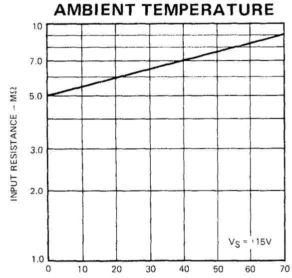


TYPICAL PERFORMANCE CURVES FOR μA747E AND μA747C

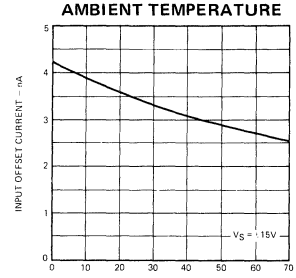
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



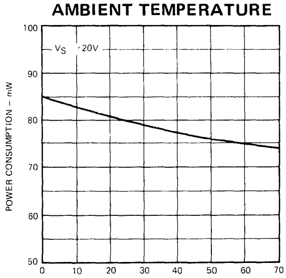
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



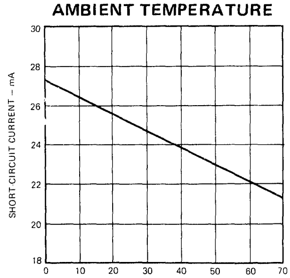
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



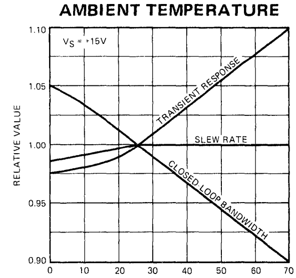
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

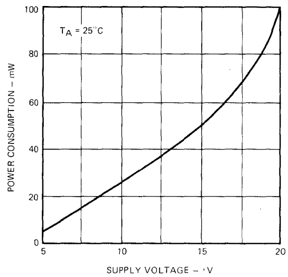


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

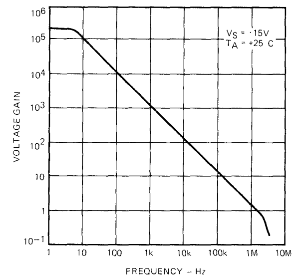


TYPICAL PERFORMANCE CURVES FOR μA747A, μA747C, μA747 AND μA747E

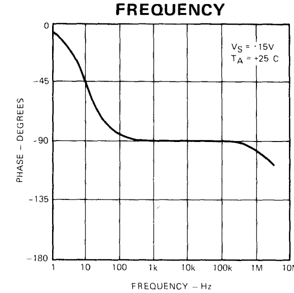
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



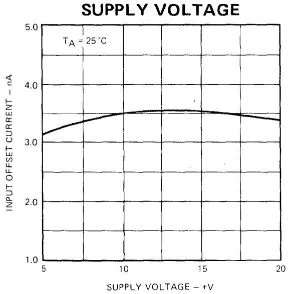
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



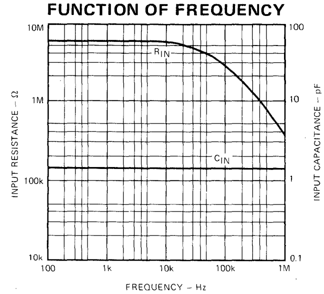
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



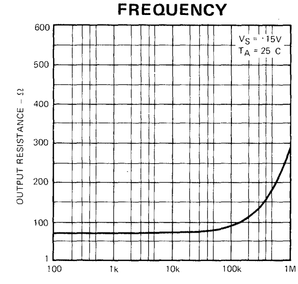
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



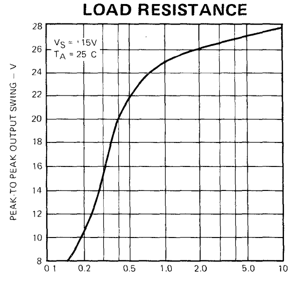
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



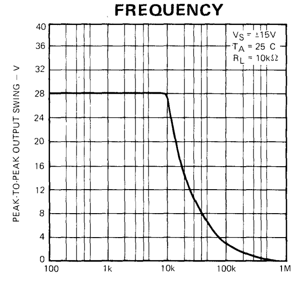
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



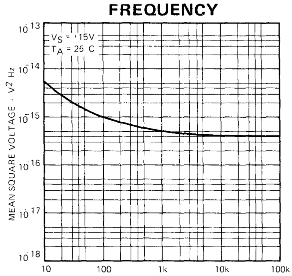
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



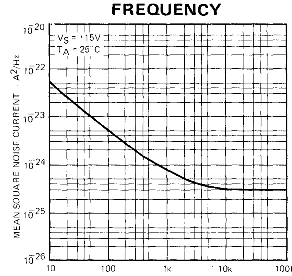
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



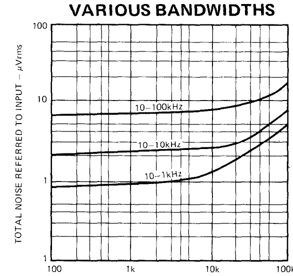
INPUT NOISE VOLTAGE DENSITY AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT DENSITY AS A FUNCTION OF FREQUENCY

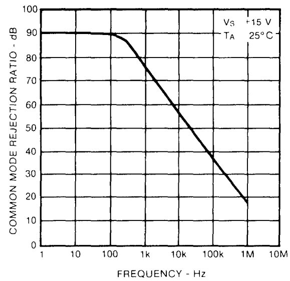


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

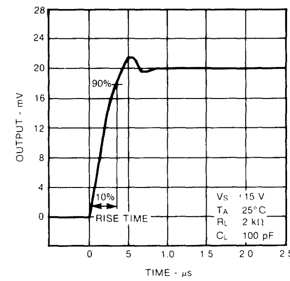


TYPICAL PERFORMANCE CURVES (Each Amplifier) FOR μA747 AND μA747C

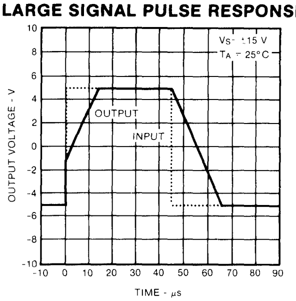
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



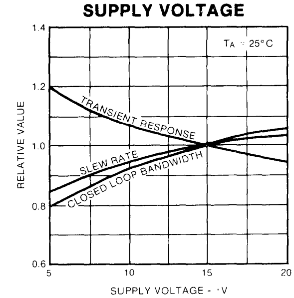
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



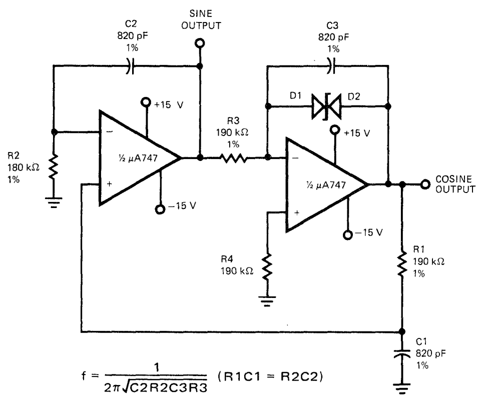
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



5

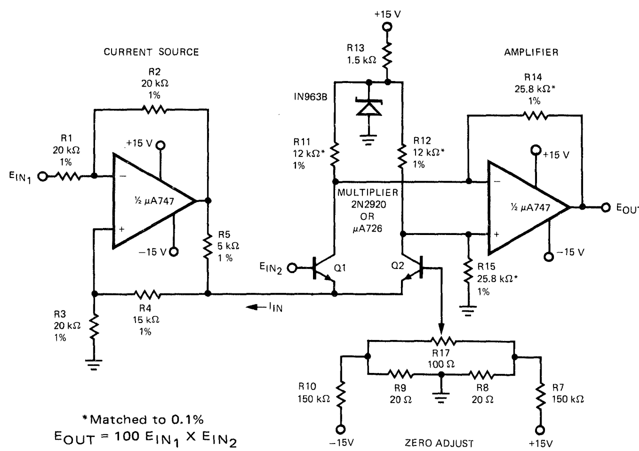
TYPICAL APPLICATIONS

QUADRATURE OSCILLATOR



$$f = \frac{1}{2\pi\sqrt{C2R2C3R3}} \quad (R1C1 = R2C2)$$

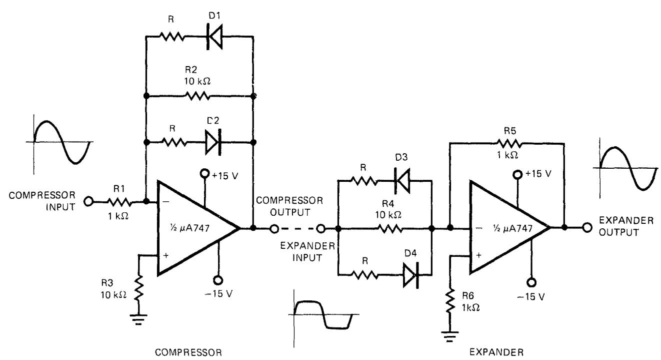
ANALOG MULTIPLIER



*Matched to 0.1%

$E_{OUT} = 100\ E_{IN_1} \times E_{IN_2}$

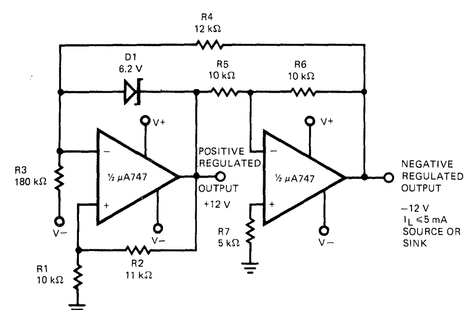
COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R1/R (10 kΩ > R ⩾ 0)

NOTE: DIODES D1 THROUGH D4 ARE MATCHED FD666 OR EQUIVALENT

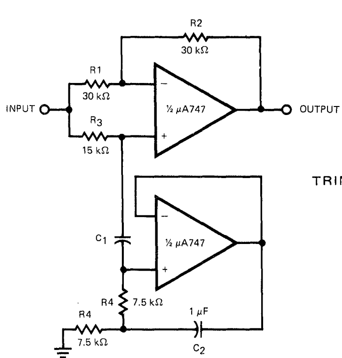
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



POSITIVE OUTPUT = $V_{D1} \times \frac{R1 + R2}{R2}$

NEGATIVE OUTPUT = −POSITIVE OUTPUT × $\frac{R6}{R5}$

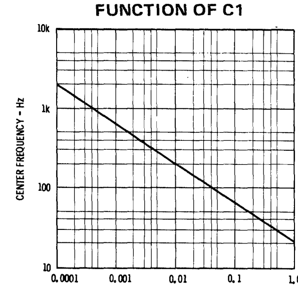
NOTCH FILTER USING THE μA747 AS A GYRATOR



TRIM R3 SUCH THAT

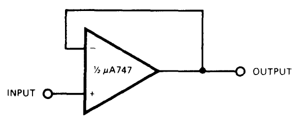
$$\frac{R1}{R2} = \frac{R3}{2\ R4}$$

NOTCH FREQUENCY AS A FUNCTION OF C1



TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



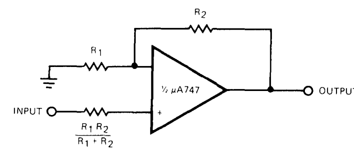
$R_{IN} = 400\ M\Omega$

$C_{IN} = 1\ pF$

$R_{OUT} << 1\ \Omega$

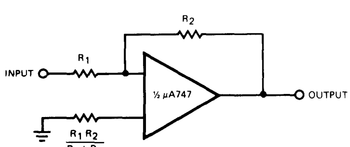
B W = 1 MHz

NON-INVERTING AMPLIFIER



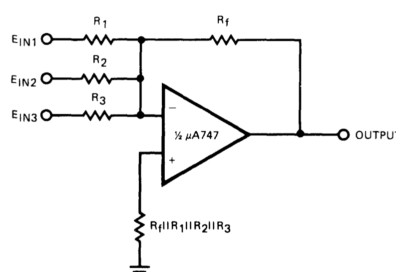
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

WEIGHTED AVERAGING AMPLIFIER



$$-E_{OUT} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_f}{R_2}\right) + E_{IN3}\left(\frac{R_f}{R_3}\right)$$

μA748
OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

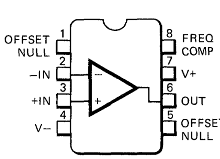
GENERAL DESCRIPTION — The μA748 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch-up make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For superior performance, see μA777 data sheet.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA748)	−55°C to +125°C
Commercial (μA748C)	0°C to +70°C
Pin Temperature (Soldering 60 s)	
Metal Can, Flatpak, and Hermetic DIPs	300°C
Molded Mini DIP	260°C
Output Short-Circuit Duration (Note 3)	Indefinite

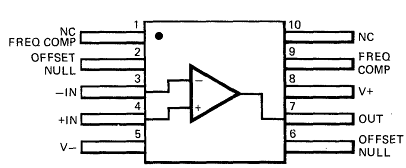
CONNECTION DIAGRAMS
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA748C	μA748TC

10-PIN FLATPAK*
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

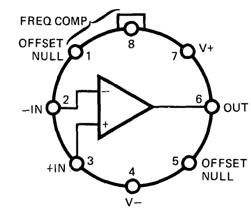


***Available on special request.**

ORDER INFORMATION

TYPE	PART NO.
μA748	μA748FM
μA748A	μA748AFM

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

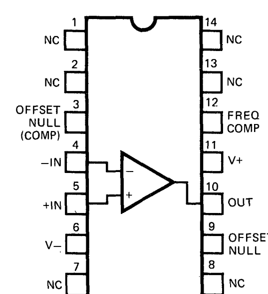


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA748	μA748HM
μA748A	μA748AHM
μA748C	μA748HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA748	μA748DM
μA748A	μA748ADM
μA748C	μA748DC

Notes and equivalent circuit on following pages.

*Planar is a patented Fairchild process.

μA748A

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C, C_C = 30pF unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50$ kΩ		0.5	2.0	mV
Input Offset Current				2.0	10	nA
Input Bias Current				20	75	nA
Input Resistance			2.0	10.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 50$ kΩ		0.5	3.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50$ kΩ		2.5	15	μV/°C
Input Offset Current					25	nA
Average Input Offset Current Drift		$25°C \leq T_A \leq +125°C$		2.5	30	pA/°C
		$-55°C \leq T_A \leq 25°C$		6.5	150	pA/°C
Input Bias Current					100	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50$ kΩ	80	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50$ kΩ		13	100	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Supply Current		T_A = +125°C		1.5	2.5	mA
		T_A = -55°C		2.0	3.3	mA
Power Consumption		T_A = +125°C		40	75	mW
		T_A = -55°C		60	100	mW

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for the DIP 5.6 mW/°C for the mini DIP and 7.1 mW/°C for the flatpak.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

μA748

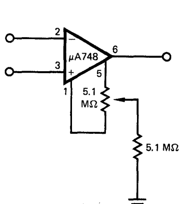
ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$pF unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	150,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs

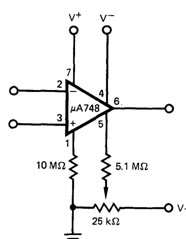
The following specifications apply for $-55°C \leq T_A \leq +125°C$:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		50	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

VOLTAGE OFFSET NULL CIRCUIT

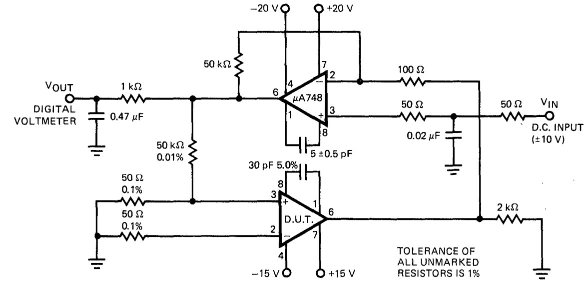


SUGGESTED



ALTERNATE

GAIN TEST CIRCUIT



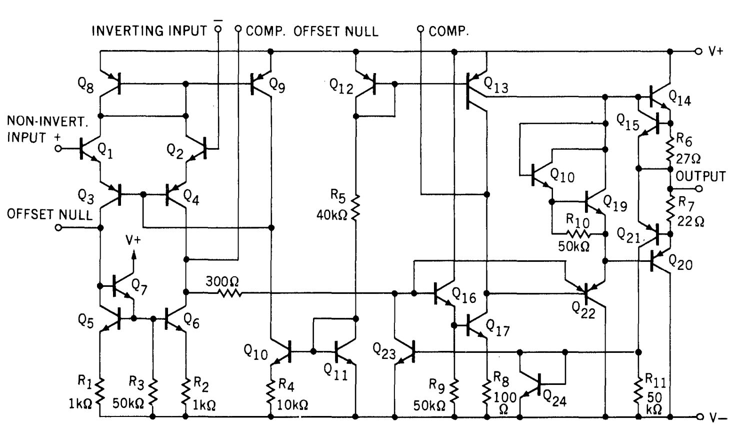
$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}} = \frac{10 \times 10^3}{V_{OUT}} \text{ FOR } V_{IN} \text{ SPECIFIED}$$

μA748C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C, C_C = 30pF unless otherwise specified.

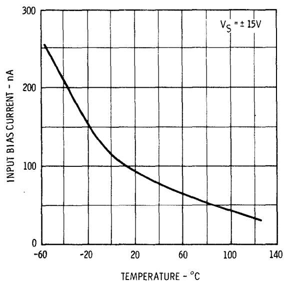
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	20,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1) — Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
Transient Response (Voltage Follower, Gain of 1) — Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10) — Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
Transient Response (Voltage Follower, Gain of 10) — Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption			60	100	mW

EQUIVALENT CIRCUIT

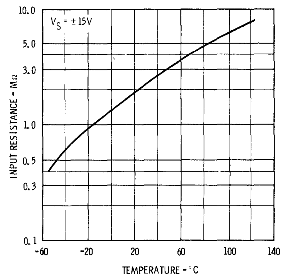


TYPICAL PERFORMANCE CURVES FOR µA748

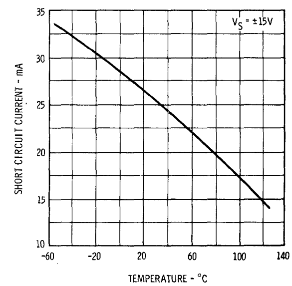
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



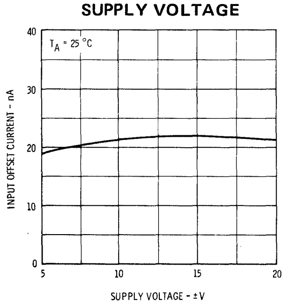
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



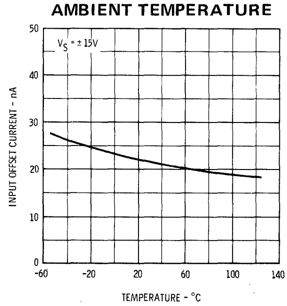
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



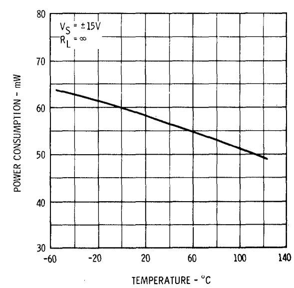
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

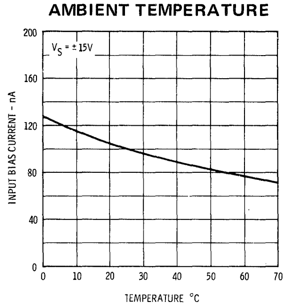


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

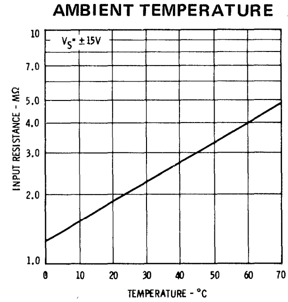


TYPICAL PERFORMANCE CURVES FOR µA748C

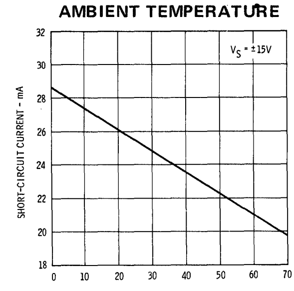
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



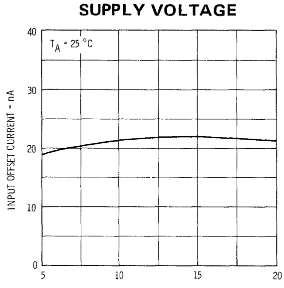
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



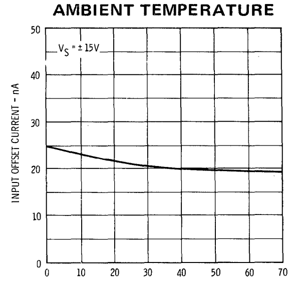
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



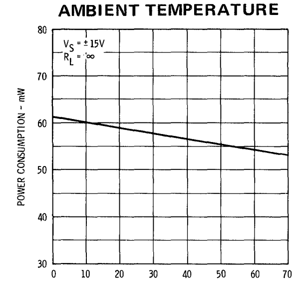
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

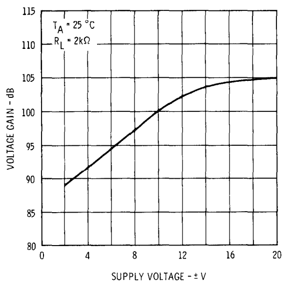


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

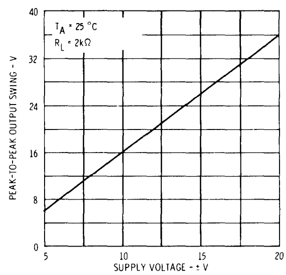


TYPICAL PERFORMANCE CURVES FOR µA748 AND µA748C

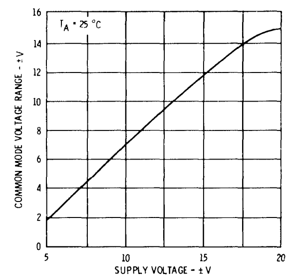
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



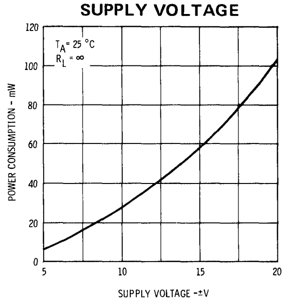
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



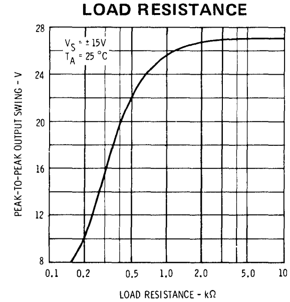
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



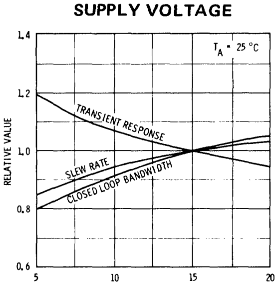
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



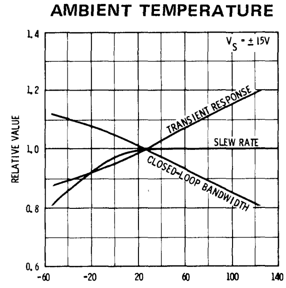
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



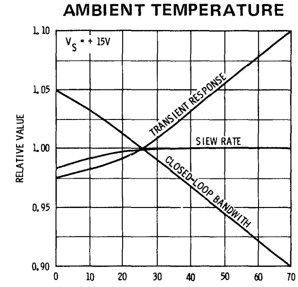
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



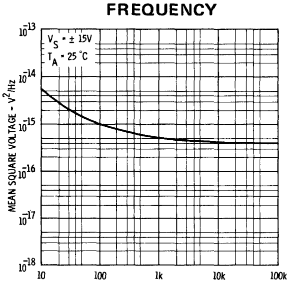
µA748 FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



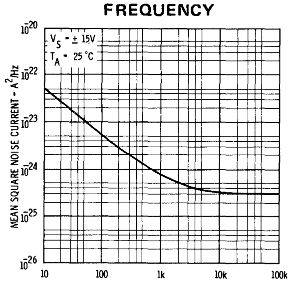
748C FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



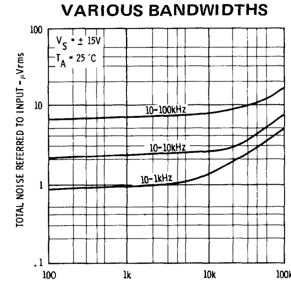
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

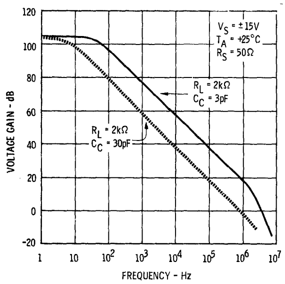


BROAD BAND NOISE FOR VARIOUS BANDWIDTHS

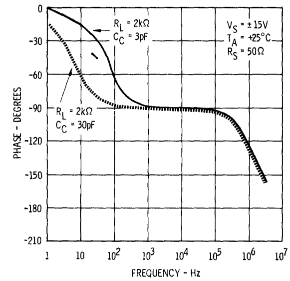


TYPICAL PERFORMANCE CURVES FOR μA748 AND μA748C

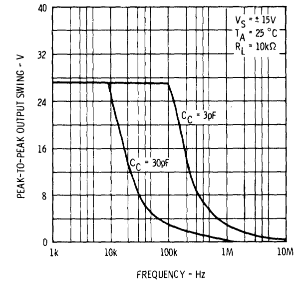
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



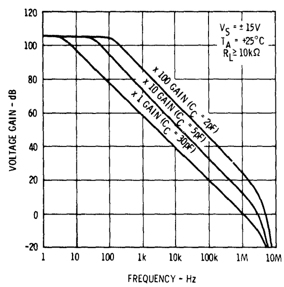
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



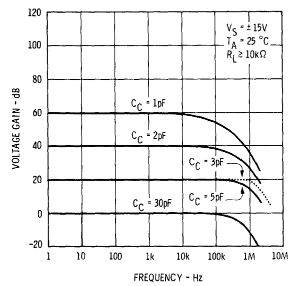
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



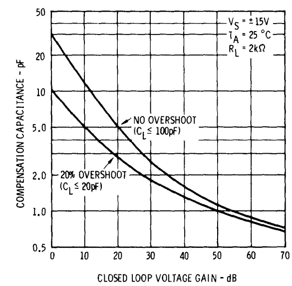
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



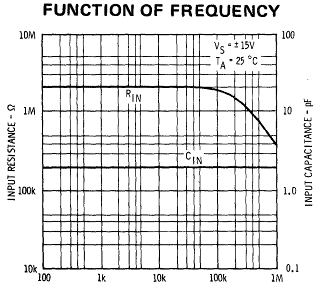
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



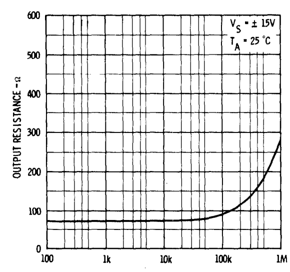
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



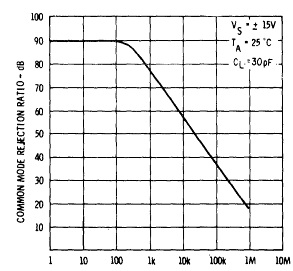
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



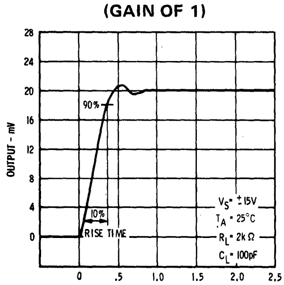
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



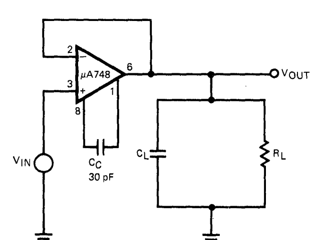
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



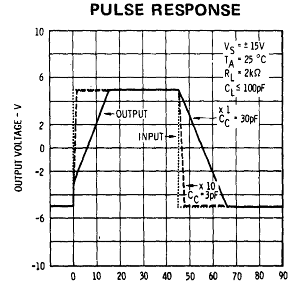
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

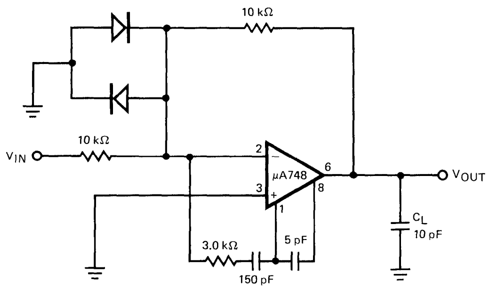


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

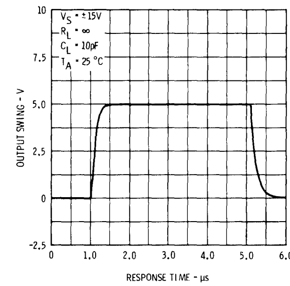


TYPICAL PERFORMANCE CURVES FOR μA748 AND μA748C

FEED FORWARD COMPENSATION

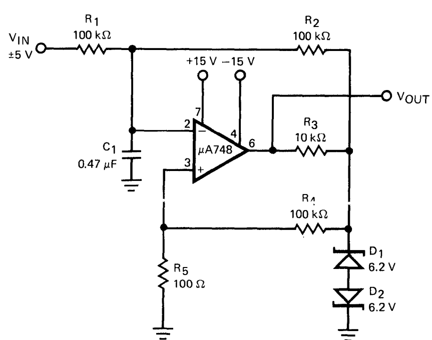


LARGE SIGNAL FEED FORWARD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

PULSE WIDTH MODULATOR



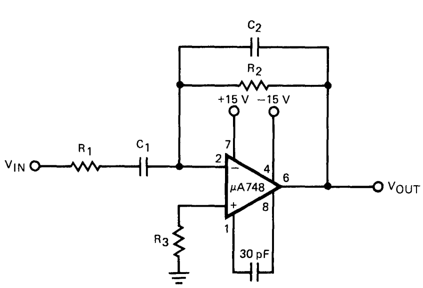
$$f_c = \frac{1}{2\pi\ R2\ C1}$$

$$f_n = \frac{1}{2\pi\ R1\ C1}$$

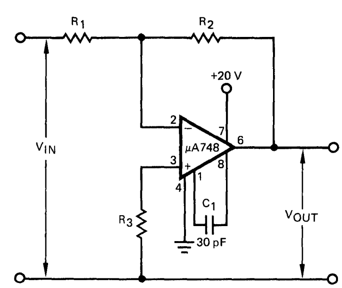
$$= \frac{1}{2\pi\ R2\ C2}$$

$$f_c < f_n < f_{unity\ gain}$$

PRACTICAL DIFFERENTIATOR



CIRCUIT FOR OPERATING THE μA748 WITHOUT A NEGATIVE SUPPLY



NOTES
1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the mini DIP and 7.1 mW/°C for the flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C case temperature or +75°C ambient temperature.

μA749

DUAL AUDIO OPERATIONAL AMPLIFIER/PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

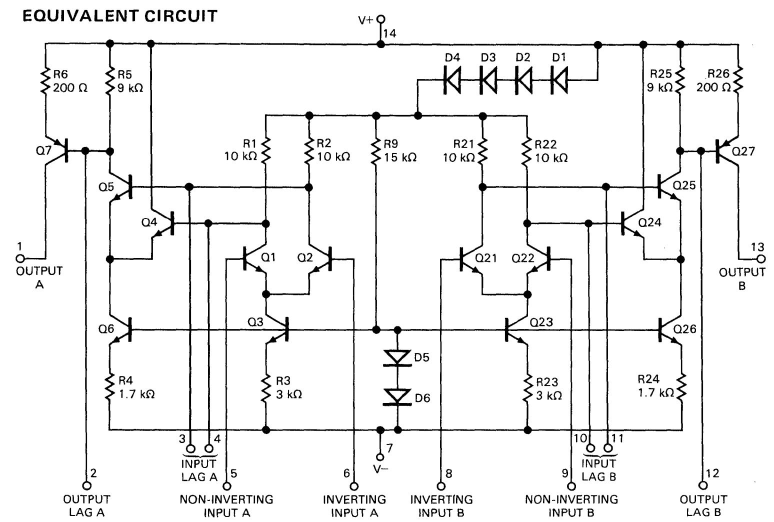
GENERAL DESCRIPTION — The μA749 consists of Two Identical High Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These 3-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, −13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

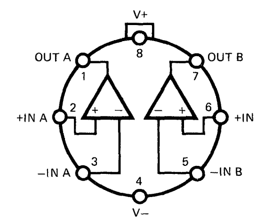
Supply Voltage (μA749 and μA749C)	±18 V
(μA749D)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2) (μA749 and μA749C)	±15 V
(μA749D)	±12 V
Storage Temperature Range	
Metal Can, Hermetic DIP	−65°C to +150°C
Molded DIP (μA749PC)	−55°C to +125°C
Operating Temperature Range	
Military (μA749)	−55°C to +125°C
Commercial (μA749C and μA749D)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

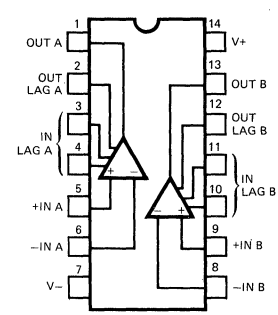


Note: Pin 4 is connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA749D	μA749DHC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA749	μA749DM
μA749C	μA749DC
μA749C	μA749PC

*Planar is a patented Fairchild process.

μA749

ELECTRICAL CHARACTERISTICS: V+ = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	400	nA
Input Bias Current			0.30	0.75	μA
Input Resistance		100	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±10 V	20,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	220	mW
Supply Current	V_{OUT} = 0		9.0	10.4	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF		2.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ f = 10 kHz		140		dB

The following specifications apply for V+ = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	300	nA
Input Bias Current			0.15	0.75	μA
Supply Current	V_{OUT} = 0		2.5	4.8	mA
Internal Power Dissipation	V_{OUT} = 0		20	36	mW
Large Signal Voltage Gain	V_{OUT} = ±2.0 V	20,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

The following specifications apply for −55°C ≤ T_A ≤ +125°C, V+ = ±15 V, R_L = 5 kΩ to Pin 7:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +125°C	6,500	20,000		V/V
	V_{OUT} = ±10 V, T_A = −55°C	20,000	30,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current	T_A = +125°C		0.05	1.0	μA
	T_A = −55°C		0.05	1.5	μA
Input Bias Current	T_A = +125°C		0.15	0.75	μA
	T_A = −55°C		0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +125°C		3.0		μV/°C
	R_S = 200 Ω, −55°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +125°C		0.5		nA/°C
	−55°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	−55°C ≤ T_A ≤ +125°C		5.0		nA/°C
Supply Current	V_{OUT} = 0, T_A = +125°C			9.7	mA
	V_{OUT} = 0, T_A = −55°C			13	mA
Internal Power Dissipation	V_{OUT} = 0, T_A = +125°C			200	mW
	V_{OUT} = 0, T_A = −55°C			300	mW

The following specifications apply for −55°C ≤ T_A ≤ +125°C, V+ = ±4.5 V, R_L = 10 kΩ to Pin 7:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.5	6.0	mV
Input Offset Current			50	750	nA
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = +125°C	5,000			V/V
	V_{OUT} = ±2.0 V, T_A = −55°C	20,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

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μA749C

ELECTRICAL CHARACTERISTICS: V+ = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	750	nA
Input Bias Current			0.30	1.5	μA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±10 V	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	350	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	330	mW
Supply Current	V_{OUT} = 0		9.0	14	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF		1.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ, f = 10 kHz		140		dB

The following specifications apply for V+ = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	600	nA
Input Bias Current			0.3	1.5	μA
Supply Current	V_{OUT} = 0		2.5		mA
Internal Power Dissipation	V_{OUT} = 0		20		mW
Large Signal Voltage Gain	V_{OUT} = ±2.0 V	15,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

The following specifications apply for 0°C ≤ T_A ≤ +70°C, V+ = ±15 V, R_L = 5 kΩ to Pin 7:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +70°C	8,000	40,000		V/V
	V_{OUT} = ±10 V, T_A = 0°C	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	9.0	mV
Input Offset Current			0.05	1.5	μA
Input Bias Current			0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +70°C		3.0		μV/°C
	R_S = 200 Ω, 0°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +70°C		0.5		nA/°C
	0°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	0°C ≤ T_A ≤ +70°C		4.0		nA/°C

The following specifications apply for 0°C ≤ T_A ≤ +70°C, V+ = ±4 V, R_L = 10 kΩ to Pin 7:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.5	9.0	mV
Input Offset Current			0.05	1.0	μA
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 70°C	8,000			V/V
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 0°C	15,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

μA749D

ELECTRICAL CHARACTERISTICS: V+ = ±6 V, R_L = 10 kΩ to Pin 4, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±4.0 V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5.0		V
Negative Output Voltage Swing		−5.5	−6.0		V
Output Resistance	f = 1.0 kHz		10		kΩ
Input Voltage Range		−4.0		+2.5	V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50	100	μV/V
Power Consumption (including load)	V_{OUT} = 0	24	36	54	mW
Supply Current (including load)	V_{OUT} = 0	2.0	3.0	4.5	mA
Turn On Delay (See Figure 5)	Open Loop, V_{IN} = ±20 mV, R_L = 5 kΩ		0.2		μs
Turn Off Delay (See Figure 5)	Open Loop, V_{IN} = ±20 mV, R_L = 5 kΩ		0.3		μs
Channel Separation (See Figure 7)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB

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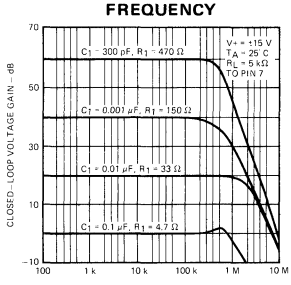
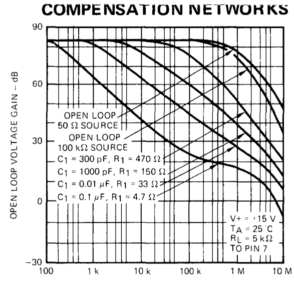
TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

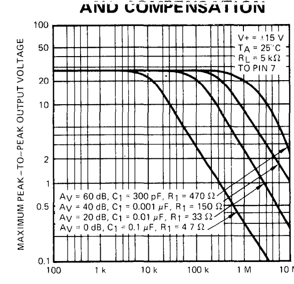
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



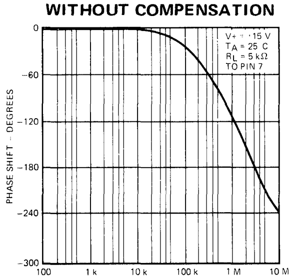
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



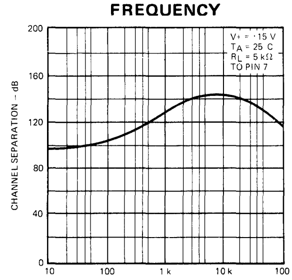
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



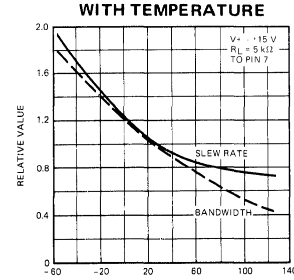
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

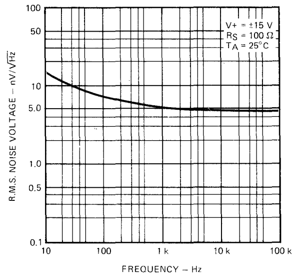


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE

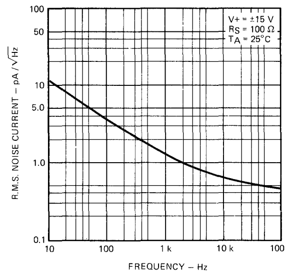


TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

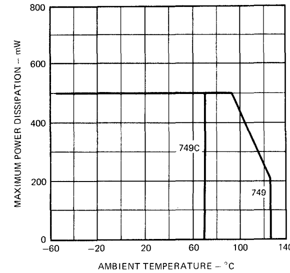
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



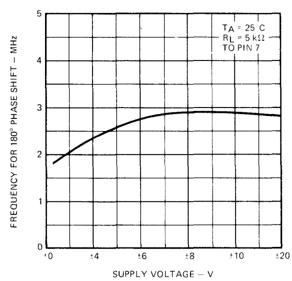
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



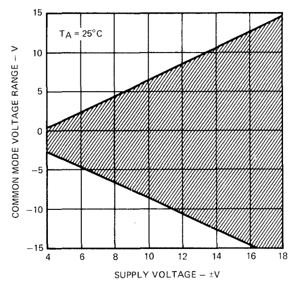
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



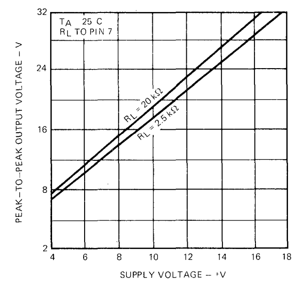
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



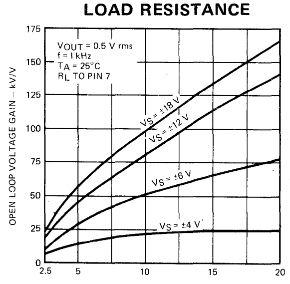
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



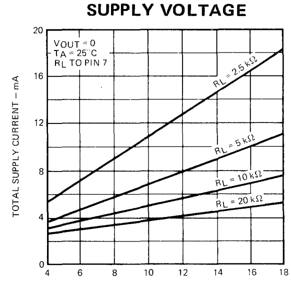
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



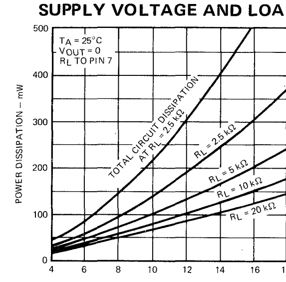
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



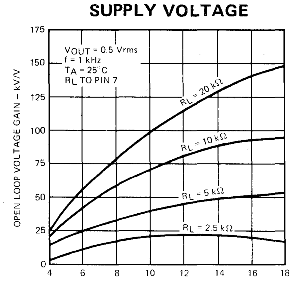
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



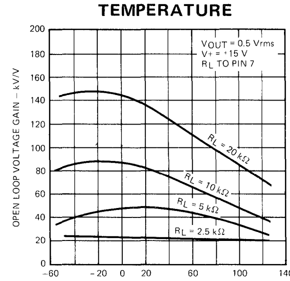
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



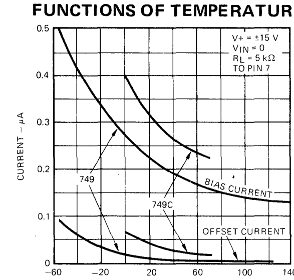
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

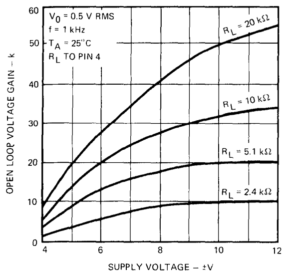


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

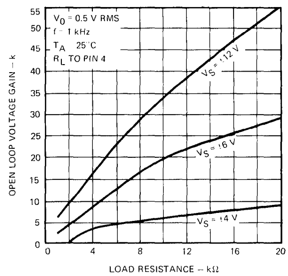


TYPICAL PERFORMANCE CURVES FOR μA749D

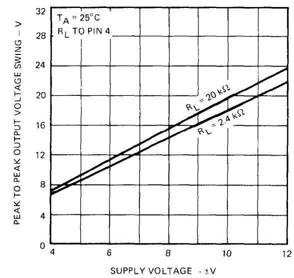
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



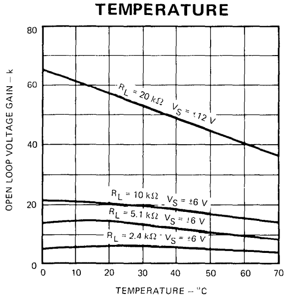
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



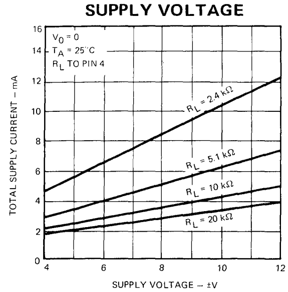
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



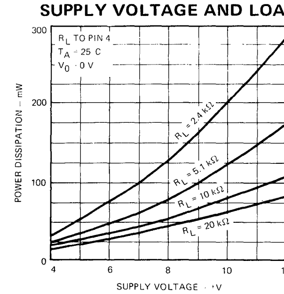
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



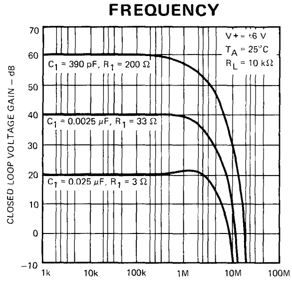
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



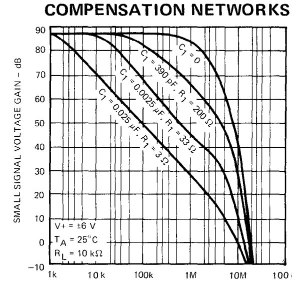
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



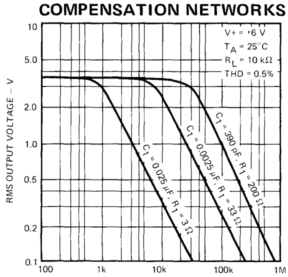
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



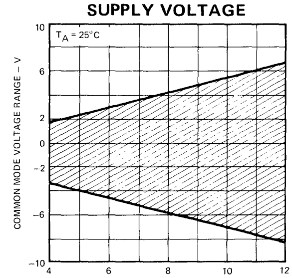
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OFFSET NULL*
NETWORK
μA749 AND μA749C

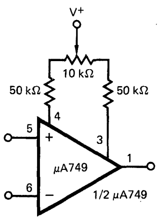


Fig. 1

FREQUENCY RESPONSE*
TEST CIRCUIT
μA749 AND μA749C

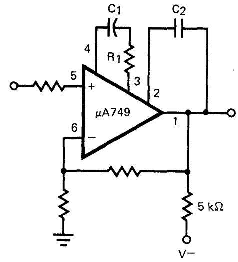


Fig. 2

PULSE RESPONSE
WAVEFORMS
μA749 AND μA749C

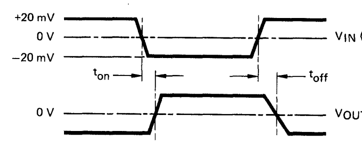


Fig. 3

CHANNEL SEPARATION*
TEST CIRCUIT
μA749 AND μA749C

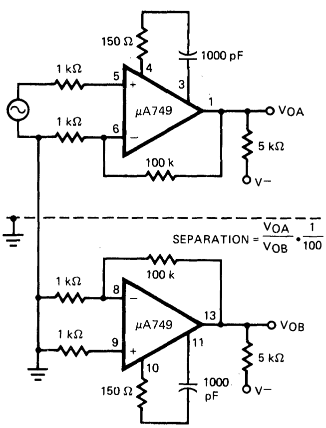


Fig. 4

PULSE RESPONSE
WAVEFORMS
μA749D

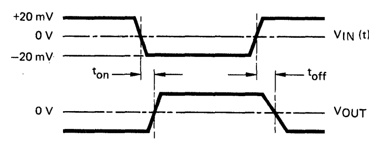


Fig. 5

FREQUENCY RESPONSE
TEST CIRCUIT
μA749D

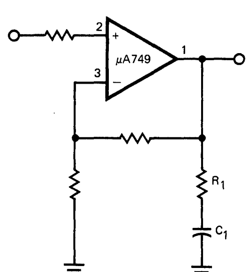


Fig. 6

CHANNEL SEPARATION
TEST CIRCUIT
μA749D

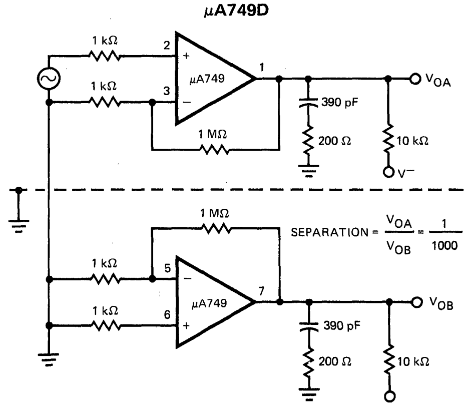
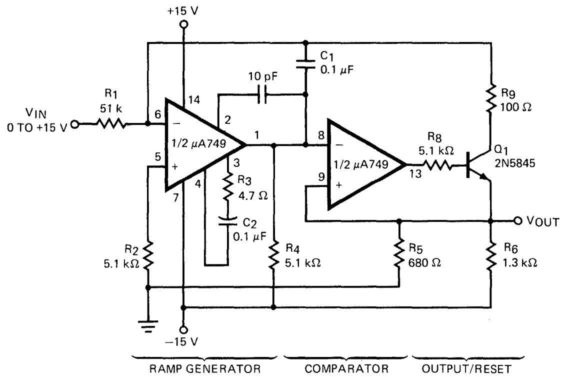


Fig. 7

*Pin numbers refer to Dual-in-line Package

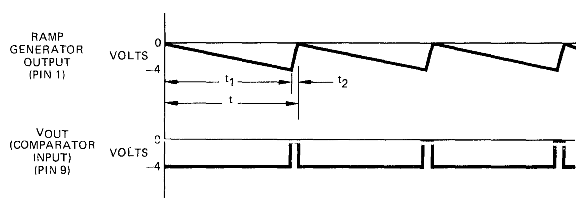
TYPICAL APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER



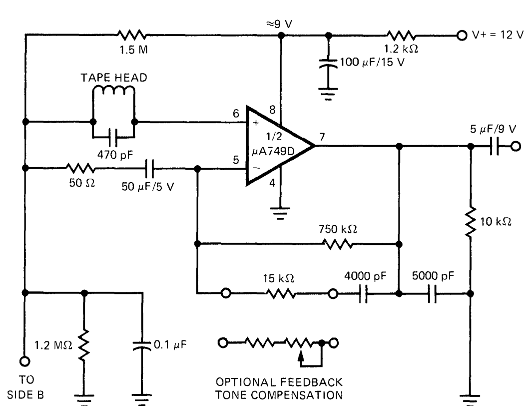
$R^* = R$ pin 1 + R9 + R_{CE} Q1 + R6 output stage.

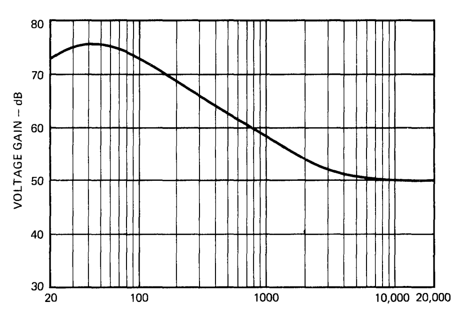
WAVEFORMS



$$t = t1 + t2 = 4\,\frac{R1\,C1}{V_{IN}} + \frac{4R^*\,C1}{15}$$

STEREO TAPE PREAMPLIFIER





TYPICAL PERFORMANCE

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

μA759

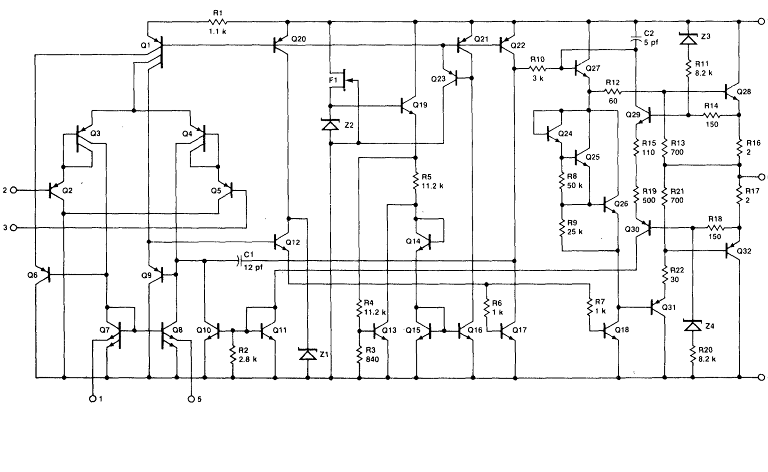
POWER OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA759 is a high performance monolithic operational amplifier constructed using the Fairchild Planar* Epitaxial process. The amplifier provides 325 mA output current and features small signal characteristics better than the μA741. The amplifier is designed to operate from a single or dual power supply and the input common mode range includes the negative supply. The high gain and high output power provide superior performance whenever an operational amplifier is needed. The μA759 employs internal current limiting, thermal shutdown and safe area compensation making it essentially indestructable. It is intended for a wide range of applications including voltage regulators, audio amplifiers, servo amplifiers and power drivers.

- **OUTPUT CURRENT — 325 mA MINIMUM**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL OUTPUT TRANSISTORS SAFE AREA PROTECTION**
- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **AVAILABLE IN THREE PACKAGE STYLES**

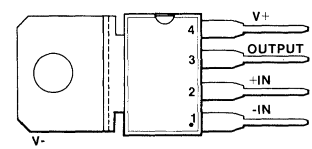
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

POWER WATT PACKAGE

(TOP VIEW)
PACKAGE OUTLINE 8Z
PACKAGE CODE U1

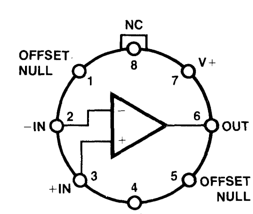


ORDER INFORMATION

TYPE	PART NO.
μA759C	μA759U1C

8-PIN METAL CAN

(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA759	μA759HM
μA759C	μA759HC

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V−	36 V
Differential Input Voltage (Note 1)	30 V
Input Voltage (Note 1)	(V− −0.3 V) to V+
Internal Power Dissipation (Note 2)	Internally Limited
Operating Junction Temperature Range	
Military (μA759)	−55°C to +150°C
Commercial (μA759C)	0°C to +125°C
Storage Temperature Range	
4-Pin Power Watt (U1)	−55°C to +150°C
8-Pin TO-99 (H)	−65°C to +150°C
Pin Temperature	
4-Pin Power Watt (U1) (Soldering, 10 s)	260°C
8-Pin TO-99 (H) (Soldering, 60 s)	300°C

NOTES:

1. For a supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

2. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the thermal resistance values on following page.

μA759

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	3.0	mV
Input Offset Current				5.0	30	nA
Input Bias Current				50	150	nA
Input Resistance			0.25	1.5		MΩ
Input Voltage Range			+13 to −V_S	+13.5 to −V_S		V
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	50 k	200 k		V/V
Supply Current				12	18	mA
Peak Output Current		$3\text{ V} \leq \lvert V_S - V_{OUT} \rvert < 10\text{ V}$	±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT} \rvert = 30$ V		±200		mA
Transient Response	Risetime	$R_L \geq 50$ Ω		300		ns
(Unity Gain)	Overshoot	$R_L \geq 50$ Ω		5.0		%
Slew Rate		$R_L \geq 50$ Ω		0.6		V/μs
Unity Gain Bandwidth				1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq 150°C$						
Input Offset Voltage		$R_S \leq 10$ kΩ			4.5	mV
Input Offset Current					60	nA
Input Bias Current					300	nA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Output Voltage Swing		$R_L \geq 50$ Ω	±10	±12.5		V

5

μA759C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current				5.0	50	nA
Input Bias Current				50	250	nA
Input Resistance			0.25	1.5		MΩ
Input Voltage Range			+13 to $-V_S$	+13.5 to $-V_S$		V
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Supply Current				12	18	mA
Peak Output Current		3 V $\leq \lvert V_S - V_{OUT} \rvert \leq$ 10 V	±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT} \rvert = 30$ V		±200		mA
Transient Response	Risetime	$R_L \geq 50$ Ω		300		ns
(Unity Gain)	Overshoot	$R_L \geq 50$ Ω		10		%
Slew Rate				0.5		V/μs
Unity Gain Bandwidth				1.0		MHz
The following specifications apply for 0°C ≤ T_J ≤ 125°C						
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current					100	nA
Input Bias Current					400	nA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	100		dB
Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Output Voltage Swing		$R_L \geq 50$ Ω	±10	±12.5		V

PACKAGE	**TYP**	**MAX**	**TYP**	**MAX**
	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
Power Watt (U1)	8.0°C/W	12°C/W	75°C/W	80°C/W
Metal Can (H)	30°C/W	40°C/W	120°C/W	185°C/W

$$P_{D\,(MAX)} = \frac{T_J\,(MAX) - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_J\,(MAX) - T_A}{\theta_{JA}} \quad \text{(Without a heat sink)}$$

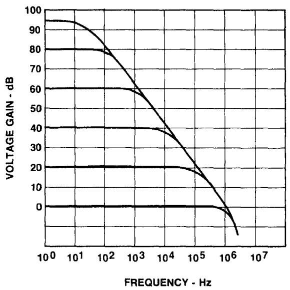
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D\,(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

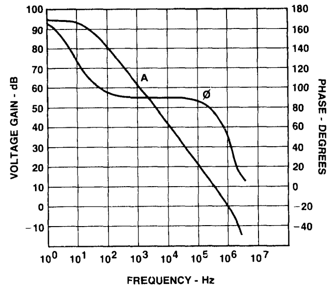
Where:
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction to ambient thermal resistance
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case to ambient thermal resistance
- θ_{CS} = Case to heat sink thermal resistance
- θ_{SA} = Heat sink to ambient thermal resistance

TYPICAL PERFORMANCE CURVES

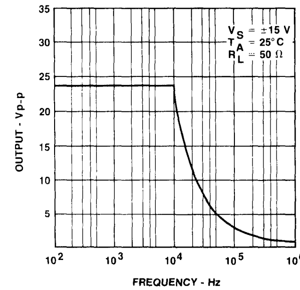
FREQUENCY RESPONSE AT VARIOUS CLOSED LOOP GAIN SETTINGS



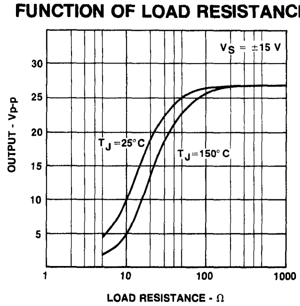
OPEN LOOP GAIN AND PHASE RESPONSE AS A FUNCTION OF FREQUENCY



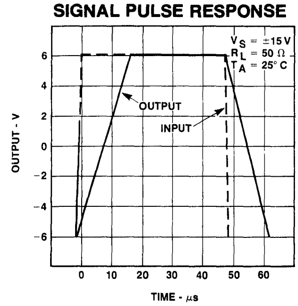
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



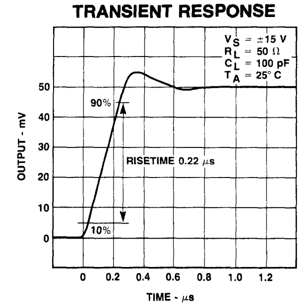
P-P OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



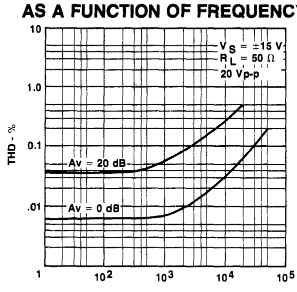
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



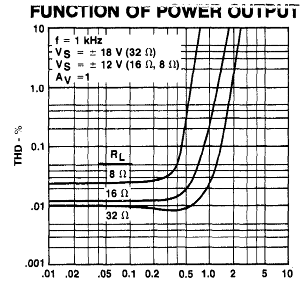
VOLTAGE FOLLOWER TRANSIENT RESPONSE



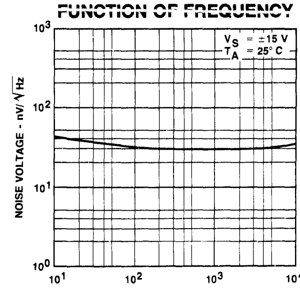
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



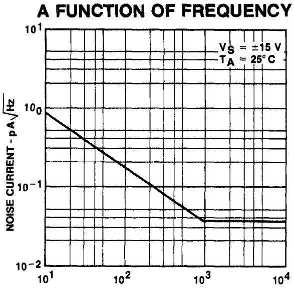
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



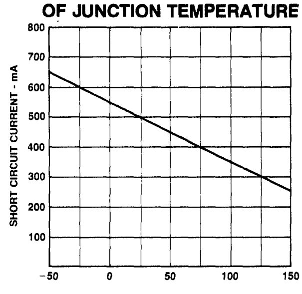
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



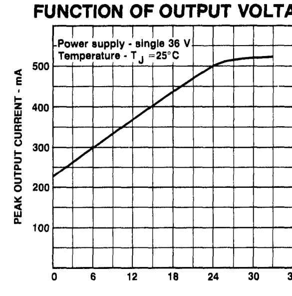
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



PEAK OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



5

MOUNTING HINTS

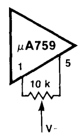
Metal Can Package (μA759HC/μA759HM)

The μA759 in the 8-Pin TO-99 metal can package must be used with a heat sink. With ±15 V power supplies, the μA759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the μA759 is internally connected to the negative power supply terminal.

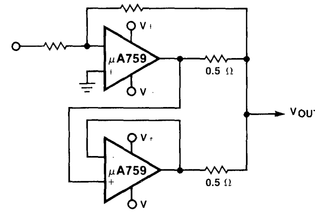
Power Watt Package (μA759U1C)

The μA759U1C is designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

OFFSET NULL CIRCUIT

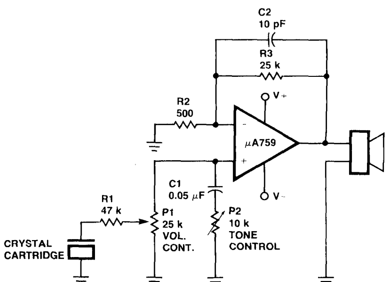


PARALLELING μA759 POWER OP AMPS

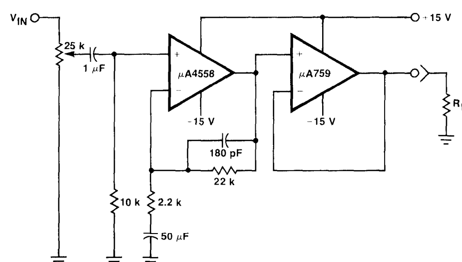


AUDIO APPLICATIONS

LOW COST PHONO AMPLIFIER

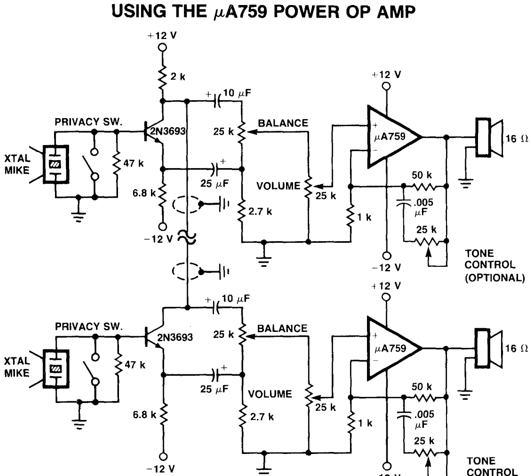


HEADPHONE AMPLIFIER



Speaker Impedance (ohms)	Output Power (watts)	Min Supply (volts)	V_{out} p-p (volts)
4	.18	9	2.4
8	.36	12	4.8
16	.72	15	9.6
32	1.44	25	19.2

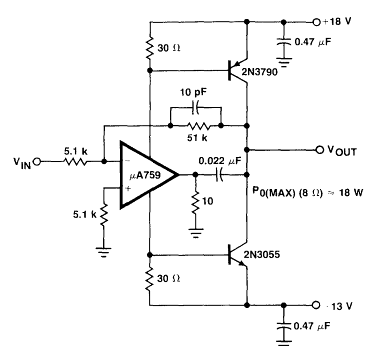
BIDIRECTIONAL INTERCOM SYSTEM USING THE μA759 POWER OP AMP



FEATURES

- Circuit Simplicity
- 1 Watt of Audio Output
- Duplex operation with only one two-wire cable as interconnect

HIGH SLEW RATE POWER OP AMP/AUDIO AMP



FEATURES

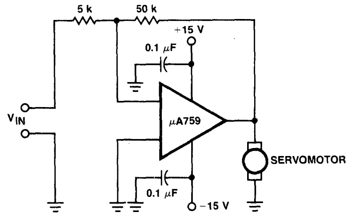
- High Slew Rate 9 V/μs
- High 3 dB Power Bandwidth 85 kHz
- 18 Watts Output Power Into An 8 Ω Load
- Low Distortion — .2%, 10 VRMS, 1 kHz Into 8 Ω

DESIGN CONSIDERATION

- $A_V \geq 10$

SERVO APPLICATIONS

DC SERVO AMPLIFIERS



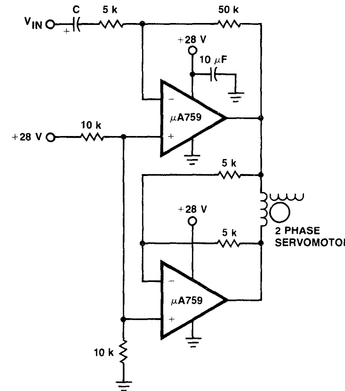
FEATURES

- Circuit Simplicity
- One Chip Means Excellent Reliability

DESIGN CONSIDERATIONS

- $I_{OUT} \leqslant 325$ mA

AC SERVO AMPLIFIER - BRIDGE TYPE



FEATURES

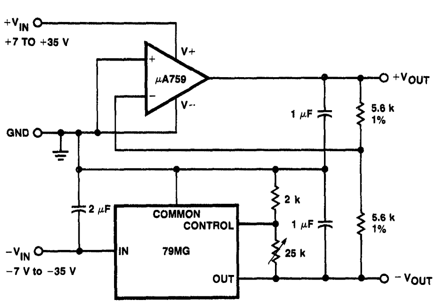
- Gain of 10
- Use of μA759 Means Simple Inexpensive Circuit

DESIGN CONSIDERATIONS

- 325 mA Max Output Current

REGULATOR APPLICATIONS

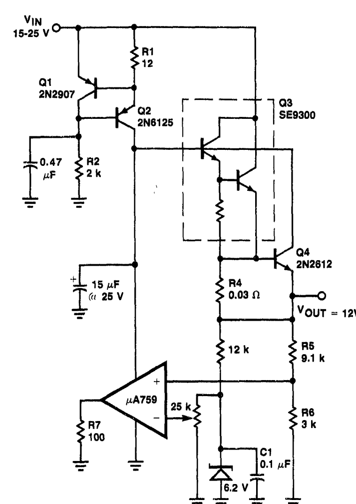
ADJUSTABLE DUAL TRACKING REGULATOR



FEATURES

- Wide Output Voltage Range (± 2.2 to ± 30 V)
- Excellent Load Regulation $\Delta V_{OUT} < \pm 5$ mV for $\Delta I_{OUT} = \pm 0.2$ A
- Excellent Line Regulation $\Delta_{OUT} < \pm 2$ mV for $\Delta\ V_{IN} = 10$ V

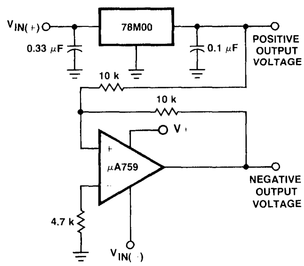
10 AMP - 12 VOLT REGULATOR



FEATURES

- Excellent Load and Line Regulation
- Excellent Temperature Coefficient-Depends Largely on Tempco of the Reference Zener

DUAL TRACKING REGULATOR



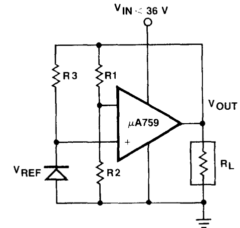
FEATURES

- Positive & Negative Outputs "Track"
- Inexpensive
- 500 mA Positive Output
- 325 mA Negative Output
- Any 78M Voltage Can be Used +5, +6, +8, +12, +15, +20, +24

DESIGN CONSIDERATIONS

- $V_{IN}(-)$ must not exceed −36 V
- $V_{IN}(-)$ must be at least 3 V more negative than $V_{OUT}(-)$

PRECISION ADJUSTABLE VOLTAGE REGULATOR



FEATURES

- Low Temperature Coefficient
  —Depends primarily on tempco of reference zener
- Excellent Load and Line Regulation
  —current through reference zener is independent of load and line
- Up to 325 mA Output Current

DESIGN CONSIDERATIONS

- $V_{IN} \leq 36$ V $\quad I_{REF} = \dfrac{V_{OUT} - V_{REF}}{R3}$
- $V_{IN} \geq V_{OUT} + 3$ V $\quad V_{OUT} = V_{REF}\dfrac{(R1 + R2)}{R2}$

5

μA776

MULTI-PURPOSE PROGRAMMABLE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

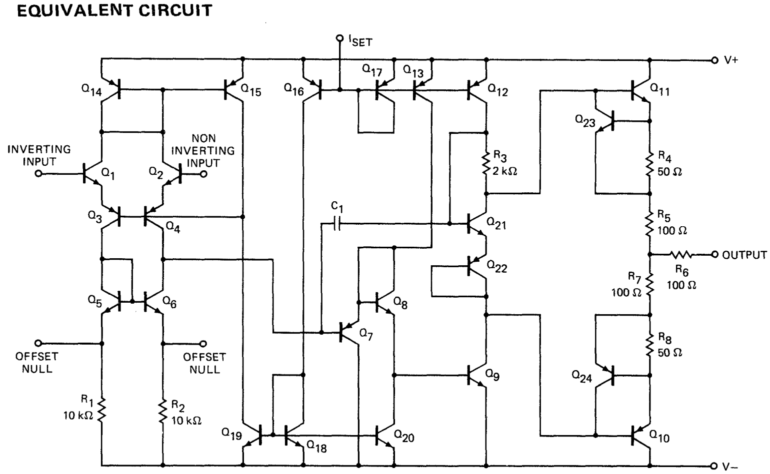
DESCRIPTION – The μA776 Programmable Operational Amplifier is constructed using the Fairchild Planar* epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch-up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

- **MICROPOWER CONSUMPTION**
- **±1.2V to ±18V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**
- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH-UP**

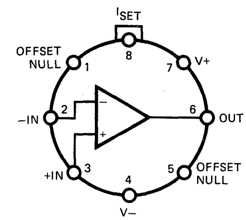
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V–	±0.5 V
I_{SET} (Maximum Current at I_{SET})	500 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V+ -2.0\text{ V}) \leq V_{SET} \leq V+$
Storage Temperature Range	
Metal Can, DIP	–65°C to +150°C
Mini DIP	–55°C to +125°C
Operating Temperature Range	
Military (μA776)	–55°C to +125°C
Commercial (μA776C)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	
Metal Can, DIP	300°C
Mini DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



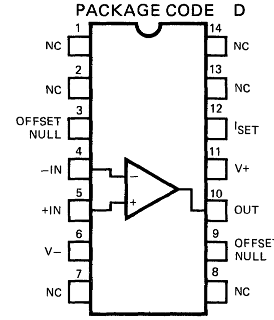
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA776	μA776HM
μA776C	μA776HC

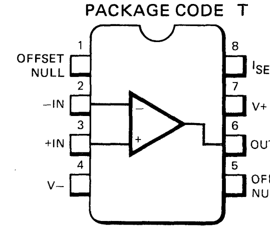
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA776	μA776DM
μA776	μA776DC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA776C	μA776TC

*Planar is a patented Fairchild process.

±15 V OPERATION FOR µA776

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	I_{SET} = 1.5µA MIN	TYP	MAX	I_{SET} = 15µA MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current	$R_S \leq 10k\Omega$		0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT} = ±10V	200k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT} = ±10V				100k	400k		V/V
Output Resistance			5.0k			1.0k		Ω
Output Short-Circuit Current			3.0			12		mA
Supply Current			20	25		160	180	µA
Power Consumption				0.75			5.4	mW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF		1.6			0.35		µs
Transient Response (unity gain) — Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/µs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply −55°C ≤ T_A ≤ +125°C								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	µV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT} = ±10V	100k			75k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				30			200	µA
Power Consumption				0.9			6.0	mW

±3 V OPERATION FOR μA776

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	I_{SET} = 1.5μA MIN	TYP	MAX	I_{SET} = 15μA MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current			0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, $V_{OUT}=\pm1V$	50k	200k					V/V
	$R_L \geq 5k\Omega$, $V_{OUT}=\pm1V$				50k	200k		V/V
Output Resistance			5k			1k		Ω
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	160	μA
Power Consumption			78	120		780	960	μW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$		3.0			0.6		μs
Transient Response (unity gain) — Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, $V_{OUT}=\pm1V$	25k						V/V
	$R_L \geq 5k\Omega$, $V_{OUT}=\pm1V$				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±1.9	±2.1		V
Supply Current				25			180	μA
Power Consumption				150			1080	μW

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for the DIP, and 5.6 mW/°C for the Mini DIP.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30$ μA.

±15 V OPERATION FOR μA776C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	I_{SET} = 1.5μA MIN	TYP	MAX	I_{SET} = 15μA MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±10V				50k	400k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			3.0			12		mA
Supply Current			20	30		160	190	μA
Power Consumption				0.9			5.7	mW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$		1.6			0.35		μs
Transient Response (unity gain) — Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply to 0°C≤T_A≤ +70°C								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k			50k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				35			200	μA
Power Consumption				1.05			6.0	mW

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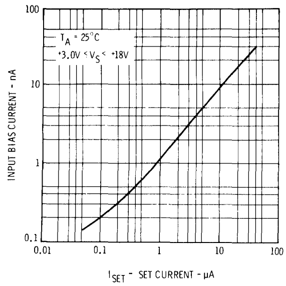
±3 V OPERATION FOR μA776C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise specified.

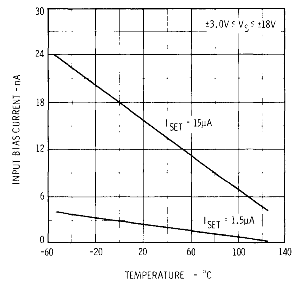
CHARACTERISTICS	CONDITIONS	I_{SET} = 1.5μA MIN	I_{SET} = 1.5μA TYP	I_{SET} = 1.5μA MAX	I_{SET} = 15μA MIN	I_{SET} = 15μA TYP	I_{SET} = 15μA MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, $V_{OUT}=\pm1V$	25k	200k					V/V
	$R_L \geq 5k\Omega$, $V_{OUT}=\pm1V$				25 k	200k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	170	μA
Power Consumption			78	120		780	1020	μW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF		3.0			0.6		μs
Transient Response (unity gain) — Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, $V_{OUT}=\pm1V$	25k						V/V
	$R_L \geq 5k\Omega$, $V_{OUT}=\pm1V$				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±2.0	±2.1		V
Supply Current				25			180	μA
Power Consumption				150			1080	μW

TYPICAL PERFORMANCE CURVES FOR μA776 AND μA776C

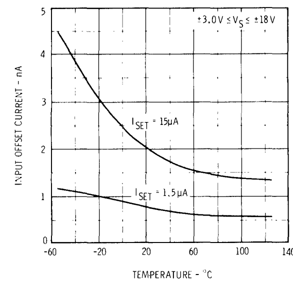
INPUT BIAS CURRENT AS A FUNCTION OF SET CURRENT



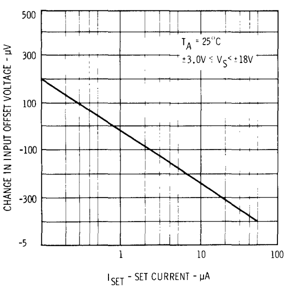
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



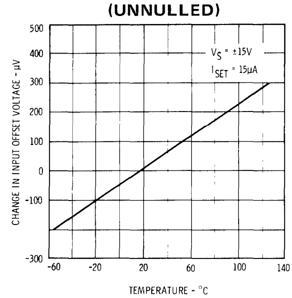
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



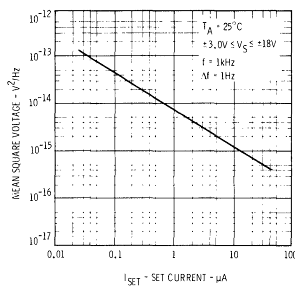
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF SET CURRENT



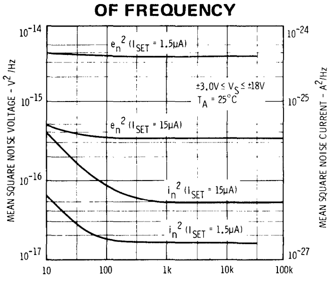
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE (UNNULLED)



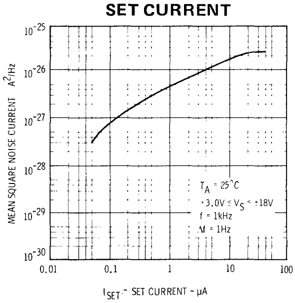
INPUT NOISE VOLTAGE AS A FUNCTION OF SET CURRENT



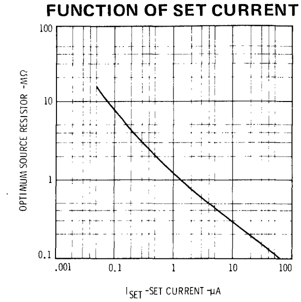
INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY



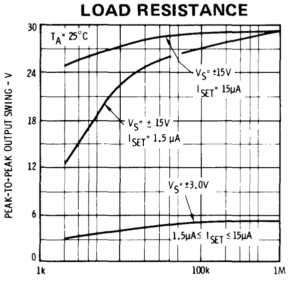
INPUT NOISE CURRENT AS A FUNCTION OF SET CURRENT



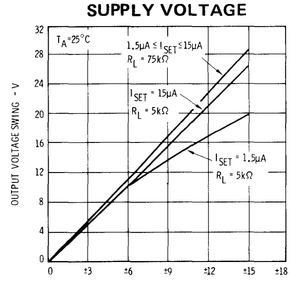
OPTIMUM SOURCE RESISTOR FOR MINIMUM NOISE AS A FUNCTION OF SET CURRENT



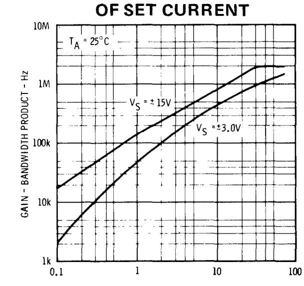
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF SET CURRENT



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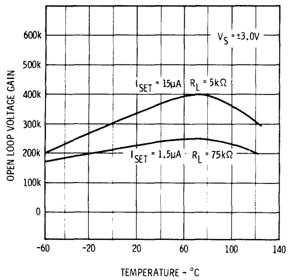
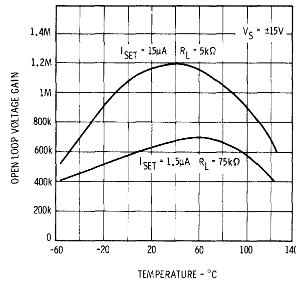
TYPICAL PERFORMANCE CURVES FOR μA776 AND μA776C

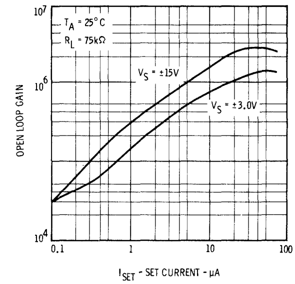
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



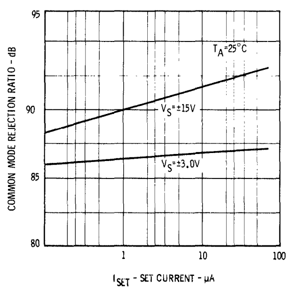
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



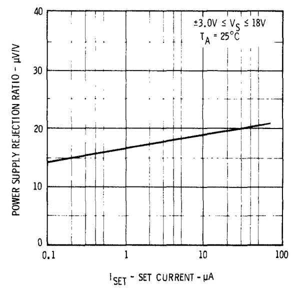
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SET CURRENT



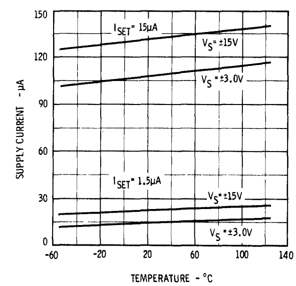
COMMON MODE REJECTION RATIO AS A FUNCTION OF SET CURRENT



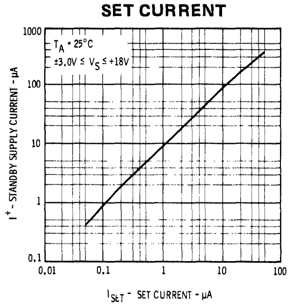
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF SET CURRENT



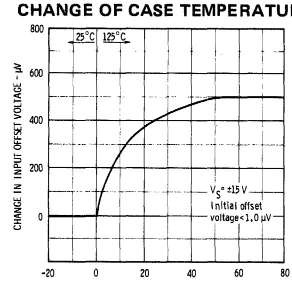
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



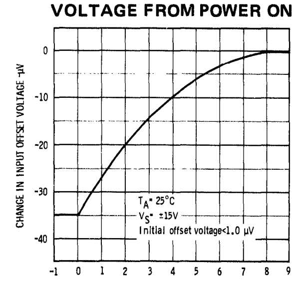
STANDBY SUPPLY CURRENT AS A FUNCTION OF SET CURRENT



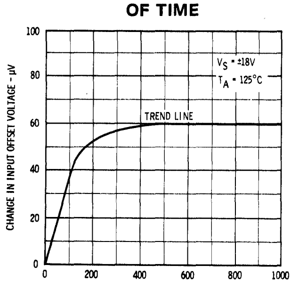
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



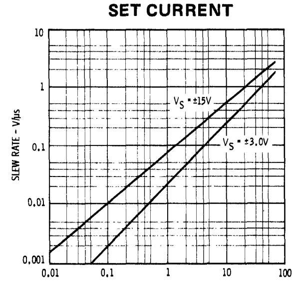
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER ON



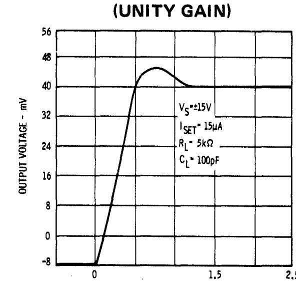
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



SLEW RATE AS A FUNCTION OF SET CURRENT

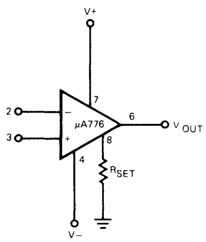


VOLTAGE FOLLOWER TRANSIENT RESPONSE (UNITY GAIN)

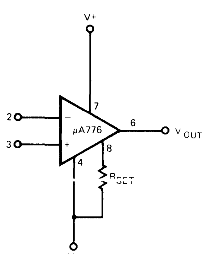


BIASING CIRCUITS

RESISTOR BIASING



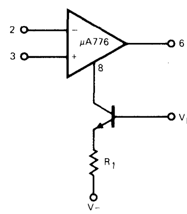
R_{SET} CONNECTED TO GROUND



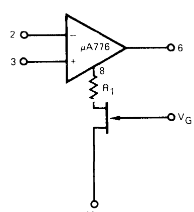
R_{SET} CONNECTED TO V^-

* Recommended for supply voltages less than ±6V.

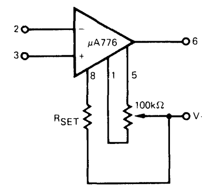
TRANSISTOR CURRENT SOURCE BIASING



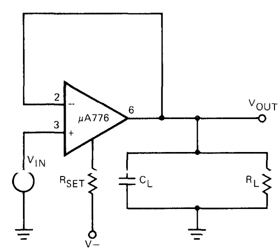
FET CURRENT SOURCE BIASING



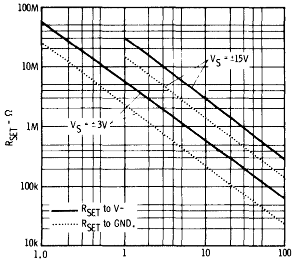
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



SET CURRENT AS A FUNCTION OF SET RESISTOR



QUIESCENT CURRENT SETTING RESISTOR (I_{SET} TO V^-)

V_S	I_{SET}	
	1.5µA	15µA
±1.5 V	1.7MΩ	170kΩ
±3.0 V	3.6MΩ	360kΩ
±6.0 V	7.5MΩ	750kΩ
±15 V	20MΩ	2.0MΩ

Note: The µA776 may be operated with R_{SET} connected to ground or V−.

I_{SET} EQUATIONS:

$$I_{SET} = \frac{V^+ - 0.7 - V^-}{R_{SET}}$$

where R_{SET} is connected to V^-

$$I_{SET} = \frac{V^+ - 0.7}{R_{SET}}$$

where R_{SET} is connected to ground.

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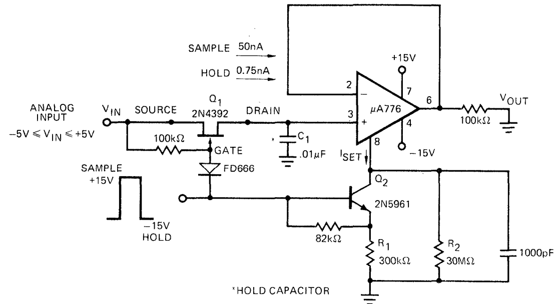
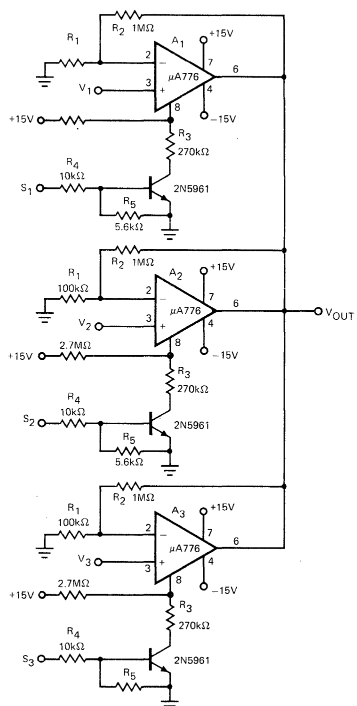
TYPICAL APPLICATIONS

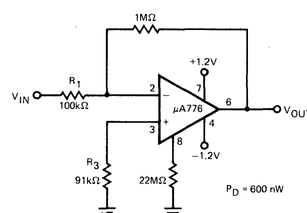
HIGH ACCURACY SAMPLE AND HOLD



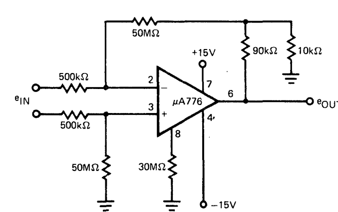
MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FETs



NANO-WATT AMPLIFIER



HIGH INPUT IMPEDANCE AMPLIFIER



μA777

PRECISION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

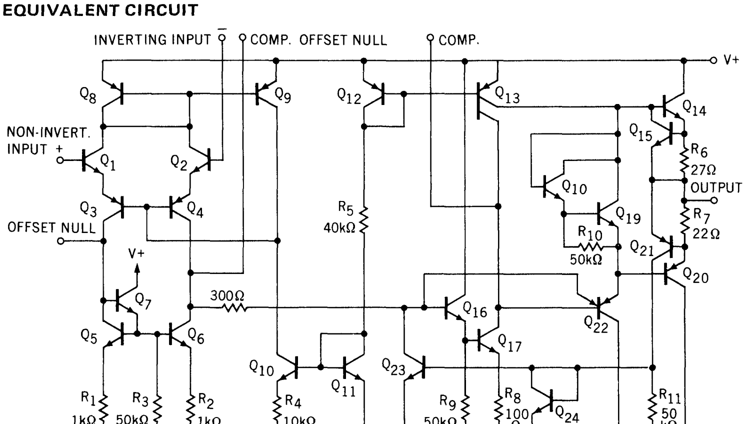
GENERAL DESCRIPTION — The μA777C is a monolithic Precision Operational Amplifier constructed using a low-noise Fairchild Planar* epitaxial process. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low-cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long-term integrators, sample and hold circuits and high-source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777C maintains full ±30 V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short-circuit protection and simple frequency compensation make the device versatile and easily used.

- **LOW OFFSET VOLTAGE AND OFFSET CURRENT**
- **LOW OFFSET VOLTAGE AND CURRENT DRIFT**
- **LOW INPUT BIAS CURRENT**
- **LOW INPUT NOISE VOLTAGE**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

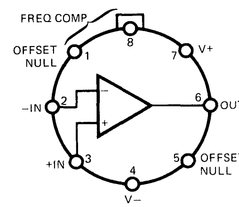
Supply Voltage	±22 V
Internal Power Dissipation	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range	
Metal Can and Hermetic DIP	-65° C to +150° C
Mini DIP	-55° C to +125° C
Operating Temperature Range	0° C to 70° C
Pin Temperature	
Metal Can and Hermetic DIP (Soldering, 60 s)	300° C
Mini DIP (Soldering, 10 s)	260° C
Output Short Circuit Duration (Note 2)	Indefinite

EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

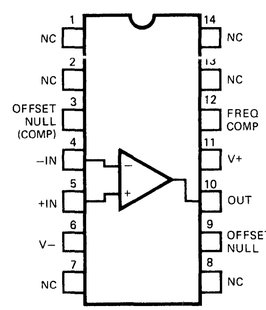


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777HC

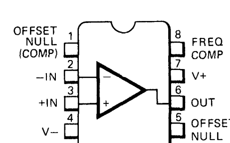
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777DC
μA777C	μA777PC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777TC

*Planar is a patented Fairchild process.

μA777

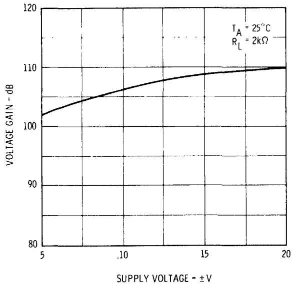
ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50$ kΩ		0.7	5.0	mV
Input Offset Current				0.7	20.0	nA
Input Bias Current				25	100	nA
Input Resistance			1.0	2.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$V	25,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \leq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$						
Input Offset Voltage		$R_S \leq 50$ kΩ		0.8	5.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50$ kΩ		4.0	30	μV/°C
Input Offset Current					40	nA
Average Input Offset Current Drift		$25°C \leq T_A \leq +70°C$		0.01	0.3	nA/°C
		$0°C \leq T_A \leq +25°C$		0.02	0.6	nA/°C
Input Bias Current					200	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50$ kΩ	70	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50$ kΩ		15	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption				60	100	mW

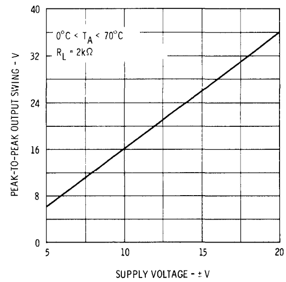
NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C Metal Can, 8.3 mW/°C for the DIP, and 5.6 mW/°C for the Mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C Case Temperature or +75°C Ambient Temperature.

TYPICAL PERFORMANCE CURVES

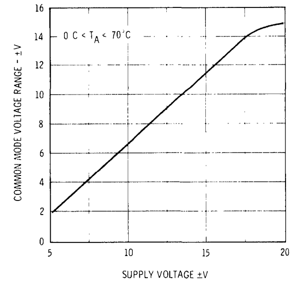
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



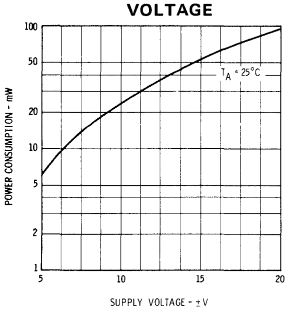
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



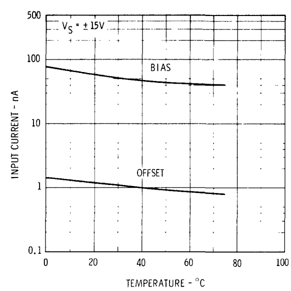
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



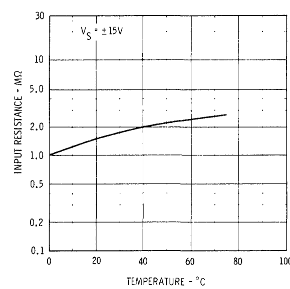
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



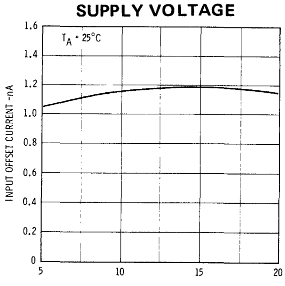
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



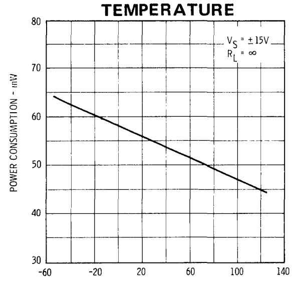
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



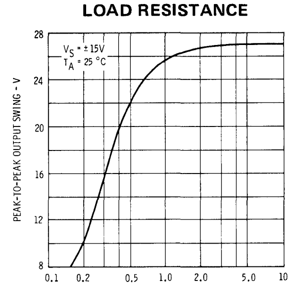
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



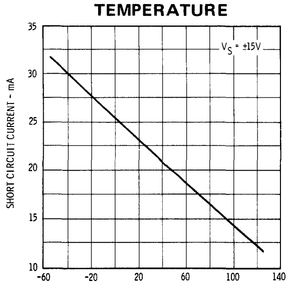
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



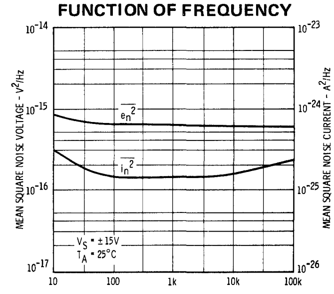
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

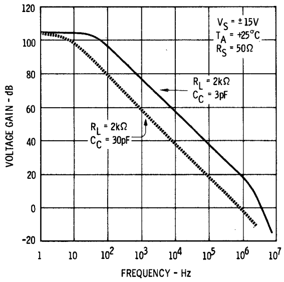


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

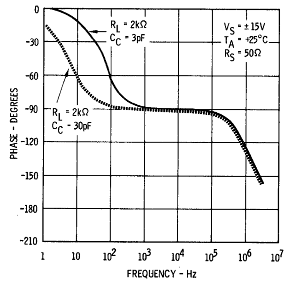


TYPICAL PERFORMANCE CURVES

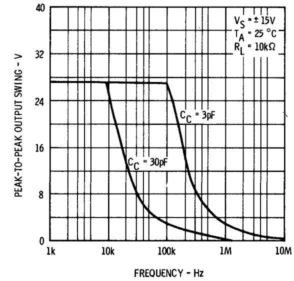
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



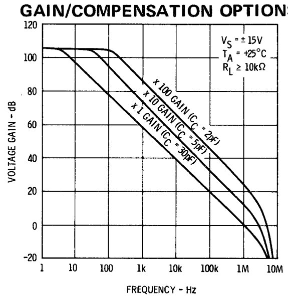
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



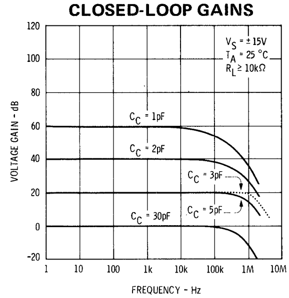
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



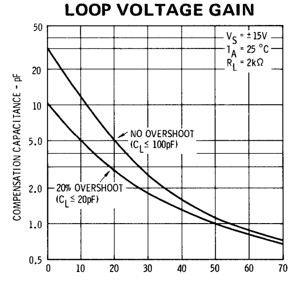
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



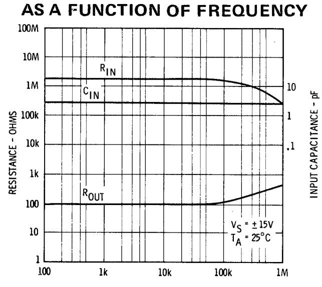
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



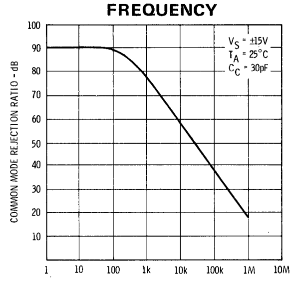
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



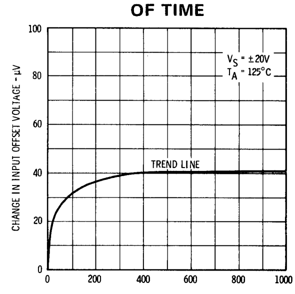
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



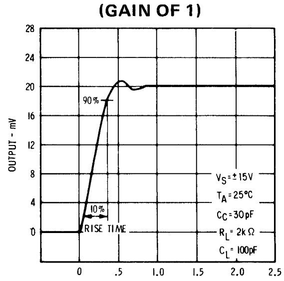
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



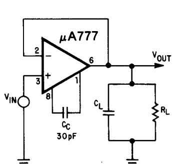
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



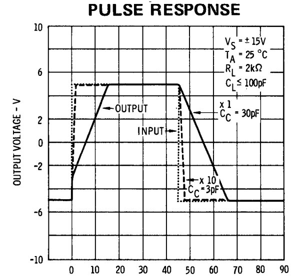
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

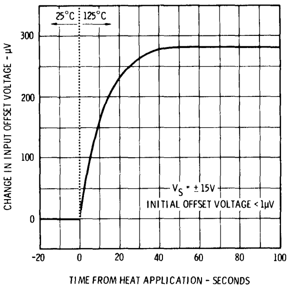


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

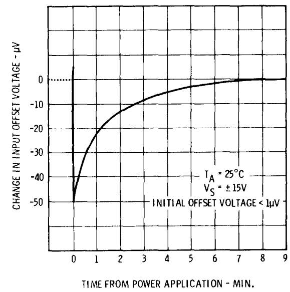


TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

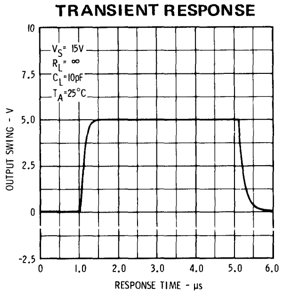


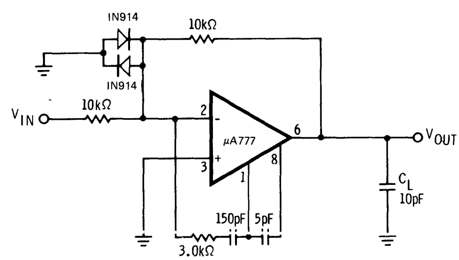
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



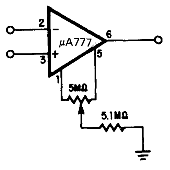
FEED FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE

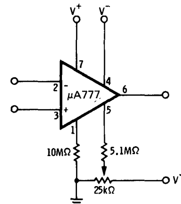




VOLTAGE OFFSET NULL CIRCUIT

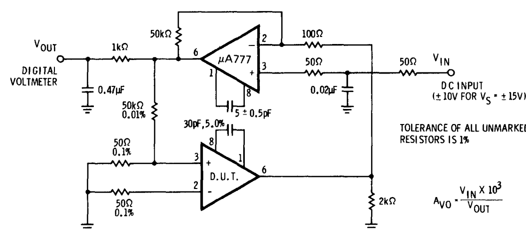


SUGGESTED



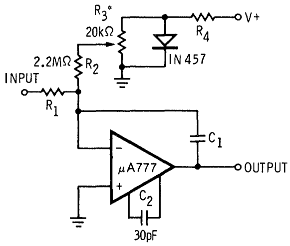
ALTERNATE

GAIN TEST CIRCUIT



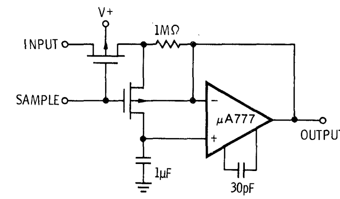
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

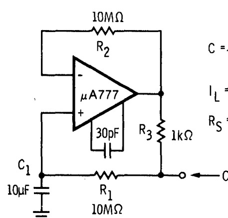


*Adjust R_3 for minimum integrator drift

SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

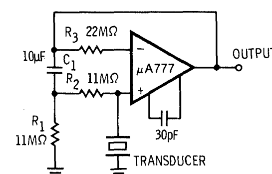


$C = \frac{R_1}{R_3} C_1$

$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$

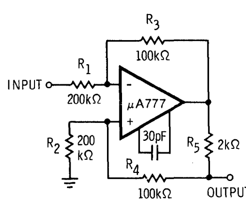
$R_S = R_3$

AMPLIFIER FOR CAPACITANCE TRANSDUCERS



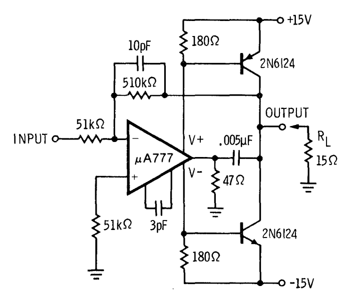
Low Frequency Cutoff $R_1 \times C_1$

BILATERAL CURRENT SOURCE

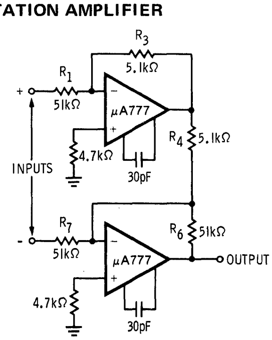


$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$; $R_1 = R_2$; $R_3 = R_4 + R_5$

HIGH SLEW RATE POWER AMPLIFIER



± 100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



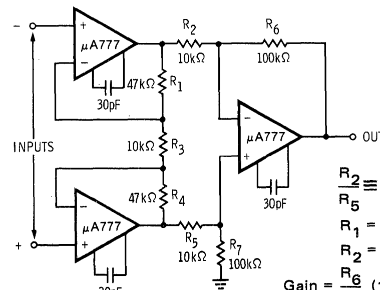
$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7}$ for best CMRR

$R_1 = R_4$

$R_2 = R_5$

$\text{Gain} = \frac{R_6}{R_2} \left(1 + \frac{2R_1}{R_3}\right)$

μA791

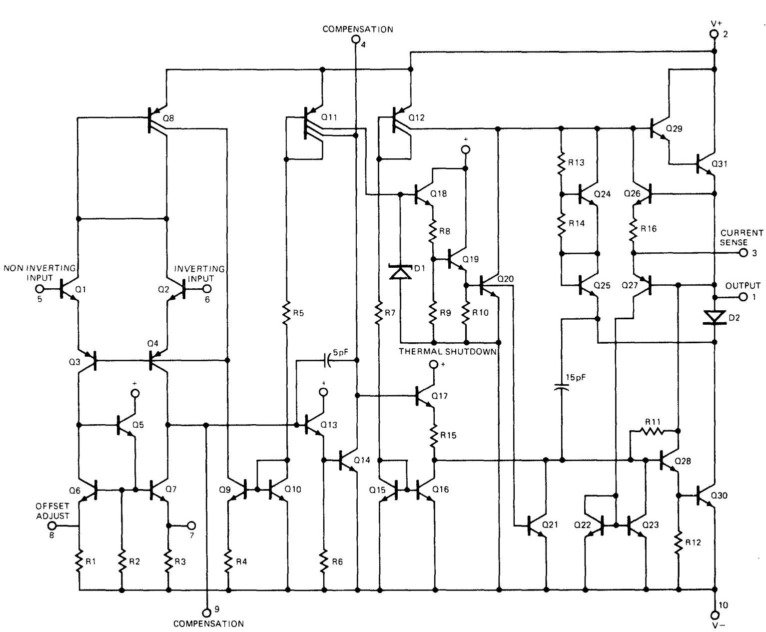
POWER OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA791 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* Epitaxial process with input characteristics similar to the μA741 operational amplifier and 1A available output current. It is intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required. The μA791 is thermal overload and short circuit protected.

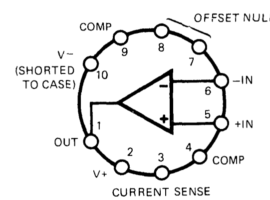
- **CURRENT OUTPUT TO 1 A**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH UP**
- **LARGE COMMON MODE AND DIFFERENTIAL MODE RANGES**
- **THERMAL OVERLOAD PROTECTION**

EQUIVALENT CIRCUIT



NOTE: Pin connections shown are for metal can.

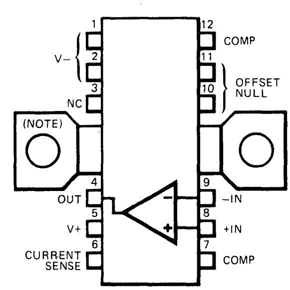
CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5H
PACKAGE CODE K



ORDER INFORMATION

TYPE	PART NO.
μA791C	μA791KC
μA791	μA791KM

12-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P5



ORDER INFORMATION

TYPE	PART NO.
μA791C	μA791P5

NOTES:
The heat sink wings on the P-package are internally connected to V−.
Both pin 1 and pin 2 must be connected externally to V−.

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (μA791)	±22 V
Commercial (μA791C)	±18 V
Peak Output Current	1.25 A
Continuous Internal Power Dissipation (Total Package) (Note 1)	Internally Limited
Peak Internal Power Dissipation (Per Output Transistor for $t \leqslant 5$ s, Note 2)	15 W
Differential Input Voltage	±30 V
Input Voltage (Note 3)	±15 V
Voltages between offset Null and V−	±0.5 V
Operating Junction Temperature	
Military (μA791)	-55° C to +150° C
Commercial (μA791C)	0° C to +125° C
Storage Temperature Range	
Metal Can	-65° C to +150° C
Molded Power DIP	-55° C to +125° C
Pin Temperatures	
Metal Can (Soldering, 60 s max.)	280° C
Molded Power DIP (Soldering, 10 s max.)	260° C

NOTES:

1. Thermal resistance of the packages (without a heat sink)

Package	Junction to Case		Junction to Ambient		Unit
	Typ	Max	Typ	Max	
TO-3 Type (5H)	4	6	35	40	°C/W
Dual In-Line Power (9W)	8	12	50	55	°C/W

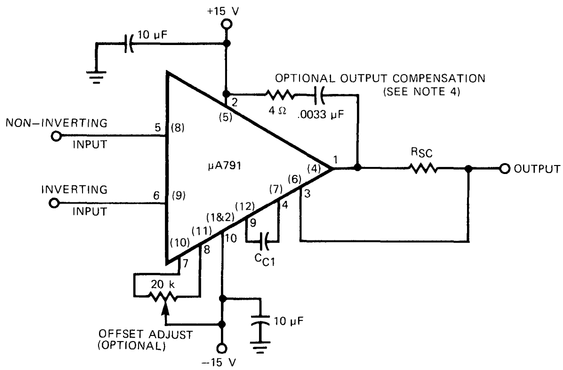
2. Under short circuit conditions, the safe operating area and dc power dissipation limitations must be observed.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

μA791C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	1.0		MΩ
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	$R_L = 1$ kΩ, $V_{OUT} = \pm 10$ V	20k			V/V
	$R_L = 10$ Ω, $V_{OUT} = \pm 10$ V	20k			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1$kΩ	±11.5	±14		V
	$R_{SC} = 0$, $R_L = 10$ Ω	±10	±12.2		V
Output Short Circuit Current	$R_{SC} = 0.7$Ω		1000		mA
	$R_{SC} = 1.5$Ω		500		mA
Supply Current (Zero Signal)				30	mA
The following specifications apply for $0°C \leqslant T_J \leqslant 125°C$					
Input Offset Voltage	$R_S \leqslant 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	$R_L = 1$ kΩ, $V_{OUT} = \pm 10$ V	15k			V/V
	$R_L = 10$ Ω, $V_{OUT} = \pm 10$ V	15k			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1$ kΩ	±10			V
	$R_{SC} = 0$, $R_L = 10$ Ω	±10			V
Supply Current (Zero signal)				30	mA

FREQUENCY COMPENSATION



GAIN	C_C
1	100 pF
10	5 pF
100	Not Req.

R_{SC}	I_{SC}
0.6Ω	1.0 A
1.5Ω	500 mA
3.0Ω	250 mA

NOTES
1. Power supply decoupling capacitors and compensation network components must have short leads and they must be located at the amplifier pins.
2. When short circuit limiting is not required, connect terminals one and three together.
3. Pin connections in parentheses are for plastic packages.
4. Output compensation may be required for some loads.

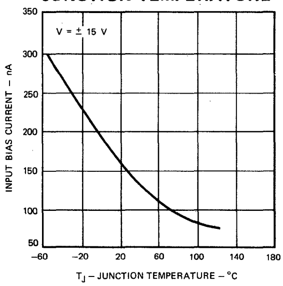
μA791

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified.

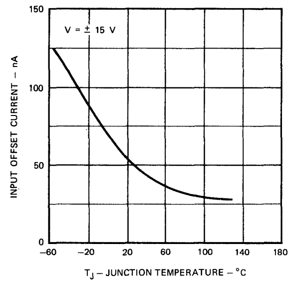
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	$R_L = 1$ kΩ	50,000			V/V
	$R_L = 10$ Ω	50,000			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1$kΩ	±12	±14		V
	$R_{SC} = 0$, $R_L = 10$Ω	±10	±12.2		V
Output Short Circuit Current	$R_{SC} = 0.7$Ω		1000		mA
	$R_{SC} = 1.5$Ω		500		mA
Supply Current (Zero Signal)				25	mA
The following specifications apply for $-55°C \leq T_J \leq 150°C$					
Input Offset Voltage	$R_S \leq 10$ kΩ			6	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	$R_L = 1$ kΩ	25,000			V/V
	$R_L = 10$Ω	25,000			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1$ kΩ	±10			V
	$R_{SC} = 0$, $R_L = 10$Ω	±10			V
Supply Current (Zero Signal)				30	mA

TYPICAL PERFORMANCE CURVES FOR μA791 AND μA791C

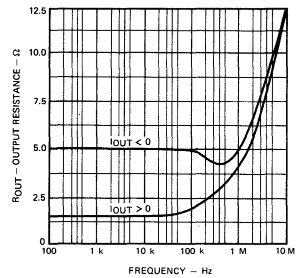
INPUT BIAS CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



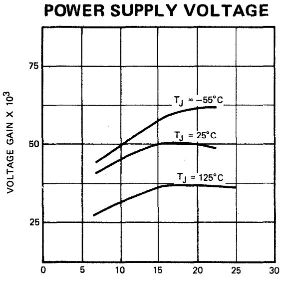
INPUT OFFSET CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



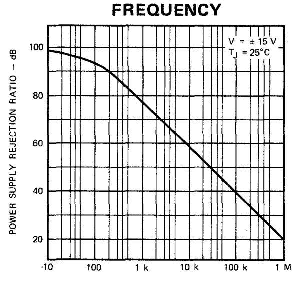
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY (OPEN LOOP)



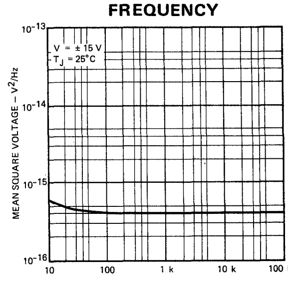
VOLTAGE GAIN AS A FUNCTION OF POWER SUPPLY VOLTAGE



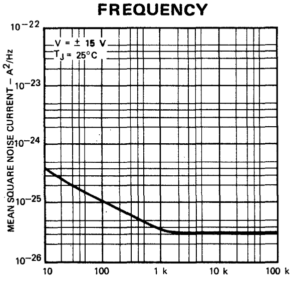
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREQUENCY



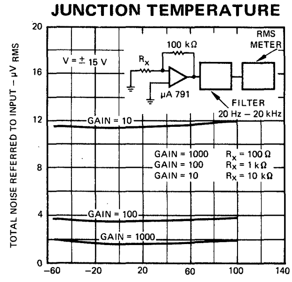
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



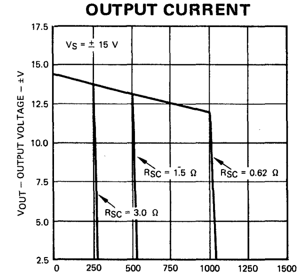
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



TOTAL NOISE (20 Hz-20 kHz) AS A FUNCTION OF JUNCTION TEMPERATURE

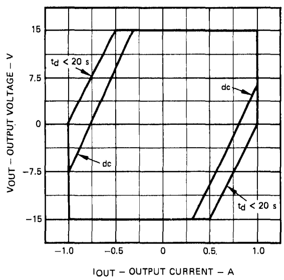


OUTPUT VOLTAGE SWING AS A FUNCTION OF OUTPUT CURRENT

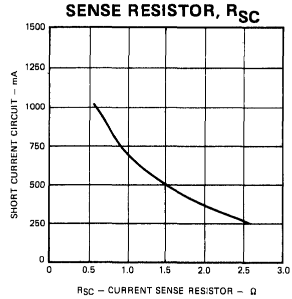


TYPICAL PERFORMANCE CURVES FOR μA791 and μA791C (Cont'd)

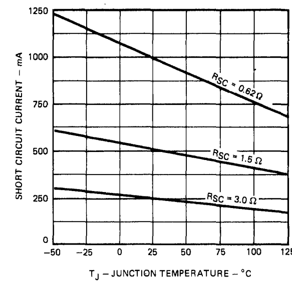
OUTPUT SAFE OPERATING AREA PER OUTPUT TRANSISTOR



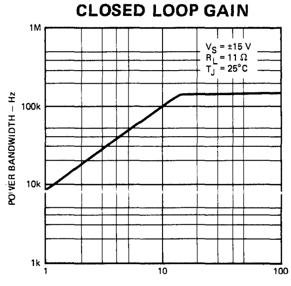
SHORT CIRCUIT CURRENT AS A FUNCTION OF CURRENT SENSE RESISTOR, R_{SC}



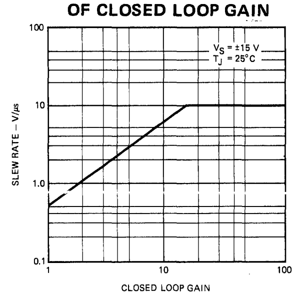
SHORT CIRCUIT CURRENT AS A FUNCTION OF CASE TEMPERATURE



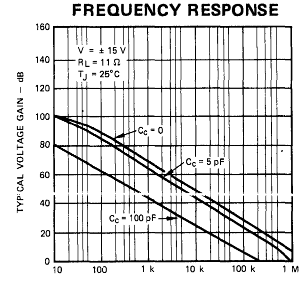
POWER BANDWIDTH AS A FUNCTION OF CLOSED LOOP GAIN



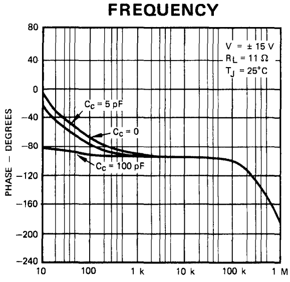
SLEW RATE AS A FUNCTION OF CLOSED LOOP GAIN



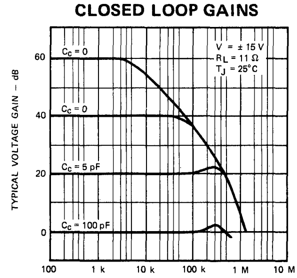
VOLTAGE GAIN AS A FUNCTION OF OPEN LOOP FREQUENCY RESPONSE



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

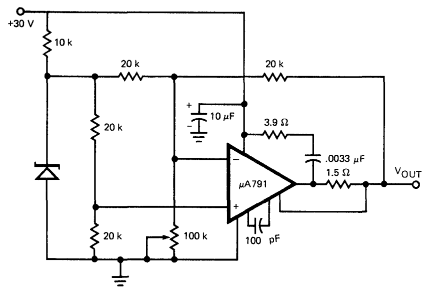


FREQUENCY RESPONSE FOR CLOSED LOOP GAINS



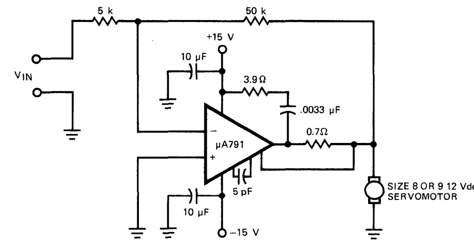
TYPICAL APPLICATIONS

POSITIVE VOLTAGE REGULATOR

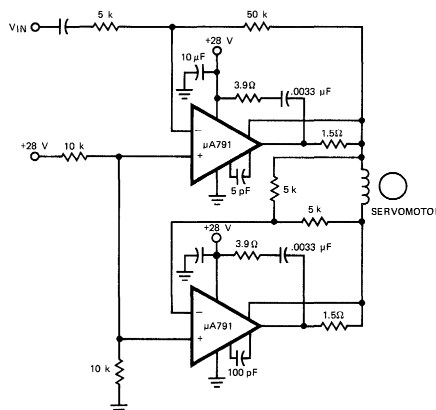


NOTES
3.0 V to 27 V regulator
500 mA output current

DC SERVO AMPLIFIER



AC SERVO AMPLIFIER BRIDGE TYPE



μA798

DUAL OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

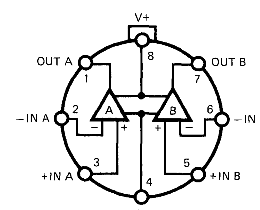
GENERAL DESCRIPTION — The μA798 is a monolithic pair of independent, high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar* epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING NEAR GROUND OR NEGATIVE SUPPLY**
- **INTERNALLY COMPENSATED**
- **WIDE POWER SUPPLY RANGE: SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY OF ±1.5 TO ±18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUT**
- **HIGH OPEN LOOP GAIN — 200 k**
- **EXCEEDS 1458 TYPE PERFORMANCE**
- **OPERATION SPECIFIED AT ±15 V AND +5 V POWER SUPPLIES**
- **HIGH OUTPUT CURRENT SINK CAPABILITY 0.8 mA AT V_{OUT} = 400 mV**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V−	36 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (V−) (Note 1)	−0.3 V (V−) to V+
Internal Power Dissipation (Note 2)	
Metal Can, Hermetic Mini DIP	500 mW
Molded Mini DIP	310 mW
Operating Temperature Range	
Commercial (C)	0°C to +70°C
Military (M)	−55°C to +125°C
Storage Temperature Range	
Molded Package (9T)	−55°C to +125°C
Hermetic Package (5S, 6T)	−65°C to +150°C
Pin Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C
Output Short-Circuit Duration	Note 5

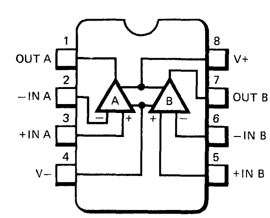
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μ798	μA798HM
μ798C	μA798HC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 6T 9T
PACKAGE CODE R T



ORDER INFORMATION

TYPE	PART NO.
μA798	μA798RM
μA798C	μA798RC
μA798C	μA798TC

*Planar is a patented Fairchild process.

5

μA798

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			10	25	nA
Input Bias Current			−50	−100	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2kΩ	50	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = −10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2k Ω, C_L = 200 pF		60		Degree
Crossover Distortion	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk		0.1		%
Output Voltage Range	R_L = 10k Ω	±13	±14		V
	R_L = 2 kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Notes 3 and 5)	±20	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.0	3.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				6.0	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−300	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	25	300		V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS: V_S = +5.0 V and Ground, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			10	30	nA
Input Bias Current			−70	−150	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ	4.0			V pk-pk
	R_L = 10 kΩ, 5.0 V $\leq V_S \leq$ 30 V	(V+)−1.5			V pk-pk
Output Sink Current	V_{IN} = 1.0 V, V_{OUT} = 200 mV	0.35			mA
Power Supply Current			2.0	3.0	mA

NOTES:

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly 6.3 mW/°C for the Metal Can (5S) and Hermetic Mini DIP (6T), 5.6 mW/°C for the Molded Mini DIP (9T).
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

µA798C

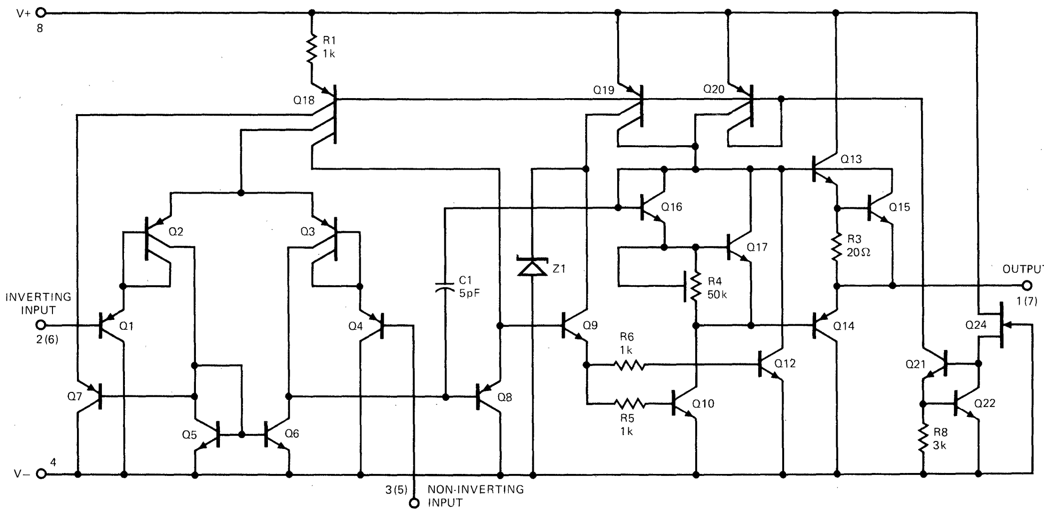
ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$, $T_A = 25°C$ unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	6.0	mV
Input Offset Current			10	50	nA
Input Bias Current			−50	−250	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2$ kΩ	20	200		V/mV
Power Bandwidth	$A_V = 1$, $R_L = 2$ kΩ, $V_{OUT} = 20$ V pk-pk		9.0		kHz
Small Signal Bandwidth	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		1.0		MHz
Slew Rate	$A_V = 1$, $V_{IN} = -10$ V to +10 V		0.6		V/µs
Rise Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		µs
Fall Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		µs
Overshoot	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		20		%
Phase Margin	$A_V = 1$, $R_L = 2$ kΩ, $C_L = 200$ pF		60		Degree
Crossover Distortion	$V_{IN} = 30$ mV pk-pk, $V_{OUT} = 2$ V pk-pk f = 10 kHz		0.1		%
Output Voltage Range	$R_L = 10$ kΩ	±13	±14		V
	$R_L = 2$ kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Notes 3 and 5)	±10	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	µV/V
	Negative		30	150	µV/V
Power Supply Current	$V_{OUT} = 0$, $R_L = \infty$		2.0	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB
The following specification apply for $0°C \leq T_A \leq 70°C$					
Input Offset Voltage				7.5	mV
Average Temperature Coefficient of Input Offset Voltage			10		µV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−400	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ, $V_{OUT} = \pm 10$ V	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	±10			V

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5.0$ V and Ground, $T_A = 25°C$ unless otherwise noted.

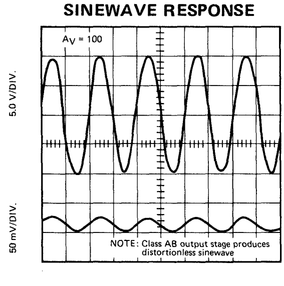
CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			10	50	nA
Input Bias Current			−80	−250	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	µV/V
Output Voltage Range	$R_L = 10$ kΩ	4.0			V pk-pk
	$R_L = 10$ kΩ, $5.0\text{ V} \leq V_S \leq 30$ V	(V+)−1.5			V pk-pk
Output Sink Current	$V_{IN} = 1.0$ V, $V_{OUT} = 200$ mV	0.35			mA
Power Supply Current			2.0	4.0	mA

1/2 OF EQUIVALENT CIRCUIT

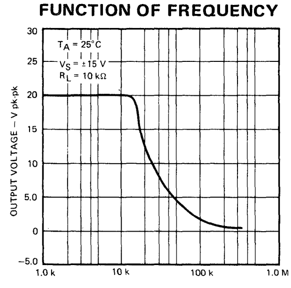


TYPICAL PERFORMANCE CURVES

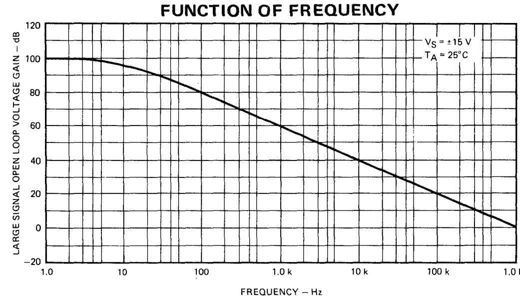
SINEWAVE RESPONSE



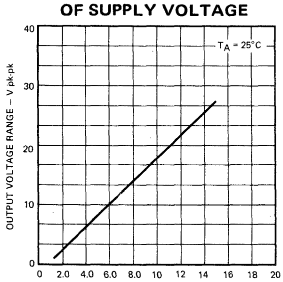
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



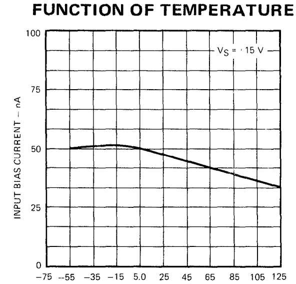
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



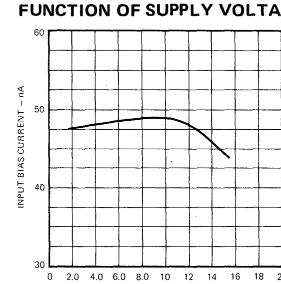
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

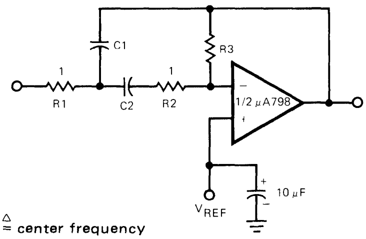


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TYPICAL APPLICATIONS

MULTIPLE FEEDBACK BANDPASS FILTER



$f_o \triangleq$ center frequency

$BW \triangleq$ Bandwidth

R in kΩ

C in μF

$Q = \frac{f_o}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let R1 = R2 = 10 kΩ

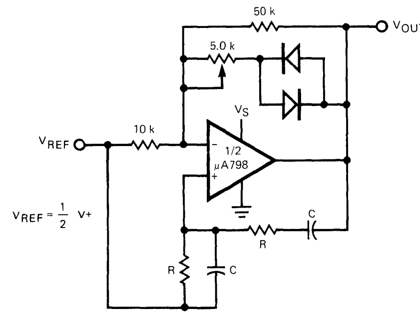
then $R3 = 9(5)^2 - 10$

R3 = 215 kΩ

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

WEIN BRIDGE OSCILLATOR

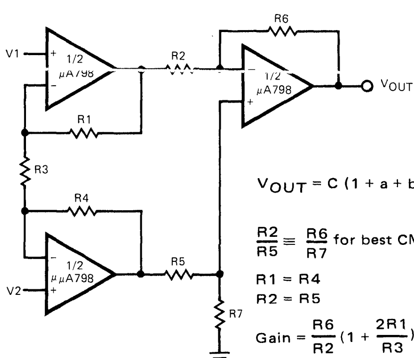


$f_o = \frac{1}{2\pi RC}$ for $f_o = 1$ kHz

R = 16 kΩ

C = 0.01 μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$V_{OUT} = C\,(1 + a + b)(V2 - V1)$

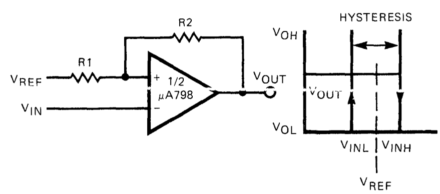
$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

R1 = R4

R2 = R5

$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right) = C\,(1 + a + b)$

COMPARATOR WITH HYSTERESIS

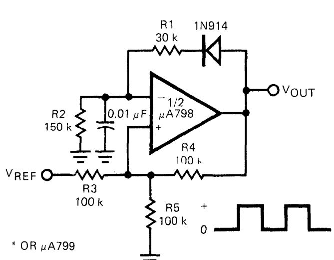


$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

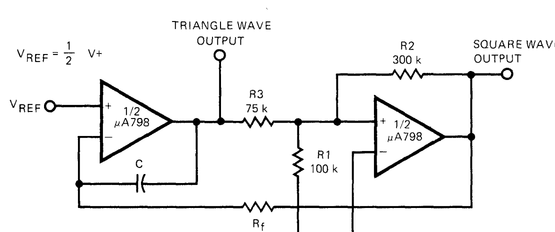
$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

PULSE GENERATOR



* OR μA799

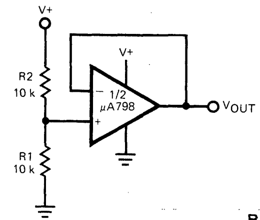
FUNCTION GENERATOR



$f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

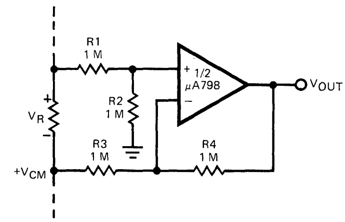
TYPICAL APPLICATIONS (Cont'd)

VOLTAGE REFERENCE



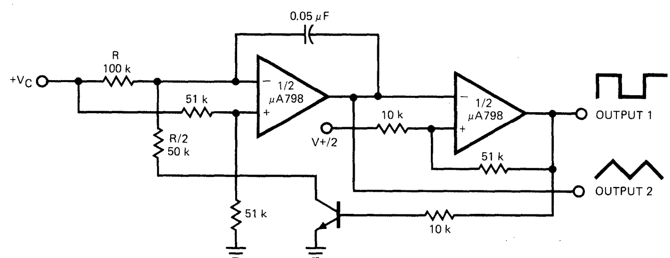
$$V_{OUT} = \frac{R1}{R1 - R2} = \frac{V+}{2}$$

GROUND REFERENCING A DIFFERENTIAL INPUT SIGNAL



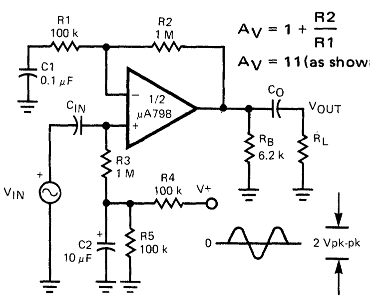
$$V_{OUT} = V_R$$

VOLTAGE CONTROLLED OSCILLATOR



*Wide Control Voltage Range:
$0V_{DC} \leqslant V_C \leqslant 2(V+ - 1.5\,V_{DC})$

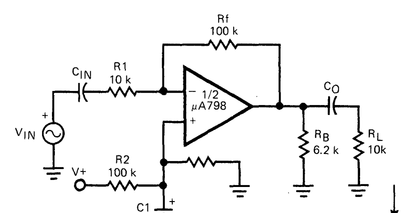
AC COUPLED NON-INVERTING AMPLIFIER



$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (as shown)

AC COUPLED INVERTING AMPLIFIER



$$A_V = \frac{Rf}{R1}$$

A_V = 10 (as shown)

μA1458 • μA1458C • μA1558

DUAL INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA1458/μA1558 are a monolithic pair of Internally Compensated High Performance Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA1458/μA1558 ideal for use as voltage followers. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

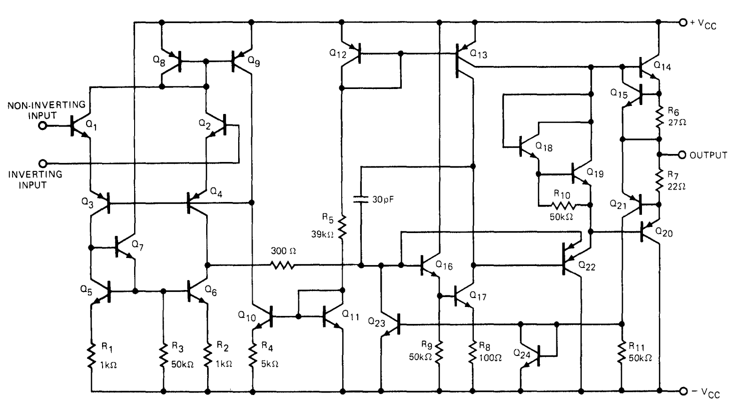
The μA1458/μA1558 are short-circuit protected and require no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see the μA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**
- **MINI DIP PACKAGE**

ABSOLUTE MAXIMUM RATINGS

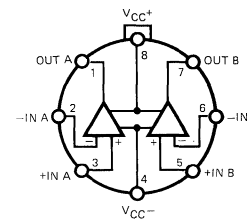
Supply Voltage	
Military (μA1558)	±22 V
Commercial (μA1458 and μA1458C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Mini DIP	310 mW
Differential Input Voltage (Note 2)	±30 V
Common-Mode Input Swing (Note 2)	±15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (μA1558)	–55°C to +125°C
Commercial (μA1458 and μA1458C)	0°C to 70°C
Pin Temperature	
Metal Can (Soldering, 60 s)	300°C
Mini DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT
(EACH SIDE)



Notes on following page.

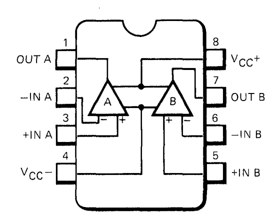
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA1458	μA1458HC
μA1458C	μA1458CHC
μA1558	μA1558HM

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
μA1458	μA1458TC
μA1458C	μA1458CTC
μA1458	μA1458RC
μA1458C	μA1458CRC
μA1558	μA1558RM

*Planar is a patented Fairchild process.

μA1458

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20 Hz, Open Loop	0.3	1.0		MΩ
Parallel Input Capacitance	f = 20 Hz, Open Loop		6.0		pF
Common-Mode Input Impedance	f = 20 Hz		200		MΩ
Common-Mode Input Voltage Swing		±12	±13		V
Equivalent Input Noise Voltage	$A_V = 100$, $R_S = 10$ kΩ, f = 1.0 kHz, BW = 1.0 Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100 Hz	70	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2.0$ kΩ	20k	100k		V/V
Power Bandwidth	$A_V = 1$, $R_L = 2.0$ kΩ, THD ≤ 5%, $V_{OUT} = 20\ V_{pk-pk}$		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	$A_V = 1$		0.8		V/μs
Output Impedance	f = 20 Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	$R_L = 10$ kΩ	±12	±14		V
Power Supply Sensitivity					
$V_{CC}-$ = Constant	$R_S \leq 10$ kΩ		30	150	μV/V
$V_{CC}+$ = Constant	$R_S \leq 10$ kΩ		30	150	μV/V
Power Supply Current	I_+		2.3	5.6	mA
	I_-		2.3	5.6	mA
Power Dissipation	$V_{OUT} = 0$		70	170	mW

The Following Specifications Apply For $0°C \leq T_A \leq 70°C$

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				0.3	μA
Input Bias Current				0.8	μA
Open Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2.0$ kΩ	15k			V/V
Output Voltage Swing	$R_L = 2.0$ kΩ	±10	±13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω		15		μV/°C

μA1458C

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	10	mV
Input Offset Current			.03	0.3	μA
Input Bias Current			0.2	0.7	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20 Hz, Open Loop		1.0		MΩ
Parallel Input Capacitance	f = 20 Hz, Open Loop		6.0		pF
Common-Mode Input Impedance	f = 20 Hz		200		MΩ
Common-Mode Input Voltage Swing		±11	±13		V
Equivalent Input Noise Voltage	A_V = 100, R_S = 10 kΩ, f = 1.0 kHz, BW = 1.0 Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100 Hz	60	90		dB
Open-Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 10 kΩ	20k	100k		V/V
Power Bandwidth	A_V = 1, R_L = 2.0 kΩ, THD ≤ 5%, V_{OUT} = 20 V_{pk-pk}		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	A_V = 1		0.8		V/μs
Output Impedance	f = 20 Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	R_L = 10 kΩ	±11	±14		V
Power Supply Sensitivity					
$V_{CC}-$ = Constant	$R_S \leq 10$ kΩ		30		μV/V
$V_{CC}+$ = Constant	$R_S \leq 10$ kΩ		30		μV/V
Power Supply Current	I_+		2.3	8.0	mA
	I_-		2.3	8.0	mA
Power Dissipation	V_{OUT} = 0		70	240	mW

The Following Specifications Apply For 0°C ≤ T_A ≤ +70°C

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 10 kΩ			12	mV
Input Offset Current				0.4	μA
Input Bias Current				1.0	μA
Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 10 kΩ	15k			V/V
Output Voltage Swing	R_L = 2.0 kΩ	±9.0	±13		V
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω		15		μV/°C

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μA1558

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			0.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20 Hz, Open Loop	0.3	1.0		MΩ
Parallel Input Capacitance	f = 20 Hz, Open Loop		6.0		pF
Common-Mode Input Impedance	f = 20 Hz		200		MΩ
Common-Mode Input Voltage Swing		±12	±13		V
Equivalent Input Noise Voltage	$A_V = 100$, $R_S = 10$ kΩ, f = 1.0 kHz, BW = 1.0 Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100 Hz	70	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2.0$ kΩ	50k	200k		V/V
Power Bandwidth	$A_V = 1$, $R_L = 2.0$ kΩ, THD ≤ 5%, $V_{OUT} = 20\ V_{pk-pk}$		14		kHz
Unity Gain Crossover Frequency (Open Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	$A_V = 1$		0.8		V/μs
Output Impedance	f = 20 Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	$R_L = 10$ kΩ	±12	±14		V
Power Supply Sensitivity					
$V_{CC}-$ = Constant	$R_S \leq 10$ kΩ		30	150	μV/V
$V_{CC}+$ = Constant	$R_S \leq 10$ kΩ		30	150	μV/V
Power Supply Current	I_+		2.3	5.0	mA
	I_-		2.3	5.0	mA
Power Dissipation	$V_{OUT} = 0$		70	150	mW

The Following Specifications Apply For $-55°C \leqslant T_A \leqslant +125°C$

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Input Offset Current				0.5	μA
Input Bias Current				1.5	μA
Open-Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2.0$ kΩ	25k			V/V
Output Voltage Swing	$R_L = 2$ kΩ	±10	±13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω		15		μV/°C

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal can and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 70°C ambient temperature.

TYPICAL PERFORMANCE CURVES FOR μA1458, μA1458C AND μA1558

($V_{CC}+$ = +15 V, $V_{CC}-$ = −15 V, T_A = 25°C unless otherwise noted)

OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF POWER SUPPLY VOLTAGES

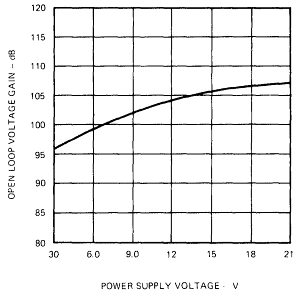


Fig. 1

OPEN-LOOP FREQUENCY RESPONSE

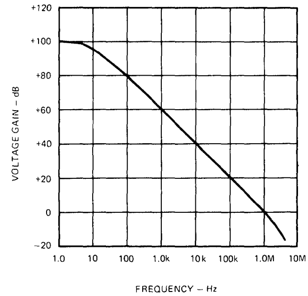


Fig. 2

POWER BANDWIDTH (LARGE SIGNAL SWING AS A FUNCTION OF FREQUENCY)

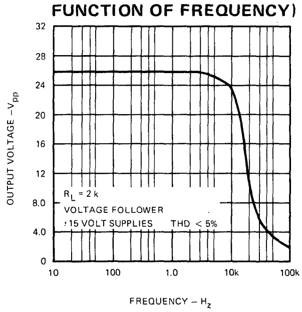


Fig. 3

POWER DISSIPATION AS A FUNCTION OF POWER SUPPLY VOLTAGE

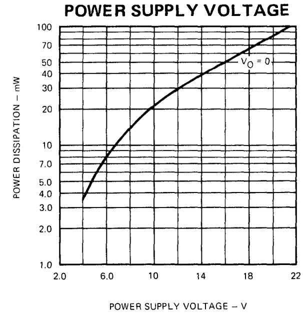


Fig. 4

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

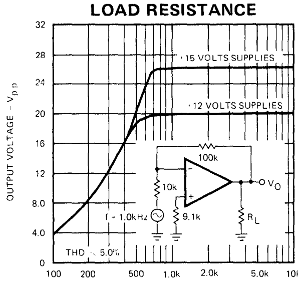


Fig. 5

OUTPUT NOISE AS A FUNCTION OF SOURCE RESISTANCE

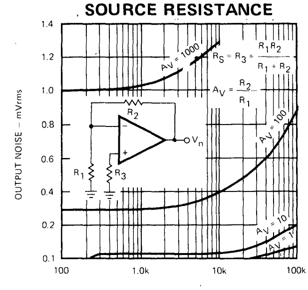


Fig. 6

5

HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER

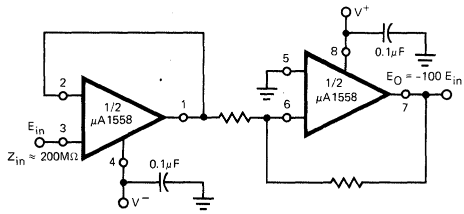
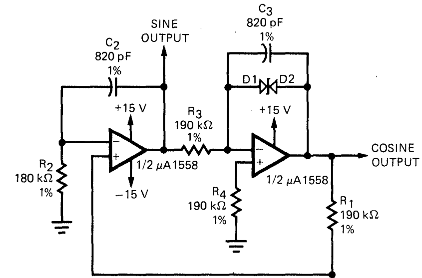


Fig. 7

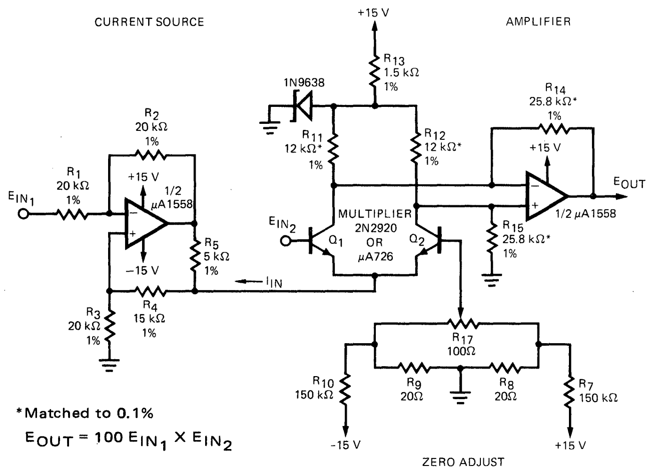
QUADRATURE OSCILLATOR



$$*f = \frac{1}{2\pi\sqrt{C_2R_2C_3R_3}} \quad (R_1C_1 = R_2C_2)$$

Fig. 8

ANALOG MULTIPLIER

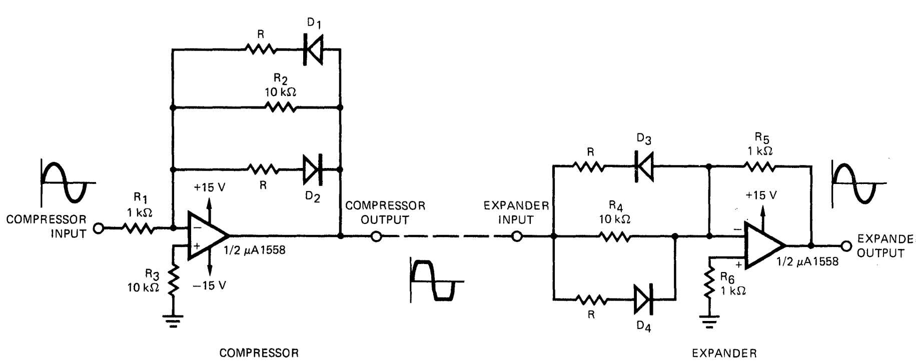


*Matched to 0.1%

$E_{OUT} = 100\ E_{IN_1} \times E_{IN_2}$

Fig. 9

COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R (10 kΩ > R ⩾ 0)

NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT.

Fig.10

µA3301 • µA3401

QUAD SINGLE-SUPPLY AMPLIFIERS

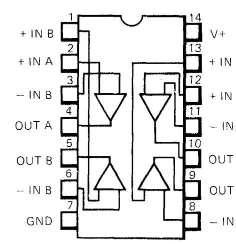
FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The µA3301/µA3401 are monolithic Quad Amplifiers consisting of four independent, dual input, internally compensated amplifiers. They are constructed using the Fairchild Planar* epitaxial process. They were designed specifically to operate from a single power supply voltage and to provide a large output voltage swing. The non-inverting input function is achieved by using a current mirror. Applications for the µA3301/µA3401 are ac amplifiers, FC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

- SINGLE SUPPLY OPERATION – +4.0 Vdc to +28 Vdc
- INTERNALLY COMPENSATED
- WIDE UNITY GAIN BANDWIDTH – 5.0 MHz
- LOW INPUT BIAS CURRENT – 50 nA TYPICAL
- HIGH OPEN LOOP GAIN – 1000 V/V MINIMUM

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 9A
PACKAGE CODE P



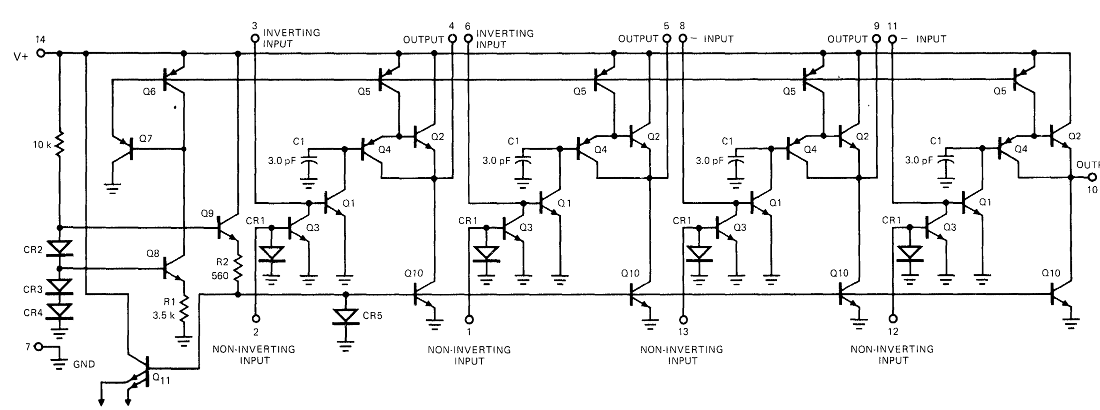
ORDER INFORMATION

TYPE	PART NO.
µA3301	µA3301PC
µA3401	µA3401PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
µA3301	+28 V
µA3401	+18 V
Non-Inverting Input Current	5.0 mA
Sink Current	50 mA
Source Current	50 mA
Internal Power Dissipation (Note 1)	670 mW
Operating Temperature Range	
µA3301	−40°C to +85°C
µA3401	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



MULTIPLE EMITTER (8) TRANSISTOR – ONE EMITTER CONNECTED TO EACH INPUT

*Planar is a patented Fairchild process.

μA3301

ELECTRICAL CHARACTERISTICS: V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	$R_L = \infty$, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Current Mirror Gain (Note 4)	(I_{Mirror} = 200 μAdc)	0.80	0.98	1.16	A/A
Output Current					
Source	V_{OH} = 0.4 Vdc	3.0	10		mA
	V_{OH} = 9.0 Vdc		7.0		mA
Sink (Note 5)	V_{OL} = 0.4 Vdc	0.5	0.87		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for $-40°C \leq T_A \leq +85°C$.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input		1600		V/V
Input Bias Current	$R_L = \infty$			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		$V_{pk\text{-}pk}$

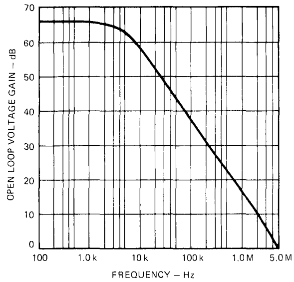
μA3401

ELECTRICAL CHARACTERISTICS: V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

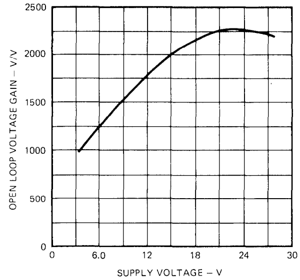
CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	$R_L = \infty$, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Output Current					
Source		5.0	10		mA
Sink (Note 5)		0.5	1.0		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for $0°C \leq T_A \leq 70°C$.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input	800			V/V
Input Bias Current	$R_L = \infty$			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		$V_{pk\text{-}pk}$

TYPICAL PERFORMANCE CURVES

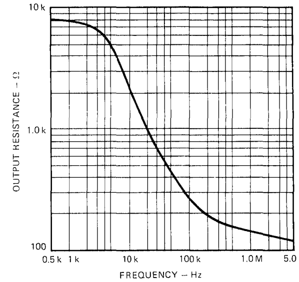
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



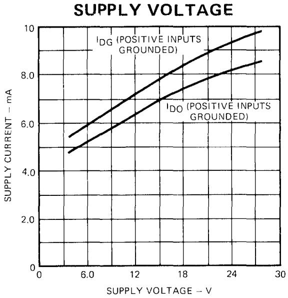
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



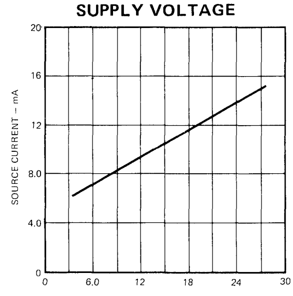
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



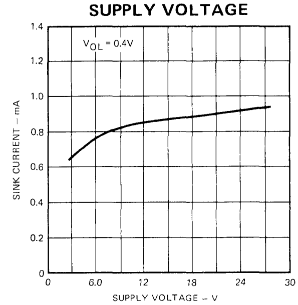
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



NOTES:

1. Rating applies to T_A up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
2. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
3. Input bias current can be defined only for the inverting input. The non-inverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the non-inverting input.
5. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
6. When used as a non-inverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
7. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.
8. The quiescent current will increase approximately 0.3 mA for each non-inverting input which is grounded. Leaving the non-inverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
9. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.
10. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration as shown in the peak-to-peak output voltage test circuit.

TEST CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

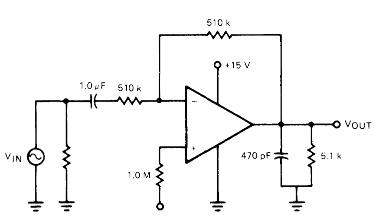
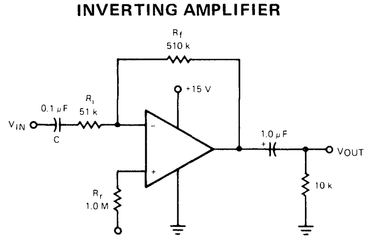


Fig. 1

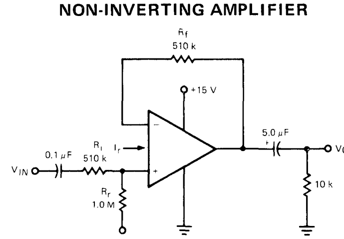
INVERTING AMPLIFIER



$$A_V = -\frac{R_f}{R_i} \text{ for } \frac{1}{\omega C} \ll R_i$$

Fig. 2

NON-INVERTING AMPLIFIER

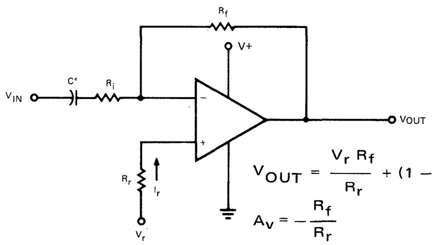


$$A_V = \frac{R_f}{R_i + \frac{26}{I_r\,(mA)}} \simeq 1 \qquad BW = 250\ kHz$$

Fig. 3

TEST CIRCUITS (Cont'd)

INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



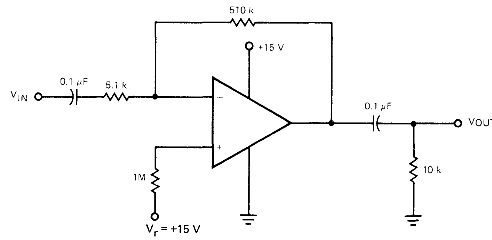
$$V_{OUT} = \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right) \phi$$

$$A_V = -\frac{R_f}{R_r}$$

*Select for low frequency response.

Fig. 4

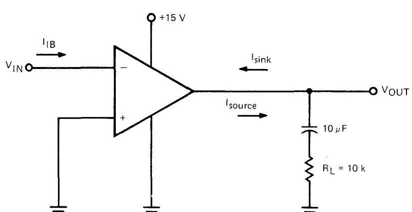
INVERTING AMPLIFIER WITH $A_V = 100$ AND $V_r = V+$



$A_V = 100$ $f_L = 300$ Hz, $f_H = 50$ kHz

Fig. 5

OPEN LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)

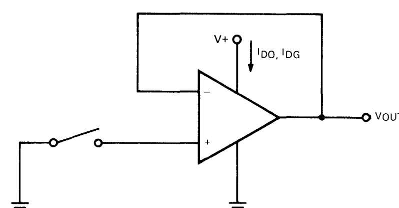


$$R_{in} = \frac{\Delta V_{IN}}{\Delta I_{IB}} \qquad A_{vol} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

Amplifier must be biased by V_{IN} in the linear operating region

Fig. 6

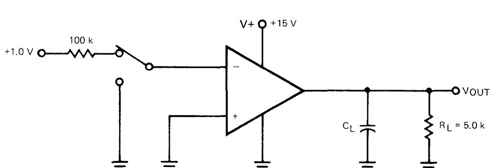
QUIESCENT POWER SUPPLY CURRENT



I_{DO} is total supply current with noninverting input open.
I_{DG} is total supply current with noninverting input grounded.

Fig. 7

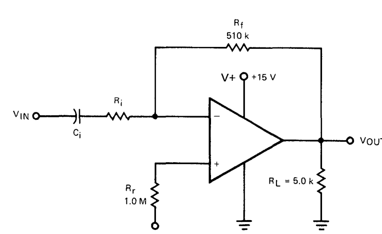
OUTPUT VOLTAGE SWING



V_{OL} measured with inverting input biased as shown.
V_{OH} measured with inverting input grounded.

Fig. 8

PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{OUT} \simeq V+ \frac{R_f}{R_r} \simeq \frac{V+}{2} \text{ for } R_r \simeq 2 R_f$$

Fig. 9

NORMAL DESIGN PROCEDURE

Output Q-Point Biasing

A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the non-inverting input to effect the biasing as shown in Figures 2 and 3. The high impedance of the collector of the non-inverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the non-inverting input current be in the 5.0 μA to 100 μA range.

V+ Reference Voltage (Figures 2 and 3)

The non-inverting input is normally returned to the V+ voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5.0 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to 1/2 R_r will now bias the amplifier output dc level to approximately:

$$\frac{V+}{2}$$

This allows for maximum dynamic range of the output voltage.

Reference Voltage Other Than V+ (Figure 4)

The biasing resistor R_r may be returned to a voltage (V_r) other than V+. By setting $R_f = R_r$, (still keeping I_r between 5.0 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{OUT} = \frac{(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 V @ +25°C).

The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5.0 μA to 100 μA.

Gain Determination — Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

Non-Inverting Amplifier

Although recommended as an inverting amplifier, the 3301/3401 may be used in the non-inverting mode (Figure 3). The amplifier gain in this configuration is subject to the same error terms that affects the output Q point biasing so the gain may deviate as much as ±20 % from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately:

$$\frac{26}{I_r}\ \Omega,$$

where I_r is input current in mA. The non-inverting gain expression is given by:

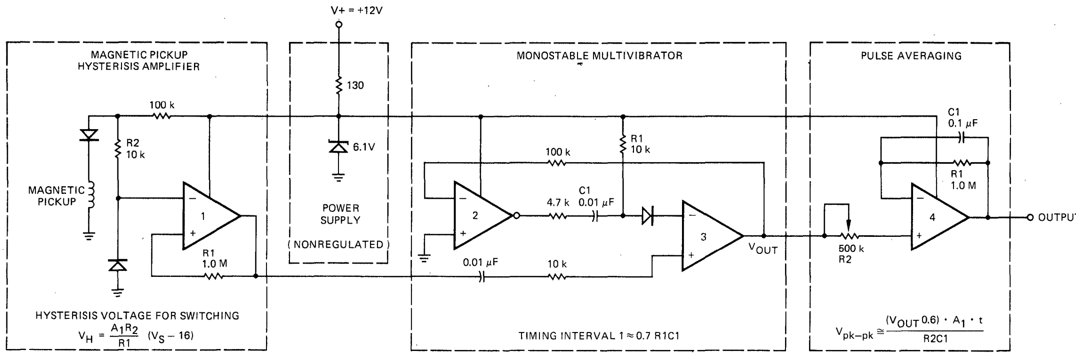
$$A_V = \frac{R_f}{R_i + \dfrac{26}{I_r\ (mA)}} \quad \pm 20\%.$$

The bandwidth of the non-inverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for non-inverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

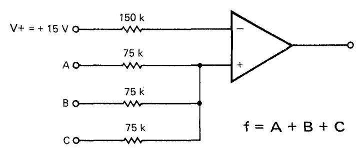
5

TYPICAL APPLICATIONS

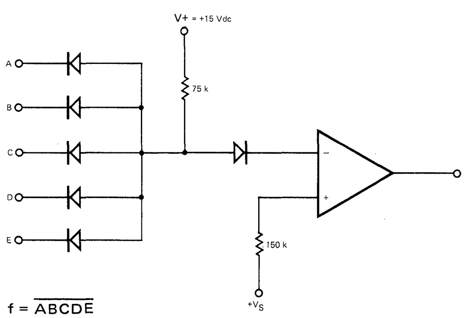
TACHOMETER CIRCUIT



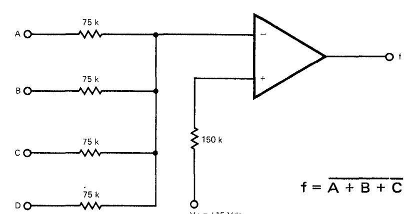
LOGIC OR GATE



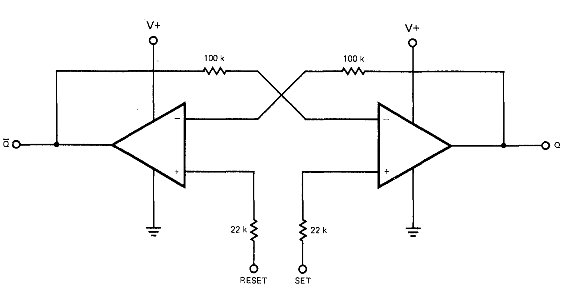
LOGIC NAND GATE (Large Fan In)



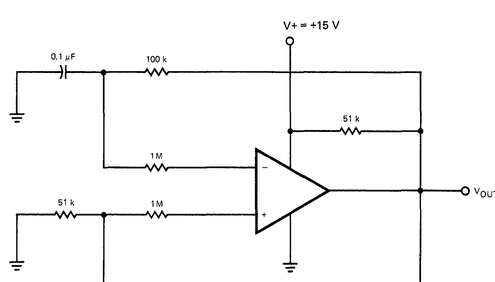
LOGIC NOR GATE



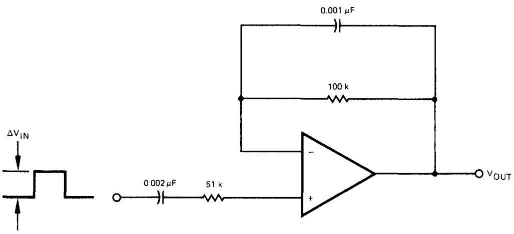
R-S FLIP-FLOP



STABLE MULTIVIBRATOR

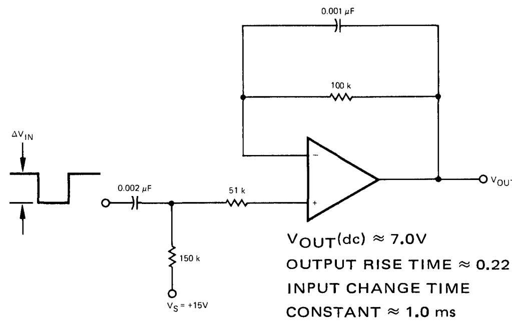


POSITIVE EDGE DIFFERENTIATOR



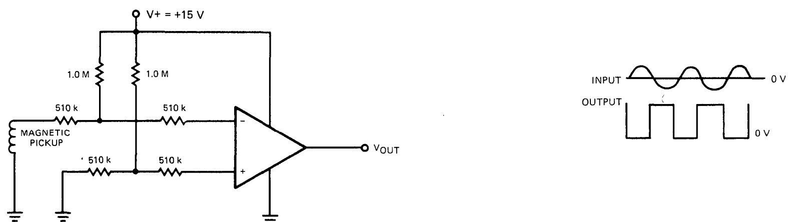
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

NEGATIVE EDGE DIFFERENTIATOR

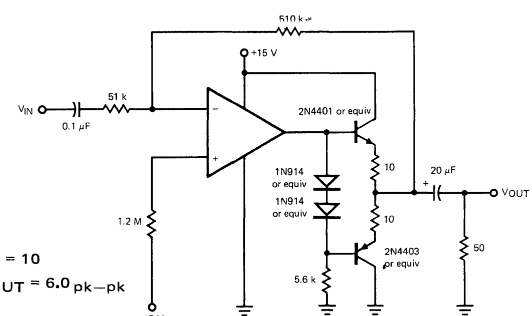


V_{OUT}(dc) ≈ 7.0V
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

ZERO CROSSING DETECTOR

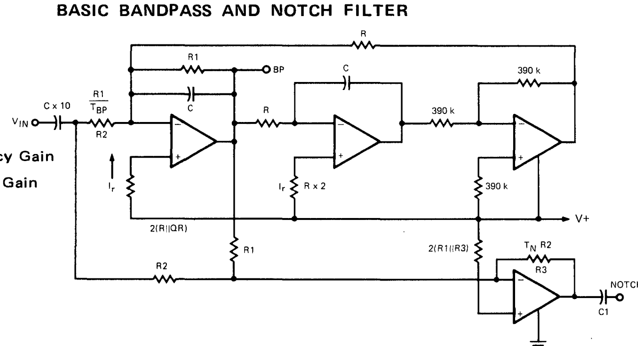


AMPLIFIER AND DRIVER FOR 50 Ω LINE



$A_V = 10$
$V_{OUT} = 6.0$ pk–pk

BASIC BANDPASS AND NOTCH FILTER



T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain
$\omega 0 = \frac{1}{RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
R3 = T_N R2

μA3303 • μA3403 • μA3503

QUAD OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA3303, μA3403 and μA3503 are monolithic Quad Operational Amplifiers consisting of four independent high-gain, internally frequency-compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. They are constructed using the Fairchild Planar* epitaxial process.

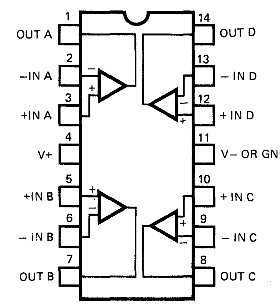
- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **FOUR INTERNALLY COMPENSATED OPERATIONAL AMPLIFIERS IN A SINGLE PACKAGE**
- **WIDE POWER SUPPLY RANGE: SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY OF ±1.5 TO ±18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUTS**
- **HIGH OPEN LOOP GAIN — 200 k**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V−		36 V
Differential Input Voltage (Note 1)		±30 V
Input Voltage (V−) (Note 1)		−0.3 V(V−) to V+
Internal Power Dissipation (Note 2)		670 mW
Operating Temperature Range	μA3303	−40°C to +85°C
	μA3403	0°C to +70°C
	μA3503	−55°C to +125°C
Storage Temperature Range		
Molded Package		−55°C to +125°C
Hermetic Package		−65°C to +150°C
Pin Temperature		
Molded Package (Soldering, 10 s)		260°C
Hermetic Package (Soldering, 60 s)		300°C

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

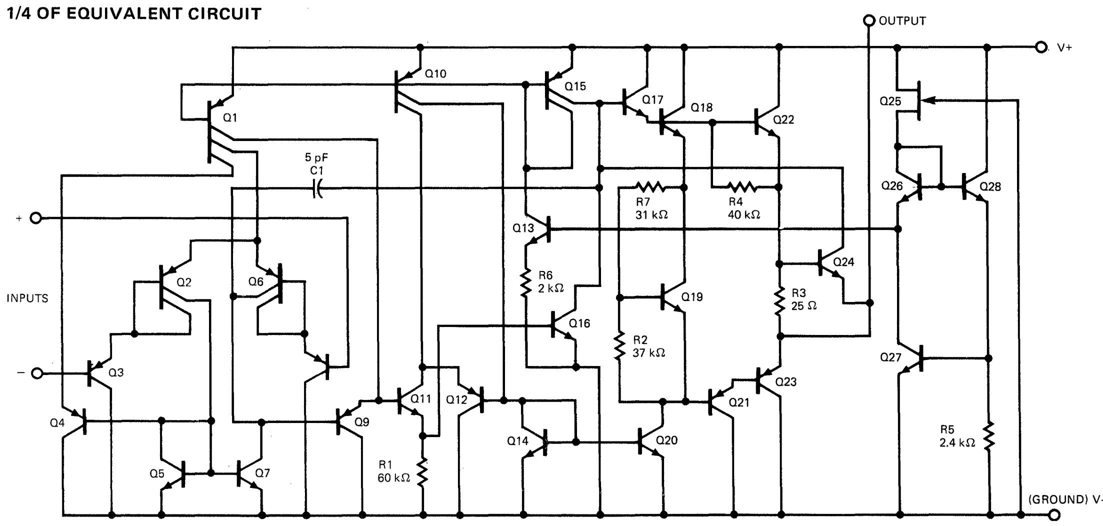
PACKAGE OUTLINES	6A	9A
PACKAGE CODES	D	P



ORDER INFORMATION

TYPE	PART NO.
μA3303	μA3303PC
μA3403	μA3403PC
μA3403	μA3403DC
μA3503	μA3503DC

1/4 OF EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

µA3303

ELECTRICAL CHARACTERISTICS: V+ = +14 V, V- = Gnd, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	75	nA
Input Bias Current			200	–500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+12 to Gnd	+12.5 to Gnd		V
Common Mode Rejection Ratio	$R_S \leqslant 10$ kΩ	70	90		dB
Large Signal Open-Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 10 V pk-pk THD = 5%		18		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1		0.6		V/µs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		µs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		µs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		5.0		%
Phase Margin	A_V = 1, R_L = 2 kΩ, C_L = 200 pF		60		Degree
Crossover Distortion	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	R_L = 10 kΩ	12	12.5		V
	R_L = 2 kΩ	10	12		V
Individual Output Short Circuit Current		±10	±30	±45	mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio			30	150	µV/V
Power Supply Current	V_{OUT} = 0, $R_L = \infty$		2.8	7.0	mA
The following specification apply for $-40°C \leqslant T_A \leqslant 85°C$					
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10		µV/°C
Input Offset Current				250	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				-1000	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	15			V/mV
Output Voltage Range	R_L = 2 kΩ	+10			V

ELECTRICAL CHARACTERISTICS: V_S+ = +5.0 V, V_S- = G, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage				10	mV
Input Offset Current				75	nA
Input Bias Current				-500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	µV/V
Output Voltage Range	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V $\leqslant V_S \leqslant$ 30 V	(V+) –1.7			V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		–120		dB

μA3403

ELECTRICAL CHARACTERISTICS: $V_S = \pm15$ V, $T_A = 25°C$ unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	$V_{OUT} = \pm10$ V, $R_L = 2$ kΩ	20	200		V/mV
Power Bandwidth	$A_V = 1$, $R_L = 2$ kΩ, $V_{OUT} = 20$ V pk-pk THD = 5%		9.0		kHz
Small Signal Bandwidth	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		1.0		MHz
Slew Rate	$A_V = 1$, $V_{IN} = -10$ V to +10 V		0.6		V/μs
Rise Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Fall Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Overshoot	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		5.0		%
Phase Margin	$A_V = 1$, $R_L = 2$ kΩ, $C_L = 200$ pF		60		Degree
Crossover Distortion	$V_{IN} = 30$ mV pk-pk, $V_{OUT} = 2$ V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	$R_L = 10$ kΩ $R_L = 2$ kΩ	±12 ±10	±13.5 ±13		V V
Individual Output Short Circuit Current		±10	±30	±45	mA
Output Impedance	f = 20 Hz		80		Ω
Power Supply Rejection Ratio	Positive Negative		30 30	150 150	μV/V μV/V
Power Supply Current	$V_{OUT} = 0$, $R_L = \infty$		2.8	7.0	mA
The following specification apply for $0°C \leq T_A \leq 70°C$					
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−800	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ, $V_{OUT} = \pm10$ V	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	±10			V

ELECTRICAL CHARACTERISTICS: $V_{S+} = +5.0$ V, $V_{S-} = G$, $T_A = 25°C$ unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	10	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range	$R_L = 10$ kΩ $R_L = 10$ kΩ, $5.0\text{ V} \leq V_S \leq 30$ V	3.5 (V+) −1.7			V pk-pk V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

μA3503

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2kΩ	50	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = −10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		5.0		%
Phase Margin	A_V = 1, R_L = 2k Ω, C_L = 200 pF		60		Degree
Crossover Distortion at f = 10 kHz	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk		1.0		%
Output Voltage Range	R_L = 10 kΩ	±12	±13.5		V
	R_L = 2 kΩ	±10	±13		V
Individual Output Short Circuit Current	(Note 3)	±20	±30	±45	mA
Output Impedance	f = 20 Hz		80		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.8	4.0	mA
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				6.0	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current			−300	−1500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	25	300		V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS: V_S = +5.0 V, V_{S^-} = G, T_A = 25°C unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, $5.0 V \leq V_S \leq 30 V$	(V+)−1.7			V pk-pk
Power Supply Current			2.5	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

NOTES:

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.

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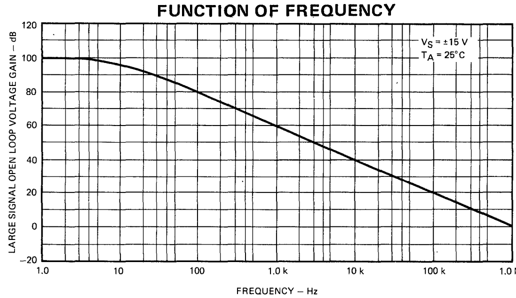
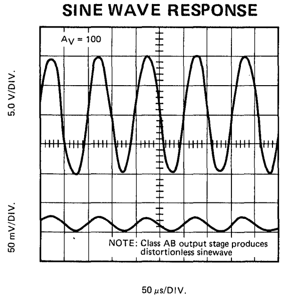
TYPICAL PERFORMANCE CURVES

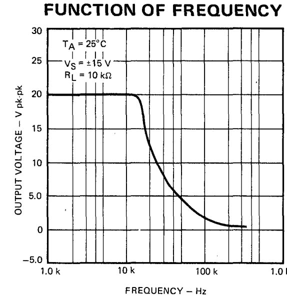
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



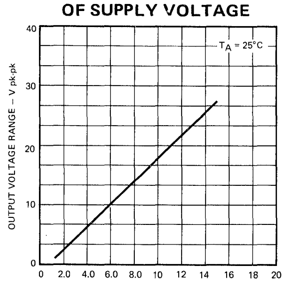
SINE WAVE RESPONSE



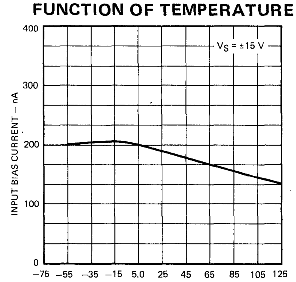
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



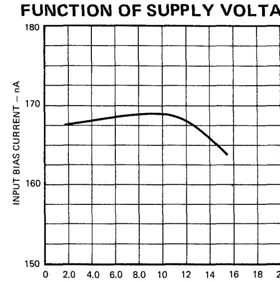
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

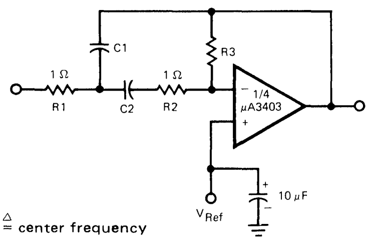


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TYPICAL APPLICATIONS

MULTIPLE FEEDBACK BANDPASS FILTER



$f_o \triangleq$ center frequency

$BW \triangleq$ Bandwidth

R in kΩ

C in μF

$Q = \frac{f_o}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let R1 = R2 = 10 kΩ

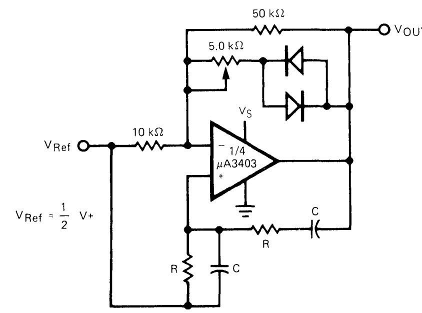
then $R3 = 9(5)^2 - 10$

R3 = 215 kΩ

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

WEIN BRIDGE OSCILLATOR

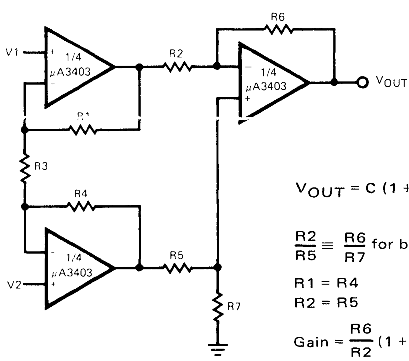


$f_o = \frac{1}{2\pi RC}$ for $f_o = 1$ kHz

R = 16 kΩ

C = 0.01 μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$V_{OUT} = C\,(1 + a + b)(V2 - V1)$

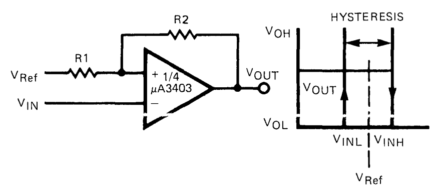
$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

R1 = R4

R2 = R5

$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right) = C\,(1 + a + b)$

COMPARATOR WITH HYSTERESIS

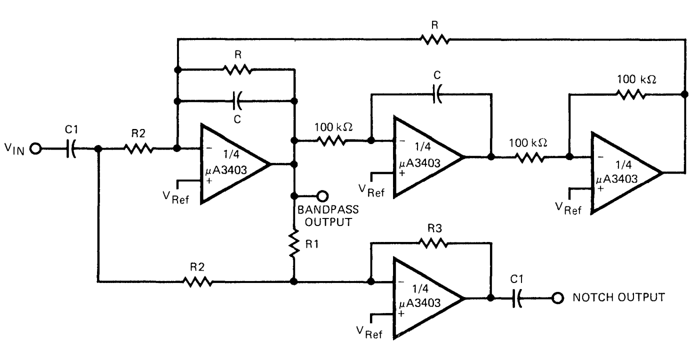


$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{Ref}) + V_{Ref}$

$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{Ref}) + V_{Ref}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

BI-QUAD FILTER



$Q = \frac{f_o}{BW}$

where

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10C$

Example:

f_o = 1000 Hz

BW = 100 Hz

$T_{BP} = 1$

$T_N = 1$

R = 160 kΩ

R1 = 1.6 MΩ

R2 = 1.6 MΩ

R3 = 1.6 MΩ

C = 0.001 μF

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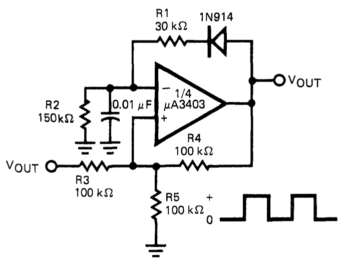
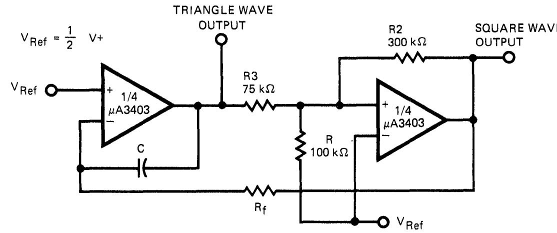
TYPICAL APPLICATIONS (Cont'd)

PULSE GENERATOR

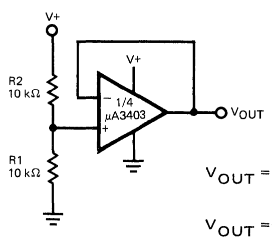


FUNCTION GENERATOR



$$f = \frac{R1 + R2}{4CR_fR1} \quad \text{if} \quad R3 = \frac{R2R1}{R2 + R1}$$

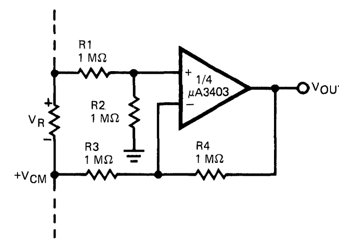
VOLTAGE REFERENCE



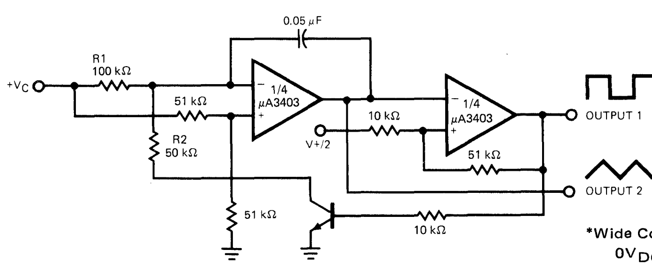
$$V_{OUT} = \frac{R1}{R1 + R2} \left(= \frac{V+}{2} \text{ as shown} \right)$$

$$V_{OUT} = \frac{1}{2} V_{CC}$$

GROUND REFERENCING A DIFFERENTIAL INPUT SIGNAL

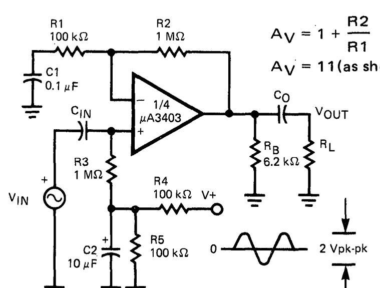


VOLTAGE CONTROLLED OSCILLATOR



*Wide Control Voltage Range:
$0V_{DC} \leq V_C \leq 2(V+ - 1.5\ V_{DC})$

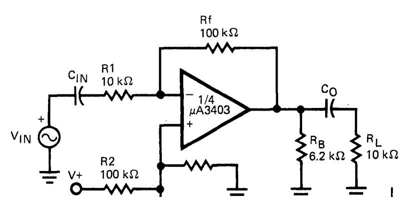
AC COUPLED NON-INVERTING AMPLIFIER



$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11(as shown)

AC COUPLED INVERTING AMPLIFIER



$$A_V = \frac{Rf}{R1}$$

A_V = 10 (as shown)

μA4136

QUAD OPERATIONAL AMPLIFIERS

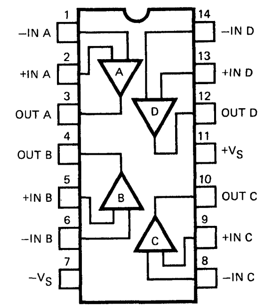
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA4136 monolithic Quad Operational Amplifiers consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the μA4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar* Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE	6A	9A
PACKAGE CODE	D	P



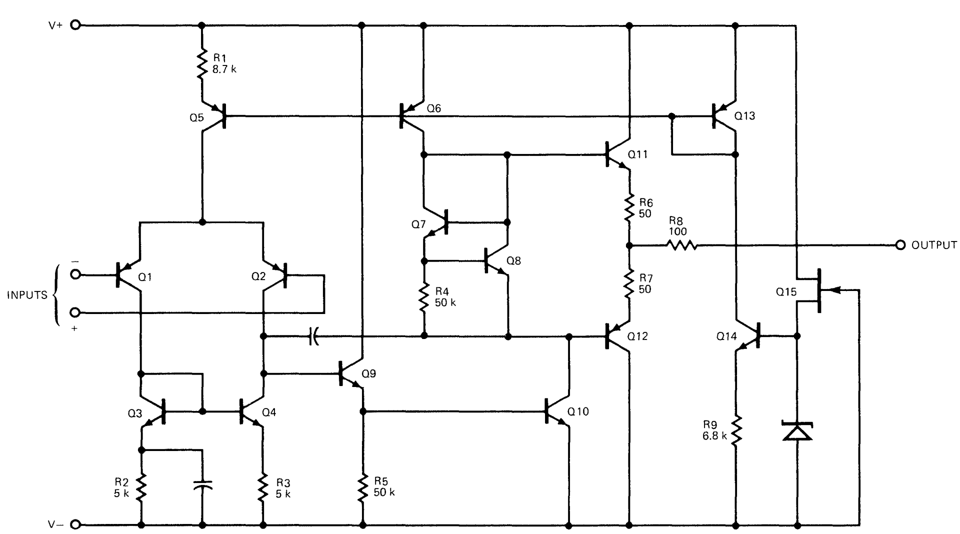
ORDER INFORMATION

TYPE	PART NO.
μA4136	μA4136DM
μA4136C	μA4136DC
μA4136C	μA4136PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA4136	±22 V
μA4136C	±18 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4136	–55°C to +125°C
μA4136C	0°C to +70°C
Storage Temperature Range	
Molded Package	–55°C to +125°C
Hermetic Package	–65°C to +150°C
Pin Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C

1/4 OF EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_S = ±15V$ unless otherwise specified

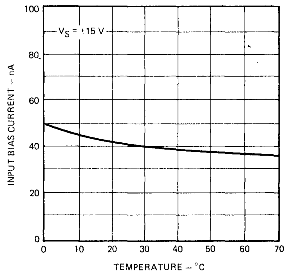
CHARACTERISTICS	CONDITIONS	μA4136 MIN	μA4136 TYP	μA4136 MAX	μA4136C MIN	μA4136C TYP	μA4136C MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = ± 10$ V	50,000	300,000		20,000	300,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			210	340		210	340	mW
Transient Response (Unity Gain) Risetime	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/μs
Channel Separation (Open Loop)	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
(Gain = 100)	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for μA4136; 0°C ≤ T_A ≤ +70°C for μA4136C.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = ± 10$ V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ, $V_S = ± 15$ V	±12			±10			V
Power Consumption	T_A = High		180	300		180	300	mW
	T_A = Low		240	400		240	400	

NOTES:

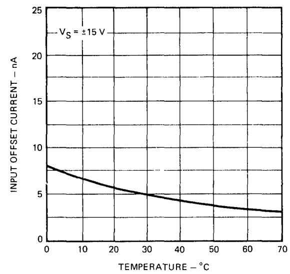
1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above $T_A = 70°C$, derate linearly at 8.3 mW/°C.
3. Short-circuit may be to ground, one amplifier only. $I_{SC} = 45$ mA (Typical).

TYPICAL PERFORMANCE CURVES

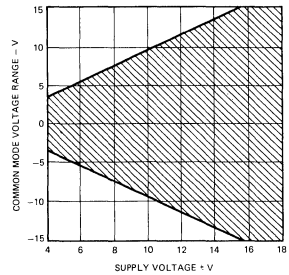
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



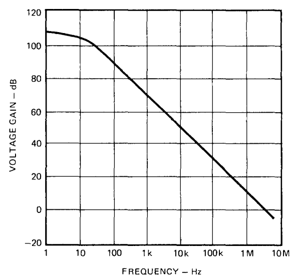
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



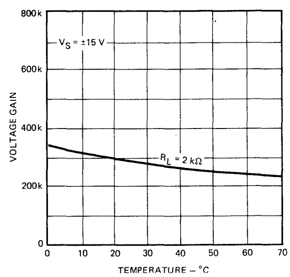
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



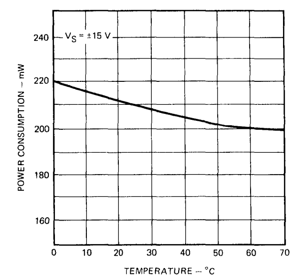
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



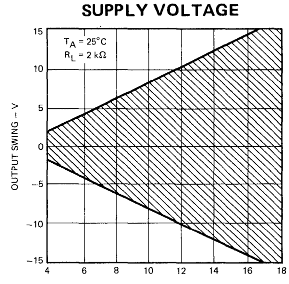
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



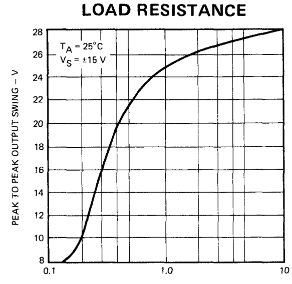
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



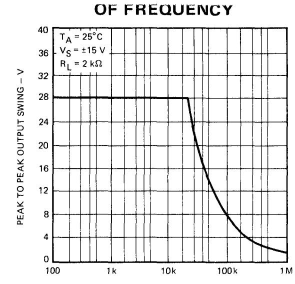
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



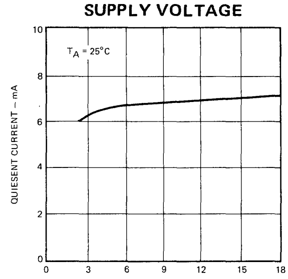
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



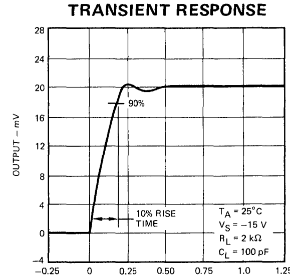
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



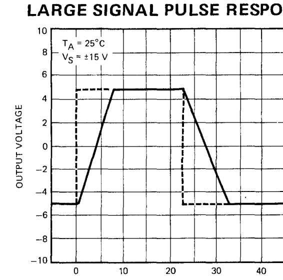
QUIESENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TRANSIENT RESPONSE

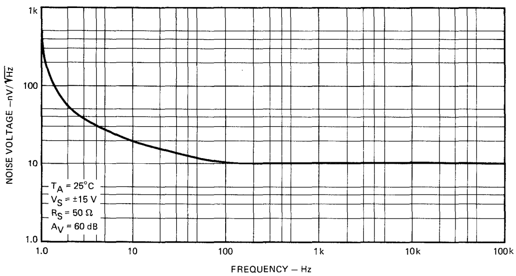


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

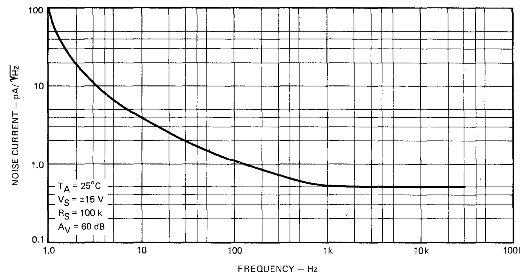


TYPICAL PERFORMANCE CURVES (Cont'd)

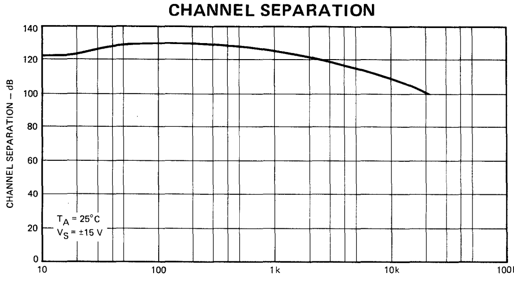
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



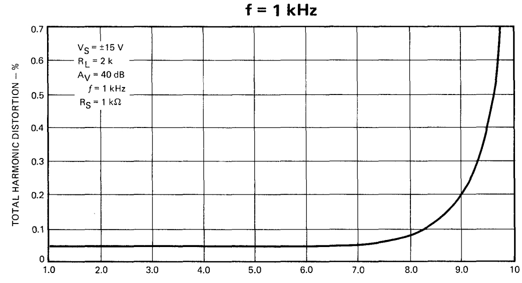
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



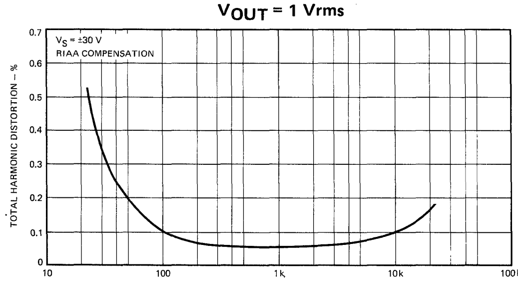
CHANNEL SEPARATION



TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT VOLTAGE f = 1 kHz

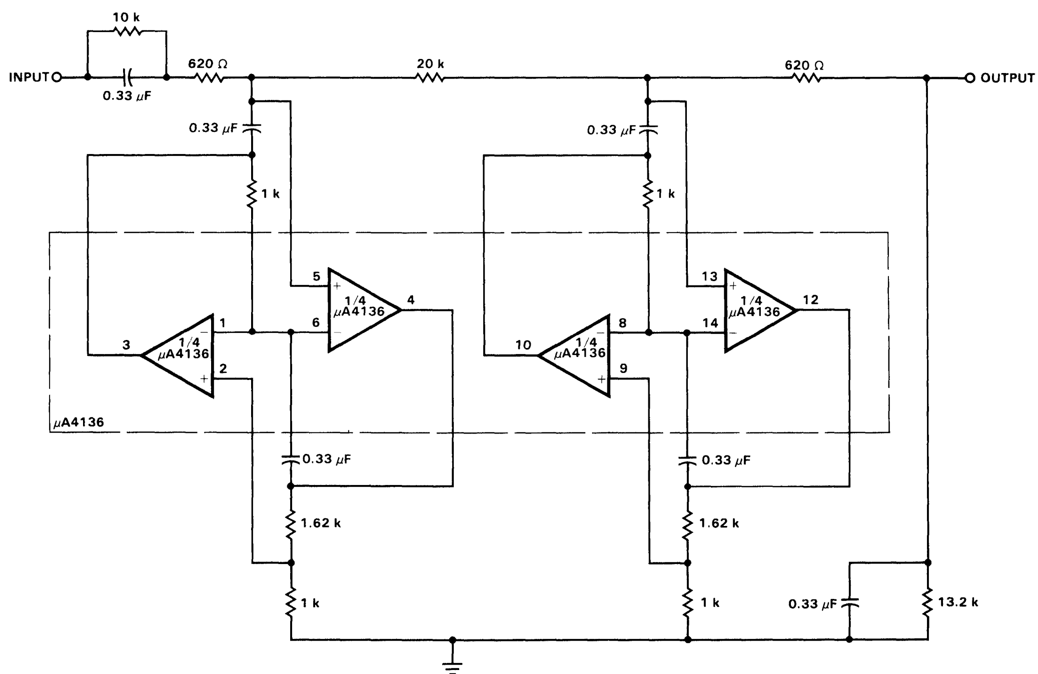


DISTORTION AS A FUNCTION OF FREQUENCY V_{OUT} = 1 Vrms

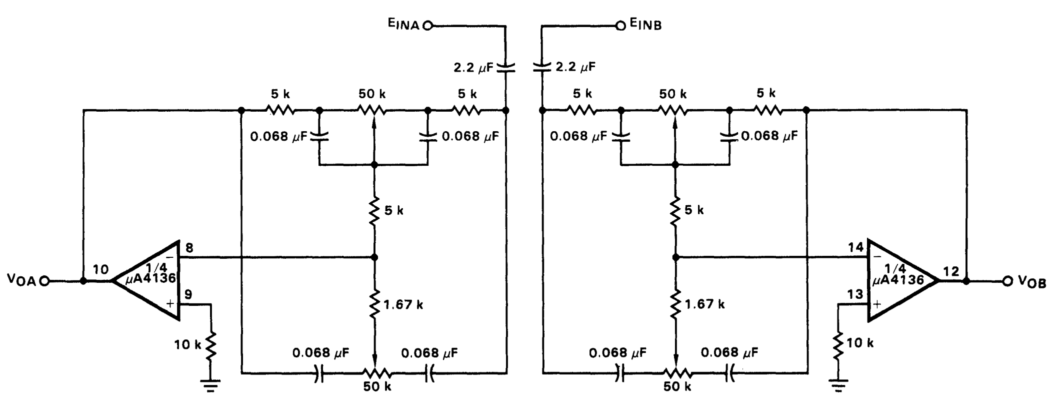


TYPICAL APPLICATIONS

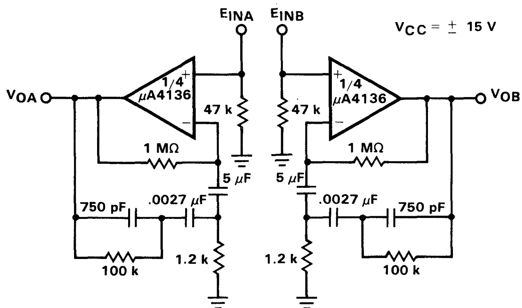
400 Hz LOWPASS BUTTERWORTH ACTIVE FILTER



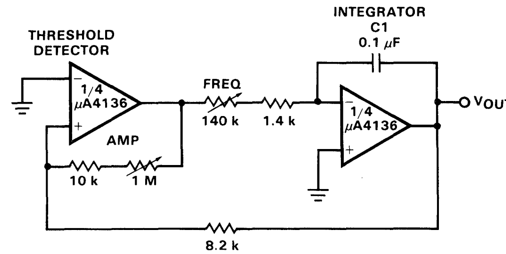
STEREO TONE CONTROL



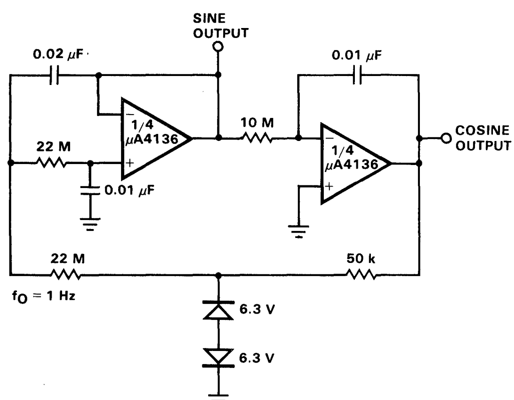
RIAA PREAMPLIFIER



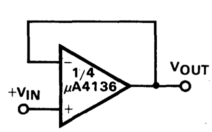
TRIANGULAR-WAVE GENERATOR



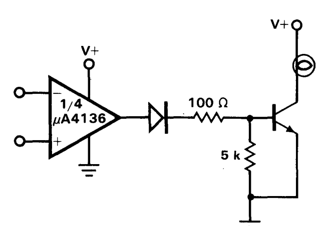
LOW FREQUENCY SINE WAVE GENERATOR WITH QUADRATURE OUTPUT



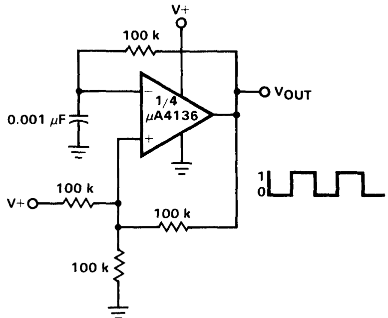
VOLTAGE FOLLOWER



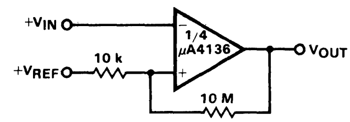
LAMP DRIVER



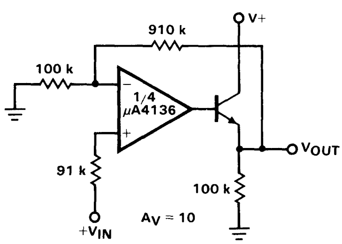
SQUAREWAVE OSCILLATOR



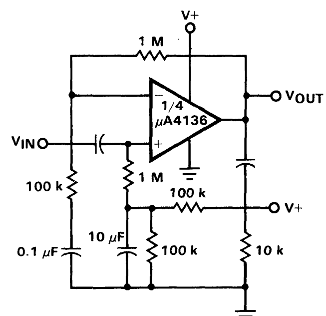
COMPARATOR WITH HYSTERESIS



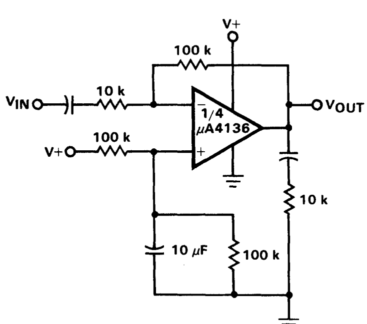
POWER AMPLIFIER



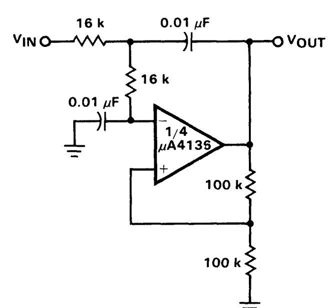
AC COUPLED NON-INVERTING AMPLIFIER



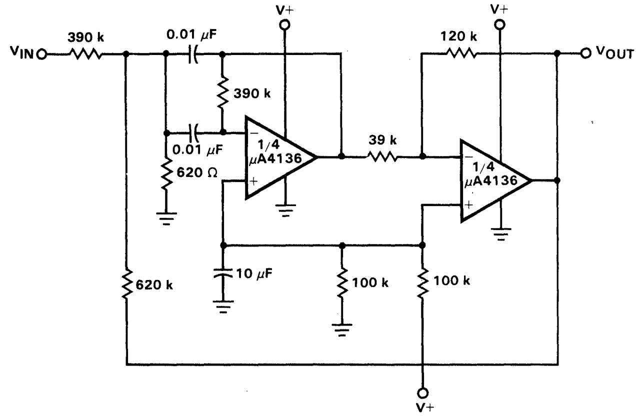
AC COUPLED INVERTING AMPLIFIER



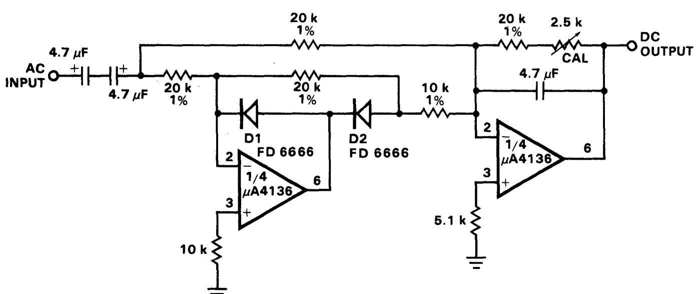
DC COUPLED 1 kHz LOW-PASS ACTIVE FILTER



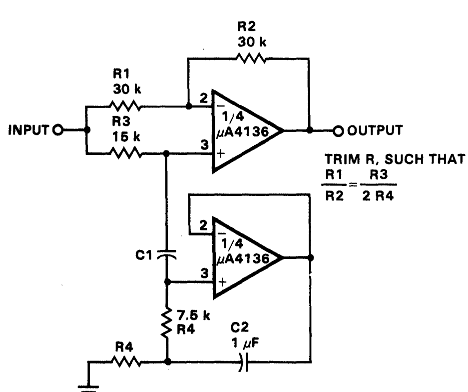
1 kHz BANDPASS ACTIVE FILTER



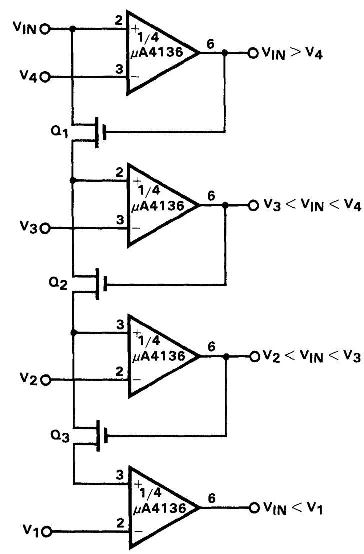
FULL-WAVE RECTIFIER AND AVERAGING FILTER



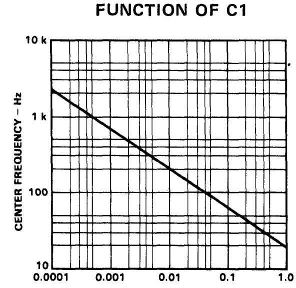
NOTCH FILTER USING THE μA4136 AS A GYRATOR



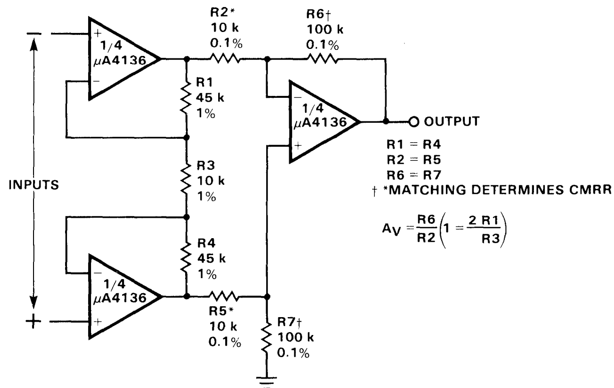
MULTIPLE APERTURE WINDOW DISCRIMINATOR



NOTCH FREQUENCY AS A FUNCTION OF C1

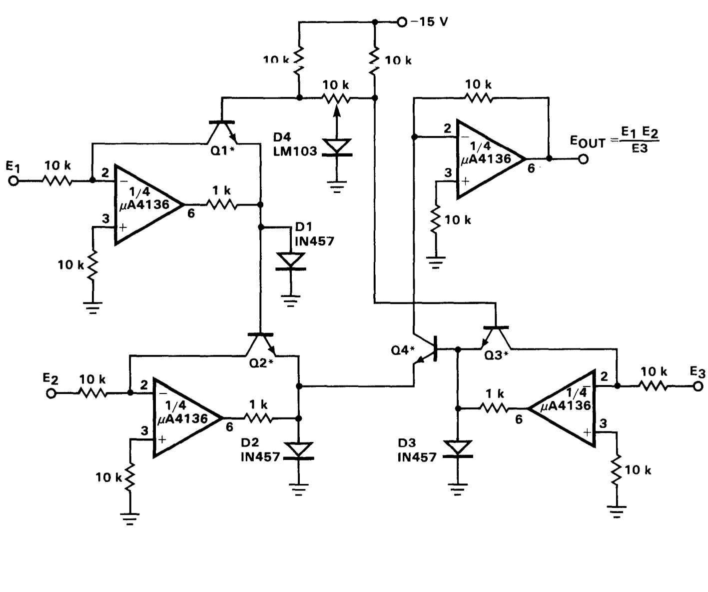


DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$$A_V = \frac{R6}{R2}\left(1 = \frac{2\,R1}{R3}\right)$$

ANALOG MULTIPLIER/DIVIDER



μA4558

DUAL OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

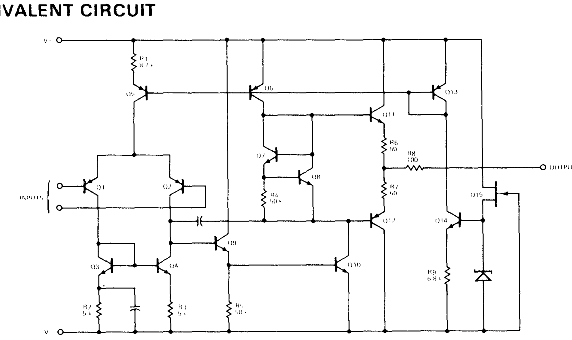
GENERAL DESCRIPTION – The μA4558 Monolithic Dual Operational Amplifiers consist of two independent high gain, internally frequency compensated operational amplifiers. The specially designed low noise input transistors allow the μA4558 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar* Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

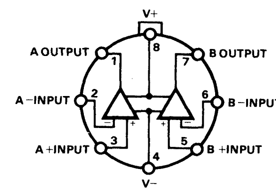
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA4558C	±18 V
μA4558	±22 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Metal Can	500 mW
Mini DIP	310 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4558	−55°C to +125°C
μA4558C	0°C to +70°C
Storage Temperature Range	
Molded Package	−55°C to +125°C
Hermetic Package	−65°C to +150°C
Pin Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C

1/2 OF EQUIVALENT CIRCUIT



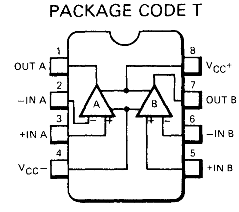
CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

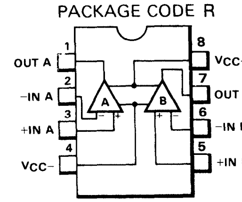
TYPE	PART NO.
μA4558C	μA4558HC
μA4558	μA4558HM

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



TYPE	PART NO.
μA4558C	μA4558TC

8-PIN MINI CER DIP
(TOP VIEW)
PACKAGE OUTLINE 6T
PACKAGE CODE R



TYPE	PART NO.
μA4558C	μA4558RC
μA4558	μA4558RM

*Planar is a patented Fairchild process.

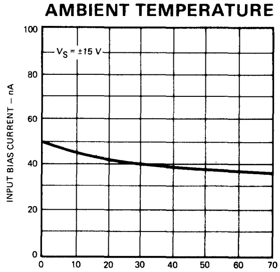
ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_S = ±15$ V unless otherwise specified

CHARACTERISTICS	CONDITIONS	μA4558			μA4558C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		30	200	nA
Input Bias Current			200	500		200	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = ±10$ V	50,000	200,000		20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			100	170		100	170	mW
Transient Response (unity Gain) Risetime	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/μs
Channel Separation (Open Loop)	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for μA4558; $0°C \leq T_A \leq +70°C$ for μA4558C.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = ±10$ V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ, $V_S = ±15$ V	±12			±10			V
Power Consumption	T_A = High		90	150		90	150	mW
	T_A = Low		120	200		120	200	

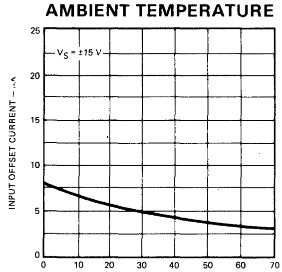
NOTES:
1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above $T_A = 70°C$, derate linearly at 6.3°C/W for the hermetic package (5S) and 5.6°C/W for the molded package (9T).
3. Short circuit may be to ground, one amplifier only. $I_{SC} = 45$ mA (Typical).

TYPICAL PERFORMANCE CURVES

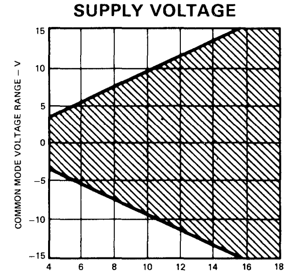
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

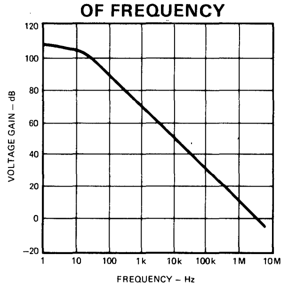


COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

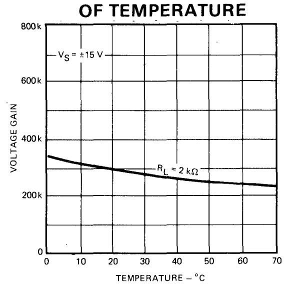


TYPICAL PERFORMANCE CURVES (Cont'd)

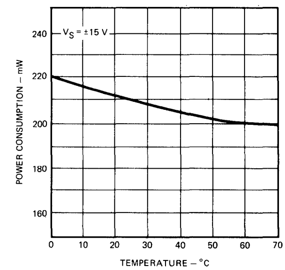
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



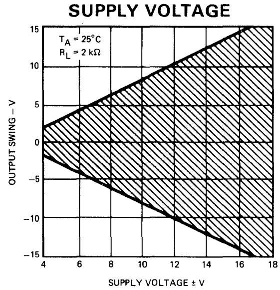
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



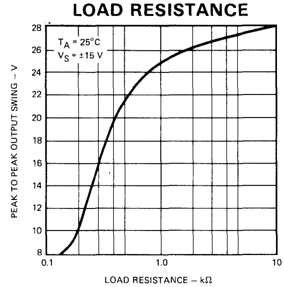
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



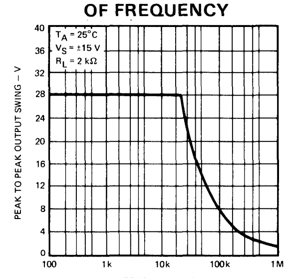
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



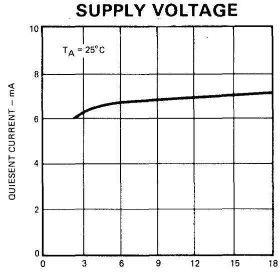
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



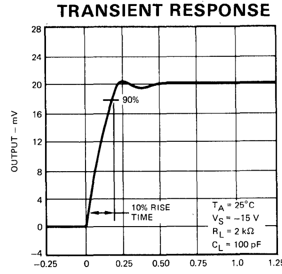
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



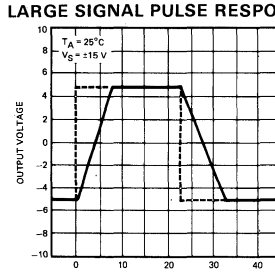
QUIESENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



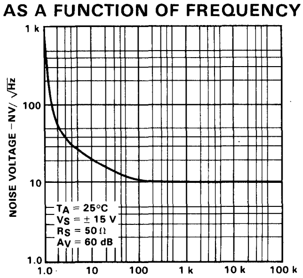
TRANSIENT RESPONSE



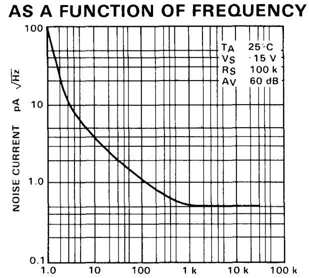
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



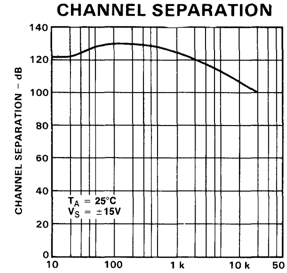
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

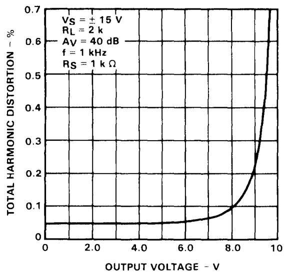


CHANNEL SEPARATION

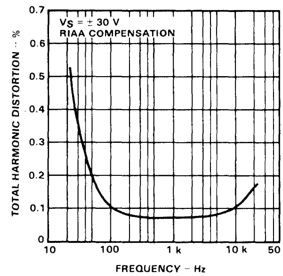


TYPICAL PERFORMANCE CURVES (Cont'd)

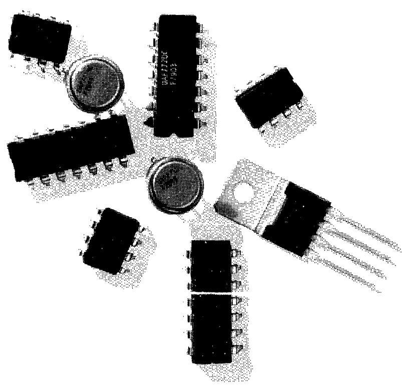
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT VOLTAGE f = 1 kHz



DISTORTION AS A FUNCTION OF FREQUENCY V_{OUT} = 1 Vrms



5



COMPARATORS

μAF111 • μAF311

FET INPUT VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

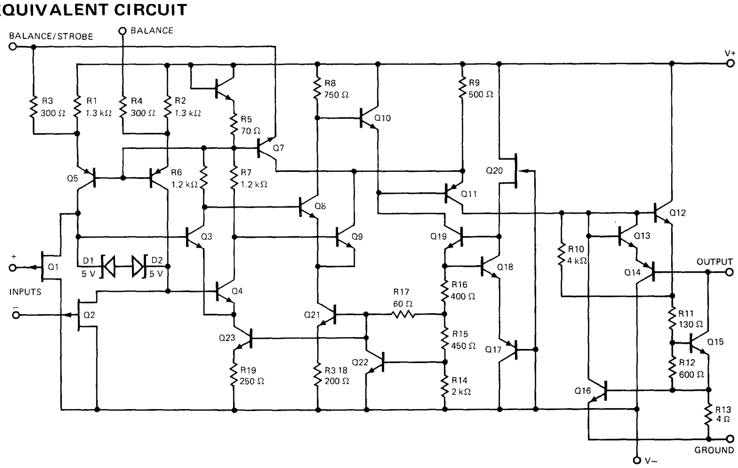
GENERAL DESCRIPTION — The μAF111 and μAF311 are monolithic, FET input Voltage Comparators, constructed using the Fairchild Planar* epitaxial process. The μAF111 series operates from the single 5 V integraetd circuit logic supply to the standard ±15 V operational amplifier supplies. The μAF111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **EXTREMELY LOW INPUT BIAS CURRENT** . . . 50 pA MAX (μAF111), 150 pA MAX (μAF311)
- **EXTREMELY LOW INPUT OFFSET CURRENT** . . . 25 pA MAX (μAF111), 75 pA MAX (μAF311)
- **DIFFERENTIAL INPUT VOLTAGE** . . . ±30 V
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

ABSOLUTE MAXIMUM RATINGS

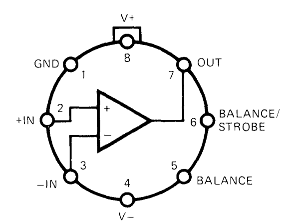
Voltage Between V+ and V− Terminals	36 V
Output to V− (μAF111)	50 V
(μAF311)	40 V
Ground to V−	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
DIP	670 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can)	
Metal Can	−65°C to +150°C
Hermetic DIP	−55°C to +125°C
Operating Temperature Range	
Military (μAF111)	−55°C to +125°C
Commercial (μAF311)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5S
PACKAGE CODE H



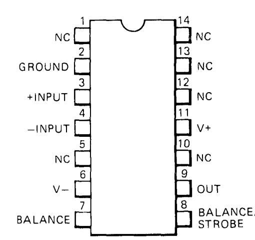
ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111HM
μAF311	μAF311HC

NOTE: Pin 4 connected to case.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111DM
μAF311	μAF311DC

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μAF111

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = −55°C to +125°C unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, R_S ⩽ 50 kΩ		0.7	4.0	mV
Input Offset Current (Note 4)	T_A = 25°C, V_{CM} = 0 (Note 6)		5.0	25	pA
Input Bias Current	T_A = 25°C, V_{CM} = 0 (Note 6)		20	50	pA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	V_{IN} ⩽ −5 mV, I_{OUT} = 50 mA T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	V_{IN} ⩾ 5 mV, V_{OUT} = 35 V T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)	R_S ⩽ 50 kΩ			6.0	mV
Input Offset Current (Note 4)	V_S = ±15 V, V_{CM} = 0 (Note 6)		2.0	3.0	nA
Input Bias Current	V_S = ±15 V, V_{CM} = 0 (Note 6)		5.0	7.0	nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	V^+ ⩾ 4.5 V, V^- = 0 V_{IN} ⩽ −6 mV, I_{SINK} ⩽ 8 mA		0.23	0.4	V
Output Leakage Current	V_{IN} ⩾ 5 mV, V_{OUT} = 35 V		0.1	0.5	μA
Positive Supply Current	T_A = 25°C		5.1	6.0	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

μAF311

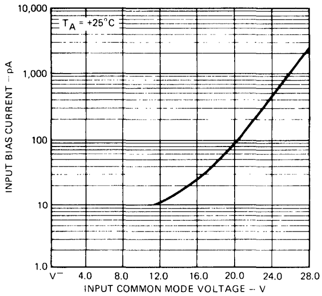
ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 0°C to +70°C unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, R_S ⩽ 50 kΩ		2.0	10	mV
Input Offset Current (Note 4)	T_A = 25°C, V_{CM} = 0 (Note 6)		5.0	75	pA
Input Bias Current	T_A = 25°C, V_{CM} = 0 (Note 6)		25	150	pA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	V_{IN} ⩽ −10 mV, I_{OUT} = 50 mA T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	V_{IN} ⩾ 10 mV, V_{OUT} = 35 V T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)	R_S ⩽ 50 kΩ			15	mV
Input Offset Current (Note 4)	V_S = ±15V, V_{CM} = 0 (Note 6)		1.0		nA
Input Bias Current	V_S = ±15 V, V_{CM} = 0 (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	V^+ ⩾ 4.5 V, V^- = 0 V_{IN} ⩽ −10 mV, I_{SINK} ⩽ 8 mA		0.23	0.4	V
Positive Supply Current	T_A = 25°C		5.1	7.5	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

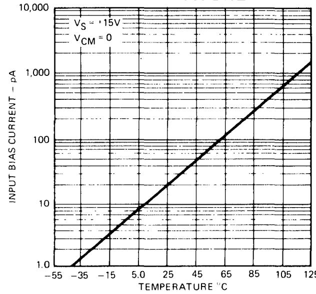
NOTES:
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. ,The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
6. For input voltages greater than 15 V above the negative supply the bias and offset currents will increase — see typical performance curves.

TYPICAL PERFORMANCE CURVES

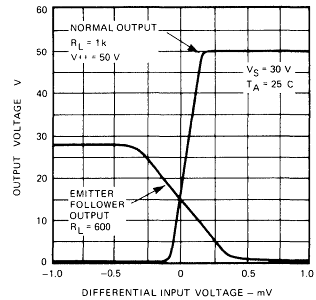
INPUT BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



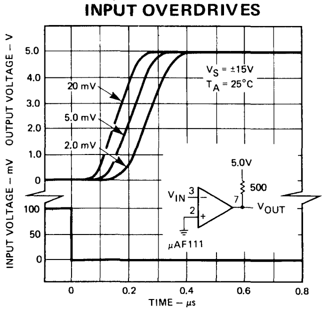
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



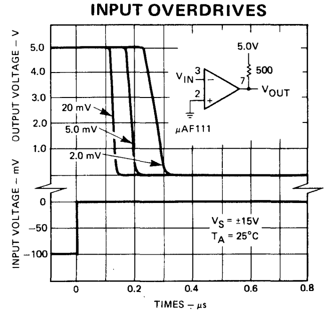
TRANSFER FUNCTION



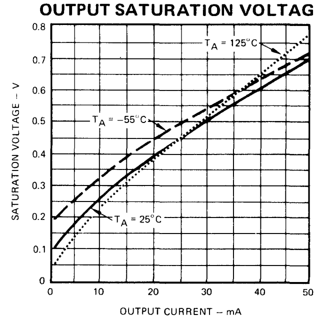
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



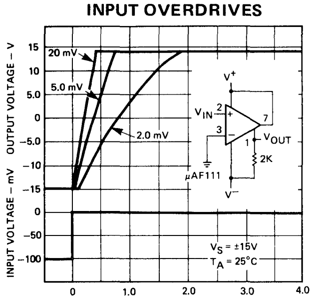
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



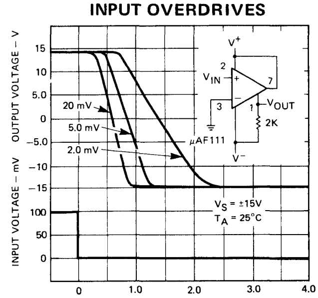
OUTPUT SATURATION VOLTAGE



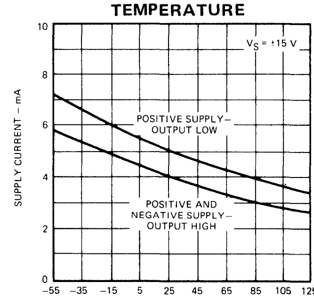
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



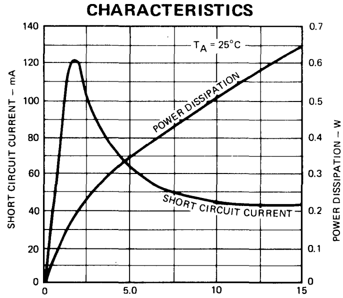
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



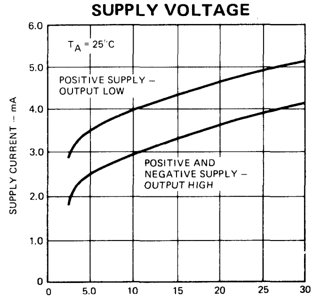
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



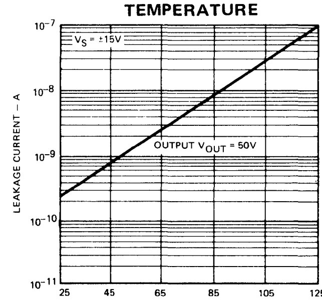
OUTPUT LIMITING CHARACTERISTICS



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



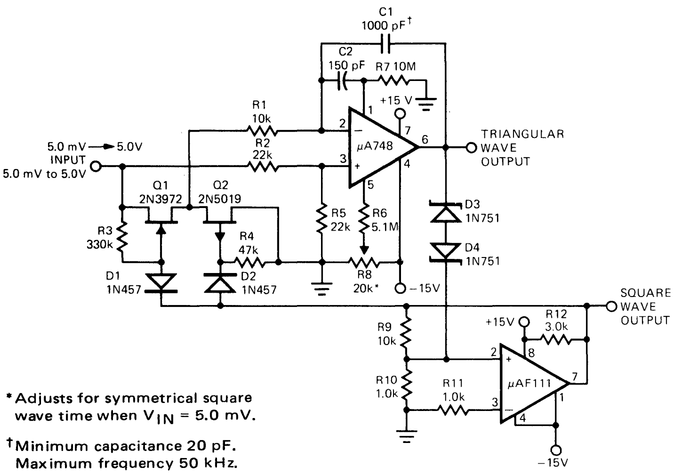
OUTPUT LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE



6

TYPICAL APPLICATIONS

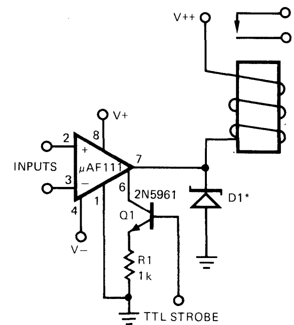
10 Hz TO 10 kHz VOLTAGE CONTROLLED OSCILLATOR



*Adjusts for symmetrical square wave time when V_{IN} = 5.0 mV.

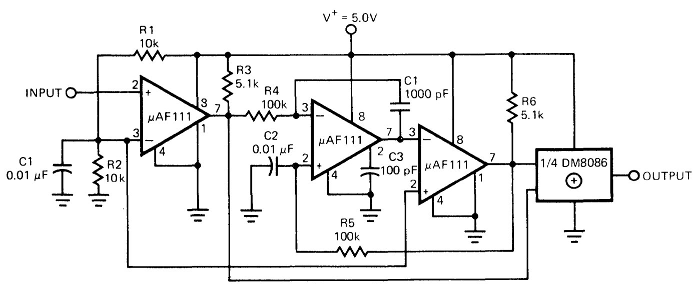
†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

RELAY DRIVER WITH STROBE



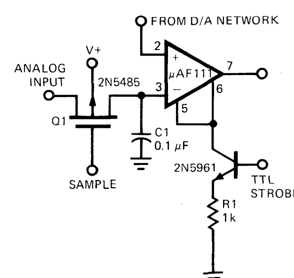
*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

FREQUENCY DOUBLER



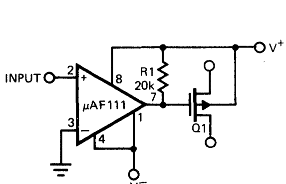
Frequency range:
Input — 5.0 kHz to 50 kHz
Output — 10 kHz to 100 kHz

STROBING OFF BOTH INPUT* AND OUTPUT STAGES

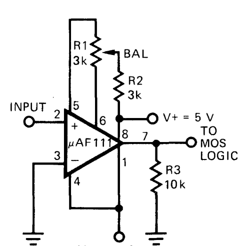


*Typical input current is 50 pA with inputs strobed off.

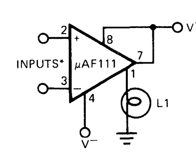
ZERO CROSSING DETECTOR DRIVING MOS SWITCH



ZERO CROSSING DETECTOR DRIVING MOS LOGIC



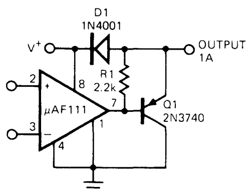
DRIVING GROUND-REFERRED LOAD



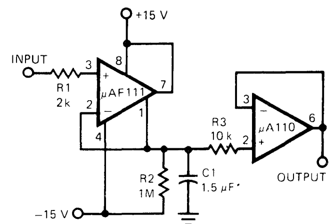
*Input polarity is reversed when using pin 1 as output.

TYPICAL APPLICATIONS (Cont'd)

COMPARATOR AND SOLENOID DRIVER

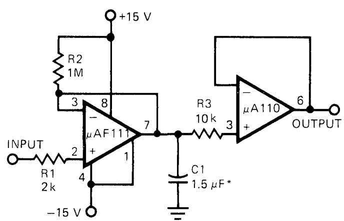


POSITIVE PEAK DETECTOR



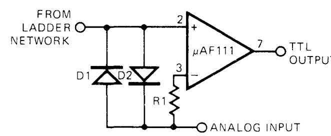
*Solid tantalum

NEGATIVE PEAK DETECTOR

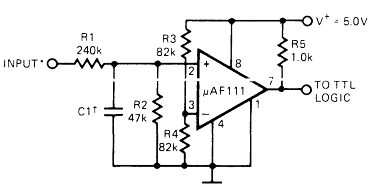


*Solid tantalum

USING CLAMP DIODES TO IMPROVE RESPONSE



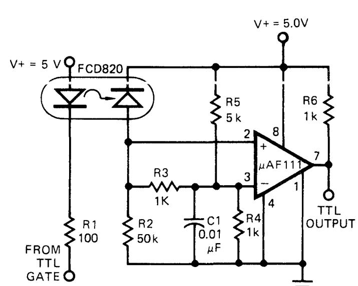
TTL INTERFACE WITH HIGH LEVEL LOGIC



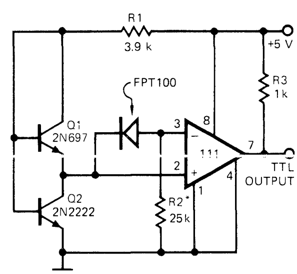
*Values shown are for a 0 to 30 V logic swing and a 15 V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

DIGITAL TRANSMISSION ISOLATOR



PRECISION PHOTODIODE COMPARATOR



*R2 sets the comparison level. At comparison, the photodiode has less than 5.0 mV across it, decreasing leakages by an order of magnitude.

DEFINITIONS:

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT – The change in input offset current over the operating temperature range divided by the operating temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE – The change in input offset voltage over the operating temperature range divided by the operating temperature range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage applied between the input terminals for which operation within specifications is assured.

INPUT BIAS CURRENT – The average of the two input currents with no signal applied.

INPUT COMMON MODE VOLTAGE RANGE – The range of common mode input voltage over the device will operate within specifications.

INPUT OFFSET CURRENT – The difference between the two input currents with the output at the logic threshold voltage.

INPUT OFFSET VOLTAGE – The voltage which must be applied to the input terminals to give the logic threshold voltage at the output.

INPUT VOLTAGE RANGE – The range of voltage on either input terminal over which the device will operate as specified.

NEGATIVE OUTPUT VOLTAGE LEVEL – The dc output voltage in the negative direction with the input voltage equal to, or greater than, a minimum specified value.

RESPONSE TIME – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level.

STROBE CURRENT – The maximum current taken by the strobe terminal during activation.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the dc output in the vicinity of the logic threshold.

μA111 • μA311

VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

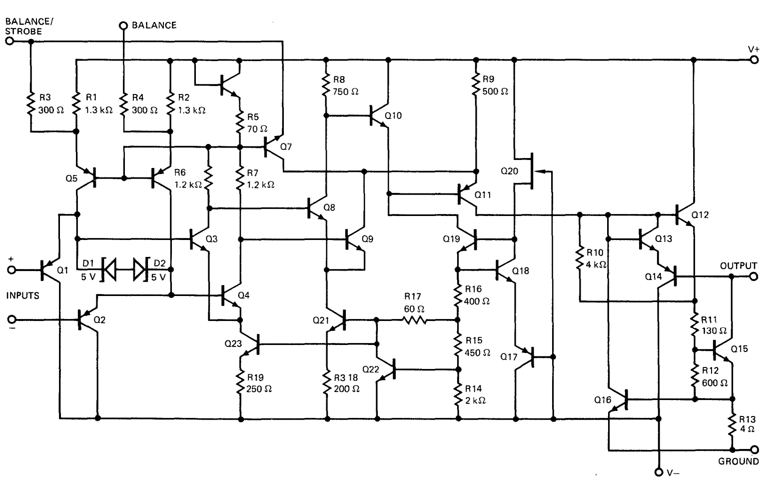
GENERAL DESCRIPTION – the μA111 and μA311 are monolithic, low input current Voltage Comparators, each constructed using the Fairchild Planar* epitaxial process. The μA111 series operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA111 series is intended for a wide range of applicatons including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- LOW INPUT BIAS CURRENT – 150 nA MAX (111), 250 nA MAX (311)
- LOW INPUT OFFSET CURRENT – 20 nA MAX (111), 50 nA MAX (311)
- DIFFERENTIAL INPUT VOLTAGE – ±30 V
- POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY

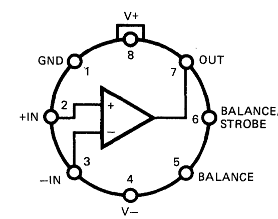
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	36 V
Output to V– (μA111)	50 V
(μA311)	40 V
Ground to V–	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can and Hermetic Mini DIP)	–65°C to +150°C
(Molded Mini DIP)	–55°C to +125°C
Operating Temperature Range	
Military (μA111)	–55°C to +125°C
Commercial (μA311)	0°C to +70°C

EQUIVALENT CIRCUIT



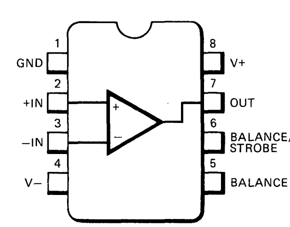
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111HM
μA311	μA311HC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111RM
μA311	μA311RC
μA311	μA311TC

*Planar is a patented Fairchild process

μA111

ELECTRICAL CHARACTERISTICS: $V_S = \pm15$ V, $T_A = -55°C$ to $+125°C$ unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leqslant 50$ kΩ		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leqslant -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geqslant 5$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leqslant 50$ kΩ			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geqslant 4.5$ V, $V^- = 0$ $V_{IN} \leqslant -6$ mV, $I_{SINK} \leqslant 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geqslant 5$ mV, $V_{OUT} = 35$ V		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

6

μA311

ELECTRICAL CHARACTERISTICS: $V_S = \pm15$ V, $T_A = 0°C$ to $+70°C$ unless otherwise specified, Note 3.

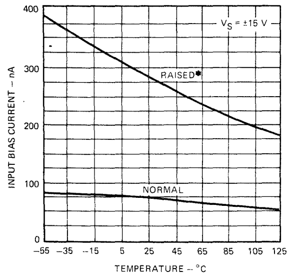
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leqslant 50$ kΩ		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leqslant -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geqslant 10$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leqslant 50$ kΩ			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geqslant 4.5$ V, $V^- = 0$ $V_{IN} \leqslant -10$ mV, $I_{SINK} \leqslant 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

NOTES:

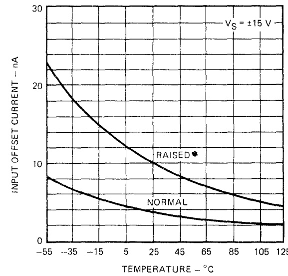
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for mini DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA111

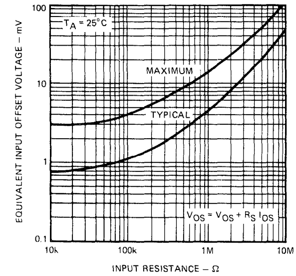
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

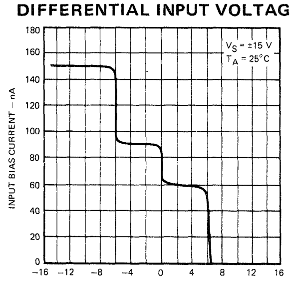


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

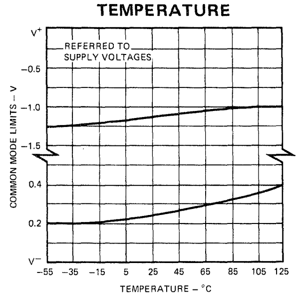


*Pins 5,6 and 8 are shorted.

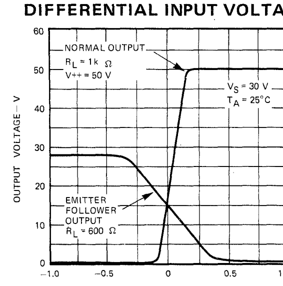
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



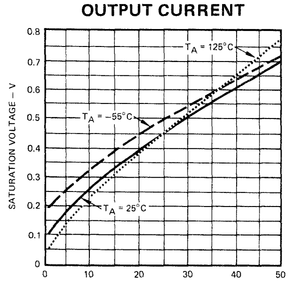
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



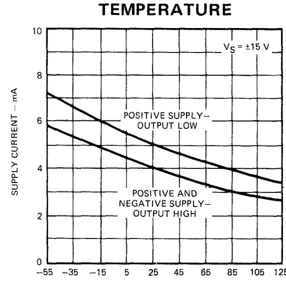
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



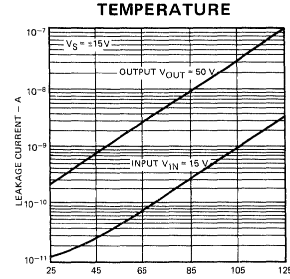
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

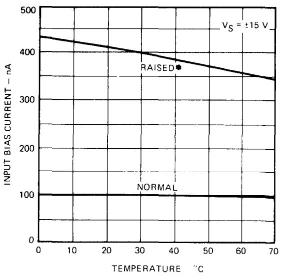


LEAKAGE CURRENTS AS A FUNCTION OF TEMPERATURE

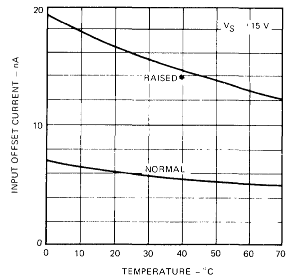


TYPICAL PERFORMANCE CURVES FOR μA311

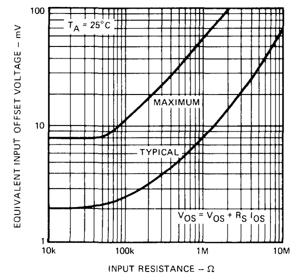
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

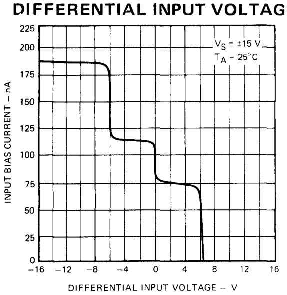


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

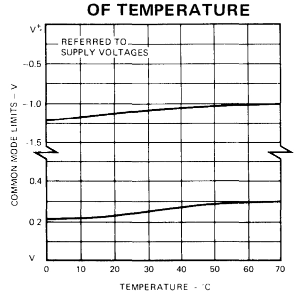


*Pins 5, 6 and 8 are shorted.

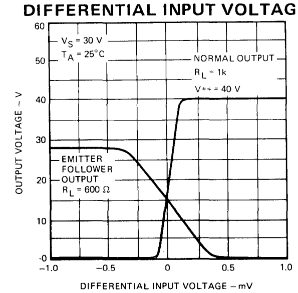
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



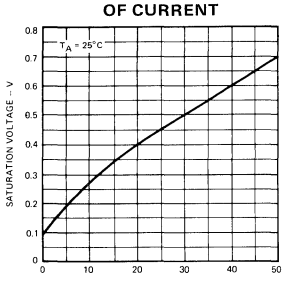
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



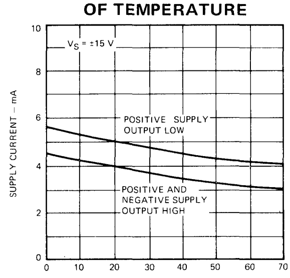
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



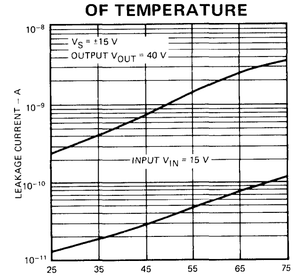
SATURATION VOLTAGE AS A FUNCTION OF CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

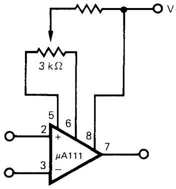


LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE



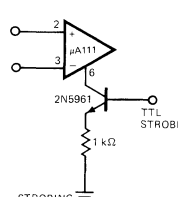
TYPICAL APPLICATIONS

OFFSET NULL CIRCUIT

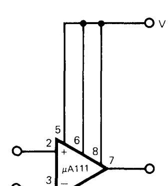


OFFSET BALANCING

STROBE CIRCUIT



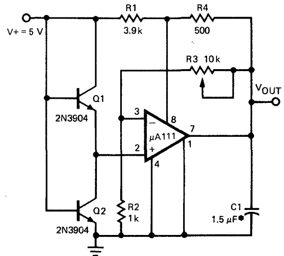
INCREASING INPUT STAGE CURRENT*



*Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs.

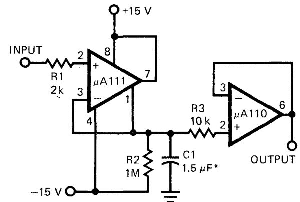
TYPICAL APPLICATIONS (Cont'd)

ADJUSTABLE LOW VOLTAGE REFERENCE SUPPLY



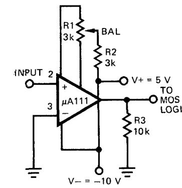
*Solid tantalum

POSITIVE PEAK DETECTOR

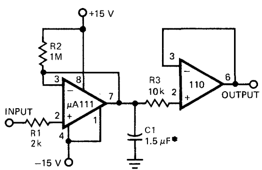


*Solid tantalum

ZERO CROSSING DETECTOR DRIVING MOS LOGIC

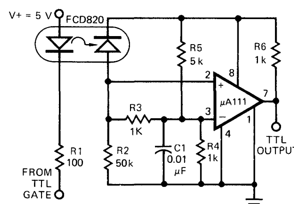


NEGATIVE PEAK DETECTOR

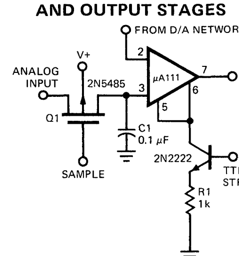


*Solid tantalum

DIGITAL TRANSMISSION ISOLATOR

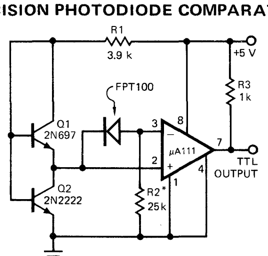


STROBING OF BOTH INPUT AND OUTPUT STAGES



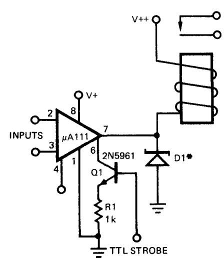
*Typical input current is 50 pA with inputs strobed off.

PRECISION PHOTODIODE COMPARATOR



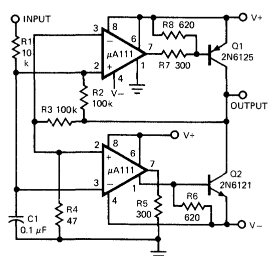
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

RELAY DRIVER WITH STROBE

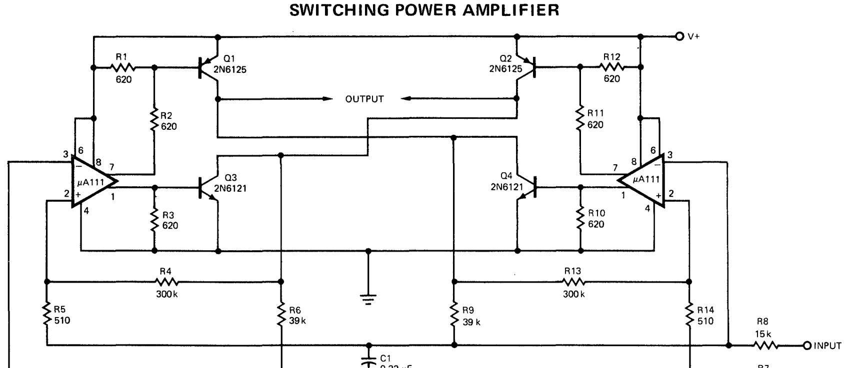


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

SWITCHING POWER AMPLIFIER



SWITCHING POWER AMPLIFIER



μA139/239/339 • μA139A/239A/339A
μA2901 • μA3302

LOW-POWER, LOW-OFFSET VOLTAGE QUAD COMPARATORS

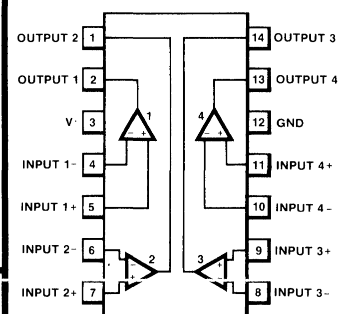
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stage allows the input common-mode voltage to include ground.

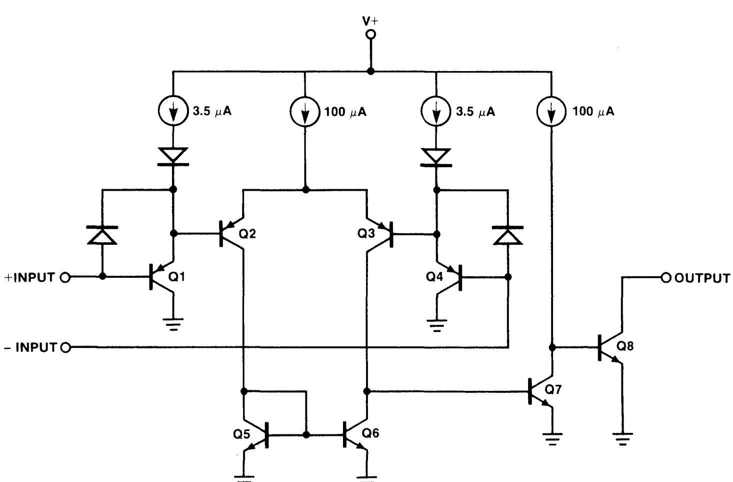
- **SINGLE SUPPLY OPERATION — +2.0 V TO +36 V**
- **DUAL SUPPLY OPERATION — ±1.0 V TO ±18 V**
- **ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN — 800 μA TYP**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**
- **LOW INPUT BIAS CURRENT — 25 nA TYP**
- **LOW INPUT OFFSET CURRENT — ±5 nA TYP**
- **LOW OFFSET VOLTAGE — ±2 mV**

CONNECTION DIAGRAM
14-PIN DIP

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



SCHEMATIC DIAGRAM



ORDER INFORMATION

TYPE	PART NO.
μA139A	μA139ADM
μA139	μA139DM
μA239A	μA239ADC
μA239A	μA239APC
μA239	μA239DC
μA239	μA239PC
μA339A	μA339ADC
μA339A	μA339APC
μA339	μA339DC
μA339	μA339PC
μA2901	μA2901DC
μA2901	μA2901PC
μA3302	μA3302DC
μA3302	μA3302PC

ELECTRICAL CHARACTERISTICS (V^+ = 5 V, Note 4)

CHARACTERISTICS	CONDITIONS	µA139A			µA239A, µA339A			µA139			µA239, µA339			µA2901			µA3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3.0	±20	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA
Input Offset Current	$I_{IN(+)}$ - $I_{IN(-)}$, T_A = 25°C		±5.0	±25		±5.0	±50		±5.0	±25		±5.0	±50		±5.0	±50		±5.0	±100	nA
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C R_L = ∞, V^+ = 30 V, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8 1.0	1.0 2.5		0.8	2.0	mA
Voltage Gain	$R_L \geq$ 15 kΩ, V^+ = 15 V (To Support Large V_O Swing), T_A = 25°C	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{ref} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300			300			300			300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $V_O \leq$ 1.5 V, T_A = 25°C	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		2.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $I_{sink} \leq$ 4.0 mA, T_A = 25°C		250	400		250	400		250	400		250	400			400		250	500	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200			200			200			200			200	nA
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9.0	15			40	mV
Input Offset Current	$I_{IN(+)}$ - $I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA
Input Common-Mode Voltage Range		0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	V
Saturation Voltage	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $I_{sink} \leq$ 4 mA			700			700			700			700		400	700			700	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V			1.0			1.0			1.0			1.0			1.0			1.0	µA
Differential Input Voltage	Keep all V_{IN}'s $\geq$ 0 V (or V−, if used), (Note 8)			V^+			V^+			36			36	0		V^+			V_{CC}	V

ABSOLUTE MAXIMUM RATINGS

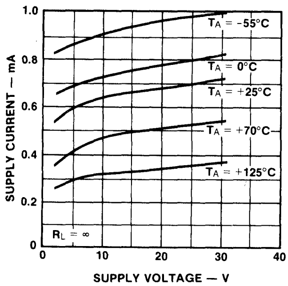
	μA139/μA239/μA339 μA139A/μA239A/μA339A μA2901	μA3302
Supply Voltage, V^+	36 V or ±18 V	28 V or ±14 V
Differential Input Voltage	36 V	28 V
Input Voltage Range	-0.3 V to +36 V	-0.3 V to +28 V
Power Dissipation (Note 1)		
9A, 6A	1 W	1 W
Output Short-Circuit to Gnd, (Note 2)	Continuous	Continuous
Input Current (V_{IN} < -0.3 V), (Note 3)	50 mA	50 mA
Operating Temperature Range		
μA339, μA339A	0° C to +70° C	
μA239, μA239A	-25° C to +85° C	
μA139, μA139A	-55° C to +125° C	
μA2901, μA3302	-40° C to +85° C	
Storage Temperature Range	-65° C to +150° C	-65° C to +150° C
Pin Temperature (Soldering, 10 s)	300° C	300° C

6

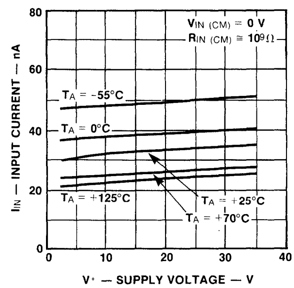
NOTES:
1. For operating at high temperatures, the μA339/μA339A, μA2901 μA3302 must be derated based on a 125° C maximum junction temperature and a thermal resistance of 125° C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The μA139 and μA139A must be derated based on a 150° C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition tiode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which negative, again returns to a value greater than -0.3 V.
4. These specifications apply for V^+ = 5.0 V and -55° C ≤ T_A ≤ +125° C, unless otherwise stated. With the μA239/μA239A, all temperature specifications are limited to -25° C ≤ T_A ≤ +85° C, the μA339/μA339A temperature specifications are limited to 0° C ≤ T_A ≤ +70° C, and the μA2901, μA3302 temperature range is -40° C ≤ T_A ≤ +85° C.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltalge range is V^+ -1.5 V, but either or both inputs can go to +30 V without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained; see typical performance characteristics section.
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
9. At output switch point, V_O ≅ 1.4 V, R_S = 0Ω with V^+ from 5 V; and over the full input common-mode range (0 V to V^+ -1.5 V).
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL PERFORMANCE CHARACTERISTICS μA139/μA239/μA339, μA139A/μA239A/μA339A, μA3302

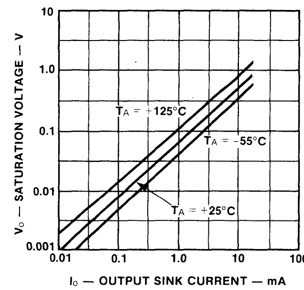
SUPPLY CURRENT



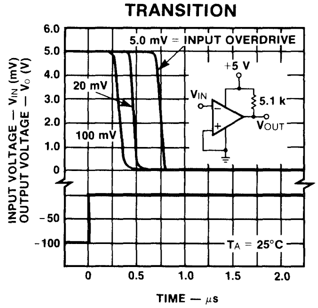
INPUT CURRENT



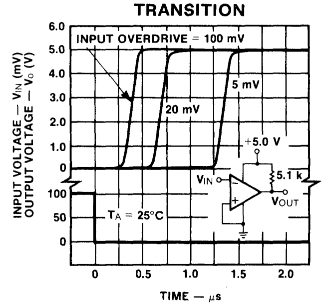
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

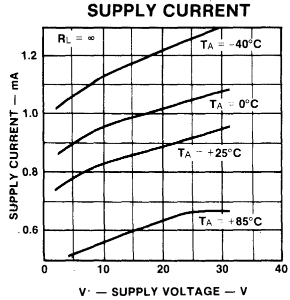


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

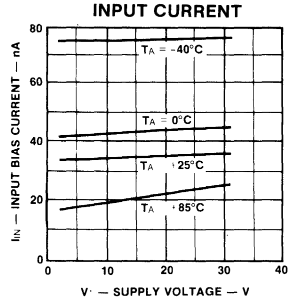


TYPICAL PERFORMANCE CHARACTERISTICS μA2901

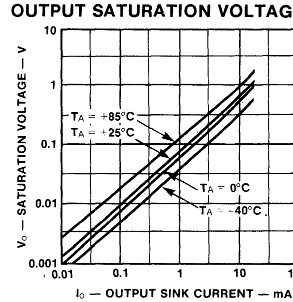
SUPPLY CURRENT



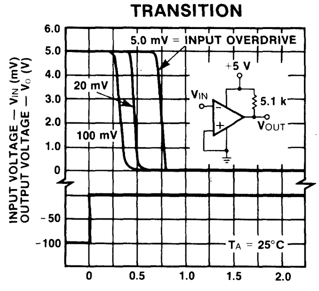
INPUT CURRENT



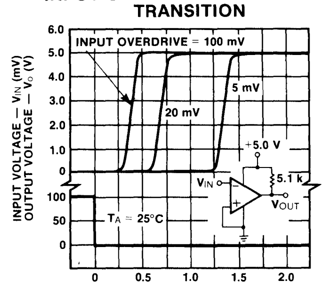
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION



APPLICATION HINTS

The μA139 series are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the μA139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V (at 25° C). An input clamp diode can be used as shown in the applications section.

The output of the μA139 series is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide an output ORing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the μA139 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

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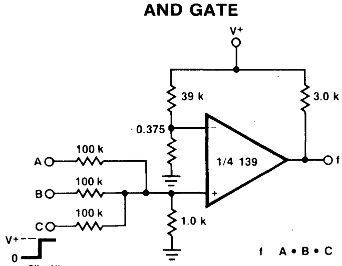
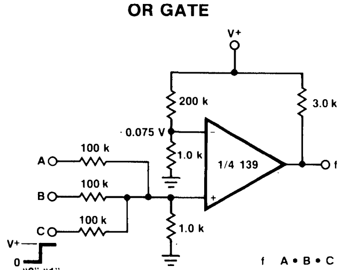
TYPICAL APPLICATIONS (V+ = 15 V)

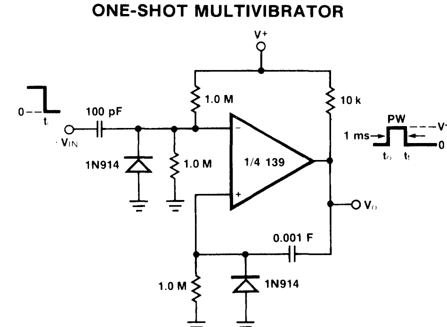
AND GATE



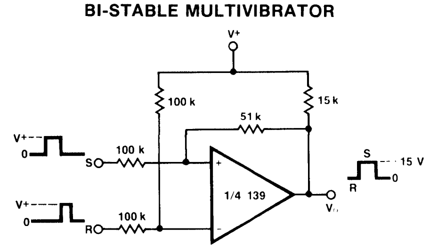
OR GATE



ONE-SHOT MULTIVIBRATOR

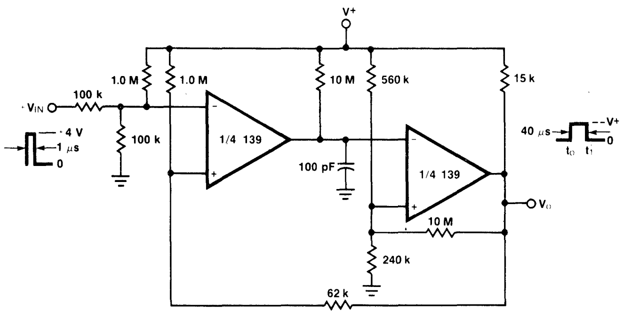


BI-STABLE MULTIVIBRATOR

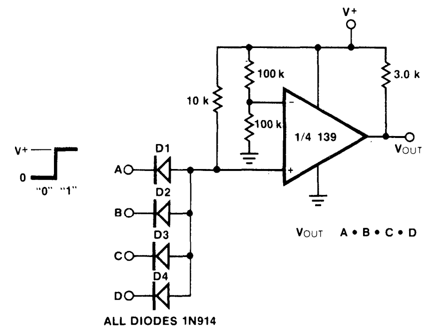


TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

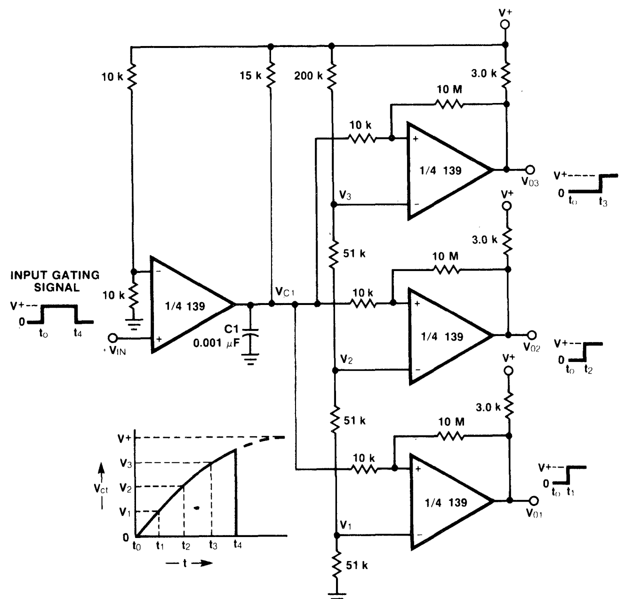
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



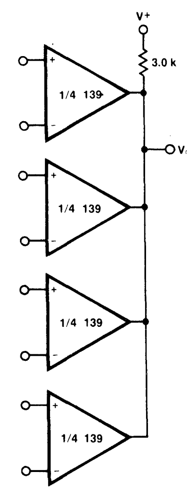
LARGE FAN-IN AND GATE



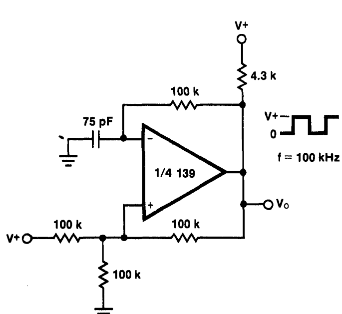
TIME DELAY GENERATOR



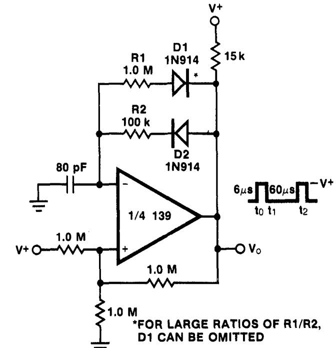
ORING THE OUTPUTS



SQUAREWAVE OSCILLATOR

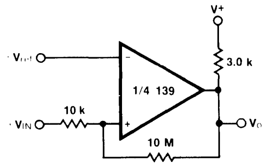


PULSE GENERATOR

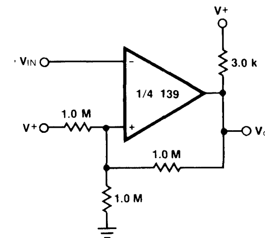


TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

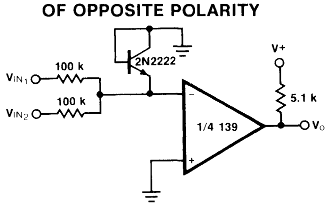
NON-INVERTING COMPARATOR WITH HYSTERESIS



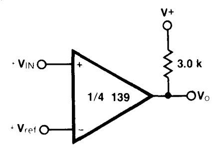
INVERTING COMPARATOR WITH HYSTERESIS



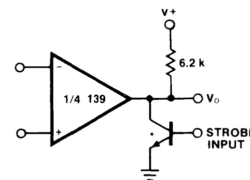
COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY



BASIC COMPARATOR

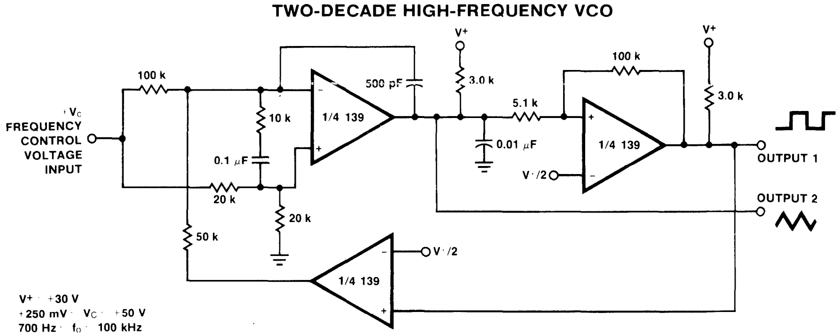


OUTPUT STROBING



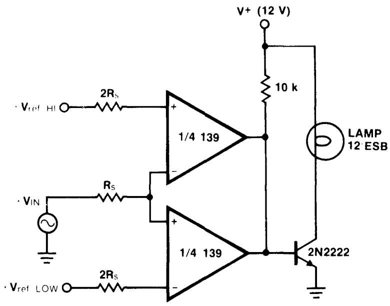
*OR LOGIC GATE WITHOUT PULL-UP RESISTOR

TWO-DECADE HIGH-FREQUENCY VCO

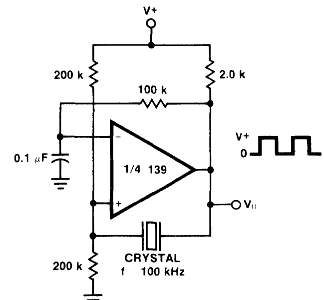


V+ = +30 V
+250 mV ≤ VC ≤ +50 V
700 Hz ≤ fo ≤ 100 kHz

LIMIT COMPARATOR

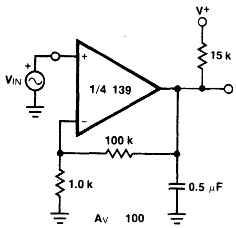


CRYSTAL CONTROLLED OSCILLATOR



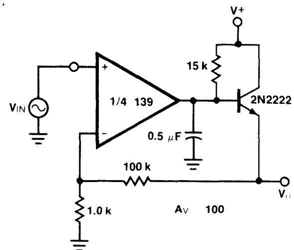
TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

LOW FREQUENCY OP AMP

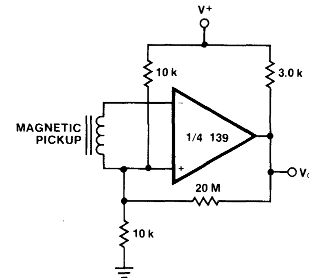


LOW FREQUENCY OP AMP (V

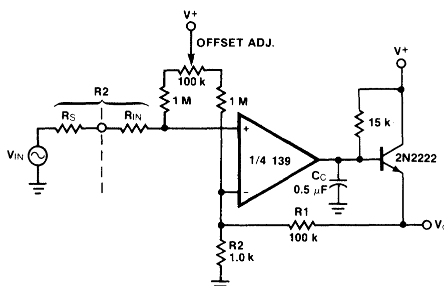
LOW FREQUENCY OP AMP (V_O = 0 V FOR V_{IN} = 0 V)



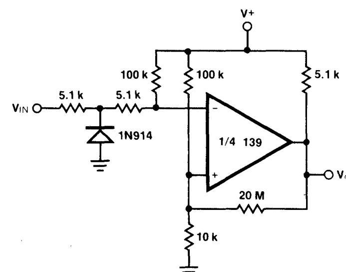
TRANSDUCER AMPLIFIER



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

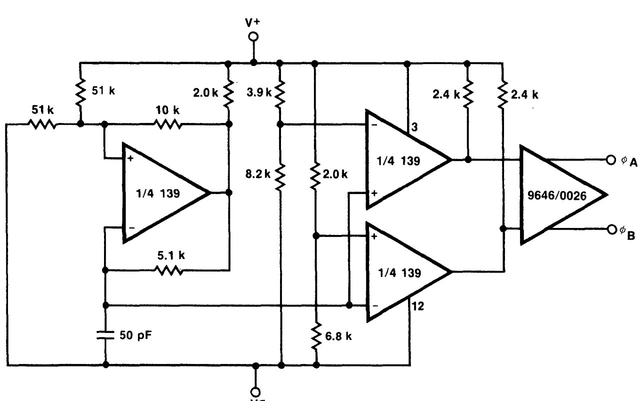


ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)

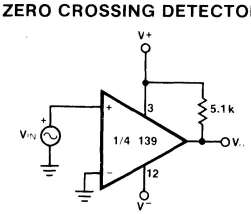


SPLIT-SUPPLY APPLICATIONS V+ = +15V and V− = -15V

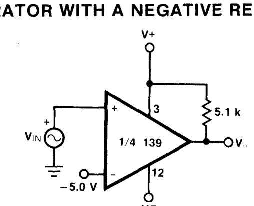
MOS CLOCK DRIVER



ZERO CROSSING DETECTOR



COMPARATOR WITH A NEGATIVE REFERENCE



μA710
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

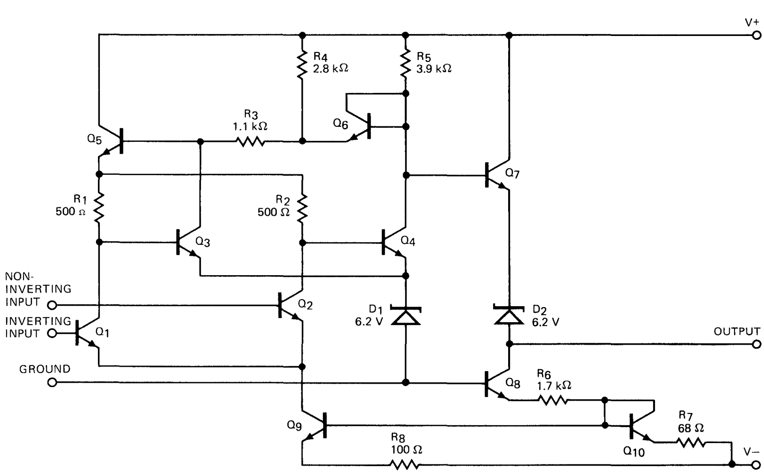
GENERAL DESCRIPTION — The μA710 is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

ABSOLUTE MAXIMUM RATINGS

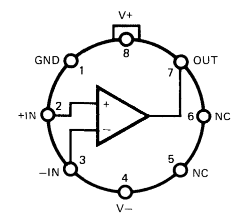
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Ouput Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Storage Temperature Range	
Metal Can, Hermetic DIP and Flatpak	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA710)	−55°C to +125°C
Commercial (μA710C)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

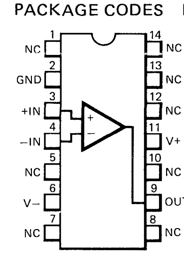


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA710	μA710HM
μA710C	μA710HC

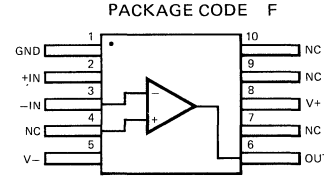
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710DM
μA710C	μA710DC
μA710C	μA710PC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710FM

*Planar is a patented Fairchild process.

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μA710

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified.

CHARACTERISTICS	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns
The following specifications apply for −55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient	$R_S = 50\ \Omega$, T_A = 25°C to T_A = +125°C		3.5	10	μV/°C
of Input Offset Voltage	$R_S = 50\ \Omega$, T_A = 25°C to T_A = −55°C		2.7	10	μV/°C
	T_A = +125°C		0.25	3.0	μA
	T_A = −55°C		1.8	7.0	μA
Average Temperature Coefficient	T_A = 25°C to T_A = +125°C		5.0	25	nA/°C
of Input Offset Current	T_A = 25°C to T_A = −55°C		15	75	nA/°C
Input Bias Current	T_A = −55°C		27	45	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	T_A = +125°C, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5	1.7		mA
	T_A = −55°C, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

μA710C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified

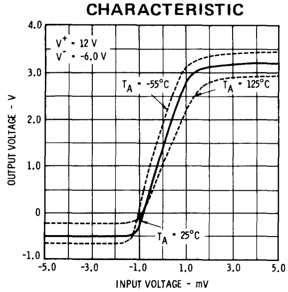
CHARACTERISTICS	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, T_A = 0°C to T_A = +70°C		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient	T_A = 25°C to T_A = +70°C		15	50	nA/°C
of Input Offset Current	T_A = 25°C to T_A = 0°C		24	100	nA/°C
Input Bias Current	T_A = 0°C		25	40	μA
Input Voltage Range	V = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

NOTES:

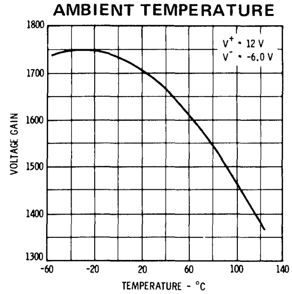
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for DIP, and 7.1 mW/°C for the Flatpak.
2. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage as follows: For 710, 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C. For 710C, 1.5 V at 0°C, 1.4 V at +25°C, and 1.2 V at +70°C.
3. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA710

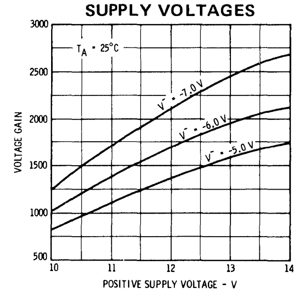
VOLTAGE TRANSFER CHARACTERISTIC



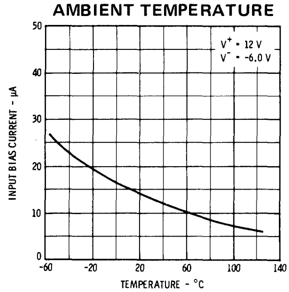
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



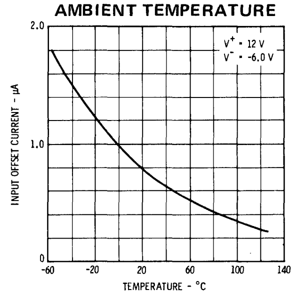
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



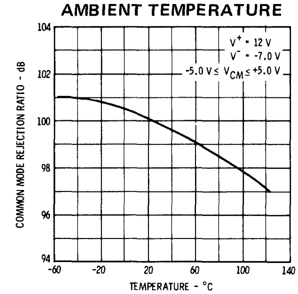
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



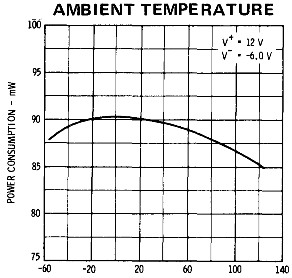
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



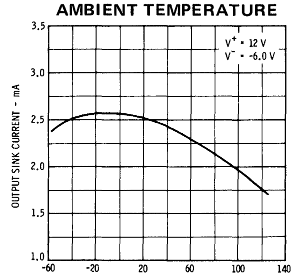
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



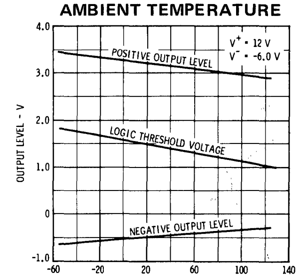
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



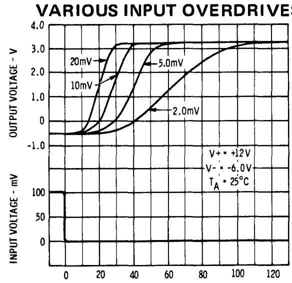
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



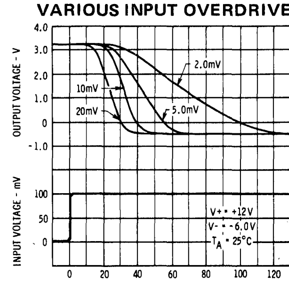
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



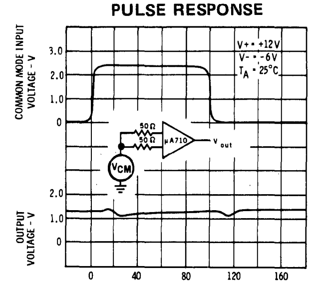
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



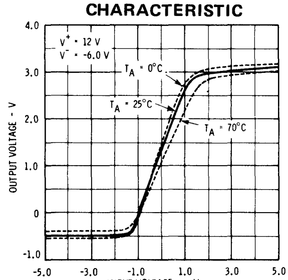
COMMON MODE PULSE RESPONSE



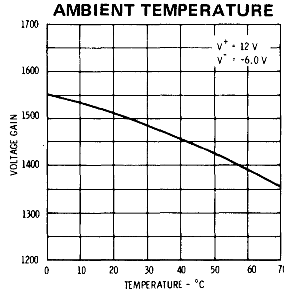
6

TYPICAL PERFORMANCE CURVES FOR μA710C

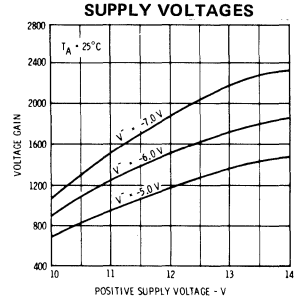
VOLTAGE TRANSFER CHARACTERISTIC



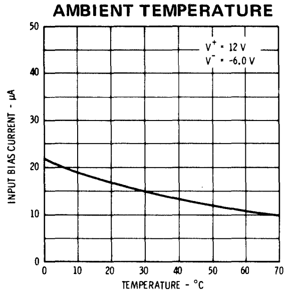
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



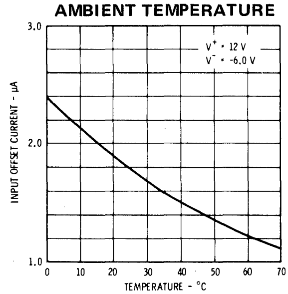
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



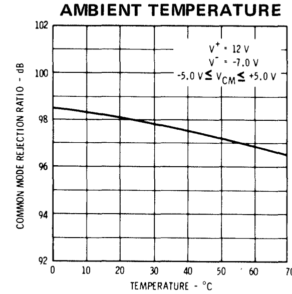
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



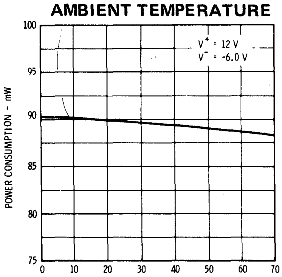
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



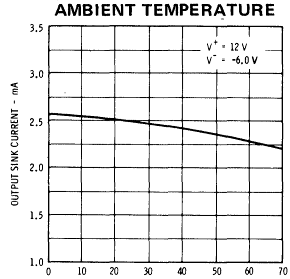
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



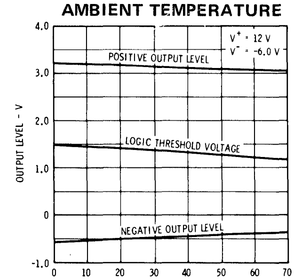
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



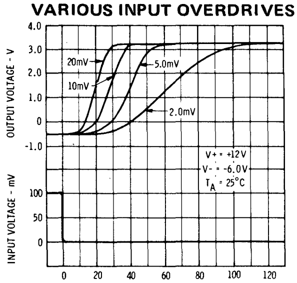
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



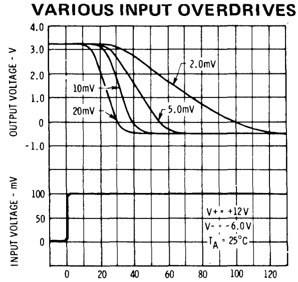
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



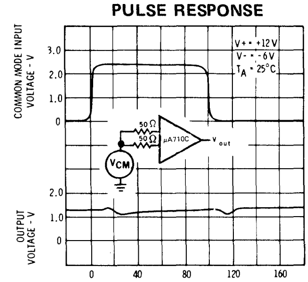
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



μA711

DUAL HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

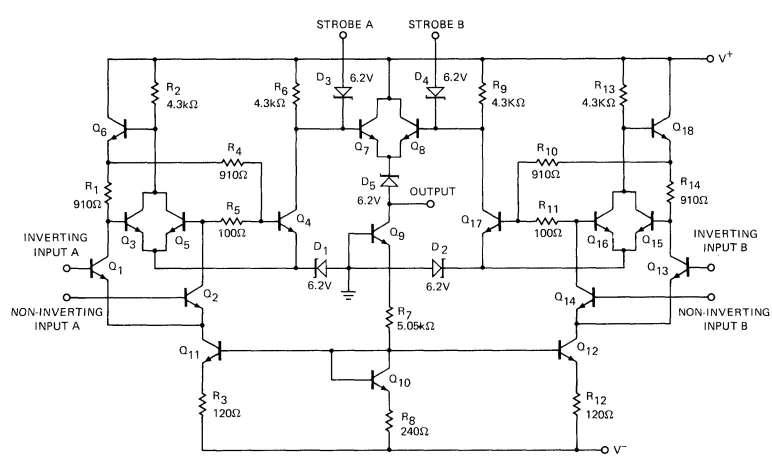
GENERAL DESCRIPTION — The μA711 is a Dual, Differential Voltage Comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-Go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar* epitaxial process.

- **FAST RESPONSE TIME . . . 40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT STROBING OF EACH COMPARATOR**

ABSOLUTE MAXIMUM RATINGS

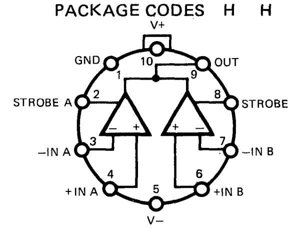
Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (μA711)	−55°C to +125°C
Commercial (μA711C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



Notes on following page.

CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEWS)
PACKAGE OUTLINES 5F 5N
PACKAGE CODES H H

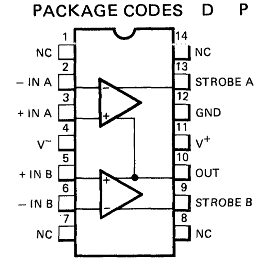


NOTE: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA711	μA711HM
μA711C	μA711HC

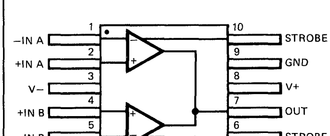
14-PIN DIP
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711DM
μA711C	μA711DC
μA711C	μA711PC

10-PIN FLATPAK
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711FM

*Planar is a patented Fairchild process.

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μA711

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V^+ = 12$ V, $V^- = -6.0$ V unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	$V_{OUT} = 1.4$ V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10$ mV, $I_O = 5$mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		8.6		mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, and 7.1 mW/°C for the Flatpak.
2. The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
   711: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C
   711C: 1.5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

μA711C

ELECTRICAL CHARACTERISTICS: T_A= 25°C, V^+= 12 V, V^-= −6.0 V unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, R_S ≤200 Ω, V_{CM} = 0		1.0	5.0	mV
	V_{OUT} = +1.4 V, R_S ≤200 Ω		1.0	7.5	mV
Input Offset Current	V_{OUT} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	V_{IN} ≥10 mV		4.5	5.0	V
Loaded Output HIGH Voltage	V_{IN} ≥10 mV, I_O = 5 mA	2.5	3.5		V
Output LOW Voltage	V_{IN} ≥10 mV	−1.0	−0.5	0	V
Strobed Output Level	V_{STROBE} ≤0.3 V	−1.0		0	V
Output Sink Current	V_{IN} ≥10 mV, V_{OUT} ≥0	0.5	0.8		mA
Strobe Current	V_{STROBE} = 100 mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} Gnd, Inverting Input = +10mV		8.6		mA
Negative Supply Current	V_{OUT}Gnd, Inverting Input = +10mV		3.9		mA
Power Consumption			130	230	mW

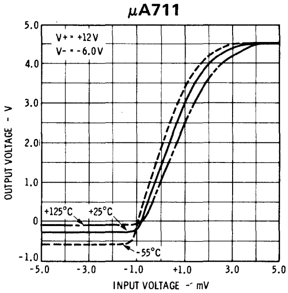
The following specifications apply for 0° C ≤ T_A ≤ +70° C:

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	R_S ≤ 200 Ω, V_{CM} = 0			6.0	mV
	R_S ≤ 200 Ω			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

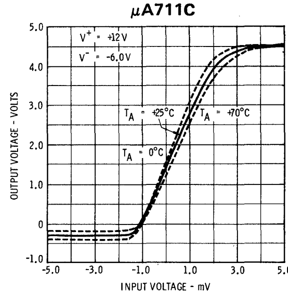
6

TYPICAL PERFORMANCE CURVES FOR µA711 AND µA711C

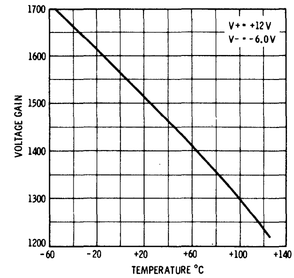
VOLTAGE TRANSFER CHARACTERISTIC µA711



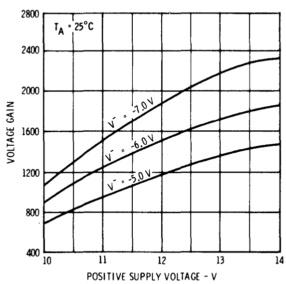
VOLTAGE TRANSFER CHARACTERISTIC µA711C



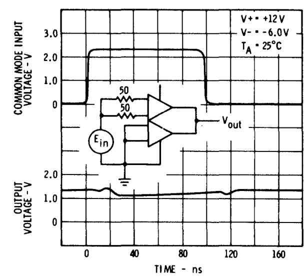
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



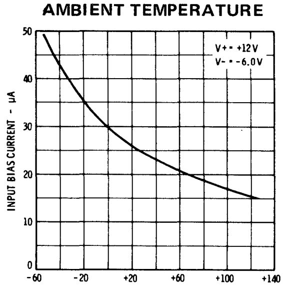
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



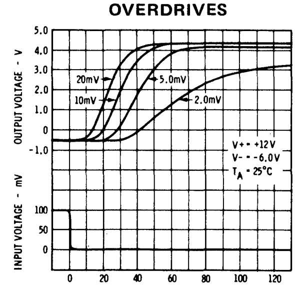
COMMON MODE PULSE RESPONSE



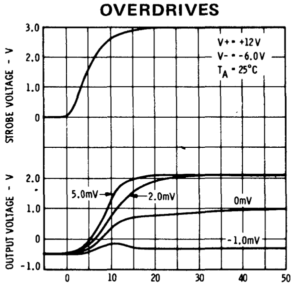
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



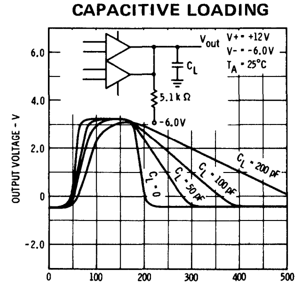
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



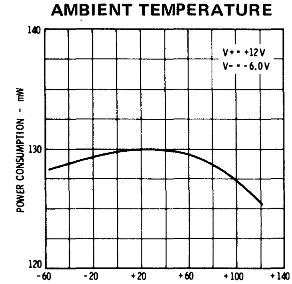
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



μA734

PRECISION VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

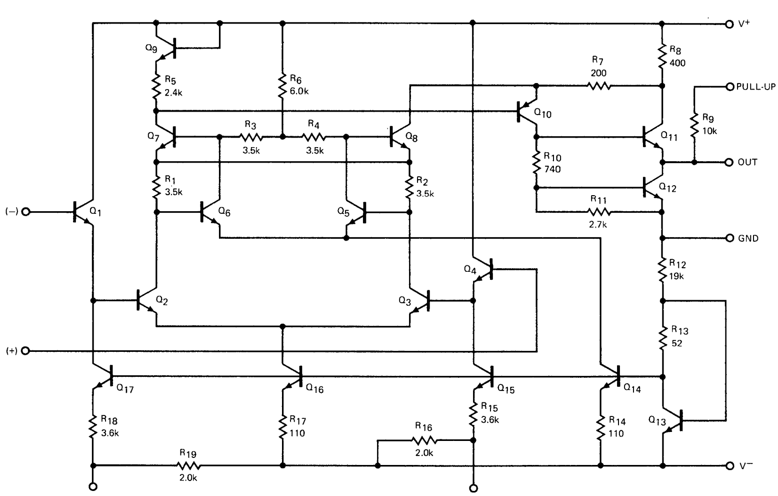
GENERAL DESCRIPTION — The μA734 is a Precision Voltage Comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility.

- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE — 55 MΩ**
- **LOW DRIFT — 3.5 μV/°C**
- **HIGH GAIN — 60 k**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE — ±5 V to ±18 V**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

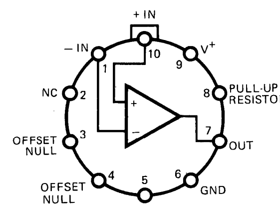
Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range (Note 1)	±13 V
Voltage Between Offset Null and V−	±0.5 V
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA734)	−55°C to +125°C
Commercial (μA734C)	0°C to +70°C
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Pin Temperature (Soldering, 60 s Max)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

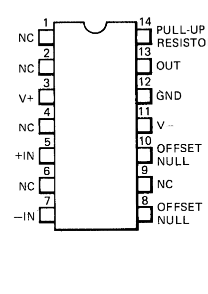
CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5N
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734HM
μ734C	μA734HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734DM
μA734C	μA734DC

*Planar is a patented Fairchild process.

±15 VOLT OPERATION FOR μA734C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 50$ kΩ		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	60 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns

The following specifications apply for 0°C ⩽ T_A ⩽ +70°C

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 50$ kΩ		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leqslant 50$ Ω		3.5	20	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +70°C		0.02	0.3	nA/°C
	T_A = +25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leqslant 50$ kΩ	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leqslant 50$ kΩ		6.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA	7.0			V
	I_{OUT} = 0.080 mA, V_8 = +5.0 V	2.4		5.0	V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

±15 VOLT OPERATION FOR μA734

ELECTRICAL CHARACTERISTICS: T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50$ kΩ		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	70 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns

The following specifications apply for $-55°C \leq T_A \leq +125°C$

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50$ kΩ		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50$ kΩ		2.5	15	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +125°C		0.01	0.1	nA/°C
	T_A = +25°C to −55°C		0.05	0.4	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50$ kΩ		5.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA	7.0			V
	I_{OUT} = 0.080 mA, V_8 = +5.0 V	2.4		5.0	V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

NOTES:
1. Rating applies for ±15 V supplies. For other supply voltages the rating is within 2 V of either supply.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for DIP.
3. Pin numbers refer to metal can package.

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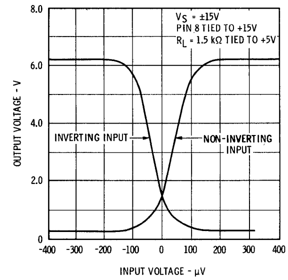
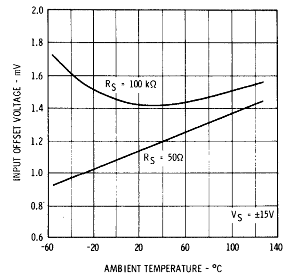
TYPICAL PERFORMANCE CURVES FOR µA734 AND µA734C (Note 2)

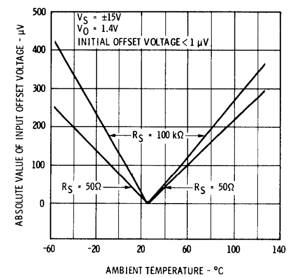
TRANSFER CHARACTERISTICS



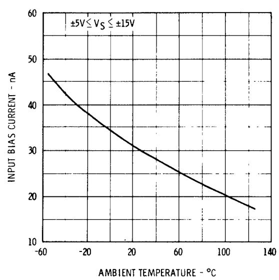
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



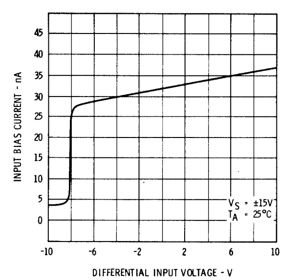
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25°C



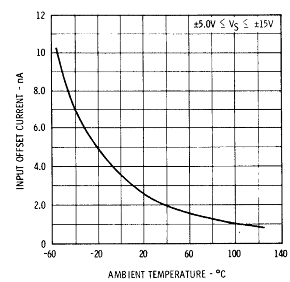
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



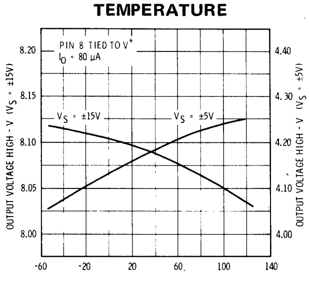
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



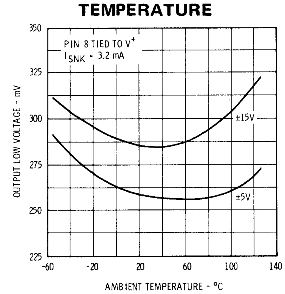
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



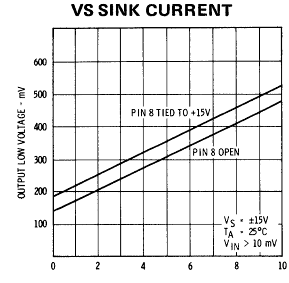
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



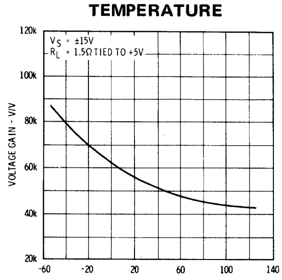
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



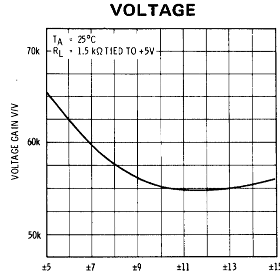
OUTPUT VOLTAGE LOW VS SINK CURRENT



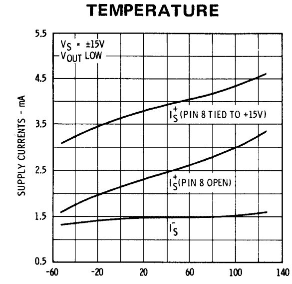
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

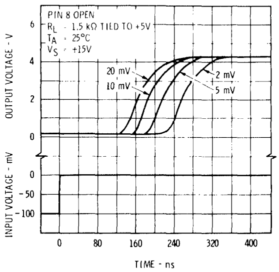


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

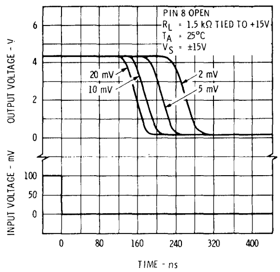


TYPICAL PERFORMANCE CURVES FOR μA734 AND μA734C (Note 2)

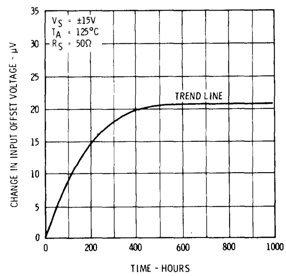
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



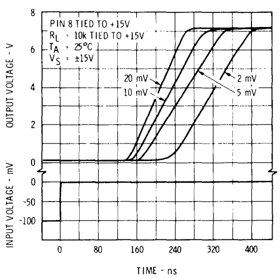
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



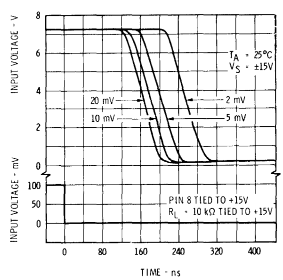
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



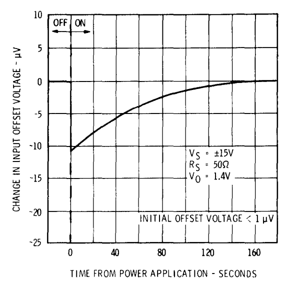
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



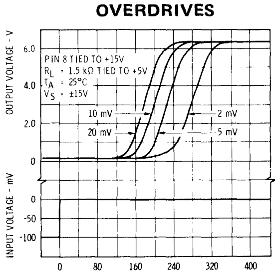
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



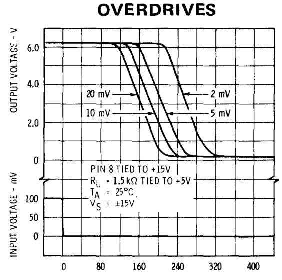
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



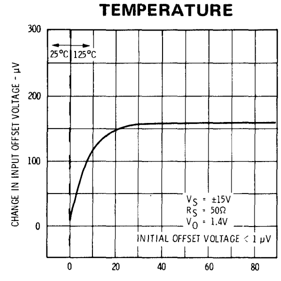
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



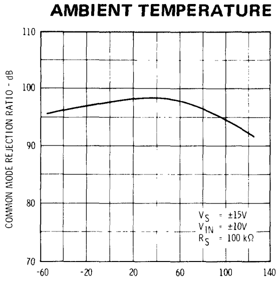
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



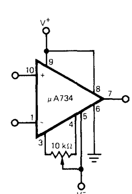
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



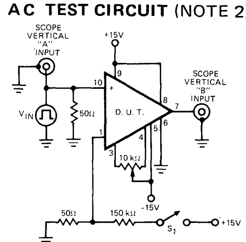
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT (NOTE 2)



AC TEST CIRCUIT (NOTE 2)



V_{IN} = -100 mV, 100 kHz

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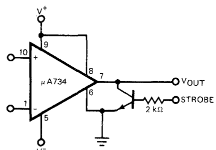
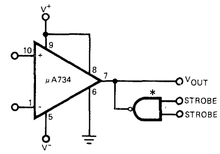
TYPICAL APPLICATIONS (Note 2)

STROBE CIRCUITRY

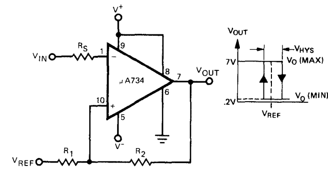


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

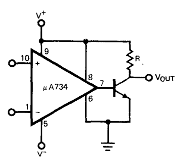
LEVEL DETECTOR WITH HYSTERESIS



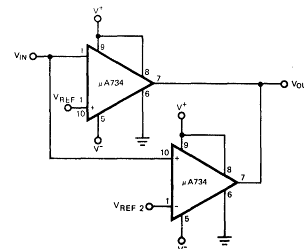
$R_S = \frac{R_1 R_2}{R_1 + R_2}$ FOR MINIMUM OFFSET

$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$

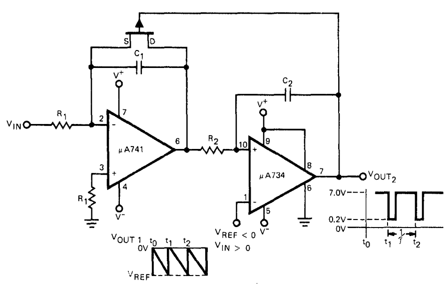
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

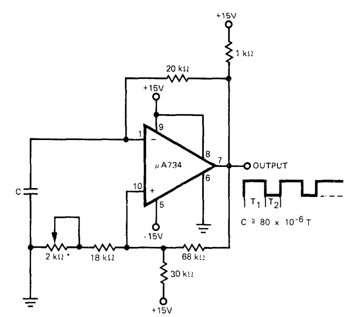


VOLTAGE CONTROLLED OSCILLATOR



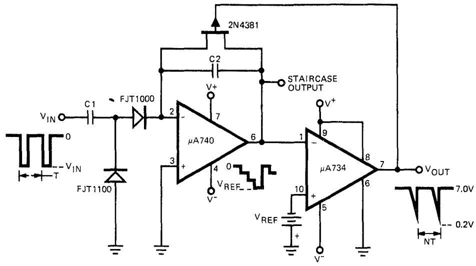
$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1}$ $\quad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$

FREE RUNNING OSCILLATOR



* Adjusts $\frac{T_1}{T_2}$

FREQUENCY DIVIDER & STAIRCASE GENERATOR

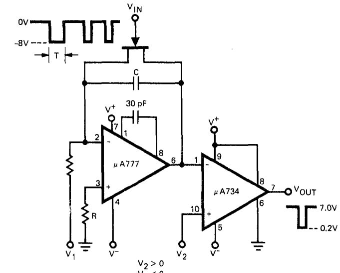


$|V_{REF}| = 2V_D + N \left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$

T In Seconds

V_D for FJT1000 $\approx 0.31V$

PULSE WIDTH DISCRIMINATOR

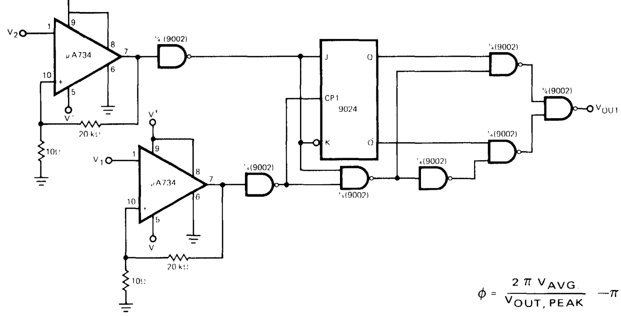


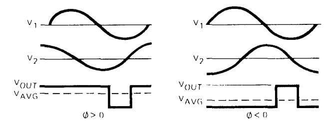
VOUT Pulse Appears

Whenever $T > \frac{R\,C\,V_2}{|V_1|}$

TYPICAL APPLICATIONS (Note 2)

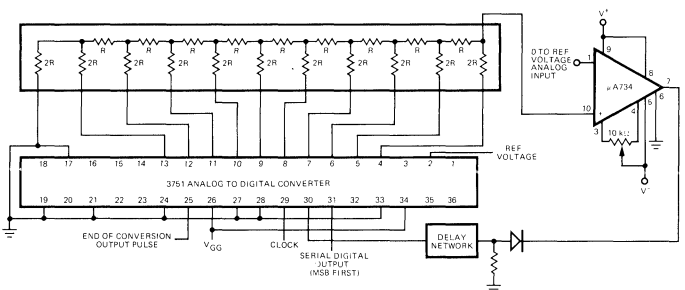
PHASE METER





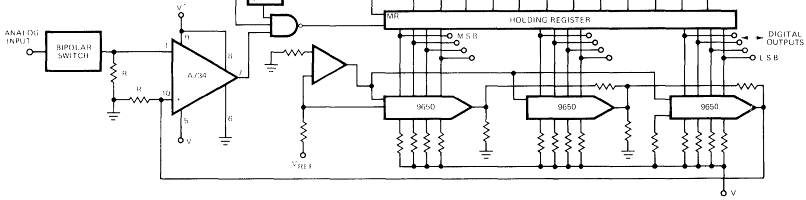
$$\phi = \frac{2\pi V_{AVG}}{V_{OUT,PEAK}} - \pi$$

12-BIT A/D CONVERTER



NO. OF BITS	R VALUE
8	12.5kΩ
9	25kΩ
10	50kΩ
12	200kΩ

12-BIT A/D CONVERTER



μA760

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

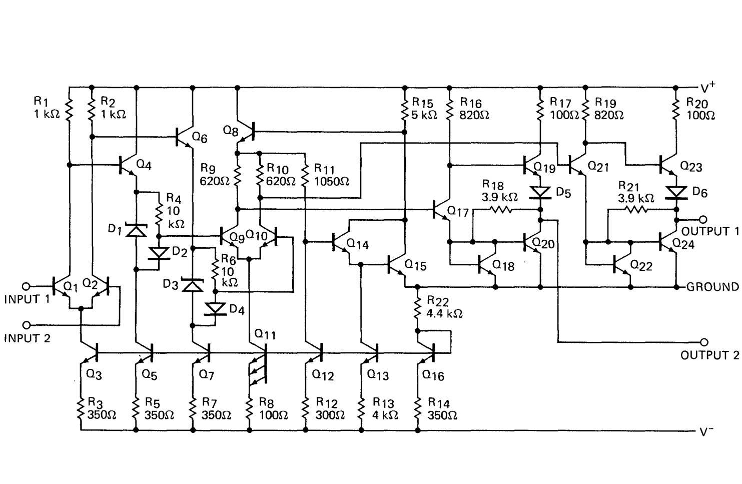
GENERAL DESCRIPTION – The μA760 is a Differential Voltage Comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 V to ±6.5 V. The μA760 can be used in high speed analog to digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED – 25 ns MAX**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+8 V
Negative Supply Voltage	-8 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	$V+ \geq V_{IN} \geq V-$
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA760)	-55°C to 125°C
Commercial (μA760C)	0°C to 70°C
Storage Temperature Range	
Metal Can and DIP	-65°C to 150°C

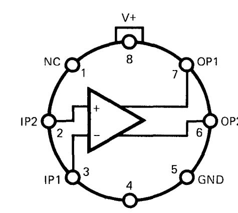
EQUIVALENT CIRCUIT



Notes on following page.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5S
PACKAGE CODE H



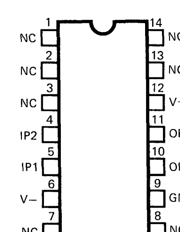
NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA760	μA760HM
μA760C	μA760HC

14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA760	μA760DM
μA760C	μA760DC

μA760

ELECTRICAL CHARACTERISTICS: V_S = ±4.5 V to ±6.5 V, T_A = −55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, T_A = −55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +125°C		2.0		nA/°C
	T_A = 25°C to T_A = −55°C		7.0		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA, V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.4	3.0		V
Output LOW Voltage (either output)	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

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μA760C

ELECTRICAL CHARACTERISTICS: V_S = ±4.5 V to ±6.5 V, T_A = -55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.

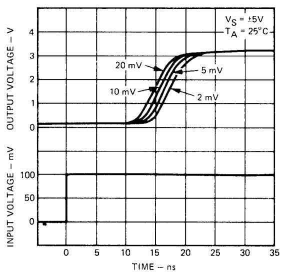
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, T_A = 25°C			10	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			10	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 0°C to T_A = +70°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C		5.0		nA/°C
	T_A = 25°C to T_A = 0°C		10		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA, V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.5	3.0		V
Output LOW Voltage (either output)	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	34	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

NOTES

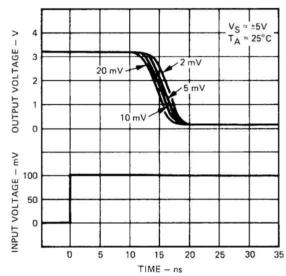
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 8.3 mW/°C for the DIP.
2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C

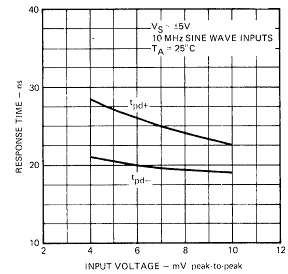
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



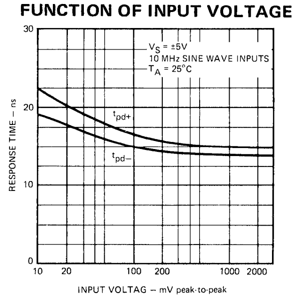
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



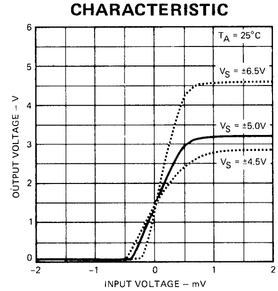
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



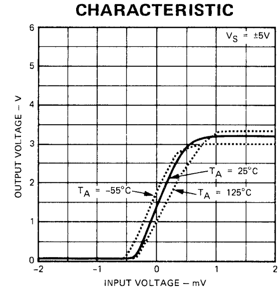
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



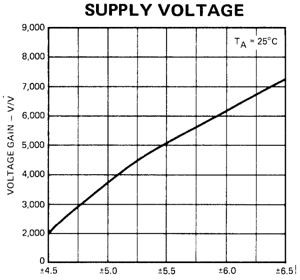
VOLTAGE TRANSFER CHARACTERISTIC



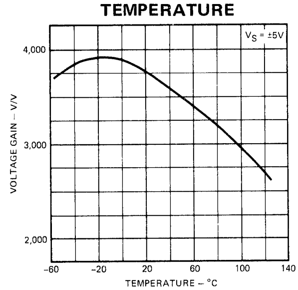
VOLTAGE TRANSFER CHARACTERISTIC



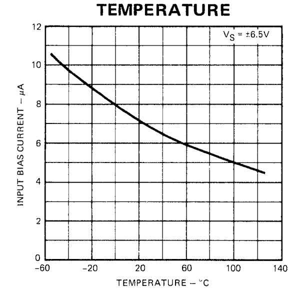
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



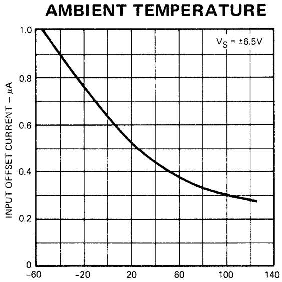
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



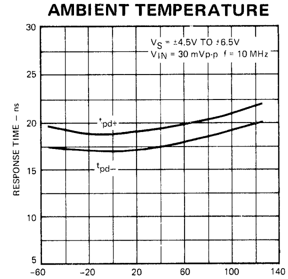
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



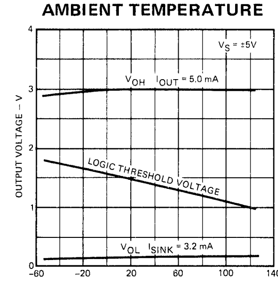
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



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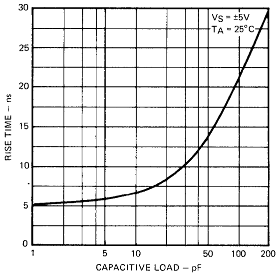
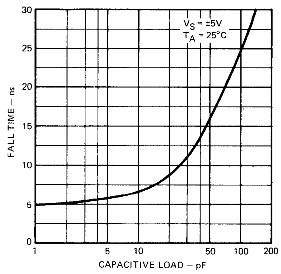
TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C (Cont'd)

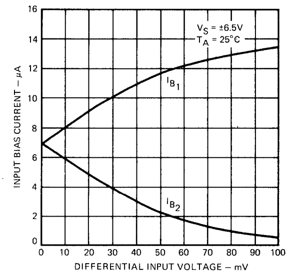
RISE TIME AS A FUNCTION OF CAPACITIVE LOAD



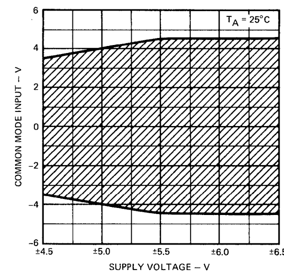
FALL TIME AS A FUNCTION OF CAPACITIVE LOAD



INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



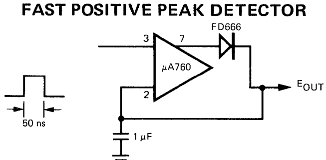
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



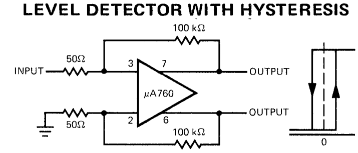
APPLICATIONS

Pin numbers shown are only for Metal Can

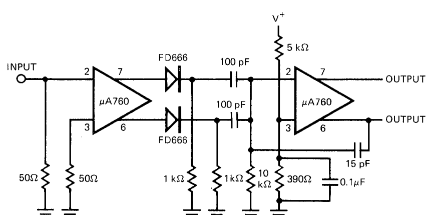
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

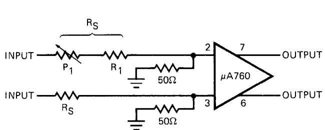


ZERO CROSSING DETECTOR



Total Delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVpk-pk

LINE RECEIVER WITH HIGH COMMON MODE RANGE



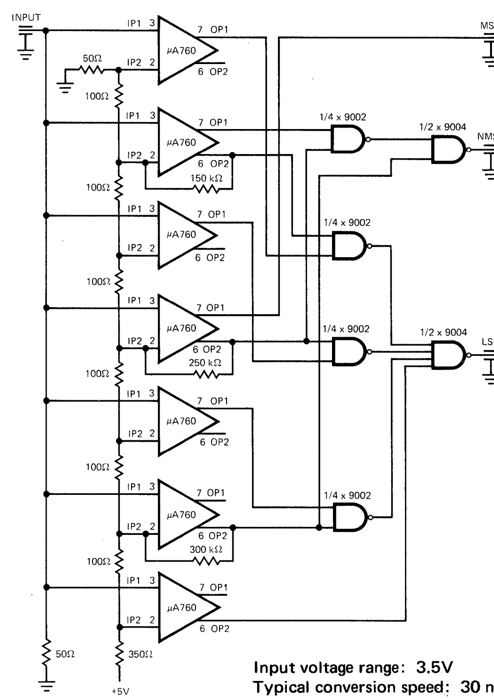
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential Input sensitivity = $5 \times \frac{RS}{50}$ mV

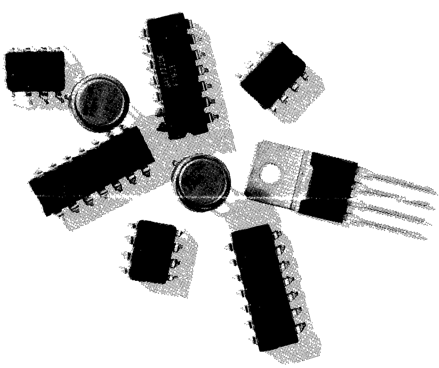
P_1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$
Common mode range = ±16V
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns



TIMERS AND SPECIAL FUNCTIONS

TIMERS

SPECIAL FUNCTIONS

μA555

SINGLE TIMING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

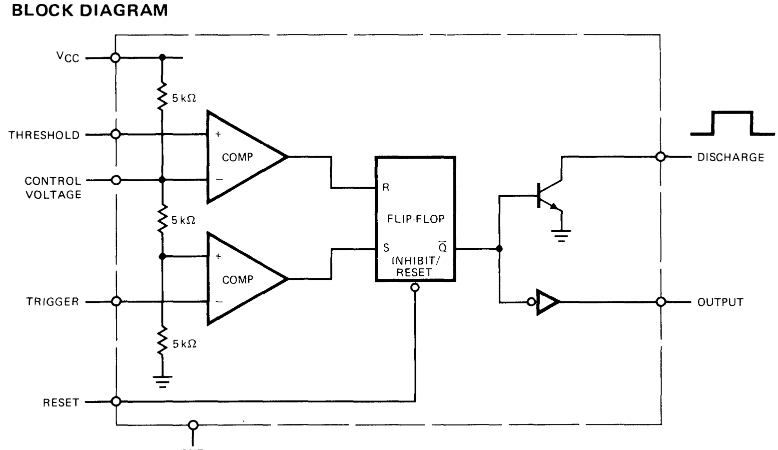
The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**
- **DIRECT REPLACEMENT FOR SE555/NE555**

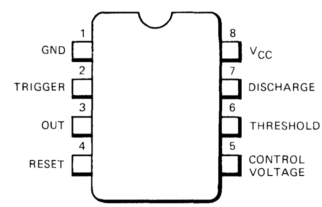
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
μA555TC/HC	0°C to +70°C
μA555HM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Plastic Mini DIP(9T) (Soldering, 10 s)	260°C
Metal Can (5T) (Soldering, 60 s)	300°C

BLOCK DIAGRAM



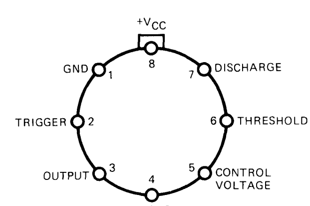
CONNECTION DIAGRAMS
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555TC

8-PIN TO-100
(TOP VIEW)
PACKAGE OUTLINE 5T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555HM
μA555	μA555HC

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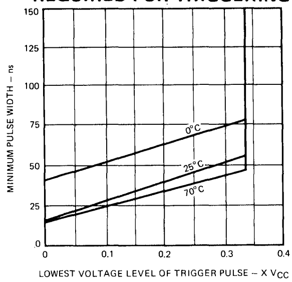
ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_{CC} = +5.0 V to +15 V, unless otherwise specified

CHARACTERISTICS	TEST CONDITIONS	μA555HM			μA555TC/HC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5.0 V, $R_L = \infty$		3.0	5.0		3.0	6.0	mA
	V_{CC} = 15 V, $R_L = \infty$ LOW State (Note 1)		10	12		10	15	mA
Timing Error								
Initial Accuracy	R_A, R_B = 1 kΩ to 100 kΩ		0.5	2.0		1.0		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage Drop (LOW)	V_{CC} = 15 V I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage Drop (HIGH)	I_{SOURCE} = 200 mA V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA V_{CC} = 15 V	13	13.3		12.75	13.3		V
	V_{CC} = 5.0 V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

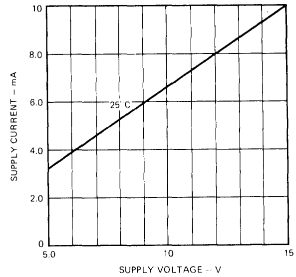
NOTES:
1. Supply Current is typically 1.0 mA less when output is HIGH.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$. For 15 V operation, the max total R = 20 MΩ.
4. For operating at elevated temperatures the device must be derated based on a +125°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

TYPICAL PERFORMANCE CURVES

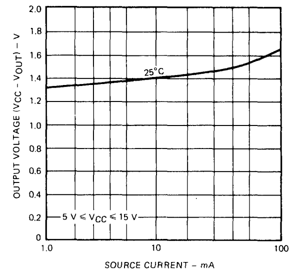
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



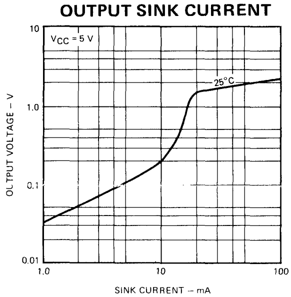
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



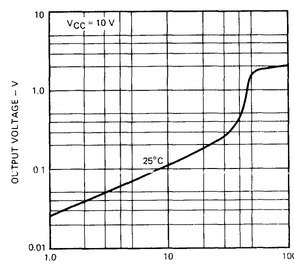
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



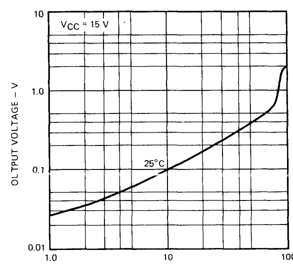
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



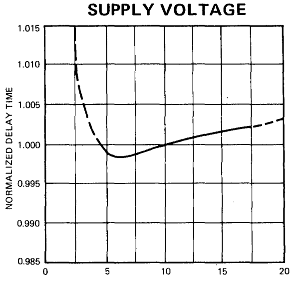
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



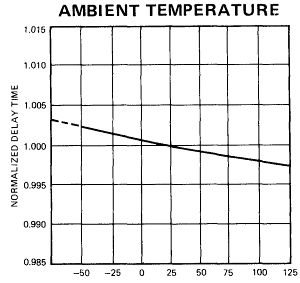
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



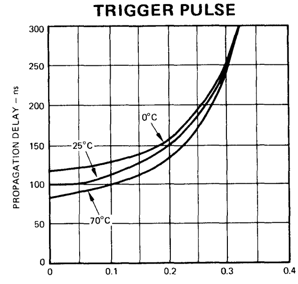
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



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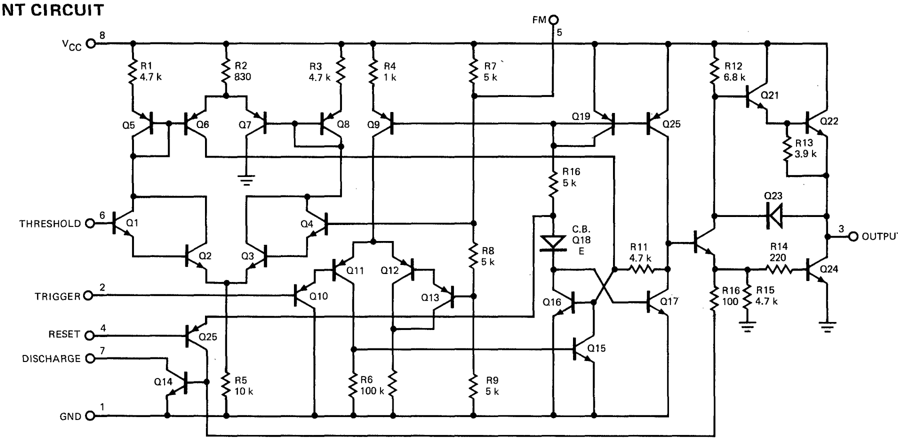
EQUIVALENT CIRCUIT



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

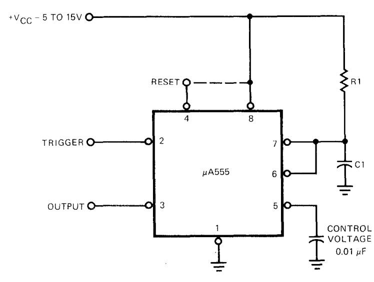


Fig. 1

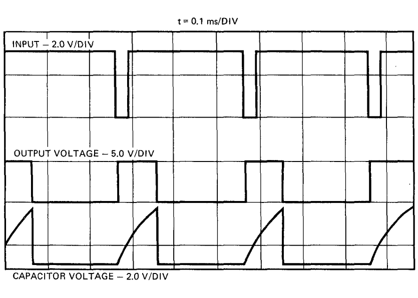


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

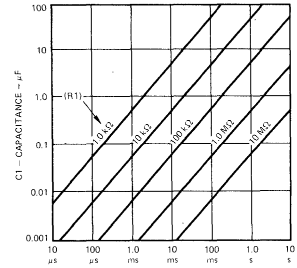


Fig. 3

TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

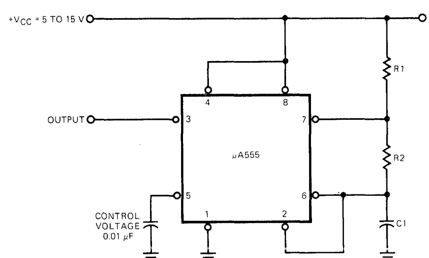


Fig. 4

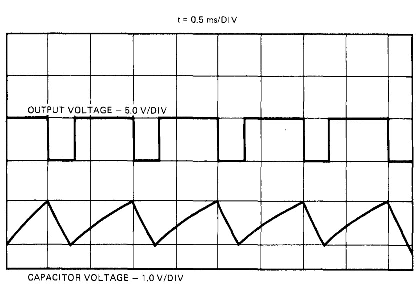


Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

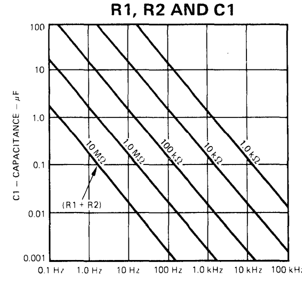


Fig. 6

7

μA556

DUAL TIMING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA556 Timing Circuits are very stable controllers for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied, ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

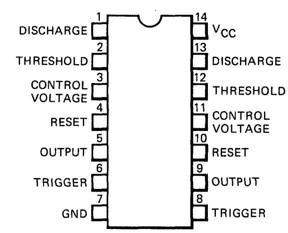
The μA556 Dual Timing Circuit is a pair of 555s for use in sequential timing or applications requiring multiple timers.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation	600 mW
Operating Temperature Ranges	
μA556 DC/PC	0°C to +70°C
μA556DM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering)	
(10 s) Plastic DIP (9A)	260°C
(60 s) Ceramic DIP (6A)	300°C

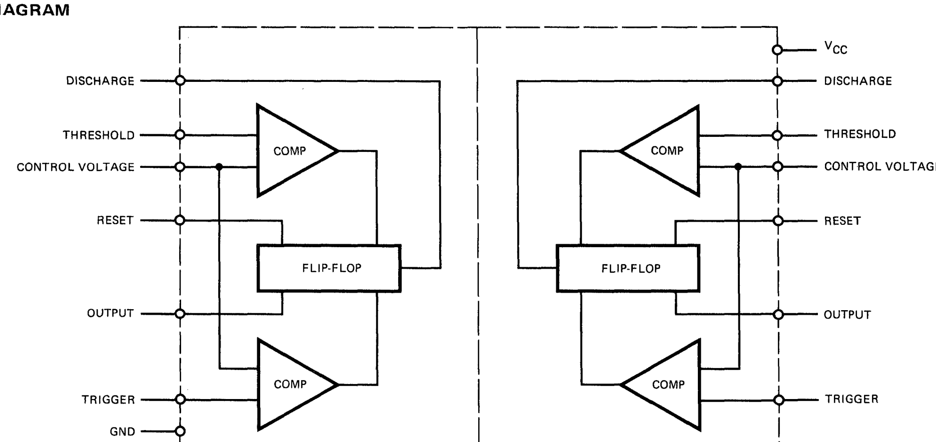
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA556	μA556DC
μA556	μA556DM
μA556	μA556PC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: T_A= 25°C, V_{CC}= +5.0 V to +15 V, unless otherwise specified

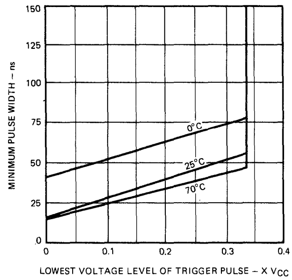
CHARACTERISTICS	TEST CONDITIONS	μA556DM			μA556DC/PC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Total)	V_{CC} = 5.0 V, R_L = ∞		6.0	10		6.0	12	mA
	V_{CC} = 15 V, R_L = ∞ LOW State (Note 1)		20	22		20	28	mA
Timing Error (Monostable)								
Initial Accuracy	R_A = 2 kΩ to 100 kΩ		0.5	1.5		0.75		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Timing Error (Astable)								
Initial Accuracy	R_A, R_B = 2 kΩ to 100 kΩ		1.5			2.25		%
Drift with Temperature	C = 0.1 μF (Note 2)		90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage (LOW)	V_{CC} = 15 V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.25		2.0	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V							
	I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage (HIGH)	I_{SOURCE} = 200 mA							
	V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15 V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5.0V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%V

NOTES:
1. Supply current when output is HIGH is typically 1.0 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 MΩ.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

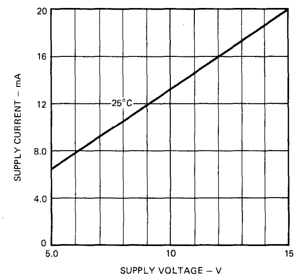
7

TYPICAL PERFORMANCE CURVES

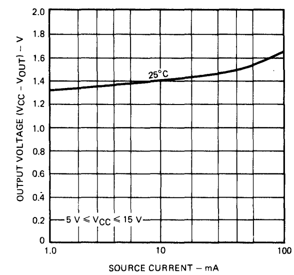
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



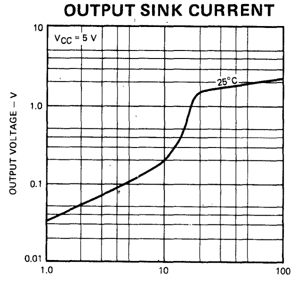
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



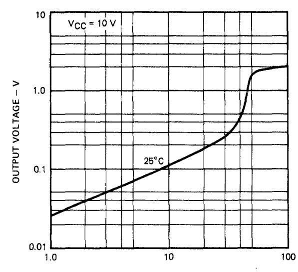
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



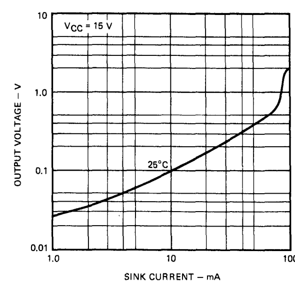
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



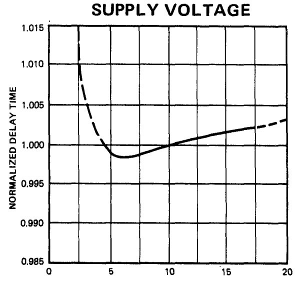
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



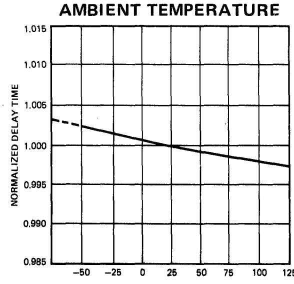
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



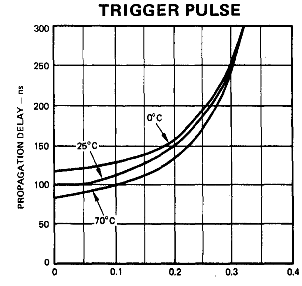
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



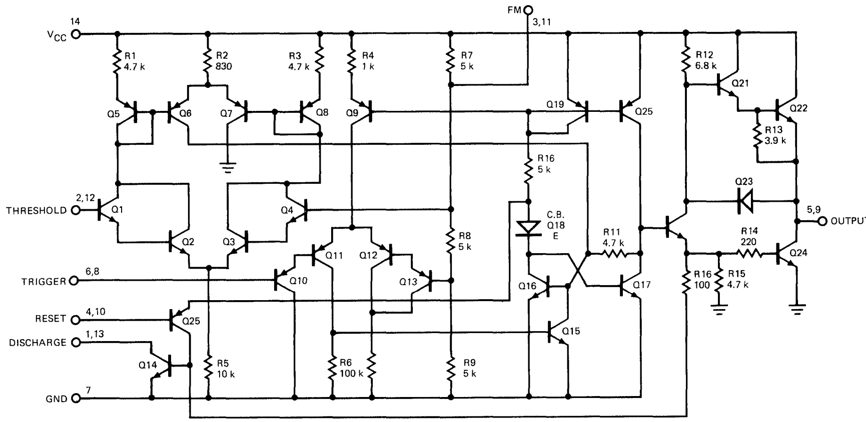
DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



EQUIVALENT CIRCUIT (One Half of μA556)



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 6) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

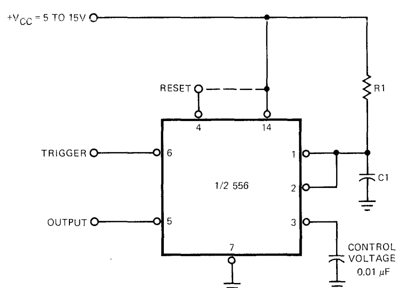


Fig. 1

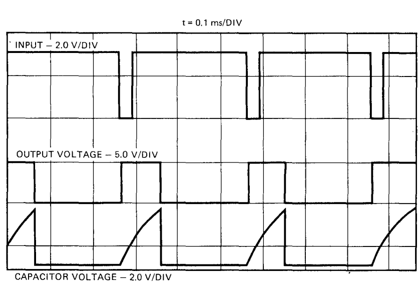


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

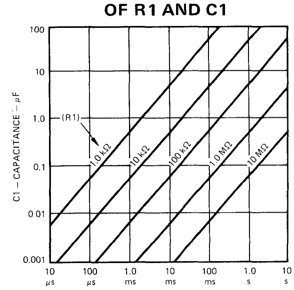


Fig. 3

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TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693 \, (R1 + R2) \, C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693 \, (R2) \, C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693 \, (R1 + 2R2) \, C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2) \, C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

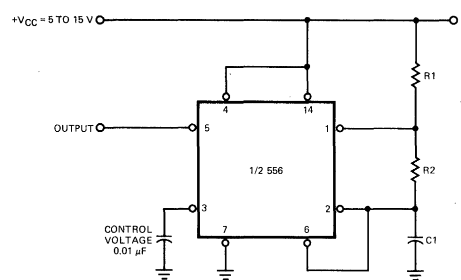
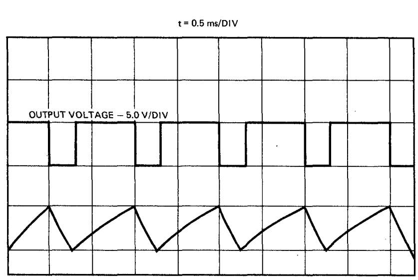


Fig. 4



R1 = R2 = 4.8 kΩ, C1 = 0.1 μF, R_L = 1 kΩ

Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

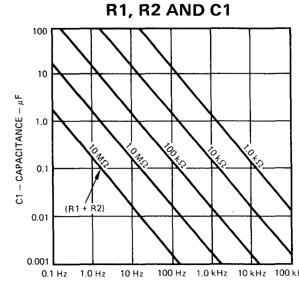


Fig. 6

μA2240

PROGRAMMABLE TIMER/COUNTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

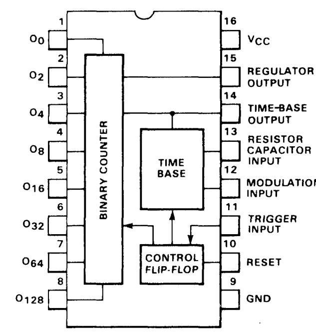
GENERAL DESCRIPTION – The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 RC TO 255 RC**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO RC TIME CONSTANT**
- **HIGH ACCURACY – 0.5%**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5 mA
Maximum Power Dissipation, Note 1	
Package Code D (Ceramic)	750 mW
Code P (Plastic)	650 mW
Operating Temperature Range Package	
Military (μA2240)	−55°C to +125°C
Commercial (μA2240C)	0°C to 70°C

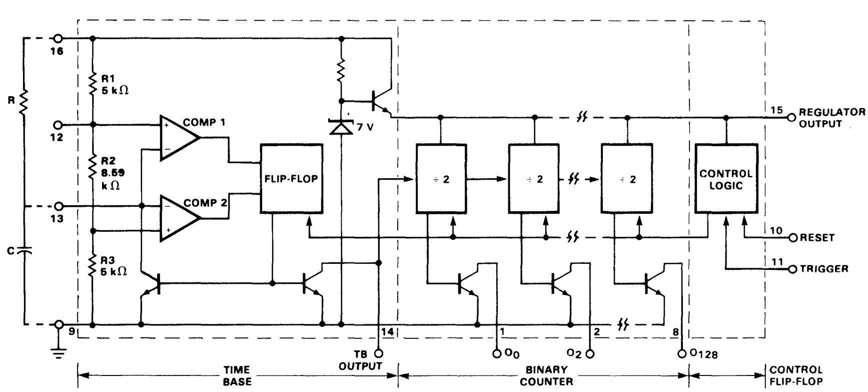
CONNECTION DIAGRAM
16-PIN DIP (TOP VIEW)
PACKAGE OUTLINES 7B, 9B
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA2240	μA2240DM
μA2240C	μA2240DC
μA2240C	μA2240PC

BLOCK DIAGRAM



NOTE 1: Above 25°C ambient derate linearly at 6.2 mW/°C for Package Code D and at 5.3 mW/°C for Package Code P.

ELECTRICAL CHARACTERISTICS: See Test Circuit Fig. 28, V_{CC} = 5 V, T_A = 25°C, R = 10 kΩ, C = 0.1 μF, unless otherwise noted

CHARACTERISTICS	CONDITIONS	μA2240			μA2240C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GENERAL CHARACTERISTICS								
Supply Voltage	For $V_{CC} \leq$ 4.5 V, Short Pin 15 to Pin 16	4.0		15	4.0		15	V
Supply Current								
Total Circuit	V_{CC} = 5 V, V_{TR} = 0, V_{RS} = 5 V		3.5	6.0		4.0	7.0	mA
	V_{CC} = 15 V, V_{TR} = 0, V_{RS} = 5 V		12	16		13	18	mA
Counter Only	See Test Circuit, Figure 29		1			1.5		mA
Regulator Output, V_{Reg}	Measured at Pin 15, V_{CC} = 5 V	4.1	4.4		3.9	4.4		V
	V_{CC} = 15 V, See Test Circuit, Figure 30	6.0	6.3	6.6	5.8	6.3	6.8	V
TIME BASE SECTION								
Timing Accuracy (Note 2)	V_{RS} = 0, V_{TR} = 5 V		0.5	2.0		0.5	5.0	%
Temperature Drift	V_{CC} = 5 V, 0°C ≤ T_J ≤ 75°C		150	300		200		ppm/°C
	V_{CC} = 15 V, 0°C ≤ T_J ≤ 75°C		80			80		ppm/°C
Supply Drift	$V_{CC} \geq$ 8 V, See Figure 23		0.05	0.2		0.08	0.3	%/V
Max Frequency	R = 1 kΩ, C = 0.007 μF	100	130			130		kHz
Modulation Voltage Level	Measured at Pin 12 V_{CC} = 5 V	3.00	3.50	4.0	2.80	3.50	4.20	V
	V_{CC} = 15 V		10.5			10.5		V
Recommended Range of Timing Components	See Figure 20							
Timing Resistor, R		0.001		10	0.001		10	MΩ
Timing Capacitor, C		0.007		1000	0.01		1000	μF
TRIGGER/RESET CONTROLS								
Trigger	Measured at Pin 11, V_{RS} = 0							
Trigger Threshold			1.4	2.0		1.4	2.0	V
Trigger Current	V_{RS} = 0, V_{TR} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			1.0			1.0		μs
Reset	Measured at Pin 10, V_{TR} = 0							
Reset Threshold			1.4	2.0		1.4	2.0	V
Reset Current	V_{TR} = 0, V_{RS} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			0.8			0.8		μs
COUNTER SECTION	See Test Circuit, Figure 30							
Max Toggle Rate	V_{RS} = 0, V_{TR} = 5 V Measured at Pin 14	0.8	1.5			1.5		MHz
Input Impedance			20			20		kΩ
Input Threshold		1.0	1.4		1.0	1.4		V
Output:	Measured at Pins 1 through 8							
Rise Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Fall Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Sink Current	$V_{OL} \leq$ 0.4 V	3.0	5.0		2.0	4.0		mA
Leakage Current	V_{OH} = 15 V		0.01	8.0		0.01	15	μA

NOTES:
2. Timing error solely introduced by μA2240, measured as % of ideal time base period of T = 1.00 RC.
3. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

FUNCTIONAL DESCRIPTION

(Figure 1 and Block Diagram, page 1)

When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive-going trigger pulse to TRIG, pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive-going reset pulse is applied to R, pin 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a Reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

In most timing applications, one or more of the counter outputs are connected to the Reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following to a trigger input.

Important Operating Information

- Ground connection is pin 9.
- Reset R (pin 10) sets all outputs HIGH.
- Trigger TRIG (pin 11) sets all outputs LOW.
- Time-base TBO (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1 k resistor.
- Normal Time-base Output TBO (pin 14) is a negative-going pulse greater than 500 ns.

  Note: Under the conditions of high supply voltages (V_{CC} > 7 V) and low values of timing capacitor (C < 0.1 μF, the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from TBO (pin 14) to ground (pin 9).
- Reset (pin 10) stops the time-base oscillator.
- Outputs $O_0 \ldots O_{128}$ (pins 1-8) sink 2 mA current with $V_{OL} \leqslant 0.4$ V.
- For use with external clock, minimum clock pulse amplitude should be 3 V, with greater than 1 μs pulse duration.

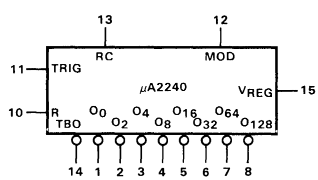


Fig. 1. Logic Diagram

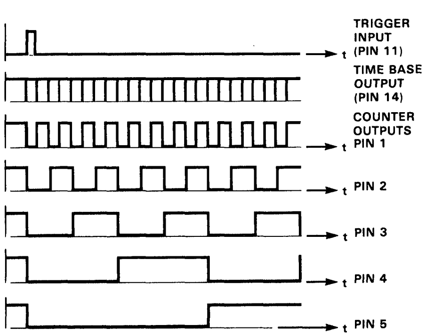


Fig. 2. Timing Diagram of Output Waveforms

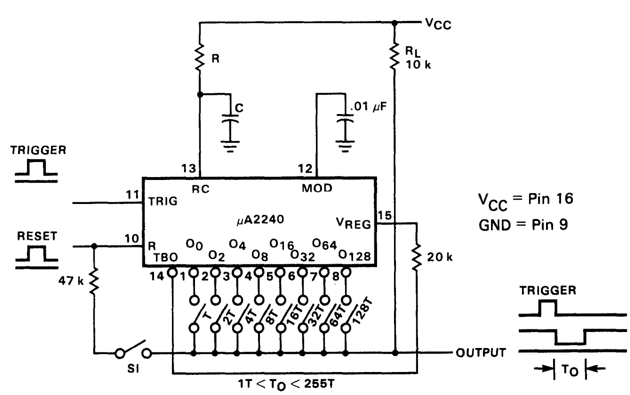


Fig. 3. Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open

7

CIRCUIT CONTROLS

Counter Outputs (O_0 . . . O_{128}, pins 1 thru 8)

The binary counter outputs are buffered open-collector type stages, as shown in the block diagram on page 1. Each output is capable of sinking 2 mA at 0.4 V V_{OL}. In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the Programming section.

Reset and Trigger Inputs (R and TRIG, pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops ($\approx$ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in *Figure 22*. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, pin 12)

The oscillator time-base period, T, can be modulated by applying a dc voltage to MOD, pin 12 (see *Figure 25*). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m)$$

where

m is an integer, $1 \leqslant m \leqslant 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

Time-Base Output (TBO, pin 14)

The time-base output is an open-collector type stage as shown in the block diagram, page, 1, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is $\approx$ +1.4 V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltages ($V_{CC} > 7$ V) and a small-value timing capacitor ($C < 0.1$ μF), the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

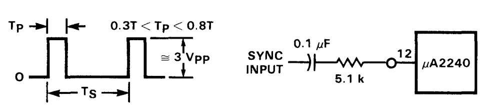


Fig. 4. Operation with External Sync. Signal

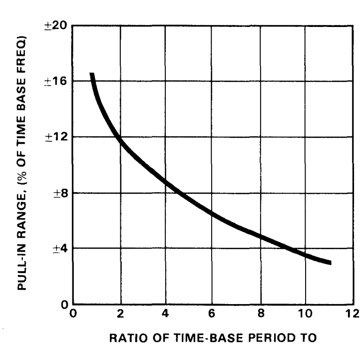


Fig. 5. Typical Pull-in Range for Harmonic Synchronization

Counter-Output Programming

The binary-counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open-collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\,T = 49\,T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\,T \leqslant T_O \leqslant 255\,T$.

Ultra Long Time-Delay Application

Two μA2240 units can be cascaded as shown in *Figure 6* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 7*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pins 15) of both units together.

ASTABLE OPERATION

The μA2240 can be operated in its astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. in astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some

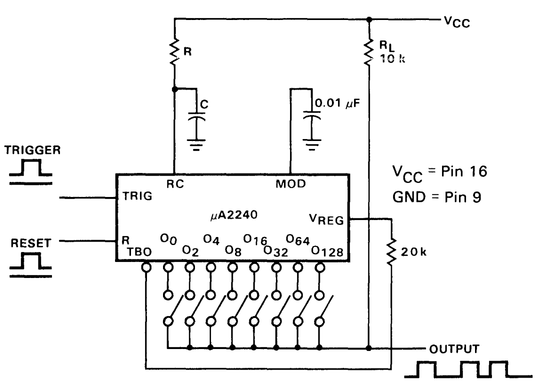


Fig. 8. Operation with External Trigger and Reset Inputs

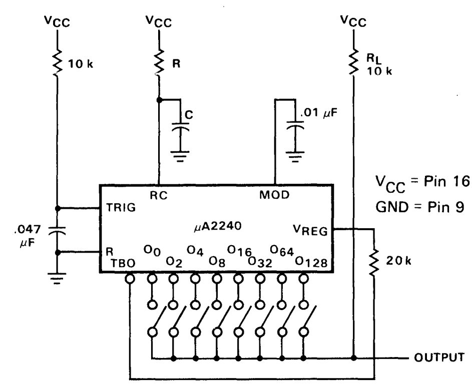


Fig. 9. Free-Running or Continuous Operation

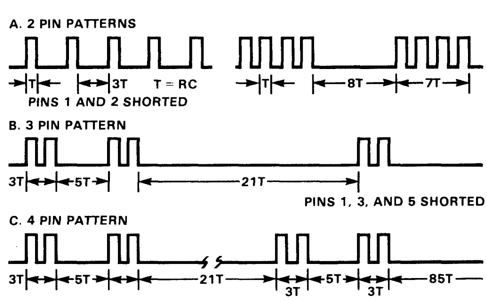


Fig. 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

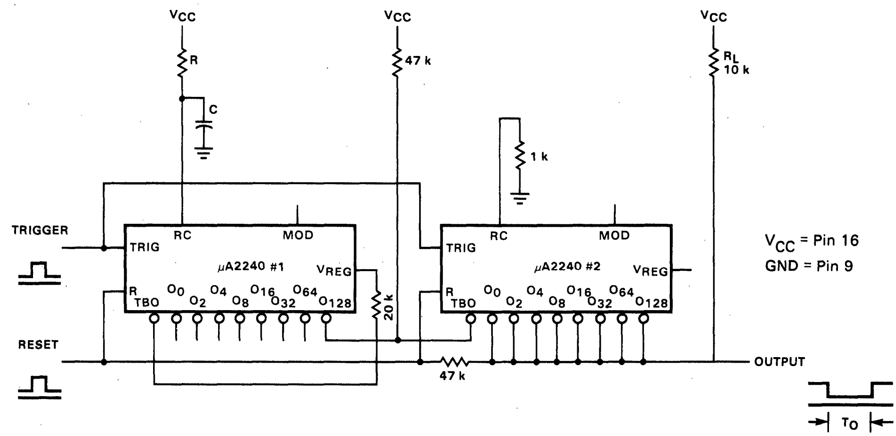


Fig. 6. Cascaded Operation for Long Delays

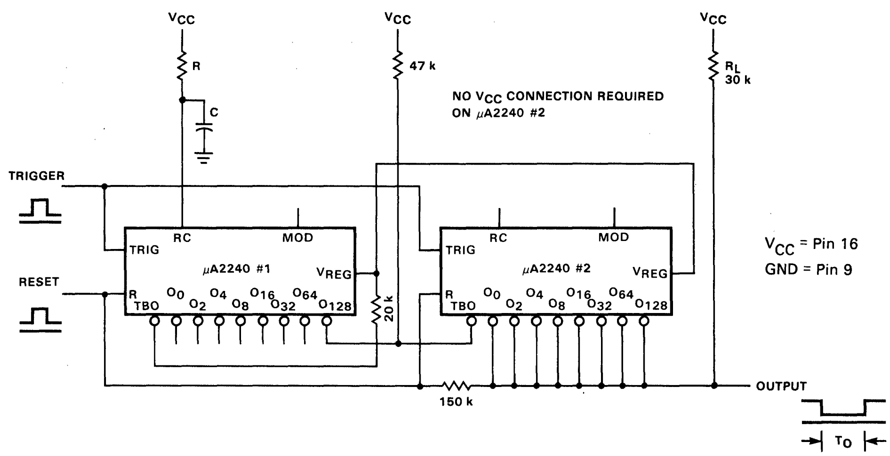


Fig. 7. Low Power Operation of Cascaded Timers

Regulator Output (V_{REG}, pin 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded (see *Figure 7*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, pin 15 should be shorted to pin 16.

MONOSTABLE OPERATION

Precision Timing
In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration, T_O, and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see *Figure 21*) and N is an integer in the range of $1 \leqslant N \leqslant 255$ as determined by the combination of counter outputs $O_0 \ldots O_{128}$, pins 1 through 8, connected to the output bus.

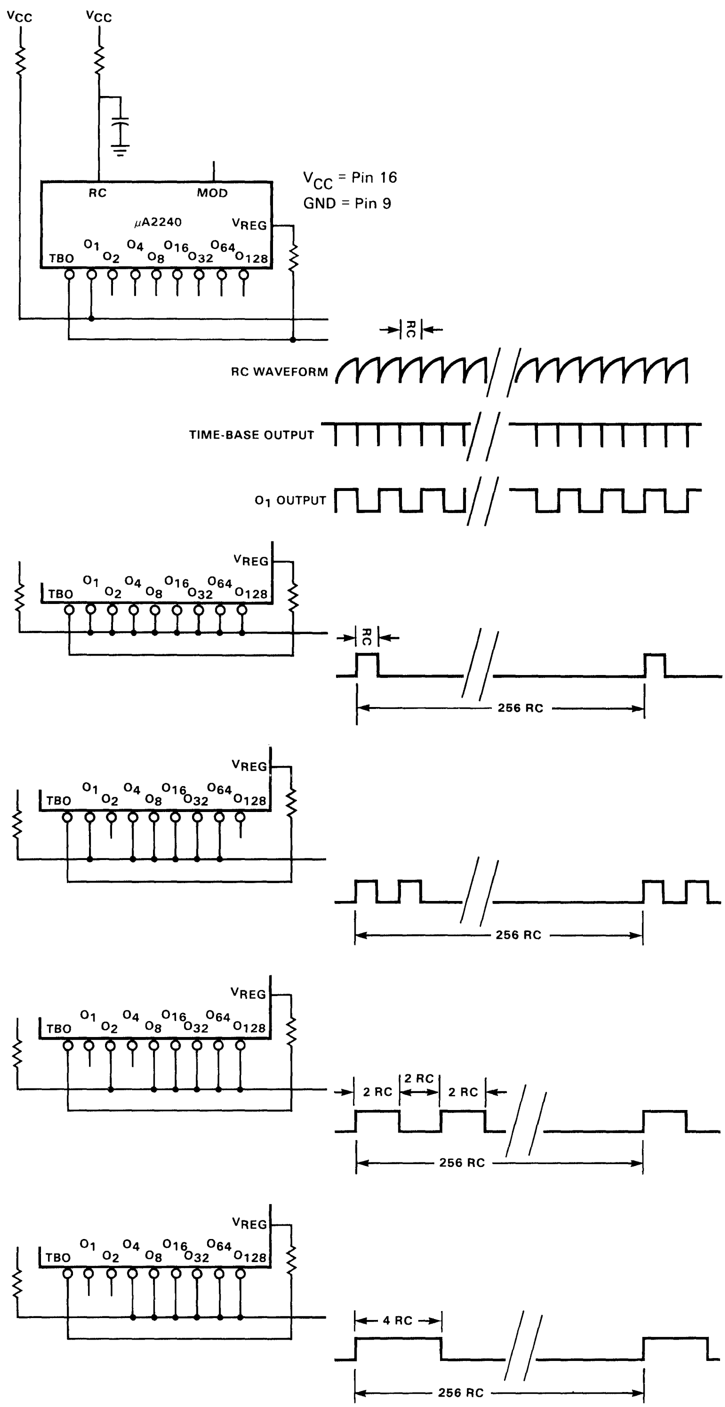


Fig. 11. Continuous Free-run Operation Examples of Output

of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

OPERATION WITH EXTERNAL CLOCK

The μA2240 can be operated with an external clock or time base by disabling the internal time-base oscillator and applying the external clock input to TBO, pin 14. The recommended circuit connection for this application is shown in *Figure 12.* The internal time base is de-activated by connecting a 1 kΩ resistor from RC, pin 13, to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 V is required. Minimum external clock pulse width must be ⩾ 1 μs.

For low power operation with supply voltages of 6 V or less, the internal time base section can be powered down by connecting V_{CC} to pin 15 and leaving pin 16 open. In this configuration, the internal time base does not draw any current and the overall current drain is reduced by ≈ 3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of the μA2240 can be used to generate 255 discrete frequencies from a given time-base output setting using the circuit connection of *Figure 13.* The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the counter outputs connected to the output bus. For example, if pins 1, 3 and 4 are connected together to the output bus, the total count is N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14 T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.

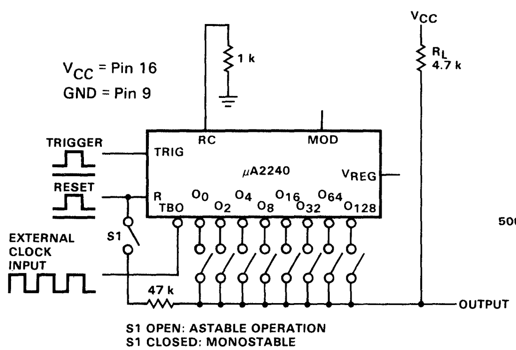


Fig. 12. Operation with External Clock

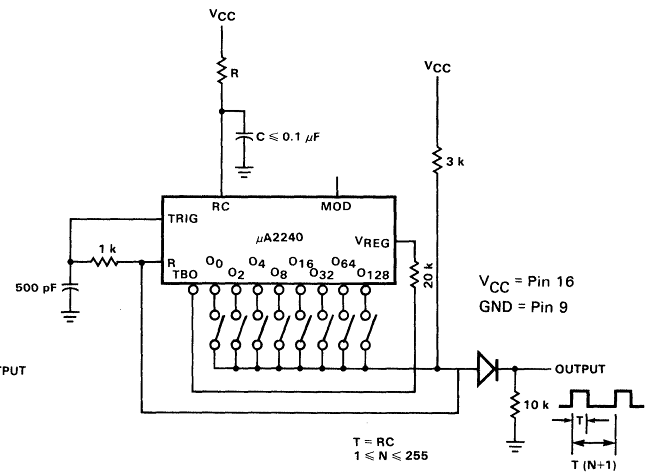


Fig. 13. Frequency Synthesis from Internal Time-Base

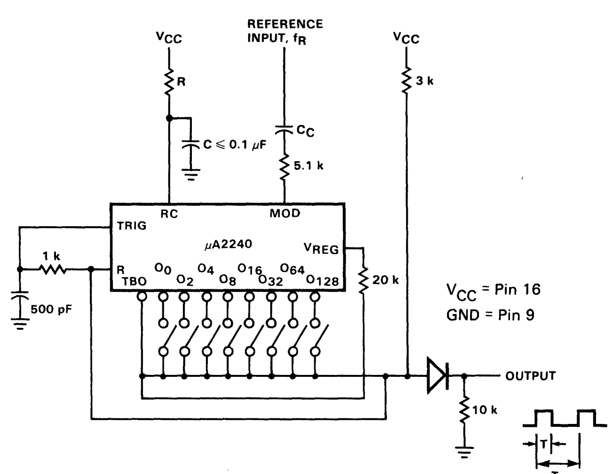


Fig. 14. Frequency Synthesis by Harmonic Locking to an External Reference

SYNTHESIS WITH HARMONIC LOCKING

The harmonic synchronization feature of the μA2240 time base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in *Figure 14* (see *Figures 4* and *5* for external sync waveform and harmonic capture range). If the time base is synchronized to (m)th harmonic of input frequency where $1 \leqslant m \leqslant 10$, the frequency f_O of the output waveform in *Figure 14* is related to the input reference frequency f_R as

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of *Figure 14* can produce 2550 different frequencies from a single fixed reference.

The circuit of *Figure 14* can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external RC to set m = 10 and setting N = 5, a 100 Hz output frequency synchronized to 60 Hz power line frequency can be obtained.

STAIRCASE GENERATOR

The μA2240 timer/counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator as shown in *Figure 15*. Under Reset condition, the output is LOW. When a trigger is applied, the op amp output goes HIGH and generates a negative-going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any level by applying a disable signal to pin 14, through a steering diode, as shown in *Figure 15*. The count is stopped when pin 14 is clamped at a voltage level $\leqslant$ 1.0 V.

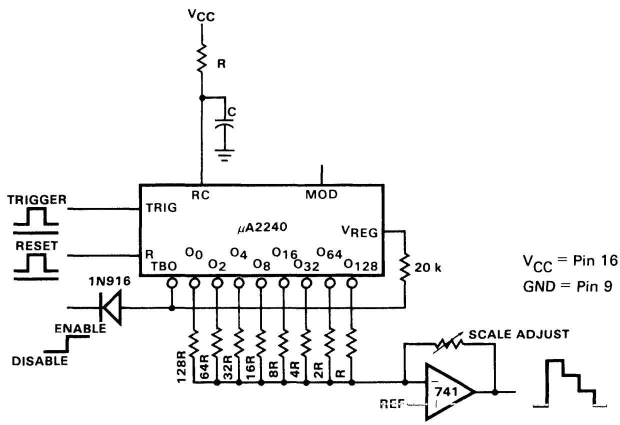


Fig. 15. Staircase Generator

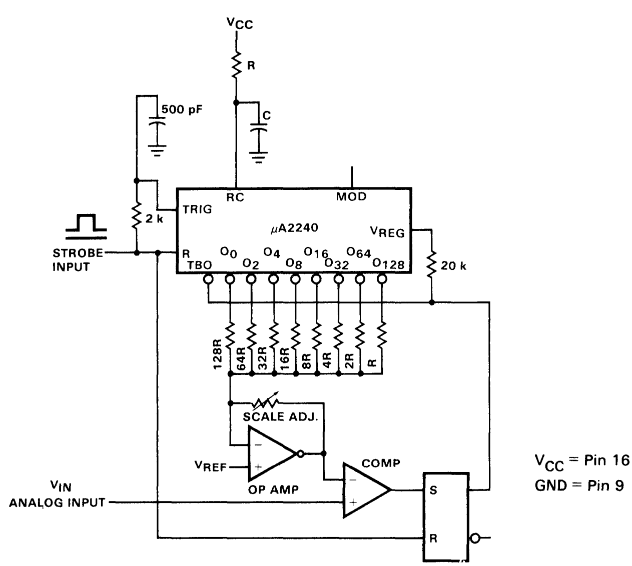


Fig. 16. Digital Sample and Hold Circuit

DIGITAL SAMPLE AND HOLD

Figure 16 shows a digital sample and hold circuit using the μA2240. Circuit operation is similar to the staircase generator described in the previous section. When a strobe input is applied, the RC low-pass network between the Reset and the Trigger inputs resets the timer, then triggers it. This strobe input also sets the output of the bistable latch to a HIGH state and activates the counter.

The circuit generates a staircase voltage at the op amp output. When the level of the staircase reaches that of the analog input to be sampled, the comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op amp output corresponds to the sampled analog input. Once the input is sampled, it is held until the next strobe signal. Minimum recycle time of the system is ≈ 6 ms.

ANALOG-TO-DIGITAL CONVERTER

Figure 17 shows a simple 8-bit A/D converter system using the μA2240. Circuit operation is very similar to that of the digital sample and hold system of *Figure 16*. In the case of A/D conversion, the digital output is obtained in parallel format from the binary-counter outputs with the output at pin 8 corresponding to the most significant bit (MSB). Recycle time is ≈ 6 ms.

DIGITAL TACHOMETER TIME BASE

A digital tachometer requires a time-base generator to supply two pulse outputs at specific intervals, *e.g.*, every second. The first pulse is a command (load) to transfer the accumulated counts in the counter section into latches (memory); the second resets the counter to zero. A simple adjustable time base, accurate to approximately ±0.5%, can be implemented using the circuit in *Figure 18*.

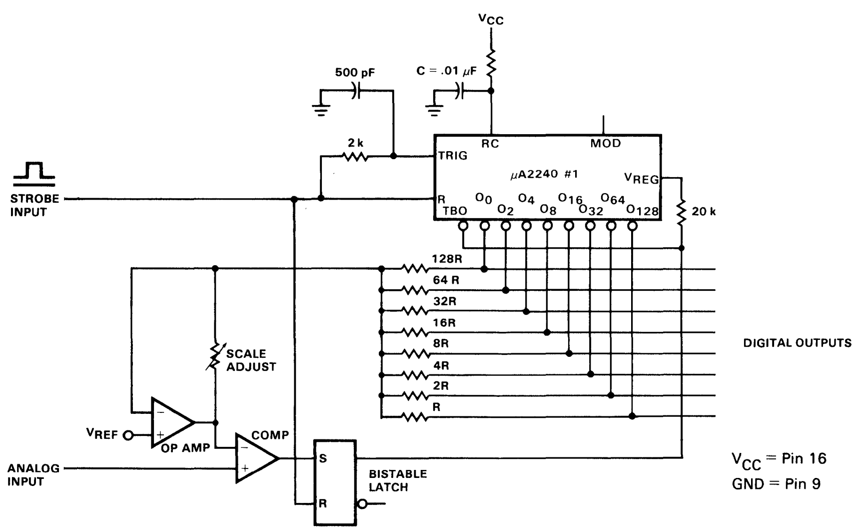


Fig. 17. Analog-to-Digital Converter

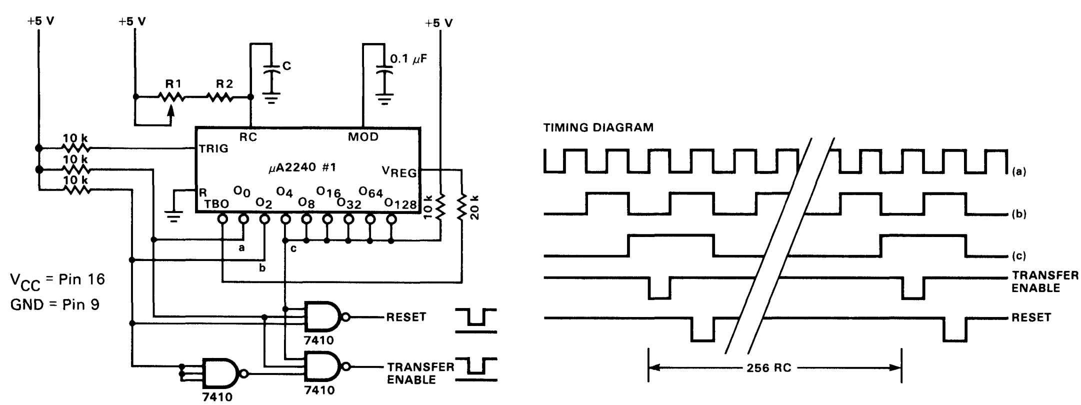


Fig. 18. Simple Time Generator for a Digital Tachometer

TYPICAL ELECTRICAL CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE IN RESET CONDITION

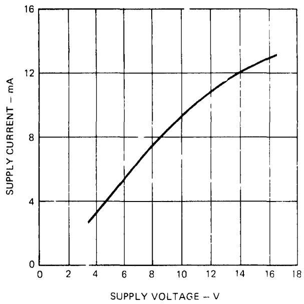


Fig. 19

RECOMMENDED RANGE OF TIMING COMPONENT VALUES

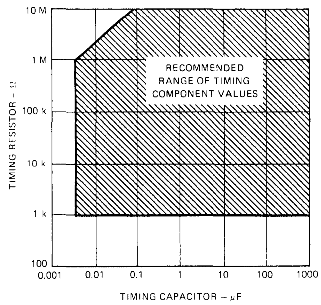


Fig. 20

TIME BASE PERIOD AS A FUNCTION OF EXTERNAL RC

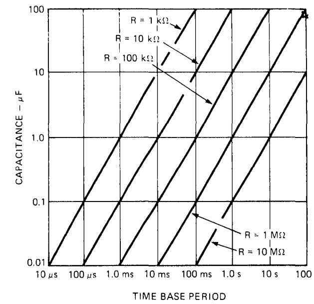


Fig. 21

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AND RESET AMPLITUDE

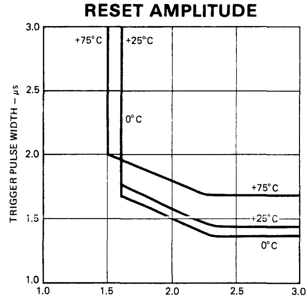


Fig. 22

TIME BASE PERIOD DRIFT AS A FUNCTION OF SUPPLY VOLTAGE

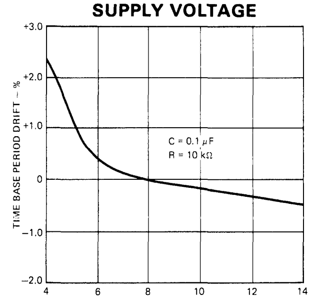


Fig. 23

MINIMUM TRIGGER/RETRIGGER TIMING AS A FUNCTION OF TIMING CAPACITOR

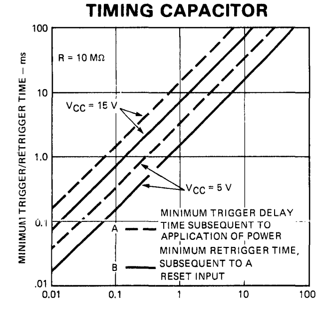


Fig. 24

NORMALIZED CHANGE IN TIME BASE PERIOD AS A FUNCTION OF MODULATION VOLTAGE

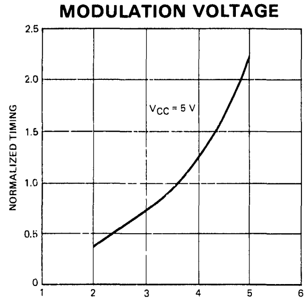


Fig. 25

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

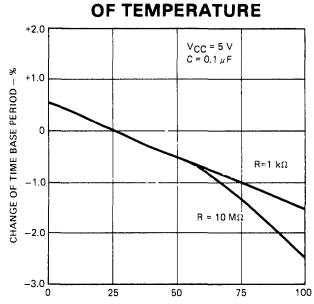


Fig. 26

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

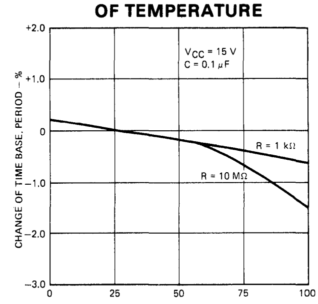


Fig. 27

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TEST CIRCUITS

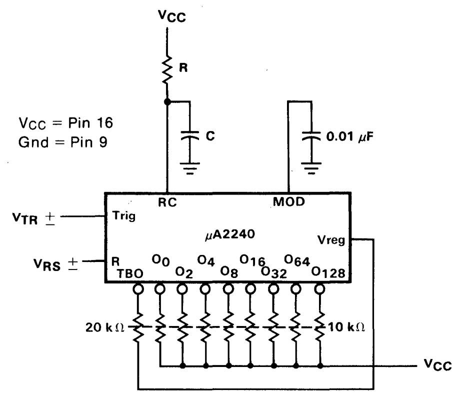


Fig. 28. Generalized Test Circuit

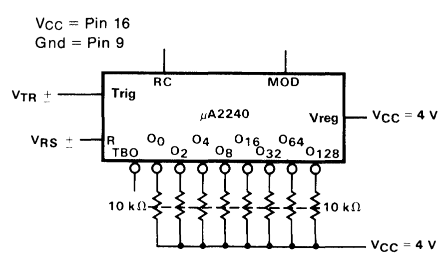


Fig. 29. Test Circuit for Low Power Operation (Time Base Powered Down)

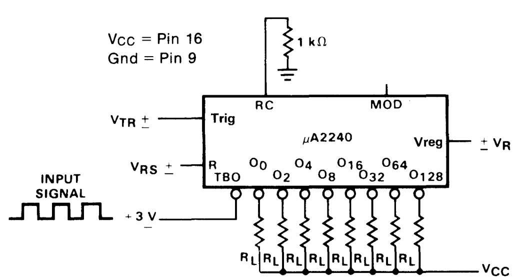


Fig. 30. Test Circuit for Counter Section

μA703

RF-IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

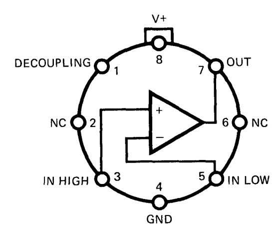
GENERAL DESCRIPTION – The μA703 is a monolithic RF-IF Amplifier constructed using the Fairchild Planar* epitaxial process and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

- **29 mmho MINIMUM FORWARD TRANSADMITTANCE**
- **1.0 mmho/0.05 mmho MAXIMUM INPUT/OUTPUT CONDUCTANCE**
- **18 pF/4.0 pF MAXIMUM INPUT/OUTPUT CAPACITANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation	200 mW
Operating Temperature Range (μA703)	−55°C to +125°C
Operating Temperature Range (μA703C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	300°C

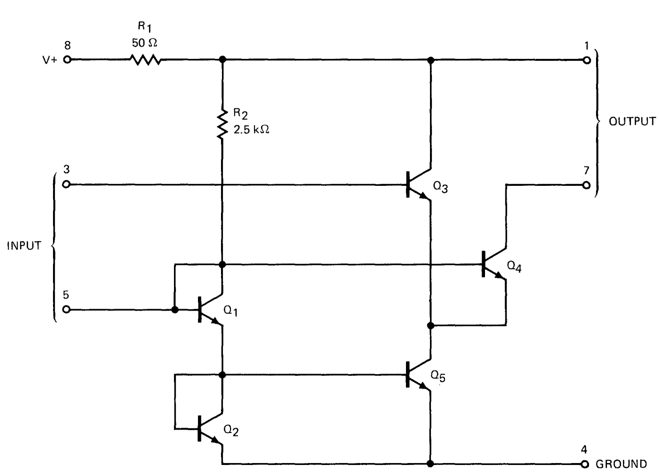
CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5C
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA703	μA703HM
μA703C	μA703HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA703

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_+ = 12 V unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption	$e_{IN} = 0$		110	170	mW
Quiescent Output Current	$e_{IN} = 0$	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	e_{IN} = 400 mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{IN} = 10 mV rms f ≤ 1 kHz	29	35		mmbo
Input Conductance	e_{IN} < 10 mV rms, f ≤ 5 MHz		0.30	0.43	mmbo
Input Capacitance	e_{IN} < 10 mV rms, f ≤ 5 MHz		7.0	16.0	pF
Output Capacitance	f ≤ 5 MHz		2.0	3.0	pF
Output Conductance	e_O ≤ 100mV rms, f ≤ 5 MHz		0.02	0.04	mmbo
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Quiescent Output Current	$e_{IN} = 0$	1.7		3.1	mA
Peak-to-Peak Output Current	e_{IN} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{IN} = 10 mV rms, f ≤ 1 kHz	21			mmbo
Input Conductance	e_{IN} < 10 mV rms, f ≤ 5 MHz			1.2	mmbo
Output Conductance	e_O ≤ 100 mV rms, f ≤ 5 MHz			0.05	mmbo

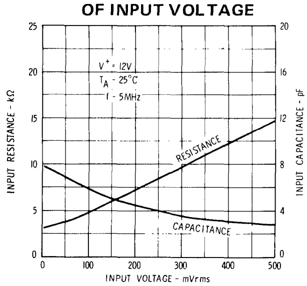
μA703C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_+ = 12 V unless otherwise specified)

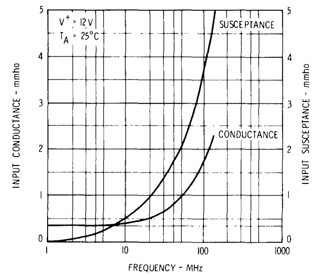
CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_{IN} = 0$		9.0	14	mA
Power Consumption	$e_{IN} = 0$		110	170	mW
Quiescent Output Current	$e_{IN} = 0$	1.5	2.5	3.3	mA
Peak-to-Peak Output Current	e_{IN} = 400 mV_{rms}, f = 1 kHz	3.0			mA
Output Saturation Voltage	I_7 = 2.5 mA			1.7	V
Forward Transadmittance	e_{IN} = 10 mV_{rms}, f = 1 kHz	29	33		mmho
Input Conductance	e_{IN} < 10 mV_{rms}, f = 10.7 MHz		0.35	1.0	mmho
Input Capacitance	e_{IN} < 10 mV_{rms}, f = 10.7 MHz		9.0	18	pF
Output Conductance	e_{OUT} = 100 mV_{rms}, f = 10.7 MHz		0.03	0.05	mmho
Output Capacitance	e_{OUT} = 100 mV_{rms}, f = 10.7 MHz		2.0	4.0	pF
Noise Figure	f = 10.7 MHz, R_S = 500 Ω		6.0		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB

TYPICAL PERFORMANCE CURVES FOR μA703

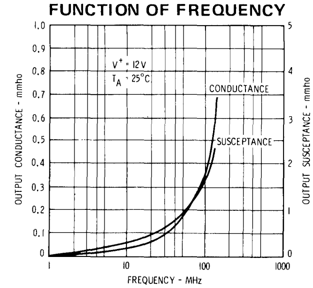
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



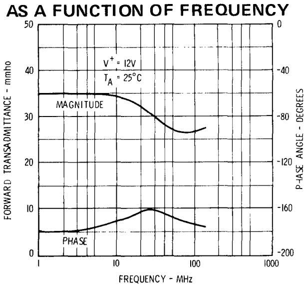
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



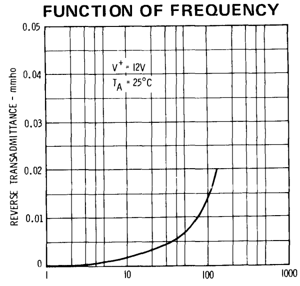
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



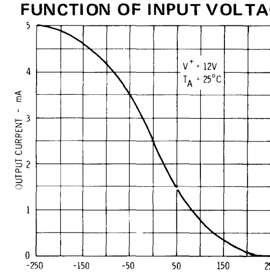
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



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μA706

5-WATT AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA706 monolithic 5.0 W Audio Amplifier is constructed using the Fairchild Planar* epitaxial process. It is ideally suited as an audio amplifier in automobile radios. Provided with adequate heat sinking, the circuit is optimized to provide 5.5 W (continuous output) into a 4.0 Ω speaker using a single 14 V supply. The circuit operates over the full automobile battery range of 6.0 V to 16 V. The μA706 incorporates such special features as self-centering bias, direct coupling to the input, low quiescent current, high input impedance and low distortion. Operation as a 5.0 W audio amplifier is achieved with minimal external components.

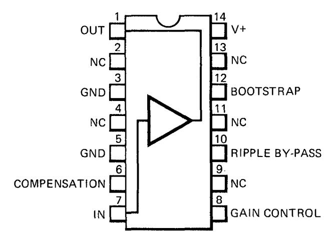
Other applications for the μA706 are home audio equipment, TV receivers and many industrial applications.

- **OUTPUT POWER 5.5 W (14 V – 4 Ω)**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**
- **HIGH PEAK OUTPUT CURRENT**
- **HIGH IMMUNITY TO DAMAGE FROM SHORT-CIRCUITED LOAD†**
- **PIN-FOR-PIN REPLACEMENT FOR TBA641B**

†The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

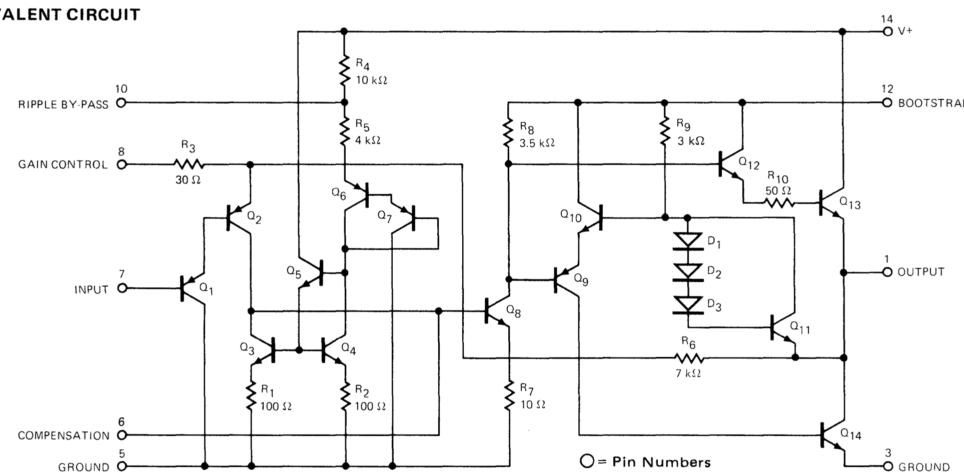
PACKAGE OUTLINES 9H 9J
PACAKGE CODES AP BP



ORDER INFORMATION

TYPE	PART NO.
μA706AC	μA706APC
μA706BC	μA706BPC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (No Signal)	25 V
Supply Voltage	16 V
Input Voltage	−0.5 V to V^+
Peak Output Current	2.5 A
Operating Temperature Range	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_C \leqslant 85°C$)	5 W
Power Dissipation ($T_A \leqslant 25°C$)	
Package Type AP	1.7 W
Package Type BP	2.3 W
Power Dissipation ($T_A \leqslant 85°C$)	
Package Type AP	0.9 W
Package Type BP	1.2 W

PACKAGE THERMAL RESISTANCE

Thermal Resistance, Junction to Ambient	
Package Type AP	73°C/W
Package Type BP	55°C/W
Thermal Resistance, Junction to Case	
Package Type AP	11°C/W
Package Type BP	12°C/W

μA706C

ELECTRICAL CHARACTERISTICS: $V_+ = 14V$, $R_L = 4\ \Omega$, $T_A = 25°C$, $\theta_{C-A} = 13°C/W$, Test Circuit 1, unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	$P_{OUT} = 0$	10	18	30	mA
Quiescent Current in Output Transistors	$P_{OUT} = 0$	7	15	27	mA
Input Bias Current			200	950	nA
DC Output Level	$R_S = 22\ k\Omega$	6.55	7.0	7.45	V
Voltage Gain, A_V	$R_B = 0\ \Omega$	43	46	49	dB
Output Power, P_{OUT}	THD = 10%, f = 1 kHz, A_V = 46 dB	4.5	5.5		W
Total Harmonic Distortion	f = 1 kHz, A_V = 46 dB				
	P_{OUT} = 50 mW		0.3		%
	P_{OUT} = 2.0 W		0.5		%
	P_{OUT} = 4.5 W		3.0		%
Equivalent Input Noise Voltage	$R_S = 22\ k\Omega$, B.W. = 10 kHz		3.5		μV
Total Supply Current	P_{OUT} = 4.5 W		510		mA
Input Impedance	A_V = 46 dB, f = 1 kHz		3.0		MΩ

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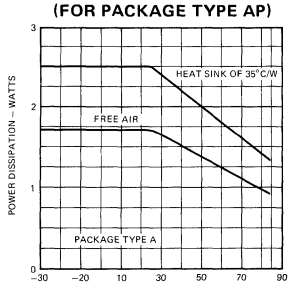
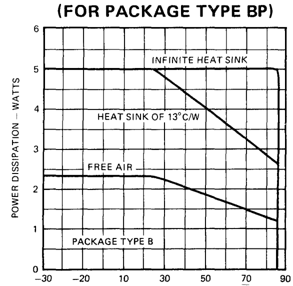
TYPICAL PERFORMANCE CURVES FOR μA706C

($T_A = 25°C$, $\theta_{C-A} = 13°C/W$, Test Circuit 1, $A_V = 46$ dB)

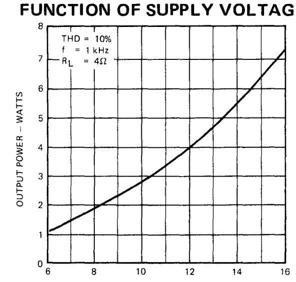
MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE AP)



MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE BP)

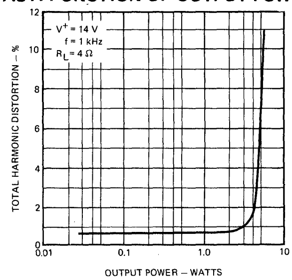


OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

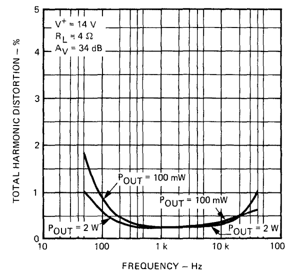


TYPICAL PERFORMANCE CURVES FOR µA706C (Cont'd)

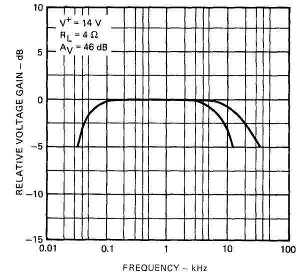
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



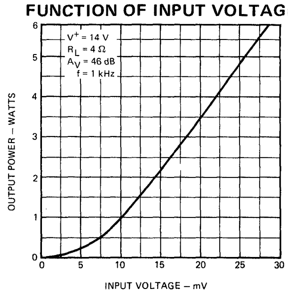
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



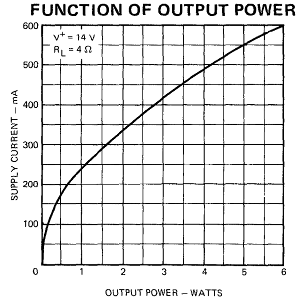
RELATIVE VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



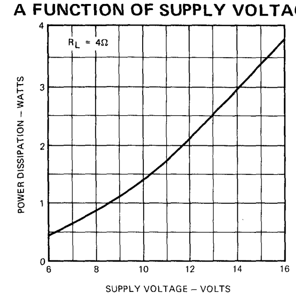
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



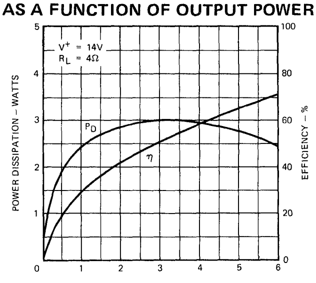
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



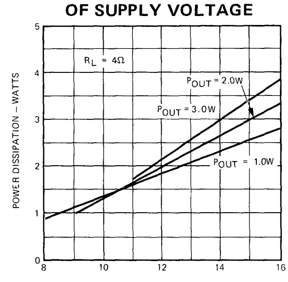
MAXIMUM POWER DISSIPATION BY THE INTEGRATED CIRCUIT AS A FUNCTION OF SUPPLY VOLTAGE



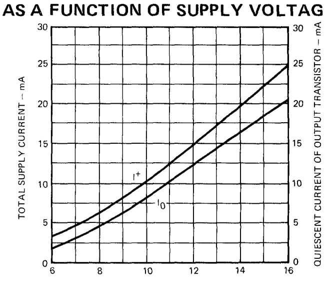
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



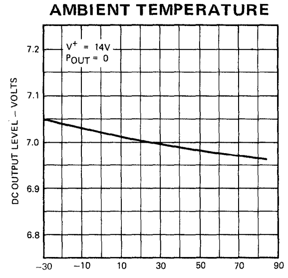
POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



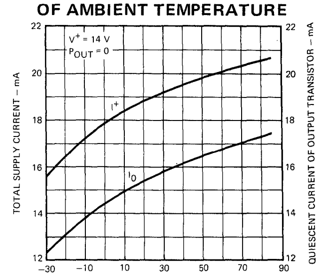
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF SUPPLY VOLTAGE



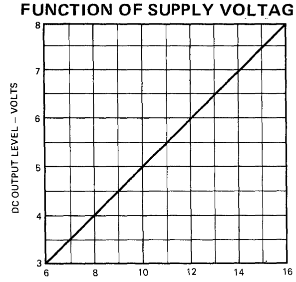
DC OUTPUT LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



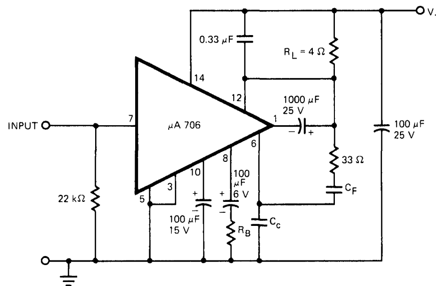
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



DC OUTPUT LEVEL AS A FUNCTION OF SUPPLY VOLTAGE

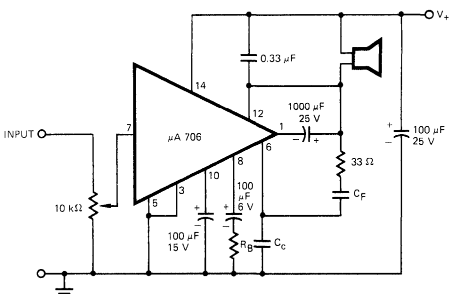


TEST CIRCUIT 1 (A_V = 46 dB, R_B = 0 Ω, C_c = 1.5 nF, C_F = 150 pF)



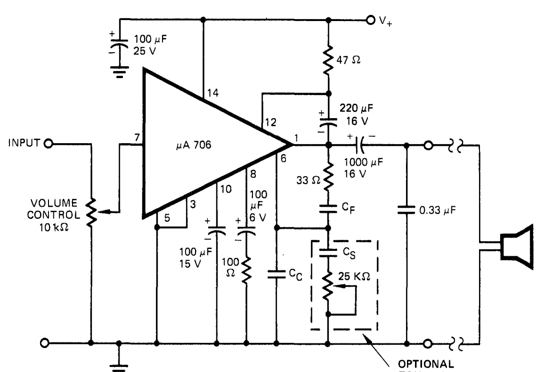
TYPICAL AUDIO APPLICATIONS

5 WATT AUDIO AMPLIFIER WITH MINIMUM COMPONENT COUNT



A_V	34 dB		46 dB	
BW	10 kHz	20 kHz	10 kHz	20 kHz
R_B	100 Ω	100 Ω	0 Ω	0 Ω
C_c	10 nF	6.8 nF	2.7 nF	1.5 nF
C_F	1 nF	470 pF	330 pF	150 pF

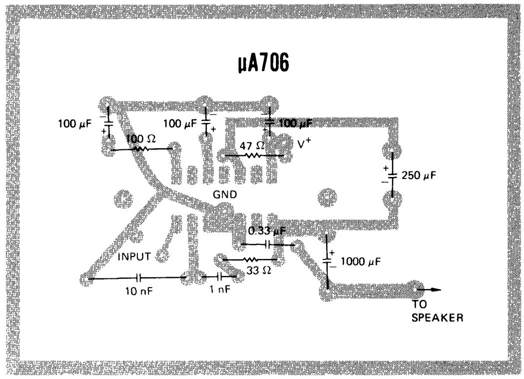
5 WATT AUDIO AMPLIFIER WITH LOAD CONNECTED TO GROUND



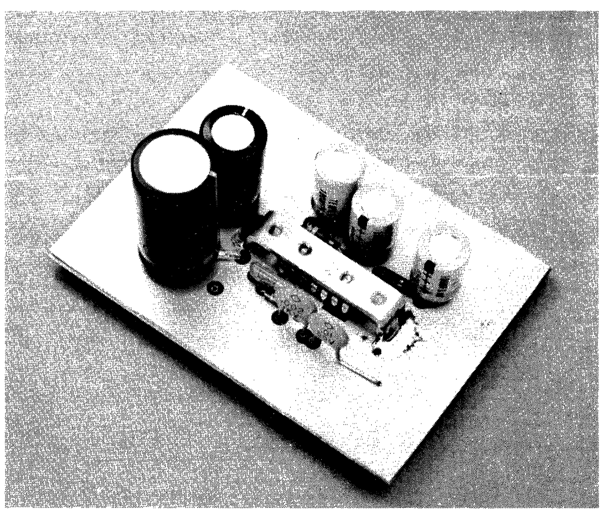
A_V	34 dB	46 dB
C_S	27 nF	5.6 nF

Note: C_S selected for 3 dB at 4 kHz.

A PC BOARD LAYOUT FOR THE 5 WATT AUDIO AMPLIFIER



PHOTOGRAPH OF THE μA706 IN A TYPICAL APPLICATION



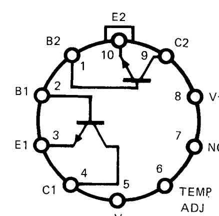
μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA726 is a Monolithic Transistor Pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers. It is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

CONNECTION DIAGRAM
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5U
PACKAGE CODE H



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (μA726)	–55°C to +125°C
Commercial (μA726C)	0°C to +85°C
Storage Temperature Range	–65°C to +150°C
Pin Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V
Internal Power Dissipation	500 mW

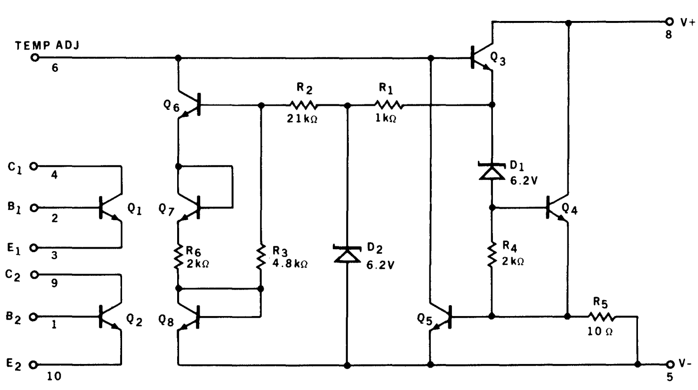
MAXIMUM RATINGS FOR EACH TRANSISTOR

Collector-to-Emitter Voltage, V_{CEO}	30V
Collector-to-Base Voltage, V_{CBO}	40V
Collector-to-Substrate Voltage, V_{CIO}	40V
Emitter-to-Base Voltage, V_{EBO}	5V
Collector Current, I_C	5 mA

ORDER INFORMATION

TYPE	PART NO.
μA726	μA726HM
μA726C	μA726HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA726

ELECTRICAL CHARACTERISTICS: $-55°C \leq T_A \leq +125°C$, $V_S = \pm15V$, $R_{adj} = 62k\Omega$ unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	50	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	200	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	150	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	500	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10kHz		10		μV p-p
Long-term Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20MHz, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

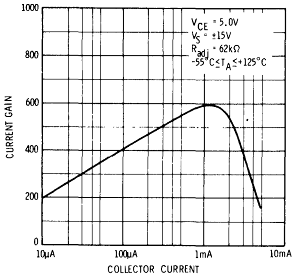
μA726C

ELECTRICAL CHARACTERISTICS: $0°C \leq T_A \leq +85°C$, $V_S = \pm15V$, $R_{adj} = 75k\Omega$ unless otherwise specified.

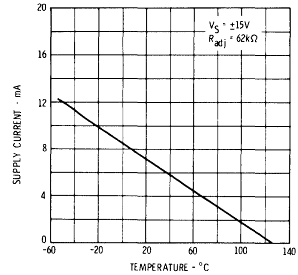
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	100	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	300	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\mu A$, $R_S = 50\Omega$		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10kHz		10		μV p-p
Long-Term Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20MHz, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

TYPICAL PERFORMANCE CURVES FOR μA726

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

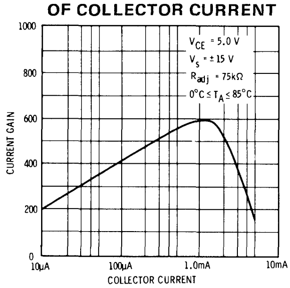


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

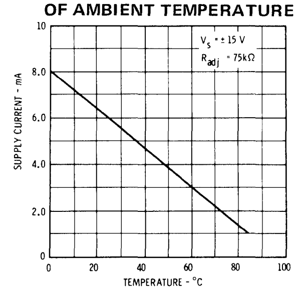


TYPICAL PERFORMANCE CURVES FOR μA726C

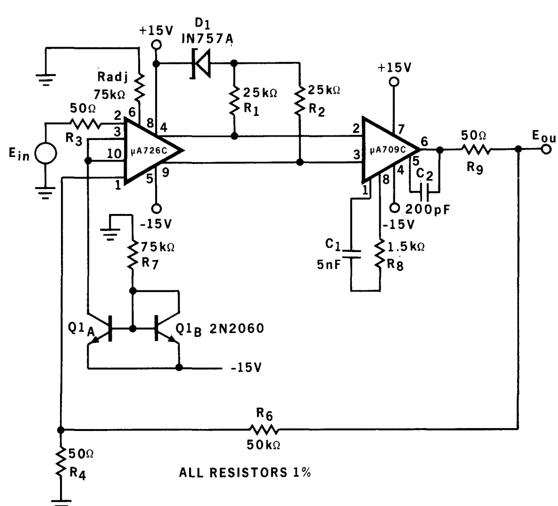
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 AMPLIFIER CIRCUIT



μA727

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

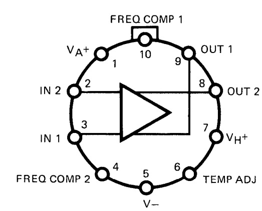
GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, Differential Input/Output Preamplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low drift dc amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gauge transducers, and A/D converters.

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE — 300 MΩ**
- **WIDE COMMON MODE RANGE — C_{MRR} = 100 dB**

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (μA727)	−55°C to +125°C
Commercial (μA727C)	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 s time limit)	300°C
Internal Power Dissipation	500 mW
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

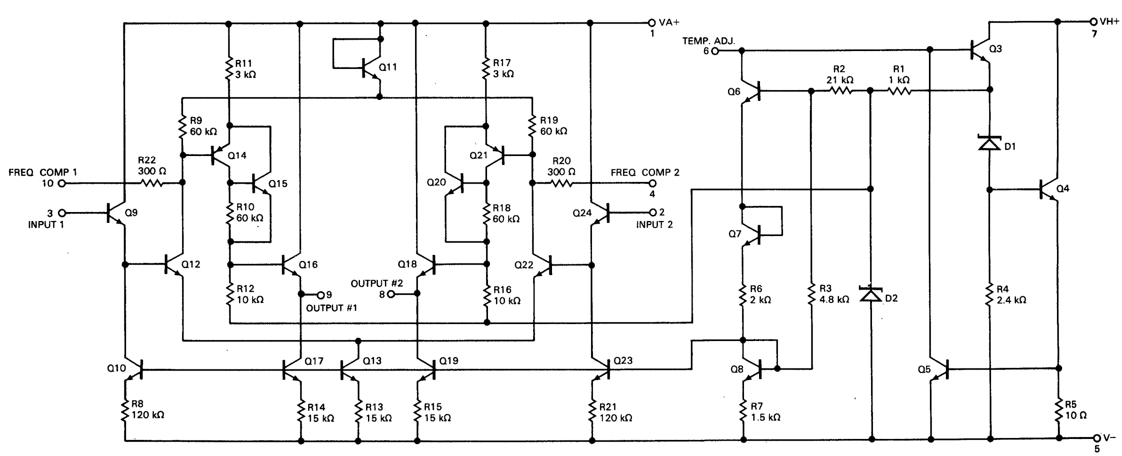
CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5I
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA727	μA727HM
μA727C	μA727HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA727

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_H+ = V_A+ = +15$ V, $V- = -15$ V, $R_{ADJ} = 330$ kΩ, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		± 5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

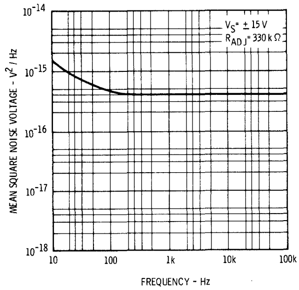
μA727C

ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H+ = V_A+ = +15$ V, $V- = -15$ V, $R_{ADJ} = 1$ MΩ, unless otherwise specified)

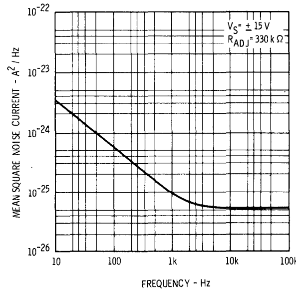
PARAMETER	CONDITONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL PERFORMANCE CURVES FOR μA727 AND μA727C

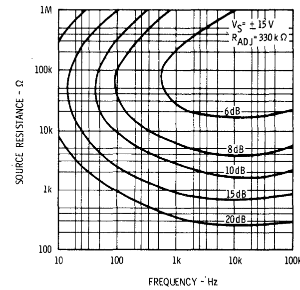
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



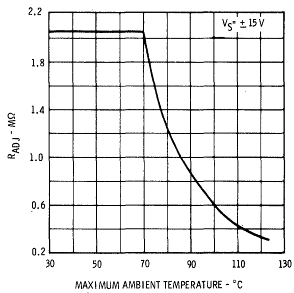
NOISE CURRENT AS A FUNCTION OF FREQUENCY



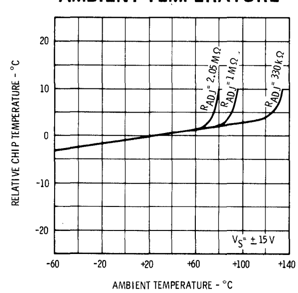
SPOT NOISE CONTOURS



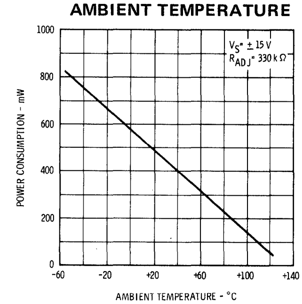
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



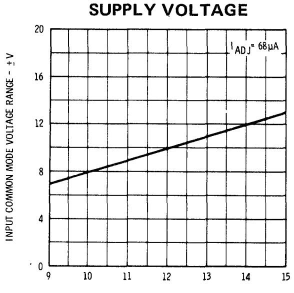
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



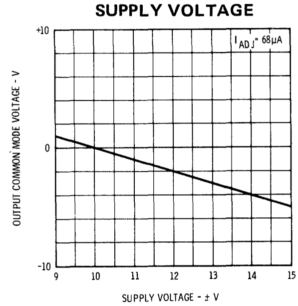
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



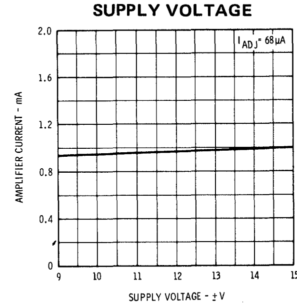
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



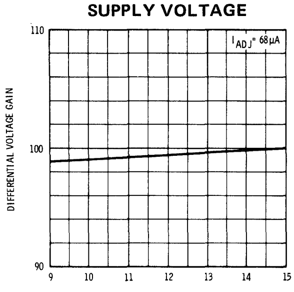
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



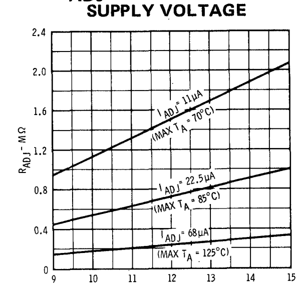
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



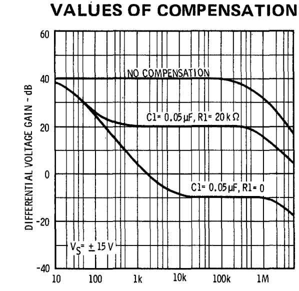
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



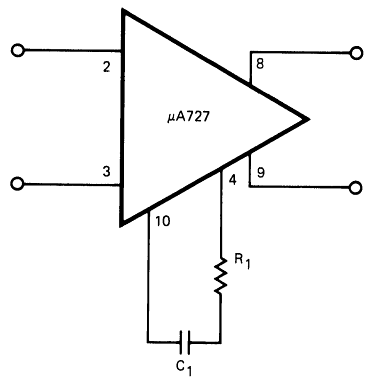
REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE



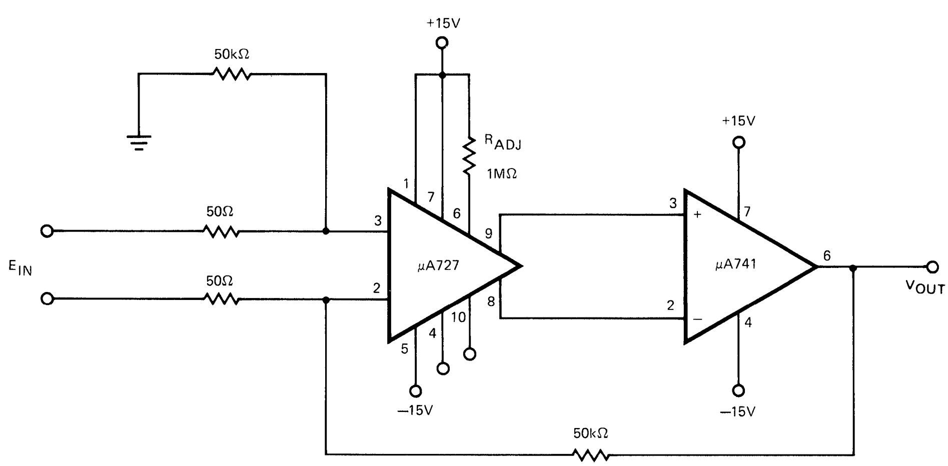
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY COMPENSATION CIRCUIT



TYPICAL X1000 CIRCUIT



μA733

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

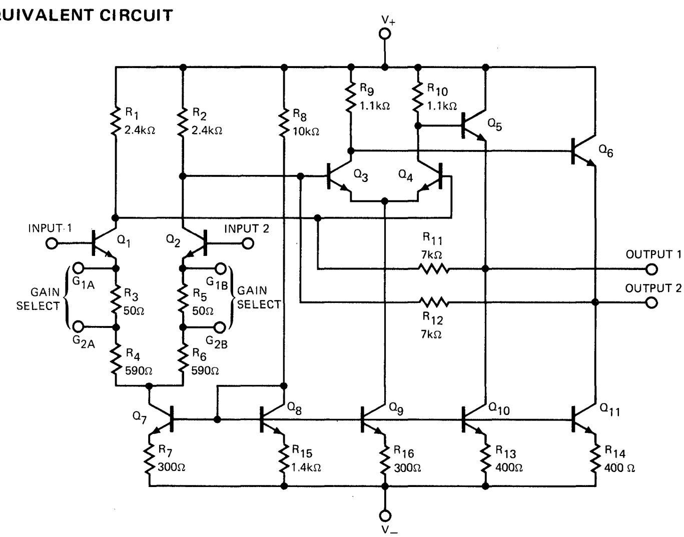
GENERAL DESCRIPTION — The μA733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range	
Military (μA733)	−55° C to +125° C
Commercial (μA733C)	0° C to +70° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 second time limit)	300° C

EQUIVALENT CIRCUIT



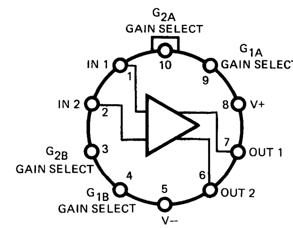
Notes on following pages.

CONNECTION DIAGRAMS

10-LEAD METAL CAN

(TOP VIEW)

PACKAGE OUTLINE 5N
PACKAGE CODE H



Note: Pin 5 connected to case.

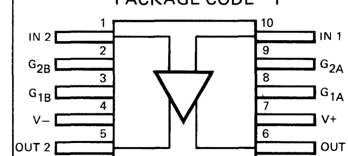
ORDER INFORMATION

TYPE	PART NO.
μA733	μA733HM
μA733C	μA733HC

10-LEAD FLATPAK

(TOP VIEW)

PACKAGE OUTLINE 3F
PACKAGE CODE F



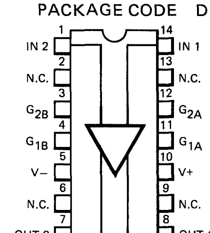
ORDER INFORMATION

TYPE	PART NO.
μA733	μA733FM

14-LEAD DIP

(TOP VIEW)

PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA733	μA733DM
μA733C	μA733DC

*Planar is a patented Fairchild process.

μA733

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

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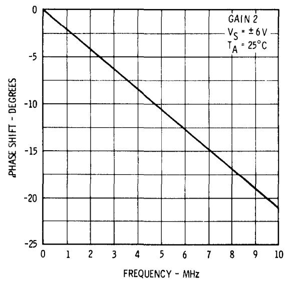
μA733C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

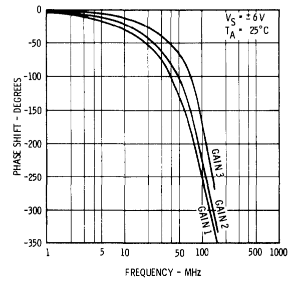
PARAMETER (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for 0°C ≤ T_A ≤ ±70°C					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{p-p}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

TYPICAL PERFORMANCE CURVES FOR μA733 AND μA733C

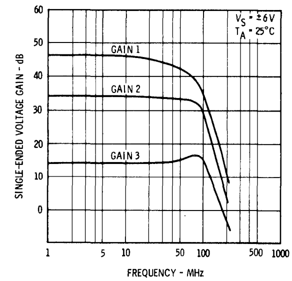
PHASE SHIFT AS A FUNCTION OF FREQUENCY



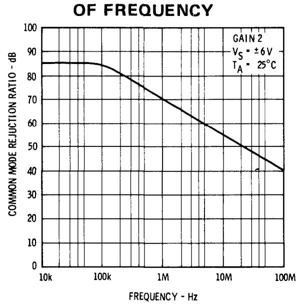
PHASE SHIFT AS A FUNCTION OF FREQUENCY



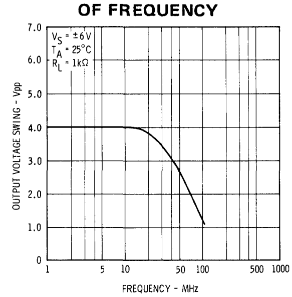
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



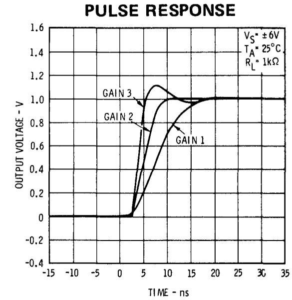
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



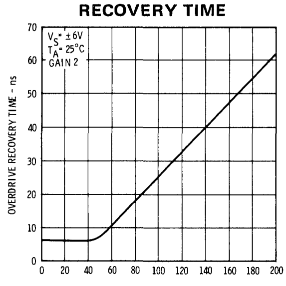
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



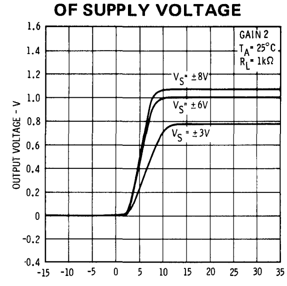
PULSE RESPONSE



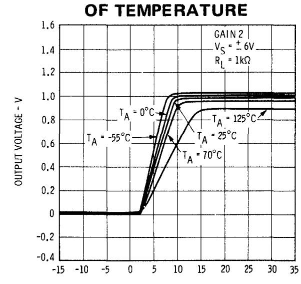
DIFFERENTIAL OVERDRIVE RECOVERY TIME



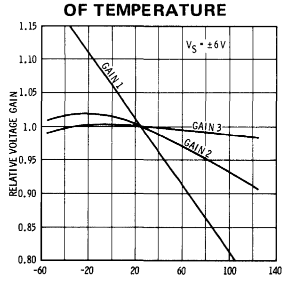
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



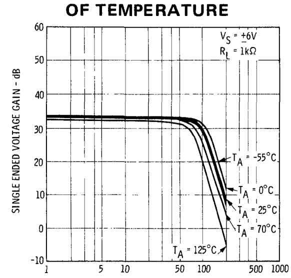
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



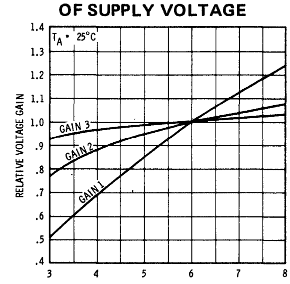
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



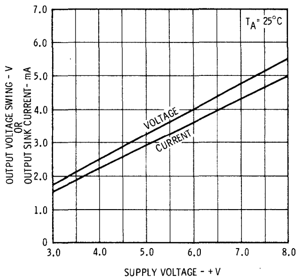
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



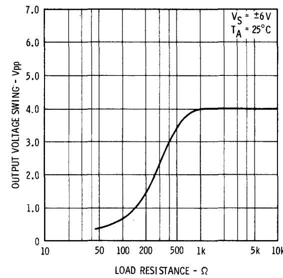
7

TYPICAL PERFORMANCE CURVES FOR μA733 AND μA733C

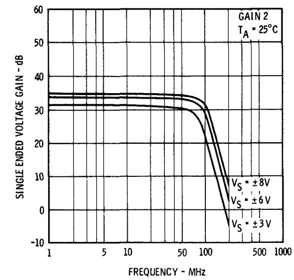
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



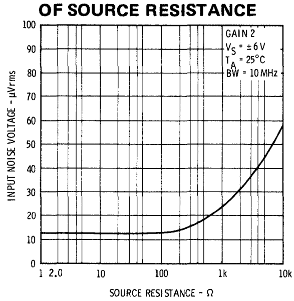
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



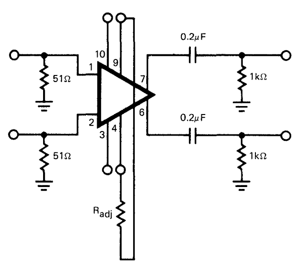
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



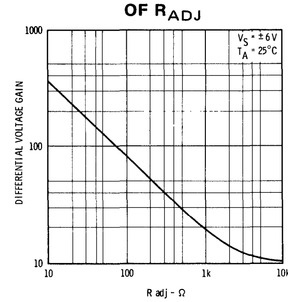
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



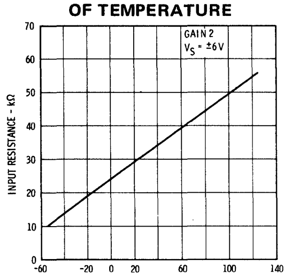
VOLTAGE GAIN ADJUST CIRCUIT



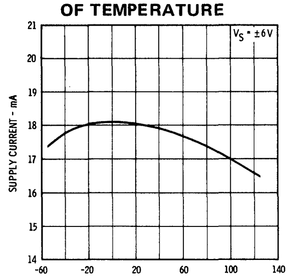
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



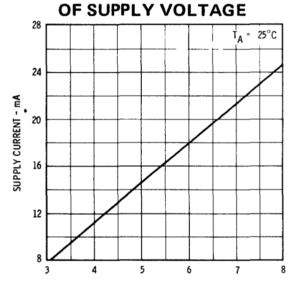
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

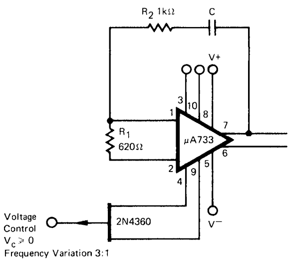


NOTES

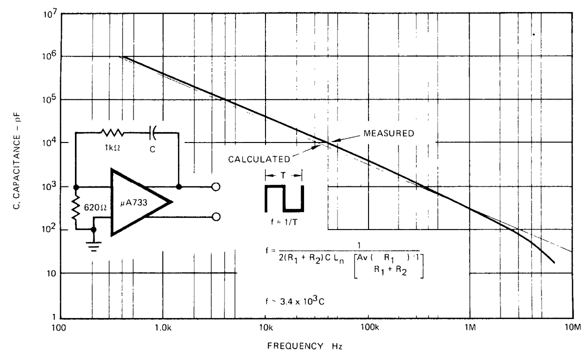
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

TYPICAL APPLICATIONS

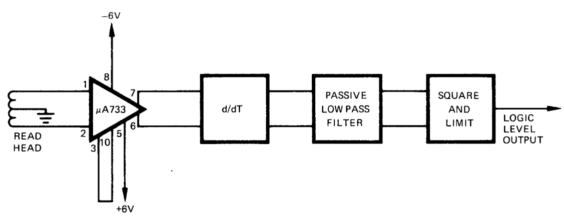
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



PHASE ENCODING PLAYBACK SYSTEM



Phase Linearity:	±4° from 2 to 5 MHz
Input Resistance:	30 kΩ
Input Capacity:	2 pF
Fixed Gain:	100

7

μA742

ZERO-CROSSING AC TRIGGER-TRIGAC

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA742 is a monolithic Zero-Crossing AC Trigger (TRIGAC) utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in ac power control circuits for operation directly off the ac line or with a separate ac or dc power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's. As a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads

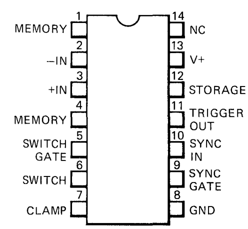
- **DESIGNED FOR APPLICATIONS IN 60Hz TO 400 Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS**
- **OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY**
- **INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES**
- **BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS**
- **PROVISIONS FOR TIME PROPORTIONING OPERATION**
- **PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI**
- **EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERINGS FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS**

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (ac Operation)	±30 mA
Continuous Current into Supply Terminal (dc Operation)	20 mA
RMS Current into Sync Input Terminal	15 mA
Current into Switch Terminal	10 mA
Power Dissipation	670 mW
Voltage at (+) or (–) Input Terminal	(Note 1)
Differential Voltage between (+) and (–) Input Terminals	±7V
Current into Clamp Terminal (Clamp ON)	20 mA
Voltage at Clamp Terminal (Clamp OFF)	25V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

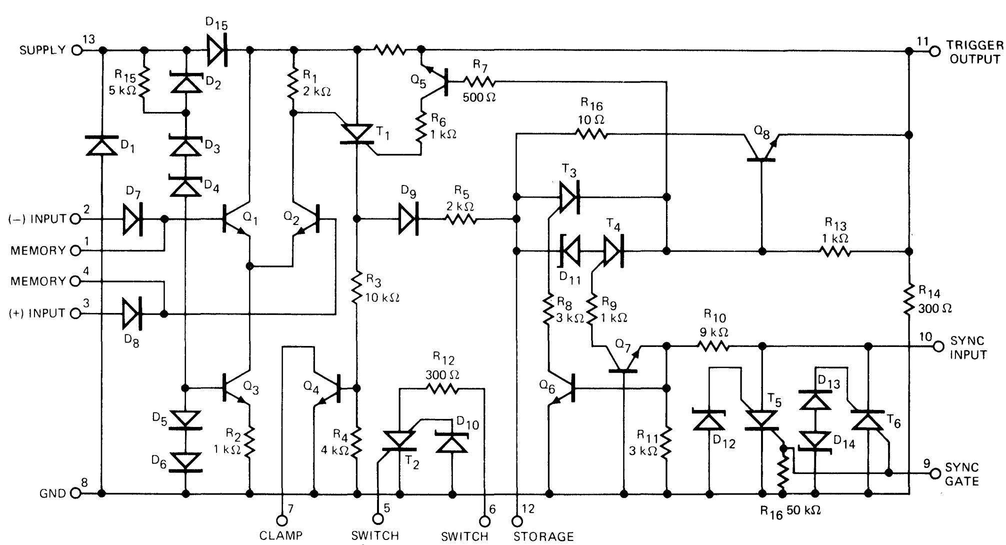
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA742C	μA742PC
μA742C	μA742DC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchild process.

μA742C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, Voltage Range at the (+) and (–) Input Terminals 2.5V to 17V; $V_{(+)\ Input} - V_{(-)\ Input} \geq$ 50mV, Test Circuit 1, unless otherwise specified.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Peak Supply Voltage	S_1 in dc position	19	21	26	V
	S_1 in ac position, positive half cycles of ac line	19	21	26	V
	S_1 in ac position, negative half cycle of ac line	-1.6	-0.95	-0.8	V
Peak Trigger Output Pulse	S_1 in ac position, beginning of positive half cycles	0.6	0.9		A
	S_1 in ac or dc position, beginning of negative half cycles	1.0	1.3		A
	S_1 in dc position beginning of positive half cycles	1.6	2.0		A
Bias Current at (+) and (–) Terminals			15	25	μA
Input Threshold Voltage for Output Pulse Enable		-50	-35	50	mV
ON Voltage at Clamp Terminal	I_7 = 1 mA		85	200	mV
ON Voltage at Switch Terminal	I_6 = 5 mA		2.6	3.0	V
Switching Voltage at Switch Terminal		6.0	7.2		V
Switching Current at Switch Terminal			15		μA
Holding Current at Switch Terminal			23	200	μA
ON Voltage at Sync Input Terminal	I_{10} = 10 mA		1.9	2.2	V
	I_{10} = -10 mA	-2.2	-1.9		V
Switching Voltage at Sync Input Terminal	I_{10} = 2 mA, positive half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV	4.5	5.8		V
	I_{10} = -2 mA, negative half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV		-7.0	-4.5	V
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles	180	410	500	μA
	Beginning of negative half cycles	-500	-280	-180	μA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles	2.0	2.7	4.0	V
	Beginning of negative half cycles	-4.0	-3.3	-2.0	V

DEFINITIONS

VOLTAGE RANGE: The range of voltage on the (+) or (–) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.
BIAS CURRENT: The average of the two currents into the (+) and (–) input terminals.

NOTES:
(1) The maximum voltage should not exceed the instantaneous supply voltage of the μA742.
(2) Rating applies for an external storage capacitor having a value of not more than 2μF.

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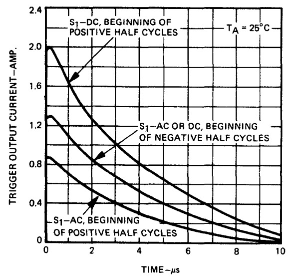
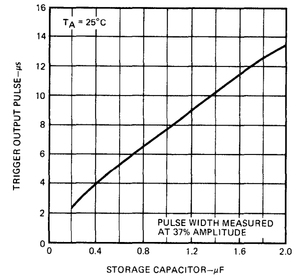
TYPICAL PERFORMANCE CURVES FOR μA742C
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

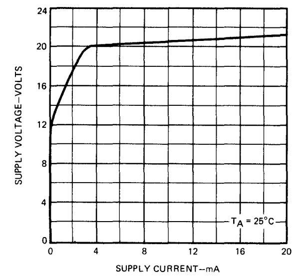
TRIGGER OUTPUT PULSE WAVE FORMS



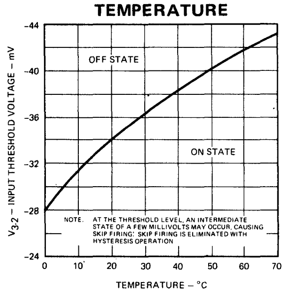
TRIGGER OUTPUT PULSE WIDTH AS A FUNCTION OF STORAGE CAPACITOR



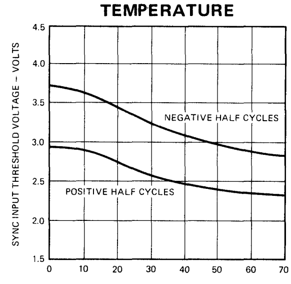
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



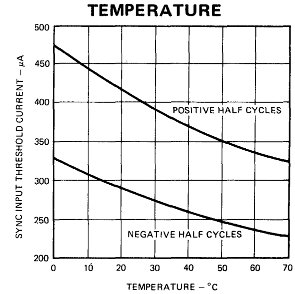
INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



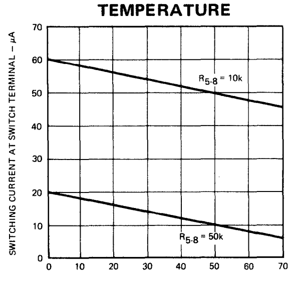
SYNC INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



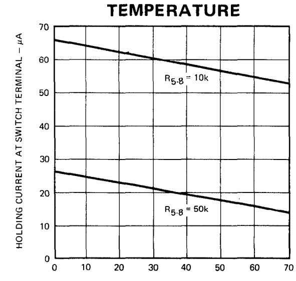
SYNC INPUT THRESHOLD CURRENT AS A FUNCTION OF TEMPERATURE



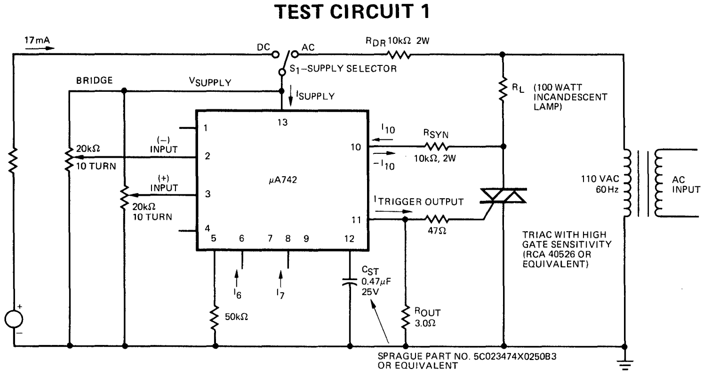
SWITCHING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



HOLDING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



TEST CIRCUIT 1



TYPICAL APPLICATIONS FOR μA742C

NOTES

*Recommended Values

AC Supply Voltage 60 Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0 kΩ	2.2 kΩ	0.47 μF/25V
110	10 kΩ	10 kΩ	0.47 μF/25V
220	22 kΩ	22 kΩ	0.47 μF/25V

FOR SUPPLY VOLTAGE FREQUENCY OF 400 Hz REDUCE C_{ST} TO .047 μF/25 V.

**Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5 mA at 20 V.

ZERO CROSSING CIRCUIT WITH DC SUPPLY

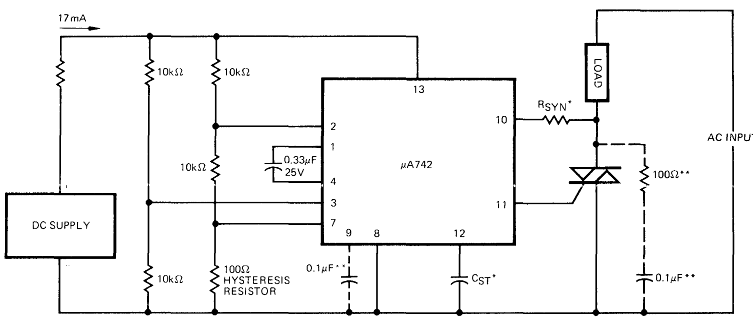


Fig. 1

ZERO CROSSING CIRCUIT

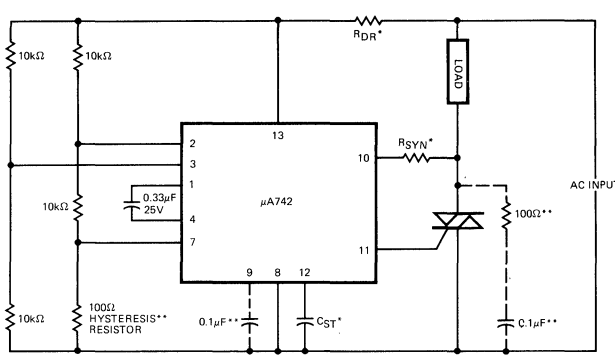


Fig. 2

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

SCR – HALF WAVE

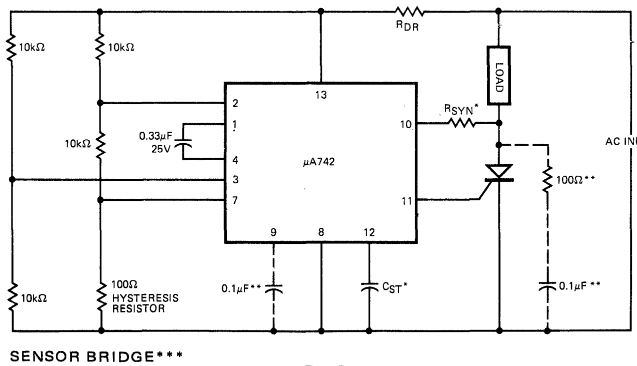


Fig. 3

INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER

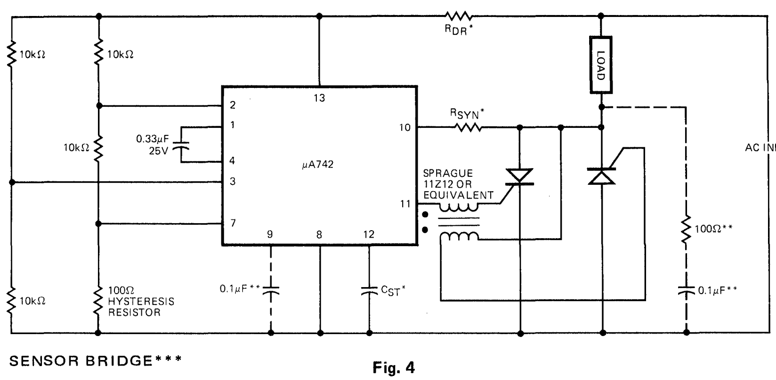


Fig. 4

INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR

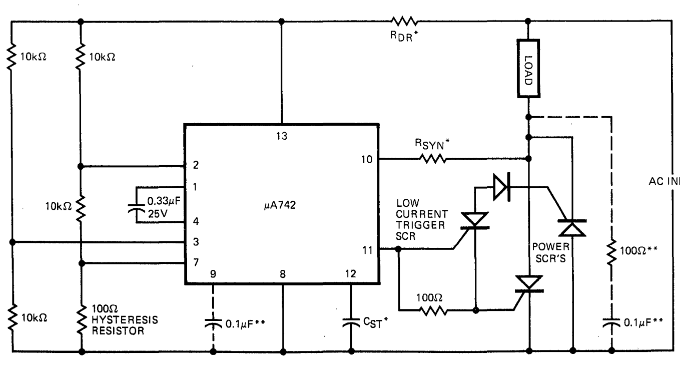


Fig. 5

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

ZERO CROSSING WITH PROPORTIONAL CONTROL

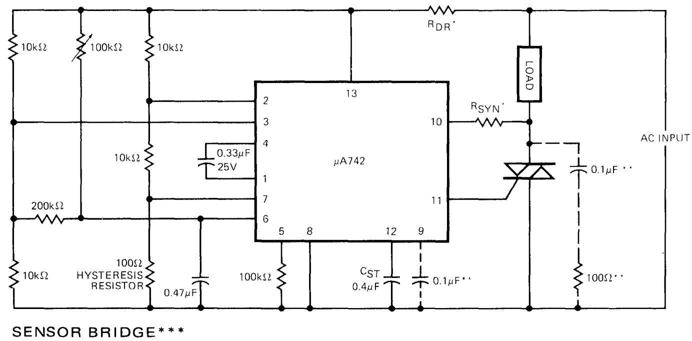


Fig. 6

ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS

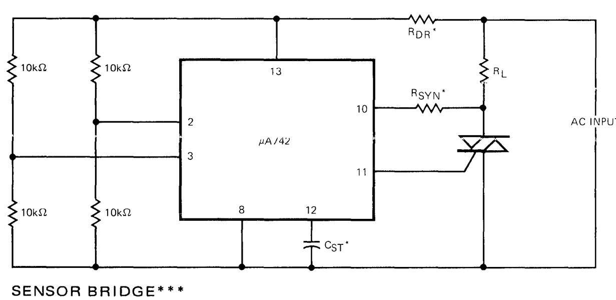


Fig. 7

7

µA757

GAIN-CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

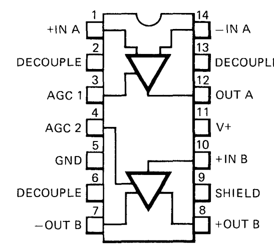
GENERAL DESCRIPTION — The µA757 is a monolithic high performance, Gain Controlled IF Amplifier constructed using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The µA757 is intended primarily as a gain controlled, intermediate frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting amplifier.

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV SIGNAL HANDLING CAPABILITY AT INPUT**
- **CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15V
Voltage at any Output Terminal	+24V
Voltage at either AGC Terminal (Note 1)	±12V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5V
Internal Power Dissipation (Note 2)	670 mW
Storage Temperature Range	
Hermetic DIP (µA757, µA757C)	−65°C to +150°C
Operating Temperature Range	
Military (µA757)	−55°C to +125°C
Commercial (µA757C)	0°C to +70°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s) µA757	300°C

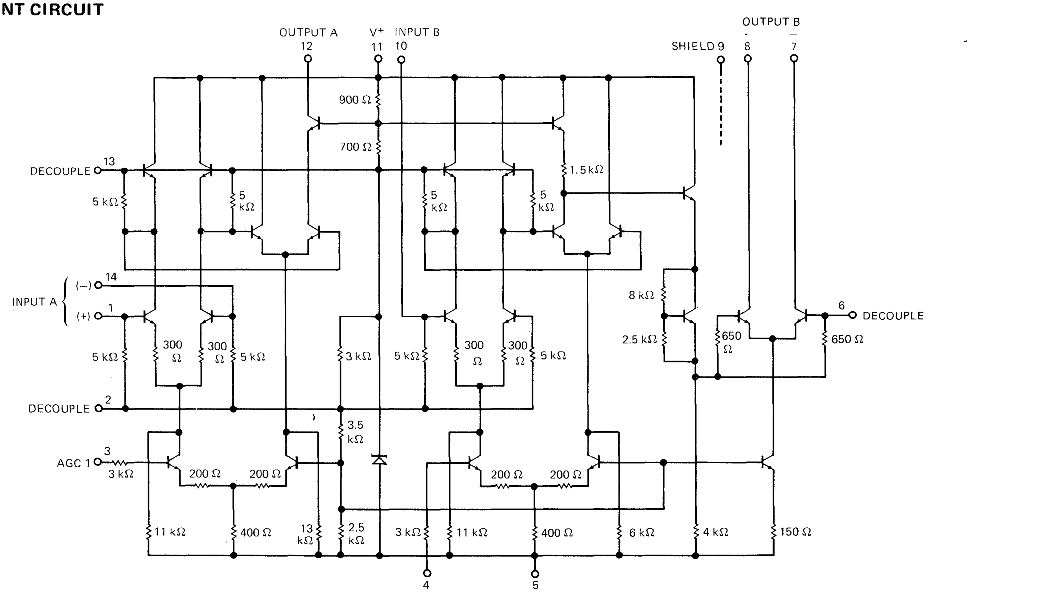
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
µA757	µA757DM
µA757C	µA757DC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchil process.

μA757

ELECTRICAL CHARACTERISTICS: V_+ = +12 V, T_A = 25°C, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		13	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1}$ = +0.8 V, f = 500 kHz			14		mmho
	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1}$ = +0.8 V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2}$ = +0.8 V, f = 500 kHz			440		mmho
	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			5.0	6.0	
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

7

μA757

ELECTRICAL CHARACTERISTICS: V_+ = +12 V, T_A = +125°C, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		14	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	55	71		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2		62		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		−1.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.4	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			6.0	7.0	V

μA757

ELECTRICAL CHARACTERISTICS: V_+ = +12 V, T_A = −55°C, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		10	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			14	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		120	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			170	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	55	68		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2		64		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		−3.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		30	70	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			4.0	6.0	V

μA757C

ELECTRICAL CHARACTERISTICS: $V_+ = +12V$, $T_A = +25°C$, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			18	22	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$V	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			220	270	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2} = +1.7$ V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal $f_1 = 500$ kHz, $e_1 = 100$ mV $f_2 = 510$ kHz, $e_2 = 100$ mV $I_{OUT} = 1$ mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1} = +0.8$ V, f = 500 kHz			14		mmho
	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	V
Noise Figure	$R_S = 1.0$ kΩ, f = 10.7 MHz			8.0		dB
	$R_S = 1.0$ kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, $f_c = 500$ kHz Interfering signal, $f_i = 510$ kHz $I_{OUT} = 0.5$ mA p-p, $V_{AGC\ 1} = +0.8$ V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2} = +0.8$ V, f = 500 kHz			440		mmho
	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0	V
Power Supply Sensitivity	$V_S = 12$ V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

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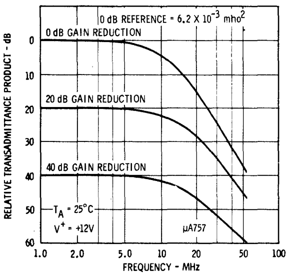
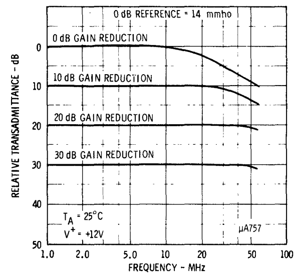
TYPICAL PERFORMANCE CURVES FOR μA757 AND μA757C

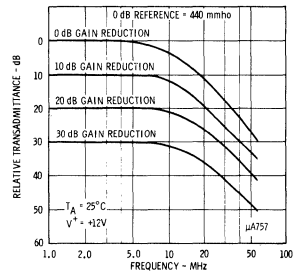
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



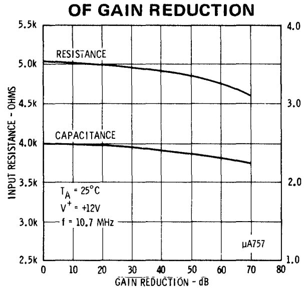
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



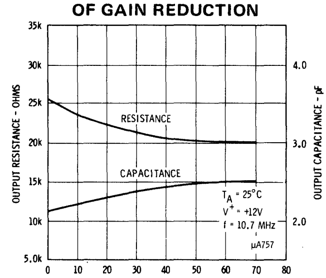
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



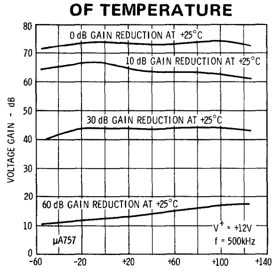
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



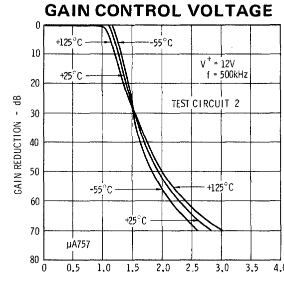
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



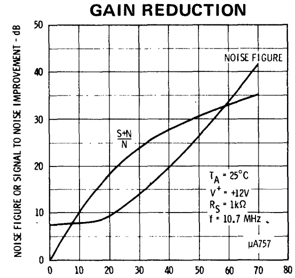
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



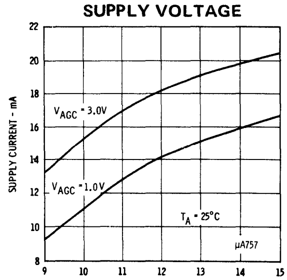
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



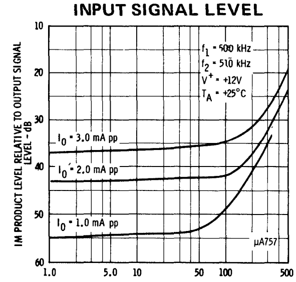
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



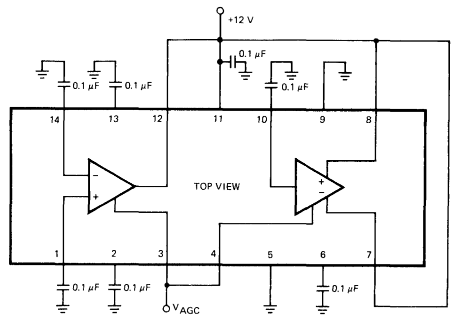
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



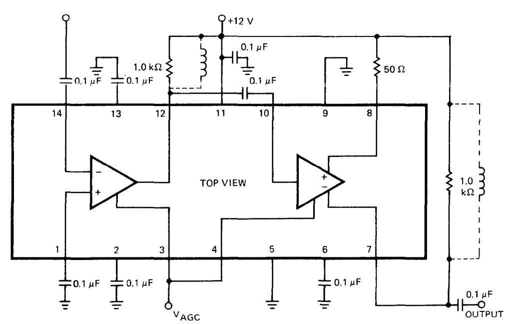
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1 (NOTE 3)



TEST CIRCUIT 2 (NOTE 2)



NOTES

1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C.

For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out. Pin 9 should be connected to GND.

µA7391

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

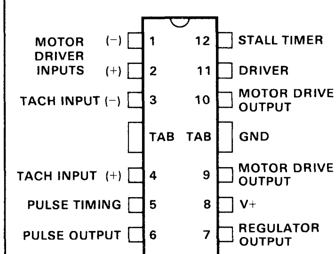
GENERAL DESCRIPTION – The µA7391 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial control applications, *e.g.*, floppy disc drive systems, data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The µA7391 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

- **PRECISION PERFORMANCE – FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM −40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE – 3.5 A STARTING SURGE CURRENT AND 2 A RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT – 100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE – 6.3 V TO 16 V**

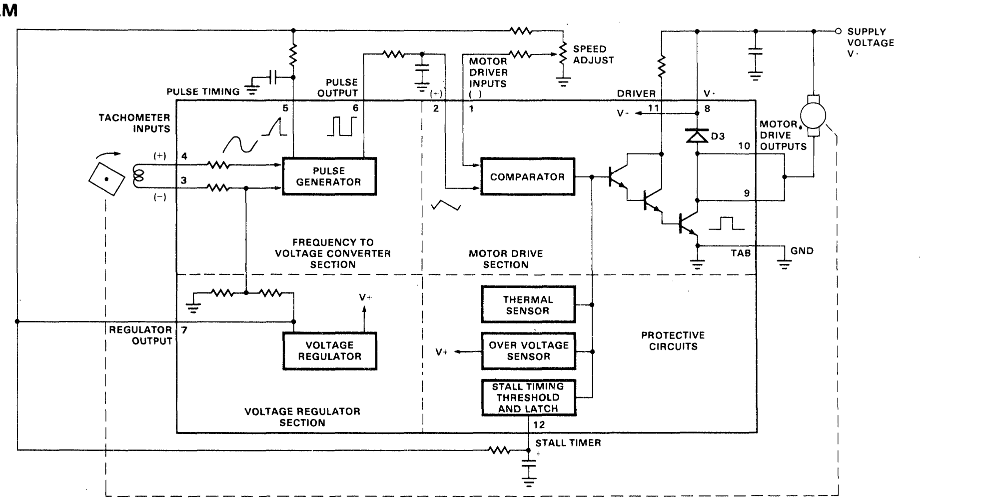
CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P6



ORDER INFORMATION

TYPE	PART NO.
µA7391	µA7391PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_8	24 V
Regulator Output Current, I_7	15 mA
Voltage Applied to Pin 5 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 4 (Tachometer Inputs)	±6 V
DC Voltage Applied to Pin 11 (Driver)	24 V
DC Voltage Applied to Pins 9 or 10 (Motor Drive Output)	V+
Continuous Current through pins 9 and 10:	
Motor Drive Output ON	2.0 A
Repetitive Surge Current through Pins 9 and 10:	
Motor Drive Output ON	3.5 A
Motor Drive Output OFF	2.0 A
Repetitive Surge Current through Pin 11	300 mA
Power Dissipation	Internally Limited
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 s)	260°C

THERMAL DATA

θ_{JC}	Thermal Resistance Junction to Case (tab) (max)	12°C/W
θ_{JA}	Thermal Resistance Junction to Ambient (max)	**70°C/W

**Obtained with tabs soldered to a printed circuit board having a minimum area of copper surrounding the tabs.

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pins 9, 10 and 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_7)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_7)	I_7 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_4 = V_3$		1.0	10	μA
Tachometer Input Positive Threshold	$(V_4 - V_3)$	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	$V_5 = 1$ V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_7$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_6)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_7 - V_6$)			0.12	0.2	V
Pulse Output HIGH Source Current	$V_6 = 1$ V	−340	−260	−180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_7$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_7$ (Note 2) T_A from −40°C to +85°C		0.3		%

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ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25° C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Driver Saturation	$I_9 + I_{10} = 2$ A, $I_{11} = 175$ mA		1.9	2.5	V
Driver Leakage Current	$V_{11} = 16$ V			5.0	μA
Motor Drive Output Saturation	$I_9 + I_{10} = 2$ A, $I_{11} = 55$ mA		0.6	1.1	V
Motor Drive Output Leakage	$V_8 = V_9 = V_{10} = 16$ V			100	μA
Flyback Diode Leakage	$V_9 = V_{10} = 1$ V			30	μA
Flyback Diode Clamp	$I_9 + I_{10} = 2$ A Motor Drive Output Off		1.6	2.5	V

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25° C, unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

NOTES:

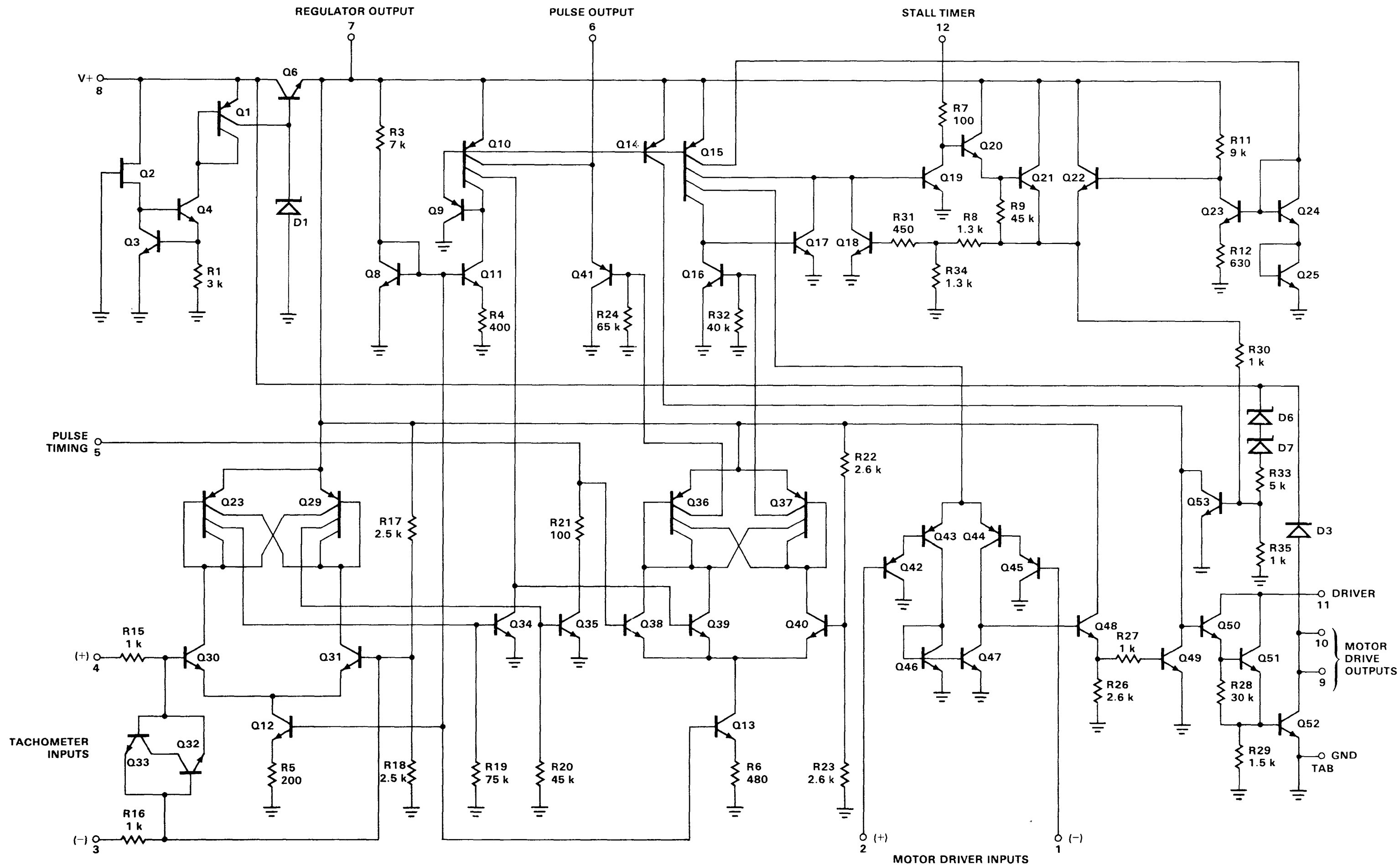
1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV(16\text{ V})}}{V_{7(16\text{ V})}}\right] - \left[\frac{V_{FV(10\text{ V})}}{V_{7(10\text{ V})}}\right] \div \left[\frac{V_{FV(14.5\text{ V})}}{V_{7(14.5\text{ V})}}\right] \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 6)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

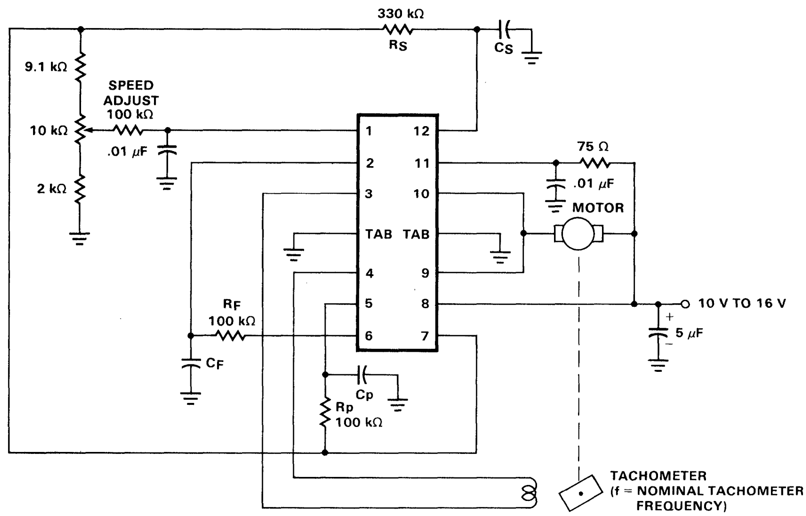
$$\left[\frac{V_{FV(85°C)}}{V_{7(85°C)}}\right] - \left[\frac{V_{FV(-40°C)}}{V_{7(-40°C)}}\right] \div \left[\frac{V_{FV(25°C)}}{V_{7(25°C)}}\right] \times 100\%$$

4. "Driver" and "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 12 should be grounded.



EQUIVALENT CIRCUIT

TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

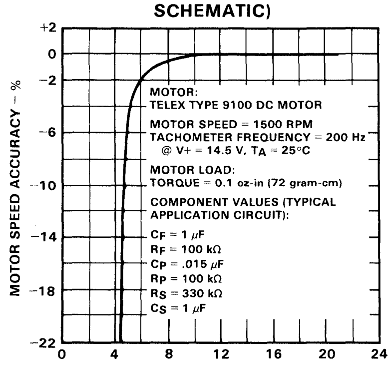
$$Cp = \frac{1}{4\ Rpf}$$

C_F = 10 Cp to 1000 Cp depending on system requirements

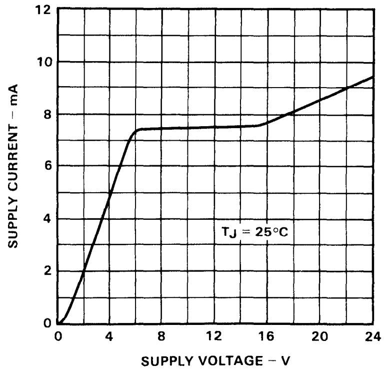
$$CS = \frac{2 \text{ x stall time-out}}{RS}$$

$R_{Motor} \geqslant 5\ \Omega$

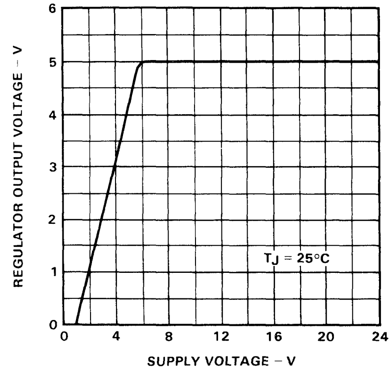
MOTOR SPEED ACCURACY AS A FUNCTION OF SUPPLY VOLTAGE (REFER TO APPLICATION SCHEMATIC)



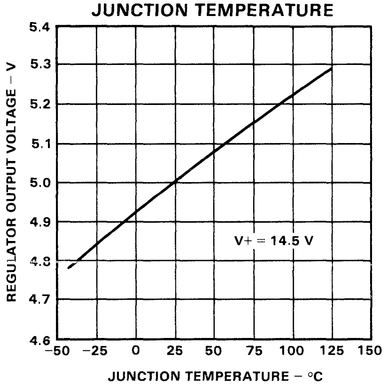
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



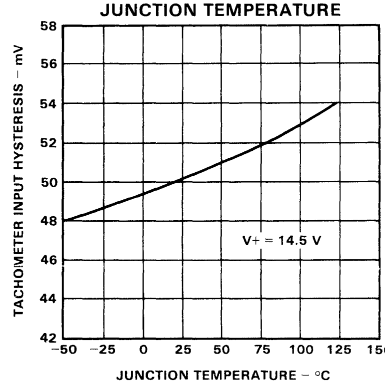
REGULATOR OUTPUT VOLTAGE AS A FUCTION OF SUPPLY VOLTAGE



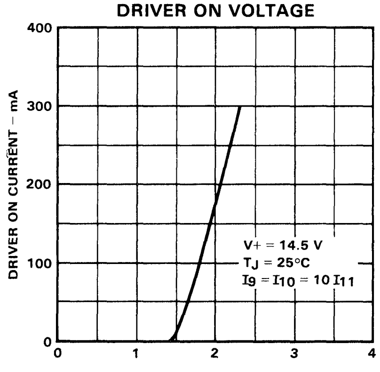
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



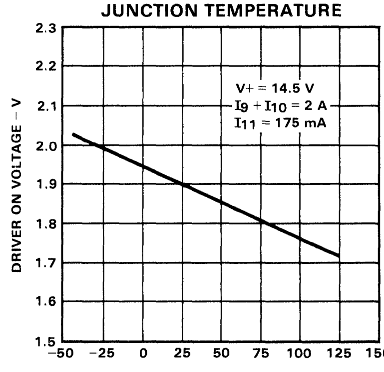
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



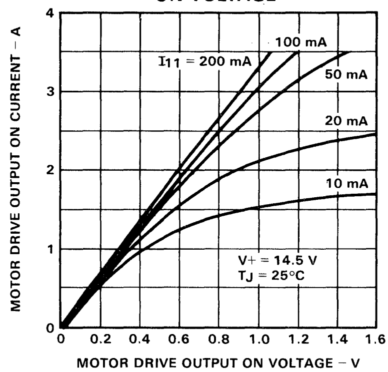
DRIVER ON CURRENT AS A FUNCTION OF DRIVER ON VOLTAGE



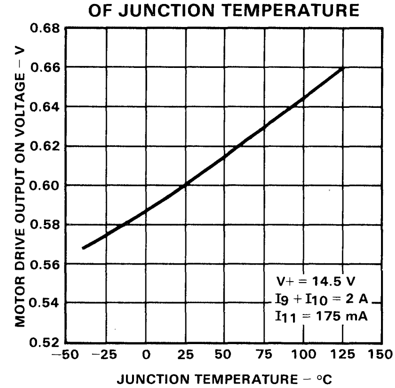
DRIVER ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



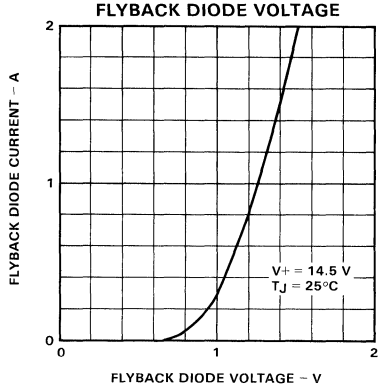
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



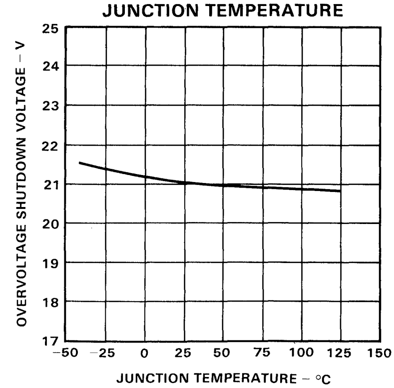
MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



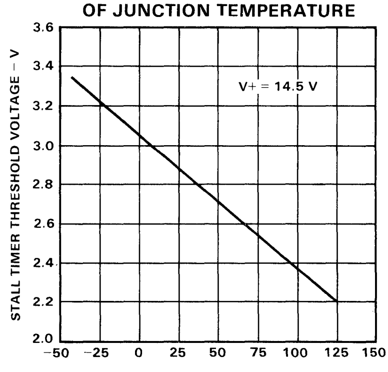
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



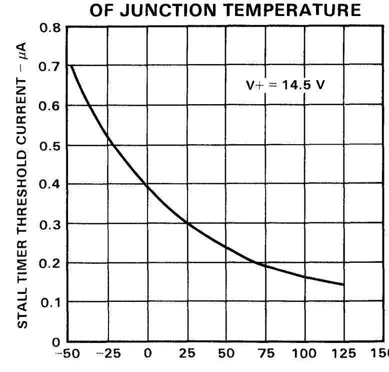
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



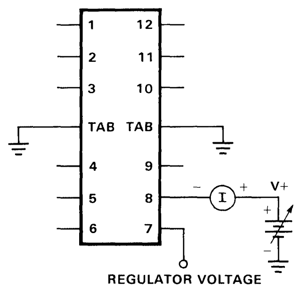
STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



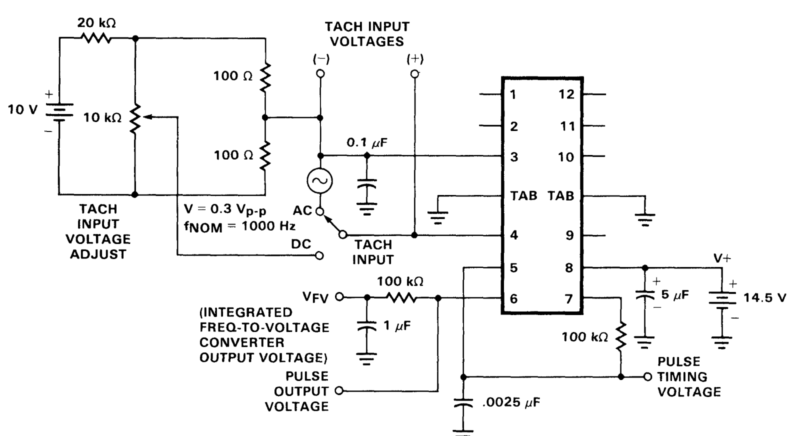
STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



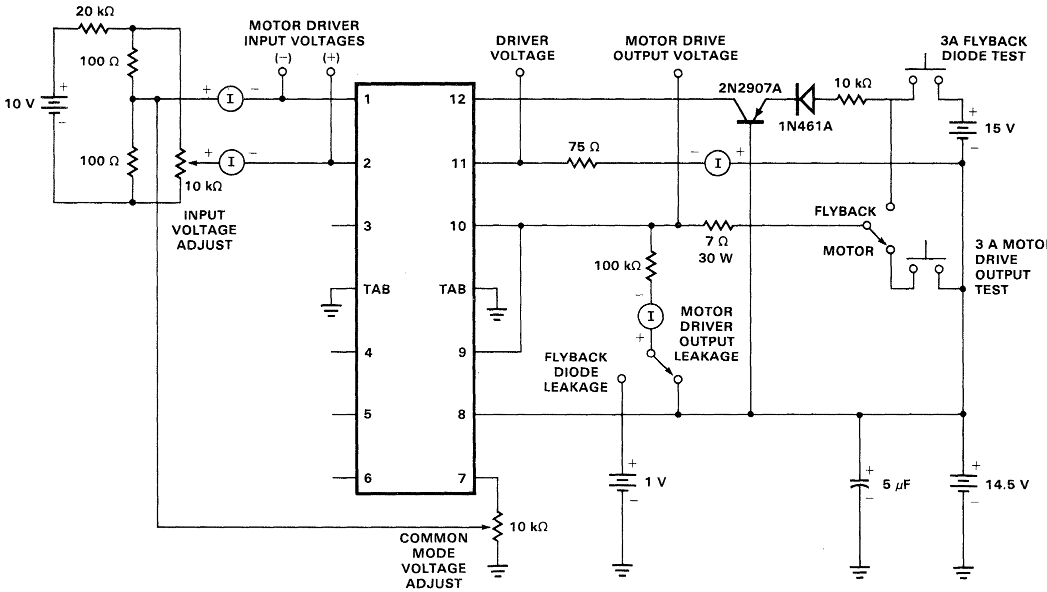
TEST CIRCUIT 1



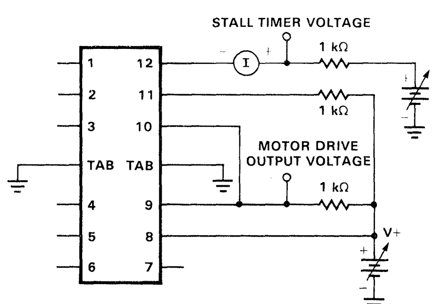
TEST CIRCUIT 2



TEST CIRCUIT 3



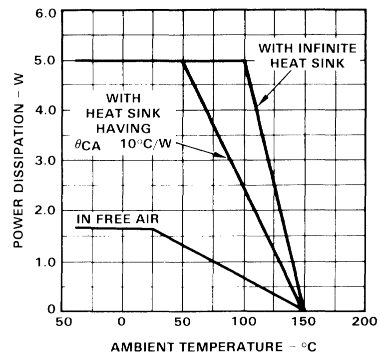
TEST CIRCUIT 4



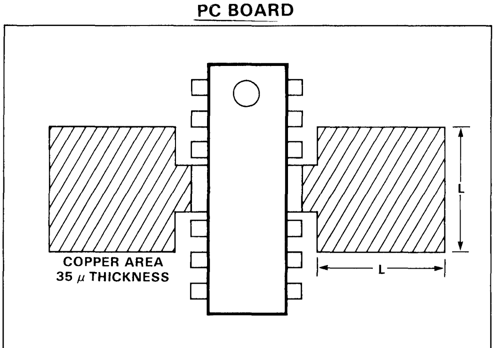
MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to an area of copper on the printed circuit board. During soldering the tabs temperature must not exceed 260°C and the soldering temperature time must not be longer than 10 seconds.

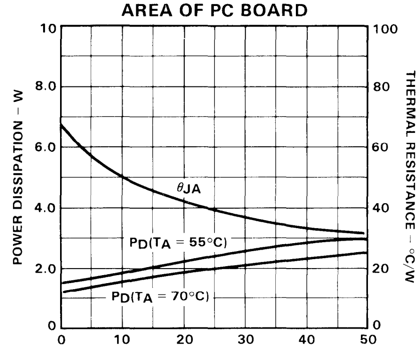
MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



PC BOARD



MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD



μA7392

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The μA7392 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

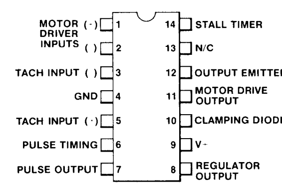
Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

The μA7392 is a low current compliment to the μA7391 for those applications requiring less current and also to drive high current output stages for very high current applications.

- **PRECISION PERFORMANCE—FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM -40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE—1.0 A STARTING SURGE CURRENT AND 300 mA RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT—100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE—6.3 V TO 16 V**
- **EMITTER OF OUTPUT STAGE AVAILABLE FOR EASE IN DRIVING POWER TRANSISTOR OUTPUT STAGES**
- **CLAMPING DIODE AVAILABLE ON SEPARATE PIN**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA7392	μA7392DM
μA7392C	μA7392DC
μA7392C	μA7392PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Pin 6 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 5 (Tachometer Inputs)	±6 V
Continuous Current through Pins 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Pins 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Pins 10 and 11 (Motor Drive OFF)	0.3 A
Power Dissipation	Internally Limited
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range (μA7392)	-55°C to +125°C
Operating Temperature Range (μA7392C)	-40°C to +85°C
Pin Temperature (Soldering 10 s)	260°C

*Planar is a patented Fairchild process

μA7392 and μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
Tachometer input Positive Threshold	$(V_5 - V_3)$	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{pk-pk}
Pulse Timing ON Resistance	V_6 = 1 V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	-340	-260	-180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_8$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_8$ (Note 2) T_A from -40°C to +85°C		0.3		%

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			5	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

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μA7392, μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

μA7392 ONLY

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	12	mA
Regulator Output Voltage		4.5	5.0	6.0	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40	100	mV

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	15	μA
Tachometer Input Positive Threshold	$(V_5 - V_3)$	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	V_6 = 1 V		300	670	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	-370	-260	-150	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$F_{FV} = 0.25\ V_8$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_8$ (Note 2) T_A from -40°C to +85°C		0.3		%

μA7392 ONLY

ELECTRICAL CHARACTERISTICS Cont. : V+ = 14.5 V, -55°C ≥ TA ≤ +125°C, unless otherwise noted.

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±30	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			10	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	1.8	2.9	4.0	V
Stall Timer Threshold Current	Note 5		0.3	4.0	μA

NOTES:

1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV}(16\ V)}{V_8(16\ V)}\right] - \left[\frac{V_{FV}(10\ V)}{V_8(10\ V)}\right] \div \left[\frac{V_{FV}(14.5\ V)}{V_8(14.5\ V)}\right] \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 7)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

$$\left[\frac{V_{FV}(85°C)}{V_8(85°\ C)}\right] - \left[\frac{V_{FV}(-40°\ C)}{V_8(-40°\ C)}\right] \div \left[\frac{V_{FV}(25°\ C)}{V_8(25°\ C)}\right] \times 100\%$$

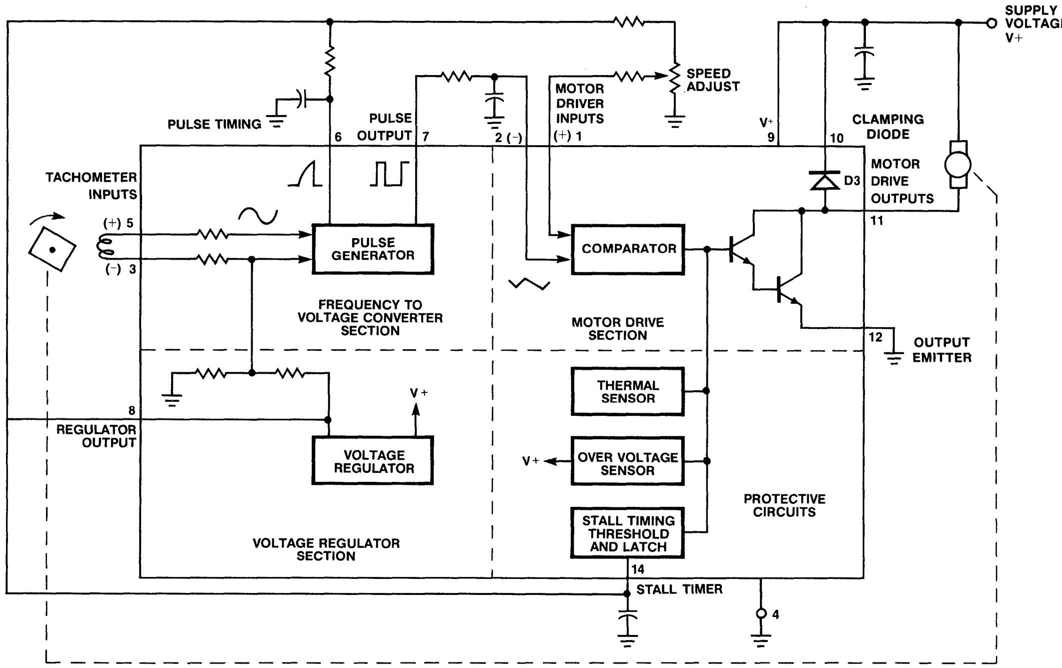
4. "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 14 should be grounded.

THERMAL DATA

		TYP	MAX	
θ_{JA} THERMAL RESISTANCE, JUNCTION TO AMBIENT				
	PLASTIC (9A)	70	80	°C/W
	CERAMIC (6A)	100	120	°C/W

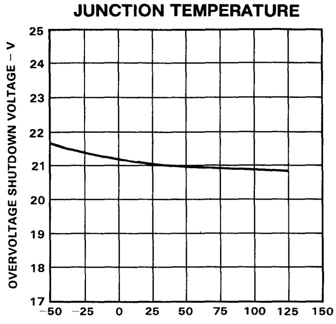
7

BLOCK DIAGRAM

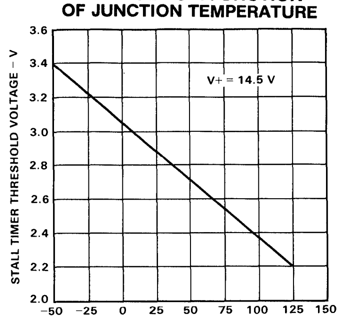


TYPICAL PERFORMANCE CURVES

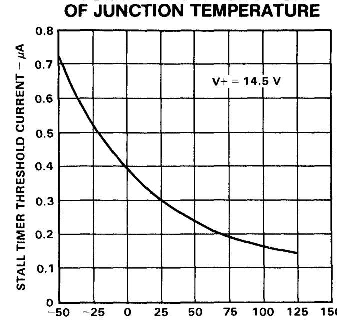
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

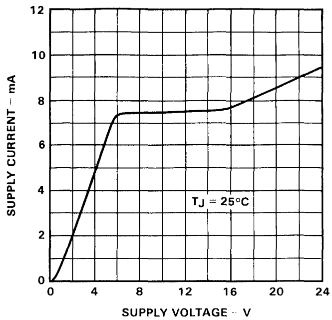


STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

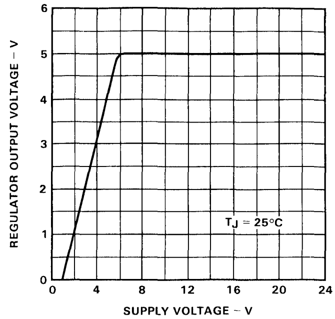


TYPICAL PERFORMANCE CURVES (Cont'd.)

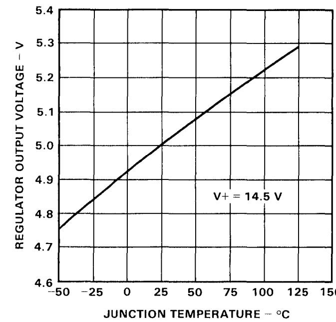
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



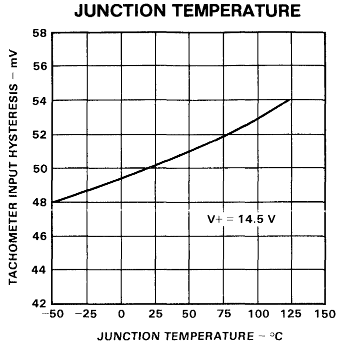
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



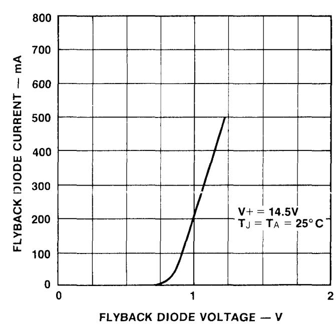
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



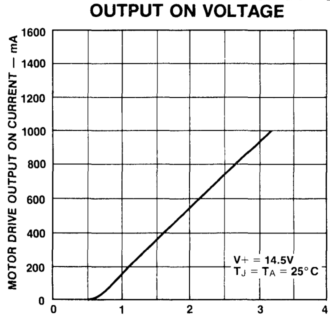
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



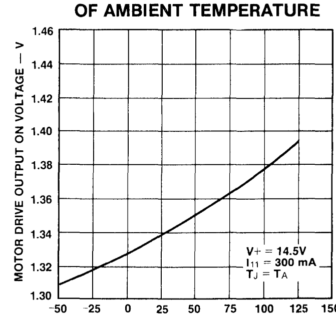
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



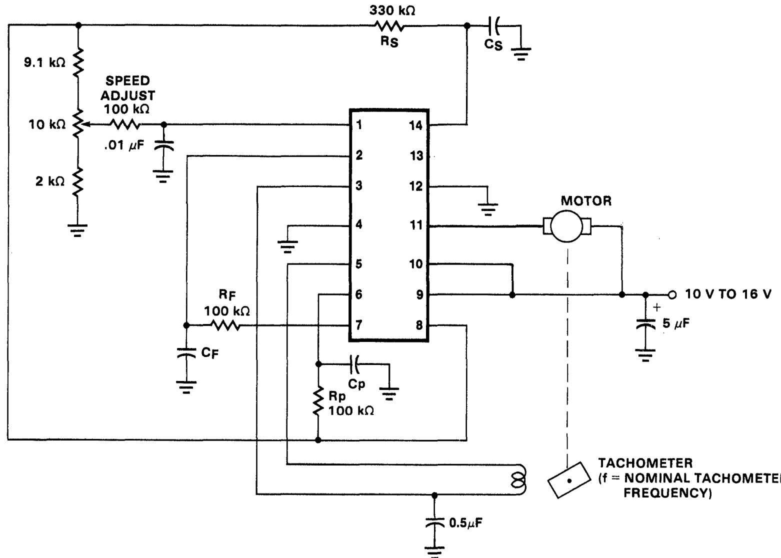
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

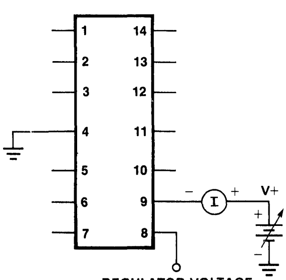
$Cp = \frac{\quad}{4\ Rpf}$

Cf = 10 Cp to 1000 Cp depending on system requirements

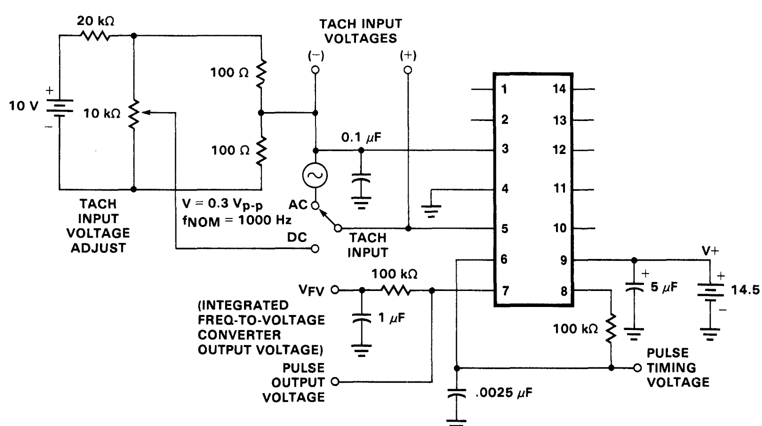
$Cs = \frac{2 \times \text{stall time-out}}{RS}$

$R_{Motor} \geq 5\ \Omega$

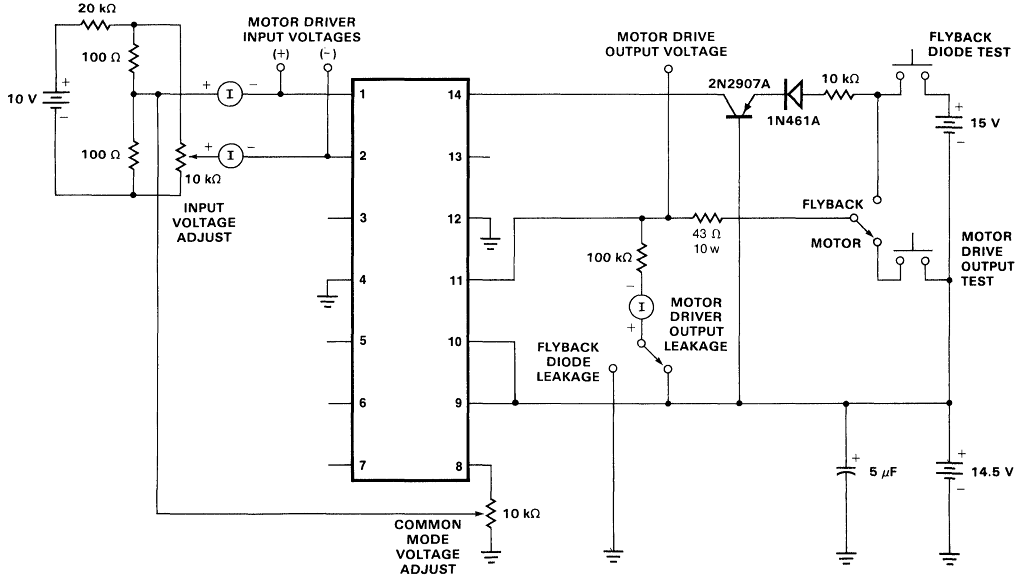
TEST CIRCUIT 1



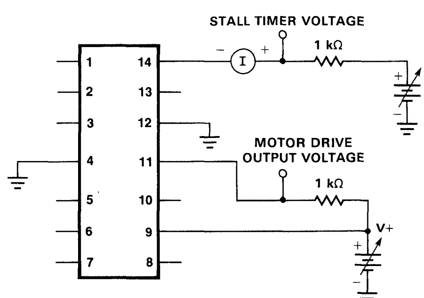
TEST CIRCUIT 2

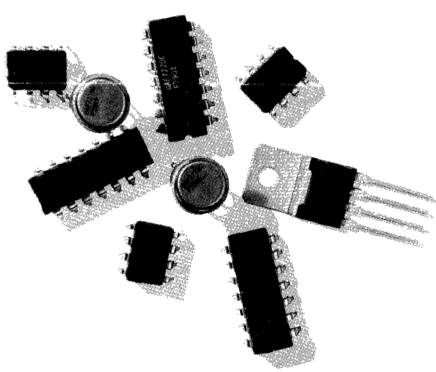


TEST CIRCUIT 3



TEST CIRCUIT 4





APPLICATION AND TESTING INFORMATION

TESTING OPERATIONAL AMPLIFIERS

WHAT IS AN OP AMP?

An operational amplifier is a direct-coupled high-gain amplifier, often powered by both a positive and a negative supply so that the output can swing both above and below ground. By itself, because of the high gain (80 dB or much higher), op amp usefulness is limited due to saturation, with the output swung as far as possible toward one of the supplies. With feedback applied, in a closed-loop configuration, the op amp becomes a useful device. Since the properties of the closed-loop circuit depend primarily on characteristics of the feedback components rather than the op amp, and since typical feedback components, i.e. resistors and capacitors, have high precision and low drift, closed-loop op amp circuits can be very accurate and stable.

The name operational amplifier is derived from one of the original uses of closed-loop op amp circuits, performing mathematical operations in analog computers. Early op amps used a single, ground-referenced inverting input, where a positive voltage change at the input caused a negative change at the output. The more versatile, modern op amps have two floating inputs — one inverting and one non-inverting. Since an op amp responds equally to the two inputs, the output depends on the difference between the inputs, known as differential inputs. A common-mode signal, applied equally to both inputs, is ignored since there is no difference between inputs. By grounding one of the inputs, the differential amplifier becomes a ground-referenced amplifier.

With negative feedback applied to an inverting input, the op amp continually adjusts the output to minimize (or null) the differential input voltage. Because the gain of the op amp is so high, the nulled input voltage is always small, regardless of the output voltage. For example, if the gain is 100,000 and the output is at 10 V, the differential input is only 100 μV, a negligible voltage. Thus, it can be said that the op amp with negative feedback is continually adjusting the outputs to keep the inputs at the same voltage.

MAJOR DC PARAMETERS

There are seven important parameters that are tested and guaranteed on all modern IC op amps. In the following discussions, input voltage refers to the differential voltage at zero common-mode voltage.

8

Input Offset Voltage V_{OS}

Ideally, the output voltage should be zero when the input voltage is zero, but practically, there will always be small mismatches in the amplifier components. Input offset voltage is the input voltage required to zero the output, typically a millivolt or two. V_{OS}, usually caused by mismatches in the base-emitter voltages of the amplifier input transistors, is undesirable in a direct-coupled circuit because the circuit will usually amplify it, causing a large dc error, which is temperature-dependent.

To avoid the effects of input currents, V_{OS} should ideally be measured at zero source impedance (resistance from each input to ground). For testing purposes, some low impedance, usually 50 ohms, is used.

Input Bias Current I_B

Although op amp inputs ideally draw no current, practically, some bias current must flow into each input. For op amps with bipolar transistors at the input, I_B is the base current of the input transistor, typically 100 nA. Where source impedance is low, I_B has no effect; but in high-impedance circuits, a voltage (I_B x source resistance) will appear at the amplifier input. This error is similar to V_{OS} and is also temperature-dependent.

Because of the design of differential stages, the two I_Bs of an op amp vary with the input voltage, but their sum remains constant. The parameter usually tested is the total input bias current $I_{B(Total)} = (I_{B(inverting)} + I_{B(non-inverting)})$. The average input bias current specified on data sheets is just $I_{B(Total)}/2$.

Occasionally, it is necessary to measure the two input currents separately. To make $I_{B(Total)}$ divide evenly between the two inputs and not in a random way, dependent on V_{OS}, the standard convention is to null the op amp in a feedback loop.

Input Offset Current I_{OS}

Because an op amp has differential inputs, many of the effects of the two input currents can be eliminated if both currents are equal, since equal effects at both inputs would cancel. Practically, the two input currents cannot be made exactly equal, so the difference between them is specified. The input offset current is the difference between the two input currents when the op amp is nulled. In applications where the inputs are operated from equal source impedance, I_{OS} is the parameter of interest.

In op amps with a simple input stage, like the μA709 or μA749, I_{OS} is dependent on the beta match of the input transistors. In more complicated devices, like the μA741, I_{OS} also depends on matching the current sources that supply the input transistors.

High-Impedance Composite Input Offset Voltage V_{OS} 10 k

The input offsets of an op amp are fully specified by either:

$$V_{OS},\ I_{B(inv)},\ I_{B(ninv)}\ \textit{or}\ V_{OS},\ I_{OS},\ I_{B(Total)}$$

In either case, common-mode and differential input voltages can be calculated for any source resistances, equal or unequal. In applications with equal source resistors, V_{OS} dominates at low impedances and I_{OS} dominates at high impedances. At some intermediate resistance, V_{OS} and I_{OS} effects are about equal and may add or cancel, depending on their signs which are statistically uncorrelated. If they add, the composite offset will be greater than V_{OS} and may even be greater than the data sheet limit for V_{OS}. To guard against this possibility, a high-impedance composite input offset voltage at a specified source resistance, usually 10 k, is tested and guaranteed. V_{OS} 10 k is not an independent parameter of an op amp; it is a calculated number, determined by the interaction of the independent parameters V_{OS} and I_{OS} with external source resistors.

Voltage Gain

The gain of an op amp, as with any other amplifier, is the ratio of a change in the output voltage to a change in the input voltage. Gain can be specified in V/V or in dB. The symbol A_{VOL} is used to indicate open-loop voltage gain, the gain of the amplifier without feedback.

Common Mode Rejection Ratio CMRR

Ideally, an op amp ignores common-mode signals. Practically, there will always be some small response. The standard convention for measuring this response is to null the amplifier, then measure the change in V_{OS} when large common-mode voltages are applied. The common mode rejection ratio CMRR is the ratio of change in V_{OS} to the change in common-mode voltage, specified in dB. To avoid a minus sign (-100 dB, -70 dB), CMRR is often specified "upside-down" as the change in common-mode voltage over the change in V_{OS}. Typical op amps have 80 to 100 dB CMRR.

Power Supply Rejection Ratio PSRR

Power supply rejection ratio is a measure of the ability of the op amp to ignore changes in the power supply voltages. The change in V_{OS} is measured as the supplies are varied. Power supply rejection ratio PSRR is the ratio of the change in V_{OS} to the total change in power supply voltage. For example, if the supplies vary from ±5 V to ±20 V, the total change is 40 - 10 = 30 V. PSRR is usually specified in μV/V or sometimes in dB, in which case the "upside-down" form is used. Typical op amps have 30 μV/V (90 dB) PSRR.

MINOR DC PARAMETERS USUALLY SPECIFIED

Output Swing

Ideally, the output voltage of an op amp should be able to swing all the way to either supply. However, real op amps saturate within a volt or two of the supplies, depending on how many base-emitter junctions and/or saturated transistors are involved. Op amp output stages are usually complementary-symmetry emitter followers, so output impedance is low, whether the op amp is sinking or sourcing output current. To ensure that both the npn and pnp are operating, both positive and negative swing are tested, with an external resistor connected to load the output.

Output Short-Circuit Current I_{SC}

Most recent op amps have a protective current limit built into the output. If the output is short circuited or otherwise overloaded, the output current limits at some safe value, typically 25 mA. The current limit circuits for each direction of current (sourcing and sinking) are independent and must be tested separately, although they are designed to limit at the same value.

I_{SC} is generally tested under worst-case conditions. For example, an input voltage is applied to cause the output to swing to positive saturation, but the output is then shorted to the negative supply and held there while I_{SC} is read. This causes maximum power dissipation in the output transistor.

Supply Current I_S or I_{SUP}

The standby current of the amplifier is measured when the output is at zero. In modern op amps that have no ground terminal, the standby current into the V+ lead is equal to the standby current out of the V- lead and could be measured at either terminal. In older op amps, such as the μA702, that do have a ground terminal, the currents must be measured separately.

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Power Consumption

Power consumption is determined by multiplying the supply current times the total supply voltage. This parameter is guaranteed by the I_S test.

Offset Adjust $V_{OS(adj)}$

Some op amps have a pair of offset adjust terminals. Zero offset voltage can be obtained by adjusting a potentiometer connected between these terminals. Test each $V_{OS(adj)}$ terminal by measuring V_{OS} while the terminal is shorted to V–. This indicates the maximum effect of the terminal on V_{OS}.

DC STRESS TESTS

Data sheets always include "absolute maximum" limits on common-mode input voltage, differential input voltage, and supply voltage. To guarantee these ranges, any of several tests can be performed. Sometimes a measurement is taken during the test if there is some measurable indication of a failure. Other times, certain voltages are simply applied and removed before the main test sequence.

Common-Mode Stress
This is not usually tested. The inputs are moved over a large common-mode voltage range during CMRR; since the absolute maximum range is only slightly larger, a separate test is usually unnecessary.

Differential Stress (Input Leakage - IL)
In this test, the inputs are subjected to absolute maximum differential input voltage. All of $I_{B(Total)}$ will flow in the more positive input and the more negative input should see nothing but leakage. Breakdown occurs if the input stage is defective. Input leakage is often measured during the test.

Supply Stress
Supply current is measured under absolute maximum supply voltages.

Internal MOS Capacitor Test - Cap Stress
Many modern op amps include a small MOS capacitor on the chip to set the amplifier frequency response. The silicon dioxide dielectric of the cap is made only thick enough to withstand the absolute maximum total supply voltage. To test the dielectric, maximum supplies are applied and the circuit is swung to whichever state puts the full voltage across the cap. The output is often measured. Typically, if the dielectric ruptures, the amplifier will latch up in an improper state; the output will go negative when it should be positive.

AC PARAMETERS
Since ac parameters are not usually tested in production, only typical values are shown on the data sheet. However, three common ac parameters should be recognized.

Risetime and Overshoot
The small-signal step response is a simple test that indicates both the bandwidth and stability of an amplifier under specified conditions. The risetime is related to the bandwidth, and the overshoot is a measure of stability.

Slew Rate
Slew rate is a large-signal phenomenon resulting from the capacitor connected to adjust the small-signal frequency response. So that the capacitors can be small, they are usually connected to high-impedance nodes in the circuit, that receive dc bias from current sources. If the amplifier is to reproduce a large signal, such as a 10 V step, the circuit no longer behaves according to its small-signal model. The current source at the compensation node cannot pump enough current into the cap to move the output far enough, fast enough. If current I is provided to the cap C, the output will *slew* toward the final value at a slew rate $dV/dt = I/C$. Slew rate limiting (or rate limiting) occurs with all large, fast signals when current to the capacitor is insufficient.

THE BASIC OP AMP TEST LOOP
All op amps are basically alike, high-gain differential amplifiers. The reason there are so many different op amps is that no one circuit design can possibly optimize all the dc and ac parameters. Op amps are designed to optimize a parameter (high gain, low power consumption, etc.) for particular applications. Fortunately for test engineers, however, the similarities of all op amps are so great that a single test circuit can be used to perform all standard dc tests. This circuit, shown in *Figure 8-1,* is the basic op amp test loop.

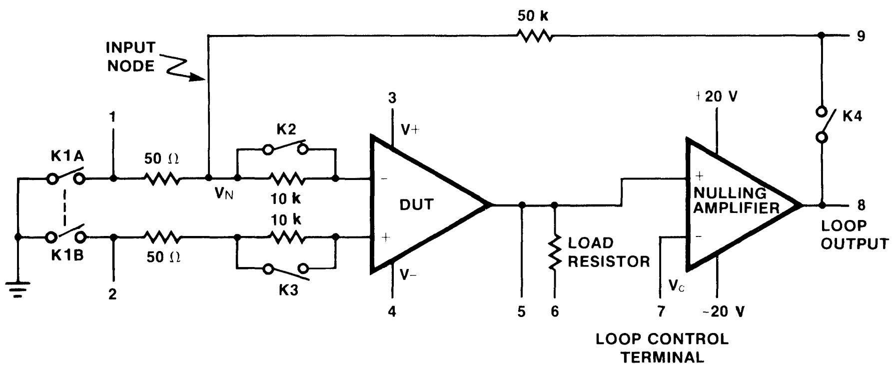

Fig. 8-1 Basic Op Amp Test Loop

Performing all tests requires five power supplies: the V+ and V- supplies for the device under test (DUT), a control voltage V_C applied at the loop control terminal, and supplies to run the nulling amplifier, usually ±15 V or ±20 V.

Operation of the test loop, with all relays closed, is as follows:

- The inverting input of the nulling amplifier is the control terminal of the loop. The DUT output is connected to the non-inverting input of the null amplifier.
- The null amplifier output controls the DUT input through the feedback divider.
- There is one inversion in the loop, provided by the DUT. Therefore, the null amplifier operates with negative feedback.
- With negative feedback, the null amplifier continually adjusts its output to keep its input voltages equal.
- Therefore, the null amplifier adjusts the loop output so that the DUT output follows the control terminal.

The input node voltage, V_N in *Figure 8-1,* is always 1/1000th of the loop output voltage (actually it is 1/1001th, but it is common to neglect the 0.1% error). Thinking in reverse, the circuit has a closed-loop gain of 1000 and any voltage V_N appears 1000 times larger at the loop output. Since the input voltages to the nulled op amp are always very small, the gain simplifies measurements.

Equations for V_N

Figure 8-2 shows the DUT portion of the test loop, leaving out the 50 Ω resistors since their effect is negligible in this analysis. V_{OS} is represented as a small voltage source moved outside the op amp. Current flows into both inputs of the op amp. With V_N adjusted by feedback to produce a DUT output of zero, and with V_{OS} accounted for externally, no voltage exists between the op amp inputs; *zero in* means *zero out.* V_N equations can now be written for the various settings of K2 and K3.

K2 closed, K3 closed: $V_{N1} = V_{OS}$

The input bias currents have no effect because there is no source resistance.

K2 closed, K3 open: $V_{N2} = V_{OS} - I_{B(ninv)} \times 10\text{ k}$

With only K3 open, V_N is a composite voltage involving V_{OS} and $I_{B(ninv)}$. To test $I_{B(ninv)}$, measure V_{N2}, then subtract it from V_{N1} (equal to V_{OS}).

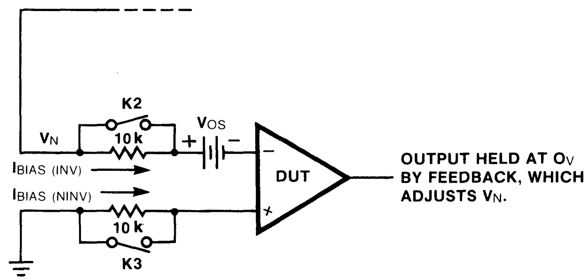

Fig. 8-2 Simplified Input Circuit For Calculating V_N

K2 open, K3 closed: $V_{N3} = V_{OS} + I_{B(inv)} \times 10\text{ k}$

To measure $I_{B(inv)}$, subtract V_{OS} from V_{N3}.

K2 open, K3 open:

$$\begin{aligned} V_{N4} &= -I_{B(ninv)}\,(10\text{ k}) + V_{OS} + I_{B(inv)}\,(10\text{ k}) \\ &= V_{OS} + \left(I_{B(inv)} - I_{B(ninv)}\right)(10\text{ k}) \\ &= V_{OS} + I_{OS}\,(10\text{ k}) \\ &= V_{OS}\ \ 10\text{ k} \end{aligned}$$

V_{N4} is the high-impedance composite input offset voltage. To measure I_{OS}, subtract V_{OS} from V_{N4}.

Each relay setting combination provides an easy way to measure some important parameter of the op amp. For a measurement of $I_{B(total)}$, measure V_{N3} and subtract it from V_{N2}.

$$\begin{aligned} \Delta V_N &= V_{OS} + I_{B(inv)}\,(10\text{ k}) + I_{B(ninv)}\,(10\text{ k}) - V_{OS} \\ &= \left(I_{B(inv)} + I_{B(ninv)}\right)(10\text{ k}) \\ &= I_{B(total)}\,(10\text{ k}) \end{aligned}$$

Testing Using the Op Amp Test Loop

For the following tests of op amp parameters, refer to the test loop schematic, *Figure 8-1,* whenever necessary. All relays are normally closed.

Input Offset Voltage V_{OS}

Set the loop control voltage V_C to zero. The nulling amplifier immediately adjusts the loop output to zero the DUT output. By definition, the input node voltage V_N equals V_{OS}; therefore, the loop output is 1000 V_{OS}. For example, if the loop output reads 1.0 V, V_{OS} is 1.0 mV.

Input Currents (Separately)

Measure V_{OS}. Then open K2 and K3 alternately and compute the changes in V_N as previously described. Because 1000 V_N is always read at the loop output, a voltage change $\Delta V_N = 1000 \times I_B \times 10\text{ k}$ will be measured. Thus, if I_B is 100 nA, the measured change will be 1.0 V.

Total Input Bias Current $I_{B(total)}$

This was explained in the previous section. Measure V_{N2}; then measure V_{N3} and subtract. The measured change at the loop output is $1000 \times I_{B(total)} \times 10\text{ k}$. An alternate method to test $I_{B(total)}$ is to open K1 and K4, tie pins 1 and 2 together, and use a current meter to read $I_{B(total)}$. The industry trend is for dynamic testing, however, since there is some small inaccuracy associated with the latter method.

High-Impedance Composite Input Offset Voltage V_{OS} 10 k
Measure V_{N4} as previously described.

Input Offset Current I_{OS}
Measure V_{OS}. Then measure V_{OS} 10 k and subtract. $\Delta V = (1000)(I_{OS})(10\ k)$.

Gain
In testing low-gain ac amplifiers, such as audio amplifiers, the normal procedure is to apply a small, known input and measure the large ac output. When testing high-gain dc amplifiers, such as op amps, the reverse procedure is used. The test loop is used to vary the output over a large, known range, and the dc change at the input is measured.

A normal test for a DUT using ±15 V supplies is to measure the average dc gain over the output range -10 V to +10 V. Since gain is always specified with a load resistor, pin 6 should be grounded. Set V_C = -10 V; the null amplifier brings the DUT output to -10 V. Measure V_N. Then set V_C to +10 V; the null amplifier brings the DUT output to +10 V. Measure the change in V_N. For example, if the gain is 100,000 and the total output change is 20 V (-10V to +10 V), the loop output change should be (1000) (20/100,000) = 200 mV.

Note that the DUT is tested at the inverting input; therefore, if the output goes from -10 V to +10 V (a positive change), a small negative change should be seen at the input.

As mentioned previously, gain is always tested with an external load resistor, often 2 k Ω. Since the op amp output stage must provide current to this resistor, the output stage must dissipate power. If the op amp is an IC, a thermal signal will then travel across the chip to the input stage, where it mixes with the true, circuit-related input signal. Depending on the relative sizes of the circuit and thermal components, this may cause peculiar readings to occur during a gain test. If the thermal component partially cancels the circuit component, the change in V_N will be smaller than normal, indicating a larger gain. If the two components cancel, no change in V_N will be read, indicating an effective gain of infinity. If the thermal component is larger than the circuit component, a wrong-polarity change in V_N will occur, indicating a "negative gain."

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There is no general agreement in industry about the significance or seriousness of "negative gain." Devices that show negative gain in a test circuit usually behave normally in customer applications. Nevertheless, a device exhibiting a large negative gain may be questionable. Fairchild's policy is to allow a wrong-polarity reading of 20-100% of the right-polarity limit.[1]

To check the linearity of the op amp transfer function, gain is sometimes tested over two different parts of the output range. That is, instead of performing a single test as the output swings from -10 V to +10 V, gain is tested as the output swings from 0 V to +10 V, and then from 0 V to -10 V. Such testing will identify units that have very high gain over part of the output range and very low gain over the other part of the range.

Common Mode Rejection Ratio CMRR
The definition of CMRR might imply that testing involves holding V_C at zero and opening K1, tying pins 1 and 2 together to a voltage V_{CM}, then varying V_{CM} and reading the change in V_N at the loop output. However, this method does not provide accurate results. Because of the 50 Ω/50 k Ω feedback divider, only 99.9% of V_{CM} appears at the inverting input of the DUT. Since there is no divider at the non-inverting input, 100% of V_{CM} appears there, causing a 0.1% differential signal injected by the unbalanced test circuit. This error, only 60 dB below V_{CM}, is disastrous, for devices typically have 80 to 100 dB CMRR.

[1]For a more complete discussion of thermal effects, see Solomon, J. E. "The Monolithic Op Amp: A Tutorial Study," IEEE Journal of Solid State Circuits, Vol. SC-9, No. 6 (Dec, 1974).

The obvious solution is to add another 50 kΩ resistor from the non-inverting input to ground, which should attenuate V_{CM} equally at both inputs to eliminate the differential error signal. The problem now becomes one of accurately matching the dividers. Advanced analysis of the four resistors as a bridge circuit indicates that, with careful matching, quite high CMRRs can be measured.

An easier solution eliminates the need for precisely matched pairs of precision resistors. Instead of holding V+, V- and V_C constant and moving pins 1 and 2, perform the inverse procedure. For example, to apply a V_{CM} of +10 V, leave K1 closed and change V+ from +15 V to +5 V. Then change V- from -15 V to -25 V and change V_C from 0 V to -10 V. From the point of view of the DUT, this is equivalent to the original method. The total supply voltage is still 30 V, the DUT output is still held at the midpoint between the supplies, and both inputs are 10 V above that midpoint, which makes $V_{CM} = +10$ V. However, from the point of view of the bridge, no V_{CM} has been applied, pins 1 and 2 are at ground as always, and V_N is the routine differential input voltage of the DUT.

This method permits accurate measurement of any CMRR without matched resistors. There is no need for a 50 k Ω resistor at the non-inverting input, since it would only shunt the 50 Ω resistor on all tests.

In summary, to measure CMRR, raise V+, V- and V_C to V_{CM} volts above nominal, and measure V_N. Then lower V+, V- and V_C to V_{CM} volts below nominal and measure the change in V_N.

Sometimes CMRR is tested with 10 k Ω source impedances (K2 and K3 open). In this case, any changes in I_{OS} contribute to the total change in V_N. A test with 10 k sources is not necessarily a more rigid test than with 50 Ω; the change in V_N may be larger or smaller, depending on how the V_{OS} and I_{OS} components interact.

Power Supply Rejection Ratio PSRR

The PSRR test is very direct and simple, with none of the problems that occur with CMRR testing. Hold V_C at zero, set both supplies to minimum values, and measure V_N. Then set both supplies to maximum values and measure the change in V_N. PSRR may also be tested with 10 kΩ source impedance.

Output Voltage Swings

Measure at pin 5, saturating the DUT output by applying a large differential input voltage.

There are three possible ways to saturate the DUT. The most direct way is to open K1 and K4 and apply the voltage directly across pins 1 and 2. Another way is to open K4 only and apply a voltage at pin 9. This voltage is divided 1000:1, so 20 V at pin 9 will apply 20 mV to the DUT input, sufficient drive for almost any op amp. The third way is similar to the second except that all relays are closed and the null amplifier applies the 20 V to pin 9. Set V_C to 15 V; the null amplifier will immediately try to bring the DUT output to 15 V, but the DUT cannot swing all the way to V+. The null amplifier output eventually saturates around 18 V and the DUT output also saturates as desired.

Since output swings are always specified with a load resistor, pin 6 should be grounded.

Output Short-Circuit Current I_{SC}

This test involves the same procedure as in measuring voltage swing, except that instead of using load resistor on pin 6, connect a current meter from pin 5 to ground or to the worst-case opposite supply. When the DUT attempts to swing in response to the input, the current meter shorts the output and measures I_{SC}.

Supply Current I_S

Specifications usually indicate the DUT output should be zero, so set V_C to 0 and measure the current into pin 3. The state of the output has little effect on the I_S reading of recent op amps, biased internally by current sources. However, in earlier devices like the μA709, I_S is heavily dependent on the output state, even with nothing connected to the output.

Offset Adjust $V_{OS(adj)}$

The DUT of *Figure 8-1* has no offset adjust pins. Devices with offset adjust pins have relays to connect them alternately, usually to V–. V_C should be set to zero and a measurement taken at the loop output. At the least, the measurement should guarantee that the adjust range is sufficient to eliminate the V_{OS} of the particular device being tested. A more rigid test might require enough range to eliminate the worst possible V_{OS}, even though the DUT has a lower V_{OS}.

Common-Mode Stress

Open K1 and K4. Apply V_{CM} directly to pins 1 and 2.

Differential Stress (IL)

Open K1 and K4. Apply voltage directly across pins 1 and 2. Measure leakage at more-negative input.

Supply Stress

Perform supply current test at specified supplies.

Cap Stress

Test like output voltage swings, using specified supplies and swinging output to specified state.

Common Variations of the Basic Test Loop

The test loop is never used in the exact simplified form shown in *Figure 8-1.* Each op amp has quirks that require some variations on the basic theme. The following are some common variations.

AC Compensation Capacitors

While ac stabilization of the test loop is a complex topic, in general, each type of op amp has its own frequency response which may or may not be externally adjustable. When preparing a test loop for a particular device, it is necessary to use the frequency-response curves of the DUT and the null amplifier to determine which stabilization scheme to use and to predict which capacitors will be required.

Loop Output Noise Filter

A small RC noise filter with time constant around 1 ms is usually attached to the loop output and all measurements taken through this filter. The waveforms at the filtered output often prove to be much cleaner than the unfiltered version.

Source Resistors

Most general-purpose op amps are tested with 10 kΩ source resistors. However, op amps with very low input currents may use 50 k, 100 k, 1 M, or even 10 M resistors for improved resolution.

Test Loop Gain

The most common form of the test loop, with 50 kΩ/50 Ω resistor combination, gives a gain of 1000. For certain tests, usually $V_{OS\,(adj)}$, the 50 kΩ is split into a 45 kΩ and a 5 kΩ resistor, and the 45 kΩ resistor can be shorted with a relay to reduce the gain to 100. For devices with very low V_{OS}, a feedback resistor of 500 kΩ can be used to give a gain of 10,000.

MOSFETs in Place of K2 and K3

Some premium devices, such as the μA108, μA156, and μA725, have extremely low I_{BIAS} and/or V_{OS}. When testing these units, if reed relays are used for K2 and K3, difficulty may arise with the low-level properties of the reeds. Typical problems include thermally-generated EMFs, leakage current, and flexing of the reeds after closing. MOSFETs are usually a good substitute when reeds prove unsatisfactory. The high contact resistance of FETs (100 Ω) is not detrimental if the current passing through them is small, i.e. 1 nA. Benefits include clean switching, no thermal offsets, no leakage, no bounce, no microphonics, and no mechanical wear.

CONCLUSION

Because it works so well on the bench or in conjunction with high-speed automatic testers, the basic op amp test loop circuit is used universally by manufacturers and others who must test operational amplifiers. The test loop is so accurate and easy to use that it benefits even those who test only a few units on the bench.

OP AMP PARAMETERS AND APPLICATIONS

The selection of an operational amplifier for a given application requires a good understanding of op amp specifications and parameters, and their significance in applications.

INPUT BIAS AND INPUT OFFSET CURRENT

Input bias current affects almost all applications of operational amplifiers, especially in high impedance circuits. Although op amp inputs ideally draw no current, for op amps to operate properly, it is necessary for some dc current (typically from pA to μA) to flow into each input (*Figure 8-3*). The input stage of the op amp is ordinarily a differential amplifier with a dc current source that sinks current from the emitters (*Figure 8-4*). The op amp inputs are the base currents for the differential amplifier transistors. Because of the differential stage design, the two base currents vary with the input voltage, but the sum remains constant. The parameter usually tested is the total input current , $I_{B\,(Total)} = I_{B1} + I_{B2}$. The input bias current I_{BIAS} specified on the data sheets, is the *average* of the two input currents *(Figure 8-3)*, and is primarily a function of the large signal current gain h_{fe} of the input stage.

Since, in reality, the two input currents cannot be made exactly equal, input offset current I_{OS} specifies the difference between these two currents (*Figure 8-3*). I_{OS} is usually caused by mismatch of the differential amplifier, which results in different input currents for the two bases. In an op amp with a simple input stage, I_{OS} is dependent on the beta match of the input transistors. In more complicated cases, I_{OS} also depends on matching the current sources of the input transistors.

Effects of Input Bias Current on Applications

The output offset voltage (V_O) due to bias current is the same for both inverting and non-inverting amplifiers *(Figure 8-5)*. Equation 1 shows the formula for V_O as a function of bias current (also see *Figure 8-6*).

$$V_O = I_{B1}\,R2 - I_{B2}\,R3\left(1 + \frac{R2}{R1}\right) \qquad (1)$$

For inverting and non-inverting operation, R3 is selected to minimize output offset without affecting gain.

When R3 equals R2 in parallel with R1,

$$R3 = \frac{R1\ R2}{R1 + R2}$$

Substituting for R3 for Equation 1

$$V_O = (I_{B1} - I_{B2})\,(R2)$$

$$V_O = I_{OS}\,R2$$

When R3 = 0

$$V_O = I_{BIAS}\,R2$$

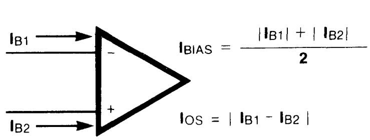


Fig. 8-3 Input Bias Current

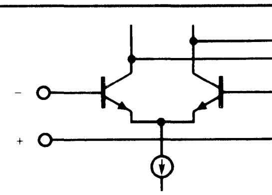


Fig. 8-4 Differential Amplifier

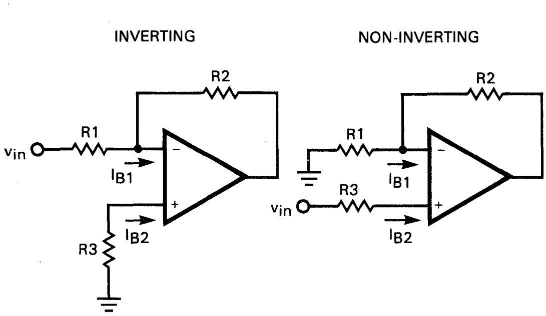


Fig. 8-5 Amplifier Configurations

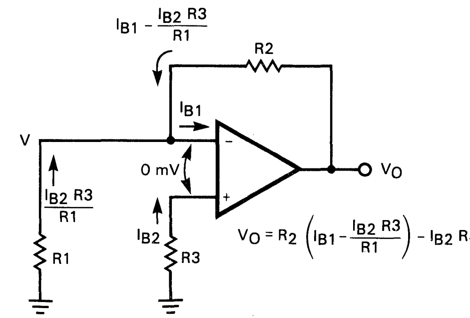


Fig. 8-6 Output Offset Voltage

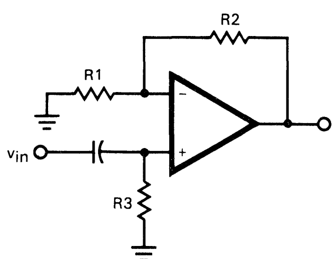


Fig. 8-7 AC Amplifier

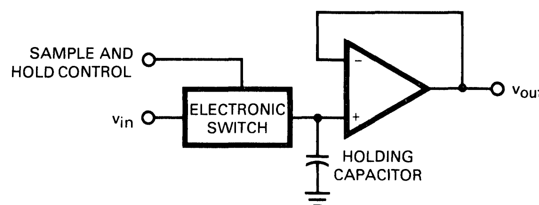


Fig. 8-8 Sample and Hold

NOTES:

- For the inverting configuration, it is usually simple to make R3 equal to R1 in parallel with R2, which reduces the output offset voltage to only I_{OS} R2. However, if the application does not require very low output offset voltage, or if the input bias current I_{BIAS} is very low, make R3 = 0 and the output offset is simply I_{BIAS} R2. Therefore, it is wise first to calculate the output offset voltage produced by the op amp assuming R3 = 0, (I_{BIAS} R2). If this offset is low enough for the **application, the use of one resistor is saved. If the offset is too high, add R3 to the circuit and then calculate offset (I_{OS} R2) to see if it meets the specification.**
- In the non-inverting configuration, R3 is part of the signal source impedance, and, in some cases, that source impedance is not well known, which complicates the minimizing of the output offset. If the source impedance is known to be very low, then a known series resistor can be added to make R3 = R1/R2. The limiting factor for increasing the value of this resistor is the op amp input impedance. If a high value of resistor is used, say 1 MΩ, and the amplifier input impedance is around 9 MΩ in the frequency range of interest, the result is a 10% drop in signal gain.
- Never forget the need for a dc current path to the op amp inputs. If the op amp is used in an ac amplifier as shown in *Figure 8-7*, notice that R3 is required to provide a dc current path to the non-inverting input. Without R3, the circuit just does not work! R3 is also necessary if the source cannot supply the bias current.
- A fixed offset is not usually much of a problem and extra input circuitry may be added to cancel it. It is usually the *drift* of the offset with temperature, time, etc., which causes problems. Therefore, once an op amp with acceptable output offset voltage is found, it is necessary to investigate the offset change as a function of temperature, supply voltage, time, etc., and assure that it will not cause problems in a particular application. Most data sheets give input bias current and offset current as functions of temperature, supply voltage, and time, and also provide temperature dependence curves.

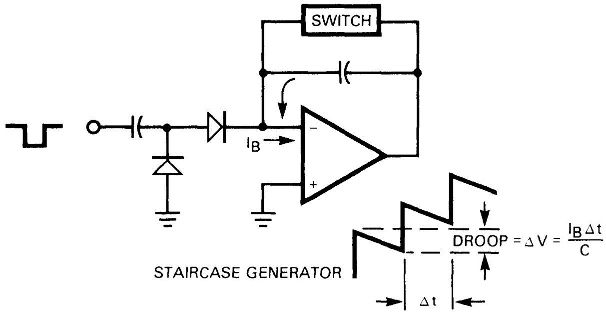


Fig. 8-9 Staircase Generator

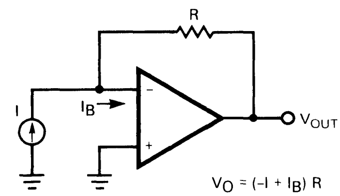


Fig. 8-10 Current-to-Voltage Conversion

Other Applications

Input bias current comes into effect in circuits where op amps act as buffers or amplifiers with a charged capacitor as a source. Because of input bias current, the charge across the capacitor starts draining even if the op amp input impedance is very high. Two examples are shown in *Figures 8-8* and *8-9*.

The sample and hold circuit shown in *Figure 8-8* consists of a voltage V_{in} which charges a holding capacitor C. When the electronic switch opens, the capacitor is expected to hold the voltage V_{in} and the op amp simply acts as a buffer. The output of the op amp, therefore, should hold the value of V_{in} at the level it was when the switch opened for as long as the switch remains open. Because of bias current and other leakage, however, the held voltage gradually changes. This voltage changes at the following rate:

$$\frac{\Delta V}{\Delta t} = \frac{I}{C} \qquad (2)$$

where I is input bias current plus the capacitor leakage.

Equation 2 determines how long a held voltage remains within specified accuracy of its original value. In this sample and hold application, the effect of input bias current shows in the holding time. For example, if the capacitor C = 1 μF, and the maximum permissible change of voltage ΔV is 10 mV, using a μA741C (I_{BIAS} = 0.5 μA) and neglecting other leakages, the holding time is expressed as follows:

$$\Delta t = \frac{C\Delta V}{I} = \frac{1 \times 10^{-6} \times 10 \times 10^{-3}}{0.5 \times 10^{-6}} = 20 \text{ ms}$$

With a μAF771A (I_{BIAS} = 100 pA), a better holding time results.

$$\Delta t = \frac{C\Delta V}{I} = \frac{10^{-6} \times 10 \times 10^{-3}}{100 \text{ X } 10^{-12}} = 100 \text{ s}$$

Low input bias current is not the only criterion for sample and hold buffers; offset voltage drift is another important parameter.

Equation 2 also applies in circuits where the voltage held is across a capacitor in a feedback loop (*Figure 8-9*).

Another application where input bias current plays a role is in current-to-voltage conversion (*Figure 8-10*).

INPUT OFFSET VOLTAGE

Ideally, when the input voltage of an op amp is zero, the output voltage should be zero. However, even with no signal applied across the inputs of the op amp, a dc voltage difference exists between the inputs, which is amplified, causing the output to be at a non-zero value. Input offset voltage V_{OS} is the input voltage required to zero the output. This applied voltage is the same magnitude as the original offset from zero, but of the opposite polarity.

Essentially every mismatch between the signal flow of the inverting inputs and the non-inverting input contributes to input offset voltage. The major contributor, however, is the V_{BE} mismatch of the differential input stage. V_{OS} is generally in the 1 to 10 mV range for non-FET input op amps. V_{OS} is undesirable in a direct-coupled circuit, because it is usually amplified by the circuit, causing a large dc error which is also temperature-dependent.

Effects of Offset Voltage on Applications

For inverting and non-inverting amplifier applications (*Figure 8-5*), the output voltage has a dc output level due to V_{OS}. Output offset voltage is given by

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) \qquad (3)$$

and derived from the following (see *Figure 8-11*):
Input bias current = 0

$$I_1 = \frac{V_{OS}}{R1} \qquad I_2 = I_1 \quad (I_{BIAS} = 0)$$

$$V_O = I_2\,R2 + I_1\,R1$$
$$V_O = I_1\,(R2 + R1)$$
$$V_O = \frac{V_{OS}}{R1}\,(R2 + R1) = V_{OS}\left(1 + \frac{R2}{R1}\right)$$

The output offset voltage given by Equation 3 is caused only by the input offset voltage V_{OS}. The output offset voltage caused by the input bias and offset current was described previously (Equation 1). The total output offset voltage is thus given by the sum of the two offsets.

Total dc output offset,

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + I_{B1}\,R2 - I_{B2}\,R3\left(1 + \frac{R2}{R1}\right) \qquad (4)$$

$$\text{For } R3 = \frac{R1\ R2}{R1 + R2}$$

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) + I_{OS}\,R2$$

where I_{OS} is the input offset current.

For R3 = 0

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) + I_{BIAS}\,R2$$

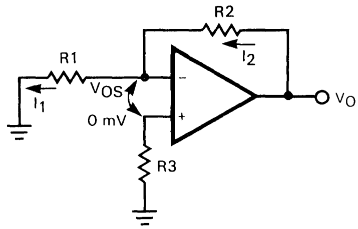


Figure 8-11

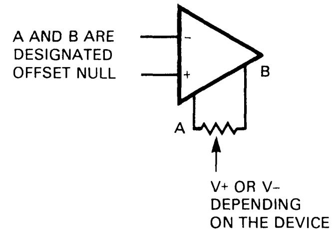


Figure 8-12

Here are some examples that will give an idea of the range of values discussed.

For a gain of 10 in an inverting configuration,
R2 = 100 kΩ, R1 = 10 kΩ, R3 = 9 kΩ

Using μA741C,
$V_{OS\ (max)}$ = 6 mV
$I_{OS(max)}$ = 200 nA
Output Offset = 86 mV max

Using μA714E,
$V_{OS(max)}$ = .075μV
$I_{OS(max)}$ = 3.8 nA
Output Offset = .38 mV

Using μAF771A,
$V_{OS(max)}$ = 2.0 mV
$I_{OS(max)}$ = 50 pA
Output Offset = 22 mV

The most objectionable factor of the input offset voltage and current is that they vary with temperature. Most op amp data sheets give input offset voltage values and temperature dependence curves.

Offset Voltage Nulling
In some op amps, offset voltage may be nulled with only an external potentiometer to two device leads (*Figure 8-12*). Usually what is happening internally is that one side of the input stage differential amplifier gets more or less current than the other side and thus causes a V_{BE} difference to null the initial V_{BE} mismatch.

Other Applications
If V_{OS} is considered as a small dc voltage source connected to an ideal op amp (*Figure 8-13*), its effect can be analyzed in almost every application. From *Figure 8-13* it is apparent that, in comparator applications, the output does not change state until the inverting input is at least a V_{OS} different from the non-inverting input. That is, if a zero crossing detector is being designed and the non-inverting input is connected to ground, the output would change state when the input reaches V_{OS} volts instead of zero volts.

High-Impedance Composite Input Offset Voltage
Common mode and differential input voltages can be calculated for any source resistances, equal or unequal. In the case of equal source resistors, at low impedances, V_{OS} dominates and at high

impedances, I_{OS} dominates. At some intermediate resistance, V_{OS} and I_{OS} effects are about equal and may add or cancel, depending on polarities. If they add, the composite offset will be larger than V_{OS} alone, maybe even larger than the data sheet limit for V_{OS}. To guard against this possibility, a high-impedance composite input offset voltage is tested and guaranteed at some specified source resistance, usually 10 k. Thus, it is common practice on data sheets to say that V_{OS} is guaranteed for all source resistances $\leq$ 10 k. Sometimes written V_{OS} 10 k, this is not an independent op amp parameter, but a calculated number determined by the interaction of the true independent parameters V_{OS} and I_{OS} with external source resistors.

OPEN LOOP VOLTAGE GAIN (AS A FUNCTION OF FREQUENCY)

As with any amplifier, the gain of an op amp is defined as the ratio of the change in output voltage to the change in input voltage causing it. A_{VOL} is used to indicate open-loop voltage gain, the gain of the amplifier without feedback. *See Figure 8-14.*

$$A_{VOL} = \frac{|V_{OUT}|}{|V_{IN}|} \tag{5}$$

Effects of Open Loop Voltage Gain on Applications

In a typical inverting application *(Figure 8-15),*

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R2}{R1} \tag{6}$$

This is true only if the op amp has infinite or very high open loop gain. However, in practical op amps, the A_{VOL} decreases with frequency until it becomes even less than one. The question is, to what frequency does Equation 6 hold true for a particular op amp?

If the derivation from Equation 6

$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

is assumed, an error arises due to neglecting A_{VOL} given by the equation:

$$\text{Closed loop gain error} = \frac{100}{1 + \dfrac{A_{VOL}\ R1}{R1 + R2}} \tag{7}$$

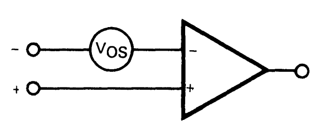


Figure 8-13

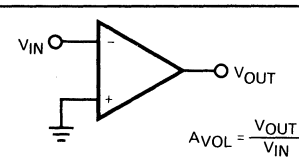


Figure 8-14

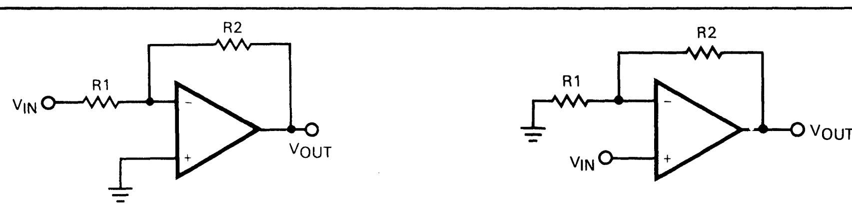


Figure 8-15

It is important to take Equation 7 into consideration when high accuracy dc operation is required and when considering frequency response. For instance, if the op amp is a μA741, connected in the inverting configuration *(Figure 8-15)* with R2/R1 = 100, $A_{VOL} = 10^4$ at 100 Hz as determined from the curve of *Figure 8-16.* From Equation 7, the error in assuming $V_{OUT}/V_{IN} = 100$ at 100 Hz is given by:

$$\frac{100}{1 + \frac{10^4 \times 1}{101}} = 1\%$$

At 10 kHz, the A_{VOL} of the μA741 is equal to 100, and the 1% error from Equation 7 becomes substantial.

$$\frac{100}{1 + \frac{100}{101}} = 50\% \;!$$

Note that when the open loop voltage gain is equal to the reciprocal of the feedback ratio (R2 + R1)/R1, the amplifier gain drops by 6 dB.

Choosing the Right Op Amp A_{VOL}

Use the following simple rule. For a dc closed loop gain y and a decrease in gain of no more than x per cent at a given maximum signal frequency f_{max}, an op amp is needed with an A_{VOL} at f_{max} given by:

$$A_{VOL} \geq \frac{100\,(1 + y)}{x} - (y + 1) \qquad (8)$$

For example, to achieve a dc closed loop gain of 100 with a decrease in gain of only 10% at 10 kHz, an operational amplifier is required with an A_{VOL} at 10 kHz of at least

$$\frac{100\,(1 + 100)}{10} - 100 + 1 = 911$$

One possibility is the μA725 which has an A_{VOL} of 1000 at 10 kHz with the proper compensation.

The graph in *Figure 8-17* is also helpful in choosing the right op amp and can be used for inverting or non-inverting configurations. The horizontal axis is the reciprocal of the feedback ratio

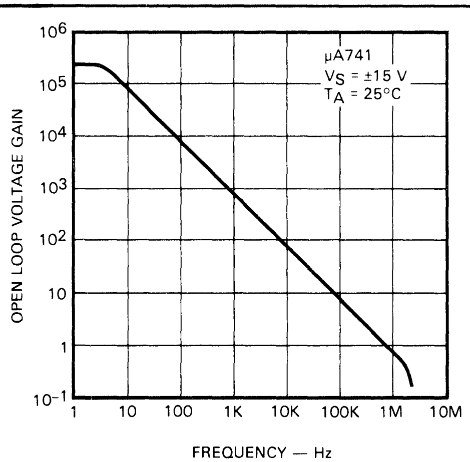


Figure 8-16

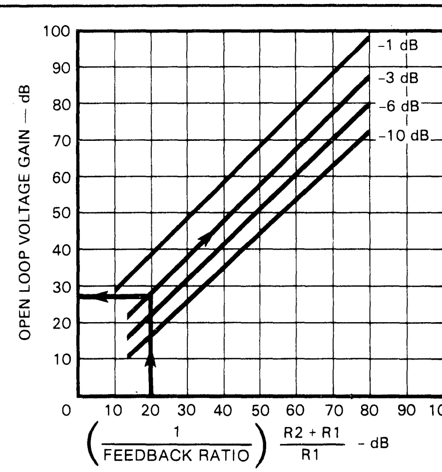


Figure 8-17

(R2 + R1)/R1 in dB. The vertical axis is the minimum A_{VOL} required to be within 1, 3, 6 or 10 dB of the dc or ideal closed loop gain, V_{OUT}/V_{IN}. For example, if R2 = 9 kΩ and R1 = 1 kΩ, (R2 + R1)/R1 = 20 dB. At the frequency where the A_{VOL} of the op amp is 28 dB, the closed loop gain will be 3 dB down from its dc value R2/R1. Therefore, to insure that amplifier gain does not fall off by more than 3 dB at f_{max}, choose an op amp with $A_{VOL} > 28$ dB at f_{max}.

Open loop voltage gain is not the only parameter that affects high frequency operation, however. Slew rate must also be considered.

SLEW RATE

Slew rate is the maximum rate of change of output voltage with respect to time, usually specified in volts per microsecond. For example, a 0.5 V/μs slew rate means that the output rises or falls no faster than 0.5 V every microsecond. Slew rate is also sometimes specified indirectly in data sheets as *output voltage swing as a function of frequency* or as *voltage follower large-signal pulse response.*

Causes of Slew Rate

Slew rate is a large-signal phenomenon caused by current limiting and saturation of an op amp internal stage. That limited current is the maximum current available to charge the compensation capacitance network, the capacitor connected to high-impedance nodes in the circuit to adjust small-signal frequency response. The voltage across the capacitor rises at a rate,

$$\frac{\Delta V}{\Delta t} = \frac{I}{C} \qquad (9)$$

This capacitor charging rate is reflected at the output and causes slew rate limiting. Slew rate limiting therefore occurs with large input signals that saturate the internal stages.

Effect of Slew Rate on Applications

In a simple application using a μA741 as a comparator (*Figure 8-18*), the output will go to about -14 V and then to +14 V each time the input signal crosses zero volts. The μA741 has a typical slew rate of 0.7 V/μs, determined under electrical specifications or calculated from the slope of the output curve in *Figure 8-19.* Therefore, the μA741 output will go to +14 V from -14 V in

$$\frac{28\ \text{V}}{0.7\ \text{V}/\mu\text{s}} = 40\ \mu\text{s}$$

If the full 28 V output swing is desired, the input signal must have at least 40 μs between zero crossings. That is, the maximum input signal frequency should be 1/(2 × 40 μs) or 12.5 kHz assuming 50% duty cycle. Even at that frequency, the output is triangular instead of square wave. For higher frequencies or a more square wave output, an op amp with a faster slew rate is needed.

As another example of the effect of slew rate, consider the simple amplifier with a gain of two in *Figure 8-20.* Again, the μA741 is used. Its open loop voltage gain as a function of frequency curve (*Figure 8-16*) indicates that the amplifier circuit will operate with a gain of two up to about 80 kHz.

What is the maximum input signal voltage that may be used up to 80 kHz? If the output is to be an undistorted sine wave, A sin ωt, then the rate of change of the output is

$$\frac{\Delta}{\Delta t} A \sin \omega t = A\omega \cos \omega t \qquad (10)$$

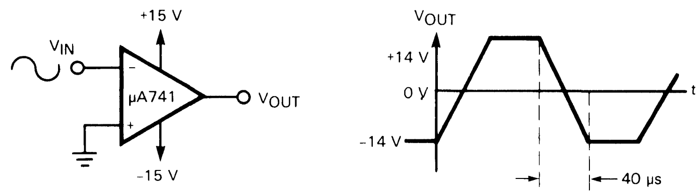


Figure 8-18

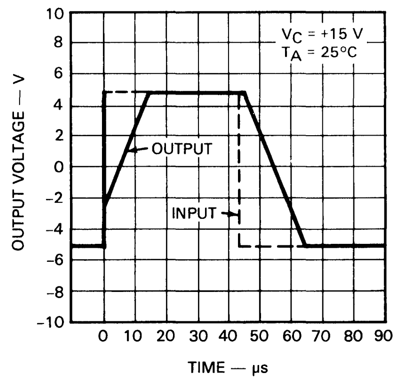


Figure 8-19

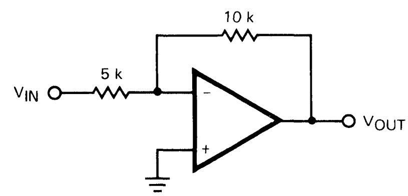


Figure 8-20

and the maximum rate of change of the output is $A\omega$. The minimum slew rate of the operational amplifier, therefore, must be equal to $A\omega$. Thus, with $\omega = 2\pi(80 \times 10^3) = 503000$ and the slew rate of the μA741 typically 0.7 V/μs, the maximum output swing A of the sine wave without distortion is

$$\frac{\text{slew rate}}{\omega} = \frac{0.7\ \text{V}/\mu\text{s}}{503000} = 1.4\ V_{pk}$$

or 2.8 $V_{pk\text{-}pk}$

The maximum input signal should, therefore, be less than 2.8/2$V_{pk\text{-}pk}$. The maximum output swing can also be easily read from the output voltage swing as a function of frequency curve on the data sheet (*Figure 8-21*). From this curve, the maximum output swing without distortion can be determined for different frequencies.

Summary

In applications where square wave outputs (comparators, oscillators, limiters, etc.) are expected, it is important to remember that the op amp output takes some time to change from one value to another. That time, which usually limits the maximum frequency of operation, is determined by the *change of output voltage divided by the slew rate.*

In applications where the output should be free of distortion, the slew rate determines the maximum frequency of operation for a desired output swing. The required slew rate can be determined by a simple formula. For a desired undistorted output voltage swing V_{pk} at a maximum frequency f_{max}, an op amp is needed with a slew rate given by

$$\text{slew rate} > 2\pi\, f_{max}\, V_{pk} \qquad (11)$$

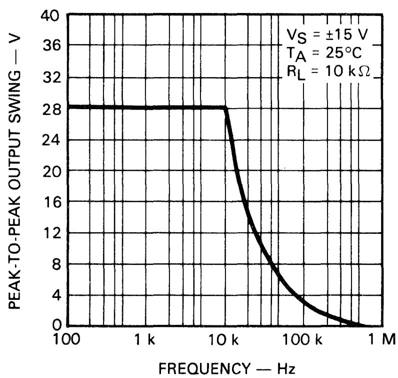


Figure 8-21

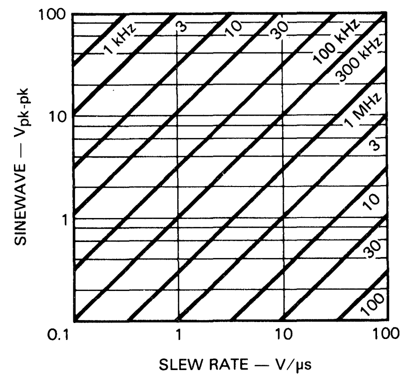


Figure 8-22

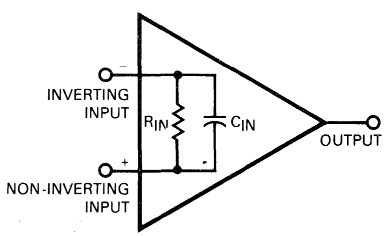


Figure 8-23

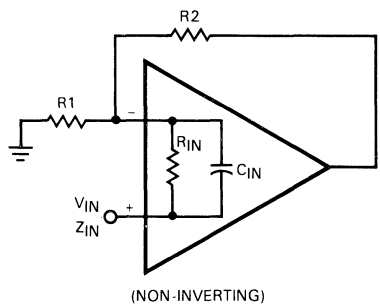


Figure 8-24

Figure 8-22 gives the slew rate required for different output swings at different frequencies. Another easy way to choose the right op amp is to check the data sheet curves of output voltage swing as a function of frequency (*Figure 8-21*). However, these curves are typical and slew rate varies as a function of supply voltage. Slew rates at different supply voltages are usually shown on the data sheet.

In some applications such as D/A or A/D converters, slew rate is not the only criterion for fast response. The settling time is another parameter to consider. High slew rate op amps sometimes have associated overshoot and ringing which may cause the output to take longer to reach a steady state than with slower slew rate op amps.

INPUT IMPEDANCE

The major factors in op amp input impedance are input resistance and input capacitance. Input resistance, or differential input resistance, usually specified in the data sheets, is the small signal resistance measured between the inverting and non-inverting inputs of the op amp. Input capacitance is the capacitance seen between the same two inputs *(see Figure 8-23).*

Effects of Input Impedance on Applications

The input impedance of an amplifier circuit with feedback is not only dependent on the op amp, but also on the circuit configuration.

Non-Inverting Configuration (Figure 8-24)
Input impedance of an amplifier in the non-inverting configuration is expressed as follows:

$$Z_{IN} = Z + \frac{A_{VOL}Z}{1 + \frac{R2}{R1}} \quad or \quad Z_{IN} = Z\left(1 + \frac{A_{VOL}}{1 + \frac{R2}{R1}}\right) \qquad (12)$$

where $A_{VOL}(\omega)$ is the open loop gain of the op amp and Z is the op amp input impedance. (See paragraph on *Open Loop Voltage Gain as a Function of Frequency.*)

As seen in Equation 12, the amplifier input impedance is equal to at least the op amp impedance and is usually much higher, due to high open loop gain.

For an op amp to operate properly, it is necessary to supply a certain dc current at the inputs. That current is given in the data sheets as input bias current and ranges in value from pA to μA depending on the op amp. In the non-inverting configuration of *Figure 8-24,* if V_{IN} has a series resistance of 1 MΩ and the input bias current of the op amp is 0.5 μA, there is a dc drop across the 1 MΩ series resistance of $0.5\ \mu A \times 1\ M\Omega = 0.5\ V$. This is independent of the signal (V_{IN}) amplitude. If V_{IN} is 1 V, there is 1 - 0.5 = 0.5 V at the non-inverting input. However, it is erroneous to assume that the op amp input impedance is 1 MΩ just because there is a straight voltage division. The drop is caused by input bias current and not by input impedance. If an ac signal is riding on the 1 V dc value of V_{IN}, the ac amplitude is not halved and only a 0.5 V offset is there constantly due to bias current. The signal amplitude is affected by the 1 MΩ series resistance and the op amp input impedance. However, dc characteristics are usually more important to consider than input impedance.

Inverting Configuration (Figure 8-26)
Input impedance of an amplifier in the inverting configuration is

$$Z_{IN} = R1 + \frac{R2\,(Z + R)}{A_{VOL}\,Z} \qquad (13)$$

$$Z_{IN} \simeq R1$$

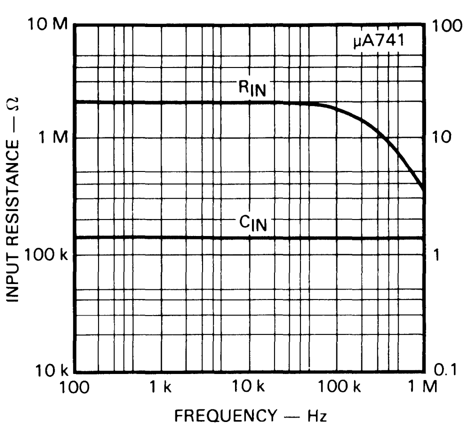


Figure 8-25

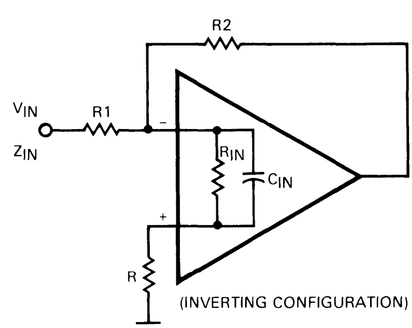


Figure 8-26

In this configuration, the effect of the op amp input impedance is minimal. The input impedance is at least R1; at high frequencies, as A_{VOL} decreases, the input impedance increases and the value of R2 (Z + R)/A_{VOL} Z becomes comparable to that of R1.

For all practical applications, however, it is safe to assume that the input impedance is just R1. Again, remember that a constant dc bias current is required at the inverting input to operate the op amp. The dc bias current limits the increase in value of R1. The higher the value of R1, the greater the magnitude of the dc offset voltage occurring at the output.

Another interesting point concerning Equation 13 is that the effect of increased input impedance at higher frequencies (A_{VOL} decreases in the denominator) is very similar to an inductance effect, usually referred to as Miller inductance. See Fairchild Application Note 321, "Operational Amplifiers as Inductors," for more detail.

USE OF OP AMP PARAMETERS IN DESIGN STEPS

The most important operational amplifier parameters have been presented and defined. These parameters are available on the data sheets for individual op amps and are useful in circuit design as well as determining which op amp to use for a specific application. Data sheet information can be used to determine circuit stability and, through a few simple steps, op amp selection for inverting and non-inverting configurations.

CIRCUIT STABILITY

Circuit stability can easily be determined by following one simple rule and referring to the phase response and open loop voltage gain curves on the op amp data sheets.

One consideration in determining circuit stability is the open loop voltage gain $A_{VOL}(\omega)$ of the op amp, the ratio of the change in output voltage to the change in input voltage. Open loop voltage gain versus frequency is readily available from the data sheets *(Figure 8-16).*

It is next necessary to consider the transfer functions for the inverting and non-inverting configurations shown in *Figures 8-27* and *8-28.* They can be expressed by the following equations:

Inverting

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z2}{Z2 + Z1}\right)\left(\frac{-A_{VOL}(\omega)}{1 + \left(\frac{A_{VOL}(\omega)}{1 + Z_2/Z_1}\right)}\right) \qquad (14)$$

Non-inverting

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{A_{VOL}(\omega)}{1 + \left(\frac{A_{VOL}(\omega)}{1 + Z_2/Z_1}\right)}\right) \qquad (15)$$

From these transfer functions, as well as from feedback theory, the stability of the inverting and non-inverting configurations can be determined by following this simple rule. The circuits will be stable if the magnitude of the term

$$\frac{A_{VOL}(\omega)}{1 + \frac{Z2}{Z1}}$$

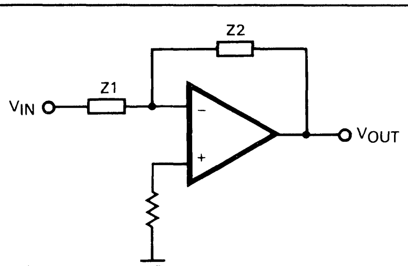


Figure 8-27

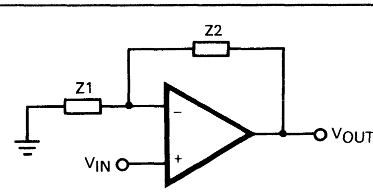


Figure 8-28

is less than unity when its phase angle reaches 180°. Stated another way, the phase angle of the above term must be less than 180° when its magnitude reaches unity. This rule is illustrated in the following example.

Amplifier and Voltage Follower Stability

In amplifiers where Z2 and Z1 are resistive, the circuit stability depends mainly on $A_{VOL}(\omega)$ because there is no phase shift in $1 + (Z2/Z1)$. For example, in the circuit of *Figure 8-29,* for R2 = R1,

$$1 + \frac{Z2}{Z1} = 2 \angle 0°$$

When $A_{VOL}(\omega) = 2$,

$$\frac{A_{VOL}(\omega)}{1 + \frac{Z2}{Z1}} = 1$$

From the open loop voltage gain curve *(Figure 8-30)*, it is apparent that $A_{VOL}(\omega) = 2$ at about 500 kHz with C_C = 30 pF. In *Figure 8-31*, note that the phase shift of the $A_{VOL}(\omega)$ is close to 180 ° at 5 MHz; therefore the circuit is potentially unstable or oscillatory. The phase is close to 110 ° at 500 kHz. Therefore the compensation, C_C = 30 pF, would be used instead of C_C = 3 pF since with C_C = 3 pF,

$$\frac{A_{VOL}(\omega)\ (5\ \text{MHz})}{1 + 1} = 1 \angle 180° \ (\text{unstable})$$

and with C_C = 30 pF,

$$\frac{A_{VOL}(\omega)\ (500\ \text{kHz})}{1 + 1} = 1 \angle 110° \ (\text{stable})$$

Summary

To determine stability for a resistive feedback circuit, the frequency at which $A_{VOL}(\omega)$ is equal to $1 + (R2/R1)$ is found on the open loop voltage gain curve. At that frequency, the ratio

$$\frac{A_{VOL}(\omega)}{1 + \frac{Z2}{Z1}} = 1$$

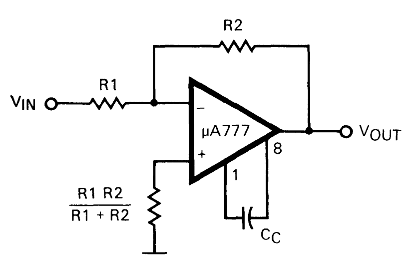


Figure 8-29

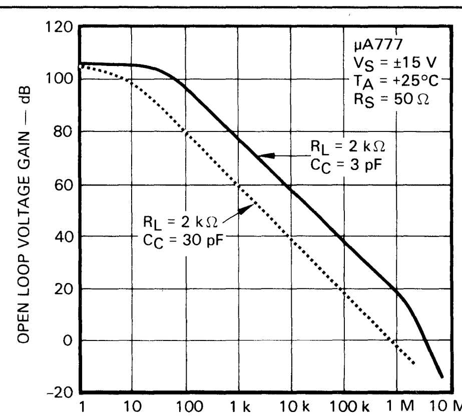


Figure 8-30

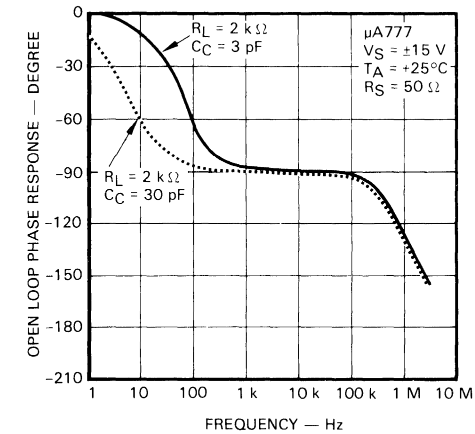


Figure 8-31

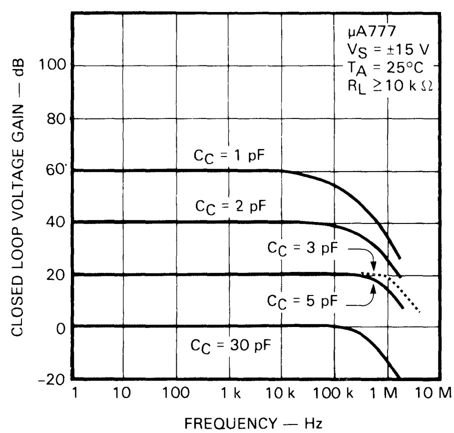


Figure 8-32

The phase shift at that frequency is then read on the op amp phase response curve. If the phase shift is less than 180°, the configuration is stable; if it is more than 180°, the configuration is unstable. Often the results of these computations are given in the data sheet as frequency response for various closed loop gains using recommended compensation networks *(Figure 8-32).*

When Z2/Z1 is non-resistive as in integrators and differentiators, the same rule holds but the phase response of both $A_{VOL\ (\omega)}$ and 1 + (Z2/Z1) must be considered. For more information on stability rules for integrators and differentiators, see Fairchild Application Note 289, "Applications of the μA741 Operational Amplifier."

DESIGN STEPS FOR INVERTING AMPLIFIERS

The first step in op amp selection is to establish circuit specifications necessary for the application. For the purpose of discussion, the following specs are assumed:

Gain = A = -9
Minimum 3 dB down frequency f_C = 10 kHz
Maximum input signal amplitude V_1 = 2 V_{pk-pk}
Maximum dc output offset voltage $V_{O\ (max)}$ = ± 25 mV
Input resistance R_{IN} = 10 kΩ
DC drift from 0 to 70° $\Delta V_{O\ (max)} \leq$ 15 mV

Step 1: Circuit Configuration

Using the inverting circuit of *Figure 8-33,* from Equation 6:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-R2}{R1} = A = -9;\ \frac{R2}{R1} = 9$$

Step 2: Frequency Response

The first op amp specification to check is the minimum open loop voltage gain, A_{VOL}, needed to meet the amplifier frequency response requirement. This is easy to do by using the graph in *Figure 8-17.* Since R2/R1 = 9, then (R2 + R1)/R1 = 10; locate the 10 ratio (20 dB) on the (R2 + R1)/R1 axis. Go up to the 3 dB line and read, on the vertical axis, the minimum A_{VOL} required, 28 dB. Therefore,

8

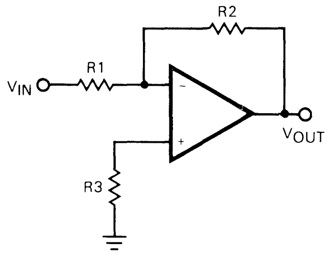


Figure 8-33

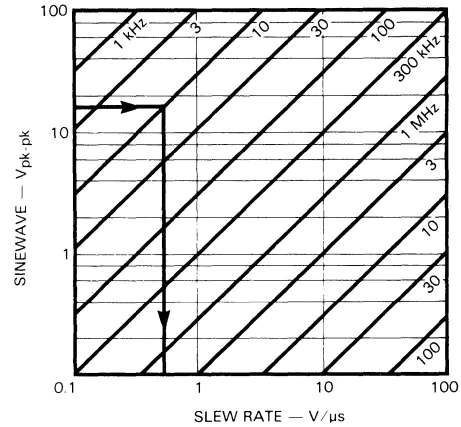


Figure 8-34

to insure that amplifier gain does not fall off by more than 3 dB at f_C, the op amp must have an open loop gain of:

(First Requirement) $A_{VOL} \geq$ 28 dB at f_C (10 kHz)

Step 3: Output Swing

Since the maximum input signal amplitude is 2 V_{pk-pk}, the maximum output swing will be 18 V_{pk-pk}. Therefore, an op amp is needed with a slew rate fast enough to give 18 V_{pk-pk} up to 10 kHz. By checking *Figure 8-34*, it is apparent that an op amp is required with:

(Second Requirement) slew rate $\geq$ 0.8 V/μs

Step 4: Maximum DC Output Offset Voltage V_O

The dc output offset voltage, V_O, for the circuit in *Figure 8-33* is given by the following derivations from Equation 4:

For R3 = 0

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + I_{BIAS} R2 \quad (16)$$

For R3 = (R1 in parallel with R2)

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + R2\, I_{OS} \quad (17)$$

where

V_{OS} = input offset voltage
I_{BIAS} = input bias current
I_{OS} = input offset current

Unless the output offset voltage spec is very wide, it is usually more economical to add R3 than to use a very low input bias current op amp. For the example in this discussion, R3 = (R1 in parallel with R2). From Equation 16 it can be seen that the V_O value will be low when R2 is small; therefore, the smallest possible value should be chosen for R2.

For the inverting configuration, the input resistance R_{IN} is at least R1. Therefore, choose R1 so that

$$R1 \geq R_{IN} \geq 10k\Omega$$

From the above and Step 1, R2/R1 = 9 and R1 $\geq$ 10 kΩ; therefore when R1 is 10 kΩ, R2 = 90 kΩ, and R3 = 9 kΩ. Equation 16 becomes

$$V_O = (1 + 9)\ V_{OS} + (90 \times 10^3)\ I_{OS}$$

Thus, an op amp is needed such that V_{OS} and I_{OS} give:

$$\text{(Third Requirement)}\ 10\ V_{OS} + (90 \times 10^3)\ I_{OS} = V_{O(max)} \leq 25\ \text{mV}$$

To simplify the search for an op amp to meet this requirement, look first for one that has the following specifications:

$$V_{OS} < \frac{V_{O(max)}}{10} = 2.5\ \text{mV}$$

$$I_{OS} < \frac{V_{O(max)}}{90 \times 10^3} = 270\ \text{nA}$$

Step 5: Drift

Drift is given by:

$$\text{(Fourth Requirement)}\quad \Delta V_O = 10\ \Delta\ V_{OS} + (90 \times 10^3)\ \Delta I_{OS} \leq \Delta V_{O(max)}\ (15\ \text{mV})$$

where ΔV_{OS} and ΔI_{OS} are the changes in input offset voltage and input offset current over the 0 to 70 ° temperature range.

DESIGN STEPS FOR NON-INVERTING AMPLIFIERS

The design steps for non-inverting amplifiers are similar to those for inverting amplifiers. For this example, the following specifications are assumed:

Gain = A = 10
Minimum 3 dB down frequency f_c = 10 kHz
Maximum input signal amplitude V_1 = 2 V_{pk-pk}
Input resistance R_{IN} = 5 MΩ minimum
Maximum dc output offset voltage $V_{O(max)}$ = $\pm$ 25 mV
DC drift from 0 to 70° $\Delta V_{O(max)} \leq$ 15 mV

8

Step 1: Circuit Configuration

For the non-inverting circuit of *Figure 8-35,* the equation for the gain is

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + R1}{R1} = A = 10$$

Step 2: Frequency Response

As with inverting amplifier design, the first op amp specification to check is the minimum open loop voltage gain, A_{VOL}, needed to meet the amplifier frequency response requirement. This is easy to do from the graph in *Figure 8-17.* Since (R2 + R1)/R1 = 10, locate the 10 ratio (20 dB) on the (R2 + R1)/R1 axis. Go up to the 3 dB line and read, on the vertical axis, the minimum A_{VOL} required,

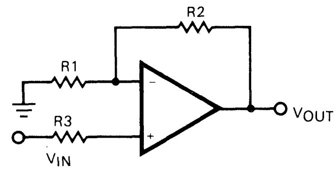


Figure 8-35

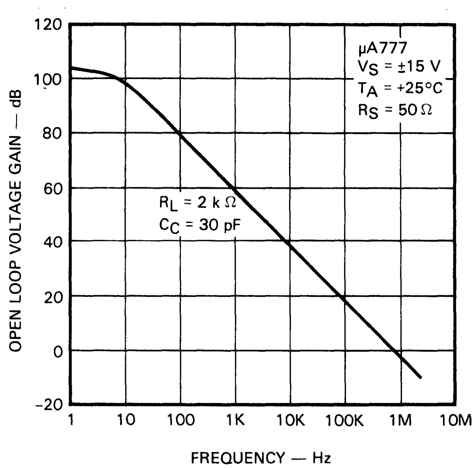


Figure 8-36

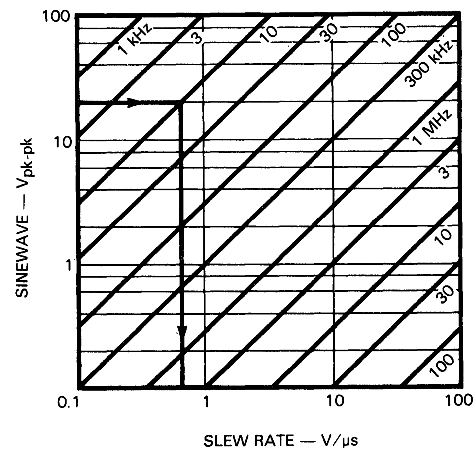


Figure 8-37

28 dB. Therefore, to insure that amplifier gain does not fall off by more than 3 dB at f_c, the op amp must have an open loop gain of:

(First Requirement) $A_{VOL} \geq 28$ dB at f_c (10 kHz)

Examination of the open loop voltage gain versus frequency curves on various op amp data sheets will quickly determine which devices will meet this requirement. *Figure 8-36* is a good example. An op amp with a gain bandwidth product of 250,000 (28 dB X 10 kHz) will do the job, assuming the op amp has just one pole.

Step 3: Output Swing

Since the maximum input signal amplitude is 2 V_{pk-pk}, the maximum output swing will be 20 V_{pk-pk}. Therefore, an op amp is needed with a slew rate fast enough to give 20 V_{pk-pk} up to 10 kHz. From *Figure 8-37,* it is apparent that an op amp is required with:

(Second Requirement) slew rate $\geq$ 0.85 V/μs

Step 4: Input Resistance

The input impedance for the non-inverting configuration is given by Equation 13:

$$Z_{IN} = Z\left(1 + \frac{A_{VOL}}{1 + \frac{R2}{R1}}\right)$$

where Z is the op amp input impedance and R3 << Z.

The op amp for this design must satisfy the amplifier input impedance requirement of 5 MΩ up to at least 10 kHz. In step 2, it was determined that the op amp must also have an A_{VOL} of no less than **28 dB (or 25 V/V) at 10 kHz. Therefore, the required op amp must have an imput impedance (Z) at 10 kHz of at least the following:**

$$\text{(Third Requirement) } Z \geq \frac{Z_{IN(min)}}{\left(1+\dfrac{A_{VOL}\,(10\text{ kHz})}{\left(1+\dfrac{R2}{R1}\right)}\right)} = \frac{5\text{ M}\Omega}{1+\dfrac{25}{10}} = \frac{5\text{ M}\Omega}{3.5}$$

$$Z \geq 1.4\text{ M}\Omega$$

From curves,such as *Figure 8-25,* of input resistance and input capacitance as a function of frequency, it is easy to select an op amp to meet the input impedance requirement.

Step 5: Maximum DC Output Offset Voltage, V_O

The dc output offset voltage, V_O, for the circuit in *Figure 8-35* is again given by following Equa-16 and 17.

For R3 = 0

$$V_O = \left(1+\frac{R2}{R1}\right)V_{OS} + I_{BIAS}\,R2 \qquad (16)$$

For R3 = (R1 in parallel with R2)

$$V_O = \left(1+\frac{R2}{R1}\right)V_{OS} + R2\,I_{OS} \qquad (17)$$

where

V_{OS} = input offset voltage
I_{BIAS} = input bias current
I_{OS} = input offset current

Unless the output offset voltage spec is very wide, it is usually more economical to add R3 than to use a very low input bias current op amp. For the example in this discussion, R3 = R1||R2. From Equation 16, it can be seen that the V_O value will be low when R2 is small; therefore the smallest possible value should be chosen for R2.

The minimum limit to this value is dependent on the capability of the op amp to drive R2. Since op amp parameters usually specify a load resistor of 2 kΩ or 10 kΩ, R2 should be larger than 10 kΩ. From steps 1 and 4:

$$\frac{R1+R2}{R1} = 10 \text{ and } R3 \ll Z$$

Therefore, choose R1 = 10 kΩ; then R2 = 90 kΩ and R3 = 9 kΩ and Equation 18 becomes

$$V_O = (1 + 9)\ V_{OS} + (100 \times 10^3)\ I_{OS}$$

Thus, an op amp is needed such that V_{OS} and I_{OS} give:

(Fourth Requirement) $10\ V_{OS} + (100 \times 10^3)\ I_{OS} \leq 25\ \text{mV} \leq V_{O(max)}$

To simplify the search for an op amp to meet this requirement, look first for one that has the following specifications:

$$V_{OS} < \frac{V_{O(max)}}{10} \text{ or } < \frac{25\ \text{mV}}{10}$$

$$I_{OS} < \frac{V_{O(max)}}{100 \times 10^3} \text{ or } < 250\ \text{nA}$$

Step 6: Drift

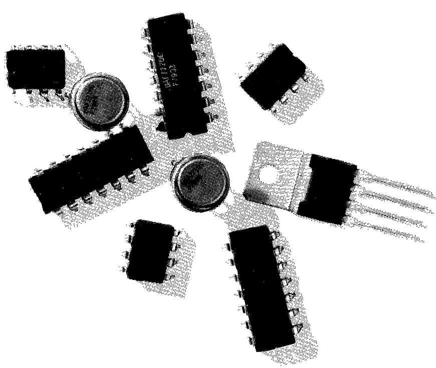
Drift is given by:

(Fifth Requirement) $\Delta V_O = 11\ \Delta V_{OS} + (100 \times 10^3)\ \Delta I_{OS} \leq \Delta V_{O(max)} (15\ \text{mV})$

where ΔV_{OS} and ΔI_{OS} are the changes in input offset voltage and input offset current over the 0 to 70° temperature range.

FINAL HINTS IN CHOOSING THE RIGHT OP AMP

It is usually best to start by finding the op amps that meet the first and second requirements; this will eliminate many. Then check the good ones against the remaining requirements starting with the lowest cost op amp. There are usually other specifications such as supply voltage and current, supply rejection, load current, common mode rejection, etc., that should be considered. However, the op amps that meet the above requirements will narrow down the field of choice to only a few, which can then be checked further to see if they meet the rest of the specifications.



ORDER INFORMATION, DICE POLICY AND PACKAGE OUTLINES

ORDER INFORMATION

Three basic units of information are contained in the code.

μA741	T	C
Device Type	Package Type	Temperature Range

DEVICE TYPE

This group of alpha numeric characters defines the data sheet which specifies the device functional and electrical characteristics.

PACKAGE TYPE

One letter represents the basic package style.

D = Dual In-line Package (Hermetic, Ceramic)
F = Flatpak (Hermetic)
H = Metal Can Package
J = Metal Power Package (TO-66 Outline)
K = Metal Power Package (TO-3 Outline)
P = Dual In-line Package (Molded)
R = Mini DIP (Hermetic, Ceramic)*
T = Mini DIP (Molded)
U = Power Package (Molded, TO-220 Outline)

*Refer to individual data sheets for details. For special requirements, contact factory.

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the PACKAGE OUTLINES section of this catalog.

TEMPERATURE RANGE

Three basic temperature grades are in common use:

C = Commercial	M = Military	V = Industrial
0°C to +70/75°C	-55°C to +125°C	-20°C to +85°C
	-55°C to + 85°C	-40°C to +85°C

Exact values and conditions are indicated on the individual data sheets.

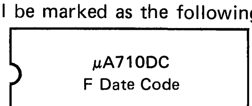
EXAMPLES

1. μA710FM
   This number code indicates a μA710 Voltage Comparator in a flatpak with military temperature rating capability.
2. μA725EHC
   This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal can with a commercial temperature rating capability.

9

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog linear circuits will be marked as the following example:



UNIQUE 38510 PROCESSING

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements (QB, QC) after the standard order code.

Detailed ordering procedures are provided in the OEM price list.

MATRIX VI PROGRAM

Additional screening to the Fairchild Matrix VI program is indicated by the QM or QR suffix to the standard order code.

OLD ORDER CODES

Devices may continue to be purchased against old order codes (Example: U5R7723393; now 723HC). However, all products will be marked with new order codes unless otherwise specified.

GENERAL INFORMATION

Fairchild linear integrated circuits, constructed using the Fairchild Planar* epitaxial process, are available in dice form incorporating these features:

- Commercial or Military Selection (Military Limits Probed at 25°C)
- MIL-STD-883, Method 2010.2, Condition B Visual
- Gold Backing
- Glass Passivation
- Protective Packaging

ELECTRICAL CHARACTERISTICS

Each die electrically tested at 25°C to guarantee commercial dc parameters.

Military grade dice are guardband tested at 25°C dc to guarantee military temperature range operation.

QUALITY ASSURANCE

All Fairchild linear dice are 100% visually inspected and conform to MIL-STD-883, Method 2010.2, Condition B. In addition, quality control visually inspects the dice to a given sampling plan.

Each die is gold backed to aid die attach. Most diec are available with glass passivation coating with only the bonding pads exposed.

SHIPPING PACKAGES

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

ORDER INFORMATION

Each linear integrated circuit die has a unique order code which describes the device type, the dice designation and type of electrical tests performed. The dice designation is denoted by a "C" and wafer designation is denoted by a "W." Examples follow:

Generic Type	Dice Order Code	Wafer Order Code
μA741C**	μA741CC	μA741WC
μA3045	μA3045CC	μA3045WC
75450B	75450BCC	75450BWC
μA101A	μA101ACC	μA101AWC
μA796C	μA796CC	μA796WC

**Some device types imply a military or commercial range by the generic type. Where this does not occur the suffix should be:

XM Military Grade Die or XC Commercial Grade Die

SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, Fairchild will negotiate with the customer to meet his requirements.

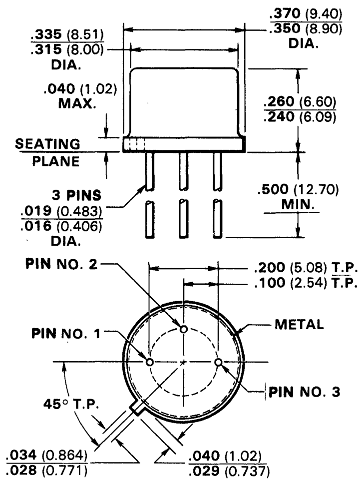
PRODUCT AVAILABLE IN DICE FORM

Please refer to FSC OEM Price List for product available in die form.

*Planar is a patented Fairchild process.

9

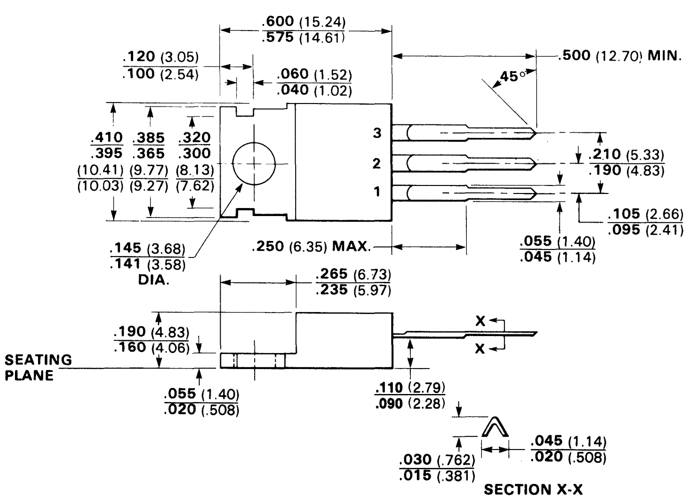
In Accordance with JEDEC (TO-39) OUTLINE



BF

NOTES:
Pins are gold-plated kovar
Pin 3 connected to case
50 mil kovar header
Package weight is 1.23 grams

In Accordance with JEDEC (TO-220) OUTLINE



EC

NOTES:
Package is silicone plastic with boron nickel-plated copper tab and pins
Mechanically interchangable with TO-66
Center pin is electrical contact with the mounting tab
Package weight is 2.1 grams

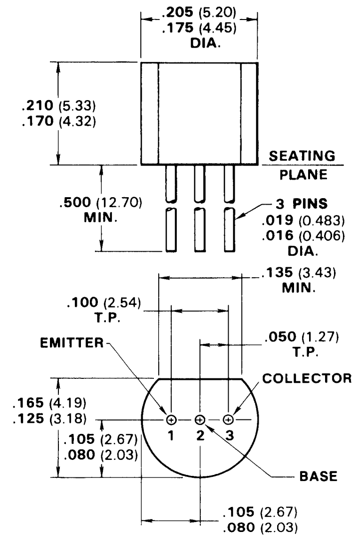
GH

NOTES:
Package is silicone plastic with nickel-plated copper tab and pins
Center pin is electrical contact with the mounting tab
Package weight is 2.1 grams
*Mechanically interchangable with TO-66

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

In Accordance with
JEDEC TO-92 OUTLINE

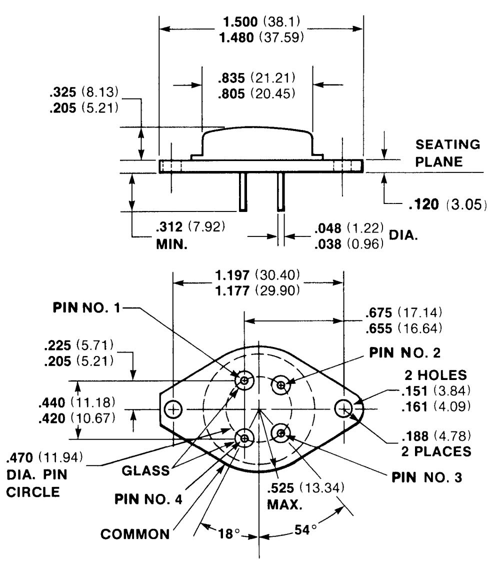


EI

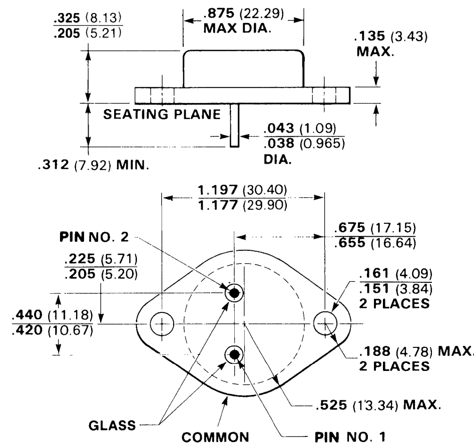
NOTES:

Pins are tin-plated copper
Package material is transfer molded thermosetting plastic
ECB configuration
Package weight is 0.25 gram

In Accordance with JEDEC (TO-3)
OUTLINE-4-PIN



JEDEC TO-3 OUTLINE*



GJ

NOTES:

Pins are gold-plated or solder dipped alloy 52
Pins 1 and 2 electrically isolated from case
Case is third electrical connection
Aluminum package with copper slug, pins are soldered in
Package weight is 7.4 grams
Aluminum cap (may be dome-type, depending prod. line)
*Except pin diamater

GK

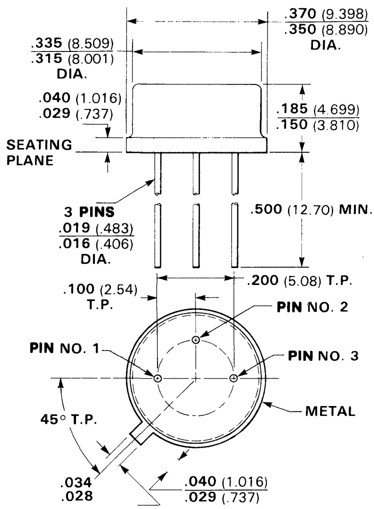
NOTES:

Pins are gold-plated or solder dipped alloy 52
All pins electrically isolated from case
Package weight is 7.4 grams
*Except number of pins and pin diameter

All dimensions in inches (bold) and millimeters (parentheses)

9

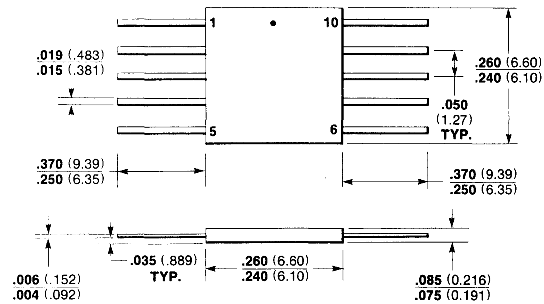
JEDEC TO-39 OUTLINE*



HC

NOTES:
Pins are gold-plated kovar
Pin 3 connected to case
Package weight is 1.23 grams
50 mil kovar header
*Dimensions same as JEDEC TO-39 except for can height

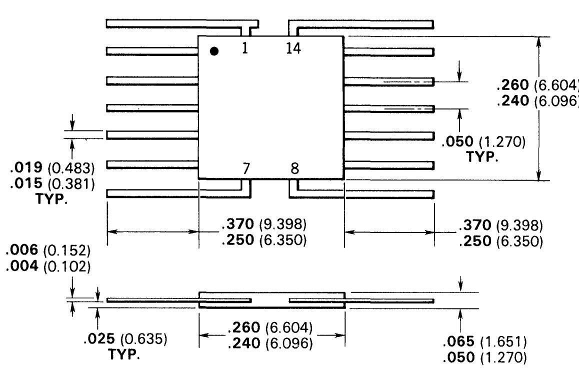
In Accordance with JEDEC (TO-91) OUTLINE 10-PIN CERPAK



3F

NOTES:
Pins are tin plated 42 alloy
Hermetically sealed alumina package
Cavity size is .130 diamater
Package weight is 0.26 grams

In Accordance with JEDEC (TO-86) OUTLINE 14-PIN CERPAK

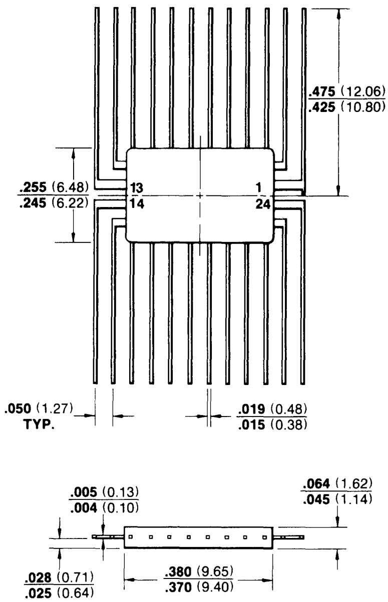


3I

NOTES:
Pins are tin-plated 42 alloy
Hermetically sealed alumina package
Pin 1 orientation may be either tab or dot
Cavity size is .130
Package weight is 0.26 gram

All dimensions in inches (bold) and millimeters (parentheses)

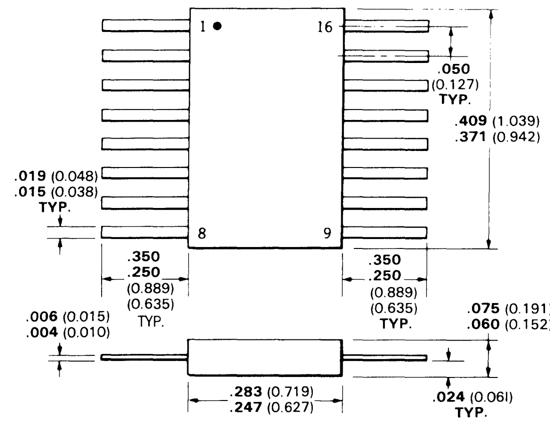
24-PIN FLATPAK



3M

NOTES:
Pins are gold-plated kovar
Package material is kovar
Cavity size is .120 x .235 (3.05 x 5.97)
Package weight is 0.8 gram

16-PIN CERPAK



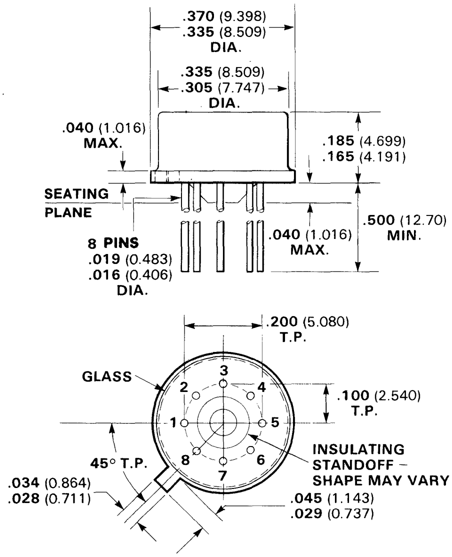
4L

NOTES:
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

All dimensions in inches (bold) and millimeters (parentheses)

9

In Accordance with JEDEC (TO-99) OUTLINE



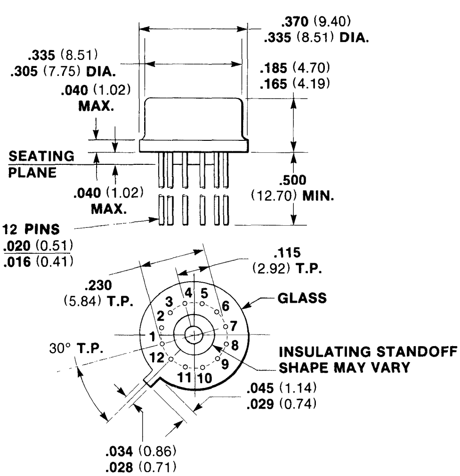
5B

NOTES:
Pins are gold-plated kovar
Seven pins thru leads No. 4 connected to case
15 mil kovar header
Package weight is 1.22 grams

5S

NOTES:
Pins are solder dipped to seating plane.
Seven pins thru, pin No. 4 connected to case.
Package weight is 1.22 grams.

JEDEC TO-101 OUTLINE



5D

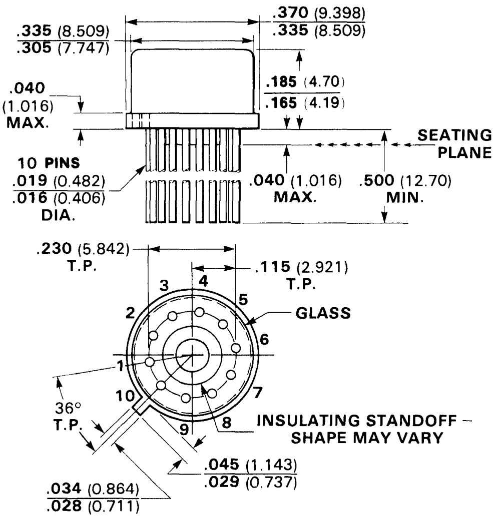
NOTES:
Pins are solder dipped to the seating plane.
Twelve pins thru
*Similar to JEDEC TO-101
Package weight is 1.4 grams

5G

NOTES:
Pins are gold-plated kovar.
Twelve pins thru
*Similar to JEDEC TO-101
Package weight is 1.08 grams.

All dimensions in inches (bold) and millimeters (parentheses)

In Accordance with
JEDEC (TO-100) OUTLINE



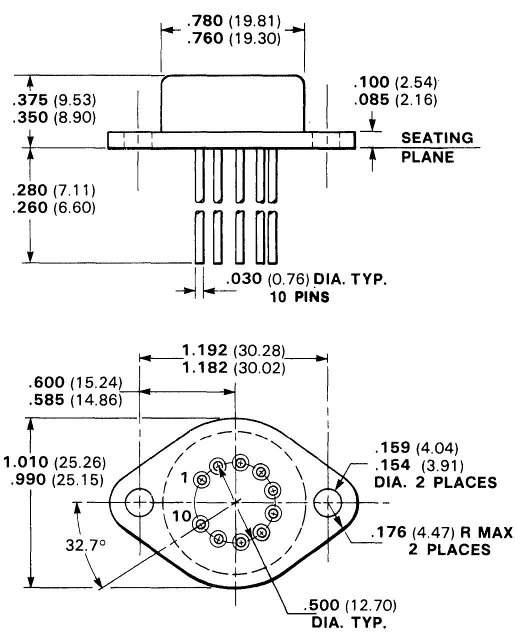
5N

NOTES:
Pins are solder dipped to the seating plane.
Nine pins thru pin No. 5 is connected to case.
15 mil kovar header
Package weight is 1.32 grams.

5F

NOTES:
Pins are gold-plated kovar
Nine pins through, pin 5 connected to case
15 mil kovar header
Package weight is 1.32

JEDEC TO-3 OUTLINE*



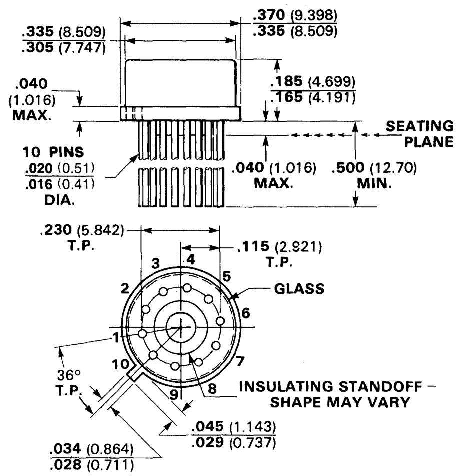
5H

NOTES:
Package material is nickel-plated CRS
Pin material is alloy 52
Glass material is corning 9010
Pin, post and base gold-plated
*Except height and number of pins

All dimensions in inches (bold) and millimeters (parentheses)

9

In Accordance with JEDEC (TO-100) OUTLINE



5I

NOTES:
Pins are solder dipped to the seating plane
Ten pins thru
High RTH package
15 mil kovar header
Package weight is 1.32 grams

5E

NOTES:
Pins are gold-plated kovar
Ten pins thru
15 mil kovar header
Package weight is 1.32 grams

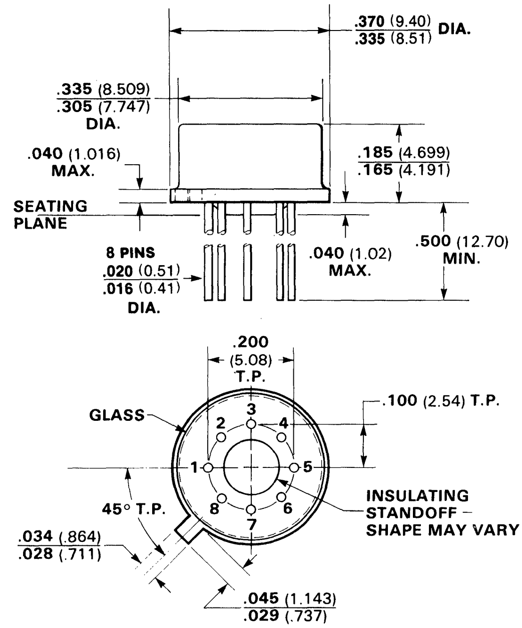
5Q

NOTES:
Pins are solder dipped to the seating plane
Ten pins thru
15 mil kovar header
Package weight is 1.32 grams

5U

NOTES:
Pins are gold-plated kovar
Ten pins through
High RTH package
15 mil kovar header
Package weight is 1.32 grams

In Accordance with JEDEC (TO-99) OUTLINE



5M

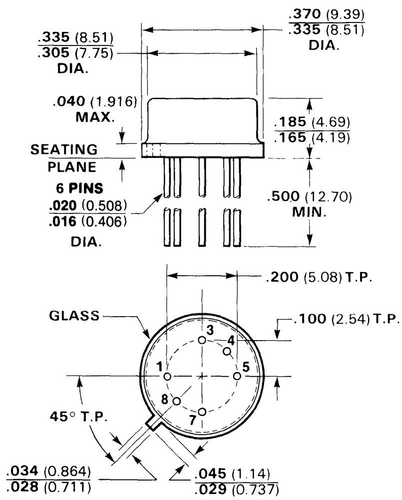
NOTES:
Pins are solder dipped to seating plane
Eight pins thru
15 mil kovar header
Package weight is 1.22 grams

5T

NOTES:
Pins are gold-plated kovar.
Eight pins thru
*Dimensions similar to JEDEC TO-100 except for 8 pins spaced 45° apart.
Package weight is 1.22 grams.

All dimensions in inches (bold) and millimeters (parentheses)

In Accordance with
JEDEC TO-78 OUTLINE



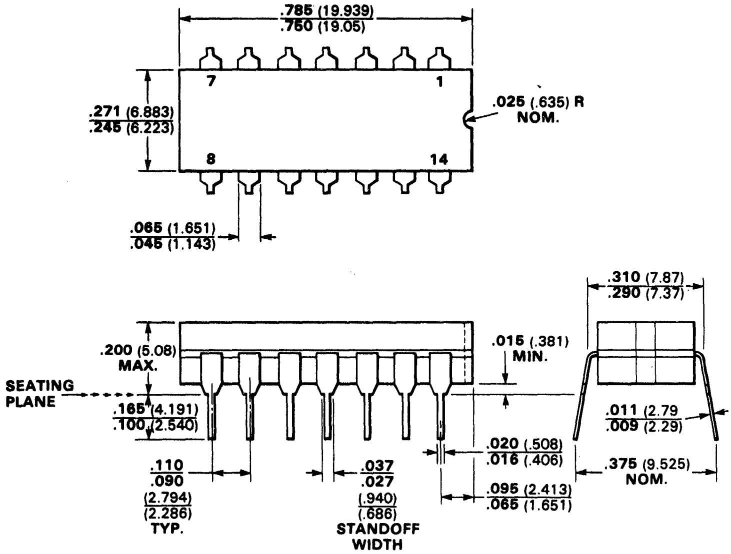
5Z

NOTES:
Pins are gold plated kovar.
Six pins thru.
Pins 2 and 6 are omitted.
Package weight is 0.95 gram.

All dimensions in inches (bold) and millimeters (parentheses)

9

In Accordance with
JEDEC (TO-116)
14-PIN HERMETIC DUAL IN-LINE



6A

NOTES:

Pins are intended for insertion in hole rows on .300" (7.620) centers

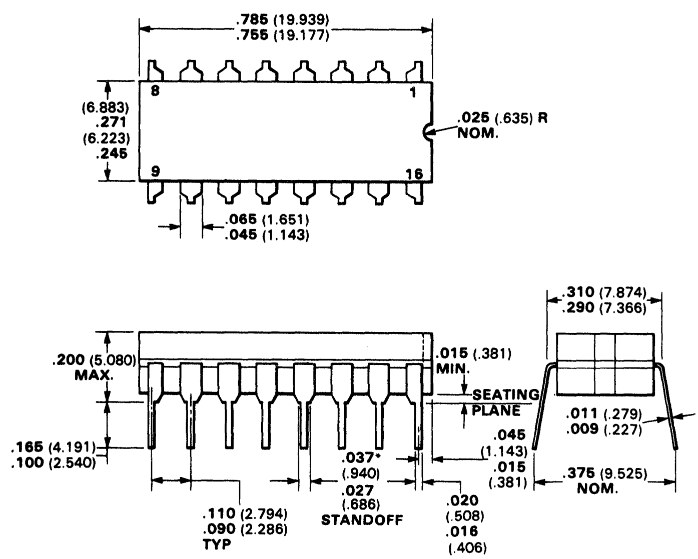
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

Pins are alloy 42

Package weight is 2.0 grams

16-PIN HERMETIC DUAL IN-LINE



6B

NOTES:

Pins are tin-plated 42 alloy

Pins are intended for insertion in hole rows on .300" centers (7.62)

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch diameter pin (0.51)

Hermetically sealed alumina package

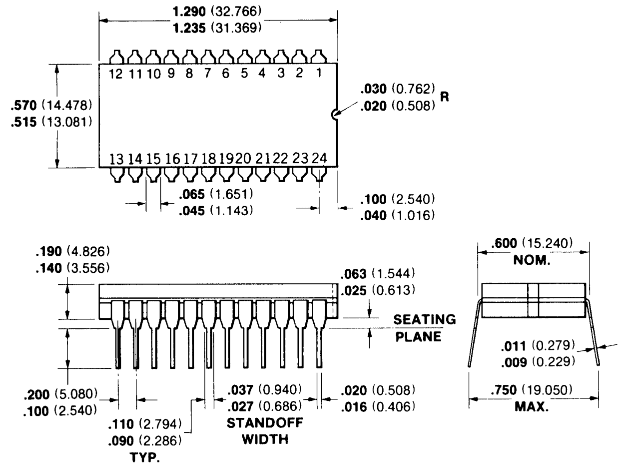
Cavity size is .110 x .140 (2.79 x 3.56)

Package weight is 2.0 grams

*The .037-.027 dimension does not apply to the corner pins

All dimensions in inches (bold) and millimeters (parentheses)

24-PIN DUAL IN-LINE

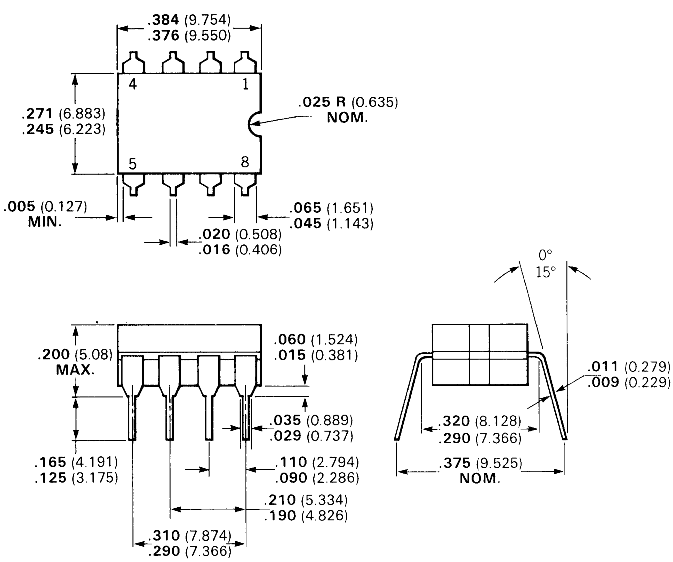


6N

NOTES:

Pins are tin-plated 42 alloy
Package material is alumina
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is .230 x .230 (5.84 x 5.84)
Package weight is 6.5 grams

8-PIN DUAL IN-LINE



6T

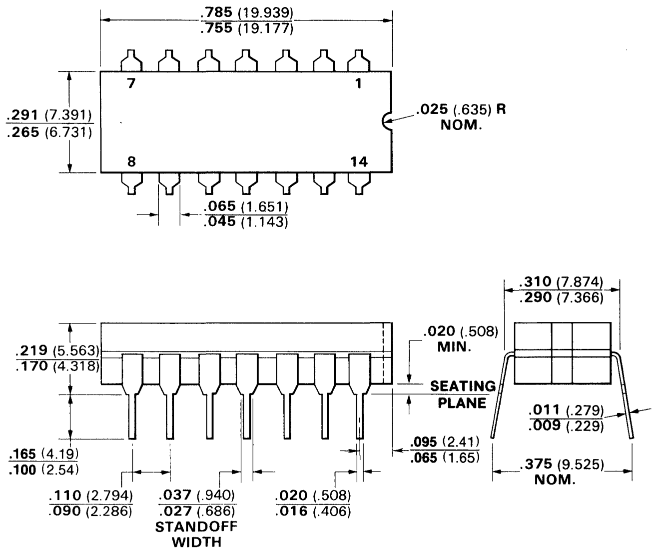
NOTES:

Pins are tin-plated kovar
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Hermetically sealed alumina package
Cavity size is .110 x .140
Package weight is 1.0 grams

All dimensions in inches (bold) and millimeters (parentheses)

9

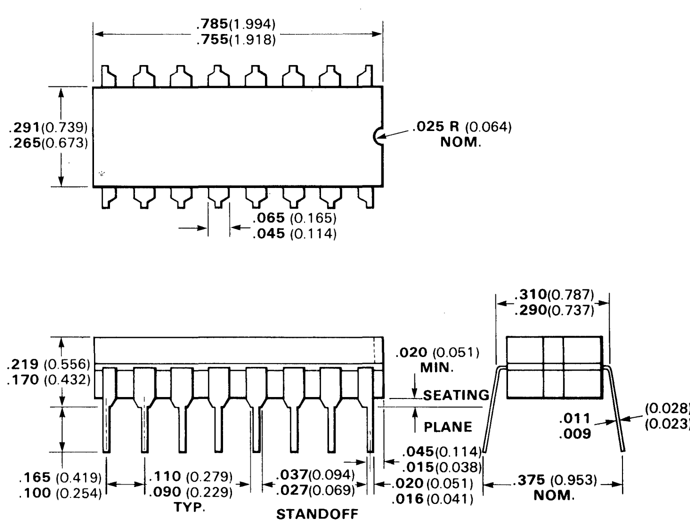
In Accordance with
14-PIN DUAL IN-LINE
(JEDEC TO-116 OUTLINE)



7A

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for a conventional .020" (0.51) diameter pin.
Hermetically sealed alumina package.
Cavity size is .130 x .250 (3.30 x 6.35)
*Similar to JEDEC TO-116 except for package width.
Package weight is 2.2 grams.

16-PIN DUAL IN-LINE

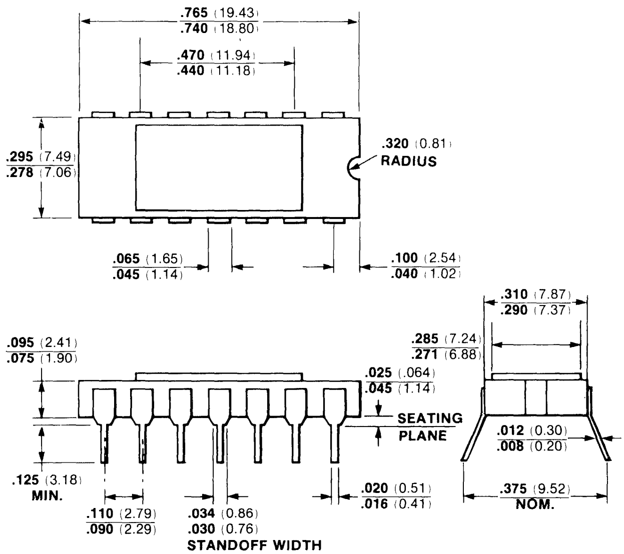


7B

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin (0.51)
Hermetically sealed alumina package
Cavity size is .130 x .230
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

All dimensions in inches (bold) and millimeters (parentheses)

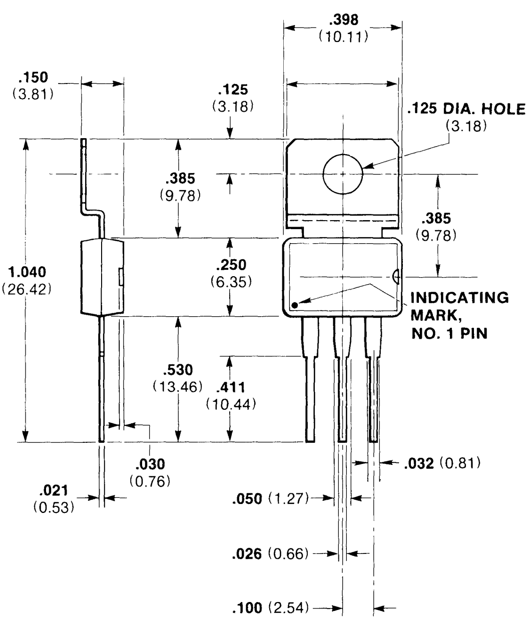
14-PIN DUAL IN-LINE (METAL CAP)



7N

NOTES:
Pins are gold-plated kovar
Package material is alumina
Pins are intended for insertion in hole rows on .300" centers (7.62)
They are purposely shipped "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Low temperature seal
Cavity size is .170 x .215 (4.32 x 5.46)
Package weight is 1.3 grams.

3-PIN SINGLE SIDE POWER PLASTIC MINIDIP



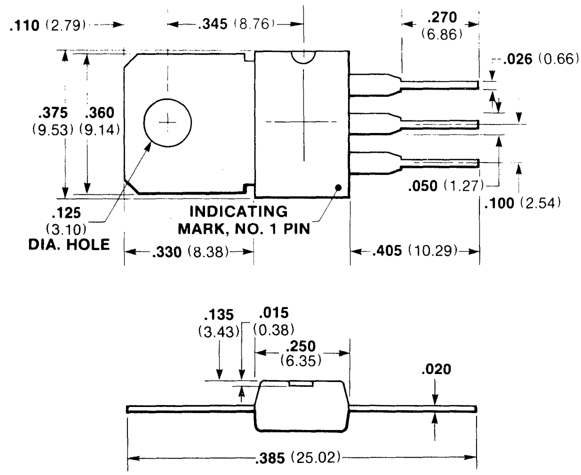
8Y (U-1)

NOTES:
Pins are tin plated copper
Package weight is 0.6 gram
Package material is plastic
Tab is electrically insulated from pins
This package is intended to be mounted with the tab flush with the top of the P.C. board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.
All dimensions nominal.

All dimensions in inches (bold) and millimeters (parentheses)

9

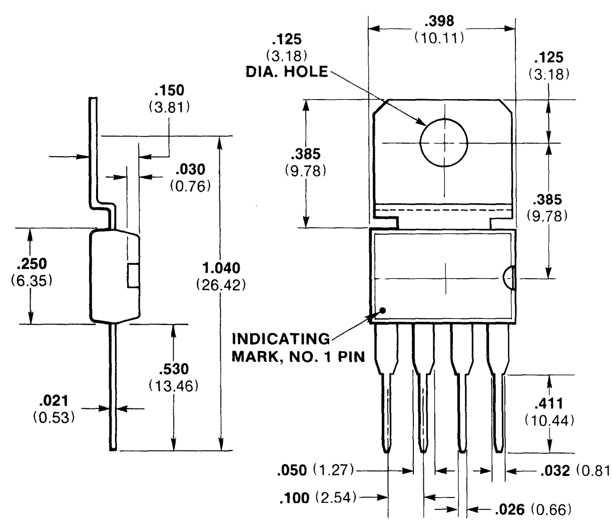
3-PIN SINGLE SIDE POWER PLASTIC MINIDIP



8Y (U-2)

NOTES:
Pins are tin plated copper
Package weight is 0.6 grams
Package material is plastic
Center pin is electrical contact with mounting tab
For detailed package configuration, refer to FSB-90717
All dimensions nominal

4-PIN SINGLE SIDE POWER PLASTIC MINIDIP

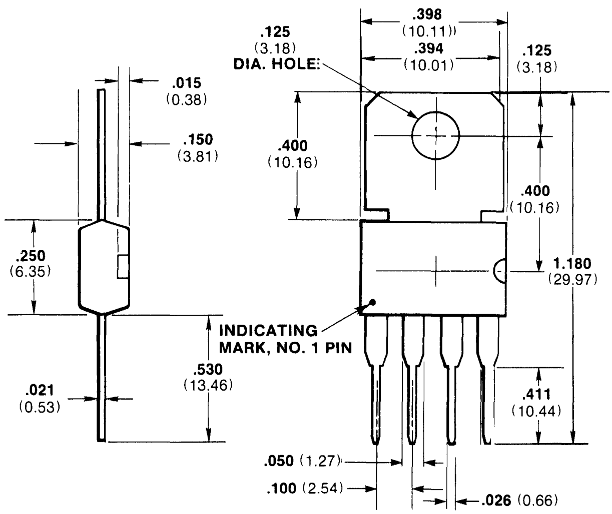


8Z (U-1)

NOTES:
Package is plastic with tin-plated copper pins
Board-drilling dimensions should equal your practice for .033 (0.84) inch diameter pins
Package weight is 0.6 gram
Tab is electrically insulated from pins
This package is intended to be mounted with the tab flush with the top of the PC board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.

All dimensions in inches (bold) and millimeters (parentheses)

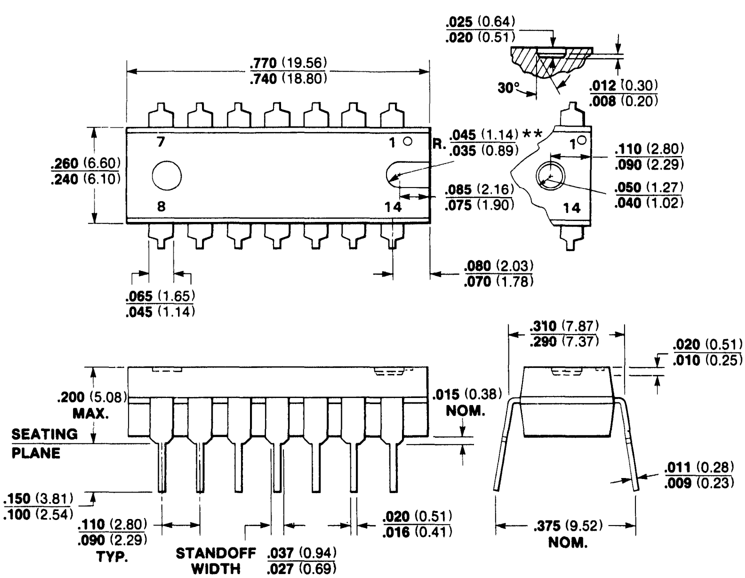
4-PIN SINGLE SIDE POWER PLASTIC MINIDIP



8Z (U-2)

NOTES:
Package is plastic with tin-plated pins
Board-drilling dimensions should equal your practice for .033 (0.84) inch diameter pin
Package weight is 0.6 gram
Tab is electrically insulated from pins

In Accordance with 14-PIN *PLASTIC DUAL IN-LINE (JEDEC TO-116 OUTLINE)

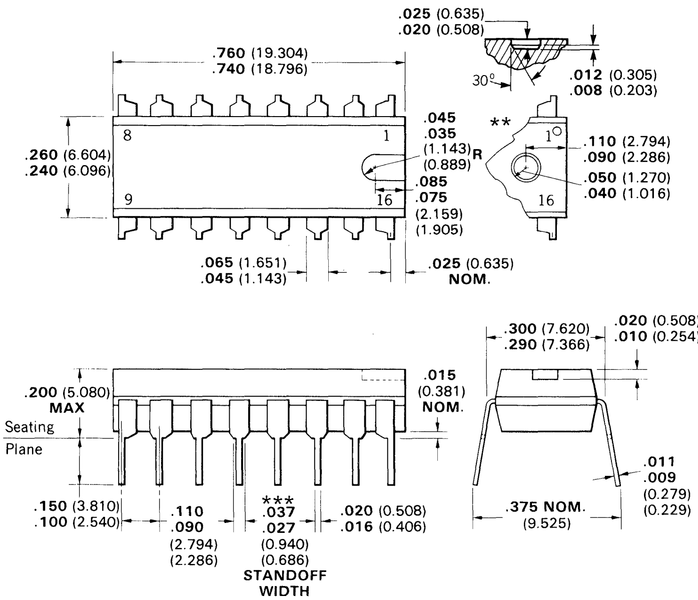


9A

NOTES:
Pins are tin plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.508) inch diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

16-PIN PLASTIC* DUAL IN-LINE

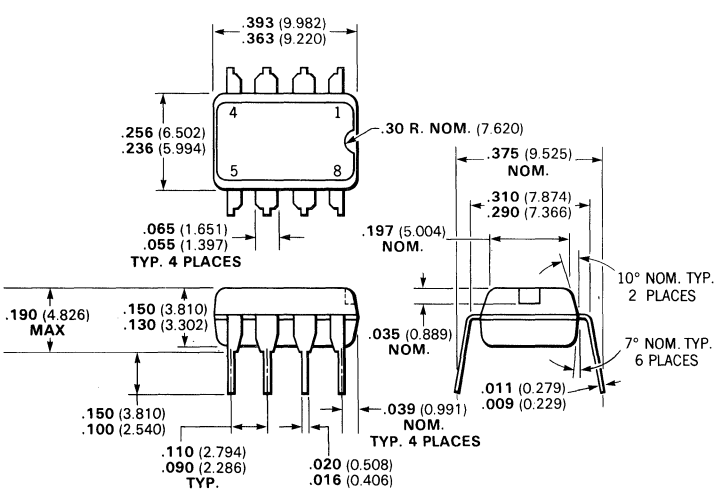


9B

NOTES:

Pins are tin-plated kovar or alloy 42 nickel.
Pins are intended for insertion in hole rows on .300" (7.62) centers
Pins purposely have a "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
***The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line

8-PIN PLASTIC DUAL IN-LINE



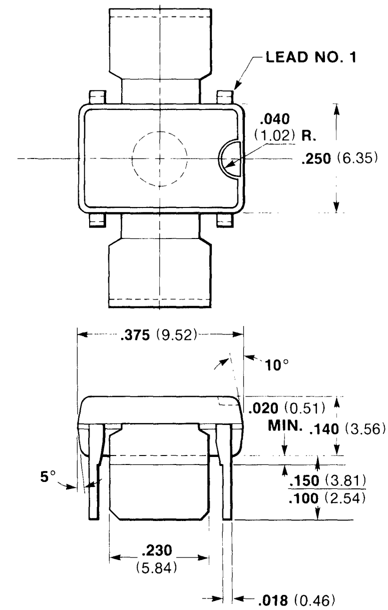
9T

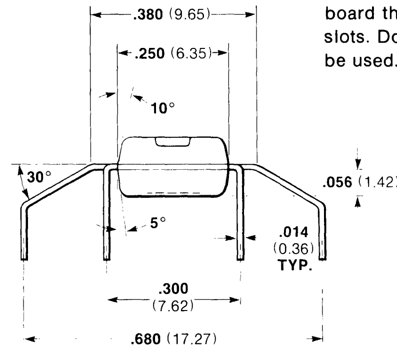
NOTES:

Pins are tin or gold-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diamater pin
Package weight is 0.6 gram

All dimensions in inches (bold) and millimeters (parentheses)

4-PIN POWER MINIDIP





9V (T1)

NOTES:

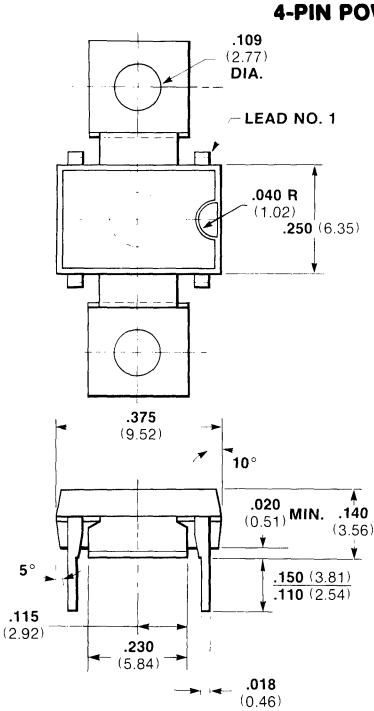
Package is plastic with tin-plated copper pins

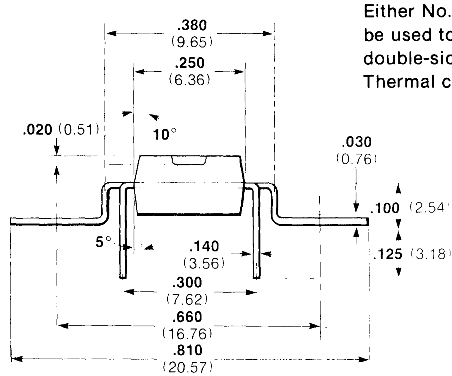
For detailed package configuration refer to FSD-90669

Package weight is 0.6 gram

T-1 package can be soldered to the PC board through .0230" x .020 (0.584 x 0.51) slots. Double or single-sided boards may be used.

4-PIN POWER MINIDIP





9V (T2)

NOTES:

Package is plastic with tin-plated copper pins and wings

For detailed package configuration refer to FSD-90670.

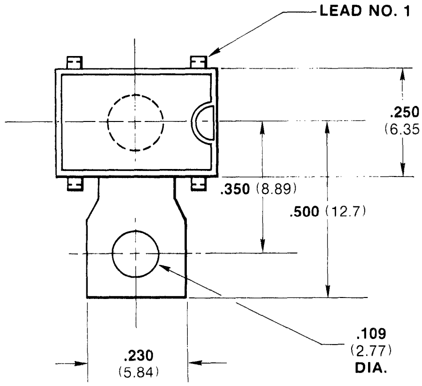
Package weight is 0.6 gram

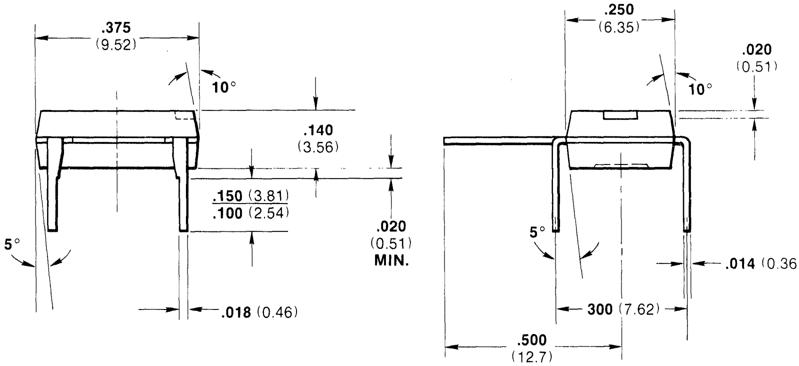
T-2 package is intended to be mounted with the tabs flush with the top of the PC board. Either No. 2-56 screws or No. 2 rivets may be used to secure the package. Single or double-sided PC boards may be used. Thermal compound is recommended.

All dimensions in inches (bold) and millimeters (parentheses)

9

4-PIN POWER MINIDIP





9V (T3)

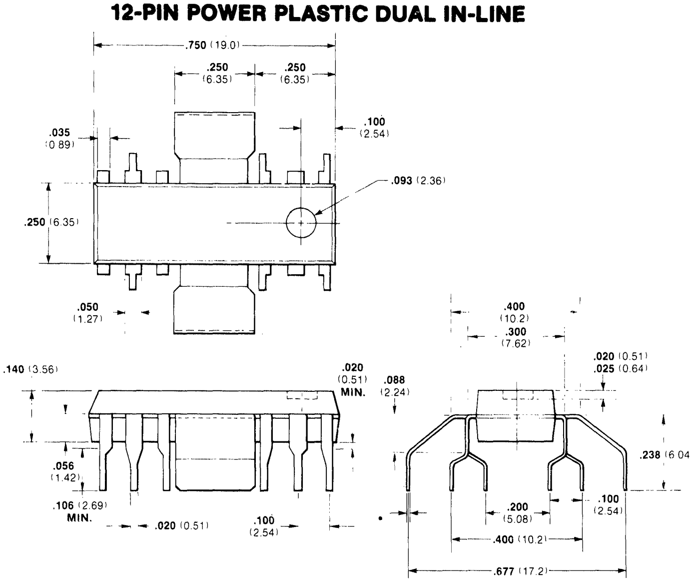
NOTES:

Package is plastic with tin-plated copper pins and wings

Package weight is 0.6 gram

T-3 package is intended for applications with an external heat sink. A No. 2 mounting hole is provided for case of mounting. The tab may be bent to any convenient angle.

12-PIN POWER PLASTIC DUAL IN-LINE



9W (P3)

NOTES:

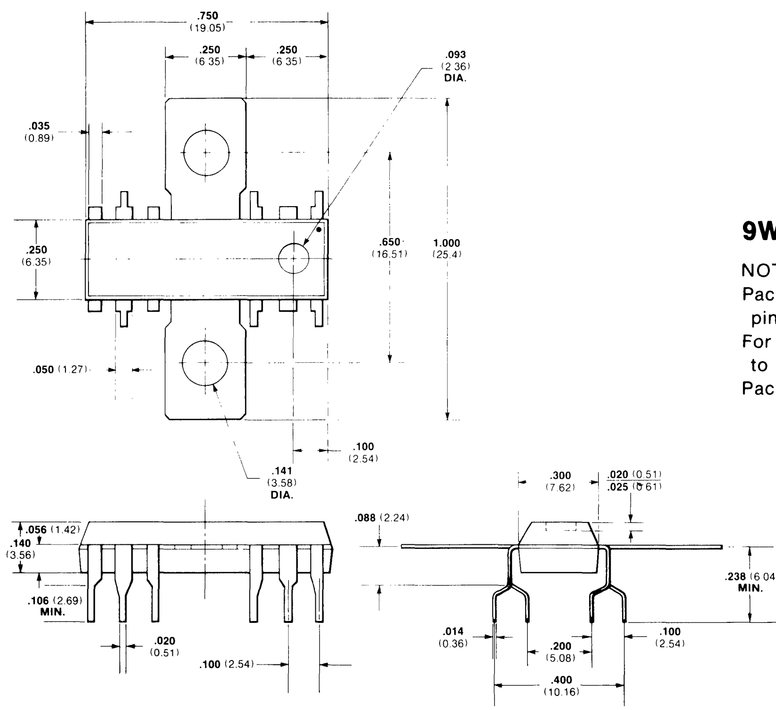
Package is plastic with tin plated copper pins and wings

For detailed package configuration refer to FSB-90698

Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

12-PIN POWER PLASTIC DUAL IN-LINE



9W (P4)

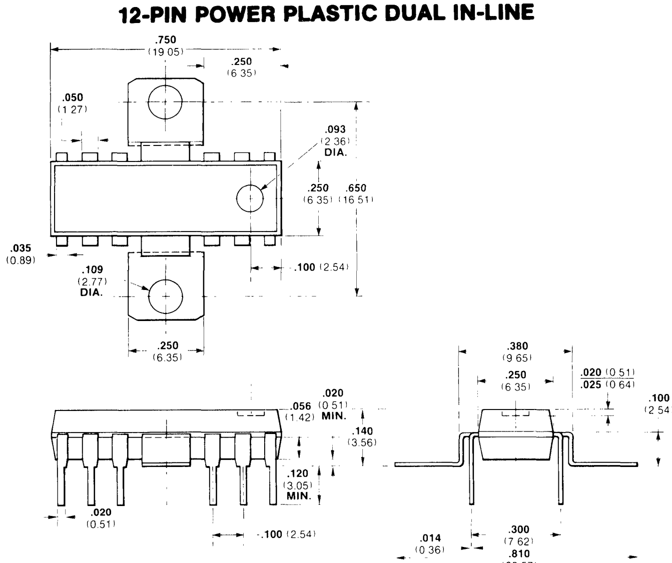
NOTES:

Package is plastic with tin-plated copper pins and wings

For detailed package configuration refer to FSB-90699

Package weight is 0.9 gram

12-PIN POWER PLASTIC DUAL IN-LINE



9W (P5)

NOTES:

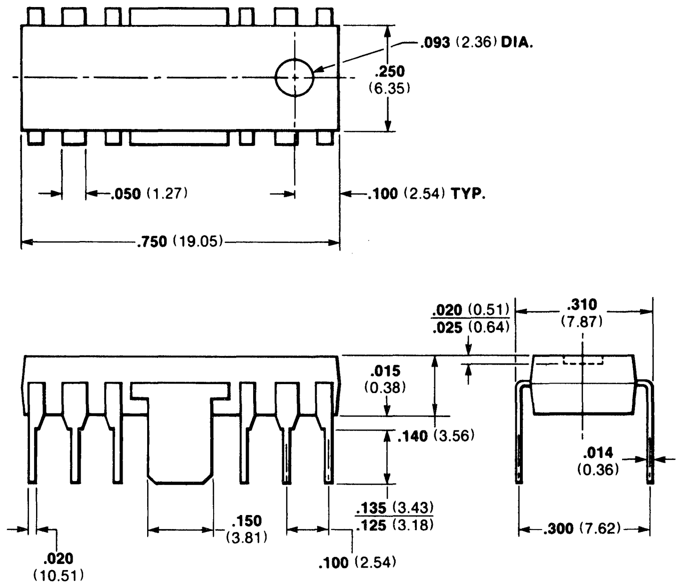
Package is plastic with tin-plated copper pins and wings

For detailed package configuration refer to FSD-90740.

Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

12-PIN PLASTIC DUAL IN-LINE



9W (P6)

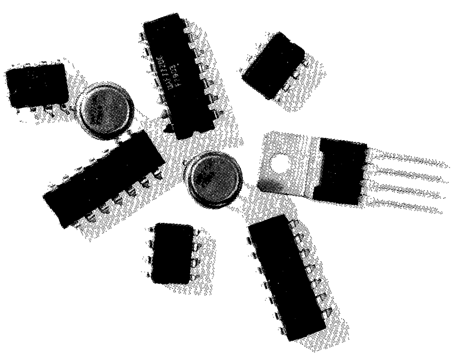
NOTES:

Package is plastic with tin-plated copper pins and wings

Package weight is 0.9 gram

The heat sinking tabs are electrically connected to the most negative potential pin

All dimensions in inches (bold) and millimeters (parentheses)



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Fairchild Semiconductor
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Suite 138
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Tel: 503-641-7871
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Houston Office
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Suite 102
Tel: 713-771-3547 TWX: 910-881-8278

Canada
Toronto Regional Office
Fairchild Semiconductor
1590 Matheson Blvd., Unit 26
Mississauga, Ontario L4W 1J1, Canada
Tel: 416-625-7070 TWX: 610-492-4311

*Field Application Engineer

Fairchild Sales Offices International

Australia
Fairchild Australia Pty Ltd.
72 Whiting Street
Artarmon 2064
New South Wales
Australia
Tel: Sydney (02)-438-2733
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Australia

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France
Fairchild Camera & Instrument S.A.
121, Avenue d'Italie
75013 Paris, France
Tel: 331-584-55 66
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Germany
Fairchild Camera and Instrument (Deutschland)
Daimlerstr 15
8046 Garching Hochbruck
Munich, Germany
Tel: (089) 320031 Telex: 52 4831 fair d

Fairchild Camera and Instrument (Deutschland)
Koenigsworther Strasse 23
3000 Hannover
W-Germany
Tel: 0511 17844 Telex: 09 22922

Fairchild Camera and Instrument (Deutschland)
Postrstrasse 37
7251 Leonberg
W-Germany
Tel: 07152 41026 Telex: 07 245711

Fairchild Camera and Instrument (Deutschland)
Waldluststrasse 1
8500 Nuernberg
W-Germany
Tel: 0911 407005 Telex: 06 23665

Hong Kong
Fairchild Semiconductor (HK) Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
Tel: K-890271 Telex: HKG-531

Italy
Fairchild Semiconduttori, S.P.A.
Via Flamenia Vecchia 653
00191 Roma, Italy
Tel: 06 327 4006 Telex: 63046 (FAIR ROM)

Fairchild Semiconduttori S.P.A.
Via Rosellini, 12
20124 Milano, Italy
Tel: 02 6 88 74 51 Telex: 36522

Japan
Fairchild Japan Corporation
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1-15-21, Shibuya
Shibuya-Ku, Tokyo 150
Japan
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(mailing address)
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Fairchild Mexicana S.A.
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Scandinavia
Fairchild Semiconductor AB
Svartengsgatan 6
S-11620 Stockholm
Sweden
Tel: 8-449255 Telex: 17759

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Fairchild Semiconductor Pty Ltd.
No. 11, Lorong 3
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Singapore 12
Tel: 531-066 Telex: FAIRSIN-RS 21376

Taiwan
Fairchild Semiconductor (Taiwan) Ltd.
Hsietsu Bldg., Room 502
47 Chung Shan North Road
Sec. 3 Taipei, Taiwan
Tel: 573205 thru 573207

Benelux
Fairchild Semiconductor
Paradijslaan 39
Eindhoven, Holland
Tel: 00-31-40-446909 Telex: 00-1451024

United Kingdom
Fairchild Camera and Instrument (UK) Ltd.
Semiconductor Division
230 High Street
Potters Bar
Hertfordshire EN6 5BU
England
Tel: 0707 51111 Telex: 262835

Fairchild Semiconductor Ltd.
17 Victoria Street
Craigshill
Livingston
West Lothian, Scotland - EH54 5BG
Tel: Livingston 0506 32891 Telex: 72629

Fairchild Semiconductor Sales Representatives United States and Canada

Alabama
Cartwright & Bean, Inc.
2400 Bob Wallace Ave., Suite 201
Huntsville, Alabama 35805
Tel: 205-533-3509

California
Celtec Company
18009 Sky Park Circle Suite B
Irvine, California 92715
Tel: 714-557-5021 TWX: 910-595-2512

Celtec Company
7867 Convoy Court, Suite 312
San Diego, California 92111
Tel: 714-279-7961 TWX: 910-335-1512

Magna Sales, Inc.
3333 Bowers Avenue
Suite 295
Santa Clara, California 95051
Tel: 408-985-1750 TWX: 910-338-0241

Colorado
Simpson Associates, Inc.
2552 Ridge Road
Littleton, Colorado 80120
Tel: 303-794-8381 TWX: 910-935-0719

Connecticut
Phoenix Sales Company
389 Main Street
Ridgefield, Connecticut 06877
Tel: 203-438-9644 TWX: 710-467-0662

Florida
Lectromech, Inc.
399 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-831-1577 TWX: 810-853-0262

Lectromech, Inc.
2280 U.S. Highway 19 North
Suite 119 Bldg. L
Clearwater, Florida 33515
Tel: 813-726-0541
TWX: 810-866-0884

Lectromech, Inc.
17 E. Hibiscus Blvd.
Suite A
Melbourne, Florida 32901
Tel: 305-725-1950
TWX: 810-853-0262

Lectromech, Inc.
1350 S. Powerline Road, Suite 104
Pompano Beach, Florida 33060
Tel: 305-974-6780 TWX: 510-954-9793

Georgia
Cartwright & Bean, Inc.
P.O. Box 52846 (Zip Code 30355)
90 W. Wieuca Square, Suite 155
Atlanta, Georgia 30342
Tel: 404-255-5262 TWX: 810-751-3220

Illinois
Micro Sales, Inc.
2258-B Landmeir Road
Elk Grove Village, Illinois 60007
Tel: 312-956-1000 TWX: 910-222-1833

Kansas
B.C. Electronic Sales, Inc.
P.O. Box 12485, Zip 66212
8190 Nieman Road
Shawnee Mission, Kansas 66214
Tel: 913-888-6680 TWX: 910-749-6414

B.C. Electronic Sales, Inc.
6405 E. Kellogg
Suite 14
Wichita, Kansas 67207
Tel: 316-684-0051

Maryland
Delta III Associates
1000 Century Plaza Suite 224
Columbia, Maryland 21044
Tel: 301-730-4700 TWX: 710-826-9654

Massachusetts
Spectrum Associates, Inc.
888 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-2796 TWX: 710-348-0424

Minnesota
PSI Company
720 W. 94th. Street
Minneapolis, Minnesota 55420
Tel: 612-884-1777 TWX: 910-576-3483

Mississippi
Cartwright & Bean, Inc.
P.O. Box 16728
5150 Keele Street
Jackson, Mississippi 39206
Tel: 601-981-1368
TWX: 810-751-3220

Missouri
B.C. Electronic Sales, Inc.
300 Brookes Drive, Suite 206
Hazelwood, Missouri 63042
Tel: 314-731-1255 TWX: 910-762-0600

Nevada
Magna Sales
4560 Wagon Wheel Road
Carson City, Nevada 89701
Tel: 702-883-0860

New Jersey
Lorac Sales, Inc.
580 Valley Road
Wayne, New Jersey 07470
Tel: 201-696-8875 TWX: 710-988-5846

New York
Lorac Sales, Inc.
550 Old Country Road, Room 410
Hicksville, New York 11801
Tel: 516-681-8746 TWX: 510-224-6480

Tri-Tech Electronics, Inc.
3215 E. Main Street
Endwell, New York 13760
Tel: 607-754-1094 TWX: 510-252-0891

Tri-Tech Electronics, Inc.
590 Perinton Hills Office Park
Fairport, New York 14450
Tel: 716-223-5720
TWX: 510-253-6356

Tri-Tech Electronics, Inc.
6836 E. Genesee Street
Fayetteville, New York 13066
Tel: 315-446-2881 TWX: 710-541-0604

Tri-Tech Electronics, Inc.
19 Davis Avenue
Poughkeepsie, New York 12603
Tel: 914-473-3880
TWX: 510-253-6356

North Carolina
Cartwright & Bean, Inc.
1165 Commercial Ave.
Charlotte, North Carolina 28205
Tel: 704-377-5673

Cartwright & Bean, Inc.
P.O. Box 18465
3948 Browning Place
Raleigh, North Carolina 27619
Tel: 919-781-6560

Ohio
The Lyons Corporation
4812 Frederick Road, Suite 101
Dayton, Ohio 45414
Tel: 513-278-0714
TWX: 810-459-1803

The Lyons Corporation
6151 Wilson Mills Road, Suite 101
Highland Heights, Ohio 44143
Tel: 216-461-8288
TWX: 810-459-1803

Oklahoma
Technical Marketing
9717 E. 42nd Street, Suite 221
Tulsa, Oklahoma 74101
Tel: 918-622-5984

Oregon
Magna Sales, Inc.
8285 S.W. Nimbus Ave., Suite 138
Beaverton, Oregon 97005
Tel: 503-641-7045
TWX: 910-467-8742

Pennsylvania
BGR Associates
2500 Office Center
2500 Maryland Road
Willow Grove, Pennsylvania 19090
Tel: 215-657-3301
TWX: 510-665-5685

The Lyons Corporation
187 Mary Avenue
Pittsburgh, Pennsylvania 15209
Tel: 412-821-6795

Tennessee
Cartwright & Bean, Inc.
P.O. Box 4760
560 S. Cooper Street
Memphis, Tennessee 38104
Tel: 901-276-4442
TWX: 810-751-3220

Cartwright & Bean, Inc.
8705 Unicorn Drive
Suite B120
Knoxville, Tennessee 37919
Tel: 615-693-7450
TWX: 810-751-3220

Texas
Technical Marketing
3320 Wiley Post Road
Carrollton, Texas 75006
Tel: 214-387-3601 TWX: 910-860-5158

Technical Marketing
6430 Hillcroft, Suite 104
Houston, Texas 77036
Tel: 713-777-9228

Utah
Simpson Associates, Inc.
P.O. Box 151430
Salt Lake City, Utah 84115
Tel: 801-571-7877
TWX: 910-935-0719

Washington
Magna Sales, Inc.
Benaroya Business Park
Building 3, Suite 115
300-120th Avenue, N.E.
Bellevue, Washington 98004
Tel: 206-455-3190

Wisconsin
Larsen Associates
10855 West Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-258-0529 TWX: 910-262-3160

Canada
R.N. Longman Sales, Inc. (L.S.I.)
1715 Meyerside Drive
Suite 1
Mississauga, Ontario, L5T 1C5 Canada
Tel: 416-677-8100 TWX: 610-492-8976

R.N. Longman Sales, Inc. (L.S.I.)
16891 Hymus Blvd.
Kirkland, Quebec
H9H 3L4 Canada
Tel: 514-694-3911
TWX: 610-422-3028

Fairchild Semiconductor Franchised Distributors United States and Canada

Alabama
Hallmark Electronics
4739 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-8700 TWX: 810-726-2187

Hamilton/Avnet Electronics
4692 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-7210
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Arizona
Hamilton/Avnet Electronics
2615 S. 21st Street
Phoenix, Arizona 85034
Tel: 602-275-7851 TWX: 910-951-1535

Kierulff Electronics
4134 East Wood Street
Phoenix, Arizona 85040
Tel: 602-243-4101

Liberty Electronics
8155 North 24th Ave.
Phoenix, Arizona 85021
Tel: 602-249-2232 TWX: 910-951-4282

California
Avnet Electronics
350 McCormick Avenue
Costa Mesa, California 92626
Tel: 714-754-6111 (Orange County)
213-558-2345 (Los Angeles)
TWX: 910-595-1928

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Electronic Distributor Division
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Sunnyvale, California 94086
Tel: 408-734-8570 TWX: 910-339-9378

Elmar Electronics
3000 Bowers Avenue
Santa Clara, California 95051
Tel: 408-727-2500 TWX: 910-338-0541

Hamilton Electro Sales
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, California 94086
Tel: 408-743-3355 TWX: 910-379-6486

Hamilton/Avnet Electronics
8917 Complex Drive
San Diego, California 92123
Tel: 714-279-2421
Telex: HAMAVELEC SDG 69-5415

Intermark Electronics, Inc.
4040 Sorrento Valley Blvd.
San Diego, California 92121
Tel: 714-279-5200

Intermark Electronics, Inc.
1802 East Carnegie Avenue
Santa Ana, California 92705
Tel: 714-540-1322

Liberty Electronics
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

Liberty Electronics/San Diego
8248 Mercury Court
San Diego, California 92111
Tel: 714-565-9171 TWX: 910-335-1590

**Sertech Laboratories
2120 Main Street, Suite 190
Huntington Beach, California 92647
Tel: 714-960-1403

Wyle Distribution Group
9525 Chesapeake
San Diego, California 92123
Tel: 714-565-9171 TWX: 910-335-1590

Colorado
Bell Industries
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

Arrow Electronics
5465 East Evans Place at Hudson
Denver, Colorado 80222
Tel: 303-758-2100

Elmar Electronics
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

Hamilton/Avnet Electronics
5921 N. Broadway
Denver, Colorado 80216
Tel: 303-534-1212 TWX: 910-931-0510

Connecticut
Cramer Electronics
12 Beaumont Road
Wallingford, Connecticut 06492
Tel: 203-265-7741

Hamilton/Avnet Electronics
643 Danbury Road
Georgetown, Connecticut 06829
Tel: 203-762-0361
TWX: None — use 710-897-1405
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Harvey Electronics
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

Florida
Arrow Electronics
1001 Northwest 62nd Street
Suite 402
Ft. Lauderdale, Florida 33309
Tel: 305-776-7790

Arrow Electronics
115 Palm Bay Road N.W.
Suite 10 Bldg. #200
Palm Bay, Florida 32905
Tel: 305-725-1408

Hallmark Electronics
1302 W. McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

Hallmark Electronics
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

Hamilton/Avnet Electronics
6800 N.W. 20th Avenue
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-954-9808

Hamilton/Avnet Electronics
3197 Tech Drive, North
St. Petersburg, Florida 33702

Schweber Electronics
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

Georgia
Arrow Electronics
3406 Oak Cliff Road
Doraville, Georgia 30340
Tel: 404-455-4054

Hamilton/Avnet Electronics
6700 Interstate 85 Access Road, Suite 1E
Norcross, Georgia 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Illinois
Hallmark Electronics, Inc.
1177 Industrial Drive
Bensenville, Illinois 60106
Tel: 312-860-3800

Hamilton/Avnet Electronics
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

Kierulff Electronics
1536 Landmeier Road
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

Schweber Electronics, Inc.
1275 Bummel Avenue
Elk Grove Village, Illinois 60007
Tel: 312-593-2740 TWX: 910-222-3453

Semiconductor Specialists, Inc.
(mailing address)
O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666
(shipping address)
195 Spangler Avenue
Elmhurst Industrial Park
Elmhurst, Illinois 60126
Tel: 312-279-1000 TWX: 910-254-0169

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Graham Electronics Supply, Inc.
133 S. Pennsylvania St.
Indianapolis, Indiana 46204
Tel: 317-634-8486 TWX: 810-341-3481

Pioneer Indiana Electronics, Inc.
6408 Castle Place Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

Kansas
Hallmark Electronics, Inc.
11870 W. 91st Street
Shawnee Mission, Kansas 66214
Tel: 913-888-4746

Hamilton/Avnet Electronics
9219 Guivira Road
Overland Park, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Louisiana
Sterling Electronics Corp.
4613 Fairfield
Metairie, Louisiana 70002
Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

Maryland
Hallmark Electronics, Inc.
6655 Amberton Drive
Baltimore, Maryland 21227
Tel: 301-796-9300

Hamilton/Avent Electronics
(mailing address)
Friendship International Airport
P.O. Box 8647
Baltimore, Maryland 21240
(shipping address)
7235 Standard Drive
Hanover, Maryland 21076
Tel: 301-796-5000 TWX: 710-862-1861
Telex: HAMAVLECA HNVE 87-968

Pioneer Washington Electronics, Inc.
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX: 710-828-9784

Schweber Electronics
9218 Gaither Road
Gaithersburg, Maryland 20760
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Tel: 617-329-2400

Hamilton/Avnet Electronics
100 E. Commerce Way
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Tel: 617-933-8000 TWX: 710-332-1201

Harvey Electronics
44 Hartwell Avenue
Lexington, Massachusetts 02173
Tel: 617-861-9200 TWX: 710-326-6617

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Pioneer/Detroit
13485 Stamford
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Tel: 313-525-1800

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Wyoming, Michigan 49508
Tel: 616-531-9300

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33540 Schoolcraft
Livonia, Michigan 48150
Tel: 313-525-8100

Arrow Electronics
3921 Varsity Drive
Ann Arbor, Michigan 48104
Tel: 313-572-1040

Minnesota
Arrow Electronics
5251 West 73rd Street
Edina, Minnesota 55435
Tel: 612-830-1800

Hamilton/Avnet Electronics
7449 Cahill Road
Edina, Minnesota 55435
Tel: 612-941-3801
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

Schweber Electronics
7402 Washington Avenue S.
Eden Prairie, Minnesota 55344
Tel: 612-941-5280

Missouri
Hallmark Electronics, Inc.
13789 Rider Trail
Earth City, Missouri 63045
Tel: 314-291-5350

Hamilton/Avnet Electronics
396 Brookes Lane
Hazelwood, Missouri 63042
Tel: 314-731-1144 TWX: 910-762-0606

New Jersey
Hamilton/Avnet Electronics
10 Industrial Road
Fairfield, New Jersey 07006
Tel: 201-575-3390 TWX: 710-994-5787

Hamilton/Avnet Electronics
#1 Keystone Avenue
Cherry Hill, New Jersey 08003
Tel: 609-424-0100 TWX: 710-940-0262

Schweber Electronics
18 Madison Road
Fairfield, New Jersey 07006
Tel: 201-227-7880 TWX: 710-480-4733

Sterling Electronics
774 Pfeiffer Blvd.
Perth Amboy, N.J. 08861
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Wilshire Electronics
102 Gaither Drive
Mt. Laurel, N.J. 08057
Tel: 215-627-1920

Wilshire Electronics
1111 Paulison Avenue
Clifton, N.J. 07011
Tel: 201-365-2600 TWX: 710-989-7052

New Mexico
Bell Industries
11728 Linn Avenue
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

Hamilton/Avnet Electronics
2450 Byalor Drive S.E.
Albuquerque, New Mexico 87119
Tel: 505-765-1500
TWX: None — use 910-379-6486
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New York
Arrow Electronics
900 Broadhollow Road
Farmingdale, New York 11735
Tel: 516-694-6800

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40-17 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-6722

Cramer Electronics
129 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-5682

Cramer Electronics
P.O. Box 370
7705 Maltlage
Liverpool, New York 13088
Tel: 315-652-1000
TWX: 710-545-2030

Components Plus, Inc.
40 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

Harvey Electronics
(mailing address)
P.O. Box 1208
Binghampton, New York 13902
(shipping address)
Vestal Parkway East
Vestal, New York 13902
Tel: 607-748-8211 TWX: 510-252-0893

Hamilton/Avnet Electronics
167 Clay Road
Rochester, New York 14623
Tel: 716-442-7820
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Ma.)

Hamilton/Avnet Electronics
16 Corporate Circle
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

Hamilton/Avnet Electronics
70 State Street
Westbury, L.I., New York 11590
Tel: 516-333-5800 TWX: 510-222-8237

Rochester Radio Supply Co., Inc.
140 W. Main Street
(P.O. Box 1971)
Rochester, New York 14603
Tel: 716-454-7800

Schweber Electronics
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

Jaco Electronics, Inc.
145 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-273-1234 TWX: 510-227-6232

Summit Distributors, Inc.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

North Carolina
Cramer Electronics
938 Burke Street
Winston Salem, North Carolina 27102
Tel: 919-725-8711

Hamilton/Avnet
2803 Industrial Drive
Raleigh, North Carolina 27609
Tel: 919-829-8030

Hallmark Electronics
1208 Front Street, Bldg. K
Raleigh, North Carolina 27609
Tel: 919-823-4465 TWX: 510-928-1831

Resco
Highway 70 West
Rural Route 8, P.O. Box 116-B
Raleigh, North Carolina 27612
Tel: 919-781-5700

Pioneer/Carolina Electronics
103 Industrial Drive
Greensboro, North Carolina 27406
Tel: 919-273-4441

Ohio
Arrow Electronics
3100 Plainfield Road
Dayton, Ohio 45432
Tel: 513-253-9176

Hamilton/Avnet Electronics
4588 Emery Industrial Parkway
Cleveland, Ohio 44128
Tel: 216-831-3500
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

Hamilton/Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

Pioneer/Cleveland
4800 E. 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

Pioneer/Dayton
1900 Troy Street
Dayton, Ohio 45404
Tel: 513-236-9900 TWX: 810-459-1622

Schweber Electronics
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

Arrow Electronics
6238 Cochran Road
Solon, Ohio 44139
Tel: 216-248-3990 TWX: 810-427-9409

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Arrow Electronics
(mailing address)
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Cincinnati, Ohio 45222
(shipping address)
10 Knollcrest Drive
Reading, Ohio 45237
Tel: 513-761-5432 TWX: 810-461-2670

Oklahoma
Hallmark Electronics
4846 S. 83rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

Radio Inc. Industrial Electronics
1000 S. Main
Tulsa, Oklahoma 74119
Tel: 918-587-9123

Pennsylvania
Hallmark Electronics, Inc.
458 Pike Road
Huntingdon Valley, Pennsylvania 19006
Tel: 215-355-7300 TWX: 510-667-1727

Pioneer/Delaware Valley Electronics
141 Gibraltar Road
Horsham, Pennsylvania 19044
Tel: 215-674-4000 TWX: 510-665-6778

Pioneer Electronics, Inc.
560 Alpha Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

Schweber Electronics
101 Rock Road
Horsham, Pennsylvania 19044
Tel: 215-441-0600

Arrow Electronics
4297 Greensburgh Pike
Suite 3114
Pittsburgh, Pennsylvania 15221
Tel: 412-351-4000

South Carolina
Dixie Electronics, Inc.
P.O. Box 408 (Zip Code 29202)
1900 Barnwell Street
Columbia, South Carolina 29201
Tel: 803-779-5332

Texas
Allied Electronics
401 E. 8th Street
Fort Worth, Texas 76102
Tel: 817-336-5401

Cramer Electronics
13715 Gamma Road
Dallas, Texas 75234
Tel: 214-386-7500 TWX: 910-860-5377

Hallmark Electronics Corp.
10109 McKalla Place Suite F
Austin, Texas 78758
Tel: 512-837-2814

Hallmark Electronics
11333 Pagemill Drive
Dallas, Texas 75243
Tel: 214-234-7300 TWX: 910-867-4721

Hallmark Electronics, Inc.
8000 Westglen
Houston, Texas 77063
Tel. 713-781-6100

Hamilton/Avnet Electronics
4445 Sigma Road
Dallas, Texas 75240
Tel: 214-661-8661
Telex: HAMAVLECB DAL 73-0511

Hamilton/Avnet Electronics
3939 Ann Arbor
Houston, Texas 77042
Tel: 713-780-1771
Telex: HAMAVLECB HOU 76-2589

Schweber Electronics, Inc.
14177 Proton Road
Dallas, Texas 75240
Tel: 214-661-5010 TWX: 910-860-5493

Schweber Electronics, Inc.
7420 Harwin Drive
Houston, Texas 77036
Tel: 713-784-3600 TWX: 910-881-1109

Sterling Electronics
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 901-881-5042
Telex: STELECO HOUA 77-5299

Utah
Bell Industries
3639 W. 2150 South
Salt Lake City, Utah 84120
Tel: 801-972-6969 TWX: 910-925-5686

Hamilton/Avnet Electronics
1585 W. 2100 South
Salt Lake City, Utah 84119
Tel: 801-972-2800
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

Washington
Hamilton/Avnet Electronics
14212 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-746-8750 TWX: 910-443-2449

Liberty Electronics
1750 132nd Avenue N.E.
Bellevue, Washington 98005
Tel: 206-453-8300 TWX: 910-444-1379

Radar Electronic Co., Inc.
168 Western Avenue W.
Seattle, Washington 98119
Tel: 206-282-2511 TWX: 910-444-2052

Wisconsin
Hamilton/Avnet Electronics
2975 Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510 TWX: 910-262-1182

Marsh Electronics, Inc.
1563 S. 100 Street
Milwaukee, Wisconsin 53214
Tel: 414-475-6000 TWX: 910-262-3321

Canada
Cam Gard Supply Ltd.
640 42nd Avenue S.E.
Calgary, Alberta, T2G 1Y6, Canada
Tel: 403-287-0520 Telex: 03-822811

Cam Gard Supply Ltd.
16236 116th Avenue
Edmonton, Alberta T5M 3V4, Canada
Tel: 403-453-6691 Telex: 03-72960

Cam Gard Supply Ltd.
4910 52nd Street
Red Deer, Alberta, T4N 2C8, Canada
Tel: 403-346-2088

Cam Gard Supply Ltd.
825 Notre Dame Drive
Kamloops, British Columbia, V2C 5N8, Canada
Tel: 604-372-3338

Cam Gard Supply Ltd.
1777 Ellice Avenue
Winnepeg, Manitoba, R3H 0W5, Canada
Tel: 204-786-8401 Telex: 07-57622

Cam Gard Supply Ltd.
Rookwood Avenue
Fredericton, New Brunswick, E3B 4Y9, Canada
Tel: 506-455-8891

Cam Gard Supply Ltd.
15 Mount Royal Blvd.
Moncton, New Brunswick, E1C 8N6, Canada
Tel: 506-855-2200

Cam Gard Supply Ltd.
3065 Robie Street
Halifax, Nova Scotia, B3K 4P6, Canada
Tel: 902-454-8581 Telex: 01-921528

Cam Gard Supply Ltd.
1303 Scarth Street
Regina, Saskatchewan, S4R 2E7, Canada
Tel: 306-525-1317 Telex: 07-12667

Cam Gard Supply Ltd.
1501 Ontario Avenue
Saskatoon, Saskatchewan, S7K 1S7, Canada
Tel: 306-652-6424 Telex: 07-42825

Electro Sonic Industrial Sales
(Toronto) Ltd.
1100 Gordon Baker Rd.
Willowdale, Ontario, M2H 3B3, Canada
Tel: 416-494-1666
Telex: ESSCO TOR 06-22030

Future Electronics Inc.
Baxter Center
1050 Baxter Road
Ottawa, Ontario, K2C 3P2, Canada
Tel: 613-820-9471

Future Electronics Inc.
4800 Dufferin Street
Downsview, Ontario, M3H 5S8, Canada
Tel: 416-663-5563

Future Electronics Corporation
5647 Ferrier Street
Montreal, Quebec, H4P 2K5, Canada
Tel: 514-731-7441

Hamilton/Avnet International
(Canada) Ltd.
3688 Nashua Drive, Units 6 & H
Mississauga, Ontario, L4V 1M5, Canada
Tel: 416-677-7432 TWX: 610-492-8867

Hamilton/Avnet International
(Canada) Ltd.
1735 Courtwood Crescent
Ottawa, Ontario, K1Z 5L9, Canada
Tel: 613-226-1700

Hamilton/Avnet International
(Canada) Ltd.
2670 Paulus Street
St. Laurent, Quebec, H4S 1G2, Canada
Tel: 514-331-6443 TWX: 610-421-3731

R.A.E. Industrial Electronics, Ltd.
3455 Gardner Court
Burnaby, British Columbia Z5G 4J7
Tel: 604-291-8866 TWX: 610-929-3065
Telex: RAE-VCR 04-54550

Semad Electronics Ltd.
620 Meloche Avenue
Dorval, Quebec, H9P 2PY, Canada
Tel: 604-2998-866 TWX: 610-422-3048

Semad Electronics Ltd.
105 Bribane Avenue
Downsview, Ontario, M3J 2K6, Canada
Tel: 416-663-5670 TWX: 610-492-2510

Semad Electronics Ltd.
1485 Laperriere Avenue
Ottawa, Ontario, K1Z 7S8, Canada
Tel: 613-722-6571 TWX: 610-562-8966

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