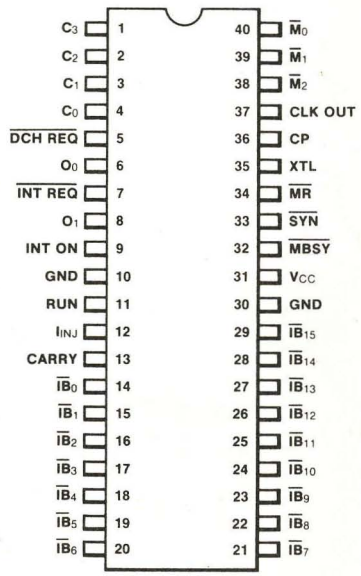
9440 MICROFLAME™
16-BIT BIPOLAR MICROPROCESSOR

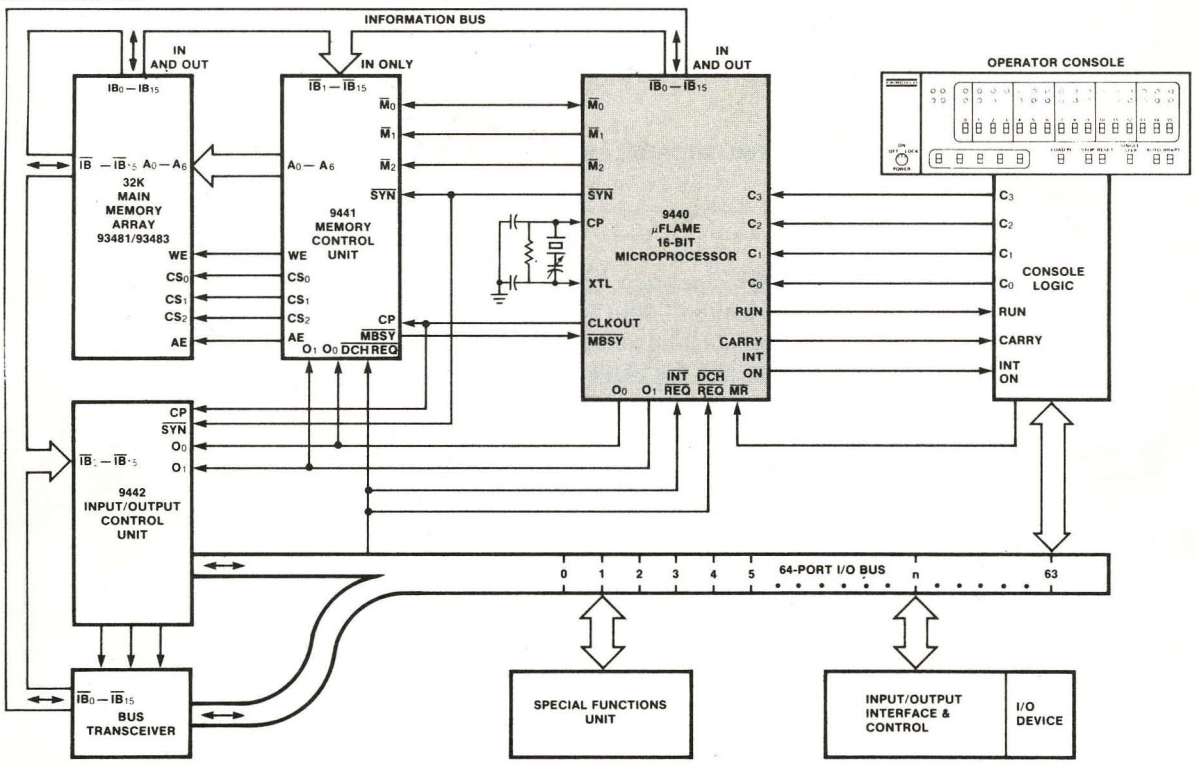
GENERAL DESCRIPTION — The 9440 MICROFLAME single-chip 16-bit bipolar processor, packaged in a 40-pin DIP, is implemented using Fairchild's Isoplanar Integrated Injection Logic technology (I^3L™). Though structurally different from the CPUs of the Data General NOVA line of minicomputers, the 9440 offers comparable performance and executes the same instruction set.

- EIGHT 16-BIT ON-CHIP REGISTERS
- 64 DIRECTLY ADDRESSABLE I/O DEVICES, EACH WITH THREE BIDIRECTIONAL I/O PORTS
- PRIORITY INTERRUPT HANDLING WITH UP TO 16 PRIORITY LEVELS
- FAST DIRECT MEMORY ACCESS AT MEMORY SPEEDS
- 16-BIT 3-STATE BIDIRECTIONAL INFORMATION BUS
- FLEXIBLE OPERATOR CONSOLE CONTROL USING ONLY FOUR LINES
- POWERFUL, WIDELY USED INSTRUCTION SET
- MULTIFUNCTION INSTRUCTIONS FOR EFFICIENT MEMORY USAGE
- 50 BASIC INSTRUCTIONS FOR A TOTAL OF 2192 DIFFERENT INSTRUCTIONS
- 8 ADDRESSING MODES
- 64K BYTES DIRECT-ADDRESSING RANGE EXTENDED TO 16M BYTES VIA MEMORY MAPPING
- 5 V POWER SUPPLY
- TTL INPUTS AND OUTPUTS
- TYPICAL 1 W POWER DISSIPATION
- FULL MILITARY TEMPERATURE RANGE VERSION
- SINGLE-CLOCK STATIC ON-CHIP OSCILLATOR, DC TO 12 MHz CLOCK RATE
- COMPATIBLE HIGH SPEED MEMORIES AVAILABLE (93481/93483)
- TOTAL SOFTWARE WITH FIRE™ SOFTWARE PACKAGE
- USEABLE IN STAND-ALONE AS WELL AS DISTRIBUTED PROCESSING APPLICATIONS

CONNECTION DIAGRAM
DIP (TOP VIEW)



SYSTEM DIAGRAM



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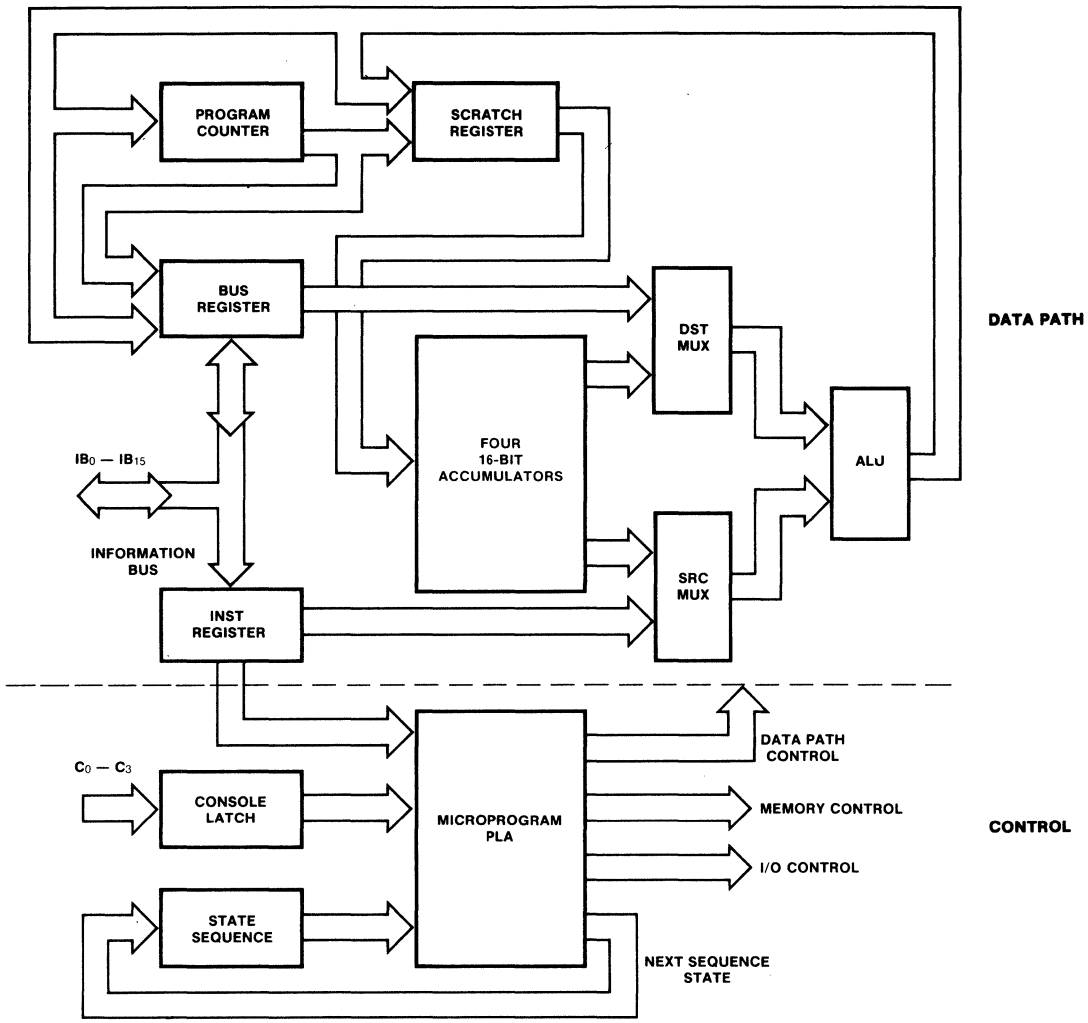


Fig. 1 9440 MICROFLAME CPU Block Diagram

9440 ARCHITECTURE *(Figure 1)*

The 9440 single-chip 16-bit bipolar processor, packaged in a 40-pin DIP, is implemented using Fairchild's Isoplanar Integrated Injection Logic technology (I^3L^{TM}). Though structurally different from the CPUs of the NOVA line of minicomputers, the 9440, as a microprocessor, offers comparable performance and executes the same instruction set.

The processor is a stored program machine using homogeneous external memory, i.e., instructions and data are stored in the same memory. Although the processor handles 16 bits of information, only 15 bits are used for addressing the memory. Thus, the intrinsic memory capacity of a 9440 system is 32,768 16-bit words.

The 9440 consists of a collection of data paths and all the necessary control circuitry. It governs peripheral I/O equipment, performs the arithmetic, logic and data handling operations and sequences the program.

Data Paths — The data path portion includes a bank of four 16-bit general-purpose registers (accumulators AC0 - AC3), two multiplexers, an ALU, and four 16-bit special registers — scratch register, bus register, instruction register and program counter. Internal data flows between the various registers via 4-bit-wide data paths.

The accumulators store the operands required for all arithmetic/logic operations. Accumulators AC2 and AC3 are also used as index registers and AC3 serves as the subroutine linkage register as well. All input-output data transfers take place through the accumulators; however, a word in a memory location may be incremented or decremented without accumulator participation. Data can be moved in either direction between the memory and any accumulator.

The destination and source multiplexers are connected to all four accumulators and select source and destination registers for each operation. The multiplexers also receive other inputs from the bus and instruction registers, which permit the ALU to be used for effective-address calculations and other purposes.

The ALU is four bits wide and operates on two 16-bit words in four consecutive steps, taking one 4-bit nibble per step. By adding the associated Carry bit to the 16-bit result from the ALU, a 17-bit word is formed which may be rotated either left or right.

Data from the ALU to the destination accumulator is held in the scratch register for one cycle. The bus register is connected to the bidirectional information bus and can either supply or receive 16 bits of data in parallel. The instruction register is loaded with 16 bits in parallel, directly from the information bus during an instruction-fetch operation. The 15-bit program counter determines the sequence in which instructions are executed. It is incremented to take instructions from consecutive locations and the instruction sequence can be altered at any time by changing the PC contents (jump-class instruction) or by incrementing PC twice (skip-class instruction).

Control — Control signals are supplied to the data path by the internal mask-programmed logic arrray (PLA). For each of 72 different data-path operations, there is a 24-bit output word in the PLA selected according to the combination of 19 input lines. These are defined in *Figure 2*.

The 9440 operates with an on-chip oscillator when a crystal is tied between CP and XTL or it can be driven by an external oscillator via the CP input. The on-chip clock logic circuit generates the internal clock signal, a synchronization signal ($\overline{\text{SYN}}$), and several other timing pulses.

A macro-instruction in the 9440 consists of several microcycles, each with a corresponding one-of-16 sequence-control state. Each microcycle consists of several phases, or nanocycles, four of which are devoted to controlling the data-path circuitry. During each of these phases, the data path circuitry operates on a 4-bit nibble out of the 16 bits of the operands and clocks its various registers at half the oscillator rate. Another phase provides the time delay required for a new output word of the PLA to become valid after the PLA inputs are changed.

The bus register and the instruction register are loaded from the information bus at different times during the execution cycle.

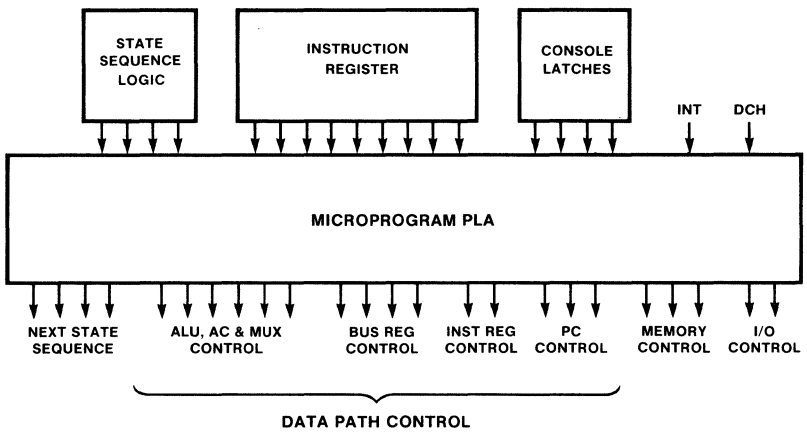


Fig. 2 Programmed Logic Array

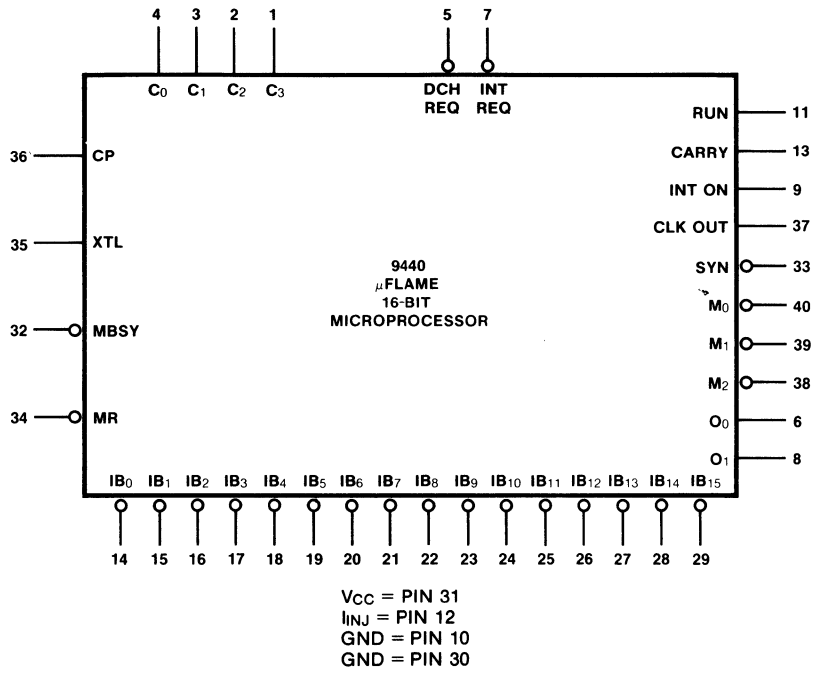


Fig. 3 Logic Symbol

9440 SIGNAL DESCRIPTIONS *(Figure 3)*

Information Bus — $\overline{IB}_0$-$\overline{IB}_{15}$ (Inputs/Outputs) — The 16-bit bidirectional 3-state information bus is used to transfer address, data and instruction information between the processor and main memory, and to transfer data and control information to and from I/O devices. A LOW level defines a binary '1'.

Status Lines — RUN, CARRY, INT ON — These lines are used to convey the status information of the processor mainly for display on an operator console.

RUN (Output) — A HIGH level on this line indicates that the 9440 is not in the WAIT state and is executing instructions or performing console operations.

CARRY (Output) — Shows the current status of the 9440 Carry flip-flop. A HIGH level is a binary '1'.

INT ON (Output) — Shows the state of the 9440 Interrupt Enable flip-flop. A HIGH level indicates that the 9440 is enabled to accept interrupts.

Operator Console Control — C_0-C_3, $\overline{MR}$ — Using the operator console, a special I/O device, the operator controls 9440 operation via the four C lines and the Master Reset line.

C_0-C_3 (Inputs) — The various console operations are coded on the Control lines as shown below. These lines must be active long enough for the 9440 to respond to the command and indicated by RUN going to the high state, and should be disabled immediately thereafter.

$\overline{MR}$ (Input) — When a LOW level is applied to Master Reset, the 9440 halts immediately and goes to a wait state. All internal registers are unaffected. The Interrupt-Enable flip-flop is cleared.

Input/Output Control — O_0-O_1, $\overline{INT\ REQ}$, $\overline{DCH\ REQ}$ — I/O devices communicate with the 9440 through the common information bus under either program or interrupt control. Also, high-speed devices can gain access to main memory via the data channel (DMA mode).

O_0, O_1 (Outputs) — To avoid conflicts on the information bus, the I/O devices are sent synchonization signals. A code, defining one of four functions, is conveyed to each I/O device over O_0 and O_1, which are valid before and during $\overline{SYN}$.

C_3	C_2	C_1	C_0	OPERATION
L	L	L	L	Examine AC0
L	L	L	H	Examine AC1
L	L	H	L	Examine AC2
L	L	H	H	Examine AC3
L	H	L	L	Examine Next
L	H	L	H	Examine Memory
L	H	H	L	Deposit Memory
L	H	H	H	Halt
H	L	L	L	Deposit AC0
H	L	L	H	Deposit AC1
H	L	H	L	Deposit AC2
H	L	H	H	Deposit AC3
H	H	L	L	Load PC
H	H	L	H	Continue
H	H	H	L	Deposit Next
H	H	H	H	No operation

Console-Operation Code

O_1	O_0	FUNCTION
L	L	Instruction Fetch
L	H	Data Channel Acknowledge
H	L	I/O Execute
H	H	No Operation

I/O-Device Code

$\overline{\text{INT REQ}}$ (Input) — The I/O devices can interrupt normal program flow by activating the Interrupt Request input. The 9440 recognizes an interrupt request at the end of the current instruction provided its Interrupt-Enable flip-flop is set.

$\overline{\text{DCH REQ}}$ (Input) — The I/O devices can gain direct access to the main memory by activating the Data Channel Request input. After the device is granted data channel access, it can control memory operation using the $\overline{M}_0$-$\overline{M}_2$ lines.

Of the four functions which can interrupt the normal flow if instruction execution, MASTER RESET ($\overline{\text{MR}}$) is the highest priority, followed in order by $\overline{\text{DCH REQ}}$, $\overline{\text{INT REQ}}$ and the Console HALT Command.

Memory Control — $\overline{M}_0$-$\overline{M}_2$, $\overline{\text{MBSY}}$ — The processor controls the main memory via the three open-collector Memory Control lines ($\overline{M}_0$-$\overline{M}_2$) and synchronizes itself to the memory cycle time indicated by the Memory-Busy ($\overline{\text{MBSY}}$) signal.

$\overline{M}_0$ (Input/Output) — A LOW level on $\overline{M}_0$ indicates a memory Read operation.

$\overline{M}_1$ (Input/Output) — A LOW level on $\overline{M}_1$ indicates a memory Write operation.

$\overline{M}_2$ (Input/Output) — A LOW level on $\overline{M}_2$ indicates that the memory address register must be loaded on or before the HIGH-to-LOW transition of $\overline{\text{SYN}}$.

During DMA operation, the 9440 is not driving the $\overline{M}$ lines. An external device can control memory by applying a LOW level on the appropriate $\overline{M}$ line.

$\overline{\text{MBSY}}$ (Input) — A LOW level on $\overline{\text{MBSY}}$ indicates a memory operation is in progress. When the 9440 starts a memory cycle, $\overline{\text{MBSY}}$ must be HIGH. If it is LOW, the processor clock logic will defer putting out $\overline{\text{SYN}}$ until $\overline{\text{MBSY}}$ becomes HIGH. For LD MAR or Write memory operations, the 9440 activates $\overline{\text{SYN}}$ and then waits for $\overline{\text{MBSY}}$ to respond with a LOW level. For a Read operation, the 9440 waits for $\overline{\text{MBSY}}$ to go LOW and back HIGH before it proceeds.

Timing — CP, XTL, CLK OUT, $\overline{\text{SYN}}$ —

CP (Input) — The 9440 can operate with an on-chip oscillator when a crystal is tied between CP and XTL or it can operate from an external clock (CP).

XTL (Input) — The XTL input is used only when operating with a crystal.

CLK OUT (Output) — The internal oscillator is available to the outside world on CLK OUT.

$\overline{\text{SYN}}$ (Output) — $\overline{\text{SYN}}$ is an active LOW synchronization signal for memory and I/O devices. It is activated once for each processor microcycle.

Power — V_{CC}, I_{INJ}, GND

V_{CC} requires 5 V, I_{INJ} requires 300 mA current source at 1.0 V.

9440 INSTRUCTIONS

Memory Reference instructions without register are used for branching (JMP, JSR) without involving accumulators. These instructions are also used for modifying memory (ISZ, DSZ). Memory Reference instructions with register are used to move 16-bit words between the memory and the accumulators.

JMP — *Jump.* The 9440 loads the effective address into the PC. The program sequence continues from that location.

JSR — *Jump to SubRoutine.* The 9440 calculates the effective address, then stores PC + 1 into AC3, loads the effective address into the PC and continues instruction execution from that location.

ISZ — *Increment and Skip if Zero.* The 9440 reads a word from the memory location specified by the effective address, increments the word and writes the result back into the same location. If the incremented word is zero, the 9440 skips the next instruction.

DSZ — *Decrement and Skip if Zero.* The 9440 reads a word from the memory location specified by the effective address; decrements it and writes the result back into the same location. If the result is zero the 9440 skips the next instruction.

LDA — *Load Accumulator.* The 9440 loads the contents of the memory location specified by the effective address into the accumulator defined by bits 3 and 4 of the instruction.

STA — *Store Accumulator.* The 9440 stores the contents of the selected accumulator into the memory location specified by the effective address; the accumulator contents are not affected.

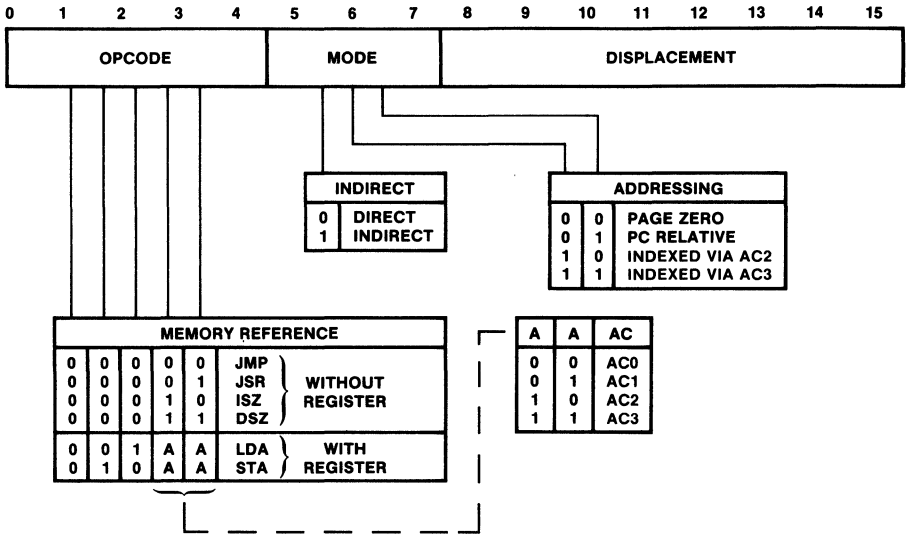
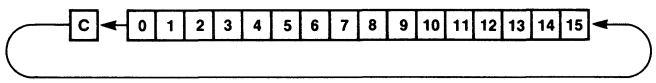
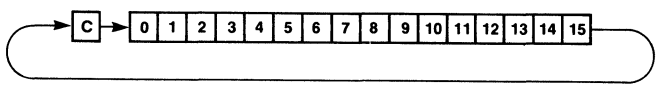


Fig. 4 Memory Reference Instructions

Arithmetic/Logic instructions perform arithmetic (ADD, ADC, INC, NEG, SUB) or Boolean (AND, COM, MOV) operations on the contents of two registers. The results of each operation together with the carry bit form a 17-bit word that can be rotated once to the left or to the right.



Rotate Left



Rotate Right

The carry bit is calculated according to a base value, as specified by the carry code. That base value is complemented if the arithmetic operation produces a carry out of bit 0; otherwise the carry bit is equal to the base value. During a byte swap operation, bits 0-7 and 8-15 of the result are swapped. The carry bit is not affected.

After the shift and still as part of the same arithmetic/logic instruction, the 9440 checks the shifted word and the new carry bit for zero or non-zero results. According to the skip code, the 9440 may skip the next instruction.

The 17-bit shifted word is loaded into the Carry FF and the destination accumulator only if bit 12 of the instruction is '0'. Loading is inhibited if bit 12 is '1'.

Arithmetic and Logic Functions

COM — *Complement.* The 9440 operates on the contents of the source accumulator, logically complementing it.

NEG — *Negate.* The 9440 calculates the 2's complement of the contents of the source accumulator. The base value for the carry bit is complemented only if SRC contained '0'.

MOV — *Move.* The 9440 takes the contents of the source accumulator, together with the base value for the carry bit, and performs the operation specified by the shift code as explained above.

INC — *Increment.* The 9440 adds '1' to the contents of the source accumulator.

ADC — *Add Complement.* The 9440 complements the contents of the source accumulator and adds it to the contents of the destination accumulator.

SUB — *Subtract.* The 9440 calculates the 2's complement of the contents of the source accumumlator and adds it to the contents of the destination accumulator (DST - SRC).

ADD — *Add.* The 9440 adds the contents of the source accumulator and the contents of the destination accumulator (SRC + DST).

AND — *And.* The 9440 computes the logic AND function on the source and destination accumulators (SRC•DST).

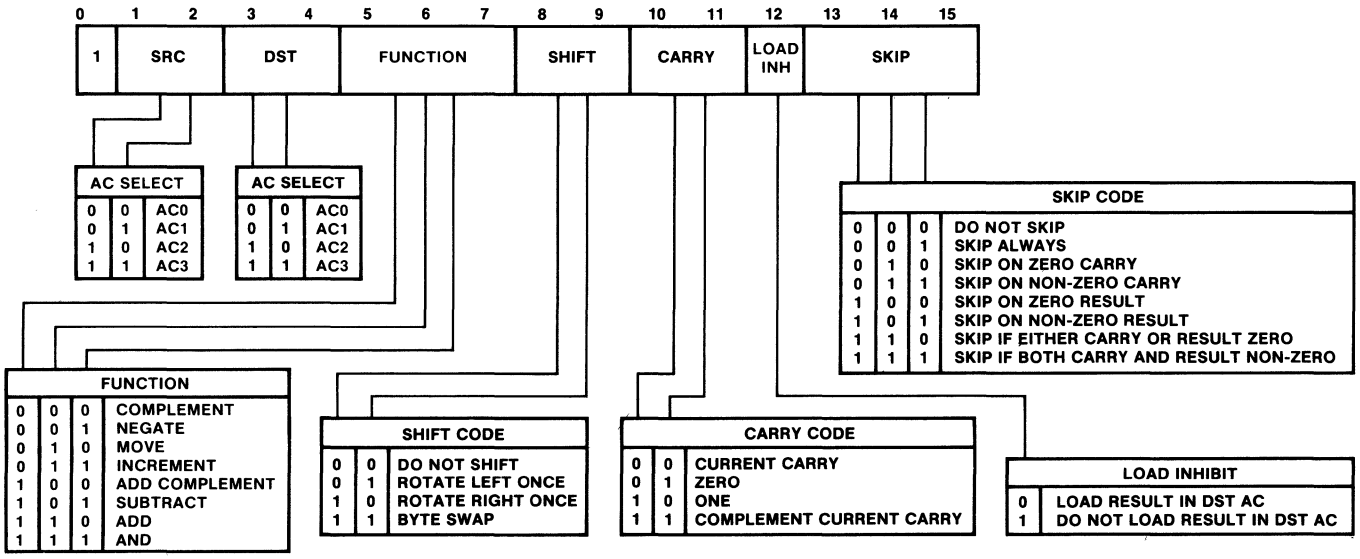


Fig. 5 Arithmetic/Logic Instructions

Input/Output instructions move data between the 9440 accumulators and three buffers in the peripheral device interface. These instructions also perform control functions in the I/O device and test the status flags in both the peripheral circuitry and the central processor.

NIO — *No Input/Output transfer.* The I/O device specified by the device code performs the control function defined by bits 8 and 9 of the instruction.

DIA/B/C — *Data In A or B or C.* The I/O device specified by the device code performs the control function and sends the contents of its A, B or C buffers to the 9440. The processor loads that data into the selected accumulator.

DOA/B/C — *Data Out A or B or C.* The 9440 sends the contents of the selected accumulator to the I/O device specified by the device code. The I/O device stores the data in its A, B or C buffers and performs the control function.

SKPBN — *Skip if Busy is Non-Zero.* The 9440 skips the next instruction if the busy flag in the I/O device specified by the device code is '1'. No control function is executed.

SKPBZ — *Skip if Busy is Zero.* The 9440 skips the next instruction if the busy flag in the I/O devices specified by the device code is '0'. No control function is executed.

SKPDN — *Skip if Done is Non-Zero.* The 9440 skips the next instruction if the done flag in the I/O device specified by the device code is '1'. No control function is executed.

SKPDZ — *Skip if Done is Zero.* The 9440 skips the next instruction if the done flag in the I/O device specified by the device code is '0'. No control function is executed.

Special Device Code-77 Instruction — Device code 77 (octal) is used for some special instructions. Some like IORST or Mask Out are common to all I/O devices; others, like Interrupt Enable or Halt are special CPU instructions. In all device code-77 instructions except the skip instructions, bits 8 and 9 control the Interrupt Enable flip-flop in the 9440; An '01' code is used to set it, '10' to reset it.

NIOS CPU — *Interrupt Enable.* The 9440 sets the Interrupt-Enable flip-flop after a delay of one instruction to allow for jumping back from an interrupt service routine.

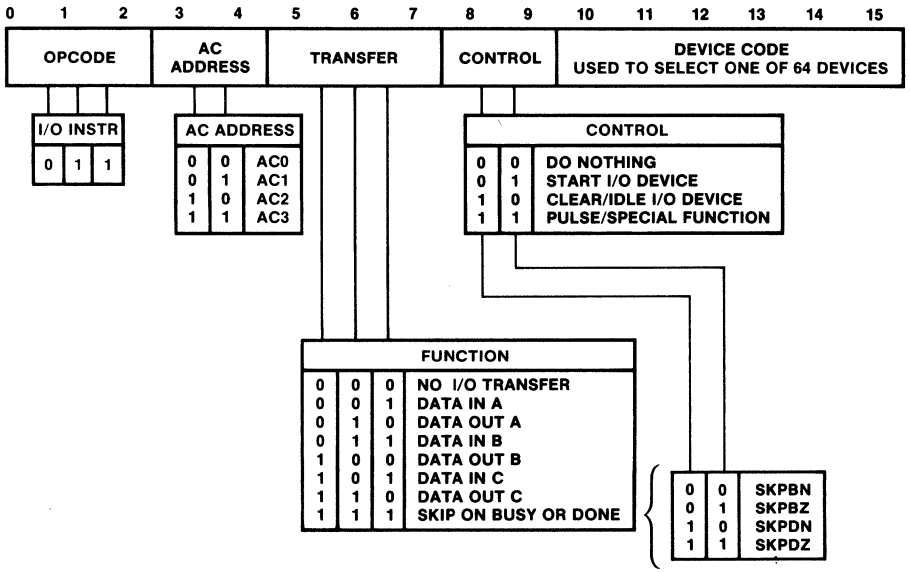


Fig. 6 Input/Output Instructions

NIOC CPU — *Interrupt Disable.* The 9440 clears the Interrupt-Enable flip-flop and does not respond to subsequent interrupt requests.

DIA CPU — *Read Switches.* The 9440 loads the contents of the front-panel switches into the specified accumulator.

DIB CPU — *Interrupt Acknowledge.* The 9440 loads the device code of the highest priority I/O device requesting an interrupt into bits 10-15 of the specified accumulator.

DOB CPU — *Mask Out.* The 9440 puts the contents of the specified accumulator on the information bus. Each I/O device is assigned a particular bit in that word. When the mask bit is '1', the device disables its interrupt.

DIC CPU — *Clear I/O Devices or IORST.* All I/O devices connected to the bus must clear their control flip-flops, including Busy and Done, and disable their interrupts.

DOC CPU — *Halt.* The 9440 halts after executing this instruction and the console displays the Halt instruction on the data light. The location of the Halt instruction is displayed on the address lights.

SKPBN CPU — *Skip if Interrupt Enable is Non-Zero.* The 9440 will skip the next instruction if the Interrupt-Enable flip-flop is enabled.

SKPBZ CPU — *Skip if Interrupt Enable is Zero.* The 9440 skips the next instruction if the Interrupt-Enable flip-flop is disabled.

9440 MODES OF ADDRESSING

The flexible addressing structure of the 9440 consists of four types of addressing — one is absolute addressing of page zero, i.e. the first 256 locations in the memory; the other three are relative addressing where an 8-bit displacment in the memory reference instruction is treated as a signed number and added to a 15-bit base address in an index register, either AC2, AC3, or PC. Each type may be either direct or indirect for a total of eight modes. Relative addressing using accumulator AC2 or AC3 is useful for accessing consecutive entries from a table in the memory, e.g., where a displacement is added to the incrmented index in the accumulator. Relative addressing utilizing the program counter is used for jumping to nearby locations when a relocatable program is executed.

In direct addressing, the 15-bit computed value is the actual address used to read or store the operand. In case of indirect addressing (bit 5 of the instruction is '1'), the computed value is the address of an address. The data read from an indirectly addressed location can be the final effective address or another nested indirect address depending on the most significant bit in that word.

Bit 0 of the word read from the indirectly addressed location is treated as another indirect bit. Bits 1-15 are the effective address if bit 0 is '0'. If bit 0 is '1', bits 1-15 point to a location in memory where the next level of indirect address resides. This process can continue indefinitely, as long as bit 0 of each word read from memory is '1'.

When locations $(20)_8$ through $(27)_8$ are indirectly addressed, the auto-increment feature takes over and the contents of the selected location are first incremented and the new value is treated as the new address, which can be either direct or indirect. Locations $(30)_8$ through $(37)_8$ are used as auto-decrement locations in a similar fashion.

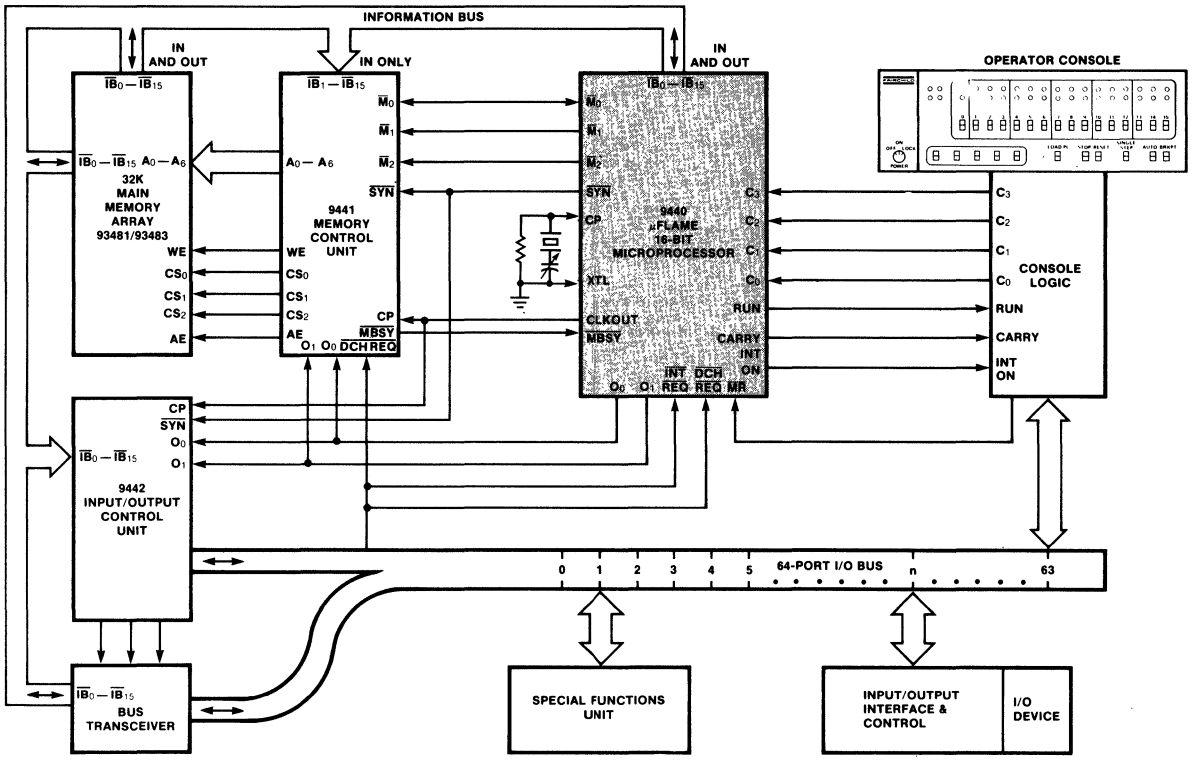


Fig. 7 9440 Microflame System

9440 SYSTEM

The 9440 CPU is a powerful machine that acts as the heart of a minicomputer-class microprocessor. However, to maximize performance, any CPU must be surrounded by support devices. A perfectly matched system can be built as shown in *Figure 7*.

Here, in addition to the 9440 CPU, the system contains the 9441 Memory Control Unit, the 9442 Input/Output Control Unit, the Special Functions Unit and an array of 93481 or 93483 I³L dynamic memories as follows:

9441 Memory Control Unit contains a 15 bit memory address register, refresh address counter and a 7-bit address multiplexer. It provides the timing and control signals to operate the I³L dynamic memory (93481, 93483) for read, write, refresh and DMA operations.

9442 Input/Output Control Unit responds to I/O instructions and generates the timing and control signals for 9440 peripheral devices.

93481 4K I³L bipolar dynamic memory. Single 5 V supply, 100 ns performance, compatible semiconductor memory.

93483 16K I³L bipolar dynamic memory. Single 5 V supply, 100 ns performance, compatible semiconductor memory.

ABSOLUTE MAXIMUM RATINGS (beyond which the useful life of the device may be impaired)

Storage Temperature	−65° to 150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 to +6.0 V
Input Voltage (dc)	−0.5 to +5.5 V
Input Current (dc)	−20 to +5 mA
Output Voltage (Output HIGH)	−0.5 to +5.5 V
Output Current (dc) (Output LOW)	+20 mA
Injector Current (I_{INJ})	+500 mA
Injector Voltage (V_{INJ})	−0.5 to +1.5 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0 to 75°C)

$I_{INJ(min)}$ = 300 mA, $I_{INJ(max)}$ = 400 mA, $V_{CC(min)}$ = 4.75 V, $V_{CC(max)}$ = 5.25 V

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		−0.9	−1.5	V	V_{CC} = 4.75 V, I_{IN} = −18 mA I_{INJ} = 300 mA
V_{OH}	Output HIGH Voltage $\overline{RUN}$, CARRY, INT ON, $\overline{SYN}$, CLK OUT, O_0, O_1	2.4	3.4		V	V_{CC} = 4.75 V, I_{OH} = −400 μA I_{INJ} = 300 mA
	Output HIGH Voltage $\overline{IB}_0$ − $\overline{IB}_{15}$	2.4	3.4		V	V_{CC} = 4.75 V, I_{OH} = −1.0 mA I_{INJ} = 300 mA
I_{CEX}	Output Leakage $\overline{M}_0$, $\overline{M}_1$, $\overline{M}_2$			1.0	mA	V_{CC} = 4.75 V, V_{OH} = 5.25 V I_{INJ} = 300 mA
V_{OL}	Output LOW Voltage		0.25	0.5	V	V_{CC} = 4.75 V, I_{OL} = 8.0 mA I_{INJ} = 300 mA
I_{IH}	Input HIGH Current C_0 — C_3, $\overline{DCH\ REQ}$, $\overline{INT\ REQ}$, $\overline{MBSY}$, $\overline{MR}$		1.0	20	μA	V_{CC} = 5.25 V, V_{IN} = 2.7 V I_{INJ} = 300 mA
	Input HIGH Current CP		2.0	40	μA	V_{CC} = 5.25 V, V_{IN} = 2.7 V I_{INJ} = 300 mA
	Input HIGH Current $\overline{IB}_0$ − $\overline{IB}_{15}$ (3-State)		5.0	100	μA	V_{CC} = 4.75 V, V_{IN} = 2.7 V I_{INJ} = 300 mA
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = 4.75 V, V_{IN} = 5.5 V I_{INJ} = 300 mA
I_{IL}	Input LOW Current All inputs except CP		−0.21	−0.36	mA	V_{CC} = 5.25V, V_{IN} = 0.4 V I_{INJ} = 300 mA
	Input LOW Current CP		−0.42	−0.72	mA	V_{CC} = 5.25 V, V_{IN} = 0.4 V I_{INJ} = 300 mA
I_{OZH}	OFF State (High Impedance) Output Current $\overline{IB}_0$ − $\overline{IB}_{15}$			100	μA	V_{CC} = 5.25 V, V_{OUT} = 2.4 V I_{INJ} = 300 mA
I_{OZL}	OFF State (High Impedance) Output Current $\overline{IB}_0$ − $\overline{IB}_{15}$		−0.21	−0.36	mA	V_{CC} = 5.25 V, V_{OUT} = 0.4 V I_{INJ} = 300 mA
I_{OS}	Output Short Circuit Current All Outputs Except $\overline{M}_0$, $\overline{M}_1$, $\overline{M}_2$	−15		−100	mA	V_{CC} = 5.25 V, V_{OUT} = 0.0 V I_{INJ} = 300 mA
I_{CC}	Supply Current		150	200	mA	V_{CC} = 5.25 V
V_{INJ}	Injector Voltage		1.0		V	I_{INJ} = 300 mA

AC CHARACTERISTICS: T_A = 0 to 75°C — Figures 8 & 9 V_{CC} = 5.0 V I_{INJ} = 300 mA

SYMBOL	CHARACTERISTIC	LIMITS-ns			NOTE
		MIN	TYP	MAX	
t_{CPSYL}	Propagation Delay, CLOCK to $\overline{SYN}$ going LOW		150		
t_{CPSYH}	Propagation Delay, CLOCK to $\overline{SYN}$ going HIGH		160		
t_{MBSYL}	Propagation Delay, $\overline{MBSY}$ going HIGH to $\overline{SYN}$ going LOW		70		
t_{MBW}	$\overline{MBSY}$ Min Pulse Width (HIGH)		30		
t_{MBS}	Set-up Time, $\overline{MBSY}$ HIGH to CLOCK		−40		
t_{MBHD}	Hold Time, $\overline{MBSY}$ HIGH after CLOCK		60		
t_{CPMH}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going HIGH		140		
t_{CPML}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going LOW		150		
t_{CPOH}	Propagation Delay, CLOCK to O_1, O_0 going HIGH		140		Fig. 9 Only
t_{CPOL}	Propagation Delay, CLOCK to O_1, O_0 going LOW		150		Fig. 8 Only
t_{CPAH}	Propagation Delay, CLOCK to ADDRESS $\overline{IB}_{0-15}$ going HIGH		170		
t_{CPAL}	Propagation Delay, CLOCK to ADDRESS $\overline{IB}_{0-15}$ going LOW		180		
t_{MBAF}	Propagation Delay, $\overline{MBSY}$ to ADDRESS $\overline{IB}_{0-15}$ going 3-state		110		
t_{DS}	Set-up Time, DATA $\overline{IB}_{0-15}$ to CLOCK		−110		
t_{DHD}	Hold Time, DATA $\overline{IB}_{0-15}$ after CLOCK		130		
t_{CS}	Set-up Time, C_3, C_2, C_1, C_0 to CLOCK		−110		
t_{CHD}	Hold Time, C_3, C_2, C_1, C_0 after CLOCK		130		
t_{CPRH}	Propagation Delay, CLOCK to RUN HIGH		140		Fig. 8 Only
t_{CPRL}	Propagation Delay, CLOCK to RUN LOW		150		
t_{DCS}	Set-up Time, $\overline{DCH\ REQ}$ to CLOCK		−110		
t_{DCHD}	Hold Time, $\overline{DCH\ REQ}$ after CLOCK		130		
t_{IS}	Set-up Time, $\overline{INT\ REQ}$ to CLOCK		−100		
t_{IHD}	Hold Time, $\overline{INT\ REQ}$ after CLOCK		120		
t_{CPCYH}	Propagation Delay, CLOCK to CARRY HIGH		160		
t_{CPCYL}	Propagation Delay, CLOCK to CARRY LOW		150		
t_{CPIOH}	Propagation Delay, CLOCK to INT ON HIGH		200		
t_{CPIOL}	Propagation Delay, CLOCK to INT ON LOW		190		

NOTES:
1. The Information Bus is driven as a result of the previous cycle.
2. The Fetch and Read cycles will be stretched out for slower memories.
3. Applies to console operation using this cycle type.
4. When the previous cycle was an I/O IN or I/O OUT cycle.
5. For a CONTINUE operation (#35 in the "9440 Instruction Execution" table on page 18).
6. For a LOAD PC, EXAMINE MEMORY or EXAMINE NEXT operations (#30, 31, 32 in the "9440 Instruction Execution" table on page 18).

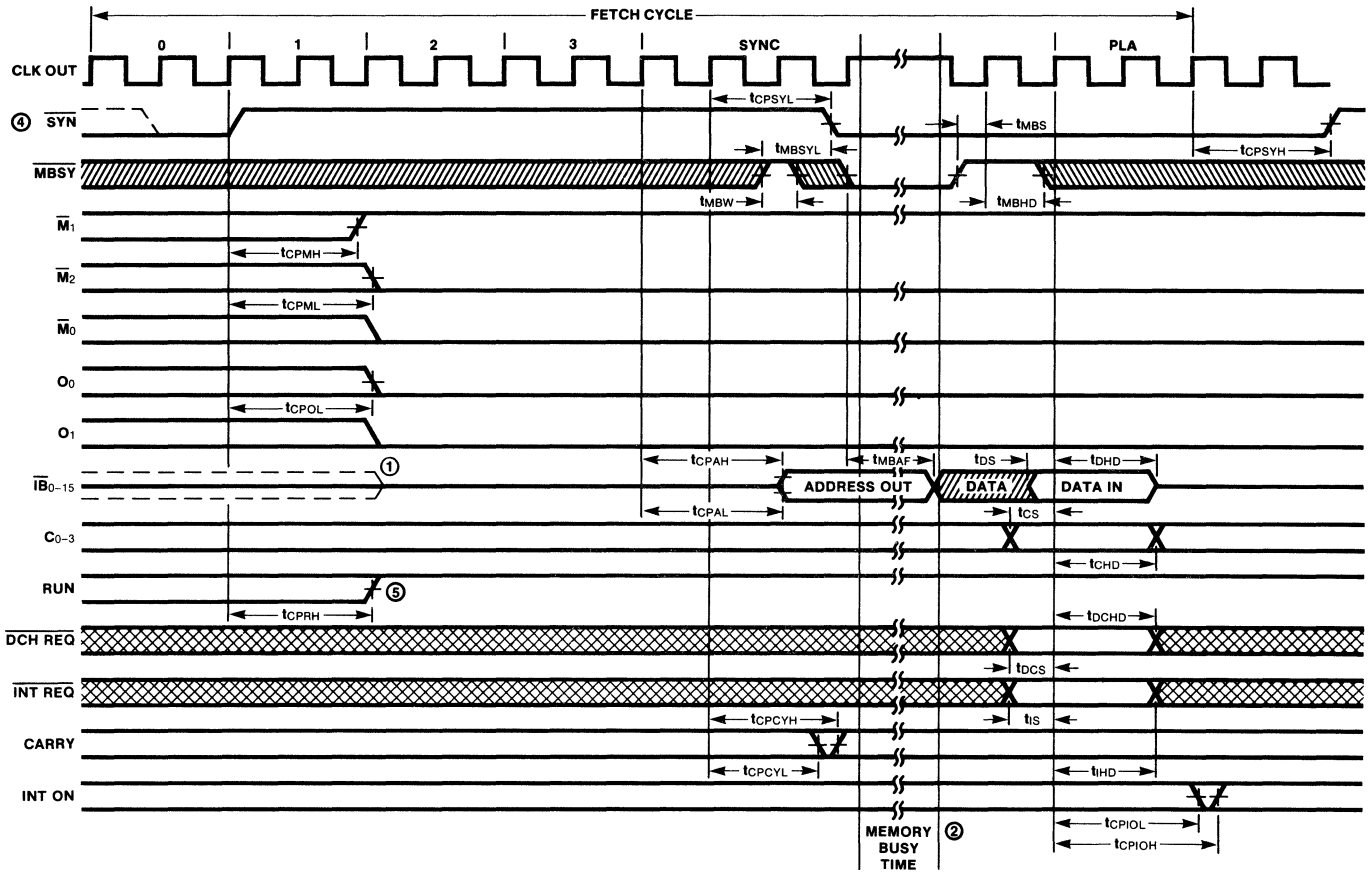
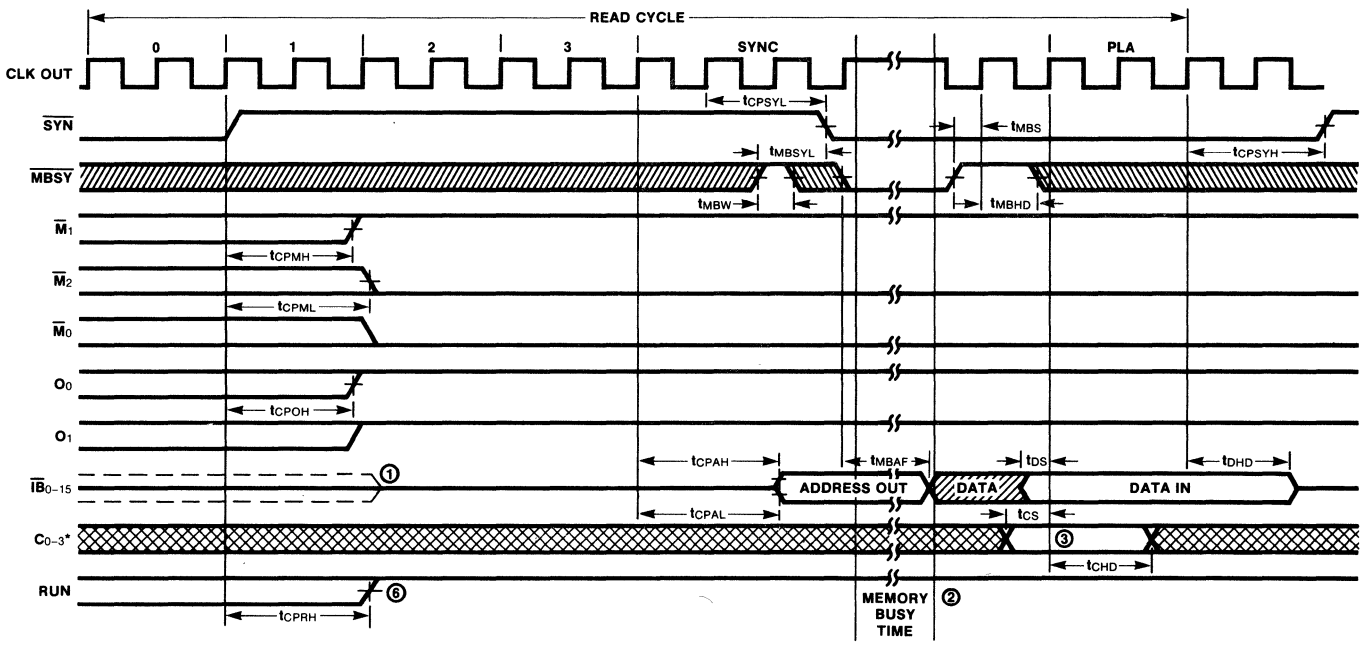


Fig. 8 Fetch Cycle



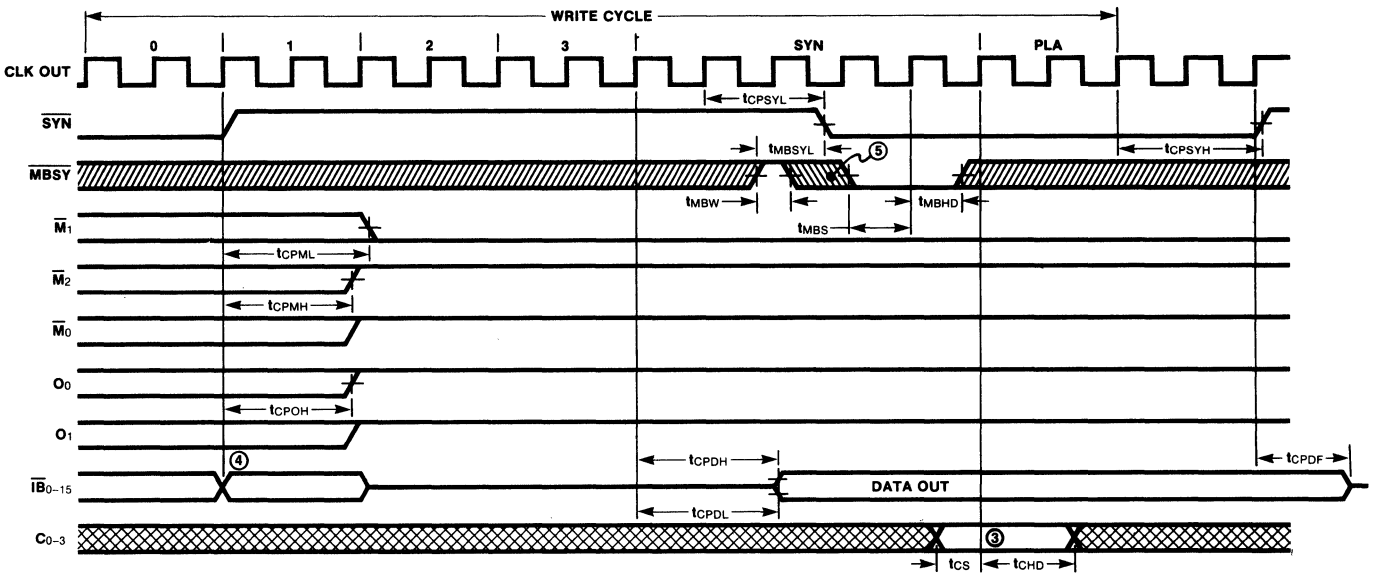
RUN, DCH REQ, INT REQ, CARRY, INT ON unaffected during this cycle.

Fig. 9 Read Cycle

AC CHARACTERISTICS: T_A = 0 to 75°C — Figures 10 & 11 V_{CC} = 5.0 V, I_{INJ} = 300 mA

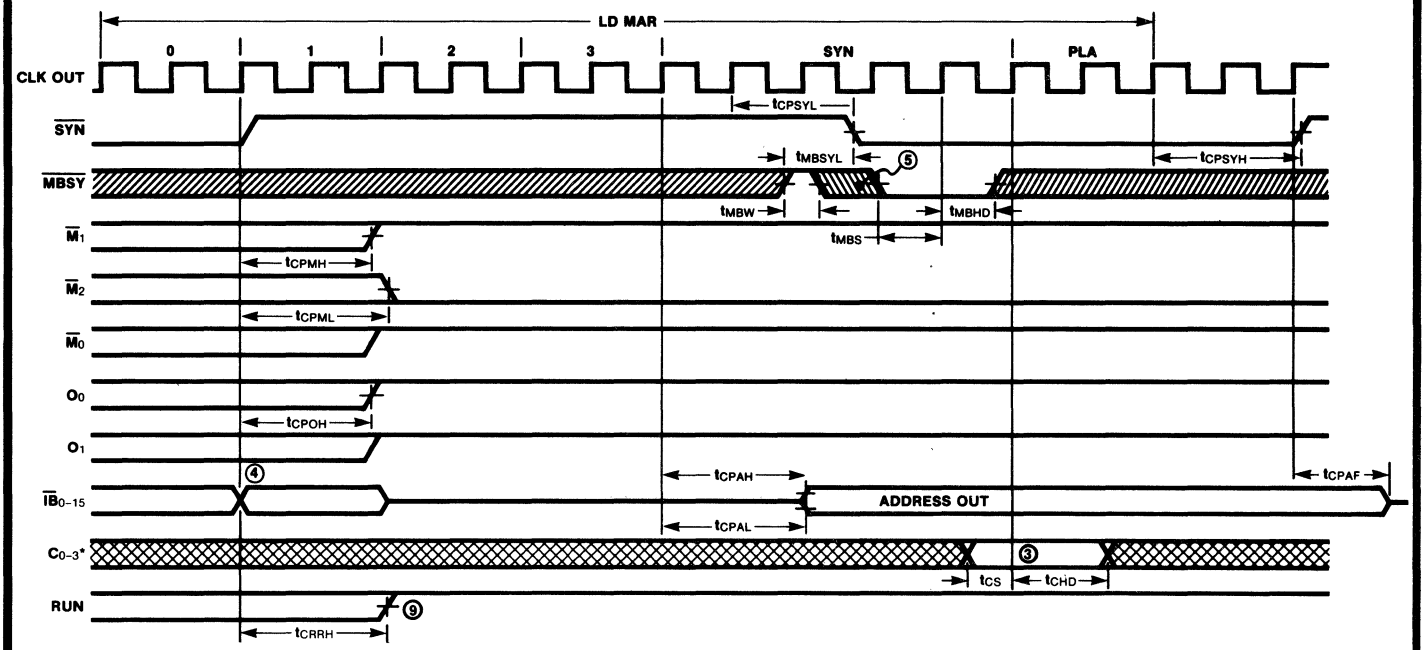
SYMBOL	CHARACTERISTIC	LIMITS-ns			NOTE
		MIN	TYP	MAX	
t_{CPSYL}	Propagation Delay, CLOCK to $\overline{SYN}$ going LOW		150		
t_{CPSYH}	Propagation Delay, CLOCK to $\overline{SYN}$ going HIGH		160		
t_{MBSYL}	Propagation Delay, $\overline{MBSY}$ going HIGH to $\overline{SYN}$ going LOW		70		
t_{MBW}	$\overline{MBSY}$ Min Pulse Width (HIGH).		30		
t_{MBS}	Set-up Time, $\overline{MBSY}$ LOW to CLOCK		–40		
t_{MBHD}	Hold Time, $\overline{MBSY}$ LOW after CLOCK		60		
t_{CPMH}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going HIGH		140		
t_{CPML}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going LOW		150		
t_{CPOH}	Propagation Delay, CLOCK to O_1, O_0 going HIGH		140		
t_{CPOL}	Propagation Delay, CLOCK to O_1, O_0 going LOW		150		
t_{CPDH}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going HIGH		170		Fig. 10 Only
t_{CPDL}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going LOW		180		
t_{CPDF}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going 3-state		110		
t_{CPAH}	Propagation Delay, CLOCK to ADDRESS $\overline{IB}_{0-15}$ going HIGH		170		Fig. 11 Only
t_{CPAL}	Propagation Delay, CLOCK to ADDRESS $\overline{IB}_{0-15}$ going LOW		180		
t_{CPAF}	Propagation Delay, CLOCK to ADDRESS $\overline{IB}_{0-15}$ going 3-state		160		
t_{CS}	Set-up Time, C_3, C_2, C_1, C_0 to CLOCK		–110		
t_{CHD}	Hold Time, C_3, C_2, C_1, C_0 after CLOCK		130		

NOTES:
7. The Information Bus is driven as a result of the previous cycle.
8. The 9440 waits for $\overline{MBSY}$ to go LOW. By holding $\overline{MBSY}$ HIGH, the user may idle the processor.
9. For DEPOSIT MEMORY or DEPOSIT NEXT operations (#33, 34 in the "9440 Instruction Execution" table on page 18).
10. For EXAMINE ACCUMULATOR or DEPOSIT ACCUMULATOR operations (#28, 29 in the "9440 Instruction Execution" table on page 18).



RUN, $\overline{DCH\ REQ}$, $\overline{INT\ REQ}$, CARRY, INT ON unaffected during this cycle.

Fig. 10 Write Cycle



DCH REQ, INT REQ, CARRY, INT ON
unaffected during this cycle.

Fig. 11 Load Memory Address Register Cycle

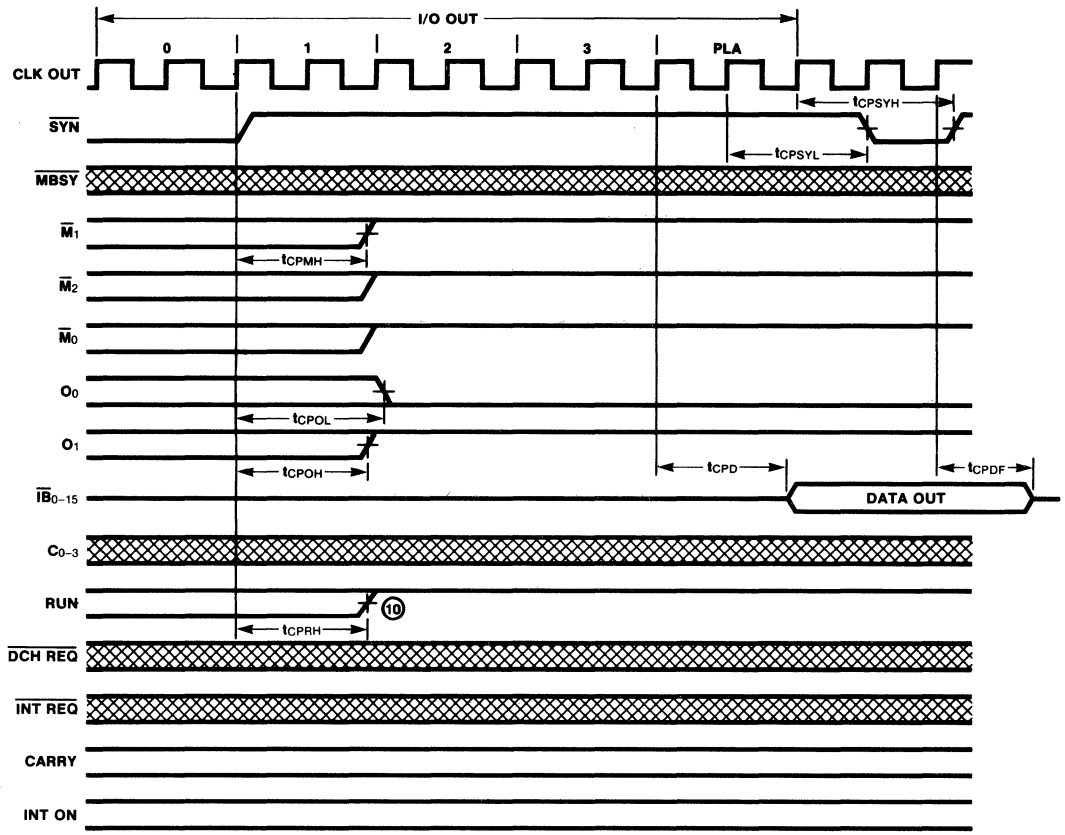


Fig. 12 I/O Out Cycle

AC CHARACTERISTICS: T_A = 0 to 75° C — Figures 12, 13, 14, 15 V_{CC} = 5.0 V, I_{INJ} = 300 mA

SYMBOL	CHARACTERISTIC	LIMITS-ns			NOTE
		MIN	TYP	MAX	
t_{CPSYL}	Propagation Delay, CLOCK to $\overline{SYN}$ going LOW		150		
t_{CPSYH}	Propagation Delay, CLOCK to $\overline{SYN}$ going HIGH		160		
t_{CPMH}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going HIGH		140		
t_{CPML}	Propagation Delay, CLOCK to $\overline{M}_2$, $\overline{M}_1$, $\overline{M}_0$ going LOW		150		
t_{CPOH}	Propagation Delay, CLOCK to O_1, O_0 going HIGH		140		
t_{CPOL}	Propagation Delay, CLOCK to O_1, O_0 going LOW		150		
t_{CPDH}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going HIGH		170		Fig. 12 Only
t_{CPDL}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going LOW		180		
t_{CPDF}	Propagation Delay, CLOCK to DATA $\overline{IB}_{0-15}$ going 3-state		110		
t_{DS}	Set-up Time, DATA $\overline{IB}_{0-15}$ to CLOCK		−110		Fig. 13 Only
t_{DHD}	Hold Time, DATA $\overline{IB}_{0-15}$ after CLOCK		130		
t_{CS}	Set-up Time, C_3, C_2, C_1, C_0 to CLOCK		−110		Fig. 14 Only
t_{CHD}	Hold Time, C_3, C_2, C_1, C_0 after CLOCK		130		

NOTES:
11. During $\overline{DCH}$, the 9440 is not driving the $\overline{M}$ lines. An external device can control the memory when a LOW is applied to the appropriate $\overline{M}$ line.
12. The 9440 floats the $\overline{IB}_{0-15}$. The Information Bus is available to the I/O devices, the Console, and the memory as needed.
13. For all the CONSOLE operations (#28-35 in the "9440 Instruction Execution" table on page 18).
14. For CONSOLE operations (#28-34 in the "9440 Instruction Execution" table on page 18).

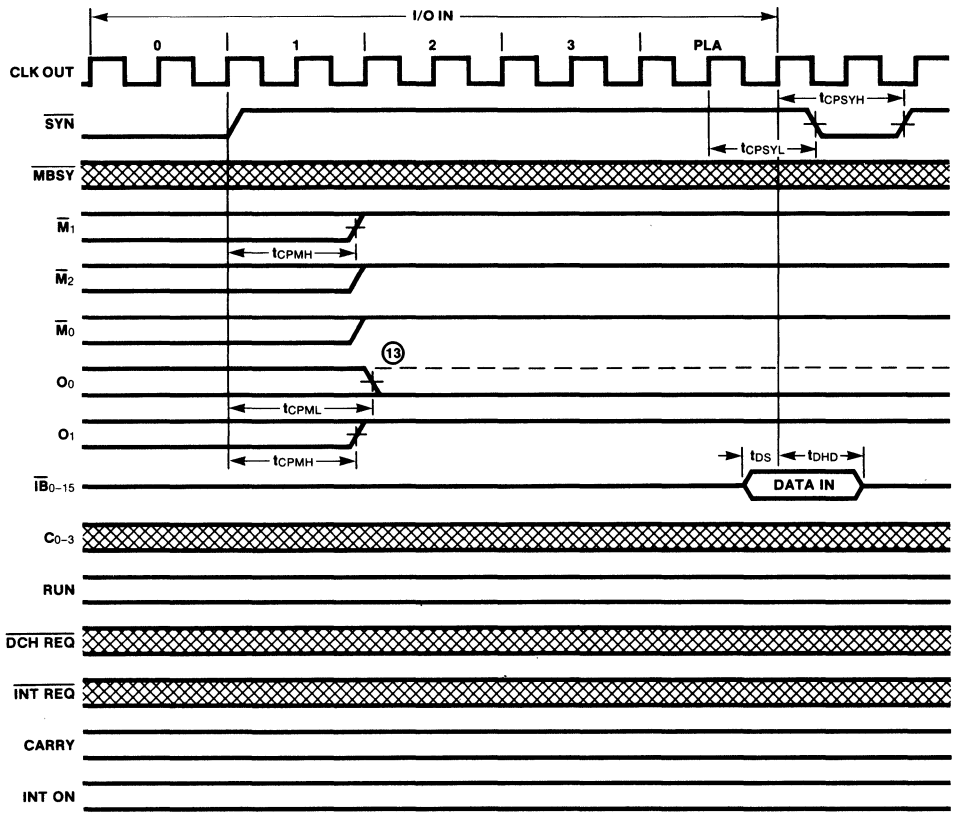


Fig. 13 I/O In Cycle

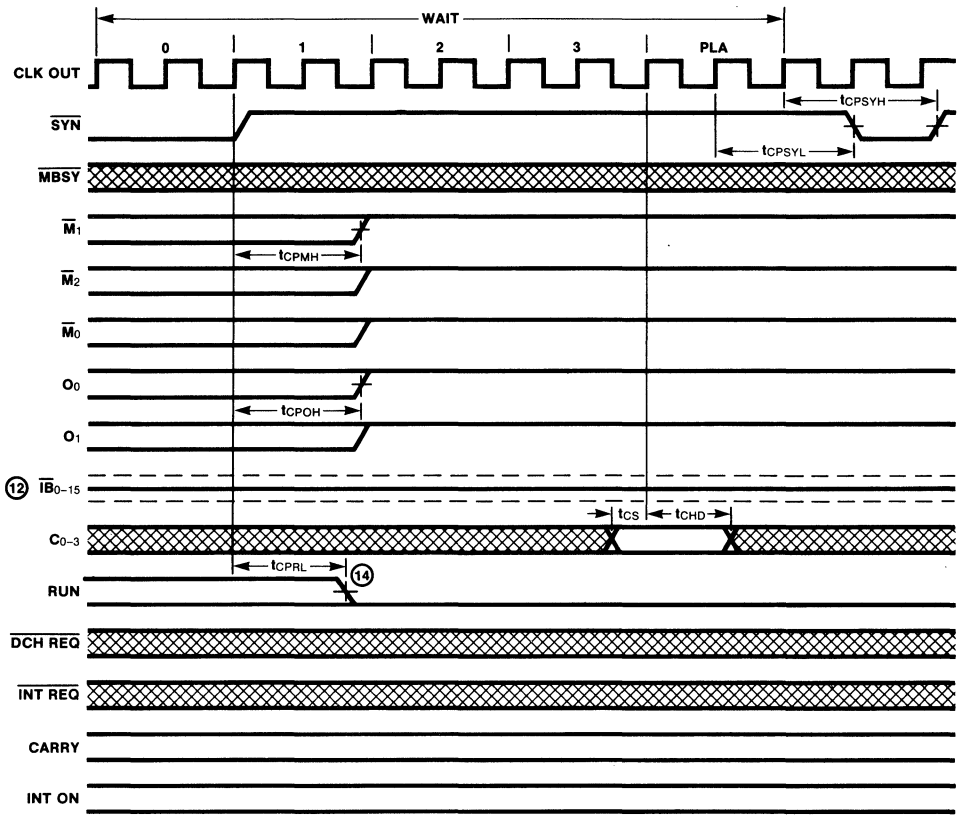


Fig. 14 Wait Cycle

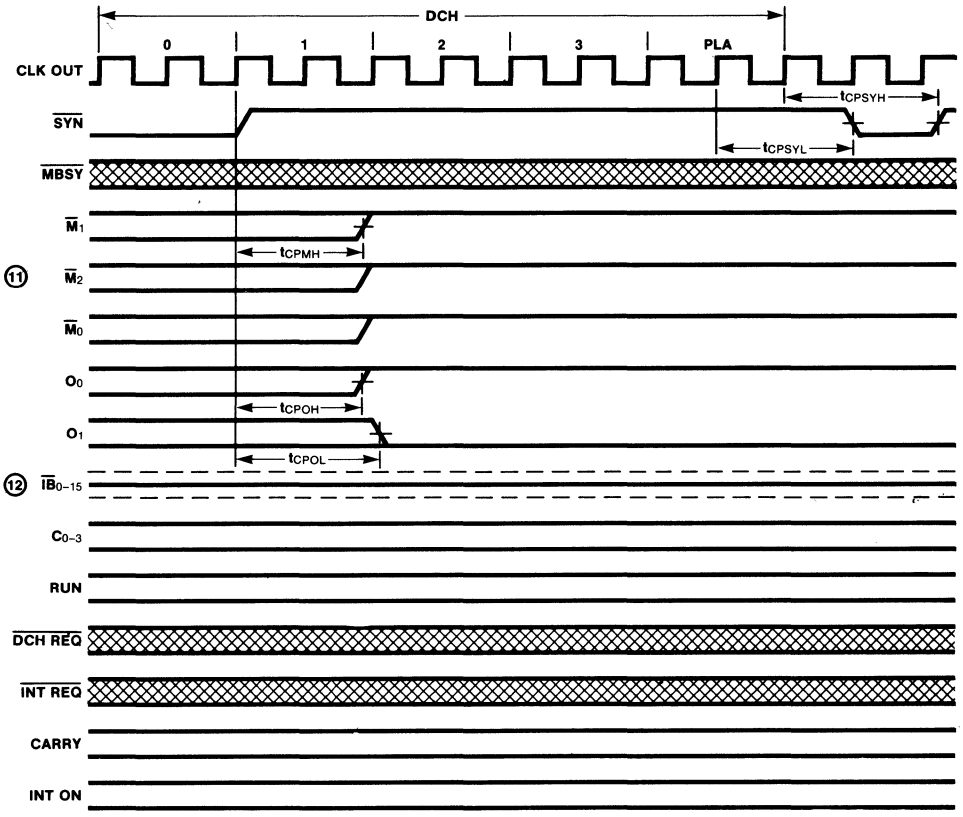


Fig. 15 Data Channel Request Cycle

9440 INSTRUCTION EXECUTION

NO.	INSTRUCTION OR OPERATION	CYCLE TYPE AND SEQUENCE*								EXECUTION TIME (μs) @		
		FETCH	READ	WRITE	LD MAR	I/O OUT	I/O IN	WAIT	DCH	8 MHz	10 MHz	12 MHz
1	Jump	1								1.875	1.5	1.25
2	Jump Indirect	3	1	2						5.50	4.4	3.66
3	Jump to Subroutine	1								1.875	1.5	1.25
4	JSR Indirect	3	1	2						5.50	4.4	3.66
5	Increment and Skip if Zero	3	1	2						5.50	4.4	3.66
6	ISZ Indirect	5	1,3	2,4						9.125	7.3	6.07
7	Decrement and Skip if Zero	3	1	2						5.50	4.4	3.66
8	DSZ Indirect	5	1,3	2,4						9.125	7.3	6.07
9	Load Accumulator	2	1							3.75	3.0	2.50
10	LDA Indirect	4	1,3	2						7.375	5.9	4.91
11	Store Accumulator	3	1	2						5.50	4.4	3.66
12	STA Indirect	5	1,3	2,4						9.125	7.3	6.07
13	Complement	1								1.875	1.5	1.25
14	Negate	1								1.875	1.5	1.25
15	Move	1								1.875	1.5	1.25
16	Increment	1								1.875	1.5	1.25
17	Add Complement	1								1.875	1.5	1.25
18	Subtract	1								1.875	1.5	1.25
19	Add	1								1.875	1.5	1.25
20	AND	1								1.875	1.5	1.25
21	ALU with Skip	1,2								3.75	3.0	2.50
22	I/O Data In	2					1			3.125	2.5	2.08
23	I/O Data Out	2				1				3.125	2.5	2.08
24	Skip on Busy or Done	2					1			3.125	2.5	2.08
25	Interrupt	5	3	2,4	1					9.0	7.2	5.98
26	Data Channel								1	1.25	1.0	0.83
27	Wait							1		1.25	1.0	0.83
28	Examine Accumulator					2	1	3		2.50	2.0	1.66
29	Deposit Accumulator					2	1	3		3.125	2.5	1.66
30	Load PC		2				1	3		3.125	2.5	2.08
31	Examine Memory		2				1	3		3.125	2.5	2.08
32	Examine Next		2				1	3		3.125	2.5	2.08
33	Deposit Memory			3	2		1	4		4.75	3.8	3.15
34	Deposit Next			3	2		1	4		4.75	3.8	3.15
35	Continue	2					1			3.125	2.5	2.08

*e.g., No. 6, ISZ Indirect:
1st cycle — READ
2nd cycle — WRITE
3rd cycle — READ
4th cycle — WRITE
5th cycle — FETCH

9440 SOFTWARE

A performance-matched package of software for the 9440 is provided to optimize the use of the 9440 in a wide range of applications. The entire software package is called the Fairchild Integrated Real-time Executive (FIRE™). The initial set of available programs consists of:

FIRE-DIAGNOSTICS for testing 9440-based systems
FIRE-LOAD bootstrap and binary loaders
FIREBUG interactive assembler, debugger and editor
} FIRE-1 PACKAGE

FIRE-SYMBUG symbolic debugger

FIRE-EDIT text editor

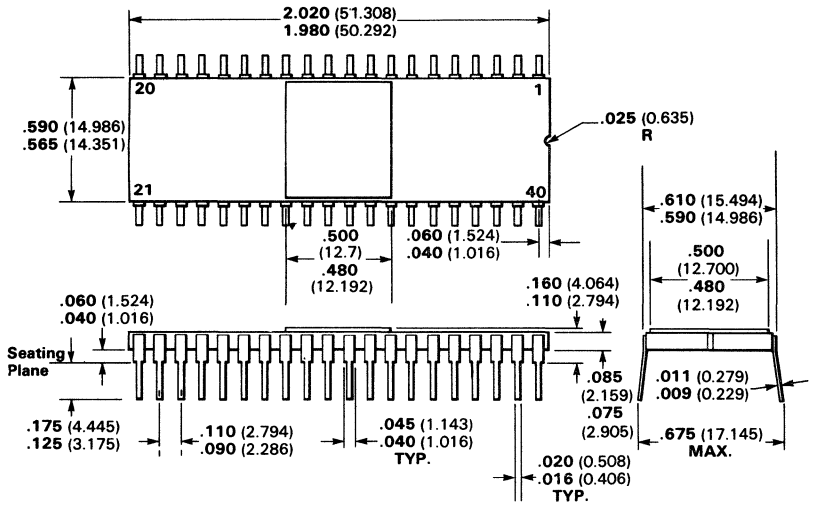
FIRE-BASIC high-level language interactive interperter

Software to be available shortly includes: a macroassembler, a floppy-disk operating system, a storage module operating system and a FORTRAN compiler.

Cross Macro Assembler, a Cross Linking Loader and a Cross Simulator Debugger are available for the FIRE Family of processors on a worldwide time sharing basis through the following company.

Mr. Michael Rooney, President
The Boston Systems Office, Inc.
469 Moody Street
Waltham, Massachusetts 02154
Tel. (617) 894-7800

PACKAGE OUTLINE
40-PIN CERAMIC DUAL
IN-LINE SIDE-BRAZED



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pin material nickel gold-plated kovar
Cap is kovar
Base is ceramic
Package weight is 6.5 grams

ORDERING INFORMATION

ORDER CODE	PACKAGE	TEMPERATURE
9440DC	CERAMIC DIP	0 TO 75°C

For other temperature ranges, contact Fairchild Sales Office.

FAIRCHILD