HIGHPOINT TECHNOLOGIES,INC.

HPT366 DATA MANUAL

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The products described in this publication are products of HighPoint Technologies.

Preface

This manual assumes some prior knowledge of current and information of HPT366 Standard.

The data manual organized into the following chapter :

Chapter 1- Overview,

Chapter 2- Signal Description,

Chapter 3- Registers.

Chapter 4- Electrical Parameters,

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Please give us your advice after you read it.

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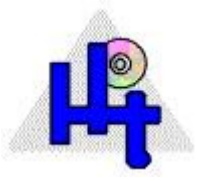
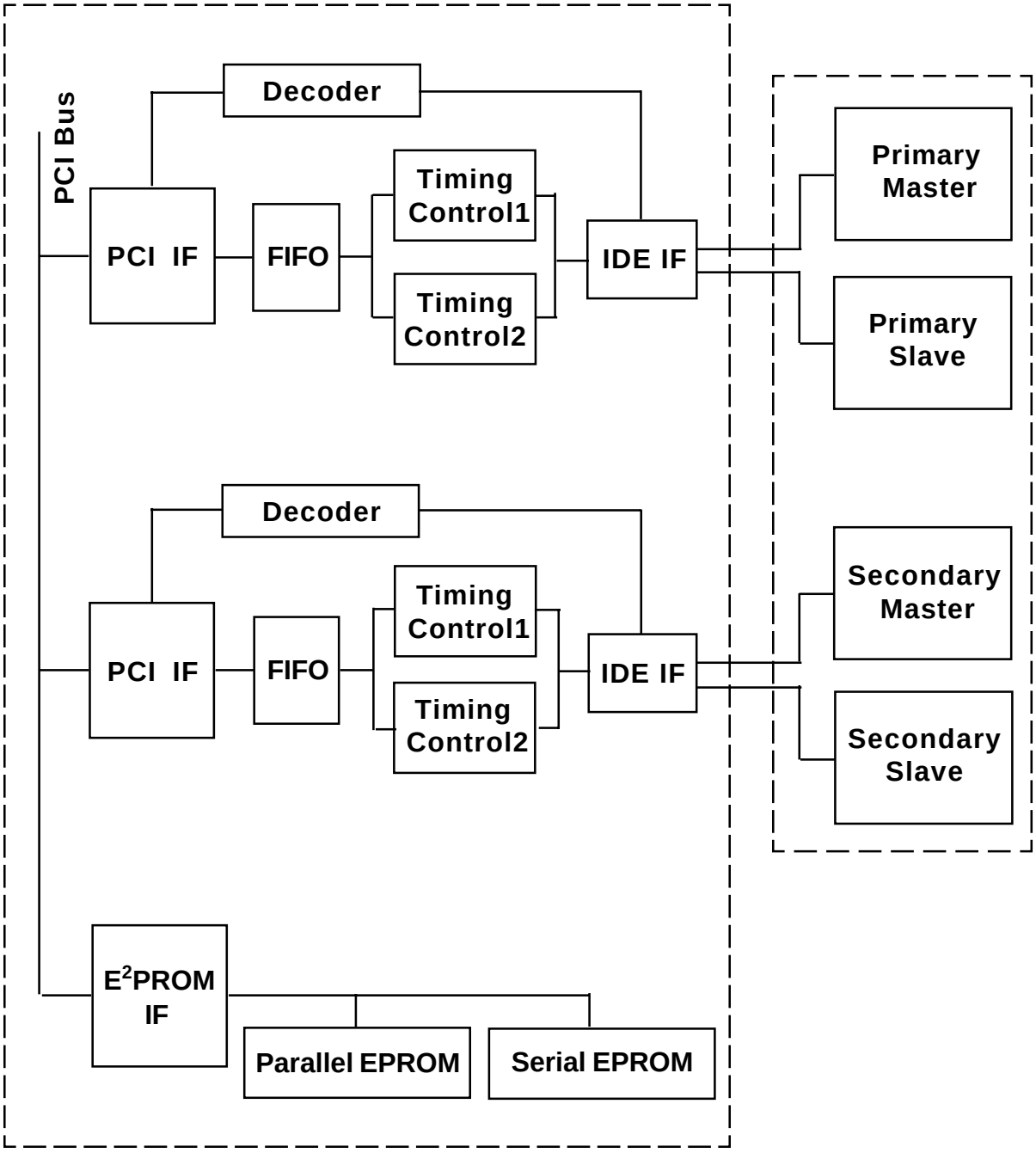
Chapter 1
Overview

Introduction

This chapter will combines information and features for the HPT366.
HPT366 has been designed to let you add additional high performance device(s) to your current computer system.



1.1 Block Diagram



1.2 Features List

There is one packages. It is 144 Pin.

- Ultra DMA 66MB/s operation.
- Two PCI functions in a single chip.
- Two independent ATA channels (one channel per PCI function).
- Dedicated ATA Bus
- 256 Byte FIFO per ATA channel.
- Large FIFO independent
- Supports all ATAPI CD-ROM, DVD-ROM, CD-R, CD-RW, LS-120, MO, Tape and ZIP devices.
- Easy Plug-and-Play feature.
- Supports up to 4 devices IDE devices. (Coexist with on-board IDE)
- Supports Hard Drive capacity large than 8.4 GB.
- Supports MS-DOS, Windows 3.x, Windows 95, Windows 98, Windows NT, OS2 WARP, Novell Netware and SCO UNIX.
- Supports booting function with Flash Memory interface.
- Automatically fine tunes to the best performance for each individual IDE/ATAPI device.
- Backward Compatible
- Concurrent PIO and bus master access (ATA port accessible during DMA transfer).
- Total ATA bus tri-state by external control and Supports Hotswap (Low signal Current)
- Reloadable PCI configuration using parallel EPROM or 2 wire serial EPROM.
- (Loading address 0 for serial size EPROM, loading address 400H for parallel EPROM.)
- 144 Pin LQFP(Dedicated Parallel EPROM pins).
- Small foot print 144 pin LQFP
- Up to 44MHz PCI bus Clock.
- Multifunction
- Embeded serial resistor on chip for ATA spec.

Chapter 2
Signal Description

Introduction Pins

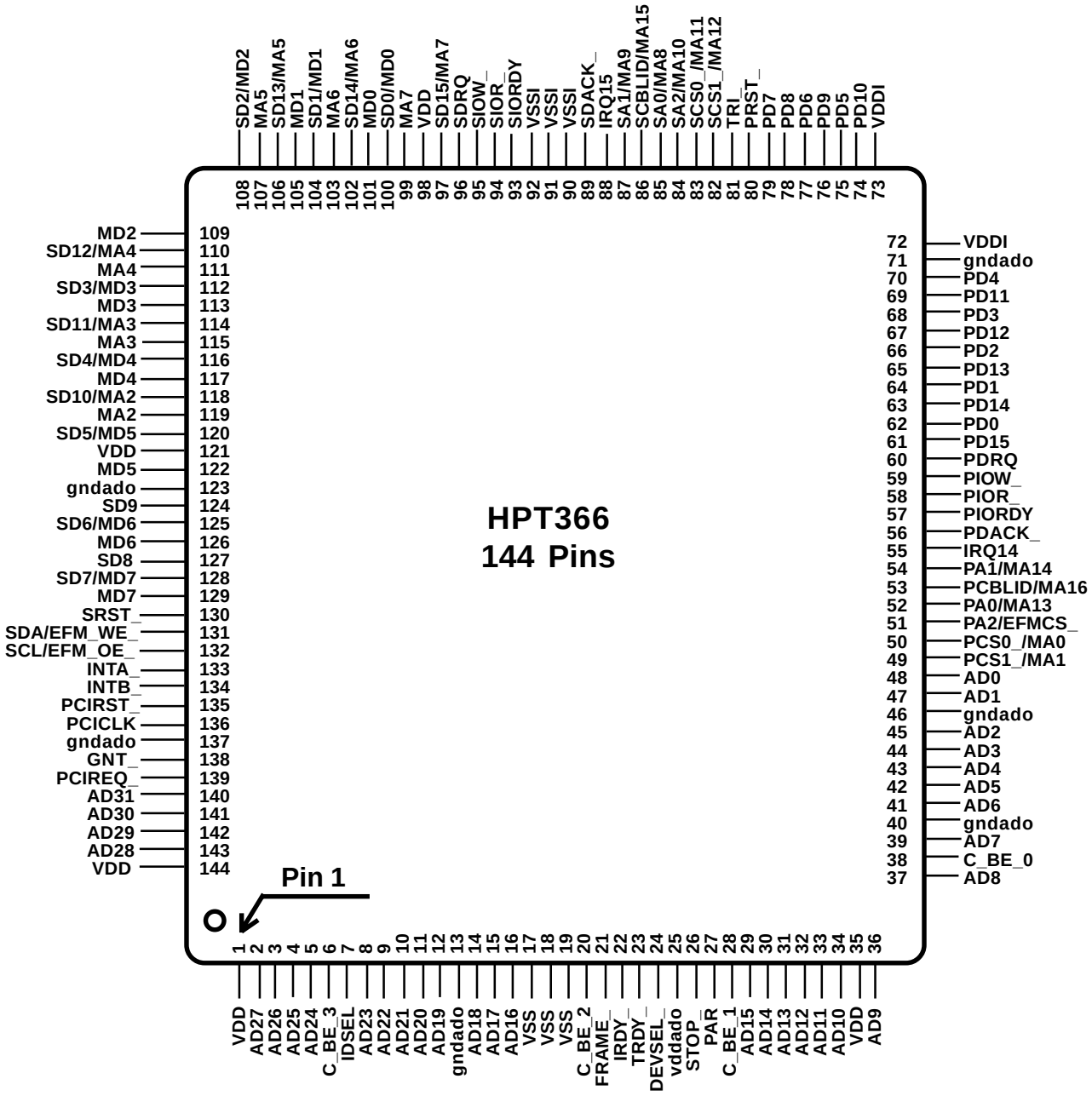
This chapter will introduction all pins for you.
The interface signals are organized into the following functional groups:

* System Pins,
* Power and Ground Pins,
* Interface Control Pins,
* Arbitration Pins,
* PCI Interrupt Pins,
* Address/Data Pins,
* IDE Interface Pins,
* EPROM Interface Pins,
* Other Pins.

There are three signal type definitions:

I ——— Input, a standard input-only signal.
O ——— Totem Pole Output, a standard output driver.
I/O ——— Input and Output.

2.1 144 Pins Signal Descriptions



2.2 144 Pins Listing

• System Pins

Pin Number	Pin Name	Type	Description
136	PCICLK	I	**Clock** provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. Clock can optionally serve as the SCSI core clock, but this may effect Fast SCSI transfer rates.
135	PCIRST_	I	**Reset PCI Bus**

• Power and Ground Pins

Pin Number	Pin Name	Type	Description
17,18,19	VSS		Ground reference power supply IC, input and output.
90,91,92	VSSI		Ground reference power supply onput, input and IC.
1,25,35, 98,121,144	VDD		Positive power supply output.
72,73	VDDI		Positive power supply output and IC.
13,40,46, 71,123,137	gndado		Ground Output

• Interface Control Pins

Pin Number	Pin Name	Type	Description
7	IDSEL	I	**Initialization Device Select** is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.
21	FRAME_	I/O	**Cycle Frame** is driven by the current master to indicate the beginning and duration of an access. FRAME_ is asserted to indicate that a bus transaction is beginning. While FRAME_ is deasserted, either the transaction is in the final data phase or the bus is idle.
22	IRDY_	I/O	**Initiator Ready** indicates the initiating agents(bus masters) ability to complete the current data phase of the transaction. IRDY_ is used with TRDY_ A data phase is completed on any clock when both IRDY_ and TRDY_ sampled asserted. During a write, IRDY_ indicates that valid data is present on AD(31-0). During a read, it indicates that master is prepared to accept data. Wait cycles are inserted until both IRDY_ and TRDY_ are asserted together.
23	TRDY_	I/O	**Target Ready** indicates the target agents(selected devices) ability to complete the current data phase of the transaction. TRDY_ is used with IRDY_. A data phase is completed on any clock when used with IRDY_. A data phase is completed on any clock when both TRDY_ and IRDY_ are sampled asserted. During a write, TRDY_ indicates that the target is prepared to accept data. During a read,it indicates that valid data is present on AD(31-0). Wait cycles are inserted until both IRDY_ and TRDY_ are asserted together.
24	DEVSEL_	I/O	**Device Select** indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
26	STOP_	I/O	**Stop** indicates that the selected target is requesting the master to stop the current transaction.

• Arbitration Pins

Pin Number	Pin Name	Type	Description
139	PCIREQ_	O	**Request** indicates to the system arbiter that this agent desires use of the PCI bus.
138	GNT_	I	**Grant** indicates to the agent that access to the PCI bus has been granted.

• PCI Interrupt Pins

Pin Number	Pin Name	Type	Description
133	INTA_	O	**Interrupt A** is used to request an interrupt.
134	INTB_	O	**Interrupt B** is used to request an interrupt and only has meaning on a multi-function device.

• Address/Data Pins

Pin Number	Pin Name	Type	Description
140,141,142, 143,2,3,4,5, 8,9,10,11,12, 14,15,16,29, 30,31,32,33, 34,36,37,39, 41,42,43,44, 45,47,48	AD(31-0)	I/O	Physical longword **Address and Data** are multiplexed on the same PCI pins. During the first clock of a transaction, AD(31-0) contain a physical byte address. During subsequent clocks, AD(31-0) contain data. A bus transaction consists of an address phase followed by one or more data phase. PCI supports both read and write bursts. AD(7-0) define the least significant byte, and AD(31-24) define the most significant byte.
6,20,28,38	C_BE_(3-0)	I/O	**Bus command and byte enables** are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE_(3-0) define the bus command. During the data phase, C_BE_(3-0) are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE_0 applies to byte 0, and C_BE_3 to byte 3.
27	PAR	I/O	**Parity** is the even parity bit that protects the AD(31-0) and C_BE_(3-0) lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

● IDE Interface Pins

Pin Number	Pin Name	Type	Description
84,87,85	SA(2-0)/ MA(10-8)	O	IDE Device Address
97,102,106, 110,114,118, 124,127,128, 125,120,116, 112,108,104, 100	SD(15-0)	I/O	IDE Data They are also used as Memory Data Bus and Memory Address Bus signal.
89	SDACK_	O	Secondary IDE DMA Acknowledge
56	PDACK_	O	Primary IDE DMA Acknowledge
93	SIORDY	I	Secondary IDE Channel I/O Ready
57	PIORDY	I	Primary IDE Channel I/O Ready
96	SDRQ	I	Secondary IDE DMA Request
60	PDRQ	I	Primary IDE DMA Request
61,63,65,67, 69,74,76,78, 79,77,75,70, 68,66,64,62	PD(15-0)	I/O	Primary IDE Data
51,54,52	PA(2-0)	O	Primary IDE Device Address Them are also used as EFMCS_ and Memory Address Bus signal.

• EPROM Interface Pins

Pin Number	Pin Name	Type	Description
53,86,54,52, 82,83,84,87, 85,97,99,102, 103,106,107, 110,111,114, 115,118,119, 49,50	MA(16-0)	O	**Memory Address Bus.** This bus is used in conjunction with the memory address strobe pins and external address latches to assemble up to a 20-bit address for an external EPROM or flash memory. This bus puts out the least significant byte first and finishes with the most significant bits. It is also used to write data to a flash memory or read data into the chip from external EPROM/flash memory. They are also use as PCBLID, SCBLID, PA(1-0), SCS1_,SCS0_,SA(2-0),SD(15-10), PCS1_ and PCS0_ signal. (Please refer to **Other Pins** for MA7.)
129,128,126, 125,122,120, 117,116,113, 112,109,108, 105,104,101, 100	MD(7-0)/ SD(7-0)	I/O	**Memory Data Bus.** This bus is used in conjunction with the memory address strobe pins and external address latches to assemble up to a 20-bit address for an external EPROM or flash memory. This bus puts out the least significant byte first and finishes with the most significant bits. It is also used to write data to a flash memory or read data into the chip from external EPROM/flash memory. All MD pins have internal pull-down resistors. They are also used Secondary IDE Data signal.
132	SCL/ EFM_OE_	O	**EPROM Output Enable.** This pin is used as an output enable signal to an external EPROM or flash memory during read operations. It is also used as a SCL signal.
131	SDA/ EFM_WE_	O	**EPROM Write Enable.** This pin is used as a write enable signal to an external flash memory. When system reset, this signal will be latched on rising edge of PCIRST_ signal. If latched values of SDA/EFM_WE_ & TRI signals are both high-LEV, the configuration will be loaded from parallel EPROM automatically. It is also used as a SDA signal.
51	PA2/ EFMCS_	O	**EPROM Chip Select.** It is also used as a Primary IDE Device Address signal.

• Other Pins

Pin Number	Pin Name	Type	Description
82	SCS1_/MA12	O	Secondary Device Chip Select 1.
83	SCS0_/MA11	O	Secondary Device Chip Select 0.
49	PCS1_/MA1	O	Primary Device Chip Select 1.
50	PCS0_/MA0	O	Primary Device Chip Select 0.
88	IRQ15	I	**Interrupt Request 15.** This pin is used to rquest an interrupt for secondary IDE port in PCI IDE Legacy Mode. (PC-AT compatible.) IRQ15 is tri-stated when IDE port 1 is in Native Mode.
55	IRQ14	I	**Interrupt Request 14.** This pin is used to request an interrupt in PCI IDE Legacy Mode. (For PC-AT compatibles.) IRQ 14 is tri-stated when IDE port 0 is in Native Mode.
94	SIOR_	O	Secondary I/O Read.
58	PIOR_	O	Primary I/O Read.
95	SIOW_	O	Secondary I/O Write.
59	PIOW_	O	Primary I/O Write.
80	PRST_	O	Primary Reset
130	SRST_	O	Secondary Reset
86	SCBLID/MA5	O	Secondary Cable Assembly Type Identifier.
53	PCBLID/MA16	O	Primary Cable Assembly Type Identifier.
81	TRI	I	When system reset, the TRI signal will be latched on rising edge of PCIRST_ signal. If the latched value of TRI is 0, the configuration will be loaded from serial EPROM automatically. When the system works normally and TRI signal is low-LEV, the outputs of ATA BUS are high- impedance.
94	MA7	I/O	When system reset, the MA7 signal will be latched on rising edge of PCIRST_ signal. If the value is 1, the IC is packaged of 144 Pins. The MA7 pin must have a external pull_up resistor (<5K).

Chapter 3
Registers

Introduction

This chapter will introduction PCI Configuration Registers and I/O Space Registers. HPT366 have two functions. In this chapter, there just list the registers of most same as PCI function 0, expect a few registers which have been listed at the same location.

3.1 Registers Listing

NO.	NAME	PAGE	ATTRIBUTE
1	Vendor ID and Device ID	3-4	
2	Command Register	3-4	
3	Status Register	3-5	
4	Revision Identification Register	3-5	
5	Class Code Register	3-6	
6	Latency Timer Register	3-6	
7	Header Type Register	3-7	PCI Configuration
8	Command Block Register	3-7	Registers
9	Control Block Register	3-8	
10	I/O Space Base Register	3-8	
11	CardBus CIS Pointer Register	3-8	
12	Subsystem Vendor ID Register	3-9	
13	Subsystem ID Register	3-9	
14	Expansion ROM Base Register	3-9	
15	Interrupt Line Register	3-10	
16	Interrupt Pin Register	3-10	

3.2 PCI Configuration Registers

The PCI Configuration registers are accessed by performing a configuration read/write to the device with its IDSEL pin asserted and the appropriate value in AD(10:8) during the address phase of the transaction. All PCI-compliant devices, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional.

Vendor ID and Device

Address: 00h-03h
Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
31:16	Device Identification Number:IDE Controller =0003h
15:0	Vendor Identification Number =1103h

***Notes:** These fields identify the manufacturer of the device and particular device.

Command Register

Address: 04h-05h
Attribute: R/W

BIT	DESCRIPTION
15:10	Reserved
9	Fast Back-to-Back Enable(Not Implemented).Hardwired 0
8 : 3	Reserved
2	Bus Master Enable.If set 1,Master Mode Enable.
1	Memory Space Enable.1=Enable.0=Disable.
0	I/O Space Enable.1=Enable.0=Disable.

Status Register

Address: 06h-07h

Attribute: Read Only

BIT	DESCRIPTION
15:14	Reserved
13	Master Abort.
12	Received Target Abort.
11	Signaled Target Abort.
10:9	DEVSEL_ Timing.Hardwired 01-Medium.
8:0	Reserved

***Notes:** Reads to this register behave normally.

Revision Identification Register

Address: 08h

Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
7 : 0	Revision ID Byte=01h.

***Note:** This field specifies device and revision identifiers.

Class Code Register

Address: 09h-0Bh

Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
23 : 0	If Compatible Mode:Class Code=010180h, If In Native Mode:Class Code=018000h.

***Notes:** This register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface.

Latency Timer Register

Address:0Dh

Attribute: R/W

BIT	DESCRIPTION
7 : 0	Latency Timer

***Notes:** The Latency Timer Register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.

Header Type Register

Address: 0Eh
Attribute: Read Only

BIT	DESCRIPTION
7 : 0	Header Type=80h.

***Notes:** This register identifies whether or not the device contains multiple functions.

Command Block Register

Primary Channel: 10h-13h
Attribute: R/W

BIT	DESCRIPTION
31 : 3	Base registers used to map Command Block registers must ask for 8 bytes of I/O space.

***Notes:** In mode the registers of the IDE channels are completely relocatable in I/O space. Base Address sters in the PCI IDE controller Configuration Space registers are used to map the IDE register into pace.

Control Block Register

Primary Channel: 14h-17h
Attribute: R/W

BIT	DESCRIPTION
31 : 2	Base Address Registers in the PCI IDE controller's Configuration Space Registers are used to map the IDE register into space. Base registers to map Control Block registers must ask for 4 bytes of I/O space. In this four-byte allocation the at offset 02h is where the Alternate Status/Device Control byte is location. Other bytes in the four-allocation(bytes at offset 0,1 and 3) are undefined and may be used for device specific purposes.

I/O Space Base Register

Address: 20h-23h
Attribute: R/W

BIT	DESCRIPTION
31:8	I/O Base Address.
7:1	Reserved.
0	Hardwired to 1.

CardBus CIS Pointer Register

Address: 28h
Attribute: Read Only. Power On Loading

Bit	Description
31:0	CardBus CIS Pointer.

Subsystem Vendor ID Register

Address: 2C-2Dh
Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
15:0	Subsystem Vendor ID.

Subsystem ID Register

Address: 2E-2Fh
Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
31:16	Subsystem ID.

Expansion ROM Base Register

Address: 30h-33h
Attribute: R/W

BIT	DESCRIPTION
31:17	ROM Base Address
16:1	Reserved
0	Address decode enable

***Notes:** This register handles the base address and size information for the expansion ROM. It functions exactly like the Base Address registers, except that the encoding of the bits is different.
The Expansion ROM Enable bit, bit 0, is the only bit defined in this register. This bit controls whether or not the device accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled, and a device is used with or without an expansion ROM depending on the system configuratio. To access the external memory interface, also set the Memory Space bit in the Command register. **It exists in function 0 only!**

Interrupt Line Register

Address: 3Ch
Attribute: R/W

BIT	DESCRIPTION
7 : 0	Interrupt Line Number.After Reset=00h.

***Notes:** This register can communicate interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value in this register tells which input of the system interrupt controller(s) the devices interrupt pin is connected to. Values in this register are specified by system architecture.

Interrupt Pin Register

Address: 3Dh
Attribute: Read Only, Power On Loading

BIT	DESCRIPTION
7 : 0	Interrupt Pin Number.Hardwired to 1.Connected to INTA_. In the function 2, Hardwired to 2. Connected to INTB_.

***Notes:** This register tells which interrupt pin the device uses. Its value is set to 01h for the Function A INTA_ signal, and 02h for the Function B INTB_ signal at power-up.

IDE Timing0 Register

Address: 40-43h
Attribute: R/W

BIT	DESCRIPTION
31	Primary Drive 0 Buffer Enable. For PIO
30	Primary Drive 0 PIO_MST Enable.
29	Primary Drive 0 Normal DMA Enable.
28	Primary Drive 0 udma Enable.
24:22	Primary Drive 0 cmd_pre_high_time.
21:19	Primary Drive 0 pre_high_time.
18:16	Primary Drive 0 udma_cycle_time.
15:12	Primary Drive 0 cmd_low_time.
11:8	Primary Drive 0 cmd_high_time.
7:4	Primary Drive 0 low time cycle number.
3:0	Primary Drive 0 high time cycle number.

IDE Timing1 Register

Address: 44-47h
Attribute: R/W

BIT	DESCRIPTION
31	Primary Drive 1 Buffer Enable. For PIO
30	Primary Drive 1 PIO_MST Enable.
29	Primary Drive 1 Normal DMA Enable.
28	Primary Drive 1 udma Enable.
24:22	Primary Drive 1 cmd_pre_high_time.
21:19	Primary Drive 1 pre_high_time.
18:16	Primary Drive 1 udma_cycle_time.
15:12	Primary Drive 1 cmd_low_time.
11:8	Primary Drive 1 cmd_high_time.
7:4	Primary Drive 1 low time cycle number.
3:0	Primary Drive 1 high time cycle number.

MISC.Control1 Register

Address: 50h
Attribute: R/W

BIT	DESCRIPTION
7	Disable channel 1Block Read/Write Bit. 1=Disable Block Read/Write. 0=Enable Block Read/Write. After Reset this bit is 0. Software can set this bit by writing a 1 to it. It is cleared by writing a 0 to this bit. This bit is R/W.
6	Disable channel 0 Block Read/Write Bit. 1=Disable Block Read/Write. 0=Enable Block Read/Write. After Reset this bit is 0. Software can set this bit by writing a 1 to it. It is cleared by writing a 0 to this bit. This bit is R/W.
5	Secondary IDE channel enable Bit. 1=Enable,0=Disable. After reset this bit is set to 1. Software can disable this bit by writing a 0 to it.
4	Primary IDE channel enable Bit.1=Enable,0=Disable. After reset this bit is set to 1.Software can disable this bit by writing a 0 to it.
3	Clear Buffer 1 Bit. 1=Clear Buffer. 0=Not Clear Buffer. Software clear buffer pointer and counter to 0 by writing this bit to 1. Clear Buffer Signal is one PCI clock Pulse only.
2	Clear Buffer 0 Bit. 1=Clear Buffer. 0=Not Clear Buffer. Software clear buffer pointer and counter to 0 by writing this bit to 1. Clear Buffer Signal is one PCI clock Pulse only.
1	Allocate Address 17x Enable Bit. 1=Enable,0=Disable. After Reset This bit is set to 0. If Dis_alc pin=0,hardware set this bit to 1 automatically. Enanble means that all Secondary IDE Device Registers are allocated to I/O. BA offset 0X18, 0X1C. This Bit=0 (Disable) means all Secondary IDE Registers are at Default IDE Addre-ss. This bit is Read Only. **(Note:In two Functions, it not existing.)**
0	Allocate Address 1Fx Enable Bit. 1=Enable,0=Disable. After Reset This bit is set to 0. If Dis_alc Pin=0,then hardware set this bit to 1 automatically. Enable means that all primary IDE Device Registers are allocated to I/O. BA OFFSET 0X10, 0X14. This Bit =0 (Disable) means all Primary IDE Registers are at Default IDE Address. This bit is Read Only. **(Note: In Function second, it's adress is 170-177 and 376.)**

MISC.Control2 Register

Address: 51h
Attribute: R/W

BIT	DESCRIPTION
15	Fast Interrupt Enable Bit. 1=enable,0=disable. If enable,Interrupt will be generated before IDE interrupt occur. After reset this bit is 0. R/W
14	Hold channel 1 Interrupt enable Bit. 1=enable,0=disable. If enable,when read from IDE interrupt will be generated after the buffer is empty. After reset this bit is 0. R/W
13	Hold channel 0 Interrupt enable Bit. 1=enable,0=disable. If enable,when read from IDE interrupt will be generated after the buffer is empty. After reset this bit is 0. R/W
12	Enable Clear SG bit. 0=Disable 1=Enable. When SG Counter is greater than IDE Transfer Size. If this bit is 1,Hardware will automatically Clear SG State Machine after Interrupt Asserted. This Bit is R/W.
11	Channel 1 Read Flush Bit. 0=Not Flush.1=Flush. Software Flush all Contents in FIFO by Writing a 1 to this bit. Flush is one PCI Clock Pulse.
10	Channel 0 Read Flush Bit. 0=Not Flush.1=Flush. Software Flush all Contents in FIFO by Writing a 1 to this bit. Flush is one PCI Clock Pulse.
9	Clear Bus Master State Machine Bit.0=Not Clear. 1=Clear. Software Clear Master State Machine by Writing a 1 to this bit. Clear Master State Machine is one PCI Clock Pulse.
8	Clear SG Counter bit. 0=Not Clear Counter. 1=Clear Counter. Software Clear SG Counter by Writing a 1 to this bit. Clear SG Counter is one PCI Clock Pulse.

MISC.Control3 Register

Address: 52h-53h

BIT	DESCRIPTION
31	Pseudo-DMA enable bit. 0=disable,1=enable. Software write a 1 to enable pseudo-dma, write a 0 to disable pseudo-dma. After reset,this bit is set to 0. R/W
30	Bus Parking AD&CBE output enable. 1=enable, 0=disable. If this bit enable when PCI GNT_ Parking on IDE,PCI AD&CBE will be drive by HPT366. After Reset this bit=0. R/W
29-27	SG State Machine Number. Read Only.
26:25	Fast Interrupt Byte counter setting Register. If 0 is set. Interrupt will be sent when the SG Counter remanin 512 Bytes. If 1 is set, Interrupt will be sent when the SG Counter remain 1K Bytes. If 2 is set, Interrupt will be sent when SG Counter remain 2K Byte. These Bits are Read/Write.
24-16	Bytes Number Remained in the channel 0 Buffer, Read Only.

MISC.Control4 Register

Address: 56h-57h

Attribute: Read Only

BIT	DESCRIPTION
31	Pseudo-DMA enable bit. 0=disable,1=enable. Software write a 1 to enable pseudo-dma, write a 0 to disable pseudo-dma. After reset,this bit is set to 0. R/W
30	Bus Parking AD&CBE output enable. 1=enable, 0=disable. If this bit enable when PCI GNT_ Parking on IDE,PCI AD&CBE will be drive by HPT366. After Reset this bit=0. R/W
29-27	SG State Machine Number. Read Only.
26:25	Fast Interrupt Byte counter setting Register. If 0 is set. Interrupt will be sent when the SG Counter remanin 512 Bytes. If 1 is set, Interrupt will be sent when the SG Counter remain 1K Bytes. If 2 is set, Interrupt will be sent when SG Counter remain 2K Byte. These Bits are Read/Write.
24-16	Bytes Number Remained in the channel 1 Buffer, Read Only.

Bus Status1 Register

Address: 58h

Attribute: Bit 0-5 is Read Only; Bit 6-7 is R/W.

BIT	DESCRIPTION
7	Secondary channel POLL_INT_EN
6	Primary channel Auto POLL Interrupt Enable. If this bit is "1", HPT366 hardware will generate an interrupt upon a successful auto Poll. (R/W)
5	Secondary channel DMARQ.
4	Secondary channel DMACK_.
3	Secondary channel IO chrdy.
2	Primary channel DMARQ.
1	Primary channel DMACK_.
0	Primary channel IO chrdy.

***Notes:** All PCI cfg registers mapping to IO Space(Addr: 20h-7bh).

Bus Status2 Register

Address: 59h

BIT	DESCRIPTION
7	Reserved
6	Function 0:1, soft Floating two functions IDE Bus; Function 1:1, soft Reset two functions IDE Bus. R/W
5	Secondary POLL_EN Reset to 0. R/W
4	Secondary IRQ_DEV1. R
3	Secondary channel IRQ_DEV0. R
2	Primary Auto POLL Function Enable. If this bit is set, HPT366 will start auto poll function after an NOP Auto Poll command is issued by the host. As defined by ATA/ATAPI-4 specification, HPT366 will return ERR bit as "0" regardless the value read from an attached device. The Auto Poll Function is terminated upon any ATA port read or write access by the host Reset to 0. R/W
1	Primary IRQ_DEV1. R
0	Auto Poll Status. "1" indicates a succerssful poll is found. R

Cable Select Register

Address: 5ah

BIT	DESCRIPTION
0	S_CBLID
1	P_CBLID

3.3 I/O Space Registers

Bus Master Command Register

Primary Channel: 00h,
Secondary Channel: 08h
Attribute: R/W

BIT	DESCRIPTION
7:4	Reserved
3	Bus Master R/W Control.Bus Master Read (Disk Write)=0,Bus Master Write (DiskRead)=1.
2:1	Reserved
0	Start/Stop Bit.Start=1, Stop=0.When This Bit is set to 1, Bus Master operation will be started. After this Bit is clear to 0,Bus Master operation will be stopped.

Bus Master Status Register

Primary Channel: 02h,
Secondary Channel: 0Ah
Attribute: R/W

BIT	DESCRIPTION
7	Reserved
6	Drive 1 DMA Capable.1=Drive support DMA, 0=Drive does not support DMA. This Bit Softw are use Only.Not affect Hardware operation.
5	Drive 0 DMA Capable.1=Drive support DMA, 0=Drive does not support DMA. This Bit Softw are use Only.Not affect Hardware operation.
4 : 3	Reserved
2	Interrupt Status Bit.1=Device issue an Interrupt, 0=Device does not issue an Interrupt. Software sets this bit to 0 by writing a 1 to it. This Bit perates on both Bus Master Mode and Slave Mode.
1	DMA Error Bit.This bit is set to 1 when target abort or master abort happened. Software set this to 0 by writing 1 to it.
0	Read Only Bit. Bus Master Active Bit. 1=Bus master operation is processing. 0=no bus master operation.

Bus Master Scatter Gather Table Base Register

Primary Channel: 04h-07h
Secondary Channel: 0Ch-0Fh
Attribute: R/W

BIT	DESCRIPTION
31:2	Bus Master Scatter Gather Table Base Address.
1 : 0	Reserved

Chapter 4
Electrical Parameters

Introduction

This chapter defines all the electrical characteristics and constraints of PCI components, systems.

The PCI electrical definition provides for 3.3V signaling environments, and all IOs of HPT366 are 5V tolerant.

4.1 3.3V Signaling Environment

The 3.3V environment is based on Vcc-relative switching voltages and is an optimized CMOS approach.

DC Specifications

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
V_{cc}	Supply Voltage		3.0	3.6	V	
V_{ih}	Input High Voltage		2.0		V	
V_{il}	Input Low Voltage			0.8	V	
V_{ipu}	Input Pull-up Voltage		$0.7V_{cc}$		V	1
I_{il}	Input Leakage Current	$0<V_{in}<V_{cc}$		± 10	uA	2
V_{oh}	Output High Voltage	I_{out}=-500uA	$0.9V_{cc}$		V	
V_{ol}	Output Low Voltage	I_{out}=1500uA		$0.1V_{cc}$	V	
C_{in}	Input Pin Capacitance			10	pF	3
C_{clk}	**CLK** Pin Capacitance		5	12	pF	
C_{IDSEL}	**IDSEL** Pin Capacitance			8	pF	4
L_{pin}	Pin Inductance			20	nH	

Notes:
1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tri-state outputs.
3. Lower capacitance on this input-only pin allows for non-resistive coupling to **AD[xx].**
4. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

AC Specifications

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
I_{oh}(AC)	Switching Current High	$0<V_{out}\leq 0.3V_{cc}$	$-12V_{cc}$		mA	1
		$0.3V_{cc}<V_{out}<0.9V_{cc}$	$-17.1(V_{cc}-V_{out})$		mA	1
		$0.7V_{cc}<V_{out}<V_{cc}$		Eqt'nC		1,2
	(Test Point)	$V_{out}=0.7V_{cc}$		$-32V_{cc}$	mA	2
I_{ol}(AC)	Switching Current Low	$V_{cc}>V_{out}\geq 0.6V_{cc}$	$16V_{cc}$		mA	1
		$0.6V_{cc}>V_{out}>0.1V_{cc}$	$26.7V_{out}$		mA	1
		$0.18V_{cc}>V_{out}>0$		Eqt'nD		1,2
	(Test Point)	$V_{out}=0.18V_{cc}$		$38V_{cc}$	mA	2
I_{cl}	Low Clamp Current	$-3<V_{in}\leq -1$	$-25+(V_{in}+1)/0.015$		mA	
I_{ch}	High Clamp Current	$V_{cc}+4>V_{in}\geq V_{cc}+1$	$25+(V_{in}-V_{cc}-1)/0.015$		mA	
$slew_r$	Output Rise Slew Rate	$0.2V_{cc}$-$0.6V_{cc}$ load	1	4	V/ns	3
$slew_f$	Output Fall Slew Rate	$0.6V_{cc}$-$0.2V_{cc}$ load	1	4	V/ns	3

***Notes:** 1. Switching current characteristics for REQ_ and GNT_ are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST_ which are system outputs.

2. Maximum current requirements must be met as drivers pull beyond the first step voltage. The equation defined maxima should be met by design.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range.

Chapter 5
Timing

Introduction

This chapter is organized into the following sections:

- Timing Parameters
- Clock Timing
- Read Transaction
- Write Transaction
- IDE Timing

5.1 Timing Parameters

The follow table provides the timing parameters for 5V and 3.3V signaling environments.

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{val}	**CLK** to Signal Valid Delay bused signals	2	11	ns	1,2
t_{val}(ptp)	**CLK** to Signal Valid Delay point to point	2	12	ns	1,2
t_{on}	Float to Active Delay	2		ns	1
t_{off}	Active to Float Delay		28	ns	1
t_{su}	Input Set up Time to **CLK**-bused signals	7		ns	2,3
$t_{su(ptp)}$	Input Set up Time to **CLK**-point to point	10,12		ns	2,3
t_{h}	Input Hold Time from **CLK**	0		ns	3
t_{rst}	Reset Active Time After Power Stable	1		ms	4
$t_{rst-clk}$	Reset Active Time After **CLK** Stable	100		us	4
$t_{rst-off}$	Reset Active to Output Float delay		40	ns	4

***Notes:** 1. For parts compliant to the 3.3V signaling environment:
Maximum times are evaluated with the following load circuits, for high-going and low-going edges respectively.
2. REQ and GNT_ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. GNT_ has a setup of 10; REQ has a setup of 12. All other signals are bused.
3. RST_ is asserted and deasserted asynchronously with respect to CLK.
4. All output drivers must be asynchronously floated when RST_ is active.

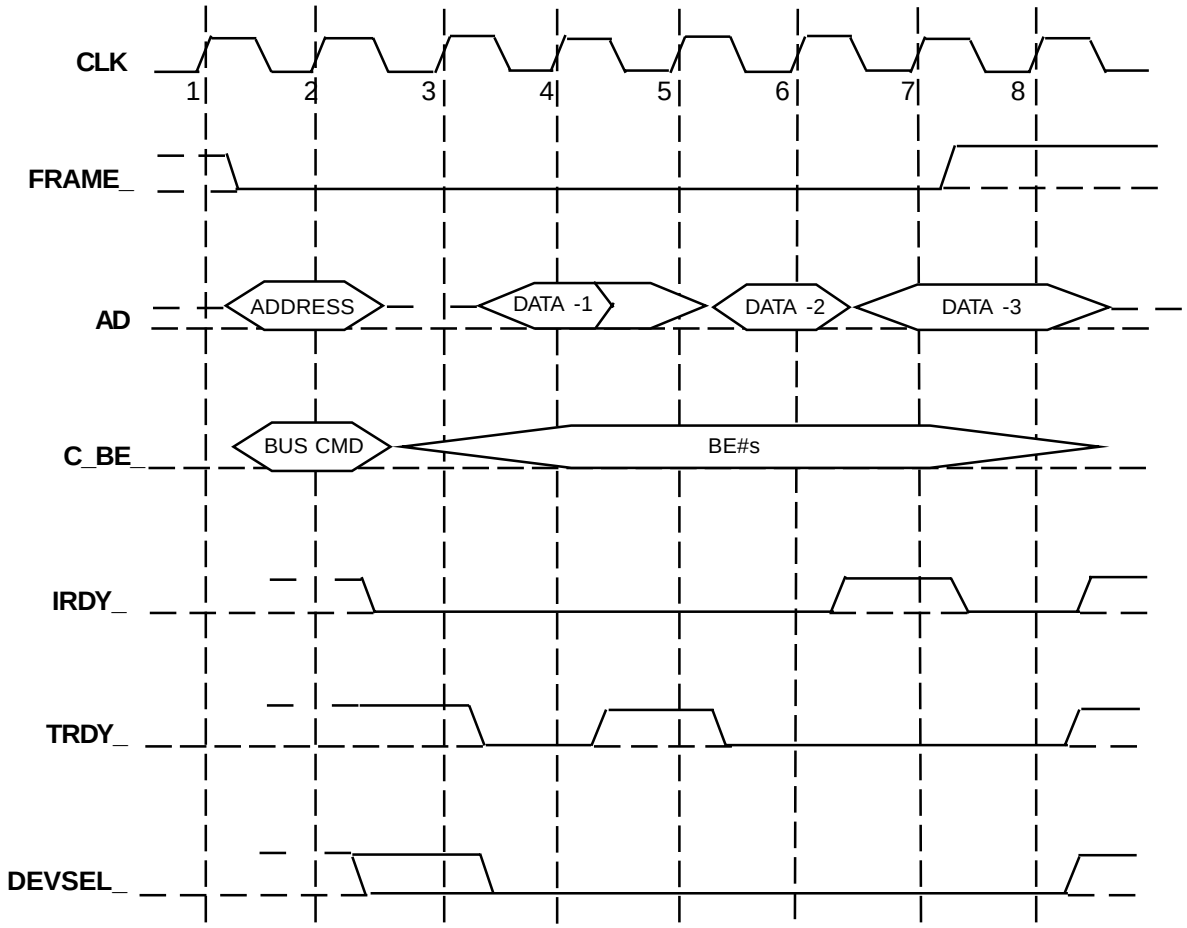
5.2 Clock Timing

Clock Specifications

		66 MHz		33 MHz			
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{cyc}	**CLK** Cycle Time	15	30	30		ns	1
t_{high}	**CLK** High Time	6		11		ns	
t_{low}	**CLK** Low Time	6		11		ns	
-	**CLK** Slew Rate	1.5	4	1	4	V/ns	2

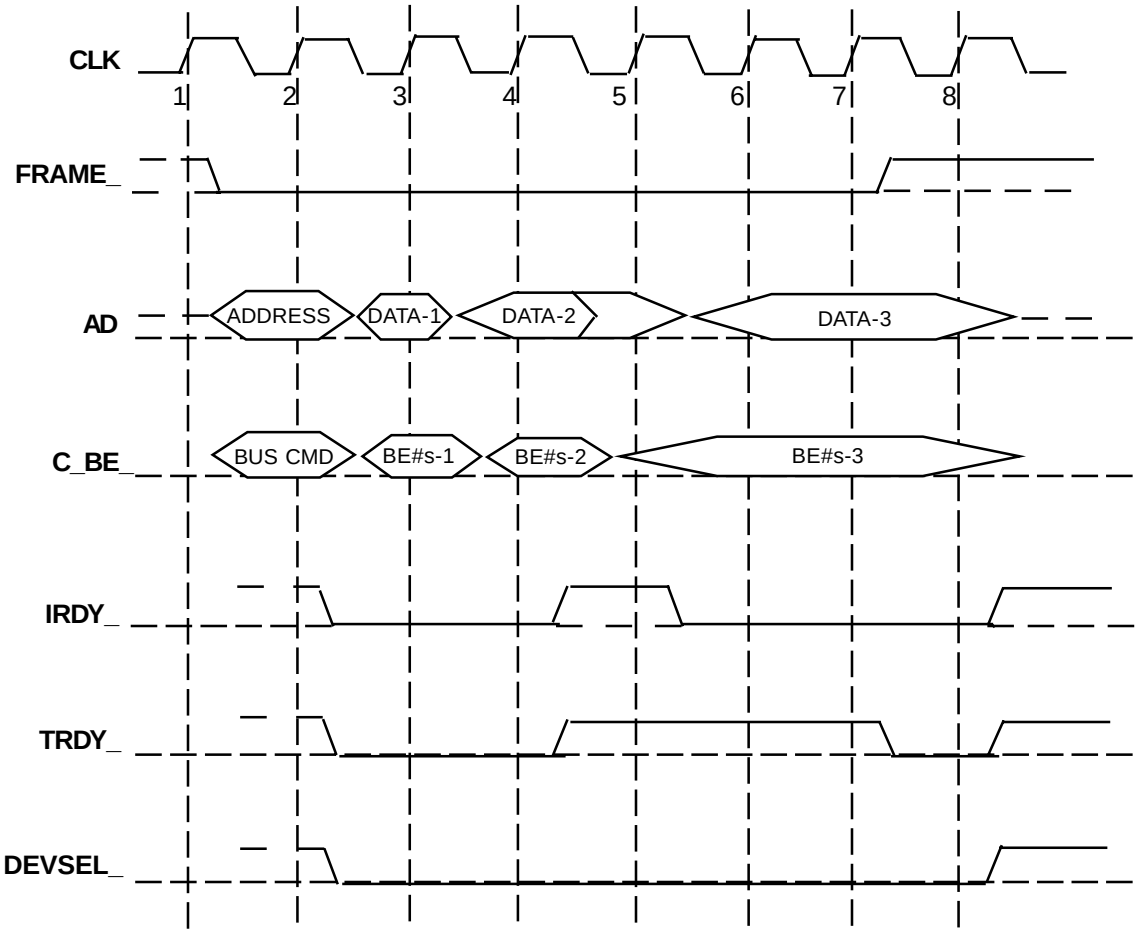
Notes:
1. In general, all 66MHz PCI components must work with any clock frequency up to 66MHz. The clock frequency may be changed at any time during the operation of the system so long as the clock edges remain clean and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
2. The minium clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

5.3 Read Transaction



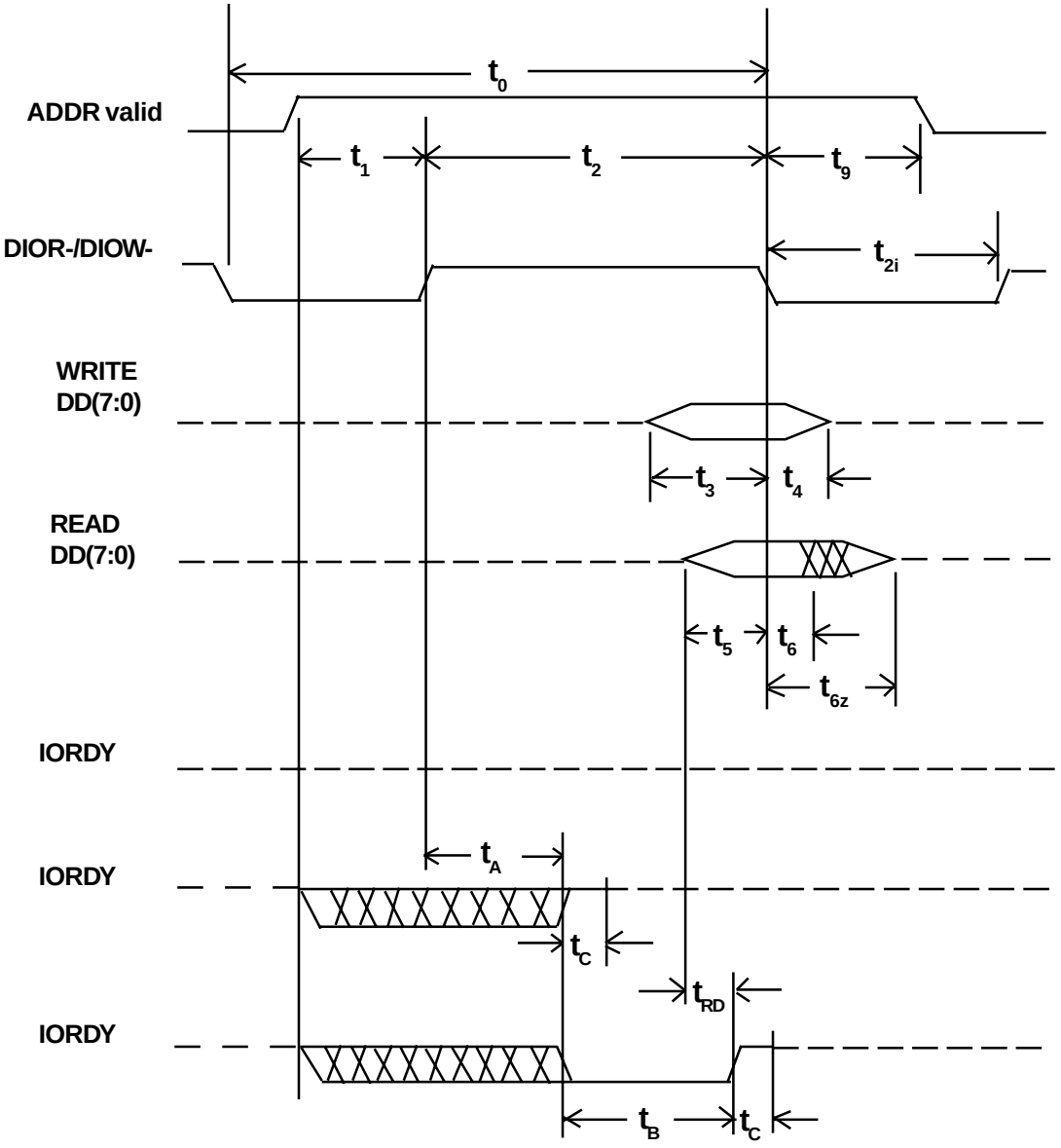
Notes: The transaction starts with an address phase which occurs when **FRAME_** is asserted for the first time and occurs on clock2. During the address phase, **AD[31:0]** contain a valid address and **C_BE_[3:0]** contain a valid bus command.

5.4 Write Transaction



***Notes:** The transaction starts when **FRAME_** is asserted for the first time which occurs on clock 2. A write transaction is similar to a read transaction except no turnaround cycle is required following the address phase because the master provides both address and data. Data phases work the same for both read and write transactions.

5.5 IDE Timing



***Notes:** 1. Device address consists of signals CS0_, CS1_ and DA(2:0).
2. Data consists of DD(7:0).
3. The negation of IORDY_ by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR-or DIOW-.

PIO Timing Parameters

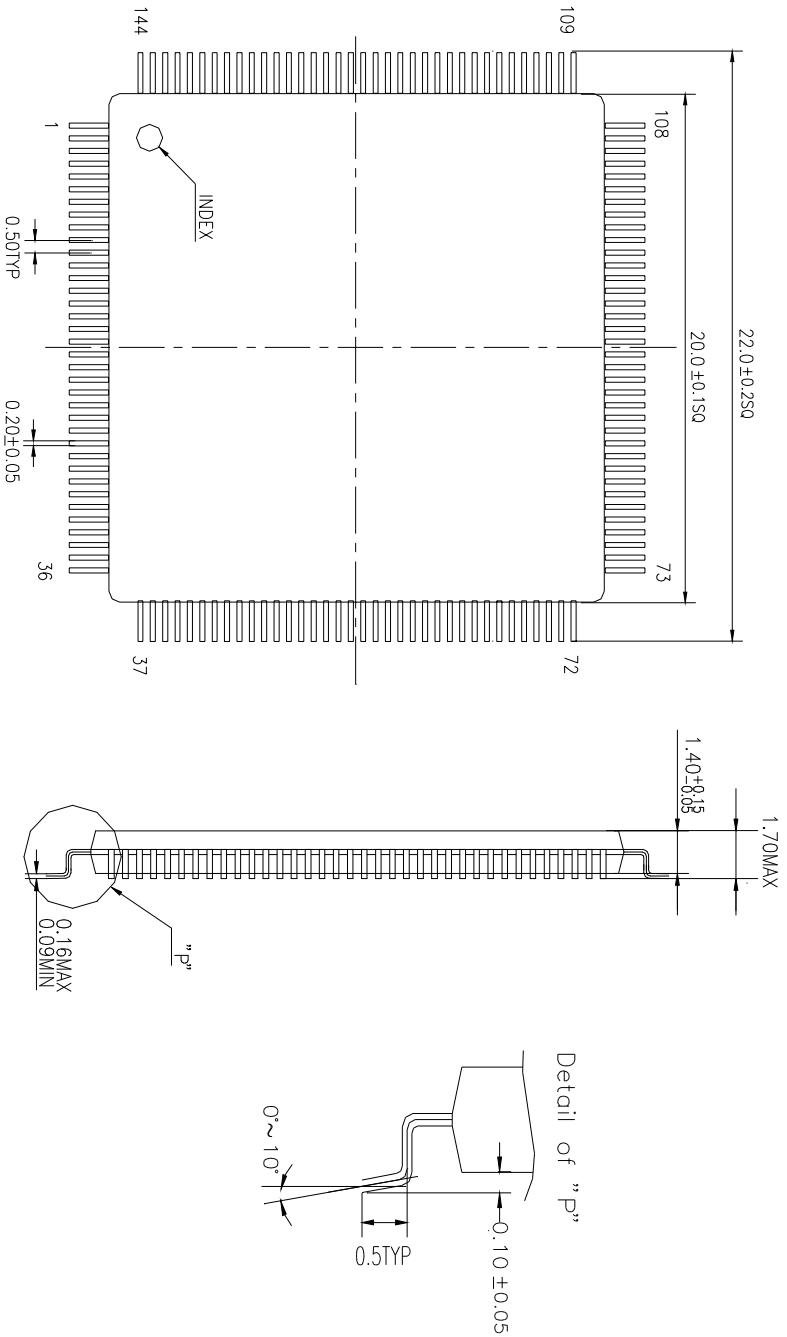
PIO	TIMING ARAMETERS	MODE0 ns	MODE1 ns	MODE2 ns	MODE3 ns	MODE4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1
t_1	Address valid to DIOR-/ DIOW- setup (min)	90	70	50	50	45	
t_2	DIOR-/DIOW- pulse width 8-bit (min)	290	290	290	80	70	1
t_{2i}	DIOR-/DIOW- recoveryfdsfe time (min)	-	-	-	70	25	1
t_3	DIOW- data setup (min)	60	45	30	30	20	
t_4	DIOW- data hold (min)	30	20	15	10	10	
t_5	DIOR- data setup (min)	50	35	20	20	20	
t_6	DIOR- data hold (min)	5	5	5	5	5	
t_{6z}	DIOR- data tristate (min)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active(if IORDY initially low after tA) (min)	0	0	0	0	0	
t_A	IORDY Setup time (min)	35	35	35	35	35	3
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release (max)	5	5	5	5	5	

Notes:
1. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements is greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device(tri-state).
3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sample. If IORDY is inactive then the host shall wait until IORDY is active fefore the PIO cycle is completed. If the device is not driving IORDY# negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY# negated at the time t_A after the activation of DIOR- or DIOW-, then tRD shall be met and t_5 is not applicable.

Appendix A
Mechanical Dimensions

This chapter contains the package drawing for the HPT366.
One configuration is available, a 144 Pins LQFP.

A.2 144 Pins LQFP

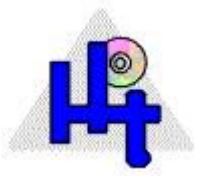


Appendix B
Diagrams

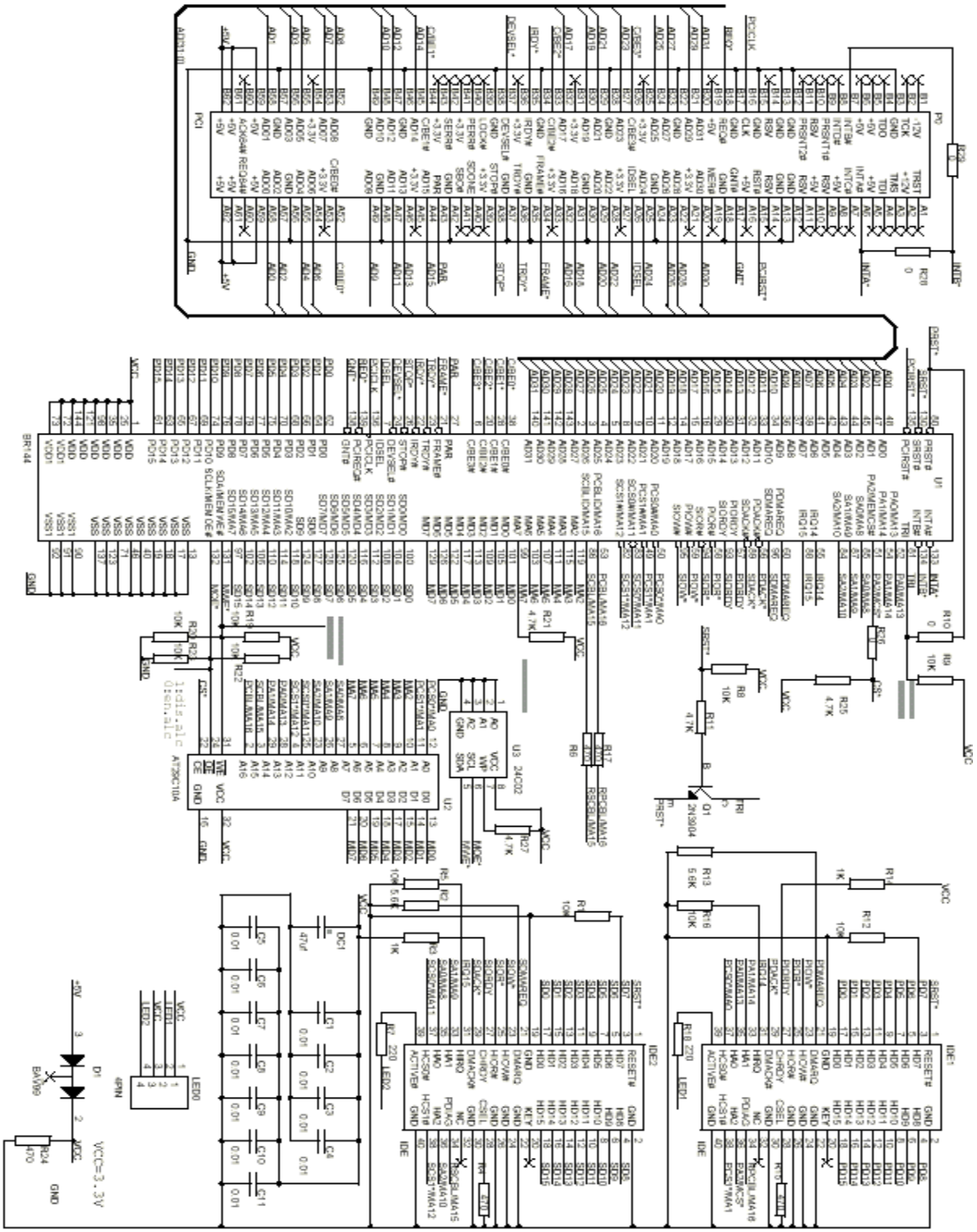
Introduction

This appendix contains the following items:

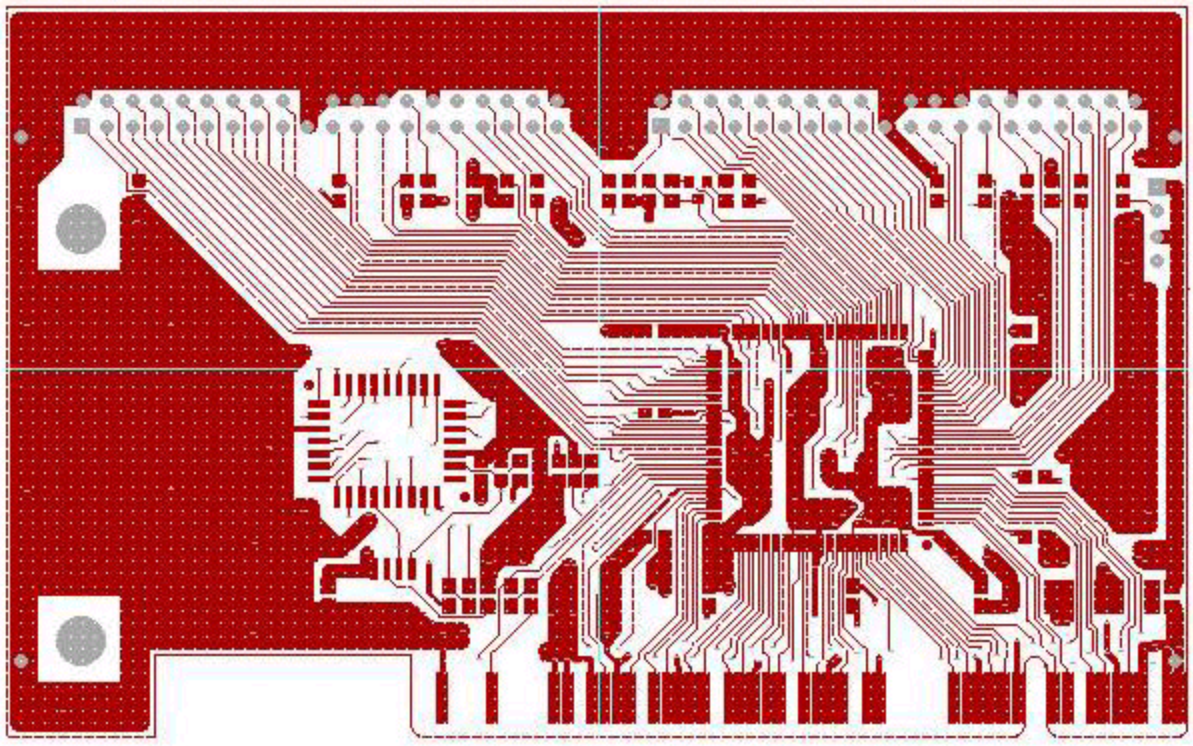
* Schematic Diagrams For Add-On Card;
* Layout For Add-On Card;
* Schematic Diagrams For Main Board.



B.1 Schematic Diagrams

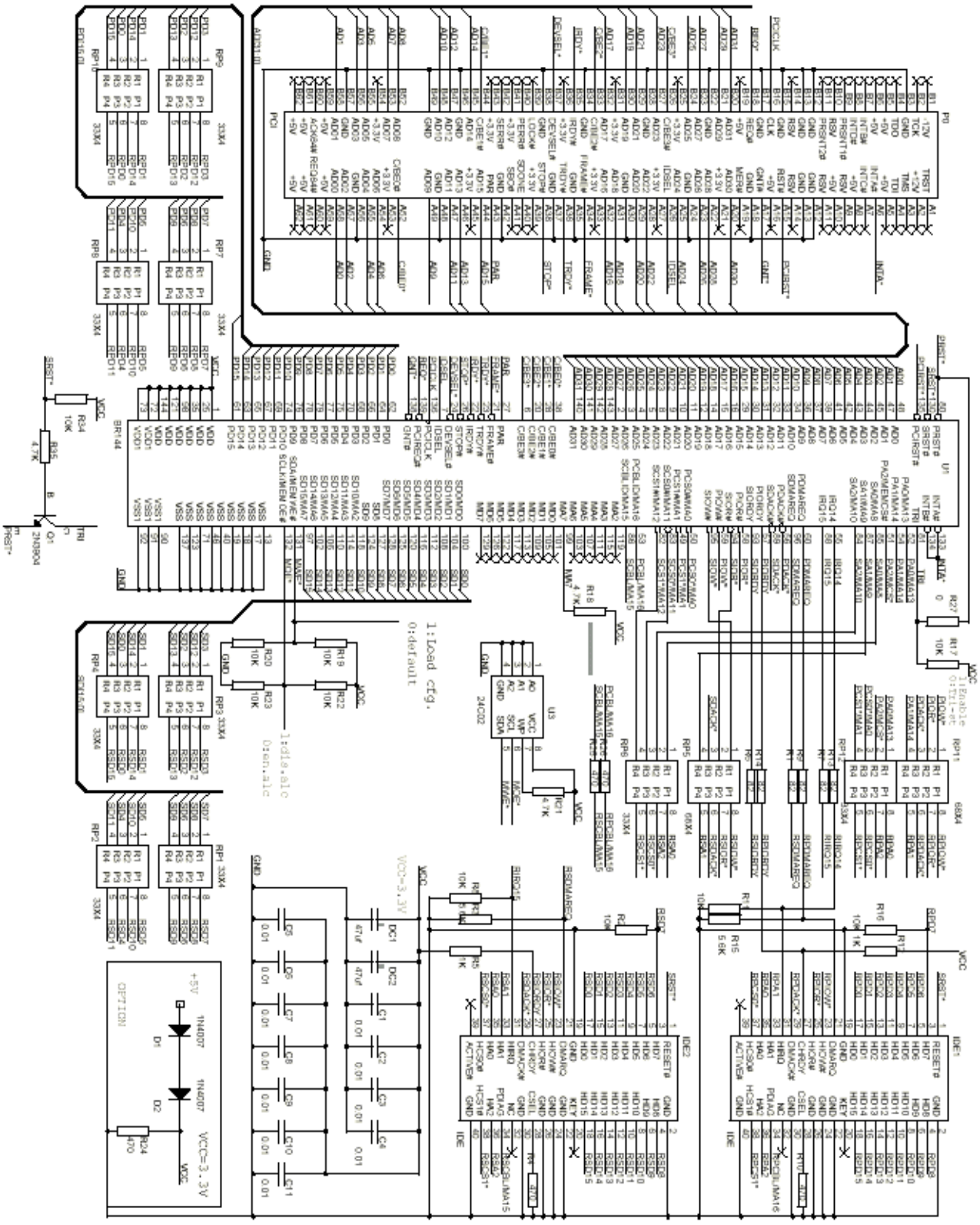


B.2 Layout



Top Layer

B.3 Schematic Diagrams For Main Board



Notes:
1. To minimize the number of PCI Interrupt Lines used this example uses only INTA_ (by connecting INTA_ and INTB_ together).
2. IDE address allocation mode is selected by using either R22 or R23 (When using R22 only, HPT366 will decode 1f0-1f7, 3f6 on PCI function 0, 170-177, 376 on PCI function 1; when using R23 only, HPT366 will decode operating system assigned addresses as specified by PCI IDE controller specification.).
3. Connecting TRI pin(Pin 81) to low will float the ATA Bus. This feature can be used for hotswap application.
4. HPT366's power supply is 3.3v. The option box on the lower right corner on the schematics may be used for system with 5v supply.