MAR.1984

HITACHI IC MEMORY DATA BOOK

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INDEX

NOTICE:

This data book includes all products in production on the data of issue. The data book may include products in a declining phase. It is advised that users contact HITACHI sales organization and check the availability of products if necessary.

■QUICK REFERENCE GUIDE TO HITACHI IC MEMORIES

■MOS RAM

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package† Pin No.	CG	G	P	FP	SP	Page
Static	4k-bit	HM6184H-35	CMOS	1024×4	35	35	+5	0.1m/0.25	18		●	●			46
		HM6148H-45			45	45					●	●			46
		HM6148H-55			55	55					●	●			46
		HM6148HL-35			35	35		5μ/0.25				●			50
		HM6148HL-45			45	45						●			50
		HM6148HL-55			55	55						●			50
		HM6147H-35		4096×1	35	35		0.1m/0.15			●	●			55
		HM6147H-45			45	45					●	●			55
		HM6147H-55			55	55					●	●			55
		HM6147HL-35			35	35		5μ/0.15				●			61
		HM6147HL-45			45	45						●			61
		HM6147HL-55			55	55						●			61
	16k-bit	HM6116-2		2048×8	120	120		0.1m/0.2	24	●	●	●	●		65
		HM6116-3			150	150		0.1m/0.18		●	●	●	●		65
		HM6116-4			200	200				●	●	●	●		65
		HM6116L-2			120	120		20μ△/0.18			●	●	●		80
		HM6116L-3			150	150		20μ△/0.16			●	●	●		80
		HM6116L-4			200	200					●	●	●		80
		HM6116A-12			120	120		0.1m/15m				●		●	98
		HM6116A-15			150	159						●		●	98
		HM6116A-20			200	200						●		●	98
		HM6116AL-12			120	120		5μ/10m				●		●	102
		HM6116AL-15			150	150						●		●	102
		HM6116AL-20			200	200						●		●	102
		HM6117-3			150	150		0.1m/0.2				●	●		106
		HM6117-4			200	200						●	●		106
		HM6117L-3			150	150		10μ/0.18				●	●		116
		HM6117L-4			200	200						●	●		116
		HM6168H-45		4096×4	45	45		0.1m/0.25	20		●	●			128
		HM6168H-55			55	55					●	●			128
		HM6168H-70			70	70					●	●			128
		HM6168HL-45			45	45		5μ/0.25				●			132
		HM6168HL-55			55	55						●			132
		HM6168HL-70			70	70						●			132
		HM6167		16384×1	70	70		0.1m/0.15	20		●	●			137
		HM6167-6			85	85					●	●			137
		HM6167-8			100	100					●	●			137
		HM6167L			70	70		5μ/0.15				●			143
		HM6167L-6			85	85						●			143
		HM6167L-8			100	100						●			143
		HM6167H-45			45	45		0.1m/0.2		●	●	●			147
		HM6167H-55			55	55				●	●	●			147
		HM6167HL-45			45	45		5μ/0.2				●			158
		HM6167HL-55			55	55						●			158
		HM6267-35**			35	35		0.1m/0.25				●			162
		HM6267-45**			45	45						●			162

(to be continued)

Mode	Total Bit	Type No.	Process	Organization (Word × bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package*						Page
									Pin No.	CG	G	P	FP	SP	
Static	64k-bit	HM6264-10	CMOS	8192×8	100	100	+5	0.1m/0.2	28			●			166
		HM6264-12			120	120						●	●		166
		HM6264-15			150	150						●	●		166
		HM6264L-10			100	100		10μ/0.2				●			176
		HM6264L-12			120	120						●	●		176
		HM6264L-15			150	150						●	●		176
		HM6287-55*		65536×1	55	55		0.1m/0.3	22	●		●			188
		HM6287-70*			70	70				●		●			188
		HM6287L-55*			55	55		10μ/0.3				●			189
		HM6287L-70*			70	70						●			189
Psude Static	256k-bit	HM65256-15*	CMOS	32768×8	150	150	+5	7m/0.3	28			●			190
		HM65256-20*			200	200						●			190
Dynamic	64k-bit	HM48416A-12	NMOS	16384×4	120	230	+5	20m/0.3	18			●			192
		HM48416A-15			150	260						●			192
		HM48416A-20			200	330						●			192
		HM4864-2		65536×1	150	270		20m/0.33	16		●	●			199
		HM4864-3			200	335					●	●			199
		HM4864A-12			120	220		20m/0.25		●	●	●			209
		HM4864A-15			150	260				●	●	●			209
		HM4864A-20			200	330				●	●	●			209
	256k-bit	HM50256-12		262144×1	120	220		20m/0.35			●	●			219
		HM50256-15			150	260					●	●			219
		HM50256-20			200	330					●	●			219
		HM50257-12			120	220		20m/0.35			●	●			226
		HM50257-15			150	260					●	●			226
		HM50257-20			200	330					●	●			226

• Under development •• Preliminary HM6116LP LFP Series : 10μW

† The package codes of CG, G, P, FP and SP are applied to the package materials as follows.
CG : Glass-sealed Caramic Leadless Chip Carrier, G : Cerdip, P : Plastic DIP,
FP : Flat Plastic Package (SOP), SP : Skinny Type Plastic DIP

■MOS ROM

Mode	Total Bit	Type No.	Process	Organization (Word × bit)	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package † Pin No.	C	G	P	FP	Page
Mask	64k-bit	HN61364	CMOS	8192×8	250	+5	5μ/50m	28			●	●	234
		HN61364H**			200						●		236
		HN61365			250			24			●		237
		HN61366			250						●		239
	128k-bit	HN613128		16384×8	250		5μ/50m	28			●	●	241
		HN613128H**			200						●		243
	256k-bit	HN61256		32768×8 or 65536×4	3500		5μ/7.5m				●	●	244
		HN613256		32768×8	250		5μ/50m				●	●	246
		HN613256H**			200						●		248
	1M-bit	HN62301**		131072×8	350		2m/75m				●		249
U. V. Erasablce & Electrically	32k-bit	HN482732A-20	NMOS	4096×8	200	+5	0.18/0.8	24		●			254
		HN482732A-25			250					●			254
		HN482732A-30			300					●			254
	64k-bit	HN482764		8192×8	250		0.18/0.55	28		●			258
		HN482764-2			200					●			258
		HN482764-3			300					●			258
		HN27C64-15	CMOS		150		0.55m 0.17			●			267
		HN27C64-20			200					●			267
		HN27C64-25			250					●			267
		HN27C64-30			300					●			267
	128k-bit	HN4827128-25	NMOS	16384×8	250		0.18 0.53			●			272
		HN4827128-30			300					●			272
		HN4827128-45			450					●			272
	256k-bit	HN27256-25**		32768×8	250		0.22 0.55			●			280
		HN27256-30**			300					●			280
One Time Electrically	64k-bit	HN482764-3	NMOS	8192×8	300	+5	0.18 0.55	28			●		263
	128k-bit	HN4827128-30**		16384×8	300		0.18 0.53				●		276
Electrically Erasable & Programmable	64k-bit	HN58064-25**	NMOS	8192×8	250	+5	0.22 0.55	28			●		284
		HN58064-30**			300						●		284
		HN58064-45**			450						●		284

• Under development ** Preliminary

† The packade codes of G, P and FP are applied to the packge material as follows.
G : Cerdip, P : Plastic DIP, FP : Plastic Flat Package

■BIPOLAR RAM

Level	Total Bit	Type No.	Organization (word×bit)	Output	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (mW/bit)	Package† Pin No.	F	G	CC	Replacement	Page
ECL 10K	256	HM10414	256×1	Open Emitter	10	−5.2	2.8	16		●		F10414	290
		HM10414-1			8					●			290
	1K	HM2110	1024×1		35		0.5			●		F10415	294
		HM2110-1			25					●		F10415A	294
		HM2112			10		0.8			●			298
		HM2112-1			8					●			298
		HM10422	256×4		10		0.8	24		●		F10422	303
		HM10422-7			7		1.0			●			308
	4K	HM10470	4096×1		25		0.2	18		●		F10470	311
		HM10470-1			15					●			311
		HM10470-20			20		0.25			●			316
		HM2142			10		0.3	20		●			319
		HM10474	1024×4		25		0.2	24		●		F10474	322
		HM10474-8**			8		0.3			●			327
		HM10474-10**			10					●			327
		HM10474-15			15		0.2			●			322
	16K	HM10480	16384×1		25		0.05	20	●	●		F10480	330
		HM10480-15**			15		0.06			●			333
		HM10480-20**			20					●			333
		HM10484-15*	4096×4		15		0.06	28		●			336
		HM10484-20*			20					●			336
ECL 100K	1K	HM100415	1024×1		10	−4.5	0.6	16		●	●	F100415	339
		HM100422	256×4		10		0.8	24	●	●	●	F100422	342
	4K	HM100470	4096×1		25		0.2	18		●		F100470	345
		HM100474	1024×4		25		0.2	24	●	●		F100474	348
		HM100474-15			15				●	●			348
	16K	HM100480	16384×1		25		0.05	20	●	●		F100480	353
		HM100480-15*			15		0.06			●			356
		HM100480-20*			20					●			356
		HM100484-15*	4096×4		15		0.06	28		●			359
		HM100484-20*			20					●			359
TTL	1K	HM2510	1024×1	Open Collector	70	+5	0.5	16		●			362
		HM2510-1			45					●		93415	362
		HM2510-2			35					●		93415A	362
		HM2511		3-state	70		0.5			●			366
		HM2511-1			45					●		93425	366

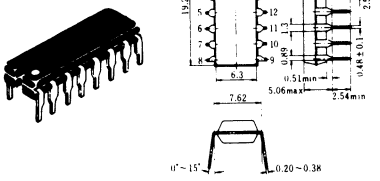
• Under development •• Preliminary

† The package codes of F,G and CC are applied to the packge materials as follows.
F : Flat Package, G : Cerdip, CC : Ceramic Leadless Chip Carrier

■ PACKAGE INFORMATION (Dimensions in mm)

● Dual-in-line Plastic

● DP-16



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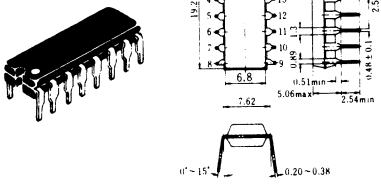

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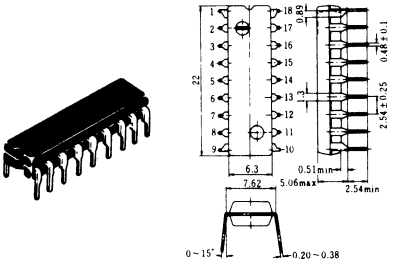

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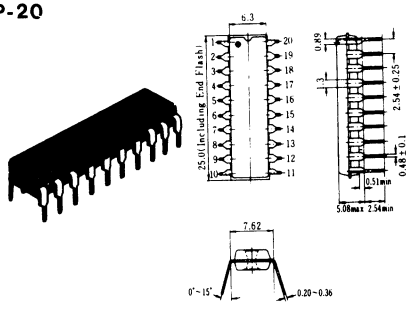

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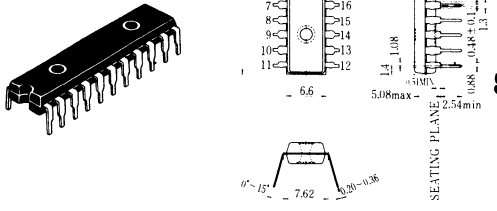

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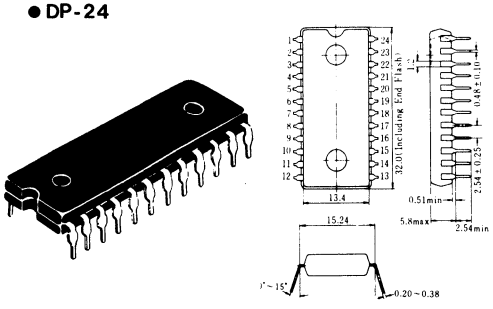

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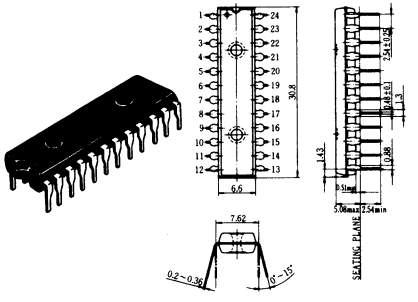

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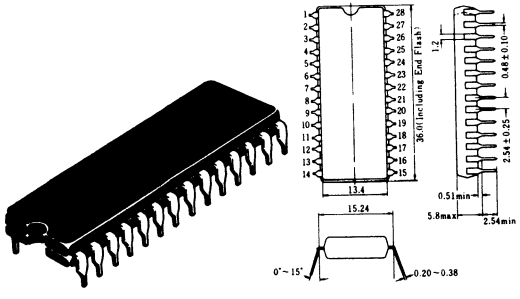
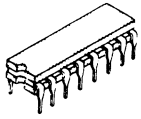


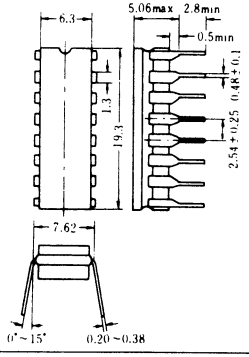
Applicable ICs

DP-16	HM4864P-2, HM4864P-3, HM4864AP-12, HM4864AP-15, HM4864AP-20
DP-16A	HM50256P-12, HM50256P-15, HM50256P-20, HM50257P-12, HM50257P-15, HM50257P-20
DP-18	HM6148HP-35, HM6148HP-45, HM6148HP-55, HM6148HLP-35, HM6148HLP-45, HM6148HLP-55, HM6147HP-35, HM6147HP-45,HM6147HP-55,HM6147HLP-35,HM6147HLP-45,HM6147HLP-55,HM48416AP-12,HM48416AP-15,HM48416AP-20
DP-20	HM6168HP-45, HM6168HP-55, HM6168HP-70, HM6168HLP-45, HM6168HLP-55, HM6168HLP-70, HM6167P, HM6167P-6, HM6167P-8, HM6167LP, HM6167LP-6, HM6167LP-8, HM6167HP-45, HM6167HP-55, HM6167HLP-45, HM6167HLP-55, HM6267P-35, HM6267P-45
DP-22A	HM6287P-55, HM6287P-70, HM6287LP-55, HM6287LP-70
DP-24	HM6116P-2, HM6116P-3, HM6116P-4, HM6116LP-2, HM6116LP-3, HM6116LP-4, HM6116AP-12, HM6116AP-15, HM6116AP-20, HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6117P-3, HM6117P-4, HM6117LP-3, HM6117LP-4, HN61365P, HN61366P
DP-24A	HM6116ASP-12, HM6116ASP-15, HM6116ASP-20, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20
DP-28	HM6264P-10, HM6264P-12, HM6264P-15, HM6264LP-10, HM6264LP-12, HM6264LP-15, HM65256P-15, HM65256P-20, HN61364P, HN61364HP, HN613128P, HN613128HP, HN61256P, HN613256P, HN613256HP, HN62301P, HN482764P-3, HN4827128P-30, HN58064P-25, HN58064P-30, HN58064P-45

● CERDIP

● DG-16





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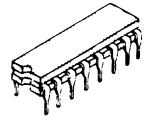

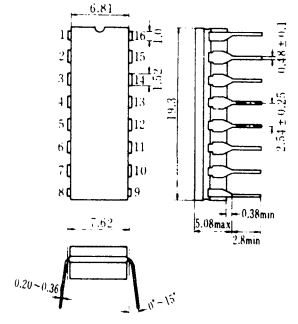

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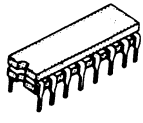

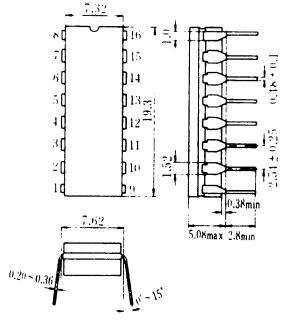

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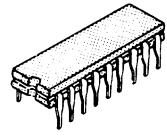

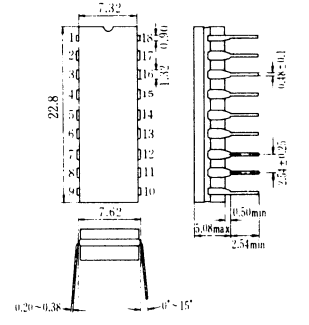

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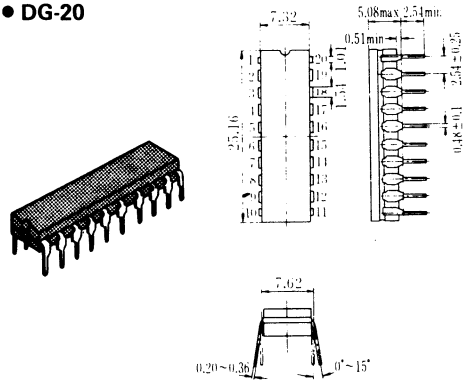

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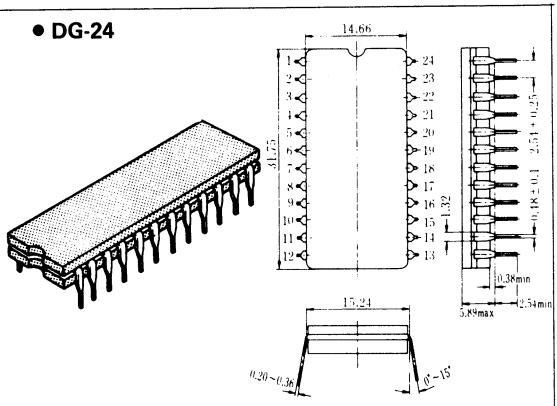

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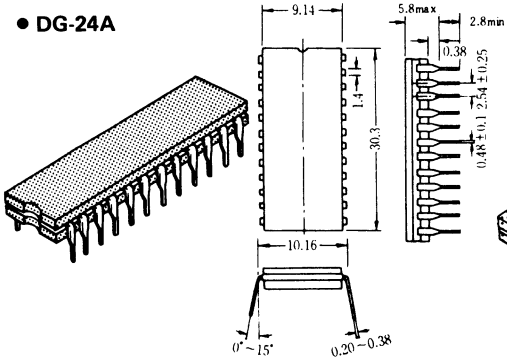
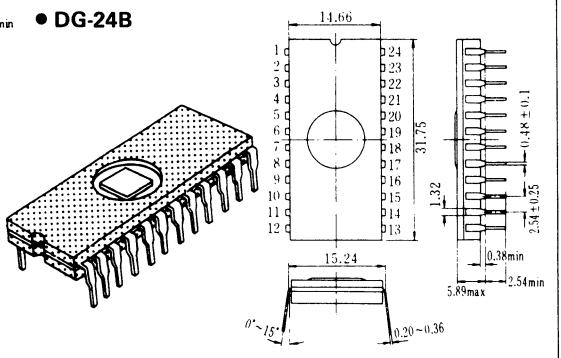
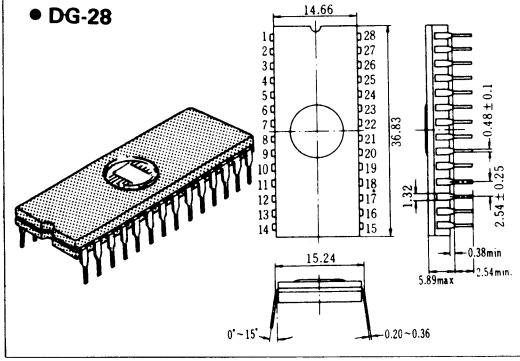


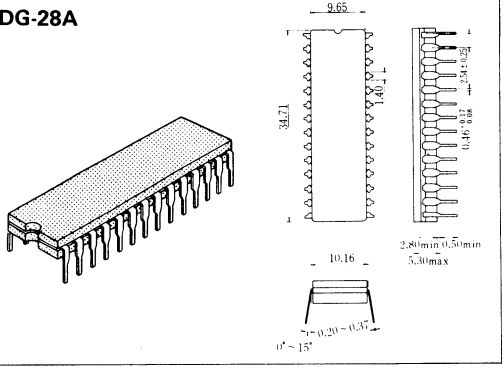
● DG-24B



● DG-28



● DG-28A

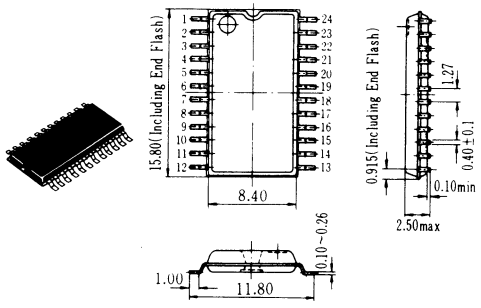


Applicable ICs

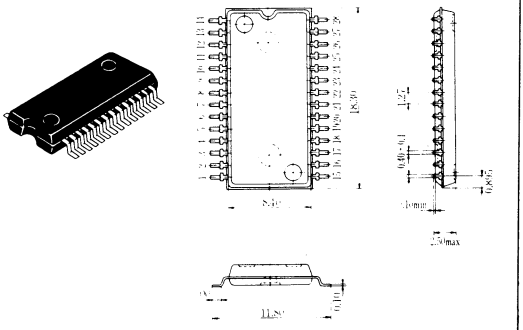
DG-16	HM10414, HM10414-1, HD2912
DG-16A	HM2110, HM2110-1, HM2112, HM2112-1, HM100415, HM2510, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-16B	HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20, HM50256-12, HM50256-15, HM50256-20, HM50257-12, HM50257-15, HM50257-20
DG-18	HM6148H-35, HM6148H-45, HM6148H-55, HM6147H-35, HM6147H-45, HM6147H-55, HM10470, HM10470-1, HM10470-15, HM100470
DG-20	HM6168H-45, HM6168H-55, HM6168H-70, HM6167, HM6167-6, HM6167-8, HM6167H-45, HM6167H-55, HM2142, HM10480, HM10480-15, HM10480-20, HM100480, HM100480-15, HM100480-20
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116-3, HM6116L-4
DG-24A	HM10422, HM10422-7, HM10474, HM10474-8, HM10474-10, HM10474-15, HM100422, HM100474, HM100474-15
DG-24B	HN482732AG-20, HN482732AG-25, HN482732AG-30
DG-28	HN482764G, HN482764G-2, HN482764G-3, HN27C64G-15, HN27C64G-20, HN27C64G-25, HN27C64G-30, HN482718G-25, HN4827128G-30, HN4827128G-45, HN27256G-25, HN27256G-30
DG-28A	HM10484-15, HM10484-20, HM100484-15, HM100484-20

● Flat Packages

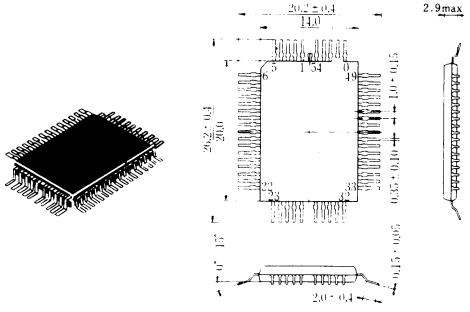
● FP-24



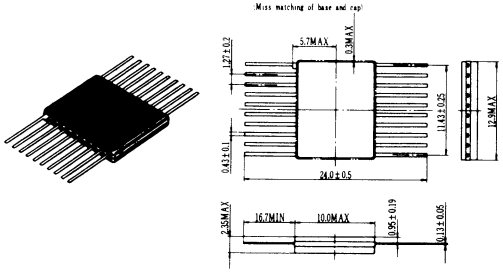
● FP-28



● FP-54



● FG-20



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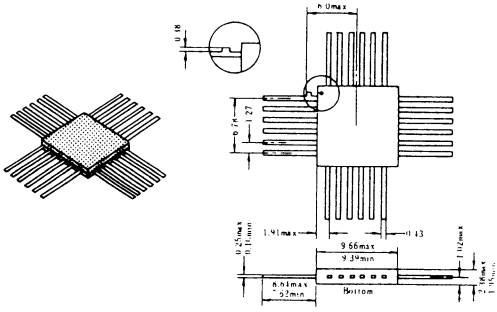
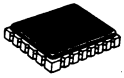


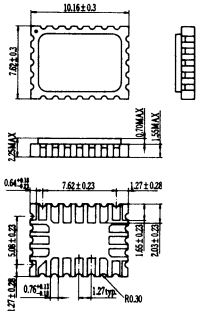
● Applicable ICs

FP-24	HM6116FP-2, HM6116FP-3, HM6116FP-4, HM6116LFP-2, HM6116LFP-3, HM6116LFP-4, HM6117FP-3, HM6117FP-4, HM6117LFP-3, HM6117LFP-4
FP-54	HN61364FP, HN613128FP, HN61256FP, HN613256FP
FG-20	HM10480F, HM100480F
FG-24	HM100422F, HM100474F, HM100474F-15

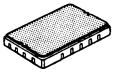
● Leadless Chip Carrier

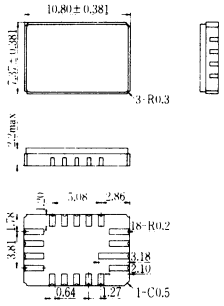
● CC-24



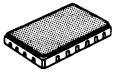


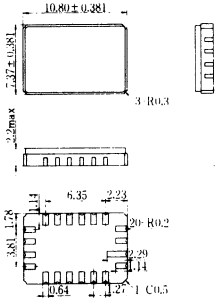
● CG-18



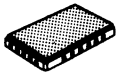


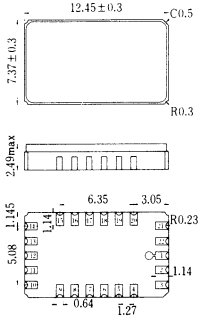
● CG-20



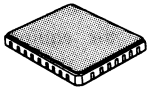


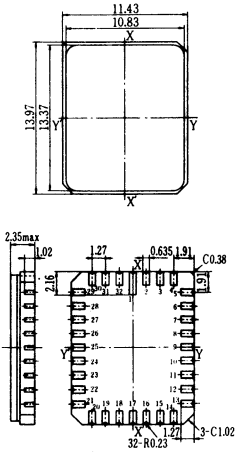
● CG-22





● CG-32





● Applicable ICs

CC-24	HM100415CC, HM100422CC
CG-18	HM4864ACG-12, HM4864ACG-15 HM4864ACG-20
CG-20	HM6167HCG-45, HM6167HCG-55
CG-22	HM6287CG-55, HM6287CG-70
CG-32	HM6116CG-2, HM6116CG-55 HM6116CG-4

■ RELIABILITY OF HITACHI IC MEMORIES

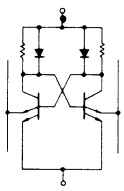
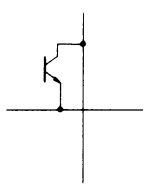
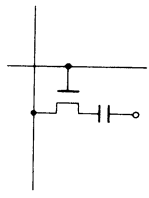
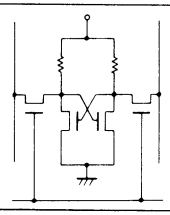
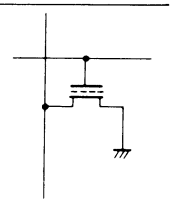
1. STRUCTURE

IC memories are structurally classified into bipolar type and MOS type. The former has a characteristic of an extremely high speed. But it is a comparatively small capacity and on the other hand, the latter features a large capacity. These IC memories are utilized by effectively taking the most of their respective characteristics.

Flows from designing, manufacturing and up to inspection for both Bipolar and MOS type IC memories are established under a unified concept, design and inspection standards. Therefore stable results concerning their reliability have been obtained with these IC memories, regardless of differences in the circuit design, pattern, layout, degree of integration, etc.

From its characteristics, the memory LSI is integrated in high density by unit patterns called "cell" and it is not exaggeration to say that they are produced in the most advanced semiconductor manufacturing technologies. To get the high reliability of such a memory which has been subjected to rapid technological advances, know-hows based on past experience from the design stage of a cell are incorporated. Farther to evaluated reliability of each respective technology applied. Reliability evaluation using TEG (Test Element Group), etc. is carried out. Examples of cell circuits of the Bipolar memory and MOS memory are shown in Table I.

● Table 1 Examples of Basic Cell Circuit of IC Memories

Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

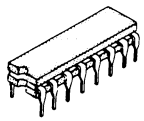
IC memory chips produced in the latest technologies are sealed in different packages. Ceramic package, Cerdip (glass-sealed type) and Plastic package are the current major IC packages. Also such packages as LCC (Leadless Chip Carrier) for high package density and SO (Small Outline) package are now under development.

Ceramic and Cerdip versions, with their hermetically sealed structure, are suitable to the equipment requiring high reliability. Plastic version, the leading semiconductor package, is applied to various kinds of equipment. Hitachi Plastic package has been improved to the close reliability level as the hermetically sealed devices. Table 2 shows examples of IC memory package outlines.

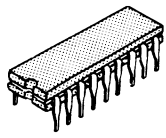
● Table 2 Examples of IC Memory Package Outlines

■ Cerdip

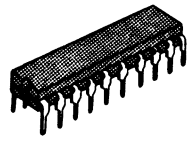
● 16 pin



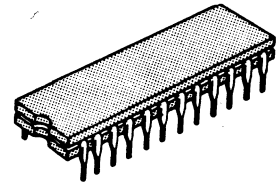
● 18 Pin



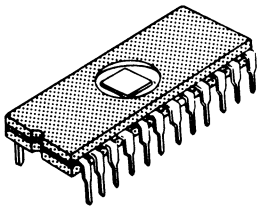
● 20 Pin



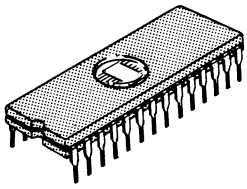
● 24 Pin



- 24 Pin with Lid

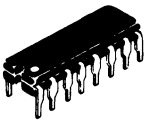


- 28 Pin with Lid

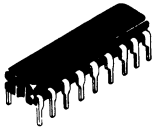


■ Plastic DIP

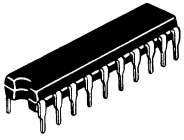
- 16 Pin



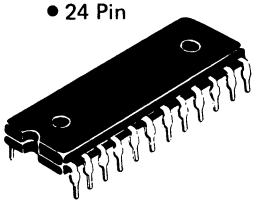
- 18 Pin



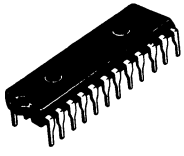
- 20 Pin



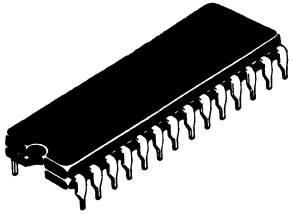
- 24 Pin



- 24 Pin



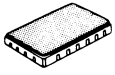
- 28 Pin



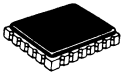
■ Leadless Chip Carrier

- 18 Pin

- 20 Pin



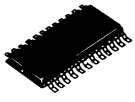
- 24 Pin



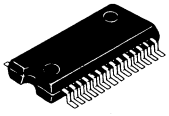
- 32 Pin

■ SOP

- 24 Pin



- 28 Pin



2. RELIABILITY DATA Results of reliability tests are listed below.

2-1 Reliability test data on Bipolar memories

The reliability test data on the Bipolar memories are shown in Tables 3 and 4. Since they are manufactured under the aforementioned standardized design rules and quality control, there is no difference in reliability among various types. In addition, it can be said that the greater the capacity, the higher the reliability per bit.

• Table 3 Results on Bipolar Memory Reliability Tests (1)

Test item	Test condition	HM10470 Cerdip				HM100422 (Chip Carrier)			
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*
High-temperature (Operating)	T_a = 125°C V_{EE} = −5.2V (HM10470)	125	C.H. 4.0×10^5	0	l/hr 2.3×10^{-6}	–	–	–	–
	T_a = 150°C V_{EE} = −5.2V (HM10470) V_{CC} = −5.0V (HM100422)	80	2.7×10^5	0	3.4×10^{-6}	40	4×10^4	0	2.3×10^{-5}
High-temperature storage	T_a = 200°C	27	2.7×10^4	0	3.4×10^{-5}	40	4×10^4	0	2.3×10^{-5}
	T_a = 295°C	20	2.0×10^4	0	4.6×10^{-5}	40	4×10^4	0	2.3×10^{-5}

* Estimated failure rate with confidence level 60%.

• Table 4 Result on Bipolar Memory Reliability Tests (2)

Test item	Test condition	HM10470 (Cerdip)		HM100422 (Chip carrier)	
		Samples	Failures	Samples	Failures
Temperature cycling	−65°C ~ +150°C, 10 cycles	120	0	40	0
Soldering heat	260°C, 10 seconds	22	0	–	–
Thermal shock	0°C ~ +100°C, 10 cycles	36	0	20	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	60	0
Variable frequency	100 ~ 2000Hz, 20G Three times each for X, Y and Z	40	0	60	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	60	0

2-2 Reliability test data on MOS memories

The reliability test data on the MOS memories are shown in Tables 5, 6 and 7. In these tables, data are shown on representative types of HM50256 (256K DRAM), HM4864AP (64K DRAM), HM6264P (64K SRAM), HM6116P/FP (16K SRAM), HN4827128 (128K EPROM) and leadless chip carrier device of 64K DRAM, 4K/16K SRAM.

• Table 5 Results on MOS Memory Reliability Test (1)

Test item	Test Condition	HM50256 (Ceramic)				HN4827128G (Cerdip)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature dynamic operation	T_a = 125°C V_{CC} = 5.5V t_{cyc} = 3μs	–	–	–	l/hr –	100	1.0×10^5	0	l/hr 9.2×10^{-6}	
	T_a = 150°C V_{CC}=8V/7V t_{cyc} = 3μs	723	1.44×10^6	7	5.8×10^{-6}	–	–	–	–	Oxide failure x 7
	T_a = 125°C V_{CC}=8V/7V t_{cyc} = 3μs	2920	1.12×10^6	2	2.8×10^{-6}	–	–	–	–	Oxide failure x 2

* Estimated failure rate with confidence level 60%.

● **Table 6 Results on MOS Memory Reliability Tests (2)**

Test item	Test condition	HM4864AP (Plastic)				HM6264P (Plastic)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
					1/hr				1/hr	
High-temperature dynamic operation	T_a = 150°C V_{CC} = 7V t_{cyc} = 3μs	173	1.73×10^5	0	1.3×10^{-6}	–	–	–	–	
	T_a = 125°C V_{CC} = 7V t_{cyc} = 3μs	173	1.73×10^5	0	1.3×10^{-6}	774	8.4×10^5	2	3.7×10^{-6}	Isolation failure×1 Defective crystal×1
High-temperature and high-humidity bias	T_a = 85°C RH = 85% V_{CC} = 5.5V	177	1.77×10^5	0	5.2×10^{-6}	304	3×10^5	0	3×10^{-6}	
Pressure cooker	T_a = 121°C RH = 85% storage	22	1.1×10^4	0	8.4×10^{-5}	55	2.2×10^4	0	4.2×10^{-5}	

* Estimated failure rate with confidence level 60%.

● **Table 7 Results on MOS Memory Reliability Tests (3)**

Test item	Test condition	HM50256 (cerdip)		EPROM (Cerdip)		HM6116P		HM6116FP		LCC		Remarks
		Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	-55°C~+150°C 10 cycles	386	0	775	0	5462	0	1838	0	860	0	
Temperature cycling	-55°C~+150°C 1000 cycles	116	0	250	0	100	0	90	0*	445	0	*500 cycles
Thermal shock	-65°C~+150°C 15 cycles	145	0	146	0	38	0	38	0	498	0	
Soldering heat	260°C 10 seconds	50	0	90	0	22	0	297	0	82	0	
Mechanical shock	1500G 0.5ms	38	0	90	0	–	–	–	–	82	0	
Variable frequency	20Hz~2000Hz 20G	38	0	90	0	–	–	–	–	82	0	
Constant-acceleration	20,000G	38	0	90	0*	–	–	–	–	82	0	*6000G

2.3 Change of electrical characteristics under endurance test for IC memories

The degradation of I_{CBO} of the cell transistor, degradation of h_{FE}, etc., can be considered as main factors in the internal elements for reliability of Bipolar memories. In actual element designing, however, it has been designed to operate in the range at which these degradations do not happen. Therefore changes of electrical characteristics including access time are not observed.

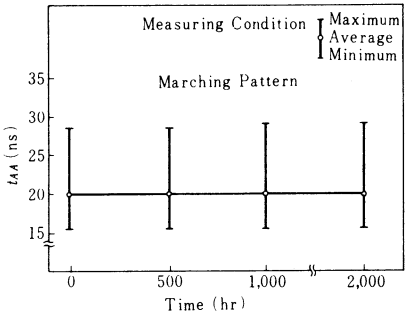
Time dependence in access time for HM10470 is shown in Fig. 1.

Fig. 1 Example of Change in Bipolar Memory Characteristics

Example	
Device name	HM10470
Test condition	Ta=125°C, V_{EE}=-5.2V
Failure criteria	t_{AA}=25ns
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Example of time change in access time for Bipolar memory



V_{TH} is a basic parameter in the MOS memories, however, it has been confirmed there is not any shift in V_{TH} for practical usage because we have applied surface stabilizing technique, clean process, etc.

In case of dynamic RAM which needs refresh cycle, refresh time is also stabilized owing to the above-mentioned process. Time dependence of Vcc min and t_{REF} characteristics for the 64K DRAM are shown in Fig. 2 and 3.

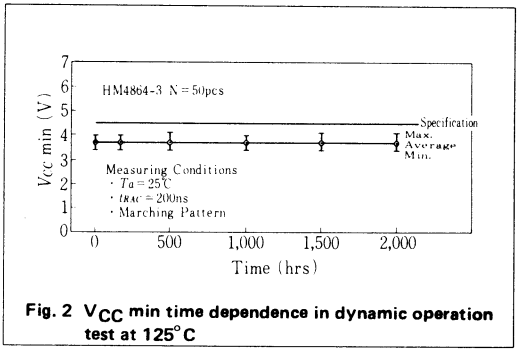


Fig. 2 V_{CC} min time dependence in dynamic operation test at 125°C

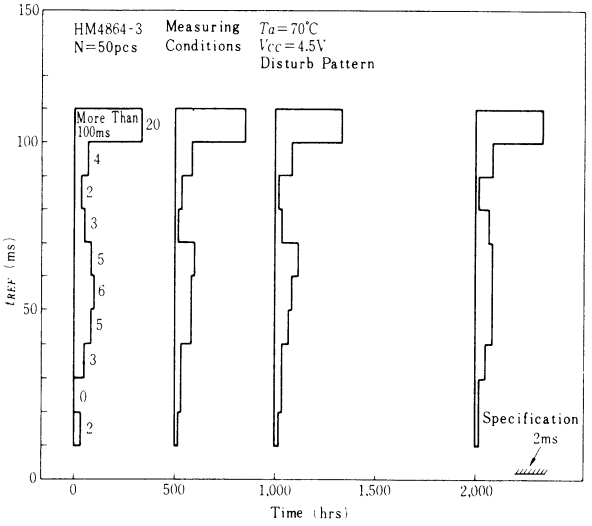


Fig. 3 Time dependence in refresh time (t_{REF}) in dynamic operation test at 125°C

2.4 Classification of failure modes

Examples of failures happened in the field are shown in Fig. 4 and 5. Since memory LSIs generally require the most fine processing in semiconductor manufacturing technology, the percentage of failures resulting from pinholes, photoresist defects, foreign materials, etc., is tending to increase. To eliminate the latent defects which are generated in these manufacturing processes, we are constantly improving these processes, and performing burn-in screening under high temperature for all memories. In addition, since the analysis of failures in the field can result in important feedback to improve their design and manufacturing, we are always exerting our efforts to collect customer process data and field data with the aim of further establishing their high reliability.

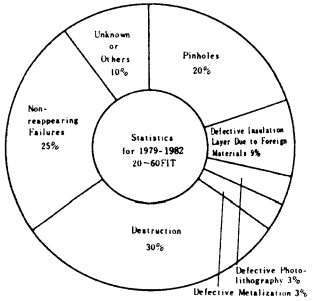


Fig. 4 Classification of Failure Modes of Bipolar Memory in the field

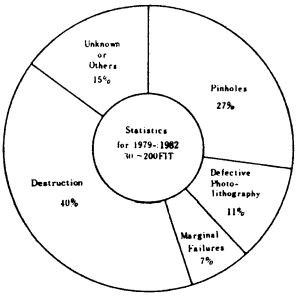
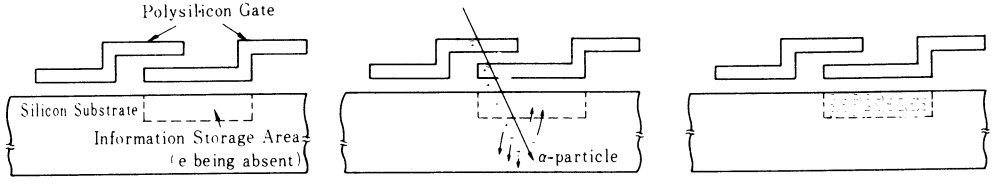


Fig. 5 Classification of Failure Modes of MOS Memory in the field

3. SOFT ERROR

3.1 Soft Error Mechanism

As mentioned before, IC memories have been increasingly miniaturized. Miniaturization, which means reduction of the horizontal plane dimensions as well as the vertical dimensions, causes signal level on the chip and storage charge of dynamic memories to be also decreased. An obstacle lying before miniaturization is soft error. Soft errors can be characterized as "transitory failures in which normal memory operation can be recovered by reprogramming information." Soft errors are caused by α-particles emitted from U and T_H contained in the packaging materials. As memory chips are exposed to α-particles, a great deal of electron-hole pairs are induced in Si substrate. These induced electrons cause memory information reversion. Fig. 6 shows the mechanism of information reversion in NMOS dynamic memory by α-particles. In case of NMOS dynamic memory, negative voltage is applied to the Si substrate. Therefore, positive holes are drawn by substrate, and only electrons cause information reversion (from information "1" to "0") of memory cell. Fig. 6 shows misoperation seen in memory cell. Such a failure mode, which is defined as "Memory cell mode of soft errors," is distinguished from "Bit line mode." "Bit line mode" of soft errors is shown in Fig. 7. As information in memory cell is read out on bit line, bit line potential changes depending on memory cell information. The changing value is very small (several 100 mV), and compared with standard potential (potential read out from dummy cell), it is amplified by sense amplifier. If bit line is exposed to α-particles during the very short period between read-out from memory cell and amplification by sense amplifier, bit line potential decreases. And as it becomes less than standard potential, misoperation from information "0" to "1" will take place. On the other hand, with decrease of standard potential, misoperation from information "1" to "0" is seen. Both are called "Bit line mode" because errors appear at irradiation of α-particles. Soft error dependence on cycle time is shown in Fig. 8.

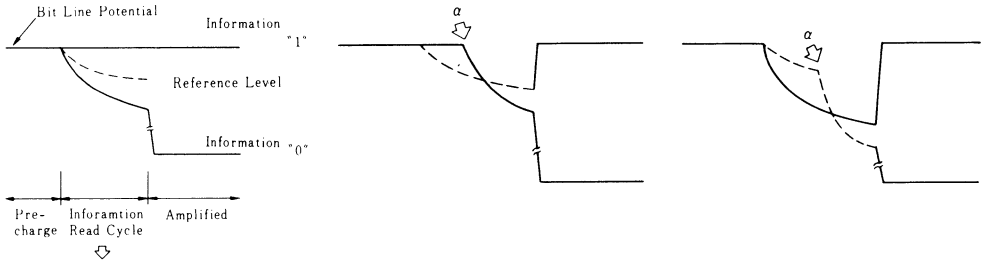


(a) Memory information at "1" (Electrons are absent) (1 Transistor type memory cell)

(b) Incident α-particle generate a large quantity of electron-hole pairs. Generated electrons enter the information storage area and holes are drawn to the substrate power supply.

(c) Inversion of memory information from "1" (electrons "absent") to "0" (electrons "filled")

Fig. 6 Misoperation in Memory Cell



(a) Read out memory information into bit line

(b) Inversion of information from "1" to "0" (fall of "1" potential)

(c) Inversion of information from "0" to "1" (fall of standard potential)

Fig. 7 Misoperation on Bit Line

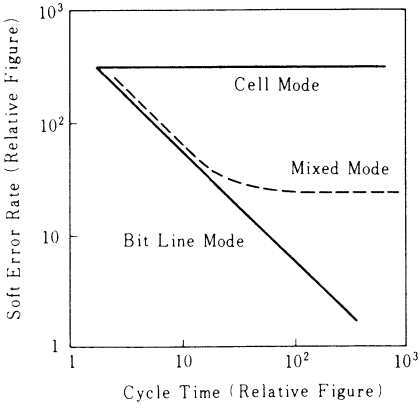


Fig. 8 Soft Error Rate's Dependence on Cycle Time

Actual products will have three types of failure modes, that is, cell mode, bit line mode and mixture of both modes. Soft error mechanism of static MOS memories and of bipolar memories are different from the above-mentioned mechanism in dynamic MOS memories.

In case of static memory, certain level of current always flows through the cell in order to retain the data in flip-flop circuit. When partial current induced by α-particles exceeds the retention current, misoperation occurs because of reversion of flip-flop circuit.

3.2 Examples of soft error preventive measures in products

At the initial stage of the 64K DRAM development, its soft error rate was estimated from accelerated irradiation test data to be higher than the expected design value. Hitachi has performed the following soft error preventive measures.

1) Selection of packaging materials which emit a minimal number of α-particles.
2) Application of chip coating technology to prevent the α-particles.
3) Use of circuitry and layout technology with inherent ability to resist α-particles.

Owing to these corrective measures, soft errors in 64K DRAM have reached a practically acceptable level. Preventive measures applied for 64K DRAM are also applied to other types. 16K DRAM with single power supply 5V family, for which chip coating was originally used, no longer requires this coating because of remarkable improvement by the third measure.

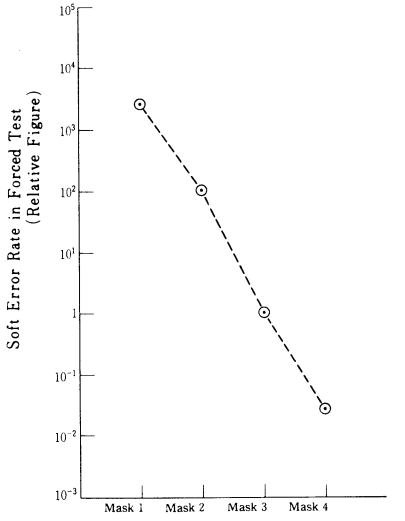


Fig. 9 Example of Soft Error Improvement on 64K-bit Dynamic RAM

3.3 Request for soft error preventative measures in system equipment

Thus our efforts to reduce soft errors have resulted in almost trouble-free memories. System reliability can be more improved by supplying some functions, that is, ECC device for lage memory system and parity bit for small one.

4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability by their application and controls the flows of design, production and test. Reliability can be roughly classified as follows:

(I) For large scale computers and electronic exchangers

(II) For important parts for auto-motive application

(III) General communication-industrial use

In using our products, therefore, we would like you to consider the classification of the application. Especially, when you are going to apply our memories to any special equipment, please do not hesitate to consult our sales engineering staff.

■ PRECAUTIONS FOR HANDLING IC MEMORIES

A variety of IC memories of high-spped, high-power and static lower power dissipation CMOS have been developed and commercially available, which allows an electronics designer to properly select the one best suited for a particular application. However, he must be familiar with the advantages and disadvantages of the devices to make the optimum selection and to prevent them from malfunctioning or, in the worst case, from breaking down. Precautions for handling IC memories given below will help the electronics designers to work out their optimum circuit designs.

1. BIPOLAR IC MEMORY

1.1 Prevention of static electricity

Bipolar memories have been considered to have high resistance to the static electricity than MOS ICs. However, the presently available high speed IC, represented by bipolar memories, must be provided with a suitable preventive measure against the static electricity. Because their diffused junctions have become thinner than the conventional types, in order to perform higher capability. Take note of the following points.

(1) Keep all terminals of a device in the conductive mat during transportation and storage to keep them at the same potential. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specially stated, all HITACHI IC memories will be shipped in our conductive mats. Store them as they are.

(2) When handling by hand IC memories for inspection or connection, his finger must be grounded as shown in Fig. 1. Do not forget to insert a 1M ohm resistor to protect him against an electric shock.

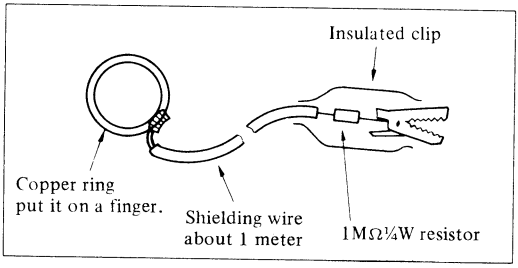


Fig. 1

(3) It is advisable to control the ambient relative humidity at about 50 per cent to prevent the occurrence of static electricity.

(4) It is also recommendable to wear cotton clothes instead of the ones made of synthetic fabrics to prevent the static electricity from occurring.

(5) It is desirable to ground the soldering iron tips. Use a low voltage soldering iron (12 or 24V), if possible.

(6) When IC memories mounted on the circuit boards are shipped, it is preferable to pack them with conductive mats.

1.2 Prevention of Reverse Insertion of IC Pinouts

In the case of reverse insertion of IC pinouts to board, ICs which have symmetrical pinouts between V_{EE} and Ground causes high current flown. Interconnection on the chip is melted and device is destroyed. Precaution must be made even for the ICs which do not have symmetrical pinouts between V_{EE} and Ground, because excess current flows and sometimes device is destroyed. On the device package, marking of No. 1 pin is stamped. Please watch this marking and insert ICs properly.

1.3 Mounting and Removal of ICs during Voltage is supplied

Usually, rather high current flows in regulator of bipolar memory. Therefore, if ICs are put in and pulled out to board during voltage is supplied, high voltage induced at current on/off destroys ICs. Mount and remove ICs after supply voltage is cut off. Same precaution must be made in measurement with tester.

1.4 Prevention of Oscillation

ECL bipolar memory has high cut-off frequency of transistor. Therefore, sometimes, oscillation is caused in relation with external circuit, and misoperation of ICs is occurred. In such cases, about 0.1 μF of capacitor, which has good high frequency characteristics, is recommended to put between ICs and voltage supply line.

1.5 Precaution on Simple "H" Level of ECL Memory

In some cases, it is seen that input of ICs is directly connected to ground to fix input as "H" level. However, it sometimes causes misoperation in conjunction with internal circuit composition. "H" and "L" level of input are specified as $V_{IL(min)}$ and $V_{IH(max)}$ for ICs respectively. Please refer them and use ICs properly.

1.6 Cooling

Power dissipation of bipolar memory is 400mW to 1000mW depending on products. In the case many bipolar memories are mounted on the board, natural convention is insufficient for cooling. Therefore, please run forced air cooling with velocity higher

than 2.5m/s. In addition, by cooling, improvement of reliability can be expected as shown in Fig. 2. We recommend the junction temperature to be kept less than 85°C for high reliability use.

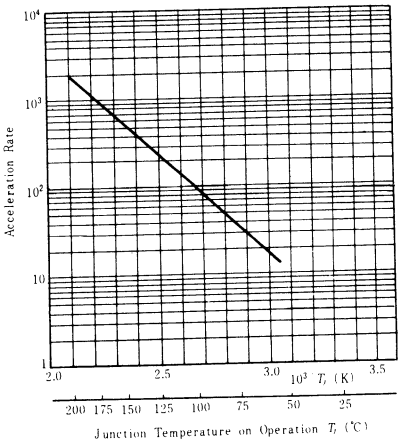


Fig. 2 Example of derating of ECL

1.7 Other Precautions

(1) Deforming of magazine and carrier
Since material of plastic magazine and carrier (for ECL flat package) is usually thermal plasticity, they deforms at temperature higher than 40 to 50°C and may not perform sufficiently. If burn-in is carried out at users, please use aluminum magazine or other metal fixtures.

(2) Shock at transportation
Glass sealed type package is fragile. Usual handling and drop test (JIS C7021 A-8) on individual devices do not cause any problem. However, it devices packed in magazine receive strong shock such as drop shock, devices hit neighbouring devices and packages may be damaged. Therefore, at transportation or loading on/off, be careful not to drop them. Even after devices are mounted on board, IC packages may be damaged if strength of board is not enough and board receives strong deforming stress. Please be careful on strength of board and handling. If any questions rose at using Hitachi products, please feel free to contact closest Hitachi representatives or offices.

2. MOS IC MEMORY

2.1 Prevention of static electricity

Similar to bipolar IC memories, suitable preventive measures should be taken for MOS IC memories by referring to paragraph 1.1.

2.2 Absorption of power source noise

The source current level flowing in the dynamic memory during the time of access is considerably different from that of stand by. Although the current difference is quite effective to save the power consumption, the current spike may be developed into the power source noise. Since all MOS IC memories are, in general, accessed while being refreshed, it is recommended to insert large capacitors (a 10 μF capacitor for every 9 pieces of 64K-bit HM4864P, for example) as well as a 0.1 μF capacitor having good high-frequency characteristics for each memory. Needless to say, it is very important to reduce the power circuit impedance when designing.

2.3 Assessment of the memory system design

It is quite effective to obtain the power margin curves (shmoo curve) for evaluating the memory system designs (timing margin or adaptability to the peripheral circuits). Investigate the V_{DD} and access time behaviors by gradually varying theri levels, and the ones which are closer to the margine shown by the memory device itself can be judged to be better than others.

2.4 Overhead parity bit

Application of MOS IC static memory especially to microcomputers has been rapidly increasing due to the advantages that MOS static memory is operated by a single 5V power source and refreshing is not required.
There are some cases where all bits are used as the information bit without inclusion of any parity bit by some circuit designing reasons. It is, however, desirable to add parity bits to thoroughly avoid the memory error.

2.5 Use under high electric field

In case MOS IC memories are placed near to high voltage source, the high electric field may cause failures in system operation.
In order to avoid the problem, it is advisable to shield the parts or keep them away enough from the high voltage source.

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual users' purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality reuired by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize the quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality. In addition, quality required by users on semiconductor devices are going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.
(2) Build the quality at the sources of manufacturing process.
(3) Execute harder the inspection and reliability confirmation of final products.
(4) Make quality level higher with field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as wel as performance and price.

It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (include process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishement of design rule, and standerdization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing

2 Effectiveness of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competition power of products, the major purpose of design review is to insure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even

for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.
(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub program of calculation, experiments, investigation, etc. will be carried out.
(3) Determine contents of reliability and methods, etc. based on design document and drawing.
(4) Check process ability of manufacturing line to achieve design goal.
(5) Discussion about preparation for production.
(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
(7) Reference of past failure experiences with similar devices, confirmation of method to provent them, and planning and execution of test program for confirmation of them. These study and decision are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
(2) Feedback of information should be made to insure satisfied level of process ability.
(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To insure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

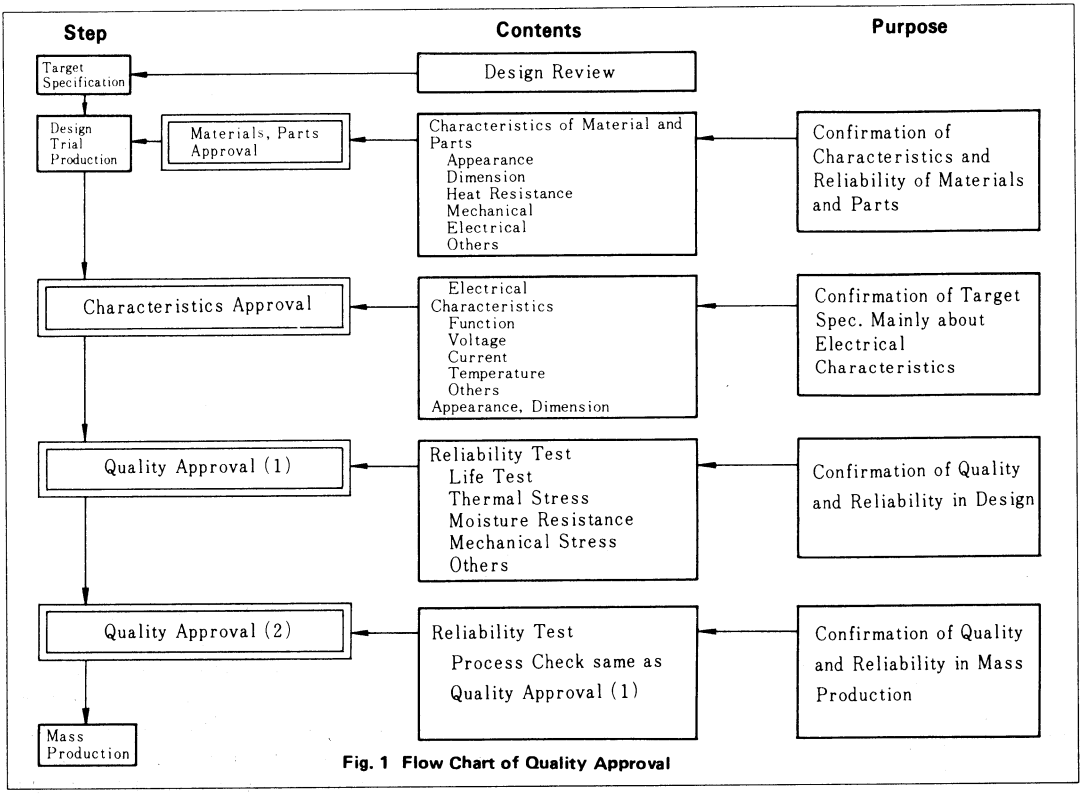


Fig. 1 Flow Chart of Quality Approval

(1) The third party executes approval objectively from the stand point of customers.
(2) Fully consider past failure experiences and information from field.
(3) Approval is needed for design change and work change.
(4) Intensive approval is executed on parts material and process.
(5) Study process ability and fluctuation factor, and set up control points at mass production.

Considering the views mentioned above, quality approval shown in Fig. 1 is executed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

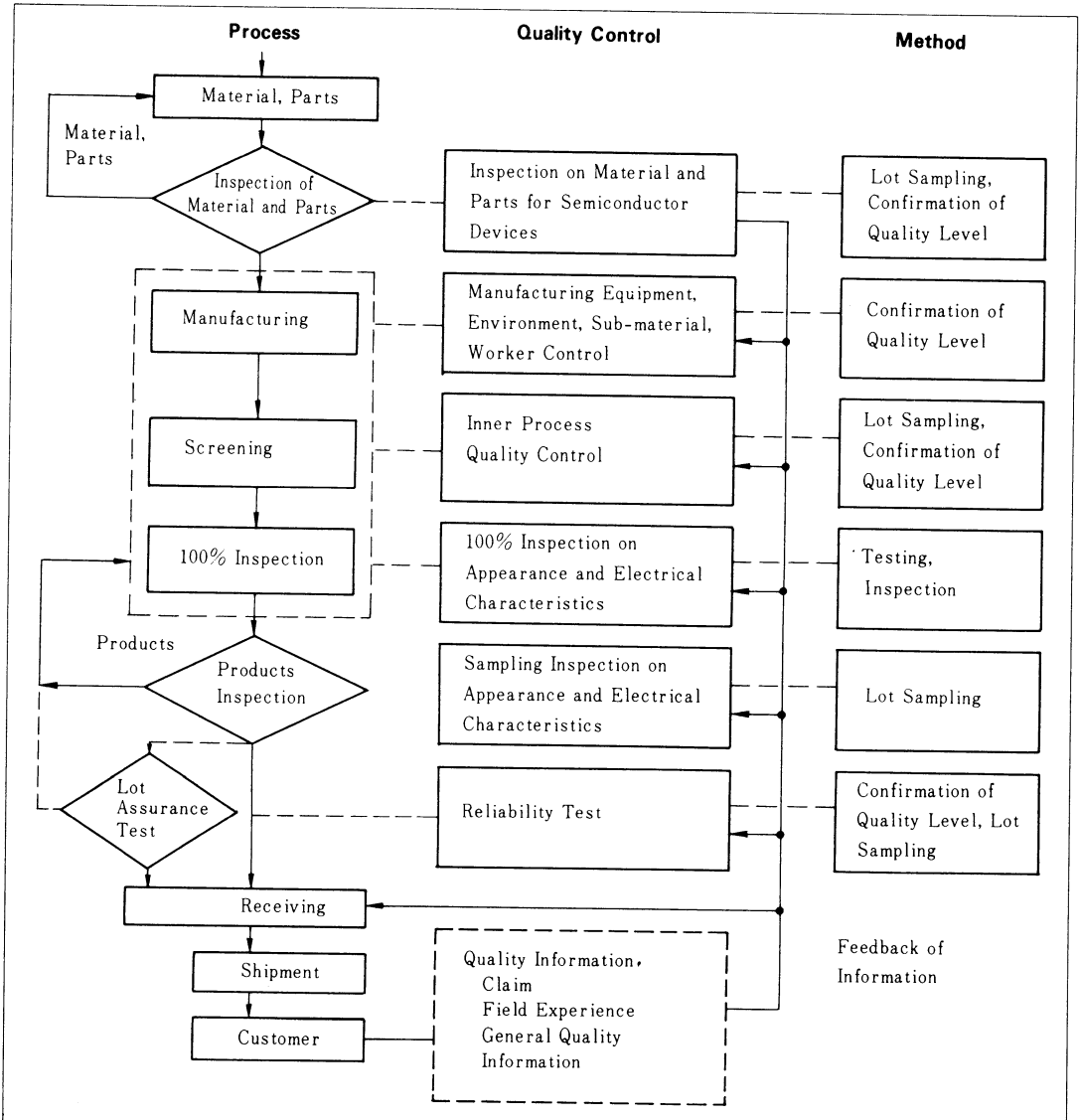


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Material

As tendency toward higher performance and higher reliability of semiconductor devices, is going, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows;

(1) Outside Vendor Technical Information Meeting
(2) Approval on outside vendors, and guidance of outside vendors
(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

• Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub materials. The manufacturing inner process quality control is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and tighter inner process quality control is executed – rigid check in each process and each lot, 100% inspection pointed process to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semi-final products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transfer of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipments are extraordinary developing as higher performance devices are needed and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain prompt operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are

checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances — temperature, humidity, dust — and the control of submaterials — gas, pure water — used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

Process	Control Point		Purpose of Control
▽ Purchase of Material			
Wafer	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
○ Surface Oxidation	Oxidation		Assurance of Resistance
□ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○ Photo Resist	Photo Resist		
□ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇ PQC Level Check			Check of Photo Resist
○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
□ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH}
◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	Breakdown Voltage Check
○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
□ Inspection on Evaporation			
◇ PQC Level Check			
□ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
□ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○ Chip Scribe		Appearance of Chip	
□ Inspection on Chip Appearance			
◇ PQC Lot Judgement			
Frame			
○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
□ Inspection after Assembling		Appearance after Assembling	
◇ PQC Lot Judgement			
Package			
○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇ PQC Level Check	Marking	Marking Strength	
○ Final Electrical Inspection			
◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
□ Appearance Inspection			
△ Sampling Inspection on Products			
○ Receiving			
Shipment			

Fig. 3 Example of Inner Process Quality Control

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

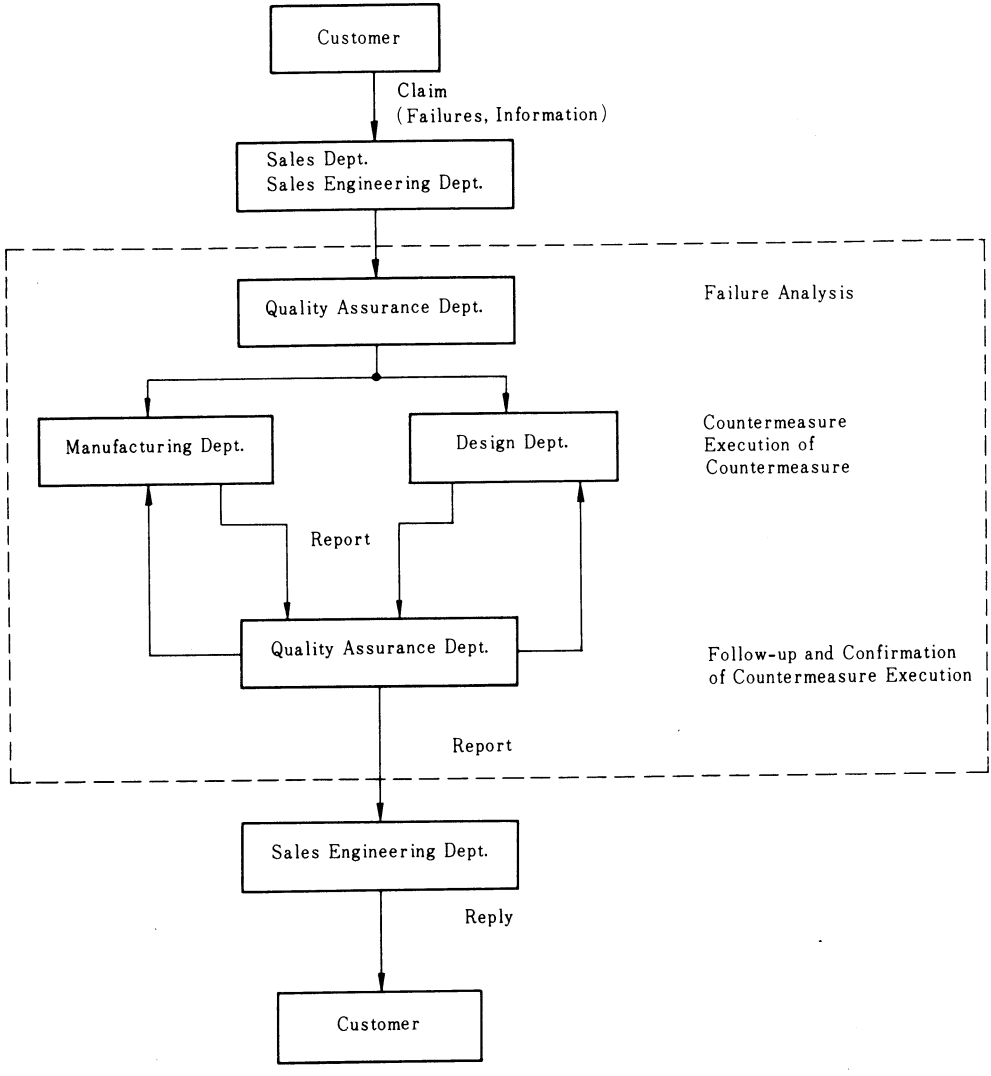


Fig. 4 Process Flow Chart of Field Failure

1. Inspection Method

Compared to conventional core memories, all peripheral circuits such as the decoder circuit, write circuit, read circuit, etc., are contained within the IC memories. As a result, all works of assembling the parts and performing electrical inspection, which had been carried out by core memory manufacturers in the past, have be come to be incorporated as works of IC manufacturers. Consequently, the electrical inspection of the memory IC has been faced to a more systematic inspection method and conventional IC inspection facilities have become completely useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a comparatively simple DC parameter facility. However, when the address input becomes multiplexed as in 16K memory, even the generation of the function test pattern becomes a serious problem. In the memory IC inspection, its quality cannot be judged by only inspecting DC characteristics related to external pins. This is because numbers of transistors, etc., related to the DC characteristics of the pins only amount to 1/1000 of all element numbers within IC memories. The following various address patterns are proposed to inspect whether or not the internal circuits are functioning correctly.

(1) All "Low", all "High"
(2) Checker flag
(3) Stripe pattern
(4) Marching
(5) Galloping
(6) Walking
(7) Ping-pong

Although there are a lot of address patterns, only representative ones have been listed. These patterns are convenient for checking the mutual finterference of bits and sometimes are patterns with maximum power dissipation. Among the abovementioned patterns, those of (1) to (4) are the socalled N patterns and these patterns are capable of checking IC memories of N bits with several sequences of N at most against the memory IC of N bits. Whereas, those of (5) to (7) are caled N^2 patterns and they need patterns several sequences of N^2

A serious problem arises in using the N^2 patterns in a large-capacity memory, for example, a long period of about 30 minutes becomes necessary to perform inspection of the 16K memory with galloping pattern. Patterns from (1) (3) are comparatively simple and good methods, but they are not perfect against a failure in the decoder circuit. As the most simple pattern for inspecting the necessary memory function, there is a "Marching" pattern.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits written in "0"s. The addressing method will be explained for a simple 16 bit memory as an example.

(1) Write "0" for all bits ..... Fig. 1(a)
(2) Read "0" of 0th address and check that the read data is "0". Hereafter, the meaning of "Read" is "checking and judging the data".
(3) Write "1" in the 0th address ..... Fig. I(b)
(4) Read "0" of 1st address
(5) Write "1" in 1st address
(6) Read "0" of nth address
(7) Write "1" in nth address ..... Fig. 1(c)
(8) Repeat above procedures (6) and (7) up to the last. Finally, all data will become "1".
(9) Since all data are "1"s in this condition, replace "0" and "1" after procedure (2) and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

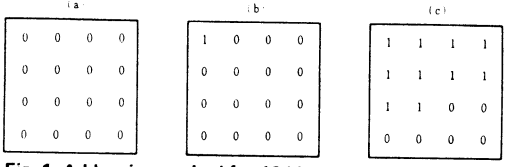


Fig. 1 Addressing method for 16 bits memory in the Marching pattern

3. Generation of Marching Pattern

The method of generating the marching pattern and displaying failed bits of the memory on the Braun tube will be introduced. Fig. 2 shows the all block diagram. The address pattern is generafed by using four synchronous 4 bit counters. All address patterns are shown in Fig. 4. This example, is for 16K bit memory, however, it can be easily understood that A14 which has a half frequency of the maximum address input A13 is the same as the data input.

The A15 signal together with the carrier signal of HD74161 is used to determinine the termination of the sequence.

As shown in Fig 2. In the read and write cycles after cleaning all bits addressing is twice the period of clearing. This switching is performed at the gate of

the binary circuit following the reference pulse generating circuit.

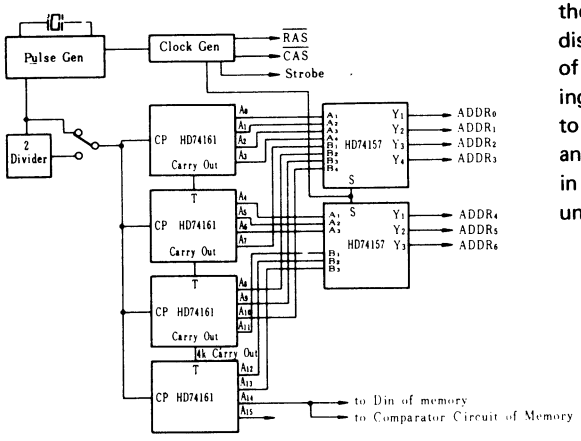


Fig. 2 Marching Pattern Generating Circuit

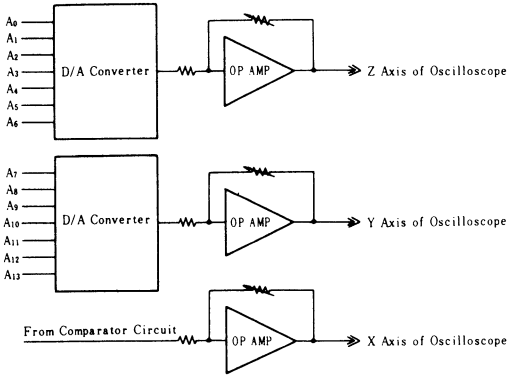


Fig. 3 Fail Bit Map Display Circuit

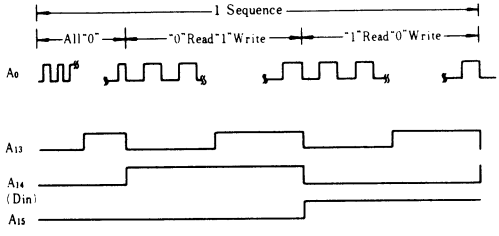
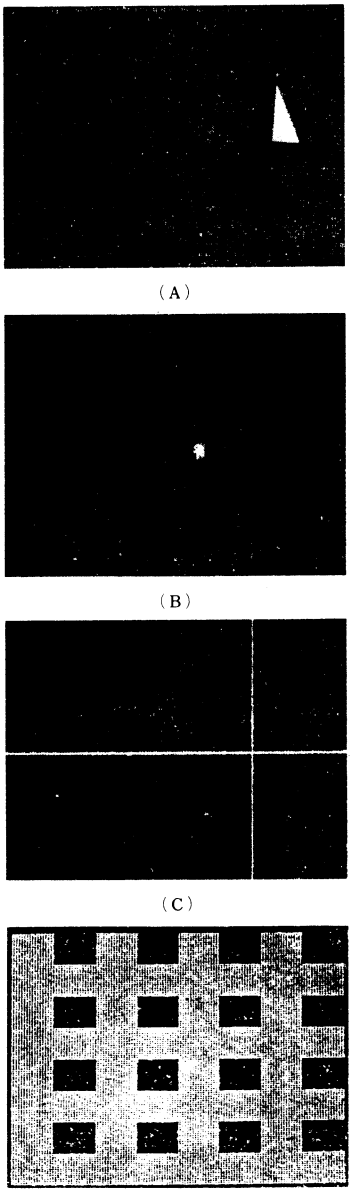


Fig. 4 Entire Pulse Relations

Input the output of HD74161 is input to the D/A converter and the output of D/A converter is connected to the oscilloscope to display → X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the fail bit map can be displayed on the CRT. Fig. 5 shows an example checking a voltage margin. By changing the power voltage V_{BB}, the increase and decrease of the failed bits can be well understood. The operation of the memory can be dynamically understood by displaying its operation on the CRT. The operation of the memory IC is extremely complicated differing from other TTLs, etc.. Its operation is not easy to understand by pulse waveform observation with an ordinary oscilloscope. The fail bit map as shown in Fig. 5 is extremely useful. It is capable of visually understanding the operation of memory IC.



(A)

(B)

(C)

(D)

Fig. 5 Example of 1 bit solid fail

4. Failure Mode

Generally, failure 70% ~ 90% of failures at users are of those called solid failure. This failure mode has no relation with access time, voltage margin and timing, and is not capable of reading from or writing to certain specified bits and is failure fixed to "0" or "1". The convenient checker, previously mentioned as simple tester, is sufficiently capable of detecting such failures. Therefore, with the exception of special cases, it can be considered that the necessity of performing high-precision measurements such as those made by memory IC manufacturers is rare.

In the inspection of memory IC at our company, full inspection under the worst conditions are performed so as to guarantee sufficient operations under all power voltage conditions and timing conditions listed in the data sheet.

An extremely accurate memory tester becomes necessary for performing high-precision inspection with 1ns accuracy. Our company is developing IC memory testers to supply memory ICs with excellent characteristics and quality to users and is establishing the system capable of developing further high-efficiency memory ICs.

■ APPLICATION OF DYNAMIC RAMS

1. Power On

After turning on power to set the memory circuitry, hold for more than 500μs and apply eight or more dummy loads before actuating the memory. The dynamic cycle may be either an ordinary memory cycle or a refresh cycle. When power is turned on, power-on current flows which varies with the rise time of V_{CC} and clock conditions, as shown in Fig. 1. If the rise time is 10μs or thereabout, the RAM does not operate dynamically and through-current passes to the internal inverter since the potential at the internal circuitry becomes unstable. Nevertheless, this through-current decreases as the operation of the internal circuitry becomes stable. With all this in mind, rise time of not shorter than 100μs is recommended for power-up.

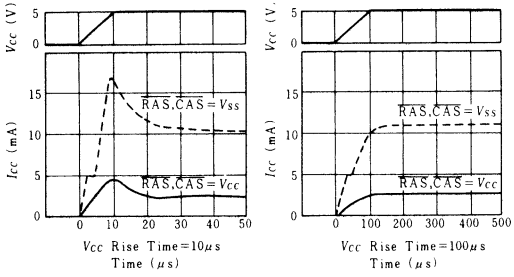


Fig. 1 Relationship between standard value of I_{CC} and V_{CC} during power-up

2. Operation Modes (See Fig. 2)

(1) Read Cycle:
First, decide the X address of the memory cell chosen and start with trailing of $\overline{RAS}$. When the X address has been held by the internal circuitry, change it to Y address. Then, trail $\overline{CAS}$ to take in the Y address. If the $\overline{WE}$ pin is at high level, output will appear on the Dout pin after a certain time.

(2) Write Cycle:
The input at Din is written in the memory cell when $\overline{WE}$ turns to low level before $\overline{CAS}$.

(3) Read/Modify/Write Cycle:
During this cycle, $\overline{CAS}$ and, then, $\overline{WE}$ are trailed down to low level so that data is read out from and written in the same address with in the same memory cycle.

(4) Page Mode Cycle:
In this cycle; $\overline{CAS}$ is cyclically moved, after taking in the X address through $\overline{RAS}$, to scan only the Y address. This permits reading out and writing in only one column data at high speed.

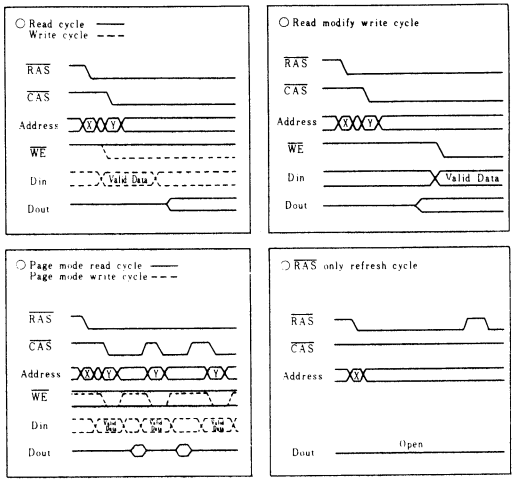


Fig. 2 Operating modes of Dynamic RAMs

2. Data Output

Dout is a TTL-compatible three-state output with two TTL-load fan outs. The output is controlled by the $\overline{CAS}$ signals; it is held while $\overline{CAS}$ is low, while Dout returns to a floating state when $\overline{CAS}$ is high. In the early write cycle, the output becomes a high-impedance one to permit the use as a common I/O terminal.

3. Refreshing

Refreshing is a process of periodical rewriting to make up for the leakage of the charge accumulated in the memory cell. This operation is implemented in the $\overline{RAS}$ only refresh cycle, ordinary read cycle, and so on. Whether 16k- or 64k-bit, all bits can be refreshed by giving a 128-cycle scanning to only the X addresses between A0 and A6. To be more specific, each cycle refreshes 128 bits for the 16k-bit Dynamic RAMs and 512 bits for the 64k-bit RAMs. Especially, the $\overline{RAS}$ only refresh cycle permits such a power-efficient refresh as calls for only approximately 75 percent of the current consumed by the read cycle. With $\overline{CAS}$ fixed at high level, the output is a high-impedance one. The HM4816A has a special function called the hidden refresh which enables holding the output by turning $\overline{CAS}$ to "low" while $\overline{RAS}$ only refresh is on. There are two methods of refreshing: concentrated and deconcentrated refreshing. The former gives a concentrated 128-cycle refresh after operating the memory for a period of 2ms maximum. In contrast, the latter repeats a refreshing cycle every 16μs following the initial 16μs (=2ms/128) memory operation. A

choice between the two modes calls for a careful consideration about the system's efficiency.

4. Operating Current for Dynamic RAMs

Fig. 3 shows the waveforms of the current applied in various operating modes (HM4864). The mean operating current in each mode equals the value obtained by dividing the integrated result of each waveform by the cycle time. The first peak current in each operating mode appears as a result of the circuit operation during the memory access time. On the other hand, the peak current during standby appear as a result of the precharging operation in each circuit. Having two circuitry operation modes — X and Y. Dynamic RAMs show different peak currents depending upon the operating timing of $\overline{RAS}$ and $\overline{CAS}$. That is, the greatest peak current appears when both X and Y circuits operate simultaneously. The maximum peak current for the HM4864, for example, is approximately 100mA. The current consumed while the memory stands by on the board is expressed in terms of the cycle time dependency shown in Fig. 4. During standby, with a once-in-every 16μs refresh, the HM4864 consumes approximately 3mA of current.

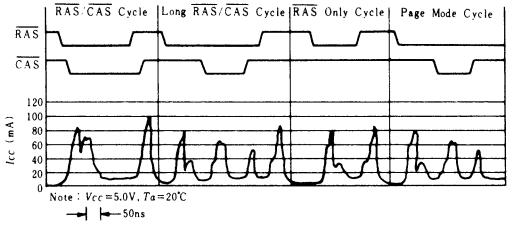


Fig. 3 Power supply voltage (HM4864)

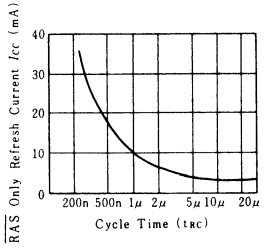


Fig. 4 Cycle time dependence of $\overline{RAS}$ only refresh current (HM4864)

5. Noise

Broadly, noise can be classified into power source noise and input signal noise. With the latter, furthermore, whether it is an overshoot or undershoot must be considered. The overshoot should be held below the highest input level specified. As to the undershoot, the input-undershoot-induced parasitic transistor effect in the input area is prevented by providing a –5V V_{BB} to the three-way power source and a built-in bias circuit on the substrate. Normally, design should be such that the input undershoot does not exceed the minimum value specified for V_{IL}, at worst. The power source noise can be further classed into low-frequency noise and high-frequency noise as shown in Fig. 5. To assure a stable memory operation, the peak-to-peak power supply voltage in the presence of low- or high-frequency noise should be held below 10 percent of its standard level. Overshoot and undershoot can be reduced by inserting a damping resistance of several tens of ohms in Dynamic RAM series. To prevent the power source noise, it is recommended to provide a condenser of 0.1μF or so to each one or two devices.

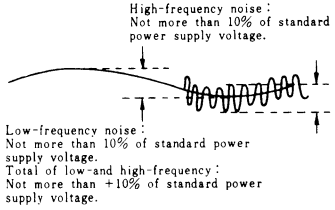


Fig. 5 Power source noise

1. PROGRAMMING & ERASING OF EPROM

1.1 Programming

Information is programmed into the memory cell of an EPROM by applying a high voltage to its drain and gate (Fig. 1 and 2). The high voltage at the drain increases the energy of the electrons in the channel area. When the energy becomes high enough, the electrons become what are known as "hot electrons" that are capable of jumping across the oxide film. Pulled by the high voltage at the gate, the hot electrons are admitted into the floating gate. The electric charge entering the floating gate changes the threshold voltage in the memory element, whereby it is stored as new information. When reading out, voltage is applied as shown in Fig. 3, and "1" and "0" are identified by checking whether or not current flows. Since the drain voltage for read-out is set at about 3V, no erroneous writing takes place. When shipped, all bits of the EPROM are held at logic "1" with all electric charge released (with no information programmed in). By changing the logic 1 to logic 0 through the application of the specified waveform and voltage, the necessary information is programmed in. The higher the V_{pp} voltage and the longer the program pulse width t_{pW}, the more will be the quantity of electrons to be programmed in, as shown in Fig. 4. If the V_{PP} exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot by the PROM programmer and take all other possible caution. Also with for the negative-voltage-induced noise at other terminals, since it can touch off a parasitic transistor effect and apparently reduce the yield voltage Hitachi's EPROMs are usually capable of being written and erased more than 100 times, although the number of times is not guaranteed because it is difficult to give an exhaustive inspection prior to shipment. At any rate, 100 times is enough since the frequency of reprogramming in practical application rarely exceeds about 10 times.

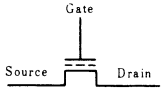


Fig. 1 Memory transistor circuit symbols

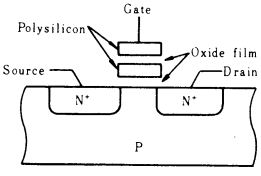


Fig. 2 Cross section of memory transistor

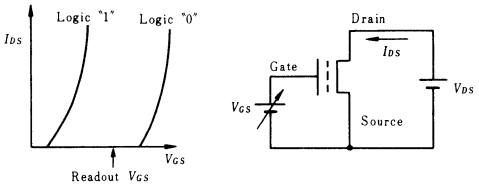
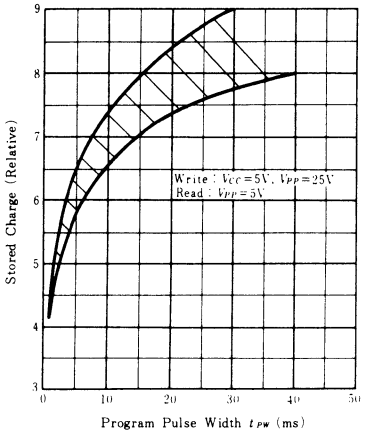


Fig. 3 Reading out stored information



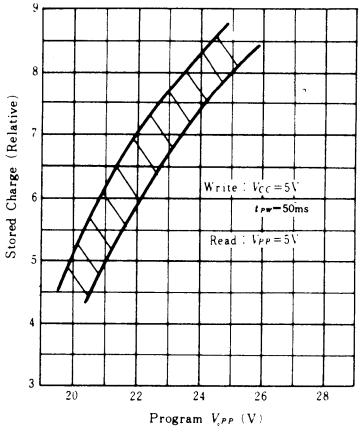


Fig. 4 Typical Programming Characteristics of EPROMs.

1.2 Erasing

Data stored in the EPROM is erased by releasing the electric charge from the floating gate through the exposure of the memory chip to ultraviolet light. Light has an energy that is inversely proportional to its wavelength. Receiving the energy of the ultraviolet light, the electrons in the floating gate are again turned into hot electrons, which jump across the oxide film into the control gate or substrate. As a result of this process, the stored information is erased. Accordingly, the stored information can not be erased by such lights whose wavelengths are too long to give adequate energy to jump over the barrier of the oxide film. For successful erasing, the wavelength and minimum exposure rate of ultraviolet light are specified as 2,537Å and 15W sec/cm^2 respectively. This condition is attained by exposing a device to an ultraviolet lamp of 12,000μW/cm^2 1.2 ~ 3cm away for approximately 20 minutes. The ultraviolet light transmission rate of the transparent lid is about 70 percent. Any contamination or foreign material at the surface of the capsule lowers the transmission rate, prolonging the erasing time. So such contamination should be recovered by use of alcohol or other solvent that does not damage the package. Fig. 5 shows typical erasure characteristics for EPROM.

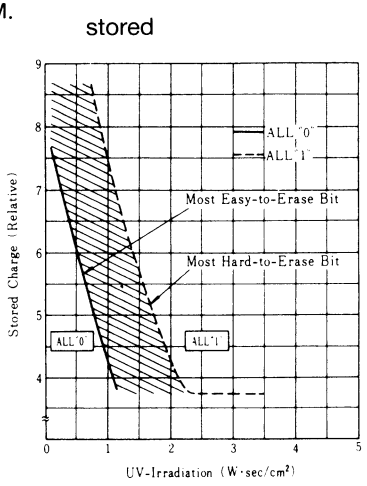


Fig. 5 Typical Erasing Characteristics

1.3 Data retention characteristic of EPROM

As a result of writing in, approximately 0.5 to 2.0 x 10^{-13} coulomb of electrons are accumulated at the floating gate. With the elapse of time, however, these electrons decrease, as a result of which the inversion of stored information can happen. The mechanism of electron dissipation is generally explained as follow:

(1) Data dissipation by heat

The accumulation of electrons at the floating gate is an unbalanced state, so the dissipation of thermally excited electron is unavoidable. Therefore, the data holding time has a close relationship with temperature. Fig. 6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

(2) Data dissipation by ultraviolet light

Ultraviolet rays at a wavelength of not greater than 3,000 ~ 4,000Å is capable of releasing the electric charge stored in the memory of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet rays, so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Fig. 7 shows examples of the data retention time under an ultraviolet eraser, sunlight and fluorescent lighting. But it should be noted that the data for fluorescent light and sunlight are not definite because of their varying ultraviolet ray contents. The ultraviolet ray content in sunlight, for example, varies greatly with seasons, weather and the composition of the atmosphere.

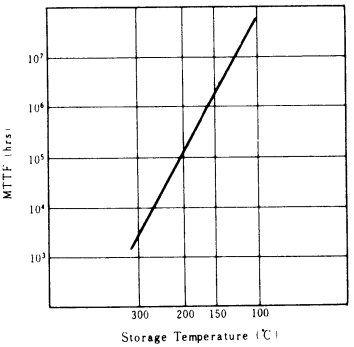


Fig. 6 Typical Data Retention Characteristics

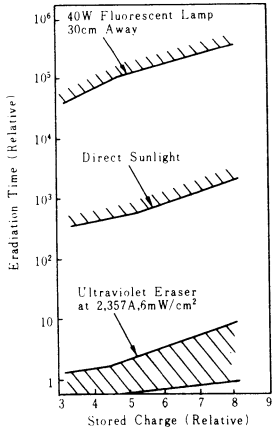


Fig. 7 EPROM's data retention time

(3) Data dissipation by voltage

This type of data dissipation occurs while information is being written in. At other memory cells lying on the same word line or data line as the memory cell being programmed, high voltage can cause the dissipation of stored electric charge. Of course, such defects are removed at the factory by pre-shipment inspection. The programming voltage and pulse width should be always kept within the specified range for the same reason.

1.4 EPROM Programmer

The 16K EPROM Programmer stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions, the Blank check function prior to programming, the programming function and the Verify function after programming are necessary. As shown in the drawing, there are also programmers provided with a reverse insertion checking function or pin contact checking function prior to the Blank Check. The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin. Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

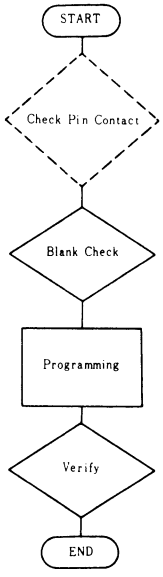
This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

(c) Blank check

This check is performed prior to programming and checks whether or not it is an erased EPROM or for preventing EPROM reprogramming. Since the output data in the erased condition are "1" (high level), check whether or not data in EPROM are all "1". It willfail-stop even when 1 bit of "0" (low level). Normally, it is designed to provide warning with a lamp or buzzer.

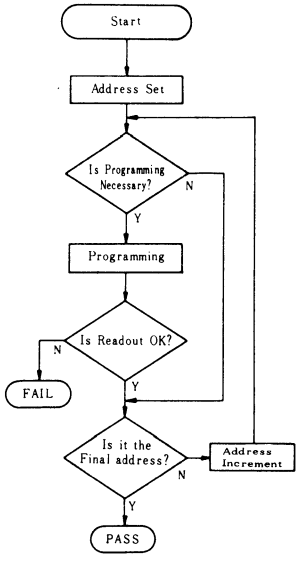
(d) Programming

The function of programming the data in the internal RAM of the programmer into EPROM and will fail-stop when programming cannot be made. The normal flow is as shown below. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



(e) Verify

This function is for checking after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer and it performes fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program

There are the following methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and retypewriter input are options.

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.

1.5 Handling EPROM

When brought in contact with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write marging setting that give a wrong impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges through the eradiation of ultraviolet rays for a short time. It is recommended to execute reprogramming after this eradiation since it reduces the electric charges in the floating gate, too. The basic cluntermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

(1) Establish a ground for the operator to handle EPROM. Avoid the use of gloves etc. that may develop a static charge.
(2) Refrain from rubbing the glass window with plastics and other substances that may develop a charge.
(3) Avoid the use of coolant sprays which contain some ions.
(4) Use shielding labels (especially those containing conductive substances) that can evenly distribute the established charge.

1.6 Shielding label

When using an EPROM in an environment where ultraviolet exposure can occur, it is advisable to put a shielding label on its glass window to absorb ultraviolet light. Specially prepared shielding labels are marketed. Metal-loaded labels are particularly effective. In choosing a shielding label, the following points should be carefully checked.

(1) Adhesiveness (mechanical strength)

Avoid repeated attaching and dusting that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on the old one since peeling may develop a static charge.)

(2) Allowable temperature range

Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass even after the label has been removed.

(3) Damp-proofness

Use the shielding label in an environment whose humidity falls within the specified allowable humidity range. Today there are few shielding labels that can meet all environmental requirements established for the EPROM. So a suitable one must be chosen for each specific application.

■ MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into the mask ROM is performed by the CAD system using a large-sized computer. You should submit the data of the ROM code in conformity with the specification explained below by either Floppy Disk, EPROM or magnetic tape. In addition, enter your instructions such as the chip select, in the "ROM Specification Identification Sheet" and attach it to the ROM code data.

1. Specification of EPROM

(1) You should submit the three set of the EPROM stored Data and spesify the address of the EPROM in case of the two or four EPROMS.

(2) The ROM Code data is input from the start address to Final Address in the EPROM.

(3) Type of EPROM

HN462716 (2K-word x 8-bit, 2716 Compatible)
HN462532 (4K-word x 8-bit, TMS2532 Compatible)
HN462732 (4K-word x 8-bit, 2732 Compatible)
HN482764 (8K-word x 8-bit, 2764 Compatible)
HN4827128 (16-K word x 8-bit, 27128 Compatible)

2. Specification of Magnetic Tape

2.1 Use the following type of magnetic type which can be entered in a magnetic tape device which is compatible with the IBM magnetic tape device.

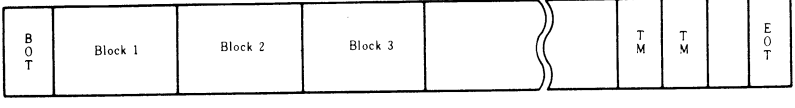
(1) Length . . . . 2,400 feet, 1,200 feet or 600 feet
(2) Width . . . . . 1/2 inch
(3) Channel . . . . . 9 channels
(4) Bit density . . . 800 BPI or 1,600 BPI (Clearly state which it is in the "ROM Specification Indentification Sheet".)

2.2 Use the EBCDIC code as the use code.

2.3 Make the format of the magnetic tape as described below.

(1) No leading tape mark
(2) No label
(3) Record size . . . . . 80 byte/1 record
(4) Block size . . . . . 10 records/1 block
(5) The end of the file should be indicated by 2 successive tape marks (TM).

2.4 Ensure that the magnetic tape becomes of 1 roll for each chip. Since extending the single-chip portion over several rools is impermissible, submit by compiling into the single-chip portion for each roll.



2.5 Data Mode

2.5.1 HMCS6800 Load Module Mode

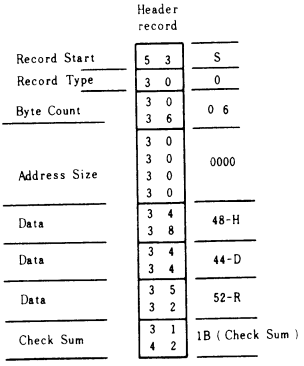
This mode is the object mode output from the assembler of HMCS6800.

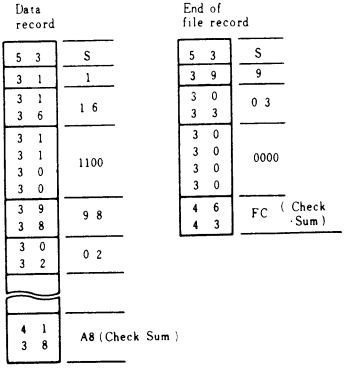
(1) Divide the 8 bit code into the upper and lower 4 bit codes and convert each into hexadecimal notation.

(Example) The code of 1100 0110 becomes as follows under binary notation.

(Upper 4 bits)	(Lower 4 bits)	Bit weight
D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	(ROM output
1 1 0 0	0 1 1 0	equivalence)

(2) The actual load module mode becomes as shown below.





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S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown below.

Example

Header Record	→S00B000058204558414D504CB5
Data Record	→S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record	→S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of File Record	→S9030000FC

(3) In case the address is skipped, perform entry into the "ROM Specification Identification Sheet" that the skipped address, and the data (00 or FF) entered into the skipped address by hexadecimal notation.

2.5.2 BNPF Mode

(1) One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.

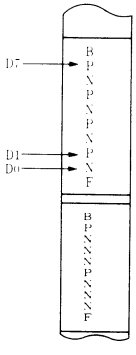
(2) The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

(Example) The code of AA by hexadecimal notation is symbolized as shown below.

(3) It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.

B ····· Indicates start of 1 word.
N ····· Indicates "0" of 1 bit data.
P ····· Indicates "1" of 1 bit data.
F ····· Indicates end or 1 word.

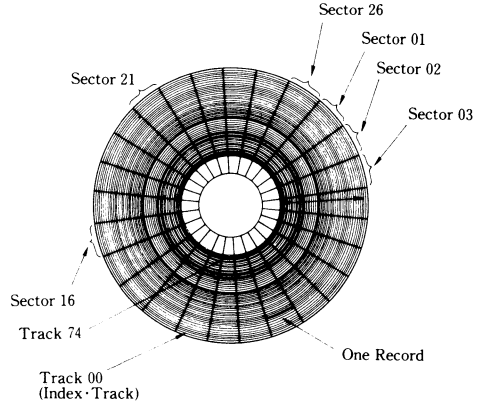
Example



3. Specification of Floppy Disk

3.1 Use the following type of Floppy Disk

(1) Type . 8 Inch Single Sided and Single Density.
(2) Number of Sector 26
(3) Number of Track 77



3.2 Use the EBCDIC code as the use code.

3.3 Make the format of the floppy disk as described below.

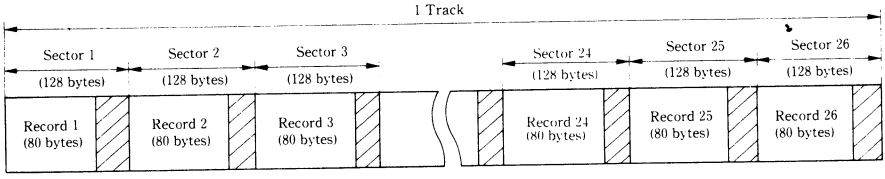
(1) Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 ~ 26
3	Data Area	01 ~ 73	01 ~ 26
4	Alternal Track	75, 76	01 ~ 26
5	Spare Track	00 74	01 ~ 06 01 ~ 26

(2) Record size . . . . . 80 byte/1 record
(3) Use the sector as below. Use one sector for one record, that is 80 bytes out of 128 bytes used for one record.

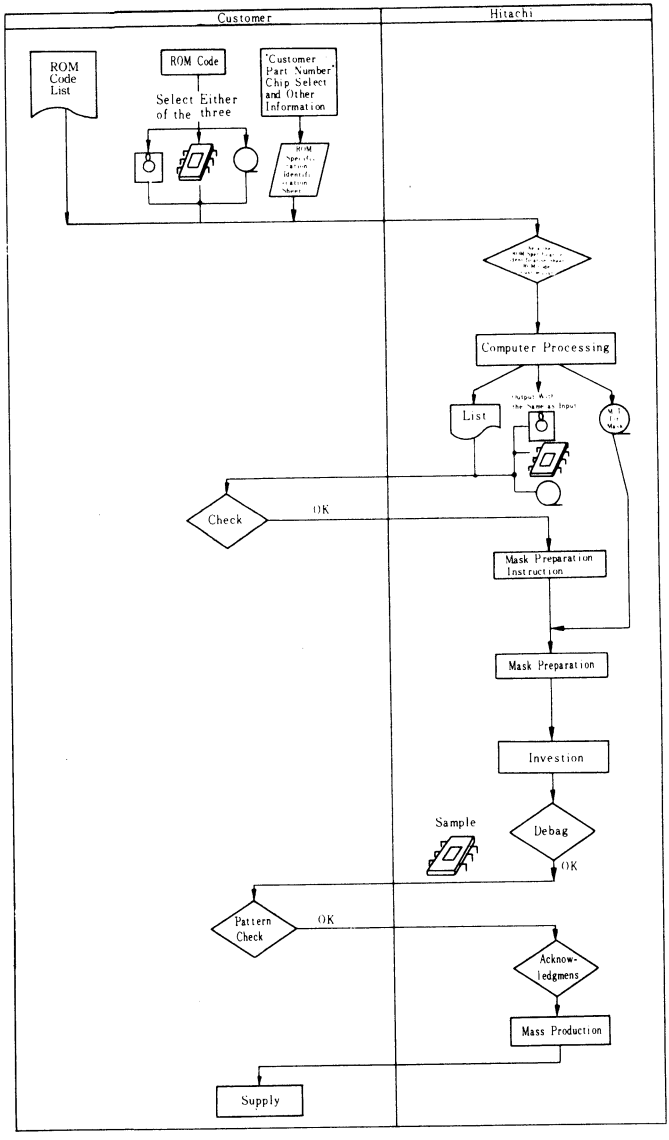
3.4 Data Mode

See 2.5



: unuse

Mask ROM Development Flowchart



DATA SHEETS

MOS STATIC RAM

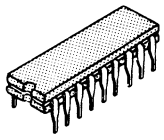
HM6148H-35, HM6148H-45, HM6148H-55, HM6148HP-35, HM6148HP-45, HM6148HP-55

1024-word x 4-bit High Speed Static CMOS RAM

■ FEATURES

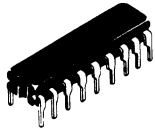
- Fast Access Time ..... 35/45/55ns (max)
- Low Power Standby and Low Power Operation; Standby: 100 μW (typ.), Operation: 175mW (typ.)
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Common Data Input and Output; Three-State Outputs
- Pin-Out Compatible with Intel 2148H

HM6148H Series



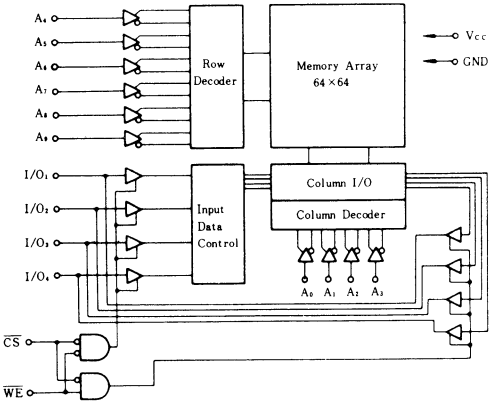
(DG-18)

HM6148HP Series

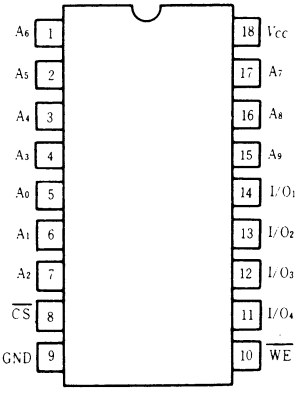


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature**	T_{bias}	−10 to +85	°C

* with respect to GND. $V_{IL\,min} = -3.5$V (Pulse width=20ns)
** under bias

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

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■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5*	—	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS[1] (Ta=0~70°C, V_{CC}=5V±10%, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=max, V_{IN}=GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2.0	μA	
Operating Power Supply Current (1)	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	35	80	mA	
Operating Power Supply Current (2)	I_{CC1}	min. cycle, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	50	100	mA	[2]
Standby Power Supply Current (1)	I_{SB}	$\overline{CS}$=V_{IH}	—	5	20	mA	
Standby Power Supply Current(2)	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	20	800	μA	
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V	
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V	

Notes) 1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
2. 120mA max. for HM6148HP-35

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

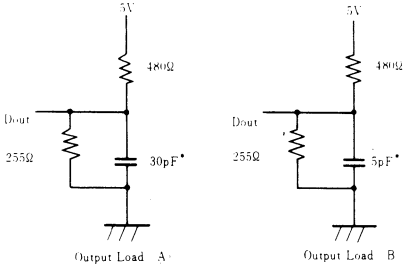
■ AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●RISE/FALL TIME

Item	Symbol	min	typ	max	Unit
Input Rise Time	t_r	—	5	100	ns
Input Fall Time	t_f	—	5	100	ns

●AC TEST CONDITIONS

Input pulse levels : GND to 3.0V
Input rise and fall times : 5ns
Input and Output timing reference levels : 1.5V
Output load : See Figure



* Including scope & jig.

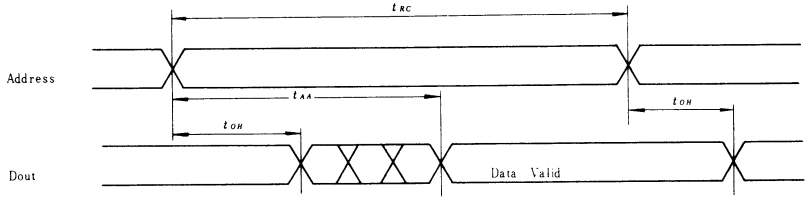
■AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise noted.)

●READ CYCLE

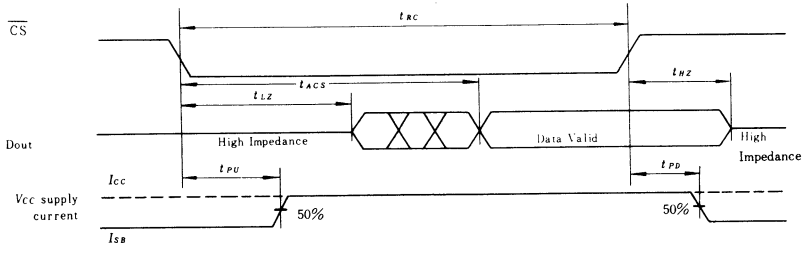
Item	Symbol	HM6148HP-35		HM6148HP-45		HM6148HP-55		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns
Address Access Time	t_{AA}	—	35	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

* Transition is measured ±500mV from high impedance voltage with Load(B). This parameter is sampled and not 100% tested.
At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

●TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



●TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



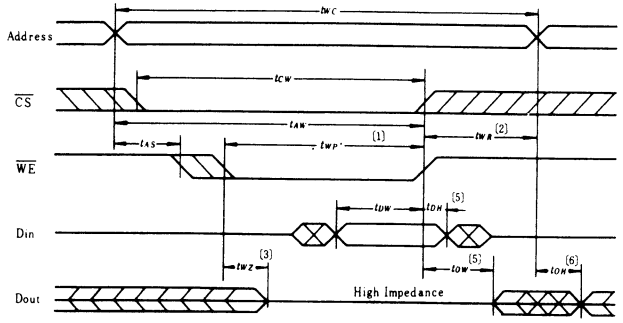
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

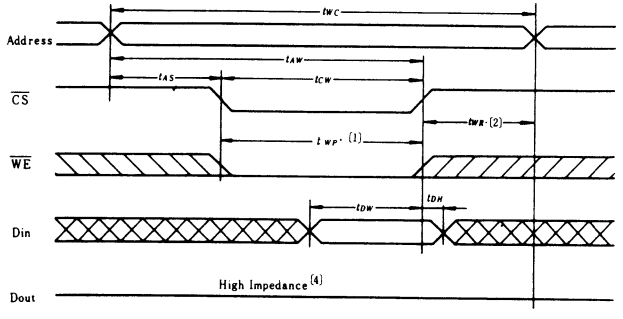
Item	Symbol	HM6148H/P-35		HM6148H/P-45		HM6148H/P-55		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	40	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	10	0	15	0	20	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	0	—	ns

* Transition is measured ±500mV from high impedance voltage with Load B.
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ Controlled)

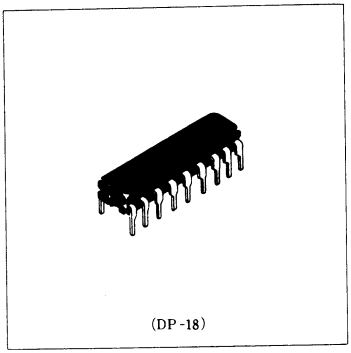


NOTES of Timing Waveform of Write

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle.

HM6148HLP-35, HM6148HLP-45, HM6148HLP-55

1024-word × 4-bit High Speed Static CMOS RAM

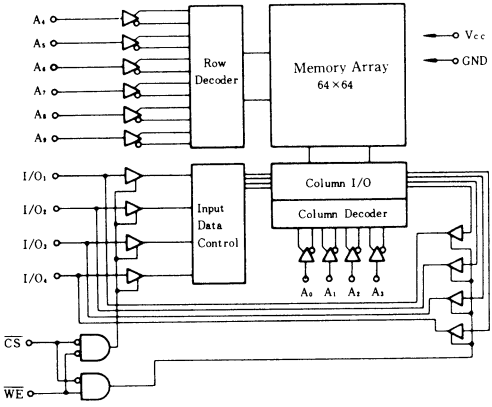


(DP-18)

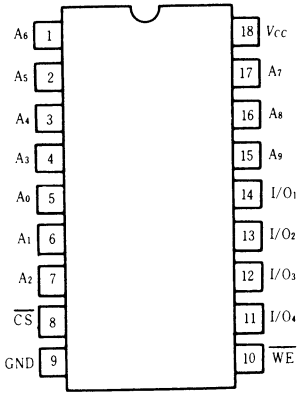
■ FEATURES

- Low Power Standby and Low Power Operation; Standby: 5μW (typ.), Operation: 175mW (typ.)
- Fast Access Time: 35/45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage *	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature **	T_{bias}	−10 to +85	°C

* with respect to GND. $V_{IL\ min} = -3.5$V (Pulse width = 20ns)

** under bias.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5 *	—	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS[1] (Ta = 0~70°C, V_{CC} = 5V±10%, GND = 0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = max, V_{in} = GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	2.0	μA	
Operating Power Supply Current (1)	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	35	80	mA	
Operating Power Supply Current (2)	I_{CC1}	min. cycle, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	50	100	mA	[2]
Standby Power Supply Current (1)	I_{SB}	$\overline{CS}$ = V_{IH}	—	5	20	mA	
Standby Power Supply Current (2)	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V	—	1	50	μA	
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V	

Notes) 1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
2. 120mA max. for HM6148HLP-35

■ CAPACITANCE (Ta = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

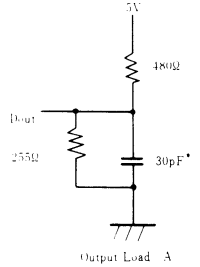
■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

● RISE/FALL TIME

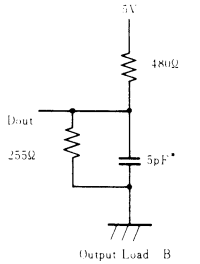
Item	Symbol	min	typ	max	Unit
Input Rise Time	t_r	—	5	100	ns
Input Fall Time	t_f	—	5	100	ns

● AC TEST CONDITIONS

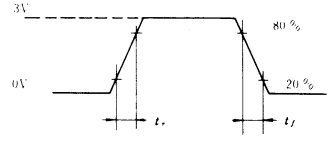
Input pulse levels : GND to 3.0V
Input rise and fall times : 5ns
Input and Output timing reference levels : 1.5V
Output load : See Figure



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})



$t_r = t_f$ = 5ns
Input Pulse Waveform

* Including scope & jig.

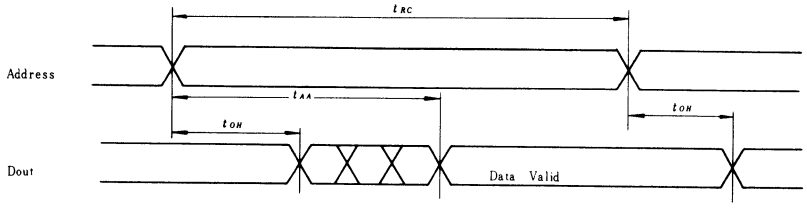
■AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise noted.)

●READ CYCLE

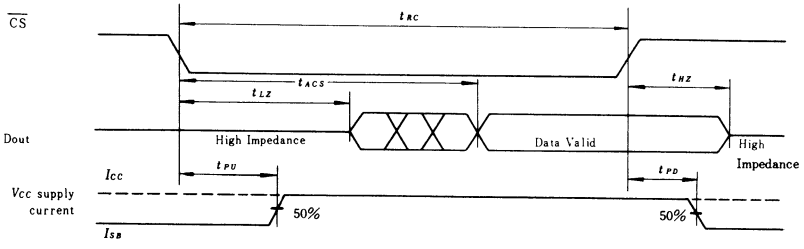
Item	Symbol	HM6148HLP-35		HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns
Address Access Time	t_{AA}	—	35	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

* Transition is measured ±500mV from high impedance voltage with Load(B). This parameter is sampled and not 100% tested.
At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

●TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



●TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



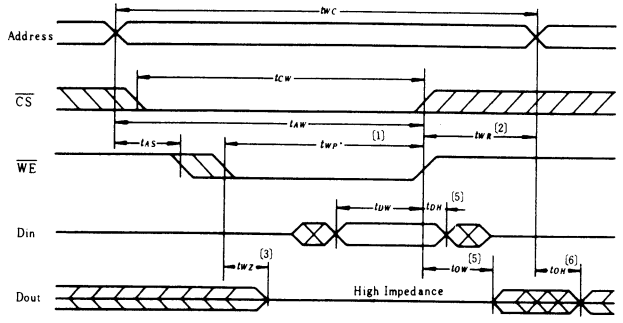
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$= V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

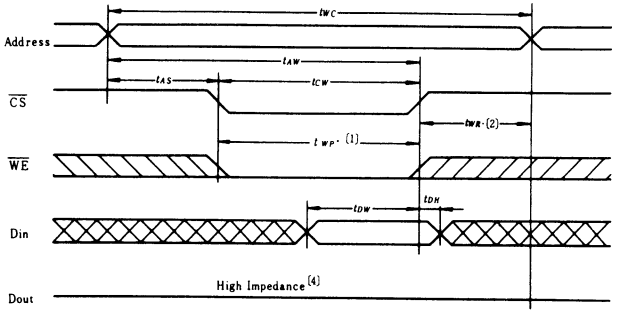
Item	Symbol	HM6148HLP-35		HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	40	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	10	0	15	0	20	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	0	—	ns

* Transition is measured ±500mV from high impedance voltage with Load B.
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ Controlled)



Notes of Timing Waveform of Write :
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle.

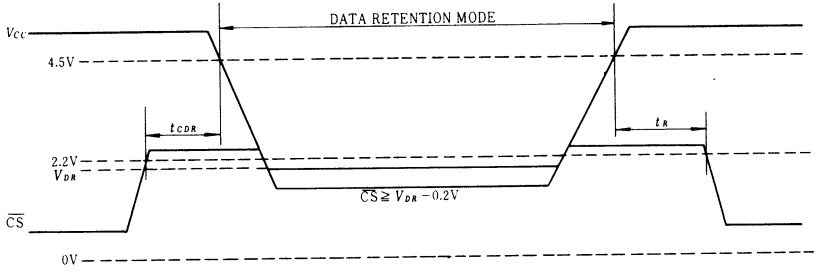
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} (1)	—	—	ns

Note) 1. t_{RC} = Read Cycle Time.

* V_{CC} = 3.0V
** V_{CC} = 2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM



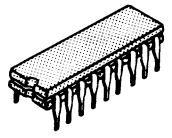
HM6147H-35, HM6147H-45, HM6147H-55, HM6147HP-35, HM6147HP-45, HM6147HP-55

4096-word×1-bit High Speed Static CMOS RAM

■FEATURES

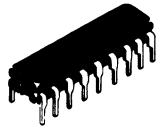
- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

HM6147H-35, HM6147H-45, HM6147H-55



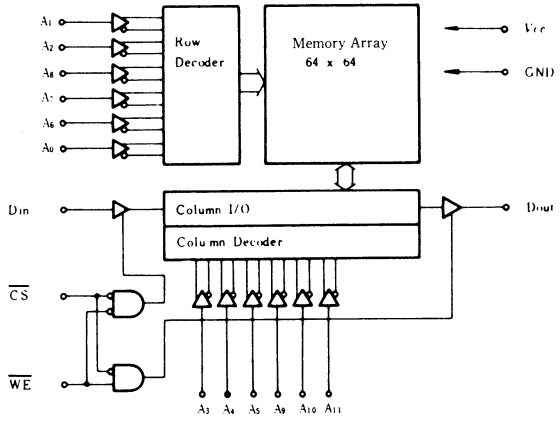
(DG-18)

HM6147HP-35, HM6147HP-45, HM6147HP-55

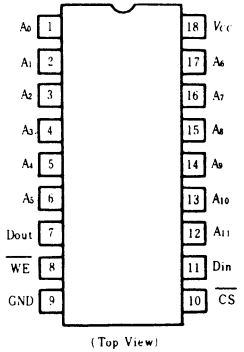


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	−3.5* to +7.0	V
DC Output Current	I_o	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (under bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

* Pulse Width 20ns, DC : −0.5V

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq Ta \leq 70°C$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width 20ns, DC : −0.5V

■DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5V \pm 10\%$, GND=0V)

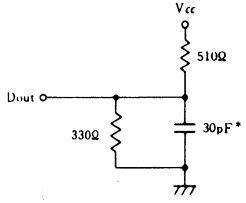
Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{out}=0V \sim V_{CC}$	—	—	10	μA
Operating Power Supply Current(1)	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2)	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1)	I_{SB}	$\overline{CS}=V_{IH}$, V_{CC}=Min to Max	—	8	20	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	20	800	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.
2. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.

■AC TEST CONDITIONS

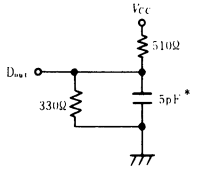
- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147H/P-35)
  0.8 to 2.0V (HM6147H/P-45/55)

Output Load A



* Including scope & jig capacitance

Output Load B



■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	6	pF

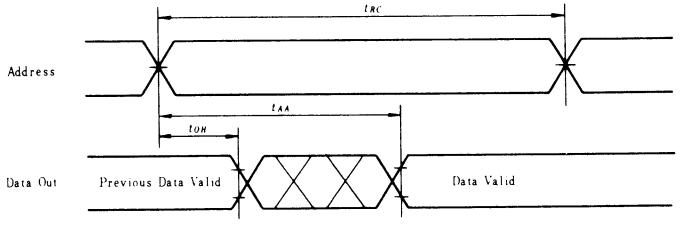
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (Ta=0℃ to 70℃, V_{CC}=5V±10%, unless otherwise noted.)

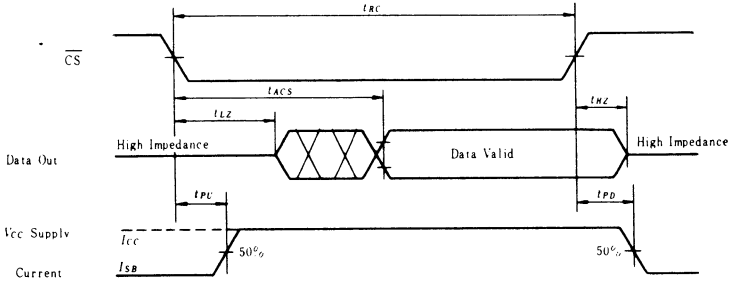
● READ CYCLE

Parameter	Symbol	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	[1]
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	[2], [3], [7]
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	[2], [3], [7]
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)

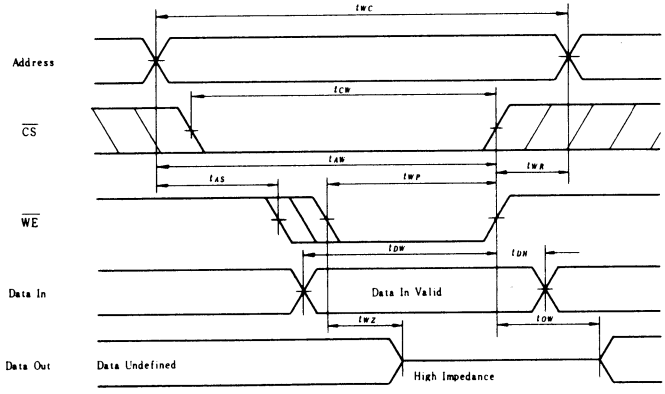


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

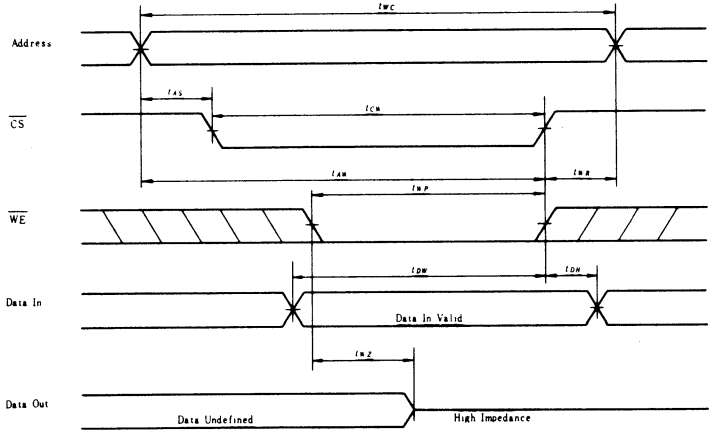
● WRITE CYCLE

Parameter	Symbol	HM6147H/P-35		HM6147H/P-45		HM6147H/P-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	[2]
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	[3], [4]
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	[3], [4]

● TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



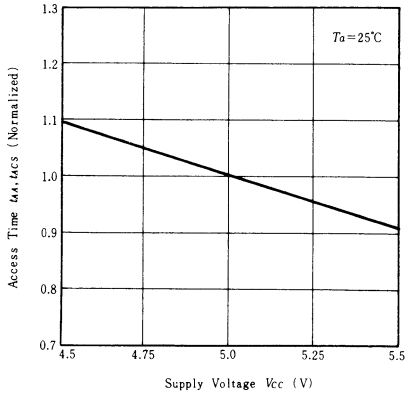
● TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



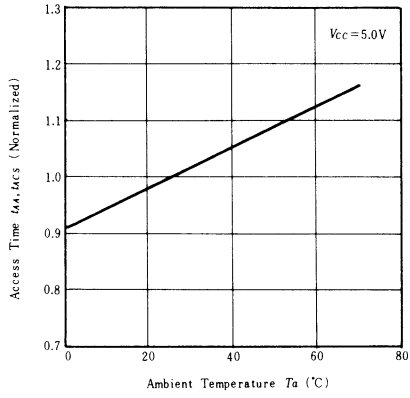
Note! $\overline{CS}$ or $\overline{WE}$ are High for Address Transition

Notes:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

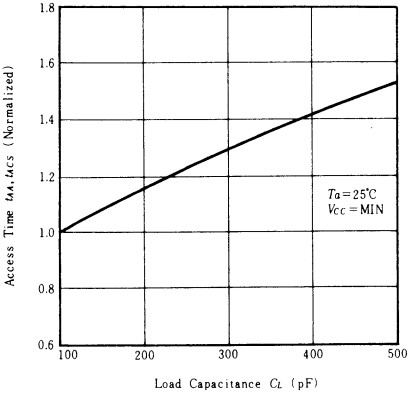
ACCESS TIME VS. SUPPLY VOLTAGE



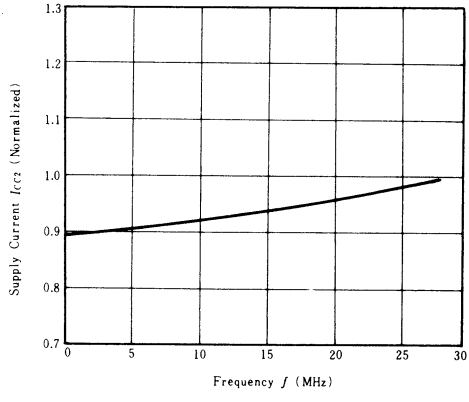
ACCESS TIME VS. AMBIENT TEMPERATURE



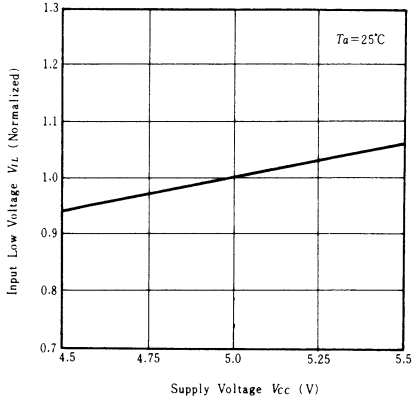
ACCESS TIME VS. LOAD CAPACITANCE



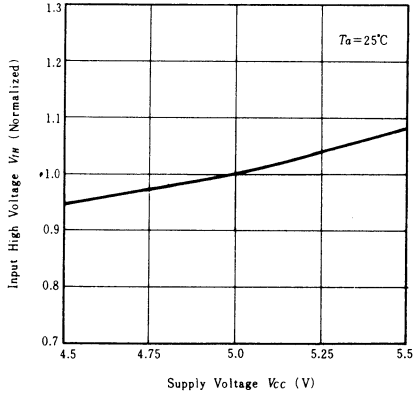
SUPPLY CURRENT VS. FREQUENCY



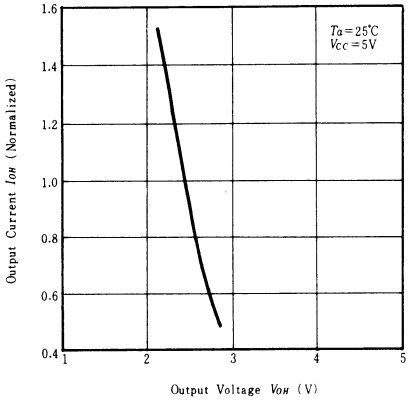
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



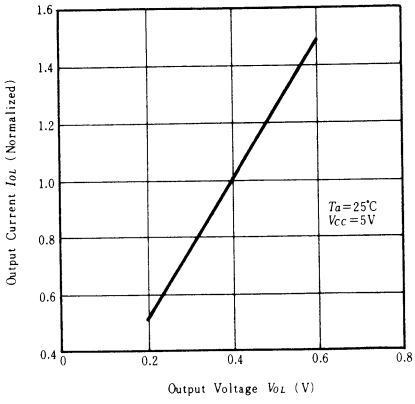
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



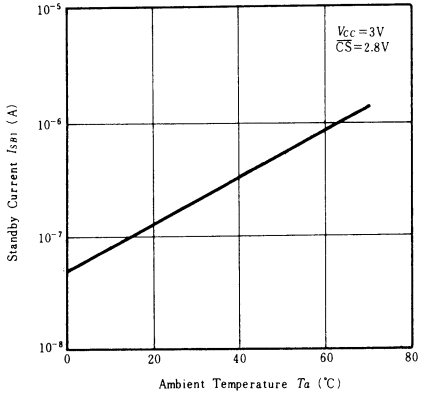
OUTPUT CURRENT VS. OUTPUT VOLTAGE



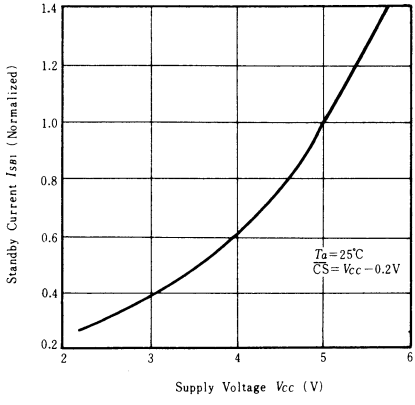
OUTPUT CURRENT VS. OUTPUT VOLTAGE



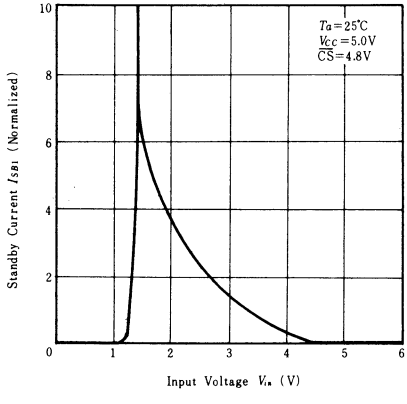
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE

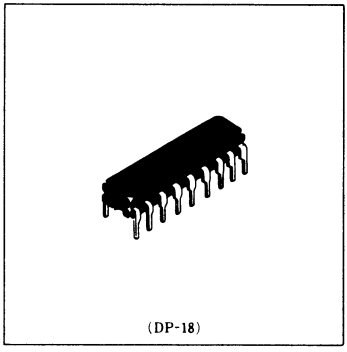


HM6147HLP-35, HM6147HLP-45, HM6147HLP-55

4096-word×1-bit High Speed Static CMOS RAM

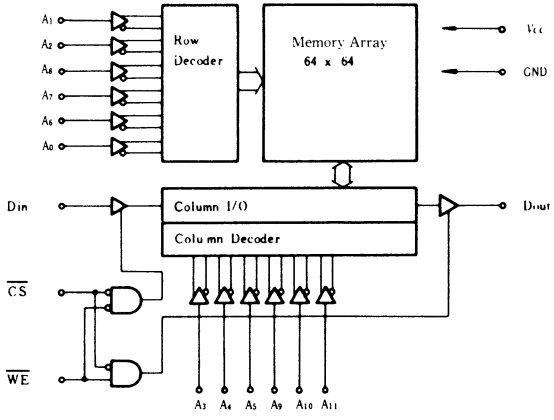
■FEATURES

- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation

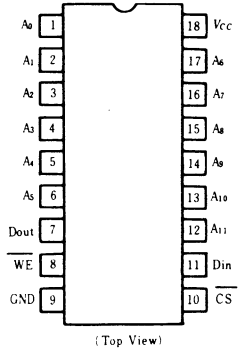


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	−3.5* to +7.0	V
DC Output Current	I_O	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (under bias)	$T_{stg\,(bias)}$	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

* Pulse Width 20ns. DC : −0.5V

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} min = −3V (Pulse width ≦ 20ns)

■DC AND OPERATING CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$, $V_{CC}=5V \pm 10\%$, GND=0V)

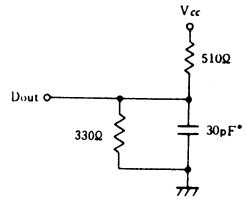
Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V$, GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{out}=0V \sim V_{CC}$	—	—	10	μA
Operating Power Supply Current(1)	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2)	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1)	I_{SB}	$\overline{CS}=V_{IH}$, V_{CC}=Min to Max	—	5	15	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	1	100	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0mA$	2.4	—	—	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.

■AC TEST CONDITIONS

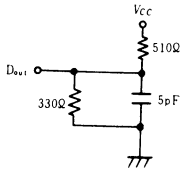
- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels:
  1.5V (HM6147HLP-35)
  0.8 to 2.0V (HM6147HLP-45/55)

Output Load A



* Including scope & jig capacitance

Output Load B



■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	6	pF

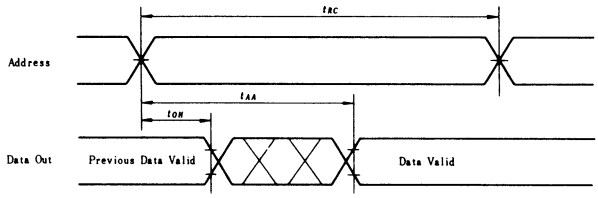
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS ($Ta=0°C$ to $70°C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted.)

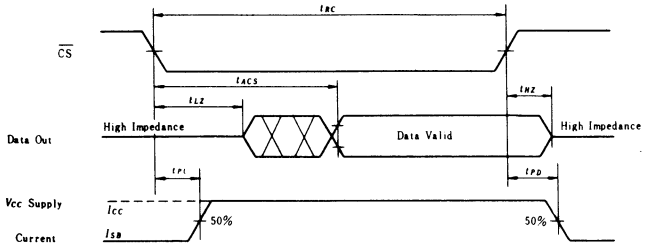
●READ CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		HM6147HLP-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	[1]
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	[2], [3], [7]
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	[2], [3], [7]
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4)(5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4)(6)

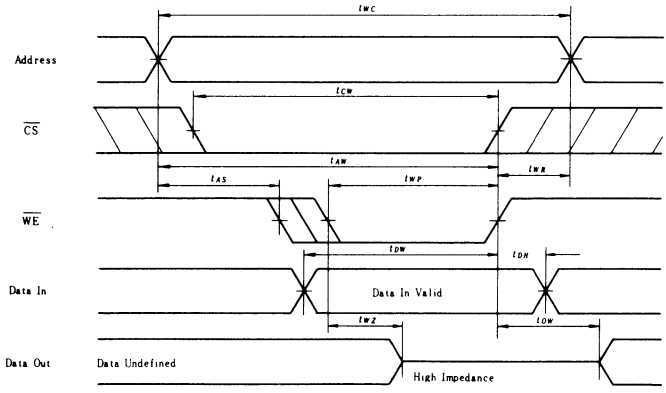


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitionining address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to divice.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

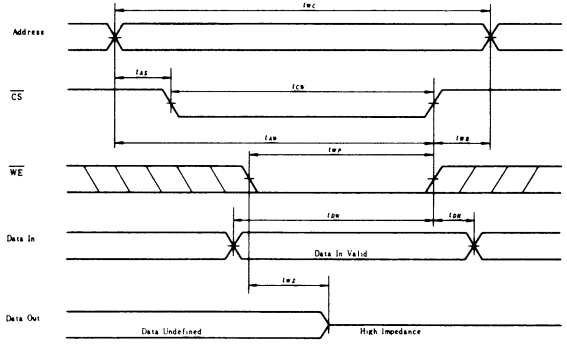
● WRITE CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		HM6147HLP-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	[2]
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	[3], [4]
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	[3], [4]

● TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



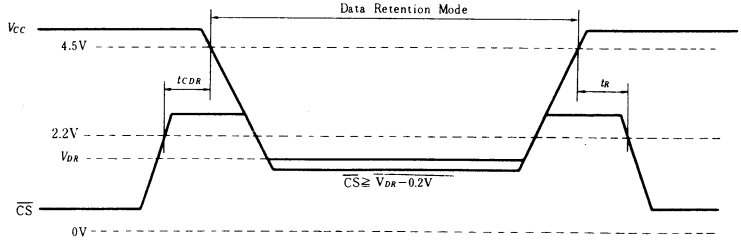
Notes:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0℃ to +70℃)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geqq 2.8V$ $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC} = Read Cycle Time.

● LOW V_{CC} DATA RETENTION WAVEFORM



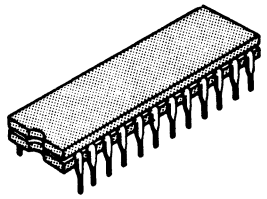
HM6116-2, HM6116-3, HM6116-4
HM6116P-2, HM6116P-3, HM6116P-4

2048-word×8-bit High Speed Static CMOS RAM

■FEATURES

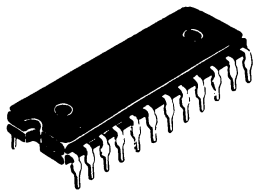
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116-2, HM6116-3, HM6116-4



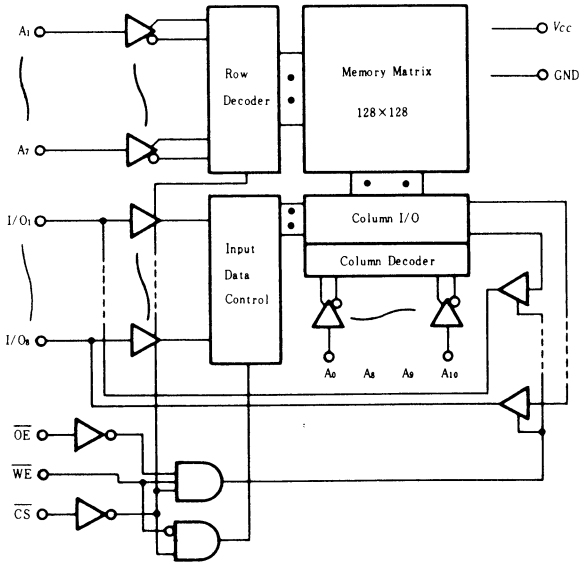
(DG-24)

HM6116P-2, HM6116P-3, HM6116P-4

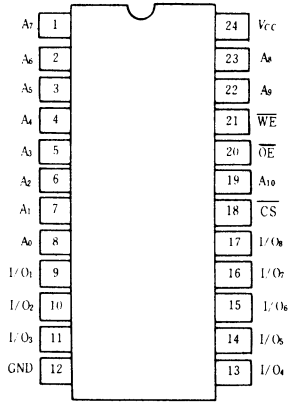


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116/P-2			HM6116/P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}-0.2V$ or $V_{in}\leq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

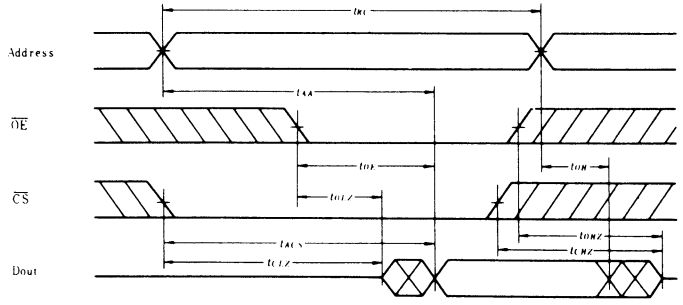
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

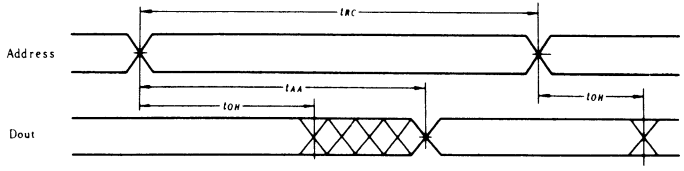
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

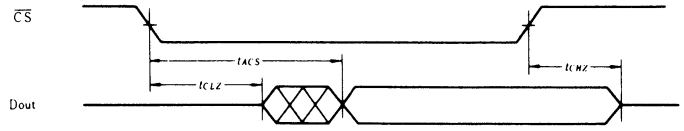
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

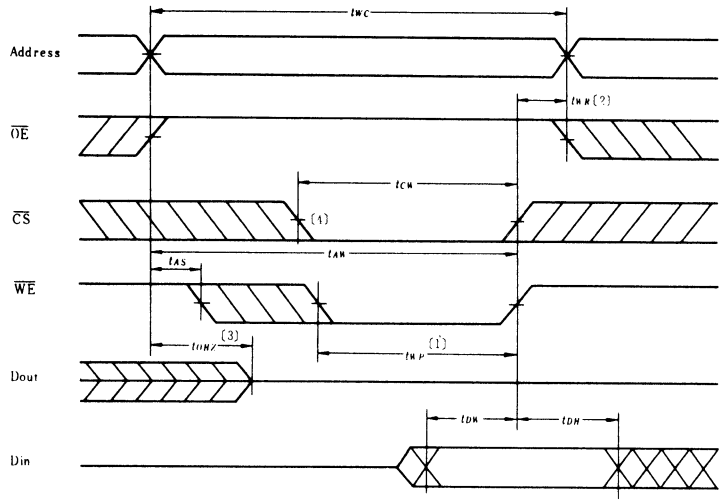


● READ CYCLE (3)[1][3][4]

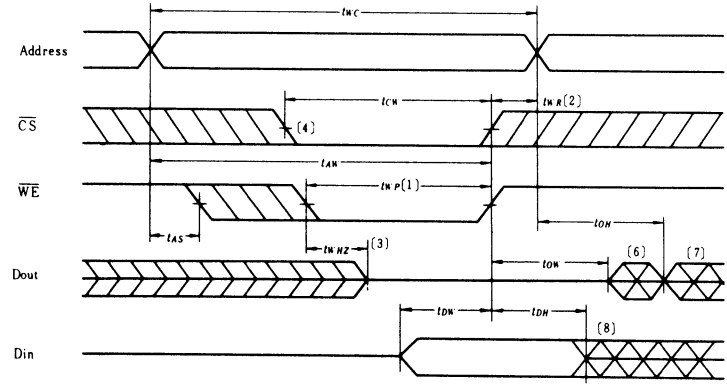


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

WRITE CYCLE (1)

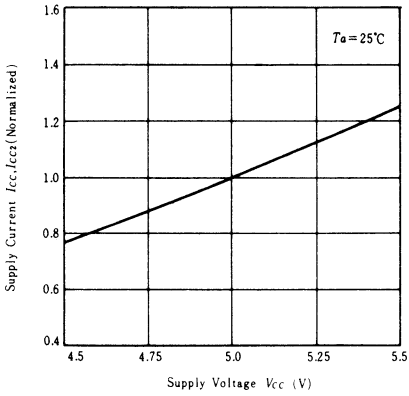


● WRITE CYCLE (2) (5)

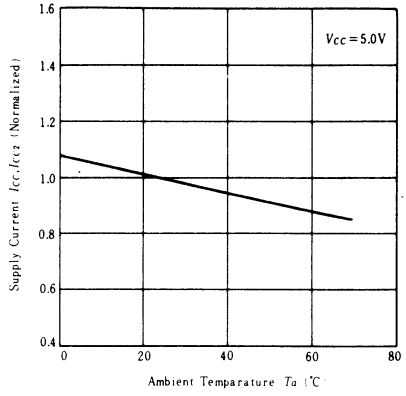


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

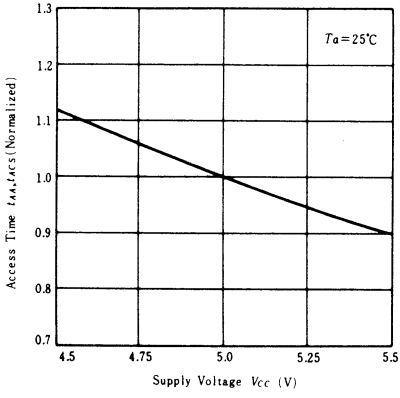
SUPPLY CURRENT vs. SUPPLY VOLTAGE



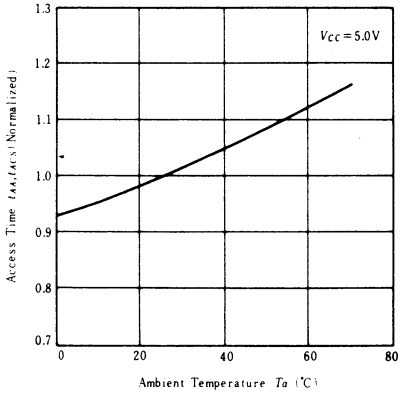
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



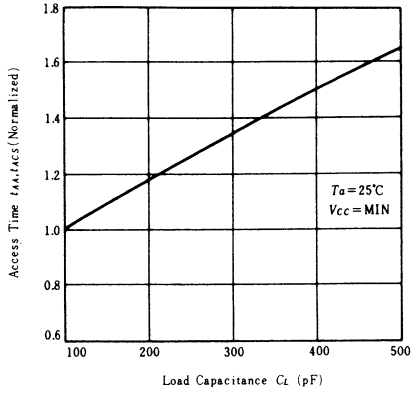
ACCESS TIME vs. SUPPLY VOLTAGE



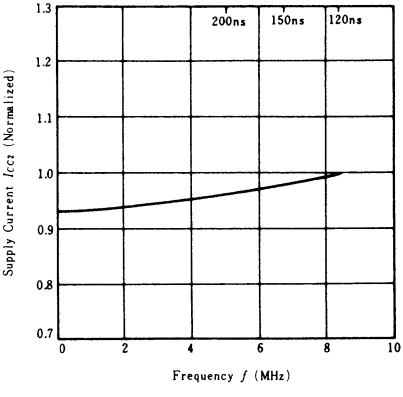
ACCESS TIME vs. AMBIENT TEMPERATURE



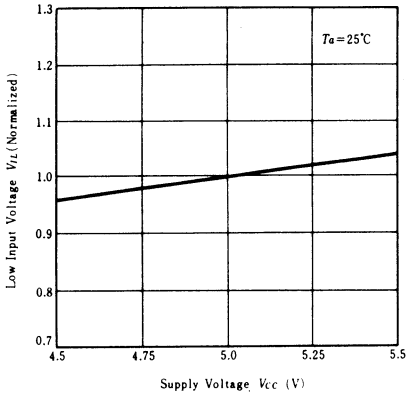
ACCESS TIME vs. LOAD CAPACITANCE



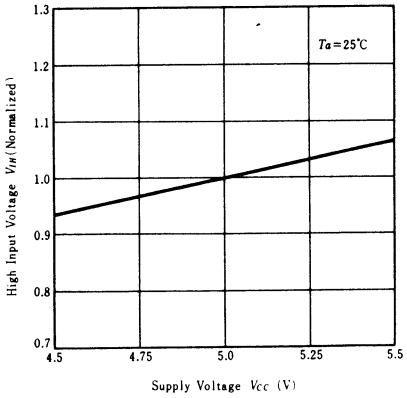
SUPPLY CURRENT vs. FREQUENCY



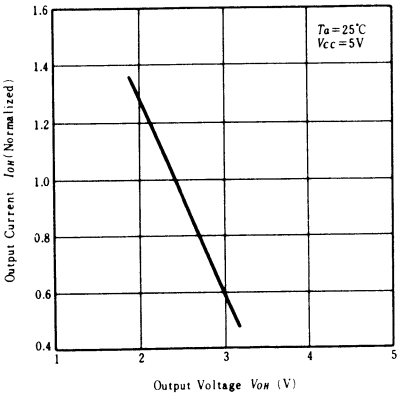
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



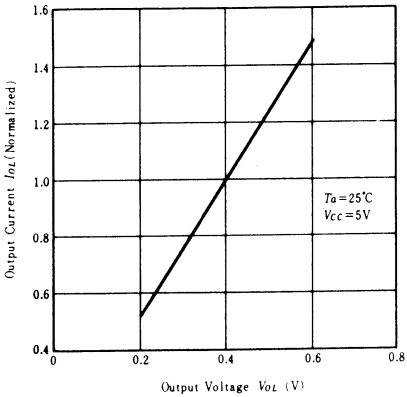
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

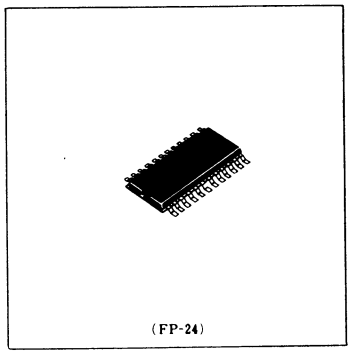


HM6116FP-2, HM6116FP-3, HM6116FP-4

2048-word×8-bit High Speed Static CMOS RAM

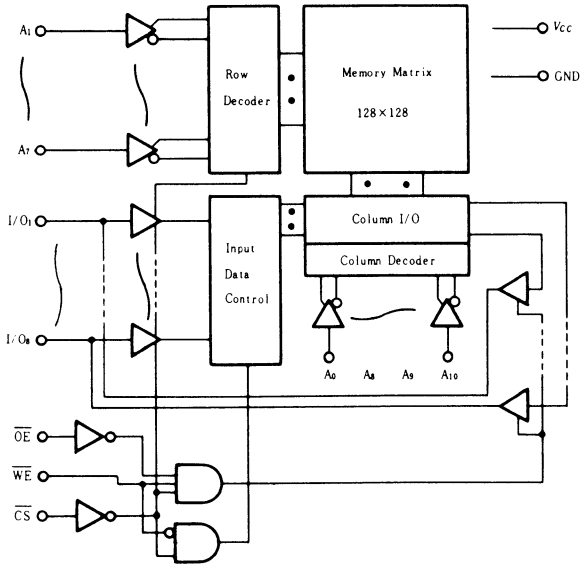
■FEATURES

- High Density Small-Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time — 120ns/150ns/200ns (max.)
- Low Power Standby — Standby: 100μW (typ.)
- Low Power Operation; — Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

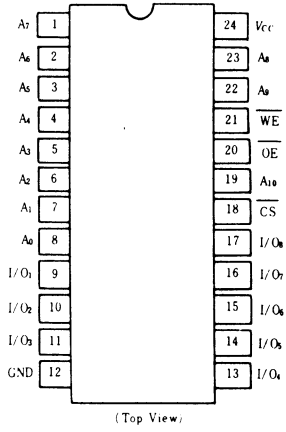


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

*Pulse Width 50ns: −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle(1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle(1)
L	L	L	Write	I_{CC}	Din	Write Cycle(2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116FP-2			HM6116FP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\geqq V_{CC}$ −0.2V or $V_{in}\leqq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

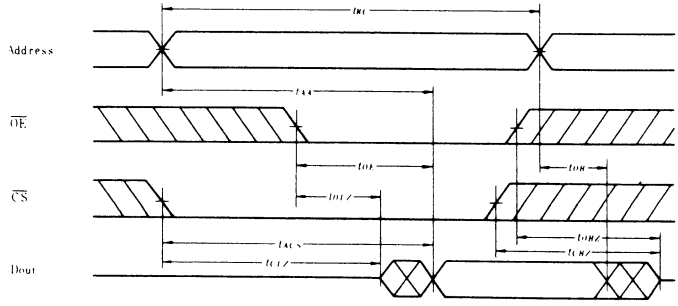
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

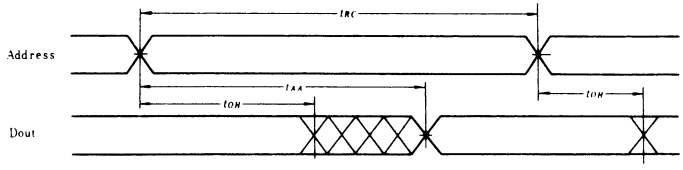
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

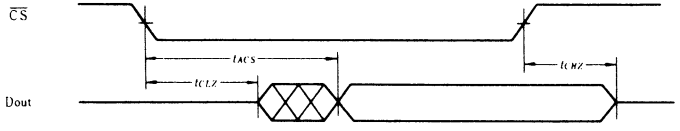
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]



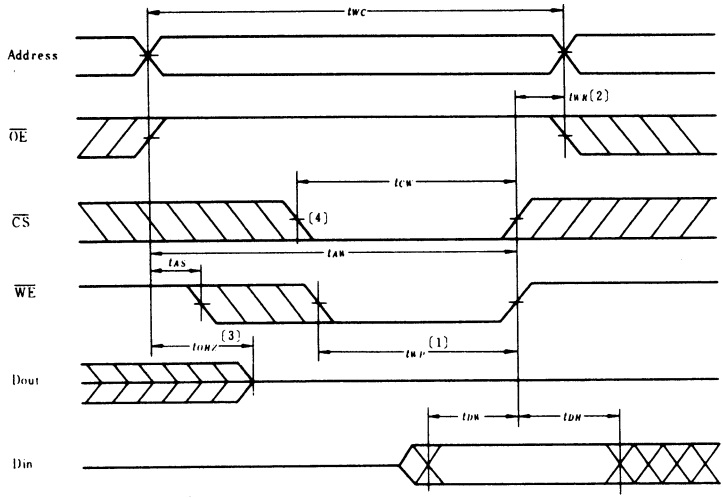
● READ CYCLE (3)[1][3][4]



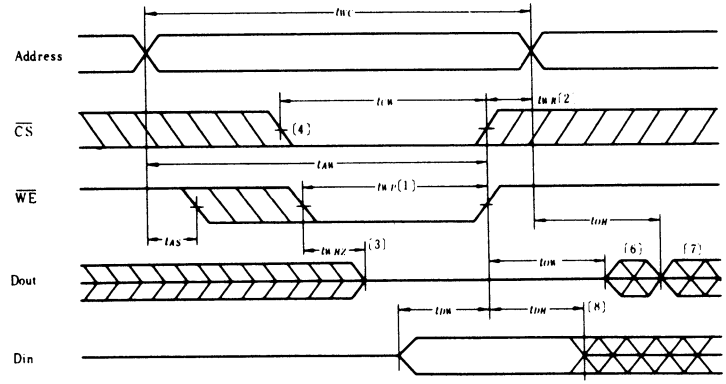
NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

■TIMING WAVEFORM

● WRITE CYCLE (1)[1]

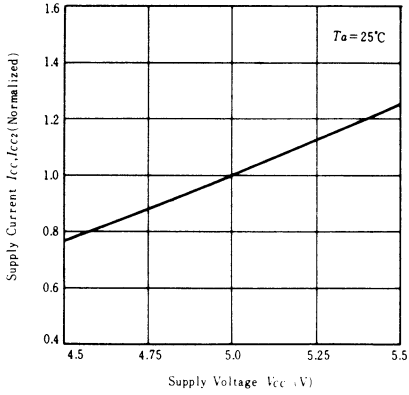


● WRITE CYCLE (2)[5]

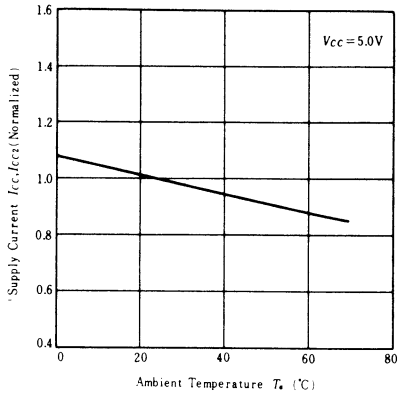


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

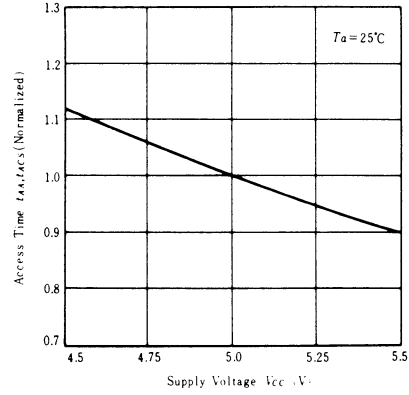
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



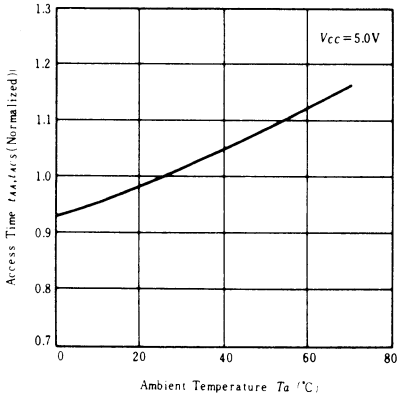
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



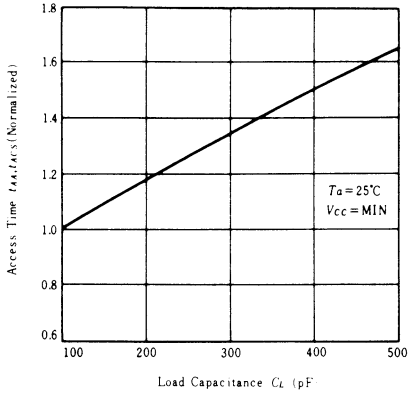
ACCESS TIME
vs. SUPPLY VOLTAGE



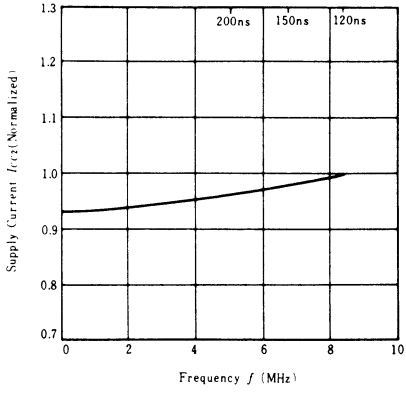
ACCESS TIME
vs. AMBIENT TEMPERATURE



ACCESS TIME
vs. LOAD CAPACITANCE



SUPPLY CURRENT
vs. FREQUENCY

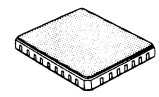


HM6116CG-2, HM6116CG-3, HM6116CG-4

2048-word×8-bit High Speed Static CMOS RAM

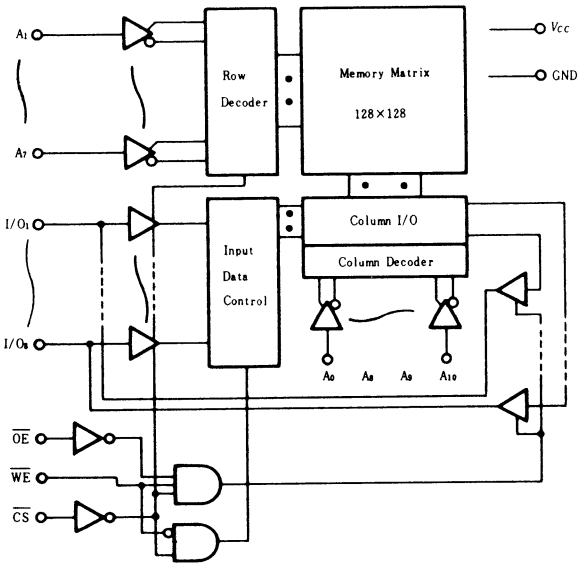
■FEATURES

- Single 5V Supply and High Density 32 pin-Leadless-Chip Carrier
- High speed. Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No Clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

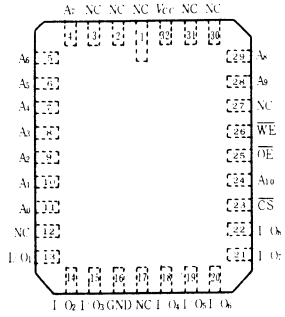


(CG-32)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to 85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116CG-2			HM6116CG-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\geqq V_{CC}-0.2V$ or $V_{in}\leqq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

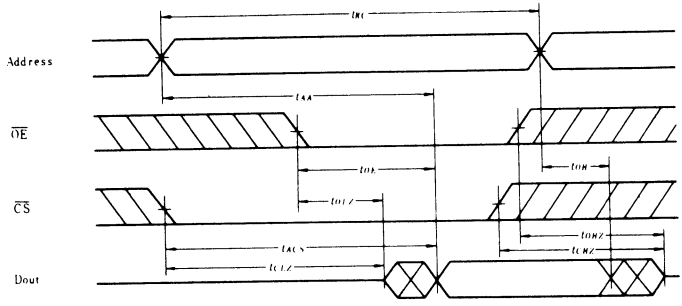
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

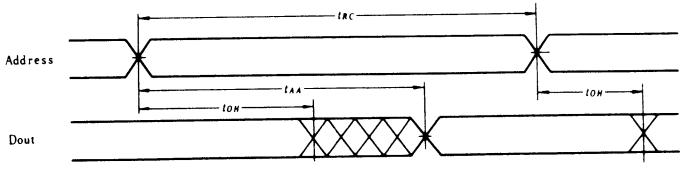
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

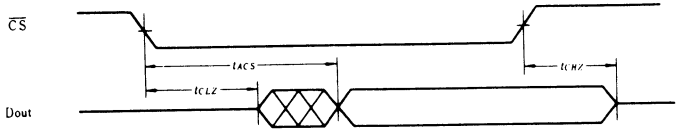
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

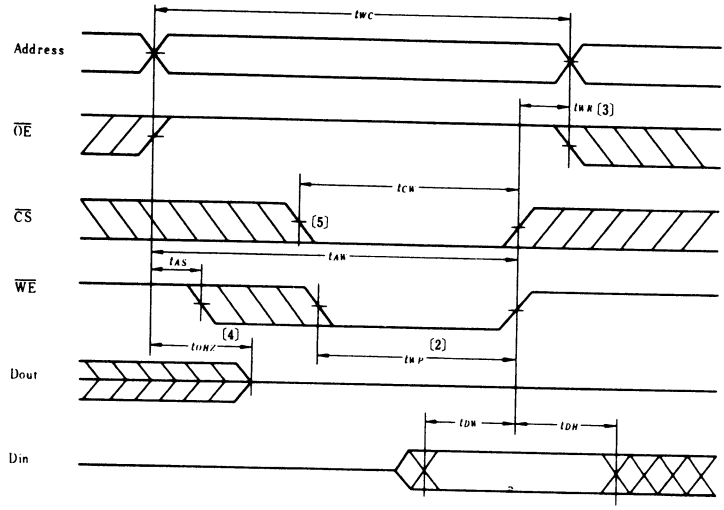


● READ CYCLE (3)[1][3][4]

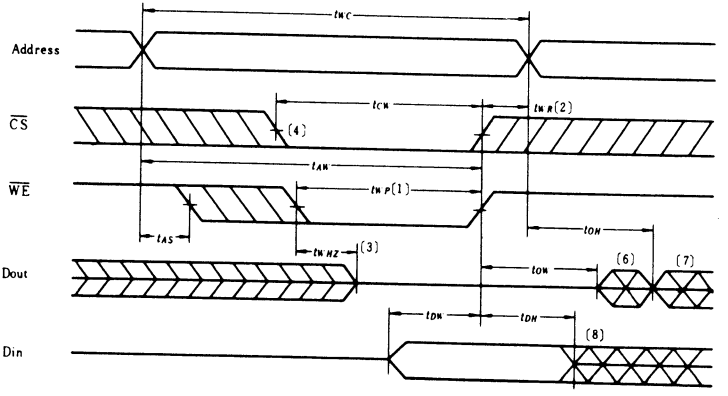


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

WRITE CYCLE (1) [1]



● WRITE CYCLE (2) [5]



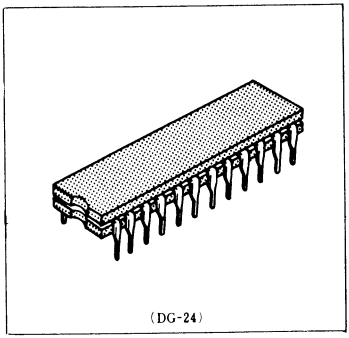
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6116L-2, HM6116L-3, HM6116L-4

2048-word × 8-bit High Speed Static CMOS RAM

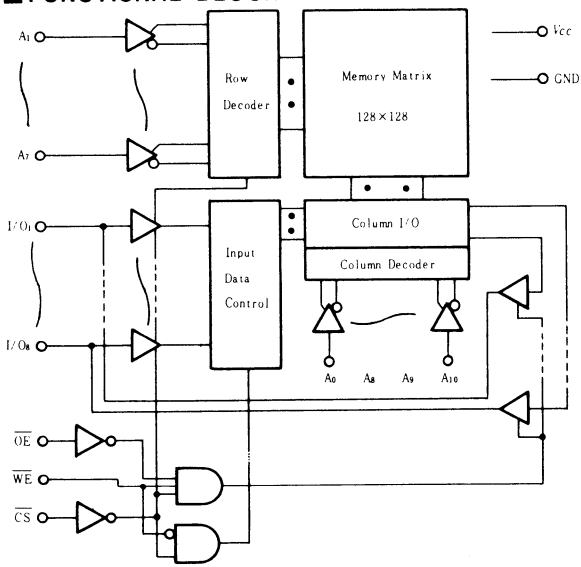
■ FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 20μW (typ.)
- Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

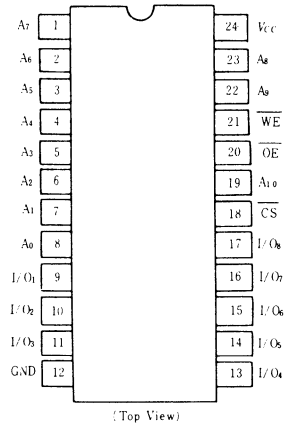


(DG-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116L-2			HM6116L-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}-0.2V$ or $V_{in}\leq 0.2V$	—	4	100	—	4	100	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

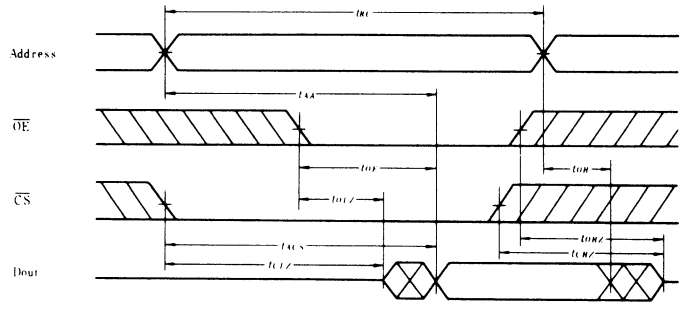
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

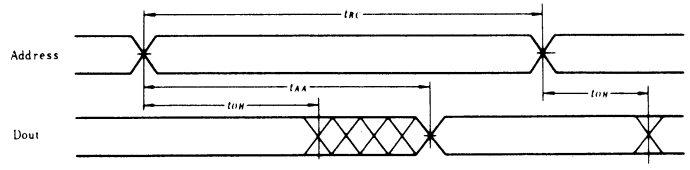
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

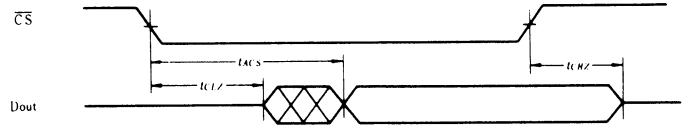
● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

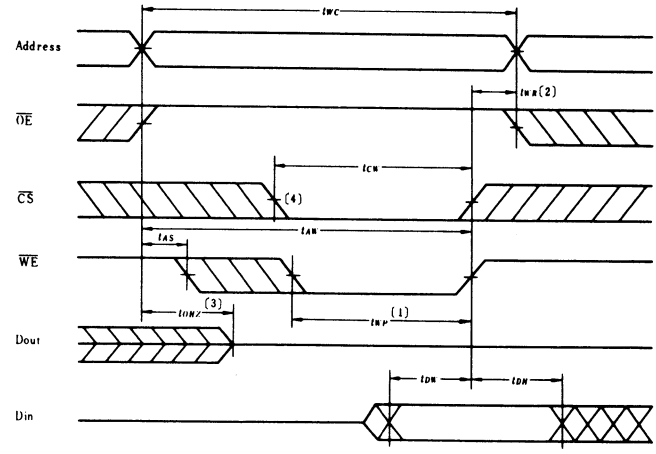


● Read Cycle (3) (1), (3), (4)

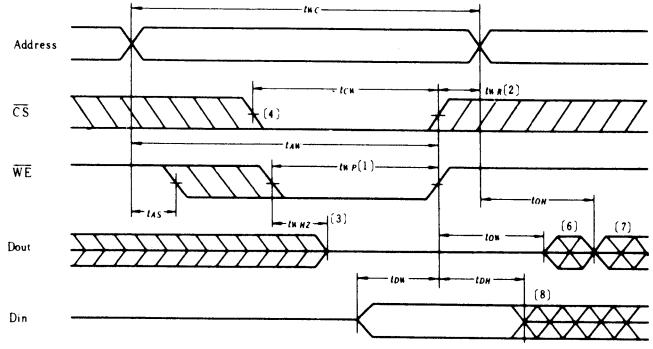


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)** (5)



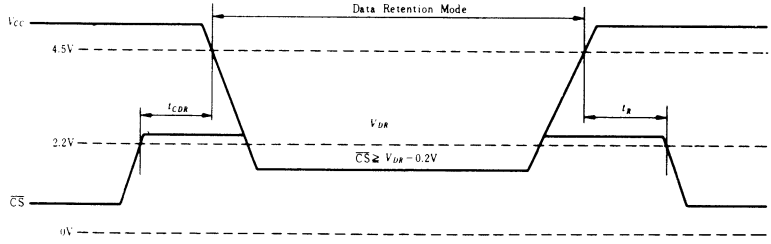
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

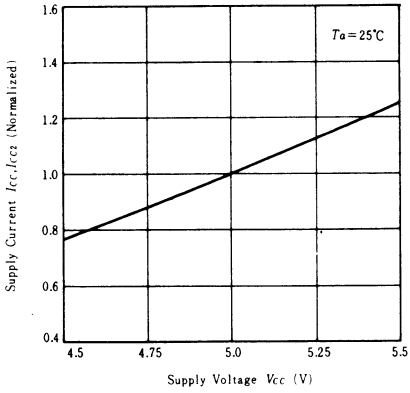
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* V_{IL}=−0.3V min.
** t_{RC}=Read Cycle Time.

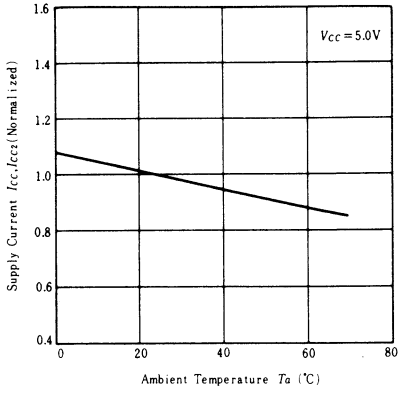
● **Low Vcc Data Retention Waveform**



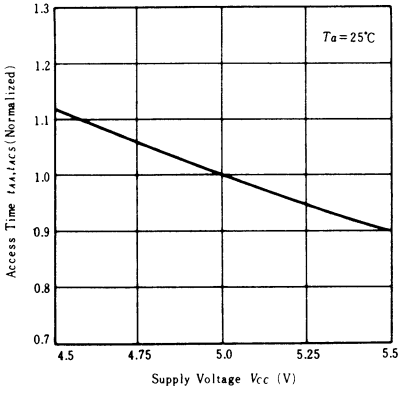
SUPPLY CURRENT vs. SUPPLY VOLTAGE



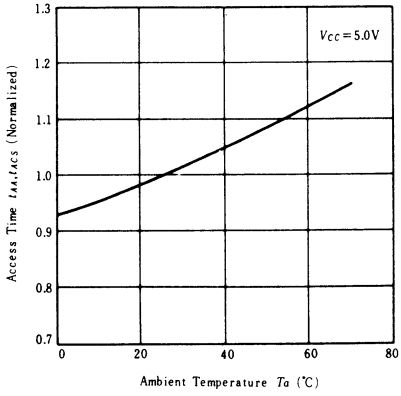
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



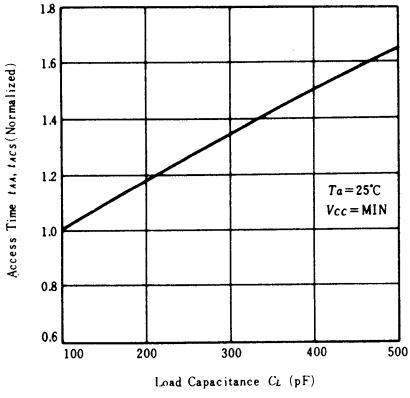
ACCESS TIME vs. SUPPLY VOLTAGE



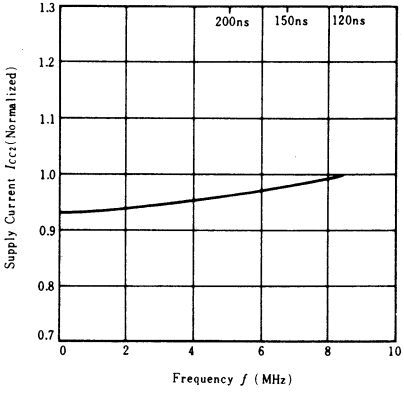
ACCESS TIME vs. AMBIENT TEMPERATURE



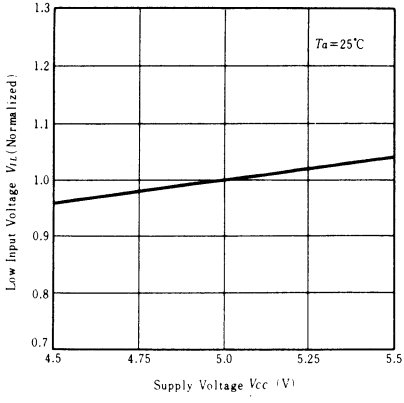
ACCESS TIME vs. LOAD CAPACITANCE



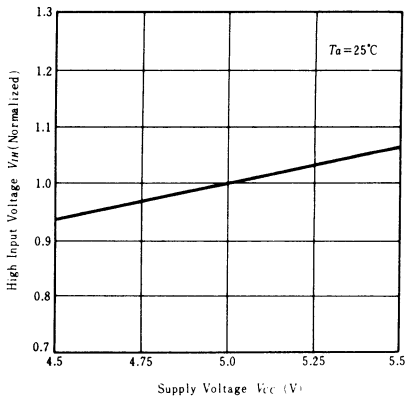
SUPPLY CURRENT vs. FREQUENCY



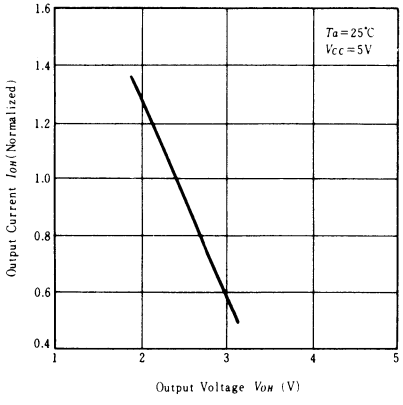
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



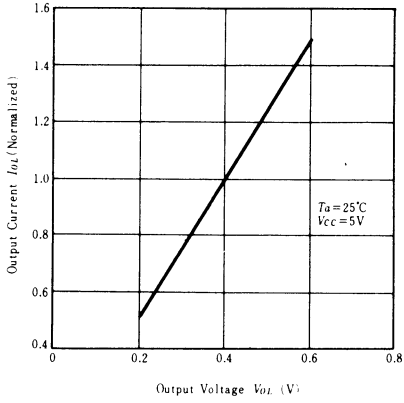
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



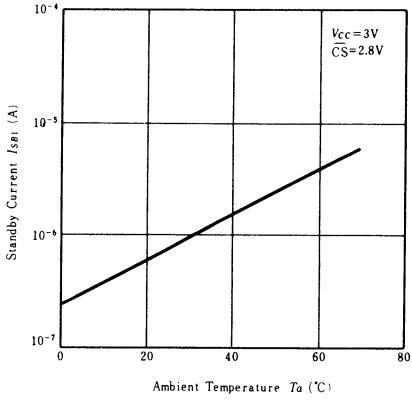
OUTPUT CURRENT vs. OUTPUT VOLTAGE



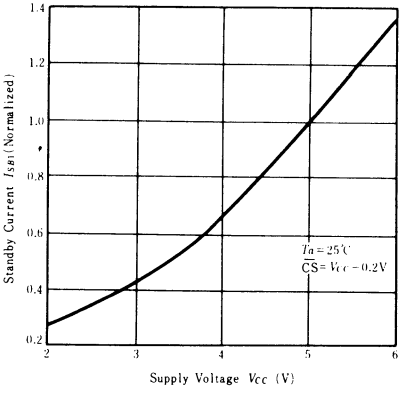
OUTPUT CURRENT vs. OUTPUT VOLTAGE



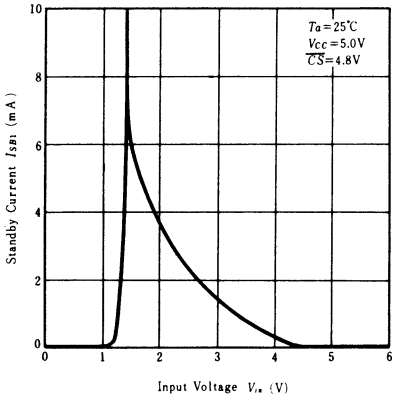
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

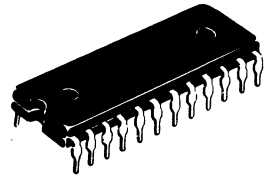


HM6116LP-2, HM6116LP-3, HM6116LP-4

2048-word × 8-bit High Speed Static CMOS RAM

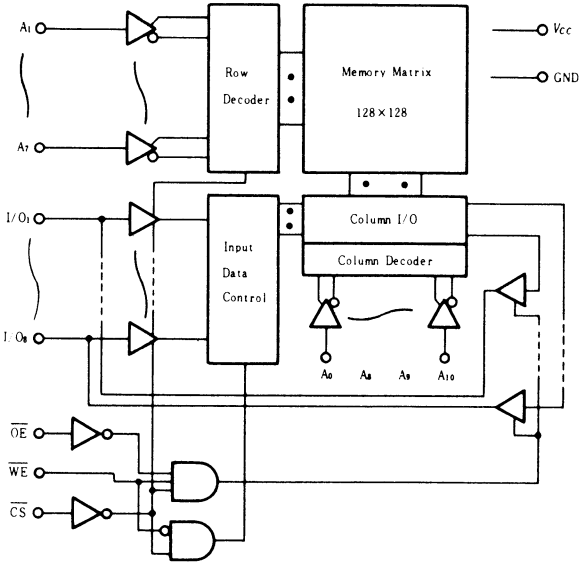
■ FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

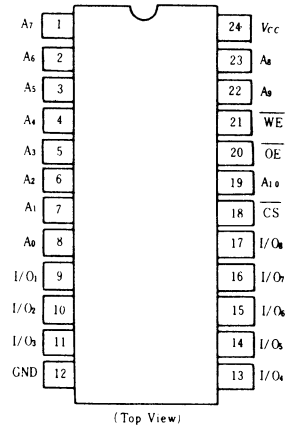


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\geqq V_{CC}-0.2V$ or $V_{in}\leqq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

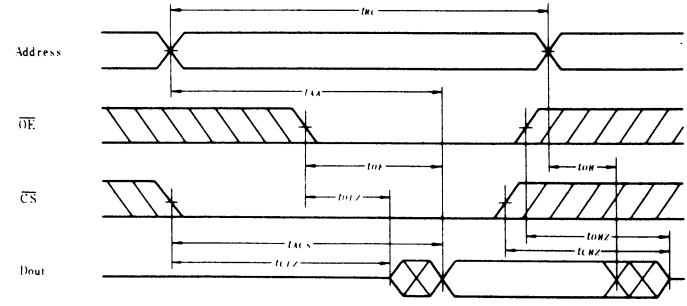
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

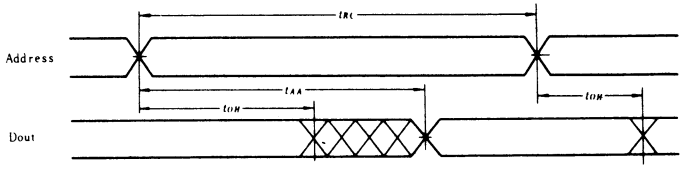
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

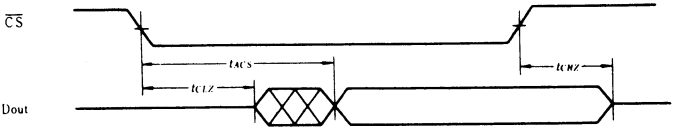
● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

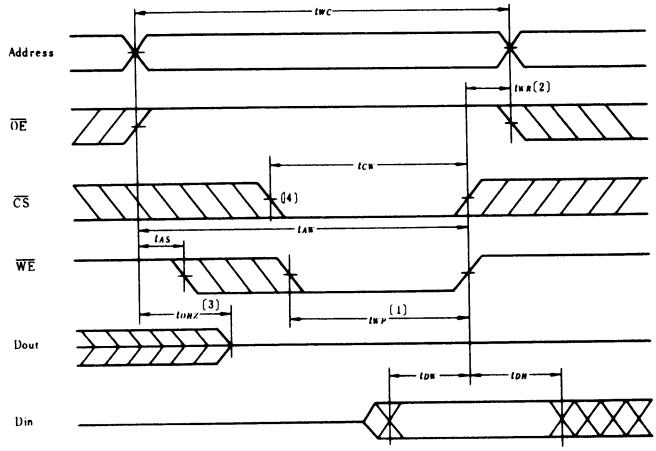


● Read Cycle (3) (1), (3), (4)

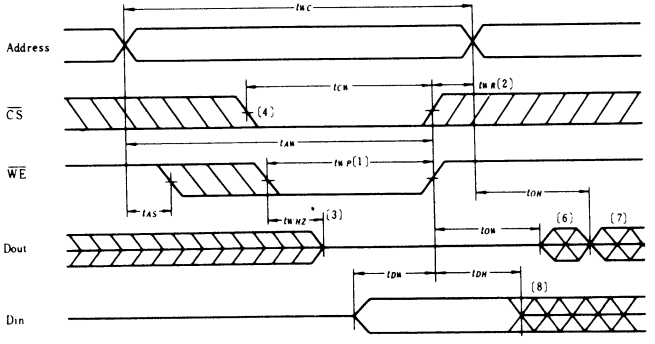


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)** (5)



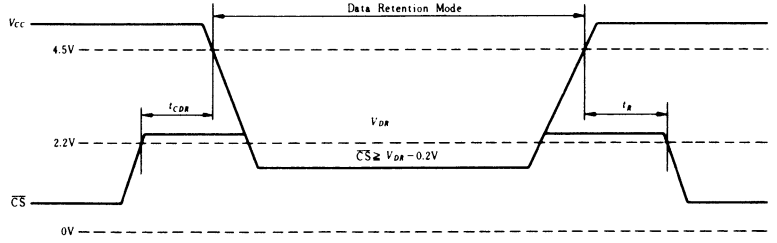
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

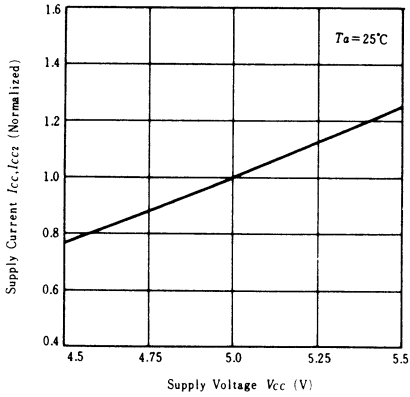
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* 10 μA max at $Ta = 0°C$ to $+40°C$, V_{IH} min = −0.3V
** t_{RC} = Read Cycle Time.

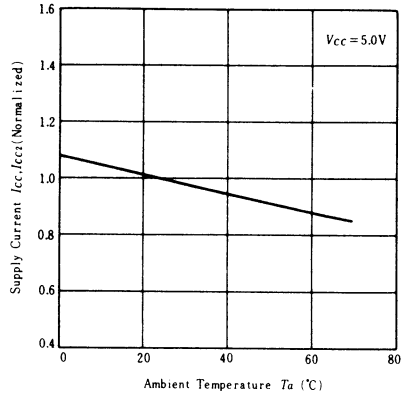
● **Low Vcc Data Retention Waveform**



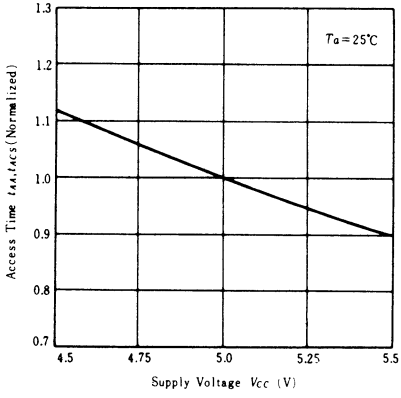
SUPPLY CURRENT vs. SUPPLY VOLTAGE



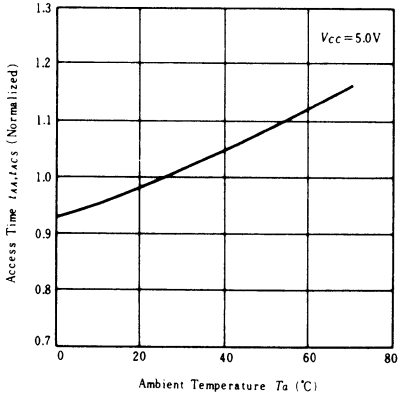
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



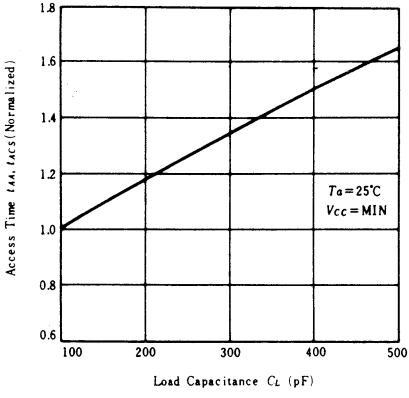
ACCESS TIME vs. SUPPLY VOLTAGE



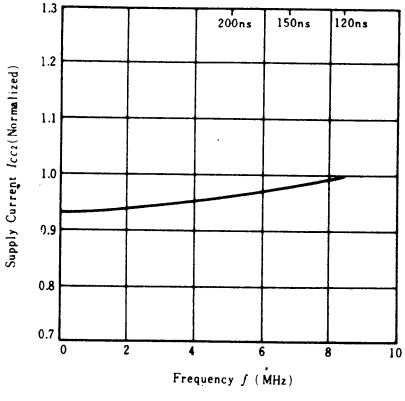
ACCESS TIME vs. AMBIENT TEMPERATURE



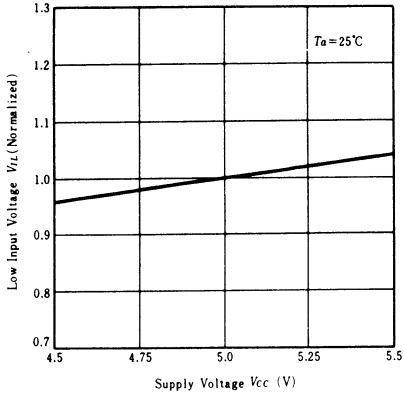
ACCESS TIME vs. LOAD CAPACITANCE



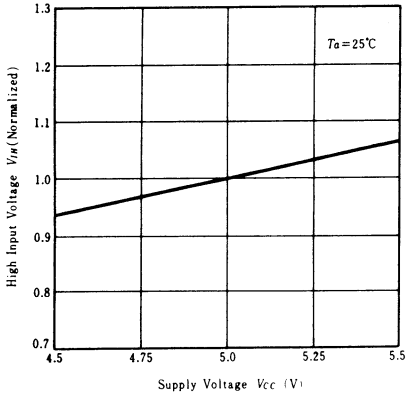
SUPPLY CURRENT vs. FREQUENCY



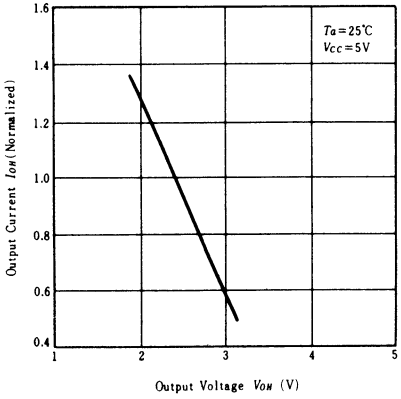
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



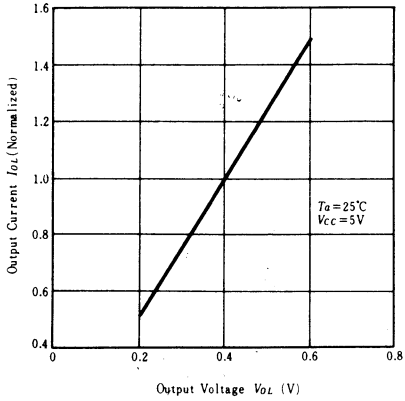
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



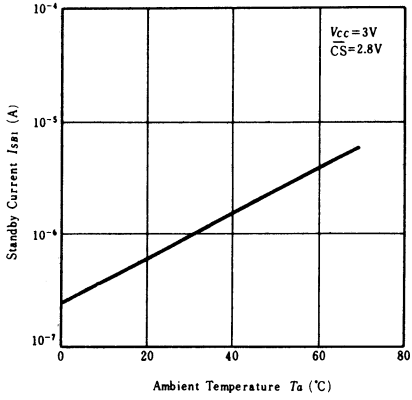
OUTPUT CURRENT vs. OUTPUT VOLTAGE



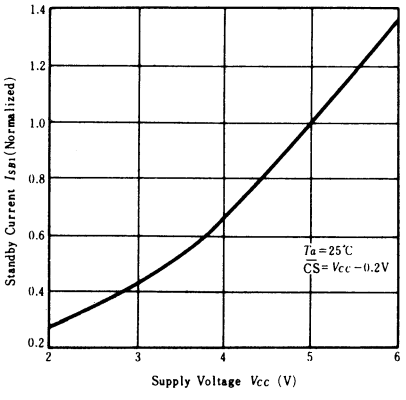
OUTPUT CURRENT vs. OUTPUT VOLTAGE



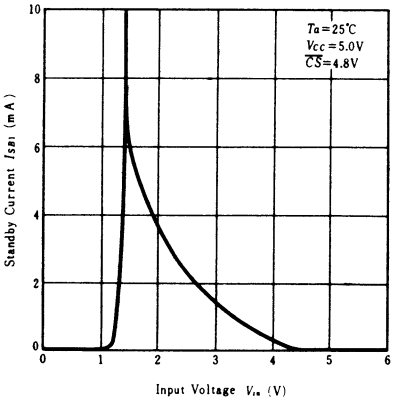
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

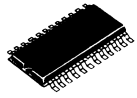


HM6116LFP-2, HM6116LFP-3, HM6116LFP-4

2048-word×8-bit High Speed Static CMOS RAM

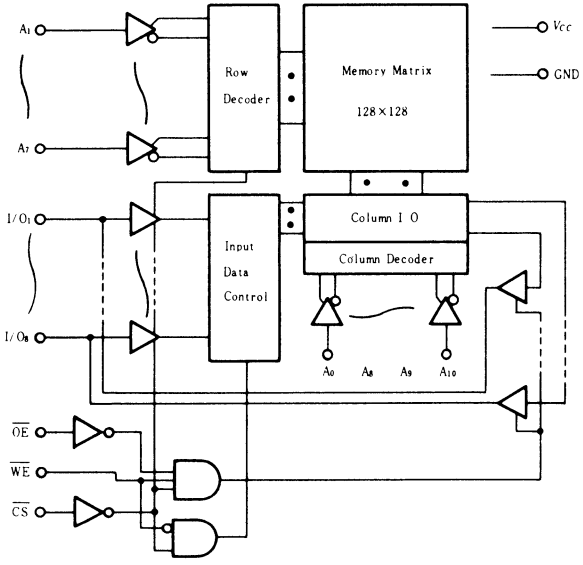
■FEATURES

- High Density Small-sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time — 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; — Standby: 10μW (typ.), Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

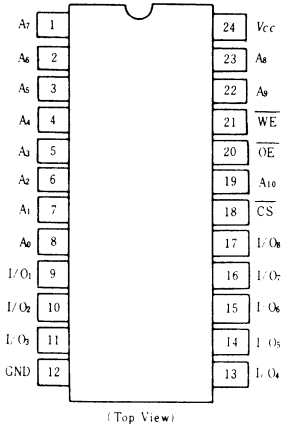


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns: −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min= −0.3V.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116LFP-2			HM6116LFP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Currnnt	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	Min cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\geqq V_{CC}-0.2V$ or $V_{in}\leqq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

●WRITE CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

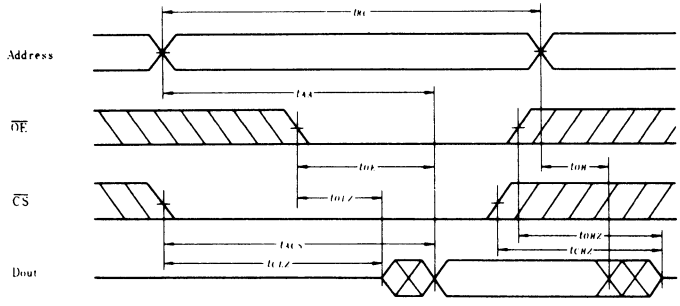
■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	Vin=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

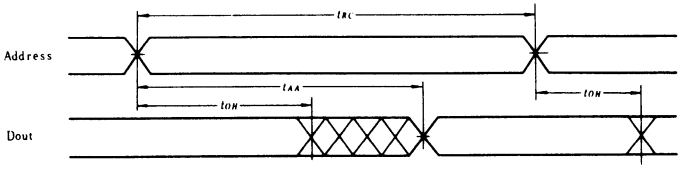
Note) This parameter is sampled and not 100% tested.

■TIMING WAVEFORM

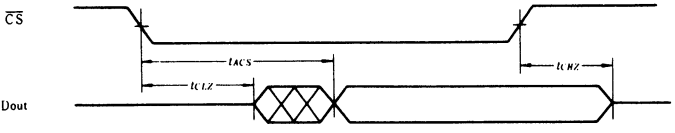
●READ CYCLE (1)[1]



●READ CYCLE (2)[1][2][4]

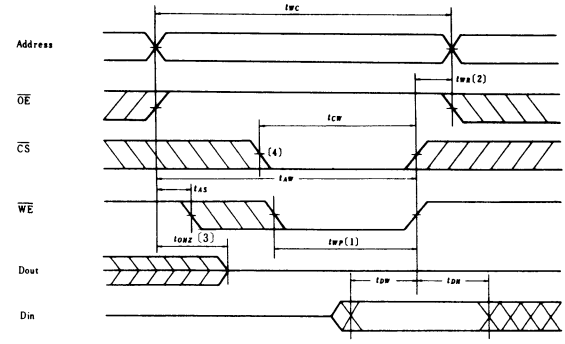


●READ CYCLE (3)[1][3][4]

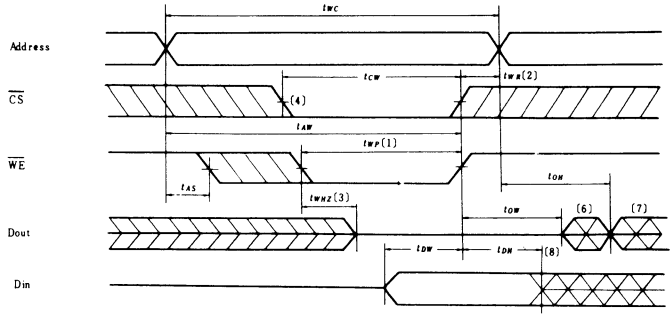


NOTES: 1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected, $\overline{CS}$ = V_{IL}
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

●WRITE CYCLE (1)



●WRITE CYCLE (2) [5]



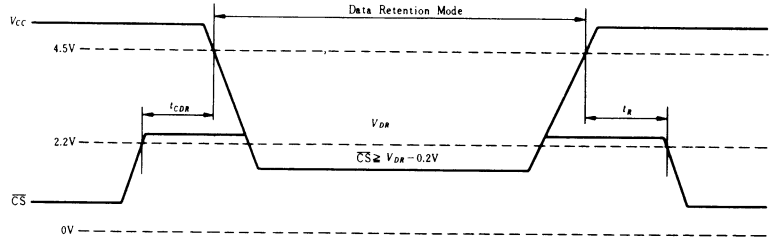
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$ $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		**t_{RC}	—	—	ns

* V_{IL} min=−0.3V, 10 μA max (at Ta=0 to +40°C)
** t_{RC}=Read Cycle Time.

●Low V_{CC} DATA RETENTION WAVEFORM



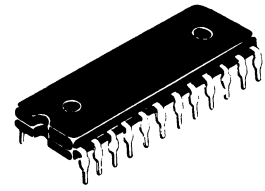
HM6116AP-12, HM6116AP-15, HM6116AP-20, HM6116ASP-12, HM6116ASP-15, HM6116ASP-20

2048-word × 8-bit High Speed Static CMOS RAM

■ FEATURES

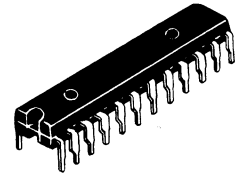
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation — Standby: 100μW (typ.); Operation: 15mW (typ.) (f = 1MHz)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116AP Series



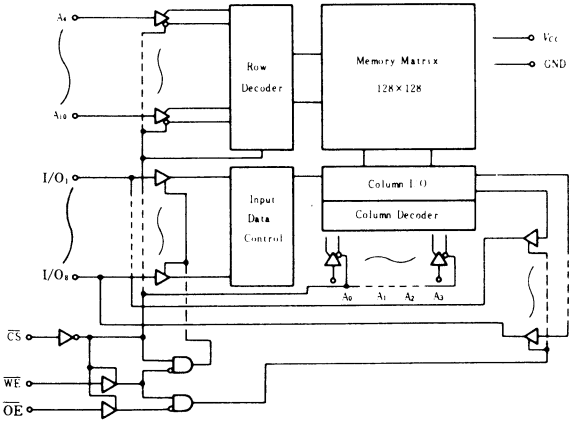
(DP-24)

HM6116ASP Series

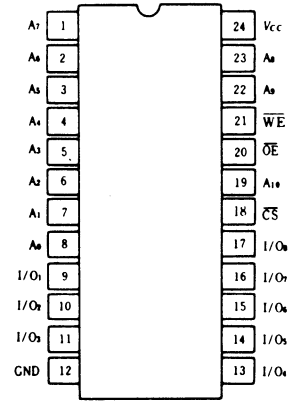


(DP-24A)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = 0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116AP/ASP-12			HM6116AP/ASP-15			HM6116AP/ASP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in} =GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	CS=V_{IH} or OE=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	CS=V_{IL}, $I_{I/O}$=0mA V_{in}=V_{IH} or V_{IL}	—	5	15	—	5	15	—	5	15	mA
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V, CS=V_{IL}, $I_{I/O}$=0mA, f=1MHz	—	3	6	—	3	6	—	3	6	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	—	35	60	—	25	45	—	20	35	mA
Standby Power Supply Current	I_{SB}	CS=V_{IH}	—	1	4	—	1	4	—	1	4	mA
	I_{SB1}	CS≧V_{CC} −0.2V	—	0.02	2	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL} =4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, T_a=25°C

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116AP/ASP-12		HM6116AP/ASP-15		HM6116AP/ASP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	55	—	60	—	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	20	—	ns

● WRITE CYCLE

Item	Symbol	HM6116AP/ ASP-12		HM6116AP/ ASP-15		HM6116AP/ ASP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

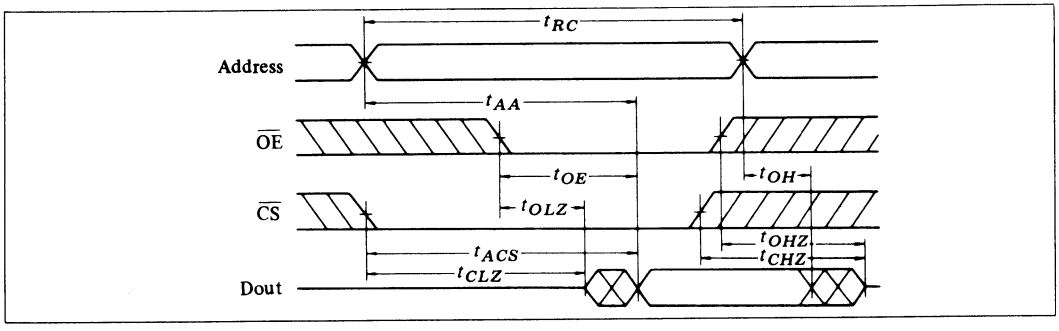
■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

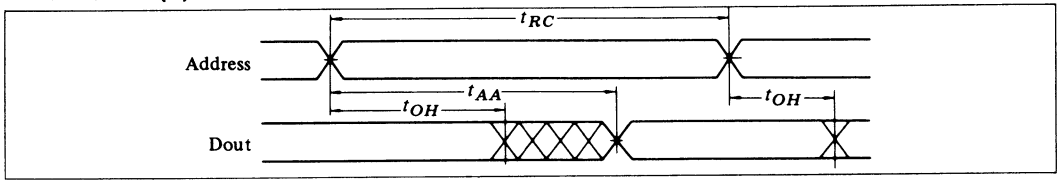
Note) This parameter is sampled and not 100% tested.

■TIMING WAVEFORM

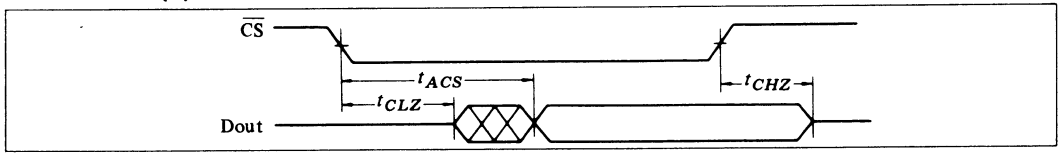
●READ CYCLE (1)[1]



●READ CYCLE (2)[1][2][4]

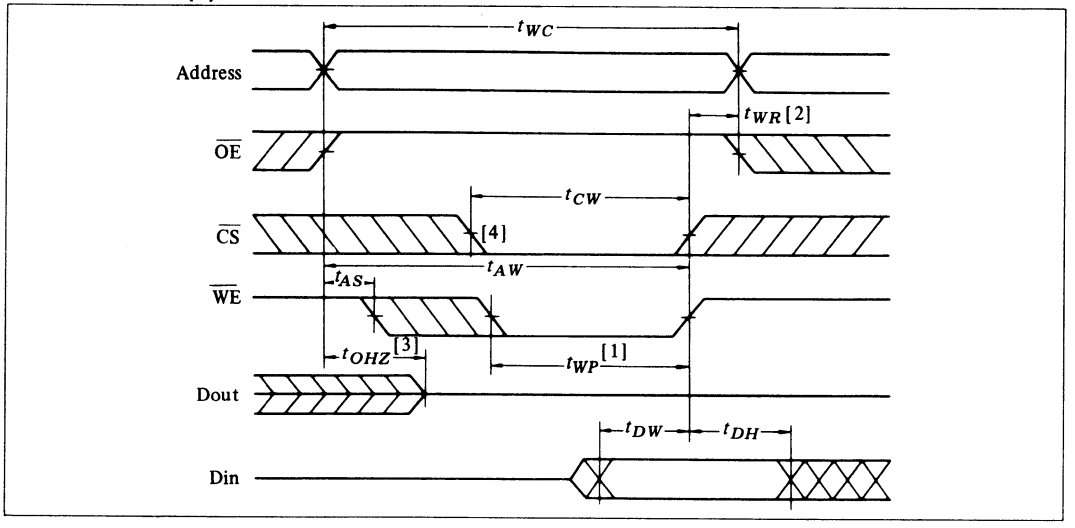


●READ CYCLE (3)[1][3][4]

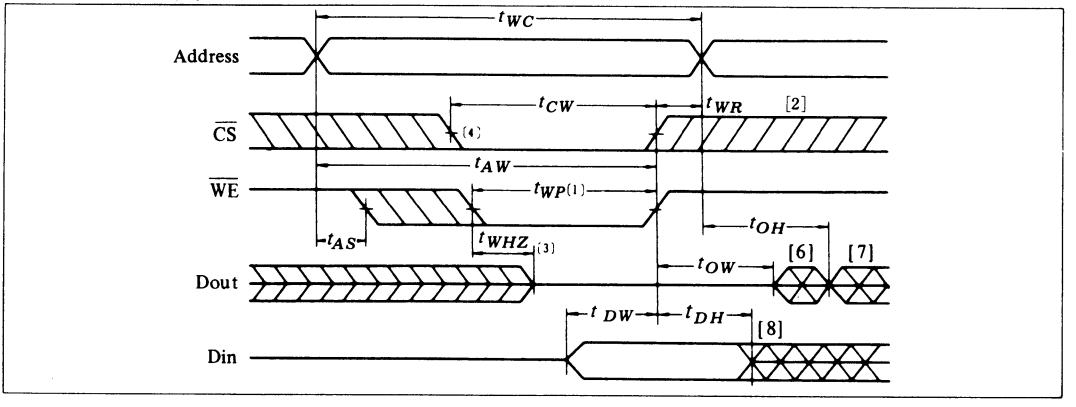


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● WRITE CYCLE(1)



● WRITE CYCLE (2)[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

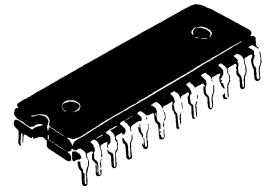
HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20

2048-word × 8-bit High Speed Static CMOS RAM

■ FEATURES

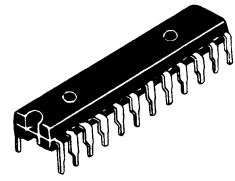
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 5μW (typ.) Operation: 10mW (typ.) (f = 1MHz)
- Capability of Battery Back up Operation
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116ALP Series



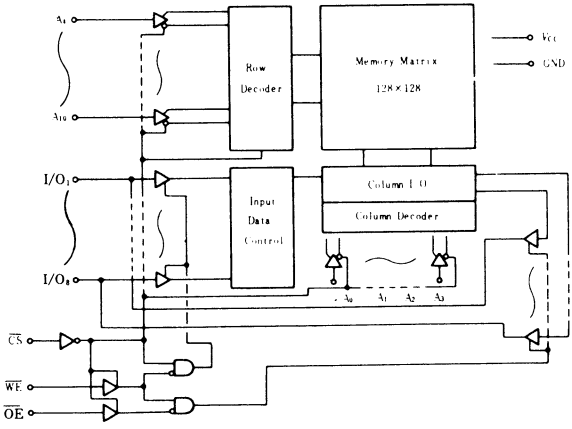
(DP-24)

HM6116ALSP Series

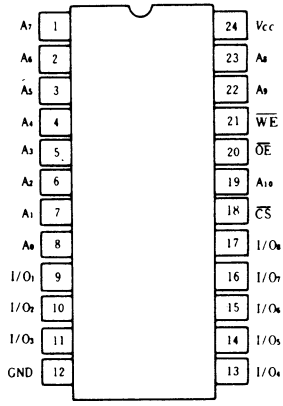


(DP-24A)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116ALP/ ALSP-12			HM6116ALP/ ALSP-15			HM6116ALP/ ALSP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	CS=V_{IH} or OE=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	CS=V_{IL}, $I_{I/O}$=0mA V_{in}=V_{IH} or V_{IL}	—	4	12	—	4	12	—	4	12	mA
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V CS=V_{IL}, $I_{I/O}$=0mA, f=1MHz	—	2	5	—	2	5	—	2	5	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	—	30	50	—	20	40	—	15	30	mA
Standby Power Supply Current	I_{SB}	CS=V_{IH}	—	0.5	3	—	0.5	3	—	0.5	3	mA
	I_{SB1}	CS≧V_{CC} −0.2V	—	1	50	—	1	50	—	1	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}= −1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, T_a=25°C

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	55	—	60	—	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	20	—	ns

● WRITE CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WOH}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

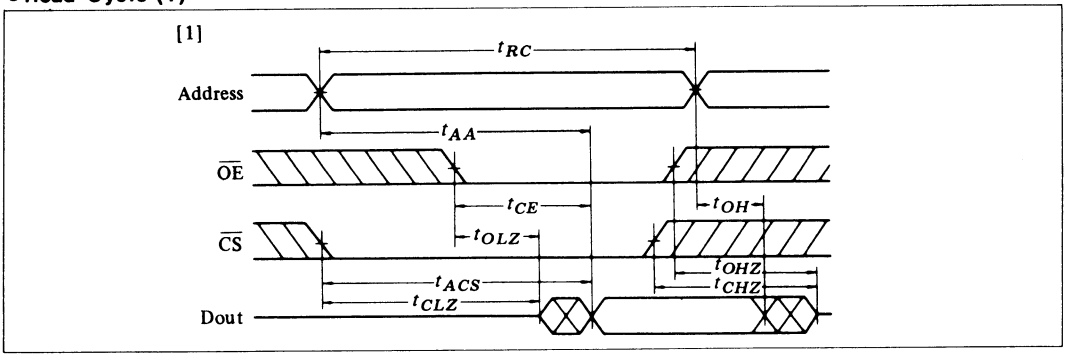
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

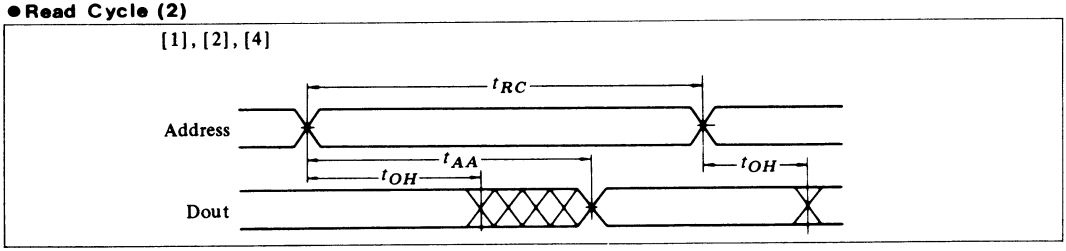
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

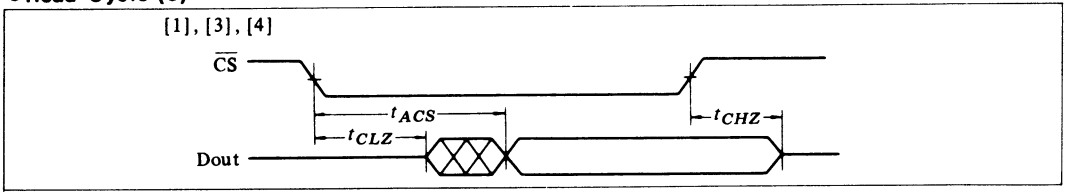
● Read Cycle (1)



● Read Cycle (2)

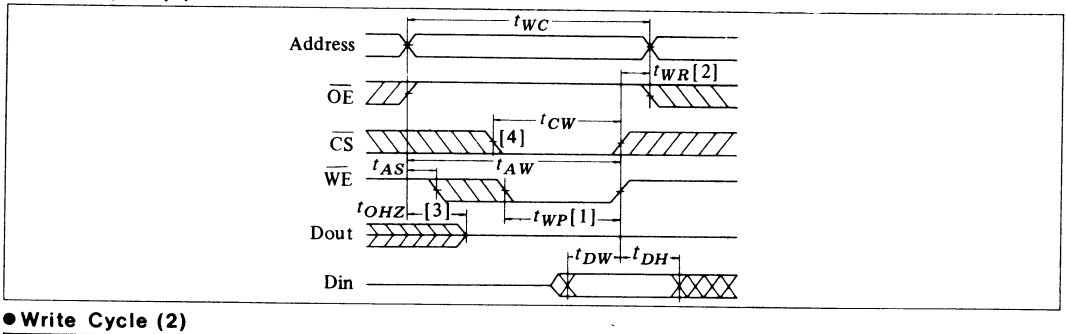


● Read Cycle (3)

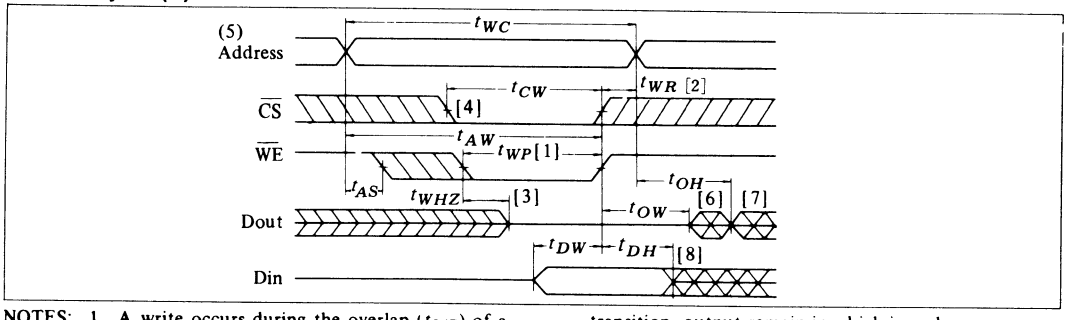


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)**



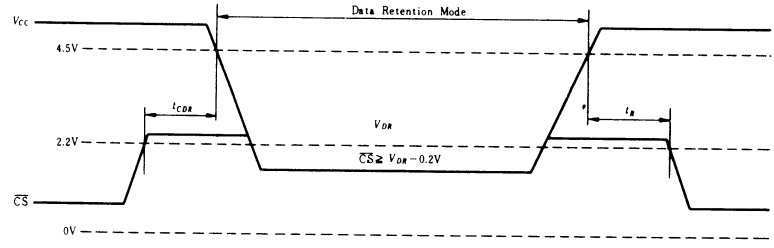
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC} = 3.0V, $\overline{CS} \geq 2.8V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

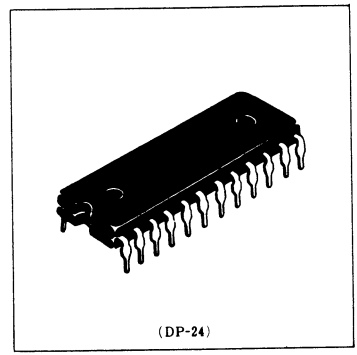
* 10 μA max at Ta = 0°C to +40°C, V_{IH} min = −0.3V
** t_{RC} = Read Cycle Time.

● **Low Vcc Data Retention Waveform**



HM6117P-3, HM6117P-4

2048-word×8-bit High Speed Static CMOS RAM

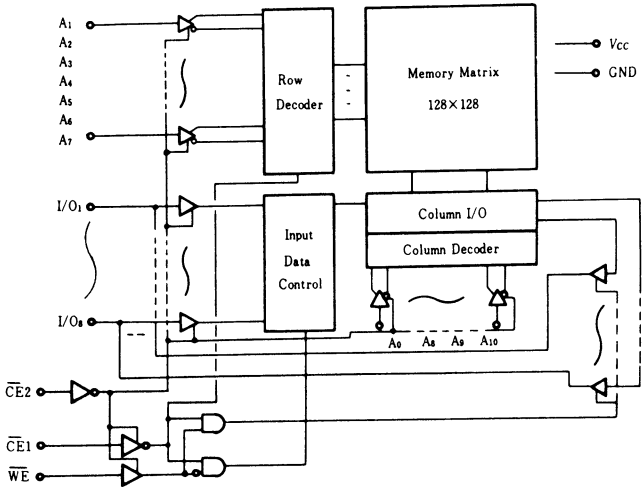


(DP-24)

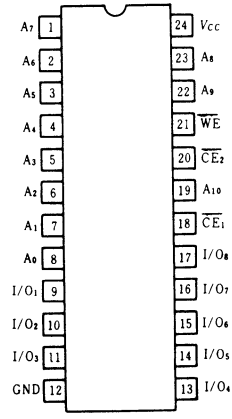
■FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time — 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse width 50ns : −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

HITACHI

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width: 50ns, DC: $V_{IL_{min}}$ = −0.3V

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	40	80	mA
Standby Power Supply Current (1): DC	I_{CCL1}*	$\overline{CE_1}\geqq V_{CC}-0.2V$, $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2): DC	I_{CCL2}*	$\overline{CE_2}\geqq V_{CC}-0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes: 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) *: $V_{IL_{min}}$=−0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

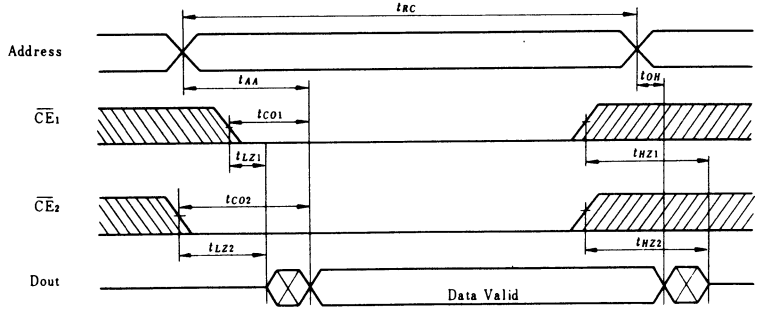
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1 TTL Gate and C_L=100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

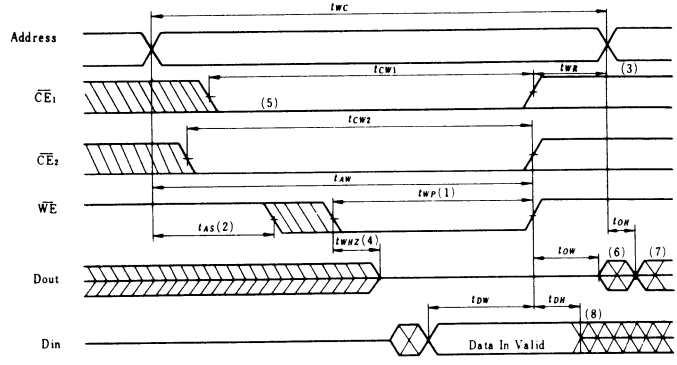


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE_2}$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

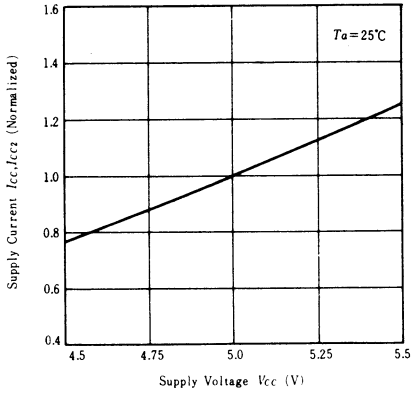
● TIMING WAVEFORM OF WRITE CYCLE



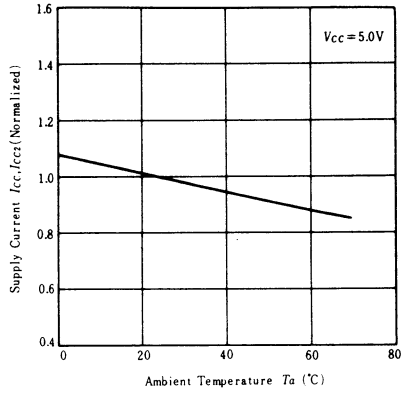
NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$.

2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

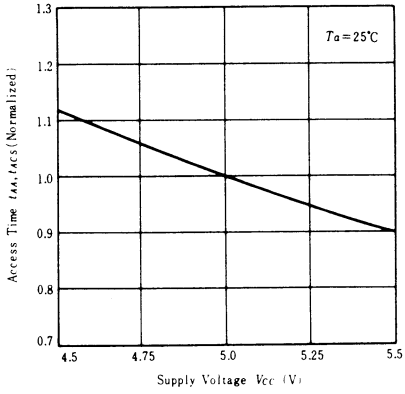
SUPPLY CURRENT vs. SUPPLY VOLTAGE



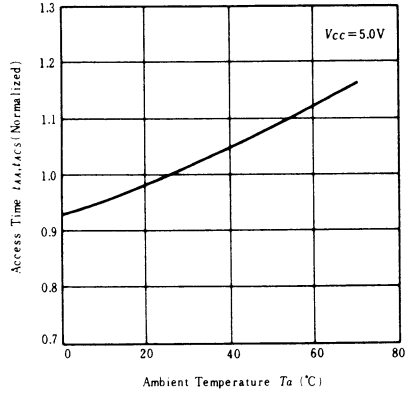
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



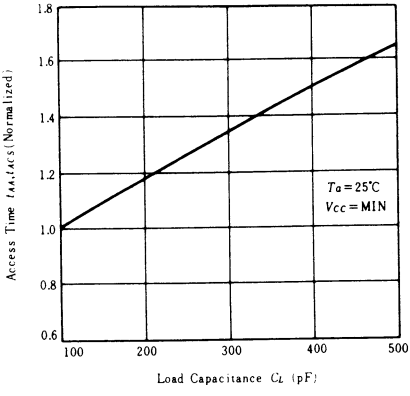
ACCESS TIME vs. SUPPLY VOLTAGE



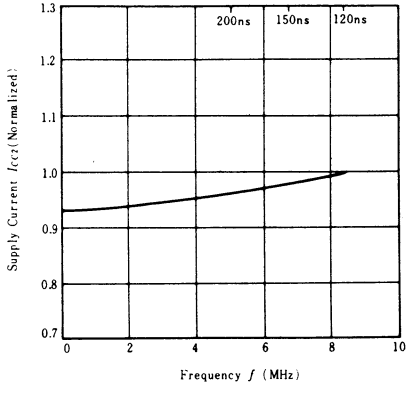
ACCESS TIME vs. AMBIENT TEMPERATURE



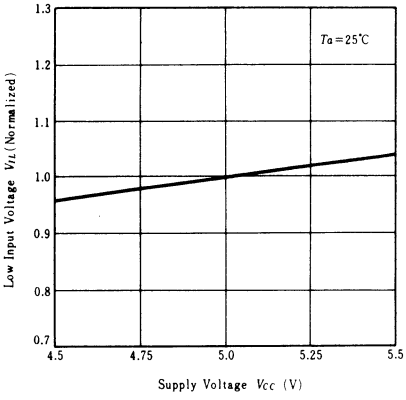
ACCESS TIME vs. LOAD CAPACITANCE



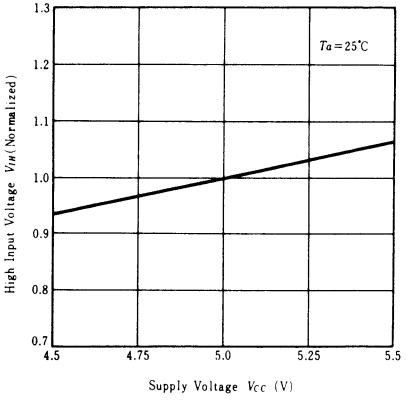
SUPPLY CURRENT vs. FREQUENCY



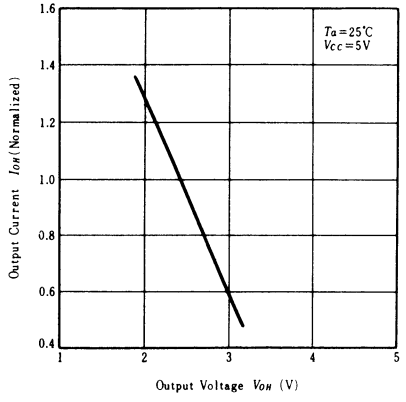
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



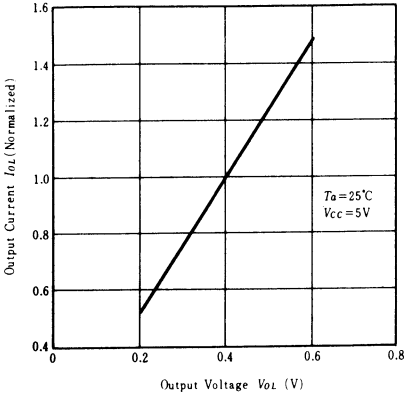
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

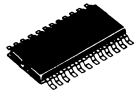


HM6117FP-3, HM6117FP-4

2048-word×8-bit High Speed Static CMOS RAM

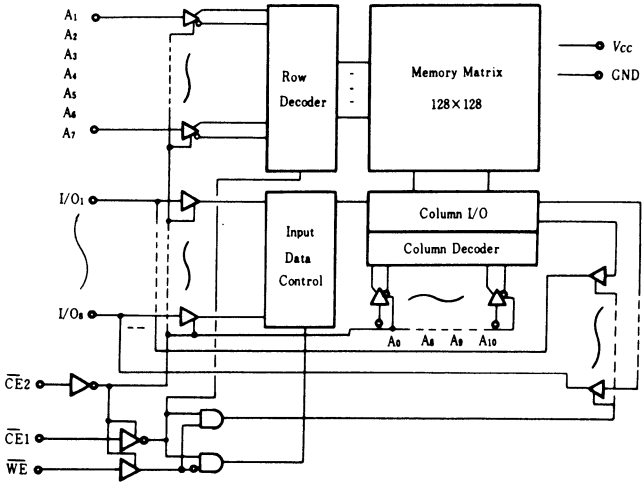
■FEATURES

- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

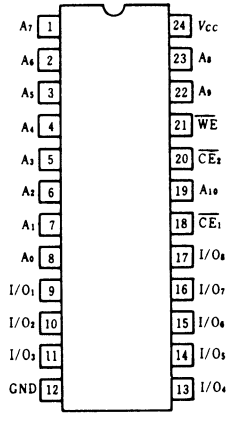


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse width 50ns: −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width : 50ns, DC : $V_{IL_{min}}$ = −0.3V

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	40	80	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1} \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2} \geqq V_{CC}-0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) * : $V_{IL_{min}}$=−0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

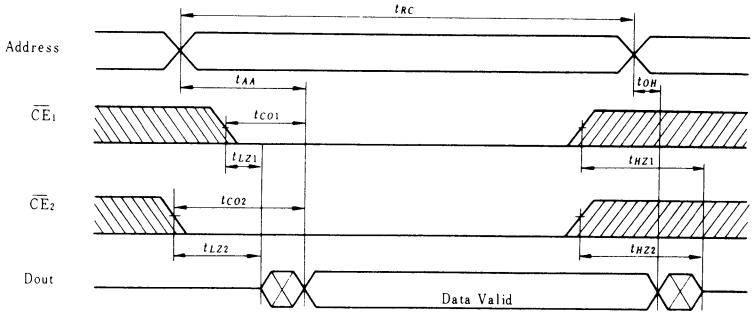
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

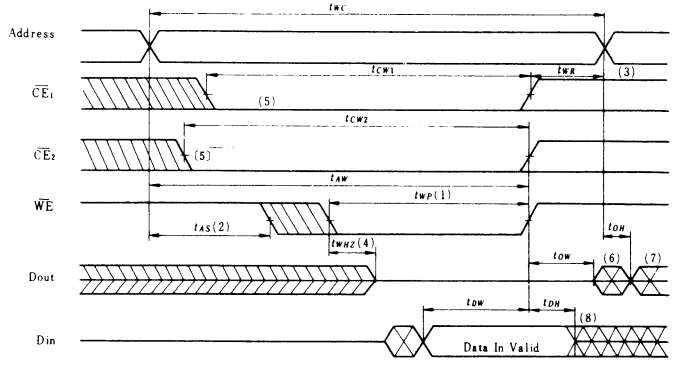


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

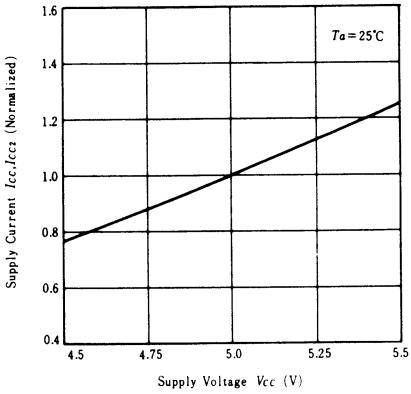
Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE

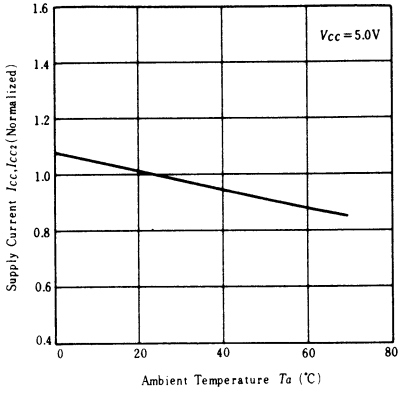


NOTES:
1. A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

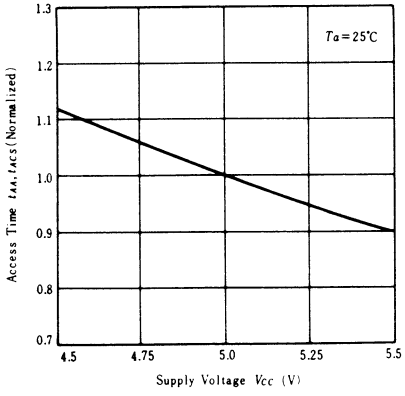
SUPPLY CURRENT vs. SUPPLY VOLTAGE



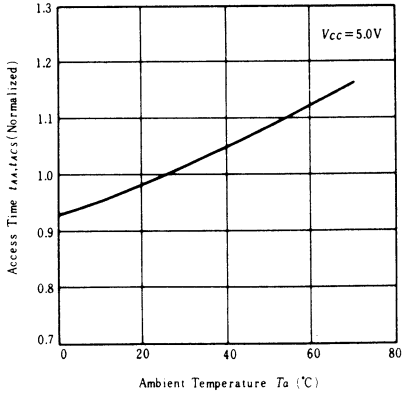
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



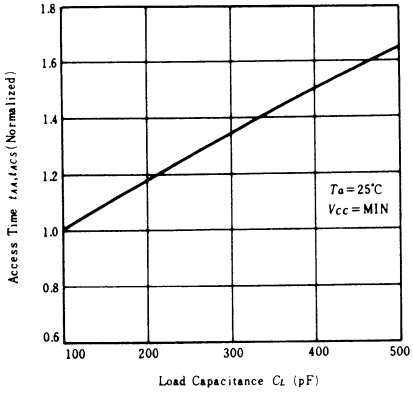
ACCESS TIME vs. SUPPLY VOLTAGE



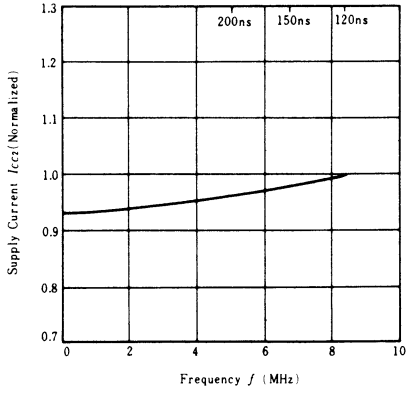
ACCESS TIME vs. AMBIENT TEMPERATURE



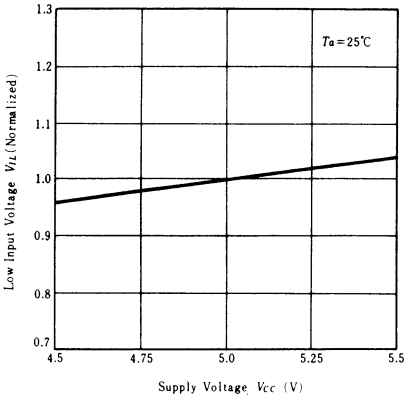
ACCESS TIME vs. LOAD CAPACITANCE



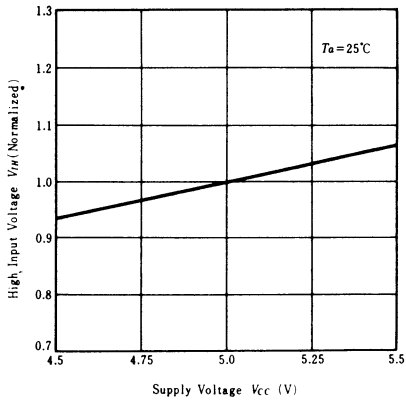
SUPPLY CURRENT vs. FREQUENCY



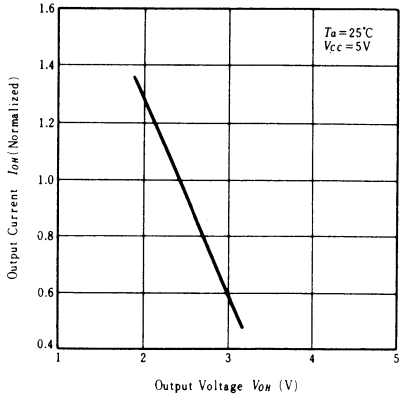
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



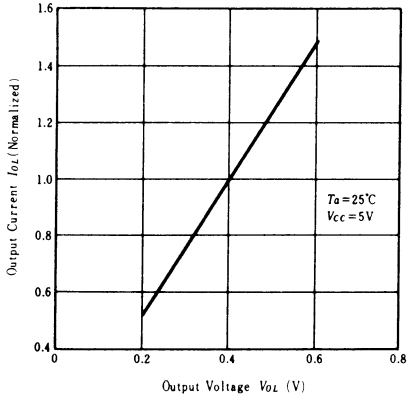
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

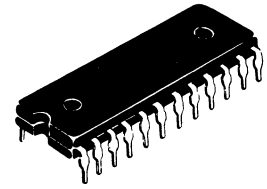


HM6117LP-3, HM6117LP-4

2048-word×8-bit High Speed Static CMOS RAM

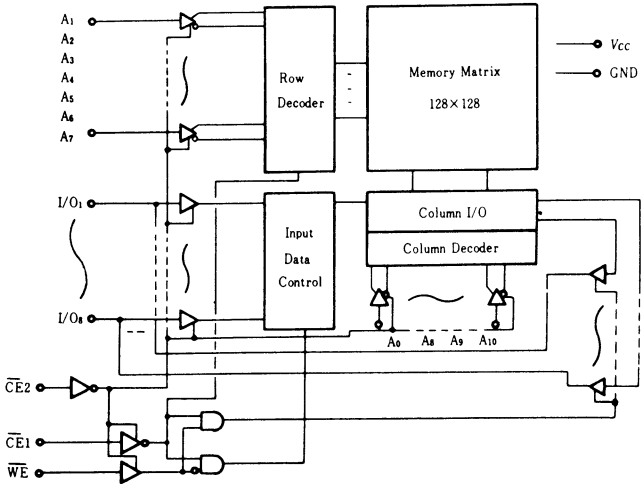
■FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

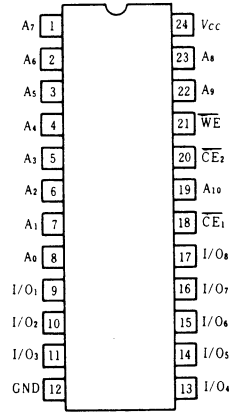


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns: −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0℃ to +70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : $V_{IL_{min}}$ = −0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC} = 5V±10%, GND = 0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN} = GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1} = V_{IH}$ or $\overline{CE_2} = V_{IH}$ $V_{I/O}$ = GND to V_{CC}	—	—	2	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1} = \overline{CE_2} = V_{IL}$, $I_{I/O}$ = 0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty = 100% $\overline{CE_1} = V_{IL}$, $\overline{CE_2} = V_{IL}$	—	35	70	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	2	50	μA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2} \geq V_{CC} - 0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC} = 5.0V, Ta = +25℃
2) * : $V_{IL_{min}}$ = −0.3V

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

Note : 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC} = 5V±10% unless otherwise noted)

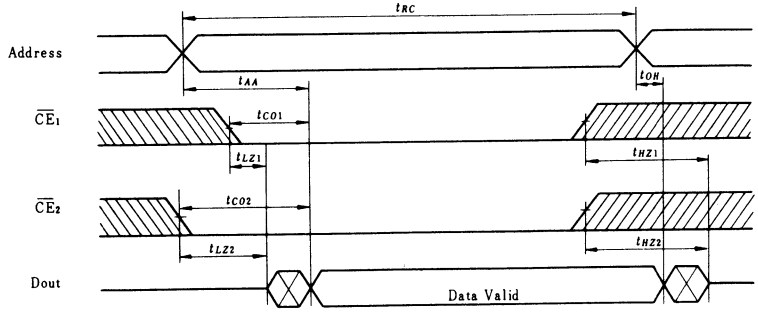
●AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

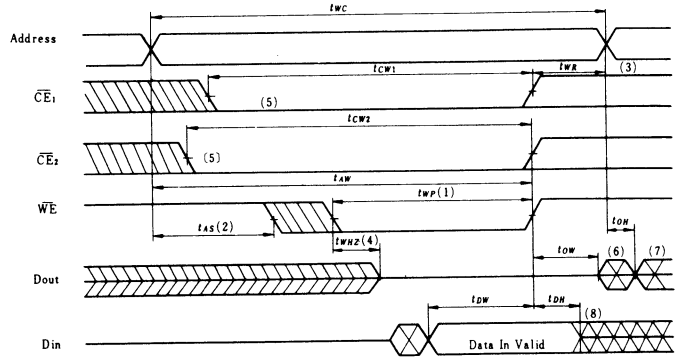


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE_2}$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$.

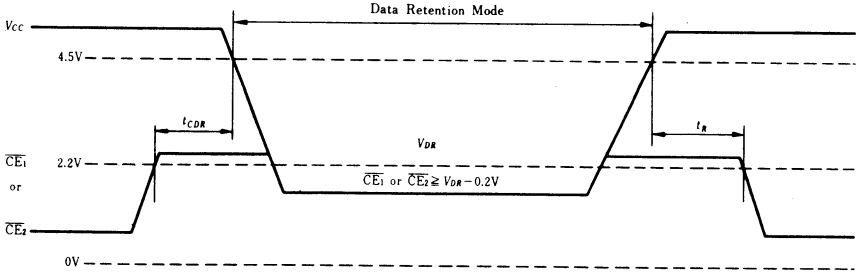
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE_1} \geqq 2.8V$, $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	V_{CC}=3.0V, $\overline{CE_2} \geqq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

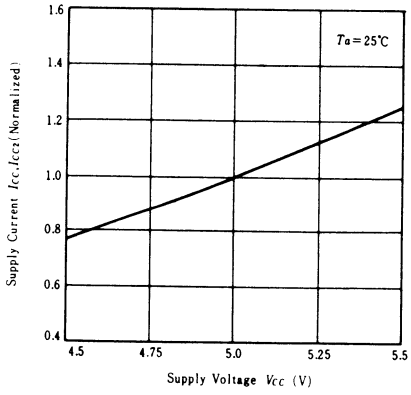
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

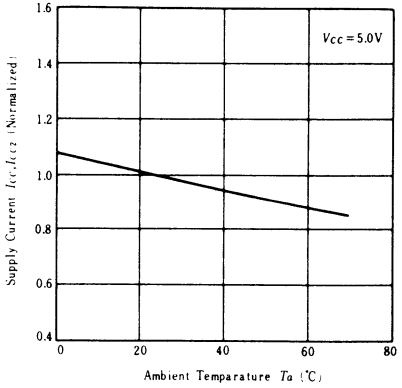


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{DE_2}$, $D_{I/O}$) must be $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$.

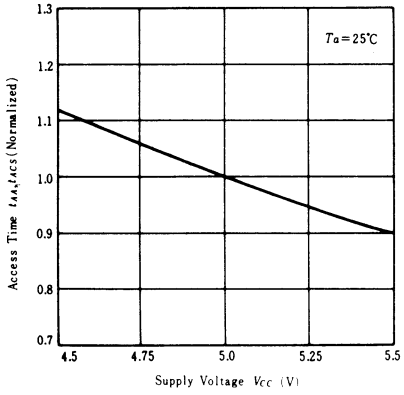
SUPPLY CURRENT vs. SUPPLY VOLTAGE



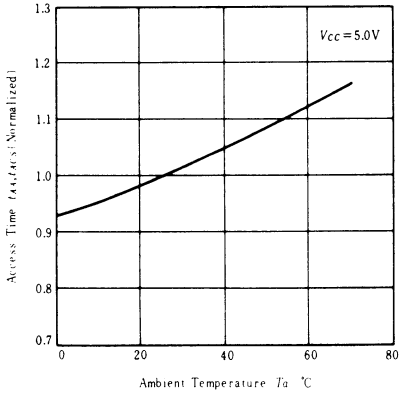
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



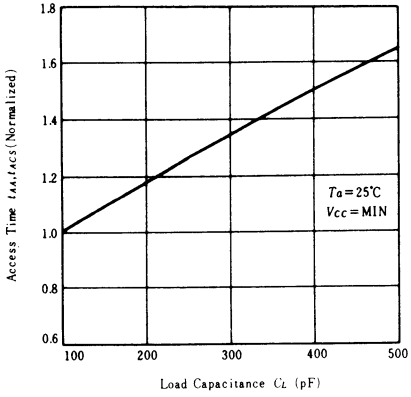
ACCESS TIME vs. SUPPLY VOLTAGE



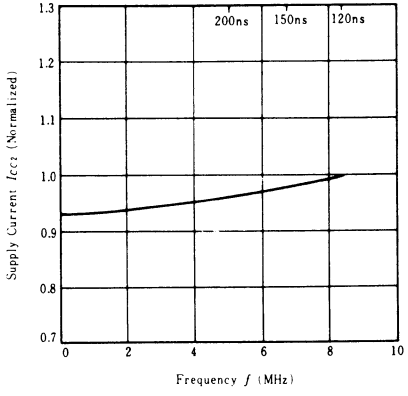
ACCESS TIME vs. AMBIENT TEMPERATURE



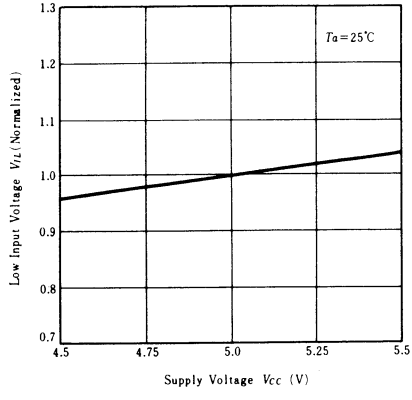
ACCESS TIME vs. LOAD CAPACITANCE



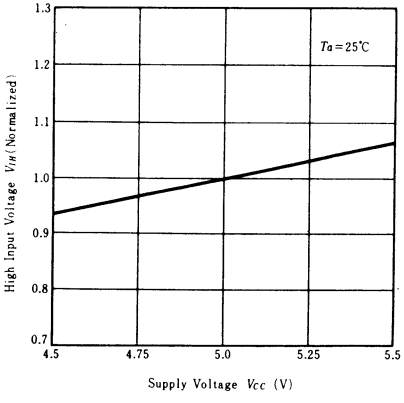
SUPPLY CURRENT vs. FREQUENCY



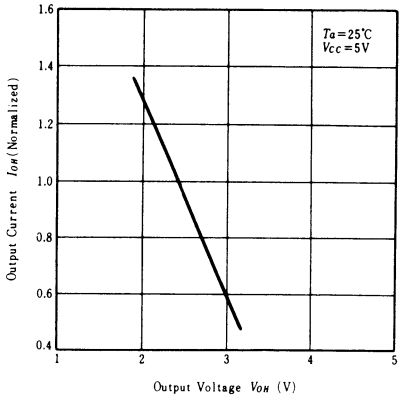
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



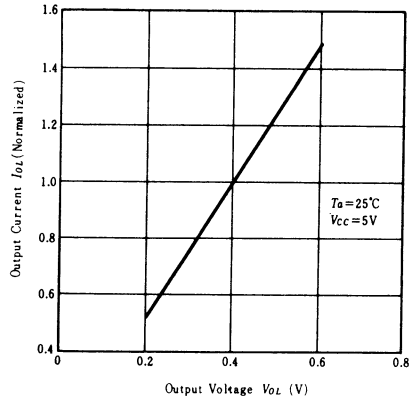
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



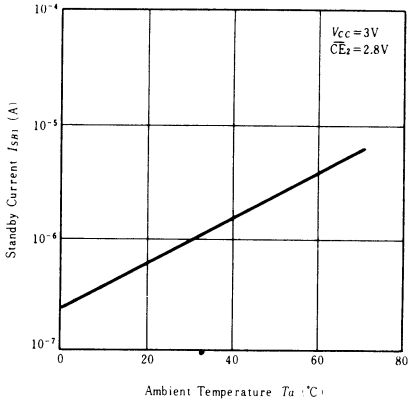
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



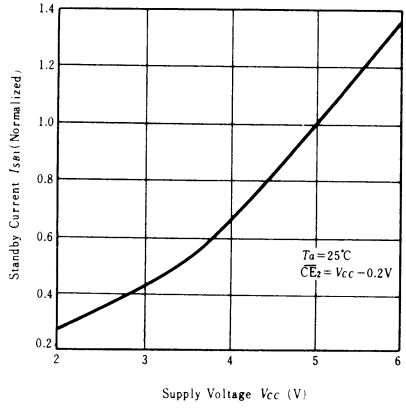
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



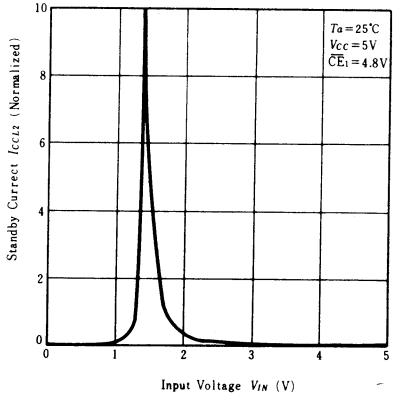
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



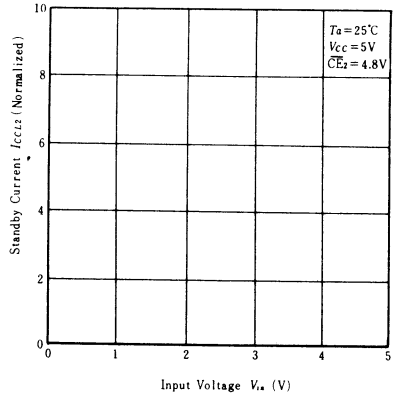
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE

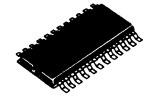


HM6117LFP-3, HM6117LFP-4

2048-word×8-bit High Speed Static CMOS RAM

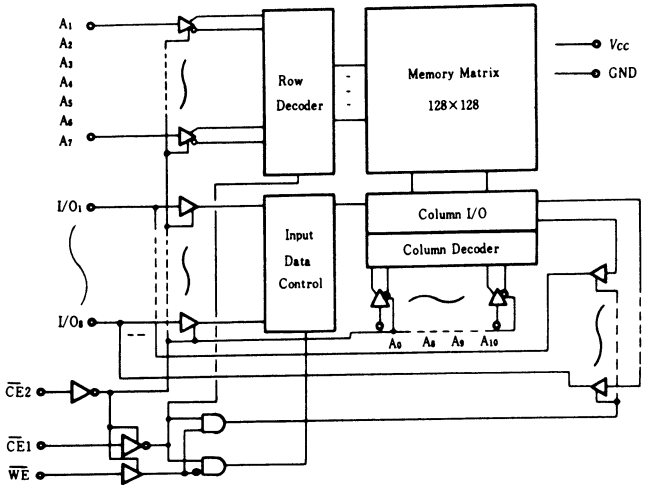
■FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

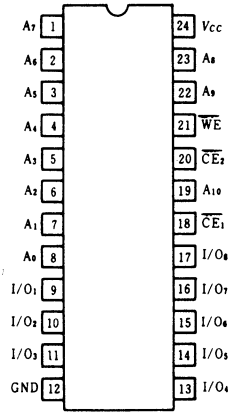


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns: −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0℃ to +70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width: 50ns, DC: $V_{IL\min}$ = −0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	35	70	mA
Standby Power Supply Current (1): DC	I_{CCL1}*	$\overline{CE_1}\geqq V_{CC}-0.2V$ $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$	—	2	50	μA
Standby Power Supply Current (2): DC	I_{CCL2}*	$\overline{CE_2}\geqq V_{CC}-0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes: 1) Typical limits are at V_{CC}=5.0V, Ta=+25℃
2) * : $V_{IL\min}$=−0.3V

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note: 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

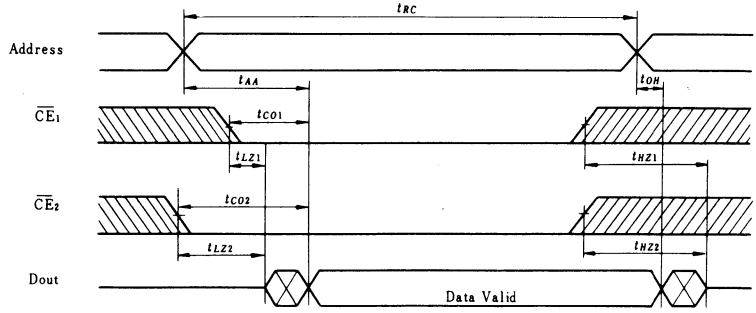
●AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

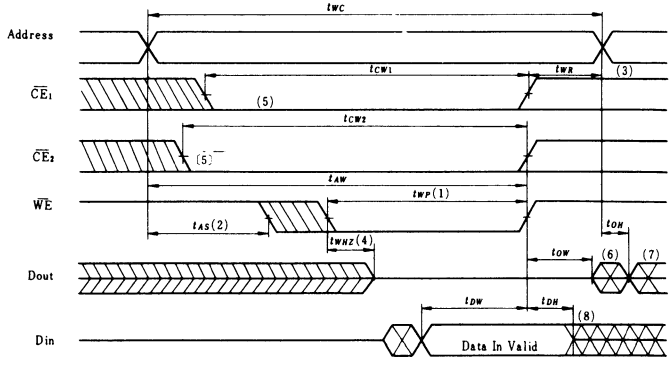


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE_2}$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$.

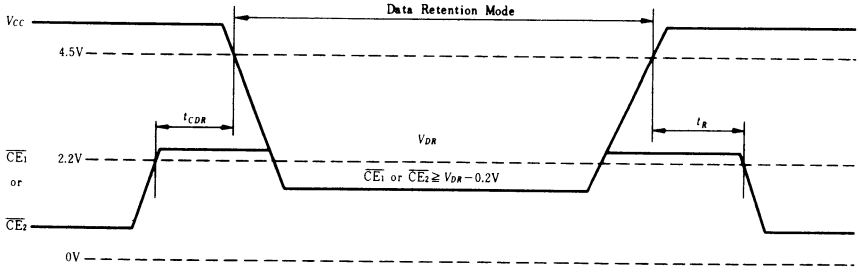
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE_1} \geqq 2.8V$, $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	V_{CC}=3.0V, $\overline{CE_2} \geqq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

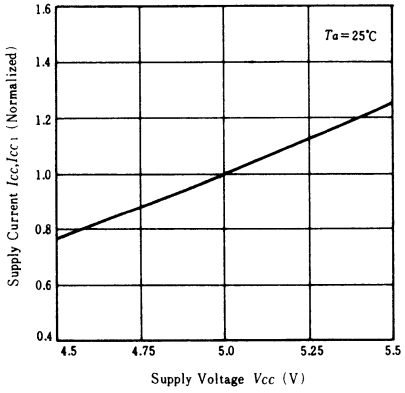
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

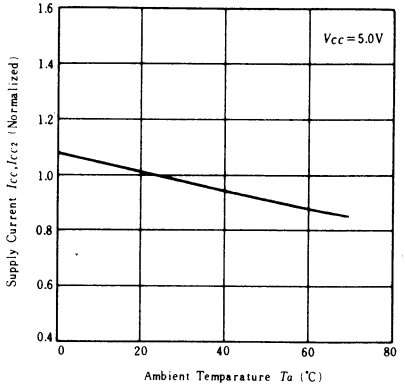


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_2}$, $D_{I/O}$) must be $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$.

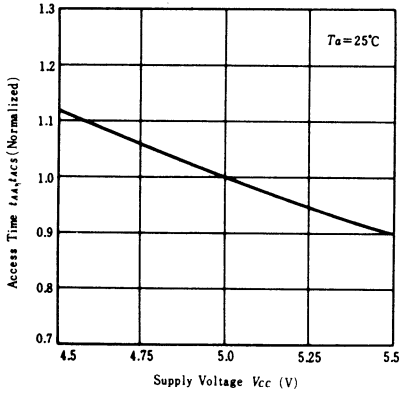
SUPPLY CURRENT vs. SUPPLY VOLTAGE



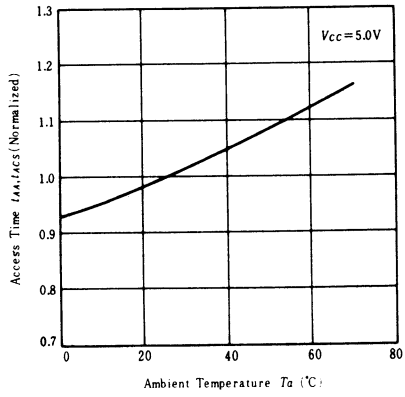
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



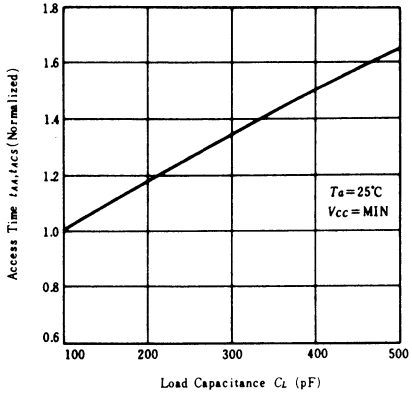
ACCESS TIME vs. SUPPLY VOLTAGE



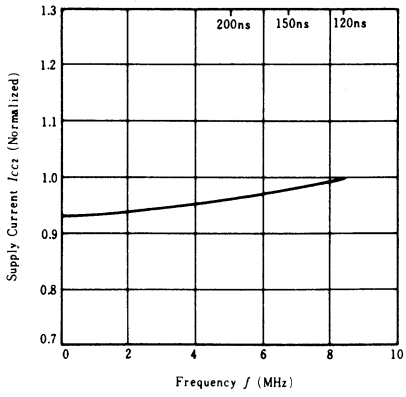
ACCESS TIME vs. AMBIENT TEMPERATURE



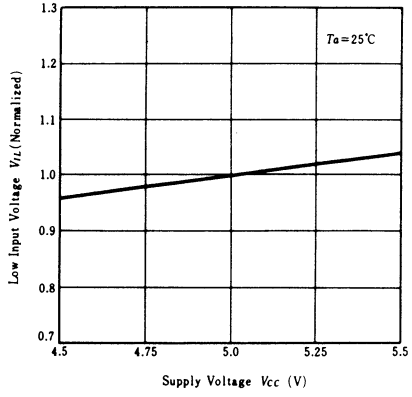
ACCESS TIME vs. LOAD CAPACITANCE



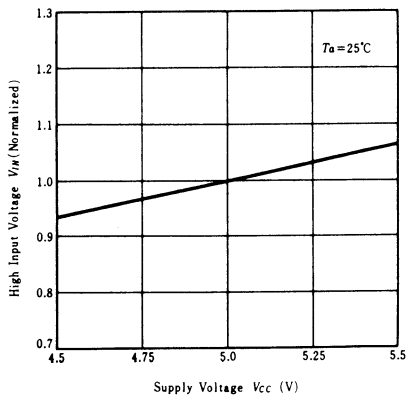
SUPPLY CURRENT vs. FREQUENCY



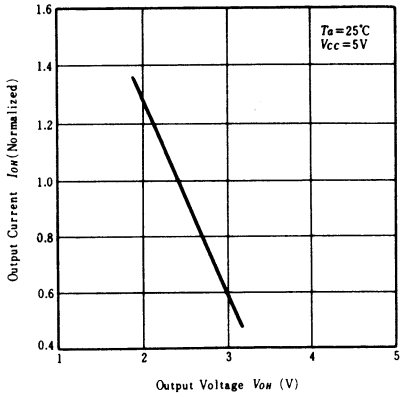
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



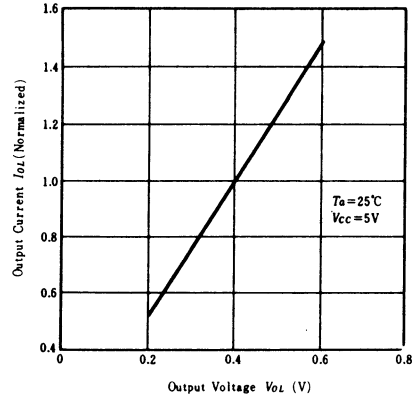
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



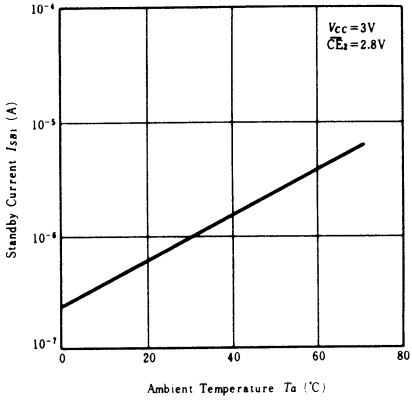
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



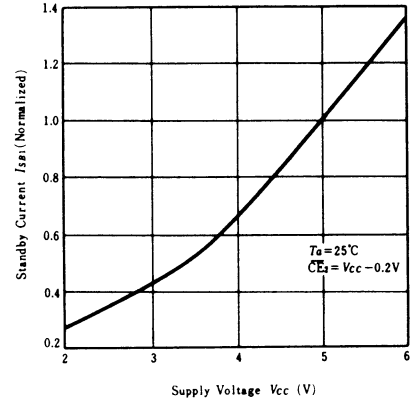
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



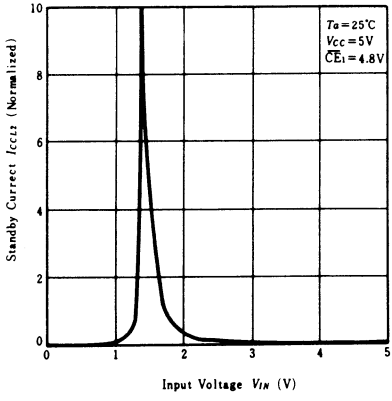
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



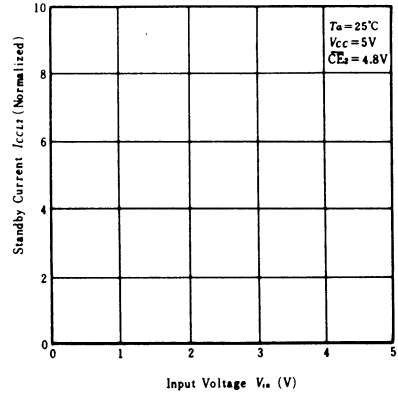
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



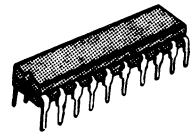
HM6168H-45, HM6168H-55, HM6168H-70, HM6168HP-45, HM6168HP-55, HM6168HP-70

4096-word × 4-bit High Speed Static CMOS RAM

■FEATURES

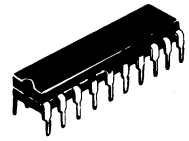
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  100μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible — All Inputs and Outputs

HM6168H-45/55/70



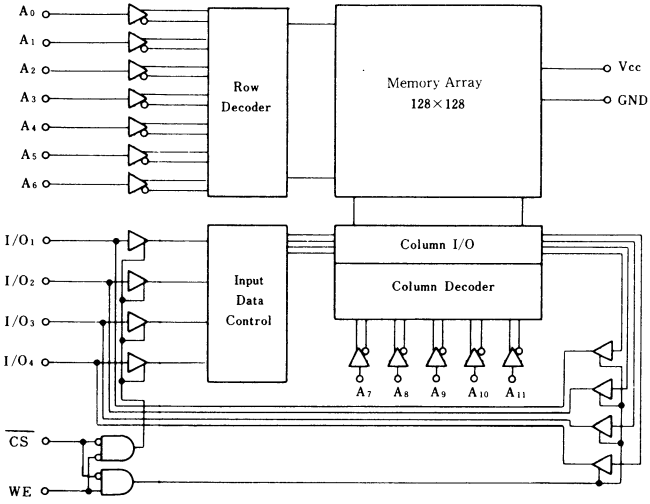
(DG-20)

HM6168HP-45/55/70

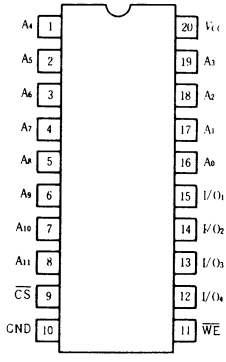


(DP-20)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*	–	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to + 70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	–	0.02	2.0	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	–	–	V

Note: Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

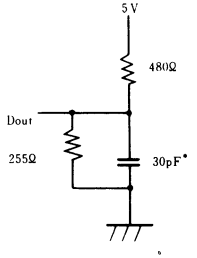
■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

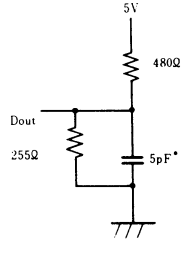
■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted.)

● AC TEST CONDITION

- Input pulse levels; GND to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figure



Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

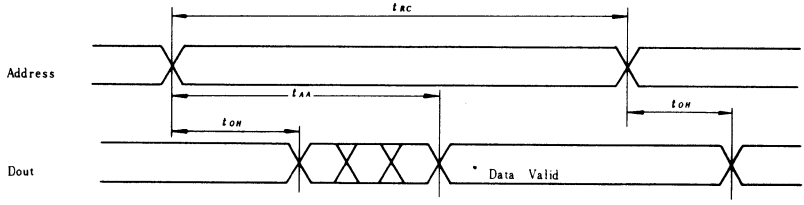
* Including scope and jig.

• READ CYCLE

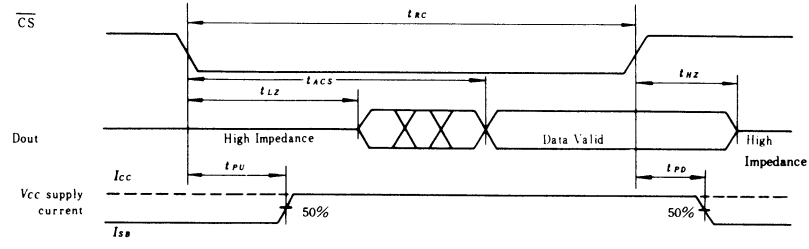
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

* Transition is measured ±500mV for high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[(1), (2)]



• TIMING WAVEFORM OF READ CYCLE NO. 2[(1), (3)]



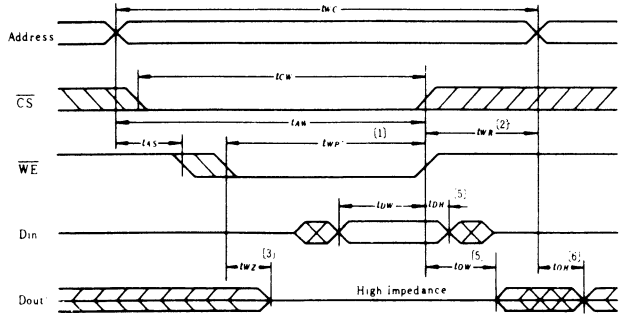
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

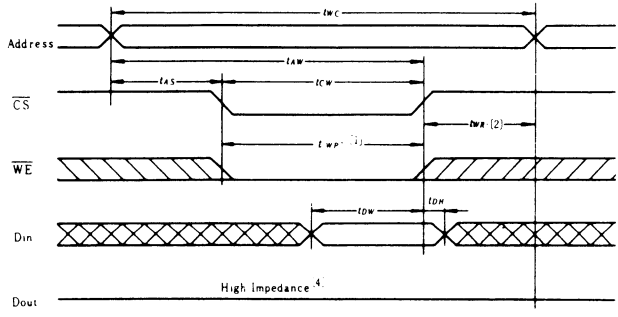
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	–	0	–	0	–	ns

* Thansition is measured ±500mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



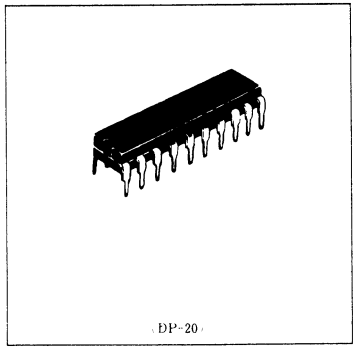
• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle.

HM6168HLP-45, HM6168HLP-55, HM6168HLP-70

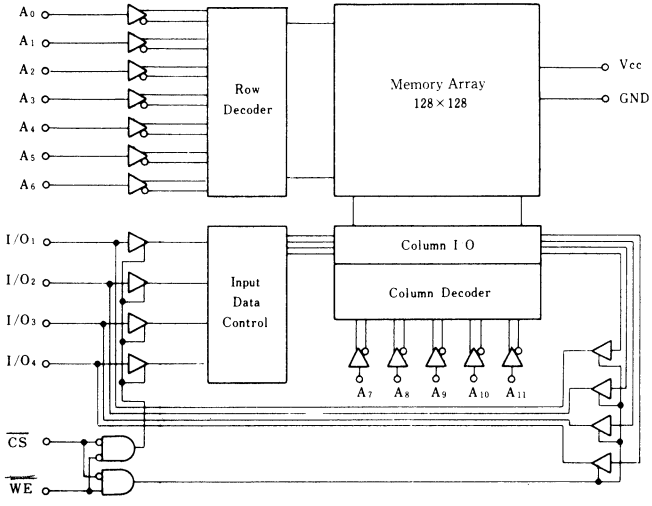
4096-word×4-bit High Speed Static CMOS RAM



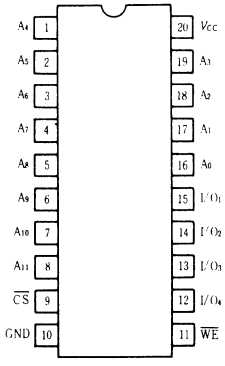
■FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  5μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible—All Inputs and Outputs
- Capable of Battery back up Operation

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC= −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*	–	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to + 70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Imput Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$=V_{CC}-0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}-0.2V	–	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Note: Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

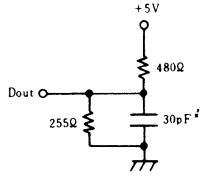
■ CAPACITANCE (Ta=25°C f=1MHz)

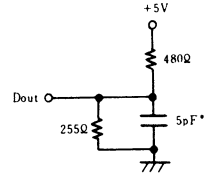
Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted)

● AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure





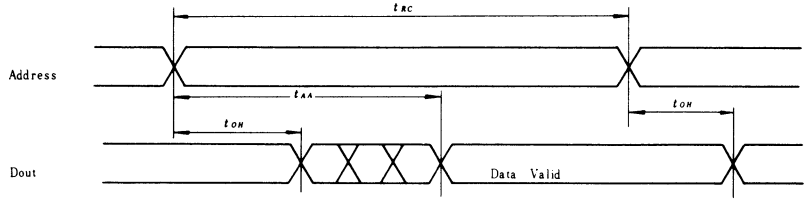
Output Load (A) * Including scope and jig. Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

• READ CYCLE

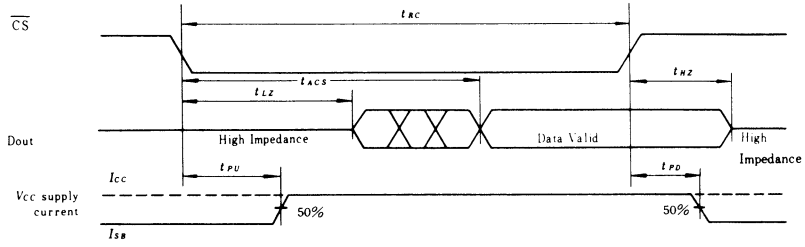
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

* Transition is measured ±500mV for high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 2(1), (2)



• TIMING WAVEFORM OF READ CYCLE NO. 2(1), (3)



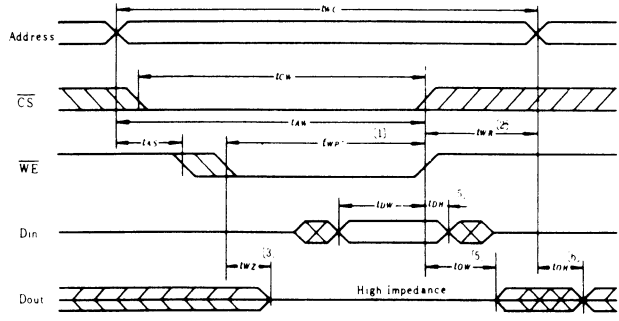
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

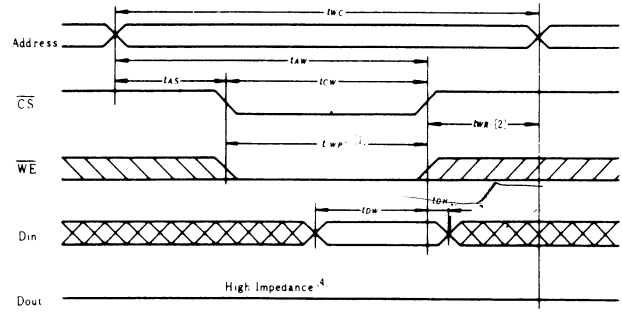
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	–	0	–	0	–	ns

* Thansition is measured ±500mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle.

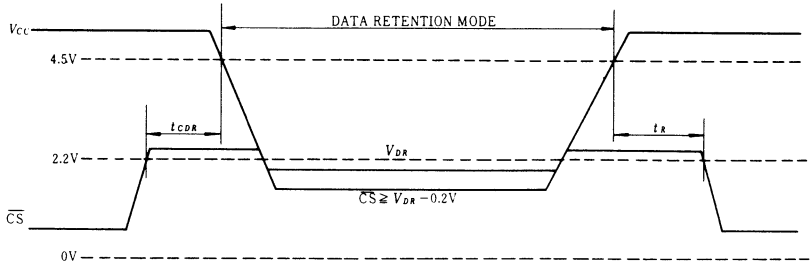
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} (1)	—	—	ns

Note 1. t_{RC} = Read Cycle Time.

* $V_{CC} = 3.0V$
** $V_{CC} = 2.0V$

●LOW V_{CC} DATA RETENTION WAVEFORM



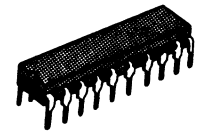
HM6167,HM6167-6,HM6167-8,
HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

■FEATURES

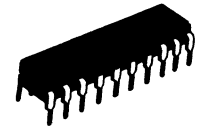
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time — 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 25mW Typ. and Operating 150mW Typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible — All Inputs and Output
- Separate Data Input and Output . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series

HM6167, HM6167-6,
HM6167-8



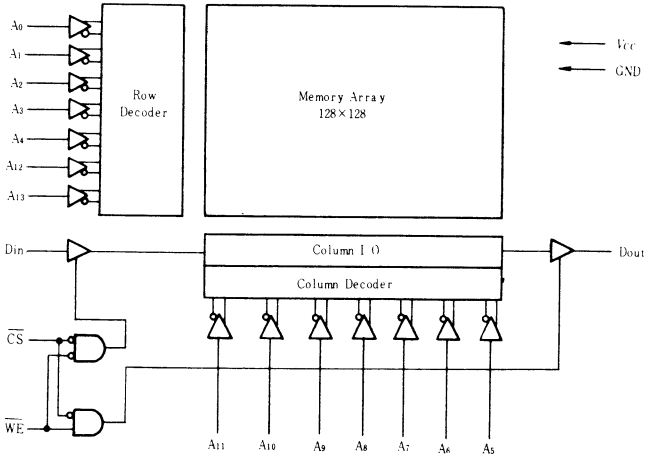
(DG-20)

HM6167P, HM6167P-6,
HM6167P-8

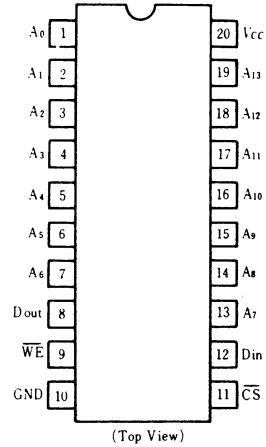


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* Pulse width 20ns : −3.5V **under bias

■RECOMMENDED DC OPERATING CONDITIONS

(0°C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width 20ns, DC : V_{IL} min = −0.3V

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to +70℃)

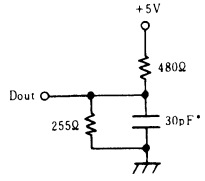
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	20	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	0.02	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25℃ and specified loading.

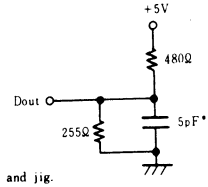
■AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	6	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to 70℃, unless otherwise noted.)

●READ CYCLE

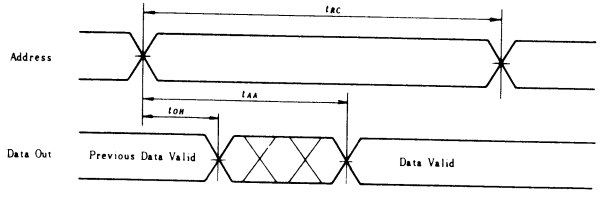
Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

● WRITE CYCLE

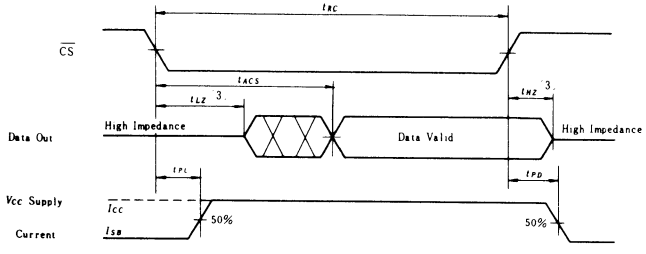
Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [1), 2)]

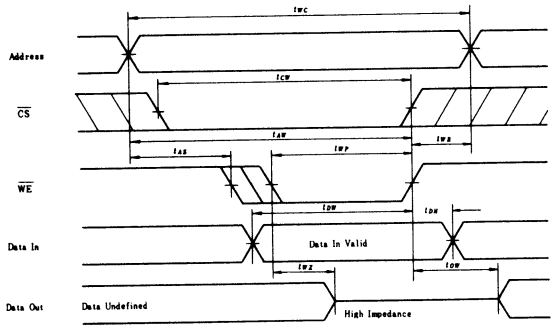


● TIMING WAVEFORM OF READ CYCLE NO. 2 [1), 3)]



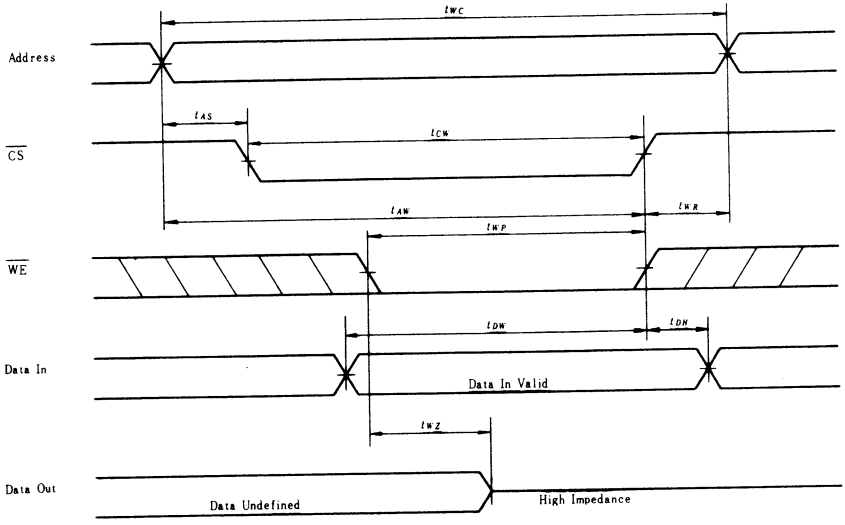
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



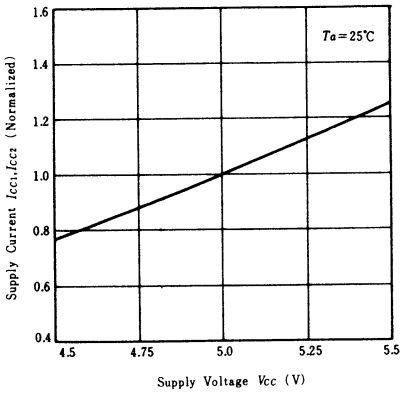
NOTE: 1. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)

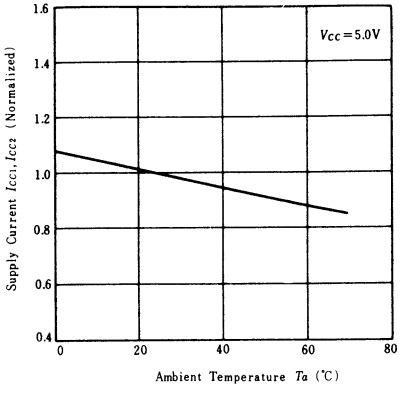


Note) Transition is measured ±500mV from steady state voltage with specified loading in Load B.

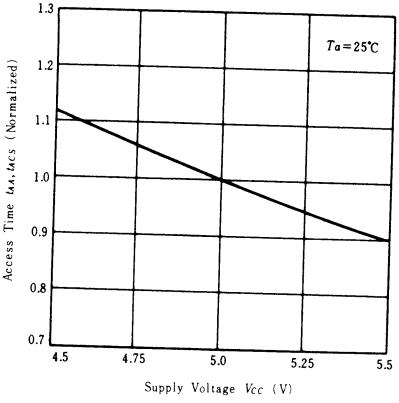
SUPPLY CURRENT vs. SUPPLY VOLTAGE



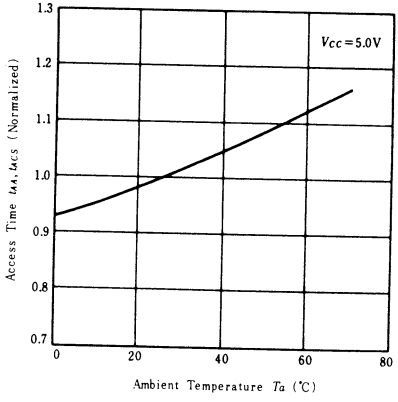
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



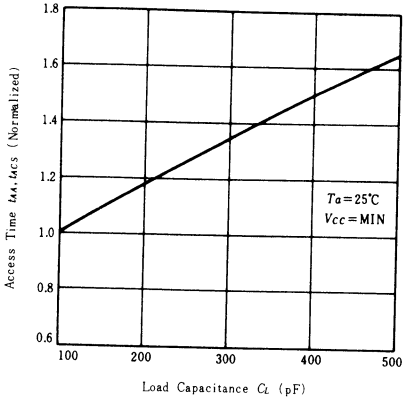
ACCESS TIME vs. SUPPLY VOLTAGE



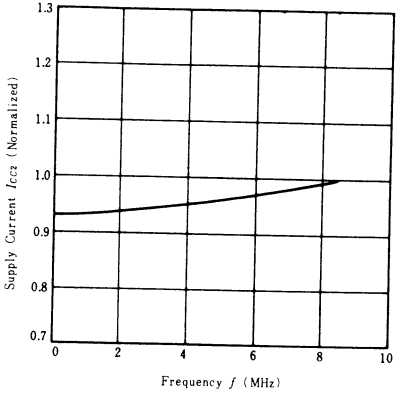
ACCESS TIME vs. AMBIENT TEMPERATURE



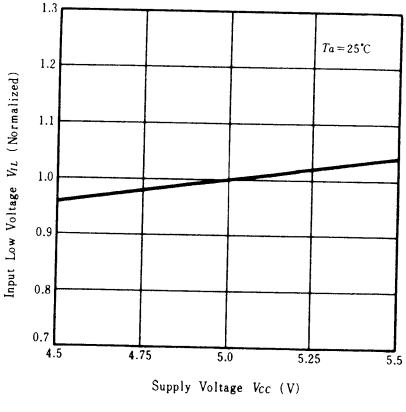
ACCESS TIME vs. LOAD CAPACITANCE



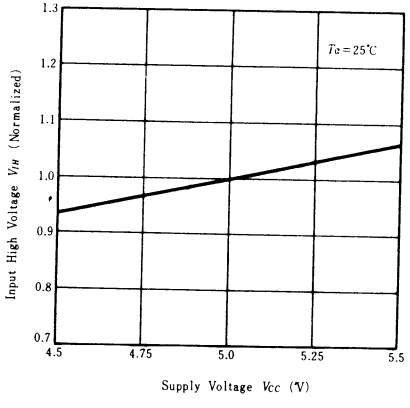
SUPPLY CURRENT vs. FREQUENCY



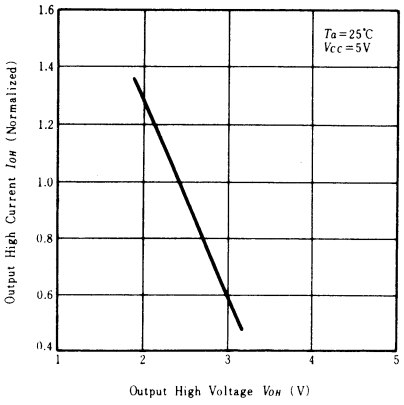
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



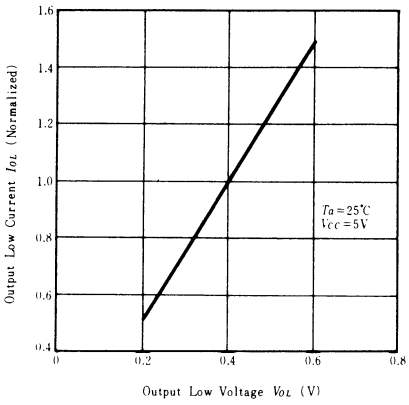
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



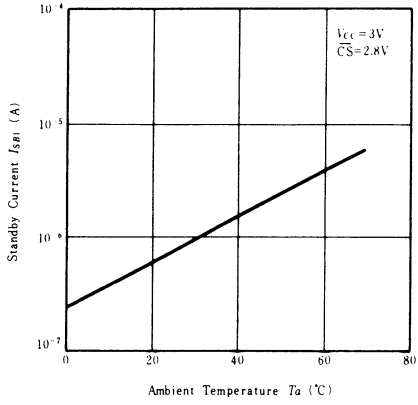
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



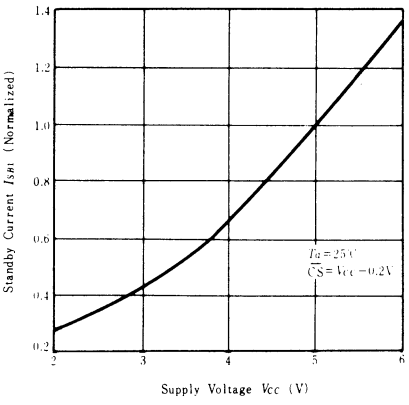
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



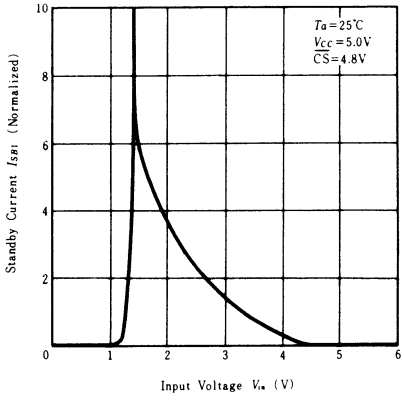
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

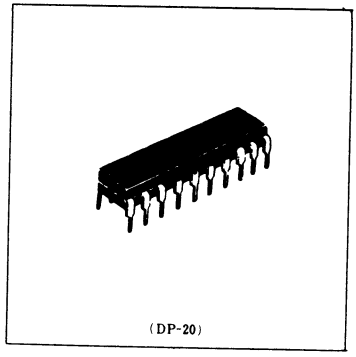


HM6167LP, HM6167LP-6, HM6167LP-8

16384-word×1-bit High Speed Static CMOS RAM

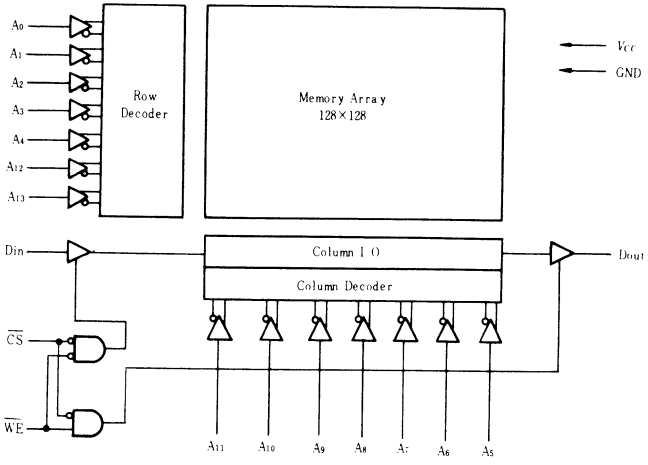
■FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory. . . . . .No Clock or Refresh Required
- Fully TTL Compatible . . . . . .All Inputs and Output
- Separate Data Input and Output . . . . . .Three State Output
- Capable of Battery Back up Operation

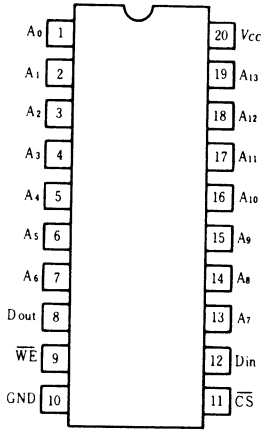


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* Pulse width 20ns −3.5V ** under bias

■RECOMMENDED DC OPERATING CONDITIONS (0 °C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width 20ns, DC, V_{IL} min = −0.3V

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $Ta=0\sim+70°C$)

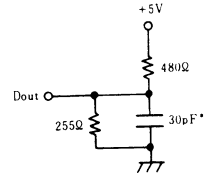
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V$ $V_{IN}=0V\sim V_{CC}$	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{I/O}=0V\sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN}\leqq0.2V$ or $V_{IN}\geqq V_{CC}-0.2V$	—	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.

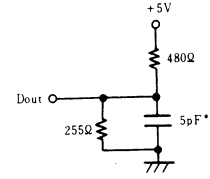
■AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	6	pF	$V_{OUT}=0V$

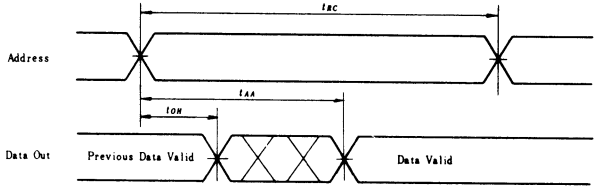
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS ($Ta=0°C$ to $+70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted.)

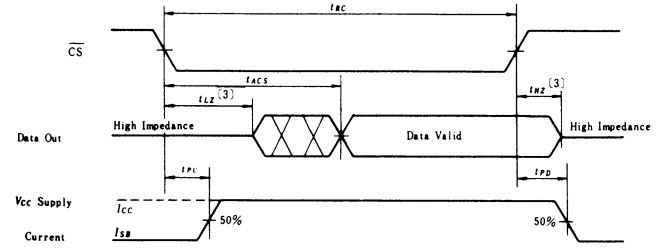
●READ CYCLE

Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

● TIMING WAVEFORM OF READ CYCLE NO. 1 [1), 2)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [1), 3)]



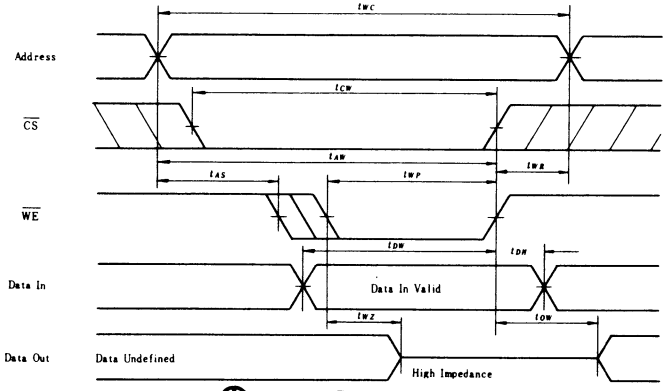
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ Cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading B.

● WRITE CYCLE

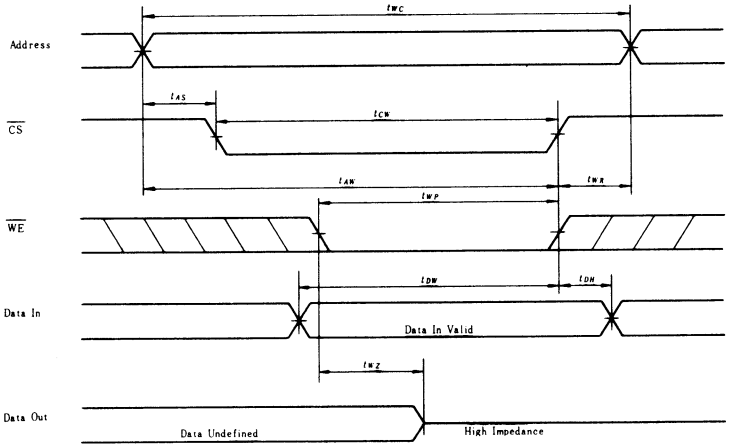
Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)



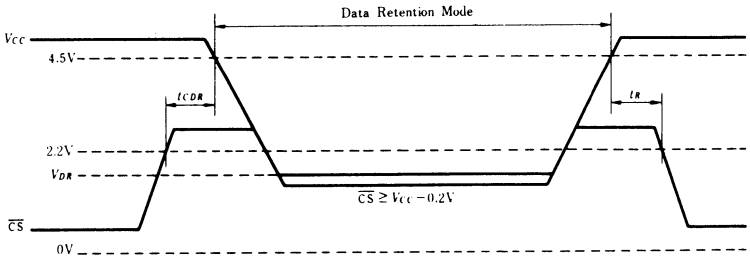
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}		2.0	—	—	V
Data Retention Current	I_{CCDR}	$\overline{CS} \geq V_{CC}-0.2V$	—	—	20*	μA
		$V_{in} \geq V_{CC}-0.2V$ or	—	—	30**	
Chip Deselect to Data Retention Time	t_{CDR}	$0V \leq V_{in} \leq 0.2V$	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}△	—	—	ns

△ t_{RC} = Read Cycle Time

* V_{CC} = 2.0V
** V_{CC} = 3.0V

■ LOW V_{CC} DATA RETENTION WAVEFORM



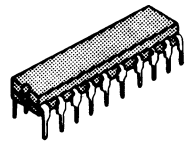
HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

16384-word x 1-bit High Speed Static CMOS RAM

■ FEATURES

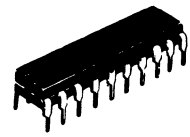
- Fast Access Time. . . . . .HM6167H/P-45 45ns (max)
  HM6167H/P-55 55ns (max)
- Low Power Standby and Low Power Operation
  Standby 100μW (typ), Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- Completely Static Memory . . . .No Clock nor Refresh Required
- Fully TTL Compatible . . . . . .All Inputs and Output
- Separate Data Input and Output. . . . . .Three State Output

HM6167H-45, HM6167H-55



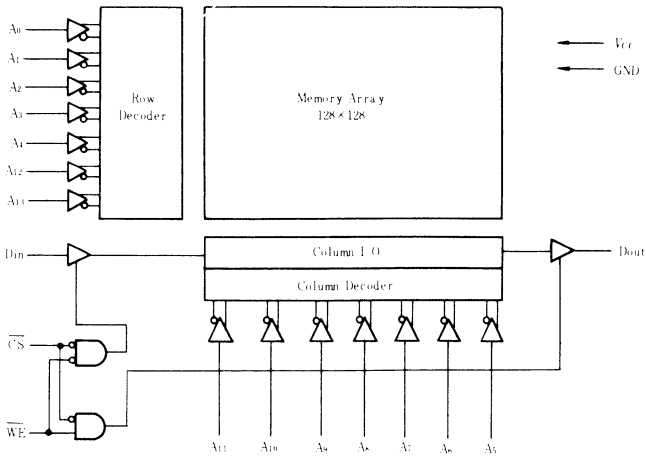
(DG-20)

HM6167HP-45, HM6167HP-55

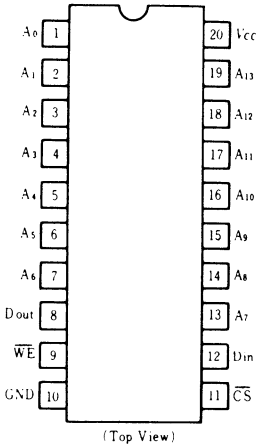


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (under bias)	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC: −0.5V

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width: 20ns, DC: V_{IL} (min) = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $Ta=0℃$ to $+70℃$)

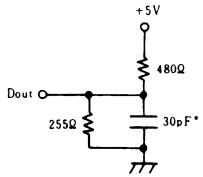
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI}\rvert$	$V_{CC}=5.5V$, $V_{IN}=0V\sim V_{CC}$	—	—	2	μA
Output Leakage Current	$\lvert I_{LO}\rvert$	$\overline{CS}=V_{IH}$, $V_{OUT}=0V\sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	10	20	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$ $V_{IN}\leqq 0.2V$ or $V_{IN}\geqq V_{CC}-0.2V$	—	0.02	2	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $Ta=25℃$ and specified loading.

■AC TEST CONDITIONS

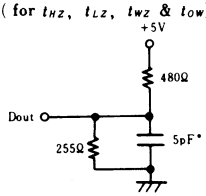
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE ($Ta=25℃$, $f=1.0MHz$)

Item	Symbol	typ	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	5	7	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

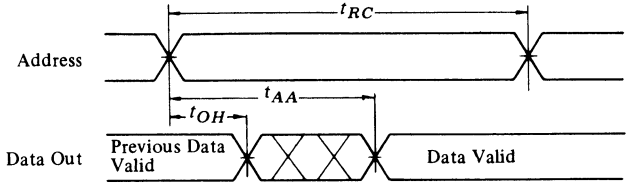
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0°C to 70°C, unless otherwise noted.)

●READ CYCLE

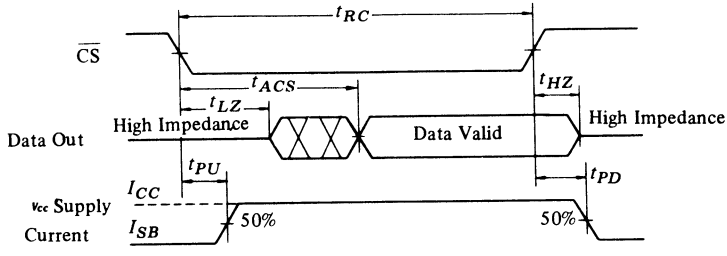
Item	Symbol	HM6167H/P-45		HM6167HP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	ns	(1)
Address Access Time	t_{AA}	–	45	–	55	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2) (3) (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	ns	

NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 [4), 5)]



●TIMING WAVEFORM OF READ CYCLE NO.2 [4), 6)]

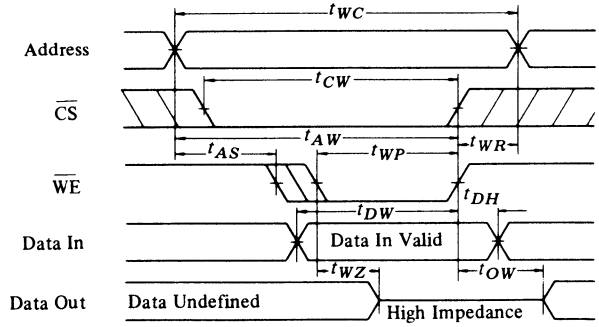


• WRITE CYCLE

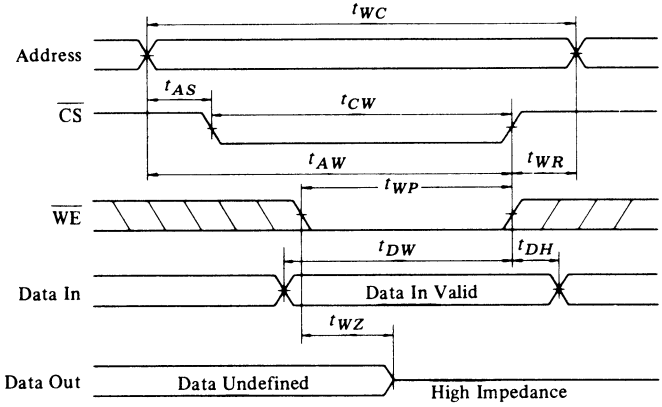
Item	Symbol	HM6167H/P-45		HM6167H/P-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	ns	(2)
Chip Selection to End of Write	t_{CW}	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

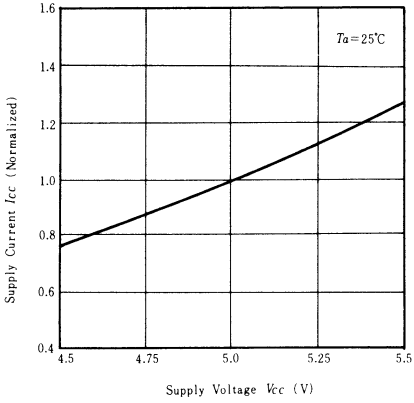
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



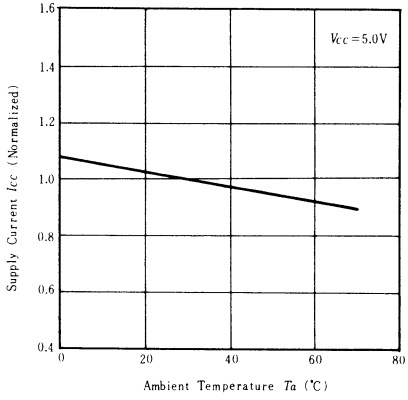
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



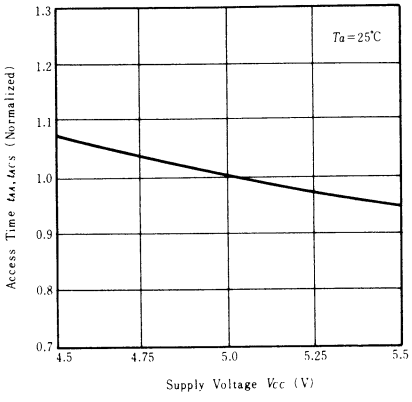
SUPPLY CURRENT vs. SUPPLY VOLTAGE



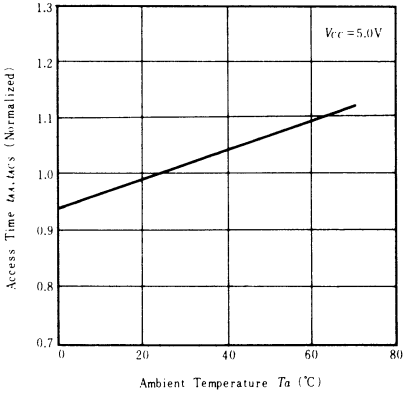
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



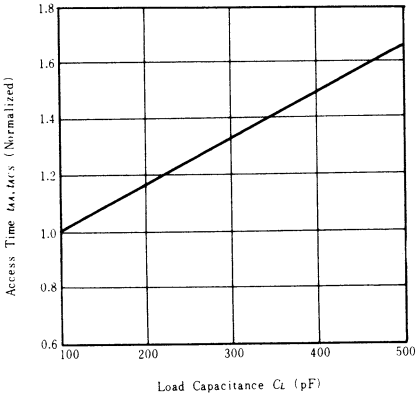
ACCESS TIME vs. SUPPLY VOLTAGE



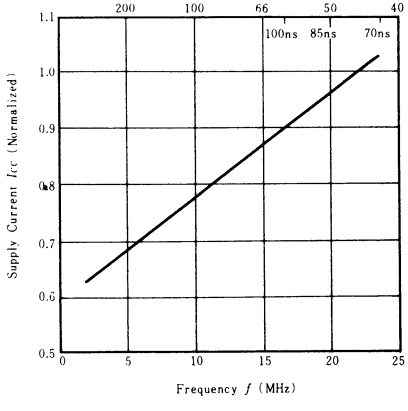
ACCESS TIME vs. AMBIENT TEMPERATURE



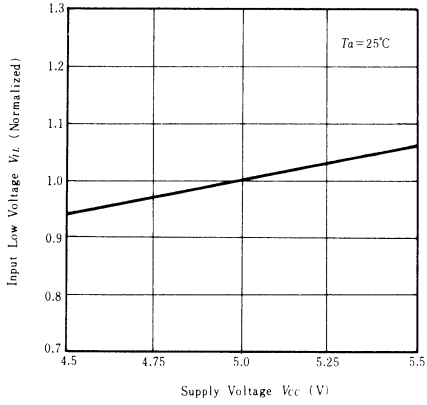
ACCESS TIME vs. LOAD CAPACITANCE



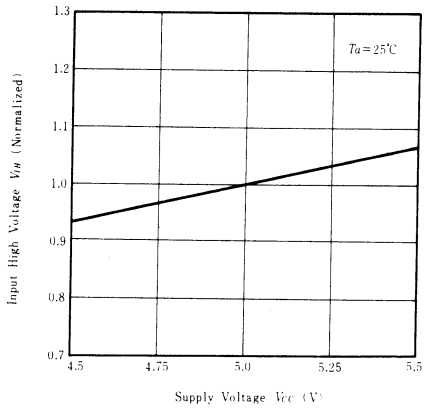
SUPPLY CURRENT vs. FREQUENCY



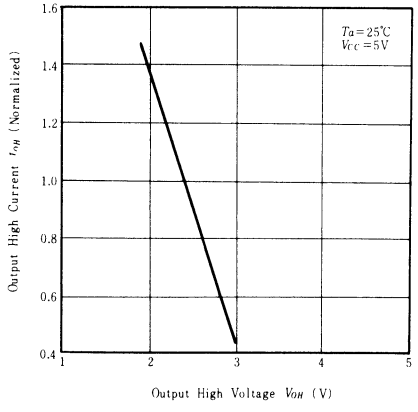
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



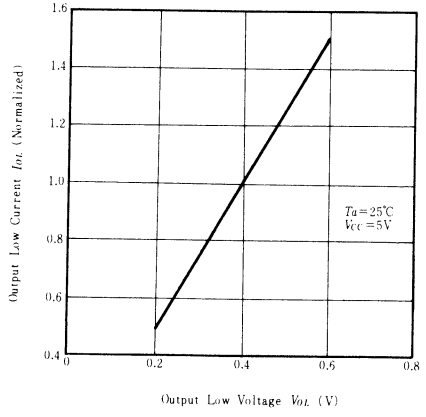
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



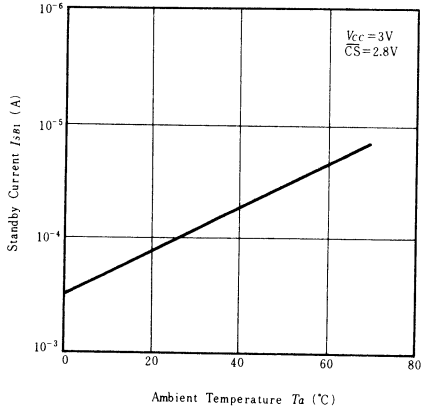
OUTPUT CURRENT vs. OUTPUT VOLTAGE



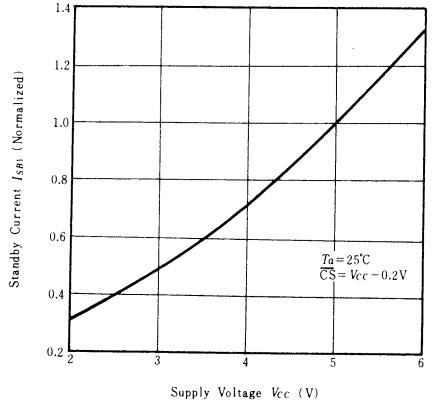
OUTPUT CURRENT vs. OUTPUT VOLTAGE



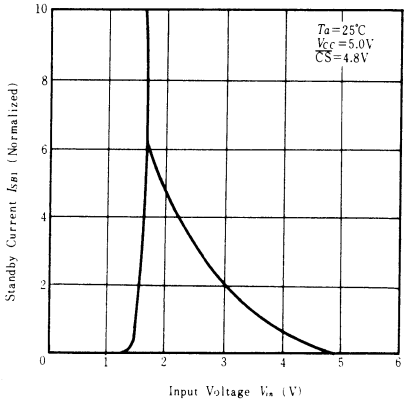
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

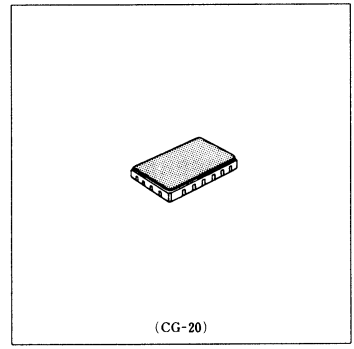


HM6167HCG-45, HM6167HCG-55

16384-word × 1-bit High Speed Static CMOS RAM

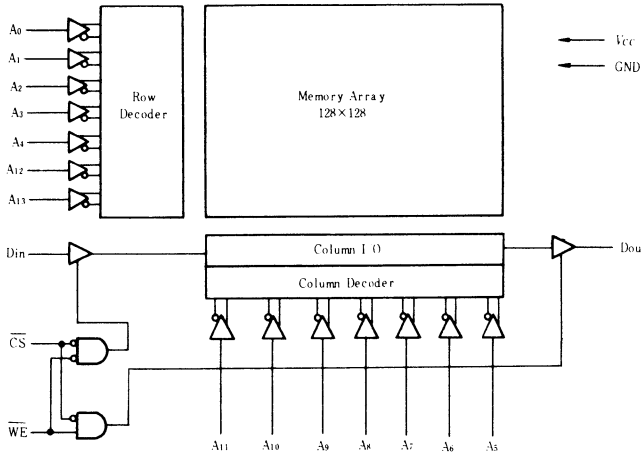
■FEATURES

- High Density 20 pin Leadless Chip Carrier
- High Speed: Fast Access Time 45/55ns Max.
- Low Power Standby and Low Power Operation
  Standby: 100μW typ., Operation: 200mW typ.
- Completely Static Memory;
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Output

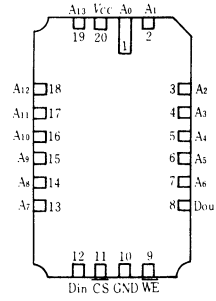


(CG-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Bottom View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. V_{IN} min = −3.5V (Pulse width 20ns)

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5*	—	0.8	V

* −3.0V (Pulse width 20ns)

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, V_{OUT}=0V to V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	10	20	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{IN}\leqq 0.2V$ or $V_{IN}\geqq V_{CC}-0.2V$	—	20	2000	μA
Output Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) * : Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Output Capacitance	C_{out}	V_{out}=0V	5	7	pF

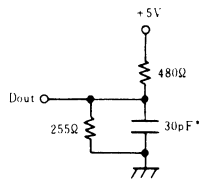
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

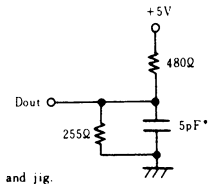
●AC TEST CONDITIONS

Input Pulse Levels: GND to 3.0V
Input Rise and Fall Times: 5 ns
Output Reference Levels: 1.5V

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



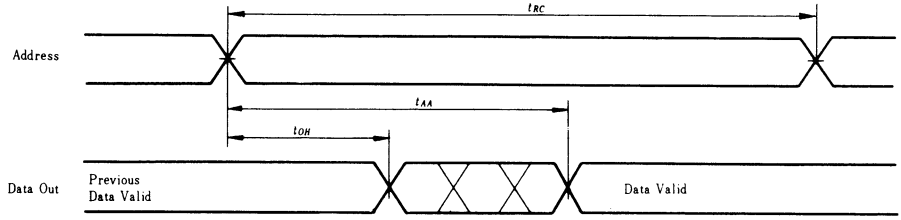
* Including scope and jig.

●READ CYCLE

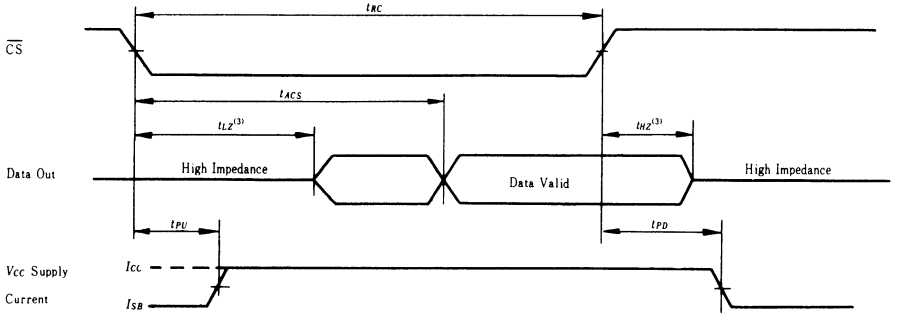
Item	Symbol	HM6167HCG-45		HM6167HCG-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	—	55	—	ns	1
Address Access Time	t_{AA}	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	2, 3, 4
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 4
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns	

Notes) 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

●Read Cycle-1 (Notes 1, 2)



●Read Cycle-2 (Notes 1, 3)



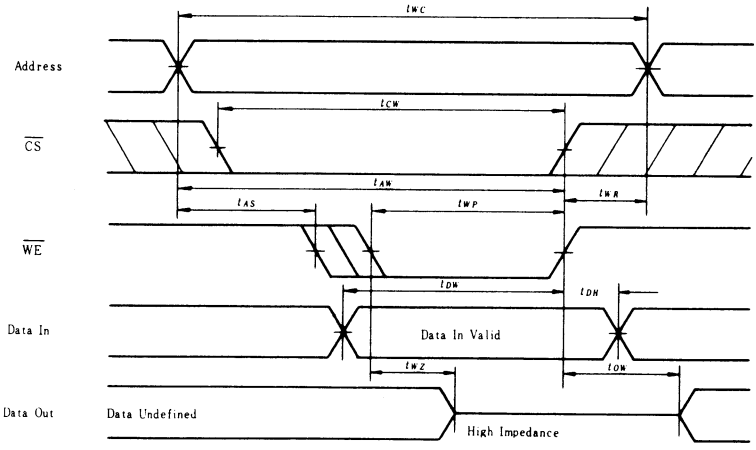
Notes) 1. $\overline{WE}$ is high for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

●WRITE CYCLE

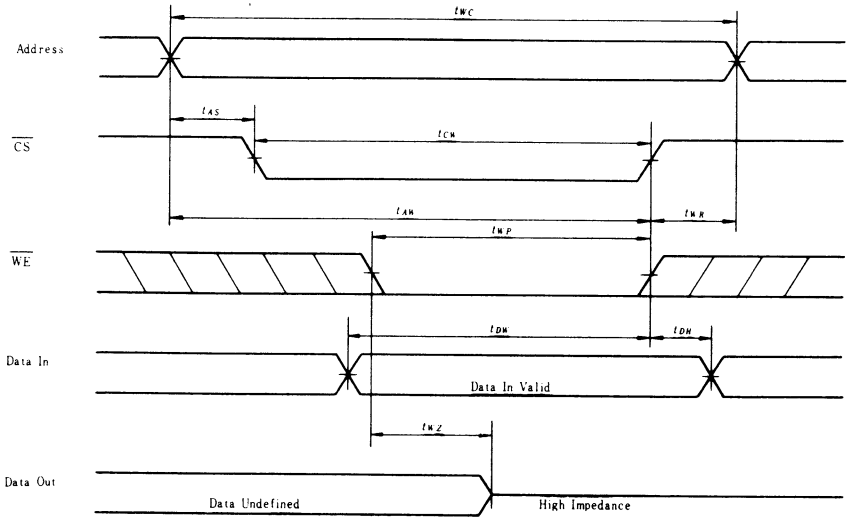
Item	Symbol	HM6167HCG-45		HM6167HCG-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	—	55	—	ns	2
Chip Selection to End of Write	t_{CW}	40	—	50	—	ns	
Address Valid to End of Write	t_{AW}	40	—	50	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	35	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	25	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● Write Cycle-1 ($\overline{WE}$ Controlled)



● Write Cycle-2 ($\overline{CS}$ Controlled)

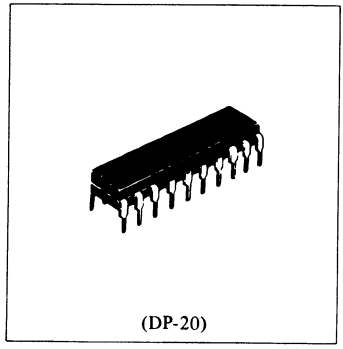


HM6167HLP-45, HM6167HLP-55

16384-word x 1-bit High Speed Static CMOS RAM

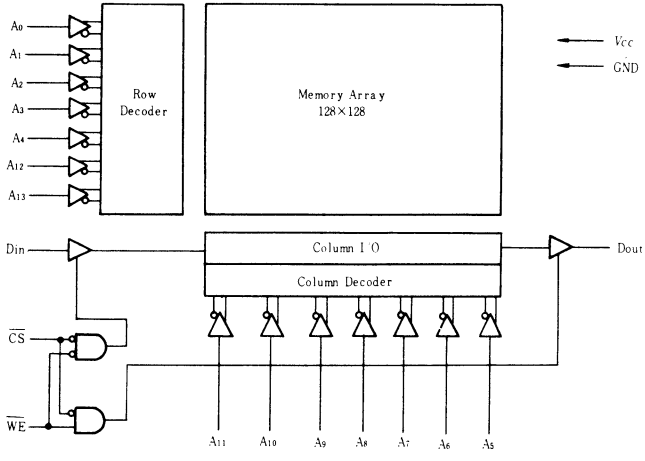
■ FEATURES

- Fast Access Time. . . . . .HM6167HLP-45 45ns (max)
  HM6167HLP-55 55ns (max)
- Low Power Standby and Low Power Operation
  Standby 5μW (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible . . . . .All Inputs and Output

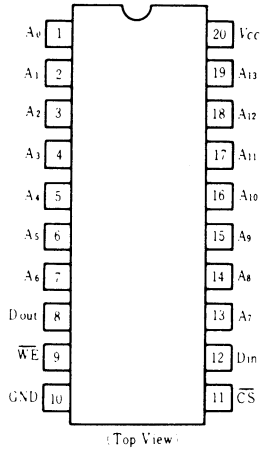


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC: −0.5V

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70°C)

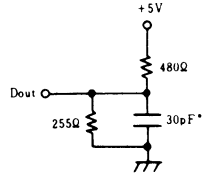
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	10	20	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

■ AC TEST CONDITIONS

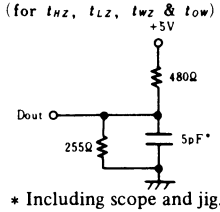
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

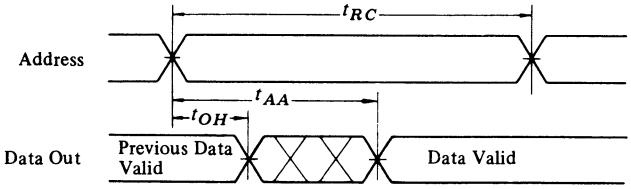
■ AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, unless otherwise noted.)

●READ CYCLE

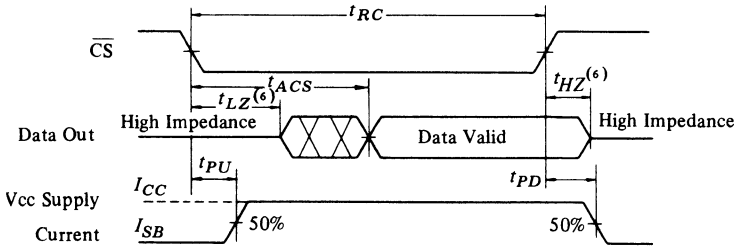
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	ns	(1)
Address Access Time	t_{AA}	–	45	–	55	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2) (3) (7)
Chip Selection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	ns	

NOTES:
1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

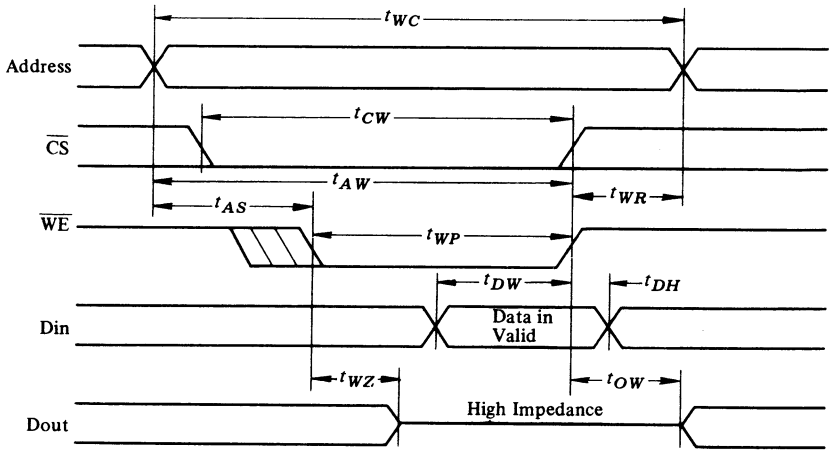


● WRITE CYCLE

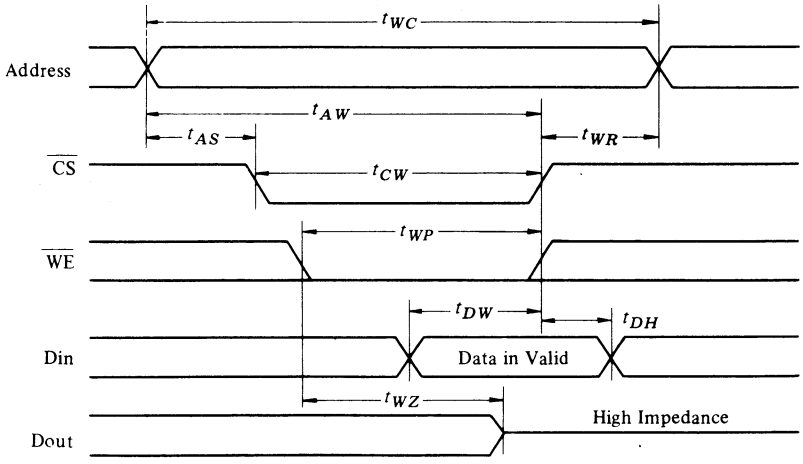
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	ns	(2)
Chip Selection to End of Write	t_{CW}	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



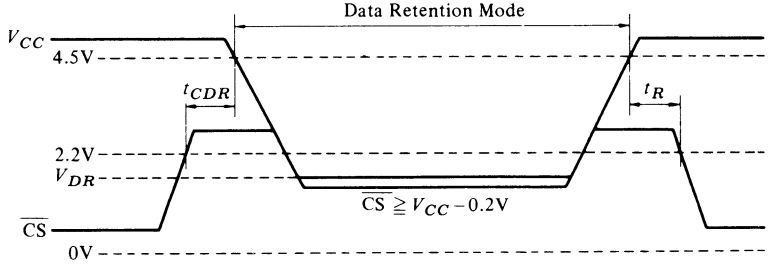
■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}		2.0	—	—	V
Data Retention Current	I_{CCDR}	$\overline{CS} \geq V_{CC}-0.2V$	—	—	20*	μA
		$V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	—	—	30**	
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}△	—	—	ns

△ t_{RC} = Read Cycle Time

* V_{CC} = 2.0V
** V_{CC} = 3.0V

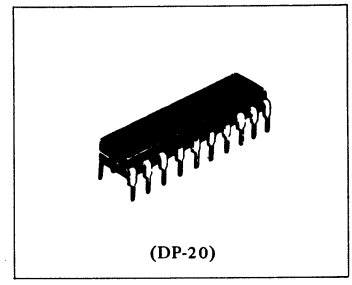
●LOW V_{CC} DATA RETENTION WAVEFORM



HM6267P-35,HM6267P-45

Preliminary

16384-word x 1-bit High Speed Static CMOS RAM

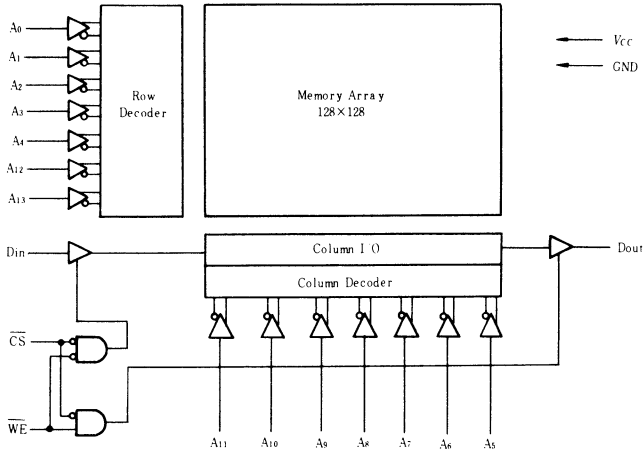


(DP-20)

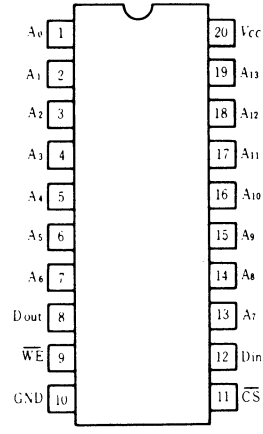
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

* with respect to GND. V_T min = -3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-3.0*	–	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = −0.5V

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HITACHI

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS[1] (V_{CC} = 5V ±10%[2], GND = 0V, T_a = 0 to +70°C)

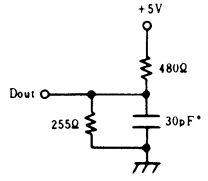
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = GND to V_{CC}	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{out} = GND to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, Output Open	–	40	80[3]	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}-0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}-0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = –4mA	2.4	–	–	V

Notes) 1. Typical limits are at V_{CC} = 5V, T_a = 25°C and specified loading.
2. V_{CC} = 5V±5% for 35ns version.
3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

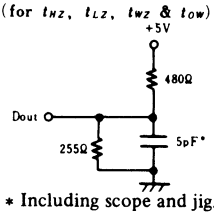
Input pulse levels: GND to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

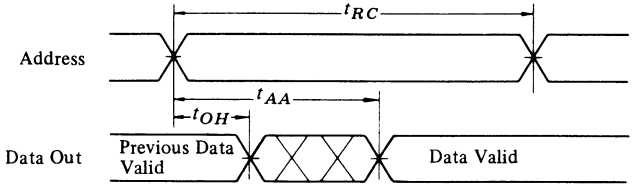
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%*, T_a = 0 to 70°C, unless otherwise noted.)

● READ CYCLE

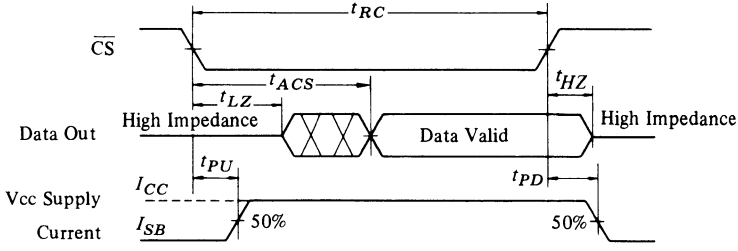
Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	ns	

* V_{CC} = 5V ± 5% for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

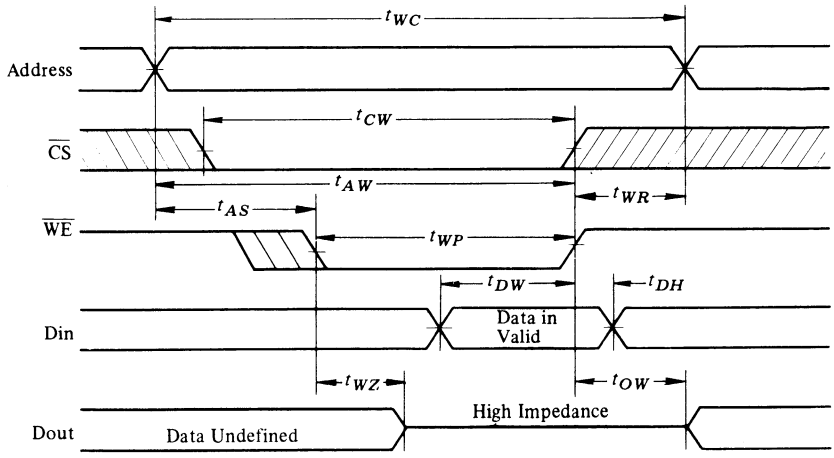


NOTES:
1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

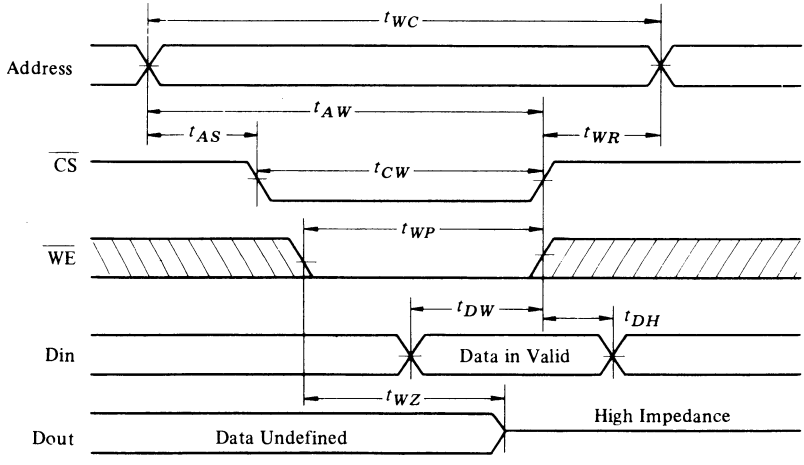
● WRITE CYCLE

Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

- **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



- **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



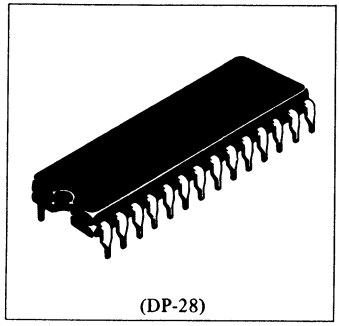
NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

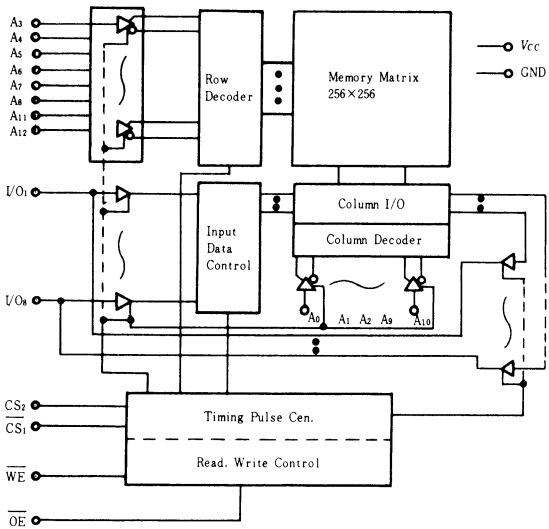
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

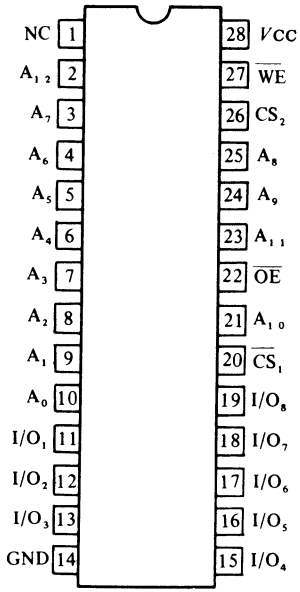


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	0.02	2	mA
	I_{SB2}**	CS2≦0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

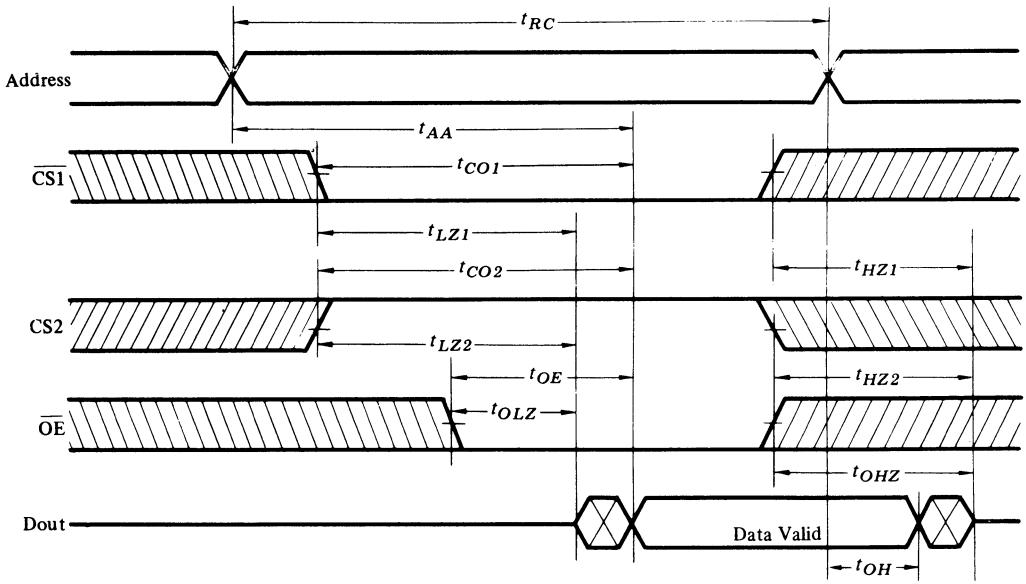
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

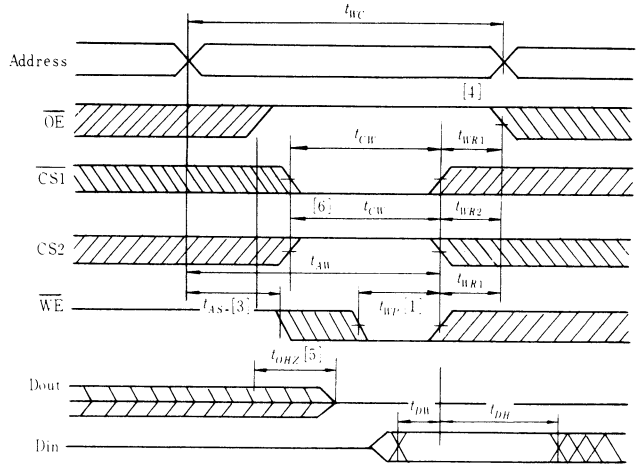


NOTE: 1) $\overline{WE}$ is high for Read Cycle

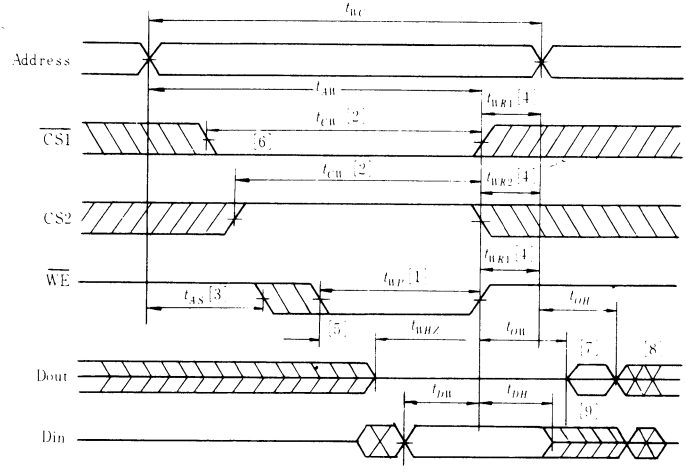
• **WRITE CYCLE**

Item		Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**

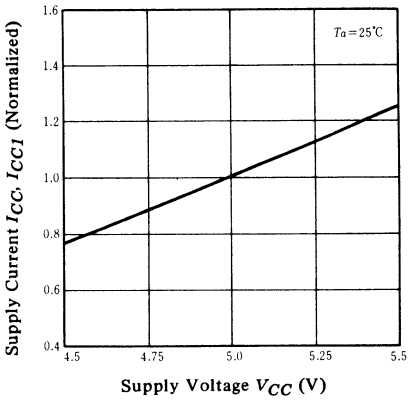


• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**

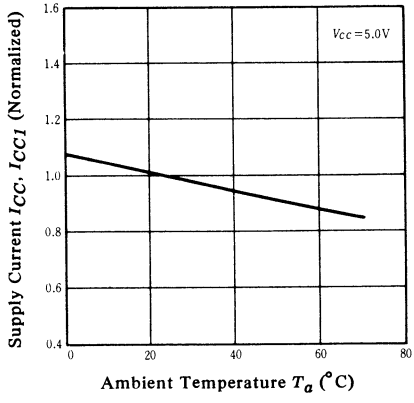


NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

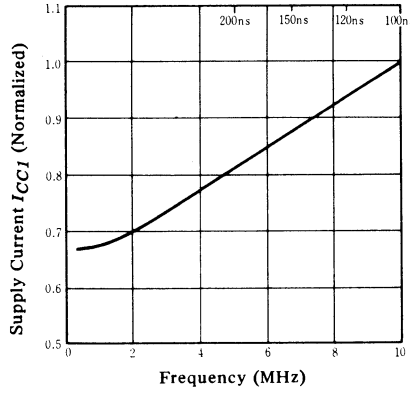
SUPPLY CURRENT vs. SUPPLY VOLTAGE



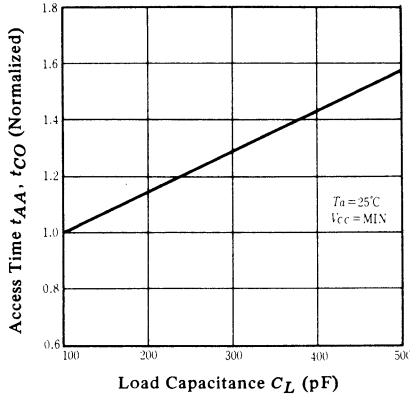
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



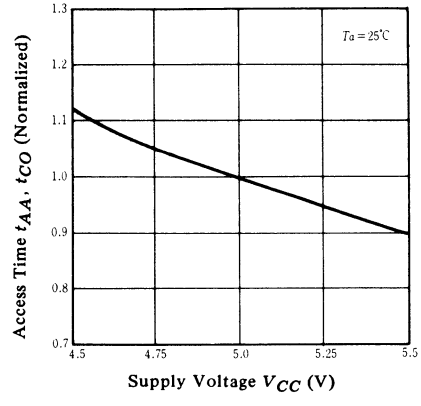
SUPPLY CURRENT vs. FREQUENCY



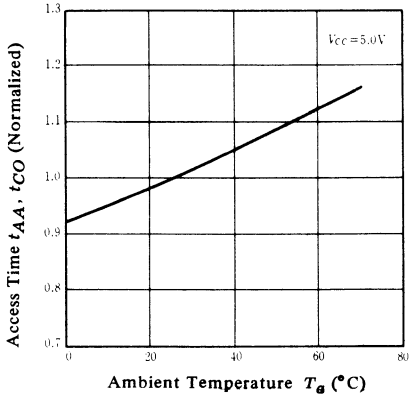
ACCESS TIME vs. LOAD CAPACITANCE



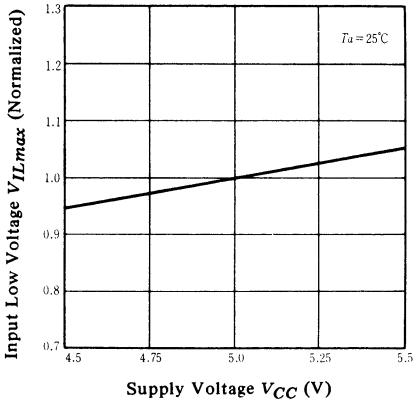
ACCESS TIME vs. SUPPLY VOLTAGE



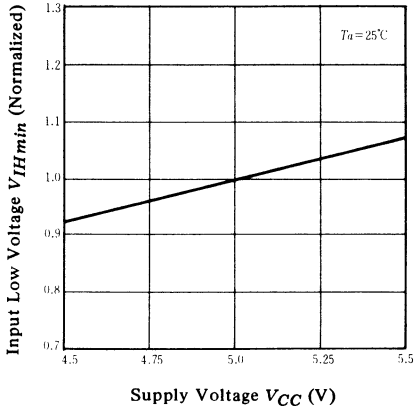
ACCESS TIME vs. AMBIENT TEMPERATURE



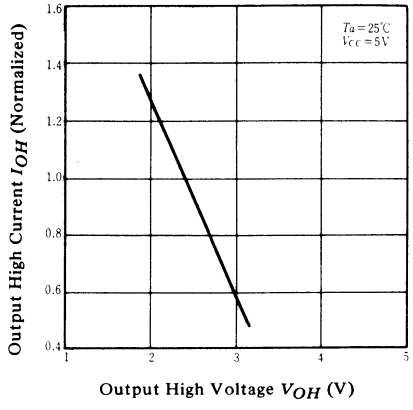
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



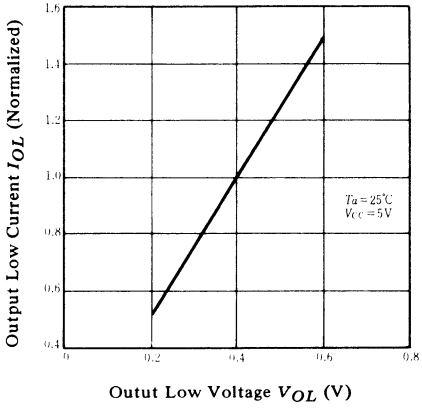
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

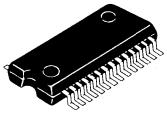


HM6264FP-12,HM6264FP-15

8192-word x 8-bit High Speed Static CMOS RAM

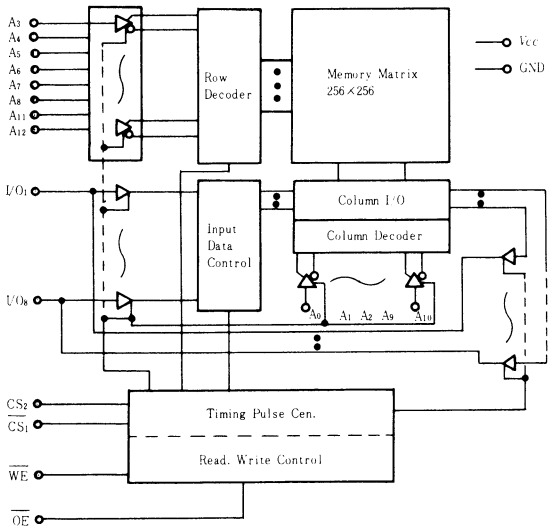
■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

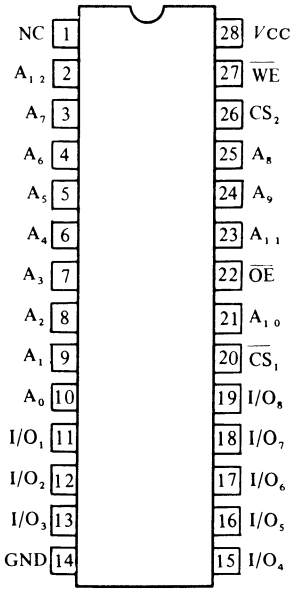


(FP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

HITACHI

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	0.02	2	mA
	I_{SB2}**	CS2≦0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

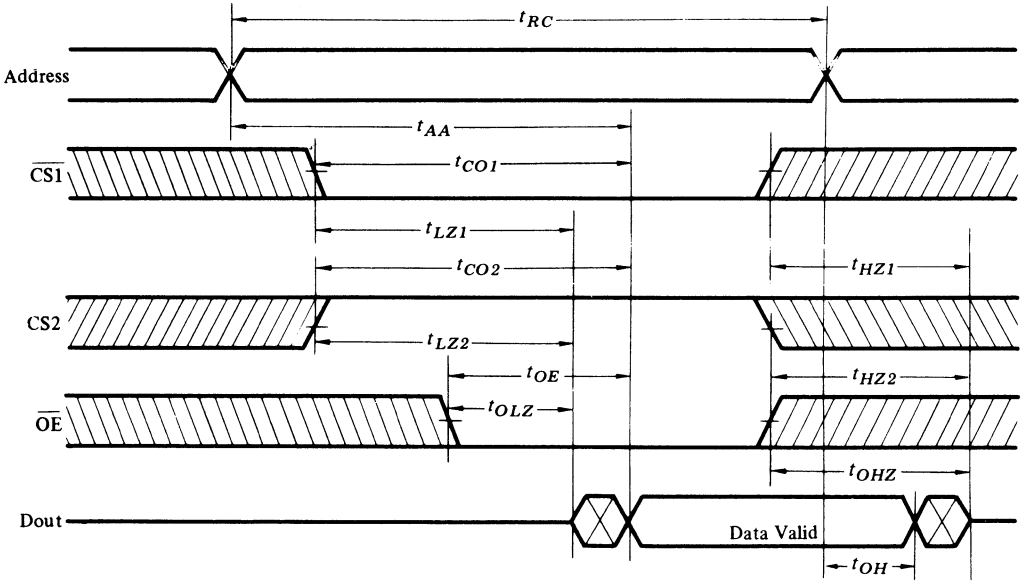
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264FP-12		HM6264FP-15		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	120	–	150	–	ns
Address Access Time		t_{AA}	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	120	–	150	ns
	CS2	t_{CO2}	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50	ns
	CS2	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

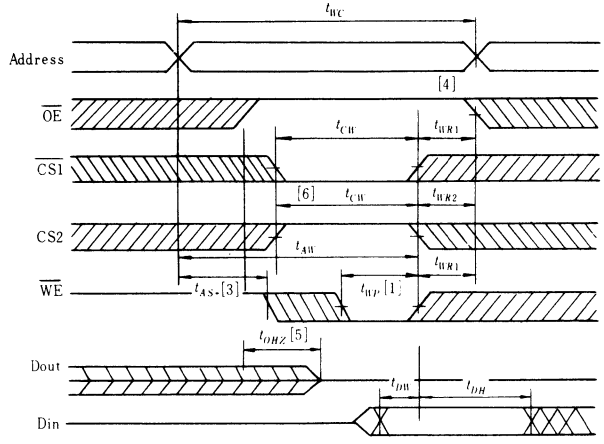


NOTE: 1) $\overline{WE}$ is high for Read Cycle

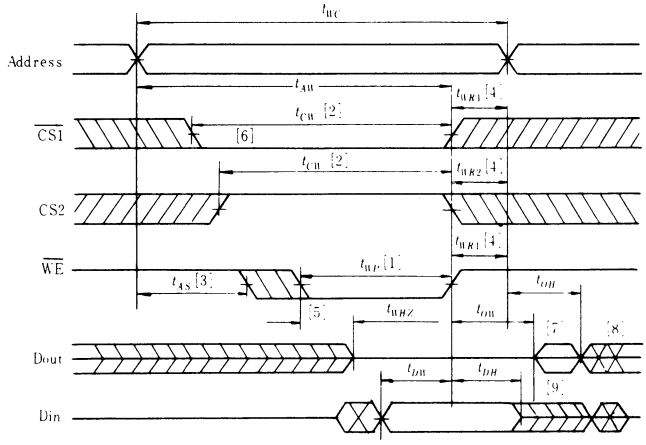
• WRITE CYCLE

Item		Symbol	HM6264FP-12		HM6264FP-15		Unit
			min	max	min	max	
Write Cycle Time		t_{WC}	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	85	–	100	–	ns
Write Pulse Width		t_{WP}	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	55	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	ns
Write to Outputiin High Z		t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	ns
OE to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



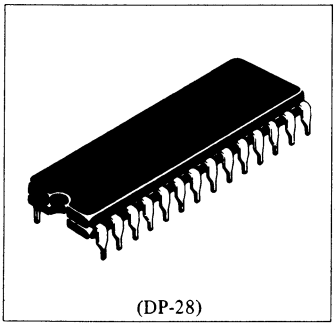
NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

HM6264LP-10, HM6264LP-12
HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

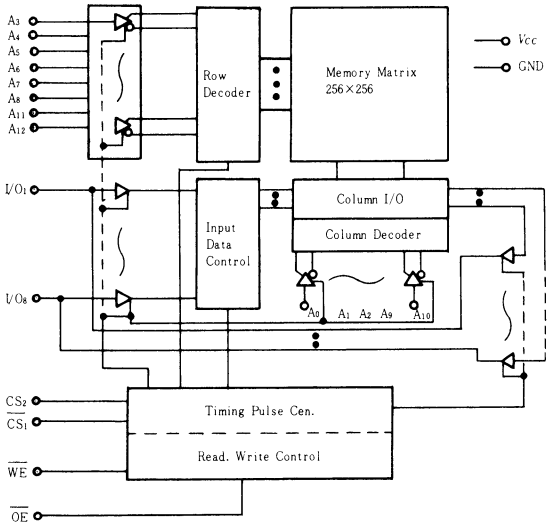
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

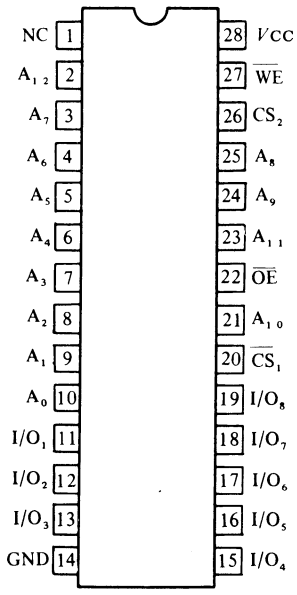


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

HITACHI

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}\geqq V_{CC}-0.2V$, CS2$\geqq V_{CC}-0.2V$ or CS2$\leqq$0.2V	–	2	100	μA
	I_{SB2}**	CS2$\leqq$0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

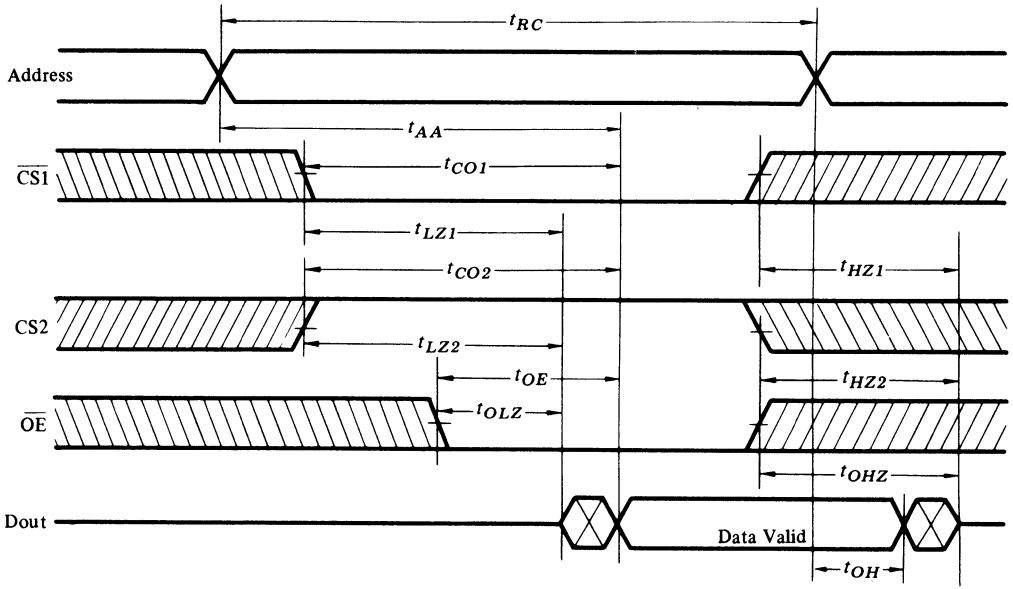
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

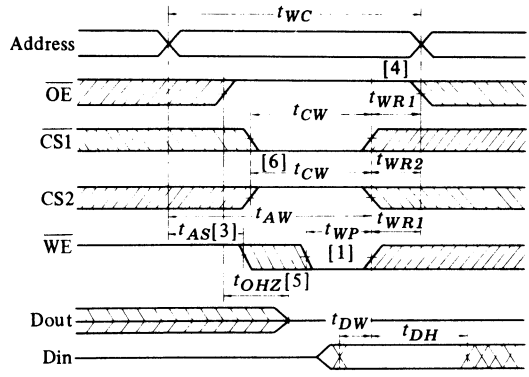


NOTE : 1) $\overline{WE}$ is high for Read Cycle

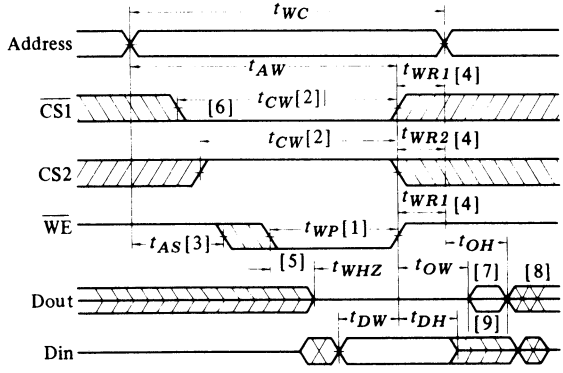
• **WRITE CYCLE**

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



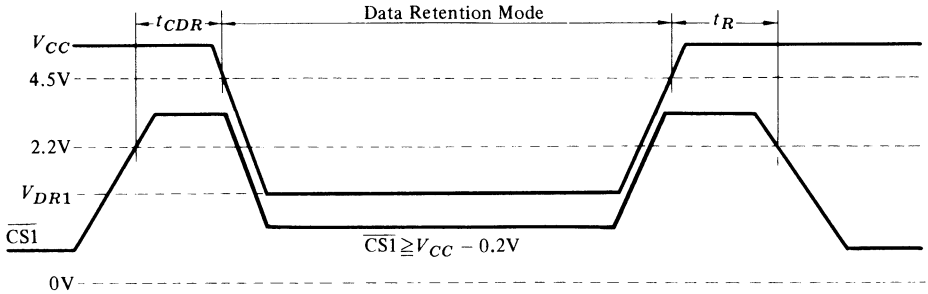
NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

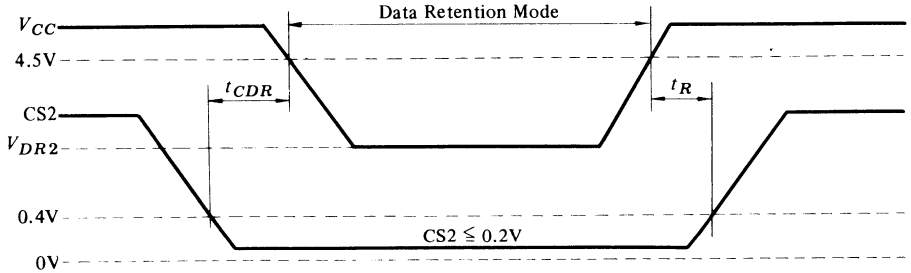
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	–	1	50*	μA
	I_{CCDR2}	V_{CC} = 3.0V, $CS2 \leqq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = -0.3V, 20μA max at T_a=0~40°C
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

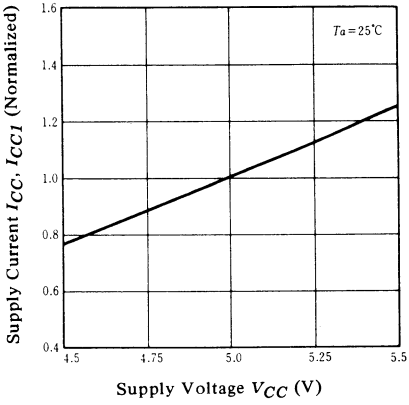


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

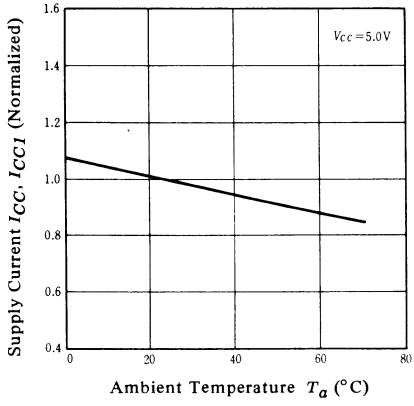


NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq Vcc - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

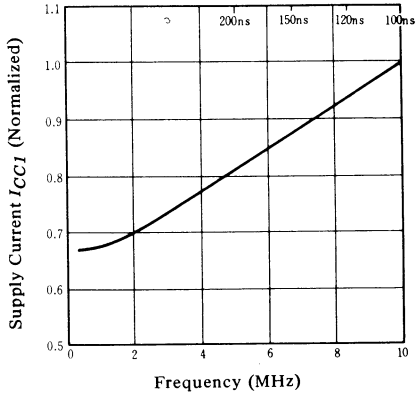
SUPPLY CURRENT vs. SUPPLY VOLTAGE



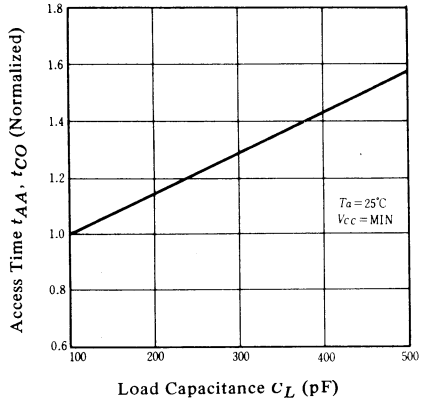
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



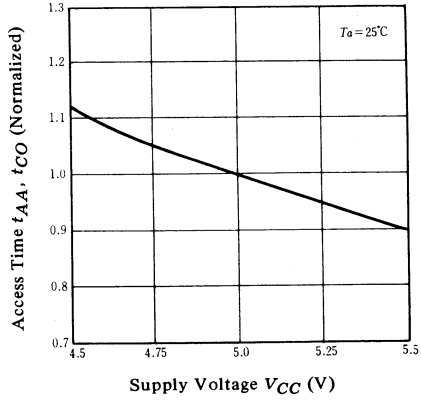
SUPPLY CURRENT vs. FREQUENCY



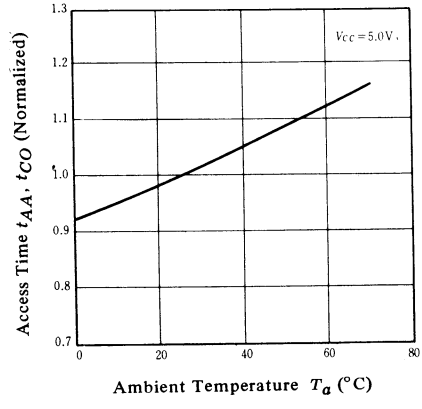
ACCESS TIME vs. LOAD CAPACITANCE



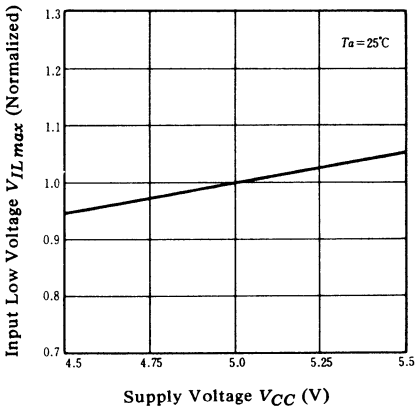
ACCESS TIME vs. SUPPLY VOLTAGE



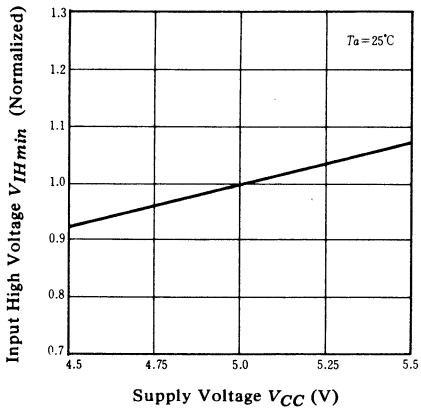
ACCESS TIME vs. AMBIENT TEMPERATURE



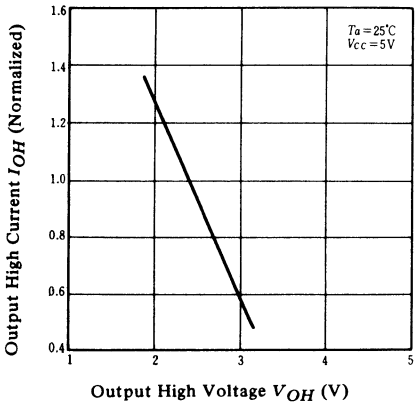
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



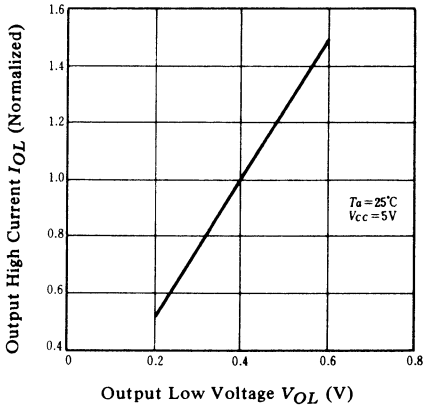
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



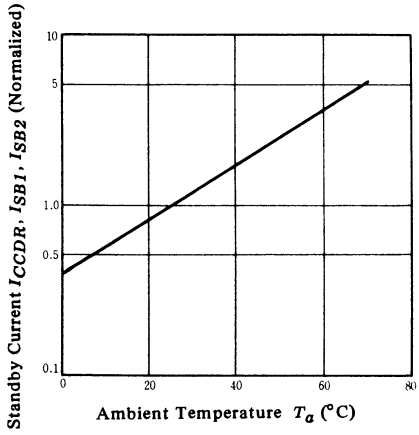
OUTPUT CURRENT vs. OUTPUT VOLTAGE



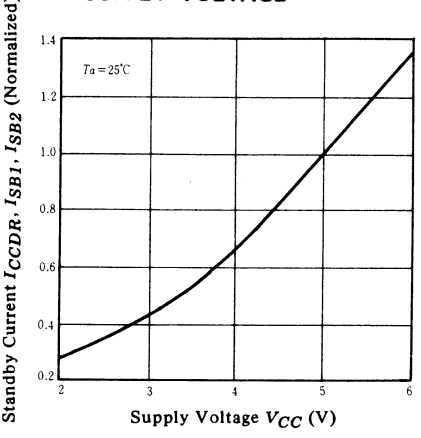
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE

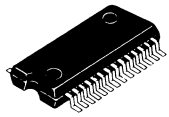


HM6264LFP-12,HM6264LFP-15

8192-word x 8-bit High Speed Static CMOS RAM

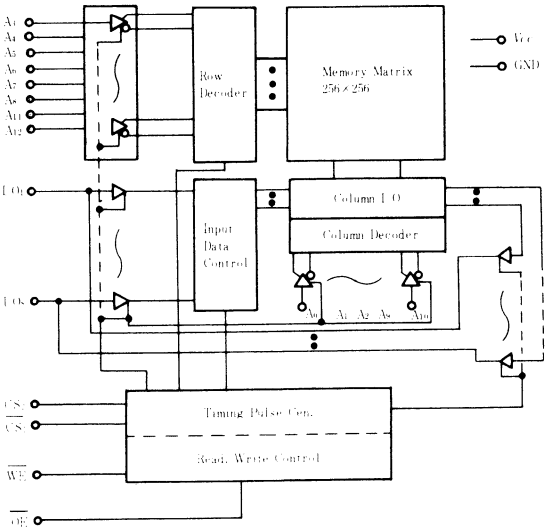
■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
  Standby: 10μW (typ.), Operation: 200mW (typ.)
- Capability of Battery Back-up Operation
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

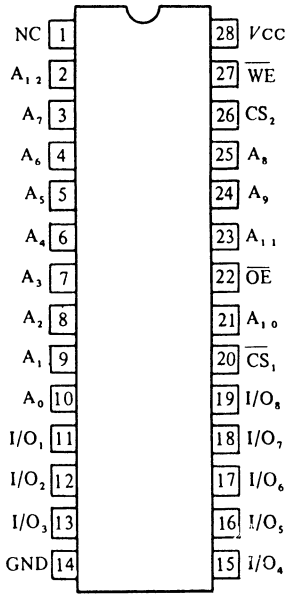


(FP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND or V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	2	100	μA
	I_{SB2}**	CS2≦0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

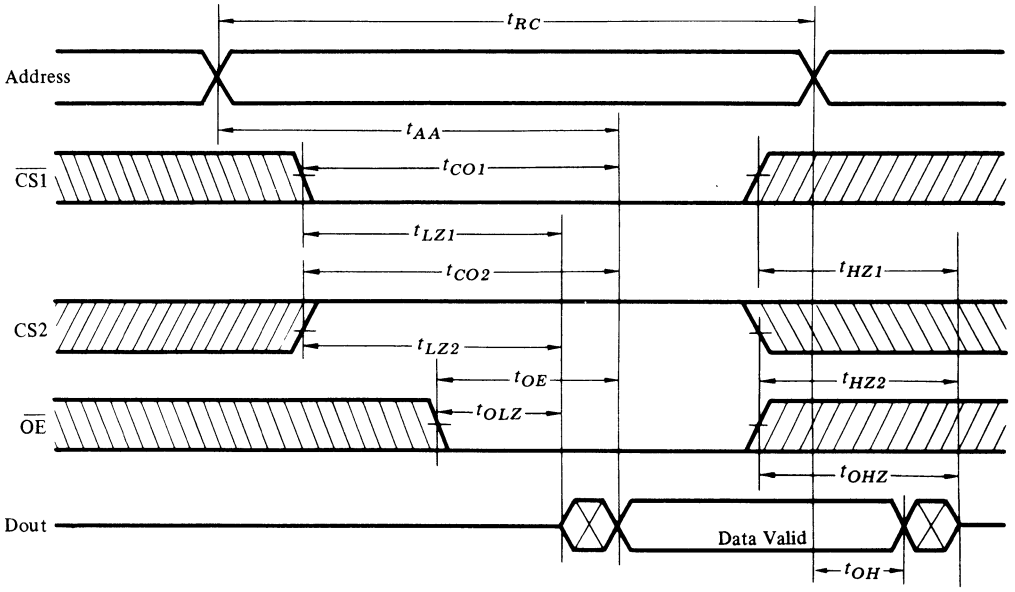
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	120	–	150	–	ns
Address Access Time		t_{AA}	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	120	–	150	ns
	CS2	t_{CO2}	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50	ns
	CS2	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

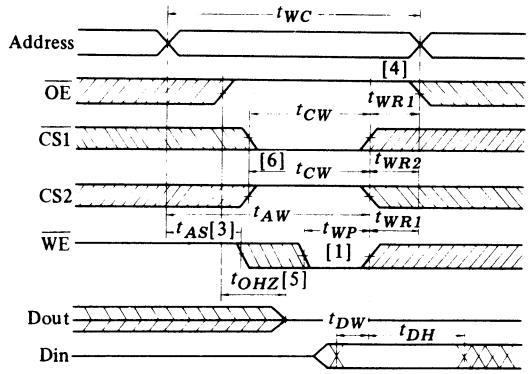


NOTE : 1) $\overline{WE}$ is high for Read Cycle

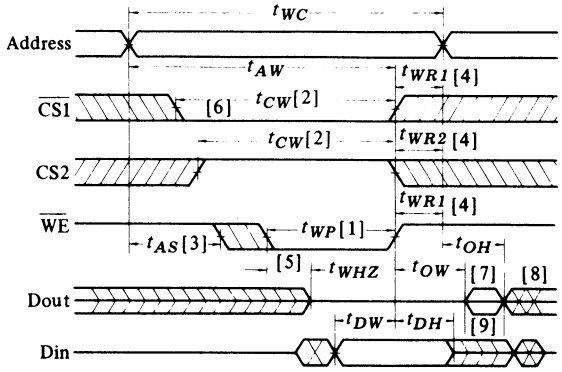
• **WRITE CYCLE**

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Write Cycle Time		t_{WC}	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	85	–	100	–	ns
Write Pulse Width		t_{WP}	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	ns
OE to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



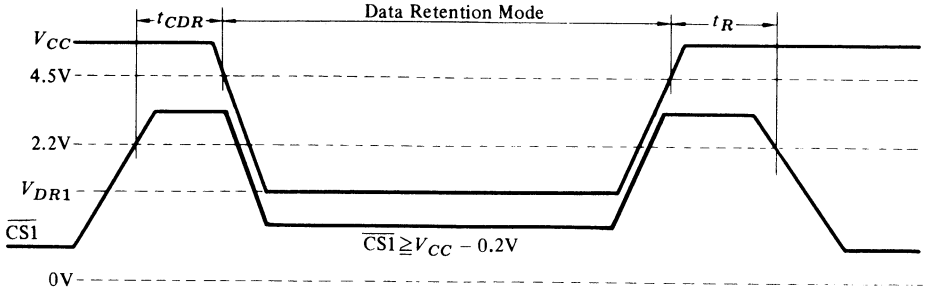
NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

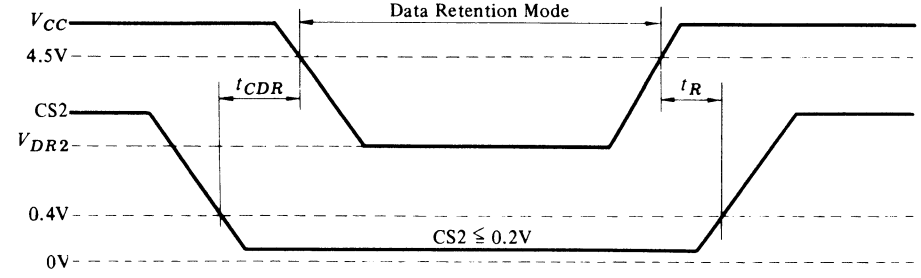
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	–	1	50*	μA
	I_{CCDR2}	V_{CC} = 3.0V, $CS2 \leqq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = −0.3V, 20μA max at T_a = 0 ~ 40°C.
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq Vcc - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM6287P/HM6287CG Series

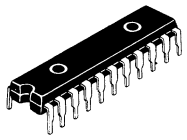
Under Development

65536-word x 1-bit High Speed Static CMOS RAM

■ FEATURES

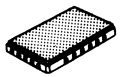
- High Speed: Fast Access Time 55/70ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 300mW (typ.)
- Single 5V Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Output

HM6287P-55, HM6287P-70



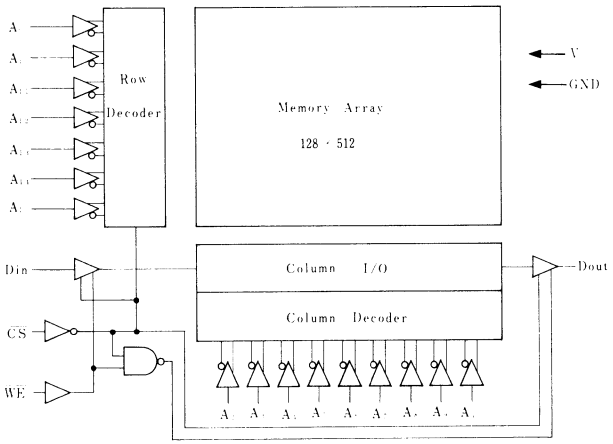
(DP-22A)

HM6287CG-55, HM6287CG-70



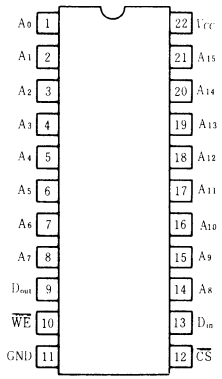
(CG-22)

■ BLOCK DIAGRAM



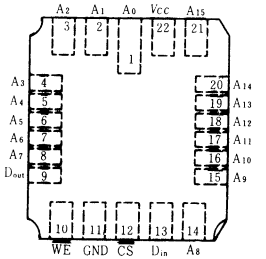
■ PIN ARRANGEMENT

- HM6287P Series



(Top View)

- HM6287CG Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature**	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. $V_{T\ min}$ = −3.5V (Pulse width 20ns)
** −55 to +125°C for Plastic DIP

HITACHI

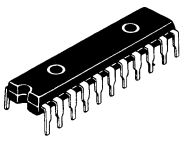
HM6287LP Series

Under Development

65536-word x 1-bit High Speed Static CMOS RAM

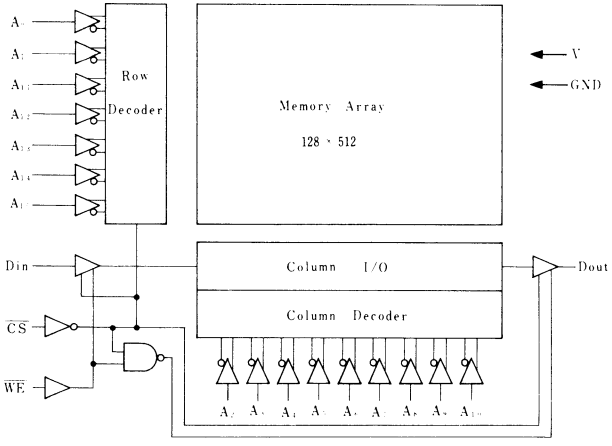
■ FEATURES

- High Speed: Fast Access Time 55/70ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 10μW (typ.), Operation: 300mW (typ.)
- Capability of Battery Back-up Operation
- Single 5V Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Output

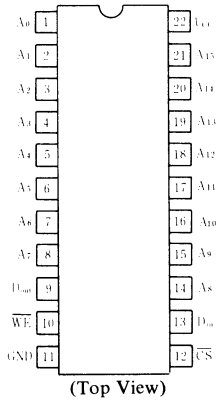


(DP-22A)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

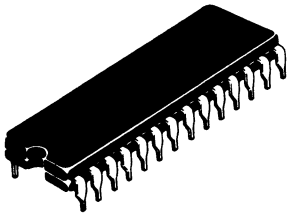
* with respect to GND. V_T min = −3.5V (Pulse width 20ns)

HM65256P Series

Under Development

32768-word x 8-bit High Speed Pseudo Static CMOS RAM

The HM65256P is a 32,768-words x 8-bits, high speed, pseudo static CMOS Random Access memory.
This new breed of pseudo static RAM utilizes HITACHI's double-layers CMOS technology and advanced circuit techniques for high performance and high functional density.
The HM65256P is offered in a standard 600 mil 28 pin dual-in-line plastic package, and guaranteed for operation from 0°C to 70°C at the condition of 5-V single power supply with ±10% tolerances.
All inputs and outputs are compatible with high performance logic families, such as Schottky TTL.
As for refresh functions, including address refresh, refresh control function available on 22 pin provides automatic and self-refresh modes.



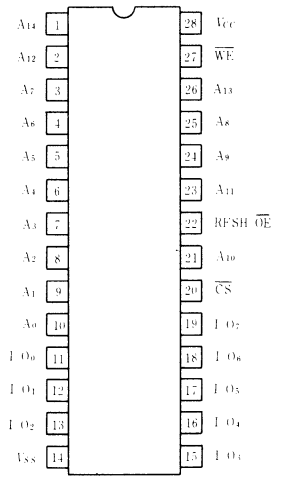
(DP-28)

■ FEATURES

- Organized as 32768-words x 8-bits
- Single 5V Power Supply
- High Speed · · · · · Access Time 150/200ns (max).
- Control on Pin-22 for automatic and self reflesh
- Equal access and cycle time
- All inputs and outputs TTL compatible
- 22 pin function

$\overline{CS}$	$\overline{OE}$/RFSH
H	RFSH
L	$\overline{OE}$

■ PIN ARRANGEMENT



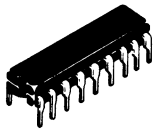
(Top View)

MOS DYNAMIC RAM

HM48416AP-12, HM48416AP-15
HM48416AP-20

16384-word × 4-bit Dynamic Random Access Memory

HM48416AP-12, HM48416AP-15, HM48416AP-20

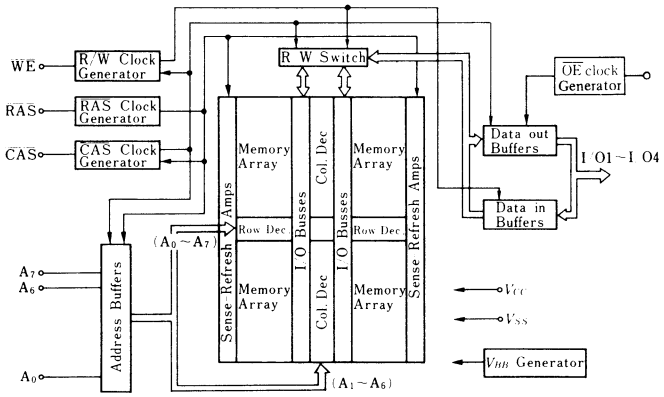


(DP-18)

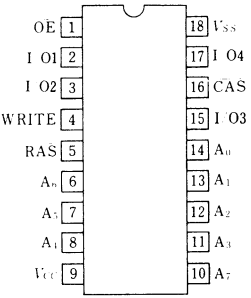
■ FEATURES

- 16384-word x 4-bit Organization
- Single 5V (±10%)
- Low Power; 303mW Active, 20mW Standby
- High speed: Access Time 120ns/150ns/200ns (max)
- Page mode capability
- Output data controlled by $\overline{CAS}$, $\overline{OE}$
- TTL compatible
- 128 refresh cycles ($A_0 \sim A_6$, 2ms)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

A0~A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1~I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperatue	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a =0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.5	V
	V_{IL}	−1.0	–	0.8	V

Note All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Paramater	Smbol	HM48416AP -12		HM48416AP -15		HM48416AP -20		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	–	60	–	55	–	45	mA	1, 2
Standby Current ($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	–	3.5	–	3.5	–	3.5	mA	
Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min)	I_{CC3}	–	42	–	38	–	33	mA	2
Standby Current ($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	–	5.5	–	5.5	–	5.5	mA	1
Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling; t_{PC}=min)	I_{CC6}	–	42	–	38	–	33	mA	1, 2
Input Leakage (0< V_{in} <6.5V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage (Dout is disabled, 0< V_{out}<5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output Levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address	C_{in1}	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$	C_{in2}	–	10	pF	1
Output Capacitance	Data In/Data out	$C_{I/O}$	–	10	pF	1, 2

Notes) 1. Capacitance mesured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10)]

Parameter	Symbol	HM48416AP-12		HM48416AP-15		HM48416AP-20		Unit	Note
		min	mas	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	230	–	260	–	330	–	ns	
Read-Write Cycle Time	t_{RWC}	320	–	360	–	450	–	ns	
Page Mode Cycle Time	t_{PC}	130	–	145	–	190	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	35	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	100	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	–	−10	–	−10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	

(to be continued)

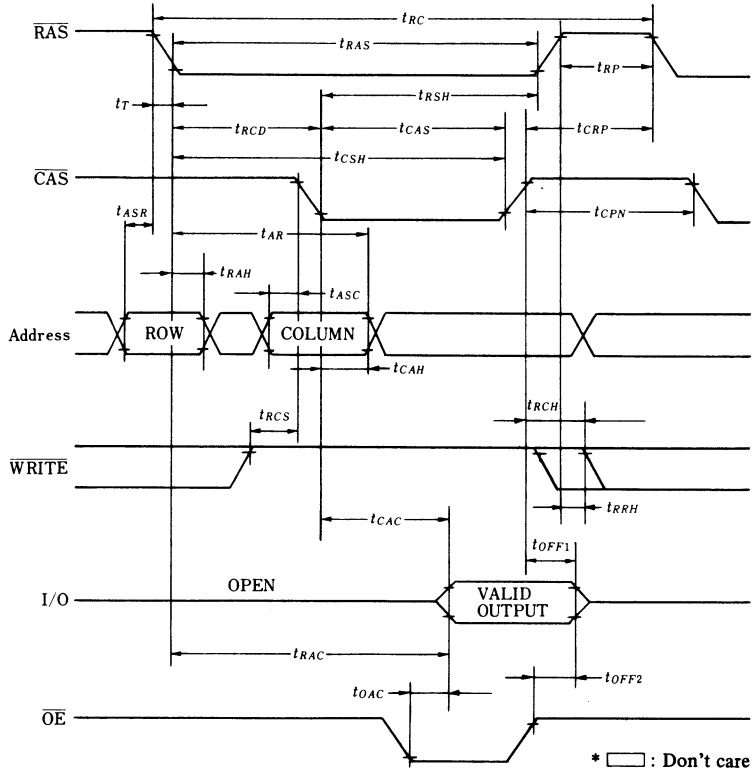
Parameter	Symbol	HM48416AP-12		HM48416AP-15		HM48416AP-20		Unit	Note
		min	max	min	max	min	max		
Write Command Hold Time refferenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time refferenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time refferenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time refferenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	2	–	2	–	2	ms	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	105	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	165	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	–	60	–	80	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	35	–	40	–	50	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	35	–	40	–	50	ns	3
Output Buffer Turn-off Delay refferenced to $\overline{OE}$	t_{OFF2}	–	35	–	40	–	50	ns	5
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	35	–	40	–	50	–	ns	11

Notes:

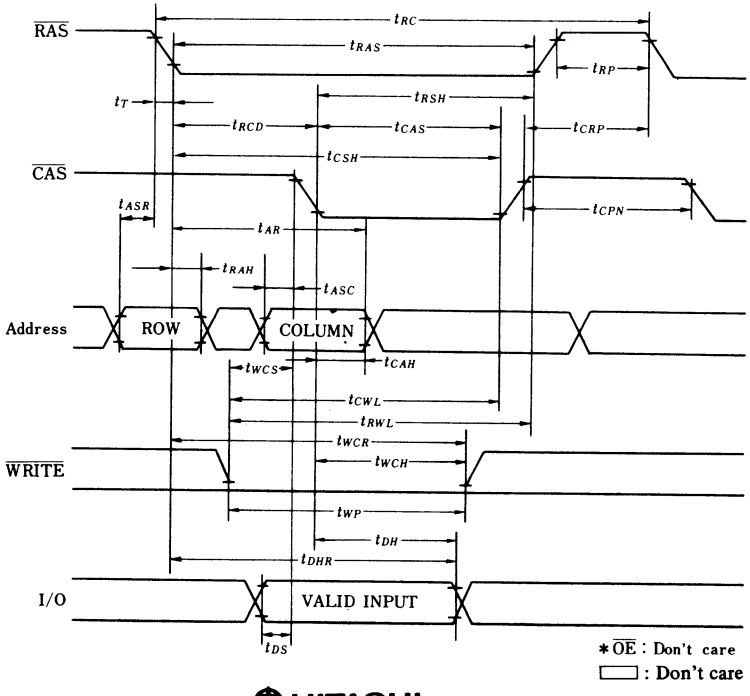
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF1} (max) and t_{OFF2} (max) define the time at which the output achieves the open circuit condition.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC}(max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write cycle and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
11. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

■ TIMING WAVEFORMS

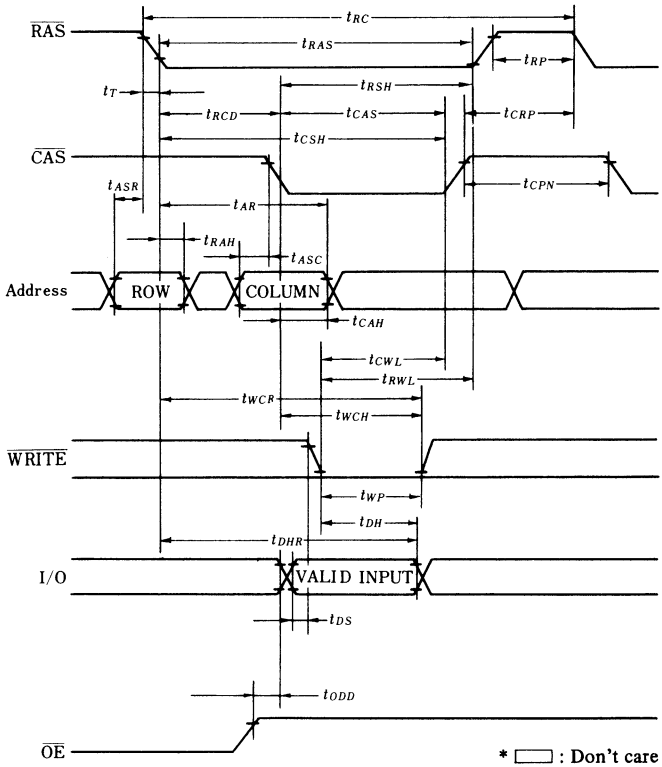
● Read Cycle



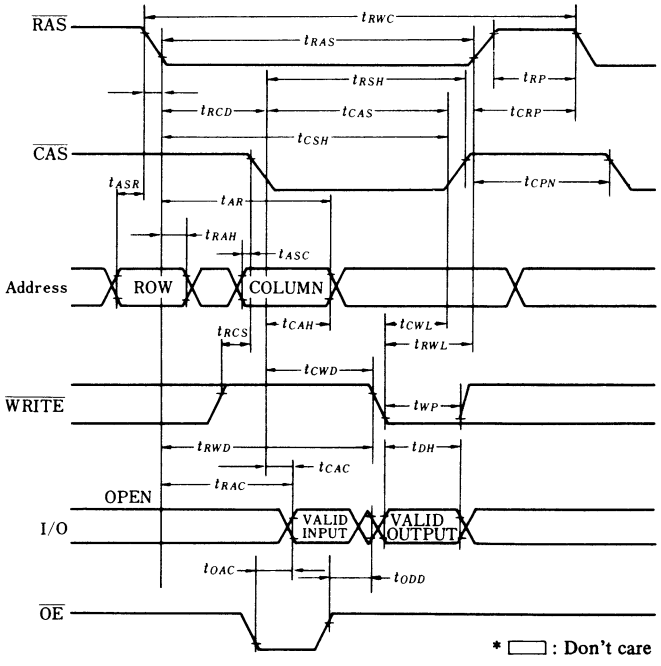
● Early Write Cycle



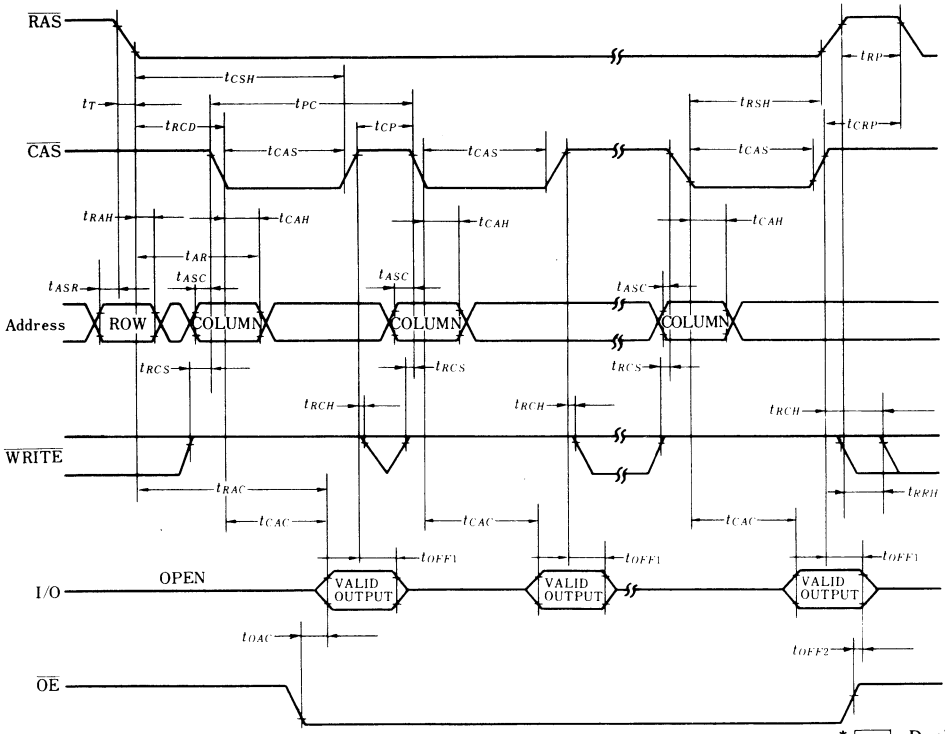
- **Delayed Write Cycle**



- **Read Modify Write Cycle**

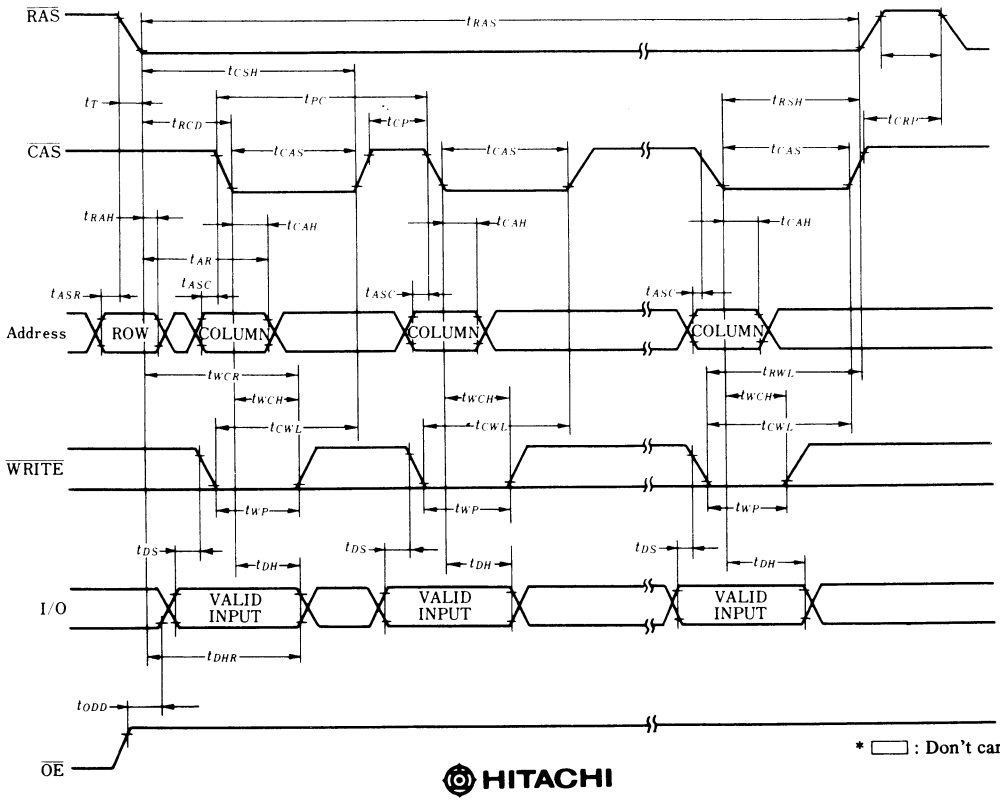


- **Page Mode Read Cycle**



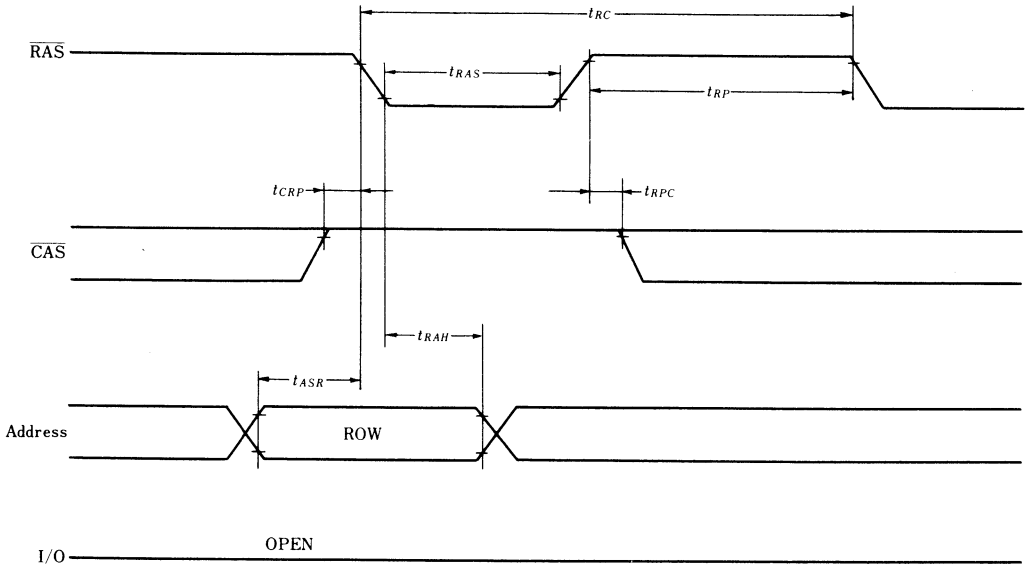
* ☐ : Don't care

- **Page Mode Write Cycle**



* ☐ : Don't care

- **$\overline{RAS}$ Only Refresh Cycle**



* $\overline{OE}$, $\overline{WE}$: Don't care
▭ : Don't care

HM4864-2, HM4864-3
HM4864P-2, HM4864P-3

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

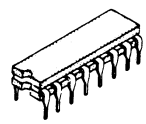
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh.

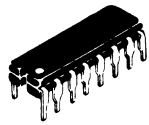
Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

HM4864-2, HM4864-3



(DG-16A)

HM4864P-2, HM4864P-3

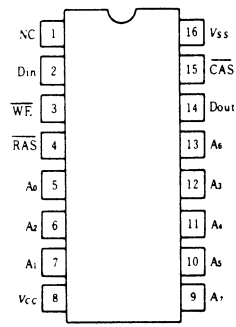


(DP-16)

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- 128 refresh cycle

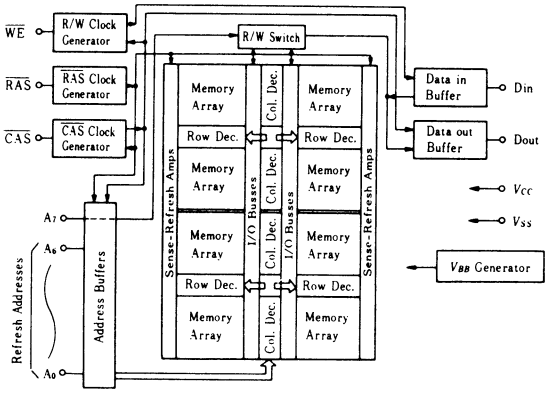
■ PIN ARRANGEMENT



(Top View)

A_0-A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_6	Refresh Address Input

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . . -65 to +150°C (Cerdip)
-55 to +125°C (Plastic)
Short-circuit Output Current . 50 mA
Power Dissipation . . . . . 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC}=min.)	I_{CC1}	—	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, Dout = High Impedance)	I_{CC2}	—	3.5	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; t_{RC}=min.)	I_{CC3}	—	45	mA	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC}=min.)	I_{CC4}	—	45	mA	2, 4
INPUT LEAKAGE Input Leakage Current, any Input (V_{in}=0 to +6.5V, all other pins not under test=0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, V_{out}=0 to +5.5V)	I_{LO}	−10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{out}=−5mA) Output Low (Logic 0) Voltage (I_{out}=4.2mA)	V_{OH} V_{OL}	2.4 0	V_{CC} 0.4	V V	

NOTES
1. All voltages referenced to V_{SS}.
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (A0-A7, Din)	C_{in1}	—	7	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	—	10	pF	1
Output Capacitance (Dout)	C_{out}	—	7	pF	1, 2

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1], [2]

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

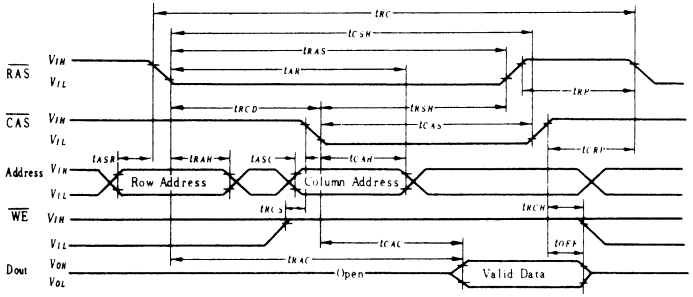
Parameter	Symbol	HM4864-2/P-2		HM4864-3/P-3		Unit	Notes
		min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	270	—	335	—	ns	
Read-Write Cycle Time	t_{RWC}	270	—	335	—	ns	
Page Mode Cycle Time	t_{PC}	170	—	225	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	150	—	200	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	100	—	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	—	135	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	—	135	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	—	200	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	65	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	—	−20	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	ns	
Column Address Set-up Time	t_{ASC}	−10	—	−10	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	95	—	120	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	—	120	—	ns	
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	55	—	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	—	120	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Refresh Period	t_{REF}	—	2	—	2	ms	
Write Command Set-up Time	t_{WCS}	−20	—	−20	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	80	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110	—	145	—	ns	10
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	ns	

NOTES

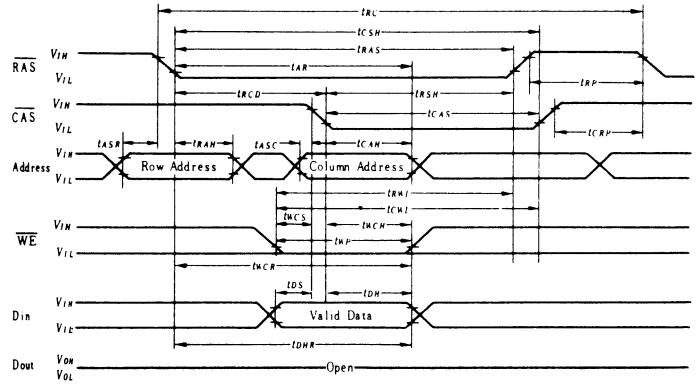
1. AC measurements assume t_T = 5ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. These parameters are reference to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

■ TIMING WAVEFORMS

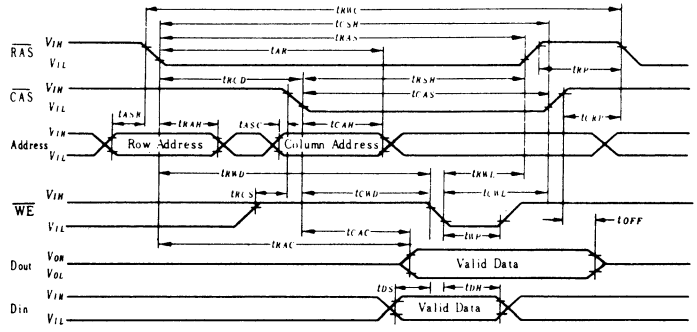
● READ CYCLE



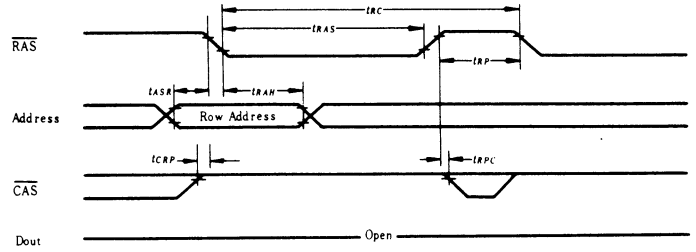
● WRITE CYCLE



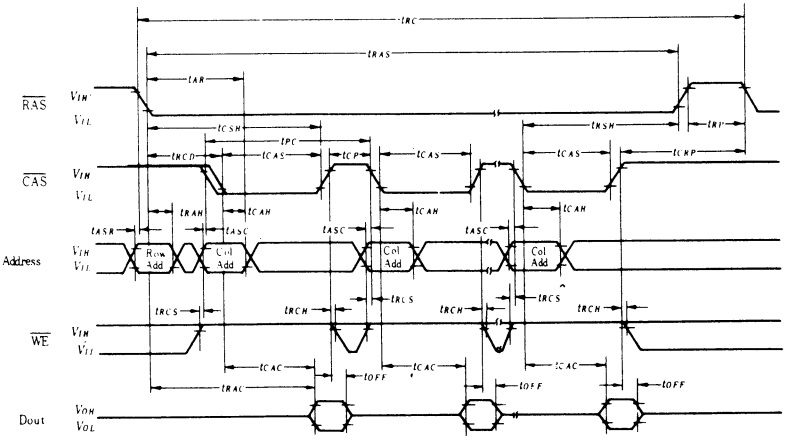
● READ-WRITE/READ-MODIFY-WRITE CYCLE



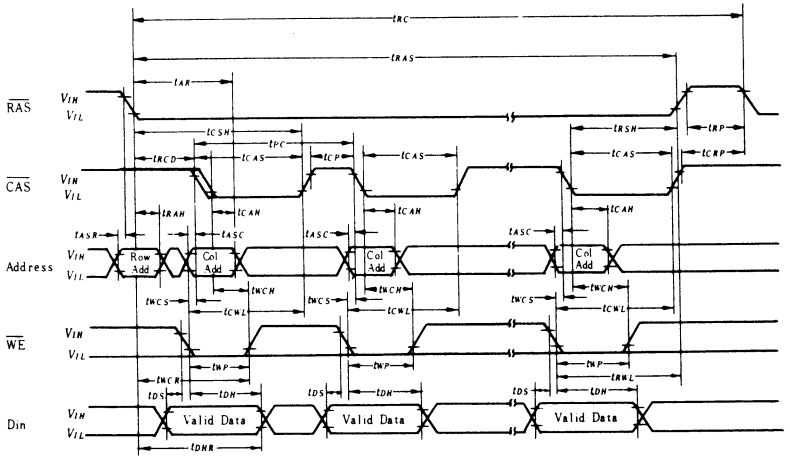
● "$\overline{RAS}$-ONLY" REFRESH CYCLE



● PAGE MODE READ CYCLE

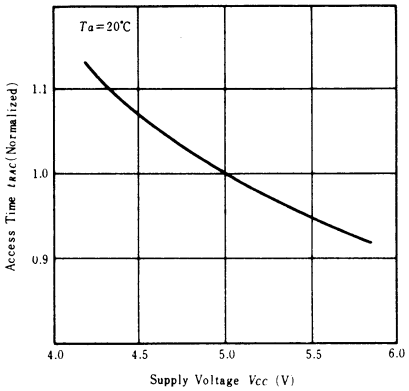


● PAGE MODE WRITE CYCLE

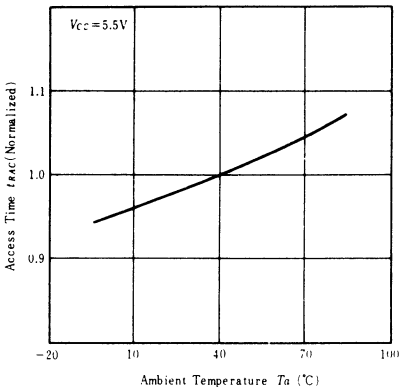


■ TYPICAL CHARACTERISTICS

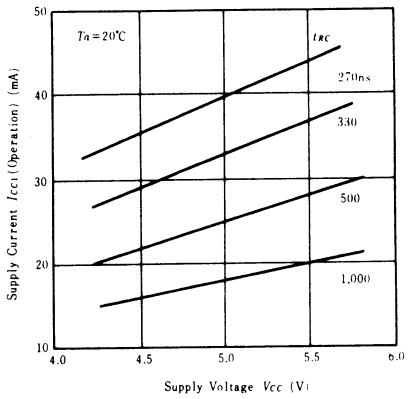
ACCESS TIME vs. SUPPLY VOLTAGE



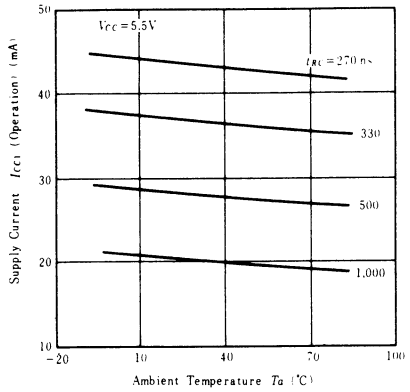
ACCESS TIME vs. AMBIENT TEMPERATURE



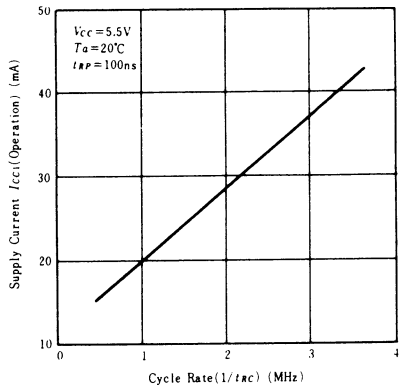
SUPPLY CURRENT vs. SUPPLY VOLTAGE



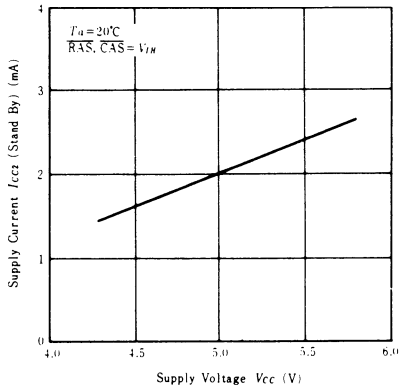
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



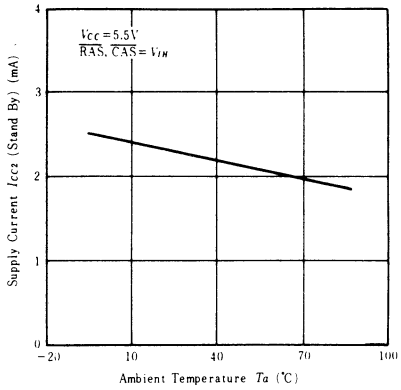
SUPPLY CURRENT vs. CYCLE RATE



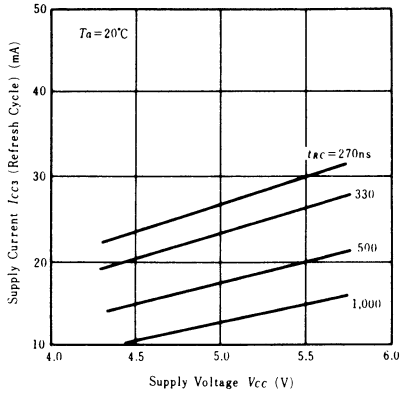
SUPPLY CURRENT vs. SUPPLY VOLTAGE



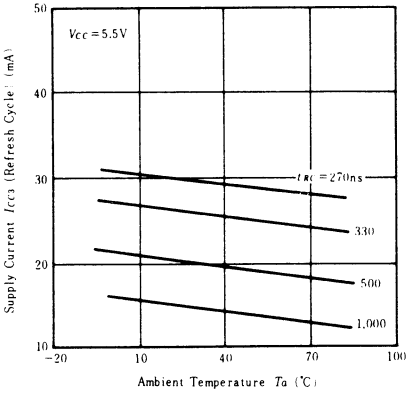
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



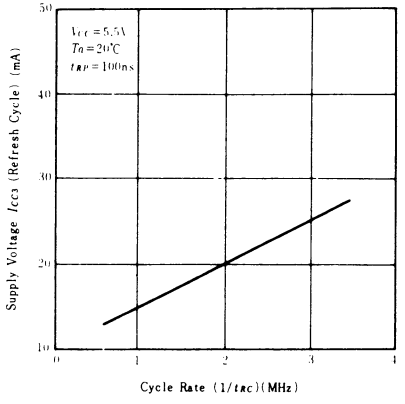
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



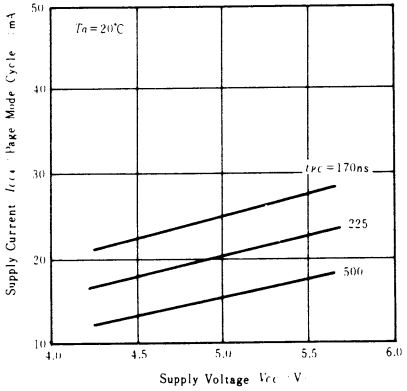
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



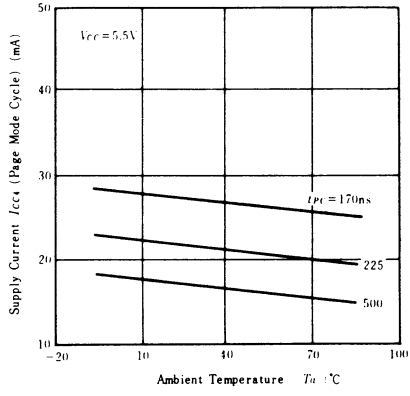
SUPPLY CURRENT
vs. CYCLE RATE



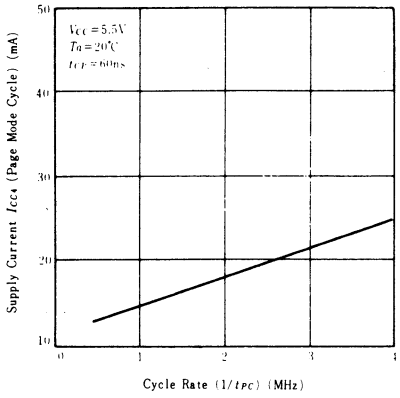
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



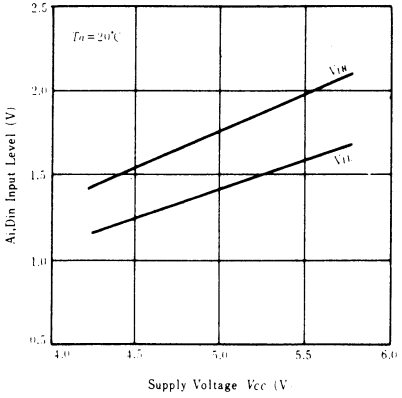
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



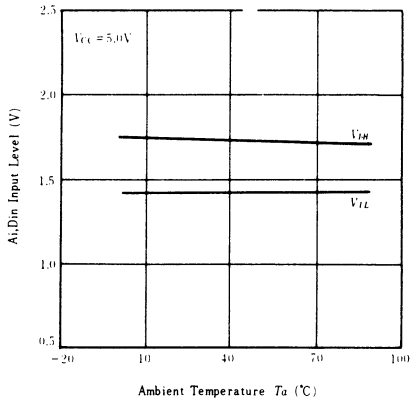
SUPPLY CURRENT vs. CYCLE RATE



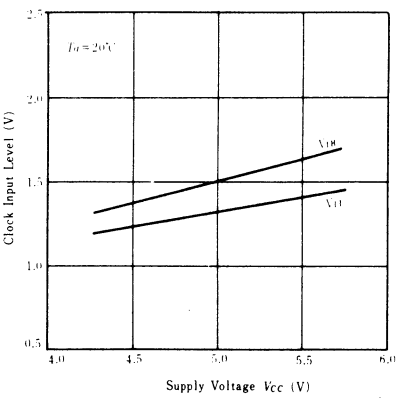
INPUT LEVEL vs. SUPPLY VOLTAGE



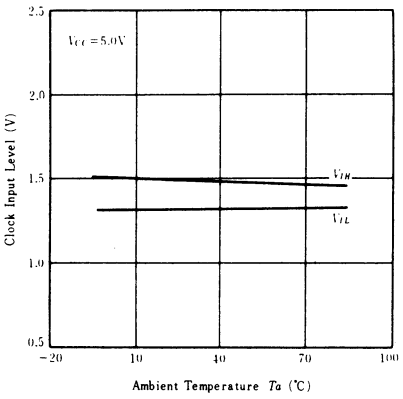
INPUT LEVEL vs. AMBIENT TEMPERATURE

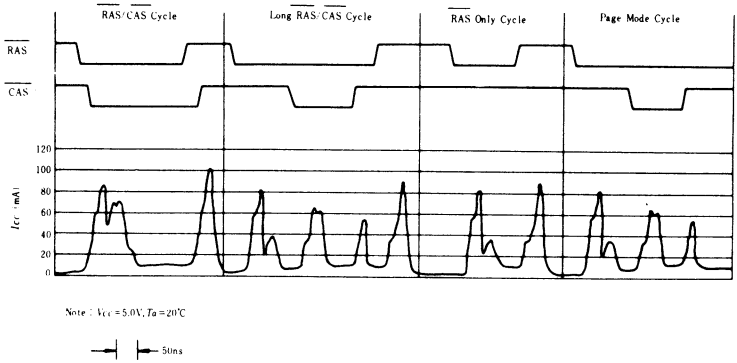


CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE





■ APPLICATION INFORMATION

●POWER ON

An initial pause of 500 μs is required after power-up and a minimum of eight (8) initialization cycle,(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) must follow an initial pause.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of V_{CC}, as shown in Fig. 1.

●READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter t_{ASR}.

Following the time when $\overline{RAS}$ reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH}. Following this interval, the address can be changed from row address to column address. When the column address is stable, $\overline{CAS}$ can be turned on. The leading edge of $\overline{CAS}$ is controlled by parameter t_{RCD}. The basic limit on the $\overline{CAS}$ leading edge is that $\overline{CAS}$ can not start until the column address is stable, and this is controlled by parameter t_{ASC}. The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH}. Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than t_{RCD} (max), the access time from $\overline{RAS}$ will be increased by the time which t_{RCD} exceeds t_{RCD} (max).

Following the time when $\overline{CAS}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC}-access time from $\overline{CAS}$.

The access time from $\overline{RAS}$–t_{RAC}–is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of t_{RAC} is derived as the sum of t_{RCD} (max) and t_{CAC}.

The selected output data is held valid internally until $\overline{CAS}$ becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF}.

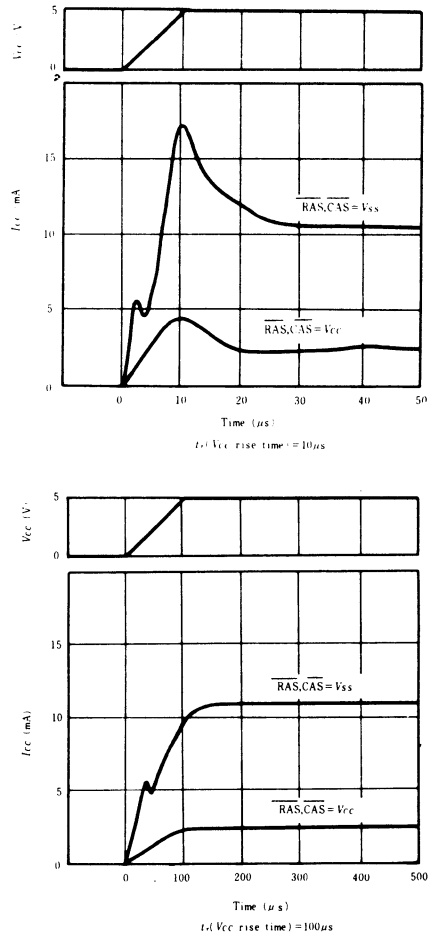


Fig. 1 I_{CC} vs. V_{CC} during power up.

• WRITE CYCLE

A write cycle is performed by bringing $\overline{WE}$ low before or during $\overline{CAS}$-on.

Two different write cycles can be defined as;

Write cycle—Write data are available at the beginning of the $\overline{CAS}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{WE}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{WE}$ reaches its low level, $\overline{WE}$ must be held stable long enough to be captured. This $\overline{WE}$-on pulse deration is called t_{WP}. The time required to capture write data in a latch is called t_{DH}. This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

$\overline{WE}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{WE}$ become critical path signals for determining cycle time.

• CLOCK-OFF TIMING

$\overline{RAS}$ and $\overline{CAS}$ must stay on for Dout stabilized to valid data. In the case of $\overline{CAS}$, this is controlled by parameter t_{CAS} (min).

In the case of $\overline{RAS}$, this is controlled by parameter t_{CAS} (min). Following the end of $\overline{RAS}$, $\overline{CAS}$ must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP}. Normally $\overline{CAS}$ is not required to be off for minimum time of t_{CRP}. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time.

• DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CAS}$ is high, Dout is in a high impedance state. When $\overline{CAS}$ is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

• REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{IL} or V_{IH} is permitted for A7. Any cycle in which $\overline{RAS}$ signal occurs refreshes the entire selected row. $\overline{RAS}$-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

• PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{RAS}$ at a logic low throughout all successive $\overline{CAS}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

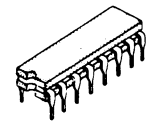
HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

65536-word × 1-bit Dynamic Random Access Memory

■ FEATURES

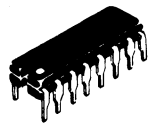
- Industry standard 16- Pin DIP (plastic, Cerdip)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120ns / 150ns / 200ns
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by $\overline{CAS}$
- TTL compatible
- 128 refresh cycles – (2ms)
- Hidden refresh capability

HM4864A-12, HM4864A-15, HM4864A-20



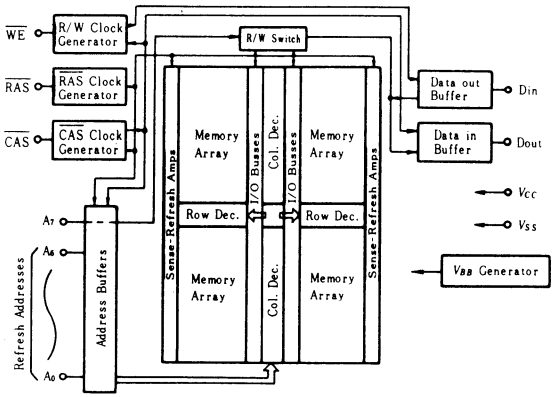
(DG-16B)

HM4864AP-12, HM4864AP-15, HM4864AP-20

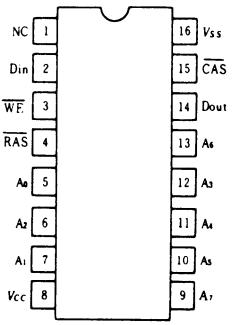


(DP-16)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	−1V to 7V
Operating temperature, Ta (Ambient)	0°C to 70°C
Storage temperature (Cerdip)	−65°C to 150°C
Storage temperature (Plastic)	−55°C to 125°C
Power dissipation	1 W
Short circuit output current	50 mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

Notes : 1. All voltages referenced to V_{SS}

A0–A7	:	Address Inputs
$\overline{CAS}$	:	Column Address Strobe
Din	:	Data In
Dout	:	Data Output
$\overline{RAS}$	:	Row Address Strobe
$\overline{WE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
A0–A6	:	Refresh Address Inputs

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM4864A/P-12		HM4864A/P-15		HM4864A/P-20		Unit	Notes
		min	max	min	max	min	ma x		
Operating Current($\overline{RAS}$,$\overline{CAS}$ Cycling:t_{RC}=min)	I_{CC1}	—	55	—	50	—	44	mA	1,2
Standby Cnrrent($\overline{RAS}$=V_{IH},Dout=High Impedance)	I_{CC2}	—	3.5	—	3.5	—	3.5	mA	
Refresh Current($\overline{RAS}$ Cycling,$\overline{CAS}$=V_{IH},t_{RC}=min)	I_{CC3}	—	42	—	38	—	33	mA	2
Standby Current($\overline{RAS}$=V_{IH},Dout Enable)	I_{CC5}	—	5.5	—	5.5	—	5.5	mA	1
Page Mode Current($\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling;t_{PC}=min)	I_{CC6}	—	38	—	35	—	31	mA	1,2
Input Leakage(0<V_{out}<6.5V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage(Dout is disabled,0<V_{out}<5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output Levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Current depends on cycle rate : maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	A_0~A_7, Din	C_{in1}	—	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{in2}	—	10	pF	1
Output Capacitance	Dout	C_{out}	—	7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

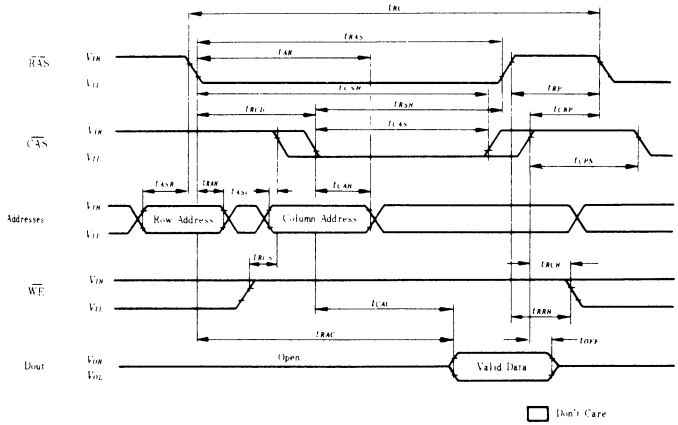
Parameter	Symbol	HM4864A-12		HM4864A-15		HM4864A-20		Unit	Notes
		min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	35	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	—	−10	—	−10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	2	—	2	—	2	ms	
Read-Write Cycle Time	t_{RWC}	245	—	280	—	345	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	—	45	—	55	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	120	—	155	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30	—	35	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

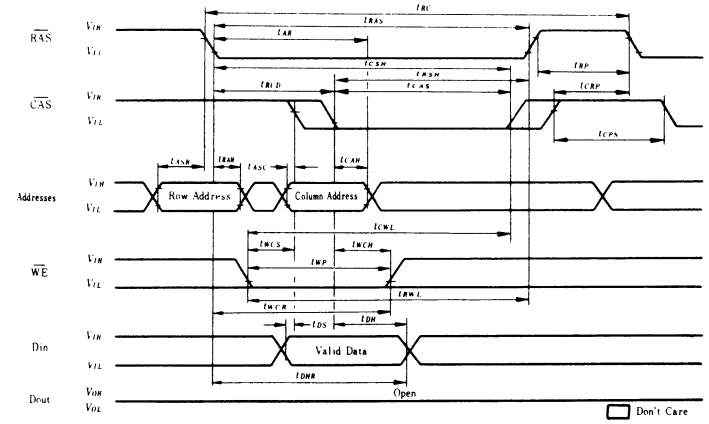
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet is electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. There parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge is delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

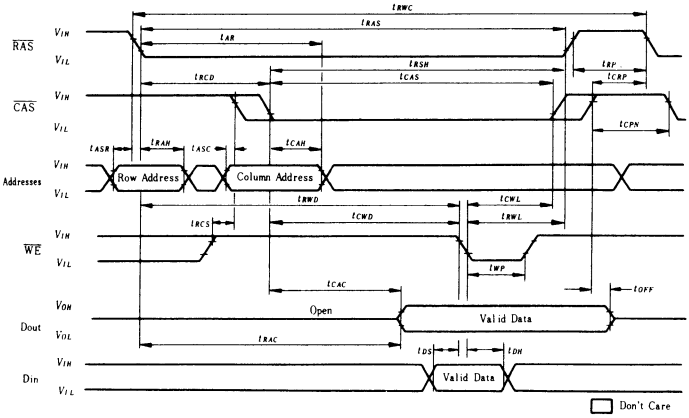
● READ CYCLE



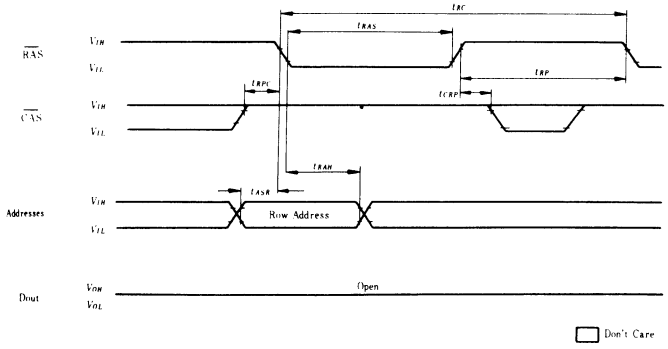
● WRITE CYCLE (EARLY WRITE)



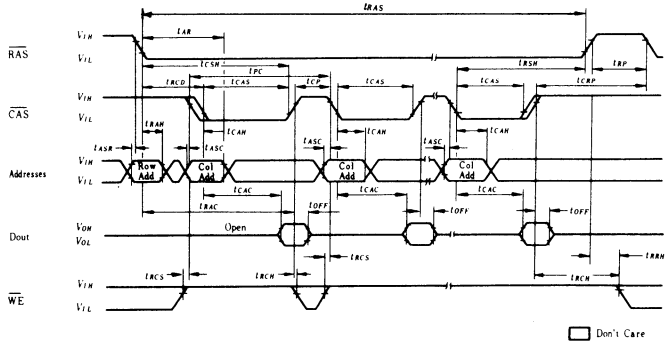
● READ-WRITE/READ-MODIFY-WRITE CYCLE



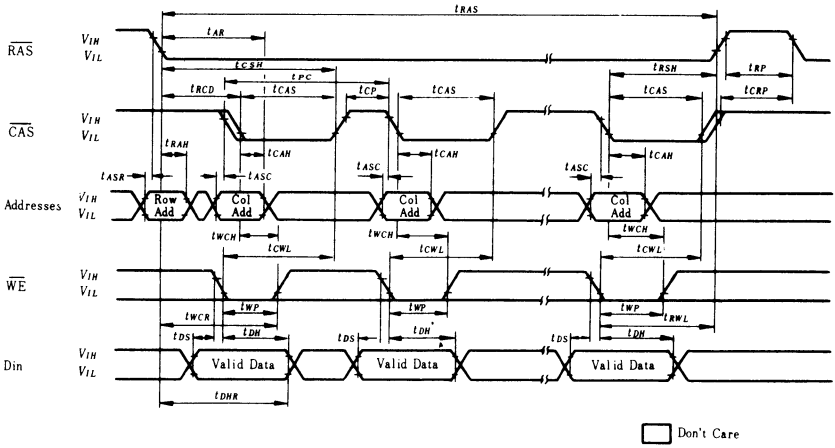
● "RAS-ONLY" REFRESH CYCLE



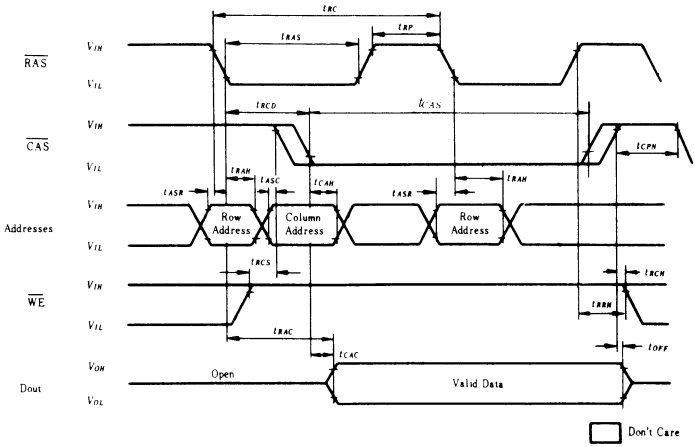
● PAGE MODE READ CYCLE



●PAGE MODE WRITE CYCLE



●HIDDEN REFRESH CYCLE

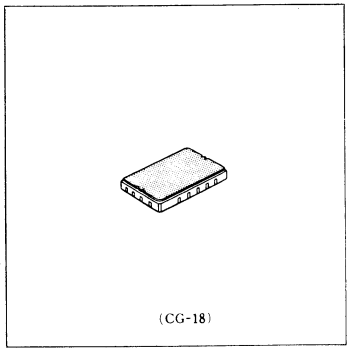


HM4864ACG-12, HM4864ACG-15, HM4864ACG-20

65536-word × 1-bit Dynamic Random Access Memory

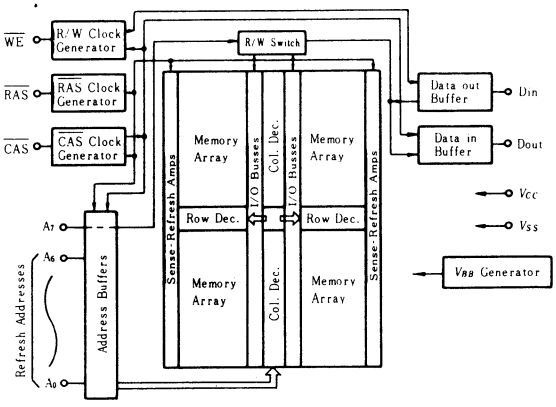
■ FEATURES

- 18-pin Leadless Chip Carrier
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120/150/200ns (max)
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by $\overline{CAS}$
- TTL compatible
- 128 refresh cycles/2ms
- Hidden refresh capability

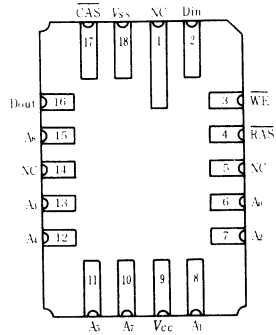


(CG-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Bottom View)

A0–A7	:	Address Inputs
$\overline{CAS}$	:	Column Address Strobe
Din	:	Data In
Dout	:	Data Output
$\overline{RAS}$	:	Row Address Strobe
$\overline{WE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
A0–A6	:	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	−1V to +7V
Operating temperature, Ta (Ambient)	0°C to +70°C
Storage temperature	−65°C to +150°C
Power Dissipation	1W
Short circuit output current	50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Notes : 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$,$\overline{CAS}$ Cycling:t_{RC}=min)	I_{CC1}	—	55	—	50	—	44	mA	1,2
Standby Cnrrent($\overline{RAS}$=V_{IH},Dout=High Impedance)	I_{CC2}	—	3.5	—	3.5	—	3.5	mA	
Refresh Current($\overline{RAS}$ Cycling,$\overline{CAS}$=V_{IH},t_{RC}=min)	I_{CC3}	—	42	—	38	—	33	mA	2
Standby Current($\overline{RAS}$=V_{IH},Dout Enable)	I_{CC5}	—	5.5	—	5.5	—	5.5	mA	1
Page Mode Current($\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling;t_{PC}=min)	I_{CC6}	—	38	—	35	—	31	mA	1,2
Input Leakage(0<V_{out}<6.5V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage(Dout is disabled,0<V_{out}<5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output Levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{O} max. is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Item		Symbol	typ	max	Unit	Notes
Input Capacitance	A_0~A_7, Din	C_{in1}	—	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{in2}	—	10	pF	1
Output Capacitance	Dout	C_{out}	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

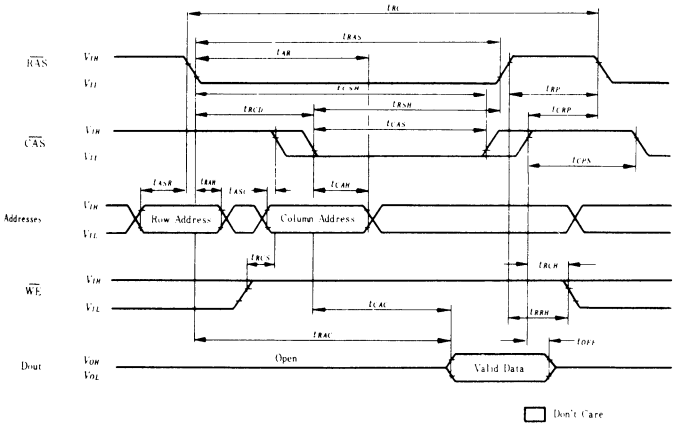
Parameter	Symbol	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
		min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	35	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	—	−10	—	−10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	2	—	2	—	2	ms	
Read-Write Cycle Time	t_{RWC}	245	—	280	—	345	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	—	45	—	55	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	120	—	155	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30	—	35	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

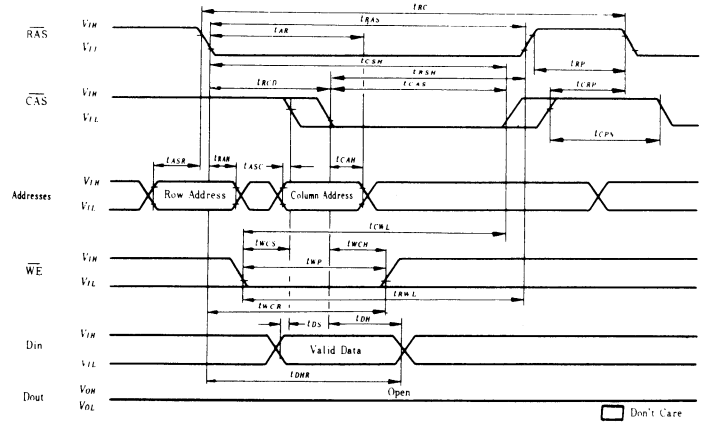
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet is electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. There parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge is delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

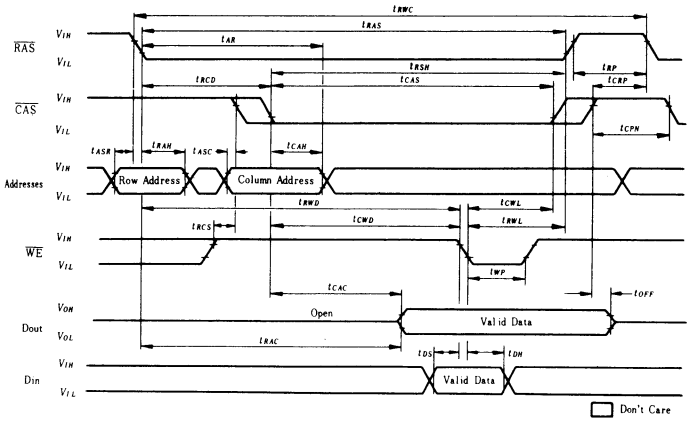
● READ CYCLE



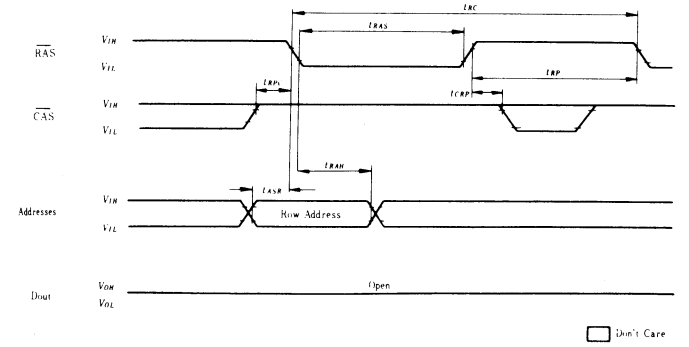
● WRITE CYCLE (EARLY WRITE)



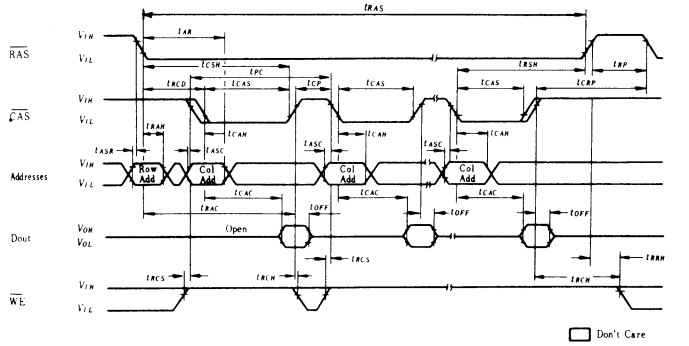
●READ-WRITE/READ-MODIFY-WRITE CYCLE



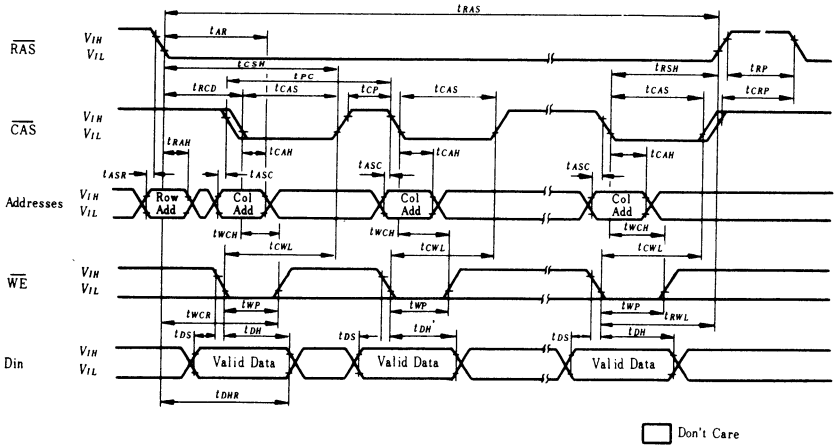
●"RAS-ONLY" REFRESH CYCLE



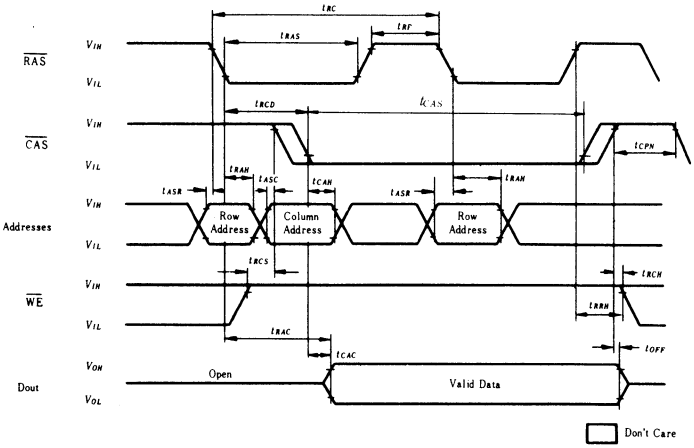
●PAGE MODE READ CYCLE



●PAGE MODE WRITE CYCLE



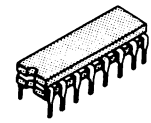
●HIDDEN REFRESH CYCLE



HM50256-12,HM50256-15, HM50256-20,HM50256P-12, HM50256P-15,HM50256P-20

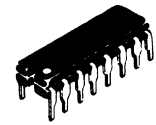
262144-word × 1-bit Dynamic Random Access Memory

HM50256 Series



(DG-16B)

HM50256P Series

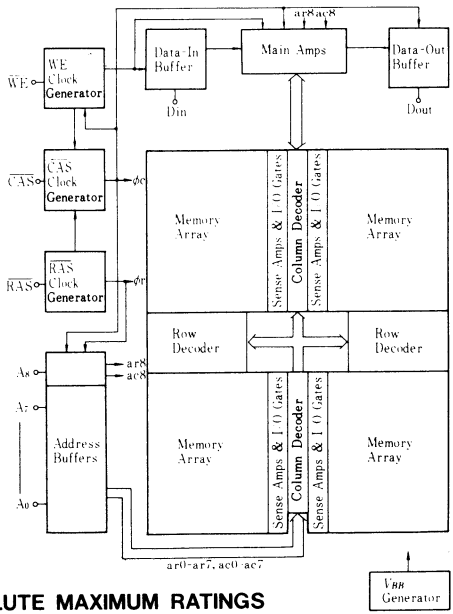


(DP-16A)

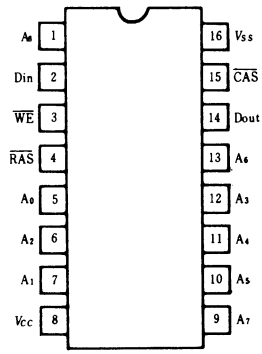
■FEATURES

- Industry Standard 16-Pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . (Cerdip) −65°C to +150°C
(Plastic DIP) −55°C to +125°C
Power dissipation 1W
Short circuit output current 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Input leakage(0< V_{out}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage(0< V_{out}<7V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks, Data-out	C_{I2}	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time(Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

(to be continued)

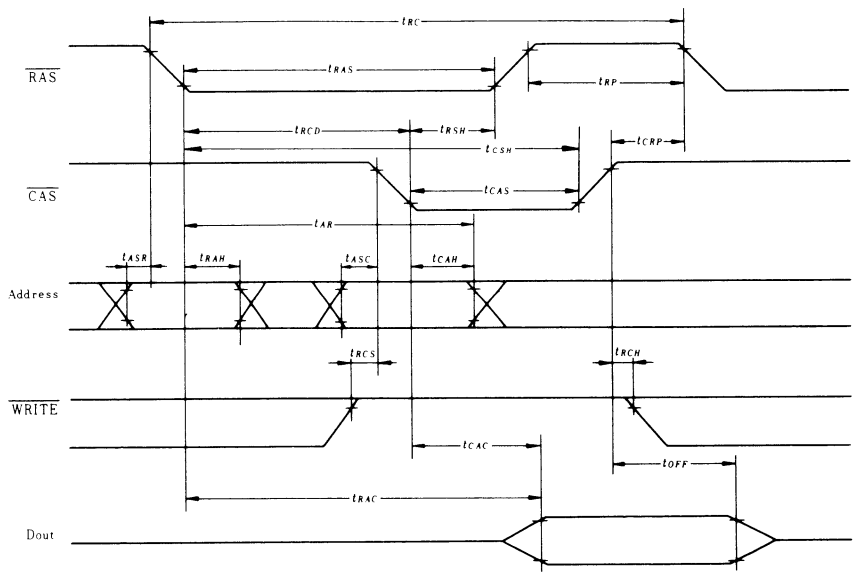
Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	75	—	100	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

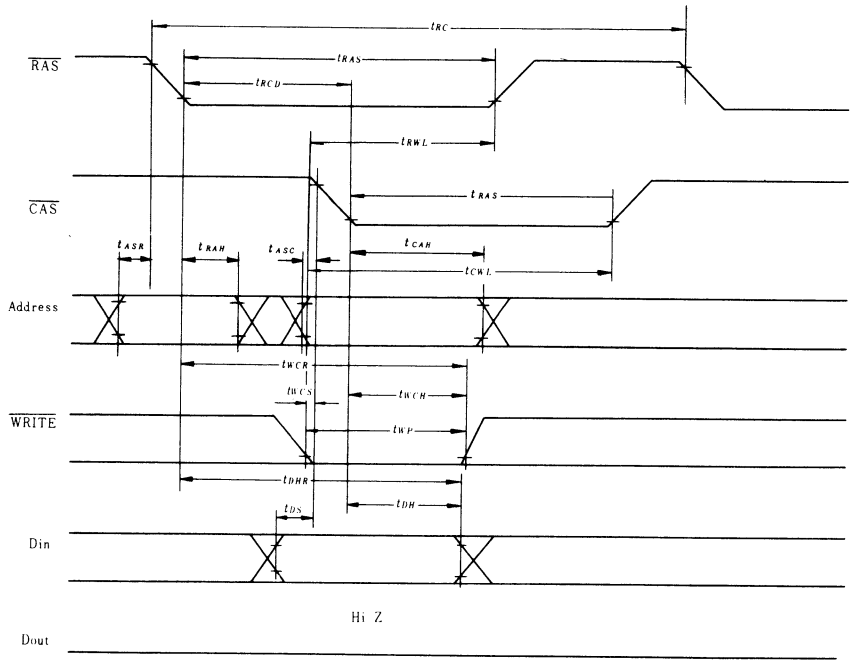
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refesh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

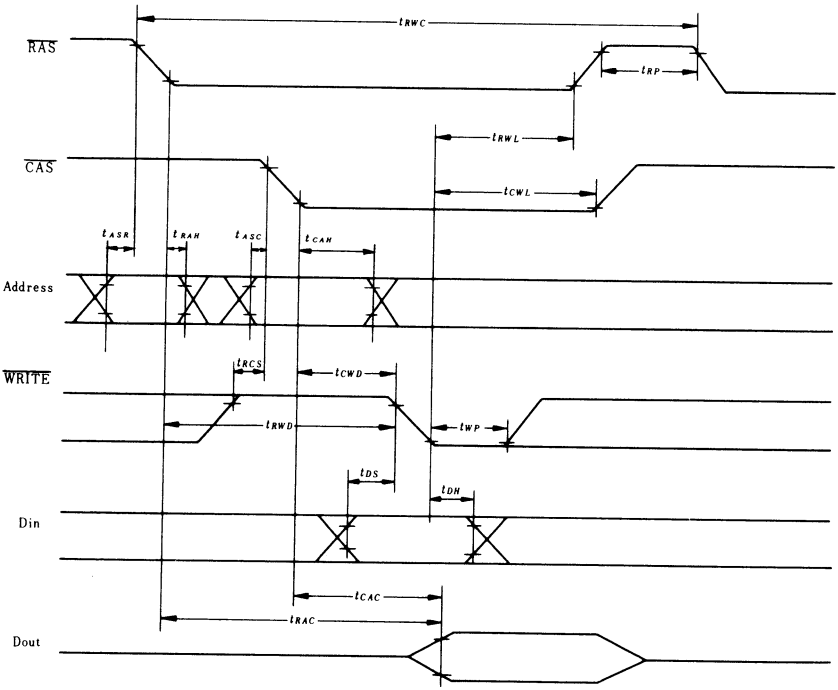
● READ CYCLE



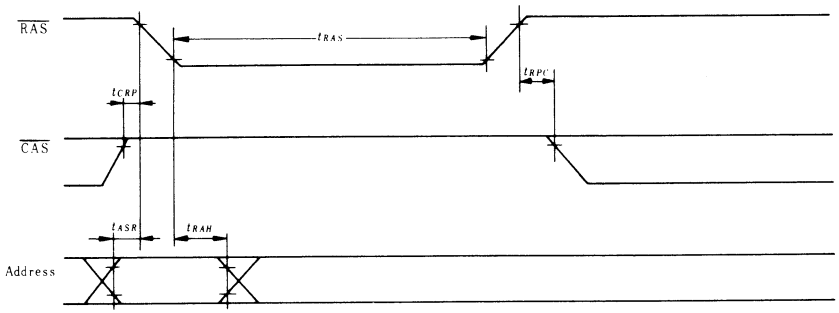
● WRITE CYCLE



● READ MODIFY WRITE CYCLE

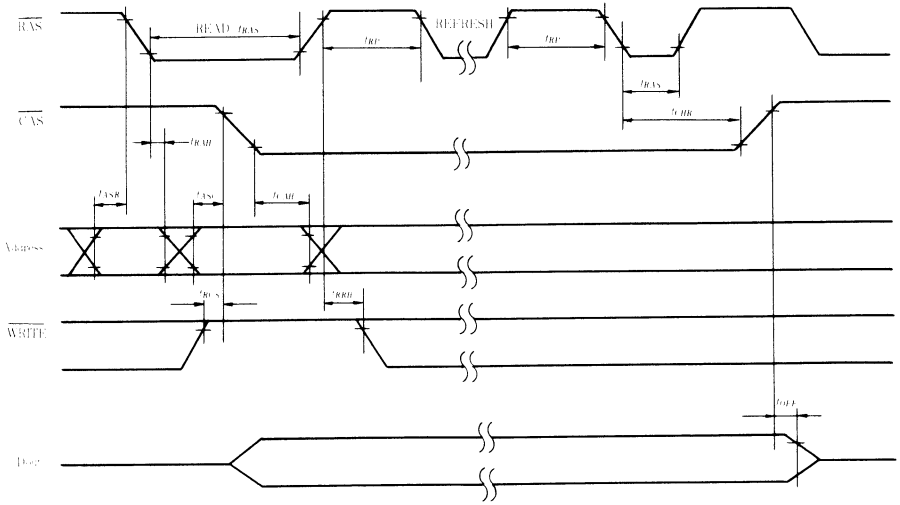


● $\overline{RAS}$ ONLY REFRESH CYCLE

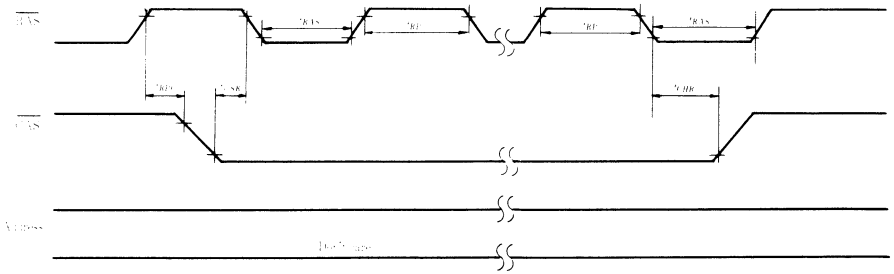


* REFRESH ADDRESS $A_0 - A_7$ ($AX_0 - AX_7$)

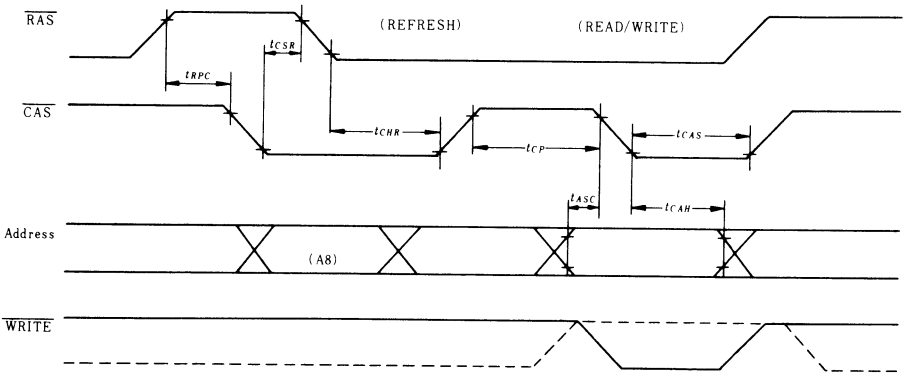
● HIDDEN REFRESH CYCLE



● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



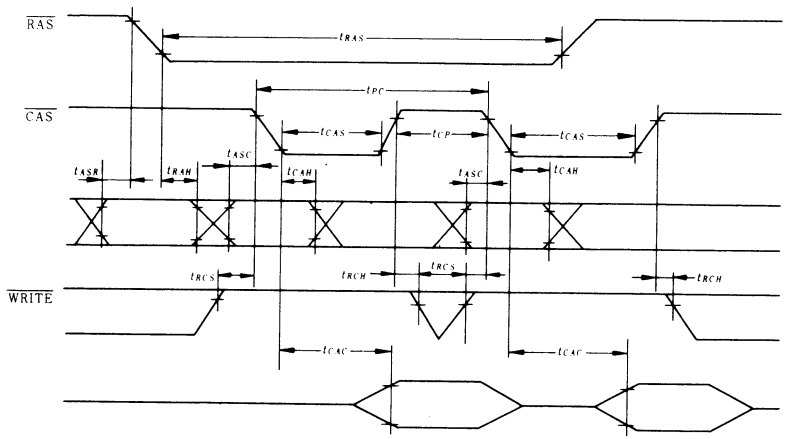
● COUNTER TEST



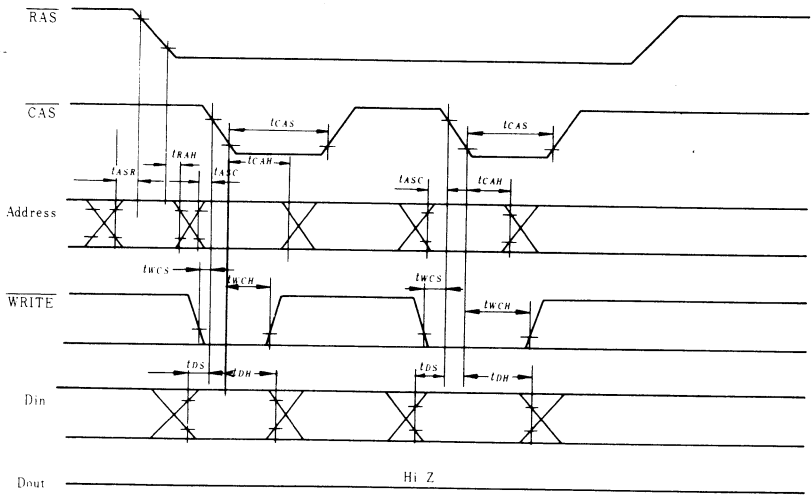
■ PAGE MODE CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit
		min	max	min	max	min	max	
Page Mode Supply Current	I_{CC7}	—	57	—	48	—	37	mA
Page Mode Read or Write Cycle	t_{PC}	120	—	145	—	190	—	ns
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns
Page Mode Read Modify Write Cycle	t_{PCM}	165	—	195	—	250	—	ns

● PAGE MODE READ CYCLE



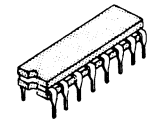
● PAGE MODE WRITE CYCLE



HM50257-12,HM50257-15, HM50257-20,HM50257P-12, HM50257P-15,HM50257P-20

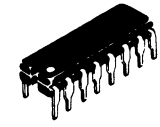
262144-word × 1-bit Dynamic Random Access Memory

HM50257 Series



(DG-16B)

HM50257P Series

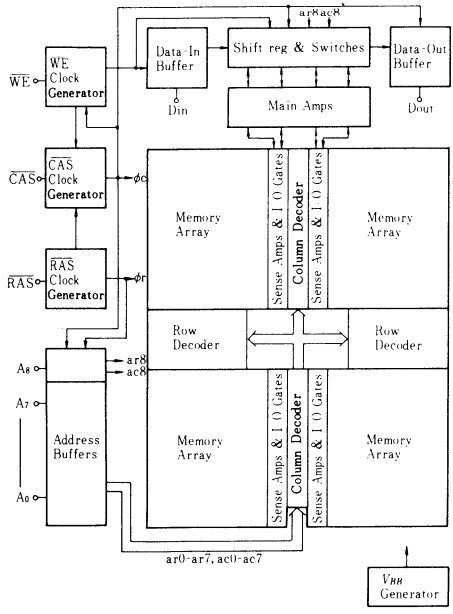


(DP-16A)

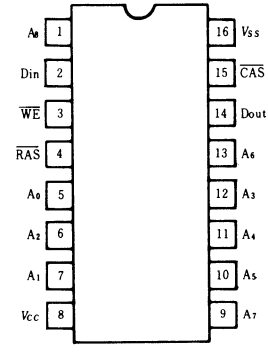
■ FEATURES

- Industry standard 16-pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles . . . . . (4ms)
- 3 Variations of refresh; $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . (Cerdip) -65°C to +150°C
(Plastic DIP) -55°C to +125°C
Power dissipation 1W
Short circuit output current 50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS}.

HITACHI

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Stand by Current ($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current ($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Input leakage (0< V_{out} <7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage (0< V_{out} <7V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected I_{CC} max. is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-In	C_{I1}	—	5	pF	1
	Clocks, Data-Out	C_{I2}	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

(to be continued)

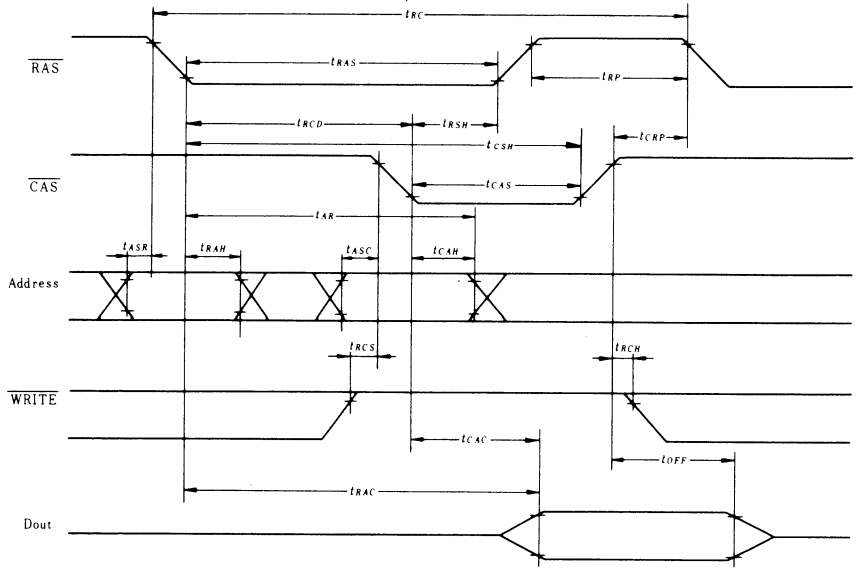
Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	75	—	100	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

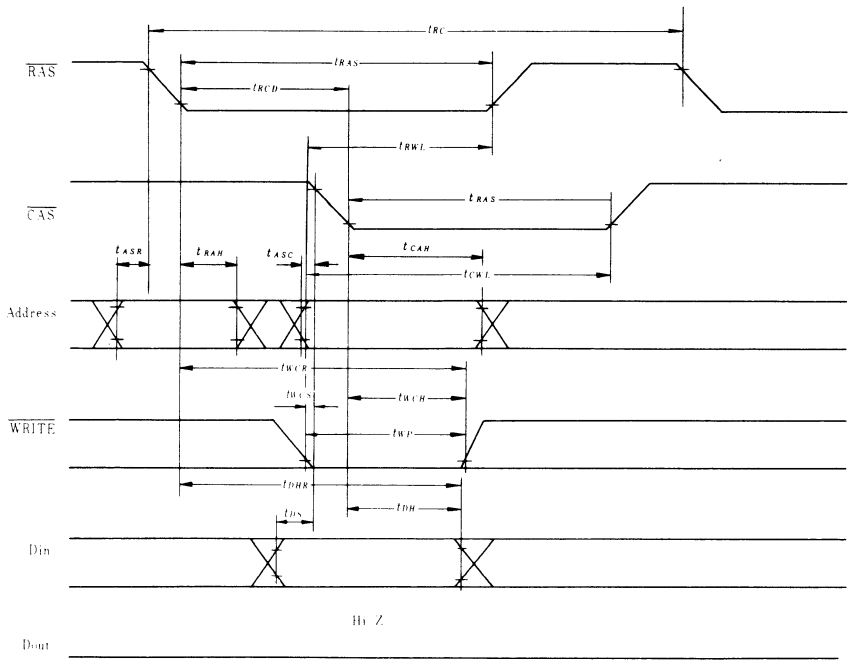
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then excute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

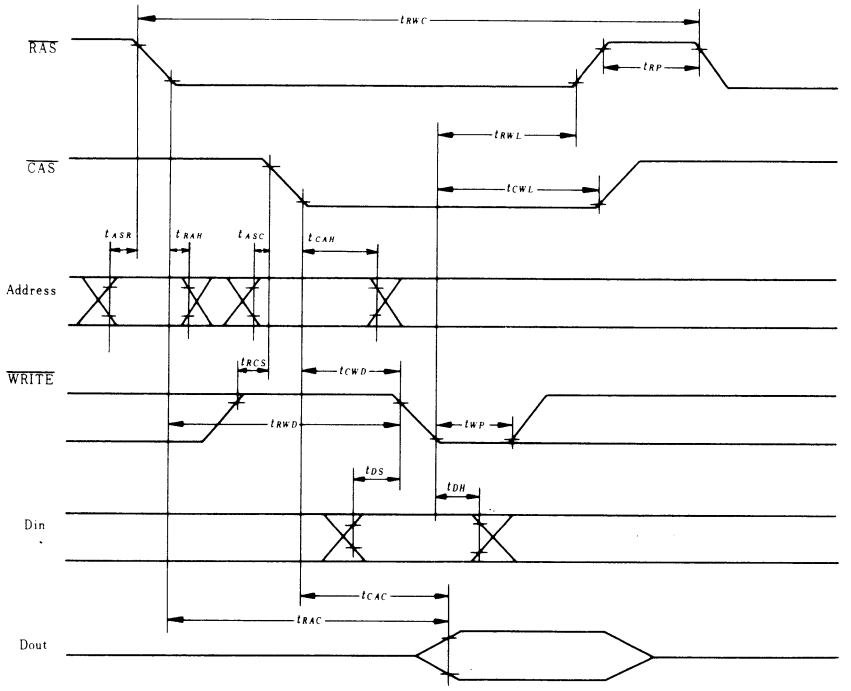
● READ CYCLE



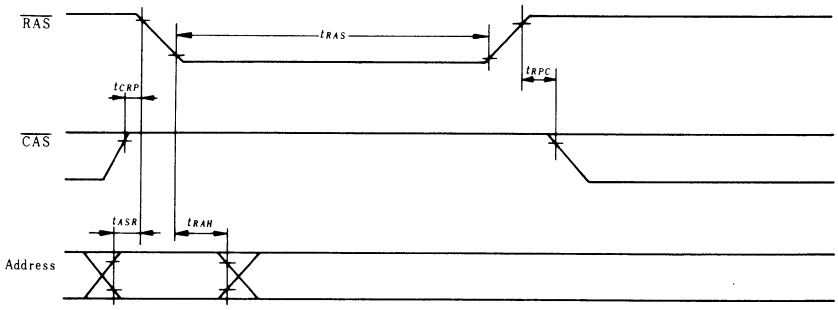
● WRITE CYCLE



● READ MODIFY WRITE CYCLE

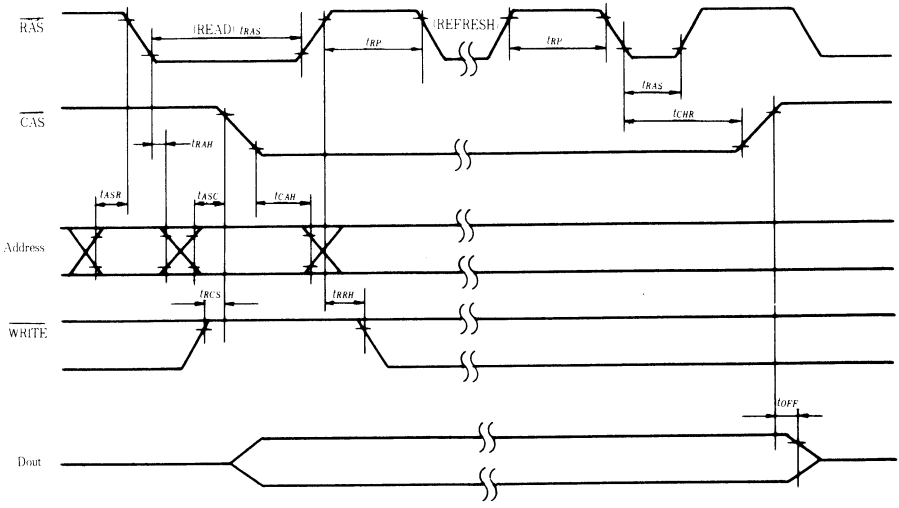


● $\overline{RAS}$ ONLY REFRESH CYCLE

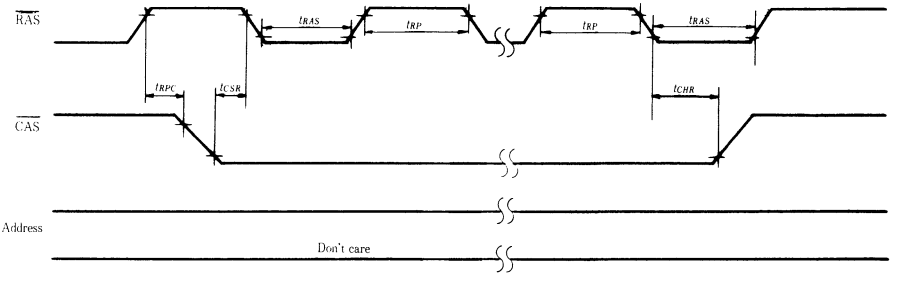


* REFRESH ADDRESS $A_0 - A_7$ ($AX_0 - AX_7$)

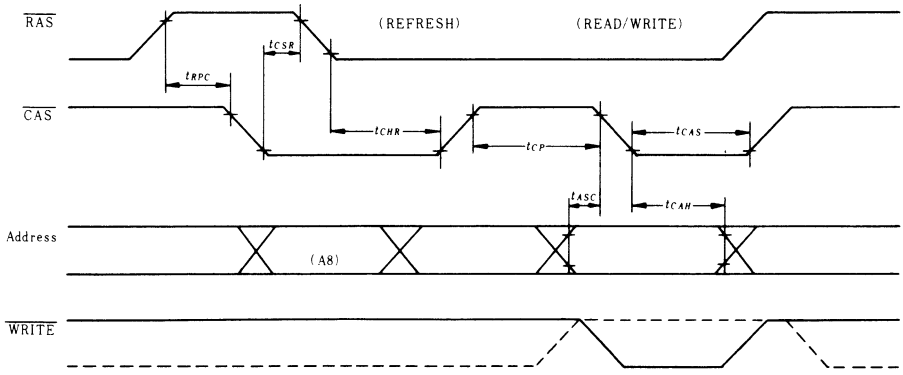
● HIDDEN REFRESH CYCLE



● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



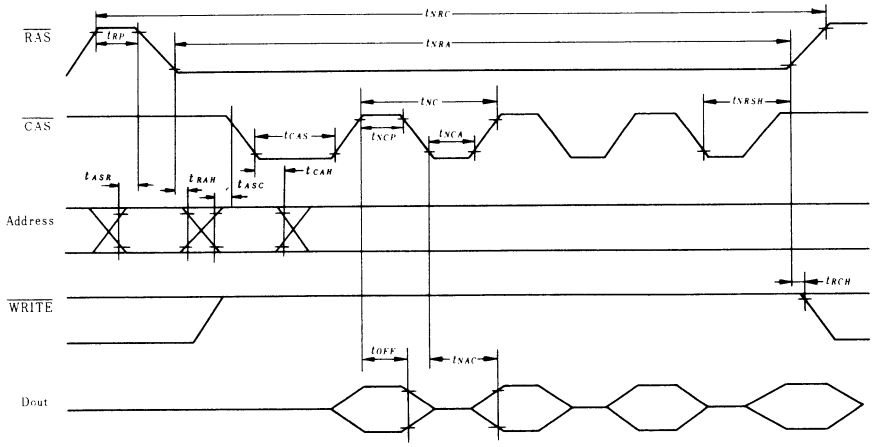
● COUNTER TEST



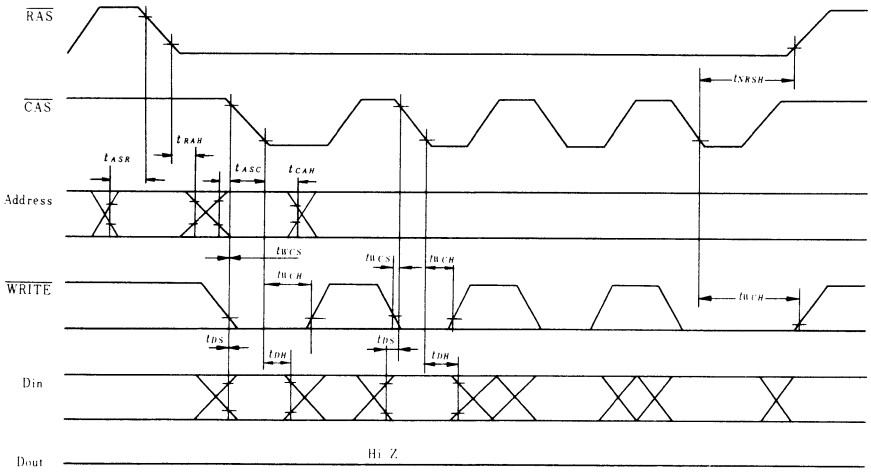
■ NIBBLE MODE CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit
		min	max	min	max	min	max	
Nibble Mode Supply Current	I_{CC8}	—	57	—	48	—	37	mA
Nibble Mode Access Time	t_{NAC}	—	25	—	25	—	35	ns
Nibble Mode $\overline{RAS}$ Cycle Time	t_{NRC}	390	—	460	—	590	—	ns
Nibble Mode $\overline{RAS}$ Pulse Width	t_{NRA}	290	—	350	—	460	—	ns
Nibble Mode Cycle Time	t_{NC}	55	—	60	—	80	—	ns
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	20	—	25	—	35	—	ns
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	—	25	—	35	—	ns
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	40	—	45	—	55	—	ns
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	20	—	25	—	35	—	ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	20	—	25	—	35	—	ns
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{NRWL}	40	—	45	—	35	—	ns
Nibble Mode Write Command Pulse Widt	t_{NWP}	20	—	25	—	35	—	ns

● NIBBLE MODE READ CYCLE



● NIBBLE MODE WRITE CYCLE



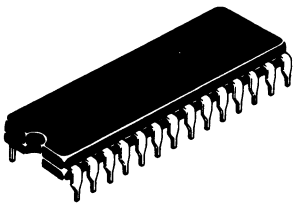
MOS MASK ROM

HN61364P, HN61364FP

8192-word x 8-bit Mask Programmable Read Only Memory

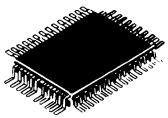
The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the CS, $\overline{OE}_0 \sim \overline{OE}_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

HN61364P



(DP-28)

HN61364FP

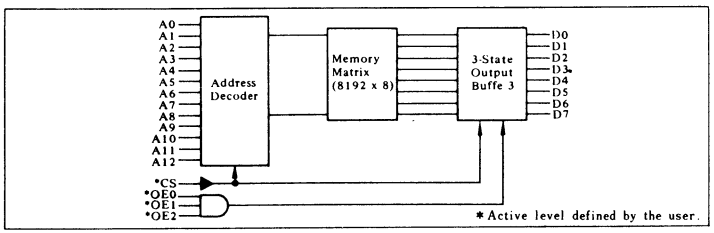


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Bias Storage Temperature	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

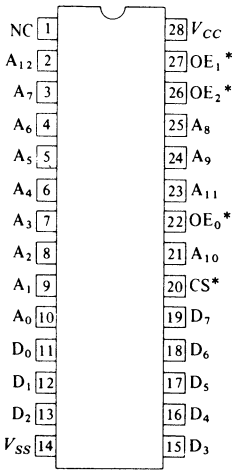
■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage *	V_{CC}	4.5	5.0	5.5	V
Input Voltage *	V_{IL}	−0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	−20	–	75	°C

* with respect to V_{SS}

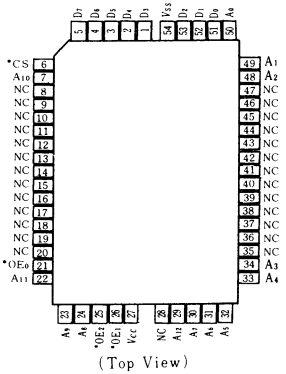
■ PIN ARRANGEMENT

● HN61364P



(Top View)

● HN61364FP



(Top View)

HITACHI

■ ELECTRICAL CHARAGTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −20 to +75°C

Item		Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage		V_{IH}		2.2	–	V_{CC}	V
Input Low-level Voltage		V_{IL}		−0.3	–	0.8	V
Output High-level Voltage		V_{OH}	I_{OH}=−205μA	2.4	–	–	V
Output Low-level Voltage		V_{OL}	I_{OL}=3.2mA	–	–	0.4	V
Input Leakage Current		I_{in}	V_{in}=0 to 5.5V	–	–	2.5	μA
Output High-level Leakage Current		I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Output Low-level Leakage Current		I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Supply Current	Active	I_{CC} *	$\overline{Vcc}$=5.5V, Iout=0mA, trc=min, duty=100%	–	10	25	mA
	Standby	I_{SB}	V_{CC}=5.5V, $\overline{CS}$≧V_{CC}−0.2V, CS≦0.2V	–	1	30	μA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, T_a=25°C	–	–	10	pF
Output Capacitance		C_{out}		–	–	15	pF

* Steady state current ** V_{CC} = 5V, T_a = 25°C

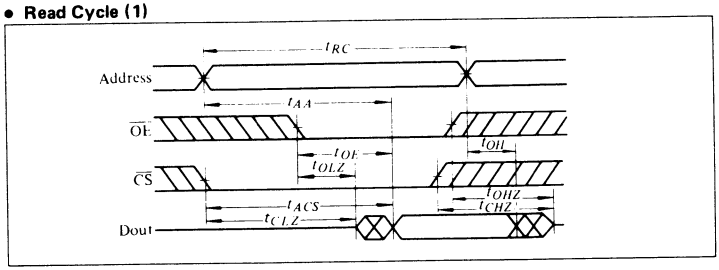
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75°C, t_r=t_f=20ns)

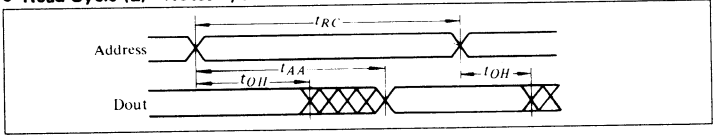
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	–	ns
Address Access Time	t_{AA}	–	250	ns
Chip Select Access Time	t_{ACS}	–	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

■ TIMING WAVEFORM

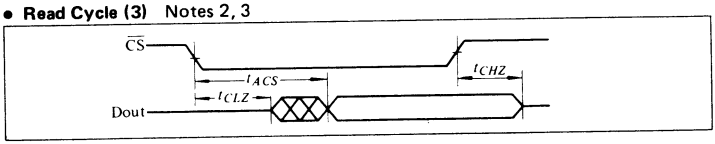
• Read Cycle (1)



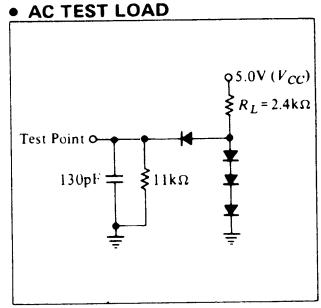
• Read Cycle (2) Notes 1, 3



• Read Cycle (3) Notes 2, 3



• AC TEST LOAD



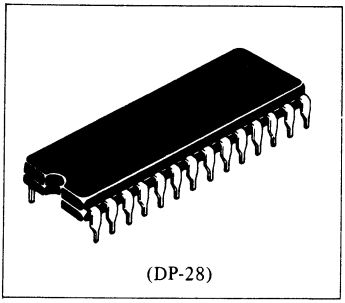
Notes) 1. t_r=t_f=20ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

NOTES:
1. Device is continuously selected.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN61364HP — Preliminary

8192-word x 8-bit Mask Programmable Read Only Memory

The HN61364HP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the CS, $OE_0 \sim OE_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

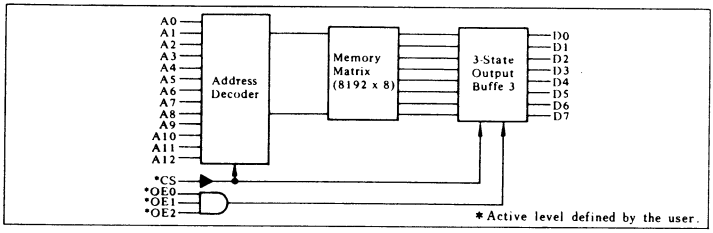


(DP-28)

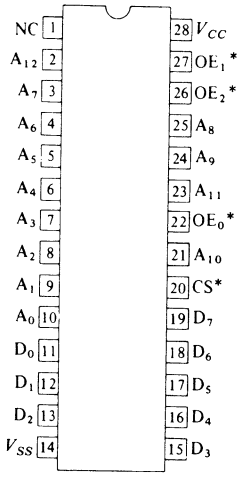
■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 200ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

NOTE:
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

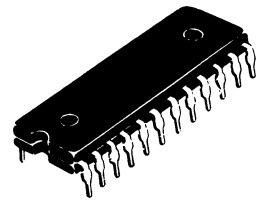
HN61365P

8192-word×8-bit Mask Programmable Read Only Memory

The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselects the output and puts the chip in a power-down mode.

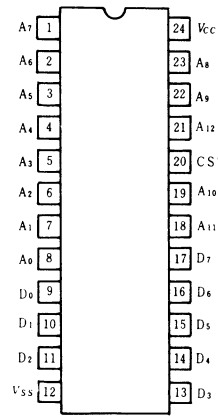


(DP-24)

■FEATURES

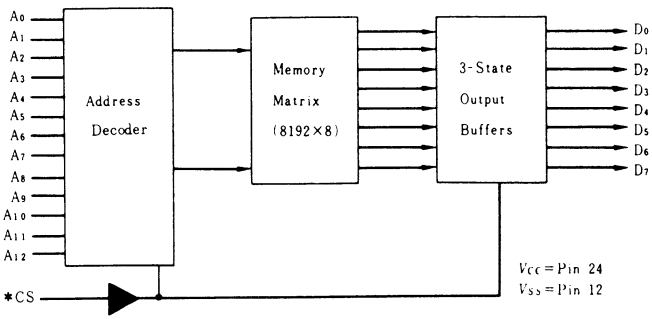
- Fully Static Operation
- Automatic Power Down
- Single +5 Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



* Active level defined by the user.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (under bias)	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	℃

* With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, V_{SS}=0V, Ta=−20 to +75℃)

Item	Symbol	Test Conditions		min	typ**	max	Unit
Input Voltage	V_{IH}			2.2	—	V_{CC}	V
	V_{IL}			−0.3	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−205μA		2.4	—	—	V
	V_{OL}	I_{OL}=3.2mA		—	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0~5.5V		—	—	2.5	μA
Output Leakage Current	I_{LOH}	CS=0.8V, $\overline{CS}$=2.2V	V_{out}=2.4V	—	—	10	μA
	I_{LOL}		V_{out}=0.4V	—	—	10	μA
Active Supply Current	I_{CC}*	V_{CC}=5.5V, I_{OUT}=0mA, t_{RC}=min, duty=100%		—	10	25	mA
Stand by Supply Current	I_{SB}	$\overline{CS}\geq V_{CC}-0.2V$, CS≦0.2V, V_{CC}=5.5V		—	1	30	μA
Input Capacitance	C_{in}	V_{in}=0V, f=1MHz, Ta=25℃		—	—	10	pF
Output Capacitance	C_{out}			—	—	15	pF

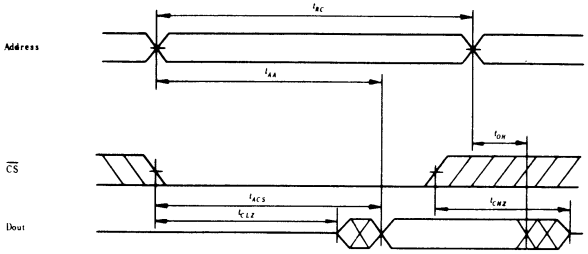
* Steady state current ** V_{CC}=5V, T_a=25℃

■RECOMMENDED AC OPERATING CHARACTERISTICS

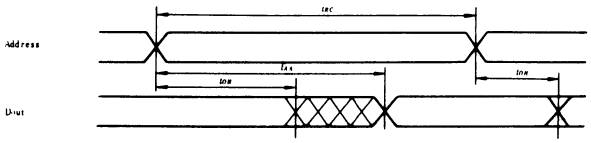
●READ SEQUENCE (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75℃, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

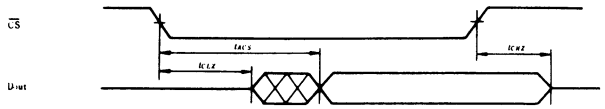
●READ CYCLE (1)



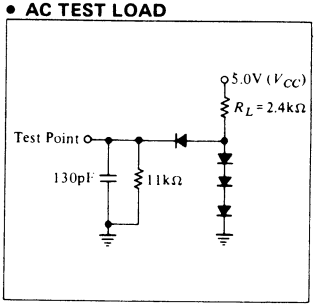
●READ CYCLE (2) (Notes 1)



●READ CYCLE (3) (Notes 2)



● AC TEST LOAD



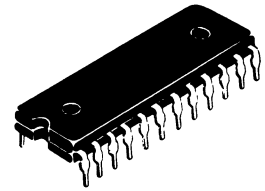
Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

Notes)
1. Device is continuously selected
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. Input pulse level : 0.8 to 2.4V
4. Input and output timing reference level : 1.5V

HN61366P

8192-word×8-bit Mask Programmable Read Only Memory

The HN61366P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the OE input and the memory content are defined by the user.

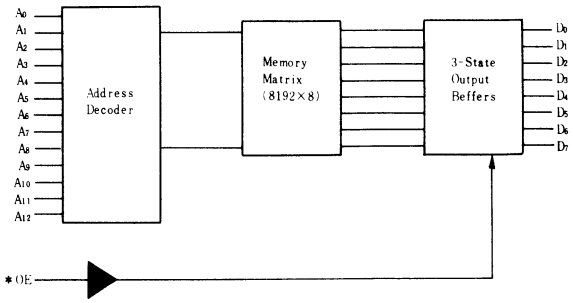


(DP-24)

■FEATURES

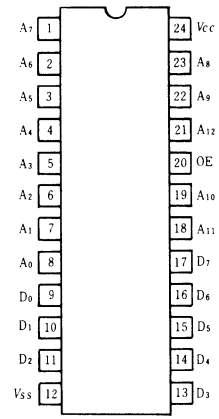
- Fully Static Operation
- Single +5V power supply
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Operation; 50mW (typ.)
- Pin Compatible with EPROM

■BLOCK DIAGRAM



* Active level defined by the user.

■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (under bias)	T_{bias}	−20 to +85	°C

* With respect to V_{SS}

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temprature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75°C)

Item	Symbol	Test Conditions		min	typ**	max	Unit
Input Voltage	V_{IH}			2.2	—	V_{CC}	V
	V_{IL}			−0.3	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−205μA		2.4	—	—	V
	V_{OL}	I_{OL}=3.2mA		—	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0~5.5V		—	—	2.5	μA
Output Leakage Current	I_{LOH}	OE=0.8V, $\overline{OE}$=2.2V	V_{OUT}=2.4V	—	—	10	μA
	I_{LOL}		V_{OUT}=0.4V	—	—	10	μA
Operating Supply Current	I_{CC}*	V_{CC}=5.5V, I_{OUT}=0mA, t_{RC}=min		—	10	25	mA
Input Capacitance	C_{in}	V_{in}=0V, f=1MHz, Ta=25°C		—	—	10	pF
Output Capacitance	C_{out}			—	—	15	pF

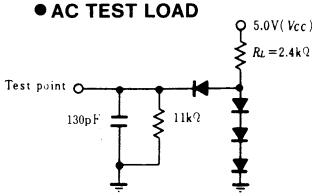
* Steady state current ** V_{CC}=5V, T_a=25°C

■RECOMMENDED AC OPERATING CONDITIONS

●READ CYCLE (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

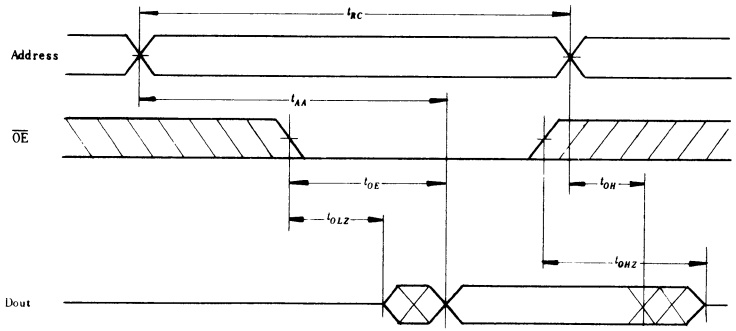
●AC TEST LOAD



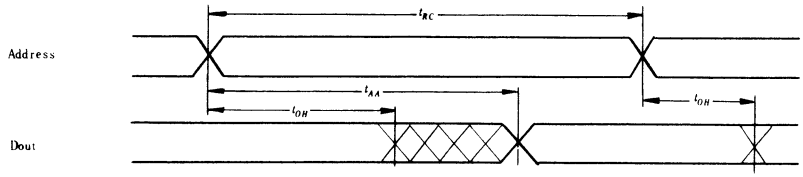
Notes: 1. t_r=t_f=20ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■TIMING WAVEFORM

●READ CYCLE (1)



●READ CYCLE (2) Note 1)



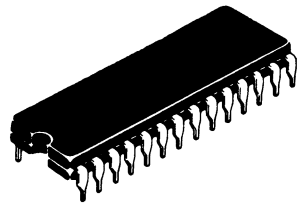
Note) 1. $\overline{OE}$=V_{IL}
2. Imput pulse level : 0.8 to 2.4V
3. Imput and output timing reference level : 1.5V

HN613128P, HN613128FP

16384-word × 8-bit Mask Programmable Read Only Memory

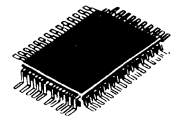
The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE_0, OE_1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613128P



(DP-28)

HN613128FP

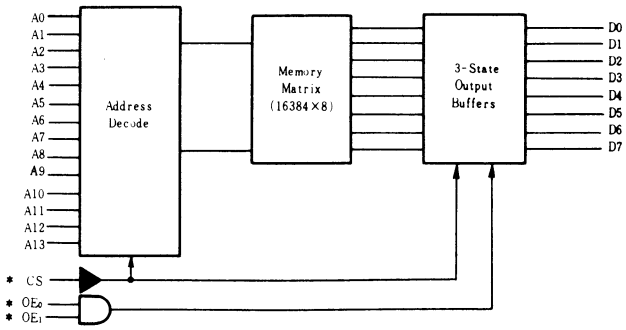


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;
  Standby: 5μW (typ.)
  Operation: 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (under bias)	T_{bias}	−20 to +85	°C

* With respect to V_{SS}.

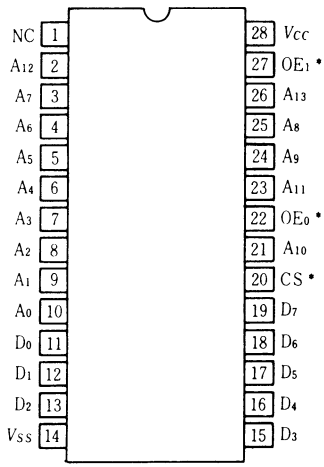
■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

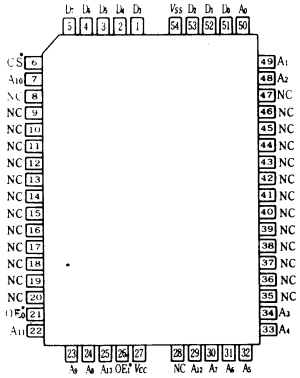
■ PIN ARRANGEMENT

● HN613128P



(Top View)

● HN613128FP



(Top View)

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C)

Item	Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage	V_{IH}		2.2	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−205μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=3.2mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}*/ I_{SB}	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min, duty=100% $\overline{CS}$≧V_{CC}−0.2V, CS≦0.2V	—	10/1	25/30	mA/μA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	10	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	15	pF

* Steady state current ** V_{CC}=5V, Ta=25°C

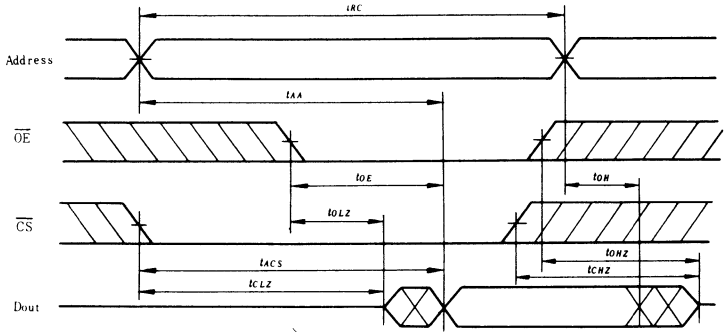
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C, All timing with t_r=t_f=20ns)

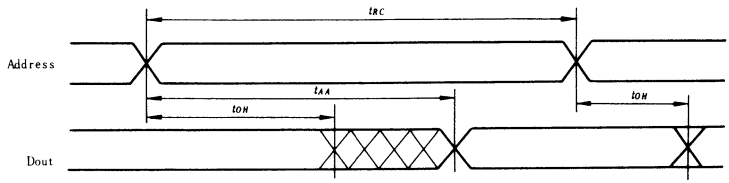
Item	Symbol	HN613128P		Unit
		min	max	
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

■ TIMING WAVEFORM

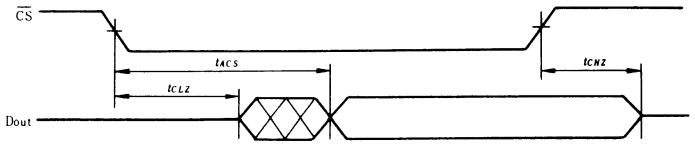
● READ CYCLE (1)



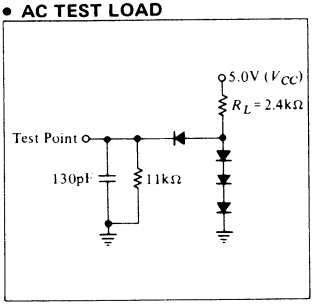
● READ CYCLE (2) (Notes 1, 3)



● READ CYCLE (3) (Notes 2, 3)



● AC TEST LOAD



Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

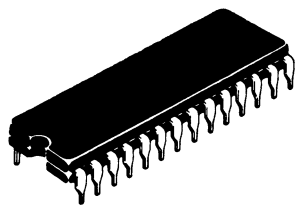
NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincide with $\overline{CS}$ transition low.
3. $\overline{OE}$ = *VIL*.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference lev 1.5V

HN613128HP — Preliminary

16384-word x 8-bit Mask Programmable Read Only Memory

The HN613128HP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE_0, OE_1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613128HP

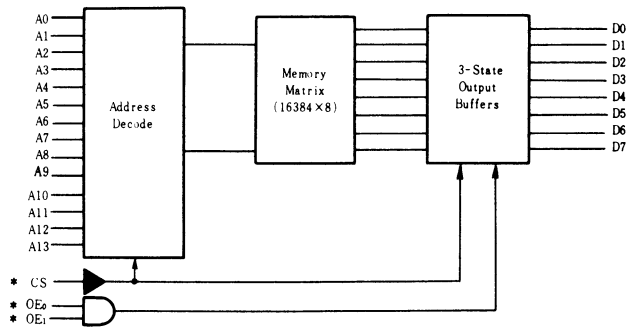


(DP-28)

■ FEATURES

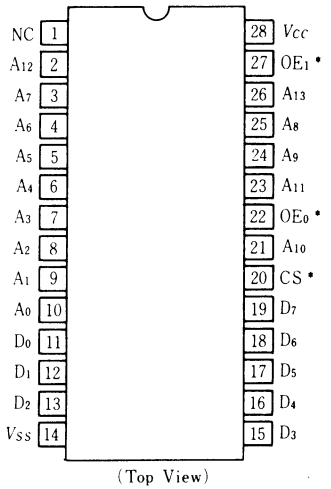
- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time: 200ns
- Lower Standby and Low Power Operation;
  - Standby: 5μW (typ.)
  - Operation: 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT



(Top View)

NOTES:

The specifications of this device are subject to change without notice.

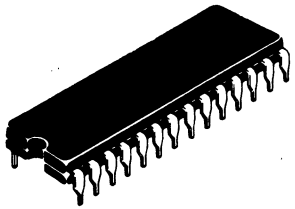
Please contact your nearest Hitachis Sales Dept, regarding specifications.

HN61256P, HN61256FP

32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

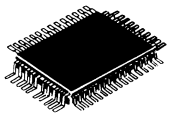
The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

HN61256P



(DP-28)

HN61256FP

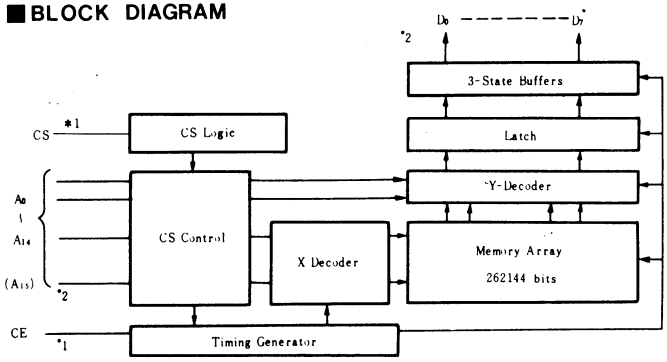


(FP-54)

■FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), Standby 5μW (typ.)
- TTL compatible
- Access time: 3.5μs (max)

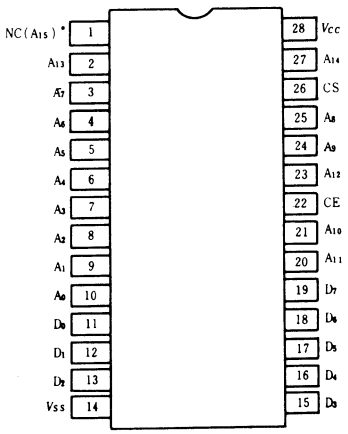
■BLOCK DIAGRAM



*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D_0 to D_3.

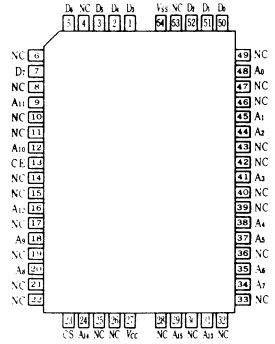
■PIN ARRANGEMENT

●HN61256P



(Top View)

●HN61256FP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3～+7.0	V
Input Voltage*	V_{in}	−0.3～+7.0	V
Operating Temperature Range	T_{opr}	0～+75	°C
Storage Temperature Range	T_{stg}	−55～+125	°C
Bias Storage Temperature Range	T_{bias}	−20～+85	°C

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75°C)

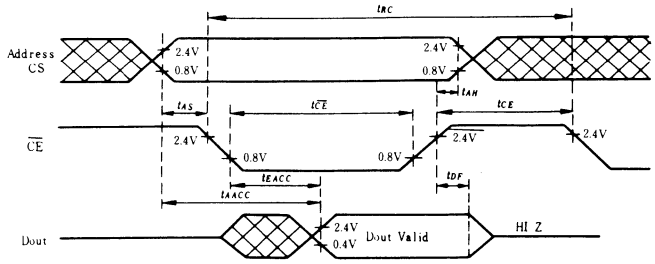
Item		Symbol	Test Condition		min	typ**	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	I_{OH}=−100μA		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	I_{OL}=1.6mA		—	—	0.4	V
Input Leakage Current		I_{in}	V_{in}=0～5.5V		—	—	2.5	μA
Output "High" Level Leakage Current		I_{LOH}	CE=0.8V	V_{out}=2.4V	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$=2.4V	V_{out}=0.4V	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$\overline{CS}\geq V_{CC}-0.2V$, $CS\leq V_{SS}+0.2V$	V_{CC}=5.5V	—	1	30	μA
	In operation	I_{CC}*	t_{RC}=4.0μs, I_{out}=0mA, $t_{\overline{CE}}$=3.0μs		—	1.5	3.0	mA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, Ta=25°C		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

* Steady state current ** V_{CC}=5V, Ta=25°C

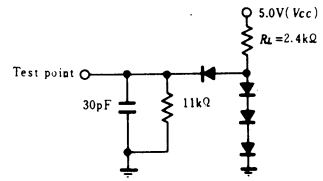
■ AC OPERATING CONDITION AND CHARACTERISTICS

● READ SEQUENCE (V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs



● AC TEST LOAD



Notes : 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

HN613256P, HN613256FP

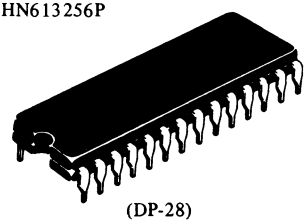
32768-word x 8-bit Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.

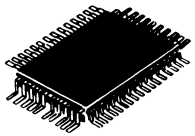
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613256P



(DP-28)

HN613256FP

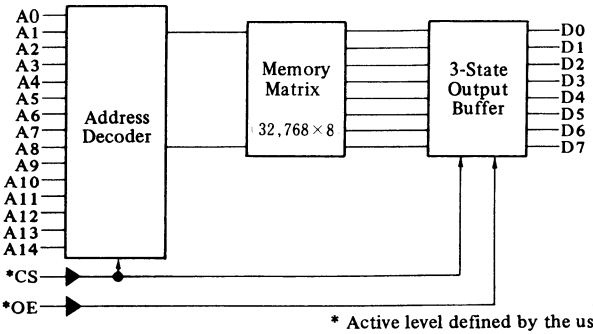


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

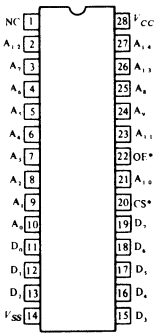
■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT

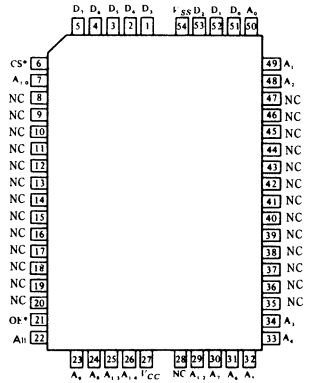
- **HN613256P**



(Top View)

* Active level can be defined by the customer.

- **HN613256FP**



(Top View)

* Active level can be defined by the customer.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

HITACHI

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, T_a = −20 ~ +75 °C)

Item		Symbol	Test Condition		min	typ **	max	Unit
Input Voltage		V_{IH}			2.2	–	V_{CC}	V
		V_{IL}			−0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = −205 µA		2.4	–	–	V
		V_{OL}	I_{OL} = 3.2 mA		–	–	0.4	V
Input Leakage Current		I_{in}	V_{in} = 0 ~ 5.5V		–	–	2.5	µA
Output Leakage Current		I_{LOH}	CS = 0.8V, $\overline{CS}$ = 2.2V	V_{out} = 2.4V	–	–	10	µA
		I_{LOL}		V_{out} = 0.4V	–	–	10	µA
Supply Current	Active	I_{CC}*	V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = min, duty = 100%.		–	10	30	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CS} \geqq V_{CC}$ − 0.2V, CS ≦ 0.2V		–	1	30	µA
Input Capacitance		C_{in}	V_{in} = 0V, f = 1 MHz, T_a = 25 °C		–	–	10	pF
Output Capacitance		C_{out}			–	–	15	pF

* Steady state current
** V_{CC}=5V, T_a=25°C

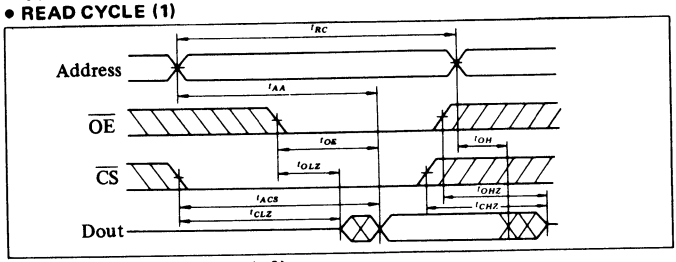
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

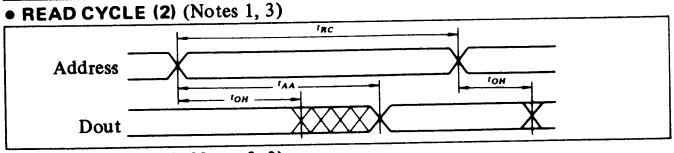
Item	Symbol	min	max	Unit
Read Cycle Time	tRC	200	–	ns
Address Access Time	tAA	–	200	ns
Chip Select Access Time	$tACS$	–	200	ns
Chip Selection to Output in Low Z	$tCLZ$	10	–	ns
Output Enable to Output Valid	tOE	–	100	ns
Output Enable to Output in Low Z	$tOLZ$	10	–	ns
Chip Deselection to Output in High Z	$tCHZ$	0	100	ns
Chip Disable to Output in High Z	$tOHZ$	0	100	ns
Output Hold from Address Change	tOH	10	–	ns

■ TIMING WAVEFORM

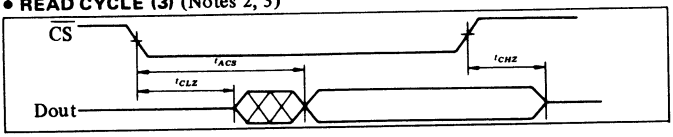
• READ CYCLE (1)



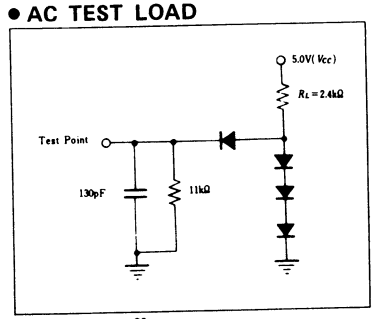
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



• AC TEST LOAD



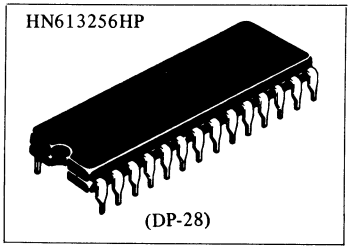
Notes : 1. $t_r = t_f$ = 20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN613256HP — Preliminary

32768-word x 8-bit Mask Programmable Read Only Memory

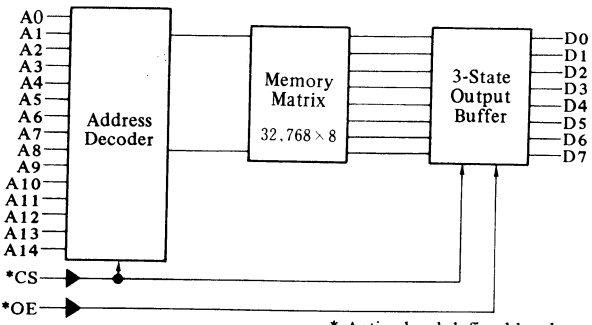
The HN613256HP is a mask-programmable, byte-organized memory designed for use in bus-organized system.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.



■ FEATURES

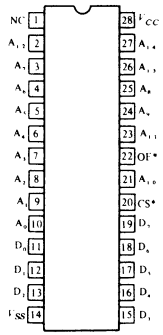
- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 200ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT



(Top View)

* Active level can be defined by the customer.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

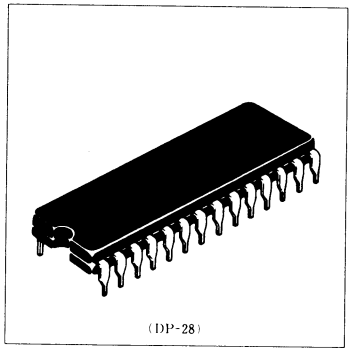
* With respect to V_{SS}.

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi Sales Dept. regarding specifications.

HITACHI

131,072-word×8-bit Mask Programmable Read Only Memory

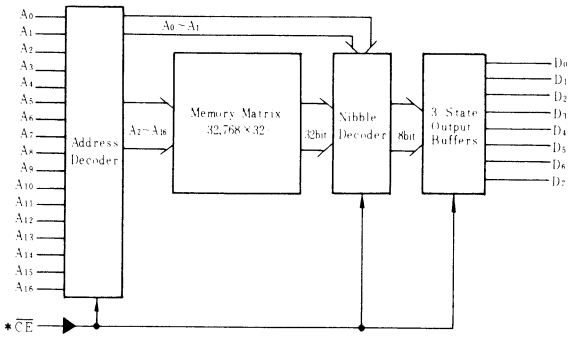
The HN62301P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The Chip Enable and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.



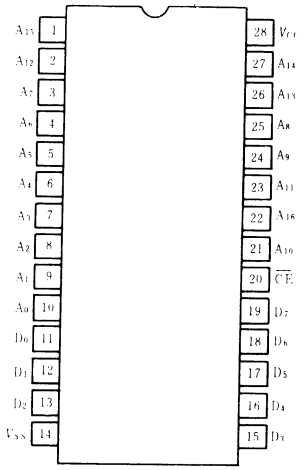
■FEATURES

- Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time-350ns
- Lower Power Standby and Low Power Operation; Standby: 2mW (typ.), Operation: 75mW (typ.)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Bias Storage Temperature Range	T_{bias}	−20 to +85	°C

* With respect to V_{SS}

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales Dept, regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.4+0.4(V_{CC}−5)	—	V_{CC}	V

* with respect to V_{ss}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions		min	typ***	max	Unit
Normal Operating Current	I_{CC1}*	t_{RC1}=min, V_{CC}=5.5V, I_{out}=0mA, duty=100%		—	15	50	mA
Nibble Operating Current	I_{CC2}*	t_{RC2}=min, V_{CC}=5.5V, I_{out}=0mA, duty=100%		—	5	15**	mA
Stand by Current	I_{SB}	$\overline{CE}$≧V_{CC}−0.2V, V_{CC}=5.5V		—	0.4	10	mA
Input Leakage Current	I_{LI}	V_{in}=0 to 5.5V, other 0V		−10	—	10	μA
Output Leakage Current	I_{LOH}	$\overline{CE}$=2.4V	V_{out}=2.4V	—	—	10	μA
	I_{LOL}		V_{out}=0.4V	—	—	10	μA
Output Voltage	V_{OH}	I_{out}=−205μA		2.4	—	—	V
	V_{OL}	I_{out}=3.2mA		—	—	0.4	V

* Steady state current *** V_{CC}=5V, T_a=25°C
** TBD

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C, 1MHz V_{in}=0V)

Item	Symbol	typ	max	Unit
Input Capacitance (A_0~A_{16}, $\overline{CE}$)	C_{in}	—	10	pF
Output Capacitance (D_0~D_7)	C_{out}	—	15	pF

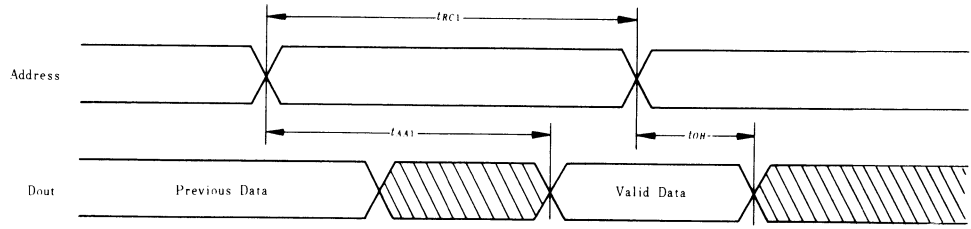
■AC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C, t_r=t_f=20ns)

Mode	Item	Symbol	min	max	Unit
Normal	Cycle Time	t_{RC1}	350	—	ns
	Address Access Time	t_{AA1}	—	350	ns
	Data Hold Time	t_{OH}	10	—	ns
$\overline{CE}$ operation	$\overline{CE}$ Access Time	t_{ACE}	—	350	ns
	$\overline{CE}$ Enable Pulse Width	t_{CE}	350	—	ns
	$\overline{CE}$ Disable Pulse Width	$t_{\overline{CE}}$	15	—	ns
	Address Set up Time	t_{AS}	0	—	ns
	Data Hold Time from $\overline{CE}$	t_{CHZ}	10	** 150	ns
	Data Set Time from $\overline{CE}$	t_{CLZ}	10	—	ns
Nibble operation***	Nibble Address Access Time*	t_{AA2}	—	100	ns
	Nibble Cycle Time	t_{RC2}	100	—	ns

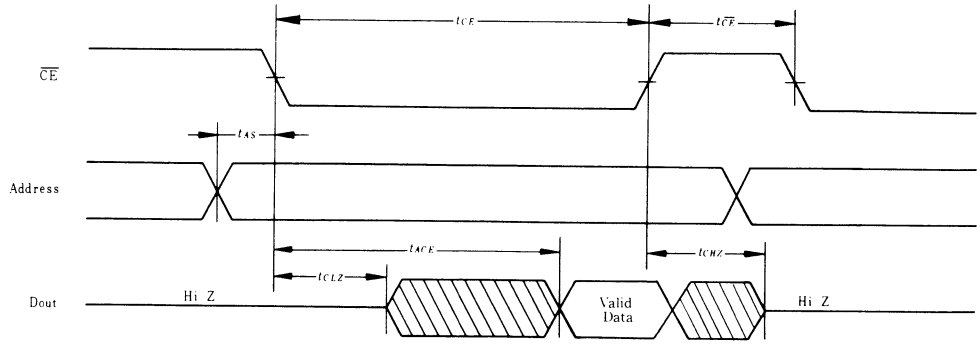
* Nibble Address A_0, A_1 **TBD
*** The specifications of this mode are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept, regarding specifications.

■TIMMING CHART

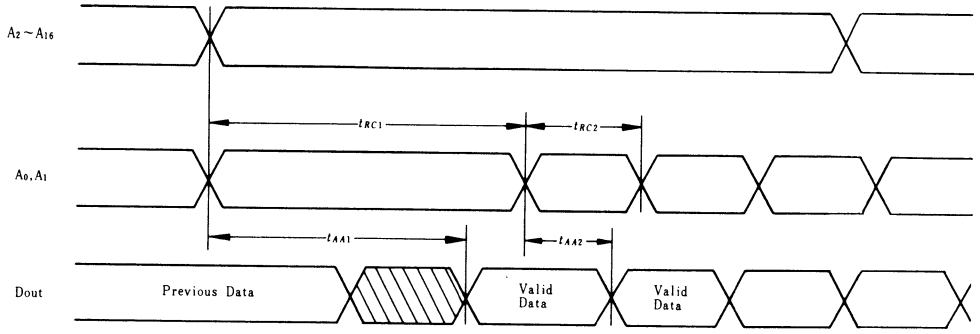
●NORMAL CYCLE ($\overline{CE}$=Low)



●$\overline{CE}$ CYCLE

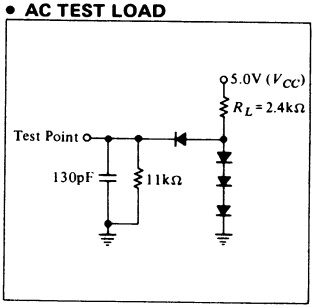


●NIBBLE CYCLE*



* Please contact your nearest Hitachi's Sales Dept. regarding specifications.

● AC TEST LOAD

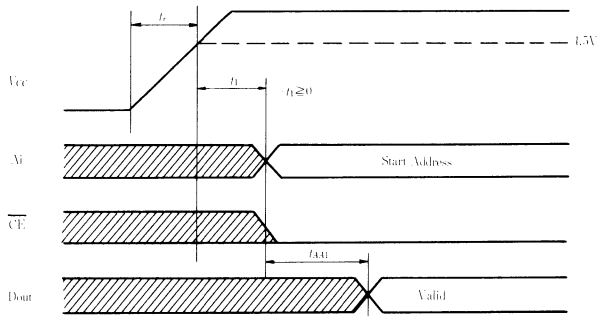


Notes) 1. $t_r = t_f = 20$ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.
4. Input pulse level : 0.8 to 2.4V
5. Input and output timing reference level : 1.5V

• $\overline{CE}$ DUMMY CYCLE

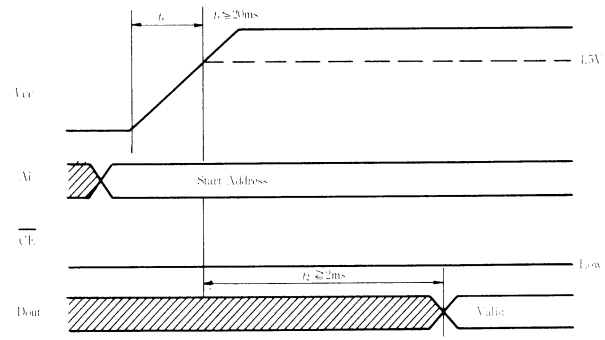
$\overline{CE}$ dummy cycle is necessary when V_{CC} rise time is longer than 20 ms.

CASE 1



(Note) 1. There is no limitation for V_{CC} rise time when at least one of addresses or $\overline{CE}$ signal is changed after power-up ($V_{CC} \geq 4.5V$). 350ns is required for the access after the transition.

CASE 2



(Note) 1. Transition of neither address nor $\overline{CE}$ is necessary for system initialization when V_{CC} rise time is less than 20ms, because of Vcc–detective-circuit-operation.
2ms is required for the access after power-up.

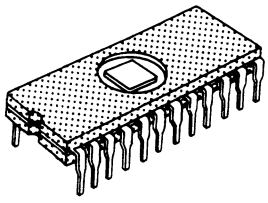
MOS PROM

HN482732AG-20, HN482732AG-25, HN482732AG-30

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.

The transparent lid on the package allow the memory content to be erased with ultraviolet light.

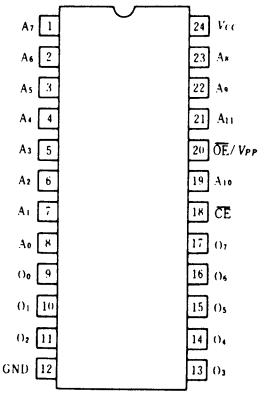


(DG-24B)

■ FEATURES

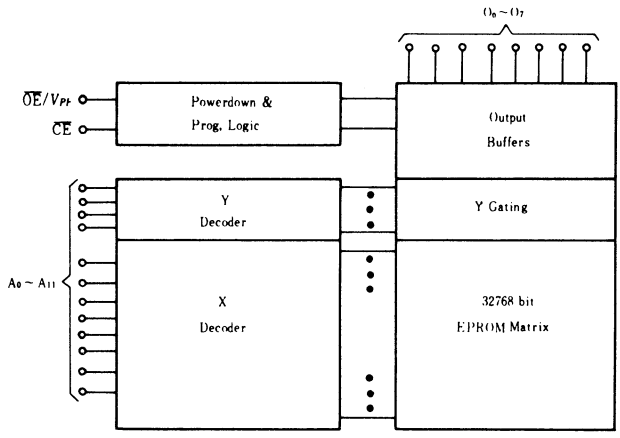
- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static..... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time ..... HN482732AG-20 200ns (max)
  HN482732AG-25 250ns (max)
  HN482732AG-30 300ns (max)
- Absolute Max. Rating of Vpp Pin ... 26.5V
- Low Stand-by Current ..... 35mA (max)
- Compatible with Intel 2732A

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Pins / MODE	CE (18)	OE/VPP (20)	Vcc (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	D_{out}
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{in}
Program Verify	V_{IL}	V_{IL}	+5	D_{out}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_{in}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	$\overline{OE}/V_{PP}$	−0.3 to 26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■ READ OPERATION

● D.C. AND OPERATING CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%, V_{pp}=V_{cc} ±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V	—	—	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}=\overline{CE}=V_{IL}$	—	—	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%, V_{pp}=V_{cc} ±0.6V)

Parameter	Symbol	Test Conditions	HN482732AG-20		HN482732AG-25		HN482732AG-30		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	—	200	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	—	200	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	10	90	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$	0	80	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	—	0	—	0	—	ns

● SWITCHING CHARACTERISTICS

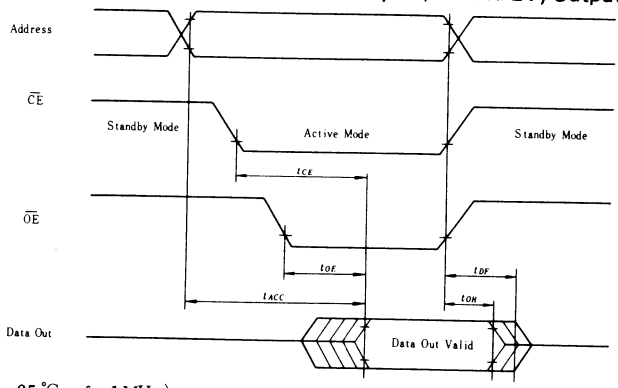
Test Conditions

Input Pulse Level: . . . . . 0.8V to 2.2V

Input Rise and Fall Times: . . . . . ≦ 20ns

Output Load: . . . . . 1 TTL Gate + 100PF

Reference Level for Measuring Timing . . . . . Inputs, 1V and 2V, Outputs; 0.8V and 2V



● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$)	C_{IN1}	V_{IN}=0V	—	—	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}	V_{IN}=0V	—	—	20	pF
Output Capacitance	C_{out}	V_{out}=0V	—	—	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=V_{IL}$ or V_{IH}	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Supply Current	I_{CC}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{PP}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Chip Enable to Output Float Delay*	t_{DF}		0	—	130	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IL}$	—	—	1	μs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	—	—	ns
V_{PP} Recovery Time	t_{VR}		2	—	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

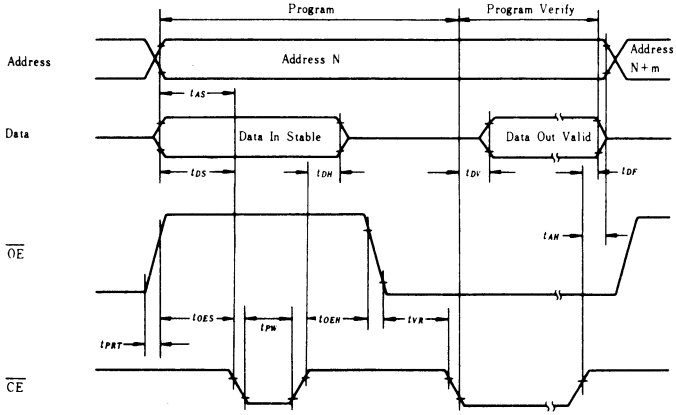
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level ..... 0.8V to 2.2V

Input Rise and Fall Time ..... ≦ 20ns

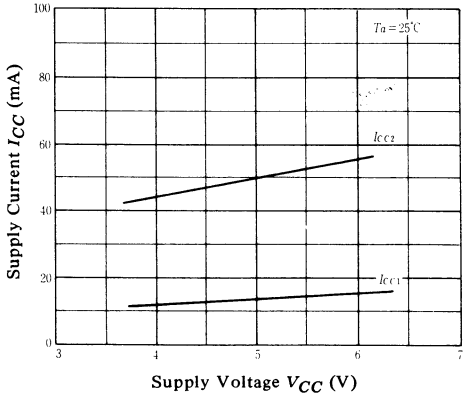
Reference Level for Measuring Timing: ..... Inputs 1V and 2V; Outputs 0.8V and 2V



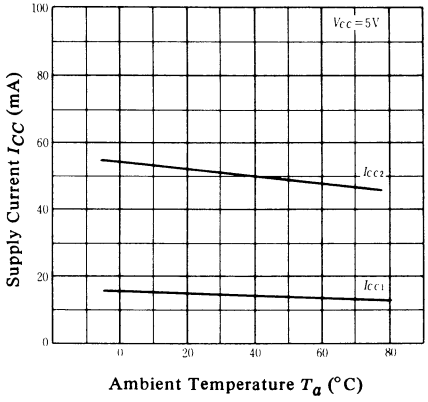
● ERASE

Erasure of HN482732A is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm^2

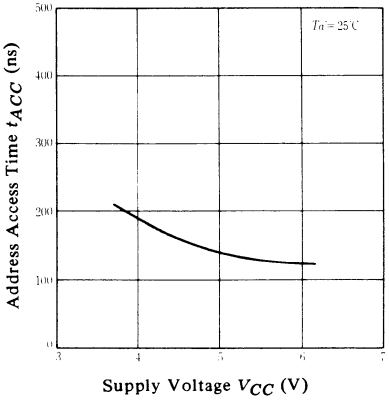
SUPPLY CURRENT vs. SUPPLY VOLTAGE



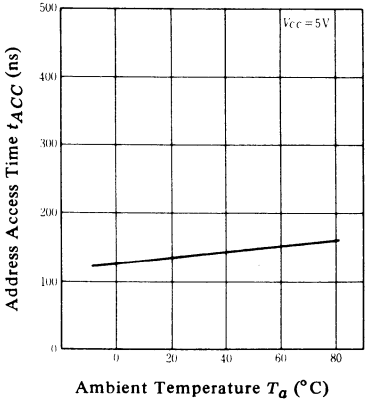
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE

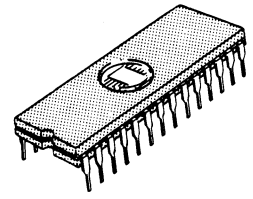


HN482764G,HN482764G-2, HN482764G-3

8192-word x 8-bit UV Erasable and Programmable Read Only Memory

The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764G, HN482764G-2
HN482764G-3

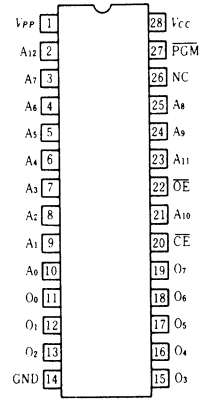


(DG-28)

■ FEATURES

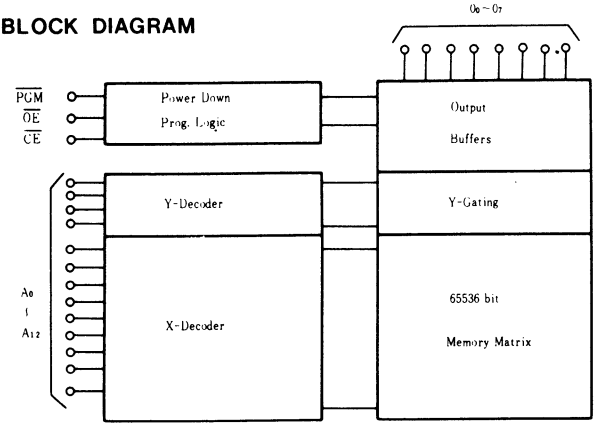
- Single Power Supply . . . . . +5V ± 5%
- Simple Programming . . . . . Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time . . . . . HN482764G-2 200ns max
  HN482764G 250ns max
  HN482764G-3 300ns max
- High Performance Programming Available
- Low Standby Current . . . . . 35mA max.
- Compatible with Intel 2764

■ PIN ARRANGMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltage*	V_T	−0.6 to +7	V
V_{PP} Voltage	V_{PP}	−0.6 to +26.5	V

* : with respect to GND

HITACHI

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{in}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	40	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

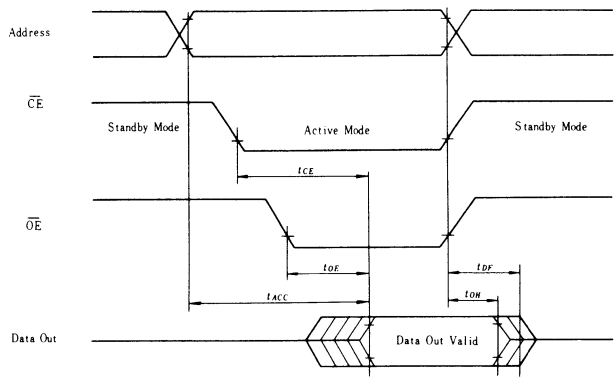
Parameter	Symbol	Test Conditions	HN482764G-2		HN482764G		HN482764G-3		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
CE to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
OE to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	10	80	10	100	10	150	ns
OE High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	70	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Output; 0.8V and 2.0V



● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

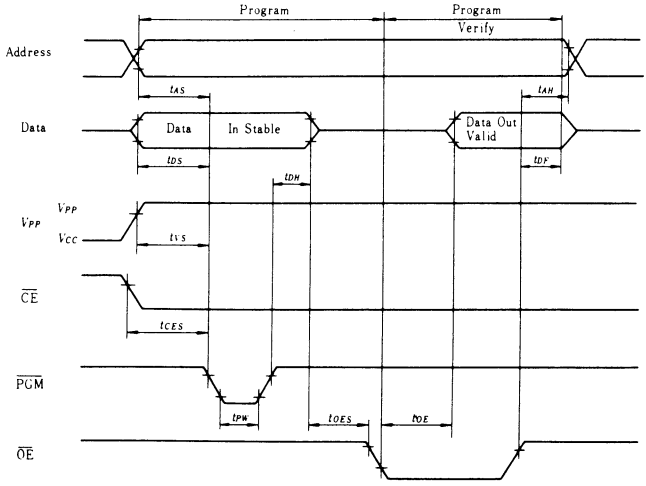
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

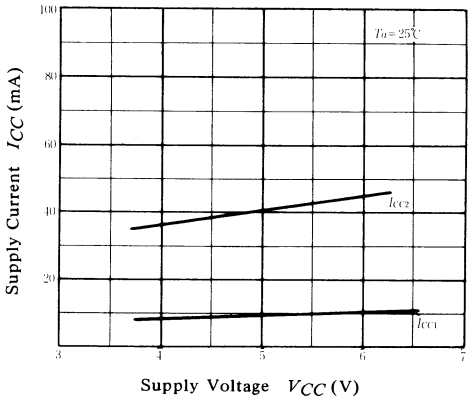
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



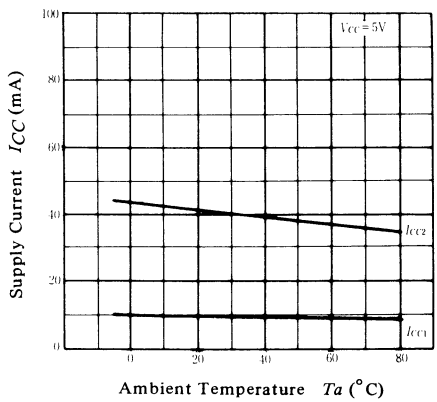
■ ERASE

Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W・sec/cm²

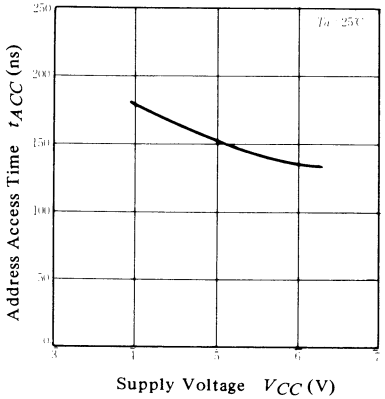
SUPPLY CURRENT VS. SUPPLY VOLTAGE



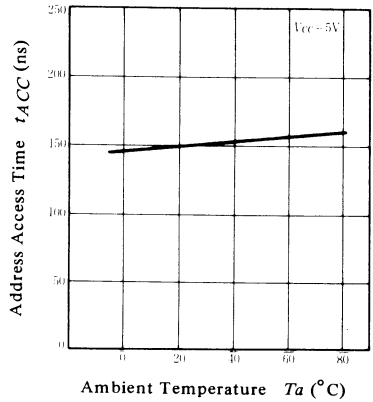
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE

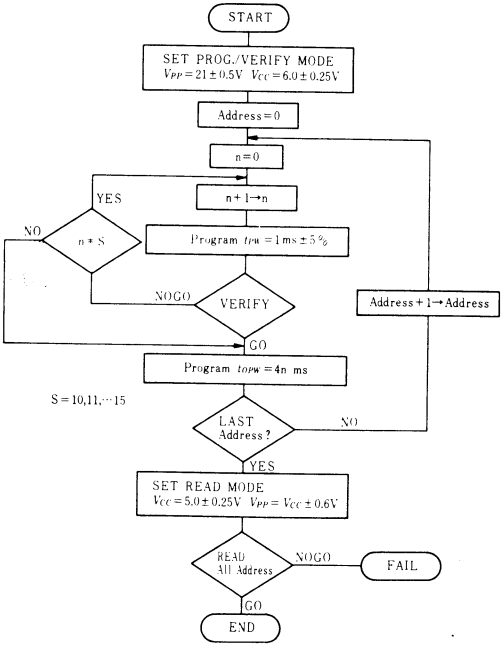


ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

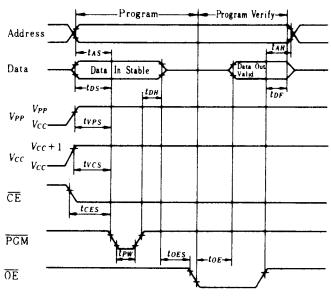
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

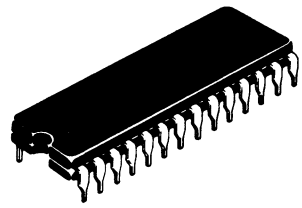


HN482764P-3

8192-word x 8-bit One Time Electrically Programmable ROM

The HN482764P-3 is a 8192 word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN482764P-3 are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, dual-in-line plastic package. Therefore, this device can not be re-written.

HN482764P-3

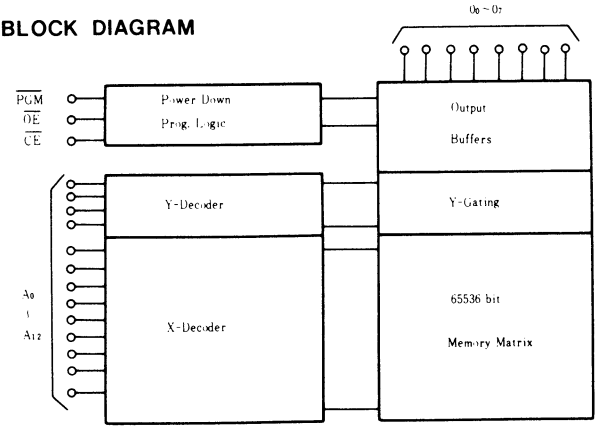


(DP-28)

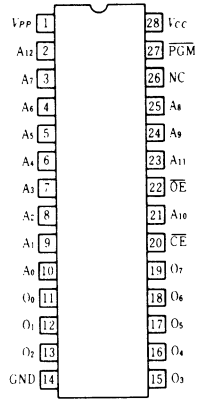
■ FEATURES

- Spring Power Supply . . . . . +5V ±5%
- Simple Programming . . . . Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time . . . . . 300ns max.
- Low Standby Current . . . . . 35mA max.
- Compatible with Intel P2764

■ BLOCK DIAGRAM



■ PIN ARRANGMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
All Input and Output Voltage*	V_T	−0.6 to +7	V
V_{PP} Voltage	V_{PP}	−0.6 to +26.5	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.25V, V_{in} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.25, V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = V_{CC} + 0.6V	–	–	15	mA
V_{CC} Current (Standby)	I_{CC1}	CE = V_{IH}	–	–	35	mA
V_{CC} Current (Active)	I_{CC2}	CE = OE = V_{IL}	–	40	100	mA
Input Low Voltage	V_{IL}		-0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400μA	2.4	–	–	V

● AC CHARACTERISTICS (T_a = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V, T_a = 0 to +70°C)

Parameter	Symbol	Test Conditions	min	max	Unit
Address to Output Delay	t_{ACC}	CE = OE = V_{IL}	–	300	ns
CE to Output Delay	t_{CE}	OE = V_{IL}	–	300	ns
OE to Output Delay	t_{OE}	CE = V_{IL}	10	150	ns
OE High to Output Float*	t_{DF}	CE = V_{IL}	0	130	ns
Address to Output Hold	t_{OH}	CE = OE = V_{IL}	0	–	ns

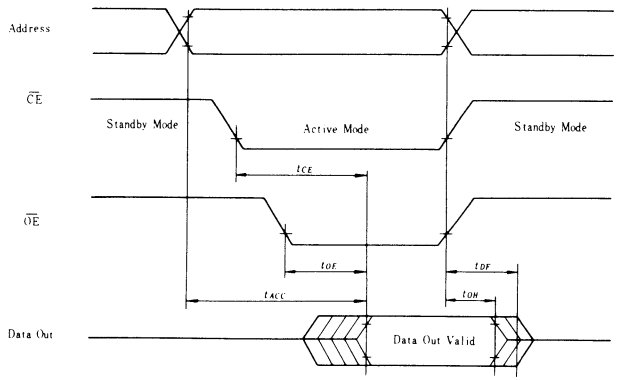
* t_{DF} defines the time at which the output achives the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levles: 0.8V to 2.2V
Input Rise and Fall Times: ≦20ns.
Output Load: 1TTL Gate + 100pF

Reference Level for Measuring Timing:
Inputs ; 1V and 2V
Outputs; 0.8V and 2V



● CAPACITANCE (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

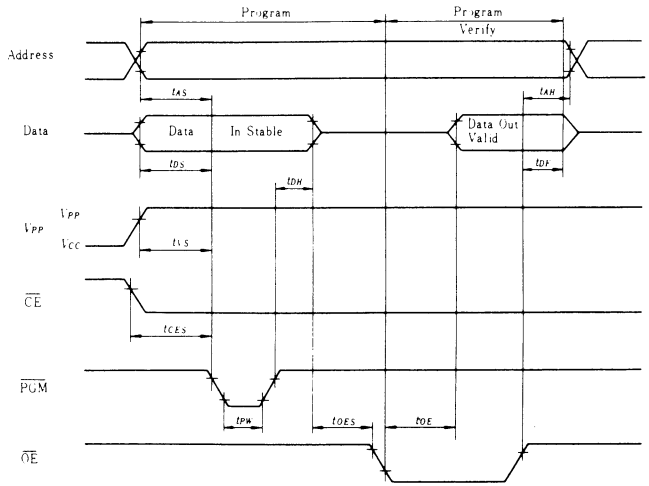
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	1 0	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

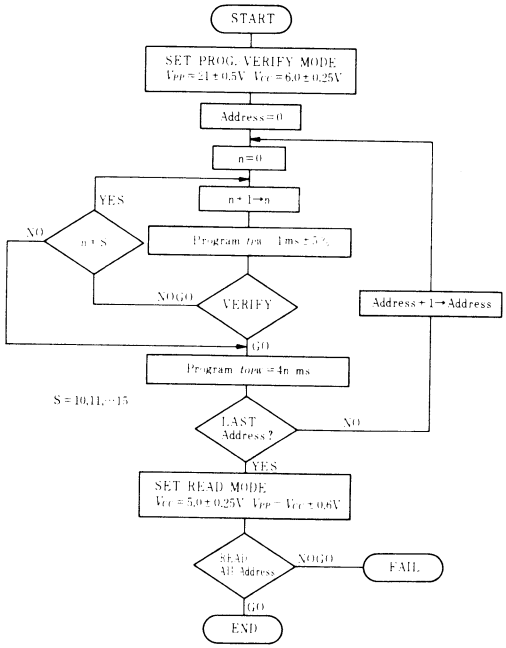
Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta = 25 °C ± 5 °C, V_{CC} = 6V ± 0.25V, V_{PP} = 21V ± 0.5V)

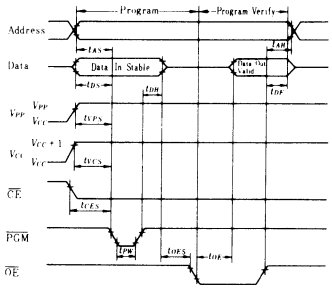
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

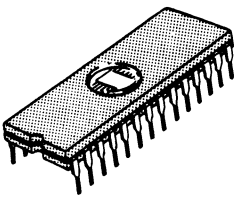


HN27C64G-15, HN27C64G-20, HN27C64G-25, HN27C64G-30

8192-word x 8-bit U.V. Erasable and Programmable CMOS ROM

The CMOS EPROM HN27C64 is a 8192-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent lid.

The transparent lid allows the memory content to be erased with ultraviolet light, where by a new pattern can then be written into the device.

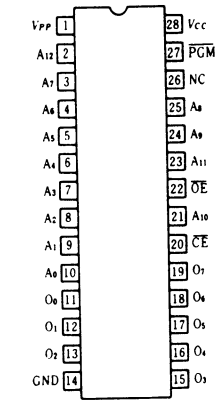


(DG-28)

■ FEATURES

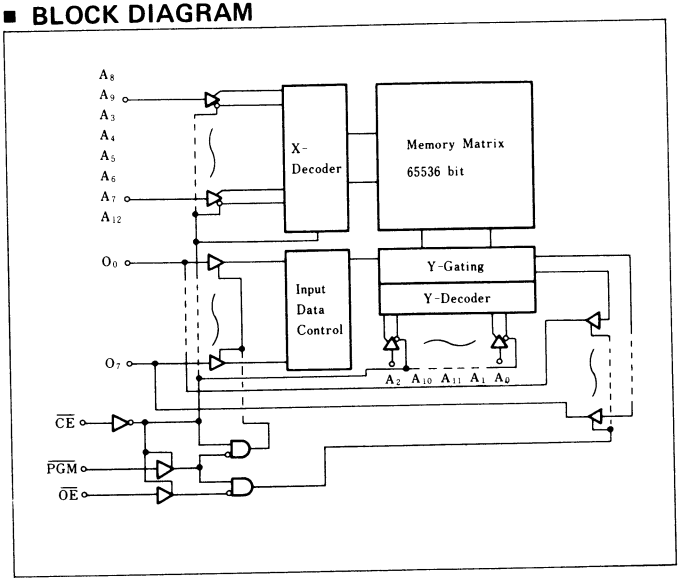
- Low Power Dissipation ..... 40mW/MHz max. (Active Mode)
  550μW max. (Stand by Mode)
- Access Time ..... 150ns max. (HN27C64G-15)
  200ns max. (HN27C64G-20)
  250ns max. (HN27C64G-25)
  300ns max. (HN27C64G-30)
- Single Power Supply ..... +5V±10%
- Simple Programming ..... Program Voltage; +21V D.C.
  Program with One 50ms Pulse
- Support High Performance Programming
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-chip Address Decode
- Compatible with Intel 2764

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*	V_T	−1.0**~ +7.0	V
V_{CC} Voltage*	V_{CC}	−0.6 ~ + 7.0	V
V_{PP} Voltage*	V_{PP}	−0.6 ~ + 25	V
Operating Temperature Range	T_{opr}	0 ~ + 70	°C
Storage Temperature Range	T_{stg}	−65 ~ + 125	°C

* With respect to GND
**Pulse Width: 50ns, DC: −0.5V

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta =0~ + 70°C, V_{CC} =5V ± 10%, V_{PP} = V_{CC} ±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC}=5.5V, V_{out}=GND to V_{CC}	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}= V_{CC} + 0.6V	–	1	100	μA
V_{CC} Current (Stand-by)	I_{SB1}	$\overline{CE}$= V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$= V_{CC} ±0.3V	–	1	100	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE}$= V_{IL}, I_{out}=0 mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0 mA	–	–	30	mA
Input Voltage	V_{IL}		−1.0*	–	0.8	V
	V_{IH}		2.2	–	V_{CC} + 1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1 mA	–	–	0.45	V
	V_{OH}	I_{OH}= −400μA	2.4	–	–	V

*Pulse Width: 50ns, DC: V_{IL} min = −0.3V

• AC CHARACTERISTICS (Ta =0~ + 70°C, V_{CC} =5V ± 10%, V_{PP} = V_{CC} ±0.6V)

Parameter	Symbol	Test Condition	HN27C64G-15		HN27C64G-20		HN27C64G-25		HN27C64G-30		Unit
			min	max	min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$= V_{IL}, $\overline{PGM}$= V_{IH}	–	150	–	200	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$= V_{IL}, $\overline{PGM}$= V_{IH}	–	150	–	200	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$= V_{IL}, $\overline{PGM}$= V_{IH}	10	60	10	70	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$= V_{IL}, $\overline{PGM}$= V_{IH}	0	50	0	60	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$= V_{IL}, $\overline{PGM}$= V_{IH}	0	–	0	–	0	–	0	–	ns

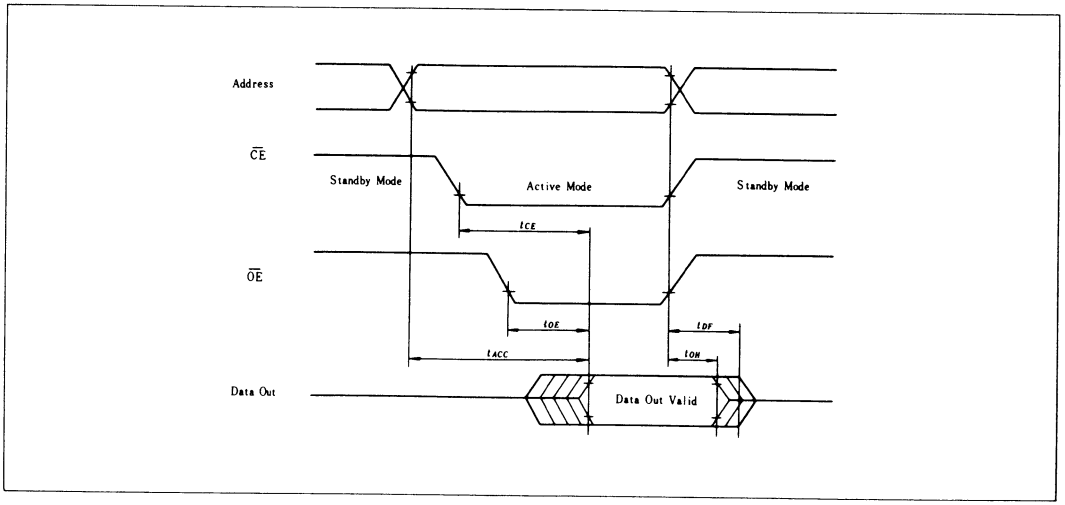
• CAPACITANCE (Ta =25°C, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Output Load:	1TTL + 100pF
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



■ PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V/0.45V	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=–400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+1.0	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	–	–	30	mA

Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 25V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}= 21V.
4. Do not alter V_{PP} either V_{IL} to 21V or 21V to V_{IL} when $\overline{CE}$=$\overline{PGM}$=Low.

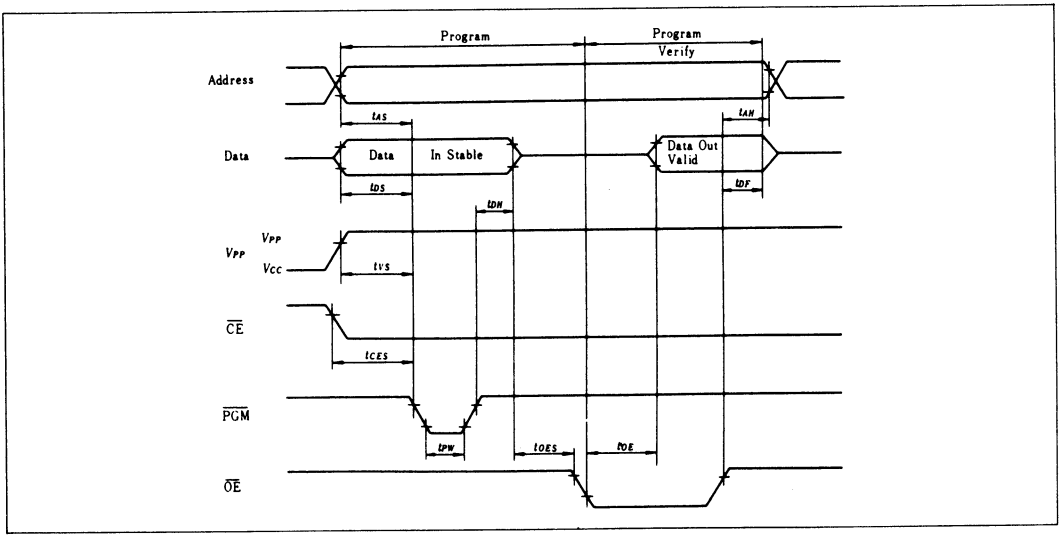
• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	–	130	ns
V_{PP} Setup Time	t_{VS}		2	–	–	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		25	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

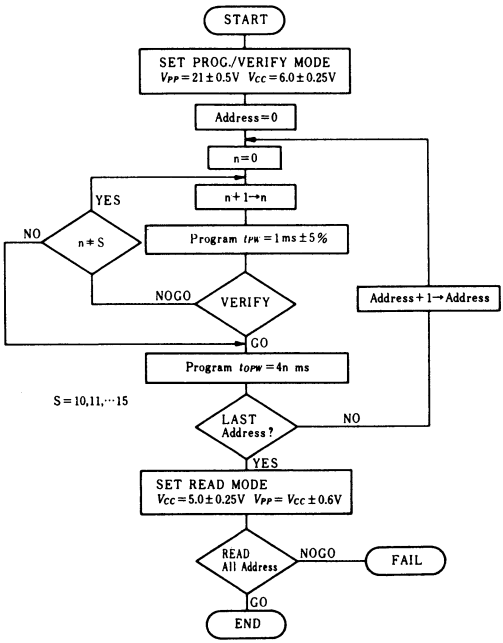


■ ERASE

Erasure of HN27C64 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm^2.

■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

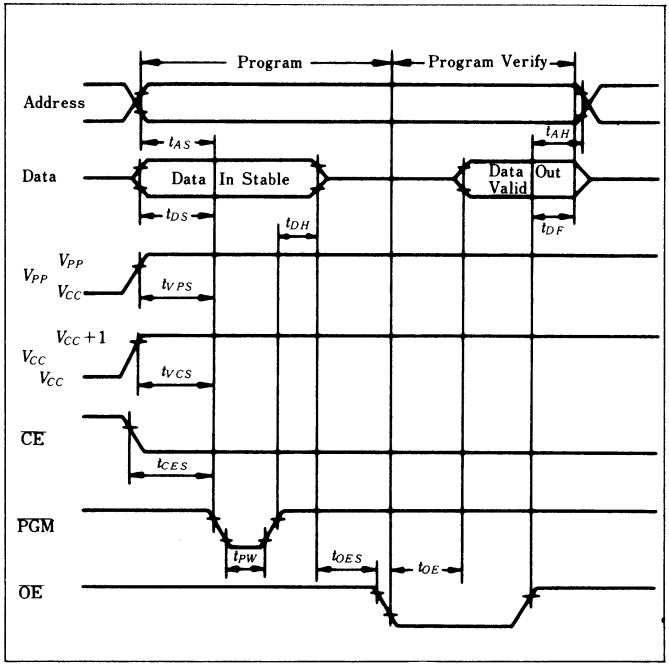
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

• SWITCHING CHARACTERISTICS

Test Condition

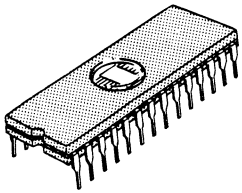
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



HN4827128G-25,
HN4827128G-30,
HN4827128G-45

16384-Word x 8-bit UV Erasable and Programmable Read Only Memory

The HN4827128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

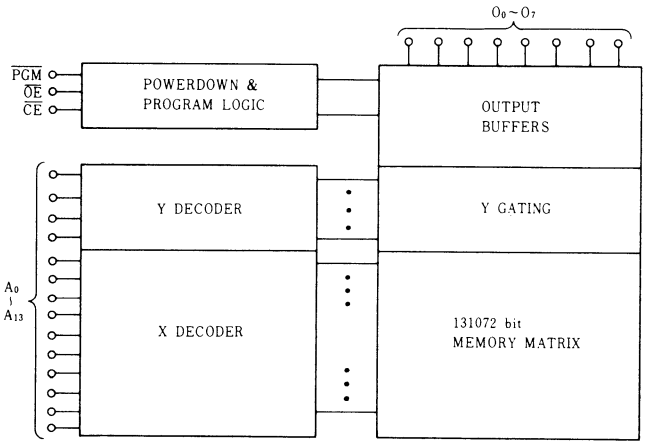


(DG-28)

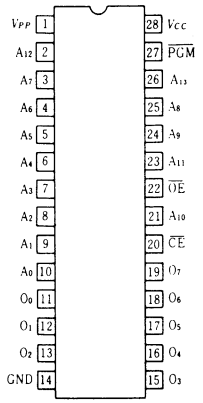
■FEATURES

- Single Power Supply . . . . . +5V ± 5%
- Simple Programming . . . . . Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
  Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 250ns/300ns/450ns
- Absolute Max. Rating of Vpp Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with INTEL 27128

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.6 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.6 to +7	V

* with respect to GND

■READ OPERATION

●DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	60	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

●AC CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

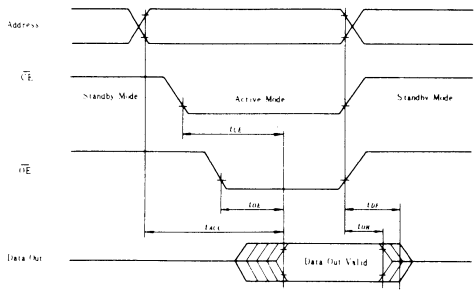
Parameter	Symbol	Test Condition	HN4827128G-25		HN4827128G-30		HN4827128G-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	—	100	—	120	—	150	ns
$\overline{OE}$ High to Output Float	t_{DF}*	$\overline{CE}$=V_{IL}	0	85	0	105	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤ 20 ns
Output Load: 1 TTL Gate + 100 pF
Reference Level for Measuring Timing: Inputs; 1V and 2V
Outputs; 0.8V and 2.0V



●CAPACITANCE (Ta=25℃, f= 1 MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

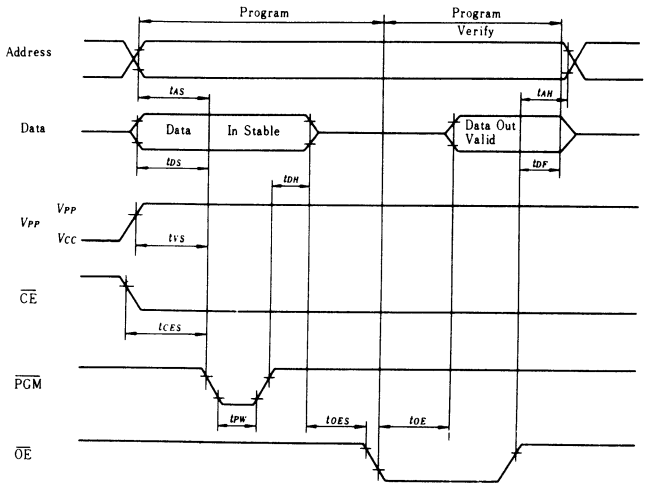
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.8V to 2.2V
Input Rise and Fall Time: ≤ 20 ns
Reference Level for Measuring Timing: Input; 1V and 2V
Output; 0.8V and 2V

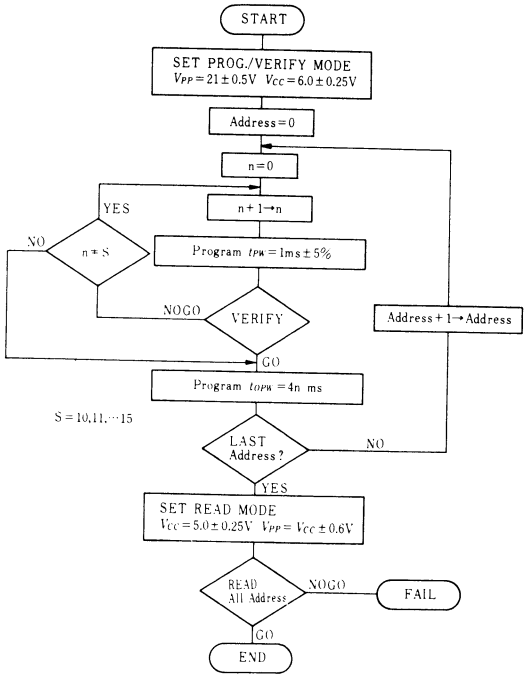


●ERASE

Erasure of HN4827128 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W·sec/cm^2.

■HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

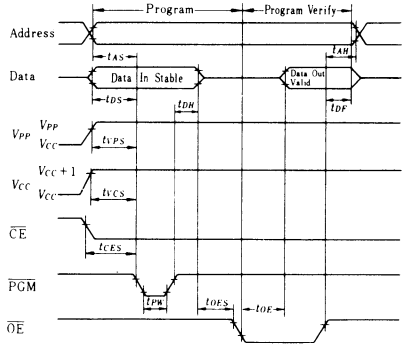
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

* t_{DF} defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flow chart.

●SWITCHING CHARACTERISTICS

Test Condition

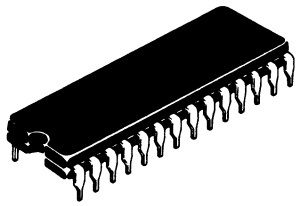
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



HN4827128P-30 — Preliminary

16384-word x 8-bit One Time Electrically Programmable ROM

The HN4827128P-30 is a 16384-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN4827128P-30 are in the "1" state (Output High).
Data is introduced by selectively programing "0" into the desired bit locations. This device is packaged in a 28 pin, dual-in-line plastic package. Therefore, this device can not be re-written.

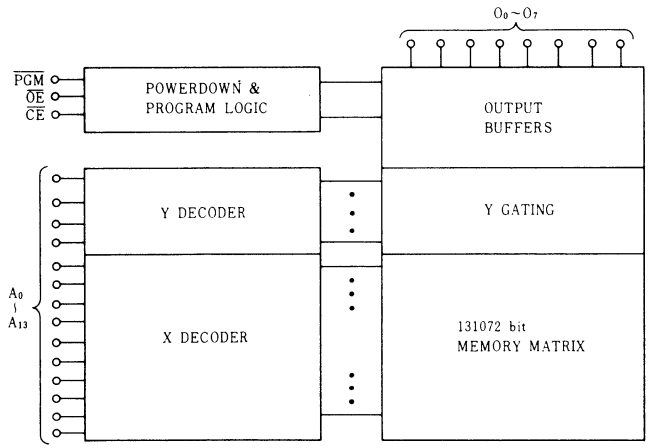


(DP-28)

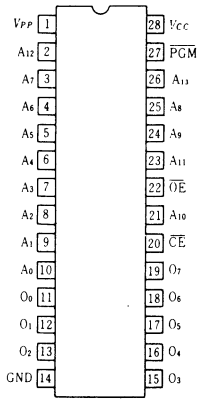
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Simple Programming . . . . . Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 300ns
- Absolute Max. Rating of V_{PP} Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with Intel 27128

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

MODE \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : Don't care

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.3 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	60	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	max	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	300	ns
CE to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	300	ns
OE to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	120	ns
OE High to Output Float*	t_{DF}	$\overline{CE}$ = V_{IL}	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

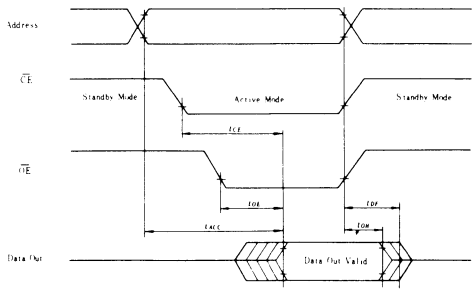
Input Pulse Levels: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

Output Load: 1 TTL Gate + 100 pF

Reference Level for Measuring Timing: Inputs; 1V and 2V

Outputs; 0.8V and 2.0V



● CAPACITANCE (Ta=25°C, f= 1 MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

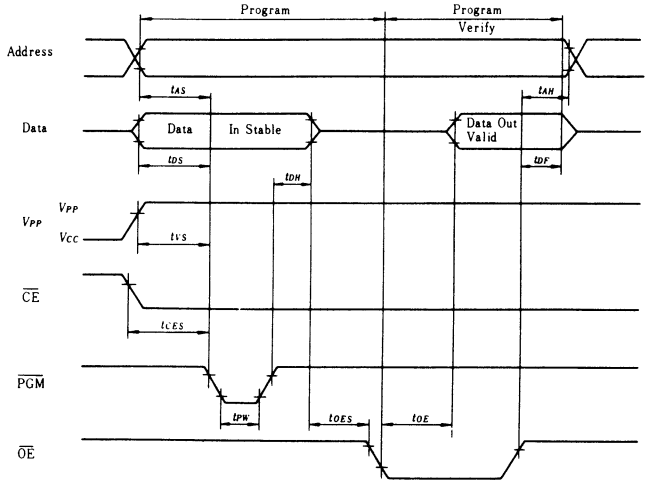
Test Condition

Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

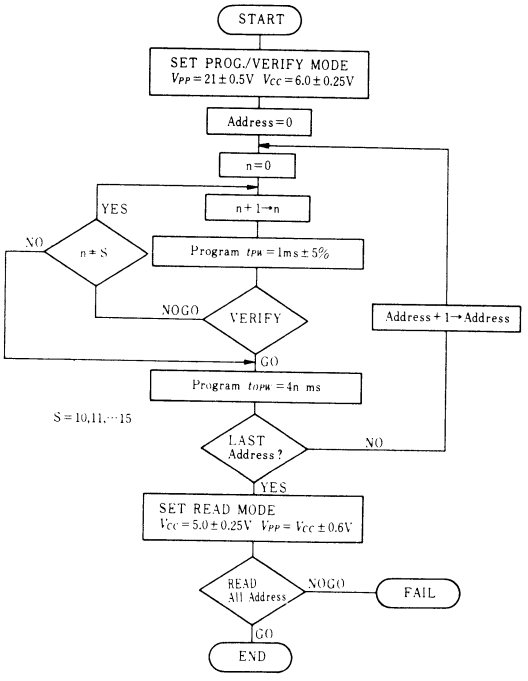
Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V



■HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

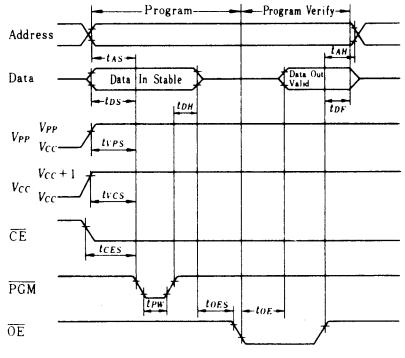
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

* t_{DF} defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flow chart.

●SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



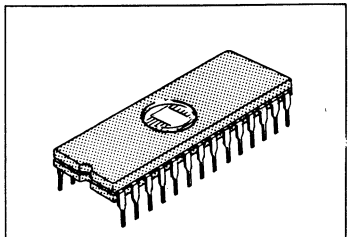
HN27256G-25, HN27256G-30

32768-word x 8-bit UV Erasable and Programmable ROM

Preliminary

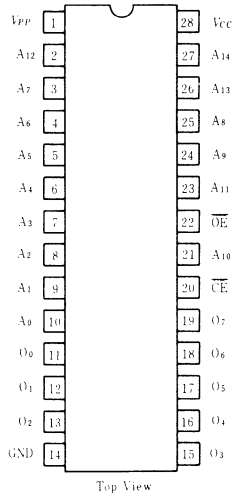
■ FEATURES

- Single Power Supply . . . . . +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
  Automated Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . HN27256G-25: 250ns(max.)
  HN27256G-30: 300ns(max.)
- Absolute Max. Rating of V_{pp} pin . . 13.0V
- Low Stand-by Current . . . . . 40mA (stand-by)
- Compatible with INTEL 27256

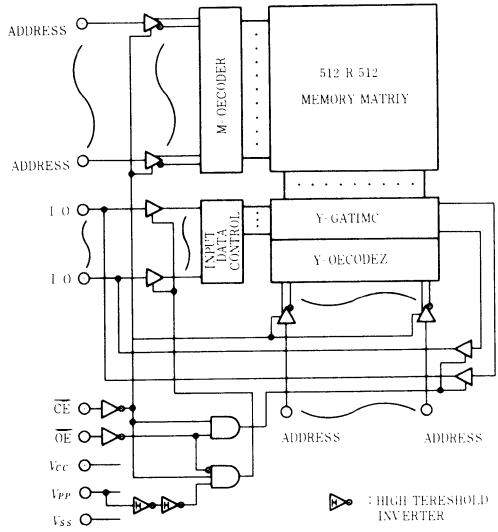


(DG-28)

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{pp} (1)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Stand by	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z

Note) X : Don't care.

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	− 65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	− 10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A_9)*	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*	V_{CC}	−0.6 to +7	V

* with respect to GND.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0~+70°C, V_{CC}=5V±5%, V_{pp}=V_{CC})

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.5 V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5 V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	45	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC} + 1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

• AC CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, V_{pp}=V_{CC})

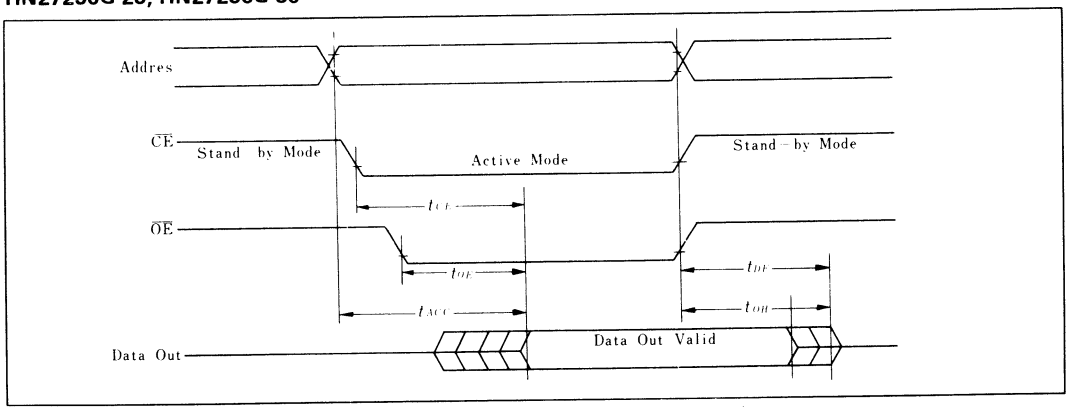
Parameter	Symbol	Test Condition	HN27256G-25		HN27256G-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{OE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

• TEST CONDITION

- Input pulse levels: 0.8V to 2.2V
- Input rise and fall time: ≤20ns
- Output load: 1 TTL Gate +100pF
- Reference level for measuring timing: Inputs ; 1.0V and 2.0V
  Outputs ; 0.8V and 2.0V

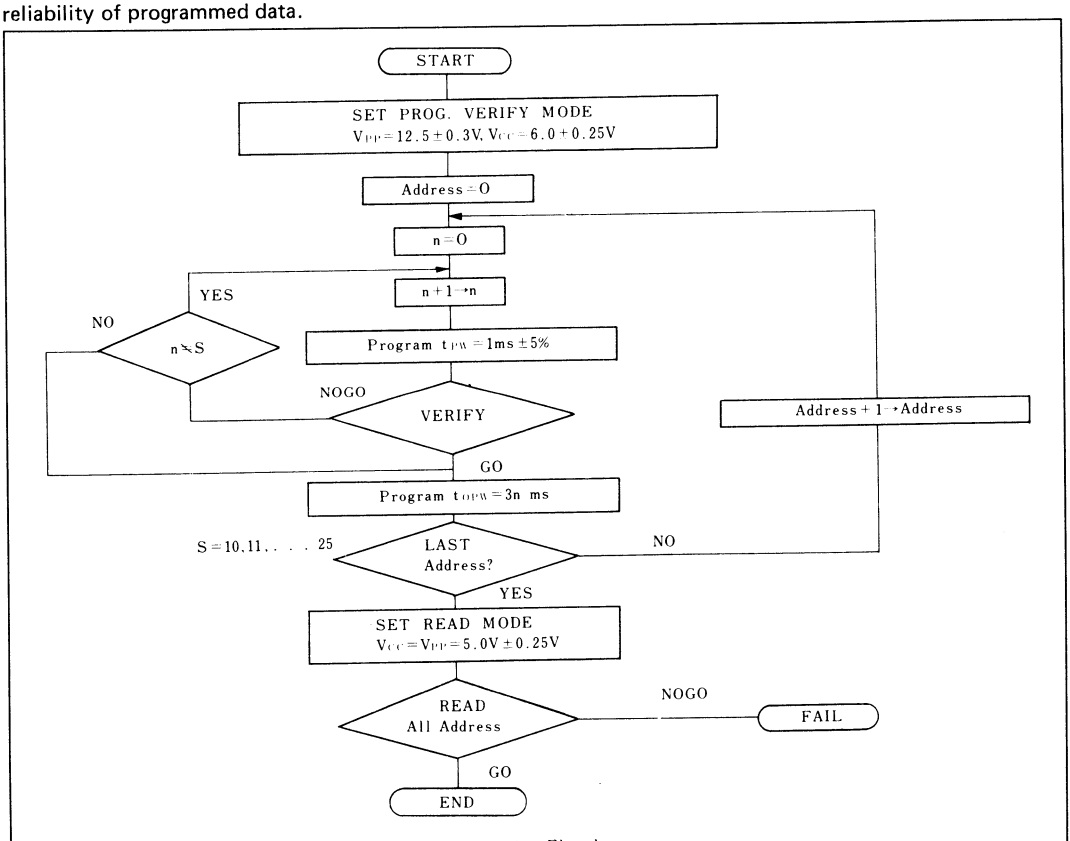


■ CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{cc} Current (Active)	I_{cc2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{cc} + 1	V
V_{pp} Supply Current	I_{pp2}	$\overline{CE}$ = V_{IL}	–	–	50	mA

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DFP}		0	–	130	ns
V_{pp} Setup Time	t_{VPS}		2	–	–	μs
V_{cc} Setup Time	t_{VCP}		2	–	–	μs
PGM Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}		2.85	–	78.75	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

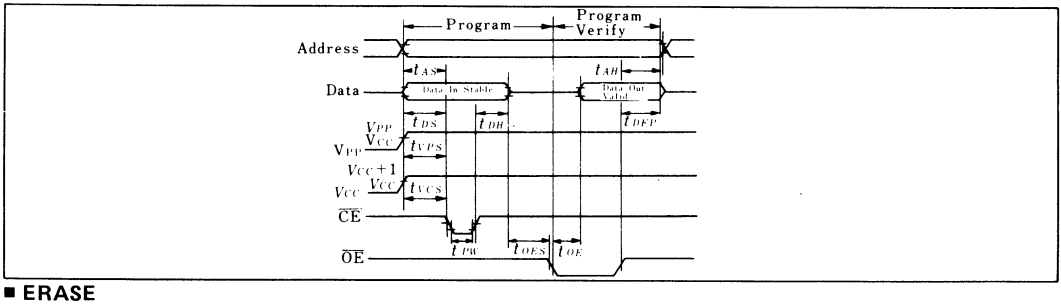
Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DFP} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

• TEST CONDITION

- Input pulse level: 0.8V to 2.2V
- Input rise and fall time: ≤20ns
- Reference level for measuring timing: Input ; 1.0V and 2.0V Output; 0.8V and 2.0V



■ ERASE

Erasure of HN27256G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2.

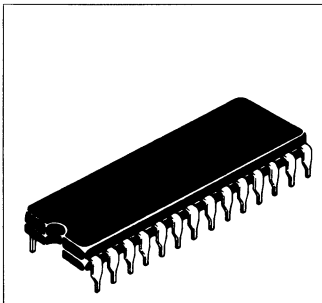
HN58064P-25,HN58064P-30, HN58064P-45

Preliminary

8192-word x 8-bit Electrically Erasable and Programmable ROM

■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Lathes
- Byte Erase/Byte Write Time . . . . . 10ms typ.
- Chip Erase Time . . . . . 20ms typ.
- Fast Access Time . . . . . 250/300/450ns max.
- Low Power Disisipation . . . . . 100mA (max) Active
  40mA (max) Standby
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles



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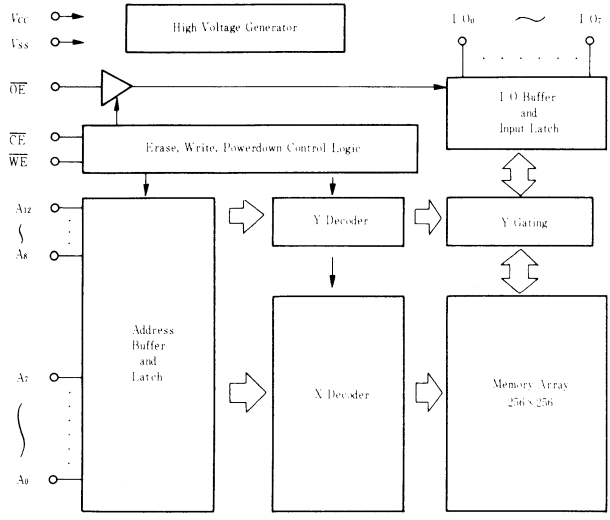
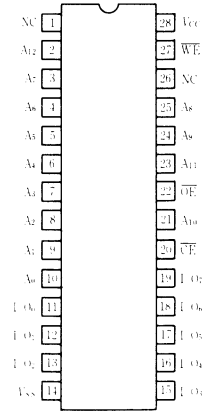
■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	D_{out}
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	$D_{in} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{in}
Chip Erase	V_{IL}	V_{IL}	V_{IL}	$D_{in} = V_{IH}$
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IL} or V_{IH}

$A_0 \sim A_{12}$	Address Input
$I/O_0 \sim I/O_7$	Data in/Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	− 55 to +125	°C

* With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.1	–	0.8	V
	V_{IH}	2.0	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V +10%)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5 ~ 0.4V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}		–	20	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	60	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{in} = 0V	–	–	12	pF

■ AC TEST CONDITIONS

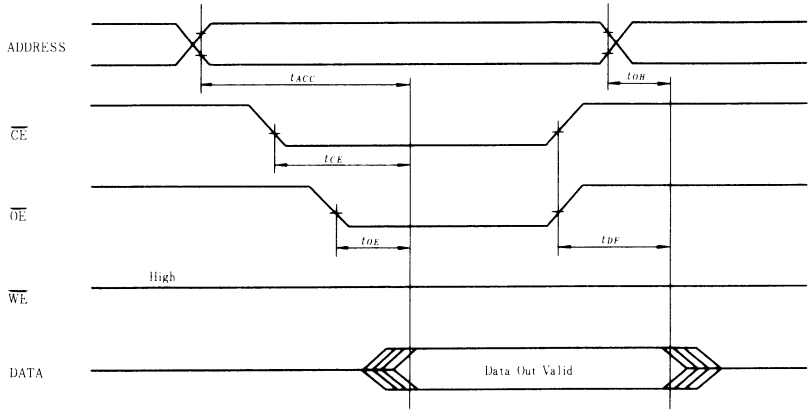
Input Pulse Levels:	0.8V to 2.0V Input
Rise and Fall Time:	≦ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Outputs; 0.8V and 2.0V

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V + 10%)

● READ OPERATION

Parameter	Symbol	Test Condition	HN58064P-25		HN58064P-30		HN58064P-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	100	–	150	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	0	–	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	90	0	130	0	130	ns

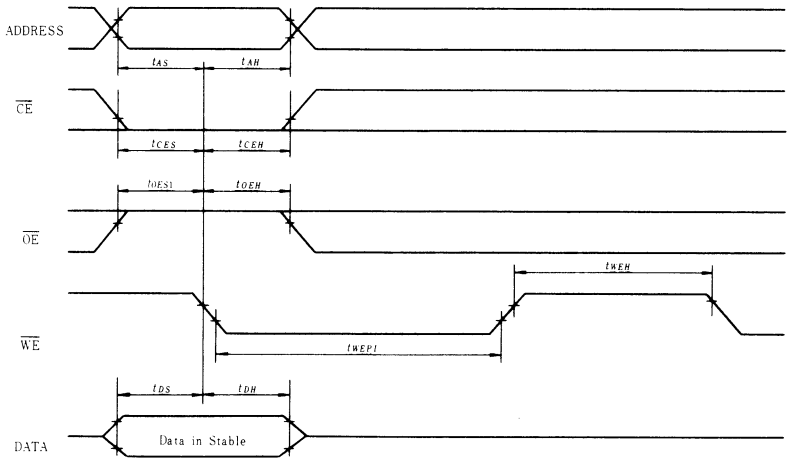
● WAVEFORM ····· READ CYCLE



● BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		10	–	–	ns
Address Hold Time	t_{AH}		50	–	–	ns
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES1}		10	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP1}		8	10	15	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

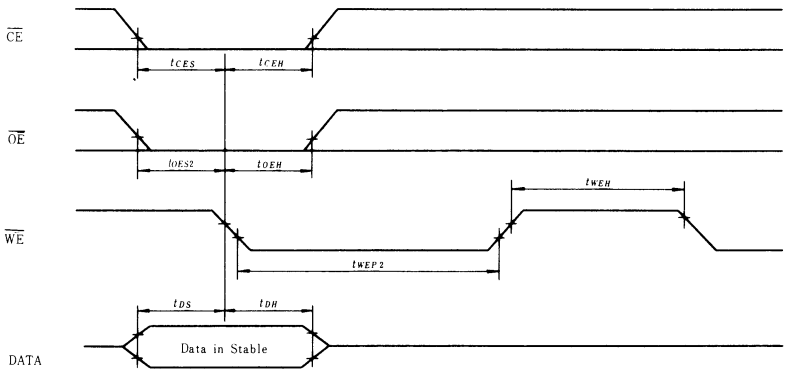
● WAVEFORM ····· ERASE AND WRITE CYCLE



● CHIP ERASE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES2}		0	–	50	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP2}		15	20	50	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

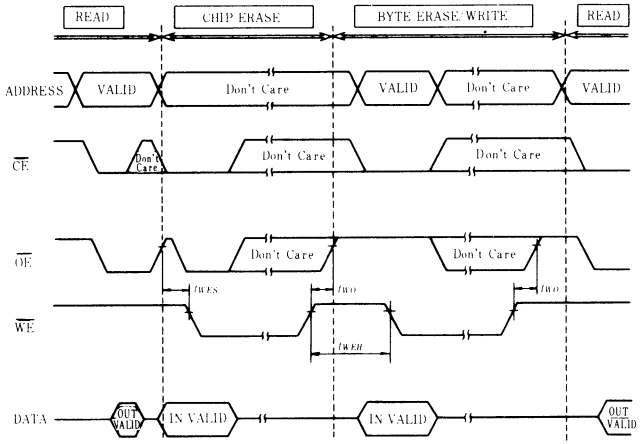
WAVE FORM ····· CHIP ERASE

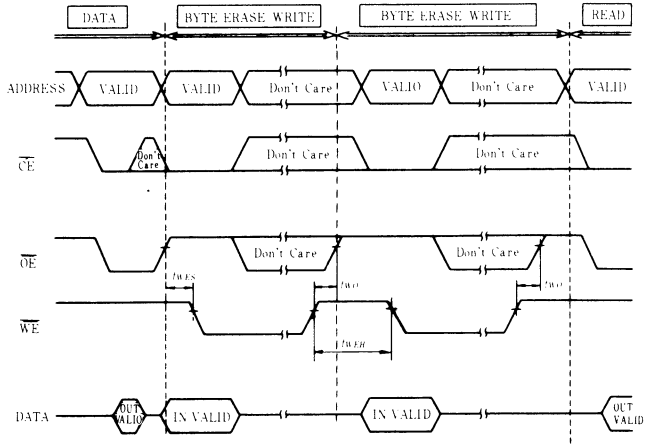


● SEQUENCE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{WE}$ Setup Time	t_{WES}		150	–	–	ns
$\overline{WE}$ to $\overline{OE}$ Time	t_{WO}		50	–	–	ns
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns

● WAVE FORM





BIPOLAR RAM

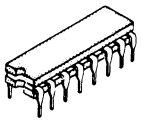
256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

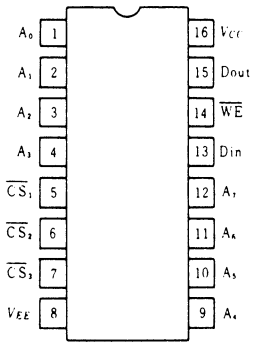
The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



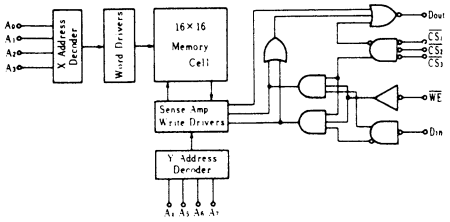
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout*	Read

× : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$, $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	+75°C	—	−130	—	mA
			0°C	−180	−140	—	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACR}		—	3	6	—	3	6	ns
Chip Select Recovery Time	t_{RCS}		—	3	6	—	3	6	ns
Address Access Time	t_{AA}		—	7	10	—	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4	—	ns
Data Setup Time	t_{WSD}		1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	ns
Write Disable Time	t_{WS}		—	—	5	ns
Write Recovery Time	t_{WR}		—	—	5	ns

3. RISE/FALL TIME

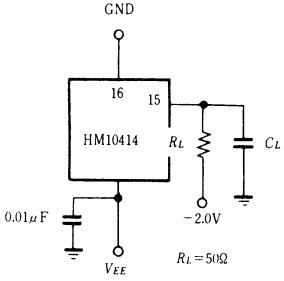
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	1.5	2.5	ns
Output Fall Time	t_f		—	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

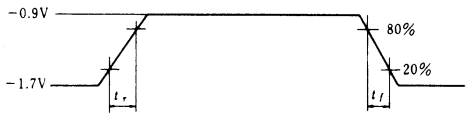
1. LOADING CONDITIONS



$R_L = 50\Omega$

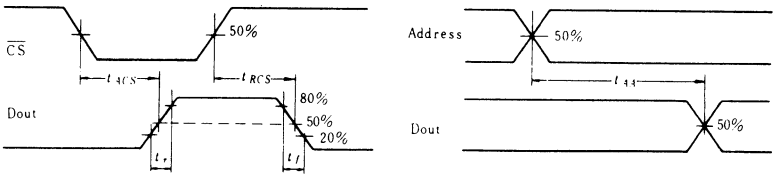
$C_L = 30pF$ (includes jig and stray capacitance)

2. INPUT PULSE

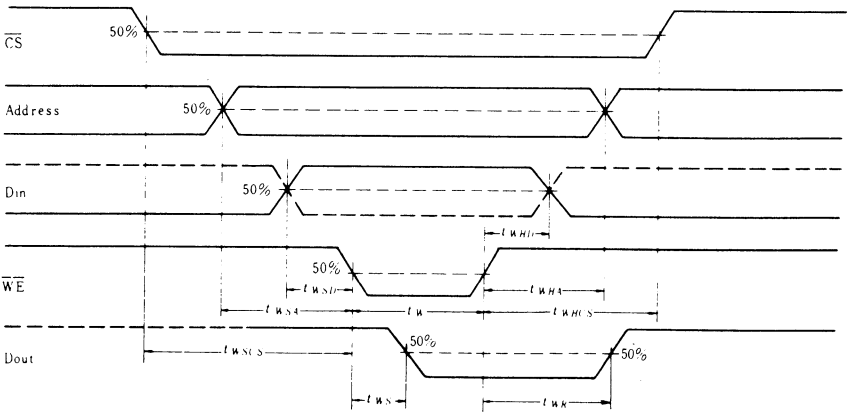


$t_r = t_f = 2.0ns$ typ

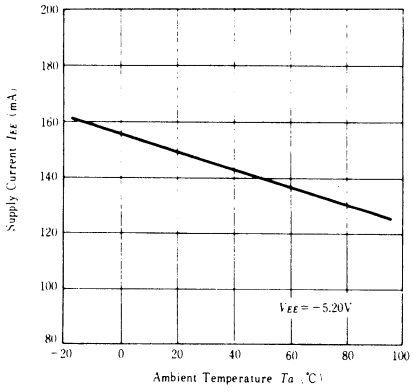
3. READ MODE



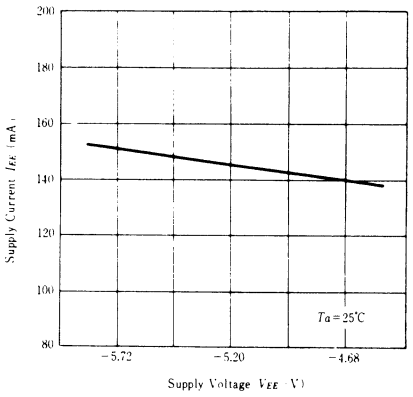
4. WRITE MODE



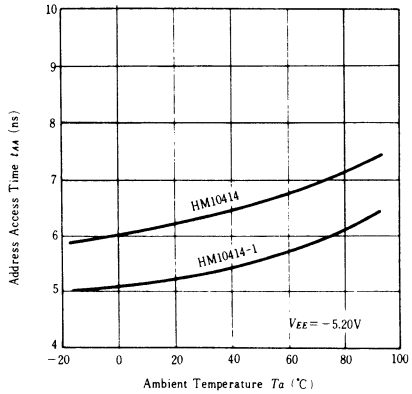
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



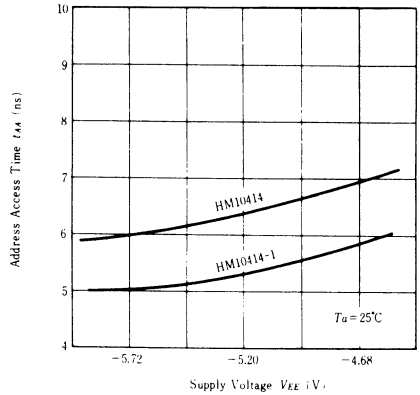
SUPPLY CURRENT vs. SUPPLY VOLTAGE



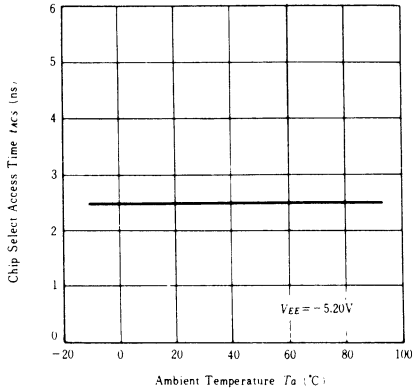
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



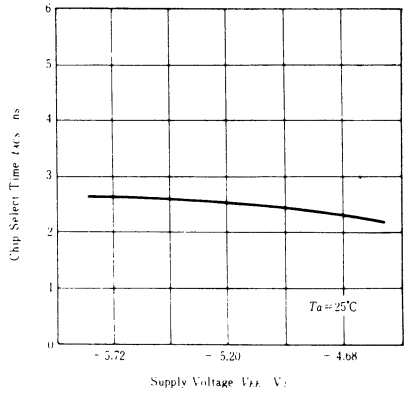
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



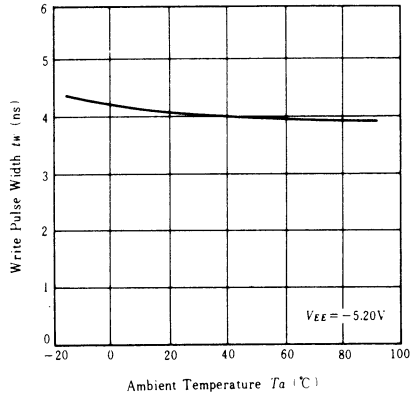
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



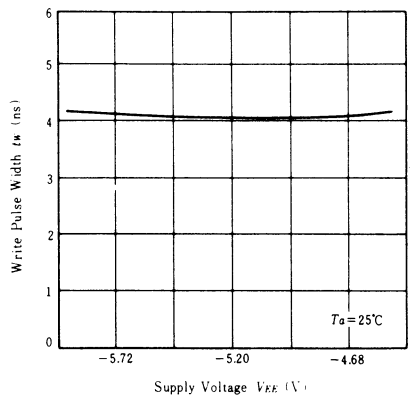
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

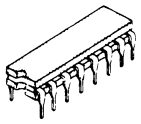


HM2110, HM2110-1

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time ..... 10ns (max.)
- Address access time ..... HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
- Power consumption ..... 0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



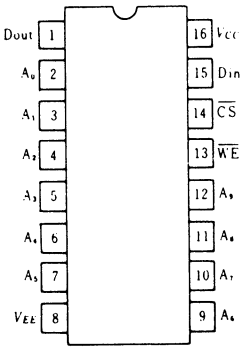
DG - 16A

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

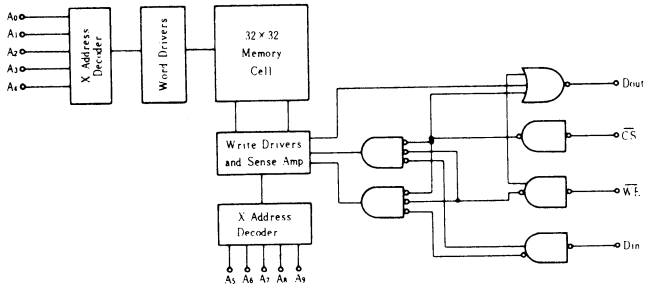
× : irrelevant
* : Read out noninverted

■ PIN ARRANGEMENT



Top View

■ BLOCK DIAGRAM



■ ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$, $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$0 \leqq Ta < 25°C$	−150	−100	—	mA
			$Ta \geqq 25°C$	−125	−90	—	

● AC CHARACTERISTICS

($V_{EE}=-5.2V \pm 5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	ns

3. RISE/FALL TIME

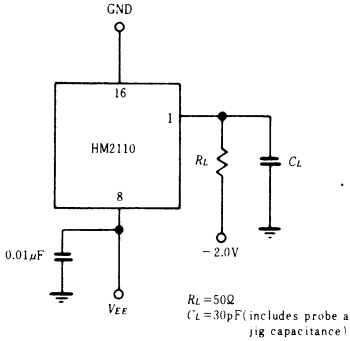
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

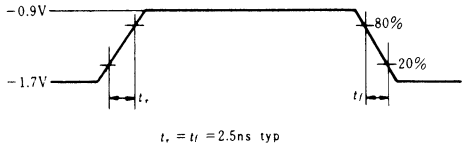
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	5	pF
Output Capacitance	C_{out}		—	7	8	pF

■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

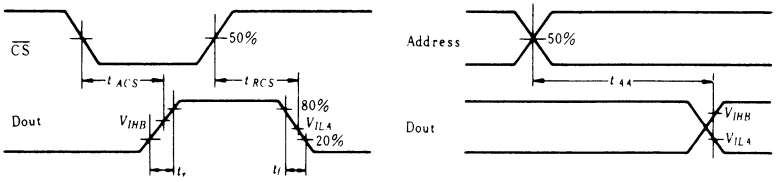


2. INPUT PULSE

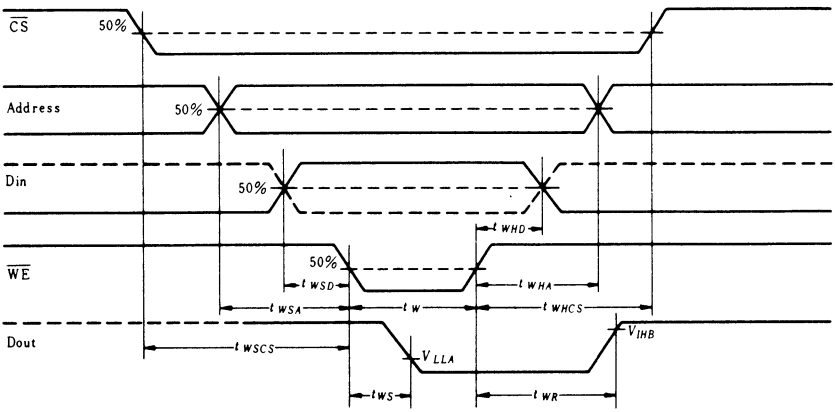


$t_r = t_f$ =2.5ns typ

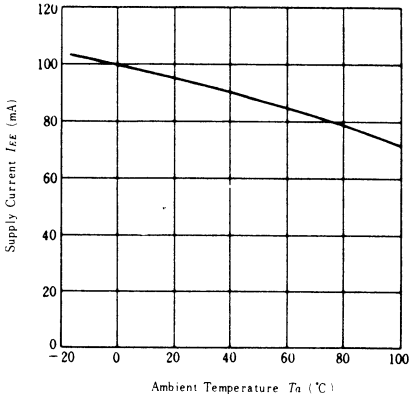
3. READ MODE



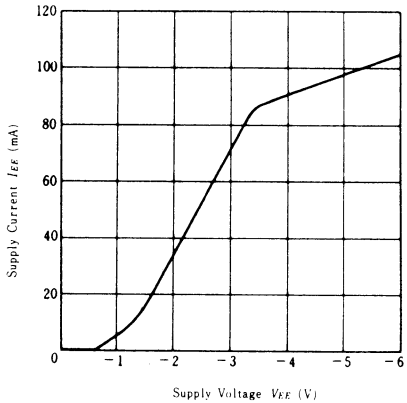
4. WRITE MODE



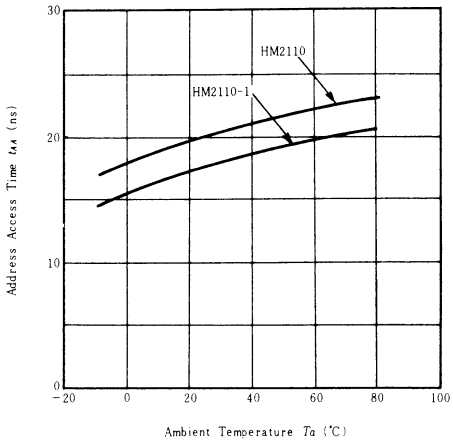
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



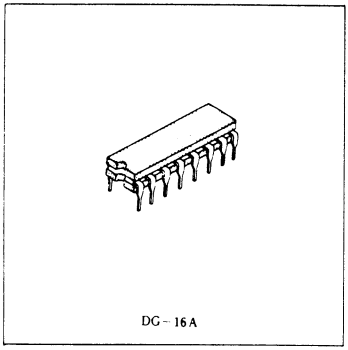
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



DG-16A

■ FEATURES

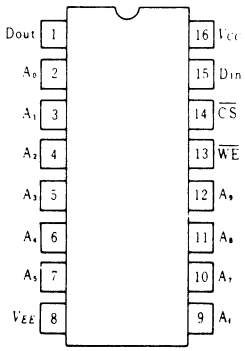
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

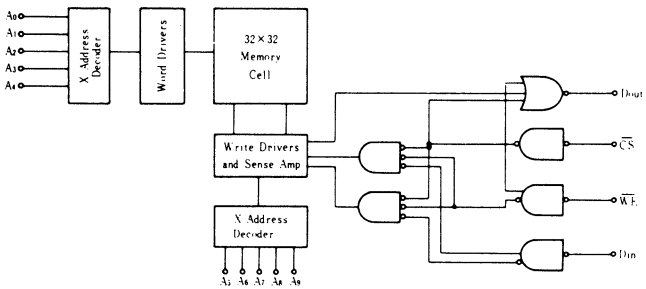
× : Irrelevant
* : Read out noniverted

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	Ta=0°C	−200	—	—	mA
			Ta=75°C	−170	—	—	

●AC CHARACTERISTICS

(V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	5	1	3	5	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=3ns	6	2	—	6	2	—	ns
Data Setup Time	t_{WSD}		1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	5	1	3	5	ns

3. RISE/FALL TIME

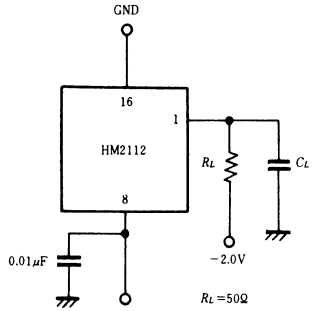
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

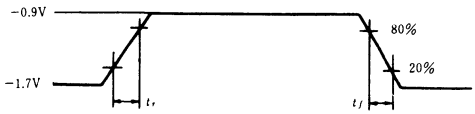
1. LOADING CONDITION



R_L=50Ω

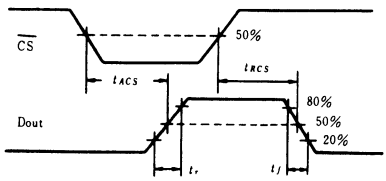
C_L=30pF(includes probe and jig capacitance)

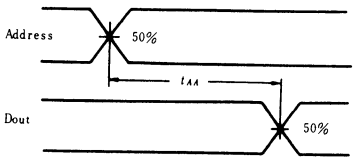
2. INPUT PULSE



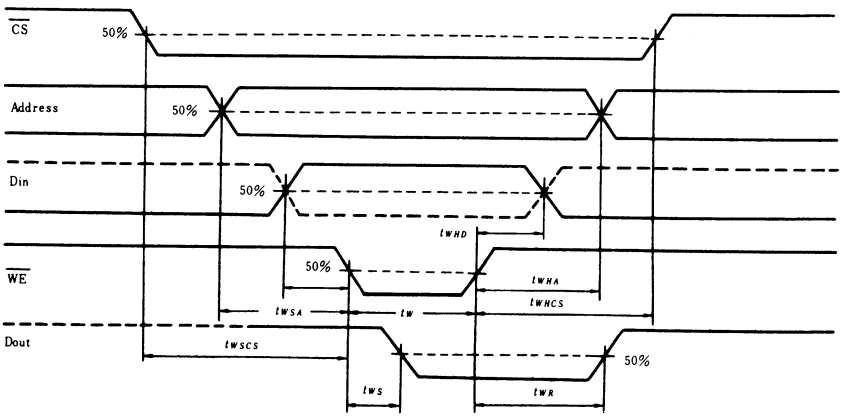
$t_r = t_f$=2.0ns typ

3. READ MODE

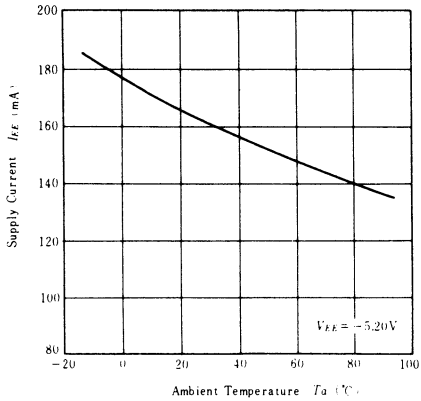




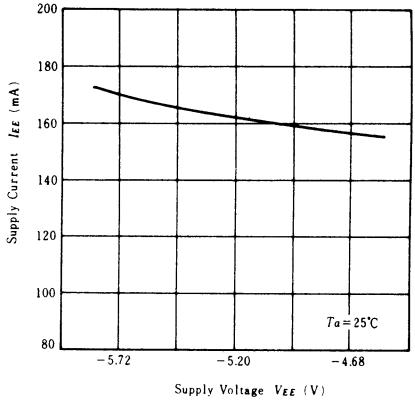
4. WRITE MODE



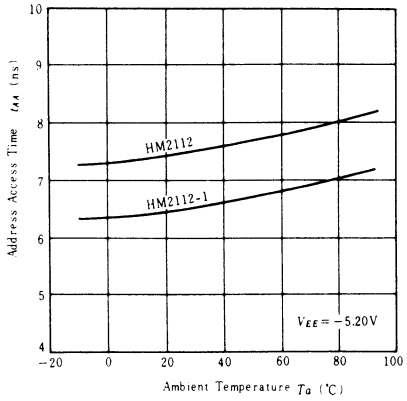
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



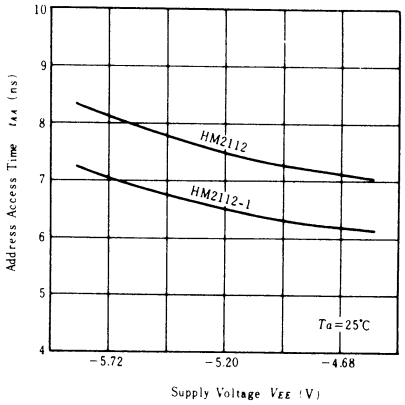
SUPPLY CURRENT vs. SUPPLY VOLTAGE



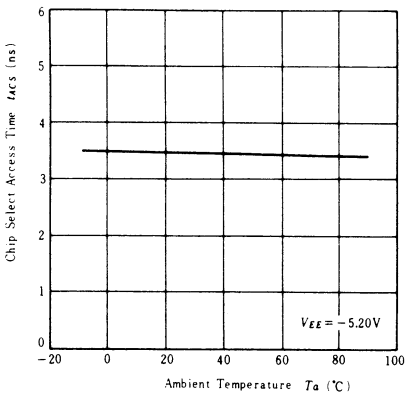
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



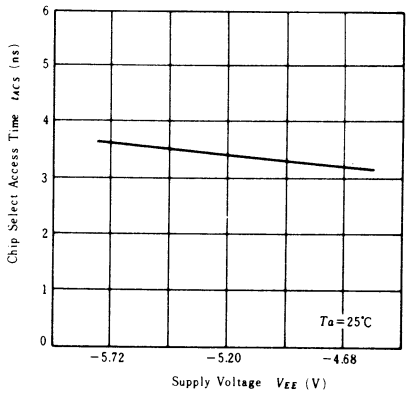
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



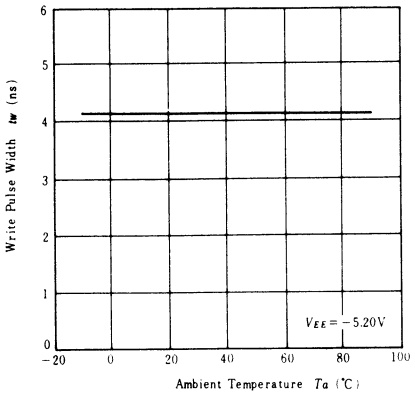
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



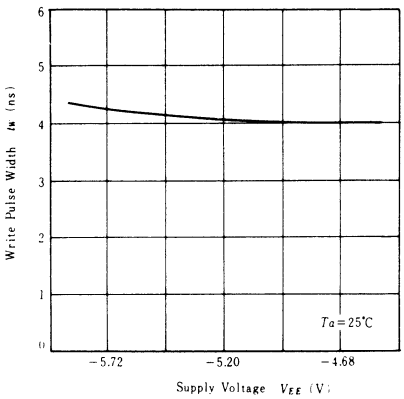
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422

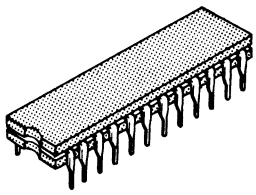
256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

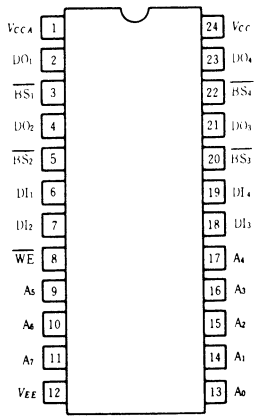


(DG-24A)

■ FEATURES

- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



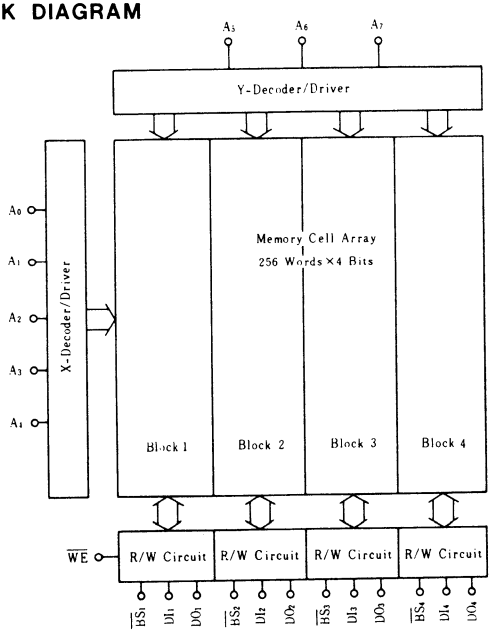
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$, $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other, $V_{IN}=V_{ILB}$	0 to +75°C	−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta=0°C	−200	−160	—	mA
			Ta=75°C	—	−145	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

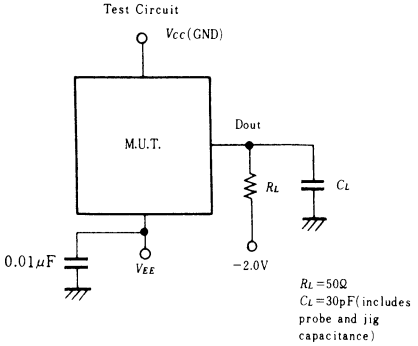
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

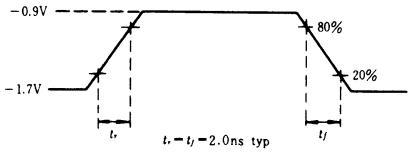
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

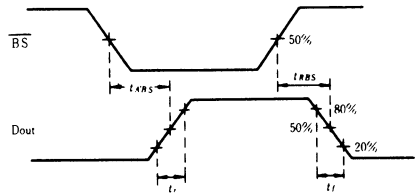
1. LOADING CONDITION

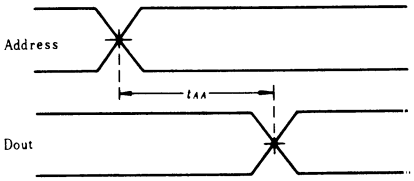


2. INPUT PULSE

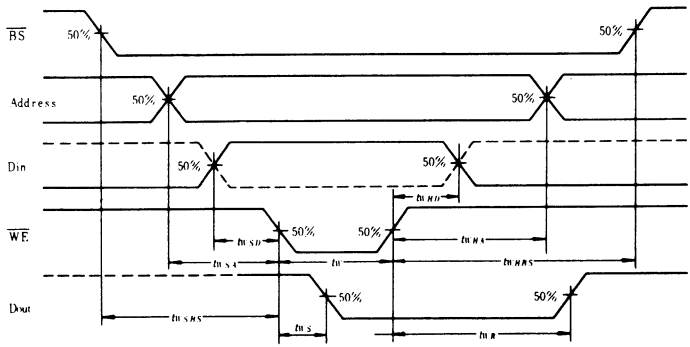


3. READ MODE

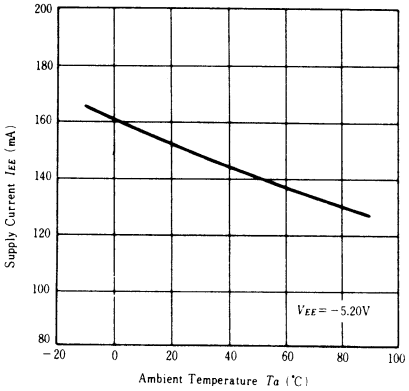




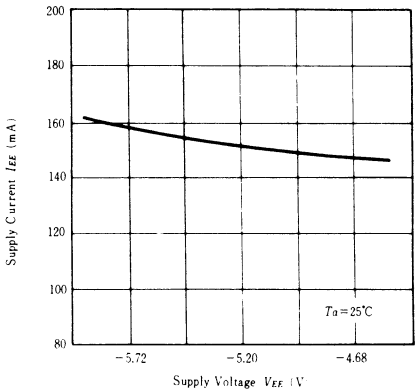
4. WRITE MODE



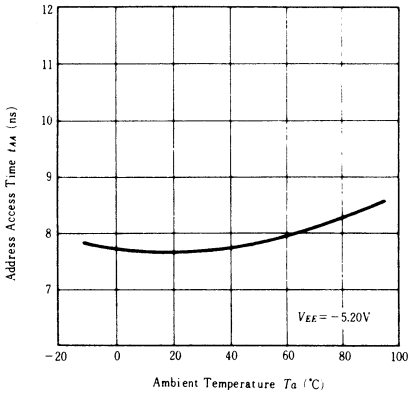
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



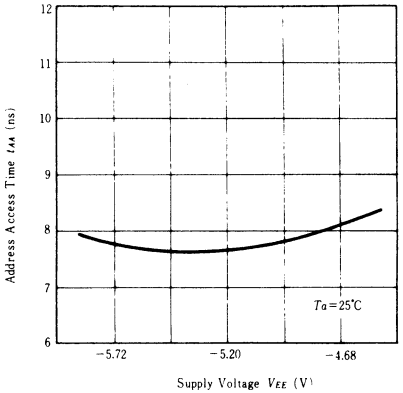
SUPPLY CURRENT vs. SUPPLY VOLTAGE



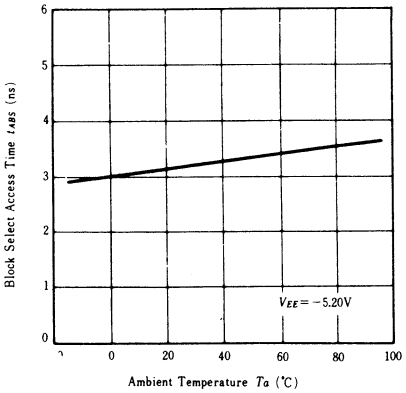
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



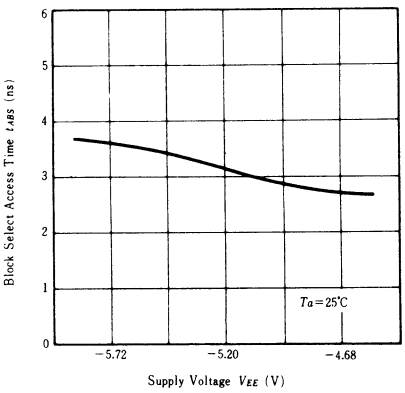
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



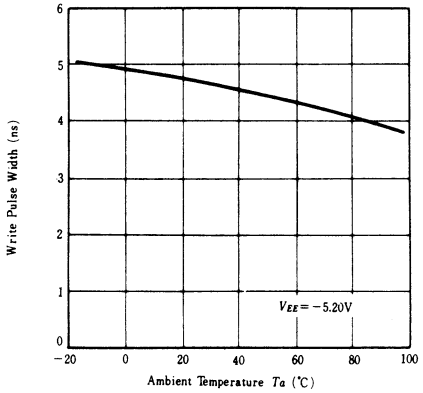
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



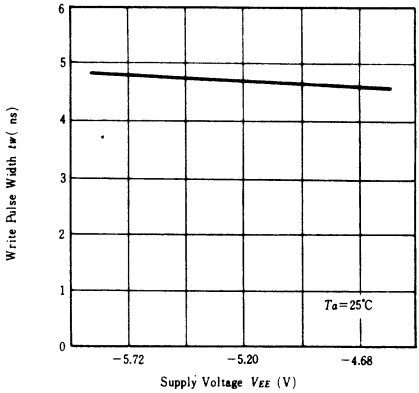
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422-7

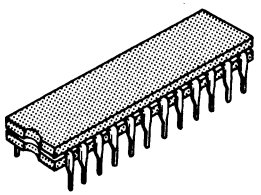
256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



(DG-24A)

■ FEATURES

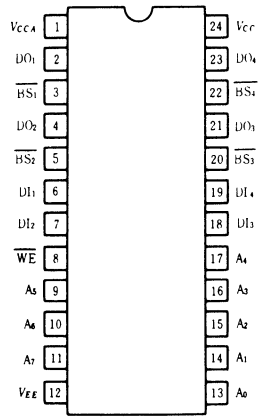
- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

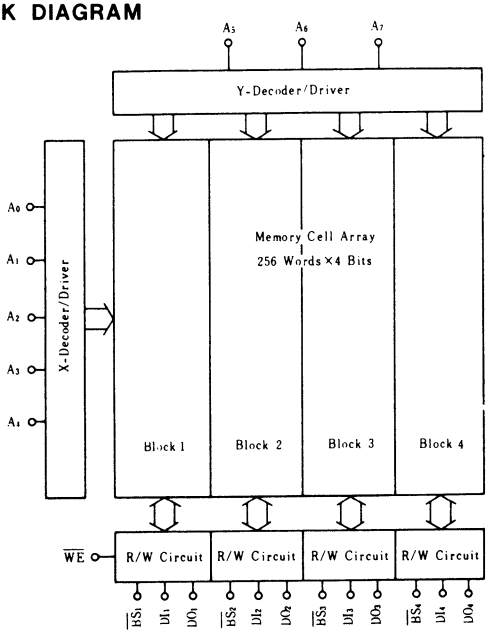
Notes) × : Irrelevant
* : Read out noninvert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



HITACHI

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−200	—	mA
			Ta = 75°C	—	−180	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	4	7	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	4	3	—	ns
Data Setup Time	t_{WSD}		1		—	ns
Data Hold Time	t_{WHD}		1		—	ns
Address Setup Time	t_{WSA}	t_W = 4ns	2		—	ns
Address Hold Time	t_{WHA}		1		—	ns
Block Select Setup Time	t_{WSBS}		1		—	ns
Block Select Hold Time	t_{WHBS}		1		—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

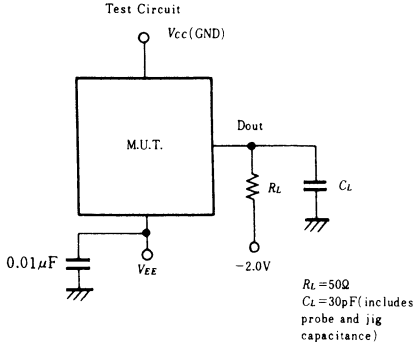
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

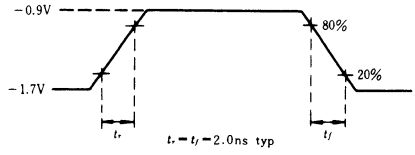
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

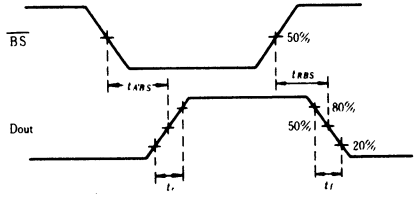
1. LOADING CONDITION

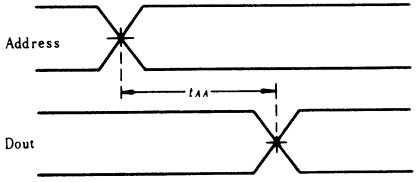


2. INPUT PULSE

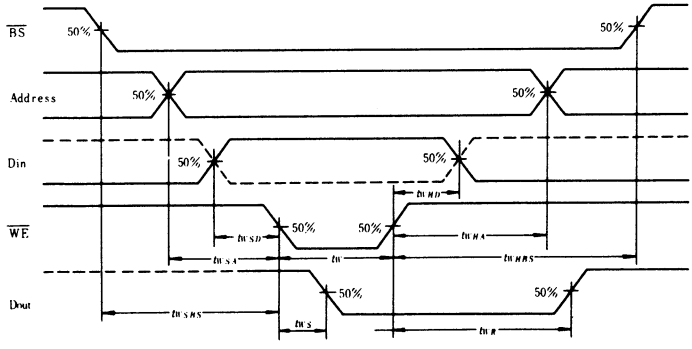


3. READ MODE





4. WRITE MODE



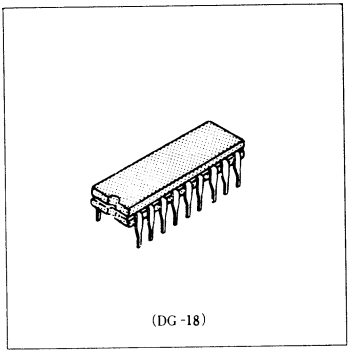
HM10470, HM10470-1

4096-word x 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

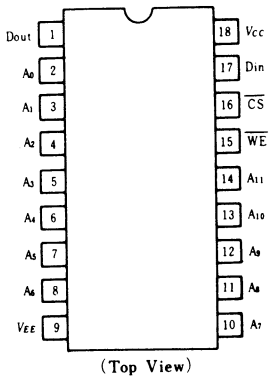
The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.



■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10470 25ns (max)
  HM10470-1 15ns (max)
- Write pulse width: HM10470 25ns (min)
  HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



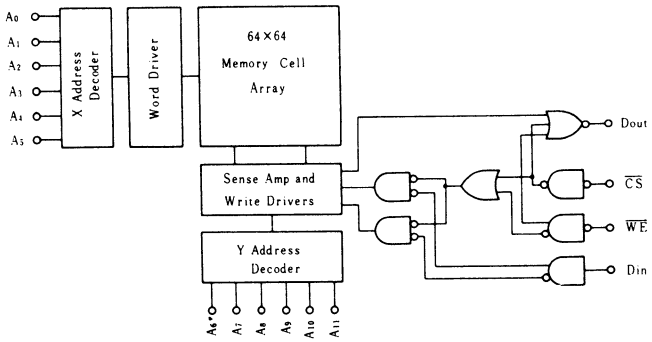
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	Ta = 0°C	−200*	−160*	—	mA
				−280**	−200**	—	
			Ta = 75°C	—	−145	—	

* HM10470
** HM10470-1

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	—	—	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	8	ns

3. RISE/FALL TIME

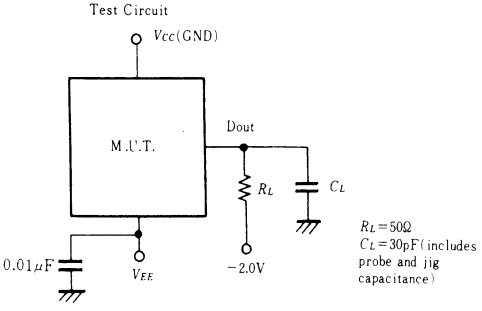
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

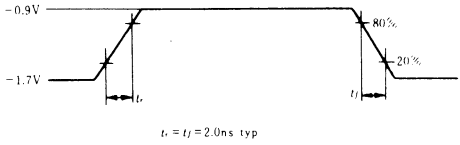
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

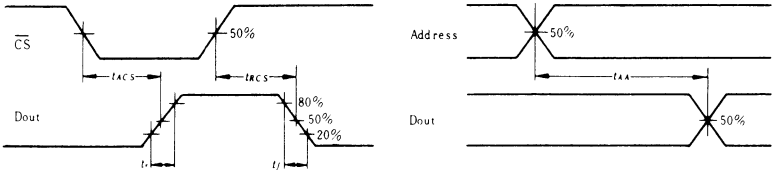
1. LOADING CONDITION



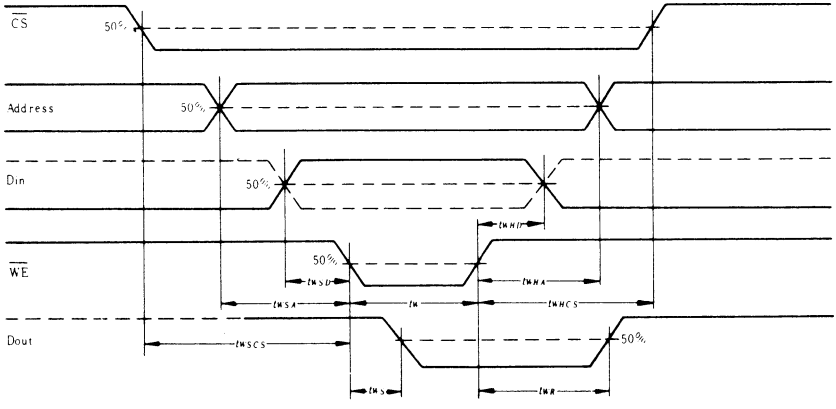
2. INPUT PULSE



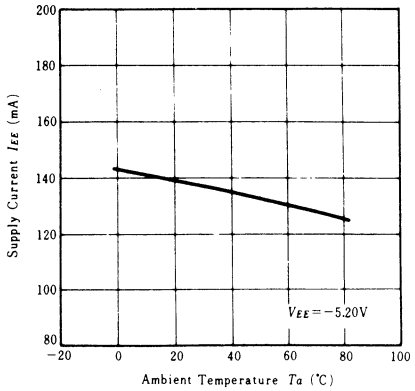
3. READ MODE



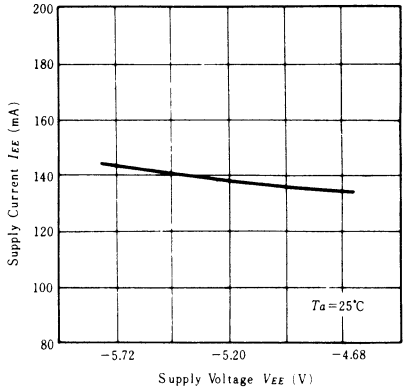
4. WRITE MODE



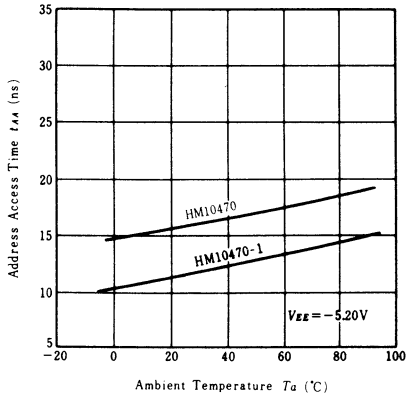
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



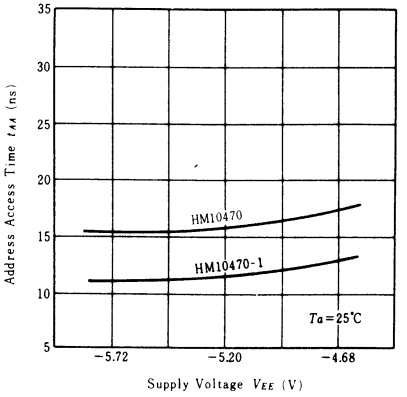
SUPPLY CURRENT vs. SUPPLY VOLTAGE



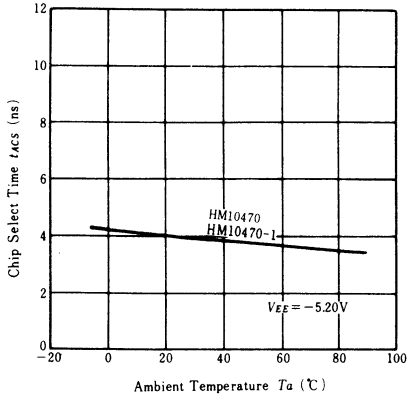
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



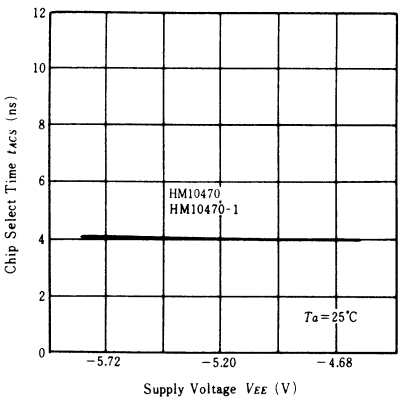
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



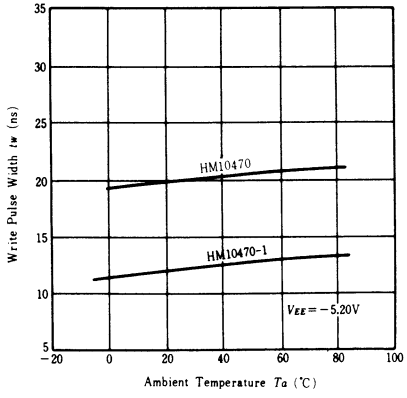
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



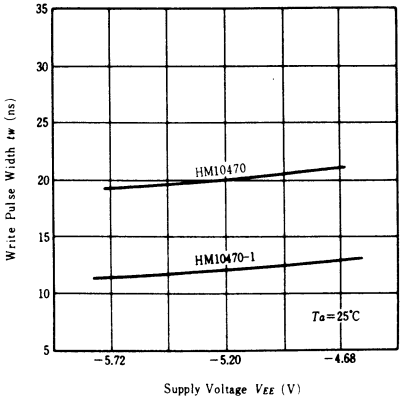
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



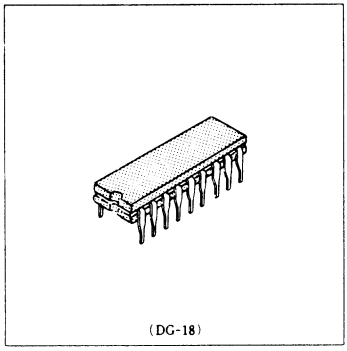
HM10470-20

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.



(DG-18)

■ FEATURES

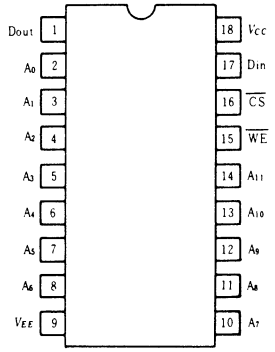
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 20ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: 0.25 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

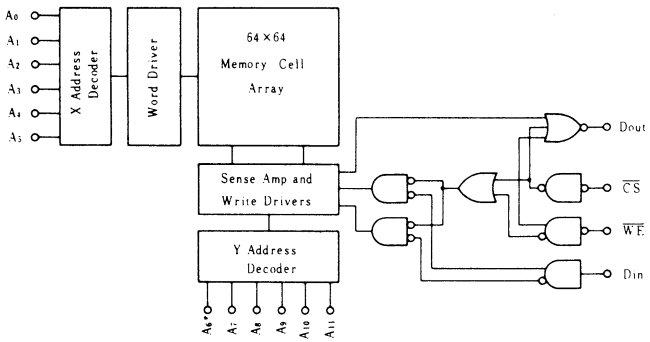
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−260	−220	—	mA
			Ta = 75°C	—	−210	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	ns
Address Access Time	t_{AA}		—	—	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = 20ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	ns
Write Recovery Time	t_{WR}		—	—	22	ns

3. RISE/FALL TIME

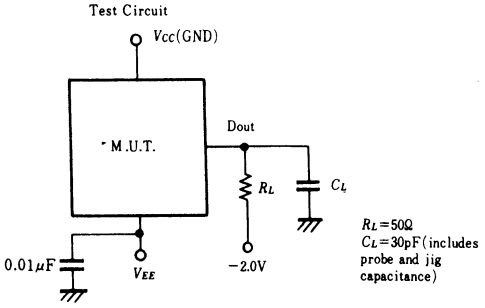
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

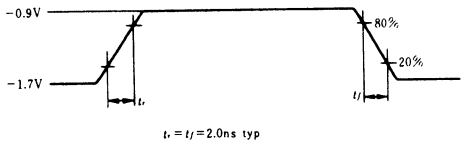
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

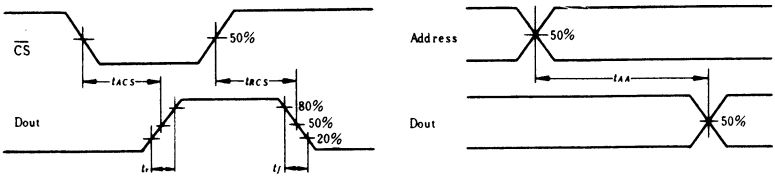
1. LOADING CONDITION



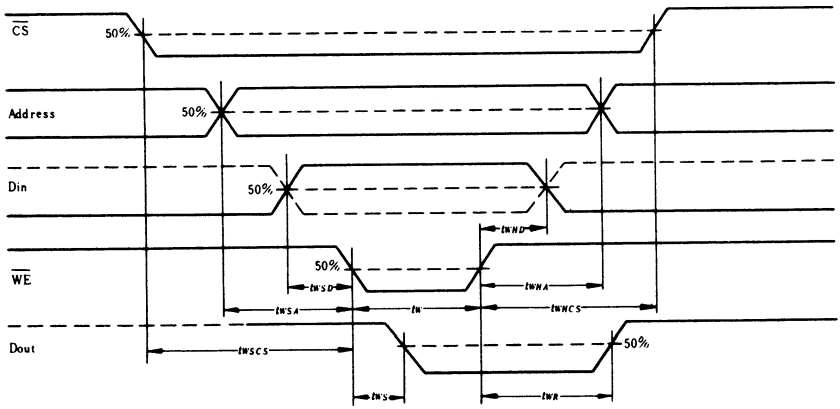
2. INPUT PULSE



3. READ MODE



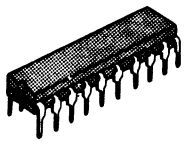
4. WRITE MODE



HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM2142 is encapsulated in cerdip-20 pin package.



(DG-20)

■ FEATURES

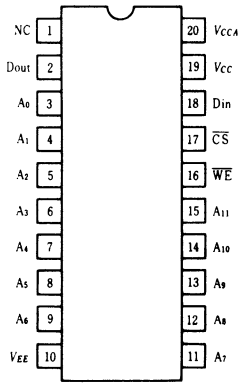
- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

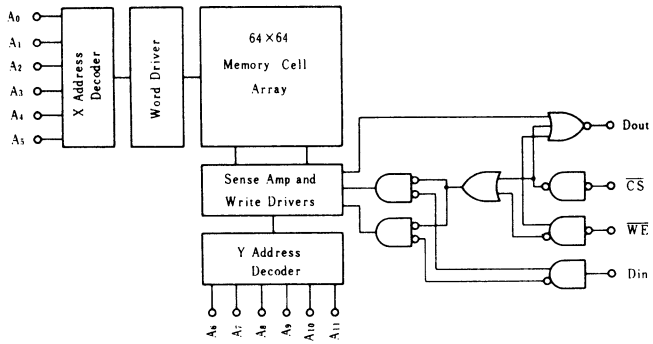
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75℃, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IH}=V_{IHA} or V_{ILB}	0℃	−1000	—	−840	mV
			+25℃	−980	—	−810	
			+75℃	−950	—	−720	
	V_{OL}		0℃	−1870	—	−1665	
			+25℃	−1850	—	−1650	
			+75℃	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IH}=V_{IHB} or V_{ILA}	0℃	−1020	—	—	mV
			+25℃	−980	—	—	
			+75℃	−920	—	—	
	V_{OLC}		0℃	—	—	−1645	
			+25℃	—	—	−1630	
			+75℃	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0℃	−1165	—	−880	mV
			+25℃	−1165	—	−880	
			+75℃	−1165	—	−880	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0℃	−1810	—	−1560	
			+25℃	−1810	—	−1560	
			+75℃	−1810	—	−1560	
Input Current	I_{IH}	V_{IN}=V_{IHA}	0 to +75℃	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75℃	0.5	—	170	
		Others (V_{IN}=V_{ILB})		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open.	Ta=0℃	−270	−240	—	mA
			Ta=75℃	—	−220	—	

● AC CHARACTERISTICS (V_{EE}=−5.2V±5%, Ta=0 to +75℃, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	ns
Address Access Time	t_{AA}		—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=3ns	10	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	ns
Address Setup Time	t_{WSA}	t_W=10ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	ns
Write Disable Time	t_{WS}		—	—	6	ns
Write Recovery Time	t_{WN}		—	—	6	ns

3. RISE/FALL TIME

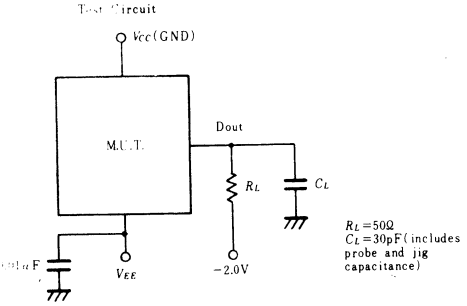
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

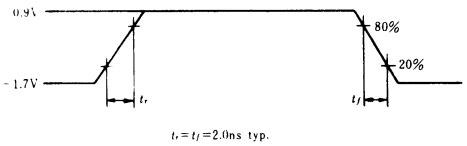
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}^*		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

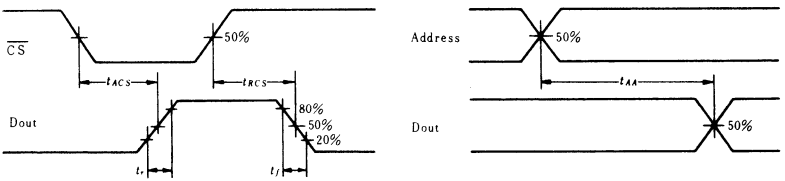
1. LOADING CONDITION



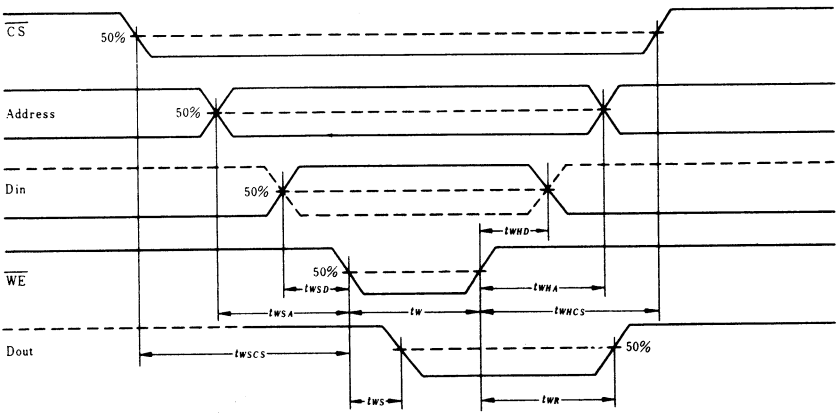
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



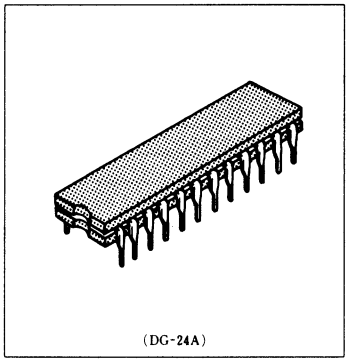
HM10474, HM10474-15

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

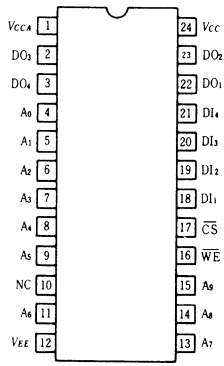


(DG-24A)

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474 25ns (max)
  HM10474-15 15ns (max)
- Write pulse width: HM10474 25ns(min)
  HM10474-15 20ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



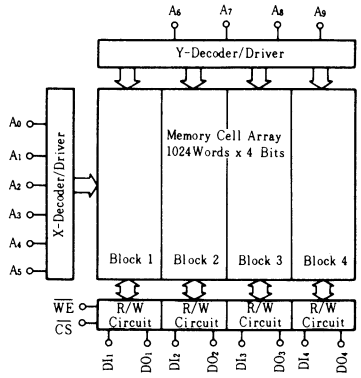
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474			HM10474-15			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	—	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474			HM10474-15			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	20	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	27	—	—	17	ns

3. RISE/FALL TIME

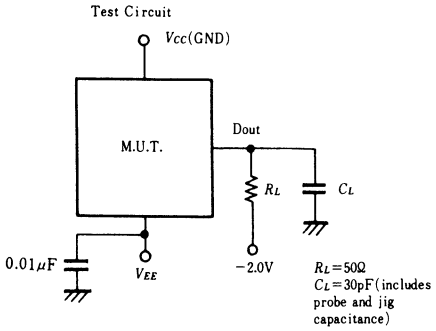
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

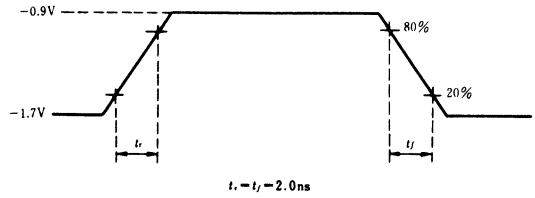
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

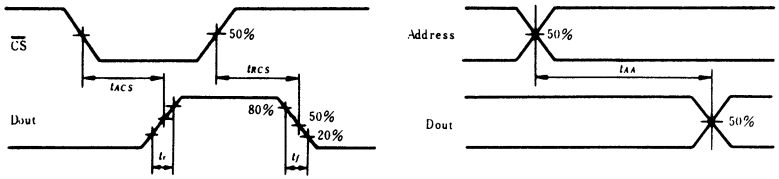
1. LOADING CONDITION



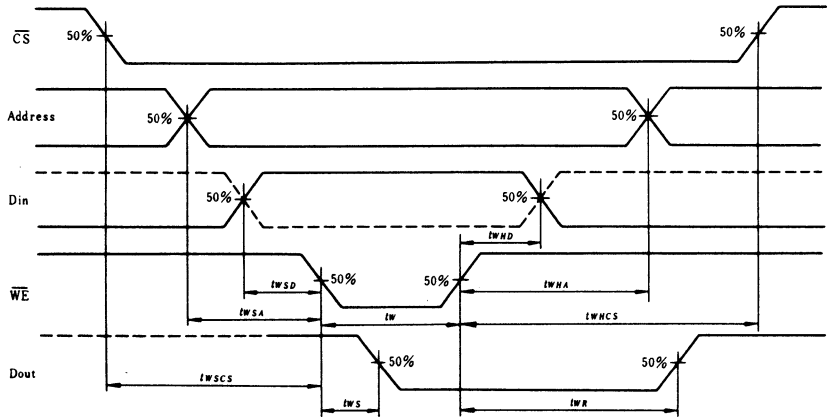
2. INPUT PULSE



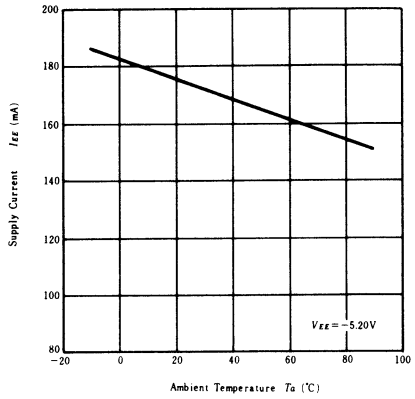
3. READ MODE



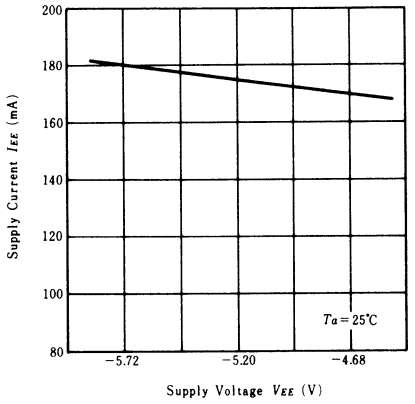
4. WRITE MODE



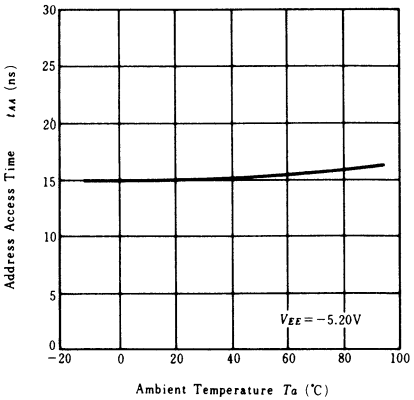
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



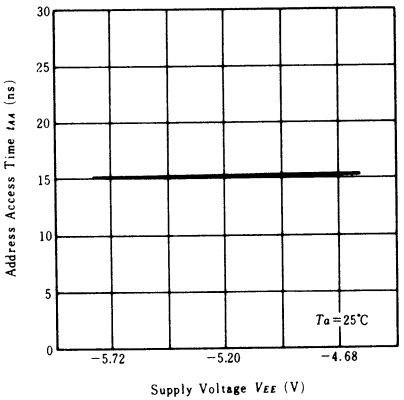
SUPPLY CURRENT vs. SUPPLY VOLTAGE



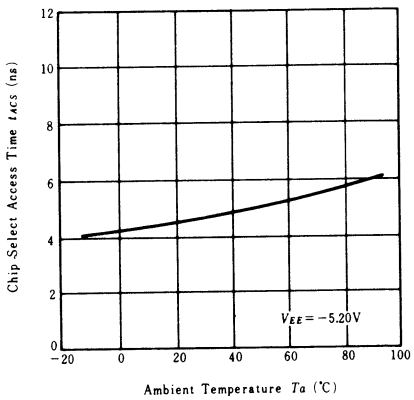
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



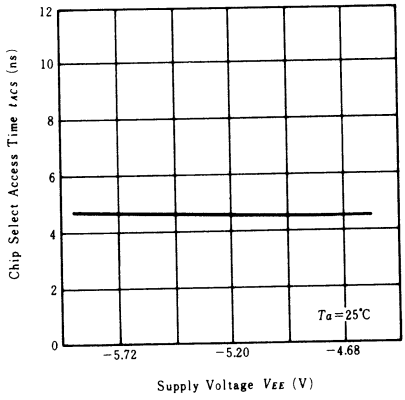
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



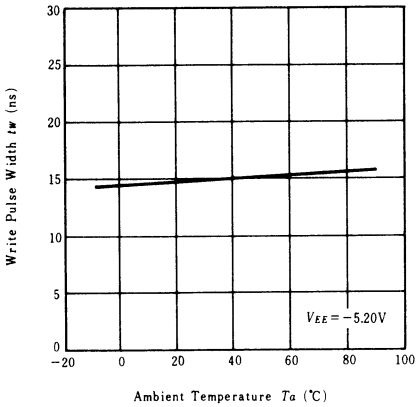
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



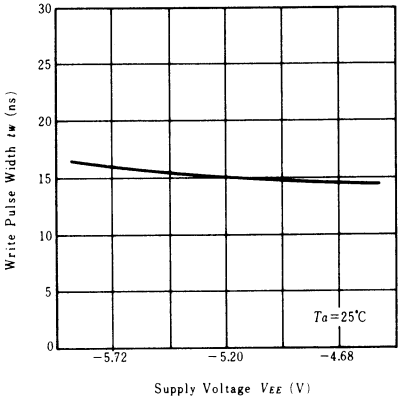
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



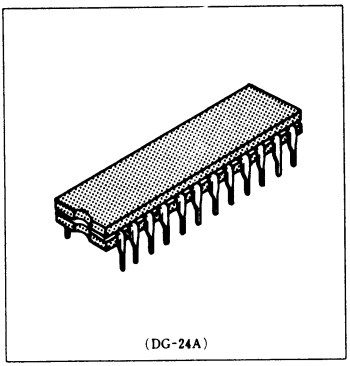
HM10474-8,HM10474-10 — Preliminary

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

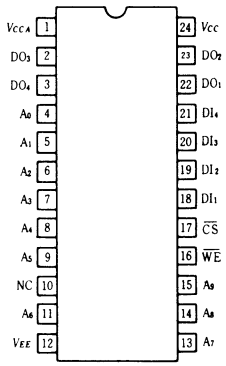


(DG-24A)

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474-8 8ns (max)
  HM10474-10 10ns (max)
- Write pulse width: HM10474-8 5ns (min)
  HM10474-10 5ns (min)
- Low power dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



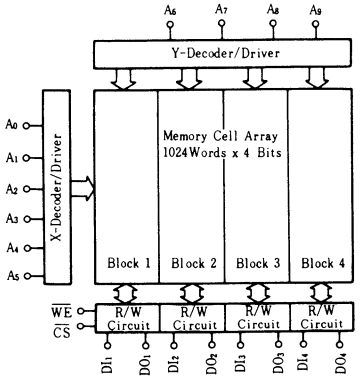
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−220	—	mA
			Ta = 75°C	—	−205	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	5	—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	5	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	5	—	—	5	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	5	—	—	5	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

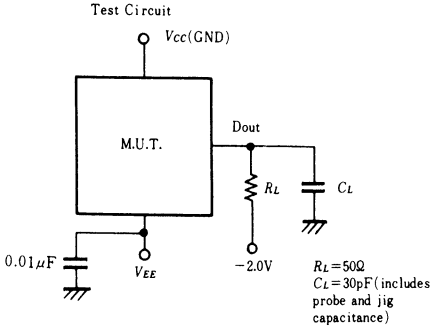
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

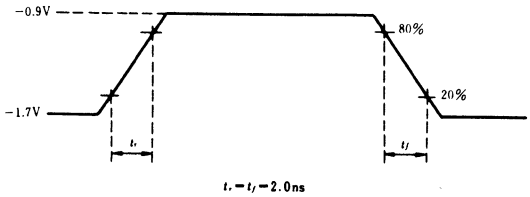
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

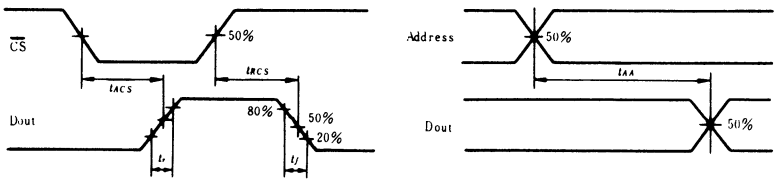
1. LOADING CONDITION



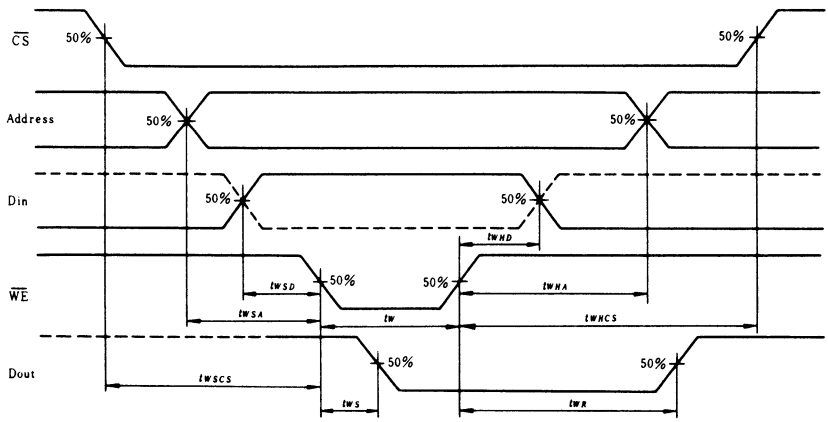
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

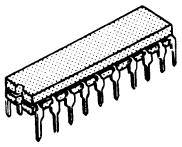


HM10480,HM10480F

16,384-words×1-bit Fully Decoded Random Access Memory

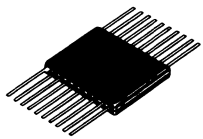
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

HM10480



(DG-20)

HM10480F



(FG-20)

■FEATURES

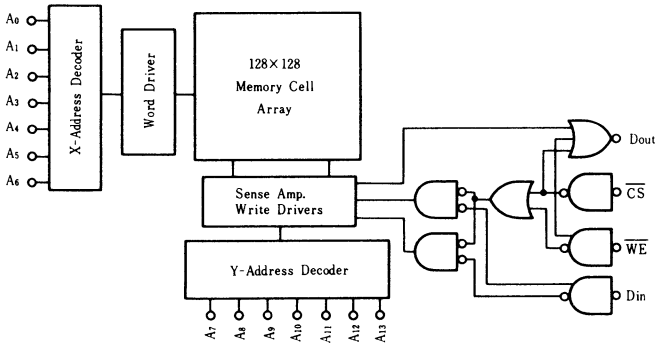
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

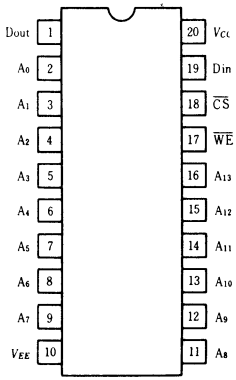
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−170	−140	—	mA
			Ta = 75°C	—	−130	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	10	ns
Address Access Time	t_{AA}		3	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

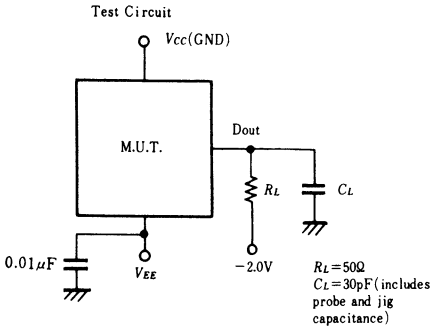
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

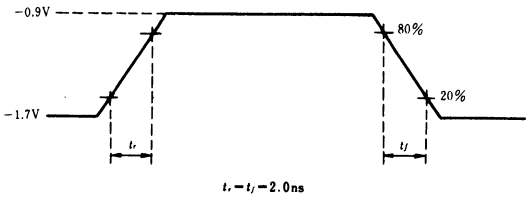
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

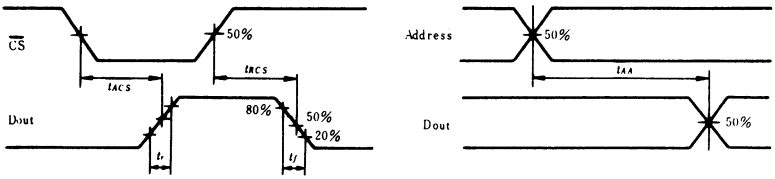
1. LOADING CONDITION



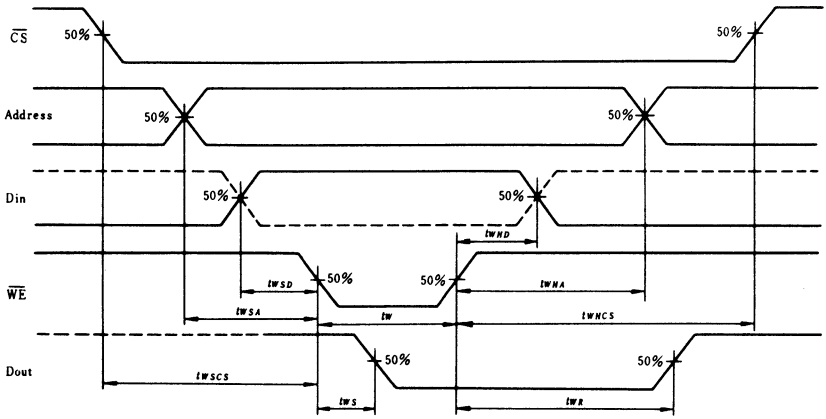
2. INPUT PULSE



3. READ MODE



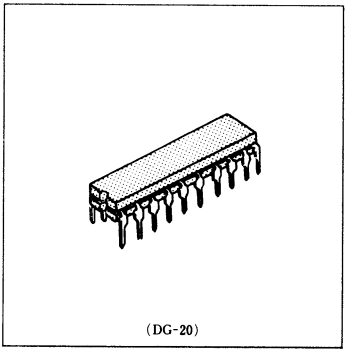
4. WRITE MODE



HM10480-15,HM10480-20—Preliminary

16,384-words × 1-bit Fully Decoded Random Access Memory

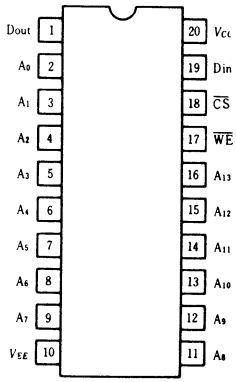
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin package, compatible with Fairchild's F10480.


(DG-20)

■FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10480-15 15ns (max)
  HM10480-20 20ns (max)
- Write pulse width: HM10480-15 15ns (min)
  HM10480-20 20ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



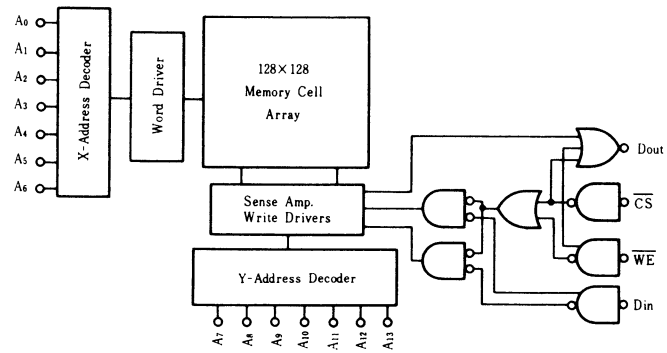
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	$Ta=0°C$	−240	−220	—	mA
			$Ta=75°C$	—	−200	—	

●AC CHARACTERISTICS ($V_{EE}=-5.2V\ \pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10480-15			HM10480-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	—	8	2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	2	—	10	ns
Address Access Time	t_{AA}		3	12	15	3	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10480-15			HM10480-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=2ns$	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=t_W$ min	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

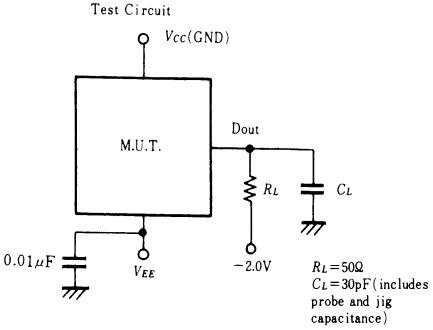
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

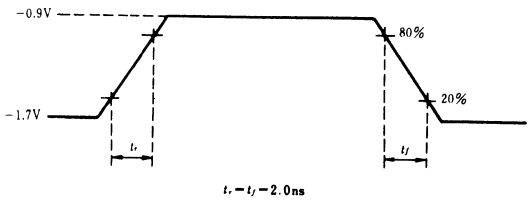
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

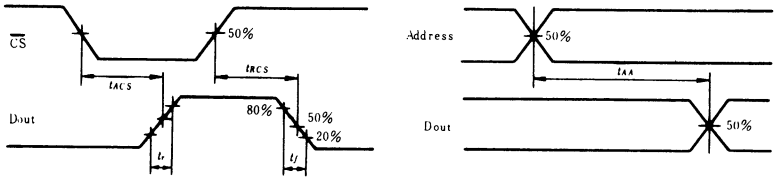
1. LOADING CONDITION



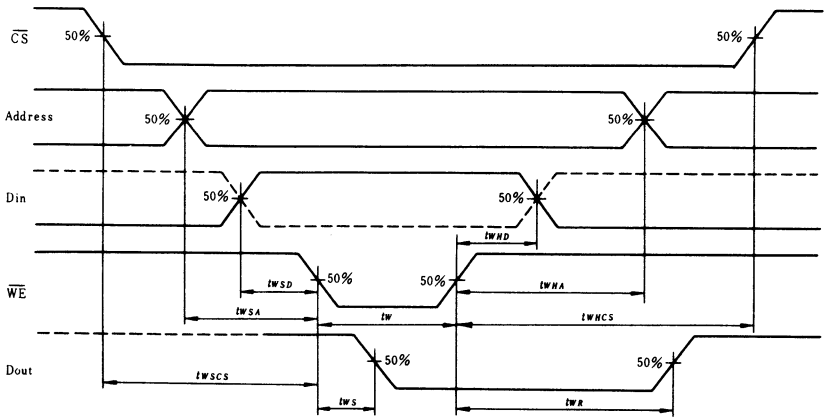
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

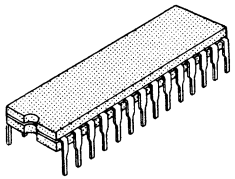


HM10484-15,HM10484-20

4096-word x 4-bit Fully Decoded Random Access Memory

Under Development

The HM10484 is ECL 10K compatible, 4096 words x 4-bit read write, random access memory developed for high speed systems such as scratch pads and control/buffer storage. The fabrication process is the Hitachi's low capacitance U-groove isolation method with double metalization. The HM10484 is encapsulated in cerdip-28 pin package.



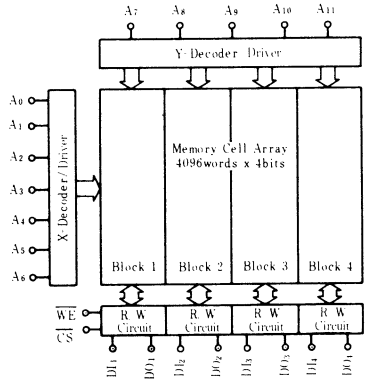
(DG-28A)

■ TRUTH TABLE

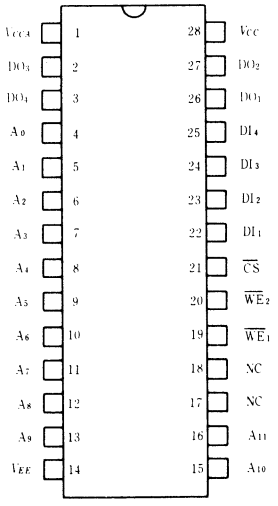
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−240	—	—	mA
			Ta = 75°C	—	—	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	—	8	2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	2	—	10	ns
Address Access Time	t_{AA}		3	12	15	3	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

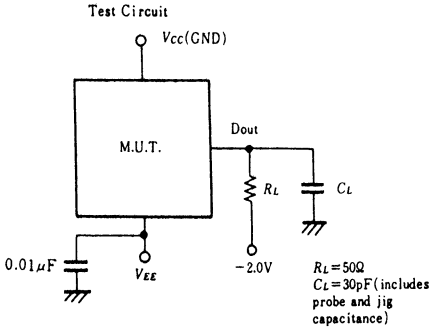
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

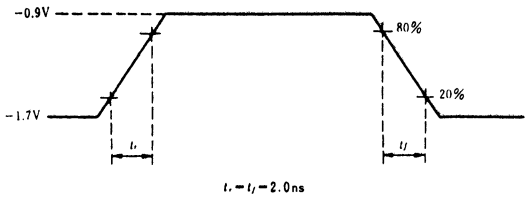
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

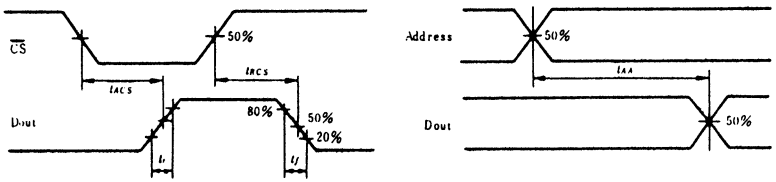
1. LOADING CONDITION



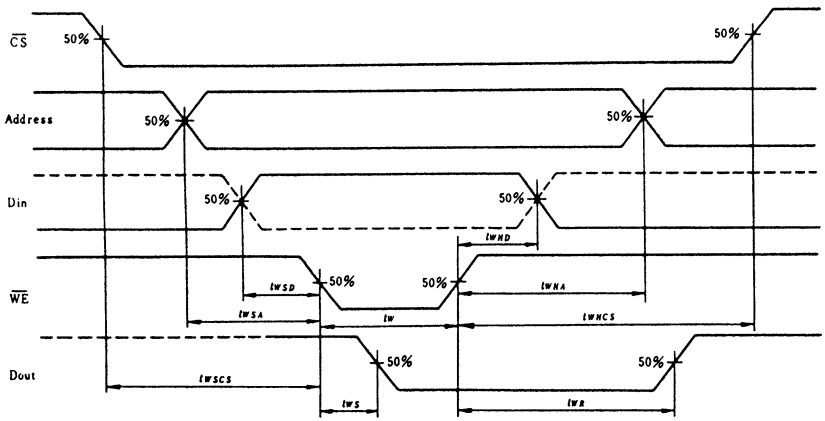
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



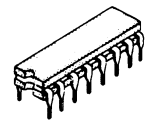
HM100415,HM100415CC

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

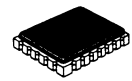
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

HM100415



(DG-16A)

HM100415CC



(CC-24)

■FEATURES

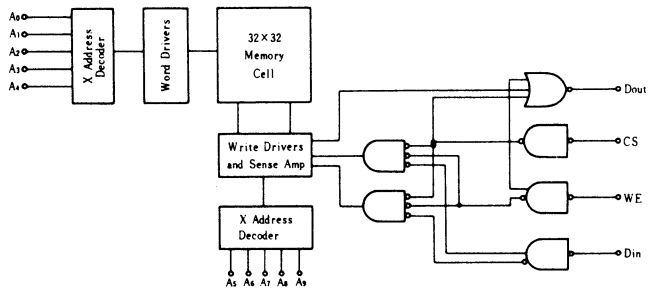
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

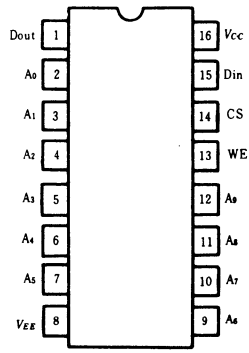
Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



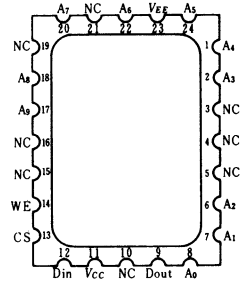
■PIN ARRANGEMENT

●HM100415



(Top View)

●HM100415CC



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

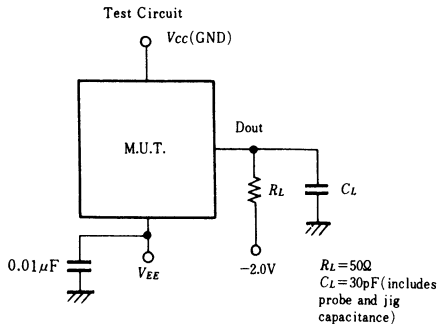
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

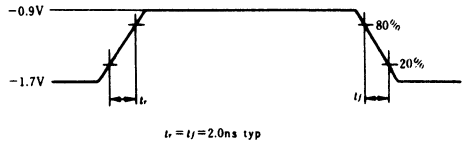
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

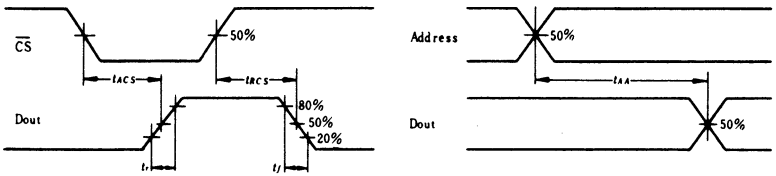
1. LOADING CONDITION



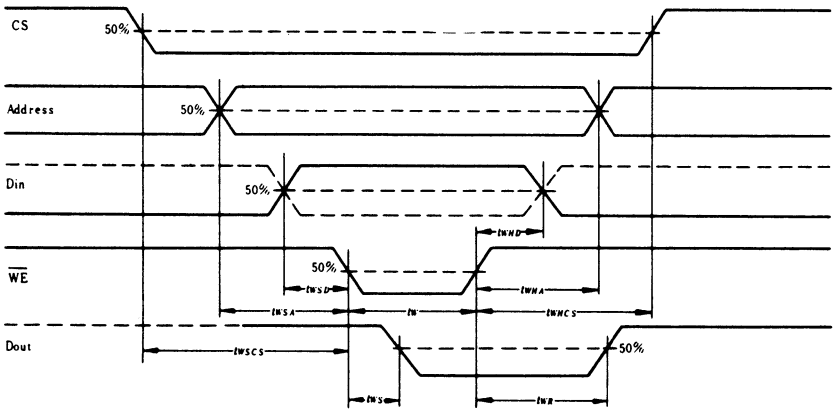
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100422,HM100422F
HM100422CC

256-word×4-bit Fully Decoded Random Access Memory

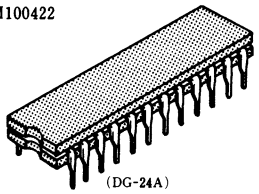
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

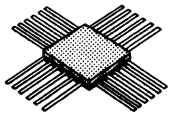
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



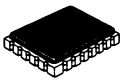
(DG-24A)

HM100422F



(FG-24)

HM100422CC



(CC-24)

■ FEATURES

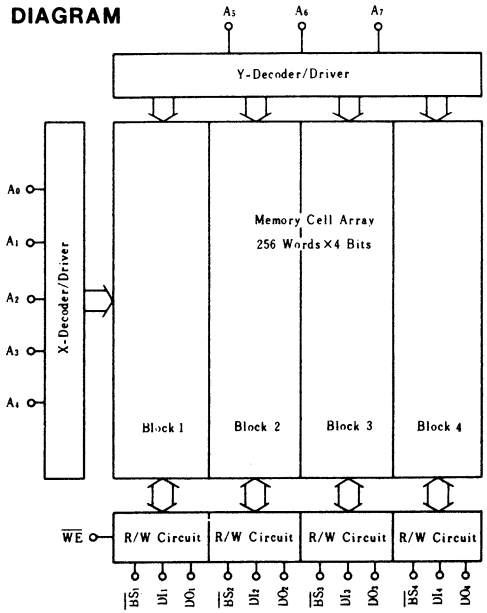
- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

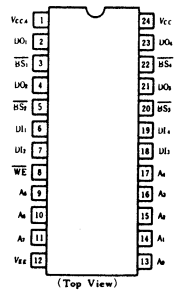
Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



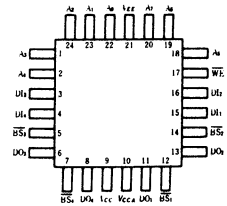
■ PIN ARRANGEMENT

● HM100422



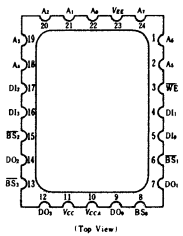
(Top View)

● HM100422F



(Top View)

● HM100422CC



(Top View)

HITACHI

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

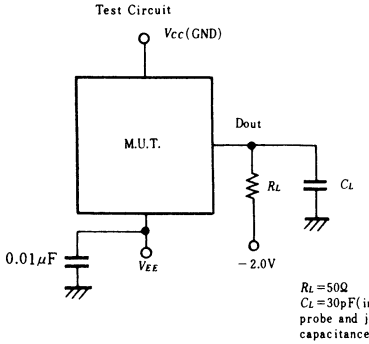
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

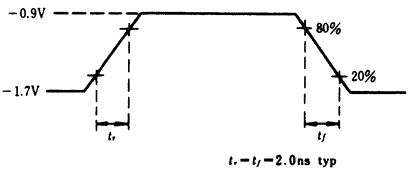
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

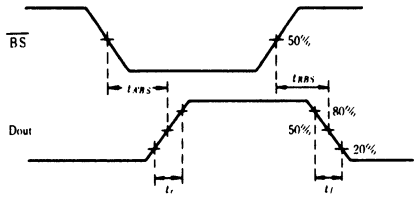
1. LOADING CONDITION

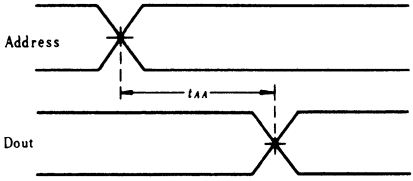


2. INPUT PULSE

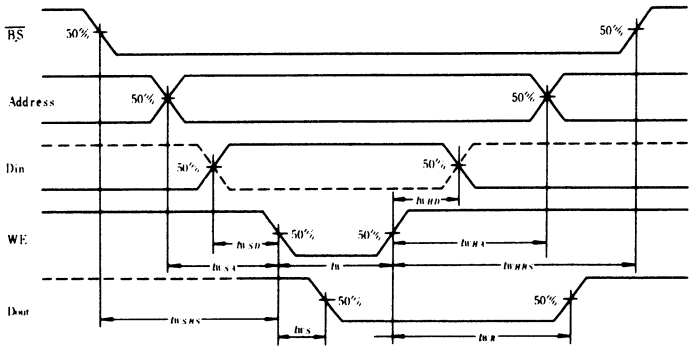


3. READ MODE





4. WRITE MODE



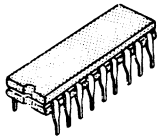
HM100470

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.



(DG-18)

■ FEATURES

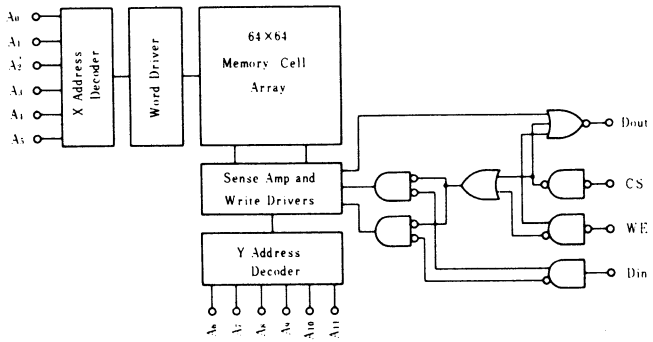
- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns (min)
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

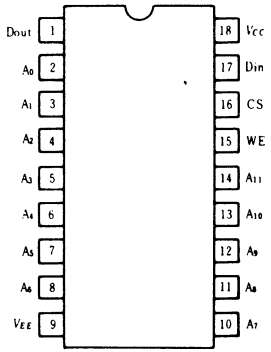
Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WAS} = 3ns	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

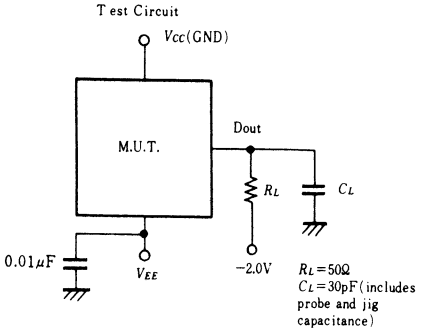
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

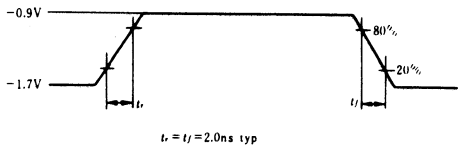
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

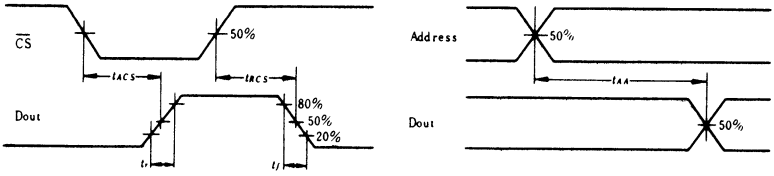
1. LOADING CONDITION



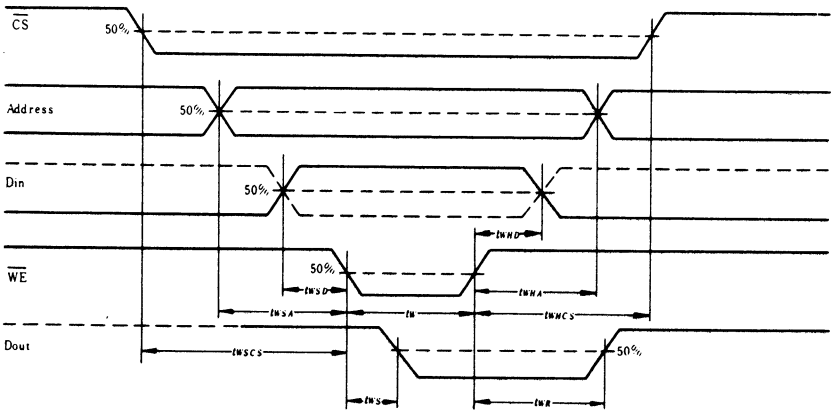
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100474,HM100474-15
HM100474F,HM100474F-15

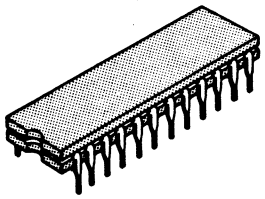
1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

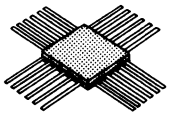
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474, HM100474-15



(DG-24A)

HM100474F, HM100474F-15



(FG-24)

■FEATURES

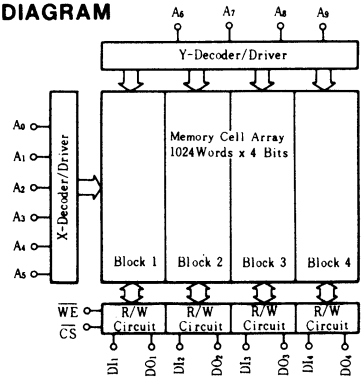
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
  HM100474/F-15 15ns(max)
- Write pulse width: HM100474/F 25ns(min)
  HM100474/F-15 20ns(min)
- Output obtainble by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



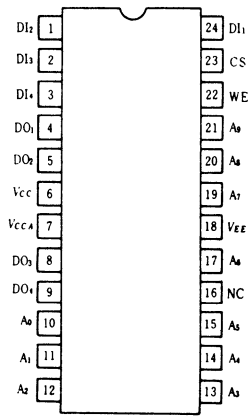
■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

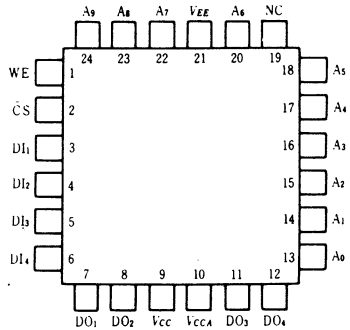
■PIN ARRANGEMENT

●HM100474,HM100474-15



(Top View)

●HM100474F, HM100474F-15



(Top View)

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	8	—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	—	—	10	ns
Address Access Time	t_{AA}		—	—	15	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	20	—	—	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = twmin	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	27	ns

3. RISE/FALL TIME

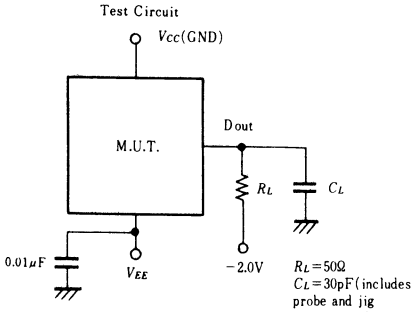
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

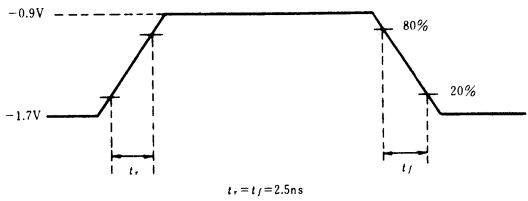
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

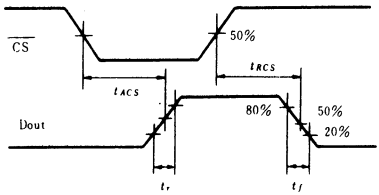
1. LOADING CONDITION

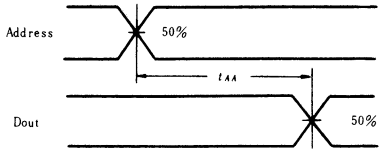


2. INPUT PULSE

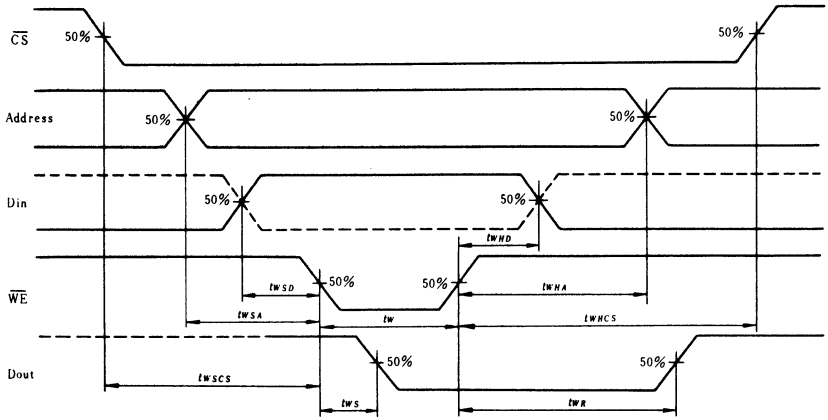


3. READ MODE

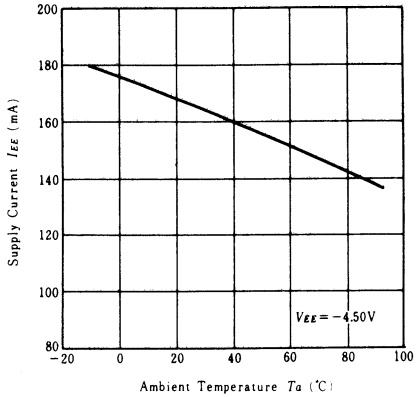




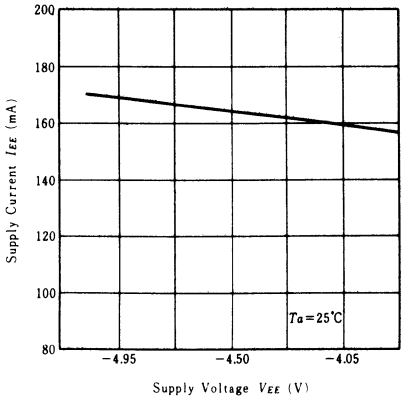
4. WRITE MODE



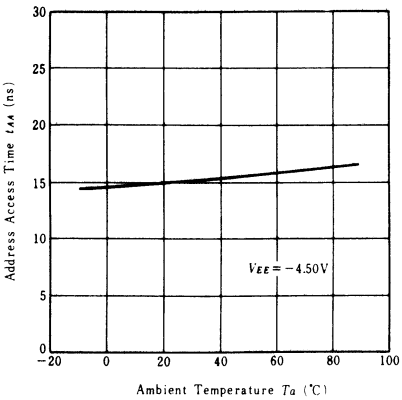
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



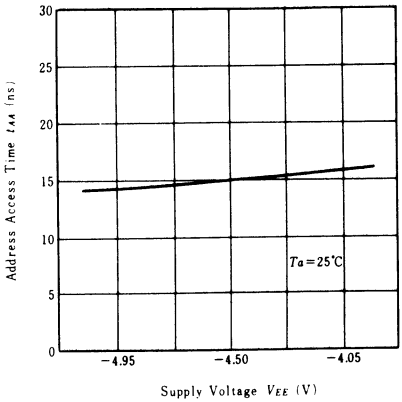
SUPPLY CURRENT vs. SUPPLY VOLTAGE



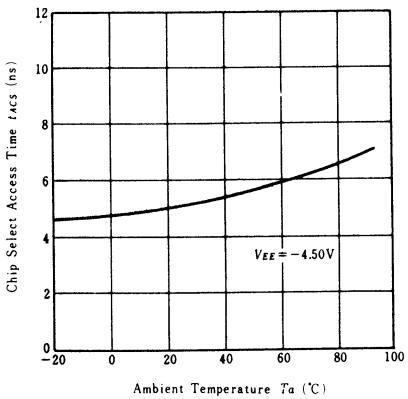
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



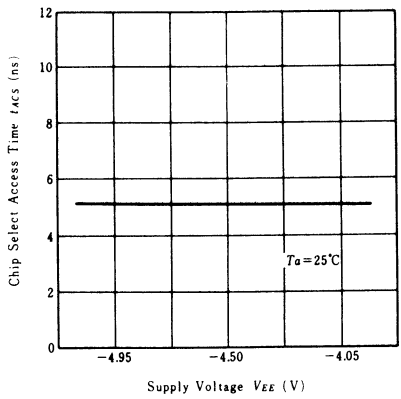
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



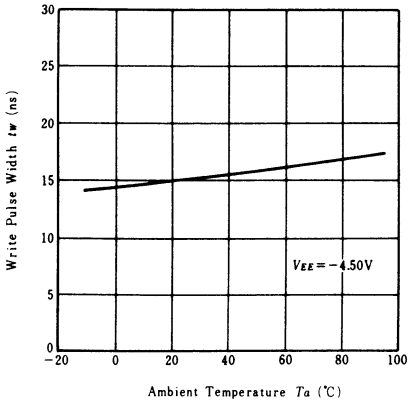
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



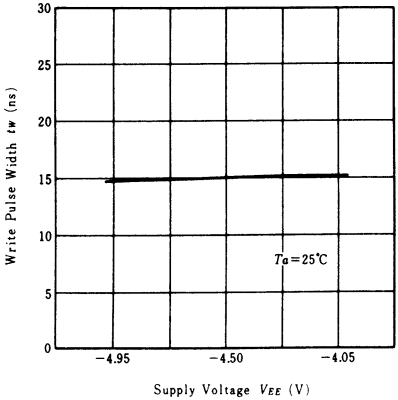
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−240	—	—	mA
			Ta = 75°C	—	—	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	—	8	2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	2	—	10	ns
Address Access Time	t_{AA}		3	12	15	3	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

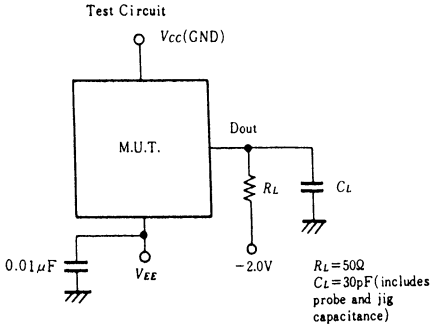
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

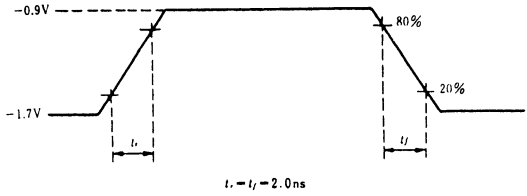
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

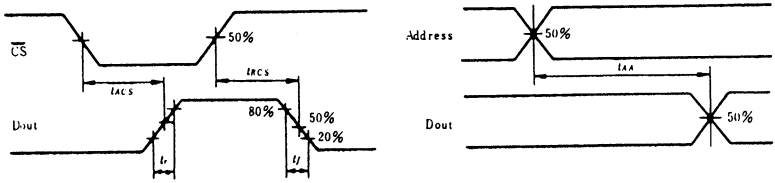
1. LOADING CONDITION



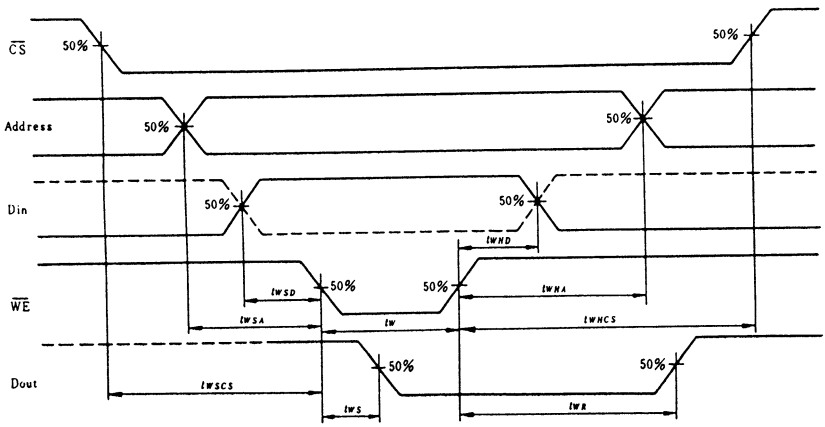
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



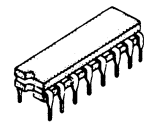
HM100415,HM100415CC

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

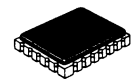
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

HM100415



(DG-16A)

HM100415CC



(CC-24)

■ FEATURES

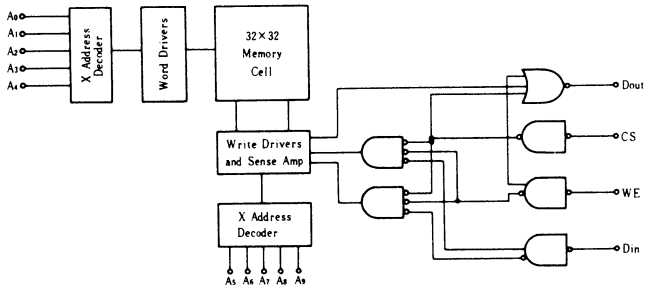
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

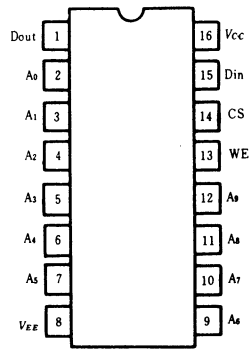
Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



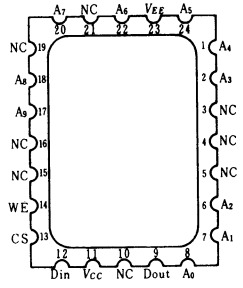
■ PIN ARRANGEMENT

●HM100415



(Top View)

●HM100415CC



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Tempe ature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-4.5V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

●AC CHARACTERISTICS ($V_{EE}=-4.5V\ \pm5\%$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

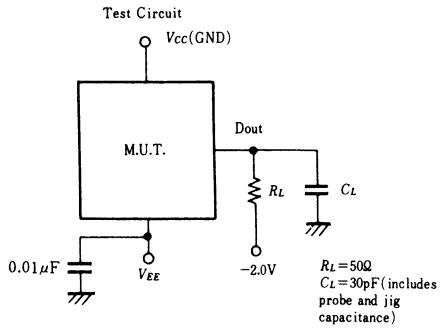
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

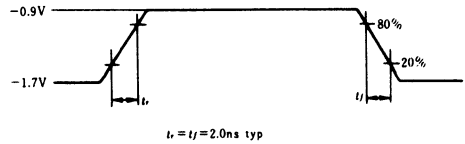
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

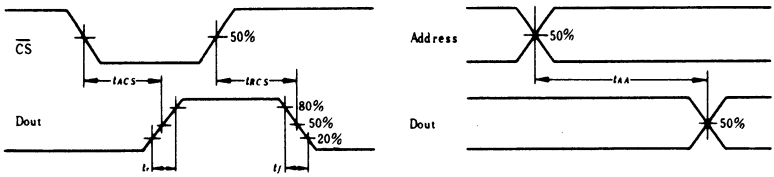


2. INPUT PULSE

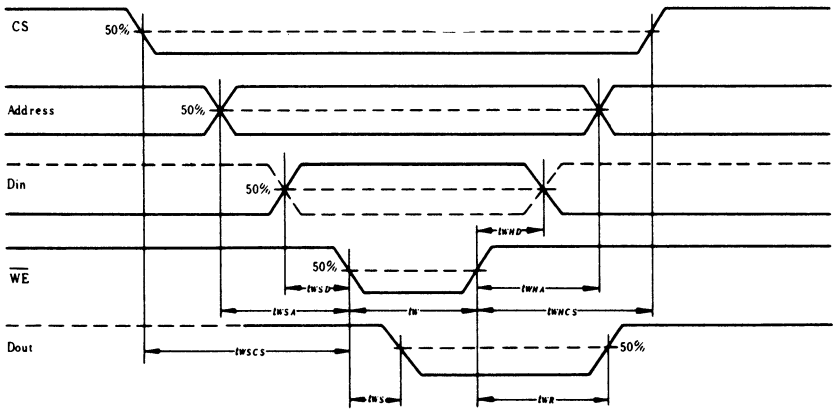


$t_r = t_f = 2.0$ns typ

3. READ MODE



4. WRITE MODE



HM100422,HM100422F
HM100422CC

256-word×4-bit Fully Decoded Random Access Memory

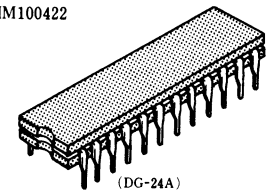
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

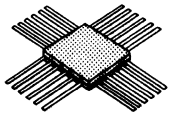
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



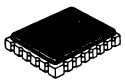
(DG-24A)

HM100422F



(FG-24)

HM100422CC



(CC-24)

■ FEATURES

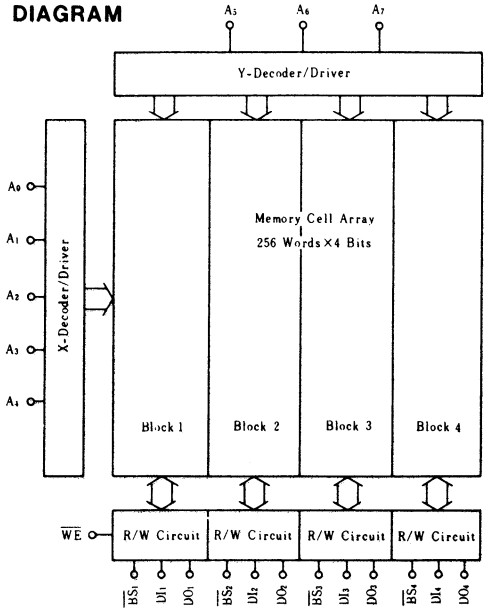
- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

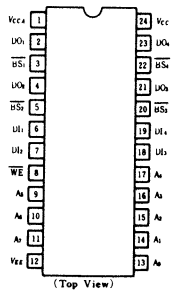
Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



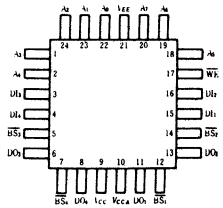
■ PIN ARRANGEMENT

●HM100422



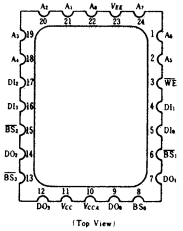
(Top View)

●HM100422F



(Top View)

●HM100422CC



(Top View)

HITACHI

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

● AC CHARACTERISTICS (V_{EE}=−4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

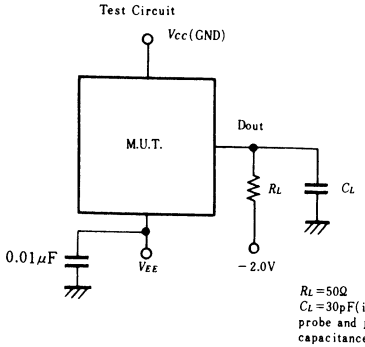
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

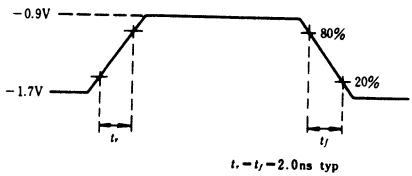
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

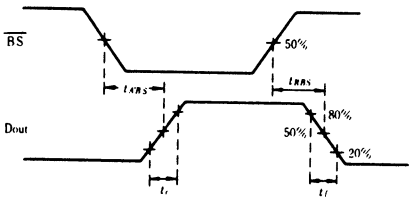
1. LOADING CONDITION

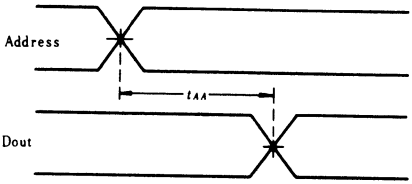


2. INPUT PULSE

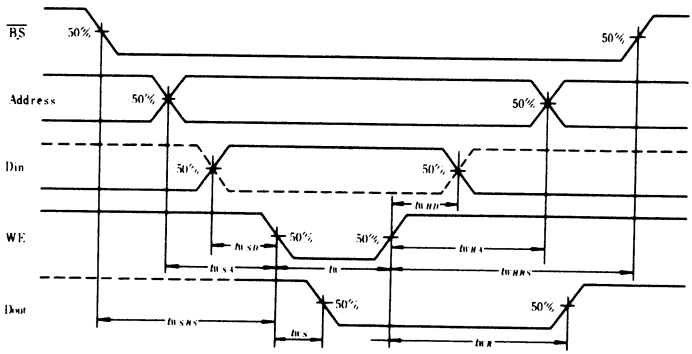


3. READ MODE





4. WRITE MODE



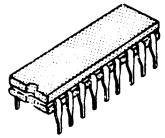
HM100470

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.



(DG-18)

■FEATURES

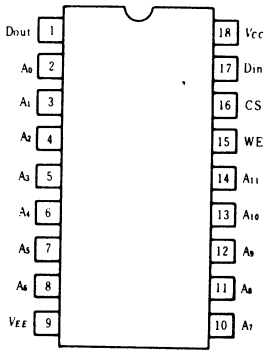
- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns (min)
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

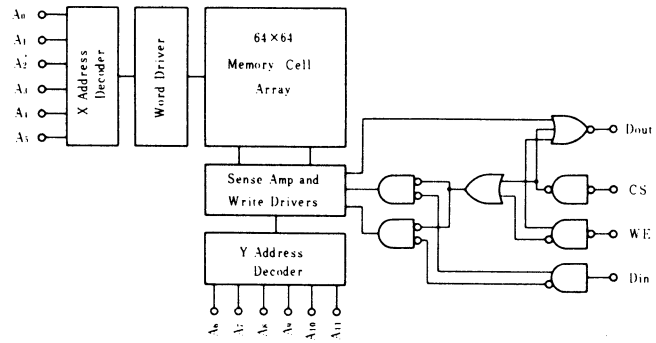
Notes) × : Irrelevant
* : Read Out Nonivert

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WAS} = 3ns	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

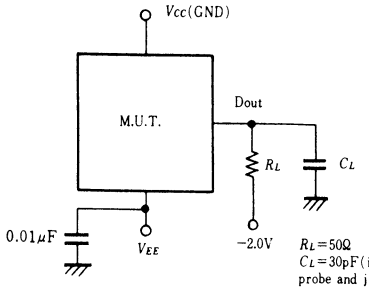
4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

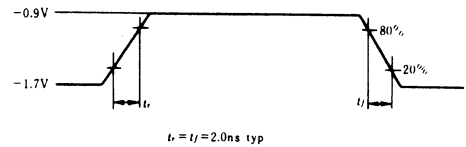
1. LOADING CONDITION

Test Circuit



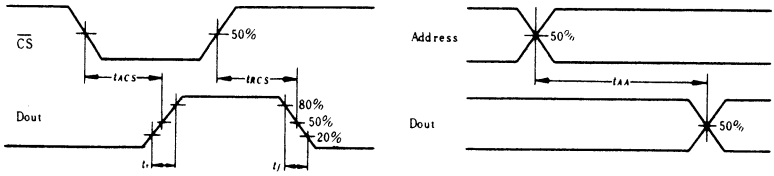
R_L=50Ω
C_L=30pF (includes probe and jig capacitance)

2. INPUT PULSE

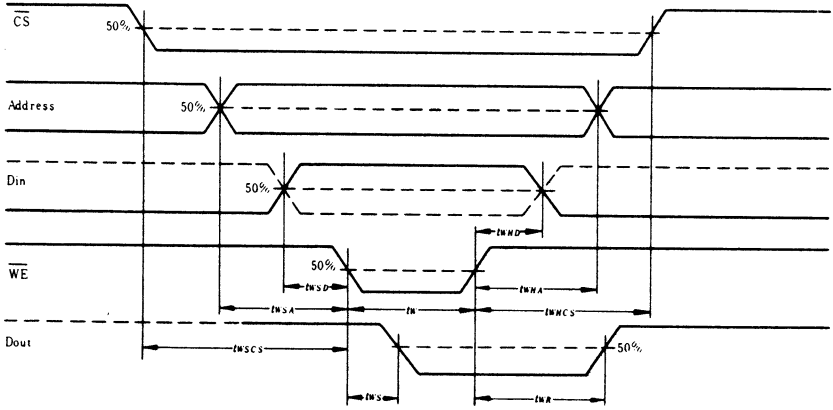


$t_r = t_f$=2.0ns typ

3. READ MODE



4. WRITE MODE



HM100474,HM100474-15
HM100474F,HM100474F-15

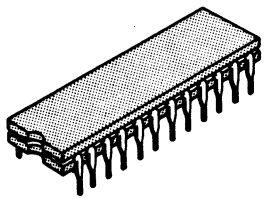
1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

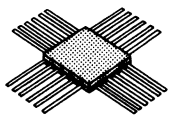
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474, HM100474-15



(DG-24A)

HM100474F, HM100474F-15



(FG-24)

■ FEATURES

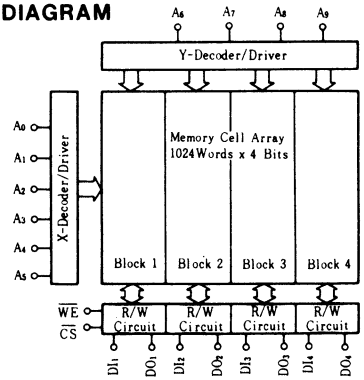
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
  HM100474/F-15 15ns(max)
- Write pulse width: HM100474/F 25ns(min)
  HM100474/F-15 20ns(min)
- Output obtainble by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



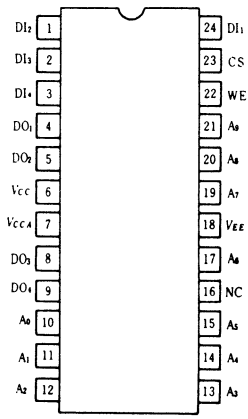
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

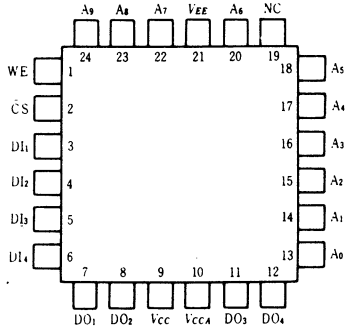
■ PIN ARRANGEMENT

● HM100474,HM100474-15



(Top View)

● HM100474F, HM100474F-15



(Top View)

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	8	—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	—	—	10	ns
Address Access Time	t_{AA}		—	—	15	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	20	—	—	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = twmin	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	27	ns

3. RISE/FALL TIME

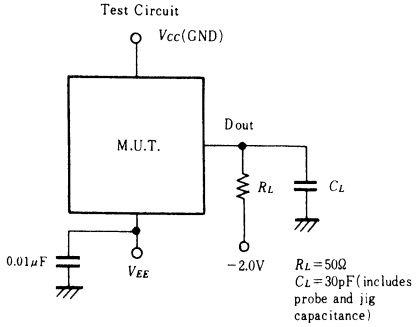
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

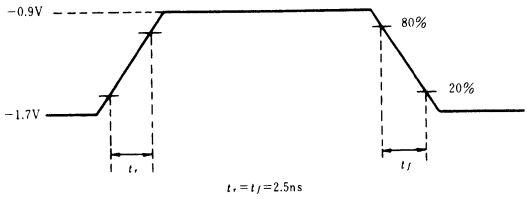
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

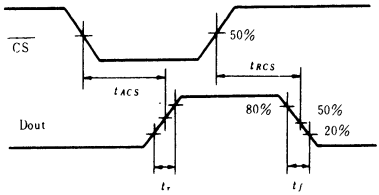
1. LOADING CONDITION

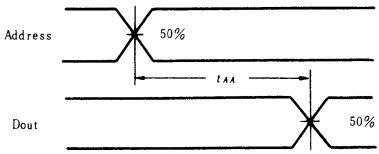


2. INPUT PULSE

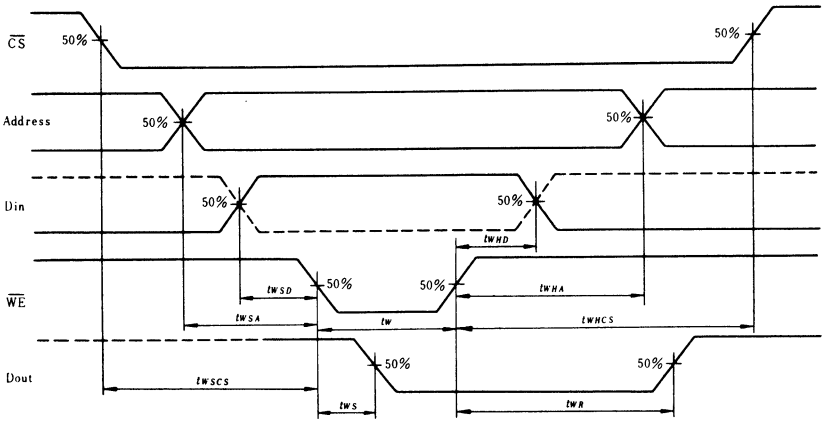


3. READ MODE

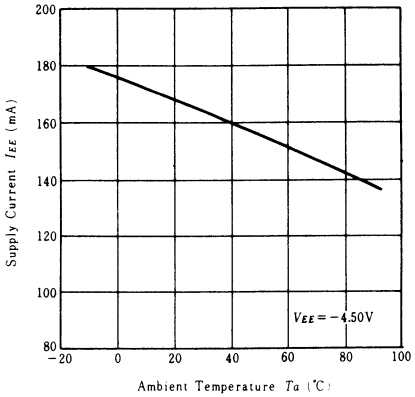




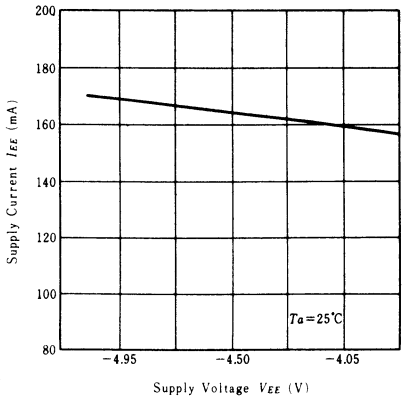
4. WRITE MODE



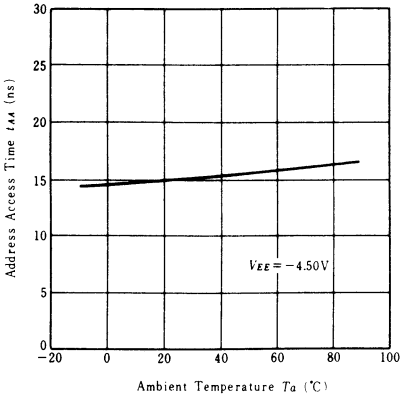
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



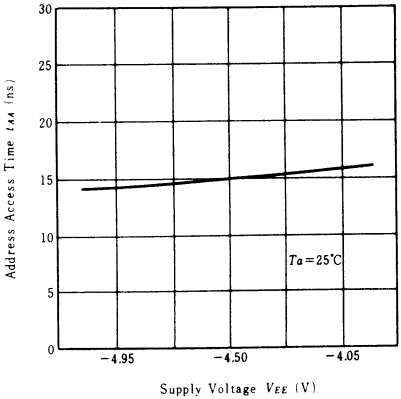
SUPPLY CURRENT vs. SUPPLY VOLTAGE



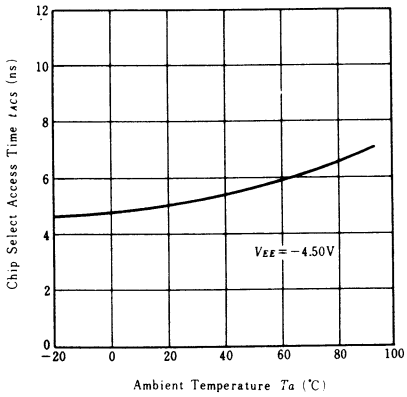
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



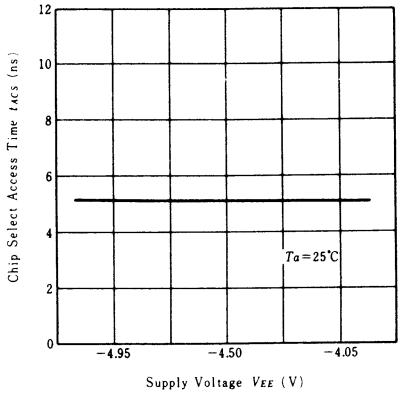
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



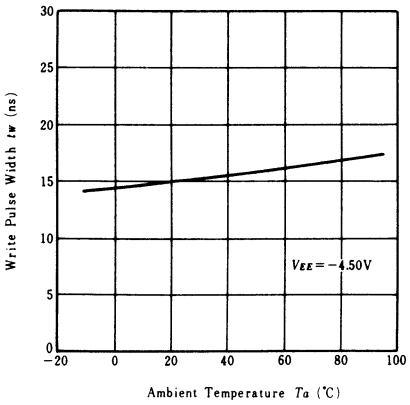
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



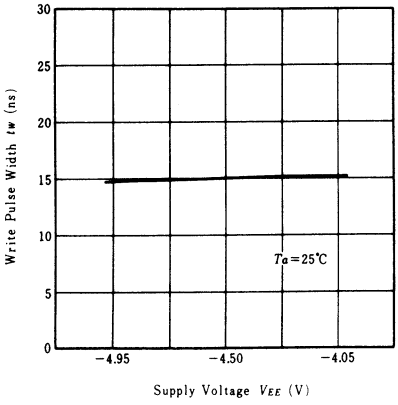
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



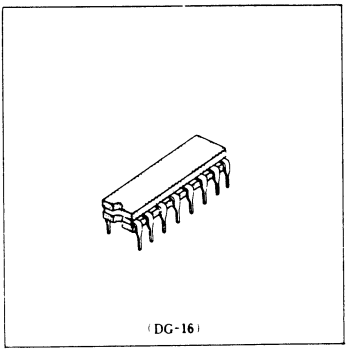
MEMORY SUPPORT CIRCUITS

HD2912

Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAND function. Its input is a TTL level and its output becomes and N MOS clock input level. It operates on two power supplies – V_{CC} (5V) and V_{DD} (12V). It anticipates taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- TTL-MOS level converter circuit
- Switching time: 50 ns (max.)
- Load capacity drivable: 600pF
- Mounted with 4 circuits
- Applicable temperature: 0 to 70°C



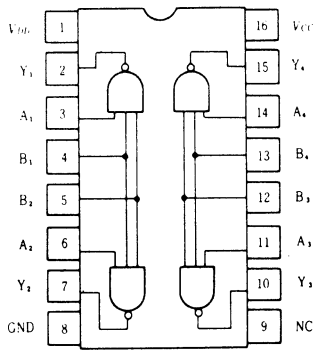
(DG-16)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2912	Unit
Supply Voltage	V_{CC}*	7.0	V
	V_{DD}*	18.0	V
Input Voltage	V_{in}*	5.5	V
Load Capacitance	C_L**	600	pF
Power Dissipation	P_T***	800	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* With respect GND
** per circuit
*** per package

■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12	12.6	V
Operating Temperature	T_{opr}	0	25	70	°C
Load Capacitance	C_L	100	—	600	pF
Damping Resistance	R_D	10	—	—	Ω

■ ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

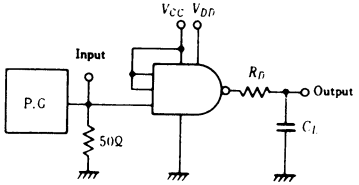
Item		Symbol	Test Condition	min	typ*	max	Unit
Input Voltage		V_{IL}		2.0	—	—	V
		V_{IH}		—	—	0.8	V
Output Voltage		V_{OL}	V_{in}=2V, I_{OL}=0.1mA	—	0.45	0.6	V
		V_{OH}	V_{in}=0.8V, I_{OH}=−0.1mA	V_{DD}−0.9	11.5	—	V
Input Current	A	I_{IL}	V_{in}=0.4V	—	−1	−1.6	mA
	B	I_{IL}		—	−2	−3.2	mA
	A	I_{IH}	V_{in}=2.4V	—	—	40	μA
	B	I_{IH}		—	—	80	μA
		I_I	V_{in}=5.5V	—	—	1	mA
Power Supply Current		I_{DDH}	V_{in}=0V	—	16	24	mA
		I_{DDL}	V_{in}=5V	—	—	0.5	mA
		I_{CCH}	V_{in}=0V	—	12	18	mA
		I_{CCL}	V_{in}=5V	—	67	100	mA
Input Clamp Voltage		V_I	I_{in}=−12mA	—	—	−1.5	V

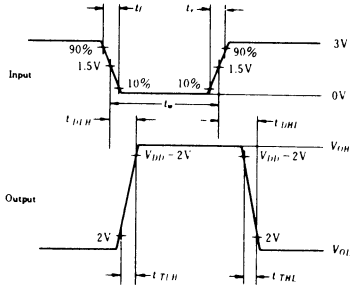
* V_{CC}=5V, V_{DD}=12V

■ SWITCHING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V, V_{DD}=12V)

Item	Symbol	Test Condition	min	typ	max	Unit
Rising Delay Time	t_{DLH}	C_L=300pF R_D=0Ω	—	35	50	ns
Falling Delay Time	t_{DHL}		—	25	45	ns
Rise Time	t_{TLH}		—	12	25	ns
Fall Time	t_{THL}		—	12	25	ns

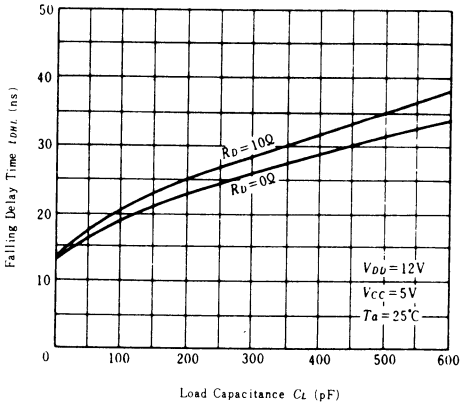
● TEST CIRCUIT AND WAVEFORMS



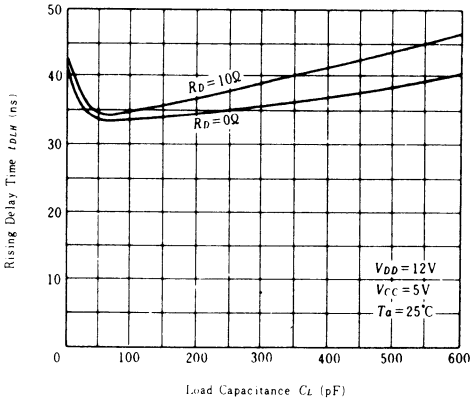


t_w = 250ns, t_{DHL} = 350ns, t_f = t_r = 10 ± 1ns

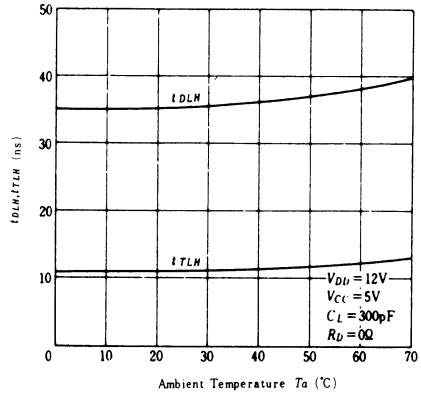
FALLING DELAY TIME vs. LOAD CAPACITANCE (1)



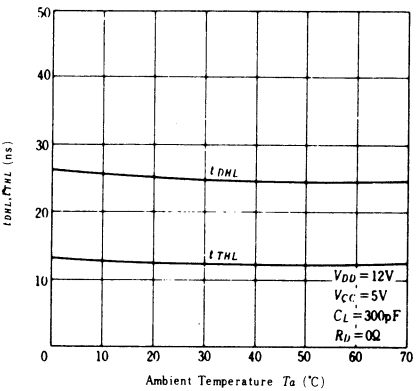
RISING DELAY TIME vs. LOAD CAPACITANCE (2)



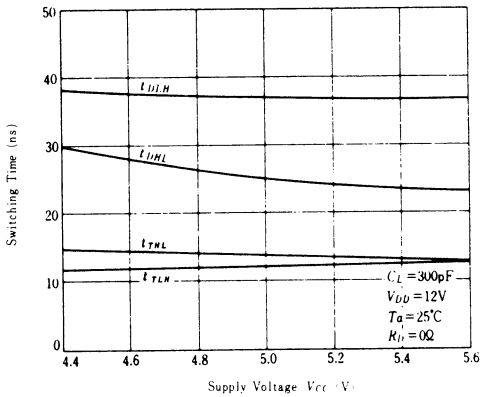
RISE TIME AND RISING DELAY TIME vs. AMBIENT TEMPERATURE



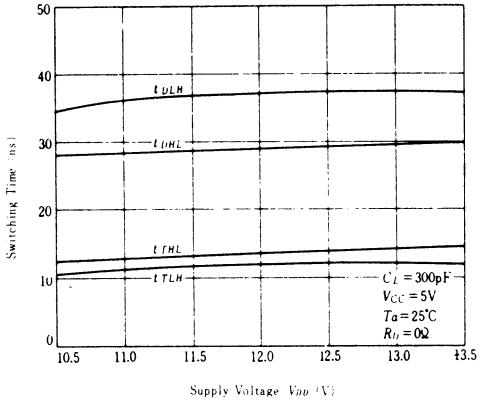
FALL TIME AND FALLING DELAY TIME vs. AMBIENT TEMPERATURE



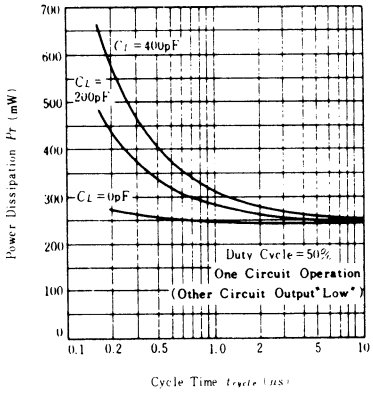
SWITCHING TIME vs. SUPPLY VOLTAGE (1)



SWITCHING TIME vs. SUPPLY VOLTAGE (2)



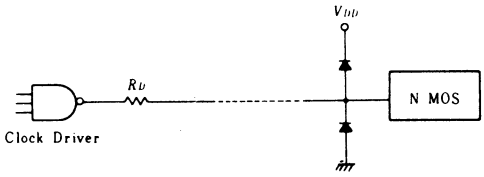
POWER DISSIPATION vs. CYCLE TIME



■ITEMS REQUIRING CARE WHEN USING THE HD2912

When measuring or mounting the HD2912, consider the following.

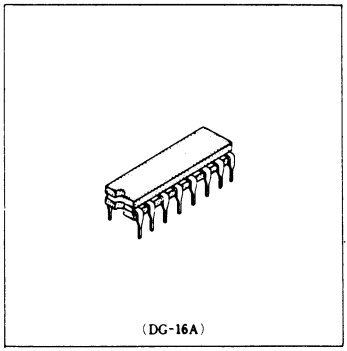
1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.
3. If its load capacity is less than a certain value (100pF), sometimes this element cannot fully provide its function. Take note of this fact when designing a system.
4. When mounting this element, it is recommended providing the output terminal with a damping resistor (R_D) or a diode terminating circuit.



HD2916

Quadruple TTL-to-NMOS Clock Drivers

The HD2916, a clock driver for the MOS memory, basically possesses a NAND function. Its Input is a TTL level and its output becomes N MOS clock input level. It operates on two power supplies $-V_{CC}$ (5V) and V_{DD} (12V). Assuming that a maximum of five units of 4K-bit N MOS memories may be connected, it is designed to drive a load capacity of 200pF at high speeds.

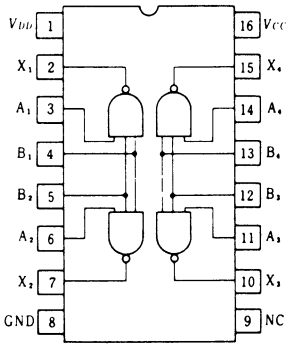


(DG-16A)

■ FEATURES

- TTL-MOS level converter
- Switching time: 50 ns (max.)
- Average power consumption: 600mW (max.)
- Load capacity drivable: 300pF
- Mounted with 4 circuits
- Applicable temperature: 10 to 65°C

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2916	Unit
Supply Voltage	V_{CC}*	−0.5 to +7	V
	V_{DD}*	−0.5 to +15	V
Input Terminal Voltage	V_{IN}*	−0.5 to +5.5	V
Output Load Capacitance	C_L**	300	pF
Power Dissipation	P_T***	700	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−50 to +150	°C

* With respect to GND
** Per circuit
*** Per package

■ RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12.0	12.6	V
Operating Temperature	T_{opr}	10	25	55	°C
Input Voltage Level	V_{IH}	2.0	—	5.5	V
	V_{IL}	−0.5	—	0.8	V

■ ELECTRICAL CHARACTERISTICS (Ta=10 to 55°C, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

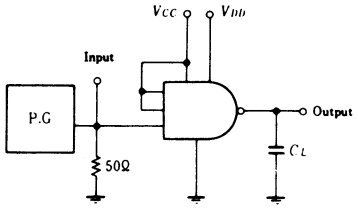
Item		Symbol	Test Condition	min	typ*	max	Unit
Input Current	A	I_{IH}	V_{IN}=2.4V	—	—	40	μA
		I_{IL}	V_{IN}=0.4V	—	−1	−2	mA
	B	I_{IH}	V_{IN}=2.4V	—	—	80	μA
		I_{IL}	V_{IN}=0.4V	—	−2	−4	mA
Output Voltage		V_{OH}	V_{IN}=0.8V, I_{OH}=−50μA	V_{DD}−0.7	V_{DD}−0.4	—	V
		V_{OL}	V_{IN}=2.0V, I_{OL}=50μA	—	0.3	0.45	V
Supply Current		I_{DDH}	V_{IN}=0V	—	13	20	mA
		I_{CCH}	V_{IN}=0V	—	13	40	mA
		I_{DDL}	V_{IN}=5V	—	—	39	mA
		I_{CCL}	V_{IN}=5V	—	40	60	mA
Average Power Dissipation		P_{TA}	C_L=300pF, f=1MHz tw=0.5μs, one circuit operation	—	300	600	mW

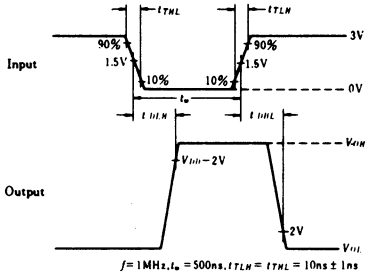
* V_{CC}=5V, V_{DD}=12V

■ SWITCHING CHARACTERISTICS (Ta=10 to 55℃, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

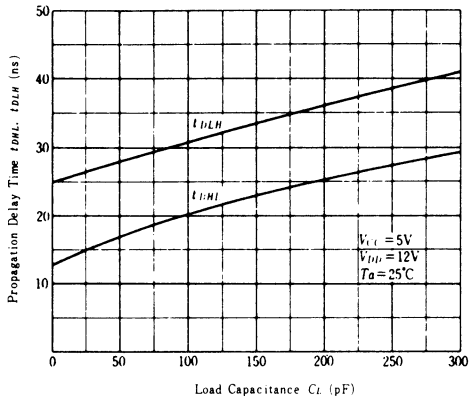
Item	Symbol	Test Condition	min	typ	max	Unit
Output Delay Time	t_{DLH}	C_L=200pF f=1MHz t_W=0.5μs	—	—	50	ns
	t_{DHL}		—	—	50	ns

● TEST CIRCUIT & WAVEFORMS

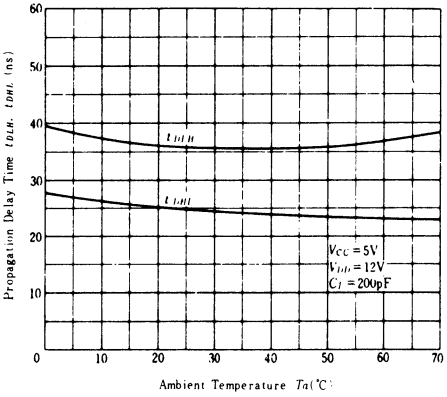




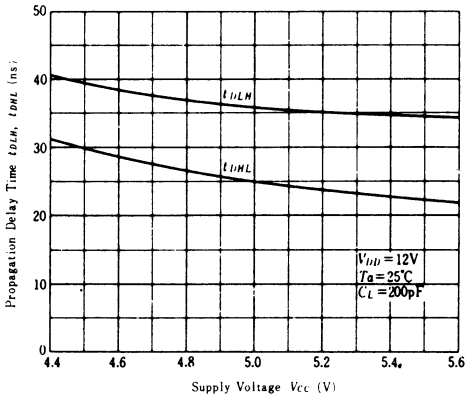
PROPAGATION DELAY TIME vs. LOAD CAPACITANCE



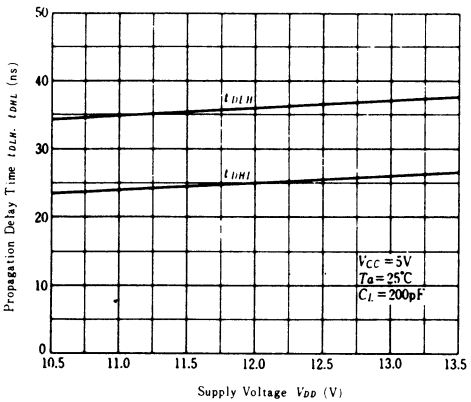
PROPAGATION DELAY TIME vs. AMBIENT TEMPERATURE



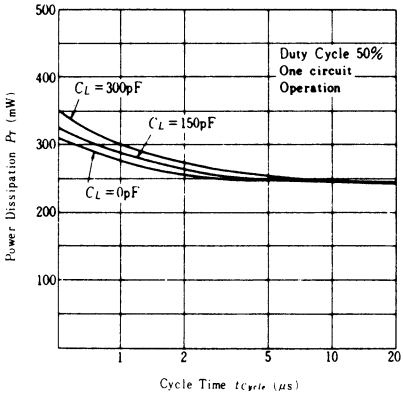
PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



POWER DISSIPATION vs. CYCLE TIME



■ITEMS REQUIRING CARE WHEN USING THE HD2916

When measuring or mounting the HD2916, consider the following:

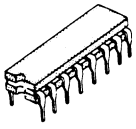
1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.

HD2923

Quadruple ECL to TTL Drivers

The HD2923 is a monolithic, high speed Quadruple ECL to TTL Driver which accepts ECL input signals. It provides high output current suitable for driving the TTL clock inputs or other address multiplexing inputs of N-channel MOS memories such as the HM4816A of MK4116. Power supply requirements are ground, +5.0 Volts and −5.2 Volts. The HD2923 requires no particular power supply sequencing in order to assure standby mode of memories, because the outputs are always "high" at applying the power. Propagation delay is 10ns MAX.

The HD2923 is fabricated by means of HITACHI's Schottky Bipolar technology to assure high performance over the 0°C to 75°C ambient temperature range.



(DG-16A)

■ FEATURES

- High Speed ..... t_{pd} = 10ns MAX. (50% to 2.2V dc out or to +1.0V dc out, 200pF Load)
- Low Power ..... 250mW typ. (DC)
- 10K ECL Compatible Inputs
- Pin Compatibility ..... MC10125 or HD10125

■ ABSOLUTE MAXIMUM RATINGS

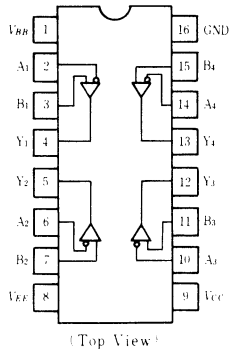
Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
	V_{EE}	−7 to +0.5	V
Input Voltage	V_{in}	V_{EE} to +0.5	V
Output Voltage	V_{out}	−1.0 to V_{CC}+1	V
Power Dissipation	P_T	1.0	W
Operating Temperature*	T_{opr}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* under bias

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Input Voltage	V_{IH}	−1.025	—	—	V
	V_{IL}	—	—	−1.520	V
Operating Temperature	T_{opr}	0	—	75	°C

■ PIN ARRANGEMENT



(Top View)

The V_{BB} reference voltage is available on pin 1 for use in single ended input biasing

■ TRUTH TABLE

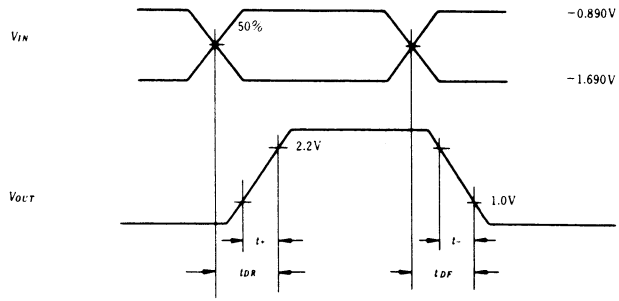
Input		Output
A	B	Y
H	V_{BB}	L
L	V_{BB}	H
H	L	L
L	H	H
V_{BB}	H	H
V_{BB}	L	L
Open	Open	H

■DC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Power Supply Drain Current	$-I_{EE}$	$V_{EE}=-5.2V$, $V_{CC}=5.0V$	—	22	27	mA
	I_{CCH}		—	23.5	29	mA
	I_{CCL}		—	34.5	42	mA
Input Current	I_{inH}	$V_{IN}=-0.81V$	—	—	115	μA
Input Leakage Current	I_{CBO}	$V_{IN}=-5.2V$	—	—	1.0	μA
Output Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OL}	$I_{OL}=5.0mA$	—	—	0.5	V
Threshold Voltage	V_{OHA}	$V_{IH}=-1.1V$, $I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OLA}	$V_{IL}=-1.48V$, $I_{OL}=5.0mA$	—	—	0.5	V
Indeterminate Input Protection Tests	V_{OHS}	All inputs $=V_{EE}$	2.7	—	—	V
		All inputs = Open	2.7	—	—	
Reference Voltage	V_{BB}		−1.420	—	−1.150	V
Common Mode Rejection Tests	V_{OHC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	2.7	—	—	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	2.7	—	—	
	V_{OLC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	—	—	0.5	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	—	—	0.5	

■AC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{DR}	50% to +2.2V, $C_L=200pF$	—	—	10	ns
	t_{DF}	50% to +1.0V, $C_L=200pF$	—	—	10	ns
Rise Time	t^+	+1.0V to +2.2V, $C_L=200pF$	—	—	5	ns
Fall Time	t^-	+2.2V to +1.0V, $C_L=200pF$	—	—	5	ns



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