PLACE™ Advanced Development Software for PEEL Arrays and PEEL Devices

Features

- **PEEL Architectural Compiler and Editor**
  - Advanced development support for PEEL Arrays and PEEL Devices
  - PC based software
  - Fast an efficient design environment
- **Architectural Editing**
  - Graphic display and control of architecture
  - Equation and state machine entry
- **Logic Compilation**
  -Auto-transformation to sum-of-products
  - Five level of logic reduction
- **Multi-level Logic Simulation**
  - Simulates internal and external signals
  - Interactive waveform editor and display
- **Translates Standard PLDs to PEEL Products**
  - Reads PLD (PAL, GAL, EPLD) JEDEC file then automatically translates to PEEL Devices and PEEL Arrays
- **Programmer Interface**
  -Interfaces to ICT's to PDS and Popular third party programmers

General Description

PLACE™ is an advanced development software package offering support for ICT's family of PEEL (Programmable Electronically Erasable Logic) Arrays and Devices. The innovative architectural editor enables graphical control of the device architecture, along with logic equation, truth table, and state machine entry, making the overall design process easy to understand. The PLACE compiler performs logic transformations so equations can be defined in a variety of formats. The compiler also features five levels of user-selectable logic reduction, including auto-demorganization, making it possible to fit more logic into every design. PLACE also provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a special waveform display. Documentation of PLACE designs is accomplished through batch printing of equations, architecture and waveform displays. System requirements for PLACE are: DOS 3.0 or greater, 540k base memory, EGA or VGA graphics, and a mouse. PLACE also supports expanded memory systems with EMS drivers conforming to the 3.2 or greater LIM EMS specification.

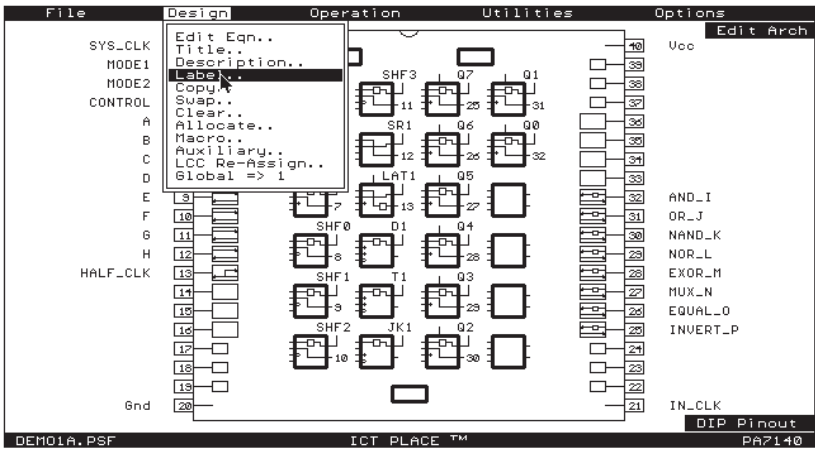


Figure 1. The PLACE architectural editor's "chip display" provides a global view of the design, allowing quick access to I/Os, registers, cells and equations.

Figure 2. The PLACE software functions in a mouse-driven windows environment allowing easy access and control of all operations. Shown here is the file selection window.

Figure 3. The architecture of each cell can be specified by selecting the desired architectural element with the mouse and then “clicking” through all possible configurations graphically on the screen. Shown here is the PA7024’s register selection of D, T or JK flip-flops.

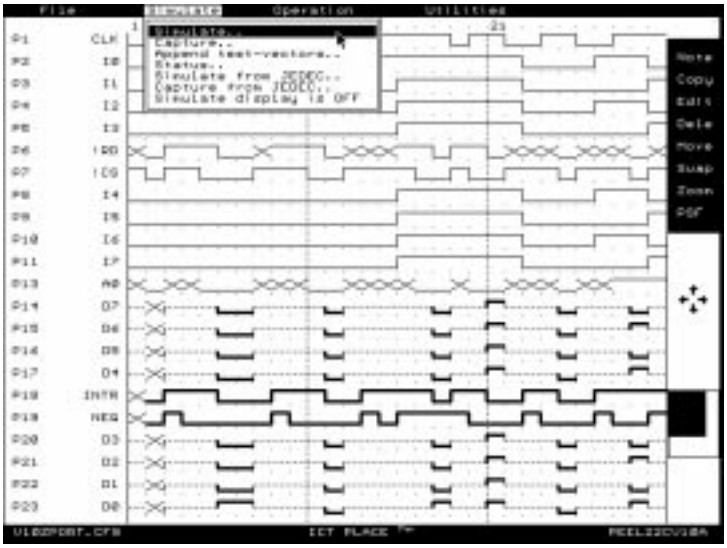


Figure 5. The PLACE logic simulator lets external and internal signals be fully simulated, analyzed and edited via a special waveform display. Output signals can be “captured” or simulated. Simulation errors are marked on the display for quick analysis.

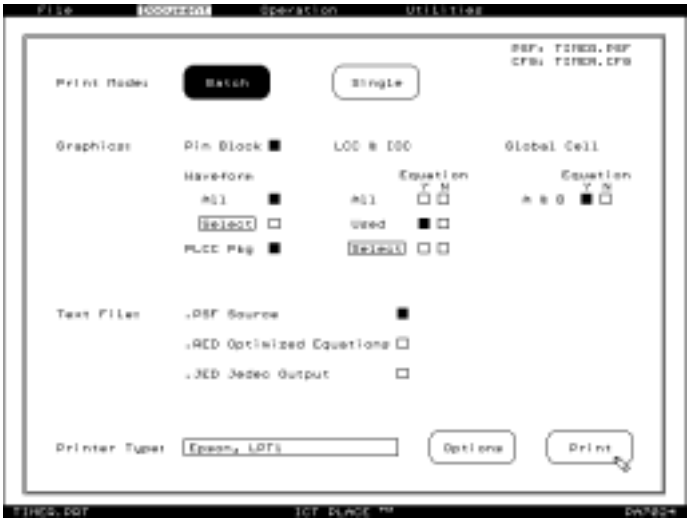


Figure 6. PLACE designs can be documented through batch or single printing of architectural configurations, waveform displays and logic descriptions including equations, state-diagrams, and truth-tables.

PEEL™ Device and Array Smart Translator

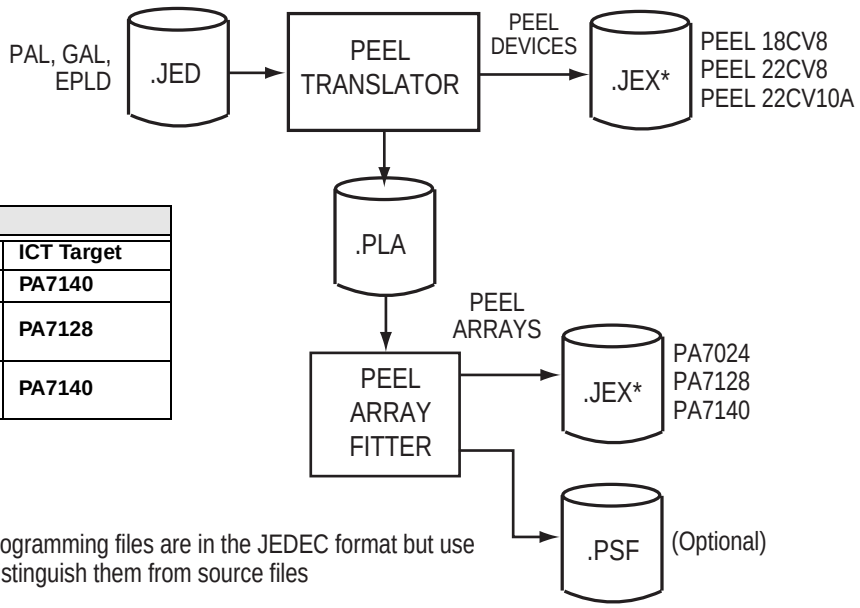
Features

- **Automatic JEDEC File Translation**
  - Translates over 50 PALs, GAL, EPLDs
  - Supports conversion into pin-compatible PEEL Devices and PEEL Arrays
- **Advanced Fitter Supports PEEL Array CPLDs**
  - Works from intermediate PLA format
  - Optimizes cell and I/O placement for best fit
  - Supports PA7024, PA7128, and PA7140
- **Creates Optional PLACE Source File**
  - Enables design changes and additions
  - Allows architectural viewing of design
  - Provides JEDEC file waveform simulator
- **Allows Easy Design Upgrades and Fixes**
  - More flexibility PEEL Devices and Arrays easily accommodate design upgrades
  - Higher effective density allows fixes for unexpected problems
- **Creates Alternate Source**
  - Superset architectures allow one type of PEEL product to replace many different PLDs
- **System Requirements**
  - PC or compatible running DOS 3.0 or greater

General Description

The PEEL™ Smart Translator software tool allows designers to automatically convert JEDEC programming files from over 50 different of PALs, GALs, and EPLDs into programming files for pin-compatible ICT PEEL Devices and PEEL Arrays. In addition to providing direct JEDEC-to-JEDEC file conversions, the Smart Translator also optionally produces PLACE source (.psf) and ABEL (.pla) files, which allow users to make easy design upgrades, salvage troubled designs, replace multiple PLD types with a single type of ICT PLD, create an alternate source, convert to EEPROM reprogrammable devices, and often reduce power consumption and device costs.

For simple PLDs, such as 20/24-pin PALs, GALs and EPLDs, the PEEL Smart Translator performs a direct JEDEC-to-JEDEC translation. For more complex PLDs, the translator first produces an intermediate file in the PLA format, then automatically invokes ICT's proprietary fitter software to efficiently map the design into the target PEEL Array JEDEC programming files. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit, easing conversion from other PLD designs. A detailed description of the fitting results is recorded in the ".rpt" (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing and simulation of the design in PLACE.



Newly Supported Devices	
Source	**ICT Target**
5C060, EP600/610	**PA7140**
AT750, GAL6001/2 PLACE/GAL26V12	**PA7128**
5CO9O, EP900 PLD910, EP910	**PA7140**

*Translator output programming files are in the JEDEC format but use .JEX extention to distinguish them from source files

Figure 1. PEEL Translator Design Flow

ABEL-to-PEEL™ (for DOS) Advanced Device Fitter

Features

- **PEEL Array Support for ABEL Software**
  - Supports PA7024, 7128, and 7140
  - Operates with ABEL 4.0 or greater
- **Maintains ABEL Design Methodology**
  - Design, compile, simulate with ABEL
  - Fitter creates JEDEC programming files
  - Operates on “Berkeley Espresso” PLA files
- **True Device Independent Design Entry**
  - I/O pin and node numbers need not be specified
  - Optimizes cell and I/O placement for best fit
  - Eases conversion from other PLD designs
- **Translation to PLACE Source File**
  - Optionally creates PLACE “.psf” source files
  - Allows architectural viewing of design
  - Alternate compiler for complex designs
  - JEDEC file waveform simulator
- **PEEL Array ABEL Design Examples**
  - Numerous examples provided for reference
  -Combinatorial, synchronous, asynchronous applications
- **System Requirements**
  - PC compatibles (DOS 5.0 or greater)
  - Sun SPARCstations (Contact ICT)

General Description

The ABEL-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL™ Array family (PA7024, PA7128, PA7140) using the ABEL 4.0 (or greater) high-level design language from Data I/O. The ABEL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on "Berkeley Espresso" PLA files that are produced by the ABEL compiler and creates PEEL™ Array JEDEC programming files. The ABEL-to-PEEL™ Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a ".log" file. The fitter also allows use of the PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array ABEL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. The ABEL-to-PEEL Fitter operates on PC compatibles with DOS 5.0 or Sun SPARCstations.

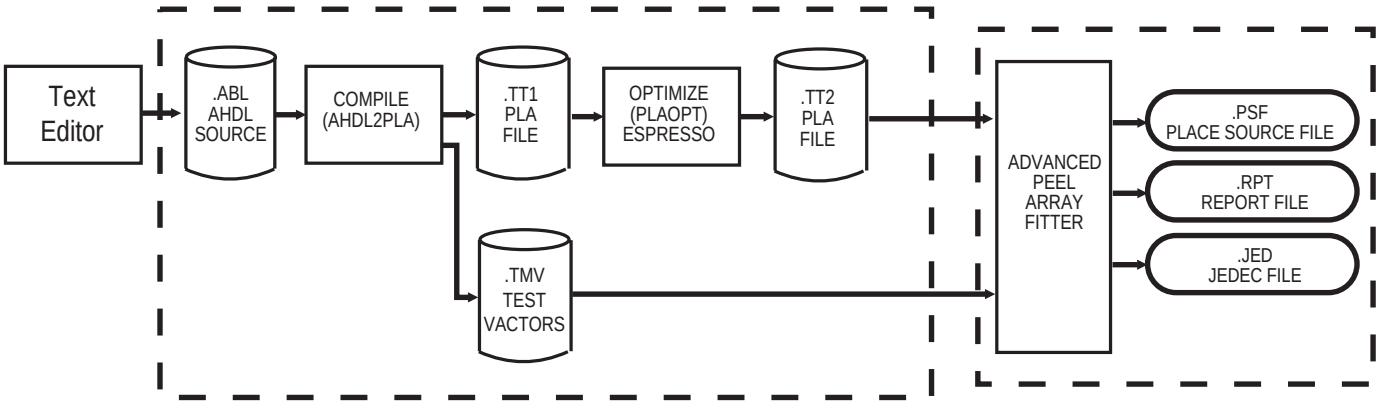


Figure 1. Design flow with the ABEL-to-PEEL Advanced Fitter

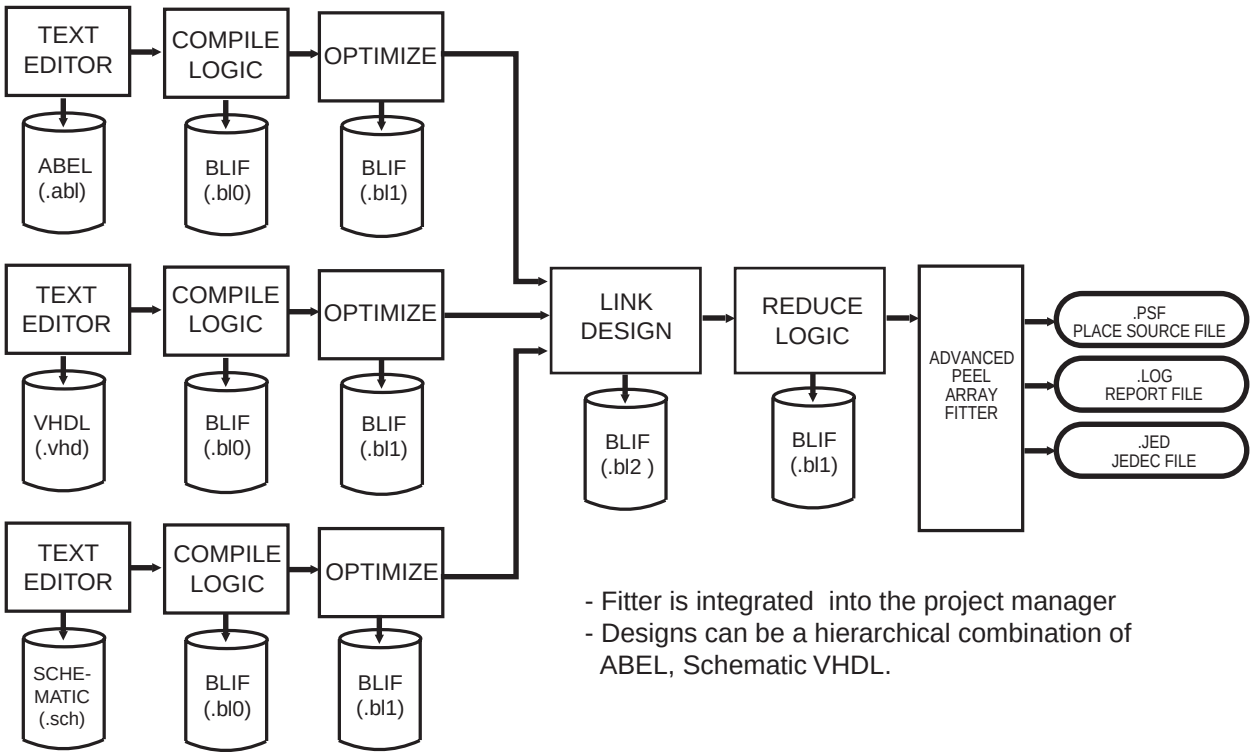
Synario®/ABEL-to-PEEL™ (for Windows)
Advanced Device Fitter

Features

- **PEEL Array Support for ABEL Software**
  - Supports PA7024, 7128, and 7140
  - Operates with ABEL 4.0 or greater
- **Maintains Synario Design Methodology**
  - Design, compile, simulate with Synario
  - Fitter creates JEDEC programming files
  - Support schematic and HDL entry
- **True Device Independent Design Entry**
  - I/O pin and node numbers need not be specified
  - Optimizes cell and I/O placement for best fit
- **Translation to PLACE Source File**
  - Optionally creates PLACE ".psf" source files
  - Allows architectural viewing of design
  - Alternate compiler for complex designs
  - JEDEC file waveform simulator
- **PEEL Array ABEL Design Examples**
  - Numerous examples provided for reference
  - Combinatorial, synchronous, asynchronous applications
- **System Requirements**
  - PC compatibles (DOS 5.0 or greater)

General Description

The Synario-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using Synario 2.0. The Synario development methodology is fully maintained through design entry, compilation and functional simulation. Design can be described using schematics and text in Data I/O's ABEL industry-standard format, or VHDL. The fitter operates on BLIF files that are produced by the Synario compiler, and creates PEEL Array JEDEC programming files. The Synario-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the fitting results is recorded in the ".log" (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE. it is also possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array Synario schematic, ABEL, and VHDL design examples are provided for reference. The Synario-to-PEEL Fitter operates on PCs and compatibles.



- Fitter is integrated into the project manager
- Designs can be a hierarchical combination of ABEL, Schematic VHDL.

Figure 1. Flow diagram for Synario

CUPL-to-PEEL™ Advanced Device Fitter

Features

- **PEEL Array Support for ABEL Software**
  - Supports PA7024, 7128, and 7140
  - Operates with ABEL 4.0 or greater
- **Maintains Synario Design Methodology**
  - Design, compile, simulate with CUPL
  - Fitter creates JEDEC programming files
  - Operates on “Berkeley Espresso” PLA files
- **True Device Independent Design Entry**
  - I/O pin and node numbers need not be specified
  - Optimizes cell and I/O placement for best fit
  - Eases conversion from other PLD designs
- **Translation to PLACE Source File**
  - Optionally creates PLACE “.psf” source files
  - Allows architectural viewing of design
  - Alternate compiler for complex designs
  - JEDEC file waveform simulator
- **PEEL Array ABEL Design Examples**
  - Numerous examples provided for reference
  - Combinatorial, synchronous, asynchronous applications
- **System Requirements**
  - PC compatibles (DOS 5.0 or greater)

General Description

The CUPL-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using the CUPL 4.5 (or greater) high- level design language from Logical Devices. The CUPL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on Berkeley Espresso” PLA files that are produced by the CUPL compiler and creates PEEL Array JEDEC programming files. The CUPL-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of I/Os and logic cells for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a “.log” file. The fitter also allows use of the PLACE software by optionally creating a '.psf" extension file which allows architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file white using the PLACE software. Numerous PEEL Array CUPL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. The CUPL-to-PEEL Fitter operates on PC compatibles with DOS 5.0 or greater.

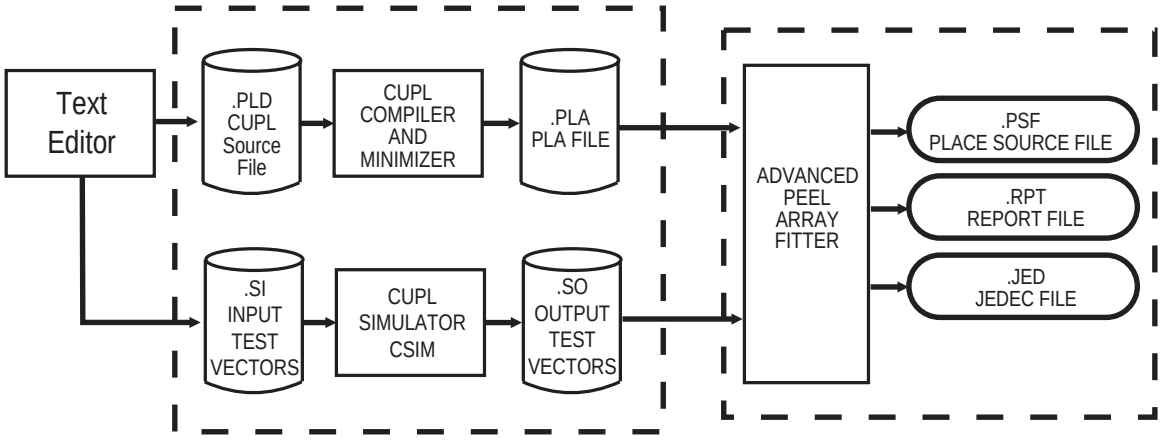


Figure 1. Design Flow for the CUPL-to-PEEL Advanced Fitter

OrCAD®-to-PEEL™ Advanced Device Fitter

Features

- **PEEL Array Support for OrCAD PLD 386+**
  - Supports PA7024, 7128, and 7140
  - Operates with OrCAD PLD 386+ 2.0 or greater
- **Maintains OrCAD Design Methodology**
  - Design, compile, simulate with OrCAD
  - Fitter creates JEDEC programming files
  - Supports schematic and HDL entry
- **True Device Independent Design Entry**
  - I/O pin and node numbers need not be specified
  - Optimizes cell and I/O placement for best fit
  - Extensive library of gate and TTL functions
- **Translation to PLACE Source File**
  - Optionally creates PLACE ".psf" source file
  - Allows architectural viewing of design
  - Alternate compiler for complex designs
  - JEDEC file waveform simulator
- **PEEL Array CUPL Design Examples**
  - Numerous examples provided for reference
  - Schematic and OrCAD HDL designs included
- **System Requirements**
  - PC compatibles (DOS 5.0 or greater)

General Description

The OrCAD-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using OrCAD PLD 386+ Programmable Logic Design Tools. The OrCAD development methodology is fully maintained through design entry, compilation and functional simulation. Designs can be described using schematics from OrCAD SDT 386+, text in OrCAD's OHDL format, or any combination of the two. The fitter operates on "Berkeley Espresso" PLA files that are produced by the OrCAD compiler, and creates PEEL Array JEDEC programming files. The OrCAD-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the fitting results is recorded in the ".rpt" (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE. It is also possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array OrCAD schematic and OHDL design examples are provided for reference. The OrCAD-to-PEEL Fitter operates on IBM or NEC-compatible PCs

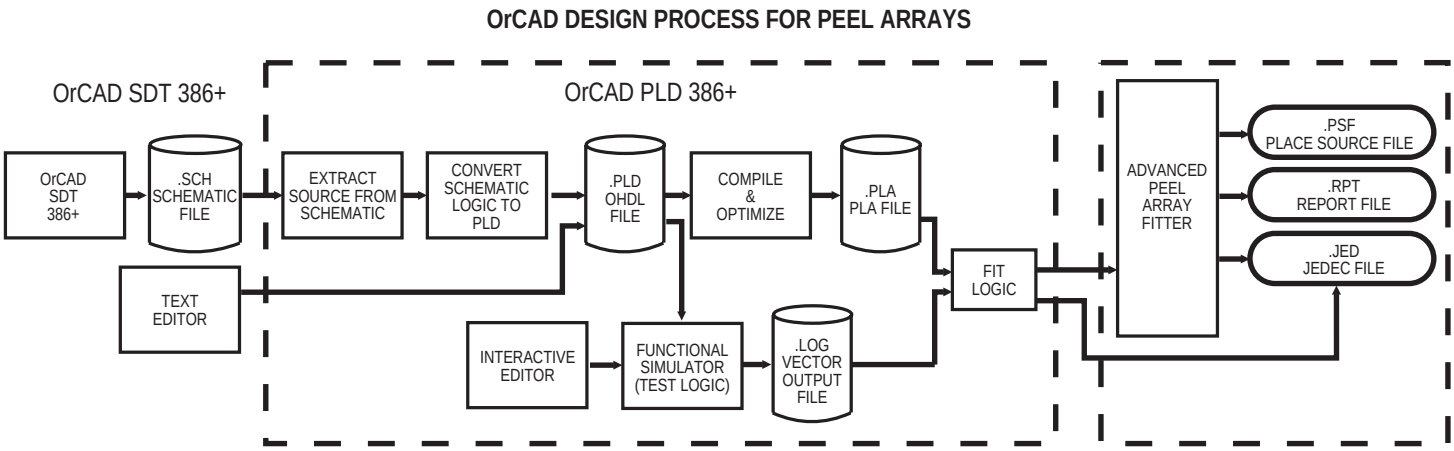


Figure 1. OrCAD design process for PEEL Arrays

PDS-3 PEEL™ Development System

Features

- **PEEL Array Support for OrCAD PLD 386+**
  - Supports PA7024, 7128, and 7140
  - Operates with OrCAD PLD 386+ 2.0 or greater
- **Maintains OrCAD Design Methodology**
  - Design, compile, simulate with OrCAD
  - Fitter creates JEDEC programming files
  - Supports schematic and HDL entry
- **True Device Independent Design Entry**
  - I/O pin and node numbers need not be specified
  - Optimizes cell and I/O placement for best fit
  - Extensive library of gate and TTL functions
- **Translation to PLACE Source File**
  - Optionally creates PLACE ".psf" source file
  - Allows architectural viewing of design
  - Alternate compiler for complex designs
  - JEDEC file waveform simulator
- **PEEL Array CUPL Design Examples**
  - Numerous examples provided for reference
  - Schematic and OrCAD HDL designs included
- **System Requirements**
  - PC compatibles (DOS 5.0 or greater)

General Description

The PEEL Development System (PDS-3) is a powerful, yet inexpensive, PC-based system for designing with Programmable Electrically Erasable Logic (PEEL) products. Equipped with ICT's PLACE Development Software (see PLACE data sheet), the PDS-3 programmer has everything needed to create PEEL Device/Array designs from concept to silicon. The standard 40-pin DIP zero-insertionforce socket handles DIP packages from 20 to 40 pins, as well as PLCC, SOIC, TSSOP and TQFP packages using optional adapters. All standard programming functions are supported including: program, read, verify and secure. Test vectors from the JEDEC file can be applied to the device for functional verification. Built-in features ensure device integrity and reliable programming including: checksum, position/continuity check, blank check, and illegal-bit check. The auto-sense features automatically activates the PDS-3 in response to the socket without any key presses. The PDS-3 can read most any PLD (e.g., PAL, GAL, EPLD) for conversion to a PEEL Device using the PLACE translator. System requirements include an IBM PC compatible computer with DOS 3.0 or greater, 640K RAM and a serial port. Note: the PDS-3 can be upgraded to a universal PLD and memory programmer, call ICT for more information.

Figure 1. PDS-3 Development System

Table 1. ICT Inc. PEEL Array Programming Support

Company	Telephone	Product	PA7024	PA7128	PA7140
Advantech Corp.	(408) 245-6678	PC-UPROG	V.1.8	V.1.9	V.1.9
Advin System	(408) 243-7000	PILOT-U40-U84	V.10.03	V.10.77	V.10.77
BP Microsystems	(800) 225-2102	BP1100	V.1.53	V.2.30	V.2.31
		BP1128	V.1.53*	V.2.30*	V.2.31*
		BP1200	V.1.53*	V.2.30*	V.2.31*
Bytek	(561) 994-3520	U153HFT-U/A	V.1.5	C.F.	C.F.
Data I/O Corp.	(800) 247-5700	2900	V.1.6*	V.3.3*	V.3.6
		3900	V.1.0*	V.2.3*	V.2.6
		Unisite	V.3.2*	V.4.4*	V.4.8*
		Autosite	V.1.0*	V.2.3*	V.2.6
		Chip-Lab	V.1.0*	V1.2*	C.F.@
Electronic Engr. Tools	(408) 734-8184	All-Max	V.1.0	V.1.0	C.F.
Hi-Lo Research Co.	011-886 2 7640215	All-07	V.3.08	V.3.08	V.3.08
ICT Inc.	(408) 434-0678	PDS-3	V.1.00*	V.1.01*	V.1.01*
Logical Devices	(303) 722-6868	Allpro 40-88	V.2.1	V.2.4	V.2.4
		Allpro 88XR	V.1.34	V.1.34	V.1.34
		ChipMaster	V.1.8	V.1.9	V.1.9
Needham's Electronics	(916) 924-8065	EMP 20	V.4.0	V.4.0	V.4.0
SMS	(408) 542-0388	Optima	C3/92*	C/93*	A/94*
		Expert	C3/92	C/93	A/94
		Plus48	C3/92	C/93	A/94
Stag Microsystems	1-888-700-7824	Eclipse	V.2.5	V.2.3	C.F.
System General	(408) 263-6667	Turpro 1/FX	V.1.68*	V.1.68K*	V.1.68K*
Tribal Microsystem	(510) 623-8859	FLEX-700	V.3.08	V.3.08	V.3.08S
Xeltek	(408) 588-9943	Superpro II	V.1.0	V.1.7C	V.1.7C
		Superpro III	V.3.1	V.3.1	V.3.1

C.F. - Call Factory, ICT Inc. 1-800-SAY-PEEL (1-800-729-7335)
Note *: The programming algorithm has been qualified by ICT as of 12/15/94. For all others, contact ICT for latest status
Note @: This device's algorithm is available on Data I/O's BBS (an extended algorithm) or on DATA I/O's Keep Current Express, call ICT or DATA I/O for more information.

Table 2. ICT Inc. PEEL Device Programming Support

Company	Telephone	Product	PEEL 18CV8	PEEL 22CV8	PEEL 22CV10A	PEEL 22CV10A+
Advantech Corp.	(408) 245-6678	PC-UPROG	V.2.0*	V.2.3	V.1.2*	V.1.2*
Advin System	(408) 243-7000	PILOT-U40-U84	V.10.78*	C.F.	V.9.94*	V.9.94*
BP Microsystems	(800) 225-2102	BP1100	V.2.31*	C.F.	V.1.53*	V.1.53*
		BP1128	V.2.31*	C.F.	V.1.53*	V.1.53*
		BP1200	V.2.31*	C.F.	V.1.53*	V.1.53*
Bytek	(561) 9994-3520	U153HFT-U/A	V.59	C.F.	V.1.5*	V.1.5*
Data I/O Corp.	(800) 247-5700	2900	V.3.3*	V.3.6	V.3.6	V.3.6
		3900	V.2.3*	V.2.6	V.2.6	V.2.6
		Unisite	V.4.4*	V.4.8	V.4.8	V.4.8
		Autosite	V.2.3	V.2.6	V.2.6	V.2.6
		Chip-Lab	V1.20	C.F.	V.1.00	V.1.00
Electronic Engr. Tools	(408) 734-8184	All-Max	(V.1.4)	C.F.	V.1.4	V.1.4
Hi-Lo Research Co.	011-886 2 7640215	All-07	V.3.34	V.3.36A	V.1.0	V.1.0
ICT Inc.	(408) 434-0678	PDS-3	V.1.3*	V.1.18*	V.1.00*	V.1.00*
Logical Devices	(303) 722-6868	Allpro 40-88	V.2.4*	C.F.	V.2.2*	V.2.2*
		Allpro 88XR	V.1.34	C.F.	V.1.0*	V.1.0*
		ChipMaster	V.2.0	V.2.3	V.1.2	V.1.2
Needham's Electronics	(916) 924-8065	EMP 20	V.4.0	V.4.0	V.4.0	V.4.0
SMS	(408) 542-0388	Optima	C1/92*	C.F.	C3/92	C3/92
		Expert	C1/92	C.F.	C3/92	C3/92
		Plus48	C1/92	C.F.	C3/92	C3/92
Stag Microsystems	1-888-700-7824	Eclipse	stPAL	C.F.	stV	stV
System General	(408) 263-6667	Turpro 1/FX	V.2.07*	V.2.15	V.1.68*	V.1.68*
Tribal Microsystem	(510) 623-8859	FLEX-700	V.3.34	V.3.36	V.1.0	V.1.0
Xeltek	(408) 588-9943	Superpro II	V.1.7C*	C.F.	V.1.0*	V.1.0*
		Superpro III	V.3.1	V.3.1	V.3.1	V.3.1

C.F. - Call Factory, ICT Inc. 1-800-SAY-PEEL (1-800-729-7335)
Note *: The programming algorithm has been qualified by ICT as of 12/15/94. For all others, contact ICT for latest status
Note @: This device's algorithm is available on Data I/O's BBS (an extended algorithm) or on DATA I/O's Keep Current