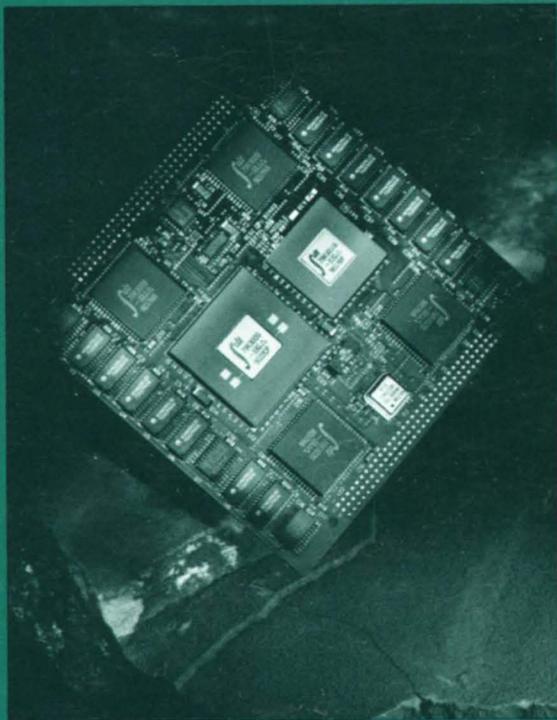


IDT RISC SUBSYSTEMS Product Information



Integrated Device Technology, Inc.

IDT RISC SUBSYSTEMS

Product Information



Integrated Device Technology, Inc.

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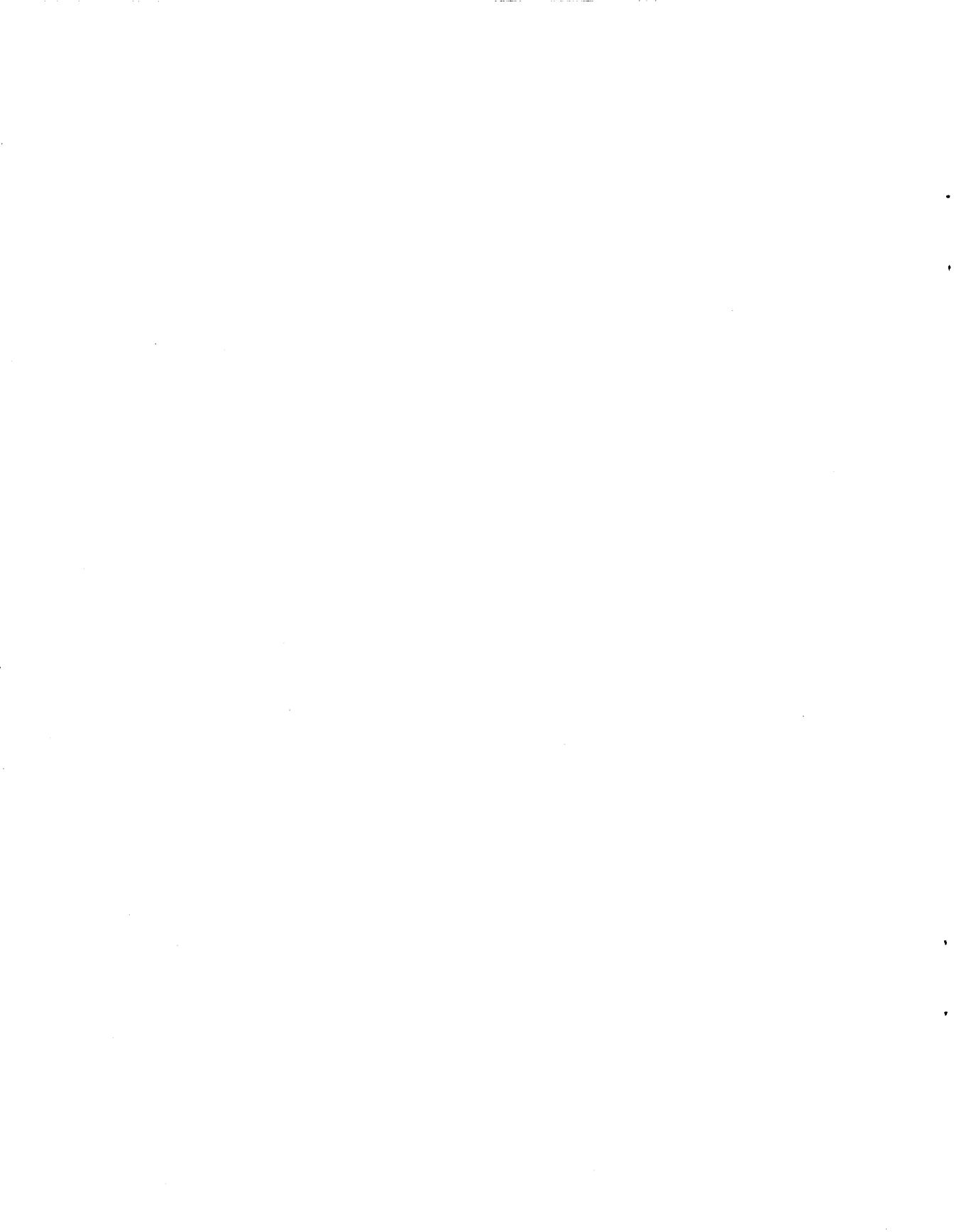
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Integrated Device Technology, Inc.

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FASTER SYSTEMS: FASTER DESIGN CYCLES

Using RISC technology, you can build systems that will run rings around an old 386 or 680x0 design. IDT's RISC SubSystems Division can help you get your design completed in record time. From pre-built modules to prototype hardware to development support and software tools, IDT takes the risk out of RISC.

Modules

Our modules contain the R3000 CPU, R3010 FPA and all the cache memory. Many include clock control, interrupt and initialization logic, as well as read and write buffers. All the components are surface-mounted on small, plug-in PC boards, burned-in and tested at the rated speed. All the tricky timing, all the high-speed design is done and tested for you. The modules can be plugged into motherboards containing main memory, I/O and the rest of the system, all of which is relatively low speed and easy to lay out using conventional design techniques.

Prototyping Platforms

To shorten your design time even more, we offer Prototyping Platforms for every module. The Prototyping Platform contains main memory, serial I/O, a powerful debug monitor in EPROM and a personality card that interfaces it directly to the module. You can download your software and you can design your own additional hardware and plug it right in. That means software and hardware development and debug can begin the moment you open the boxes and plug the boards together.

Development Support

Of course, you can develop R3000 software on one of the fast, powerful MIPS workstation systems. But we also offer a complete R3000 development system in a Macintosh II computer. Click an icon on your Mac and a new window opens under Multifinder with the UNIX operating system in it. The UNIX code is actually running on a fast R3000 system board right inside the Mac, and you can run all the MIPS development tools, including the System Programmers Package, on it. Cross-software tools for PCs running either MS-DOS or Xenix are also available.

Software

IDT's RISC SubSystems Division offers R3000 software that makes your own software development faster and easier. You can use our Software Integration Manager to control your prototypes, to debug software and to manage I/O drivers. You can put our Monitor into your own hardware to do initial hardware debug. You can use our floating point libraries to develop fast ROMable code for systems not using the Floating Point Accelerator device. And our cross-software makes efficient C-program compilation possible with low cost PCs.





Integrated Device Technology, Inc.

R3000 CPU MODULES For General Applications

IDT7RS101

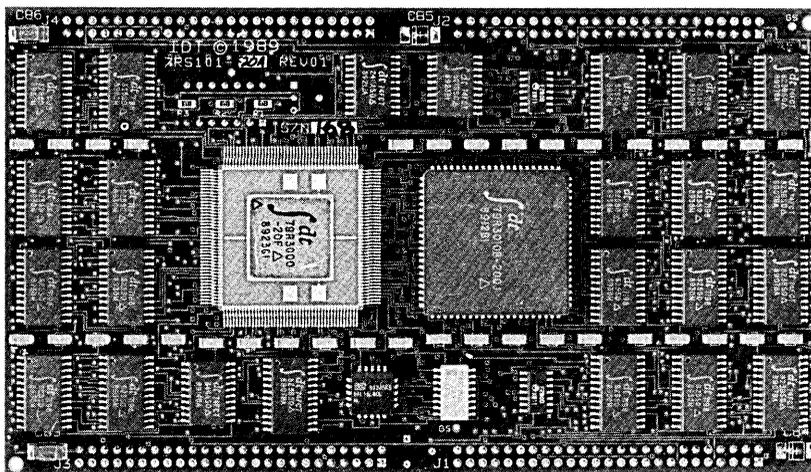
FEATURES:

- R3000 CPU on 3.7" x 6.5" plug-in module
- 64K each Instruction and Data Caches
- On-board clock generation
- Four-word read buffer for block refill. Single word write buffer
- On-board parity generation
- Five user interrupts into on-board register
- Available with or without Floating Point Accelerator
- Cache supports full 32-bit address space
- 100% burn-in and functional test at rated speed.

POWERFUL GENERAL PURPOSE R3000 MODULE:

The IDT7RS101 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, 64 Kbytes each of data and instruction cache memory, a single word write buffer and a four-word read buffer to support block refill. Clock generation, reset, control and interrupt functions are included on the module to simplify the remainder of the system design. Parity bits on incoming data words may be generated automatically on the module, transparent to the rest of the system. Alternatively, parity may be handled in the user system, with on-board circuits only performing optional parity check functions. Five user interrupts are provided with an on-board clocked register to ensure synchronized activity with the R3000 timings.

The module is constructed using surface mount devices on a 3.72 by 6.5" epoxy laminate board, and is connected to the user's system via four 50-pin Insulation Displacement Connectors.



7RS101 Module. Actual Size 3.72" x 6.50 "

ARCHITECTURAL HIGHLIGHTS

Four-word Read Buffer

The 7RS101 includes a single write buffer and a four-word deep read buffer. Cache read miss operations (memory data not currently stored in the cache) may be handled either with a four-word block refill or with a single-word fetch and cache update. All control signals are available to implement either option. Address mapping can be used to force block refills on some addresses (for example, instructions) and single-word updates on other addresses (for example, data).

Clock Generation

The clocks for both the R3000 and the R3010 are automatically generated on the module using a very accurate and stable delay line driven by a single user-supplied input clock signal. There are three buffered clock output signals for use with external control logic and system timing, each of which is an identical inverted version of the R3000 output, SYSOUT#.

Parity Generation

The R3000 Processor requires incoming data words to consist of 32 bits of data and 4 bits of parity. The 7RS101 module can be set to either of two modes for parity handling. It can check parity and report errors on incoming data that consists of 32 data bits and 4 parity bits. In the other mode, it can generate parity on 32 bits of incoming data and supply the full 36 bits to the CPU.

Initialization Options

The R3000 requires mode selection to be made during the RESET initialization sequence. The 7RS101 module provides three pins that can simply be tied High or Low by the user to select some of the R3000's options: Instruction Streaming on or off, Partial Word Store on or off, and BigEndian or LittleEndian byte order.

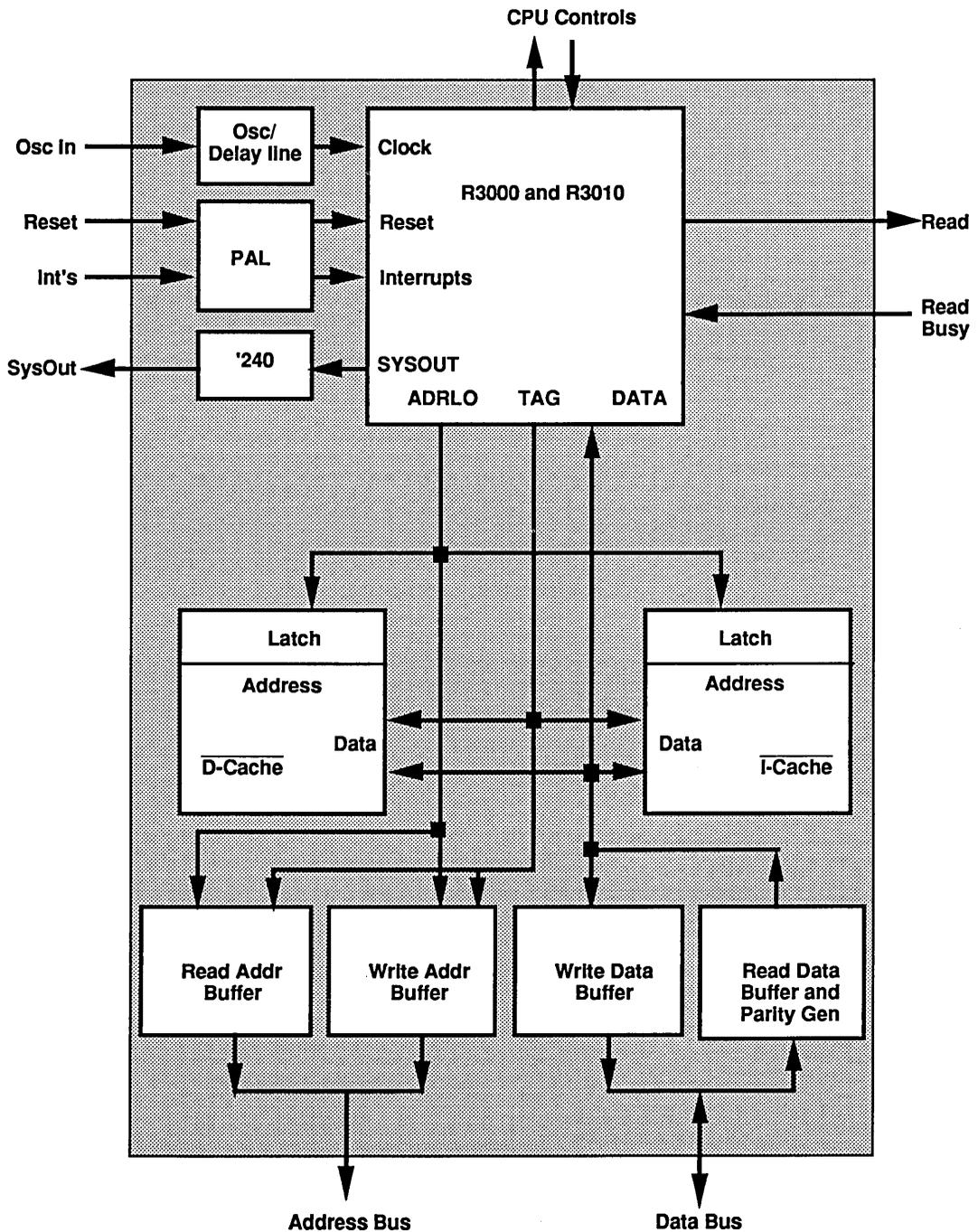
User Interrupts

Six user interrupt inputs are provided. Each of these is a negative-true signal, terminated with a 4.7K ohm pull-up load resistor on the module, so pins may be left unconnected if they are not used. The interrupt signals are clocked into an Interrupt Input Register on the module by the CPU clock SYSOUT. This ensures that the interrupt inputs to the R3000 are synchronized to its clock. One of the interrupts is reserved for use by the R3010 FPA; the other 5 are available for the user.

Buffered Outputs

The address and data lines coming out of the module are buffered, and can support substantial bus drive. All control signals except those coming directly from the R3000 or R3010 are also buffered.

FUNCTIONAL BLOCK DIAGRAM



SIGNALS PROVIDED ON MODULE PINS

Signal	Type	Functional Description
MD00-MD31	I/O	Memory data lines to/from main memory system.
PAR0-PAR3	I/O	Parity bits for data lines. Unconnected if on-board parity generation selected.
MA00-MA31	OUT	Memory address lines to main memory system. These are registered outputs.
CA2-CA3	OUT	Block refill counter outputs. These lines are normally used instead of MA02-MA03, since they are the outputs of the counter used to implement the 4-word block refill function.
RACT(0:1)	OUT	Positive-true outputs indicating the states of the R3000 outputs, ACCTYP(0:1), which identify the size of data transactions for read/write cycles. These are registered outputs, like MA00-MA31.
BACT2	OUT	Buffered ACCTYP(2) output from R3000, used to distinguish between cache and non-cache memory operations.
AOE#	IN	Negative-true input to enable the 3-state register output pins, MA00-MA31 and RACT(0:1).
UINT0-UINT5	IN	User interrupt inputs. Each has a 4.7K ohm pullup load resistor. UINT1 is reserved for R3010 FPA usage.
OSCIN	IN	Oscillator input clock signal. (2x clock rate).
MRES#	IN	Negative-true master reset input.
RESSW1-3	IN	Mode selection inputs used to determine R3000 setup options during reset initialization sequence. Each has a 4.7K ohm pullup load resistor. Jumpers or switches to ground select the desired options.
SYSOUT1-3	OUT	Buffered clock outputs for synchronizing external events. Each of these is an identical clock signal, representing the inverted form of the R3000 output, SYSOUT#.
MEMRD#	OUT	Direct negative-true output from R3000, used to indicate that a memory read cycle is in progress.
MEMWR#	OUT	Direct negative-true output from R3000, used to indicate that a memory write cycle is in progress.
RBSY	IN	Positive-true input used to request a memory read stall initiation and termination. This signal is normally held in its asserted state and de-asserted at the completion of CPU stalls.
WBSY#	IN	Negative-true input used to request a busy indication for subsequent memory write operations.
BLKR#	IN	Negative-true input used to request a block read sequence for read operations from main memory.
AEN#	IN	Negative-true input used to enable the clock for loading the address register.
CEN	IN	Positive-true input used to enable the increment of the block refill address counter for pins CA2-CA3.
PHOLD	IN	Positive-true input used to inhibit clocking of the read buffer. This signal is normally the complement of the CEN input.
WOE#	IN	Negative-true input used to enable the data output drivers for main memory write cycles.
WCTL#	IN	Negative-true input used to enable the clock to load data into the write data register for main memory write cycles.
CPC0	IN	Direct input to R3000 Processor, used to indicate the size of the data (block, word, byte, or other) for memory read cycles.
CPC1	OUT	Connection between the R3000 Processor and the R3010 FPA. Indicates the status of the conditional branch. This pin is provided for diagnostic purposes, only.
EXC#	OUT	Direct output from R3000, indicating the EXC# signal between the R3000 and the R3010.
RUN#	OUT	Negative-true output from the R3000, indicating that the R3000 is in its RUN state (not stalled).
BERR#	IN	Negative-true input to R3000 (with 4.7K ohm pullup), indicating a bus error in main memory.
FPA#	OUT	Negative-true output from R3010, indicating the presence of R3010 FPA on the module.
POE#	IN	Negative-true input with 4.7K ohm pullup resistor, used to enable the on-board parity generation logic. It is left unconnected if parity is to be handled by user system.
PERR#	OUT	Negative-true output which indicates a parity error on incoming data when on-board parity generation is not selected.
TAGV	OUT	Tag validity indicator, connected between R3000 and cache memory. Provided for diagnostic purposes, only.

RELATED PRODUCTS

Prototyping System

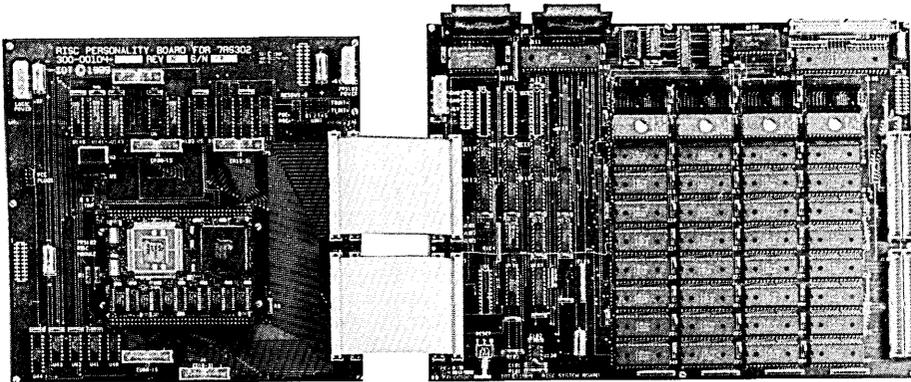
The 7RS101 module can be placed into immediate service using our flexible 7RS301 Prototyping Platform. The system includes two boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1Mb of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's Software Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP 16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



ORDERING INFORMATION

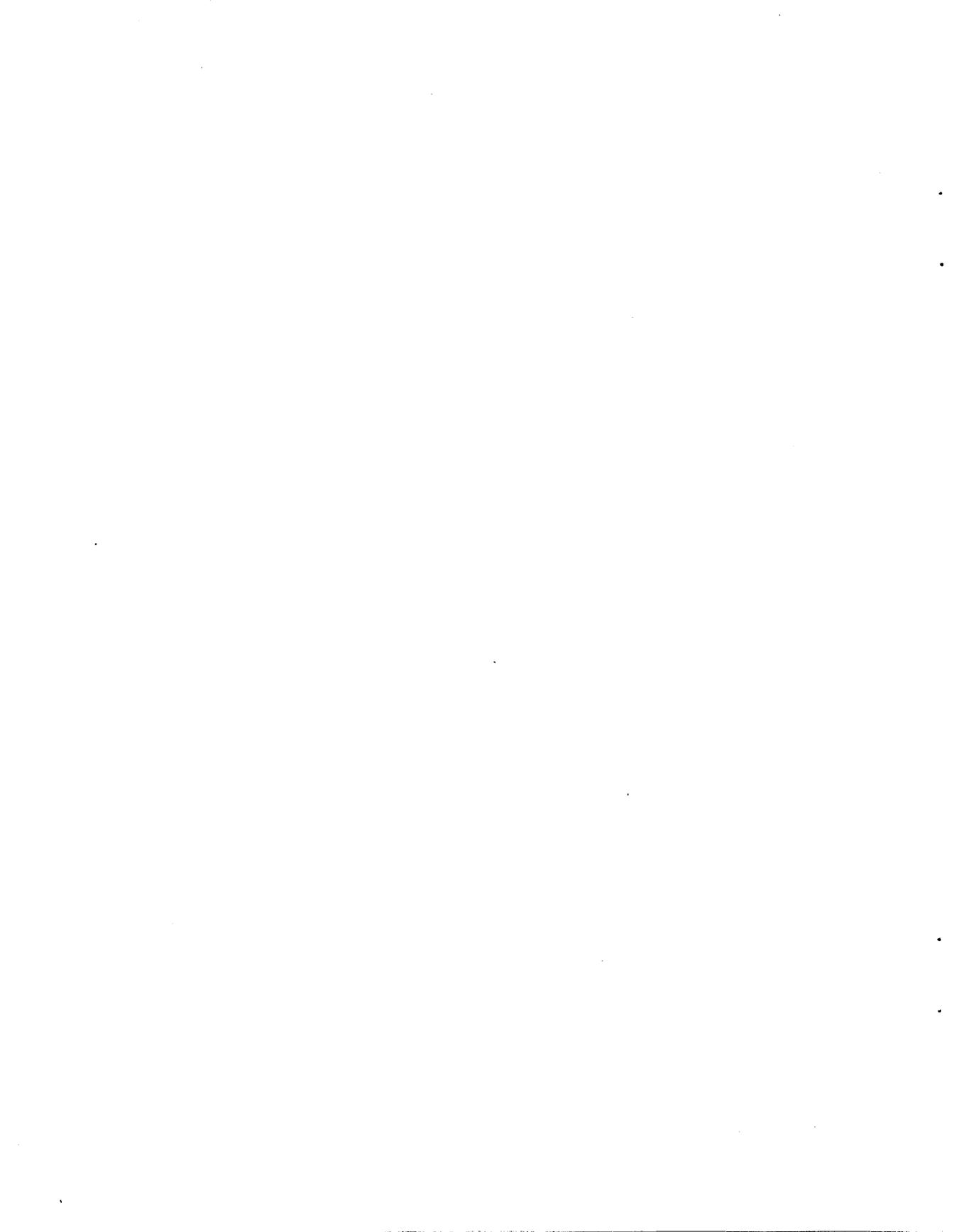
Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS101F16A	R3000	R3010	64K	64K	16 MHz	
7RS101F20A	R3000	R3010	64K	64K	20 MHz	
7RS101F25A	R3000	R3010	64K	64K	25 MHz	
7RS101F30A	R3000	R3010	64K	64K	30 MHz	
7RS101-16A	R3000	None	64K	64K	16 MHz	
7RS101-20A	R3000	None	64K	64K	20 MHz	
7RS101-25A	R3000	None	64K	64K	25 MHz	
7RS101-30A	R3000	None	64K	64K	30 MHz	

ADDITIONAL INFORMATION

For detailed technical specifications on this module refer to the 7RS101 Product Specification and User's Manual.

CUSTOM OPTIONS

Some features of the 7RS101 can be modified on special order. Contact your IDT sales office for information.





Integrated Device Technology, Inc.

R3000 CPU MODULES For Compact Systems

IDT7RS102

FEATURES:

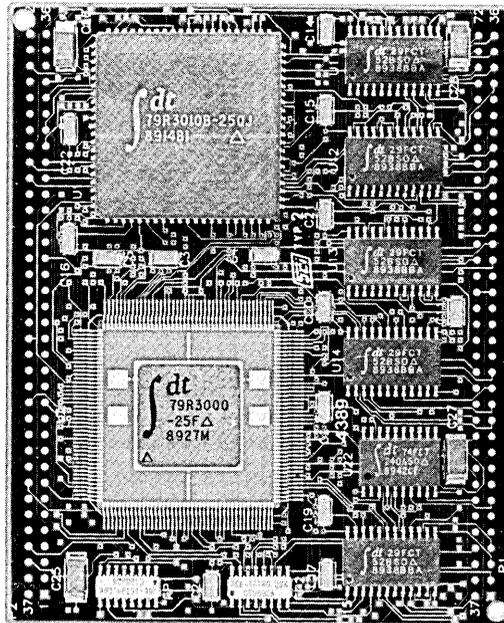
- Cache Size: 16K Instruction, 16K Data
- Extremely small size: 3.2" x 3.9"
- Processor Speeds up to 25 MHz
- Includes R3010 Floating Point Accelerator
- Single word Read and Write Buffers
- 100% burn-in and functional test at rated speed.

R3000 MODULE FOR GENERAL USE IN SMALL SYSTEMS:

The IDT7RS102 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 16 Kbytes each of data and instruction cache memory, a single word read buffer and a single word write buffer.

Cache misses are handled with single word read requests to memory, providing a simple interface to any type of main memory system.

The module is constructed using surface mount devices on a 3.2" by 3.9" epoxy laminate board, and is connected to the user's system via 144 pins located in two pin row regions on the board.



7RS102 Module. Actual Size 3.2" x 3.9"

ARCHITECTURAL HIGHLIGHTS

Small and Simple

The 7RS102 module is designed to be as small as possible and to provide a simple interface to the user's system. The 16K caches are the smallest useful for most systems.

R3010 Floating Point Accelerator

The R3010 Floating Point Accelerator (FPA) is included as an integral part of the module. It operates in conjunction with the R3000 RISC Processor and greatly improves the system performance by expanding the instruction set to include very fast floating point capabilities. All timing and control connections are on the module and are completely transparent to the user.

Clock Generation

The clock inputs to the 7RS102 are the direct connections to the clocks for both the R3000 and the R3010. These clocks must be generated in the user system and applied to the module.

Cache Memory

Cache memory is provided on the module for a capacity of 16K bytes for each of the two R3000 cache memory systems (Instruction Cache and Data Cache). Memory operations which require main memory data transfers are conveniently handled by means of a variety of on-board control signals.

Cache read miss operations are handled as single-word fetch and cache update. Non-cache read operations (such as I/O reads) are indicated by means of control signals and are easily accommodated by the user.

Parity Generation

The R3000 Processor requires incoming data words to consist of 32 bits of data and a 4-bit parity code. Each of the 4 parity bits applies to a particular byte in the word. The required parity is even. The user system is required to generate parity for incoming data to the module and may optionally check parity for data being passed to main memory.

Address and Data Buffers

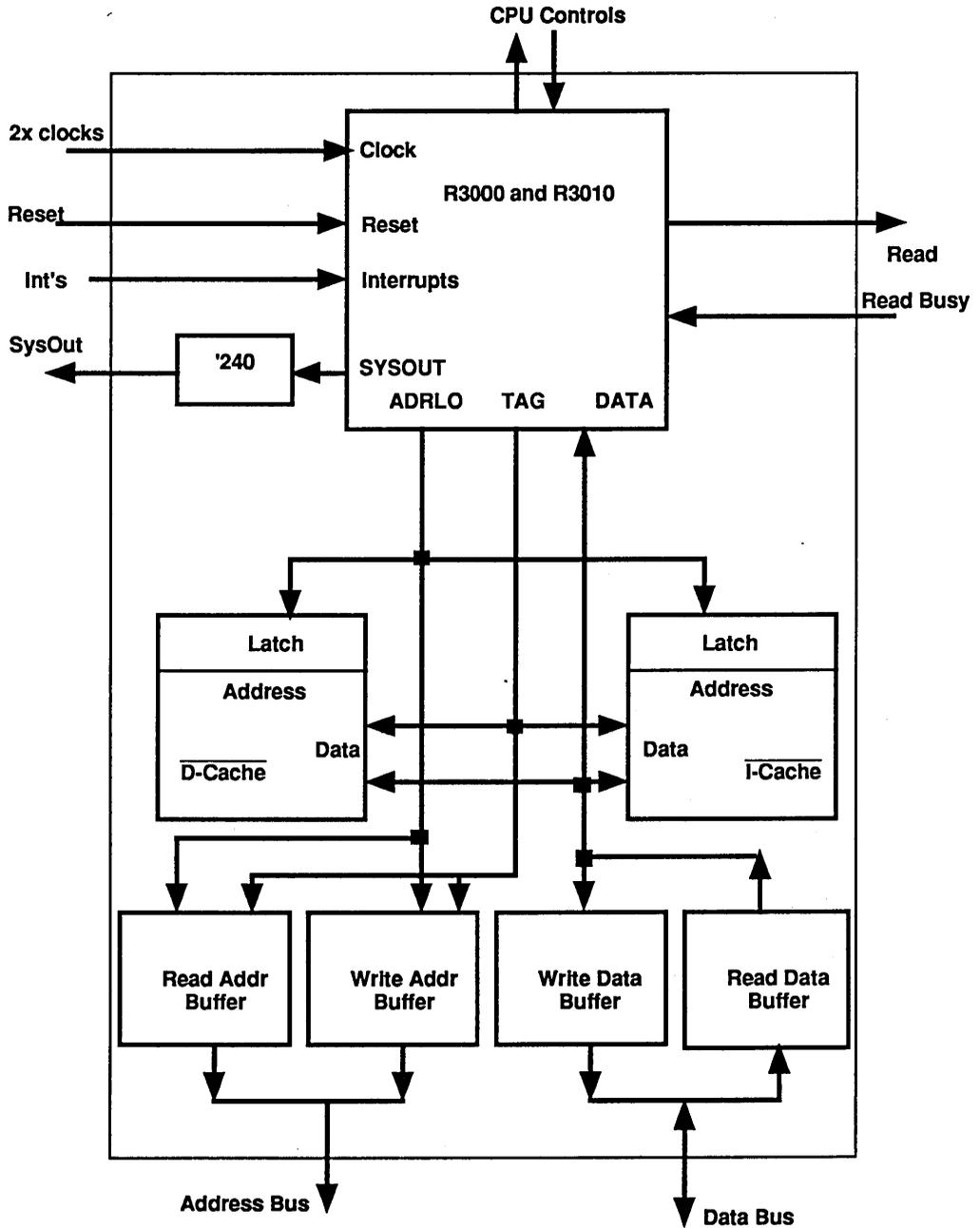
The address and data lines coming out of the module are buffered and can support substantial drive requirements. The address pins are direct outputs from registers and include the signals MACT0-MACT2. The three-state output drivers may be disabled by de-asserting the output enable control line, AOE. This is not normally done, but is provided as a feature for systems which may require it.

The data pins are driven by Bi-directional Registers. Enable/disable control of the three-state output drivers is accomplished with the signal, DOE. Memory write cycles utilize a single-word write buffer on the module which permits the R3000 Processor to continue running while data is being written into main memory. USER INTERRUPT INPUTS

R3000 User Interrupts

Six user interrupt inputs are provided, INT0-INT5. Each of these is a negative-true signal, terminated with a 10K ohm pullup load resistor on the module. In this way, the pin may be left unconnected if it is not to be used. The interrupt signals are connected directly to the interrupt pins of the R3000 Processor. INT1 is a reserved pin on this version of the module and is required for use by the R3010 FPA. As a result, it may not be used and must be left unconnected.

FUNCTIONAL BLOCK DIAGRAM



SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
MD00-MD31	I/O	Memory data lines to/from main memory system.
MPAR0-MPAR3	I/O	Parity bits for data lines. Parity must be supplied to the 7RS102 module, in accordance with R3000 requirements.
MA00-MA31	OUT	Memory address lines to the main memory system. These are registered outputs.
MACT0-MACT2	OUT	Positive-true outputs indicating the states of the R3000 outputs, ACCTYP(0:2), which identify the nature of the data transactions for read/write cycles. These are registered outputs, like MA00-MA31.
MTAGV	OUT	Registered TAGV output from R3000.
ACCTYP2	OUT	Unbuffered ACCTYP(2) output from R3000, used to distinguish between cache and non-cache memory operations.
AOE#	IN	Negative-true input to enable the three-state register output pins, MA00-MA31, MACT0-MACT2, and MTAGV.
INT0-INT5	IN	Interrupt inputs. Each has a 10K ohm pullup loadresistor. INT1 is reserved for R3010 FPA usage.
CLK2XPHI	IN	Clock input for R3000 and R3010. Timings must conform to R3000 specifications.
CLK2XRD	IN	Clock input for R3000 and R3010. Timings must conform to R3000 specifications.
CLK2XSYS	IN	Clock input for R3000 and R3010. Timings must conform to R3000 specifications.
CLK2XSMP	IN	Clock input for R3000 and R3010. Timings must conform to R3000 specifications.
MRES#	IN	Negative-true master reset input. Connects directly to R3000 RES# input pin.
SYSOUT1-3	IN	Buffered clock outputs for synchronizing external events. Each of these is an identical clock signal, representing the inverted form of the R3000 output, SYSOUT#.
MEMRD#	OUT	Direct negative-true output from R3000, used to indicate that a memory read cycle is in progress.
MEMWR#	OUT	Direct negative-true output from R3000, used to indicate that a memory write cycle is in progress.
RBSY	IN	Positive-true input used to request a memory read stall initiation and termination. This signal is normally held in its asserted state and deasserted at the completion of stalls.
WBSY#	IN	Negative-true input used to request a busy indication for subsequent memory write operations.
ACE#	IN	Negative-true input used to enable the clock for loading the address register.
RDEN#	IN	Negative-true input used to enable the clock for loading the data register for memory read cycles..
DOE#	IN	Negative-true input used to enable the three-state data outputs, MD00-MD31 and MPAR0-MPAR3.
WCTL#	IN	Negative-true input used to enable the clock to load data into the write data register for main memory write cycles.
CPC0	IN	Direct input to the R3000, used to indicate the size of the data (block, word, byte, or other) for memory read cycles.
CPC1	OUT	Connection between the R3000 Processor and the R3010 FPA, indicating the status of the conditional branch. This pin is provided for diagnostic purposes, only.
CPC2, CPC3	I/O	Direct connections to R3000 pins.
EXC#	OUT	Direct output from R3000, indicating the EXC# signal between the R3000 and the R3010.
RUN#	OUT	Negative-true output from the R3000, indicating that the R3000 is in its RUN state (not stalled).
BERR#	IN	Negative-true input to R3000, used to indicate a bus error in main memory.
FPA#	OUT	Negative-true output from R3010, indicating the presence of R3010 FPA on the module.

RELATED PRODUCTS

Prototyping System

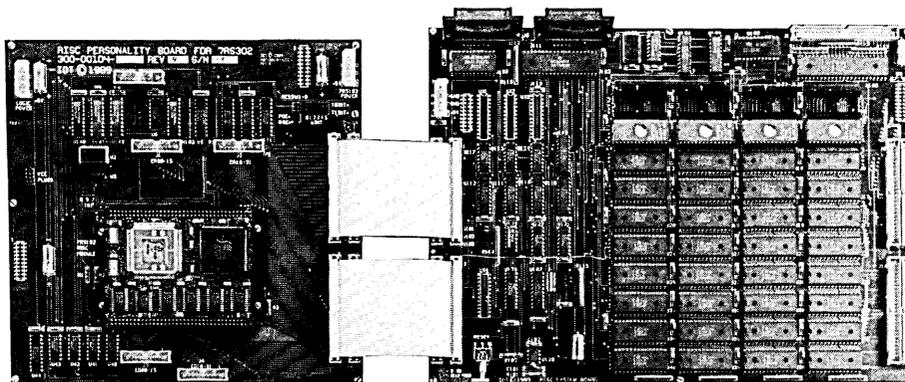
The 7RS102 module can be placed into immediate service using our flexible 7RS302 Prototyping Platform. The system includes two boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1Mb of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's IDT/sim System Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP 16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



Module Prototyping Platform.
The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

ORDERING INFORMATION

Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS102-16A	R3000	R3010	16K	16K	16 MHz	
7RS102-20A	R3000	R3010	16K	16K	20 MHz	
7RS102-25A	R3000	R3010	16K	16K	25 MHz	
7RS102F16A	R3000	R3010	16K	16K	16 MHz	
7RS102F20A	R3000	R3010	16K	16K	20 MHz	
7RS102F25A	R3000	R3010	16K	16K	25 MHz	

ADDITIONAL INFORMATION

For more details on the 7RS102 module, refer to the 7RS102 Technical Specification and User's Manual.





Integrated Device Technology, Inc.

R3000 CPU MODULES For Compact Systems

IDT7RS103

FEATURES:

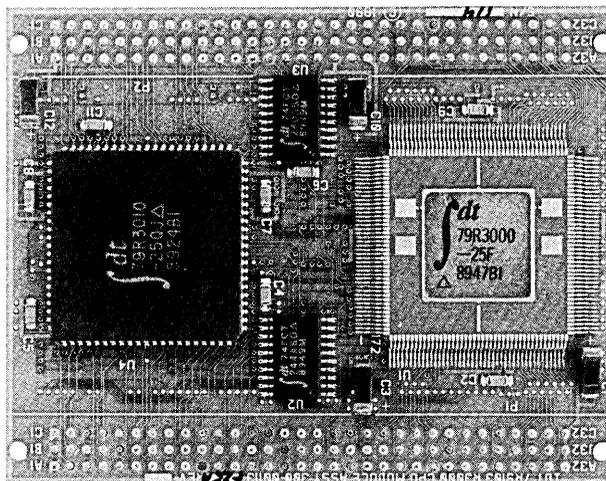
- Cache Size: 16K Instruction, 16K Data
- Extremely small size: 2.9" x 3.7"
- Processor Speeds up to 25 MHz
- Includes R3010 Floating Point Accelerator
- On-board delay line to create R3000 clocks.
- 100% burn-in and functional test at rated speed.

R3000 MODULE FOR COMPACT HIGH PERFORMANCE SYSTEMS:

The IDT7RS103 is a reduced instruction set computer (RISC) CPU SubSystem, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, optionally the R3010 Floating Point Accelerator, and 16K bytes each of data and instruction cache memory. The delay line to generate the three R3000 2x clock signals is included on the module, so the module can be driven from a single 2x clock.

Externally, the user system supplies the R3000 control signals and the read and write buffers.

The module is constructed using surface mount devices on both sides of a 2.9" x 3.7" epoxy laminate board, and is connected to the user's system via 192 pins located in two pin row regions on the board.



7RS103 Module. Actual Size 2.9" x 3.7"

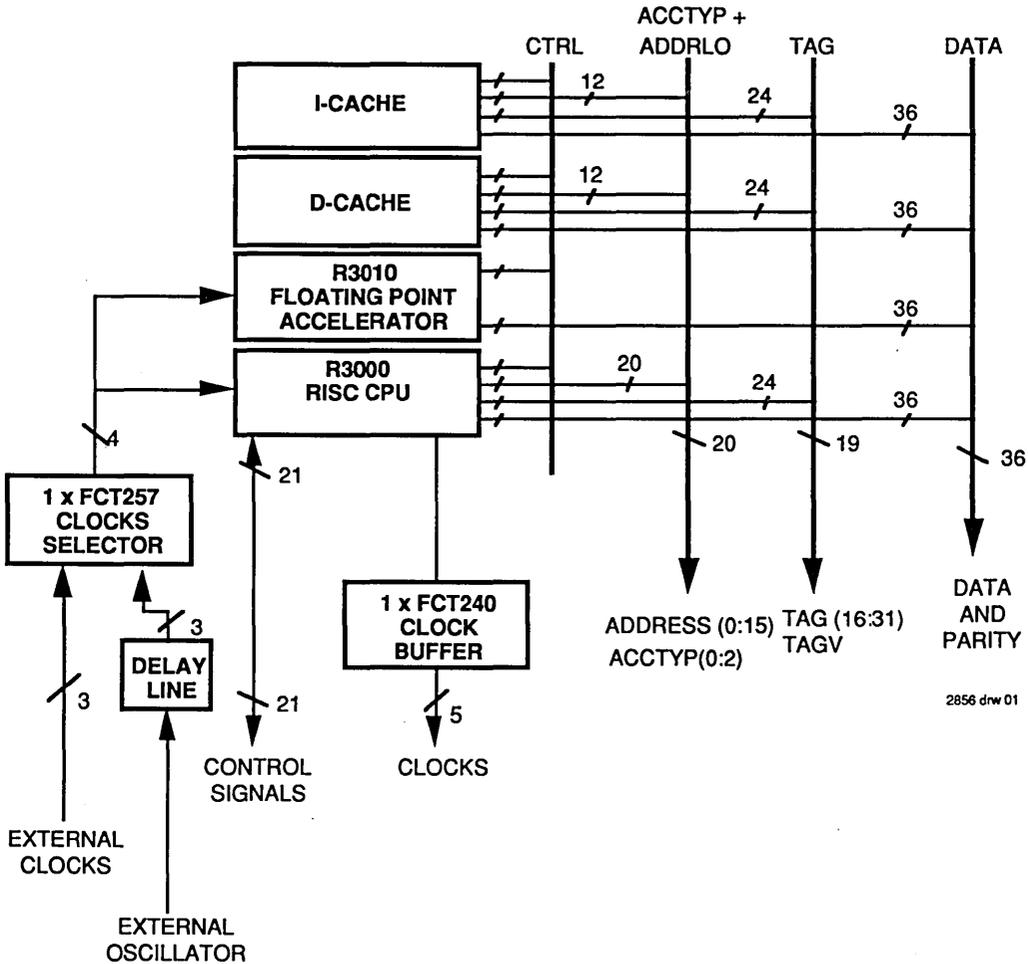
ARCHITECTURAL HIGHLIGHTS:

The Minimal Module

The 7RS103 is designed to provide an R3000 RISC SubSystem in as small a space as possible. It includes only the CPU (and FPA), cache memories, and a delay line to generate the 2x clocks to the R3000. The read and write buffers and control logic are handled off the module by the user's system. This makes the module ideal for use with ASICs or other unique implementations of main memory interface.

The R3000 timing and control signals are brought directly off the module. The R3000 data sheet should be consulted for all the timing specifications. One of the interrupt inputs is required by the R3010 on versions that include the FPA device.

FUNCTIONAL BLOCK DIAGRAM



SIGNALS PROVIDED ON MODULE PINS

Pin Name	Type	Functional Description
D00-D31	I/O	Memory data lines to/from main memory system.
DP0-DP3	I/O	Parity bits for data lines. Parity must be supplied to the 7RS103 module, in accordance with R3000 requirements.
A00-A15	OUT	Address lines from the R3000. (lower 16 bits)
T16-T31	OUT	Tag lines from the R3000. (higher 16 bits)
ACCTYP0-	OUT	Positive-true outputs indicating the states of the R3000 ACCTYP2 outputs, ACCTYP(0:2), which identify the nature of the data transactions for read/write cycles.
TAGV	OUT	Connection between cache and R3000.
INT0-INT5	IN	Interrupt inputs. Each has a 10K ohm pullup load resistor.
EXTOSC	IN	External oscillator input (Needed when using on-board delay line)
ECLKHPI		
ECLKRD SMP		
ECLKSYS	IN	The 2x Clock inputs for R3000 and R3010. Timings must conform to R3000 specifications. (Needed when not using on board delay line)
MRES#	IN	Negative-true master reset input. Connects directly to R3000 RES# input pin.
BSYSOUTA-	OUT	Buffered clock outputs for synchronizing external events.
BSYSOUTD		Each of these is an identical clock signal, representing the inverted form of the R3000 output, SYSOUT#.
BSYSOUT#	OUT	Buffered R3000 clock output, SYSOUT# for synchronizing external events. Non-inverted form of SYSOUT#.
MEMRD#	OUT	Direct negative-true output from R3000, used to indicate that a memory read cycle is in progress.
MEMWR#	OUT	Direct negative-true output from R3000, used to indicate that a memory write cycle is in progress.
RBSY	IN	Positive-true input used to request a memory read stall initiation and termination. This signal is normally held in its asserted state and deasserted at the completion of stalls.
WBSY#	IN	Negative-true input used to request a busy indication for subsequent memory write operations.
CPC0	IN	Direct input to the R3000, used to indicate the size of the data (block, word, byte, or other) for memory read cycles.
CPC1	OUT	Connection between the R3000 Processor and the R3010 FPA, indicating the status of the conditional branch. This pin is provided for diagnostic purposes, only.
CPC2, CPC3	I/O	Direct connections to R3000 pins.
EXC#	OUT	Direct output from R3000, indicating the EXC# signal between the R3000 and the R3010.
RUN#	OUT	Negative-true output from the R3000, indicating that the R3000 is in its RUN state (not stalled).
BERR#	IN	Negative-true input to R3000, used to indicate a bus error in main memory.
FPA#	OUT	Negative-true output indicating the presence of R3010 FPA on the module.
XEN#	OUT	Direct negative true output from the R3000. Used for read buffers output enable.
FPINT#	OUT	Negative-true R3010 interrupt request.

ORDERING INFORMATION

Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS103-16A	R3000	NONE	16K	16K	16 MHz	
7RS103-20A	R3000	NONE	16K	16K	20 MHz	
7RS103-25A	R3000	NONE	16K	16K	25 MHz	
7RS103F16A	R3000	R3010	16K	16K	16 MHz	
7RS103F20A	R3000	R3010	16K	16K	20 MHz	
7RS103F25A	R3000	R3010	16K	16K	25 MHz	
7RS103N44A16A	R3000A	NONE	16K	16K	16 MHz	
7RS103N44A20A	R3000A	NONE	16K	16K	20 MHz	
7RS103N44A25A	R3000A	NONE	16K	16K	25 MHz	
7RS103F44A16A	R3000A	R3010A	16K	16K	16 MHz	
7RS103F44A20A	R3000A	R3010A	16K	16K	20 MHz	
7RS103F44A25A	R3000A	R3010A	16K	16K	25 MHz	

MORE INFORMATION

For more information on this module, ask your IDT sales office for the Technical Specification and User's Manual.



Integrated Device Technology, Inc.

R3000 CPU MODULES For High Performance and MultiProcessor Systems

IDT7RS107

FEATURES:

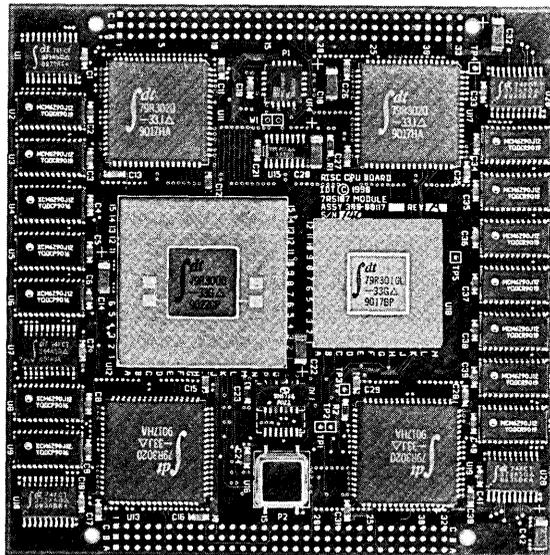
- Cache Size: 64K Instruction, 64K Data
- Processor Speeds up to 33 MHz
- Includes R3010 Floating Point Accelerator
- 1-word Read Buffer; 4-word Write Buffer
- Supports R3000 Multiprocessor Features
- Entire I-Cache can be invalidated with external cache reset signal
- Eight-word block refills
- On-board oscillator, delay line, and reset circuitry.
- 100% burn-in and functional test at rated speed.

R3000 MODULE FOR HIGH PERFORMANCE CPUS AND MULTIPROCESSOR SYSTEMS:

The IDT7RS107 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 64 Kbytes each of data and instruction cache memory, a single word read buffer and a four-word write buffer. Clock generation, reset, control and interrupt functions are included on the module to simplify the remainder of the system design.

The 107 module is designed to support the R3000's multiprocessor features. Data in the D-cache can be invalidated by the R3000 CPU. It is also possible to invalidate the entire contents of the I-cache in a single cycle by using an external cache reset signal.

The module is constructed using surface mount devices on a 5.2" by 5.2" epoxy laminate board, and is connected to the user's system via 195 pins located in two pin row regions on the board.



7RS107 Module. Actual Size 5.2" x 5.2"

ARCHITECTURAL HIGHLIGHTS

Uses R3020 Write Buffers

R3020 chips are used on the module to provide a "smart" four-deep write buffer between the CPU and external memory. These devices store data and addresses for up to four write requests to main memory, and handle the handshaking with the memory controller. The R3020s support features such as byte gathering (combining multiple byte writes to the same address in the buffer into a single write) and address matching (a read or write to an address already in the write buffer will be detected so the user software can take appropriate action). The R3020's Match signals are OR'ed on the module to produce a single output, labeled CONFLICT.

Resettable Instruction Cache

The 7RS107 module permits invalidation of the entire instruction cache via a "cache reset" pin on the module. This feature is used to wipe the cache clean when the a block of instructions in main memory have been changed by a DMA operation. It is usually much faster than invalidating each affecting tag individually.

Multiprocessor Invalidate In Data Cache

The module supports the R3000's multiprocessor cache invalidate feature, so that data cache coherency can be maintained when data held in the cache is altered externally. The R3000's MP Stall and MP Invalidate signals are available as pins on the module. The user's system stalls the processor and then provides an address to the module while signaling MP Invalidate. The module stores the address in a latch and applies it to the cache at the right time for the R3000 to invalidate the referenced tag.

Eight-Word Block Refill

The module refills both the instruction and data caches from memory in eight-word blocks. Following a cache miss, the processor will request a memory read at the missed address and wait for a data ready acknowledgement. When an acknowledge is received, the processor will load eight words into cache on eight successive clock cycles. The memory interface must supply the correct eight words (address A4A3A2 = 0 to 7) at the processor's speed, 40 ns intervals for a 25 MHz system. Interleaved memory is usually the best way to support this requirement. The processor's CPC0 pin, available as a pin on the module, can be used to over-ride the block refill on data, but instructions refills must always be in 8-word blocks. The processor performs instruction streaming during the refill.

On-board Oscillator and Delay Line

All the clock generation circuitry required by the R3000 system is on the module. A jumper can be used to select between the on-board crystal oscillator or an external oscillator input. A delay line on the module is used to set the timing for register strobes and other critical signals relative to the R3000 clock. The R3000 clock output "SYSOUT" is made available to the user system through eight pins on the module, each independently buffered.

R3000 Reset and Initialization Logic

The initialization logic for the R3000 CPU is contained on the module. A "Cold Reset" pin on the module starts the required 15 ms reset signal to the CPU, and then provides the initialization vectors during the last few cycles. A second reset pin is provided to reinitialize the CPU without repeating the 15 ms delay. The R3000 is initialized to "Big-Endian" operation.

Five User Interrupt Lines

Five pins on the module are used for user interrupt inputs. The user interrupts are synchronized in registers on the module before being sent to the R3000. Interrupt 2 is used for the Floating Point Accelerator, if present.

External R3000 Condition Code Pin

The R3000 input CPC0 is available as a pin on the module. During initialization, this pin is programmed as a Condition Code test pin, so the R3000 can do a Test and Branch in a single cycle based on its state. During read stalls, the pin determines whether a single word or 8 words will be read. Reads into the instruction cache must always be block refills.

TYPICAL APPLICATIONS

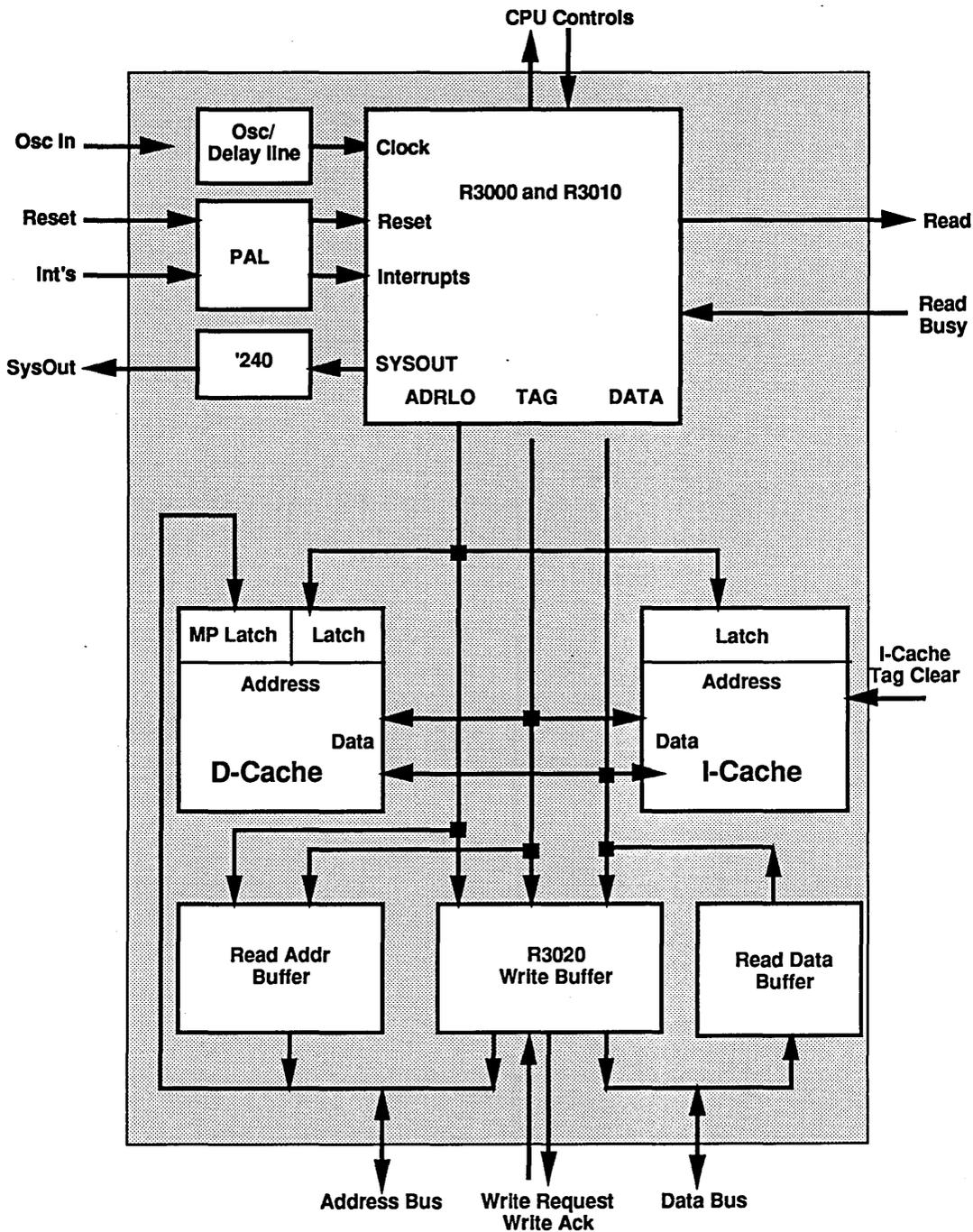
The 7RS107 module is designed for applications that run complex operating systems, such as UNIX™, or that need outside control of cache memory contents, such as multiprocessor systems.

The module supports the R3000's ability to invalidate entries in the data cache, allowing multiple processor systems to maintain cache coherency.

The module is offered with the maximum possible cache sizes (64K each) that can be supported by the R3000 in a multiprocessor configuration. These sizes are well suited to running UNIX at very high instruction rates as well.

The R3020 Write Buffer is used to provide a four-word deep write buffer, which is ideal for most UNIX systems.

FUNCTIONAL BLOCK DIAGRAM



SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
MA0...MA31	I/O	32-bit address from the module to external memory. This is an output from the 3020 Write Buffer except during the MP Invalidate function, when it is the input to the MP cache address latch.
MD0...MD31	I/O	32-bit data bus between the module and external memory. Driven from the 3020 Write Buffer during writes; input to the Read Data Buffer during reads.
BACT0,1,2	O	The three R3000 AccType status signals, driven from the 3020 Write Buffer during writes and from a latch during reads.
MDP0...MDP3	I/O	The four parity bits for the MD data. Output during writes and input during reads.
CP_CpCond0, 2, 3	I	The three flag inputs to the R3000 CPU. CPC0 is used during read stalls to control block refill of the data cache. (The instruction cache must always be block refilled.) CPC2 and CPC3 are the MP stall and invalidate controls.
ALOE	I	Data Cache Address Latch Output Enable. When LOW, enables the output of the latch holding the data cache address supplied by the R3000. It should be LOW at all times except when the MP Latch is being used to invalidate a cache address.
MPALOE	I	Data Cache MP Address Latch Output Enable. This input is used to enable the output of the latch holding the address supplied by the user system during an MP stall cycle. It should be enabled (LOW) only during the MP invalidate operation.
BSYSOUT2...9	O	Eight buffered inverted copies of the R3000 signal "SYSOUT" for use in the user's system.
UINT0,1,3,4,5	I	Interrupt inputs to the R3000. These signals are synchronized to SYSOUT on the module. R3000 interrupt 2 is used for the Floating Point Accelerator.
BRESET	O	Buffered copy of the reset signal created on the module to reset the CPU. LOW during Reset.
WB_WbFull	O	Write Busy. Status signal created by the R3020 write buffer. Goes LOW to indicate the buffer is full.
CPU_BusError	I	Input to the R3000 indicating a bus error has occurred.
RESETC	I	Cold Reset to the module. The module creates a 15 ms long reset to the R3000 and executes the R3000 initialization sequence when this pin goes LOW.
FP_FpPresent	O	This signal can be used to detect the presence of an FPA on the module. To be used, it must be connected to a 4.7K pullup resistor. The pin will be LOW if the FPA is present.
RESETI	I	Active LOW asynchronous clear to the I-Cache Tag RAMS. Sets the entire I-Cache invalid.
WB_OutEn	I	Write Buffer Output Enable. When LOW, turns on the outputs of the R3020 write buffers.
WB_Request	O	Output from the R3020 to indicate that there is data in the buffer to be written to memory. Active LOW
WB_Acknowledge	I	Input to the R3020 to indicate data has been written into memory.
CONFLICT	O	The OR of all the R3020 Match signals; indicates the address on the R3020 inputs matches one of the addresses currently in the write buffer.
RABOE	I	Read Address Buffer Output Enable. When LOW, turns on outputs of the buffers containing the read address.
RDBCE	I	Read Data Buffer Clock Enable. When LOW, enables the clock (SYSOUT) to the Read Data Buffers.
READ	O	Status signal output. LOW during reads.
RABLE	I	Read Address Buffer Latch Enable. When HIGH, enables the Read Address Buffer latches.
WB_LatchErrAddr	I	Latch Error Address input to the R3020.
WB_EnErrAddr	I	Enable Error Address input to R3020.
CP_MemRd	O	R3000 output signal. When LOW, there is a request for a read from external memory.
CP_RdBusy	I	Read Busy. Input to the R3000 to indicate acknowledgment of the MEMRD request.
RESETX	I	Additional Reset command. Same as RESETC, but does not go through the 15 ms delay. Can be used to re-initialize the R3000 when power is on.

RELATED PRODUCTS

Prototyping System

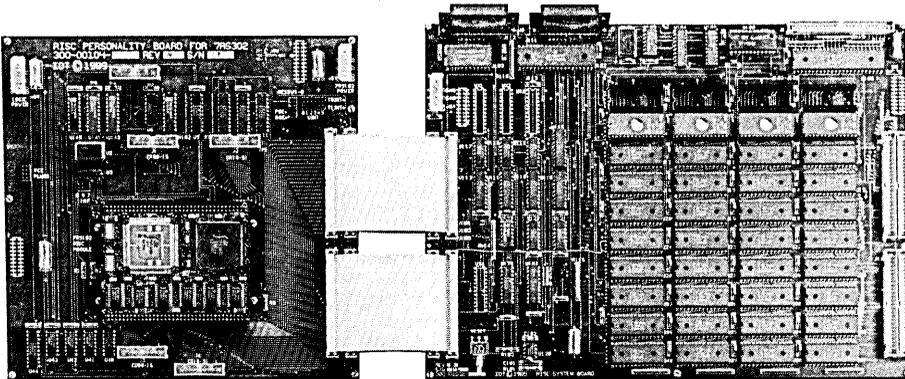
The 7RS107 module can be placed into immediate service using our flexible 7RS307 Prototyping Platform. The system includes two boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1Mb of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's Software Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP 16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



A Module Prototyping Platform.

The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

ORDERING INFORMATION

Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS107-16A	R3000	NONE	64K	64K	16 MHz	
7RS107-20A	R3000	NONE	64K	64K	20 MHz	
7RS107-25A	R3000	NONE	64K	64K	25 MHz	
7RS107-33A	R3000	NONE	64K	64K	33 MHz	
7RS107F16A	R3000	R3010	64K	64K	16 MHz	
7RS107F20A	R3000	R3010	64K	64K	20 MHz	
7RS107F25A	R3000	R3010	64K	64K	25 MHz	
7RS107F33A	R3000	R3010	64K	64K	33 MHz	
7RS107N66A16A	R3000A	NONE	64K	64K	16 MHz	
7RS107N66A20A	R3000A	NONE	64K	64K	20 MHz	
7RS107N66A25A	R3000A	NONE	64K	64K	25 MHz	
7RS107N66A33A	R3000A	NONE	64K	64K	33 MHz	
7RS107F66A16A	R3000A	R3010A	64K	64K	16 MHz	
7RS107F66A20A	R3000A	R3010A	64K	64K	20 MHz	
7RS107F66A25A	R3000A	R3010A	64K	64K	25 MHz	
7RS107F66A33A	R3000A	R3010A	64K	64K	33 MHz	

CUSTOM OPTIONS

Some features of the 7RS107 can be modified by special order. Contact your IDT sales office for details.

Software modifications include: initialization mode for the R3000, endian option, size of block refill, instruction streaming option.

Manufacturing options include pin length, style, and plating; special marking; additional burn-in, and socketing of the CPU and/or FPA.



Integrated Device Technology, Inc.

PROTOTYPING PLATFORM For Any IDT RISC CPU Module

IDT7RS300 Series

FEATURES:

- Use with any module to form a complete R3000 based computer system.
- Includes 1024K bytes of static RAM main memory, and 256K bytes of EPROM
- IDT's System Integration Manager in EPROM. Supports downloading software, single step, and other debugging needs.
- Two RS232C serial ports (68681), parallel port (IDT7134 dual-port RAM), and programmable interval timer (8254).
- Address bus, data bus, and all necessary control signals provided on connectors (four 50-pin IDCs) to permit user expansion.
- Direct connections to HP 16500 Logic Analyzer
- Fastest way to get an R3000 system up and running.

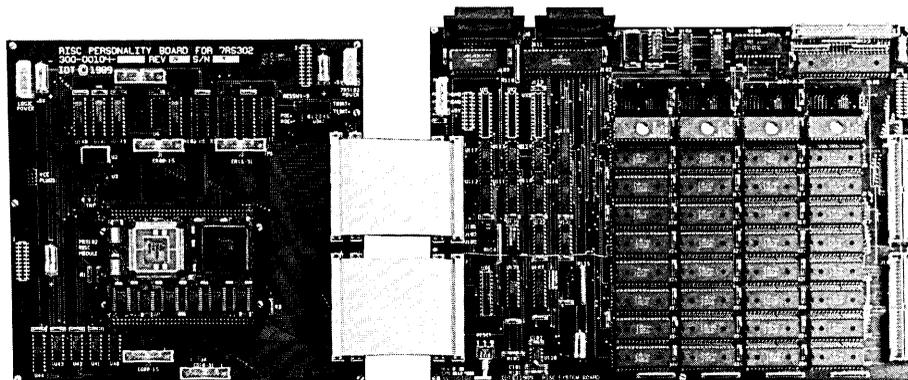
DESCRIPTION:

The IDT7RS300 series Prototyping Platforms consist of two separate PC boards which connect together by means of convenient ribbon cables to form the total system.

The System Board contains the non-CPU system functional units: static RAM main memory, EPROM monitor, two serial ports, a parallel port (utilizing an IDT7134 Dual-Port RAM), a free-running programmable timer, and expansion connectors to permit additional hardware to be added. It is designed to be placed on a flat table-top surface. Standoffs are provided for physical support. Access to all components on the board is readily available with this packaging approach. The Personality Board contains control logic and a socket for the a particular RISC module. The Personality Board is also designed for table-top use.

The EPROM on the System Board contains IDT's System Integration Manager (IDT/sim), a powerful tool for downloading software and debugging both hardware and software. Drivers can easily be added to support other I/O devices or changes in I/O addresses.

Software can be downloaded into the board from a MIPS machine, from an IDT MacStation development system, or from a PC running IDT's Cross Development Software.



The 302 version of the Prototyping Platform.
The System Board is on the right; the personality card and 102 module on the left.

FLEXIBLE PROTOTYPING PLATFORMS

System Description

The 7RS300 series RISC Prototyping Platform is designed to simplify the initial prototyping of both hardware and software for systems using one of the IDT RISC SubSystem Modules. The System Board is very general, and is the same in all of the 300 series Platforms. It contains basic control logic, mostly in PALs, 1 megabyte of static main memory, 256K of EPROM, a counter/timer, and I/O ports. Static RAM is used for main memory to provide the simplest interface to the module. The EPROM contains IDT's System Integration Manager in about 80K; the rest is available for user software.

The System Board connects to a personality board for the module through a pair of ribbon connectors. Each module architecture uses a different personality board. The personality board provides such features as clock generation, R3000 reset and initialization, read and write buffers, etc., to the extent that they are not already on the module. The personality board also contains five 20-pin plugs that can be directly connected to an HP 16500 series Logic Analyzer, and provides a uniform interface to the System Board.

System Board Hardware

The System Board is powered by a single 5 volt supply connected to a plug on the board. The plug conforms to the standard used for PCs, so an ordinary inexpensive PC power supply works easily with the board. A terminal can be connected to one of the RS-232 ports to act as the terminal for the Software Integration Manager. The other serial port is generally used to download software from some host system. Alternatively, there is an 8-bit wide parallel port built using dual port RAM that can be used for higher speed download.

Four 50-pin IDC (3M) connectors are configured for connecting additional hardware to the System Board. They contain the following signals:

- 32 bits of address
- 32 bits of data, and 4 parity bits
- SYSOUT (buffered clock from the R3000)
- RESET# (copy of the R3000's Reset signal)
- Parity and Address output enables from the address and data registers (to permit tri-stating other data onto these lines).
- Six interrupt lines to the R3000. These are registered or not, depending on the module.
- The four byte Write Enable signals.
- Five decoded chip select outputs from the upper 16 bits of address (1FE6 through 1FEE).
- MEMRD#, used to enable output devices in the expansion system during data read cycles.
- Auxillary input and output signals from the 68681 dual UART
- MREQ# and XACK# handshaking signals for controlling the timing of data transfers.

Personality Board Hardware

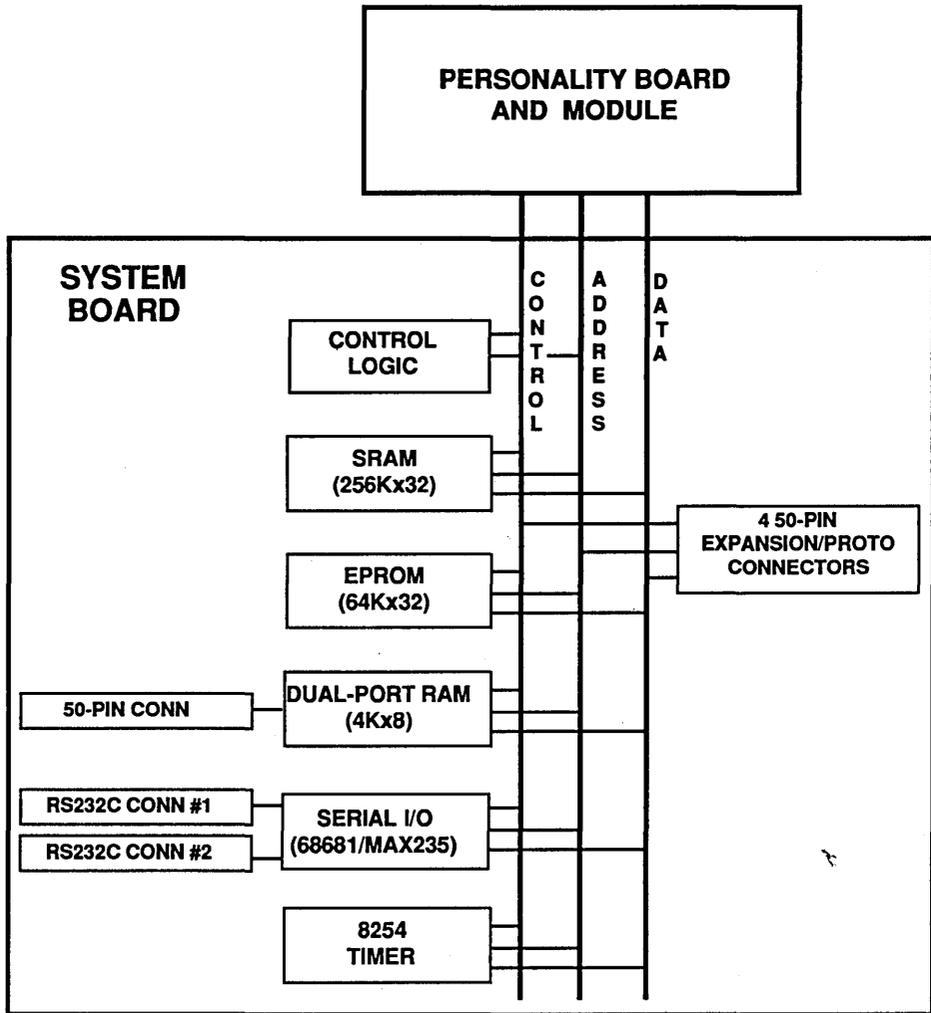
The personality board connects to the system board through two ribbon connectors. It contains a cut out area and plugs which accept the appropriate module. There are two five-volt power connectors, again using standard PC plugs. One power supply is for the personality card, the other for the module.

Five connectors are pre-wired to connect the modules signals to an HP logic analyzer. Because of the speed of the signals in the R3000 system, the connectors are placed on the slow side of the read/write buffers, so for disassembly and trace purposes, the R3000 must be run uncached.

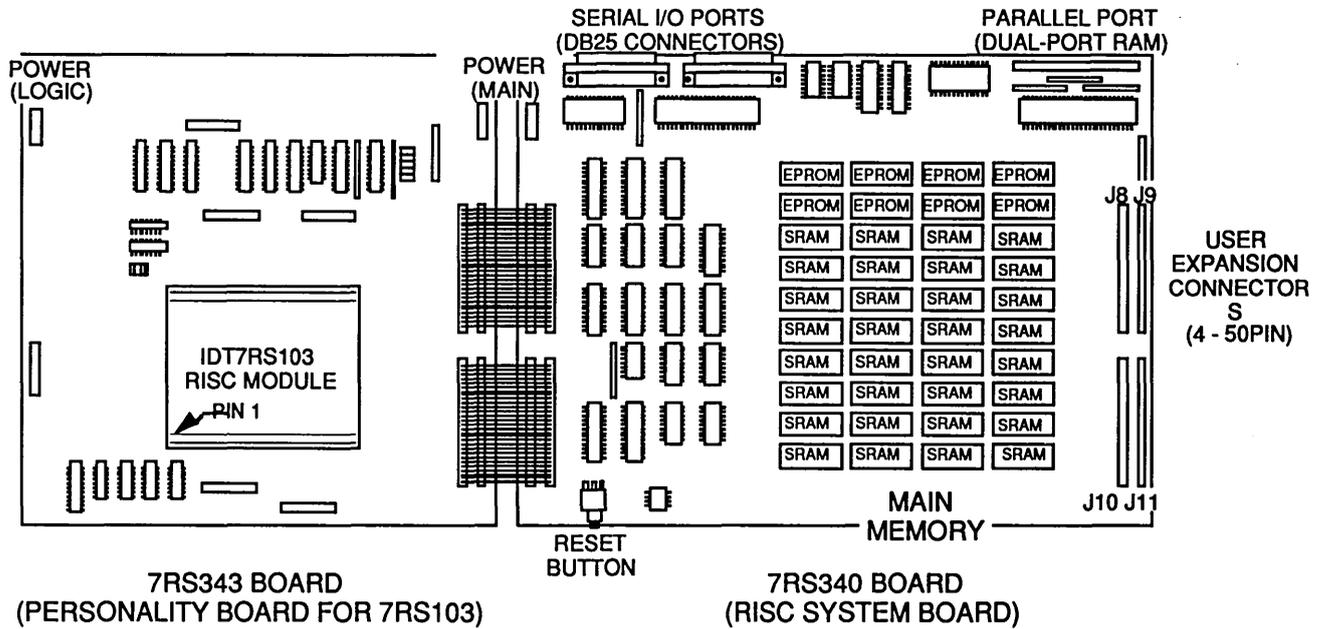
Software Included

The System Board contains IDT's System Integration Manager (IDT/sim) in EPROM.

FUNCTIONAL BLOCK DIAGRAM



Block Diagram of the 7RS300 Series Prototyping Platforms



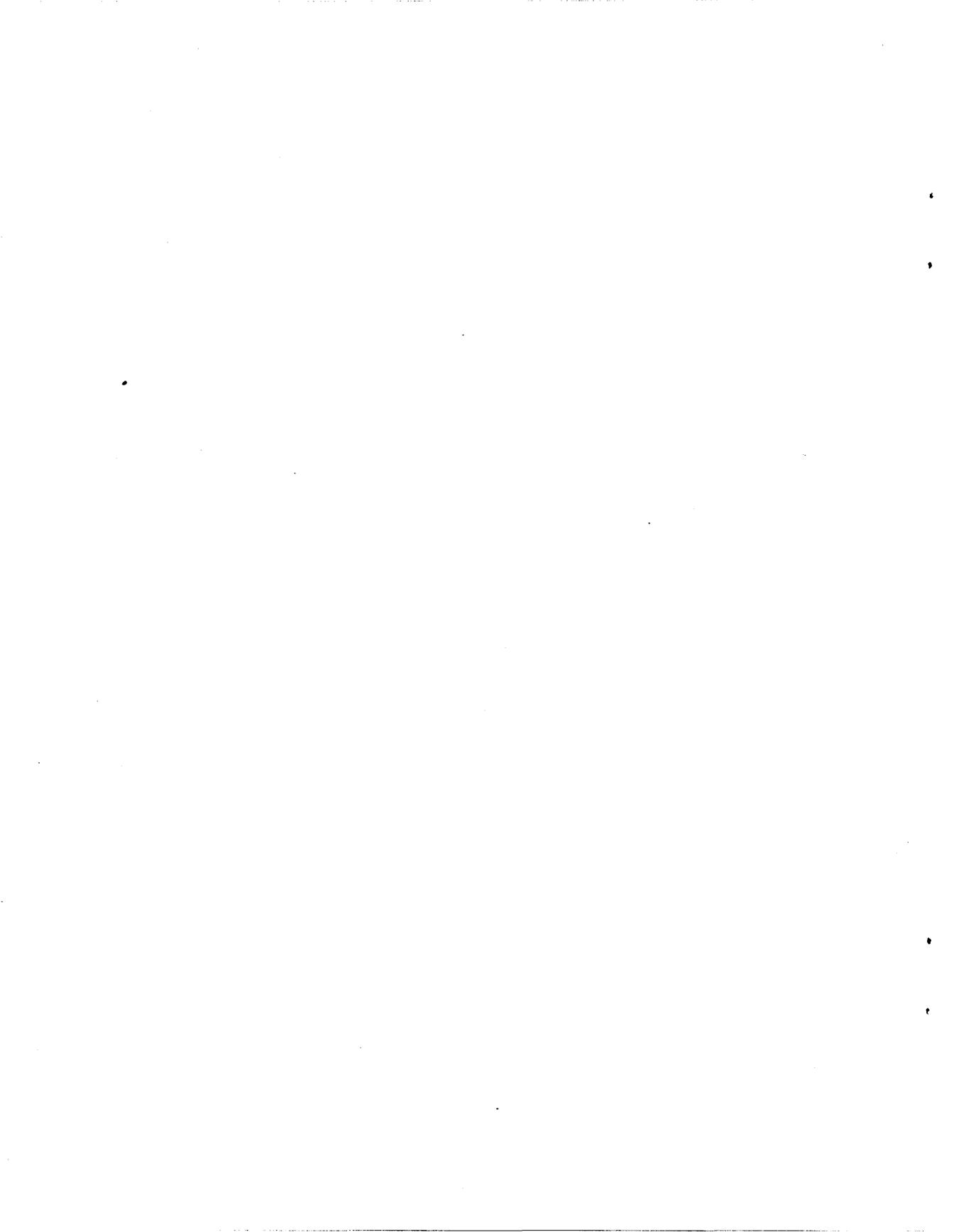
Layout of the series 300 Prototyping Platform.
The configuration shown is for the 7RS103 module.

ORDERING INFORMATION

Ordering Part Number	Speed
FOR USE WITH THE 7RS101 ARCHITECTURE	
7RS301-16	16 MHz
7RS301-20	20 MHz
7RS301-25	25 MHz
7RS301-30	30 MHz
FOR USE WITH THE 7RS102 ARCHITECTURE	
7RS302-16	16 MHz
7RS302-20	20 MHz
7RS302-25	25 MHz
FOR USE WITH THE 7RS103 ARCHITECTURE	
7RS303-16	16 MHz
7RS303-20	20 MHz
7RS303-25	25 MHz
FOR USE WITH THE 7RS107 ARCHITECTURE	
7RS307-16	16 MHz
7RS307-20	20 MHz
7RS307-25	25 MHz
7RS307-33	33 MHz

INCLUDED WITH SYSTEMS

Each Prototyping Platform includes the System Board, completely populated with 1 Mb of RAM and 256K of EPROM, with the Software Integration Manager in the EPROM. Each System also includes the appropriate personality card for the module architecture indicated and configured for the speed indicated. Documentation includes complete schematics for both the system board and the personality board, including all the PAL equations for the control circuitry.





Integrated Device Technology, Inc.

R3000 PGA ADAPTOR

IDT7RS363

FEATURES:

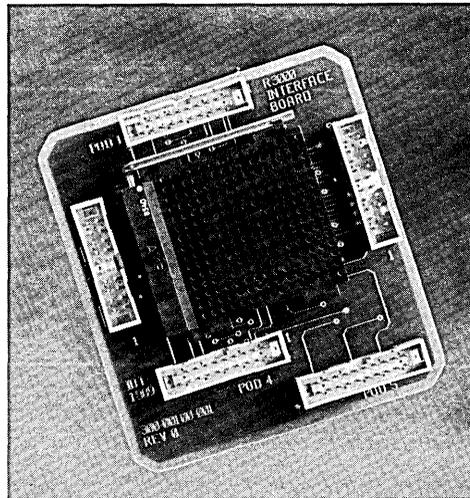
- Simple and direct connection to HP 16500A Logic Analyzer System.
- Probe points to 32 address, 32 data and 16 control signals of R3000.
- Several clocks available for signal strobes.
- Compact physical size permits its use in target system with minimal impact on spacing requirements.
- Setup files for 16500A Logic Analyzer assures speedy startup.
- No active components.
- Compact design assures minimal added lead capacitances (approx 5 pF).

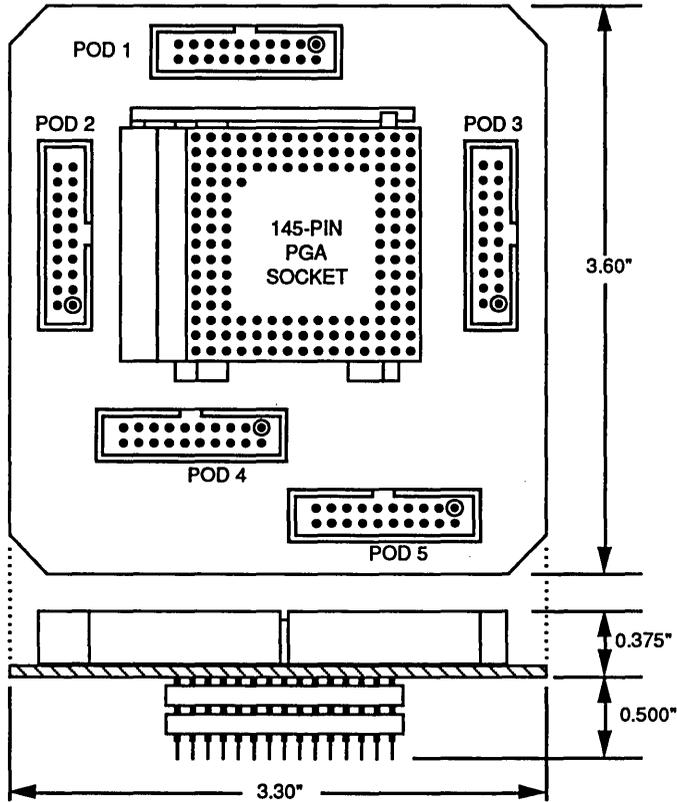
DESCRIPTION:

The IDT7RS363 is an adapter card intended for use in performing diagnostics on the operation of the IDT79R3000 RISC Processor on a Hewlett-Packard model 16500A Logic Analysis system. It contains no active components. Instead, it is used as a socket adaptor for the R3000, and all address, all data, and many control lines are made accessible for capture by the logic analyzer. It may only be used with the pin grid array (PGA) package of the R3000 and requires the logic analyzer system to be equipped with 5 HP Termination Adapters, P/N 01650-63201, to provide for the direct connection to the analyzer input pods.

For ease of setup, a diskette is provided, as a part of the 7RS363, which contains files loadable directly into the HP logic analyzer. These files automatically set up the logic analyzer by assigning the pods and the individual input channels directly to the signals captured from the R3000. In this way, the logic analyzer display will immediately represent the captured signals with all the proper signal names displayed.

The 7RS363 may also be used as a simple diagnostic tool, separate from its use as a logic analyzer adapter card. This is accomplished by virtue of the fact that all necessary signals of the R3000 are immediately accessible as test points on the card.





ORDERING INFORMATION

The PGA Adaptor is shipped with documentation describing all the pin connections.

PGA Adaptor for R30007RS363



Integrated Device Technology, Inc.

R3000 DISASSEMBLER for Use with the HP 16500 Logic Analyzer

IDT7RS364

FEATURES:

- Disassembler for the IDT79R3000 RISC microprocessor on the HP16500 logic analyzer.
- Interfaces to the IDT7RS301 And IDT7RS302 TargetSystem Boards.
- Allows actual code tracing.
- Direct Connection to IDT 7RS300 series Prototyping Platforms
- Can Be Used with Any R3000 System

DESCRIPTION:

The IDT7RS364 Disassembler for the HP16500 logic analyzer is a useful tool meant to ease the task of debugging software run on the IDT7RS301/302 TargetSystem Boards. The HP16500 itself allows the engineer to capture the CPU's executed opcodes. However, the IDT7RS364 will allow the engineer to trace the actual code executed by the processor without having to resort to lookup tables. The IDT7RS364 will decode the opcodes captured by the logic analyzer into the correct instruction mnemonic so that the engineer will know the exact processor state.

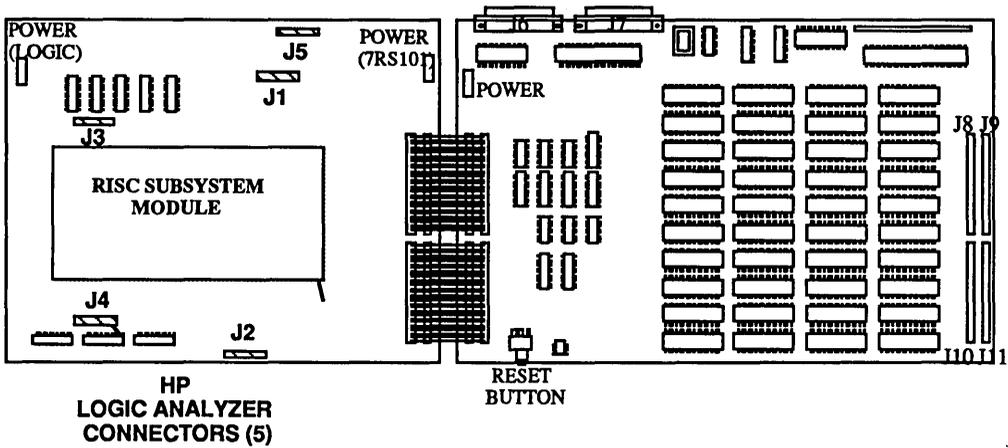
The IDT7RS364 will only capture main memory accesses (see Figure 1). Therefore its operation is guaranteed only if the software is being run in uncached address space.

State/Timing A
Listing 1
Invasm
Print
Run

Markers Off

Label>	ADDR	R3000 MNEMONIC
Base>	Hex	Hex
33	1FC04AD0	LW s1,0x0034(sp)
34	1FC04AD4	B 0x1FC04B20
35	0001F96C	LOAD DATA 0x00006602
36	1FC04AD8	NOP
37	1FC04B20	LI at,0x00006601
38	1FC04B24	BEQ s1,at,0x1FC04ADC
39	1FC04B28	NOP
40	1FC04B2C	MOVE a0,s0
41	1FC04B30	LW a1,0x0034(sp)
42	1FC04B34	LW a2,0x0038(sp)
43	0001F96C	LOAD DATA 0x00006602
44	1FC04B38	LW t1,0x0020(s0)
45	0001F970	LOAD DATA 0x00000000
46	1FC04B3C	NOP
47	000018DC	LOAD DATA 0xBFC162D0
48	1FC04B40	LW t2,0x0014(t1)

Typical Screen Display



The 7RS301 Prototyping Platform for the 7RS101 Modules.
The five connectors for the logic analyzer are on the module personality card.

ORDERING INFORMATION

The Disassembler is shipped on a 3.5" diskette for the HP16500 series Logic Analyzers. Included is complete set-up documentation and drawings showing how to use it with systems other than the 7RS300 series Prototyping Platforms.

Disassembler7RS364



Integrated Device Technology, Inc.

R3000 AND R3001 EVALUATION BOARDS

IDT7RS382
IDT7RS383

FEATURES:

- Complete RISC Example System
- Available for R3000 or R3001 CPUs
- Supplied with complete schematics and PAL equations
- Includes R3010 Floating Point Accelerator, Data and Instruction Caches (16k bytes each), 128Kb of main memory, and 128Kb of EPROM
- IDT's System Integration Manager included in EPROM
- Connectors provided for easy expansion.
- CPU and FPA in PGA Sockets for easy connection to Logic Analyzers.

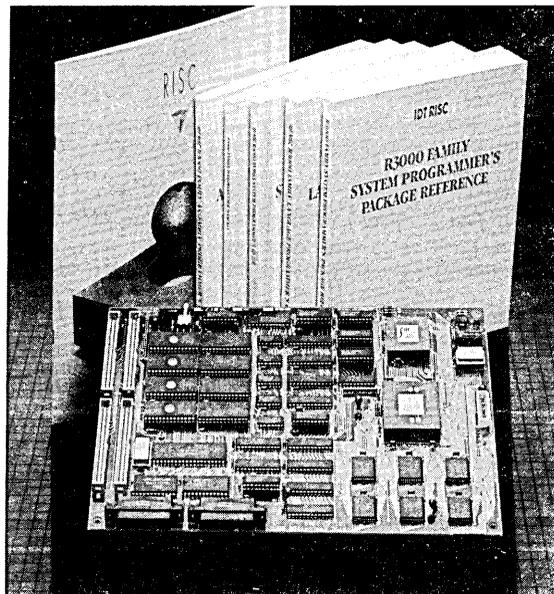
DESCRIPTION:

The IDT7RS382 and 7RS3833 are complete RISC systems intended for use as low-cost evaluation systems. They are completely self-contained on a single printed circuit board and require only a simple CRT terminal and a 5 volt power supply for operation.

The board contains the RISC CPU (R3000 on the 7RS382 and R3001 on the 7RS383) and a IDT79R3010 Floating Point Accelerator (FPA), as well as 16 Kbytes of Cache RAM for each of the data and instruction caches, EPROM, static main memory, two serial ports, a free-running programmable timer, and expansion connectors to permit external systems to be added. In addition, the system also contains clock timing, reset initialization logic, and read/write buffer control logic.

The EPROM contains IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing, and I/O.

The board is 11 inches long and 7.5 inches wide and is designed to be placed on a flat table-top surface. Standoffs are provided for physical support. Access to all components on the board is readily available with this packaging approach.



COMPLETE SINGLE BOARD COMPUTERS

The 7RS382 and 7RS383 Evaluation Boards are complete single board RISC computers, requiring only a 5 volt power supply and an RS-232 terminal for operation.

Both systems are intended as examples of typical designs using the R3000 and R3001 CPU chips. All the schematics and details of the designs are supplied with the boards.

The boards can also serve as a prototyping platform. Connectors are provided to add additional hardware on a wire wrap board. A 20-pin plug, J5 on the drawings, provides 16 control signals that can be connected to a logic

analyzer. Both the CPU and the FPA chips are mounted in PGA sockets, so a PGA adaptor (7RS363) can be used to connect all the CPU pins to a logic analyzer.

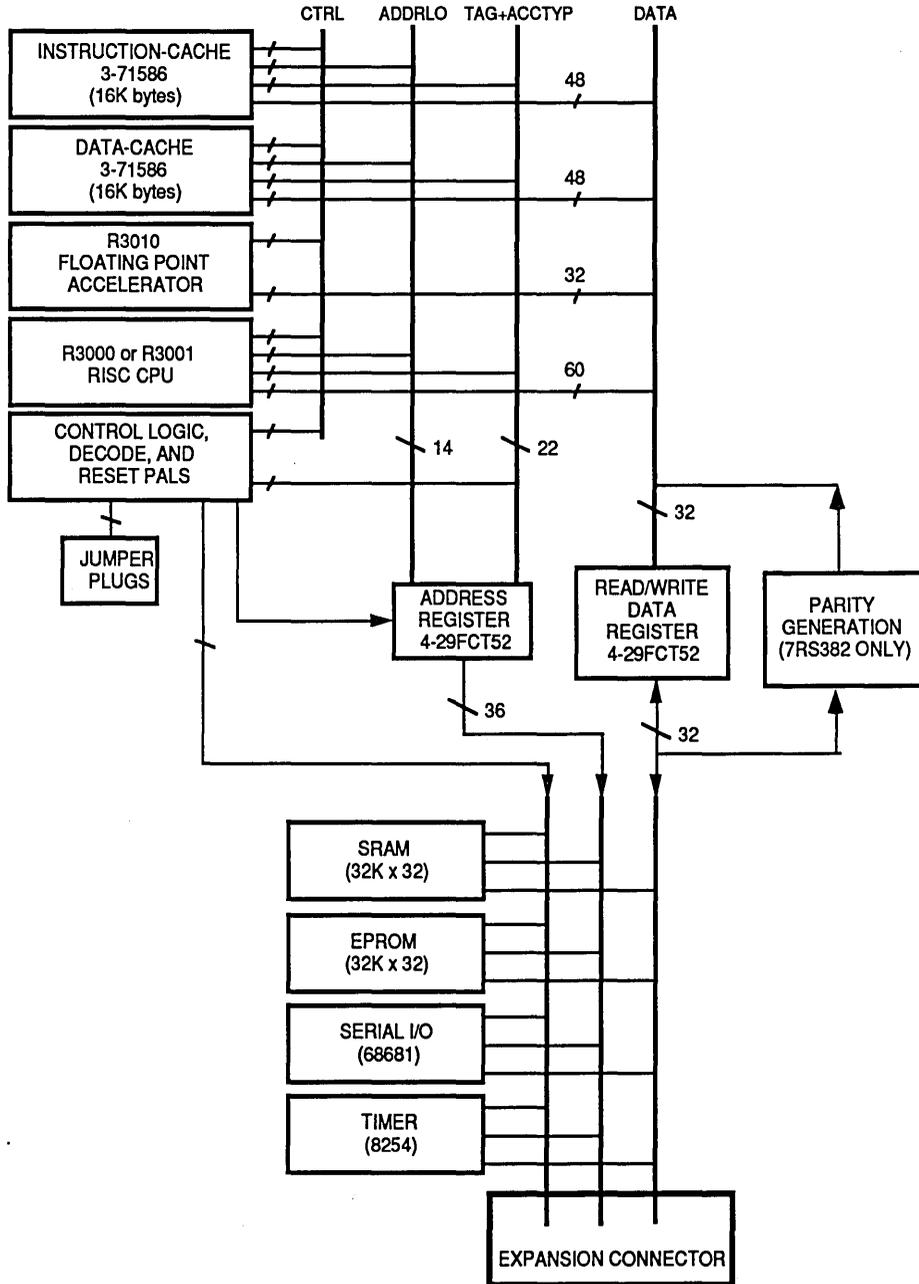
The 7RS383 (but not the 7RS382) can accept larger RAM and EPROM devices, supporting up to 512 Kb of EPROM and 2 Mb of static RAM.

Software supplied in the EPROM permits downloading of R3000 code compiled on a PC, MacStation, or MIPS machine. Commands are available to set break-points, single step, examine and modify memory, etc.

SIGNALS SUPPLIED ON EXPANSION CONNECTOR

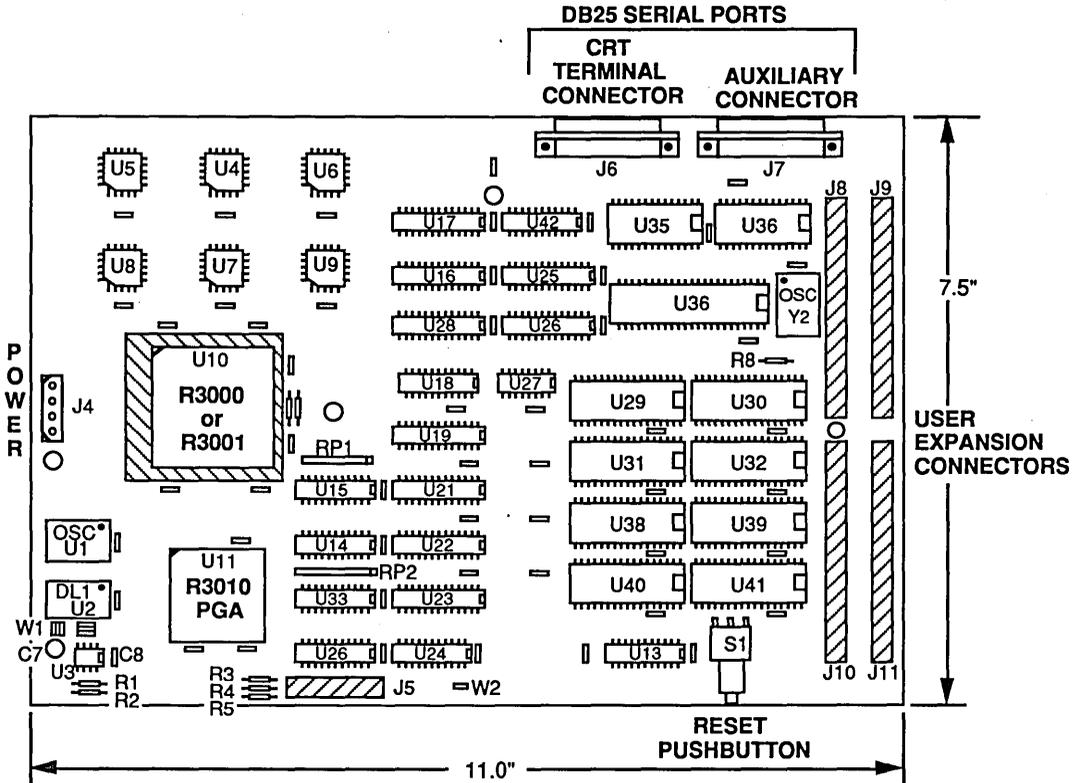
Signal Name	I or O	Description
EA00-EA31	I/O	32-bit buffered address bus
ED00-ED31	I/O	32-bit buffered data bus
SYSOUT	O	Buffered SYSOUT Clock from CPU; used to synchronize data transfers
MRES#	O	Copy of the Reset signal to the CPU
MREQ	O	Memory Request output (handshaking signal for data transfers)
XACK#	I	Acknowledge input (handshaking for data transfers)
OP3-OP5	O	Auxillary output pins from the 68681 UART
IP4-IP5	I	Auxillary input pin to the 68681 UART
WEA-WED	O	Write Enables for the four bytes of the data word
UCS1A-UCS1D	O	Four chip select signals decoded from the high order address bits.
INT0	I	Interrupt input to the R3000
PMRD#	O	Memory Read output signal. Used to enable output drivers in the expansion system during data read operations

FUNCTIONAL BLOCK DIAGRAM



The 7RS383 (with R3001) does not require parity;
the 7RS382 (with R3000) includes parity generation logic on the board.

PHYSICAL LAYOUT



7RS383 shown. 7RS382 is slightly different.

ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware.

Evaluation Board with R3000 CPU	7RS382
Evaluation Board with R3001 CPU	7RS383



Integrated Device Technology, Inc.

MACSTATION™ 2 R3000 Development System

IDT7RS502

FEATURES:

- 10 VAX MIPS RISC Computer inside any Macintosh II
- Includes UNIX V 3 Operating System
- Supplied with MIPS C-Compiler, Assembler, and Symbolic Debugger
- Will support any MIPS software packages, including SPP, SPP/e, FORTRAN.
- Uses all Macintosh peripherals for I/O
- Multifinder and System 7 Compatible

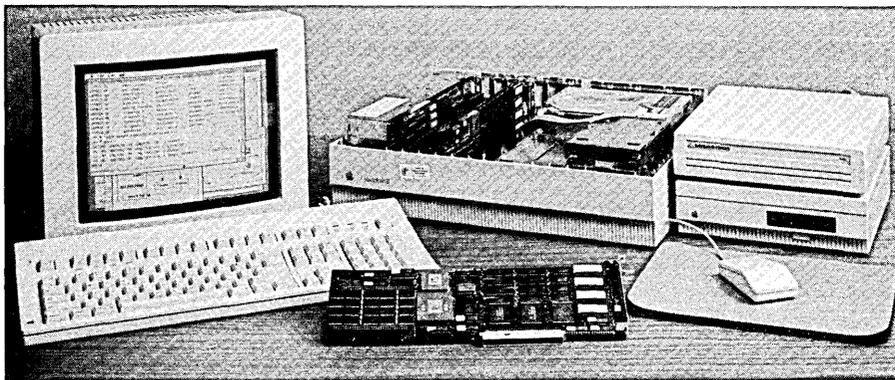
R3000 COMPUTER PLUGS INTO A MACINTOSH II:

The MacStation 2 is an R3000 based workstation consisting of a Macintosh II computer and a high-performance R3000 CPU that plugs into the NuBus inside the Mac. The R3000 CPU runs IDT/ux, IDT's port of MIPS RISC/os UNIX V 3, in a window under Multifinder.

The UNIX window is opened by double-clicking an icon on the Mac screen. The window is essentially a terminal emulator. When the window is opened, IDT/ux starts up on the R3000 CPU. Users can switch back and forth between the IDT/ux window and other Macintosh windows freely.

The system includes MIPS powerful C Compiler. Source code is written using any Macintosh text editing program, and a single command in the IDT/ux window will copy the file into the UNIX file system and compile it. Any other software written for MIPS RISC/os can be ported to the MacStation 2.

The MacStation hardware uses two slots in the Macintosh. The MacStation software is supplied on tapes and requires approximately 160 Mb of hard disc space when loaded.



MacStation 2

MACSTATION 2 HARDWARE

RISC CPU Card

The CPU card is a 16 MHz R3000 system, using the Floating Point Accelerator and 64 Kb each of instruction and data caches. The necessary hardware to run UNIX is also on the board. EPROMs on the card contain IDT's System Integration Manager (IDT/sim) which provides many debug and control features at the monitor level. The board communicates with all I/O via the Macintosh NuBus.

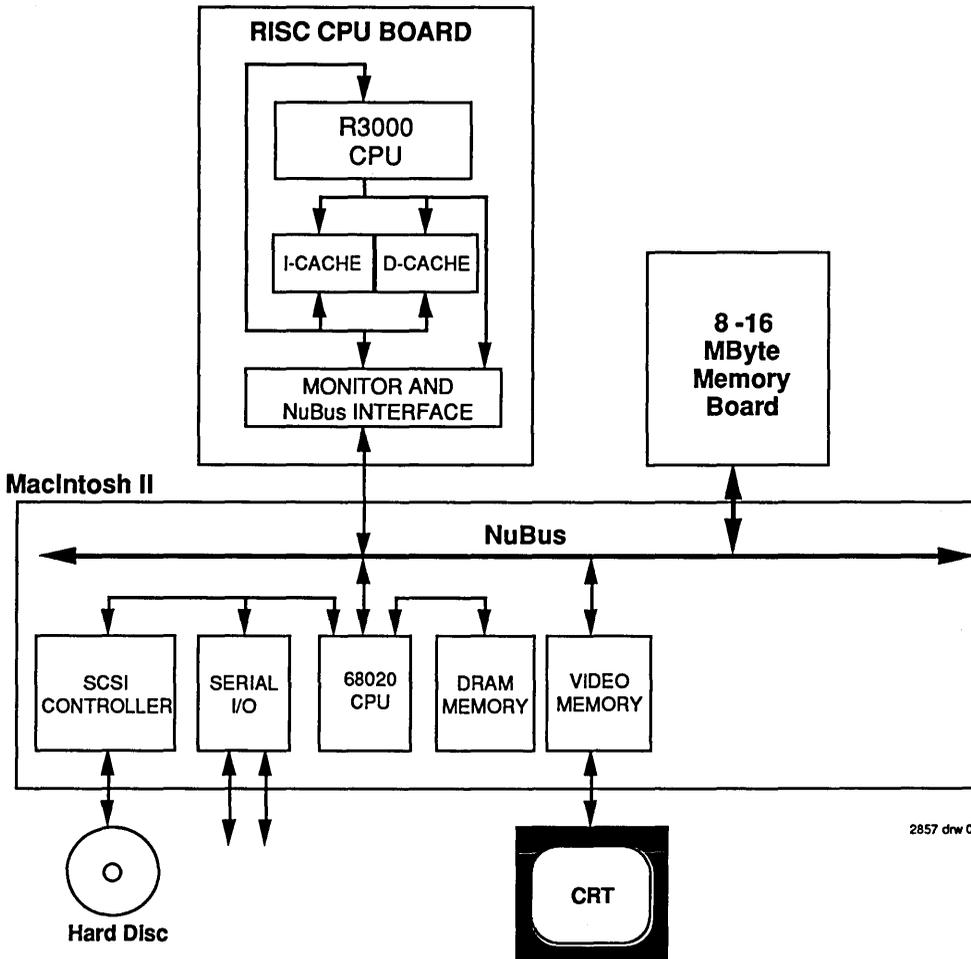
Main Memory

The MacStation 2 includes 8 Megabytes of memory on a separate NuBus card. This permits reasonably large programs to execute without excessive disc swapping. The memory may be expanded to 16 Mb by simply adding an 8 Mb extension card, available separately.

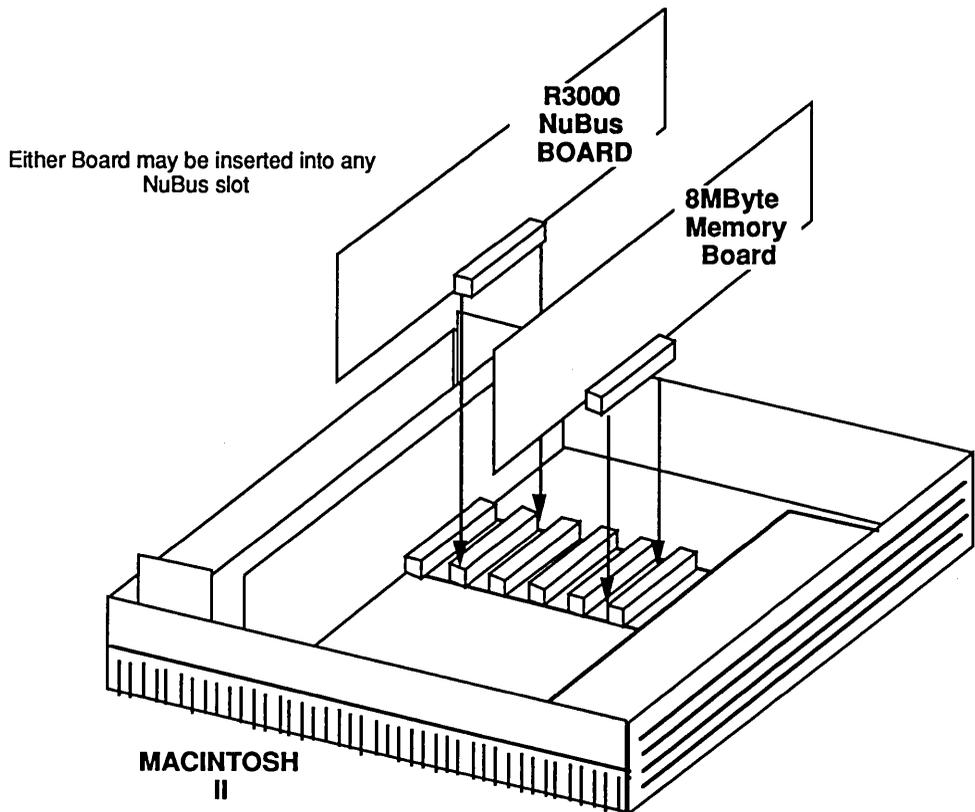
MACSTATION 2 SOFTWARE

The MacStation is shipped with all the software on tapes. It may be ordered with a 160 Mb hard disc with the software pre-installed, but tapes are still included for backup.

FUNCTIONAL BLOCK DIAGRAM



2857 drw 01



ORDERING INFORMATION

The MacStation 2 may be ordered in a variety of forms, ranging from the essential boards and software to complete systems with software pre-installed. The IDT/ux operating system requires a signed single-system license agreement which must be executed before the system can be shipped. Contact your IDT sales office for a sample of the license.

MacStation Boards7RS502B8-L
Includes R3000 NuBus CPU card, 8 Mbyte NuBus Memory card, IDT/ux. Requires a Macintosh II computer, system 6.01 or later, Apple tape drive, at least 160 Mbytes of free disc space.

MacStation Conversion Kit7RS502TD8-L
Everything to convert a Macintosh II to a MacStation. Includes the MacStation boards, IDT/ux, a tape drive, a 160 Mbyte Hard Disc and cables.

Memory Expansion Card7RS502X8
Adds 8 Mbytes to the Memory Card, raising total available to IDT/ux to 16 Mbytes.

Standard MonoChrome System7RS502MXM-L
Includes the MacStation Boards, IDT/ux, tape drive, 160 Mb external hard disc, cables. Also includes Macintosh IIx computer with 4 Mbytes of internal memory and 80 Mb internal hard disc, monochrome 13" monitor and video card, extended keyboard.

High Performance

MonoChrome System7RS502MFXM-L
Includes the MacStation Boards, IDT/ux, tape drive, 160 Mb external hard disc, cables. Also includes Macintosh IIx computer with 4 Mbytes of internal memory and 80 Mb internal hard disc, monochrome 13" monitor and video card, extended keyboard.

Other Macintosh system configurations.

The MacStation can be supplied with any desired Macintosh configuration. Contact factory for a quotation.

IDT/ux Documentation

This is an eight-manual set of documentation for MIPS RISC/os (UNIX V 3 with BSD extensions). Included are: RISC/os Programmer's Reference Manual, User's Reference Manual, System Administration Reference Manual, System Administrator's Guide, Programmer's Guide, User's Guide, Streams Primer and Programmer's Guide, Guide to BSD on RISC/os.

IDT/ux Documentation Package7RS551BDU

Other MIPS Software for MacStation

The following MIPS products are available for the MacStation. All require assigned license agreement prior to shipment. Contact your IDT sales office for a sample of the agreement.

SPP for MacStation7RS992SMT-L
Source Code, site license, includes documentation

SPP/e for MacStation7RS993SMT-L
Source Code, site license, includes documentation

FORTTRAN for MacStation7RS994BMT-L
Single user binary license, includes documentation



Integrated Device Technology, Inc.

IDT/sim SYSTEM INTEGRATION MANAGER ROMable Debugging Kernal

IDT7RS901

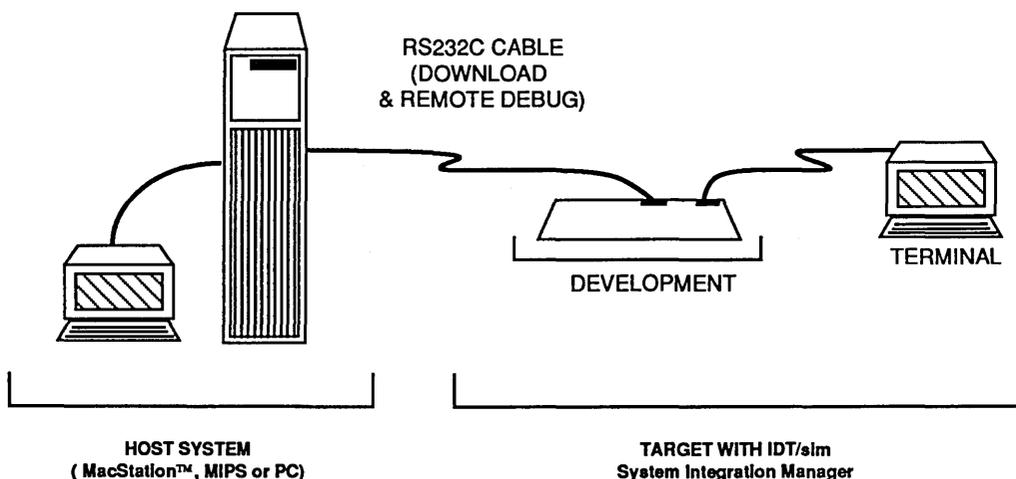
FEATURES:

- Provides complete control over hardware and software for system integration
- Fits in 82Kb of EPROM space, plus 16Kb of RAM.
- Provides CPU control for register and memory manipulation, cache access, and TLB management.
- Includes standard I/O support
- Easy to add new commands and new I/O drivers.
- Complete support for MIPS symbolic debuggers. No additional code required.
- Supports downloading code in either ASCII or binary formats.

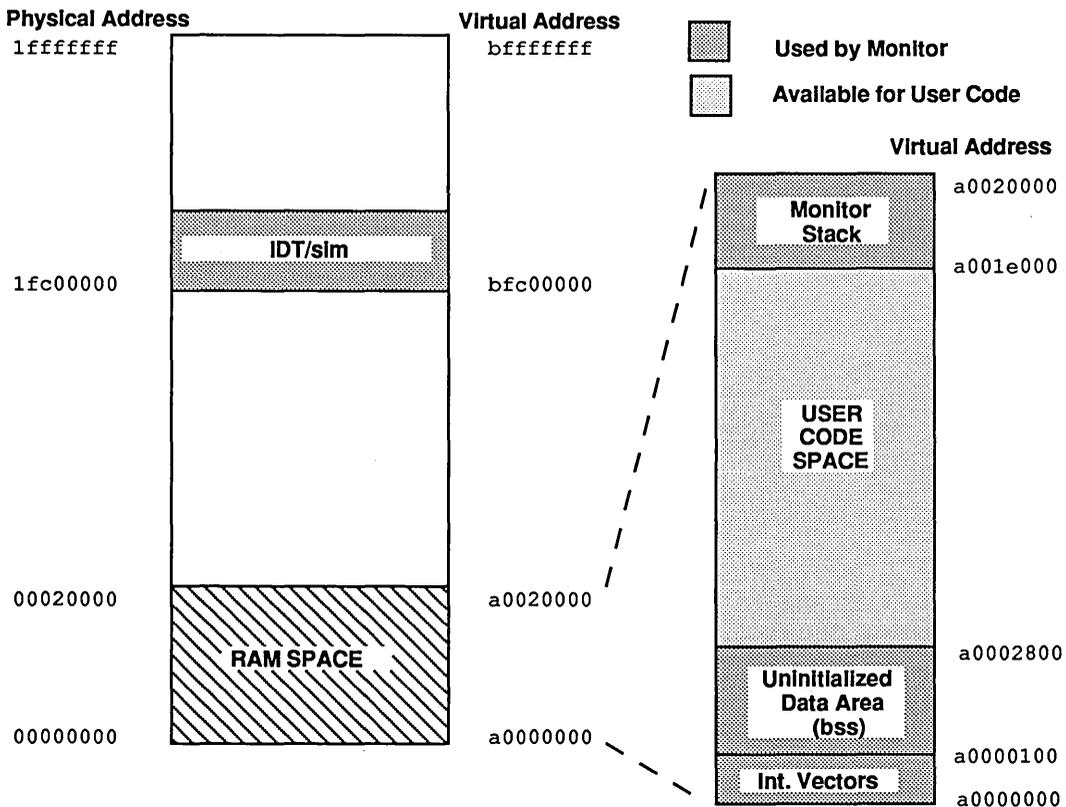
POWERFUL TOOL FOR R3000 SOFTWARE/ HARDWARE INTEGRATION:

The IDT7RS901 System Integration Manager (IDT/sim) is a ROMable software product that permits convenient control and debug of RISC systems built around the MIPS R3000 architecture. It permits users to quickly develop and debug stand-alone systems. Facilities are included to operate the CPU under controlled conditions, examining and altering the contents of memory, manipulating and controlling R3000 resources (such as cache, TLB and coprocessors), loading programs from host machines, and controlling the path of execution of loaded programs. Remote (source/symbolic) debugging is also supported.

IDT/sim requires 82Kb of EPROM space for code and data and 16Kb of ram sapce for uninitialized variable data and stack. The minimal I/O system supported uses UARTS. The default drivers support the 2681 or 68681 devices. Other devices can be added easily.



Debug Commands	Provides commands for CPU control such as execution, register and memory manipulation, cache access and TLB management.
Run Time Support	IDT/sim provides numerous entry points that client programs may access to preform standard operations. These include i/o support (open, close, read, write etc.), standard console i/o support (get/put char/string , printf) and facilities to install new commands and device drivers.
Remote Debug	Complete remote (source/symbolic) debug support is provided for operation with MIPS symbolic debuggers (DBX). This feature is incorporated into the monitor residing in EPROM so the user does not have to download any additional code (ie dbgmon) to debug code running on his target system. Additionally an easy to use interface is provided so user code that is interrupt driven may be debugged.
Download Support	Supports downloading code from a host to the users target machine. Both ASCII and binary formats are supported.



LIST OF COMMANDS

- rad [-o|-d|-h]*
 Set the default radix to the requested base.
- seg [-0|-1|-2|-u]*
 Set the default segment to the requested k-segment.
- history|h*
 Displays the last 8 commands entered
- help? [commandlist]*
 Prints a list of the commands available in the monitor.
- regsel|rs [-c|-h]*
 Selects display format for register names.
- checksum|cs*
 Display the checksums for each of the 'EPROMs'.
- init|i*
 Initialize prom monitor (warm reset)
- dbgint|di [-e|-d-] <DEV>*
 Debug interrupt enable/disable - allows 'break key' to gen extr. int.
- fill|f [-w|-h|-b|-l|-r] <RANGE> [value_list.]*
 Fills memory specified by range with value_list..
- sub [-w|-h|-b|-l|-r] <address>*
 This command allows the user to examine and change memory interactively.
- dump|d [-w|-h] <RANGE>*
 Display contents of memory.
- move|m [-w|-b|-h] <RANGE> <destination>*
 Move the block of memory
- compare|cp [-w|-b|-h] <RANGE> <destination>*
 Compare the block of memory
- search|sr [-w|-b|-h] <RANGE> <value> [mask]*
 Search the area of memory for a value.
- wc [-i] [-w|-b|-h] <RANGE> [value_list]*
 Fill cache memory with a pattern.
- cacheflush|cf [-i|-d]*
 Flush both the i-cache and the d-cache.
- rc [-i] [-w|-b|-h] <RANGE>*
 Display cache memory.
- fr <reg#|name> <value>*
 Put <value> into the register
- dr [reg#|name]*
 Print out the current contents of registers.
- dis <RANGE>*
 Disassemble the contents of memory.
- tlbdump|td [RANGE]*
 Dumps the contents of the translation buffer.
- tlbflush|tf [RANGE]*
 Flushes the contents of the translation buffer.
- tlbmap|tm [-i index] [-ndgv] <vaddress> <paddress>*
 Specify virtual to physical mapping in the translation buffer.
- tlbpid|ti [pid]*
 Displays the current process identifier (pid).
- tlbptov|tp <physaddr>*
 Search the translation buffer for translations which map to <physaddr>.
- load|l <_device> [format]*
 Down load from an I/O device.
- debug|db [DEV]*
 Enter remote symbolic debug mode with host.
- go|g [-n] <address>*
 Begin execution at address
- gotill|gt <address>*
 Continue execution from the current PC till break address encountered
- call|ca <address> [arg1 arg2 ... arg8]*
 Invoke a 'C' language subroutine.
- step|s [<count>]*
 Execute a specified number of instructions.
- cont|c*
 Continues execution of the client process from where it last halted execution.
- brk|b [addresslist]*
 Display currently set breakpoints or set break point at each of the addresses.
- unbrk|ub <bnumlist>*
 Unset breakpoints listed.

LIST OF RUN TIME SUPPORT ENTRY POINTS

- __exit()***
Returns control to the monitor.
- __atob(str,intptr,base,seg)***
Converts an ascii string to an integer.
- __clear_cache(begin_addr,num_bytes)***
Clears a selected area in I and D cache
- __cli(cmd_table,prompt)***
General purpose command line interpreter
- __flush_cache()***
Flushes both the I and D cache.
- __get_range(str,start,end)***
Parses the range specification.
- __getchar()***
Get a character from the standard input device.
- __gets(str)***
Get a string from the standard input device.
- __help(argc,argv,cmd_table)***
Print the usage line for all specified commands
- __install_commands(cmd_table)***
Allows the user to extend the command set of the standard monitor.
- __install_immediate_int(ptr_user_int_rt)***
Installs a pointer to a user interrupt function that will be called by the monitor when an exception/interrupt occurs.
- __ninstall_new_dev(dt_ptr,diptr)***
Installs a new device driver that will be recognized by IDT/sim
- __install_normal_int(ptr_user_int_rt)***
Installs a pointer to a user interrupt function that will be called by the monitor when an exception/interrupt occurs.
- __ioctl(fd,cmd,arg)***
Sets flags for i/o characteristics and/or calls driver ioctl routines.
- __open(device,flags)***
Opens a device for reading and/or writing.
- __printf(format,[args])***
Formatted print routine
- __putchar(c)***
Output a character to the standard output device.
- __puts(str)***
Output a string to the standard output device.
- __read(fd,buf,cnt)***
Read data from an external device.
- __reset()***
Resets the monitor
- __setjmp(cur_cntx)***
Save the current context so that non-local goto's may be implemented.
- __longjmp(cur_cntx)***
Restores the saved context so that non-local goto's may be implemented.
- __showchar(c)***
Prints the character passed to it in a visible manner
- __strcat(s,t)***
Concatenate two strings (39)
- __strcmp(s,t)***
Compare two strings (36)
- __strcpy(s,t)***
Copy one sting to another (38)
- __strlen(s)***
Determine the number of characters in a string. (37)
- __tokenize(cmdline,argv)***
Parse command line and build argc/argv structure
- __write(fd,buf,cnt)***
Write data to an external device.

ORDERING INFORMATION

To order the IDT System Integration Manager, order the Developmental Use License AND order the software on the appropriate media. The license will be shipped to you for signature; on return the software will be shipped. You may also order binary distribution rights for the run-time version of the monitor. Ask your IDT sales office for information.

- Developmental Use License** 7RS901SLV
Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product.
- Source for PC/AT, MS-DOS,**
1.2 Mb Floppy 7RS901SAF-L
Use with IDT/c C-Compiler (7RS903). Developmental Use License number must be referenced on order, or must be ordered simultaneously.
- Source for 286/386 PC, SCO Xenix** 7RS901SXX-L
Use with IDT/c C-Compiler (7RS903). Developmental Use License number must be referenced on order, or must be ordered simultaneously.
- Source for IDT MacStation, on Mac Disc** 7RS901SMD-L
Use with MIPS C Compiler supplied with MacStation or with IDT/c. Developmental Use License number must be referenced on order, or must be ordered simultaneously.
- Source for MIPS Machine,**
QIC-24 TAR Tape 7RS901SUU-L
Use with MIPS C Compiler or with IDT/c. Developmental Use License number must be referenced on order, or must be ordered simultaneously.
- Maintenance Agreement** 7RS901SSY
One year free minor updates, and discounted upgrade to major update versions. We supply a direct telephone contact for support.
- Binary Distribution Rights** 7RS901BLP-L
Extension to Developmental Use License to permit inclusion of binary code into end product. Development Use License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. Additional copies are subject to the royalty below, or a one-time buyout.
- Binary Distribution Sublicense** 7RS901BLC-L
Per Copy Royalty for distribution of runtimes developed using the System Integration Manager beyond the first 100..



Integrated Device Technology, Inc.

IDT/c Multi-Host C-Compiler System

IDT7RS903

FEATURES:

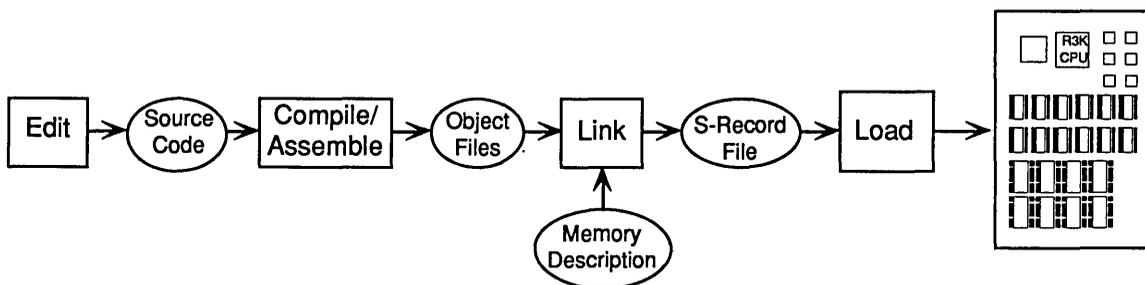
- Includes C-compiler, Optimizing Scheduler, Assembler, and Linker
- Meets Plum Hall 2.00 validation to ANSI C
- Runs on PC/ATs under MS-DOS™ or XENIX™, on MIPS machines, and on MacStation™
- Supports entire IDT family of MIPS ISA Processors: R3000, R3001, R3051, and R3052
- Loader communicates with IDT's System Integration Manager (IDT/sim)
- Linker provides control over multiple memory segments

OPTIMIZING C-COMPILER SYSTEM:

IDT/c consists of a set of software products that run on a variety of platforms, and which together produce highly efficient code for R3000 CPUs. The code can be downloaded in several formats to a target machine for execution. On the target machine, the code can be controlled with IDT's System Integration Manager (IDT/sim).

The compiler is based on the popular GNU C compiler, and is fully compliant with ANSI C.

The entire package is available for execution on 286 or 386 machines under MS-DOS or XENIX, as well as the MIPS workstations and IDT's MacStation single user workstation.



IDT/c System Flow

DESCRIPTION

The IDT/c C-Compiler System is a complete development package for CPUs based on the R3000 architecture. It contains an optimizing cross compiler, scheduler optimizer, cross assembler, linker, and a downloader. The 'C' compiler is compliant with ANSI 'C' standard and performs the optimizations available in state of the art 'C' compilers. The assembler is compatible with files written for the MIPS assembler. It supports the R3000 machine instructions and architecture described in the book by Gerry Kane, "MIPS RISC Architecture" and is specified the "R3000 Family Assembler Instruction Set Definitions" from IDT. The IDT/c package runs on a variety of host machines and operating systems and is part of IDT's cross development system tools which include other packages such as debug monitors and libraries.

Compiler

The C pre-processor is GNU cpp. All C- preprocessing features are supported. The compiler is the GNU 'C' optimizing compiler available from the Free Software Foundation. (The source to the 'C' compiler pass is available on UU-Net. The combination of binary version of GCC from IDT and the IDT cross assembler has been tested for compliance to the ANSI 'C' standard using the Plum Hall test suite and is compliant.

Optimizing Scheduler and Assembler

The IDT scheduler and cross assembler takes advantage of the advances made recently by RISC microprocessors. Some of these include the simple native instruction set augmented by a richer synthetic instruction set. The scheduler first expands the the synthetic instructions to the native instruction set. It then rearranges code to allow for and take advantage of R3000 pipeline architecture. At the same time the scheduler analyzes loads of static constants and makes use of previously loaded constants that are close in value. There are some extensions in the IDT cross assembler that provide programmer with more control over code generation, such as 'laiu' - load address upper and 'oria' - load address lower, enabling direct programming in pure assembly language.

The IDT cross assembler input is compatible with source code written for the MIPS assembler. It implements the R3000 native instruction set as defined in the "MIPS RISC ARCHITECTURE" book by GERRY KANE. The assembler produces .files which are later linked together with other files to produce an executable file.

Linker

The linker combines together separately assembled program files into one object module. It uses information from a memory description file to determine where the object module will be placed in the R3000 address map. Command line switches may be used to override the memory description file.

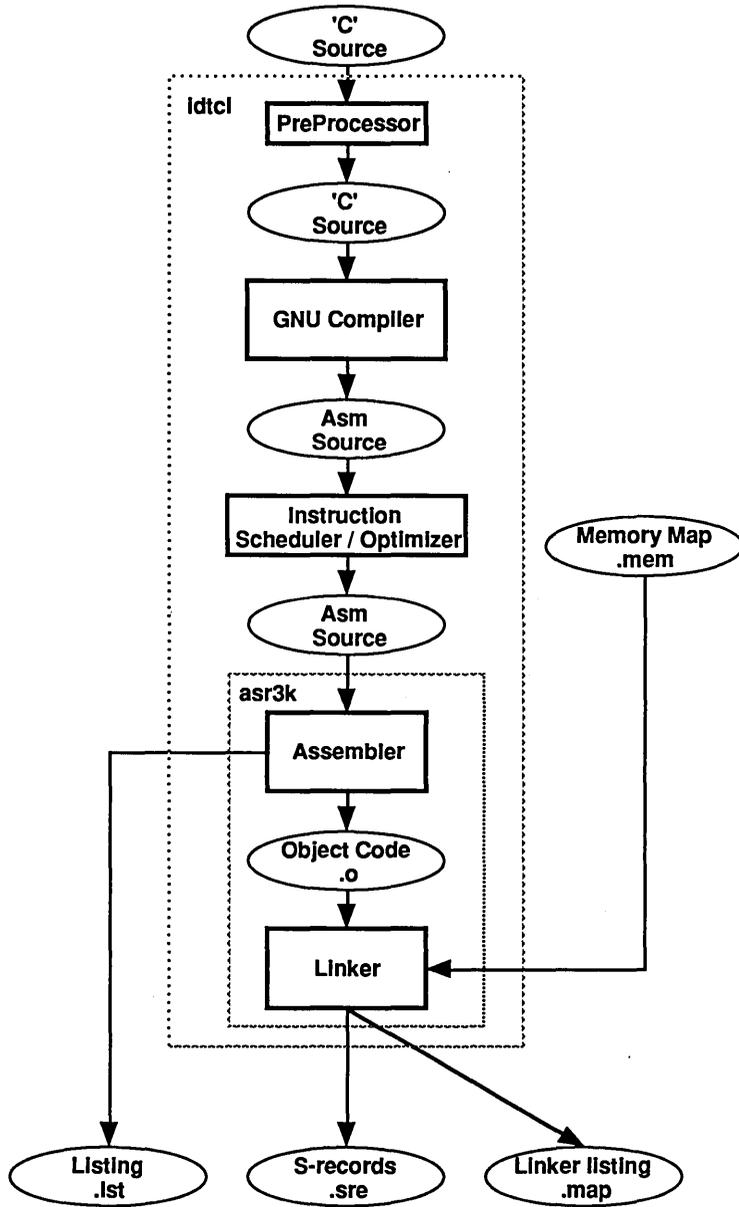
The memory description file tells linker what address classes are legal, what addresses exist within those classes, and what addresses should be written to output files. The file consists of a sequence of class specifications (CODE, DATA, etc.) and associated address ranges. In this way the linker can be instructed to place code at different locations. The linker can output S-record files (.sre) for direct downloading to target boards or EPROM programmers.

Memory description file

The memory description file tells linker what address classes are legal, what addresses exist within those classes, and what addresses should be written to output files. There are three types of file formats supported: S-Records (DUMP), INTEL hex (INTEL), and image (BINARY). The S-Record files are useful in down loading to target boards, where as the INTEL hex format files are useful for EPROM programming because the linker provides for the code to be divided into multiple files under this format.

Invocation

The pre-processor, compiler, scheduler, assembler and linker are controlled by a single driver program, 'itdcl'. The exact way in which 'itdcl' controls the compiler, assembler and linker depends on the host operating system environment.



IDT/c Flow

COMMAND LINE SWITCHES

- E :**
pre-process only. .S file is expected. Pre-processed file is written to the standard output.
- O :**
optimize (GNU cc -O option).
-O1 : optimize even more (GNU cc options: -fstrength-reduce -fforce-addr -fforce-mem -fcombine-regs -finline-functions).
- c :**
assemble only, do not link. Expected are filenames with .s or .S suffixes. Output files (in absence of -o) will have .o suffix.
- ZA :**
produce assembly listing.
- o xxx :**
name output file The default output name is 'out.sre'.
- ZL :**
produce link map.
- Fxxx.xxx :**
Use xxx.xxx as memory layout description file. In absence of -F option the default is to use file idt.mem in default library directory.
- ZThhhhhhhh :**
Specify text loading address, hhhhhhhh is address in hex, up to 8 hex digits. This will override .mem file definitions.
- ZDhhhhhhhhh :**
Specify data loading address, hhhhhhhh is address in hex, up to 8 hex digits. This will override .mem file definitions.
- e name :**
Use global 'name' as program start address.
- noenv :**
Do not include default library modules which define the order of program sections and global symbols that point to beginning and end of text, data and bss.
- nostdlib :**
Do not include library for linking with IDT PROM monitor.

OPTIMIZATIONS

Multiple optimizations passes are performed by the GCC compiler. The following is a list of the passes and a brief description:

Jump optimization

Simplifies jumps to the following instruction, jumps across jumps, and jumps to jumps; while deleting unreferenced labels and unreachable code.

Register Scan and common subexpression elimination

Finds first and last use of each register for purposes of subexpression elimination while performing constant propagation.

Loop optimization and strength reduction

Moves constant expression code outside of dynamic loop.

Data flow analysis

The program is divided into basic blocks and identifies the life of values in registers. Once done, then code producing unused results can be eliminated and unreachable loops are eliminated.

Local register allocation

Allocates registers to be used inside each basic block.

Global register allocation

Assigns registers for values which live across basic block boundaries.

The final pass is to generate assembler code. At this point peephole optimizations are performed as well as generating and optimizing the function entry and exit code sequences.

ASSEMBLER DIRECTIVES

.align n, n=1-3
 align so that n least significant bits of address are 0.

.ascii "string"
 assemble string.

.bss
 store following into bss section.

.byte arg,arg,...,arg
 assemble arguments into consecutive bytes.

.data
 store following into data section.

.end name
 Included for MIPS asm compatibility but ignored.

.ent name
 Included for MIPS asm compatibility but ignored.

.extern name,n
 Import symbol 'name' that refers to n bytes of storage
 . (included for MIPS asm compatibility and ignored).

.globl name
 export defined symbol.

.half arg,arg,...,arg
 assemble arguments into consecutive halfwords.

.set argument
 argument can be :
at
 error flag every use of \$1.
noat
 disable errors due to user's usage of \$1 (at).
reorder
 enable scheduling to resolve pipeline conflicts.
noreorder
 disable scheduling.

.space n
 skip next n bytes, advancing location counter by n.

.text
 store following into text section.

.word arg,arg,...,arg
 assemble arguments into consecutive words.

SEGMENT

The SEGMENT directive selects the address segment where the following code or data will be stored. It is used to implement '.text', '.data' and '.bss' which are MIPS compatible segments. Using this directive the user can create other custom segments.

ORDERING INFORMATION

The IDT/c C-Compiler includes an efficient C-compiler based on the popular GNU C. The compiler's output is passed through an optimizer, and the resulting code assembled and linked. A single host system license is included.

For PC/AT, MS-DOS, on 1.2 Mb Floppy	7RS903BAF-N
For 286 machine, SCO Xenix, on Disc	7RS903BYX-N
For 386 machine, SCO Xenix, on Disc	7RS903BXX-N
For MIPS machine RISC/os, on QIC-24 TAR	7RS903BUU-N
Maintenance <i>Includes free upgrades for one year and direct telephone contact for support</i>	7RS903BSY



Integrated Device Technology, Inc.

CROSS ASSEMBLER For IBM PCs and Clones

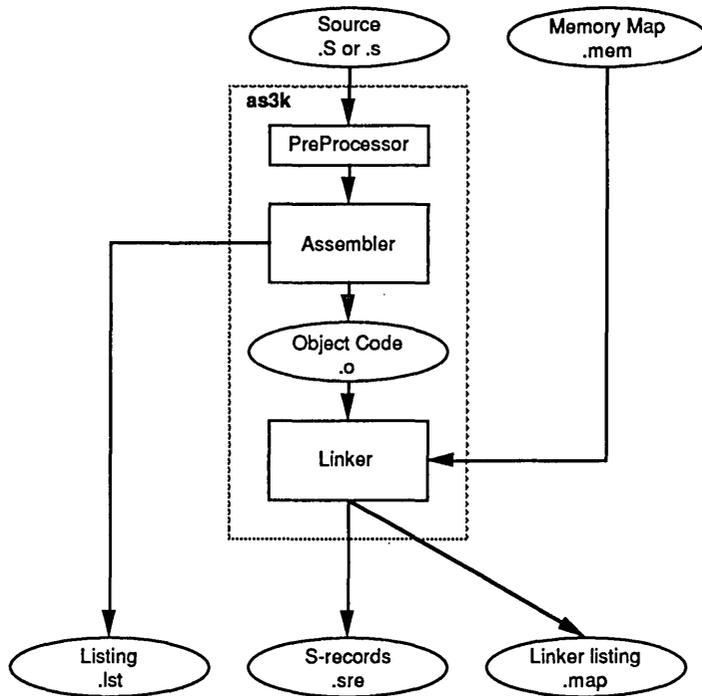
IDT7RS904

FEATURES:

- C-Like Preprocessor allows programmer to extend instruction set
- Provides for separate code segments loaded at different memory locations.
- Outputs S-records and Intel HEX
- Provides symbolic and hex instruction listing
- Lists Absolute addresses of code segments and symbols
- Interfaces to IDT System Integration Manager

DESCRIPTION:

IDT7RS904 is a cross assembler with a C-like pre-processor and linker that produces Motorola S-record or INTEL HEX downloadable files and a downloader. It is intended for cross-development with R3000 as target architecture. The assembler is compatible with files written for the MIPS assembler. The assembler supports the R3000 machine instructions and architecture described in the book by Gerry Kane, "MIPS RISC Architecture". The cross assembler package runs on variety of host machines and operating systems. The pre-processor, assembler and linker are invoked by a single driver named "asr3k".



Assembler Flow

PRODUCT FEATURES

Preprocessor

The C-like pre-processor is provided to process assembly language files such that the programmer can extend the instruction set of the cross assembler. All C- preprocessing features are supported.

Assembler

Assemblers for R3000 differ from 'classical' assemblers because they attempt to transparently provide the richer instruction set. This is due to the RISC architecture, which provides only essential instructions and achieves high performance in return. In order to enable higher efficiency in assembly-language programming, assemblers introduce instructions that do not directly map into the machines instruction set. In this way programmers in effect can program with a richer instruction set than that of the processor.

The 7RS904 is compatible with the MIPS assembler. It implements the R3000 instruction set as defined in the "MIPS RISC ARCHITECTURE" book by GERRY KANE (appendix D). With a few exceptions programs written for the MIPS assembler will directly compile. The cross assembler varies from the MIPS assembler in that it requires labels, if present, to start in column 1 and operators to start in a column greater than 1.

Linker

The linker combines together, separately assembled program files into one object module. It uses information from the memory description file to determine where the object module will be placed in the R3000 address map. Command line switches may be used to override memory description file.

Memory description file

The memory description file tells linker what address classes are legal, what addresses exist within those classes, and what addresses should be written to output files. The memory description file consists of a sequence of class

specifications (CODE, DATA, etc.) and associated address ranges. In this way the linker can be instructed to place code at different locations.

The linker can generate three different types of output files. The file type is controlled from the memory description file, by placing a FILETYPE specification in the output file specification line. There are three choices: DUMP - Generates single .sre S-record file. (default), INTEL - Intel hex file format, BINARY - Generates a binary image of the file.

Downloadable files

The linker can output S-record files (.sre), in which individual S- records are lines of text as interpreted by the host system conventions, ie. they are separated by line delimiters. The 'dl' program can convert files to S-records with no intervening delimiters.

EPROM files

The linker can output INTEL hex files for the purposes of burning EPROMs. The linker may be instructed to divide the output code and data segments into multiple files to accomodate separate sockets and address spaces.

Extensions

There are some extensions in the cross assembler that provide the programmer with more control over code generation, such as 'lau' - load address upper and 'lal' - load address lower, enabling direct programming in pure assembly language.

lal reg,addr

Load Address Lower. Loads (using ori) lower 16 bits of address into register. Address is relocatable symbol (can be external).

lau reg,addr

Load Address Upper. Loads (using lui) upper 16 bits of address into register. The lower 16 bits are cleared. Address is relocatable symbol (can be external).

ORDERING INFORMATION

7RS904 Cross Assembler for PCs

This is a macro-assembler that runs on any PC running MS-DOS. A single user license is included.

For PC/XT, MS-DOS, on 320 Kb Floppy	7RS904BPL-N
For PC/AT, MS-DOS, on 1.2 Mb Floppy	7RS904BAF-N



Integrated Device Technology, Inc.

IDT/FP FLOATING POINT LIBRARY For use with R3000 Compilers

**ADVANCE
INFORMATION
IDT7RS905**

FEATURES:

- Conforms to IEEE 754 format
- Converts ASCII to/from Floating Point
- Converts Integer to/from Floating Point
- Adheres to IEEE 754 Error Handling
- Works with IDT/c on PCs, MacStation, or MIPS machine, and with MIPS C-Compiler on either IDT MacStation or MIPS Machine.

DESCRIPTION:

The IDT7RS905 product is a floating point (IEEE-754) arithmetic library for use in IDT79R3000 systems that do not incorporate a IDT79R3010 floating point coprocessor. It provides the basic single and double precision arithmetic functions (add, subtract, multiply and divide) as well conversion routines between different precisions, integer and ascii formats. The IEEE-754 single precision floating point format represents numbers ranging from $\pm 1.2E-38$ to $\pm 3.4E+38$ with 24 bit mantissa precision. The double precision format offers a range of $\pm 2.2D-308$ to $\pm 1.8D308$ with a 53 bit mantissa. The accuracy of the floating point library is within one least significant bit. The IEEE floating point format defines special representations for underflow (result = zero), overflow (result = + INF or - INF), and invalid operation (result = Not a Number, NaN). The floating point library adheres to the IEEE-754 error handling procedure in all applicable cases.

SUPPORTED OPERATIONS

Addition	FPADD(a,b) & DPADD(a,b)
Subtraction	FPSUB(a,b) & DPSUB(a,b)
Multiplication	FPMUL(a,b) & DPMUL(a,b)
Division	FPDIV(a,b) & DPDIV(a,b)
Comparison	FPCMP(a,b) & DPCMP(a,b)
Integer to FP	FPFLT(int) & DPFLT(int)
FP to Integer	FPINT(sp) & DPINT(dp)
DP to SP	DPTOSP(dp)
SP to DP	SPTODP(sp)
ASCII to FP	FASCBIN() & DASCBIN()
FP to ASCII	FBINASC() & DBINASC()

ORDERING INFORMATION

This software contains a library of floating point routines that perform functions equivalent to the R3010 Floating Point Accelerator chip. The routines can be linked with output from any of the compilers listed below, and are ROMable. The execution time is roughly 30 times that required by the R3010. The Developmental Use License and copies of the software in one or more media should be ordered separately. The license must be signed before the software is shipped.

Developmental Use License	7RS905BLV
<i>Permits purchase of up to six copies of the software in any media, and permits up to six copies running in developmental machines, but does not permit inclusion of code in an end product.</i>	
Binary Distribution Right	7RS905BLP-L
<i>Permits unlimited, royalty free distribution of run-times containing the Floating Point Library .</i>	
For use with 7RS903BAF-N (PC)	7RS905BAF-L
For use with MacStation	7RS905BMD-N
For use with MIPS machine, RISC/os	7RS905BUU-L
For use with 7RS903BXX (386 Xenix Disc)	7RS905BXX-L
For use with 7RS903BYX (286 Xenix Disc)	7RS905BYX-L
Binary Distribution Rights	7RS905BLP
<i>Permits royalty-free distribution of run-time code.</i>	
Maintenance	7RS905BSY
<i>One year free updates</i>	



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