



# Intel<sup>®</sup> 450NX PCIset

**82454NX PCI Expander Bridge (PXB)**

**82453NX Data Path Multiplexor (MUX)**

**82452NX RAS/CAS Generator (RCG)**

**82451NX Memory & I/O Controller (MIOC)**

**Order Number: 243771-004**

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## 1.1 Overview

The Intel® 450NX PCIset provides an integrated Host-to-PCI bridge and memory controller optimized for multiprocessor systems and standard high-volume (SHV) servers based on the Pentium® II Xeon™ processor variant of the P6 family. The Intel 450NX PCIset consists of four components: 82454NX PCI Expander Bridge (PXB), 82451NX Memory and I/O Bridge Controller (MIOC), 82452NX RAS/CAS Generator (RCG), and 82453NX Data Path Multiplexor (MUX). Figure 1-1 illustrates a typical SHV server system based on the Intel 450NX PCIset. The system bus interface supports up to 4 Pentium II Xeon processors at 100 MHz. An additional bus mastering agent such as a cluster bridge can be supported at reduced frequencies. Two dedicated PCI Expander Bridges (PXBs) can be connected via the Expander

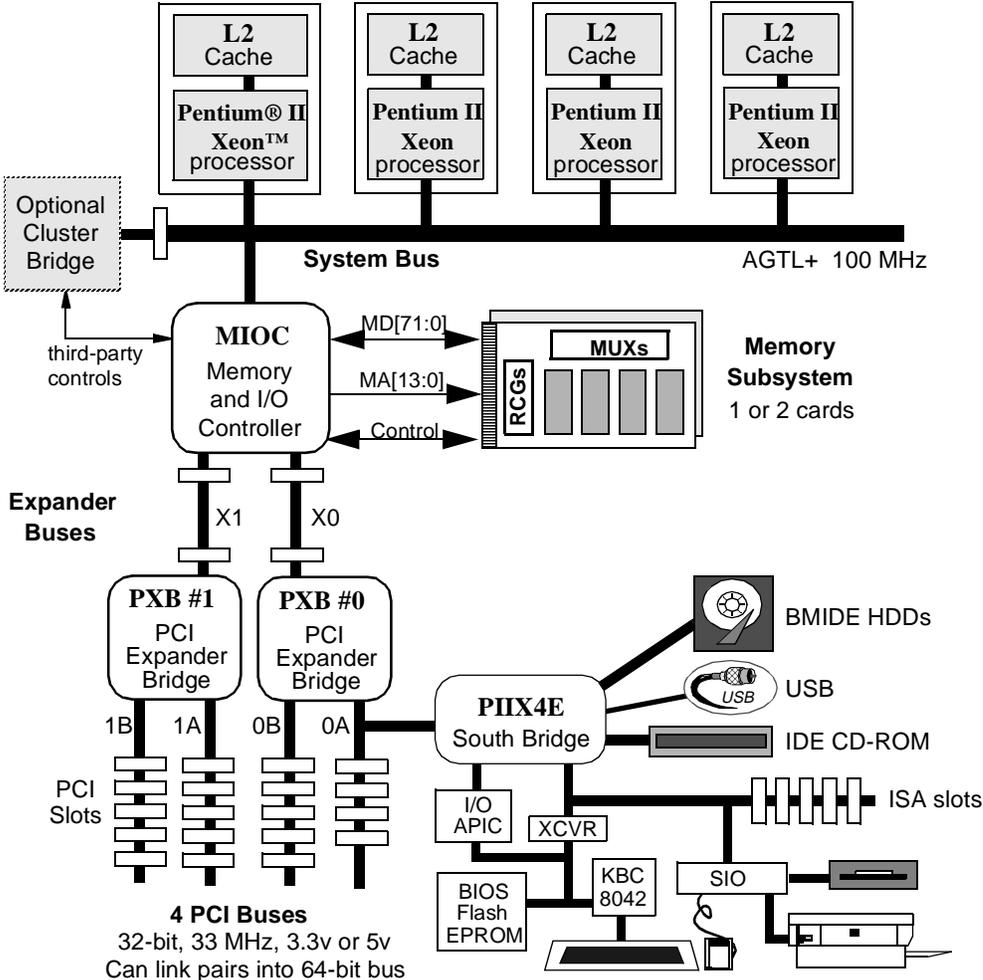


Figure 1-1: Simplified Intel® 450NX PCIset System Block Diagram

Bus. Each PXB provides two independent 32-bit, 33 MHz PCI buses, with an option to link the two buses into a single 64-bit, 33 MHz bus. The Intel 450NX PCIset memory subsystem supports one or two memory cards. Each card is comprised of an RCG, a DRAM array, and two MUXs. The MIOC issues requests to the RCG components on each card to generate RAS#, CAS#, and WE# outputs to the DRAMs. The MUX components provide the datapath for the DRAM arrays. Up to 8 GB of memory in various configurations are supported.

Other capabilities of the Intel 450NX PCIset include:

- Full Pentium® II Xeon™ processor bus interface (36-bit address, 64-bit data) at 100 MHz.
- Support for two dedicated PCI expander bridges (PXBs) attached *behind* the system bus so as not to add additional electrical load to the system bus.
- Support for both internal and external system bus and I/O bus arbitration.

### Supporting Devices

The Intel 450NX PCIset is designed to support the PIIX4E south bridge. The PIIX4E is a highly integrated multi-functional component that supports the following capabilities:

- PCI Rev 2.1-compliant PCI-to-ISA Bridge with support for 33-MHz PCI operations
- Enhanced DMA controller
- 8259 Compatible Programmable Interrupt Controller
- System Timer functions
- Integrated IDE controller with Ultra DMA/33 support

## 1.2 Intel® 450NX PCIset Components

### MIOC Memory and I/O Bridge Controller

The MIOC accepts access requests from the system bus and directs those accesses to memory or one of the PCI buses. The MIOC also accepts inbound requests from the PCI buses. The MIOC provides the data port and buffering for data transferred between the system bus, PXBs and memory. In addition, the MIOC generates the appropriate controls to the RCG and MUX components to control data transfer to and from the memory.

### PXB PCI Expander Bridge

The PXB provides the interface to two independent 32-bit, 33 MHz Rev 2.1-compliant PCI buses. The PXB is both a master and target on each PCI bus.

### RCG RAS/CAS Generator

The RCG is responsible for accepting memory requests from the MIOC and converting these into the specific signals and timings required by the DRAM. Each RCG controls up to four banks of memory.

### MUX Data Path Multiplexor

The MUX provides the multiplexing and staging required to support memory interleaving between the DRAMs and the MIOC. Each MUX provides the data path for one-half of a Qword for each of four interleaves.

## 1.3 Intel® 450NX PCIset Feature Summary

### System Bus Support

- Fully supports the Pentium® II Xeon™ processor bus protocol at bus frequencies up to 100 MHz.
- Functionally and electrically compatible with the original and Pentium II P6 family processor buses.
- Fully supports 4-way multiprocessing, with performance scaling to 3.5x that of a uni-processor system.
- Full 36-bit address decode and drive capability.
- Full 64-bit data bus (32-bit data bus mode is not supported).
- Parity protection on address and control signals, ECC protection on data signals.
- 8-deep in-order queue; 24-deep memory request queue; 2-deep outbound read-request queue per PCI bus; 6-deep outbound write-posting queue per PCI bus.
- AGTL+ bus driver technology.
- Intel® 450NX PCIset adds only one load to the system bus.
- Intel 450GX PCIset-compatible third-party request/grant and control signals, allowing cluster bridges to be placed on the system bus.

### DRAM Interface Support

- Memory technologies supported are 16- and 64-Mbit, 60nsec and 50nsec 3.3v EDO DRAM devices.
- Supports from 32 MB to 8 GB of memory, in 64 MB increments after the initial 32 MB.
- Supports 4-way interleaved operation, with 2-way interleave supported in the first bank of card 0 to permit entry-level systems with minimal memory.
- Supports memory address bit permuting (ABP) to obtain alternate row selection bits.
- Supports card-to-card interleaving to further distribute memory accesses across multiple banks of memory.
- Staggered CAS-before-RAS refresh.
- ECC with single-bit error correction and scrub-on-error in the memory.
- Extensive Host-to-Memory and PCI-to-Memory write data buffering.

### I/O Bridge Support

- Up to four independent 32-bit PCI ports (using two PXBs)
  - each supports up to 10 electrical loads (connectors count as loads).
  - each provides internal arbitration for up to 6 masters plus a south bridge on the compatibility PCI bus, or external arbitration.
- Synchronous operation to the system bus clock using a 3:1 system bus/PCI bus gearing ratio.
  - 3:1 ratio supports a 100 MHz system bus and 33.33 MHz PCI bus.
  - 3:1 ratio supports a 90 MHz system bus and 30 MHz PCI bus (or lower, depending on effect of 6th load).
- Parity protection on all PCI signals.
- Inbound read prefetches of up to 4 cache lines.
- Outbound write assembly of full/partial line writes.
- Data streaming support from PCI to DRAM.

**System Management Features**

- Provides controlled access to the Intel Architecture System Management Mode (SMM) memory space (SM RAM).

**Test & Tuning Features**

- Signal interconnectivity testing via boundary scan.
- Access to internal control and status registers via JTAG TAP port. I2C access is *not* provided in the PCIset; however, error indicators are reported to pins which can be monitored and sampled using I2C capabilities if provided elsewhere in the system.
- System bus, memory and I/O performance counters with programmable events.

**Reliability/Availability/Serviceability (RAS) Features**

- ECC coverage of system data bus and memory; parity coverage of system bus controls, PCI bus, and Expander bus.
- ECC bits can be corrupted via selective masking for diagnostics.
- Fault recording of the first two ECC errors. Each includes error type and syndrome. Memory ECC error logs include the effective address, allowing identification of the failing location. Error logs are not affected by reset, allowing recovery software to examine the logs.

## 1.4 Packaging & Power

- Table 1-1 indicates the signal count, package and power for each component in the Intel® 450NX PCIset. In a common high-end configuration, using two memory cards (each with one RCG and two MUX components), two PXBs and 3.3 V supplies, the Intel 450NX PCIset would contribute approximately 47 watts.

**Table 1-1: Signals, Pins, Packaging and Power**

| Chip | Signals | Package               | Footprint | Power <sup>1</sup> |
|------|---------|-----------------------|-----------|--------------------|
| MIOC | 348     | PLGA-540 <sup>2</sup> | 42.5 mm   | 13.2 W             |
| PXB  | 177     | PLGA-540 <sup>2</sup> | 42.5 mm   | 7.8 W              |
| RCG  | 173     | BGA-324               | 27.0 mm   | 2.5 W              |
| MUX  | 207     | BGA-324               | 27.0 mm   | 3.3 W              |

Notes:

1. Assumes 3.3 V supplies.
2. Requires heat sink.

This chapter provides a detailed description of all signals used in any component in the Intel® 450NX PCIset.

## 2.1 Conventions

The terms *assertion* and *deassertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *deassert*, or *deassertion*, indicates that the signal is inactive.

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name the signal is asserted when at the high voltage level.

When discussing data values used inside the chip set, the *logical* value is used; i.e., a data value described as "1101b" would appear as "1101b" on an active-high bus, and as "0010b" on an active-low bus. When discussing the assertion of a value on the actual pin, the physical value is used; i.e., asserting an active-low signal produces a "0" value on the pin.

The following notations are used to describe the signal type:

|            |                                                  |
|------------|--------------------------------------------------|
| <b>I</b>   | Input pin                                        |
| <b>O</b>   | Output pin                                       |
| <b>I/O</b> | Bidirectional (input/output) pin                 |
| <b>OD</b>  | Open drain output pin (other than AGTL+ signals) |

The signal description also includes the type of buffer used for the particular signal:

|               |                                                          |
|---------------|----------------------------------------------------------|
| <b>AGTL+</b>  | Open drain AGTL+ interface.                              |
| <b>PCI</b>    | PCI-compliant 3.3 V/5 V-tolerant interface               |
| <b>LVTTTL</b> | Low-voltage (3.3 V) TTL-compatible signals.              |
| <b>2.5V</b>   | 2.5 V CMOS signals.                                      |
| <b>Analog</b> | Typically a voltage reference or specialty power supply. |

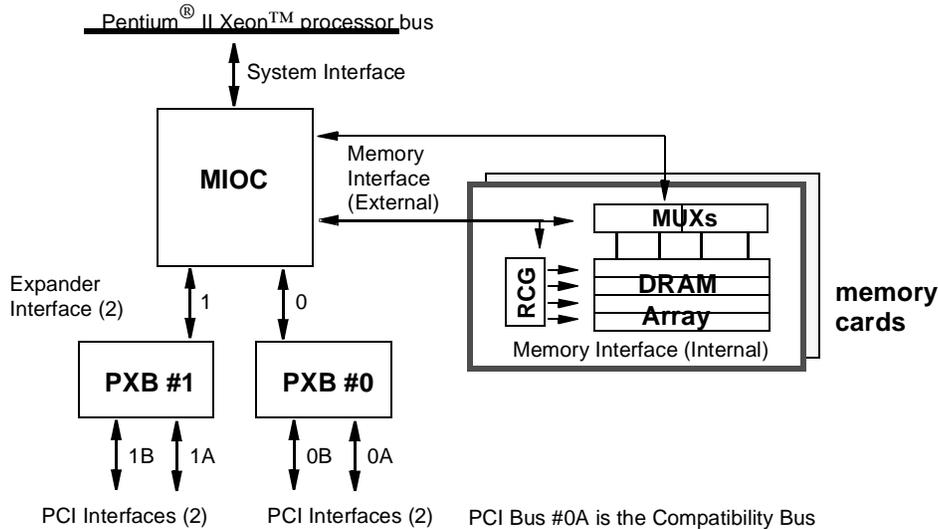
Some signals or groups of signals have multiple versions. These signal groups may represent distinct but similar ports or interfaces, or may represent identical copies of the signal used to reduce loading effects. The following conventions are used:

- RR(A,B,C)XX expands to: RRAXX, RRBXX, and RRCXX
- RR(A,...,D)XX expands to: RRAXX, RRBXX, RRCXX, and RRDXX
- RRpXX, where p=A,B,C expands to: RRAXX, RRBXX, and RRCXX

Typically, *upper case* groups (e.g., "(A,B,C)") represent functionally similar but logically distinct signals; each signal provides an independent control, and may or may not be asserted at the same time as the other signals in the grouping. In contrast, *lower case* groups (e.g., "(a,b,c)") typically represent identical duplicates of a common signal provided to reduce loading.

## 2.2 Summary

Figure 2-1 illustrates the partitioning of interfaces across the components in the Intel® 450NX PCIsset. The remainder of this section lists the signals and signal counts in each interface by component. The signal functions are described in subsequent sections.



**Figure 2-1: Interface Summary: Partitioning**

### 2.2.1 Signal Summary, By Component

The following tables provide summary lists of all signals in each component, sorted alphabetically within interface type. The signals are described in a later section.

## 2.2.1.1 MIOC Signal List

| <b>System Interface</b>                       |             |              |           | <b>134</b>    |
|-----------------------------------------------|-------------|--------------|-----------|---------------|
| A[35:3]#                                      | AGTL+ I/O   | DEP[7:0]#    | AGTL+ I/O |               |
| ADS#                                          | AGTL+ I/O   | DRDY#        | AGTL+ I/O |               |
| AERR#                                         | AGTL+ I/O   | HIT#         | AGTL+ I   |               |
| AP[1:0]#                                      | AGTL+ I/O   | HITM#        | AGTL+ I   |               |
| BERR#                                         | AGTL+ I/O   | INIT#        | 2.5V OD   |               |
| BINIT#                                        | AGTL+ I/O   | LOCK#        | AGTL+ I   |               |
| BNR#                                          | AGTL+ I/O   | REQ[4:0]#    | AGTL+ I/O |               |
| BP[1:0]#                                      | LVTTTL I/OD | RP#          | AGTL+ I/O |               |
| BPRI#                                         | AGTL+ I/O   | RS[2:0]#     | AGTL+ I/O |               |
| BREQ[0]#                                      | AGTL+ O     | RSP#         | AGTL+ I/O |               |
| D[63:0]#                                      | AGTL+ I/O   | TRDY#        | AGTL+ I/O |               |
| DBSY#                                         | AGTL+ I/O   |              |           |               |
| DEFER#                                        | AGTL+ I/O   |              |           |               |
| <b>Third-Party Agent Interface</b>            |             |              |           | <b>4</b>      |
| IOGNT#                                        | LVTTTL I    | TPCTL[1:0]   | LVTTTL I  |               |
| IOREQ#                                        | LVTTTL O    |              |           |               |
| <b>Memory Subsystem / External Interface</b>  |             |              |           | <b>119</b>    |
| BANK[2:0]#                                    | AGTL+ O     | DVALID(a,b)# | AGTL+ O   |               |
| CARD[1:0]#                                    | AGTL+ O     | MA[13:0]#    | AGTL+ O   |               |
| CMND[1:0]#                                    | AGTL+ O     | MD[71:0]#    | AGTL+ I/O |               |
| CSTB#                                         | AGTL+ O     | MRESET#      | AGTL+ O   |               |
| DCMPLT(a,b)#                                  | AGTL+ I/O   | PHIT(a,b)#   | AGTL+ I   |               |
| DOFF[1:0]#                                    | AGTL+ O     | ROW#         | AGTL+ O   |               |
| DSEL[1:0]#                                    | AGTL+ O     | RCMPLT(a,b)# | AGTL+ I   |               |
| DSTBN[3:0]#                                   | AGTL+ I/O   | RHIT(a,b)#   | AGTL+ I   |               |
| DSTBP[3:0]#                                   | AGTL+ I/O   | WDEVT#       | AGTL+ O   |               |
| <b>Expander Interface (two per MIOC: 0,1)</b> |             |              |           | <b>2 x 33</b> |
| X(0,1)ADS#                                    | AGTL+ I/O   | X(0,1)HSTBP# | AGTL+ O   |               |
| X(0,1)BE[1:0]#                                | AGTL+ I/O   | X(0,1)PAR#   | AGTL+ I/O |               |
| X(0,1)BLK#                                    | AGTL+ O     | X(0,1)RST#   | AGTL+ O   |               |
| X(0,1)CLK                                     | CMOS O      | X(0,1)RSTB#  | AGTL+ O   |               |
| X(0,1)CLKB                                    | CMOS O      | X(0,1)RSTFB# | AGTL+ I   |               |
| X(0,1)CLKFB                                   | CMOS I      | X(0,1)XRST#  | AGTL+ I   |               |
| X(0,1)D[15:0]#                                | AGTL+ I/O   | X(0,1)XSTBN# | AGTL+ I   |               |
| X(0,1)HRST#                                   | AGTL+ O     | X(0,1)XSTBP# | AGTL+ I   |               |
| X(0,1)HSTBN#                                  | AGTL+ O     |              |           |               |
| <b>Common Support Signals</b>                 |             |              |           | <b>16</b>     |
| CRES[1:0]                                     | Analog I    | TMS          | 2.5V I    |               |
| TCK                                           | 2.5V I      | TRST#        | 2.5V I    |               |
| TDI                                           | 2.5V I      | VCCA (3)     | Analog I  |               |
| TDO                                           | 2.5V OD     | VREF (6)     | Analog I  |               |

| Component-Specific Support Signals |        |      |         |        | 9          |
|------------------------------------|--------|------|---------|--------|------------|
| CRESET#                            | LVTTTL | O    | PWRGD   | LVTTTL | I          |
| ERR[1:0]#                          | LVTTTL | I/OD | PWRGDB  | LVTTTL | O          |
| HCLKIN                             | 2.5V   | I    | RESET#  | AGTL+  | I/O        |
| INTREQ#                            | LVTTTL | O    | SMIACT# | LVTTTL | O          |
| <b>TOTAL SIGNALS</b>               |        |      |         |        | <b>348</b> |

## 2.2.1.2 PXB Signal List

| PCI Bus Interface (2 per PXB: A,B)                   |        |      |                 |        | 2 x 61     |
|------------------------------------------------------|--------|------|-----------------|--------|------------|
| P(A,B)AD[31:0]                                       | PCI    | I/O  | P(A,B)PAR       | PCI    | I/O        |
| P(A,B)C/BE[3:0]#                                     | PCI    | I/O  | P(A,B)PERR#     | PCI    | I/O        |
| P(A,B)CLKFB                                          | LVTTTL | I    | P(A,B)REQ[5:0]# | PCI    | I          |
| P(A,B)CLK                                            | LVTTTL | O    | P(A,B)RST#      | PCI    | O          |
| P(A,B)DEVSEL#                                        | PCI    | I/O  | P(A,B)SERR#     | PCI    | OD         |
| P(A,B)FRAME#                                         | PCI    | I/O  | P(A,B)STOP#     | PCI    | I/O        |
| P(A,B)GNT[5:0]#                                      | PCI    | O    | P(A,B)TRDY#     | PCI    | I/O        |
| P(A,B)IRDY#                                          | PCI    | I/O  | P(A,B)XARB#     | PCI    | I          |
| P(A,B)LOCK#                                          | PCI    | I/O  |                 |        |            |
| PCI Bus Interface / Non-Duplicated (one set per PXB) |        |      |                 |        | 6          |
| ACK64#                                               | PCI    | I/O  | PHLDA#          | PCI    | O          |
| MODE64#                                              | PCI    | I    | REQ64#          | PCI    | I/O        |
| PHOLD#                                               | PCI    | I    | WSC#            | PCI    | O          |
| Expander Interface (one per PXB)                     |        |      |                 |        | 30         |
| XADS#                                                | AGTL+  | I/O  | XHSTBP#         | AGTL+  | I          |
| XBE[1:0]#                                            | AGTL+  | I/O  | XIB             | AGTL+  | O          |
| XBLK#                                                | AGTL+  | I    | XPAR#           | AGTL+  | I/O        |
| XCLK                                                 | CMOS   | I    | XRST#           | AGTL+  | I          |
| XD[15:0]#                                            | AGTL+  | I/O  | XXRTS#          | AGTL+  | O          |
| XHRTS#                                               | AGTL+  | I    | XXSTBN#         | AGTL+  | O          |
| XHSTBN#                                              | AGTL+  | I    | XXSTBP#         | AGTL+  | O          |
| Common Support Signals                               |        |      |                 |        | 12         |
| CRES[1:0]                                            | Analog | I    | TMS             | 2.5V   | I          |
| TCK                                                  | 2.5V   | I    | TRST#           | 2.5V   | I          |
| TDI                                                  | 2.5V   | I    | VCCA (3)        | Analog | I          |
| TDO                                                  | 2.5V   | OD   | VREF (2)        | Analog | I          |
| Component-Specific Support Signals                   |        |      |                 |        | 8          |
| INTRQ(A,B)#                                          | PCI    | OD   | PIIXOK#         | LVTTTL | I          |
| P(A,B)MON[1:0]#                                      | LVTTTL | I/OD | PWRGD           | LVTTTL | I          |
| <b>TOTAL SIGNALS</b>                                 |        |      |                 |        | <b>177</b> |

## 2.2.1.3 RCG Signal List

| Memory Subsystem / External Interface |           |                             |          | 27  |
|---------------------------------------|-----------|-----------------------------|----------|-----|
| BANK[2:0]#                            | AGTL+ I   | MRESET#                     | AGTL+ I  |     |
| CARD#                                 | AGTL+ I   | PHIT#                       | AGTL+ O  |     |
| CMND[1:0]#                            | AGTL+ I   | RCMPLT#                     | AGTL+ O  |     |
| CSTB#                                 | AGTL+ I   | RHIT#                       | AGTL+ O  |     |
| GRCMPLT#                              | AGTL+ I/O | ROW#                        | AGTL+ I  |     |
| MA[13:0]#                             | AGTL+ I   |                             |          |     |
| Memory Subsystem / Internal Interface |           |                             |          | 123 |
| ADDR(A,B,C,D)[13:0]                   | LVTTTL O  | LRD#                        | AGTL+ O  |     |
| AVWP#                                 | AGTL+ O   | RAS(A,B,C,D)(a,b,c,d)[1:0]# | LVTTTL O |     |
| CAS(A,B,C,D)(a,b,c,d)[1:0]#           | LVTTTL O  | WDME#                       | AGTL+ O  |     |
| LDSTB#                                | AGTL+ O   | WE(A,B,C,D)(a,b)#           | LVTTTL O |     |
| Common Support Signals                |           |                             |          | 10  |
| CRES[1:0]                             | Analog I  | TMS                         | 2.5 V I  |     |
| TCK                                   | 2.5V I    | TRST#                       | 2.5 V I  |     |
| TDI                                   | 2.5V I    | VCCA                        | Analog I |     |
| TDO                                   | 2.5V OD   | VREF (2)                    | Analog I |     |
| Component-Specific Support Signals    |           |                             |          | 4   |
| BANKID#                               | LVTTTL I  | DR50T#                      | LVTTTL I |     |
| DR50H#                                | LVTTTL I  | HCLKIN                      | 2.5 V I  |     |
| TOTAL SIGNALS                         |           |                             |          | 173 |

## 2.2.1.4 MUX Signal List

| Memory Subsystem / External Interface |            |           |            | 48  |
|---------------------------------------|------------|-----------|------------|-----|
| DCMPLT#                               | AGTL+ I/O  | DVALID#   | AGTL+ I    |     |
| DOFF[1:0]#                            | AGTL+ I    | GDCMPLT#  | AGTL+ I/O  |     |
| DSEL#                                 | AGTL+ I    | MD[35:0]# | AGTL+ I/O  |     |
| DSTBP[1:0]#                           | AGTL+ I/O  | MRESET#   | AGTL+ I    |     |
| DSTBN[1:0]#                           | AGTL+ I/O  | WDEVT#    | AGTL+ I    |     |
| Memory Subsystem / Internal Interface |            |           |            | 148 |
| AVWP#                                 | AGTL+ I    | Q1D[35:0] | LVTTTL I/O |     |
| LDSTB#                                | AGTL+ I    | Q2D[35:0] | LVTTTL I/O |     |
| LRD#                                  | AGTL+ I    | Q3D[35:0] | LVTTTL I/O |     |
| Q0D[35:0]                             | LVTTTL I/O | WDME#     | AGTL+ I    |     |
| Common Support Signals                |            |           |            | 10  |
| CRES[1:0]                             | Analog I   | TMS       | 2.5 V I    |     |
| TCK                                   | 2.5 V I    | TRST#     | 2.5 V I    |     |
| TDI                                   | 2.5 V I    | VCCA      | Analog I   |     |
| TDO                                   | 2.5 V OD   | VREF (2)  | Analog I   |     |
| Component-Specific Support Signals    |            |           |            | 1   |
| HCLKIN                                | 2.5 V I    |           |            |     |
| TOTAL SIGNALS                         |            |           |            | 207 |

## 2.3 System Interface

The MIOC provides the Intel<sup>®</sup> 450NX PCIset's sole connection to the system bus. This section describes the Intel 450NX PCIset-specific uses of these signals.

### 2.3.1 System / MIOC Interface

|          |                                                                                                                                                                                                                                                             |            |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| A[35:3]# | <b>Address Bus</b><br>A[35:3]# connect to the system address bus. During processor cycles the A[35:3]# are inputs. The MIOC drives A[35:3]# during snoop cycles on behalf of PCI initiators. The address bus is inverted on the system bus.                 | AGTL+ I/O  |
| ADS#     | <b>Address Strobe</b><br>The system bus owner asserts ADS# to indicate the first of two cycles of a <i>request phase</i> .                                                                                                                                  | AGTL+ I/O  |
| AERR#    | <b>Address Parity Error</b><br>AERR# is asserted by any agent that detects an address parity error.                                                                                                                                                         | AGTL+ I/O  |
| AP[1:0]# | <b>Address Parity</b><br>Parity protection on the address bus. AP#[1] covers A#[35:24], and AP#[0] covers A#[23:3]. They are valid on both cycles of the request.                                                                                           | AGTL+ I/O  |
| BERR#    | <b>Bus Error</b><br>This signal is asserted by any agent that observes an unrecoverable bus protocol violation.                                                                                                                                             | AGTL+ I/O  |
| BINIT#   | <b>Bus Initialization</b><br>BINIT# is asserted to re-initialize the bus state machines. The MIOC will terminate any ongoing PCI transaction and reset its inbound and outbound queues. No configuration registers or error logging registers are affected. | AGTL+ I/O  |
| BNR#     | <b>Block Next Request</b><br>Used to block the current request bus owner from issuing a new request.                                                                                                                                                        | AGTL+ I/O  |
| BP[1:0]# | <b>Performance Monitoring</b><br>In normal operation, the MIOC can be configured to drive performance monitoring data out of either of these pins, similar in function to the BP pins provided on the processors.                                           | LVTTL I/OD |
| BPRI#    | <b>Priority Agent Bus Request</b><br>The MIOC is the only Priority Agent on the system bus. It asserts this signal to obtain ownership of the address bus. BPRI# has priority over symmetric bus requests.                                                  | AGTL+ O    |
| BREQ[0]# | <b>Symmetric Agent Bus Request</b><br>This signal is asserted by the MIOC when RESET# is asserted, to select the boot processor. It is deasserted 2 host clocks after RESET# is deasserted.                                                                 | AGTL+ O    |

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                      |           |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|-----|--------------|-----|-------|-----|---------|-----|----------|-----|--------------------|-----|-----------------|-----|-------------|-----------|
| D[63:0]#  | <b>Data</b><br>These signals are connected to the system data bus. The data signals are inverted on the system bus.                                                                                                                                                                                                                                                                                                                                  | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| DBSY#     | <b>Data Bus Busy</b><br>Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.                                                                                                                                                                                                                                                                                                                                 | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| DEP[7:0]# | <b>Data Bus ECC/Parity</b><br>These signals provide parity or ECC for the D#[63:0] signals. The MIOC only provides ECC.                                                                                                                                                                                                                                                                                                                              | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| DEFER#    | <b>Defer</b><br>DEFER# is driven by the addressed agent to indicate that the transaction cannot be guaranteed to be globally observed.                                                                                                                                                                                                                                                                                                               | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| DRDY#     | <b>Data Ready</b><br>Asserted for each cycle that valid data is transferred.                                                                                                                                                                                                                                                                                                                                                                         | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| HIT#      | <b>Hit</b><br>The MIOC never asserts HIT#; it has no cache, and never snoop stalls.                                                                                                                                                                                                                                                                                                                                                                  | AGTL+ I   |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| HITM#     | <b>Hit Modified</b><br>The MIOC never asserts HITM#; it has no cache, and never snoop stalls.                                                                                                                                                                                                                                                                                                                                                        | AGTL+ I   |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| INIT#     | <b>Soft Reset</b><br>INIT# may be asserted to request a soft reset of the processors. During a system hard reset, the INIT# signal may be optionally asserted to cause the processors to initiate their BIST. The INIT# signal is <i>not</i> asserted during power-good reset.                                                                                                                                                                       | 2.5V OD   |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| LOCK#     | <b>Lock</b><br>All system bus cycles sampled with the assertion of LOCK# and ADS#, until the negation of LOCK#, must be atomic; i.e., no PCI activity to DRAM is allowed and the locked cycle must be translated to PCI if targeted for the PCI bus.                                                                                                                                                                                                 | AGTL+ I   |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| REQ[4:0]# | <b>Request Command</b><br>Asserted during both clocks of a request phase. In the first clock, the signals define the transaction type to a level which is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.                                                                                                                                                | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| RP#       | <b>Request Parity</b><br>Even parity protection on ADS# and REQ[4:0]#. It is valid on both cycles of the request.                                                                                                                                                                                                                                                                                                                                    | AGTL+ I/O |                    |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| RS[2:0]#  | <b>Response Signals</b><br>Indicate response type as shown below:<br><table border="0" style="margin-left: 2em;"> <tr> <td>000</td> <td>Idle state</td> <td>100</td> <td>Hard failure</td> </tr> <tr> <td>001</td> <td>Retry</td> <td>101</td> <td>No Data</td> </tr> <tr> <td>010</td> <td>Deferred</td> <td>110</td> <td>Implicit writeback</td> </tr> <tr> <td>011</td> <td><i>reserved</i></td> <td>111</td> <td>Normal Data</td> </tr> </table> | 000       | Idle state         | 100 | Hard failure | 001 | Retry | 101 | No Data | 010 | Deferred | 110 | Implicit writeback | 011 | <i>reserved</i> | 111 | Normal Data | AGTL+ I/O |
| 000       | Idle state                                                                                                                                                                                                                                                                                                                                                                                                                                           | 100       | Hard failure       |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| 001       | Retry                                                                                                                                                                                                                                                                                                                                                                                                                                                | 101       | No Data            |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| 010       | Deferred                                                                                                                                                                                                                                                                                                                                                                                                                                             | 110       | Implicit writeback |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |
| 011       | <i>reserved</i>                                                                                                                                                                                                                                                                                                                                                                                                                                      | 111       | Normal Data        |     |              |     |       |     |         |     |          |     |                    |     |                 |     |             |           |

|       |                                                                                                                      |           |
|-------|----------------------------------------------------------------------------------------------------------------------|-----------|
| RSP#  | <b>Response Parity Signal</b><br>Parity protection on RS[2:0]#.                                                      | AGTL+ I/O |
| TRDY# | <b>Target Ready</b><br>Indicates that the target of the system transaction is able to enter the data transfer phase. | AGTL+ I/O |

## 2.3.2 Third-Party Agent / MIOC Interface

The following signals provide support for an additional non-processor, third-party agent (TPA) on the system bus. Such agents may need priority access to the system bus itself, or may need to intervene in transactions between the processors and the Intel® 450NX PCIset.

|            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |         |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| IOGNT#     | <b>I/O Grant</b><br>The IOGNT# signal has two modes: Internal Arbitration Mode and External Arbitration Mode, selected by a bit in the MIOC's CONFIG register. In Internal Arbitration Mode IOGNT# is an input from another bridge device which is requesting ownership of the BPRI# signal. In external arbitration mode, this bridge requests BPRI# ownership from an external bridge arbiter. IOGNT# should be asserted by the external arbiter when this MIOC has been granted ownership of the BPRI# signal. | LVTTL I |
| IOREQ#     | <b>I/O Request</b><br>The IOREQ# signal has two modes: Internal Arbitration Mode and External Arbitration Mode, selected by a bit in the MIOC's CONFIG register. In Internal Arbitration Mode IOREQ# is the grant to another bridge device that is making a request for ownership of the BPRI# signal. In external arbitration mode this signal is asserted to request ownership of the BPRI# signal.                                                                                                             | LVTTL O |
| TPCTL[1:0] | <b>Third Party Control</b><br>These signals allow an agent participating in transactions between the Intel® 450NX PCIset and another bus agent as a "third-party" to control the responses generated by the Intel 450NX PCIset.                                                                                                                                                                                                                                                                                   | LVTTL I |
|            | 00 <b>Accept</b> The MIOC will accept the request and provide the normal response.                                                                                                                                                                                                                                                                                                                                                                                                                                |         |
|            | 01 <i>reserved</i> -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         |
|            | 10 <b>Retry</b> The MIOC will generate a RETRY response.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |
|            | 11 <b>Defer</b> The MIOC will generate a DEFERRED response.                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |

## 2.4 PCI Interface

### 2.4.1 Primary Bus

There are two primary PCI buses per PXB, identified as the "a" bus and the "b" bus groups. Each signal name includes a "p", indicating the PCI bus port; **p = A or B**.

|                     |                                                                                                                                                                                                                                                                                                                                              |         |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PpAD[31:0]</b>   | <b>PCI Address/Data</b><br>PCI Address and Data signals are multiplexed on this bus. The physical byte address is output during the address phase and the data follows in the subsequent data phase(s).                                                                                                                                      | PCI I/O |
| <b>PpC/BE[3:0]#</b> | <b>Command/Byte Enable</b><br>PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables.                                                                                             | PCI I/O |
| <b>PpCLK</b>        | <b>PCI Clock</b><br>This signal is an output with a derived frequency equal to 1/3 of the system bus frequency.                                                                                                                                                                                                                              | LVTTL O |
| <b>PpCLKFB</b>      | <b>PCI Clock Feedback</b><br>This signal is connected to the output of a low skew PCI clock buffer tree. It is used to synchronize the PCI clock driven from PpCLK to the clock used for the internal PCI logic.                                                                                                                             | LVTTL I |
| <b>PpDEVSEL#</b>    | <b>Device Select</b><br>DEVSEL# is driven by the device that has decoded its address as the target of the current access.                                                                                                                                                                                                                    | PCI I/O |
| <b>PpFRAME#</b>     | <b>Frame</b><br>The PXB asserts FRAME# to indicate the start of a bus transaction. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the PXB acts as a PCI target.                                                                              | PCI I/O |
| <b>PpIRDY#</b>      | <b>Initiator Ready</b><br>This signal is asserted by a master to indicate its ability to complete the current data transfer. IRDY# is an output when the PXB acts as a PCI initiator and an input when the PXB acts as a PCI target.                                                                                                         | PCI I/O |
| <b>PpPAR</b>        | <b>Parity</b><br>PAR is driven by the PXB when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the PXB when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#. | PCI I/O |
| <b>PpRST#</b>       | <b>PCI Reset</b><br>PCI Bus Reset forces the PCI interfaces of each device to a known state. The PXB generates a minimum 1 ms pulse on RST#.                                                                                                                                                                                                 | PCI O   |
| <b>PpPERR#</b>      | <b>PCI Parity Error</b><br>Pulsed by an agent receiving data with bad parity one clock after PAR is asserted. The PXB will generate PERR# active if it detects a parity error on the PCI bus and the PERR# Enable bit in the PCICMD register is set.                                                                                         | PCI I/O |
| <b>PpLOCK#</b>      | <b>Lock</b><br>LOCK# indicates an exclusive bus operation and may require multiple transactions to complete. It is possible for different agents to use the PCI Bus while a single initiator retains ownership of the LOCK# signal.                                                                                                          | PCI I/O |

|                |                                                                                                                                                                                                                                                |         |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>PpTRDY#</b> | <b>Target Ready</b><br>The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is an input when the PXB acts as a PCI master and an output when the PXB acts as a PCI target. | PCI I/O |
| <b>PpSERR#</b> | <b>System Error</b><br>The PXB asserts this signal to indicate an error condition.                                                                                                                                                             | PCI OD  |
| <b>PpSTOP#</b> | <b>Stop</b><br>STOP# is used for disconnect, retry, and abort sequences on the PCI Bus. It is an input when the PXB acts as a PCI initiator and an output when the PXB acts as a PCI target.                                                   | PCI I/O |

## 2.4.2 64-bit Access Support

These signals are used only in 64-bit bus mode. There is one set per PXB.

|                |                                                                                                                                                                                                                                                                                                                                                                                                             |         |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>ACK64#</b>  | <b>64-bit Access Acknowledge</b><br>This signal is driven by the accessed target to indicate its willingness to transfer 64-bit data. When the PXB is the bus target, this signal is an output. If asserted, the PXB will transfer 64-bit data; otherwise, the PXB will transfer 32-bit data. When the PXB is the bus master, this signal is an input.                                                      | PCI I/O |
| <b>MODE64#</b> | <b>64-bit Bus Mode</b><br>A strapping pin that selects whether the pair of 32-bit PCI buses are used as two independent 32-bit buses, or linked together as a single 64-bit bus. If asserted, the buses are used as a single 64-bit bus: the 32-bit data bus of the PCI "B" port becomes the high Dword of the 64-bit bus. An internal pull-up insures that the pin appears deasserted if left unconnected. | PCI I   |
| <b>REQ64#</b>  | <b>64-bit Access Request</b><br>This signal is driven by the bus master to indicate it's desire to transfer 64-bit data. When the PXB is the bus master, this signal is an output. The PXB will assert this signal if it can transfer 64-bit data. When the PXB is the bus target, this signal is an input.                                                                                                 | PCI I/O |

The following 64-bit extension signals are mapped from the existing "B" port signals:

|           |      |             |
|-----------|------|-------------|
| AD[63:32] | from | PBAD[31:0]  |
| C/BE[7:4] | from | PBC/BE[3:0] |
| PAR64     | from | PBPAR       |

All other controls and status signals in 64-bit operation are taken from the Bus "A" signal set. Unused pins on the "B" side should be tied inactive.

## 2.4.3 Internal vs. External Arbitration

Each PXB supports both internal arbitration and external arbitration, independently for each PCI bus. While in internal arbitration mode, six pairs of request/grant signals are used to support up to six PCI masters on the bus (plus the PXB itself, and the PIIX4E south bridge on

the compatibility PCI bus). While in external arbitration mode, only one pair (#0) are used, and have different meanings.

Each signal name includes a “p”, indicating the PCI bus port; **p = A or B**.

**PpXARB# External Arbitration Mode** PCI I  
A strapping pin, sampled at the trailing edge of reset. If asserted, the PCI bus is controlled using an external arbiter. If deasserted, the PCI bus is controlled using the PXB’s internal arbiter. An internal pull-up insures that the pin appears deasserted if left unconnected.

#### Internal Arbitration Mode (per PCI bus, p=A,B)

**PpREQ[5:0]# PCI Bus Request** PCI I  
Six independent PCI bus request signals used by the internal PCI arbiter for PCI initiator arbitration. Unused signals should be strapped inactive.

**PpGNT[5:0]# PCI Grant** PCI O  
Six independent PCI bus grant signals used by the internal PCI arbiter for PCI initiator arbitration.

#### External Arbitration Mode (per PCI bus, p=A,B)

When operating in external arbitration mode, REQ[5:1]# and GNT[5:1]# signals are not used. The REQ[0]# signal is redefined as HGNT#, and the GNT[0]# signal is redefined as HREQ#.

**PpHREQ# Host Request** PCI O  
Generated by the PXB to the external PCI arbiter to request control of the PCI bus to perform a Host-PCI access.

**PpHGNT# Host Grant** PCI I  
Generated by the external PCI arbiter to grant the PCI bus to the PXB to perform a Host-PCI transfer.

## 2.4.4 PIIX4E Interface

The compatibility PCI bus (PCI Bus 0A) supports a PIIX4E south bridge, and requires several additional handshake signals, provided by the PXB. They are active only for Bus 0A.

#### NOTE

*These signals, and the associated PHOLDA# and WSC# protocols, cannot be used with the PXB in external arbiter mode.*

**PHOLD# PCI Hold** PCI I  
This signal is the PIIX4E’s request for the PCI bus.

**PHLDA# PCI Hold Acknowledge** PCI O  
This signal is driven by the PXB to grant PCI bus ownership to the PIIX4E.

|      |                                                                                                                                                                                                         |       |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WSC# | <b>Write Snoop Complete</b>                                                                                                                                                                             | PCI O |
|      | This signal is asserted active to indicate completion of snoop activity on the system bus on the behalf of the last PCI-DRAM write transaction, and that it is safe to send the APIC interrupt message. |       |

## 2.5 Memory Subsystem Interface

The memory subsystem is comprised of the DRAM arrays and the associated RCGs and MUXs. There is the external interface (between the MIOC and the memory subsystem), and the internal interface (between the various parts of the memory subsystem.)

### 2.5.1 External Interface

|            |                                                                                                                                                                                                                                                                                                              |                      |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| BANK[2:0]# | <b>Bank Selects</b>                                                                                                                                                                                                                                                                                          | AGTL+ MIOC→ RCG      |
|            | These signals indicate which memory bank will service this access. BANK[2:0]# are connected to all RCGs on both memory cards.                                                                                                                                                                                |                      |
| CARD[1:0]# | <b>Card Selects</b>                                                                                                                                                                                                                                                                                          | AGTL+ MIOC→ RCG      |
|            | These signals indicate which memory card will service this access. Valid patterns in the Intel® 450NX PCIsset are 01b=card0 and 10b=card1, allowing CARD[0]# to be connected only to card 0 and CARD[1]# to be connected only to card 1. Each CARD signal is connected to all RCGs on the given memory card. |                      |
| CMND[1:0]# | <b>Access Command</b>                                                                                                                                                                                                                                                                                        | AGTL+ MIOC→ RCG      |
|            | These signals encode the command of the current operation. CMND[1:0]# are connected to all RCGs on both memory cards.                                                                                                                                                                                        |                      |
| CSTB#      | <b>Command Strobe</b>                                                                                                                                                                                                                                                                                        | AGTL+ MIOC→ RCG      |
|            | This strobe, when activated, indicates the initiation of an access. This signal is connected to all RCGs on both memory cards.                                                                                                                                                                               |                      |
| MA[13:0]#  | <b>Memory Address bus</b>                                                                                                                                                                                                                                                                                    | AGTL+ MIOC→ RCG      |
|            | These signals define the address of the location to be accessed in the DRAM., and are driven on two successive clock cycles to provide up to 28 bits of effective memory address. The signals are connected to all RCGs on both memory cards.                                                                |                      |
| ROW#       | <b>Row Selects</b>                                                                                                                                                                                                                                                                                           | AGTL+ MIOC→ RCG      |
|            | These signals indicate which row in the selected memory bank will service this access. These signals are connected to all RCGs on both memory cards.                                                                                                                                                         |                      |
| GRCMPLT#   | <b>Global RCMPLT#</b>                                                                                                                                                                                                                                                                                        | AGTL+, I/O, all RCGs |
|            | A “global” version of the RCMPLT(a,b)# signals, asserted coincident with RCMPLT#, and by the same agent. Whereas each RCMPLT# signal connects the RCGs on one card with the MIOC, the GRCMPLT# signal connects the                                                                                           |                      |

RCGs across both cards while excluding the MIOC. This allows all RCGs to monitor each request completion without placing undue loading on the RCMPLT# signals.

|                            |                                                                                                                                                                                                                                                                                                        |                                  |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| MRESET#                    | <b>Memory Subsystem Reset</b>                                                                                                                                                                                                                                                                          | AGTL+ MIOC→ RCG/MUX              |
|                            | This signal represents a hard reset of the memory subsystem. It is asserted following PWRGD or upon the MIOC issuing a processor RESET due to software invocation.                                                                                                                                     |                                  |
| RCMPLTa#<br>RCMPLTb#       | <b>Request Complete</b>                                                                                                                                                                                                                                                                                | AGTL+ RCG→ MIOC                  |
|                            | This signal, which is driven by the currently active RCG, indicates the completion of a request into the memory array. Typically the “a” signal connects the MIOC and all RCGs on Card #0, while the “b” signal connects the MIOC and all RCGs on Card #1.                                             |                                  |
| PHIT(a,b)#<br>RHIT(a,b)#   | <b>Page and Row Hit Status</b>                                                                                                                                                                                                                                                                         | AGTL+ RCG→ MIOC                  |
|                            | These signals indicate what resource, if any, delayed the initiation of a read. Typically the “a” signal connects the MIOC and all RCGs on Card #0, while the “b” signal connects the MIOC and all RCGs on Card #1.                                                                                    |                                  |
| DSTBP[3:0]#<br>DSTBN[3:0]# | <b>Data Strobes</b>                                                                                                                                                                                                                                                                                    | AGTL+ MUX↔ MIOC                  |
|                            | This set of four signal-pairs are strobes which qualify the data transferred between the MUX and MIOC. Each strobe pair qualifies 18 bits (two bytes and two check bits), as follows:                                                                                                                  |                                  |
|                            | DSTB[0]# qualifies MD[17:00]#.                                                                                                                                                                                                                                                                         | DSTB[2]# qualifies MD[53:36]#.   |
|                            | DSTB[1]# qualifies MD[35:18]#.                                                                                                                                                                                                                                                                         | DSTB[3]# qualifies MD[71:54]#.   |
|                            | In a 4:1 interleaved system, with 2 MUXs per card, DSTB[1:0]# strobes the low MUX and DSTB[3:2]# strobes the high MUX. In a 2:1 interleaved system, with only a single MUX per card, DSTB[1:0]# strobes the MUX, and DSTB[3:2]# is not used.                                                           |                                  |
| MD[71:36]#<br>MD[35:00]#   | <b>Memory Data</b>                                                                                                                                                                                                                                                                                     | AGTL+ MUX↔ MIOC                  |
|                            | These signals are connected to the external datapath of the MUXs. Each MUX provides 36 bits of the 72-bit datapath to the MIOC.                                                                                                                                                                        |                                  |
| DCMPLTa#<br>DCMPLTb#       | <b>Data Transfer Complete</b>                                                                                                                                                                                                                                                                          | AGTL+ MUX→ MIOC/MUX<br>MIOC→MUXs |
|                            | This signal is driven by the source of the data transfer: the MIOC for writes, and the MUX for reads. DCMPLT# active indicates that the data transfer is complete. Typically the “a” signal connects the MIOC and all MUXs on Card #0, while the “b” signal connects the MIOC and all MUXs on Card #1. |                                  |
| DOFF[1:0]#                 | <b>Data Offset</b>                                                                                                                                                                                                                                                                                     | AGTL+ MIOC→ MUX                  |
|                            | These two bits, when qualified by the DVALID# signal, define the initial Qword access order for the data transfer. The result is that the critical chunk is accessed first and the remaining chunks are accessed in Intel “Toggle” order.                                                              |                                  |

|                      |                                                                                                                                                                                                                                                                                                                                                                                |                      |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| DSEL#                | <b>Data Card Select</b>                                                                                                                                                                                                                                                                                                                                                        | AGTL+ MIOC→ MUX      |
|                      | This signal, when qualified by the DVALID# signal, selects which card the memory transfer is coming from or destined towards. Each memory card uses a single DSEL# input, sent to each MUX on the card. The MIOC provides two DSEL# outputs (DSEL[1:0]#), one sent to each card.                                                                                               |                      |
| DVALIDa#<br>DVALIDb# | <b>Data Transfer Complete</b>                                                                                                                                                                                                                                                                                                                                                  | AGTL+ MIOC→ MUX      |
|                      | This signal indicates that the DSEL[1:0]#, DOFF[1:0]#, and WDEVT# signals are valid. Typically the “a” signal connects the MIOC and all MUXs on Card #0, while the “b” signal connects the MIOC and all MUXs on Card #1.                                                                                                                                                       |                      |
| GDCMPLT#             | <b>Global DCMPLT#</b>                                                                                                                                                                                                                                                                                                                                                          | AGTL+, I/O, all MUXs |
|                      | A “global” version of the DCMPLT(a,b)# signals, asserted coincident with DCMPLT#, and by the same agent. Whereas each DCMPLT# signal connects the MUXs on one card with the MIOC, the GDCMPLT# signal connects the MUXs across both cards while excluding the MIOC. This allows all MUXs to monitor each data completion without placing undue loading on the DCMPLT# signals. |                      |
| WDEVT#               | <b>Write Data Event</b>                                                                                                                                                                                                                                                                                                                                                        | AGTL+ MIOC→ MUX      |
|                      | This signal, when qualified by the DVALID# signal, indicates the type of data transfer command. If asserted, the command represents a write data transfer. If deasserted, the command represents a read data transfer.                                                                                                                                                         |                      |

## 2.5.2 Internal Interface

### 2.5.2.1 RCG / DRAM Interface

Each RCG provides four sets of signals to drive four banks in the DRAM array. In each of the following signal names, the “**B**” indicates a set of signals per bank. Each RCG controls four banks; therefore **B** = **A, B, C** or **D**.

|                                  |                                                                                                                                                                                                                                         |                  |
|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| CAS $\mathbf{B}$ (a,b,c,d)[1:0]# | <b>Column Address Strobes</b>                                                                                                                                                                                                           | LVTTTL RCG→ DRAM |
|                                  | These signals are used to latch the column address into the DRAMs. The “a”, “b”, “c” and “d” versions are duplicates for load reduction.                                                                                                |                  |
| ADDR $\mathbf{B}$ [13:0]         | <b>DRAM Address</b>                                                                                                                                                                                                                     | LVTTTL RCG→ DRAM |
|                                  | ADDR is used to provide the multiplexed row and column address to DRAM.                                                                                                                                                                 |                  |
| RAS $\mathbf{B}$ (a,b,c,d)[1:0]# | <b>Row Address Strobe</b>                                                                                                                                                                                                               | LVTTTL RCG→ DRAM |
|                                  | The RAS signals are used to latch the row address into the DRAMs. Each signal is used to select one DRAM row. The 1:0 signals indicate which row within the bank. The “a”, “b”, “c” and “d” versions are duplicates for load reduction. |                  |
| WE $\mathbf{B}$ (a,b)#           | <b>Write Enable Signal</b>                                                                                                                                                                                                              | LVTTTL RCG→ DRAM |
|                                  | WE# is asserted during writes to main memory. The “a” and “b” versions are duplicates for load reduction.                                                                                                                               |                  |

### 2.5.2.2 DRAM / MUX Interface

|           |                                                                                                                                                                   |                 |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| Q0D[35:0] | <b>Memory Data, Interleave 0</b><br>These signals are connected to the output of the DRAMs. This is one-half of a Quad-word and is connected to interleave zero.  | LVTTL DRAM↔ MUX |
| Q1D[35:0] | <b>Memory Data, Interleave 1</b><br>These signals are connected to the output of the DRAMs. This is one-half of a Quad-word and is connected to interleave one.   | LVTTL DRAM↔ MUX |
| Q2D[35:0] | <b>Memory Data, Interleave 2</b><br>These signals are connected to the output of the DRAMs. This is one-half of a Quad-word and is connected to interleave two.   | LVTTL DRAM↔ MUX |
| Q3D[35:0] | <b>Memory Data, Interleave 3</b><br>These signals are connected to the output of the DRAMs. This is one-half of a Quad-word and is connected to interleave three. | LVTTL DRAM↔ MUX |

### 2.5.2.3 RCG / MUX Interface

|        |                                                                                                               |                |
|--------|---------------------------------------------------------------------------------------------------------------|----------------|
| AVWP#  | <b>Advance MUX Write Path Pointers</b><br>This signal is activated by an RCG after performing a memory write. | AGTL+ RCG→ MUX |
| LDSTB# | <b>Load Data Strobe</b><br>This signal controls when read data is latched from the DRAM data bus.             | AGTL+ RCG→ MUX |
| LRD#   | <b>Load Read Data</b><br>This signal indicates when read data is ready to load from the DRAMs.                | AGTL+ RCG→ MUX |
| WDME#  | <b>Write Data to Memory Enable</b><br>This signal enables the MUXes to drive write data to the DRAMs.         | AGTL+ RCG→ MUX |

## 2.6 Expander Interface

The MIOC component has two Expander interfaces, one for each of the two PXBs supported by Intel® 450NX PCIset. These two high speed, low latency interfaces are identified as the **X0** bus and the **X1** bus groups.

Each signal name includes a “**p**”, indicating the Expander port. On the MIOC, **p = 0** or **1**, designating one of the two interfaces. On the PXB, **p** is not used.

|            |                                                                                                                |                 |
|------------|----------------------------------------------------------------------------------------------------------------|-----------------|
| XpADS#     | <b>Address / Data Strobe.</b><br>Bidirectional signal asserted by the sending agent during data transmission.  | AGTL+ MIOC↔ PXB |
| XpBE[1:0]# | <b>Byte Enables.</b><br>Bidirectional signals indicating valid bytes during the data phases of a transmission. | AGTL+ MIOC↔ PXB |

|                                    |                                                                                                                                 |                 |
|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>XpD[15:0]#</b>                  | <b>Datapath</b><br>This bidirectional datapath is used to transfer addresses and data between the MIOC and the PCI Expander.    | AGTL+ MIOC↔ PXB |
| <b>XpHRTS#</b>                     | <b>Host Request to Send.</b><br>Request to use the bidirectional Expander bus sent from MIOC to PXB, synchronous to HCLKIN.     | AGTL+ MIOC→ PXB |
| <b>XpHSTBP#</b><br><b>XpHSTBN#</b> | <b>Host Strobes</b><br>This pair of opposite-phase strobes are used by the PXB to latch and synchronize incoming data.          | AGTL+ MIOC→ PXB |
| <b>XpPAR#</b>                      | <b>Bus Parity.</b><br>Bidirectional signal indicating even parity across XD[15:0] and XBE[1:0].                                 | AGTL+ MIOC↔ PXB |
| <b>XpXRTS#</b>                     | <b>Expander Request to Send.</b><br>Request to use the bidirectional Expander bus sent from PXB to MIOC, synchronous to HCLKIN. | AGTL+ PXB→ MIOC |
| <b>XpXSTBP#</b><br><b>XpXSTBN#</b> | <b>Expander Strobes</b><br>This pair of opposite-phase strobes are used by the MIOC to latch and synchronize incoming data.     | AGTL+ PXB→ MIOC |

**Support Signals**

|                |                                                                                                                                                                                                                                                                                 |                 |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>XpBLK</b>   | <b>Block Counters.</b><br>This signal is asserted when the Performance Counter Master Enable bit in the MIOC's CONFIG register is set, and is used to affect a nearly simultaneous stop/start of the performance counters across both the MIOC and all PXBs.                    | AGTL+ MIOC→ PXB |
| <b>XpCLK</b>   | <b>Host Clock.</b><br>This is the primary clock source provided to the PXB, analogous to HCLKIN for the MIOC, RCG and MUX. Inside the PXB, it is divided by 3 to produce a PCI clock output at 33.33 MHz from an HCLKIN of 100 MHz.                                             | CMOS MIOC→ PXB  |
| <b>XpCLKB</b>  | <b>Host Clock, 2nd Version.</b><br>This is a duplicate of the XpCLK signal, to be used in maintaining PLL synchronization in the MIOC. See XpCLKFB below.                                                                                                                       | CMOS MIOC→ ext  |
| <b>XpCLKFB</b> | <b>Host Clock, Feedback.</b><br>This signal is a length-matched copy of the XpCLK signal sent to the PXB, used to maintain PLL synchronization in the MIOC. The XpCLKB signal is length-matched to the XpCLK's path to the PXB, then returned to the MIOC as the XpCLKFB input. | CMOS ext→ MIOC  |
| <b>XpIB</b>    | <b>Driving Inbound.</b><br>This active-high signal is asserted when the PXB is driving data over the Expander bus. This pin is not connected to the MIOC.                                                                                                                       | AGTL+ PXB→ ext  |
| <b>XpRST#</b>  | <b>PXB Reset.</b><br>This signal issues a hard reset of the PXB, including the dependent PCI buses.                                                                                                                                                                             | AGTL+ MIOC→ PXB |

|                 |                                                                                                                                                            |                 |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>XpRSTB#</b>  | <b>PXB Reset, 2nd Version.</b><br>This is a duplicate of the XpRST# signal, to be used in maintaining PLL synchronization in the MIOC. See XpRSTFB# below. | AGTL+ MIOC→ ext |
| <b>XpRSTFB#</b> | <b>PXB Reset, Feedback.</b><br>The XpRSTB# signal is length-matched to the XpRST#'s path to the PXB, then returned to the MIOC as the XpRSTFB# input.      | AGTL+ ext→ MIOC |

## 2.7 Common Support Signals

### 2.7.1 JTAG Interface

All four components in the Intel® 450NX PCIset have a JTAG Test Access Port (TAP) to allow access to internal registers and perform boundary scan. Each interface is identical.

|              |                                                                                                                              |         |
|--------------|------------------------------------------------------------------------------------------------------------------------------|---------|
| <b>TCK</b>   | <b>Test Clock</b><br>Test Clock is used to clock state information and data into and out of the device during boundary scan. | 2.5V I  |
| <b>TDI</b>   | <b>Test Data Input</b><br>Test Input is used to serially shift data and instructions into the TAP.                           | 2.5V I  |
| <b>TDO</b>   | <b>Test Output</b><br>Test Output is used to shift data out of the device.                                                   | 2.5V OD |
| <b>TMS</b>   | <b>Test Mode Select</b><br>Test Mode Select is used to control the state of the TAP controller.                              | 2.5V I  |
| <b>TRST#</b> | <b>Test Reset</b><br>Test Reset is used to reset the TAP controller logic.                                                   | 2.5V I  |

### 2.7.2 Reference Signals

All four components have the following support signals to provide voltage references or compensation for the AGTL+ interfaces or the PLL circuitry.

|                  |                                                                                                                                                                                                                   |          |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <b>CRES[1:0]</b> | <b>I/O Buffer Compensation Resistor Terminals</b><br>For correct component operation an external 768 ohm resistor must be connected between CRES1 and CRES0. This resistor should have a minimum precision of 1%. | Analog I |
| <b>VCCA (n)</b>  | <b>PLL Analog Voltage</b><br>This pin is an independent power supply for a PLL. In normal operation, this pin provides power to the PLL, and requires special decoupling (refer to Electrical Characteristics).   | Analog I |

**VREF (n)**      **AGTL+ Reference Voltage**      Analog I  
 This is the reference voltage derived from the termination voltage to the pull-up resistors. The MIOC has 6 VREF pins, while the PXB, RCG and MUX each have 2 VREF pins.

## 2.8 Component-Specific Support Signals

### 2.8.1 MIOC

**CRESET#**      **Clock Selection Reset.**      LVTTL O  
 This is a delayed version of the RESET# signal provided to the processors. This signal is asserted asynchronously along with RESET#, but is deasserted two system bus clocks following the deassertion of RESET#.

**ERR[1:0]#**      **Error Code**      LVTTL I/OD  
 These pins reflect irrecoverable errors detectable by the Intel 450NX PCIset.

| ERR | Error Type             | Associated Error s Flags                                                           |
|-----|------------------------|------------------------------------------------------------------------------------|
| 00  | No error               |                                                                                    |
| 01  | PCIset Internal Error  | Expander Bus Parity                                                                |
| 10  | Multi-Bit Memory Error | Multi-Bit Memory ECC error                                                         |
| 11  | System Bus Error       | Address Parity, Request Parity, Protocol Violation, BERR, Multi-Bit Host ECC error |

**HCLKIN**      **Host Clock In**      2.5V I  
 This pin receives a buffered system clock. This is a single trace from the clock synthesizer to minimize clock skew.

**INTREQ#**      **Interrupt Request**      LVTTL O  
 This pin is asserted by the MIOC when an internal event occurs and sets a status flag, and that flag has been configured to request an interrupt.

**PWRGD**      **Power Good**      LVTTL I  
 This pin should be connected to a 3.3 V version of the system's power good indicator, and should be asserted only after all power supplies and clocks have reached their stable references and been stable for at least 1 msec.

**PWRGDB**      **Buffered Power Good**      LVTTL O  
 A buffered (but not synchronized) version of the PWRGD input, which is used to drive the PWRGD input on each PXB in the system.

**RESET#**      **Reset**      AGTL+ I/O  
 In normal operation, this signal is an output. The MIOC will reset the system bus either on power-up or when programmed through the Reset Control register.

**SMIACT#**      **SMI Active.**      LVTTL O  
This signal provides a visible indicator that the system has entered System Management Mode.

## 2.8.2      **PXB**

**INTRQ(A,B)#**      **Interrupt Requests**      PCI OD  
These pins are asserted by the PXB when an internal event occurs and sets a status flag, and that flag has been configured to request an interrupt. There is one pin for each side (A,B) of the PXB. The signals may be connected to the standard PCI bus interrupt request lines.

**PAMON[1:0]#**  
**PBMON[1:0]#**      **Performance Monitors**      LVTTL I/OD  
These pins track the two performance monitoring counters associated with each PCI bus (a,b) in the PXB. PMON[0] tracks the PMD[0] counter while PMON[1] tracks the PMD[1] counter.

**PIIXOK#**      **PIIX Reset Complete.**      LVTTL I  
This signal is tied to the PIIX's CPURST output, and is used to detect when the PIIX completes its reset functions.

**PWRGD**      **Power Good**      LVTTL I  
This input should be driven from the MIOC's PWRGDB output.

## 2.8.3      **RCG**

**BANKID#**      **Bank Identifier**      LVTTL I  
This strapping pin should be tied high (deasserted), or have an external pullup.

**DR50H#**      **50ns DRAM "Here".**      LVTTL I  
This strapping pin selects between 60ns and 50ns DRAM timings for this RCG.  
Deasserted:    60ns timings will be used.  
Asserted:      50ns timings will be used.

**DR50T#**      **50ns DRAM "There".**      LVTTL I  
This strapping pin should match the DR50H# strapping pin described above.

**HCLKIN**      **Host Clock In**      2.5V I  
This pin receives a buffered system clock.

## 2.8.4      **MUX**

**HCLKIN**      **Host Clock In**      2.5V I  
This pin receives a buffered system clock.



The Intel® 450NX PCIset internal registers (both I/O Mapped and Configuration registers) are accessible by the processor. Each MIOC, and each PCI bus in each PXB has an independent configuration space. This chapter provides detailed descriptions of each register.

## 3.1 Access Restrictions

### Register Attributes

|            |                                                                                                                                                                                |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Read Only  | Writes to this register have no effect.                                                                                                                                        |
| Read/Write | Data may be read from and written to this register. Selected bits in the register may be designated as "read-only"; such bits are not affected by data writes to the register. |
| Read/Clear | Data may be read from the register. A data write operates strictly as a clear:                                                                                                 |
| Sticky     | Data in this register remains valid and unchanged, during and following any reset except the <i>power-good</i> reset.                                                          |

## 3.2 I/O Mapped Registers

The Intel® 450NX PCIset contains two registers that reside in the processor I/O address space: the Configuration Address (CONFIG\_ADDRESS) Register and the Configuration Data (CONFIG\_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

### 3.2.1 CONFIG\_ADDRESS: Configuration Address Register

|                |              |            |            |
|----------------|--------------|------------|------------|
| I/O Address:   | CF8h [Dword] | Size:      | 32 bits    |
| Default Value: | 00000000h    | Attribute: | Read/Write |

The CONFIG\_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.



## 3.3 MIOC Configuration Space

Table 3-1: MIOC Configuration Space <sup>1</sup>

|        |      |         |        |     |        |                 |         |        |        |
|--------|------|---------|--------|-----|--------|-----------------|---------|--------|--------|
| DID    |      | VID     |        | 00h | DBC 01 |                 | DBC 00  |        | 80h    |
|        |      |         |        | 04h | DBC 03 |                 | DBC 02  |        | 84h    |
| CLASS  |      |         | RID    | 08h | DBC 05 |                 | DBC 04  |        | 88h    |
| HDR    |      |         |        | 0Ch | DBC 07 |                 | DBC 06  |        | 8Ch    |
|        |      |         |        | 10h | DBC 09 |                 | DBC 08  |        | 90h    |
|        |      |         |        | 14h | DBC 11 |                 | DBC 10  |        | 94h    |
|        |      |         |        | 18h | DBC 13 |                 | DBC 12  |        | 98h    |
|        |      |         |        | 1Ch | DBC 15 |                 | DBC 14  |        | 9Ch    |
|        |      |         |        | 24h | RCGP   | <i>Reserved</i> |         |        | A0h    |
|        |      |         |        | 28h |        |                 | REFRESH |        | A4h    |
|        |      |         |        | 2Ch |        |                 | MEA1    | MEA0   | A8h    |
|        |      |         |        | 30h |        |                 |         |        | ACh    |
|        |      |         |        | 34h | MEL1   |                 | MEL0    |        | B0h    |
|        |      |         |        | 38h | HEL1   |                 | HEL0    |        | B4h    |
|        |      |         |        | 3Ch |        |                 | ECCMSK  | ECCCMD | B8h    |
| CHKCON |      | RC      | CONFIG | 40h | ROUTE0 |                 | TCAP0   |        | C0h    |
|        |      | ERRCMD  | ERRSTS | 44h |        |                 | TCAP1   |        | C4h    |
|        |      | BUFSIZ  |        | 48h | ROUTE1 |                 | TCAP2   |        | C8h    |
| CVCR   |      | CVDR    |        | 4Ch |        |                 | TCAP3   |        | CCh    |
|        |      | TOM     |        | 50h | BUSNO1 |                 | SUBB0   | SUBA0  | BUSNO0 |
| LXGT   |      | LXGB    |        | 54h | DEVMAP |                 | SUBB1   | SUBA1  | D4h    |
|        |      | HXGB    |        | 58h | PMD0   |                 |         |        | D8h    |
|        |      | HXGT    |        | 5Ch |        |                 | PMR0    | PMD0   | DCh    |
| MAR2   | MAR1 | MAR0    | GAPEN  | 60h | PMD1   |                 |         |        | E0h    |
| MAR6   | MAR5 | MAR4    | MAR3   | 64h |        |                 | PMR1    | PMD1   | E4h    |
| IOAR   |      | IOABASE |        | 68h | PME1   |                 | PME0    |        | E8h    |
| SMRAM  |      |         |        | 6Ch |        |                 |         |        | ECh    |
|        |      | MMBASE  |        | 70h |        |                 |         |        | F0h    |
| MMR1   |      | MMR0    |        | 74h |        |                 |         |        | F4h    |
| MMR3   |      | MMR2    |        | 78h |        |                 |         |        | F8h    |
| IOR    |      | ISA     |        | 7Ch |        |                 |         |        | FCh    |

1. The first 64 bytes are predefined in the PCI Specification. All other locations are defined specifically for the component of interest.

Table 3-1 illustrates the MIOC's Configuration Space Map. Many of these registers affect both host-initiated transactions and PCI-initiated transactions, and are therefore duplicated in both the MIOC and PXB Configuration Spaces. It is software's responsibility to ensure that both sets of registers are programmed consistently to achieve correct operation.

### 3.3.1 BUFSIZ: Buffer Sizes

|                 |         |            |           |
|-----------------|---------|------------|-----------|
| Address Offset: | 48-4Ah  | Size:      | 24 bits   |
| Default Value:  | 304310h | Attribute: | Read Only |

| <b><u>Bits</u></b> | <b><u>Description</u></b> |
|--------------------|---------------------------|
|--------------------|---------------------------|

- |       |                                                                                                                                                                                                              |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:18 | <p><b>Inbound Write Transaction Capacity.</b><br/>Total number of inbound write transactions, per Expander Port, that can be accepted by the MIOC.<br/>Value=12.</p>                                         |
| 17:12 | <p><b>Inbound Read Transaction Capacity.</b><br/>Total number of inbound read transactions, per Expander Port, that can be accepted by the MIOC.<br/>Value=4.</p>                                            |
| 11:6  | <p><b>Inbound Write Data Buffer Capacity.</b><br/>Total number of data buffers, per Expander Port, available in the MIOC for use by inbound write transactions, in increments of 32 bytes.<br/>Value=12.</p> |
| 5:0   | <p><b>Inbound Read Data Buffer Capacity.</b><br/>Total number of data buffers, per Expander Port, available in the MIOC for use by inbound read transactions, in increments of 32 bytes.<br/>Value=16.</p>   |



### 3. Register Descriptions

- 5     **Live Port #1 Flag.**  
If set, the port is "live".  
Default=0.
  
- 4     **Live Port #0 Flag.**  
If set, the port is "live."  
Default=1.
  
- 3:2    *reserved*
  
- 1     **Test Port #1 Enable.**  
Setting this enable triggers the check connection protocol for port 1.  
Default=0.
  
- 0     **Test Port #0 Enable.**  
Setting this enable triggers the check connection protocol for port 0.  
Default=0.

**NOTE**

*Setting both Test Port #1 Enable and Test Port #0 Enable simultaneously is prohibited, and will have unpredictable results, up to and including system hangs requiring a full system reset. Inactive PXBs should be disabled by writing the corresponding Reset Expander Port bit in the RC register. Transactions sent to inactive PXBs can result in system hangs.*

### 3.3.4 CLASS: Class Code Register

Address Offset: 09 - 0Bh                      Size:        24 bits  
Default Value:  060000h                     Attribute:  Read Only

**Bits**    **Description**

- 23:16   **Base Class**  
For the MIOC, this field is hardwired to 06h.
  
- 15:8     **Sub-Class**  
For the MIOC, this field is hardwired to 00h.
  
- 7:0      **Register-Level Programming Interface**  
For the MIOC this field is hardwired to 00h.

### 3.3.5 CONFIG: Software-Defined Configuration Register

Address Offset: 40-41h                      Size:        16 bits  
Default Value:  1000h                     Attribute:  Read/Write

**Bits**    **Description**

- 15:13    *reserved (0)*

- 12     **Outbound Fairness Disable.**  
 When this bit is clear, Host-PCI writes and reads that receive a retry by the MIOC follow a fairness algorithm to guarantee that retried transactions receive first priority before new transactions. If set, Host-PCI writes and reads are serviced in the order first observed without regard to retry history. Default=1.
- 11     **Performance Counter Master Enable (PCME).**  
 This bit provides a mechanism to (nearly) simultaneously freeze or start the performance counters across both the MIOC and PXBs.  
 If this bit is cleared the MIOC's and PXB's performance counters will not increment  
 If set the MIOC's and PXB's performance counters resume normal operation.  
 Default = 0.
- 10     *reserved (0)*
- 9      **Third Party Support Disable**  
 If set, performance optimizations are enabled that may result in coherency violations in the presence of a third party agent. This bit should be clear for systems with TPAs.  
 Default = 0.
- 8      **External Arbiter Enable.**  
 If set, access to the system bus is controlled by an external arbiter. If cleared, the MIOC's internal arbiter is used. Default=0.
- 7      **WC Write Post During I/O Bridge Access Enable (UWPE).**  
 This bit should be cleared for normal operation. Default=0.
- 6      **Outbound I/O Write Posting Enable.**  
 If set, Host-PCI I/O writes will be posted. If cleared, Host-PCI I/O writes will not be posted. In normal operation, this enable should be set. Default=0.
- 5      **Read-Around-Write Enable (RAWE).**  
 If RAW is set, it enables the read-around-write capability for the MIOC and memory subsystem. If cleared, read accesses will not advance past any previously posted writes. In normal operation, this enable should be set. Default=0.
- 4      **ISA Expansion Aliasing Enable.**  
 If set, every I/O access with an address in the range x100-x3FFh, x500-x7FFh, x900-xBFF and xD00-xFFFh is internally aliased to the range 0100-03FFh before any other address range checking is performed. This bit only affects routing, the unmasked address is passed to the PCI bus. Default=0.
- 3      *reserved (0)*
- 2      **Card to Card Interleave Enable.**  
 If set, Host or PCI accesses to memory are distributed to both memory cards on a cache line granularity. This provides a performance enhancement for systems which utilize two memory cards. When this bit is clear, C2C interleaving is disabled. Default = 0.

- 1:0 **Memory Address Bit Permuting.**  
 The MIOC supports cache-line permuting across banks. This field controls the type of permuting used, as follows:
- 00b No permuting.
  - 01b 2-way Permuting.
  - 10b 4-way Permuting.
  - 11b *reserved*
- Default=0.

### 3.3.6 CVCR: Configuration Values Captured on Reset

Address Offset: 4E-4Fh                      Size:        16 bits  
 Default Value:  0000h                      Attribute:  Read-Only

This register captures the configuration values driven on A#[15:0] at the trailing edge of RESET#. This allows an external device to override the default values provided by the MIOC via its CVDR register.

#### **Bits**    **Description**

- 15:13 *reserved (0)*
- 12:11 **APIC Cluster ID.**  
 Captured from A#[12:11]. Represents the APIC Cluster identifier.
- 10 **Enable BINIT# Input.**  
 Captured from A#[10]. If set, the MIOC will observe the assertion of the BINIT# input. Further details on BINIT# processing may be found in the ERRCMD register.
- 9 **Enable BERR# Input.**  
 Captured from A#[9]. If set, the MIOC will observe the assertion of the BERR# input. Further details on BERR# processing may be found in the ERRCMD register.
- 8 **Enable AERR# Input.**  
 Captured from A#[8]. If set, the MIOC will observe the assertion of the AERR# input. Further details on AERR# processing may be found in the ERRCMD register. If this enable is asserted, then the BINIT# Driver Enable in the ERRCMD register must also be asserted.
- 7 **In-Order Queue Depth 1.**  
 Captured from A#[7]. If set, the MIOC will limit its In-Order Queue Depth to 1 (no pipelining support), instead of the usual 8.
- 6 **1M Power-on Reset Vector.**  
 Captured from A#[6]. This bit has no meaning for the MIOC. If set, all Pentium® II Xeon™ processors on the system bus will use the 1MB-1 (000FFFFFFh) reset vector, instead of their usual 4 GB-1 (FFFFFFFFFh) vector.
- 5 **Enable FRC Mode.**  
 Captured from A#[5]. This bit has no meaning for the MIOC. If set, all Pentium II Xeon processors on the system bus will enter FRC-enabled mode.
- 4:0 *reserved (0)*



Unused DBC registers should be configured as inactive, with the Bank Present bit cleared and the TOB field set to that of the previous bank, indicating that the amount of memory in that bank is zero.

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15                 | <b>4:1 Interleave.</b><br>If set, bank is a 4:1 interleave. If cleared, bank is a 2:1 interleave.<br>Default=1.                                                                                                                                                                                                                                                                                                                                                             |
| 14                 | <b>Single Row.</b><br>This bit is set if the bank contains only a single row. If cleared, the bank contains two rows; <i>both rows must be configured identically</i> . Default=0.                                                                                                                                                                                                                                                                                          |
| 13                 | <b>Bank Present.</b><br>This bit is set to indicate that this memory bank is present, and refresh cycles should be issued to the bank. This bit must be cleared if this bank is not physically present.<br>Default=1.                                                                                                                                                                                                                                                       |
| 12:10              | <i>reserved (0)</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:0                | <b>Top of Bank (TOB).</b><br>This field contains the effective address of the top of memory in this bank <i>and all lower banks</i> , and is used to determine which bank is selected. Each TOB field specifies the amount of memory, in 32 MB chunks, contained in this bank <i>and all lower banks</i> . Unpopulated banks must have their TOB set equal to that of the previous bank indicating that the amount of memory in that bank is zero.<br>Default = 200h, each. |

### 3.3.9 DEVMAP: System Bus PCI Device Map

|                 |        |            |                       |
|-----------------|--------|------------|-----------------------|
| Address Offset: | D6-D7h | Size:      | 16 bits               |
| Default Value:  | 0005h  | Attribute: | Read/Write, Read Only |

This register indicates which PCI devices on the system bus have active configuration spaces. At reset, DEVMAP is initialized with all devices *not present* except the MIOC and the compatibility PCI bus.

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                                                                                                                                                                                                        |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15                 | <i>reserved (0)</i>                                                                                                                                                                                                                                                                                              |
| 14:0               | <b>PCI Bus #0, Device [30:16] Present.</b><br>Each bit corresponds to a device on PCI Bus #0 (numbers 16-30). If set, the device is present in the system and is expected to respond to configuration cycles directed to it. Bit 0 is hardwired "on", and is read-only.<br>Default=0005h (MIOC, PCI #0A present) |









- 4     **Low Expansion Gap Enable.**  
When set, the Low Expansion Gap (LXG) is enabled. Default=0.
- 3     **High BIOS Space Enable.**  
If set, a 2 MByte space is opened at location (4 GB - 2 MB), and accesses into this address range will be directed to the compatibility PCI bus instead of memory. Default=1.
- 2     **High Graphics Adapter Space Enable.**  
If set, a 64 KB space is opened in the upper half of the Graphics Adapter portion of the Low Compatibility Region (address range B\_0000h-BFFFFh), and accesses into this address range will be directed to the compatibility PCI bus instead of memory. Default=1.
- 1     **Low Graphics Adapter Space Enable.**  
If set, a 64 KB space is opened in the lower half of the Graphics Adapter portion of the Low Compatibility Region (address range A\_0000h-AFFFFh), and accesses into this address will be directed to the compatibility PCI bus instead of memory. Default=1.
- 0     *reserved (0)*

### 3.3.16 HDR: Header Type Register

|                 |     |            |           |
|-----------------|-----|------------|-----------|
| Address Offset: | 0Eh | Size:      | 8 bits    |
| Default Value:  | 00h | Attribute: | Read Only |

This register identifies the header layout of the configuration space. Writes to this register have no effect.

| <b>Bits</b> | <b>Description</b> |
|-------------|--------------------|
|-------------|--------------------|

- |     |                                                                                                                        |
|-----|------------------------------------------------------------------------------------------------------------------------|
| 7   | <b>Multi-function Device.</b><br>The MIOC is not a multi-function device, and this bit is hardwired to 0.              |
| 6:0 | <b>Configuration Layout.</b><br>This field is hardwired to 00h, which represents the default PCI configuration layout. |

### 3.3.17 HEL[1:0] Host Bus Error Log

|                 |            |            |                    |
|-----------------|------------|------------|--------------------|
| Address Offset: | B4-B7h     | Size:      | 16 bits each       |
| Default Value:  | 0000h each | Attribute: | Read/Write, Sticky |

These registers are loaded on the first and second ECC errors detected on data received from the system bus. HEL[0] logs the first error, and HEL[1] logs the second. The registers hold their data until reloaded due to a new error condition, or until they are explicitly cleared by software or a *power-good* reset.

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                 |
|--------------------|---------------------------------------------------------------------------------------------------------------------------|
| 15:8               | <b>Syndrome.</b><br>Holds the calculated syndrome that identifies the specific bit in error.                              |
| 7:2                | <i>reserved (0)</i>                                                                                                       |
| 1                  | <b>Multiple-Bit Error Logged (MBE).</b><br>This flag is set if the logged error was a multiple-bit (uncorrectable) error. |
| 0                  | <b>Single-Bit Error Logged (SBE).</b><br>This flag is set if the logged error was a single-bit (correctable) error.       |

### 3.3.18 HXGB: High Expansion Gap Base

|                 |         |            |            |
|-----------------|---------|------------|------------|
| Address Offset: | 58-5Ah  | Size:      | 24 bits    |
| Default Value:  | 000000h | Attribute: | Read/Write |

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                                                                     |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0               | <b>Gap Base Address.</b><br>This field specifies the A[43:20] portion of the gap's base address, in 1 MB increments. The A[19:0] portions of the gap's base address are zero. |

### 3.3.19 HXGT: High Expansion Gap Top

|                 |         |            |            |
|-----------------|---------|------------|------------|
| Address Offset: | 5C-5Eh  | Size:      | 24 bits    |
| Default Value:  | 000000h | Attribute: | Read/Write |

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                                                                     |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0               | <b>Gap Top Address.</b><br>This field specifies the A[43:20] portion of the gap's highest address, in 1 MB increments. The A[19:0] portion of the gap's top address is FFFFh. |

### 3.3.20 IOABASE: I/O APIC Base Address

|                 |        |            |            |
|-----------------|--------|------------|------------|
| Address Offset: | 68-69h | Size:      | 16 bits    |
| Default Value:  | 0FECh  | Attribute: | Read/Write |

| <b><u>Bits</u></b> | <b><u>Description</u></b>                                                                                                                                                                       |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12              | <i>reserved (0)</i>                                                                                                                                                                             |
| 11:0               | <b>I/O APIC Base Address.</b><br>This field specifies the A[31:20] portion of the I/O APIC Space's base address, in 1 MB increments. The A[43:32] and A[19:0] portions of the address are zero. |













|                                           |                                         |         |                                         |
|-------------------------------------------|-----------------------------------------|---------|-----------------------------------------|
| 00 0110                                   | <i>reserved</i>                         | 00 1110 | Memory Read                             |
| 00 0111                                   | <i>reserved</i>                         | 00 1111 | Memory Write                            |
| <b>Generic (Grouped) Bus Transactions</b> |                                         |         |                                         |
| 010 000                                   | Any bus transaction                     | 010 100 | Any I/O transaction                     |
| 010 001                                   | Any memory transaction                  | 010 101 | Any I/O or memory transactions          |
| 010 010                                   | Any memory read                         | 010 110 | Any I/O or memory read                  |
| 010 011                                   | Any memory write                        | 010 111 | Any I/O or memory write                 |
| <b>Bus Signal Assertions</b>              |                                         |         |                                         |
| 011 000                                   | HIT <sup>1,2</sup>                      | 011 100 | BNR <sup>1,2</sup>                      |
| 011 001                                   | HITM <sup>1,2</sup>                     | 011 101 | BPRI <sup>2</sup>                       |
| 011 010                                   | RETRY <sup>1,2</sup>                    | 011 110 | LOCK <sup>2</sup>                       |
| 011 011                                   | DEFER <sup>1,2</sup>                    | 011 111 | <i>reserved</i>                         |
| <b>Memory Hits/Misses</b>                 |                                         |         |                                         |
| 100 000                                   | Bank was idle <sup>1,2</sup>            | 100 010 | Waited for address lines <sup>1,2</sup> |
| 100 001                                   | Waited for Row precharge <sup>1,2</sup> | 100 011 | Hit open page <sup>1,2</sup>            |

All other encodings are reserved.

Notes:

1. Counting data cycles is undefined for this selection.
2. The Agent, Destination and Length fields cannot be applied to this selection, and should be programmed to "any".

### 3.3.33 PMR[1:0]: Performance Monitoring Response

Address Offset: DDh, E5h                      Size: 8 bits each  
 Default Value: 00h each                      Attribute: Read/Write

The PMR register specifies how the event selected by the corresponding PME register affects the associated PMD register, the BP[1:0] pins, and the INTREQ# pin. Events defined by PME[0] can be driven out BP0 and events defined by PME[1] can be driven out BP1.

#### **Bits**      **Description**

- 7:6      **Interrupt Assertion**  
 Defines how selected event affects INTREQ# assertion. Whenever INTREQ# is asserted, a flag for this counter is set in the Error Status (ERRSTS) register, so that software can determine the cause of the interrupt. This flag is reset by writing the ERRSTS register.
- 0      Selected event does not assert INTREQ#
  - 1      *reserved*
  - 2      Assert INTREQ# pin when event occurs
  - 3      Assert INTREQ# pin when counter overflows
- 5:4      **Performance Monitoring pin assertion**  
 Defines how the selected event affects the Performance Monitoring pin for this counter.
- 0      Selected event does not assert this counters PM pin
  - 1      *reserved*
  - 2      Assert this counter's PM pin when event occurs
  - 3      Assert this counter's PM pin when counter overflows







**24 SMM Space Locked (D\_LCK).**

When software writes a 1 to this bit, the hardware will clear the D\_OPEN bit, and both D\_LCK and D\_OPEN then become read only. No application software, except the SMI handler, should violate or change the contents of SMM memory. Default=0.

**23:20 SMM Space Size.**

This field specifies the size of the SMM RAM space, in 64 KB increments.

|    |        |    |        |    |        |    |        |
|----|--------|----|--------|----|--------|----|--------|
| 0h | 64 KB  | 4h | 320 KB | 8h | 576 KB | Ch | 832 KB |
| 1h | 128 KB | 5h | 384 KB | 9h | 640 KB | Dh | 896 KB |
| 2h | 192 KB | 6h | 448 KB | Ah | 704 KB | Eh | 960 KB |
| 3h | 256 KB | 7h | 512 KB | Bh | 768 KB | Fh | 1 MB   |

Default: 0h (64 KB).

19:16 *reserved (0)*

**15:0 SMM Space Base Address.**

This field specifies the A[31:16] portion of the SMM RAM space base address (A[15:0]=0000h). The space may be relocated anywhere below the 4 GB boundary and the Top of Memory (TOM); however, the base address must be aligned on the next highest power-of-2 natural boundary given the chosen size. Incorrect alignment results in indeterminate operation. Default: 000Ah.

**Table 3-3: SMRAM Space Cycles**

| SMRAM | D_OPEN | D_CODE | D_LCK | SMMEM | Code Fetch          | Data Reference      | Usage                                                                                                                                                                         |
|-------|--------|--------|-------|-------|---------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | X      | X      | X     | X     | Normal <sup>1</sup> | Normal <sup>1</sup> | SMM RAM space is not supported.                                                                                                                                               |
| 1     | 0      | 0      | X     | 0     | PCI 0a              | PCI 0A              | Normal SMM usage. Accesses to the SMM RAM space from processors in SMM will access the DRAM. Accesses by processors not in SMM will be diverted to the compatibility PCI bus. |
| 1     | 0      | 0      | X     | 1     | DRAM                | DRAM                |                                                                                                                                                                               |
| 1     | 0      | 1      | X     | 0     | PCI 0A              | PCI 0A              | A modification of the normal SMM usage, in which only code fetches are accepted from processors in SMM mode.                                                                  |
| 1     | 0      | 1      | X     | 1     | DRAM                | PCI 0A              |                                                                                                                                                                               |
| X     | 1      | 1      | X     | X     | Illegal Combination |                     |                                                                                                                                                                               |
| 1     | 1      | 0      | 0     | X     | DRAM                | DRAM                | Full access by any agent to SMM RAM space.                                                                                                                                    |

1. SMRAM functions are disabled.

### 3.3.40 SUBA[1:0]: Bus A Subordinate Bus Number, per PXB

Address Offset: D1h, D4h

Default Value: 00h each

Size: 8 bits each

Attribute: Read/Write

See the description of BUSNO.



5:0 **Outbound Read Data Buffer Capacity.**  
 This field specifies the total number of data buffers, per PXB/PCI port, available in the PXB for use by outbound read transactions, in increments of 32 bytes.  
 MIOC maximum: 16                      Minimum allowed: 2                      Default= 2

### 3.3.43 TOM: Top of Memory

Address Offset: 50-52h                      Size: 24 bits  
 Default Value: 000FFFh                      Attribute: Read/Write

#### **Bits**    **Description**

23:0 **Memory Address Ceiling.**  
 Represents bits A[43:20] of the highest physical address to be directed toward this node's DRAM. The lower A[19:0] bits of this address are FFFFh.  
 Default=000FFFh (4 GB-1).

### 3.3.44 VID: Vendor Identification Register

Address Offset: 00 - 01h                      Size: 16 bits  
 Default Value: 8086h                      Attributes: Read Only

#### **Bits**    **Description**

15:0 **Vendor Identification Number.**  
 This is a 16-bit value assigned to Intel. Intel VID = 8086h.

## 3.4 PXB Configuration Space

Each PXB supports two independent PCI buses (Bus "A" and Bus "B"), which can be configured independently. Each PCI bus therefore has its own configuration space. Both configuration spaces are identical. When operating the PXB in 64-bit Bus Mode, only the A-side configuration space is used. The B-side configuration space is not accessible while in 64-bit mode.

Table 3-4 illustrates the PXB/PCI Bus Configuration Space Map.

**Table 3-4: PXB Configuration Space <sup>1</sup>**

|         |        |        |        |     |      |        |      |       |       |      |      |
|---------|--------|--------|--------|-----|------|--------|------|-------|-------|------|------|
| DID     |        | VID    |        | 00h |      |        |      |       | 80h   |      |      |
| PCISTS  |        | PCICMD |        | 04h |      |        |      |       | 84h   |      |      |
| CLASS   |        |        | RID    | 08h |      |        |      |       | 88h   |      |      |
| HDR     | MLT    | CLS    |        | 0Ch |      |        |      |       | 8Ch   |      |      |
|         |        |        |        | 10h |      |        |      |       | 90h   |      |      |
|         |        |        |        | 14h |      |        |      |       |       | 94h  |      |
|         |        |        |        | 18h |      |        |      |       |       |      | 98h  |
|         |        |        |        | 1Ch |      |        |      |       |       |      | 9Ch  |
|         |        |        |        | 24h |      |        |      |       |       |      | A0h  |
|         |        |        |        | 28h |      |        |      |       |       |      | A4h  |
|         |        |        |        | 2Ch |      |        |      |       |       |      | A8h  |
|         |        |        |        | 30h |      |        |      |       |       |      | ACCh |
|         |        |        |        | 34h |      |        |      |       |       |      | B0h  |
|         |        |        |        | 38h |      |        |      |       |       |      | B4h  |
|         |        |        |        | 3Ch |      |        |      |       |       |      | B8h  |
|         |        |        |        | MTT |      | CONFIG |      | 40h   | ROUTE | TCAP |      |
| RC      | ERRCMD |        | ERRSTS | 44h |      |        |      | TMODE | C4h   |      |      |
| BUFSIZ  |        |        |        | 48h |      |        |      |       | C8h   |      |      |
|         |        |        |        | 4Ch |      |        |      |       | CCh   |      |      |
| TOM     |        |        |        | 50h |      |        |      |       | D0h   |      |      |
| LXGT    |        | LXGB   |        | 54h |      |        |      |       | D4h   |      |      |
| HXGB    |        |        |        | 58h | PMD0 |        |      |       | D8h   |      |      |
| HXGT    |        |        |        | 5Ch |      |        | PMR0 | PMD0  | DCh   |      |      |
| MAR2    | MAR1   | MAR0   | GAPEN  | 60h | PMD1 |        |      |       | E0h   |      |      |
| MAR6    | MAR5   | MAR4   | MAR3   | 64h |      |        | PMR1 | PMD1  | E4h   |      |      |
| IOABASE |        |        |        | 68h | PME1 |        | PME0 |       | E8h   |      |      |
| SMRAM   |        |        |        | 6Ch |      |        |      |       | ECh   |      |      |
| MMBASE  |        |        |        | 70h |      |        |      |       | F0h   |      |      |
|         |        |        |        | 74h |      |        |      |       | F4h   |      |      |
| MMT     |        |        |        | 78h |      |        |      |       | F8h   |      |      |
|         |        |        |        | 7Ch |      |        |      |       | FCh   |      |      |
| ISA     |        |        |        |     |      |        |      |       |       |      |      |

1. The first 64 bytes are predefined in the PCI Specification. All other locations are defined specifically for the component of interest.





- 8     **Outbound Write Around Retried/Partial Read Enable.**  
 If set, the PXB allows outbound writes to pass retried or partially completed (i.e., disconnected) outbound reads. This enable *must* be set for Pentium® II Xeon™ processor/Intel® 450NX PCIset systems. Default=1.
- 7     **Burst Write Combining Enable (BWCE).**  
 If set, back-to-back sequentially addressed outbound writes may be combined in the outbound write buffers before placement on the PCI bus. When the BWCE is cleared, all outbound write combining is disabled, and each host transaction results in a corresponding transaction on the PCI bus. Default=0.
- 6     **Re-streaming Buffer Enable.**  
 If set, the data returned and buffered for a Delayed Inbound Read may be re-accessed following a disconnect. If cleared, following a disconnect, the buffer is invalidated, and a subsequent read to the next location will initiate a new read. Default=0 (Disabled).
- 5:4   **Read Prefetch Size.**  
 This field configures the number of Dwords that will be prefetched on Memory Read Multiple commands. Legal values are:
- |    |                          |    |                          |
|----|--------------------------|----|--------------------------|
| 00 | 16 Dwords (2 x 32 bytes) | 10 | 64 Dwords (8 x 32 bytes) |
| 01 | 32 Dwords (4 x 32 bytes) | 11 | <i>reserved</i>          |
- The normal selection is 32 Dwords. The 64 Dword selection provides highest performance when the PXB is in 64-bit bus mode. Default=01 (32 Dwords).
- 3     **External Arbiter Enable.**  
 This is a read-only bit that selects internal or external arbitration for the PCI bus. The bit reflects the state of the P(A,B)XARB# strapping pin for this bus (A or B). Default=[P(A,B)XARB pin].
- 2     **64-bit Bus Enable.**  
 This is a read-only bit that selects whether the PXB operates as two 32-bit PCI buses or a single 64-bit PCI bus. The bit reflects the state of the MODE64# strapping pin. Default=[MODE64# pin].
- 1     **Host/PCI Bus Gearing Ratio.**  
 This is a read-only bit that selects the system clock to PCI clock gearing ratio. The bit reflects the state of the GEAR4# strapping pin. This bit should be cleared (i.e., GEAR4# is high, or deasserted), resulting in a system clock/ PCI clock gearing ratio of 3:1. Default=[GEAR4# pin].
- 0     *reserved*

### 3.4.5 DID: Device Identification Register

|                 |          |             |           |
|-----------------|----------|-------------|-----------|
| Address Offset: | 02 - 03h | Size:       | 16 bits   |
| Default Value:  | 84CBh    | Attributes: | Read Only |







### 3.4.12 IOABASE: I/O APIC Base Address

|                 |        |            |            |
|-----------------|--------|------------|------------|
| Address Offset: | 68-69h | Size:      | 16 bits    |
| Default Value:  | 0FECh  | Attribute: | Read/Write |

This register defines the base address of the 1MB I/O APIC Space address range. IOABASE applies to both host-initiated transactions and PCI-initiated inbound transactions, and is therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.13 ISA: ISA Space

|                 |     |            |            |
|-----------------|-----|------------|------------|
| Address Offset: | 7Ch | Size:      | 8 bits     |
| Default Value:  | 00h | Attribute: | Read/Write |

This register defines the ISA Space address range. The register applies to both host-initiated transactions and PCI-initiated inbound transactions, and is therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.14 LXGB: Low Expansion Gap Base

|                 |        |            |            |
|-----------------|--------|------------|------------|
| Address Offset: | 54-55h | Size:      | 16 bits    |
| Default Value:  | 0000h  | Attribute: | Read/Write |

This register defines the starting address of the Low Expansion Gap (LXG). LXGB register applies to both host-initiated transactions and PCI-initiated inbound transactions, and is therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.15 LXGT: Low Expansion Gap Top

|                 |        |            |            |
|-----------------|--------|------------|------------|
| Address Offset: | 56-57h | Size:      | 16 bits    |
| Default Value:  | 0000h  | Attribute: | Read/Write |

LXGT defines the highest address of the Low Expansion Gap (LXG), above. This register applies to both host-initiated transactions and PCI-initiated inbound transactions, and is therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.16 MAR[6:0]: Memory Attribute Region Registers

|                 |                                      |            |             |
|-----------------|--------------------------------------|------------|-------------|
| Address Offset: | 61-67h                               | Size:      | 8 bits each |
| Default Value:  | 03h for MAR[0]<br>00h for all others | Attribute: | Read/Write  |

The Intel 450NX PCIset allows programmable memory attributes on 14 memory segments of various sizes in the 640 Kbyte to 1 MByte address range. Seven Memory Attribute Region (MAR) registers are used to support these features. These registers apply to both host-initiated transactions and PCI-initiated transactions, and are therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.17 MLT: Master Latency Timer Register

|                 |     |            |            |
|-----------------|-----|------------|------------|
| Address Offset: | 0Dh | Size:      | 8 bits     |
| Default Value:  | 00h | Attribute: | Read/Write |

MLT is an 8-bit register that controls the amount of time (measured in PCI clocks) the Intel 450NX PCIset, as a bus master, can burst data on the PCI Bus. The Count Value is an 8 bit quantity; however, MLT[2:0] are reserved and assumed to be 0 when determining the Count Value. The number of clocks programmed in the MLT represents the guaranteed time slice allotted to the Intel 450NX PCIset, after which it must complete the current data transfer phase and then surrender the bus as soon as its bus grant is removed.

#### **Bits**    **Description**

7:3    **Master Latency Timer Count Value.**  
Counter value in 8 PCI clock units.

2:0    *reserved (0)*

### 3.4.18 MMBASE: Memory-Mapped PCI Base

|                 |        |            |            |
|-----------------|--------|------------|------------|
| Address Offset: | 70-71h | Size:      | 16 bits    |
| Default Value:  | 0002h  | Attribute: | Read/Write |

The MMBASE register specifies the starting address of this memory-mapped PCI range, and is identical to the MMBASE register in the MIOC. The MMT register specifies the highest address that will be directed to PCI Bus #1B, and corresponds identically to the MMR[3] register in the MIOC. The MMBASE register must be programmed identically to the MMBASE register in the MIOC to achieve correct functioning. See the MIOC Configuration Space for a detailed description.



- 7     **Address/Data Stepping.**  
The PXB does not support address/data stepping, and this bit is hardwired to 0.
- 6     **Parity Error Response (PERRE).**  
If PERRE is set, the PXB will report parity errors on data received by asserting the PERR# signal. Address parity errors are not reported using PERR#, but instead through the SERR# signal, and only if both PERRE and SERRE are set. If PERRE is cleared, then PCI parity errors are not reported by the PXB. Default=0.
- 5     *reserved (0)*
- 4     **Memory Write and Invalidate Enable.**  
Selects whether the PXB, as a PCI master, can generate Memory Write and Invalidate cycles. Default=1.
- 3     **Special Cycle Enable.**  
The PXB will ignore all special cycles generated on the PCI bus, and this bit is hardwired to 0.
- 2     **Bus Master Enable.**  
The PXB does not permit disabling of its bus master capability, and this bit is hardwired to 1.
- 1     **Memory Access Enable.**  
The PXB does not permit disabling access to main memory, and this bit is hardwired to 1.
- 0     **I/O Access Enable.**  
The PXB does not respond to PCI I/O cycles, and this bit is hardwired to 0.

### 3.4.22 PCISTS: PCI Status Register

Address Offset: 06 - 07h                      Size:        16 bits  
Default Value:  0280h                      Attribute:  Read/Write Clear, Sticky

This is a PCI specification required register, with a fixed format.

| <b>Bits</b> | <b>Description</b>                                                                                                                                                                                                |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15          | <b>Parity Error (PE).</b><br>This bit is set when the PXB detects a parity error in data or address on the PCI bus. This bit remains set until explicitly cleared by software writing a 1 to this bit. Default=0. |
| 14          | <b>Signaled System Error (SSE).</b><br>This bit is set when the PXB asserts the SERR# signal. This bit remains set until explicitly cleared by software writing a 1 to this bit. Default=0.                       |

- 13     **Received Master Abort (RMA).**  
 This bit is set when the PXB, as bus master, terminates its transaction (except for Special Cycles) with a master abort. This bit remains set until explicitly cleared by software writing a 1 to this bit.  
 Default=0.
- 12     **Received Target Abort (RTA).**  
 This bit is set when the PXB, as bus master, receives a target abort for its transaction. This bit remains set until explicitly cleared by software writing a 1 to this bit.  
 Default=0.
- 11     **Signaled Target Abort (STA).**  
 This bit is set when the PXB, as bus target, terminates a transaction with target abort. This bit remains set until explicitly cleared by software writing a 1 to this bit.  
 Default=0.
- 10:9   **DEVSEL# Timing (DEVT).**  
 This 2-bit field encodes the timing of the DEVSEL# signal when the PXB responds as a target, and represents the slowest time that the PXB asserts DEVSEL# for any bus command except Configuration Reads or Writes. This field is hardwired to the value 01b (medium).
- 8       **Data Parity Error (DPE).**  
 This bit is set when all of the following conditions are met:  
 1. The PXB asserted PERR# or sampled PERR# asserted.  
 2. The PXB was the initiator for the operation in which the error occurred.  
 3. The PERRE bit in the PCICMD register is set.  
 This bit remains set until explicitly cleared by software writing a 1 to this bit.  
 Default=0.
- 7       **Fast Back-to-Back (FB2B).**  
 The PXB supports fast back-to-back transactions, and this bit is hardwired to 1.
- 6       **UDF Supported.**  
 The PXB does not support User Definable Features (UDF), and this bit is hardwired to 0.
- 5       **66 MHz Capable.**  
 The PXB is not capable of running at 66 MHz, and this bit is hardwired to 0.
- 4:0     *reserved (0)*

### 3.4.23 PMD[1:0]: Performance Monitoring Data Register

|                 |                    |            |              |
|-----------------|--------------------|------------|--------------|
| Address Offset: | D8-DCh, E0-E4h     | Size:      | 40 bits each |
| Default Value:  | 000000000000h each | Attribute: | Read/Write   |

Two performance monitoring counters, with associated event selection and control registers, are provided for each PCI bus in the PXB. The PMD registers hold the performance monitoring count values. Event selection is controlled by the PME registers, and the action performed on event detection is controlled by the PMR registers.

**Bits**    **Description**39:0    **Count Value.****3.4.24 PME[1:0]: Performance Monitoring Event Selection**Address Offset: E8 - EBh  
Default Value: 0000h eachSize: 16 bits each  
Attribute: Read/Write**Bits**    **Description**15    *reserved (0)***14    Count Data Cycles**1: Count the data cycles associated with the selected transactions.  
0: Count the selected event**13:10    Initiating Agent Selection.**

This field qualifies the tracking of bus transactions by limiting event detection to those transactions issued by specific agents.

|      |                 |      |                                            |
|------|-----------------|------|--------------------------------------------|
| 0000 | Agent 0         | 1000 | <i>reserved</i>                            |
| 0001 | Agent 1         | 1001 | <i>reserved</i>                            |
| 0010 | Agent 2         | 1010 | <i>reserved</i>                            |
| 0011 | Agent 3         | 1011 | <i>reserved</i>                            |
| 0100 | Agent 4         | 1100 | <i>reserved</i>                            |
| 0101 | Agent 5         | 1101 | south bridge                               |
| 0110 | <i>reserved</i> | 1110 | Intel® 450NX PCIset agent (i.e., outbound) |
| 0111 | <i>reserved</i> | 1111 | Any agent                                  |

**Note:** This field is applicable only if the PCI bus is operated in internal arbiter mode. If the bus is operated using an external arbiter, this field must be set to *Any Agent* to trigger any events.**9:8    Transaction Destination Selection.**

This field qualifies the tracking of bus transactions by limiting event detection to those transactions directed to a specific resource.

|    |             |    |             |
|----|-------------|----|-------------|
| 00 | Any         | 10 | PCI Target  |
| 01 | Main Memory | 11 | Third party |

7:6    *reserved*

5:0 **Event Selection.**

This field specifies the basic PCI bus transaction or PCI bus signal to be monitored.

**Individual Bus Transactions**

|         |                 |         |                           |
|---------|-----------------|---------|---------------------------|
| 00 0000 | <i>reserved</i> | 00 1000 | <i>reserved</i>           |
| 00 0001 | <i>reserved</i> | 00 1001 | <i>reserved</i>           |
| 00 0010 | I/O Read        | 00 1010 | <i>reserved</i>           |
| 00 0011 | I/O Write       | 00 1011 | <i>reserved</i>           |
| 00 0100 | <i>reserved</i> | 00 1100 | Memory Read Multiple      |
| 00 0101 | <i>reserved</i> | 00 1101 | Dual Address Cycle        |
| 00 0110 | Memory Read     | 00 1110 | Memory Read Line          |
| 00 0111 | Memory Write    | 00 1111 | Memory Write & Invalidate |

**Generic (Grouped) Bus Transactions**

|         |                        |         |                                |
|---------|------------------------|---------|--------------------------------|
| 010 000 | Any bus transaction    | 010 100 | Any I/O transaction            |
| 010 001 | Any memory transaction | 010 101 | Any I/O or memory transactions |
| 010 010 | Any memory read        | 010 110 | Any I/O read or memory read    |
| 010 011 | Any memory write       | 010 111 | Any I/O read or memory write   |

**Bus Signal Assertions**

|         |                    |         |                 |
|---------|--------------------|---------|-----------------|
| 011 000 | <i>reserved</i>    | 011 100 | <i>reserved</i> |
| 011 001 | <i>reserved</i>    | 011 101 | <i>reserved</i> |
| 011 010 | RETRY <sup>1</sup> | 011 110 | LOCK            |
| 011 011 | <i>reserved</i>    | 011 111 | ACK64           |

All other encodings are reserved.

Note:

1. Counting data cycles is undefined for this selection.

### 3.4.25 PMR[1:0]: Performance Monitoring Response

Address Offset: DDh, E5h                      Size: 8 bits each  
 Default Value: 0000h each                    Attribute: Read/Write

There are two PMR registers for each PCI bus, one for each PMD counter. Each PMR register specifies how the event selected by the corresponding PME register affects the associated PMD register, P(A,B)MON# pins, and the INT(A,B)RQ# pins.

| <b>Bits</b> | <b>Description</b> |
|-------------|--------------------|
|-------------|--------------------|

7:6 **Interrupt Assertion**

Defines how selected event affects INTRQ# assertion. Whenever INTRQ# is asserted, a flag for this counter is set in the Error Status Register, so that software can determine the cause of the interrupt. This flag is reset by writing the Error Status Register.

- |   |                                          |
|---|------------------------------------------|
| 0 | Selected event does not assert INTRQ #   |
| 1 | <i>reserved</i>                          |
| 2 | Assert INTRQ# pin when event occurs      |
| 3 | Assert INTRQ# pin when counter overflows |

5:4 **Performance Monitoring pin assertion**

Defines how the selected event affects the PMON# pin for this counter.

- |   |                                                       |
|---|-------------------------------------------------------|
| 0 | PMON# pin is tristated. Selected event has no effect. |
| 1 | <i>reserved</i>                                       |





and the Top of Memory (TOM); however, the base address must be aligned on the next highest power-of-2 natural boundary given the chosen size. Incorrect alignment results in indeterminate operation.

Default: 000Ah (representing a base address of A0000h)

### 3.4.30 TCAP: Target Capacity

Address Offset: C0-C2h                      Size:            24 bits  
 Default Value:  041082h                    Attribute:    Read/Write

This register is programmed with the maximum number of transactions and data bytes that the receiving MIOC can accept from this PXB/PCI port for inbound transactions. The MIOC space has a set of four similar TCAP registers, one per PXB/PCI bus, that is programmed with the transaction and data limits for *outbound* transactions.

If the PXB is in 32-bit bus mode, divide the MIOC BUFSIZ limits in half. If the PXB is in 64-bit bus mode, the full MIOC BUFSIZ limits can be used, except in either case, the PXB's maximum values (shown below) cannot be exceeded.

#### **Bits    Description**

- 23:18    **Inbound Write Transaction Capacity.**  
 This field specifies the total number of inbound write transactions that can be forwarded and enqueued in the MIOC from this PXB/PCI port.
- |            |                 |                    |            |
|------------|-----------------|--------------------|------------|
| 32-bit Bus | PXB maximum: 6  | Minimum allowed: 1 | Default= 1 |
| 64-bit Bus | PXB maximum: 12 | Minimum allowed: 1 | Default= 1 |
- 17:12    **Inbound Read Transaction Capacity.**  
 This field specifies the total number of inbound read transactions that can be forwarded and enqueued in the MIOC from this PXB/PCI port.
- |            |                |                    |            |
|------------|----------------|--------------------|------------|
| 32-bit Bus | PXB maximum: 2 | Minimum allowed: 1 | Default= 1 |
| 64-bit Bus | PXB maximum: 2 | Minimum allowed: 1 | Default= 1 |
- 11:6     **Inbound Write Data Buffer Capacity.**  
 This field specifies the total number of data buffers available in the MIOC for use by inbound write transactions from this PXB/PCI port, in increments of 32 bytes.
- |            |                 |                    |            |
|------------|-----------------|--------------------|------------|
| 32-bit Bus | PXB maximum: 6  | Minimum allowed: 2 | Default= 2 |
| 64-bit Bus | PXB maximum: 12 | Minimum allowed: 2 | Default= 2 |
- 5:0      **Inbound Read Data Buffer Capacity.**  
 This field specifies the total number of data buffers available in the MIOC for use by inbound read transactions from this PXB/PCI port, in increments of 32 bytes.
- |            |                 |                    |            |
|------------|-----------------|--------------------|------------|
| 32-bit Bus | PXB maximum: 8  | Minimum allowed: 2 | Default= 2 |
| 64-bit Bus | PXB maximum: 16 | Minimum allowed: 2 | Default= 2 |

### 3.4.31 TMODE: Timer Mode

Address Offset: C4h                            Size:            8 bits  
 Default Value:  00h                            Attribute:    Read/Write

This register allows nominally fixed-duration timers to be adjusted to shorter values for test purposes.

| <u>Bits</u> | <u>Description</u> |
|-------------|--------------------|
|-------------|--------------------|

|     |                     |
|-----|---------------------|
| 7:2 | <i>reserved (0)</i> |
|-----|---------------------|

|     |                                                 |
|-----|-------------------------------------------------|
| 1:0 | <b>Delayed Read Request Expiration Counter.</b> |
|-----|-------------------------------------------------|

This counter is strictly for test purposes. Changing it from the default value is a violation of the PCI specification.

|    |                                |
|----|--------------------------------|
| 00 | normal mode ( $2^{15}$ clocks) |
| 01 | 128 clocks                     |
| 10 | 64 clocks                      |
| 11 | 16 clocks                      |

### 3.4.32 TOM: Top of Memory

|                        |                       |
|------------------------|-----------------------|
| Address Offset: 50-52h | Size: 24 bits         |
| Default Value: 000FFFh | Attribute: Read/Write |

This register specifies the highest physical address that could be directed to the memory. This register applies to both host-initiated transactions and PCI-initiated inbound transactions, and is therefore duplicated in both the MIOC and PXB Configuration Spaces. Software must ensure that both sets are programmed identically to achieve correct functioning. See the MIOC Configuration Space for a detailed description.

### 3.4.33 VID: Vendor Identification Register

|                          |                       |
|--------------------------|-----------------------|
| Address Offset: 00 - 01h | Size: 16 bits         |
| Default Value: 8086h     | Attributes: Read Only |

| <u>Bits</u> | <u>Description</u> |
|-------------|--------------------|
|-------------|--------------------|

|      |                                      |
|------|--------------------------------------|
| 15:0 | <b>Vendor Identification Number.</b> |
|------|--------------------------------------|

This is a 16-bit value assigned to Intel. Intel VID = 8086h.



## 4.1 Memory Address Map

A Pentium® II Xeon™ processor system based on the Intel® 450NX PCIset supports up to 64 GBytes of addressable memory space. Within this memory address range the Intel 450NX PCIset has two structured compatibility regions, two expansion gaps, and two general purpose memory-mapped I/O spaces, as illustrated in Figure 4-1. The two compatibility regions are the 1 MB Low Compatibility Region at the bottom of the address space, and the 20 MB High Compatibility Region just below the 4 GB boundary. The two expansion gaps allow holes to be opened in the address space, where accesses can be directed to the PCI buses or to a third-party agent, instead of to memory. The two I/O spaces allow control over which addresses are forwarded to each of the four PCI buses supported by the Intel 450NX PCIset.

### Spaces and Gaps

The Intel 450NX PCIset memory address map is based on *spaces* and *gaps*.

A *space* is an address range where the access is directed to a specific destination, usually (but not always) a PCI bus. Any DRAM behind the space is not reclaimed, unless it is also covered by a gap (described below). The Intel 450NX PCIset supports a variety of spaces with fixed or configurable address ranges and individual enables.

A *gap* is a memory-mapped address range where the access is specifically *not* directed to DRAM. The DRAM behind the gap is reclaimed; that is, the effective address presented to the memory has the gaps subtracted from it, presenting a contiguous address space to the memory. The gap does not control where the access is directed. Accesses may be directed through an overlapping space, or left unclaimed on the system bus for a third-party agent to claim. In typical maps, large spaces will be contained within gaps, to reclaim the DRAM that would otherwise be wasted. The Intel 450NX PCIset supports two configurable gaps.

### Low Compatibility Region

The Low Compatibility Region spans the first 1 MB address range (0h to F\_FFFFh). This region is divided into five subregions, some of which are further subdivided.

- The 640 KB DOS Region is split into a 512 KB DOS area (memory only) and a 128 KB ISA Window, which can be mapped to either main memory or the PCI memory.
- The 128 KB Graphics Adapter Memory is normally mapped to a video device on the PCI bus, typically a VGA controller. This region is also the default location of the configuration SMM RAM space.

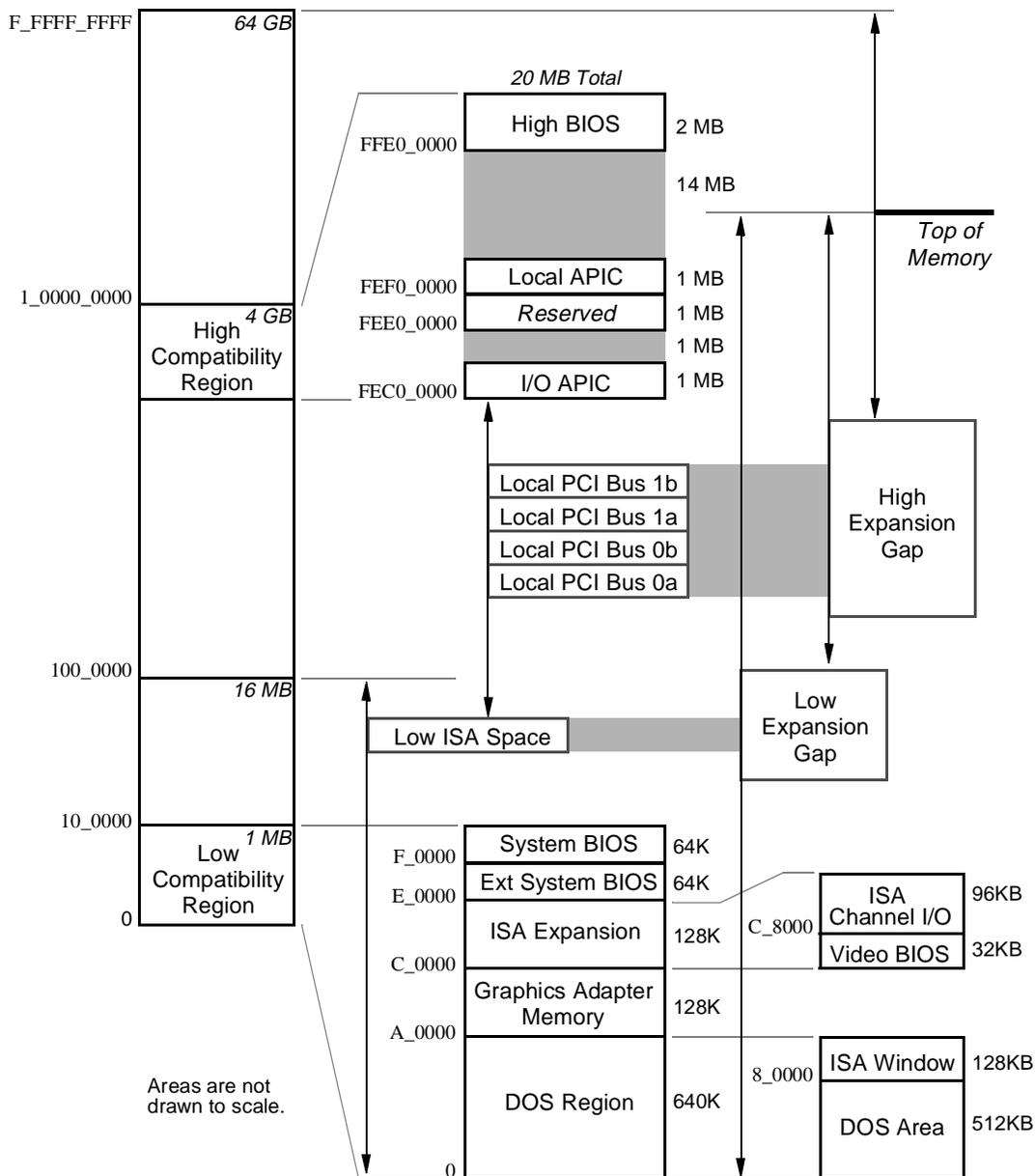
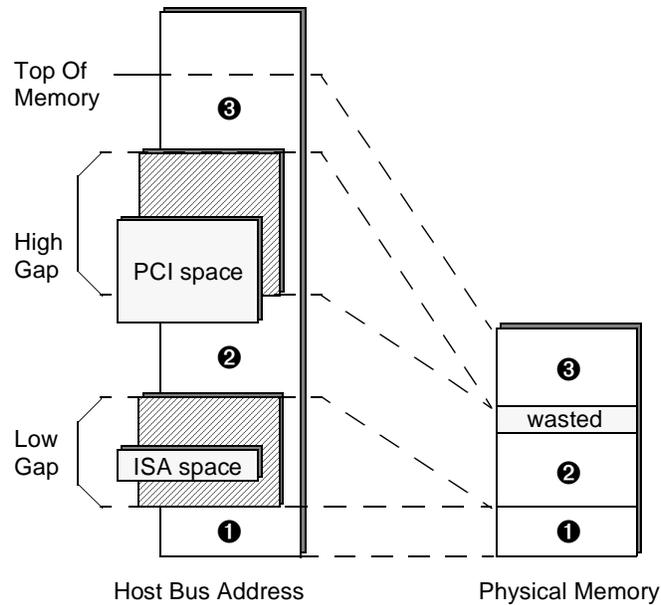


Figure 4-1: System Memory Address Space

- The 128 KB ISA Expansion Region is divided into eight 16 KB blocks that can be independently configured for read/write accessibility. Typically, these blocks are mapped through the PCI bridge to ISA space. Memory that is disabled is not remapped. Traditionally, the lower 32 KB contains the video BIOS located on a video card, and the upper 96 KB is made available to expand memory windows in 16 KB blocks depending on the requirements of other channel devices in the corresponding ISA space.
- The 64 KB Extended System BIOS Region is divided into four 16 KB blocks and may be mapped either to memory or the compatibility PCI bus. Typically, this area is used for RAM or ROM. Selecting appropriate read/write attributes for this region allows the BIOS to be “shadowed” into RAM.



**Figure 4-2: Gaps, Spaces and Reclaiming Physical Memory**

- The 64 KB System BIOS Region is treated as a single block and is normally mapped to the compatibility PCI bus. Selecting appropriate read/write attributes for this region allows the BIOS to be “shadowed” into RAM. After power-on reset, the Intel® 450NX PCIset has this area configured to direct accesses to PCI memory, allowing fetches from the boot ROM during system initialization.

#### High Compatibility Region

The High Compatibility Region spans 20 MB immediately below the 4 GB address boundary (address range FEC0\_0000h to FFFF\_FFFFh). This region supports four fixed spaces with predefined functions for compatibility with PC-based systems.

- The 2 MB High BIOS Space is where the processor begins execution after reset. Following power-on, the Intel® 450NX PCIset has this space enabled; accesses will be directed to the compatibility PCI bus. If an ISA bridge is also used, this area is then aliased by the ISA bridge to the top of the ISA address range (14-16 MB). If this space is disabled, accesses will be directed to memory (unless superseded by an expansion gap.)
- The 1 MB Local APIC Space is reserved for use by the processor. In Pentium® II Xeon™ processors, this contains the default local APIC space (which can be remapped to the I/O APIC space, below). Accesses to this region will not be claimed by the Intel 450NX PCIset. *No resources should be mapped to this region.*
- The 1 MB Reserved Space is defined for future use. *No resources should be mapped to this region.*
- The 1 MB I/O APIC Configuration Space provides an area where I/O APIC units in the system can be mapped, and the I/O APICs within the processors can be remapped for consistency of access. At least one I/O APIC must be included in an Intel 450NX PCIset-based system. The I/O APIC space may be relocated anywhere in the 4 GB boundary.

### Top of Memory and Expansion Gaps

A “Top of Memory” pointer identifies the highest memory-mapped address that can be serviced by this node. Accesses to addresses above this pointer will not be directed to local memory or the PCI buses, but will be allowed to sit unclaimed on the system bus. A third-party agent on the system bus may claim such accesses, either servicing them with its own local resources or forwarding them to other nodes for service (i.e., a cluster bridge). Any access that remains unclaimed will eventually timeout in the Intel 450NX PCIset; on timeout the access is claimed by the Intel 450NX PCIset and terminated.

Below the Top of Memory, there are two programmable expansion gaps: the Low Expansion Gap and the High Expansion Gap. Each gap, if enabled, opens a “hole” in the physical address space, where accesses will not be directed to memory. Instead, these accesses may be directed to one of the PCI buses, or will be allowed to sit unclaimed on the system bus where they may be claimed by a third-party agent, as above.

Both expansion gaps are defined using base and top addresses, on 1MB boundaries. The Low Expansion Gap must be located *above* the Low Compatibility Region, and *below* the High Expansion Gap, the 4 GB boundary, and the Top of Memory. The High Expansion Gap must be located *above* the enabled Low Expansion Gap, *above* 1MB, and *below* the Top of Memory. At power-on, both gaps are disabled.

## 4.1.1 Memory-Mapped I/O Spaces

The Intel® 450NX PCIset provides two programmable I/O spaces: the Low ISA Space and the PCI Space. Both spaces allow accesses to be directed to a PCI bus. Any region defined as memory-mapped I/O must have a UC (UnCacheable) memory type, set in the Pentium II Xeon processor’s MTTR registers.

### Low ISA Space

The Low ISA Space is provided to support older ISA devices which cannot be relocated above the 16 MB address limit of older systems. Accesses to this space will be directed down to the compatibility PCI bus (0A). The Low ISA Space can start on any 1 MB boundary below 16 MB, and can be of size 1, 2, 4 or 8 MB.

### PCI Space

The PCI Space consists of four contiguous address ranges, allowing accesses to be directed to each of the four PCI buses supported by the Intel 450NX PCIset. Each address range corresponds to a PCI bus, and is configurable on 1 MB boundaries.

## 4.1.2 SMM RAM Support

Intel Architecture processors include a System Management Mode (SMM) that defines a protected region of memory called SM RAM. The Intel 450NX PCIset allows an SM RAM region to be defined and enabled. When enabled, memory reads and writes to addresses that fall within the SM RAM address range are protected accesses. If the configuration enables permit access, and the requesting agent asserts SMMEM# (privileged access), the MIOC will



### Restricted-Access Addresses

By default, all Host-PCI I/O writes will be posted. However, in traditional Intel-architecture systems, there are certain I/O addresses to which posting is not desirable, due to ordering side effects. Table 4-1 lists the I/O addresses for which I/O write posting will not be supported, regardless of the posting enable in the MIOC's CONFIG register. These accesses will be deferred instead.

**Table 4-1: Non-Postable I/O Addresses**

| Address      | Function                                            |
|--------------|-----------------------------------------------------|
| 0020h-0021h  | 8259A Interrupt Controller, Master, Interrupt Masks |
| 0060h-0064h  | Keyboard controller: com/status and data            |
| 0070h        | NMI# Mask                                           |
| 0092h        | A20 Gate                                            |
| 00A0h-00A1h  | 8259A Interrupt Controller, Slave, Interrupt Masks  |
| 00F0h        | IGNNE#, IRQ13                                       |
| 0CF8h, 0CFCh | PCI configuration space access                      |

## 4.3 PCI Configuration Space

The Intel® 450NX PCIsset provides a PCI-compatible configuration space for the MIOC, and two in the PXB—one for each PCI bus. I/O reads and writes issued on the system bus are normally claimed by the MIOC and forwarded through the PXBs as I/O reads and writes on the PCI bus. However, I/O accesses to the **0CF8h** and **0CFCh** addresses are defined as special configuration accesses for I/O devices.

Each configuration space is selected using a Bus Number and a Device Number within that bus. PCI buses are numbered in ascending order within hierarchical buses. PCI Bus #0 represents both the compatibility PCI bus as well as the devices in the Intel 450NX PCIsset and any third party agents attached to the system bus.

The MIOC and each PCI bus within each PXB in the system is assigned a unique Device Number on Bus #0, as shown in Table 4-2. The PXBs are numbered based on the Expander bus port used.

**Table 4-2: Device Numbers for Bus Number 0<sup>1 2</sup>**

| Device Number | Device                    | Device Number | Device |
|---------------|---------------------------|---------------|--------|
| 10h           | MIOC                      | 18h           |        |
| 11h           | reserved                  | 19h           |        |
| 12h           | PXB 0, Bus a <sup>3</sup> | 1Ah           |        |
| 13h           | PXB 0, Bus b              | 1Bh           |        |

**Table 4-2: Device Numbers for Bus Number 0 (Continued)<sup>1 2</sup>**

| <b>Device Number</b> | <b>Device</b> | <b>Device Number</b> | <b>Device</b>            |
|----------------------|---------------|----------------------|--------------------------|
| 14h                  | PXB 1, Bus a  | 1Ch                  | <i>Third Party Agent</i> |
| 15h                  | PXB 1, Bus b  | 1Dh                  | <i>Third Party Agent</i> |
| 16h                  |               | 1Eh                  | <i>Third Party Agent</i> |
| 17h                  |               | 1Fh                  | n/a <sup>4</sup>         |

1. Device numbers 0-15 represent devices actually on the compatibility PCI bus.
2. Shaded columns are defined for future PCIset compatibility.
3. This is the compatibility PCI bus.
4. Bus #0/Device # 31 is used (along with a Function Number of all 1's and a Register Number of all 0's) to generate a PCI Special Cycle. Therefore Bus #0/Device #31 is never mapped to a device.



## 5.1 System Bus

The host interface of the Intel® 450NX PCIset is targeted toward Pentium® II Xeon™ processor-based multiprocessor systems, and is specifically optimized for four processors sharing a common bus with bus clock frequencies of 100 MHz. The MIOC provides the system bus address, control and data interfaces for the Intel 450NX PCIset, and represents a single electrical load on the system bus.

The Intel 450NX PCIset recognizes and supports a large subset of the transaction types that are defined for the P6 family processor's bus interface. However, each of these transaction types have a multitude of response types, some of which are not supported by this controller. The responses that are supported by the MIOC are: *Normal without Data*, *Normal with Data*, *Retry*, *Implicit Write Back*, *Deferred Response*. Refer to the chapter on Transactions for more details on the transaction types supported by the Intel 450NX PCIset.

## 5.2 PCI Bus

Each PXB provides two independent 32-bit, 33 MHz Rev. 2.1-compliant PCI interfaces which support 5 volt or 3 volt PCI devices. Each bus will support up to 10 electrical loads, where the PXB and the PIIX4E south bridge each represent one load, and each connector/device pair represents two loads. The internal bus arbiter supports six PCI bus masters in addition to the PXB itself and the south bridge on the compatibility bus. The compatibility bus is always bus #0A (PXB #0, Bus A).

The PCI buses are operated synchronously with the system bus, using the system bus clock as the master clock. A system bus/PCI bus clock ratio of 3:1 supports the Intel Pentium® II Xeon™ processor at 100 MHz with 33.3 MHz PCI bus, or a degraded 90 MHz system bus with a 30 MHz PCI bus (or lower, depending on the effect of the 6th load on the system bus).

A configuration option allows the two 32-bit PCI buses (A and B) on a single PXB to be operated in combination as a single 64-bit PCI bus. Bus A data represents the low Dword, while bus B data represents the high Dword.

## 5.3 Expander Bus

The Expander Interface provides a bidirectional path for data and control between the PXB and MIOC components. The Expander bus consists of a 16 bit wide data bus which carries command, address, data, and transaction information. There are two additional bits that carry

Byte enable information for data fields. All 18 of these bits are protected by an even parity signal. Two synchronous arbitration signals (one in each direction) are used for each Expander bus.

### 5.3.1 Expander Electrical Signal and Clock Distribution

The Expander bus is designed to allow multiple high bandwidth I/O ports to be added to the Intel® 450NX PCIsset with minimal impact on signal pin count. The Expander bus also provides flexibility in server system topology by allowing the I/O subsystem to be located away from the main PCIsset. This flexibility is achieved with a signaling scheme that uses a combination of synchronous and source synchronous clocking. This is illustrated in Figure 5-1.

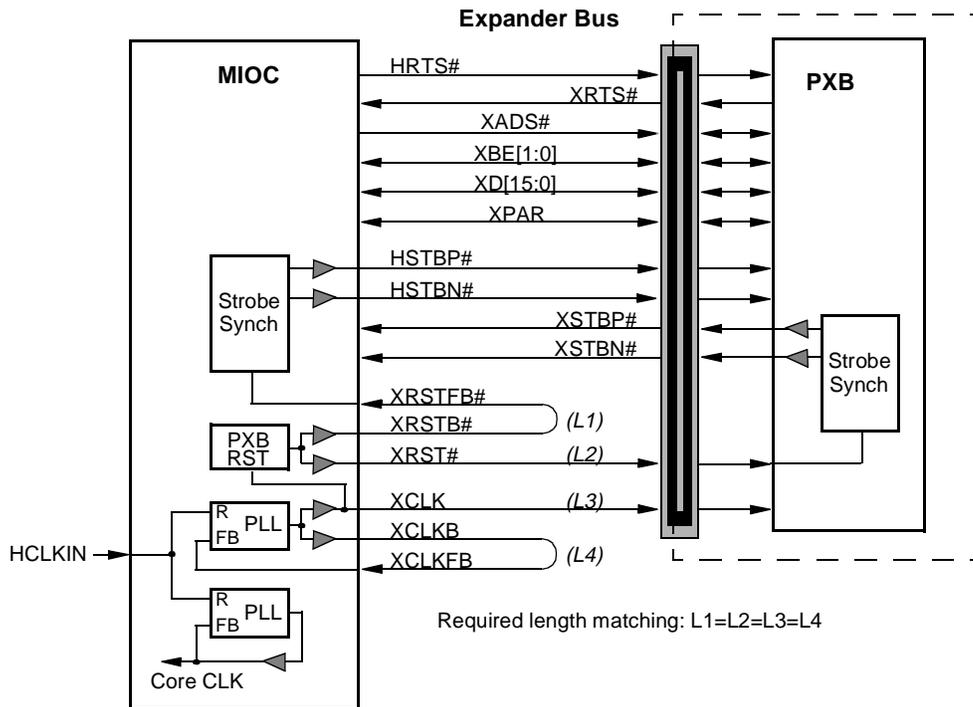


Figure 5-1: Expander Bus Clock Distribution

## 5.4 Third-Party Agents

In addition to the processors and the Intel® 450NX PCIsset, the Pentium® II Xeon™ processor bus allows for additional bus masters, generically referred to as *third-party agents (TPA)*. These agents may be symmetric agents, in which case they must participate in the bus arbitration algorithm used by the processors. They may also be priority agents, in which case they must negotiate with the Intel 450NX PCIsset for control of the system bus.

The Intel 450NX PCIset supports the same request/grant and third-party control signals originally provided by the Intel 450GX PCIset. These signals are used to exchange priority ownership of the bus between the TPA and the Intel 450NX PCIset. The Intel 450NX PCIset makes no assumptions about the relative priorities between the Intel 450NX PCIset and the TPA, and will grant priority ownership at the next natural transaction boundary. The Intel 450NX PCIset also makes no assumptions about the frequency of TPA requests or the duration of TPA bus ownership; it is the responsibility of the TPA to ensure that its use of the system bus is commensurate with its intended purpose and expected system performance.

## 5.5 Connectors

Connectors are permitted only for the memory cards and between the MIOC and PXBs. Between MIOC and PXB, some degree of “stretch” distance is possible, with specific distance dependent on the design and medium chosen. Connectors are specifically not permitted between the MIOC and the system bus.



## 6.1 Overview

The Intel 450NX<sup>®</sup> PCIset's memory subsystem consists of one or two memory cards. Each card is comprised of one RCG component, a DRAM array, and two MUX components. Table 6-1 summarizes the Intel 450NX PCIset's general memory characteristics.

**Table 6-1: General Memory Characteristics**

|                   |                                                                             |
|-------------------|-----------------------------------------------------------------------------|
| DRAM type         | Extended Data Out (EDO)                                                     |
| Memory modules    | 72-bit, single and double high DIMMs                                        |
| DRAM technologies | 16 Mbit and 64 Mbit<br>50 and 60 nsec<br>3.3 V                              |
| Interleaves       | 4:1, 2:1 (in bank 0, of card 0)                                             |
| Memory size       | 2:1 interleave: 32 MB<br>4:1 interleave: 64 MB to 8 GB, in 64 MB increments |

### 6.1.1 Physical Organization

The Intel<sup>®</sup> 450NX PCIset supports up to 8 banks of memory, configured across one or two memory cards. Each bank can support up to 1 GB using 64 Mbit double-high DIMMs to provide a total of 8 GB of memory in 8 banks. Each bank can support one or two rows of 2 or 4 interleaves. Each row represents a set of memory devices simultaneously selected by a RAS# signal. Each interleave generates 72 bits (64 data, 8 ECC) of data per row using one DIMM. Four interleaves provide a total of 256 bits of data (32 bytes) which is one cache line for the Pentium<sup>®</sup> II Xeon<sup>™</sup> processor. Data from multiple interleaves are combined by the MUXs to exchange 72 bits of data with the MIOC at an effective rate of one cache line every 30ns (effective rate: 1.067 GB/s) for a 4-way interleaved memory. Figure 6-1 illustrates this configuration.

#### The RCG and MUX Components

The RCGs generate the signals to control accesses to the main memory DRAMs. The RCG initiates no activity until it receives a command from the MIOC. The maximum number of RCGs per Intel 450NX PCIset system is two. Each RCG controls up to four banks of DRAM. Each bank of memory may consist of one (for single-sided DIMMs) or two (for double-sided or double-high DIMMs) rows. Internally, each RCG component contains four RAS/CAS control units (RCCUs), each dedicated to one bank of DRAM. This is illustrated in Figure 6-2.

Each MUX component has four 36-bit data I/O connections to DRAM (one 18-bit path for each of four possible interleaved quad-words) and one 36-bit data I/O connection to the MD

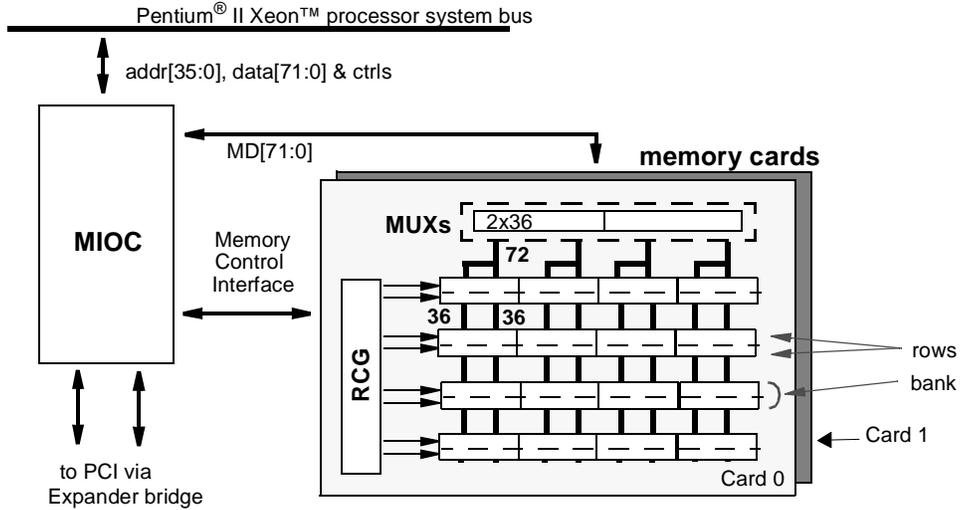


Figure 6-1: Memory Configuration Using 2 Cards

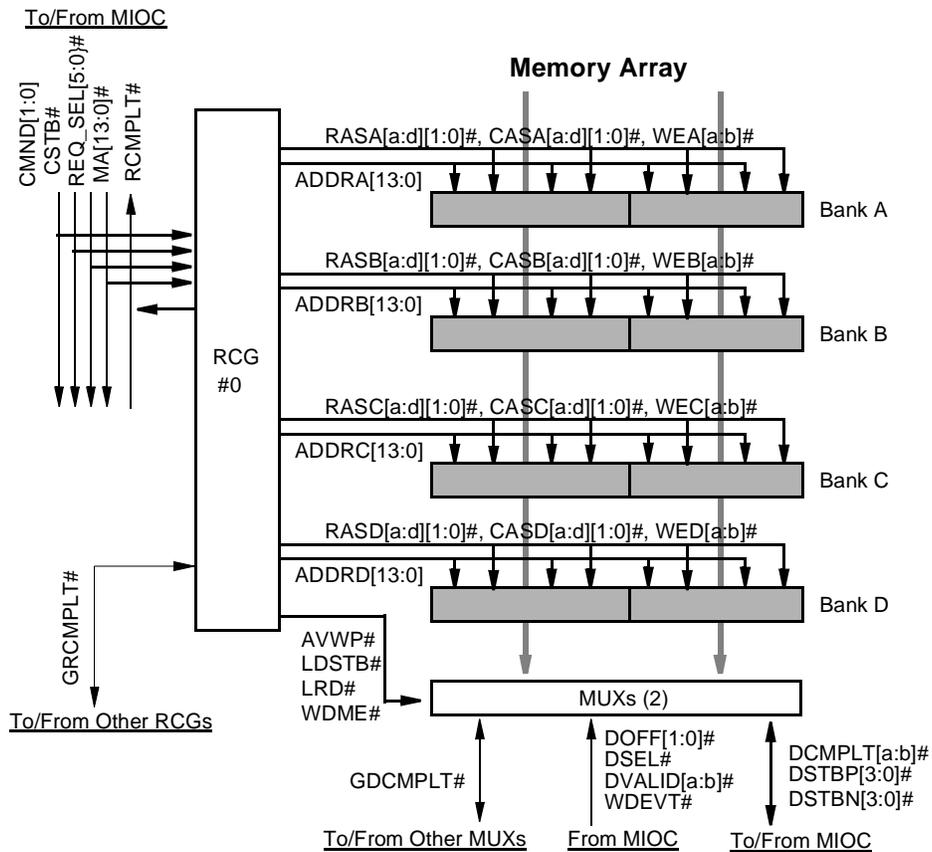


Figure 6-2: Example Showing RCG/MUX Control Signals

bus. There are two MUX components per board to provide a 72-bit data path from each of four possible interleaved quad-words to the MD bus. This is illustrated in Figure 6-3.

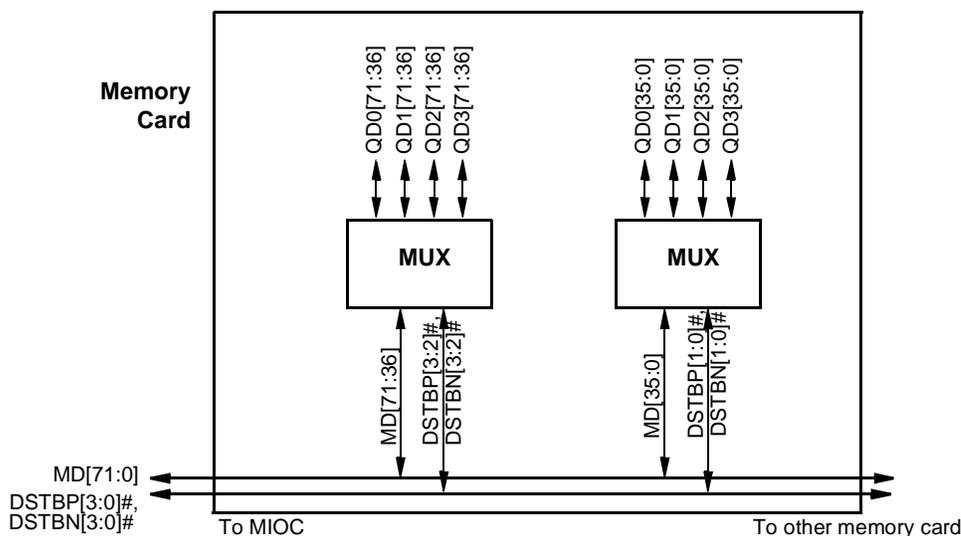


Figure 6-3: Memory Card Datapath

## 6.1.2 Configuration Rules and Limitations

Memory array configurations are governed by the following rules:

- Either one or two cards can be populated in a working system.
- Any number of memory rows, on either card, can be populated in a working system.
- Memory banks can be populated in any order on either card.
- Cards designed to support 4:1 interleaving will also support 2:1 interleaves (in the first bank only).
- Within any given row, the populated interleaves must have DIMMs of uniform size.
- Memory sizes (16 MB vs. 64 MB) may be mixed within a memory card, but must be the same within a bank.
- Memory speeds (60ns or faster) may be mixed, but all four banks within an RCG operate at the same speed, and must therefore be configured to the slowest DIMM in the set.

### 6.1.2.1 Interleaving

The Intel 450NX PCIset supports 4:1 interleaving across all banks, and 2:1 interleaving in the first bank of card #0 only. The Intel 450NX PCIset does not support non-interleaved configurations. Interleave configuration register programming must be consistent across the entire memory system. For example, if one bank is configured as 4:1 then the entire memory sub-system must be 4:1 and the associated memory bank configuration registers must be programmed as 4:1.

To support a 4:1 interleave requires two MUXs. Supporting a 2:1 interleave requires only one MUX. A two-MUX design will also support 2:1 interleaves. An entry-level card (i.e., 2:1

interleave) that may be expanded beyond the first bank must therefore be designed using two MUXs.

Table 6-2 gives a summary of the characteristics of memory configurations supported by the Intel 450NX PCIset for 4-way interleaved memory cards.

**Table 6-2: Minimum and Maximum Memory Size Per Card**

| DRAM Technology & Config. |         | DIMM Size | Addressing              |              |          | Memory Size for 4-way Interleave |             |                         |
|---------------------------|---------|-----------|-------------------------|--------------|----------|----------------------------------|-------------|-------------------------|
|                           |         |           | Mode                    | Size row/col |          | Min (DIMMs)                      | Max (DIMMs) | Max (Double-high DIMMs) |
| 16M                       | 2M x 8  | 2M x 72   | Asymmetric              | 11           | 10       | 64 MB                            | 256 MB      | 512 MB                  |
|                           | 4M x 4  | 4M x 72   | Symmetric<br>Asymmetric | 11<br>12     | 11<br>10 | 128 MB                           | 512 MB      | 1 GB                    |
| 64M                       | 8M x 8  | 8M x 72   | Asymmetric              | 12           | 11       | 256 MB                           | 1 GB        | 2 GB                    |
|                           | 16M x 4 | 16M x 72  | Symmetric<br>Asymmetric | 12<br>13     | 12<br>11 | 512 MB                           | 2 GB        | 4 GB                    |

### 6.1.2.2 Address Bit Permuting Rules and Limitations

The Intel 450NX PCIset supports permuting of cache lines across two or four populated banks. For a complete description of the operation of Address Bit Permuting (ABP) see Section 6.1.3.

The following rules and limitations are required for ABP to operate properly.

- All banks must be in 4:1 interleave mode.
- There must be a power of two number of banks populated.
- All banks within an ABP group (2 banks in 2 bank permuting and 4 banks in 4 bank permuting) must be the same size.
- All populated rows must be adjacent and start at bank 0.
- Both cards in a system must be configured to allow equivalent ABP settings (i.e., Card 0 and Card 1 must both be configured according to the above rules for the current setting of the ABP enable.)

### 6.1.2.3 Card to Card (C2C) Interleaving Rules and limitations

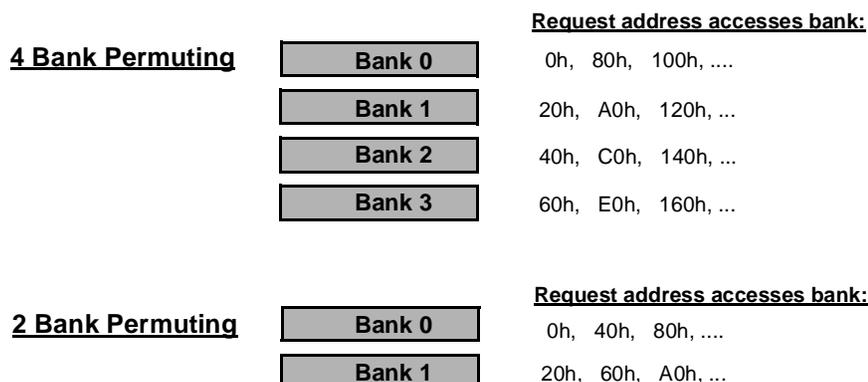
Card to Card Interleaving is described in detail in Section 6.1.4. All of the ABP rules defined above apply to C2C interleaving, plus the following rules:

- The memory cards must be identically populated with memory DIMMs of the same size and type.
- The DBC registers must be programmed in the alternate C2C order as defined in the C2C functional description in Section 6.1.4.

### 6.1.3 Address Bit Permuting

Address Bit Permuting works by increasing the likelihood that requests spaced closely together in time access different banks of memory which will already be closed and precharged.

This is achieved by distributing the addresses, on a cache line size granularity, across either two or four banks of memory. The lowest order address bits which define a cache line are used as the bank selects into the memory array so that all requests to a zero based cache line are directed at bank 0. This is illustrated in Figure 6-4.



**Figure 6-4: Effect of Address Bit Permuting on Bank Access Order**

### 6.1.4 Card to Card (C2C) Interleaving

The purpose of the C2C feature is to further distribute memory accesses across multiple banks of memory as done with the ABP modes. This mode is supported in addition to the standard ABP modes so that maximum distribution of memory accesses and hence, maximum sustained bandwidth can be achieved.

The distribution of accesses to each memory card with C2C enabled is by cache line with all even cache lines sent to Card 0 and all odd cache lines sent to Card 1. The feature can be enabled, if all of the restrictions are met, by setting bit 2 of the MIOC CONFIG register.

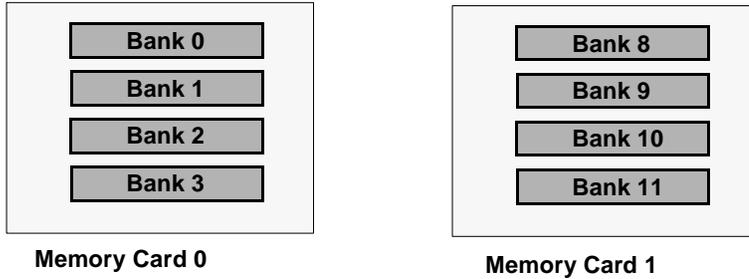
With C2C enabled the DRAM Bank Configuration Registers become mapped to the physical memory differently than with C2C disabled (default mode). Figure 6-5 shows both the C2C disabled and enabled modes mapping of DRAM Bank Configuration Registers to physical bank location.

With C2C enabled and 2 bank ABP enabled Banks 0, 1, 2 and 3 must all be the same size and type and Banks 4, 5, 6 and 7 (if present) must be the same size and type.

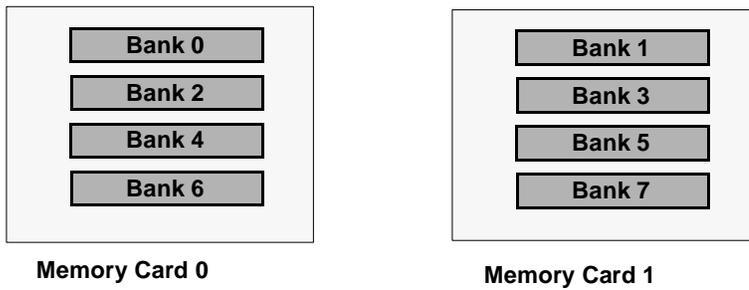
With C2C enabled and 4 bank ABP enabled Banks 0 through 7 must all be the same size and type.

With C2C enabled and no ABP enabled each pair of consecutive banks must be of the same size and type. For example Banks 0 and 1 must be the same size and type and Banks 2 and 3 must be the same size and type but need not match Banks 0 and 1.

**C2C Disabled Bank Register Ordering**



**C2C Enabled Bank Register Ordering**



**Figure 6-5: DRAM Bank Configuration Register Programming with C2C Disabled and Enabled**

**6.1.5 Memory Initialization**

The MIOC provides an MRESET# output, which is asserted on power-good reset, system hard reset, and a BINIT reset. The MRESET# signal is sent to all RCGs and MUXs in the memory subsystem. When asserted, each RCG and MUX clears their transaction queues, data buffers and transaction state. Any transactions that may have been in-progress or pending in the memory subsystem are lost. Note that this may corrupt the contents of the DRAMs, and could leave the DRAMs themselves in an intermediate state, unable to accept a new transaction. Following MRESET# deassertion, the MIOC will re-initialize the memory subsystem by issuing eight CAS#-before-RAS# refreshes per bank (this does not affect the data held in the memory).

This chapter describes the transactions supported by the Intel® 450NX PCIset.

## 7.1 Host To/From Memory Transactions

### 7.1.1 Reads and Writes

The Read transactions supported by the Intel 450NX PCIset are: *Partial Reads*, *Part-line Reads*, *Cache Line Reads*, *Memory Read and Invalidate (length > 0)*, *Memory Read and Invalidate (length = 0)*, *Memory Read (length = 0)*.

The Write transactions supported by the Intel 450NX PCIset are: *Partial Writes*, *Part-line Writes*, *Cache Line Writes*.

### 7.1.2 Cache Coherency Cycles

The MIOC implements an implicit writeback response during system bus read and write transactions when a system bus agent asserts HITM# during the snoop phase. In the read case the MIOC snarfs the writeback data and updates the DRAM. The write case has two data transfers: the requesting agent's data followed by the snooping agent's writeback data.

### 7.1.3 Interrupt Acknowledge Cycles

A processor agent issues an Interrupt Acknowledge cycle in response to an interrupt from an 8259-compatible interrupt controller. The Interrupt Acknowledge cycle is similar to a partial read transaction, except that the address bus does not contain a valid address. The interrupt acknowledge request issued by the processor is deferred by the MIOC and forwarded to PXB #0, which performs a PCI Interrupt Acknowledge cycle on PCI bus #0A (the compatibility PCI bus).

### 7.1.4 Locked Cycles

The system bus specification provides a means of performing a bus lock. Any Host-PCI locked transaction will initiate a PCI locked sequence. The processor implements the bus lock

mechanism which means that no change of bus ownership can occur from the time the agent has established the locked sequence (i.e., asserts **LOCK#** signal on the first transaction and data is returned) until it is completed. The DRAM is locked from the PCI perspective until the host locked transaction is completed.

## 7.1.5 Branch Trace Cycles

An agent issues a Branch Trace Cycle for taken branches if execution tracing is enabled. The address **Aa[35:3]#** is reserved and can be driven to any value. **D[63:32]#** carries the linear address of the instruction causing the branch and **D[31:0]#** carries the target linear address. The MIOC will respond and retire this transaction but will not latch the value on the data lines or provide any additional support for this type of cycle.

## 7.1.6 Special Cycles

Special cycles are used to indicate to the system some internal processor conditions. The first address phase **Aa[35:3]#** is undefined and can be driven to any value. The second address phase, **Ab[15:8]#** defines the type of Special Cycle issued by the processor. Table 7-1 below specifies the cycle type and definition as well as the action taken by the MIOC when the corresponding cycles are identified.

**Table 7-1: MIOC Actions on Special Cycles**

| <b>Ab[15:8]</b> | <b>Cycle Type</b>      | <b>Action Taken</b>                                                                                                                                                                                                               |
|-----------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0000 0000       | NOP                    | This transaction has no side-effects.                                                                                                                                                                                             |
| 0000 0001       | Shutdown               | This cycle is claimed by the MIOC. No corresponding cycle is delivered to the PCI bus. The MIOC asserts <b>INIT#</b> back to the agent for a minimum of 4 clocks.                                                                 |
| 0000 0010       | Flush                  | The MIOC claims this cycle and retires it.                                                                                                                                                                                        |
| 0000 0011       | Halt                   | This cycle is claimed by the MIOC, forwarded to the compatibility PCI bus as a Special Halt Cycle, and retired on the system bus after it is terminated on the PCI bus via a master abort mechanism.                              |
| 0000 0100       | Sync                   | The MIOC claims this cycle and retires it.                                                                                                                                                                                        |
| 0000 0101       | Flush Acknowledge      | The MIOC claims this cycle and retires it.                                                                                                                                                                                        |
| 0000 0110       | Stop Clock Acknowledge | This cycle is claimed by the MIOC and propagated to the PCI bus as a Special Stop Grant Cycle. It is completed on the system bus after it is terminated on the PCI bus via a master abort mechanism.                              |
| 0000 0111       | SMI Acknowledge        | The MIOC's <b>SMIACT#</b> signal will be asserted upon detecting an SMI Acknowledge cycle with <b>SMMEM#</b> asserted, and will remain asserted until detecting a subsequent SMI Acknowledge cycle with <b>SMMEM#</b> deasserted. |
| all others      | <i>Reserved</i>        |                                                                                                                                                                                                                                   |

## 7.1.7 System Management Mode Accesses

The Intel 450NX PCIsset uses an SMRAM configuration register to enable, define and control access to the SMM RAM space. The SMM RAM space defaults to location A000h, with a size of 64 KB, but may be relocated and grown in increments of 64 KB. A master enable (SMRAME) and three access-control enables (Open, Closed, Locked) determine how accesses to the space are to be serviced. Table 7-2 summarizes how accesses to the SMM RAM space are serviced.

**Table 7-2: SMRAM Space Cycles**

| SMRAME | D_OPEN | C_CODE | C_LCK | SMMEM | Code Fetch          | Data Reference      | Usage                                                                                                                                                                         |
|--------|--------|--------|-------|-------|---------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | X      | X      | X     | X     | Normal <sup>1</sup> | Normal <sup>1</sup> | SMM RAM space is not supported.                                                                                                                                               |
| 1      | 0      | 0      | X     | 0     | PCI 0a              | PCI 0a              | Normal SMM usage. Accesses to the SMM RAM space from processors in SMM will access the DRAM. Accesses by processors not in SMM will be diverted to the compatibility PCI bus. |
| 1      | 0      | 0      | X     | 1     | DRAM                | DRAM                |                                                                                                                                                                               |
| 1      | 0      | 1      | X     | 0     | PCI 0a              | PCI 0a              | A modification of the normal SMM usage, in which only code fetches are accepted from processors in SMM mode.                                                                  |
| 1      | 0      | 1      | X     | 1     | DRAM                | PCI 0a              |                                                                                                                                                                               |
| 1      | 1      | X      | 0     | X     | DRAM                | DRAM                | Full access by any agent to SMM RAM space. Typically used by the BIOS to initialize SMM RAM space.                                                                            |

1. SMRAM functions are disabled. The access is serviced like any other. The address is checked against the other space and gap definitions to determine its disposition -- to PCI, to memory, or to the system bus for a third party agent to claim.

## 7.1.8 Third-Party Intervention

The Intel 450NX PCIsset supports the same third-party control sideband controls that were defined in Intel 450GX PCIsset. These controls allow an external agent on the system bus to affect the way in which the MIOC responds to a system bus request to memory. This external agent is referred to as a “third-party” to the transaction. When a third-party agent intervenes in the normal transaction flow, both the MIOC and the third-party share responsibility for generating the appropriate response; however, the MIOC is always the “owner” of the transaction, and hence must be the responding bus agent.

The third-party controls how the MIOC responds by asserting a code on the sideband TPCTL[1:0] signals during the snoop phase. The MIOC samples these signals in the last cycle of the snoop phase. Table 7-3 indicates the actions possible using the TPCTL[1:0] signals.

Table 7-3: TPCTL[1:0] Operations

| TPCTL [1:0] | Action                                                                                                                                              |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 00          | <b>Accept.</b> The MIOC accepts the request, and provides the normal response. The third-party agent is not involved in the transaction.            |
| 01          | <b>Hard Fail.</b> Not supported by the Intel <sup>®</sup> 450NX PCIset.                                                                             |
| 10          | <b>Retry.</b> The MIOC will generate a retry response. The access will be retried by the requesting agent.                                          |
| 11          | <b>Defer.</b> The MIOC will issue a defer response, and the third-party agent will complete the transaction at a later time using a deferred reply. |

## 7.2 Outbound Transactions

### 7.2.1 Supported Outbound Accesses

The PXB translates valid system bus commands into PCI bus requests. For all Host-PCI transactions the PXB is a non-caching agent since the Intel 450NX PCIset does not support cacheability on PCI. However, the PXB must respond appropriately to the system bus commands that are cache oriented.

### 7.2.2 Outbound Locked Transactions

The Intel 450NX PCIset supports memory-mapped outbound locked operations. I/O-mapped outbound locked transactions are *not* supported. Further, a locked transaction cannot be initiated with a zero-length read. These restrictions are consistent with the transactions supported by the processor.

### 7.2.3 Outbound Write Combining

The Intel 450NX PCIset provides its own write combining for Host-PCI write transactions. If enabled, and multiple Host-PCI writes target sequential locations in the PCI space, the data is combined and sent to the PCI bus as a single write burst. *This holds true for all memory attributes, not just WC.* There is no corresponding write-combining for the Host-DRAM path.

### 7.2.4 Third-Party Intervention on Outbounds

The use of the third-party control signals (TPCTL) is not supported for outbound transactions (Host-PCI). Assertion of the TPCTL signals during an outbound transaction will have

indeterminate results. Assertion of DEFER# during an outbound transaction will also have indeterminate results.

## 7.3 Inbound Transactions

For all inbound transactions, the Intel® 450NX MIOC will use an Agent ID of **'1001b'** (9). This is the same agent ID used by the Intel 450GX PCIset, which the Intel 450NX PCIset replaces.

Note that memory-mapped accesses across PCI buses (i.e., peer-to-peer transfers) are not supported. Also, inbound I/O transactions are not supported, either to other PCI buses or to the system bus.

### 7.3.1 Inbound LOCKs

Inbound (PCI-to-system bus) LOCKs are not supported in the Intel 450NX PCIset. Use of inbound locks on the Intel 450NX PCIset may result in unanticipated behavior. The Intel 450NX PCIset is NOT compatible with devices on the compatibility PCI bus which are capable of initiating inbound bus- or resource-locks. Deadlock may occur between outbound locked transactions, south bridge-initiated Secure Sideband Requests (PHOLD#), and LOCK# assertion by the offending device. Devices capable of asserting LOCK# to access memory should not be used on the compatibility PCI bus.

### 7.3.2 South Bridge Accesses

The PXB's Bus 'a' has sideband signals to support the PIIX4E south bridge for ISA expansion. The PXB does not support an EISA bridge.

#### **WSC# Handshake**

When the PIIX4E south bridge issues an interrupt for an ISA master, it must first check that any writes posted from ISA to memory have been observed before the interrupt is issued. This action is necessary to guarantee that an ISA write followed by an ISA interrupt is observed in that same order by a processor on the system bus.

Whenever the compatibility bus PXB receives a write from the south bridge, it will deassert the WSC# (Write Snoop complete) signal. WSC# will remain de-asserted until the write Completion for that write has returned. When the Completion returns, WSC# is again asserted. While WSC# is de-asserted the PXB must retry any additional writes from the south bridge.

The PXB will only support the WSC# Handshake when the internal arbiter is used. When operating in external arbiter mode, the PXB will always hold WSC# asserted. The WSC# mode may be disabled by a bit in the PXB's CONFIG register. If disabled, WSC# stays asserted and inbound writes from the south bridge are accepted.

**Distributed DMA**

Distributed DMA across the PCI bus is not supported by the Intel 450NX PCIset. This function is incompatible with the passive release mechanism portion of the PHOLD#/PHLDA# protocol used to grant PCI bus access to south bridges.

**Accesses Prohibited to Third-Party Agent**

The Intel 450NX PCIset only supports inbound south bridge accesses to memory. Inbound accesses from a south bridge using the PHOLD#/PHLDA# protocol, directed to a third-party agent on the system bus, are not supported. Such accesses, involving interactions with unknown and unpredictable agents, could violate the rules governing the PHOLD#/PHLDA# protocol, potentially leading to deadlocks.

## 7.4 Configuration Accesses

The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The Intel<sup>®</sup> 450NX PCIset supports only Mechanism #1.

Mechanism #1 defines two I/O-space locations: an address register (CONFIG\_ADDRESS) at location **0CF8h**, and a data register (CONFIG\_DATA) at location **0CFCh**. The Intel 450NX PCIset provides a PCI-compatible configuration space for the MIOC, and one for each PCI bus in the PXB.

- If the MIOC detects the I/O request is a configuration access to its own configuration space, it will service that request entirely within the MIOC. Reads result in data being returned to the system bus.
- If the MIOC detects the I/O request is a configuration access to a PXB configuration space, it will forward the request to the appropriate PXB for servicing. The request is not forwarded to a PCI bus. Reads will result in data being returned by the PXB through the MIOC to the system bus.
- If the MIOC detects the I/O request is a configuration access to a third-party agent on the system bus, it will leave the access unclaimed on the system bus. The third-party agent may claim the access, with reads resulting in data being returned by the third-party agent to the system bus.
- Otherwise, the access is forwarded on to the PXB to be placed on the PCI bus as a Configuration Read or Configuration Write cycle. Reads will result in data being returned through the PXB and MIOC back to the system bus, just as in normal Outbound Read operations.

## 8.1 PCI Arbitration Scheme

The PCI Specification Rev 2.1 requires that the arbiter implement a fairness algorithm to avoid deadlocks and that it assert only a single GNT# signal on any rising clock. The arbitration algorithm is fundamentally not part of the PCI Specification.

The PXB contains an internal PCI arbiter. This arbiter can be disabled either when the PXB operates with I/O bridges which include this function, or when a customized PCI arbiter solution is required. The Internal PCI Arbiter has the following features:

- Support for 6 PCI masters, Host and I/O Bridge
- 2 Level Round Robin
- Bus Lock Implementation
- Bus Parking on last agent using the bus
- 4-PCI clock grant (FRAME#) time-out
- Multi Transaction Timer (MTT) mechanism
- PCI arbitration is independent from the system bus arbitration
- PIIX4E-compatible protocol (EISA bridges are *not* supported)
- PCI Protocol Requirements

## 8.2 Host Arbitration Scheme

The system bus arbitration protocol supports two classes of bus agents: symmetric agents and priority agents. The processors arbitrate for the system bus as symmetric agents using their own signaling. Symmetric agents implement fair, distributed arbitration using a round-robin algorithm. The MIOC, as an I/O agent, uses a priority agent arbitration protocol to obtain the ownership of the system bus. Priority agents use the BPRI# signal to immediately obtain bus ownership.

Besides two classes of arbitration agents (symmetric and priority agents), each bus agent has two mechanisms available that act as arbitration modifiers: the bus lock (LOCK#) and the request stall (BNR#).

### 8.2.1 Third Party Arbitration

The Intel 450NX PCIset requests the system bus with BPRI#. If multiple bridges or a third party agent is on the system bus, an arbitration method is required to establish bus ownership among multiple requesting bridges (which bridge can drive BPRI#). This arbitration is transparent to the Pentium® II Xeon™ processors or other symmetric bus agents. Only one bridge is allowed to drive BPRI# at a time.

## 8.3 South Bridge Support

The Intel® 450NX PCIset is designed to work with the PIIX4E south bridge which connects the PCI bus to ISA bus and I/O APIC components. Note that the protocols described here apply only when the Intel 450NX PCIset is used in internal arbiter mode — use of the PIIX4E in external arbiter configurations is not supported.

The Intel 450NX PCIset does *not* guarantee ISA access latencies of < 2.5 usec. ISA devices which require these latencies to be met (GAT mode timing) are not supported.

### 8.3.1 I/O Bridge Configuration Example.

The basic I/O bridge configuration supported by the Intel 450NX PCIset is shown in Figure 8-1. The figure shows the sideband signals that connect the PXB to the PIIX4E, I/O APIC components and the external arbiter. Note that PHOLD#/PHLDA# are connected between PXB and the PIIX4E, and WSC# output from PXB is connected to the APICACK2# input of the stand-alone I/O APIC component. If the configuration does not have I/O APIC component, then WSC# pin is left unconnected.

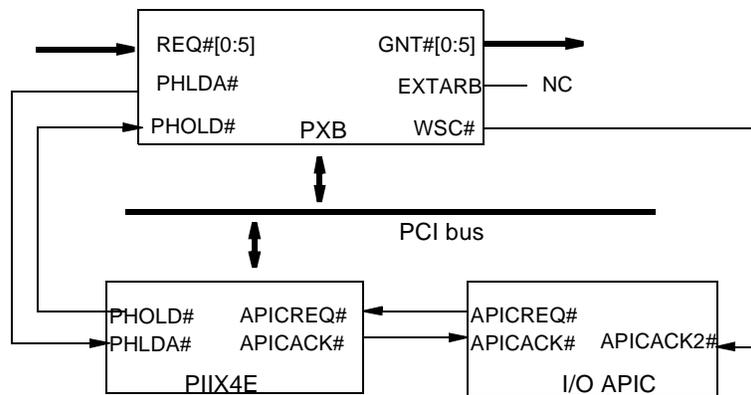


Figure 8-1: ISA Bridge with the I/O APIC (Internal Arbiter)

### 8.3.2 PHOLD#/PHLDA# Protocol

The PIIX4E uses only two signals to obtain the ownership of the PCI bus. The PIIX4E will assert PHOLD# to indicate that an ISA master is requesting to run a cycle (*DREQ* active) or an integrated PCI-IDE bus-mastering device is requesting the PCI bus.

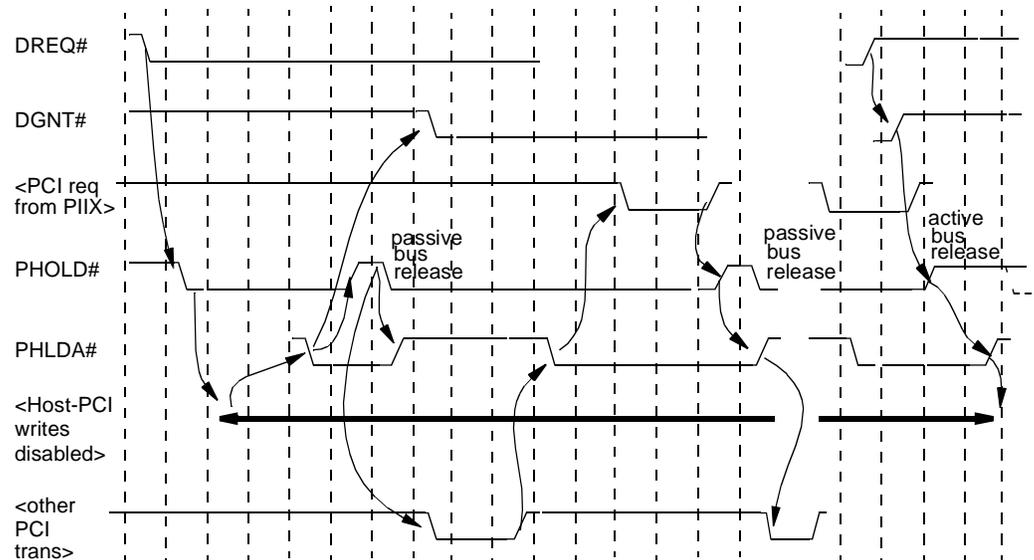


Figure 8-2: PHOLD#/PHLDA# Protocol Showing Active and Passive Bus Release

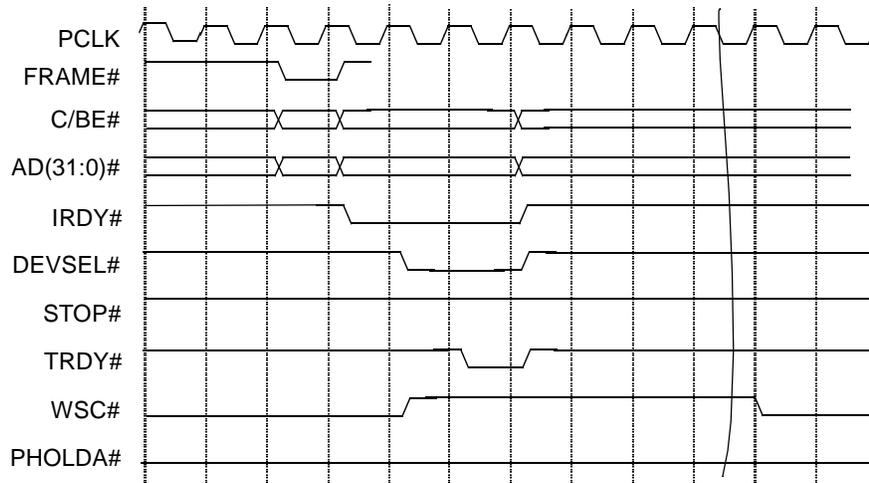
### 8.3.3 WSC# Protocol

The WSC# (Write Snoop Complete) is a status signal output from the Intel 450NX PCIset PXB. The WSC# assertion indicates that all necessary snoops for a previously posted PCI-DRAM write have been completed on the system bus.

The WSC# signal is primarily used by the I/O APIC device connected to the ISA bridge. The I/O APIC uses this signal to maintain data coherency and ordering of transactions in the system.

#### NOTE

The WSC# Handshake only applies if the PXB is in internal arbiter mode.



**Figure 8-3: WSC# Signal Functionality**

This chapter describes the data integrity support and general error detection and reporting mechanisms used in the Intel® 450NX PCIset.

## 9.1 DRAM Integrity

Both the system data bus and the Intel® 450NX PCIset's memory subsystem use a common Error Correcting Code which provides SEC/DED/NED coverage. The ECC used is capable of correcting single-bit errors and detecting 100% of double-bit errors over one code word.

### 9.1.1 ECC Generation

When enabled, the DRAM ECC mechanism allows automatic generation of an 8-bit protection code for the 64-bit (Qword) of data during DRAM write operations. Note that when ECC is intended to be enabled, the whole DRAM array *must* be first initialized by doing writes before the DRAM read operations can be performed. This will establish the correlation between 64-bit data and associated 8-bit ECC code which does not exist after power-on. This function is *not* provided by hardware.

### 9.1.2 ECC Checking and Correction

During DRAM read operations, a full Qword of data (8 bytes) is always transferred from the DRAM to the MIOC regardless of the size of the originally requested data. Both 64-bit data and 8-bit ECC code are transferred simultaneously from the DRAM to the MIOC. The ECC checking logic in the MIOC uses the received 72 bit Data + ECC to generate the check syndrome. If a single-bit error is detected the ECC logic corrects the identified incorrect data bit.

### 9.1.3 ECC Error Reporting

When ECC checking is enabled, single-bit and multiple-bit errors detected by the ECC logic are logged in the MIOC. The first two errors detected on reads-from-memory are logged, as are the first two errors detected on data received from the system bus.

For memory errors, the error type (single-bit or multi-bit), syndrome, chunk and effective address are logged. The first two memory errors (single-bit or multi-bit) will be logged in the

MEL and MEA registers. For bus errors, the error type, syndrome and chunk are logged. The first two system bus errors (single-bit or multi-bit) will be logged in the HEL registers.

All ECC error logging registers are sticky through reset, allowing software to determine the source of an error after restoring the system to functioning mode. The logging registers hold their values until explicitly cleared by software.

### **Error Signaling Mechanism**

Single-bit correctable errors are not critical from the point-of-view of presenting the correct value of data to the system. The DRAM (if the cause of error is a DRAM array) will still contain faulty data which will cause the repetition of error detection and recovery for the subsequent accesses to the same location.

Multi-bit uncorrectable errors are fatal system errors and will cause the MIOC to assert the BERR# signal if enabled in the ERRCMD register. The uncorrected data is forwarded to its destination. For the first two multi-bit uncorrectable errors, the MIOC will log in the MEA register the row number where the error occurred. This information can be used later to point to a faulty DRAM DIMM.

The MEA/MEL registers log only the first two errors. After the first two errors have been logged, the MEA/MEL registers will not be updated. However, normal error detection still continues, the ERR[1:0]# and BERR# signals are still asserted as appropriate, and scrubbing of the memory still continues.

## **9.1.4 Memory Scrubbing**

The Intel 450NX PCIset provides a “scrub-on-error” (demand scrubbing) mechanism, wherein corrected data for single-bit errors will be automatically written back into the memory subsystem by the MIOC. Note that this is not the same as “walk-through” scrubbing, in which every memory location is systematically accessed, checked and corrected on a regular basis. The scrub-on-error mechanism will scrub only those locations accessed during normal operation and thus complements the software controlled “walk-through” scrubbing.

## **9.1.5 Debug/Diagnostic Support**

The MIOC supports in-system testing of ECC functions. An ECC Mask Register (ECCMSK) can be programmed with a masking function. Subsequent writes into memory will store a masked version of the computed ECC. Subsequent reads of the memory locations written while masked will return an invalid ECC code. If the mask register is left at 0h (the default), the normal computed ECC is written to memory.

## **9.2 System Bus Integrity**

A variety of system bus error detection features are provided by the MIOC. Particularly, the system data bus is checked for ECC errors on Host-DRAM and Host-PCI writes.

Additionally, the MIOC supports parity checking on the system address and request/response signals.

### 9.2.1 System Bus Control & Data Integrity

The MIOC detects errors on the system data bus by checking the ECC provided with data and the parity flag provided with control signals. In turn, the MIOC will generate new ECC with data and parity with control signals so that bus errors can be detected by receiving clients.

The request control signals ADS# and REQ#[4:0] are covered with the Request Parity signal RP#, which is computed as even parity. This ensures that it is deasserted when all covered signals are deasserted.

The address signals A#[35:3] are covered by the Address Parity signal AP#[1:0], which is also configured for even parity. This ensures that each is deasserted when all covered signals are deasserted. AP#[1] covers A#[35:24] and AP#[0] covers A#[23:3].

Response signals RS#[2:0] are protected by RSP#. RSP# is computed as even parity. This ensures that it is deasserted when all covered signals are deasserted.

## 9.3 PCI Integrity

The PCI bus provides a single even-parity bit (PAR) that covers the AD[31:0] and C/BE#[3:0] lines. The agent that drives the AD[31:0] lines is responsible for driving PAR. Any undefined signals must still be driven to a valid logic level and included in the parity calculation.

Parity generation is not optional on the PCI bus; however, parity error detection and reporting is optional. The PXB will always detect an address parity error, even if it is not the selected target. The PXB will detect data parity errors if it is either the master or the target of a transaction, and will optionally report them to the system.

Address parity errors are reported using the SERR# signal. Data parity errors are reported using the PERR# signal. The ERRCMD (Error Command) register provides the capability to configure the PXB to propagate PERR# signaled error conditions onto the SERR# signal.

## 9.4 Expander Bus

Each Expander bus has a parity bit covering all data and control signals for each clock cycle. Parity is generated at the expander bus interface by the sender, and checked at the expander bus interface in the receiver. Detected parity errors are reported at the receiving component — outbound packets report parity errors in the PXB, while inbound packets report parity errors in the MIOC.



## 10.1 Post Reset Initialization

### 10.1.1 Reset Configuration Using CVDR/CVCR

All system bus devices must sample the following configuration options at reset:

- Address/request/response parity checking: Enabled or Disabled
- AERR# detection enable
- BERR# detection enable
- BINIT# detection enable
- FRC mode: Enabled or Disabled
- Power-on reset vector: 1M or 4G
- In-Order Queue depth: 1 or 8
- APIC cluster ID: 0, 1, 2, or 3
- Symmetric agent arbitration ID: 0, 1, 2, 3

The MIOC provides both the Symmetric Arbitration ID parameter and other parameters. (Refer to the CVDR register description.)

#### 10.1.1.1 Configuration Protocol

A Pentium® II Xeon™ processor-based system is initialized and configured in the following manner.

1. The system is powered. The power-supply provides resets for the Intel® 450NX PCIset through the PWRGD signal. The MIOC and PXBs assert their resets while the PWRGD signal is not asserted. PCI reset is driven to tristate the PCI buses in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances.
2. All Intel 450NX PCIset components are initialized, with their internal registers defaulting to the power-on values.
3. The MIOC will drive the appropriate system bus data lines with the initial configuration values that defaulted in the *Configuration Values Driven on Reset* (CVDR) register.
4. On the rising edge of RESET#, the MIOC will continue driving the appropriate system bus lines with the configuration values. These values are driven at least one clock after the rising edge of RESET#.

5. All system bus devices will capture the system configuration parameters from the appropriate system bus lines on the rising edge of RESET#. The MIOC captures these values in its *Configuration Values Captured on Reset (CVCR)* register. (This allows an external device to over-ride the MIOC default parameters.)
6. All system bus devices are now ready for further programming. The MIOC will respond to BIOS code fetches.
7. If a change in the system bus system configuration is desired, the MIOC's CVDR register can be programmed with the desired values.
8. After the CVDR register is programmed, the MIOC must be programmed to do a hard reset, through the Reset Control (RC) register.
9. When the MIOC performs a hard reset, all system bus devices are again reset. This reset repeats steps 2-8, except that the CVDR register is not effected by the reset. This register is only re-initialized by the PWRGD signal.

### 10.1.1.2 Special Considerations for Third-Party Agents

One of the settings available in the CVDR/CVCR registers allows the Bus In-Order Queue Depth to be set to 1, instead of the usual 8. When IOQ Depth=1, there is a case where a Third-Party Agent can starve the system bus.

Therefore, any system containing a TPA must either:

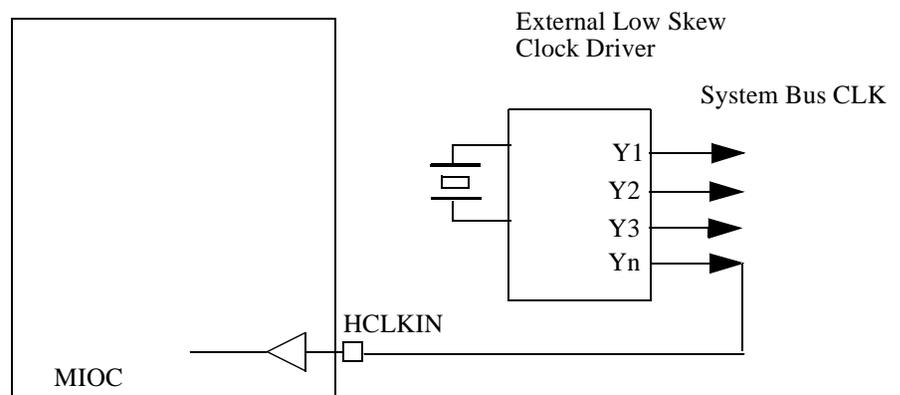
- require that the TPA back-off its BPRI# arbitration requests sufficiently to allow the symmetric agents access to the bus, *or*
- not use IOQ depth=1.

This chapter describes the generation, distribution and interaction between the various clocks in an Intel® 450NX PCIsset-based system, as well as the various reset functionality supported by the Intel 450NX PCIsset.

## 11.1 Clocking

The Pentium® II Xeon™ processor uses a clock ratio scheme where the system bus clock frequency is multiplied to produce the processor's core frequency. The MIOC supports a system bus frequency optimized for 100 MHz. The Intel® 450NX PCIsset should be used at a bus frequency which provides the required clock frequency for the PCI interfaces. The external clock generator is responsible for generating the system clock. The Intel 450NX PCIsset's core clock is equal to the system bus clock rate. The Intel 450NX PCIsset is responsible for driving the signals which the processor uses to determine the core to bus clock ratio.

The MIOC receives an output of a clock generator on the HCLKIN pin, as illustrated in Figure 11-1. The MIOC uses the HCLKIN signal to drive the host and memory interfaces and the core. This clock is doubled for the MD bus and the Expander buses.



**Figure 11-1: Host Clock Generation and Distribution**

PCI clock distribution is illustrated in Figure 11-2. The PXB provides a PCI bus clock that is generated by dividing the internal host clock frequency by three. The PCI clock is output through the PCLK pin. Externally this PCI clock drives a low skew clock driver which in turn supplies multiple copies of the PCI clock to the PCI bus. One of the outputs of the external clock driver is fed back into the PXB. A PLL in the PXB forces the external PCI clock to phase lock to the internal PCI clock tree.

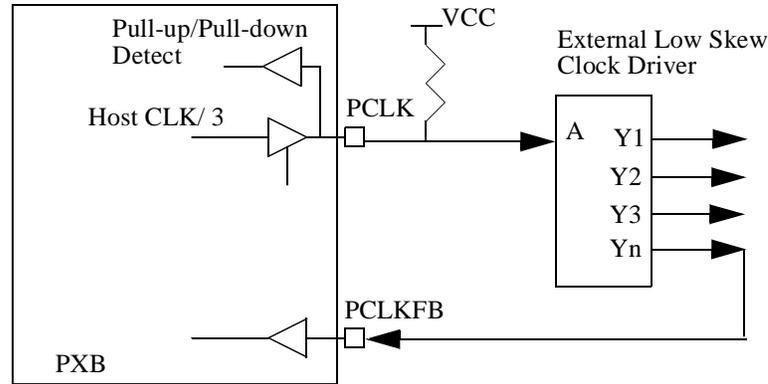


Figure 11-2: PCI Clock Generation and Distribution

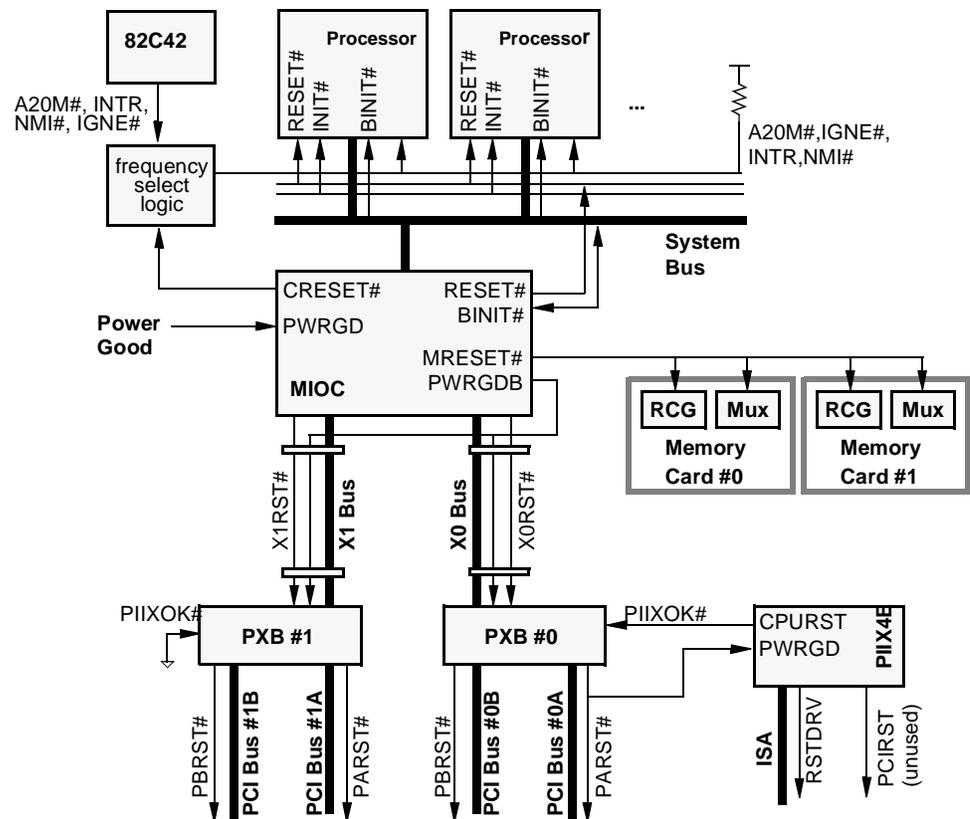
## 11.2 System Reset

Five varieties of reset functions are supported by the Intel® 450NX PCIset.

- A *Power-Good Reset* is triggered by an externally generated signal which indicates that the power supplies and clocks are stable. This reset clears all configuration and transaction state in the Intel 450NX PCIset, as well as asserting resets to the processors, PCI buses, and PIIX, if present.
- A *System Hard Reset* is a software-initiated reset that performs nearly the same functions as the power-good reset. The key difference is that the system hard reset does not clear "sticky" error flags in the Intel 450NX PCIset, thus allowing an error handler to determine the cause of a failure that resulted in reset. Also, hard reset may optionally trigger the processor's Built-In Self-Test (BIST).
- A *Soft Reset* is another software-initiated reset which affects only the processors. This reset may also be generated by certain I/O activities.
- A *BINIT Reset* results from a catastrophic transaction error on the system bus. The memory and the MIOC's configuration space are untouched.
- A *PXB Reset* is a software-initiated reset that affects only a single PXB and its dependent PCI buses. This reset may be used in high-availability systems, where it is desirable to allow the processors and one PXB to continue operation in the event of failure of a single PXB.

### 11.2.1 Intel® 450NX PCIset Reset Structure

Figure 11-3 shows the recommended reset structure for an Intel 450NX PCIset-based system including the PIIX4E south bridge. Note that the primary system power-good signal is provided to the MIOC, which then distributes a variety of reset signals to the rest of the system.



**Figure 11-3: Recommended RESET Distribution for Intel® 450NX PCIsset-Based Systems Including a PIIX4E South Bridge**

### Power Good

The reference system shown here assumes a single "power good" signal that indicates clean power supplies and clocks to the MIOC and both PXBs. For routing convenience and drive capability, the MIOC provides a buffered version of its PWRGD input (PWRGDB), which should be connected to the PWRGD inputs of each PXB. Refer to the Electrical Characteristics for additional PWRGD requirements.

### RESET#

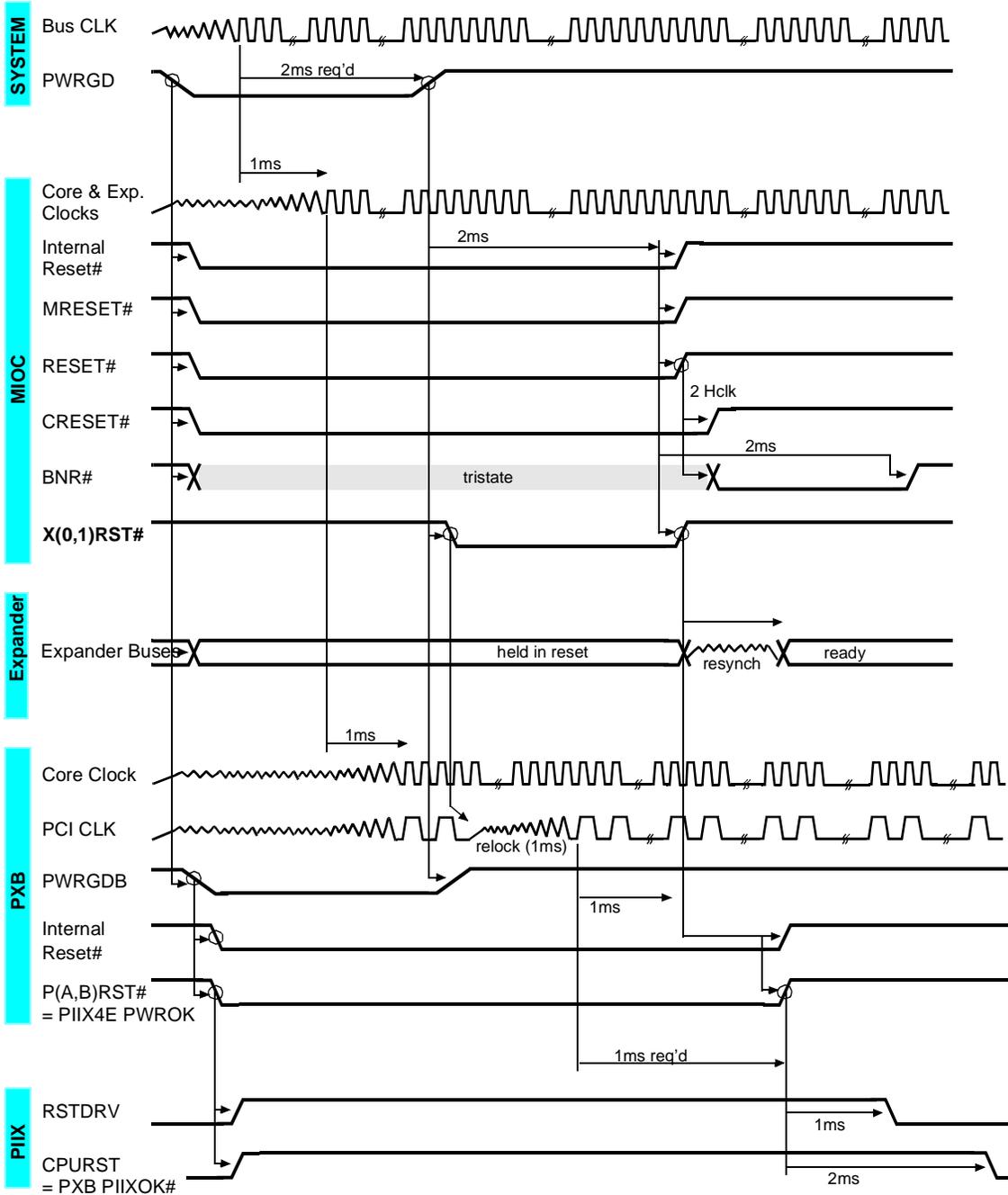
The RESET# signal is directed to the processors. Assertion of this signal puts all processors in a known state, and invalidates their L1 and L2 caches. When this signal is deasserted, the processor begins to execute from address 00\_FFFF\_FFF0h. The Boot ROM must respond to this address range regardless of where it physically resides in the system.

### CRESET#

The CRESET# signal tracks RESET#, but is held asserted two clocks longer than RESET#. It is provided to allow an external frequency selection mux to drive the system-bus-to-core-clock ratio onto pins LINT[1:0], IGNNE#, and A20M# of the system bus during RESET#.

**MRESET#**

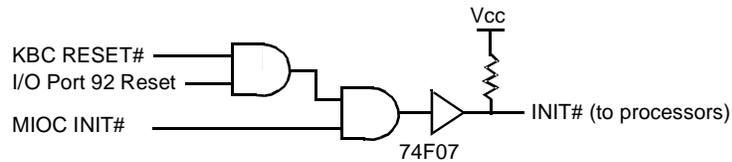
The MRESET# signal is sent to all RCGs and MUXs in the memory subsystem. When asserted, each RCG and MUX clears their transaction state and data buffers. Any transactions that may have been in-progress or pending in the memory subsystem are lost. Upon MRESET# deassertion, the MIOC will re-initialize the memory subsystem by issuing 8 CAS-before-RAS refreshes per bank (this does not affect the data held in the memory).



**Figure 11-4: Power-Good Reset**

### Soft Reset

A *Soft Reset* is a reset directed to the processors on the system bus which does not affect the configuration or transaction state of the Intel 450NX PCIset or the dependent PCI buses. To support this function, the system design must externally combine the MIOC's INIT# output with the I/O port 92h and keyboard controller soft reset sources as shown in Figure 11-5.



**Figure 11-5: Soft Reset**

### PXB Reset

A *PXB Reset* is a software-initiated reset that affects only a single PXB and its dependent PCI buses. Figure 11-4 illustrates a software-initiated PXB Reset.

#### Reset Without Disturbing PCI Clocks

PCICLK<sub>A</sub> and PCICLK<sub>B</sub> must be re-phased whenever any type of reset is asserted if the Intel 450NX PCIset is to be deterministic relative to that reset. The behavior of these clocks cannot be guaranteed during this re-phasing. A bit in the PXB RC register can be cleared by a configuration write to defeat the PCI clock re-phasing, so that PCICLK<sub>A</sub> and PCICLK<sub>B</sub> remain well behaved through resets.

## 11.2.2 Output States During Reset

The following tables shows the signal states of the Intel 450NX PCIset components during a Power-Good Reset or System Hard Reset. Inputs are denoted by “-”.

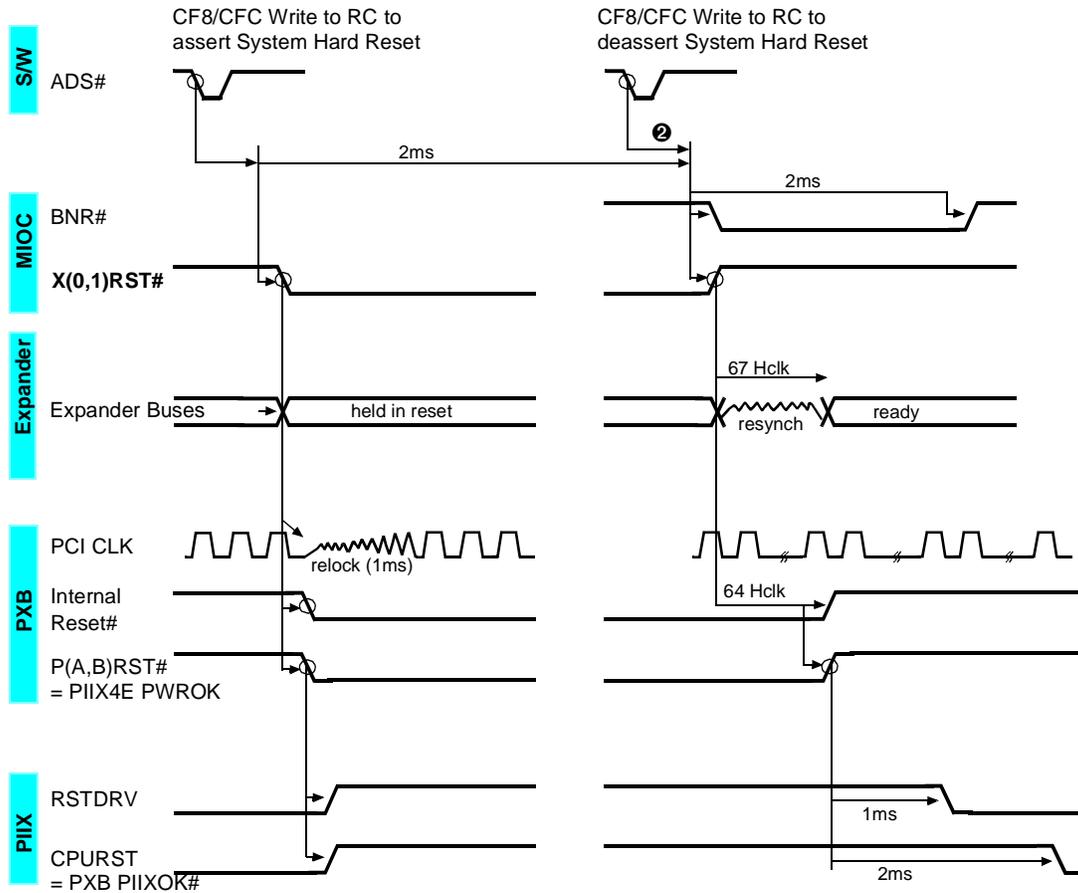


Figure 11-6: Software-Initiated PXB Reset

11.2.2.1 MIOC Reset State

| Host Interface |                       |           |                       |
|----------------|-----------------------|-----------|-----------------------|
| A[35:3]#       | Tristate <sup>1</sup> | DEP[7:0]# | Tristate              |
| ADS#           | Tristate              | DRDY#     | Tristate              |
| AERR#          | Tristate              | HIT#      | -                     |
| AP[1:0]#       | Tristate              | HITM#     | -                     |
| BERR#          | Tristate              | INIT#     | Tristate <sup>3</sup> |
| BINIT#         | Tristate              | LOCK#     | -                     |
| BNR#           | Tristate              | REQ[4:0]# | Tristate              |
| BP[1:0]#       | Tristate              | RP#       | Tristate              |
| BPRI#          | Tristate              | RS[2:0]#  | Tristate              |
| BREQ[0]#       | Asserted <sup>2</sup> | RSP#      | Tristate              |
| D[63:0]#       | Tristate              | TRDY#     | Tristate              |
| DBSY#          | Tristate              |           |                       |
| DEFER#         | Tristate              |           |                       |

| <b>Third-Party Agent Interface</b>            |            |              |                          |
|-----------------------------------------------|------------|--------------|--------------------------|
| IOGNT#                                        | -          | TPCTL[1:0]   | -                        |
| IOREQ#                                        | Tristate   |              |                          |
| <b>Memory Subsystem / External Interface</b>  |            |              |                          |
| BANK[2:0]#                                    | Deasserted | DVALID(a,b)# | Deasserted               |
| CARD[1:0]#                                    | Deasserted | MA[13:0]#    | Deasserted               |
| CMND[1:0]#                                    | Deasserted | MD[71:0]#    | Tristate                 |
| CSTB#                                         | Deasserted | MRESET#      | Asserted                 |
| DCMPLT(a,b)#                                  | Tristate   | PHIT(a,b)#   | -                        |
| DOFF[1:0]#                                    | Deasserted | ROW#         | Deasserted               |
| DSEL[1:0]#                                    | Deasserted | RCMPLT(a,b)# | -                        |
| DSTBN[3:0]#                                   | Tristate   | RHIT(a,b)#   | -                        |
| DSTBP[3:0]#                                   | Tristate   | WDEVT#       | Deasserted               |
| <b>Expander Interface (two per MIOC: 0,1)</b> |            |              |                          |
| X(0,1)ADS#                                    | Tristate   | X(0,1)HSTBP# | Toggling                 |
| X(0,1)BE[1:0]#                                | Tristate   | X(0,1)PAR#   | Tristate                 |
| X(0,1)BLK#                                    | Deasserted | X(0,1)RST#   | Asserted                 |
| X(0,1)CLK                                     | Toggling   | X(0,1)RSTB#  | Asserted                 |
| X(0,1)CLKB                                    | Toggling   | X(0,1)RSTFB# | -                        |
| X(0,1)CLKFB                                   | -          | X(0,1)XRTS#  | -                        |
| X(0,1)D[15:0]#                                | Tristate   | X(0,1)XSTBN# | -                        |
| X(0,1)HRTS#                                   | Toggling   | X(0,1)XSTBP# | -                        |
| X(0,1)HSTBN#                                  | Toggling   |              |                          |
| <b>Common Support Signals</b>                 |            |              |                          |
| CRES[1:0]                                     | Strapped   | TMS          | -                        |
| TCK                                           | -          | TRST#        | -                        |
| TDI                                           | -          | VCCA (3)     | Reference                |
| TDO                                           | OD         | VREF (6)     | Reference                |
| <b>Component-Specific Support Signals</b>     |            |              |                          |
| CRESET#                                       | Asserted   | PWRGD        | - <sup>4</sup>           |
| ERR[1:0]#                                     | Tristate   | PWRGDB       | De/asserted <sup>4</sup> |
| HCLKIN                                        | Toggling   | RESET#       | Asserted                 |
| INTREQ#                                       | Deasserted | SMIACT#      | Deasserted               |

**Notes:**

1. The Pentium® II Xeon™ processor allows for configuring a variety of processor and bus variables during the reset sequence. During RESET# assertion, and for one clock past the trailing edge of RESET#, the Intel 450NX PCIset MIOC will drive the contents of its CVDR register onto A[15:3]#. All system bus devices (including the MIOC) are required to sample these address lines using the trailing edge of reset, and modify their internal configuration accordingly. Note the initial value of CVDR may be changed by the boot processor, and the reset process re-engaged. This allows the processors and buses to power-up in a "safe" state, yet allow re-configuration based on specific system constraints.
2. BREQ0# must stay asserted (low) for a minimum of 2 system clocks after the rising edge of RESET#. The MIOC then releases (tristates) the BREQ0# signal.
3. INIT# is not asserted during power-up. It may be optionally asserted during system hard reset through the RC register to cause the processors to initiate BIST.
4. The PWRGDB output is asserted if the PWRGD input is asserted (i.e., a power-good reset). For a system hard reset, the PWRGDB output is deasserted.

## 11.2.2.2 PXB Reset State

| <b>PCI Bus Interface (2 per PXB: A,B)</b>                   |            |                 |              |
|-------------------------------------------------------------|------------|-----------------|--------------|
| P(A,B)AD[31:0]                                              | Tristate   | P(A,B)PAR       | Tristate     |
| P(A,B)C/BE[3:0]#                                            | Tristate   | P(A,B)PERR#     | Tristate     |
| P(A,B)CLKFB                                                 | -          | P(A,B)REQ[5:0]# | - (see note) |
| P(A,B)CLK                                                   | Toggling   | P(A,B)RST#      | Asserted     |
| P(A,B)DEVSEL#                                               | Tristate   | P(A,B)SERR#     | Open         |
| P(A,B)FRAME#                                                | Tristate   | P(A,B)STOP#     | Tristate     |
| P(A,B)GNT[5:0]#                                             | Tristate   | P(A,B)TRDY#     | Tristate     |
| P(A,B)IRDY#                                                 | Tristate   | P(A,B)XARB#     | Strapped     |
| P(A,B)LOCK#                                                 | Tristate   |                 |              |
| <b>PCI Bus Interface / Non-Duplicated (one set per PXB)</b> |            |                 |              |
| ACK64#                                                      | Tristate   | PHLDA#          | Tristate     |
| MODE64#                                                     | Strapped   | REQ64#          | Asserted     |
| PHOLD#                                                      | -          | WSC#            | Tristate     |
| <b>Expander Interface (one per PXB)</b>                     |            |                 |              |
| XADS#                                                       | Tristate   | XHSTBP#         | -            |
| XBE[1:0]#                                                   | Tristate   | XIB             | Deasserted   |
| XBLK#                                                       | -          | XPAR#           | Tristate     |
| XCLK                                                        | Toggling   | XRST#           | Asserted     |
| XD[15:0]#                                                   | Tristate   | XXRTS#          | Deasserted   |
| XHRTS#                                                      | -          | XXSTBN#         | Deasserted   |
| XHSTBN#                                                     | -          | XXSTBP#         | Deasserted   |
| <b>Common Support Signals</b>                               |            |                 |              |
| CRES[1:0]                                                   | Strapped   | TMS             | -            |
| TCK                                                         | -          | TRST#           | -            |
| TDI                                                         | -          | VCCA (3)        | Reference    |
| TDO                                                         | OD         | VREF (2)        | Reference    |
| <b>Component-Specific Support Signals</b>                   |            |                 |              |
| INTRQ(A,B)#                                                 | Deasserted | PIIXOK#         | -            |
| LONGXB#                                                     | Strapped   | PWRGD           | -            |
| P(A,B)MON[1:0]#                                             | Tristate   |                 |              |

Note:

The P(A,B)REQ[5:0]# signals are inputs to the PXB. During reset, these inputs are ignored. However, these signals become "live" immediately following reset deassertion. All unconnected REQ# inputs should be strapped deasserted. All connected REQ# inputs should have weak pullups.

## 11.2.2.3 RCG Reset State

| Memory Subsystem / External Interface |            |                             |            |
|---------------------------------------|------------|-----------------------------|------------|
| BANK[2:0]#                            | -          | MRESET#                     | -          |
| CARD#                                 | -          | PHIT#                       | Deasserted |
| CMND[1:0]#                            | -          | RCMPLT#                     | Deasserted |
| CSTB#                                 | -          | RHIT#                       | Deasserted |
| GRCMPLT#                              | Deasserted | ROW#                        | -          |
| MA[13:0]#                             | -          |                             |            |
| Memory Subsystem / Internal Interface |            |                             |            |
| ADDR(A,B,C,D)[13:0]                   | Deasserted | LRD#                        | Deasserted |
| AVWP#                                 | Deasserted | RAS(A,B,C,D)(a,b,c,d)[1:0]# | Deasserted |
| CAS(A,B,C,D)(a,b,c,d)[1:0]#           | Deasserted | WDME#                       | Deasserted |
| LDSTB#                                | Deasserted | WE(A,B,C,D)(a,b)#           | Deasserted |
| Common Support Signals                |            |                             |            |
| CRES[1:0]                             | -          | TMS                         | -          |
| TCK                                   | -          | TRST#                       | -          |
| TDI                                   | -          | VCCA                        | Reference  |
| TDO                                   | Tristate   | VREF (2)                    | Reference  |
| Component-Specific Support Signals    |            |                             |            |
| BANKID#                               | Strapped   | DR50T#                      | Strapped   |
| DR50H#                                | Strapped   | HCLKIN                      | Toggling   |

## 11.2.2.4 MUX Reset State

| Memory Subsystem / External Interface |            |           |            |
|---------------------------------------|------------|-----------|------------|
| DCMPLT#                               | Deasserted | DVALID#   | -          |
| DOFF[1:0]#                            | -          | GDCMPLT#  | Deasserted |
| DSEL#                                 | -          | MD[35:0]# | Tristate   |
| DSTBP[1:0]#                           | Tristate   | MRESET#   | -          |
| DSTBN[1:0]#                           | Tristate   | WDEVT#    | -          |
| Memory Subsystem / Internal Interface |            |           |            |
| AVWP#                                 | -          | Q1D[35:0] | Tristate   |
| LDSTB#                                | -          | Q2D[35:0] | Tristate   |
| LRD#                                  | -          | Q3D[35:0] | Tristate   |
| Q0D[35:0]                             | Tristate   | WDME#     | -          |
| Common Support Signals                |            |           |            |
| CRES[1:0]                             | Strapped   | TMS       | -          |
| TCK                                   | -          | TRST#     | -          |
| TDI                                   | -          | VCCA      | Reference  |
| TDO                                   | Tristate   | VREF (2)  | Reference  |
| Component-Specific Support Signals    |            |           |            |
| HCLKIN                                | Toggling   |           |            |



## 12.1 Signal Specifications

### 12.1.1 Unused Pins

For reliable operation, always connect unused inputs to an appropriate signal level. Unused AGTL+ inputs should be connected to  $V_{TT}$ . Unused active low 3.3 V-tolerant inputs should be connected to 3.3 V. Unused active high inputs should be connected to ground ( $V_{SS}$ ). When tying bidirectional signals to power or ground, a resistor must be used. When tying *any* signal to power or ground, a resistor will also allow for fully testing the processor and PCIset after board assembly. It is suggested that  $\sim 10K\Omega$  resistors be used for pull-ups and  $\sim 1K\Omega$  resistors be used as pull-downs.

### 12.1.2 Signal Groups

In order to simplify the following discussion, signals have been combined into groups of like characteristics (see below). Refer to Chapter 2 for a description of the signals and their functions.

**Table 12-1: Signal Groups MIOC**

| Pin Group                                           | Signals                                                                                                                                                                                                                                                          | Notes |
|-----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| AGTL+ Input                                         | LOCK#, PHIT(a,b)#, RCMPLT(a,b)#, RHIT(a,b)#, X(0,1)RSTFB#, X(0,1)XRTS#, X(0,1)XSTBN#, X(0,1)XSTBP#, HIT#, HITM#                                                                                                                                                  |       |
| AGTL+ Output                                        | BR[0]#, BANK[2:0]#, BREQ[0]#, CARD[1:0]#, CMND[1:0]#, CSTB#, DOFF[1:0]#, DSEL[1:0]#, DVALID(a,b)#, MA[13:0]#, MRESET#, ROW#, X(0,1)BLK#, X(0,1)HRTS#, X(0,1)HSTBN#, X(0,1)HSTBP#, X(0,1)RST#, X(0,1)RSTB#, WDEVT#                                                |       |
| AGTL+ I/O                                           | A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BPRI#, D[63:0]#, DBSY#, DCMPLT(a,b)#, DEFER#, DEP[7:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, MD[71:0]#, REQ[4:0]#, RESET#, RP#, RS[2:0]#, RSP#, TRDY#, X(0,1)ADS#, X(0,1)BE[1:0]#, X(0,1)D[15:0]#, X(0,1)PAR# |       |
| CMOS 14 mA 2.5 V Open Drain Output (3.3 V Tolerant) | INIT#, TDO                                                                                                                                                                                                                                                       |       |
| CMOS Input 3.3 V                                    | IOGNT#, TPCTL[1:0], PWRGD,                                                                                                                                                                                                                                       |       |

**Table 12-1: Signal Groups MIOC (Continued)**

|                                                        |                                                                  |   |
|--------------------------------------------------------|------------------------------------------------------------------|---|
| CMOS Input 2.5 V (3.3 V Tolerant)                      | HCLKIN, X(0,1)CLKFB, TMS, TDI, TCK, TRST#                        | 1 |
| CMOS I/O 14mA 2.5 V Open Drain Output (3.3 V Tolerant) | BP[1:0]#, ERR[1:0]#                                              |   |
| CMOS Output 10mA 3.3 V                                 | CRESET#, INTREQ#, IOREQ#, SMIACT#, PWRGDB, X(0,1)CLK, X(0,1)CLKB |   |
| Analog signals                                         | CRES[1:0], VCCA[2:0], VREF[5:0]                                  |   |

Note:

1. HCLKIN is equivalent to the Processor BCLK

**Table 12-2: Signal Groups PXB**

| Pin Group                                          | Signals                                                                                                                                                                                                                        | Notes |
|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| AGTL+ Input                                        | XBLK#, XHRSTS#, XHSTBN#, XHSTBP#, XRST#                                                                                                                                                                                        |       |
| AGTL+ Output                                       | XIB, XXRTS#, XXSTBN#, XXSTBP#                                                                                                                                                                                                  |       |
| AGTL+ I/O                                          | XADS#, XBE[1:0], XD[15:0]#, XPAR#                                                                                                                                                                                              |       |
| CMOS Input 2.5 V (3.3 V Tolerant)                  | XCLK, TMS, TDI, TCK, TRST#                                                                                                                                                                                                     |       |
| CMOS Input 3.3 V                                   | P(A,B)CLKFB, PIIXOK#, PWRGD                                                                                                                                                                                                    |       |
| CMOS Output 10mA, 3.3 V                            | P(A,B)CLK                                                                                                                                                                                                                      |       |
| CMOS 14mA 2.5 V Open Drain Output (3.3 V Tolerant) | TDO                                                                                                                                                                                                                            |       |
| CMOS I/O 14mA, 3.3 V Open Drain Output             | P(A,B)MON[1:0]#                                                                                                                                                                                                                |       |
| Analog Signals                                     | CRES[1:0], VCCA[2:0], VREF[1:0]                                                                                                                                                                                                |       |
| PCI Signals (Non-Duplicated)                       | ACK64#, MODE64#, PHOLD#, PHLDA#, REQ64#, WSC#                                                                                                                                                                                  |       |
| PCI Signals                                        | INTRQ(A,B)#, P(A,B)AD[31:0], P(A,B)C/BE#[3:0], P(A,B)DEVSEL#, P(A,B)FRAME#, P(A,B)GNT[5:0]#, P(A,B)IRDY#, P(A,B)LOCK#, P(A,B)PAR, P(A,B)PERR#, P(A,B)REQ(5:0)#, P(A,B)RST#, P(A,B)SERR#, P(A,B)STOP#, P(A,B)TRDY#, P(A,B)XARB# |       |

**Table 12-3: Signal Groups MUX**

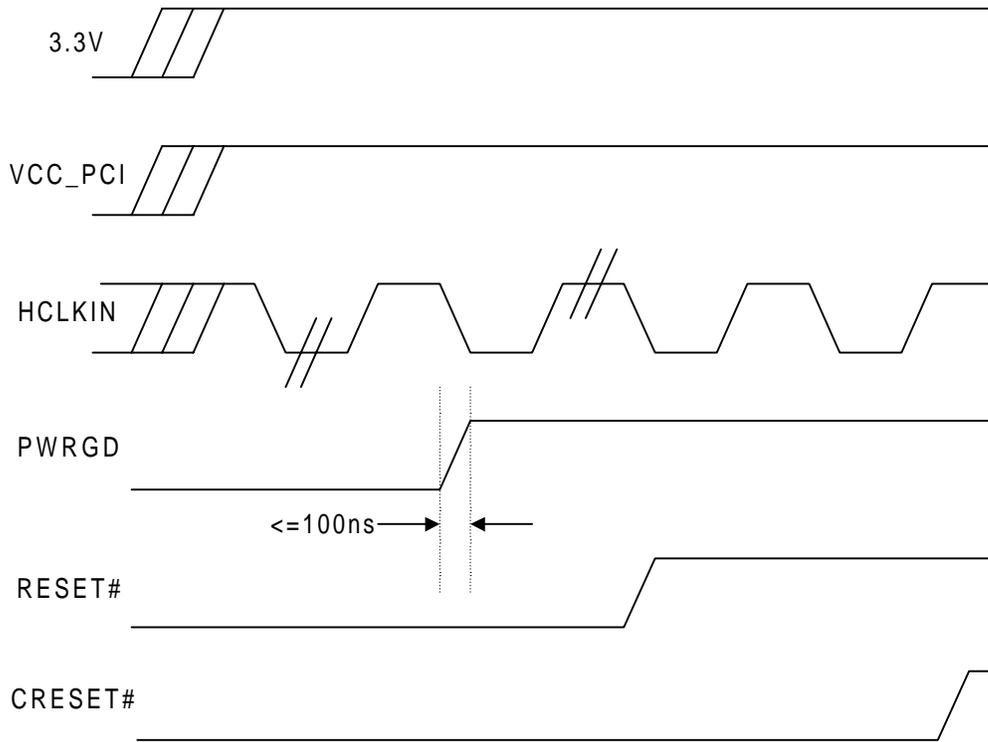
| Pin Group                                           | Signals                                                                  | Notes |
|-----------------------------------------------------|--------------------------------------------------------------------------|-------|
| AGTL+ Input                                         | AVWP#, DOFF[1:0]#, DSEL#, DVALID#, LD-STB#, LRD#, WDEVT#, WDME#, MRESET# |       |
| AGTL+ I/O                                           | DCMPLT#, DSTBP[1:0]#, DSTBN[1:0]#, GDCMPLT#, MD[35:0]#                   |       |
| CMOS Input 2.5 V (3.3 V Tolerant)                   | HCLKIN, TMS, TDI, TCK, TRST#                                             |       |
| CMOS 14mA, 2.5 V Open Drain Output (3.3 V Tolerant) | TDO                                                                      |       |
| CMOS I/O 10mA, 3.3 V                                | Q0D[35:0], Q1D[35:0], Q2D[35:0], Q3D[35:0]                               |       |
| Analog Signals                                      | CRES[1:0], VCCA, VREF[1:0]                                               |       |

**Table 12-4: Signal Groups RCG**

| Pin Group                                           | Signals                                                                                           | Notes |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------|-------|
| AGTL+ Input                                         | BANK[2:0]#, CARD#, CMND[1:0]#, CSTB#, MA[13:0]#, MRESET#, ROW#                                    |       |
| AGTL+ Output                                        | AVWP#, LDSTB#, LRD#, PHIT#, RCMPLT#, RHIT#, WDME#                                                 |       |
| AGTL+ I/O                                           | GRCMPLT#                                                                                          |       |
| CMOS Input 3.3 V                                    | BANKID#, DR50H#, DR50T#                                                                           |       |
| CMOS Input 2.5 V (3.3 V Tolerant)                   | HCLKIN, TMS, TDI, TCK, TRST#                                                                      |       |
| CMOS 14mA, 2.5 V Open Drain Output (3.3 V Tolerant) | TDO                                                                                               |       |
| CMOS Output 10mA, 3.3 V                             | ADDR(A,B,C,D)[13:0]#, WE(A,B,C,D)(a,b)#, CAS(A,B,C,D)(a,b,c,d)[1:0]#, RAS(A,B,C,D)(a,b,c,d)[1:0]# |       |
| Analog Signals                                      | CRES[1:0], VCCA, VREF[1:0]                                                                        |       |

### 12.1.3 The Power Good Signal: PWRGD

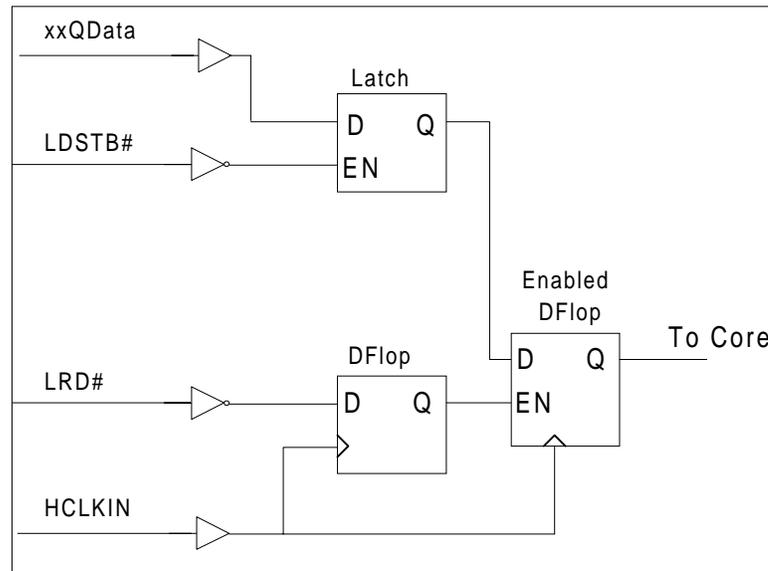
PWRGD is a 3.3 V-tolerant input to the PCI Bridge and memory controller components. It is expected that this signal will be a *clean* indication that the clocks and the 3.3 V, VCC\_PCI supplies are within their specifications. ‘Clean’ implies that PWRGD will remain low, (capable of sinking leakage current) without glitches, from the time that the power supplies are turned on until they become valid. The signal will then have a single low to high transition to a high (3. V) state with a minimum of 100ns slew rate. Figure 12-1 illustrates the relationship of PWRGD to HCLKIN and system reset signals.



**Figure 12-1: PWRGD Relationship**

The PWRGD inputs to the Intel® 450NX PCIset and to the Pentium® II Xeon™ processor(s) should be driven with an “AND” of ‘Power-Good’ signals from the 5 V, 3.3 V and V<sub>CCcoreP</sub> supplies. The output of this logic should be a 3.3 V level and should have a pull-down resistor at the output to cover the period when this logic is not receiving power.

### 12.1.4 LDSTB# Usage

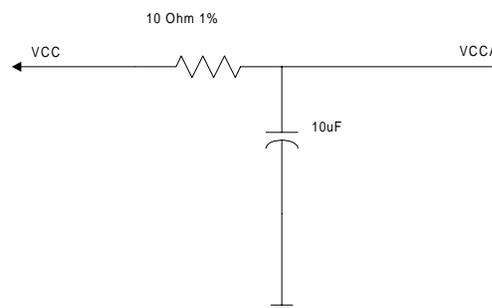


**Figure 12-2: LDSTB# Usage**

LDSTB# opens a flow-through latch to enable fine tuning of the read data timing. By adjusting the trace length of the LDSTB# signal it is possible to match the CAS# or RAS# timings (whichever is last) for optimal timing margin on DRAM read cycles.

### 12.1.5 VCCA Pins

The VCCA inputs provide the analog supply voltage used by the internal PLLs. To ensure PLL stability, a filter circuit must be used from the board VCC. Figure 12-3 shows a recommended circuit. It is important to note that a separate filter for each VCCA pin is necessary to avoid feeding noise from one analog circuit to another.



**Figure 12-3: VCCA filter**

## 12.2 Maximum Ratings

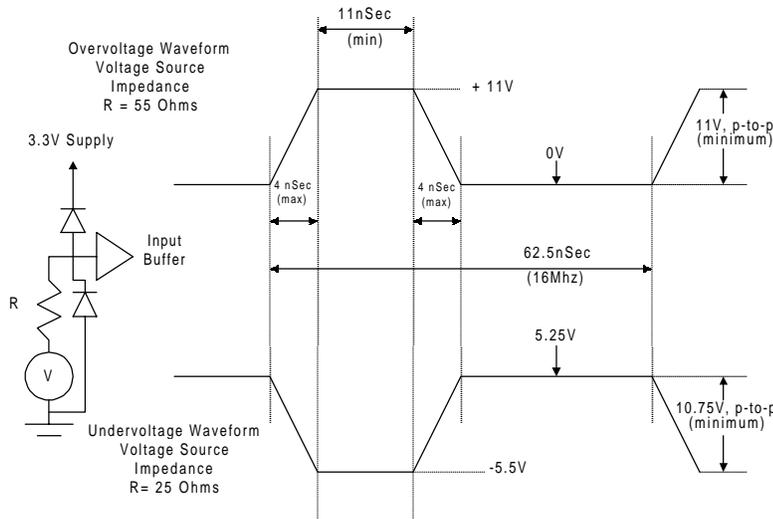
Table 12-5 contains stress ratings for the Intel® 450NX PCIset. Functional operation at the absolute maximum and minimum ratings is neither implied nor guaranteed. The Intel 450NX PCIset **should not receive a clock while subjected to these conditions**. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Intel 450NX PCIset contains protective circuitry to resist damage from static discharge, care should always be taken to avoid high static voltages or electric fields.

**Table 12-5: Absolute Maximum Ratings**

| Symbol            | Parameter                                                       | Min  | Max                                           | Unit | Notes |
|-------------------|-----------------------------------------------------------------|------|-----------------------------------------------|------|-------|
| V <sub>CC3</sub>  | 3.3 V Supply Voltage with respect to V <sub>SS</sub>            | -0.5 | 4.3                                           | V    |       |
| V <sub>IN</sub>   | AGTL+ Buffer DC Input Voltage with respect to V <sub>SS</sub>   | -0.5 | V <sub>tt</sub> + 0.5<br>(not to exceed 3.0)  | V    | 1     |
| V <sub>IN3</sub>  | 3.3 V Tolerant DC Input Voltage with respect to V <sub>SS</sub> | -0.5 | V <sub>CC3</sub> + 0.9<br>(not to exceed 4.3) | V    | 2     |
| V <sub>IN5</sub>  | 5 V Tolerant DC Input Voltage with respect to V <sub>SS</sub>   | -0.5 | V <sub>CC-PCI</sub> + 0.5                     | V    | 3     |
| T <sub>STOR</sub> | Storage Temperature                                             | -65  | 150                                           | °C   |       |

Notes:

1. Parameter applies to the AGTL+ signal groups only.
2. Parameter applies to 3.3 V-tolerant and JTAG signal groups only.
3. Parameter applies to 5 V-tolerant signal groups and PCI signals only. V<sub>CC-PCI</sub> is the voltage level on the PCI Bus.



**Figure 12-4: Maximum AC Waveforms for 5 V Signaling (PCI Signals)**

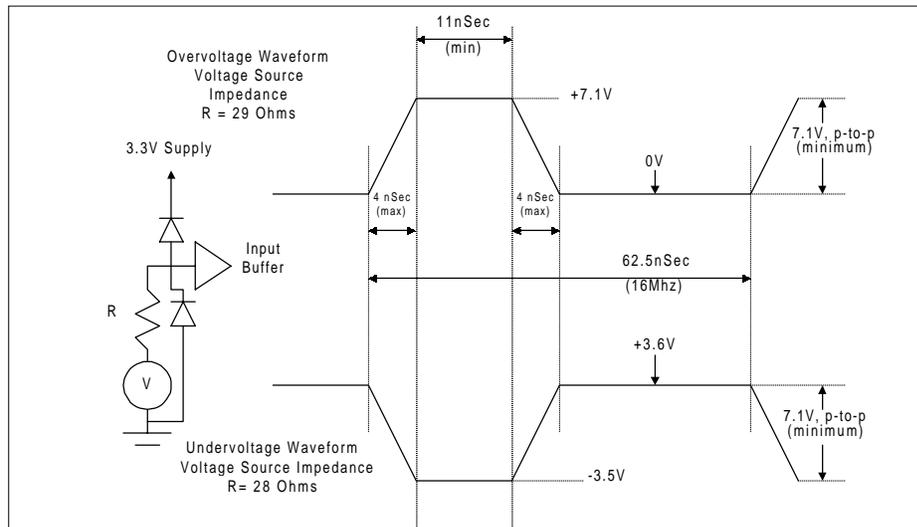


Figure 12-5: Maximum AC Waveforms for 3.3 V Signaling (PCI Signals)

## 12.3 DC Specifications

Table 12-6 through Table 12-10 list the DC specifications associated with the Intel<sup>®</sup> 450NX PCIset. Care should be taken to read any notes associated with each parameter listed.

Table 12-6: Intel<sup>®</sup> 450NX PCIset Power Parameters

| Symbol                    | Parameter                                   | Min  | Typ | Max  | Unit | Notes   |
|---------------------------|---------------------------------------------|------|-----|------|------|---------|
| V <sub>CC3</sub>          | Device V <sub>CC</sub>                      | 3.13 | 3.3 | 3.46 | V    | 1       |
| V <sub>CC-PCI (3.3)</sub> | PCI V <sub>CC</sub> for 3.3 V PCI Operation | 3.0  | 3.3 | 3.6  | V    | 2, 4    |
| V <sub>CC-PCI (5)</sub>   | PCI V <sub>CC</sub> for 5.0 V PCI Operation | 4.5  | 5.0 | 5.5  | V    | 2, 4, 5 |
| I <sub>CC-PCI</sub>       | Clamping Diode Leakage Current              |      |     | 2    | mA   | 3       |
| T <sub>C</sub>            | Operating Case Temperature                  | 0    |     | 85   | °C   |         |

Notes:

1. 3.3 V +/-5%.
2. The Intel<sup>®</sup> 450NX PCIset PXB will support either a 5 V or 3.3 V PCI Bus.
3. At 33 MHz.
4. From PCI Specification Rev 2.1.
5. Pin List VCC (A-N).

**Table 12-7: Intel® 450NX PCIsset Power Specifications**

| Symbol    | Parameter                    | Max  | Unit | Notes   |
|-----------|------------------------------|------|------|---------|
| $P_{MAX}$ | Max Power Dissipation PXB    | 7.8  | W    | 1, 2, 5 |
|           | MIOC                         | 13.2 | W    | 1, 2, 5 |
|           | MUX                          | 3.3  | W    | 1, 2, 5 |
|           | RCG                          | 2.5  | W    | 1, 5    |
| $I_{CC3}$ | Max Power Supply Current PXB | 2.2  | A    | 1, 4    |
|           | MIOC                         | 3.3  | A    | 1, 4    |
|           | MUX                          | 0.87 | A    | 1, 4    |
|           | RCG                          | 0.7  | A    | 1       |
| $I_{SS}$  | Max Power Supply Current PXB | 3.3  | A    | 1, 3    |
|           | MIOC                         | 18.1 | A    | 1, 3    |
|           | MUX                          | 2.5  | A    | 1, 3    |
|           | RCG                          | 0.8  | A    | 1, 3    |

Notes:

1. Frequency = 100 MHz.
2. This specification is a combination of core power ( $I_{CC3}$ ), and power dissipated in the AGTL+ outputs and I/O.
3.  $I_{SS}$  is the maximum supply current consumption when all AGTL+ signals are low.
4. The  $I_{CC}$  Specification does not include the AGTL+ output current to GND.

Table 12-8 lists the nominal specifications for the AGTL+ termination voltage ( $V_{TT}$ ) and the AGTL+ reference voltage ( $V_{REF}$ ).

**Table 12-8: Intel® 450NX PCIsset AGTL+ Bus DC Specifications**

| Symbol    | Parameter               | Min                | Typ          | Max                | Unit | Notes |
|-----------|-------------------------|--------------------|--------------|--------------------|------|-------|
| $V_{TT}$  | Bus Termination Voltage |                    | 1.5          |                    | V    | 1     |
| $V_{REF}$ | Input Reference Voltage | $2/3 V_{TT} - 2\%$ | $2/3 V_{TT}$ | $2/3 V_{TT} + 2\%$ | V    | 2, 3  |

Notes:

1. +/-9% during maximum di/dt and +/- 3% steady state, as measured at component  $V_{TT}$  pins.
2. Where  $V_{TT}$  tolerance can range from - 9% to +9%, as noted above.
3.  $V_{REF}$  should be created from  $V_{TT}$  by a voltage divider of 1% resistors.

Some of the signals on the MIOC, PXB, MUX and RCG are in the AGTL+ signal group. These signals are specified to be terminated to 1.5V. The DC specifications for these signals are shown in Table 12-9.

**Table 12-9: Intel® 450NX PCIset DC Specifications (AGTL+ Signal Groups)** $V_{CC3} = 3.3 \text{ V}$  (5%,  $T_{CASE} = 0 \text{ to } 85 \text{ }^\circ\text{C}$ )

| Symbol    | Parameter                 | Min             | Max             | Unit | Notes |
|-----------|---------------------------|-----------------|-----------------|------|-------|
| $V_{IL}$  | Input Low Voltage         | -0.3            | $V_{REF} - 0.2$ | V    | 1     |
| $V_{IH}$  | Input High Voltage        | $V_{REF} + 0.2$ | 2.185           | V    | 1     |
| $V_{OL}$  | Output Low Voltage        |                 | 0.6             | V    | 2     |
| $V_{OH}$  | Output High Voltage       | 1.2             | --              | V    | 3     |
| $I_{OH}$  | Output High Current       | 2               | 20              | mA   |       |
| $I_{OL}$  | Output Low Current        | 38              | 55              | mA   | 2     |
| $I_{LI}$  | Input Leakage Current     |                 | +/- 15          | uA   | 4     |
| $I_{REF}$ | Reference Voltage Current |                 | +/- 15          | uA   | 5     |
| $I_{LO}$  | Output Leakage Current    |                 | +/- 15          | uA   | 6     |
| $C_{IN}$  | Input Capacitance         |                 | 10              | pF   | 7     |
| $C_O$     | Output Capacitance        |                 | 10              | pF   | 7     |
| $C_{I/O}$ | I/O Capacitance           |                 | 10              | pF   | 7     |

## Notes:

1.  $V_{REF}$  worst case. Noise on  $V_{REF}$  should be accounted for. Refer to the *Pentium® Pro Family Developer's Manual* for more information on  $V_{REF}$ .
2. Parameter measured into a  $25 \text{ } \Omega$  resistor to  $V_{TT}$  (1.5 V).
3. A high level is maintained by the external pull-up resistors. AGTL+ is an open drain bus. Refer to the *Pentium® Pro Family Developer's Manual* for information on  $V_{TT}$ .
4. ( $0 \leq V_{IN} \leq V_{CC3}$ )
5. Total current for all  $V_{REF}$  pins.
6. ( $0 \leq V_{OUT} \leq V_{CC3}$ )
7. Total of I/O buffer and package parasitics.

**Table 12-10: Intel® 450NX PCIset DC Specifications (Non AGTL+ Groups)** $V_{CC3} = 3.3 \text{ V}$  (5%,  $T_{CASE} = 0 \text{ to } 85 \text{ }^\circ\text{C}$ )

| Symbol      | Pin Group             | Parameter                | Min  | Max  | Unit | Notes/Test Conditions |
|-------------|-----------------------|--------------------------|------|------|------|-----------------------|
| $C_{IN}$    | All                   | Input Capacitance        |      | 10   | pF   | 1                     |
| $C_O$       | All                   | Output Capacitance       |      | 10   | pF   |                       |
| $C_{I/O}$   | All                   | I/O Capacitance          |      | 10   | pF   |                       |
| $C_{CLK}$   | HCLKIN                | HCLKIN Input Capacitance |      | 10   | pF   |                       |
| $C_{TCK}$   | TCK                   | TCK Input Capacitance    |      | 8    | pF   |                       |
| $I_{OL-14}$ | CMOS 2.5 V<br>OD 14mA | Output Low Current       | 14.0 |      | mA   |                       |
| $I_{OL-10}$ | CMOS 10mA             | Output Low Current       | 10.0 |      | mA   | 2                     |
| $V_{OL}$    | CMOS 10mA             | Output Low Voltage       |      | 0.45 | V    |                       |

**Table 12-10: Intel® 450NX PCIset DC Specifications (Non AGTL+ Groups) (Continued)** $V_{CC3} = 3.3\text{ V}$  (5%,  $T_{CASE} = 0\text{ to }85\text{ }^{\circ}\text{C}$ )

| Symbol       | Pin Group             | Parameter              | Min   | Max                  | Unit | Notes/Test Conditions |
|--------------|-----------------------|------------------------|-------|----------------------|------|-----------------------|
| $V_{OL}$     | CMOS 2.5 V<br>OD 14mA | Output Low Voltage     |       | 0.45                 | V    | 11                    |
| $V_{OH}$     | CMOS 10mA             | Output High Voltage    | 2.4   |                      | V    | 9                     |
| $V_{OH}$     | CMOS 2.5 V<br>OD 14mA | Output High Voltage    | --    |                      |      | 8, 11                 |
| $I_{LO}$     | CMOS 10mA             | Output Leakage Current |       | +/-10                | uA   | 3                     |
| $I_{LI}$     | CMOS Input            | Input Leakage Current  |       | +/-10                | uA   | 4, 5                  |
| $V_{IL}$     | CMOS Input            | Input Low Voltage      | -0.5  | 0.8                  | V    |                       |
| $V_{IH}$     | CMOS Input            | Input High Voltage     | 2.0   | 3.6                  | V    |                       |
| $V_{IL}$     | CMOS 2.5 V<br>Input   | Input Low Voltage      | -0.5  | 0.7                  | V    | 11                    |
| $V_{IH}$     | CMOS 2.5 V<br>Input   | Input High Voltage     | 1.7   | 3.6                  | V    | 11                    |
| $V_{IL-PCI}$ | PCI                   | Input Low Voltage      | - 0.5 | 0.8                  | V    | 6                     |
| $V_{IH-PCI}$ | PCI                   | Input High Voltage     | 2.0   | $V_{CC-PCI}$<br>+0.5 | V    | 6, 7                  |
| $V_{OL-PCI}$ | PCI                   | Output Low Voltage     |       | 0.55                 | V    | 6                     |
| $V_{OH-PCI}$ | PCI                   | Output High Voltage    | 2.4   |                      | V    | 6                     |
| $I_{OL-PCI}$ | PCI                   | Output Low Current     | 6.0   |                      | mA   | 6                     |
| $I_{LI-PCI}$ | PCI                   | Input Leakage Current  |       | +/-70                | uA   | 6                     |
| $I_{LO-PCI}$ | PCI                   | Output Leakage Current |       | +/-10                | uA   | 6                     |

## Notes:

1. Except HCLK, TCK
2.  $V_{OL} = 0.4\text{V}$
3. ( $0 \leq V_{OUT} \leq V_{CC3}$ )
4. ( $0 \leq V_{IN} \leq V_{CC3}$ )
5. -100uA for pins with 50K pullups, +100uA for pins with 50K pulldowns.
6. 5 V-tolerant 3.3V I/O buffer.
7.  $V_{CC-PCI} = \text{PCI Bus Voltage}$ .
8. Determined by 2.5 V connected through a 150 ohm resistor.
9. Measured with 10ma load.
10. Specifications for PCI are from PCI Specification Rev 2.1.
11. 3.3 V-tolerant 2.5 V Input or Output buffer.

## 12.4 AC Specifications

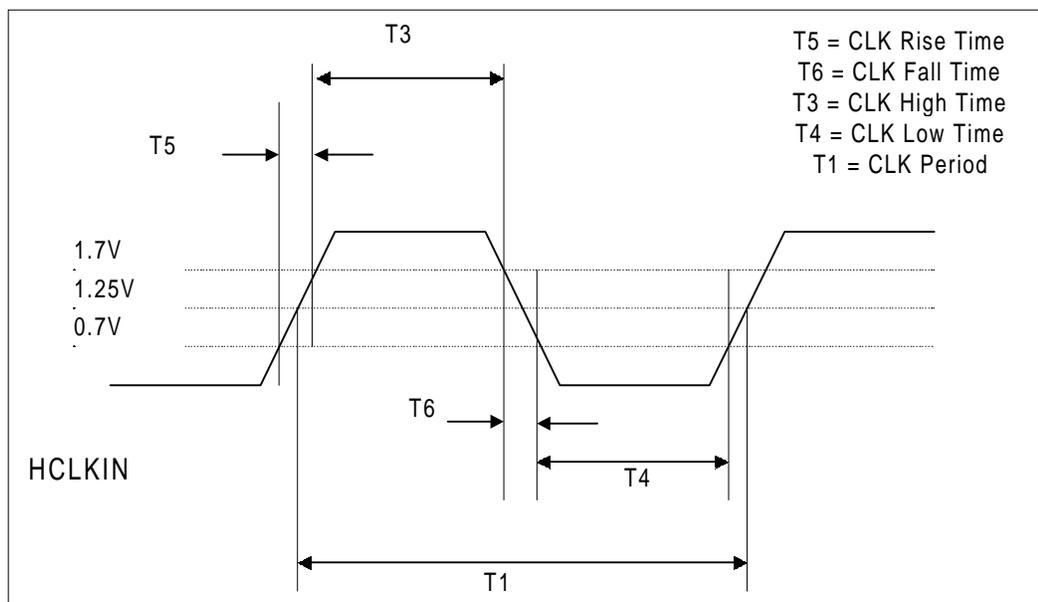


Figure 12-6: CLK Waveform

Table 12-11: Intel® 450NX PCIset Clock Specifications

$V_{CC3} = 3.3\text{ V (5\%, } T_{CASE} = 0\text{ to }85\text{ }^{\circ}\text{C)}$

| Symbol | Parameter            | Min | Max    | Unit | Notes |
|--------|----------------------|-----|--------|------|-------|
|        | Host Interface:      |     |        |      |       |
|        | Bus Frequency        | 90  | 100    | MHz  |       |
| T1     | CLK Period           | 10  | 11.11  | ns   | 1     |
| T2     | CLK Period Stability |     | +/-100 | ps   | 1     |
| T3     | CLK High Time        | 3   |        | ns   | 1     |
| T4     | CLK Low Time         | 3   |        | ns   | 1     |
| T5     | CLK Rise Time        | 0.5 | 1.5    | ns   | 1     |
| T6     | CLK Fall Time        | 0.5 | 1.5    | ns   | 1     |
| T9     | TCK Frequency        |     | 16.67  | MHz  |       |
| T72    | TCK Hightime         | 25  |        | ns   |       |
| T73    | TCK Lowtime          | 25  |        | ns   |       |
| T74    | TCK rise time        |     | 5      | ns   |       |
| T75    | TCK fall time        |     | 5      | ns   |       |

Note:

1. These specifications apply to all clock inputs for all four Intel® 450NX PCIset components.

Table 12-12: Intel® 450NX PCIset MIOC AC Specifications

V<sub>CC3</sub> = 3.3V (5%, T<sub>CASE</sub> = 0 to 85 °C)

| Symbol | Parameter                                                                                                                                     | Setup Min | Hold Min | Delay Min | Delay Max | Unit | Notes |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------|-----------|-----------|------|-------|
|        | Host Interface:                                                                                                                               |           |          |           |           |      |       |
| T10A   | A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BPRI#, D[63:0]#, DBSY#, DEFER#, DEP[7:0]#, DRDY#, REQ[4:0]#, RP#, RS[2:0]#, RSP#, TRDY# | 1.58      | 0.63     | -0.15     | 2.65      | ns   | 8     |
| T17    | BP[1:0]                                                                                                                                       | 2.0       | 0.5      | 1.0       | 5.0       | ns   | 10    |
| T11    | BR0#                                                                                                                                          |           |          | -0.15     | 2.65      | ns   | 8     |
| T13A   | HIT#, HITM#, LOCK#                                                                                                                            | 1.58      | 0.63     |           |           | ns   |       |
| T12    | INIT#                                                                                                                                         |           |          | 1.0       | 5.0       | ns   | 9     |
|        | Third-Party Agent Interface:                                                                                                                  |           |          |           |           |      |       |
| T14    | IOREQ#                                                                                                                                        |           |          | 0.0       | 3.5       | ns   | 3     |
| T15    | IOGNT#                                                                                                                                        | 2.0       | 0.5      |           |           | ns   |       |
| T16    | TPCTL[1:0]                                                                                                                                    | 2.0       | 0.5      |           |           | ns   |       |
|        | Memory Interface:                                                                                                                             |           |          |           |           |      |       |
| T11    | BANK[2:0]#, CARD[1:0]#, CMND[1:0]#, CSTB#, DOFF[1:0], DSEL[1:0]#, DVALID(a,b)#, MA[13:0]#, ROW#, WDEVT#                                       |           |          | -0.15     | 2.65      | ns   | 8     |
| T11    | MRESET#                                                                                                                                       |           |          | -0.15     | 2.65      | ns   | 7, 8  |
| T10    | DCMPLT(a,b)#                                                                                                                                  | 1.88      | 0.63     | -0.15     | 2.65      | ns   | 8     |
| T13    | PHIT(a,b)#, RCM-PLT(a,b)#, RHIT(a,b)#                                                                                                         | 1.88      | 0.63     |           |           | ns   |       |
|        | MD(71:0)#, DST-BP(3:0)#, DST-BN(3:0)#                                                                                                         |           |          |           |           |      | 11    |
|        |                                                                                                                                               |           |          |           |           |      | 11    |
|        |                                                                                                                                               |           |          |           |           |      | 11    |

**Table 12-12: Intel® 450NX PCIset MIOC AC Specifications (Continued)**V<sub>CC3</sub> = 3.3V (5%, T<sub>CASE</sub> = 0 to 85 °C)

| Symbol | Parameter                                | Setup Min | Hold Min | Delay Min | Delay Max | Unit | Notes    |
|--------|------------------------------------------|-----------|----------|-----------|-----------|------|----------|
|        | Expander Interface<br>(two per MIOC:0,1) |           |          |           |           |      |          |
| T21    | X(0,1)RST#,<br>X(0,1)RSTB#               |           |          | -0.1      | 3.25      | ns   | 7, 8     |
| T23    | X(0,1)RSTFB#,<br>X(0,1)XRTS#             | 1.88      | 0.63     |           |           | ns   |          |
| T11    | X(0,1)HRTS#                              |           |          | -0.15     | 2.65      | ns   | 8        |
|        | Other                                    |           |          |           |           |      |          |
| T39    | CRESET#                                  |           |          | 1.0       | 4.1       | ns   | 3        |
| T25    | ERR[1:0]#                                | 2.0       | 0.5      | 1.0       | 5.0       | ns   | 10       |
| T70    | INTREQ#, SMI-<br>ACT#                    |           |          | 0.0       | 3.5       | ns   | 3        |
| T71    | PWRGD                                    | 4.0       | 1.0      |           |           | ns   | 1, 6     |
| T70    | PWRGDB                                   |           |          | 0.0       | 3.5       | ns   | 3, 5, 13 |
| T21    | RESET#                                   |           |          | -0.1      | 3.25      | ns   | 7, 8, 12 |
|        | Testability<br>Signals:                  |           |          |           |           |      |          |
| T26    | TRST#                                    |           |          |           |           | ns   | 4, 6     |
| T27    | TMS                                      | 5.0       | 14.0     |           |           | ns   | 2        |
| T27    | TDI                                      | 5.0       | 14.0     |           |           | ns   | 2        |
| T28    | TDO                                      |           |          | 1.0       | 10.0      | ns   | 2, 3     |
| T29    | TDO on/off delay                         |           |          |           | 25.0      | ns   | 2, 3     |

## Notes:

1. The power supply must wait until all voltages are stable for at least 1ms, and then assert the PWRGD signal.
2. 3.3 V-tolerant signals. Inputs are referenced to TCK rising, outputs are referenced to TCK falling.
3. Min and Max timings are measured with 0pF load.
4. TRST# requires a pulse width of 40 ns.
5. This output is asynchronous.
6. This input is asynchronous.
7. Asynchronous assertion with synchronous deassertion.
8. Min and Max timings are measured with 0pf and 25 Ohms to V<sub>tt</sub>.
9. Min and Max timings are measured with 0pf and 150 Ohms to 2.5 V.
10. Min and Max timings are measured with 0pf and 230 Ohm to 3.3 V.
11. See Table 12-16 for source synchronous timings.
12. Minimum pulse width 1.0ms.
13. PWRGDB is the buffered output of PWRGD, and has no relation to HCLKIN.

Table 12-13: Intel® 450NX PCIset PXB AC Specifications

V<sub>CC3</sub> = 3.3 V (5%, T<sub>CASE</sub> = 0 to 85 °C)

| Symbol | Parameter                                                                                                                                                                            | Setup Min | Hold Min | Delay Min | Delay Max | Unit | Notes |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------|-----------|-----------|------|-------|
|        | PCI Interface                                                                                                                                                                        |           |          |           |           |      |       |
| T30    | P(A,B)AD[31:0],<br>P(A,B)C/BE[3:0]#,<br>P(A,B)TRDY#,<br>P(A,B)STOP#,<br>P(A,B)LOCK#,<br>P(A,B)DEVSEL#,<br>P(A,B)PAR,<br>P(A,B)IRDY#,<br>P(A,B)FRAME#,<br>P(A,B)PERR#,<br>P(A,B)XARB# | 7.0       | 0.0      | 2.0       | 11.0      | ns   | 1, 3  |
| T31    | P(A,B)REQ[5:0]#                                                                                                                                                                      | 12.0      | 0.0      |           |           | ns   | 1, 3  |
| T32    | P(A,B)GNT[5:0]#                                                                                                                                                                      |           |          | 2.0       | 12.0      | ns   | 1, 3  |
| T34    | INTRQ(A,B)#,<br>P(A,B)RST#,<br>P(A,B)SERR#                                                                                                                                           |           |          | 2.0       | 11.0      | ns   | 1, 3  |
| T33    | ACK64#                                                                                                                                                                               | 7.0       | 0.0      | 2.0       | 11.0      | ns   | 1, 3  |
| T35    | PHOLD#                                                                                                                                                                               | 7.0       | 0.0      |           |           | ns   | 1     |
| T36    | PHLDA#                                                                                                                                                                               |           |          | 2.0       | 12.0      | ns   | 1, 3  |
| T37    | REQ64#                                                                                                                                                                               | 7.0       | 0.0      | 2.0       | 11.0      | ns   | 1, 3  |
| T38    | WSC#                                                                                                                                                                                 |           |          | 2.0       | 12.0      | ns   | 1, 3  |
|        |                                                                                                                                                                                      |           |          |           |           |      |       |
|        | Expander Interface<br>(one per PXB)                                                                                                                                                  |           |          |           |           |      |       |
| T40    | XRST#                                                                                                                                                                                | 2.8       | 0.0      |           |           | ns   | 6     |
| T11    | XXRTS#                                                                                                                                                                               |           |          | -0.15     | 2.65      | ns   | 8     |
| T13    | XHRTS#                                                                                                                                                                               | 1.88      | 0.63     |           |           | ns   |       |
|        | OTHER                                                                                                                                                                                |           |          |           |           |      |       |
| T47    | P(A,B)MON[1:0]#                                                                                                                                                                      | 4.0       | 0.5      | 1.0       | 6.0       | ns   | 4     |
| T46    | PIIXOK#                                                                                                                                                                              | 7.0       | 0.0      |           |           | ns   | 1     |
|        |                                                                                                                                                                                      |           |          |           |           |      |       |
|        | Testability Signals:                                                                                                                                                                 |           |          |           |           |      |       |
| T26    | TRST#                                                                                                                                                                                |           |          |           |           | ns   | 5, 7  |
| T27    | TMS                                                                                                                                                                                  | 5.0       | 14.0     |           |           | ns   | 2     |
| T27    | TDI                                                                                                                                                                                  | 5.0       | 14.0     |           |           | ns   | 2     |
| T28    | TDO                                                                                                                                                                                  |           |          | 1.0       | 10.0      | ns   | 2, 4  |
| T29    | TDO on/off delay                                                                                                                                                                     |           |          |           | 25.0      | ns   | 2, 4  |

## Notes:

1. 5 V-tolerant.
2. 3.3 V-tolerant signals. Inputs are referenced to TCK rising, outputs are referenced to TCK falling.
3. Min timings are measured with 0pF load, Max timings are measured with 50pF load.
4. Min and Max timings are measured with 0pF load.
5. TRST# requires a pulse width of 40 ns.
6. This signal has an asynchronous assertion and a synchronous deassertion.
7. This input is asynchronous.

**PCI Bus Signal Waveforms:** All PCI Bus signals are referenced to the PCLK Rising edge. For more information on the PCI Bus signals and waveforms, please refer to the *PCI Specification*.

**Table 12-14: Intel® 450NX PCIset RCG AC Specifications**

$V_{CC3} = 3.3 \text{ V}$  (5%,  $T_{CASE} = 0 \text{ to } 85 \text{ }^\circ\text{C}$ )

| Symbol | Parameter                                             | Setup Min | Hold Min | Delay Min | Delay Max | Unit | Notes |
|--------|-------------------------------------------------------|-----------|----------|-----------|-----------|------|-------|
|        | Memory Subsystem/ External Interface                  |           |          |           |           |      |       |
| T50    | BANK[2:0]#, CARD#, CMND[1:0]#, CSTB#, MA[13:0]#, ROW# | 2.80      | 0.0      |           |           | ns   |       |
| T51    | GRCMPLT#                                              | 2.80      | 0.0      | -0.15     | 2.65      | ns   | 6     |
| T52    | PHIT#, RCMPLT#, RHIT#                                 |           |          | -0.15     | 2.65      | ns   | 6     |
|        | Memory Subsystem/Internal Interface                   |           |          |           |           |      |       |
| T52    | AVWP#, LRD#, WDME#, LD-STB#                           |           |          | -0.15     | 2.65      | ns   | 6     |
| T53    | CAS(A,B,C,D)(a,b,c,d)[1:0]#                           |           |          | 0.0       | 3.5       | ns   | 3     |
| T54    | ADDR(A,B,C,D)[13:0]#                                  |           |          | 1.0       | 5.5       | ns   | 3     |
| T53    | RAS(A,B,C,D)(a,b,c,d)[1:0]#                           |           |          | 0.0       | 3.5       | ns   | 3     |
| T53    | WE(A,B,C,D)(a,b)#                                     |           |          | 0.0       | 3.5       | ns   | 3     |
|        | Other                                                 |           |          |           |           |      |       |
| T50    | MRESET#                                               | 2.8       | 0.0      |           |           | ns   | 5     |
| T26    | TRST#                                                 |           |          |           |           | ns   | 4, 7  |
| T27    | TMS                                                   | 5.0       | 14.0     |           |           | ns   | 2     |
| T27    | TDI                                                   | 5.0       | 14.0     |           |           | ns   | 2     |
| T28    | TDO                                                   |           |          | 1.0       | 10.0      | ns   | 2, 3  |
| T29    | TDO on/off delay                                      |           |          |           | 25.0      | ns   | 2, 3  |

## Notes:

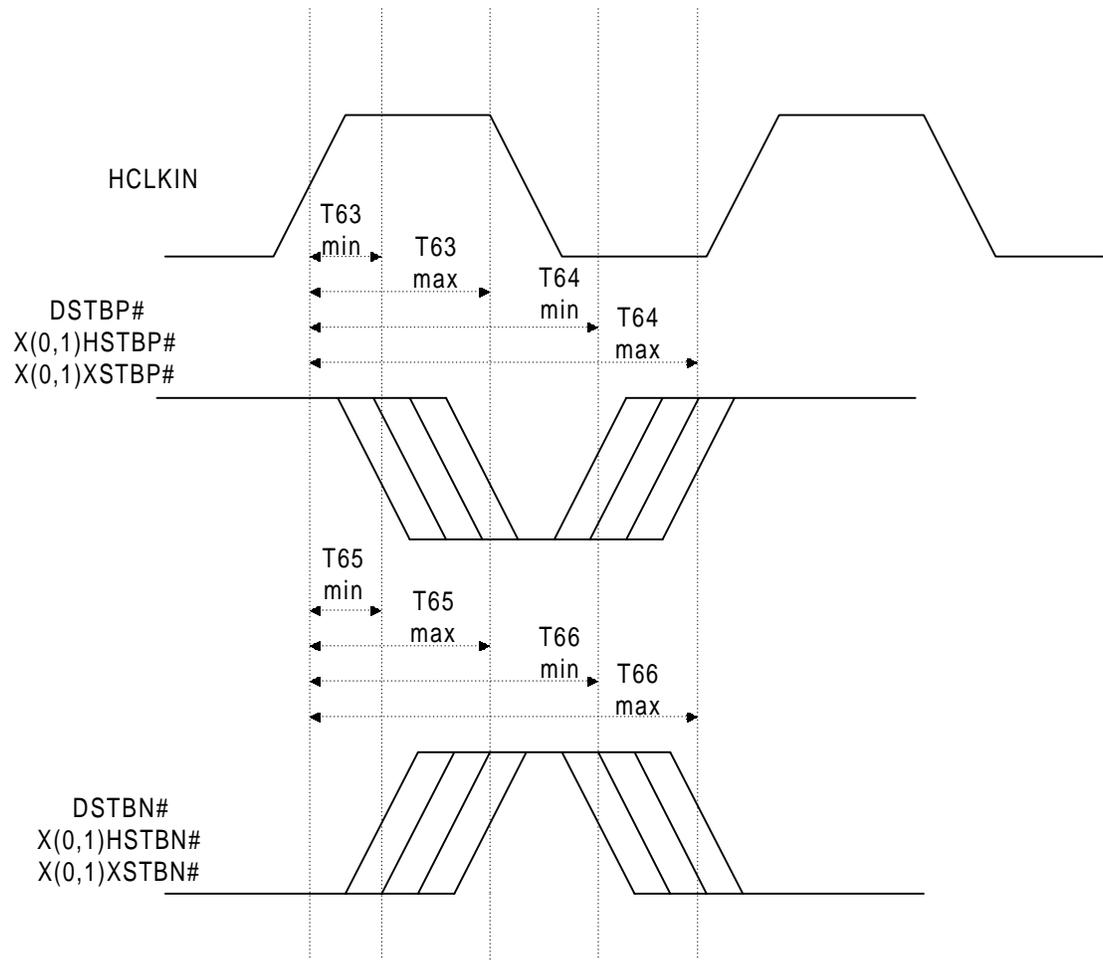
1. The power supply must wait until all voltages are stable for at least 1ms, and then assert the PWRGD signal.
2. 3.3- tolerant signals. Inputs are referenced to TCK rising, outputs are referenced to TCK falling.
3. Min and Max timings are measured with 0pF load.
4. TRST# requires a pulse width of 40 ns.
5. Max delay timing requirement from MIOC to RCGs and MUXs is two clock cycles. Asynchronous assertion and synchronous deassertion.
6. Min and Max timings are measured with 0pF and  $25\Omega$  to  $V_{tt}$  (1.5 V).
7. This input is asynchronous.

**Table 12-15: Intel® 450NX PCIset MUX AC Specifications** $V_{CC3} = 3.3\text{ V}$  (5%,  $T_{CASE} = 0$  to  $85^{\circ}\text{C}$ )

| Symbol | Parameter                                     | Setup Min | Hold Min | Delay Min | Delay Max | Unit | Notes |
|--------|-----------------------------------------------|-----------|----------|-----------|-----------|------|-------|
|        | Memory Subsystem/<br>External Interface       |           |          |           |           |      |       |
| T60    | DCMPLT#                                       | 2.8       | 0.0      | -0.15     | 2.65      | ns   | 6     |
| T61    | DOFF[1:0]#, DSEL#,<br>DVALID#, WDEVT#         | 2.8       | 0.0      |           |           | ns   | 8     |
| T60    | GDCMPLT#                                      | 2.8       | 0.0      | -0.15     | 2.65      | ns   | 6     |
| T67    | LDSTB#                                        | 3.0       | 1.0      |           |           | ns   |       |
|        | Memory Subsystem/<br>Internal Interface       |           |          |           |           |      |       |
| T62    | AVWP#, WDME#                                  | 3.5       | 0.0      |           |           | ns   |       |
| T62    | LRD#                                          | 3.5       | 0.0      |           |           | ns   |       |
| T68    | Q0D[35:0], Q1D[35:0],<br>Q2D[35:0], Q3D[35:0] | 1.0       | 4.0      | 0.0       | 3.5       | ns   | 2, 4  |
|        | Other                                         |           |          |           |           |      |       |
| T69    | MRESET#                                       | 2.8       | 0.0      |           |           | ns   | 5     |
|        | Testability Signals:                          |           |          |           |           |      |       |
| T26    | TRST#                                         |           |          |           |           | ns   | 3, 7  |
| T27    | TMS, TDI                                      | 5.0       | 14.0     |           |           | ns   | 1     |
| T28    | TDO                                           |           |          | 1.0       | 10.0      | ns   | 1, 2  |
| T29    | TDO on/off delay                              |           |          |           | 25.0      | ns   | 1, 2  |

## Notes:

- 3.3 V-tolerant signals. Inputs are referenced to TCK rising, outputs are referenced to TCK falling.
- Min and Max timings are measured with 0pF load.
- TRST# requires a pulse width of 40 ns.
- Input timings are referenced from LDSTB# rising edge. Output timings are referenced from HCLKIN.
- Max delay timing requirement from MIOC to RCGs and MUXs is two clock cycles. Asynchronous assertion and synchronous deassertion.
- Min and Max timings are measured with 0pF and  $25\Omega$  to  $V_{tt}$  (1.5 V).
- This input is asynchronous.
- DOFF[1:0]#, DSEL#, WDEVT# max delay timing requirement from MIOC to MUX is two clock cycles.



**Figure 12-7: Source Synchronous Strobe Timing**

**Table 12-16: 100 MHz Source Synchronous Timing**

| Symbol | Parameter                                                  | Delay Min | Delay Max | Skew | Unit | Notes   |
|--------|------------------------------------------------------------|-----------|-----------|------|------|---------|
| T63    | DSTBP(3:0)#, X(0,1)HSTBP#,<br>X(0,1)XSTBP#<br>Falling Edge | 2.35      | 5.15      |      | ns   | 1, 2, 4 |
| T64    | DSTBP(3:0)#, X(0,1)HSTBP#,<br>X(0,1)XSTBP#<br>Rising Edge  | 7.35      | 10.15     |      | ns   | 1, 3, 4 |
| T65    | DSTBN(3:0)#, X(0,1)HSTBN#,<br>X(0,1)XSTBN#<br>Rising Edge  | 2.35      | 5.15      |      | ns   | 1, 2, 4 |
| T66    | DSTBN(3:0)#, X(0,1)HSTBN#,<br>X(0,1)XSTBN#<br>Falling Edge | 7.35      | 10.15     |      | ns   | 1, 3, 4 |

## Notes:

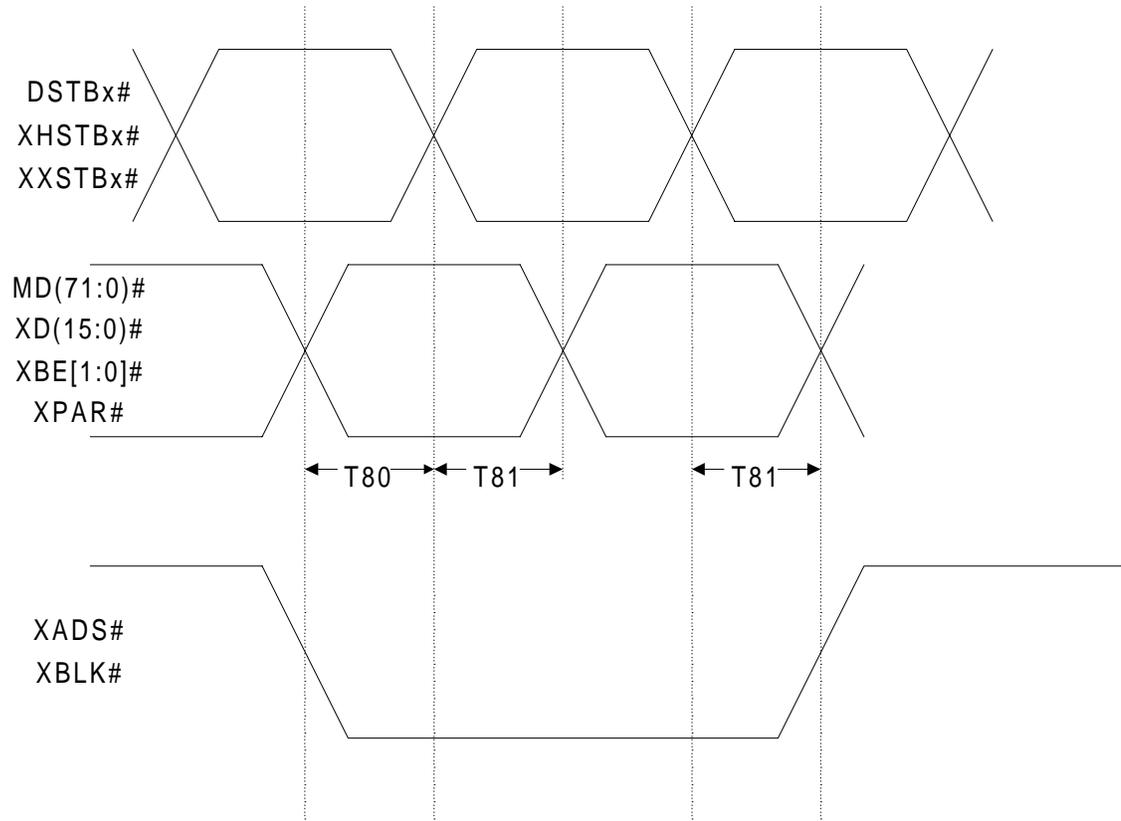
1. Relative to HCLKIN Rising edge.
2. Strobe timings are generated from an internal clock which is a multiple of HCLKIN. This enables the strobes to track system timings staying centered within the data window. Numbers given are for 100 MHz operation. Timings for other frequencies can be calculated by  $\text{Strobe\_Min\_Time} = [-0.15 + (1/\text{Bus\_Freq})1/4]$  ns and  $\text{Strobe\_Max\_Time} = [2.65 + (1/\text{Bus\_Freq})1/4]$  ns.
3. Strobe timings are generated from an internal clock which is a multiple of HCLKIN. This enables the strobes to track system timings staying centered within the data window. Numbers given are for 100 MHz operation. Timings for other frequencies can be calculated by  $\text{Strobe\_Min\_Time} = [-0.15 + (1/\text{Bus\_Freq})3/4]$  ns and  $\text{Strobe\_Max\_Time} = [2.65 + (1/\text{Bus\_Freq})3/4]$  ns.
4. Min and Max timings are measured with 0pF and  $25\Omega$  to Vtt (1.5 V).

**Table 12-17: Source Synchronous Signal to Strobe Timings (at source)**

| Symbol | Parameter                                                                                    | Setup Min | Setup Max | Hold Min | Hold Max | Notes |
|--------|----------------------------------------------------------------------------------------------|-----------|-----------|----------|----------|-------|
| T80    | MD(71:0)#,<br>X(0,1)D[15:0]#,<br>X(0,1)ADS#,<br>X(0,1)BE[1:0]#,<br>X(0,1)BLK#,<br>X(0,1)PAR# | 2.0       | 2.75      |          |          | 1-5   |
| T81    | MD(71:0)#,<br>X(0,1)D[15:0]#,<br>X(0,1)ADS#,<br>X(0,1)BE[1:0]#,<br>X(0,1)BLK#,<br>X(0,1)PAR# |           |           | 2.0      | 2.75     | 1-5   |

## Notes:

1. MD(71:0)# strobes are single-ended, and the falling edge of the strobe is used to capture data; Expander strobes are differential.
2. Values are guaranteed by design.
3. Setup Max and Hold Max are specified at frequency= 100 MHz.
4. Timings for other frequencies can be calculated as follows: T80 Setup\_Max =  $[(1/\text{Bus\_Freq})1/4 + .250]$  ns, T81 Hold\_Max =  $[(1/\text{Bus\_Freq})1/4 + .250]$  ns, where .250ns represents the error margin around strobe placement.
5. Data delay times relative to HCLK for any bus frequency can be calculated as follows... For First Data: Data\_Min\_Time =  $[-0.15]$  ns and Data\_Max\_Time =  $[2.65]$  ns; For Second Data: Data\_Min\_Time =  $[-0.15 + (1/\text{Bus\_Freq})/2]$  ns and Data\_Max\_Time =  $[2.65 + (1/\text{Bus\_Freq})/2]$  ns.



**Figure 12-8: Source Synchronous Signal to Strobe Timings (at source)**

**Table 12-18: 100 MHz Source Synchronous Timing (at destination)**

| Symbol | Parameter                                                                                         | Setup Min | Hold Min | Unit | Notes |
|--------|---------------------------------------------------------------------------------------------------|-----------|----------|------|-------|
| T20    | DSTBN(3:0)#,<br>DSTBP(3:0)#<br>X(0,1)XSTBN#<br>X(0,1)XSTBP#                                       | 7.0       |          | ns   | 1,4   |
| T24    | MD(71:0)#                                                                                         | 1.5       | 1.5      | ns   | 2     |
| T22    | X(0,1)D[15:0]#,<br>X(0,1)ADS#,<br>X(0,1)BE[1:0]#,<br>X(0,1)BLK#,<br>X(0,1)D[15:0]#,<br>X(0,1)PAR# | 1.75      | 1.0      | ns   | 3     |

Notes:

1. Setup in relation to “capture” HCLKIN.
2. With respect to the DSTBs.
3. With respect to the HSTBs.
4. Applies to Expander bus source synchronous signals. For synchronous signals (RTS#) the maximum clock skew between MIOC and PXB plus the flight time must not exceed 4.97nS.

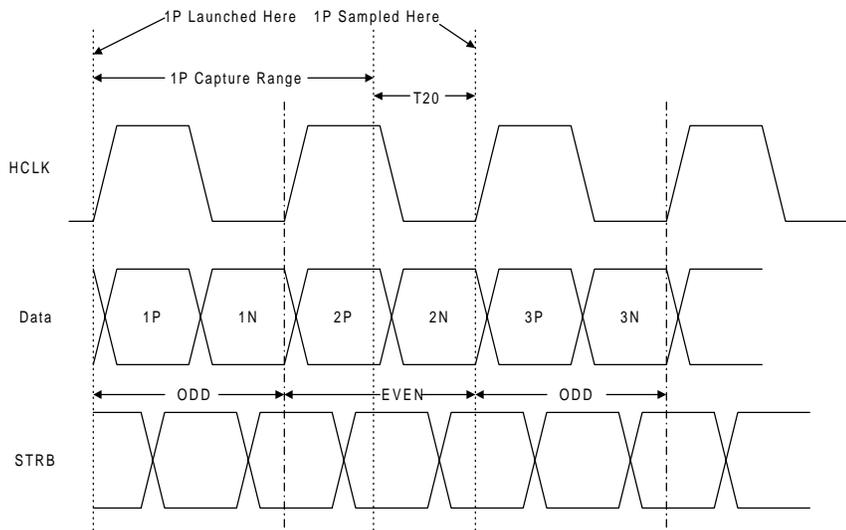


Figure 12-9: Source Synchronous Data Transfer

## 12.5 Source Synchronous Data Transfers

A Source Synchronous packet has a two clock period delivery time, and is divided into positive and negative phases of even and odd cycles. During this two clock window, packets are launched synchronously and sampled synchronously. Signals launched with a positive phase “even” clock are sampled on a positive phase of next “even” clock. Between launch and sample, signals are captured with source synchronous strobes.

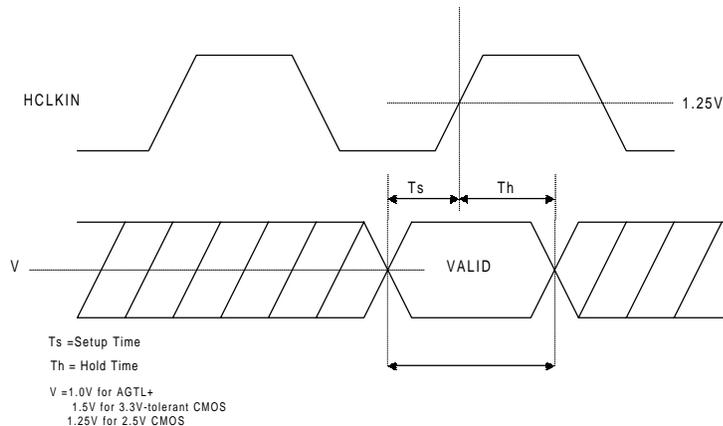
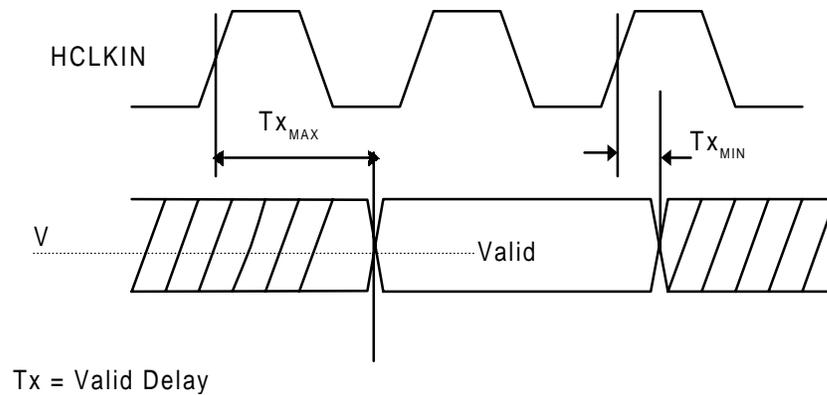


Figure 12-10: Setup and Hold Timings



**Figure 12-11: Valid Delay Timing**

## 12.6 I/O Signal Simulations: Ensuring I/O Timings

It is highly recommended that system designers run extensive simulations on their Pentium® II Xeon™ processor/Intel® 450NX PCIset-based designs. These simulations should include the memory subsystem design as well. Please refer to the *Pentium® Pro Family Developer's Manual* for more information.

## 12.7 Signal Quality Specifications

Signals driven by any component on the Pentium® II Xeon™ processor bus must meet signal quality specifications to guarantee that the components read data properly, and to ensure that incoming signals do not affect the long term reliability of the components. There are three signal quality parameters defined: Overshoot/Undershoot, Ringback, and Settling Limit, which are discussed in the next sections.

### 12.7.1 Intel® 450NX PCIset Ringback Specification

This section discusses the ringback specification for the parameters in the AGTL+ signal groups on the Intel® 450NX PCIset.

Case A requires less time than Case B from the  $V_{REF}$  crossing until the ringback into the "overdrive" region. The longer time from  $V_{REF}$  crossing until the ringback into the "overdrive" region required in Case B allows the ringback to be closer to  $V_{REF}$  for a defined period.

**Table 12-19: Intel® 450NX PCIset AGTL+ Signal Groups Ringback Tolerance: Case A**

| Parameter                                | Min  | Unit | Figure  | Notes |
|------------------------------------------|------|------|---------|-------|
| $\alpha$ Overshoot                       | 100  | mV   | 12 & 13 | 1     |
| $\tau$ Minimum Time at High or Low       | 2.25 | ns   | 12 & 13 | 1     |
| $\rho$ Amplitude of Ringback             | -100 | mV   | 12 & 13 | 1     |
| $\delta$ Duration of Squarewave Ringback | N/A  | ns   | 12 & 13 | 1     |
| $\phi$ Final Settling Voltage            | 100  | mV   | 12 & 13 | 1     |

Note:

1. Specified for an edge rate of 0.8-1.3 V/ns. See the *Pentium® Pro Family Developer's Manual* for the definition of these terms. See Figure 12-12 and Figure 12-13 for the generic waveforms. All values are determined by design/characterization.

**Table 12-20: Intel® 450NX PCIset AGTL+ Signal Groups Ringback Tolerance: Case B**

| Parameter                                | Min | Unit | Figure  | Notes |
|------------------------------------------|-----|------|---------|-------|
| $\alpha$ Overshoot                       | 100 | mV   | 12 & 13 | 1     |
| $\tau$ Minimum Time at High or Low       | 2.7 | ns   | 12      | 1     |
| $\tau$ Minimum Time at Low               | 3.7 | ns   | 13      | 1     |
| $\rho$ Amplitude of Ringback             | -0  | mV   | 12 & 13 | 1     |
| $\delta$ Duration of Squarewave Ringback | 2   | ns   | 12 & 13 | 1     |
| $\phi$ Final Settling Voltage            | 100 | mV   | 12 & 13 | 1     |

Note:

1. Specified for an edge rate of 0.8-1.3 V/ns. See the *Pentium® Pro Family Developer's Manual* for the definition of these terms. See the figures below for the generic waveforms. All values are determined by design/characterization.

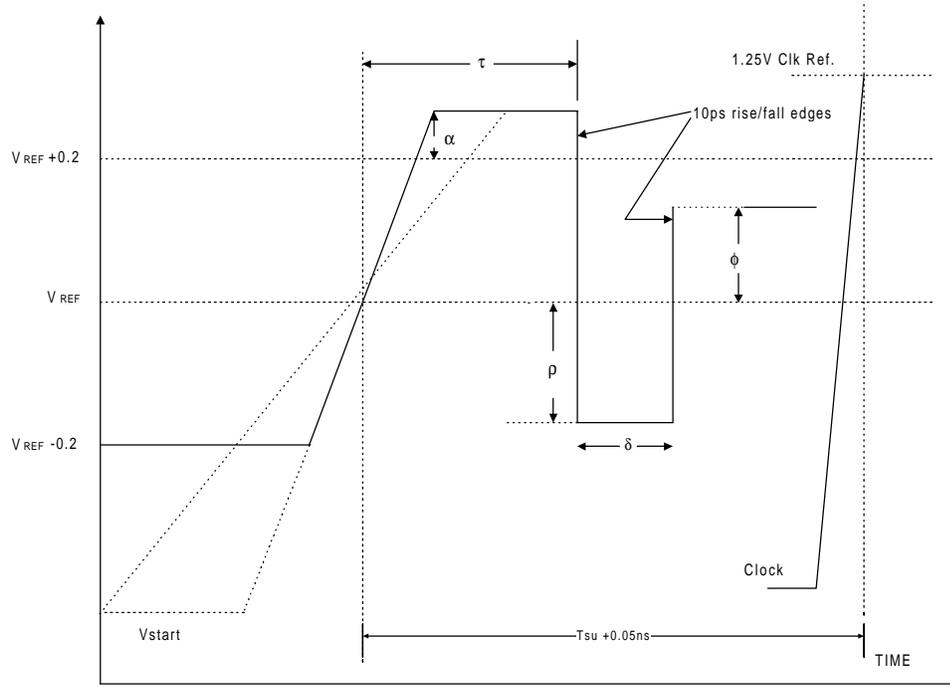


Figure 12-12: Standard Input Lo-to-Hi Waveform for Characterizing Receiver Ringback Tolerance

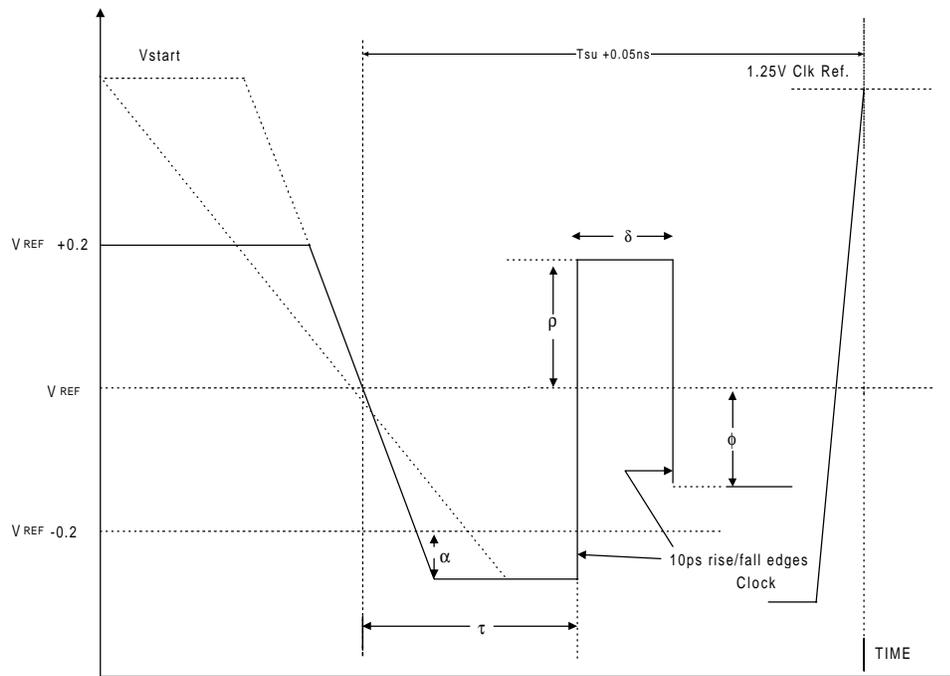


Figure 12-13: Standard Input Hi-to-Lo Waveform for Characterizing Receiver Ringback Tolerance

### 12.7.2 Intel® 450NX PCIset Undershoot Specification

The undershoot specification for the Intel 450NX PCIset components (and Pentium II Xeon processor) is as follows:

The Pentium II Xeon processor bus signals AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM# (only) are capable of sinking an 85mA current pulse at a 2.4% average time duty cycle. This is equivalent to -1.7V applied to a 20Ω source in series with the device pin for 5.38 ns at 100 MHz with a utilization of 5%.

This test covers the AC operating conditions only

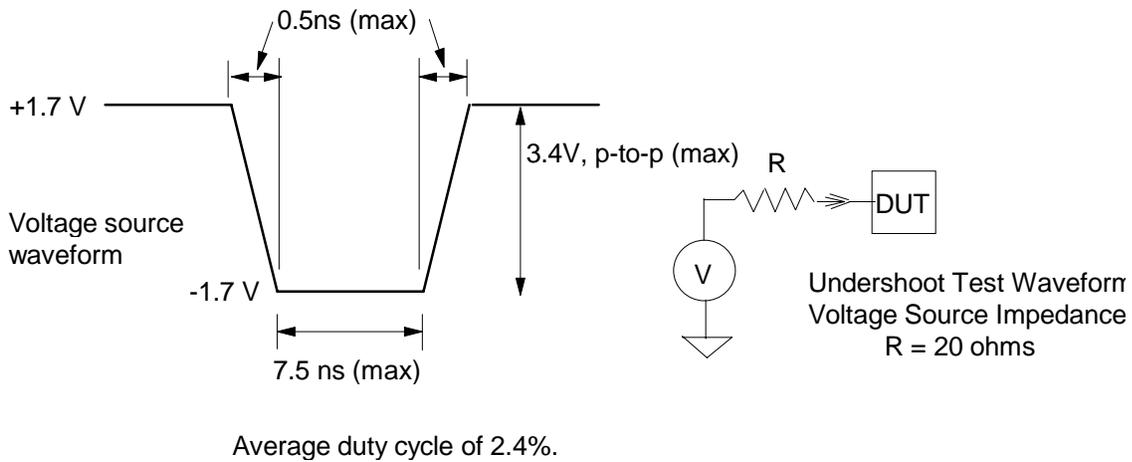


Figure 12-14: Undershoot Test Setup

### 12.7.3 Skew Requirements

The skew requirement for XpRST# versus XpRSTFB#, and XpCLK versus XpCLKFB is +/- 125ps.

The electrical length (delay) from the XpCLK# signal pin on the MIOC to the clock input of the PXB must match the delay to the XpCLKFB# pin on the MIOC by that amount. The same is true with XpRST# and XpRSTFB#.

## 12.8 Intel® 450NX PCIset Thermal Specifications

### 12.8.1 Thermal Solution Performance

The system's thermal solution must adequately control the package temperatures below the maximum and above the minimum specified. The performance of any thermal solution is defined as the thermal resistance between the package and the ambient air around the part (package to ambient). The lower the thermal resistance between the package and the ambient air, the more efficient the thermal solution is. The required  $\theta$  package to ambient is dependent upon the maximum allowed package temperature ( $T_{\text{Package}}$ ), the local ambient temperature (TLA), and the package power ( $P_{\text{Package}}$ ).

$$\text{Package to ambient} = (T_{\text{Package}} - T_{\text{LA}}) / P_{\text{Package}}$$

TLA is a function of the system design. Table 12-21 and Table 12-22 provide the resulting thermal solution performance required for an Intel® 450NX PCIset at different ambient air temperatures around the parts.

**Table 12-21: Example Thermal Solution Performance for MIOC at Package Power of 13.2 Watts**

| Local Ambient Temperature (TLA)       |       |       |       |
|---------------------------------------|-------|-------|-------|
|                                       | 35° C | 40° C | 45° C |
| $\theta$ Package to ambient °C/(Watt) | 3.79  | 3.41  | 3.03  |

**Table 12-22: Example Thermal Solution Performance for PXB at Package Power of 7.8 Watts**

| Local Ambient Temperature (TLA)       |       |       |       |
|---------------------------------------|-------|-------|-------|
|                                       | 35° C | 40° C | 45° C |
| $\theta$ Package to ambient °C/(Watt) | 6.41  | 5.76  | 5.13  |

The  $\theta$  package to ambient value is made up of two primary components: the thermal resistance between the package and heatsink ( $\theta$  package to heatsink) and the thermal resistance between the heatsink and the ambient air around the part ( $\theta$  heatsink to air). A critical but controllable factor to decrease the value of  $\theta$  package to heatsink is management of the thermal interface between the package and heatsink. The other controllable factor ( $\theta$  heatsink to air) is determined by the design of the heatsink and airflow around the heatsink.

## 12.9 Mechanical Specifications

### 12.9.1 Pin Lists Sorted by Pin Number:

Table 12-23: MIOC Pin List Sorted by Pin

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| A01   | GND    |     | Power       |                 |                          |
| A02   | GND    |     | Power       |                 |                          |
| A03   | GND    |     | Power       |                 |                          |
| A04   | DBSY#  | I/O | AGTL+       | 55ma            |                          |
| A05   | A07#   | I/O | AGTL+       | 55ma            |                          |
| A06   | GND    |     | Power       |                 |                          |
| A07   | A13#   | I/O | AGTL+       | 55ma            |                          |
| A08   | VTT    |     | Power       |                 |                          |
| A09   | A20#   | I/O | AGTL+       | 55ma            |                          |
| A10   | GND    |     | Power       |                 |                          |
| A11   | GND    |     | Power       |                 |                          |
| A12   | A29#   | I/O | AGTL+       | 55ma            |                          |
| A13   | A34#   | I/O | AGTL+       |                 |                          |
| A14   | GND    |     | Power       |                 |                          |
| A15   | D01#   | I/O | AGTL+       | 55ma            |                          |
| A16   | GND    |     | Power       |                 |                          |
| A17   | CRES1  | I   | Analog      |                 |                          |
| A18   | D12#   | I/O | AGTL+       | 55ma            |                          |
| A19   | GND    |     | Power       |                 |                          |
| A20   | D19#   | I/O | AGTL+       | 55ma            |                          |
| A21   | D22#   | I/O | AGTL+       | 55ma            |                          |
| A22   | GND    |     | Power       |                 |                          |
| A23   | GND    |     | Power       |                 |                          |
| A24   | D32#   | I/O | AGTL+       | 55ma            |                          |
| A25   | VTT    |     | Power       |                 |                          |
| A26   | D38#   | I/O | AGTL+       | 55ma            |                          |
| A27   | GND    |     | Power       |                 |                          |
| A28   | D46#   | I/O | AGTL+       | 55ma            |                          |
| A29   | D49#   | I/O | AGTL+       | 55ma            |                          |
| A30   | VCC    |     | Power       |                 |                          |
| A31   | VCC    |     | Power       |                 |                          |
| A32   | VCC    |     | Power       |                 |                          |
| B01   | GND    |     | Power       |                 |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| B02   | GND    |     | Power       |                 |                          |
| B03   | RS0#   | I/O | AGTL+       | 55ma            |                          |
| B04   | A03#   | I/O | AGTL+       | 55ma            |                          |
| B05   | GND    |     | Power       |                 |                          |
| B06   | A10#   | I/O | AGTL+       | 55ma            |                          |
| B07   | A14#   | I/O | AGTL+       | 55ma            |                          |
| B08   | VTT    |     | Power       |                 |                          |
| B09   | A21#   | I/O | AGTL+       | 55ma            |                          |
| B10   | A24#   | I/O | AGTL+       | 55ma            |                          |
| B11   | A27#   | I/O | AGTL+       | 55ma            |                          |
| B12   | A30#   | I/O | AGTL+       | 55ma            |                          |
| B13   | A35#   | I/O | AGTL+       | 55ma            |                          |
| B14   | DRDY#  | I/O | AGTL+       | 55ma            |                          |
| B15   | D02#   | I/O | AGTL+       | 55ma            |                          |
| B16   | D06#   | I/O | AGTL+       | 55ma            |                          |
| B17   | D09#   | I/O | AGTL+       | 55ma            |                          |
| B18   | D13#   | I/O | AGTL+       | 55ma            |                          |
| B19   | D17#   | I/O | AGTL+       | 55ma            |                          |
| B20   | D20#   | I/O | AGTL+       | 55ma            |                          |
| B21   | D23#   | I/O | AGTL+       | 55ma            |                          |
| B22   | D27#   | I/O | AGTL+       | 55ma            |                          |
| B23   | D29#   | I/O | AGTL+       | 55ma            |                          |
| B24   | D33#   | I/O | AGTL+       | 55ma            |                          |
| B25   | VTT    |     | Power       |                 |                          |
| B26   | D39#   | I/O | AGTL+       | 55ma            |                          |
| B27   | D43#   | I/O | AGTL+       | 55ma            |                          |
| B28   | GND    |     | Power       |                 |                          |
| B29   | D50#   | I/O | AGTL+       | 55ma            |                          |
| B30   | D54#   | I/O | AGTL+       | 55ma            |                          |
| B31   | VCC    |     | Power       |                 |                          |
| B32   | VCC    |     | Power       |                 |                          |
| C01   | GND    |     | Power       |                 |                          |
| C02   | BNR#   | I/O | AGTL+       | 55ma            |                          |
| C03   | RS1#   | I/O | AGTL+       | 55ma            |                          |
| C04   | A04#   | I/O | AGTL+       | 55ma            |                          |
| C05   | A08#   | I/O | AGTL+       | 55ma            |                          |
| C06   | A11#   | I/O | AGTL+       | 55ma            |                          |
| C07   | A15#   | I/O | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| C08   | A18#   | I/O | AGTL+       | 55ma            |                          |
| C09   | A22#   | I/O | AGTL+       | 55ma            |                          |
| C10   | VCC    |     | Power       |                 |                          |
| C11   | CRES0  | I   | Analog      |                 |                          |
| C12   | A31#   | I/O | AGTL+       | 55ma            |                          |
| C13   | VCC    |     | Power       |                 |                          |
| C14   | VCC    |     | Power       |                 |                          |
| C15   | D03#   | I/O | AGTL+       | 55ma            |                          |
| C16   | VTT    |     | Power       |                 |                          |
| C17   | VTT    |     | Power       |                 |                          |
| C18   | D14#   | I/O | AGTL+       | 55ma            |                          |
| C19   | VCC    |     | Power       |                 |                          |
| C20   | VCC    |     | Power       |                 |                          |
| C21   | D24#   | I/O | AGTL+       | 55ma            |                          |
| C22   | VCC    |     | Power       |                 |                          |
| C23   | N/C    |     |             |                 |                          |
| C24   | D34#   | I/O | AGTL+       | 55ma            |                          |
| C25   | D36#   | I/O | AGTL+       | 55ma            |                          |
| C26   | D40#   | I/O | AGTL+       | 55ma            |                          |
| C27   | D44#   | I/O | AGTL+       | 55ma            |                          |
| C28   | D47#   | I/O | AGTL+       | 55ma            |                          |
| C29   | D51#   | I/O | AGTL+       | 55ma            |                          |
| C30   | D55#   | I/O | AGTL+       | 55ma            |                          |
| C31   | D57#   | I/O | AGTL+       | 55ma            |                          |
| C32   | VCC    |     | Power       |                 |                          |
| D01   | BPRI#  | I/O | AGTL+       | 55ma            |                          |
| D02   | TRDY#  | I/O | AGTL+       | 55ma            |                          |
| D03   | VTT    |     | Power       |                 |                          |
| D04   | A05#   | I/O | AGTL+       | 55ma            |                          |
| D05   | VTT    |     | Power       |                 |                          |
| D06   | A12#   | I/O | AGTL+       | 55ma            |                          |
| D07   | A16#   | I/O | AGTL+       | 55ma            |                          |
| D08   | GND    |     | Power       |                 |                          |
| D09   | A23#   | I/O | AGTL+       | 55ma            |                          |
| D10   | A25#   | I/O | AGTL+       | 55ma            |                          |
| D11   | A28#   | I/O | AGTL+       | 55ma            |                          |
| D12   | A32#   | I/O | AGTL+       | 55ma            |                          |
| D13   | BERR#  | I/O | AGTL+       | 55ma            |                          |

**Table 12-23: MIOC Pin List Sorted by Pin (Continued)**

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| D14   | D00#   | I/O | AGTL+       | 55ma            |                          |
| D15   | D04#   | I/O | AGTL+       | 55ma            |                          |
| D16   | D07#   | I/O | AGTL+       | 55ma            |                          |
| D17   | D10#   | I/O | AGTL+       | 55ma            |                          |
| D18   | D15#   | I/O | AGTL+       | 55ma            |                          |
| D19   | D18#   | I/O | AGTL+       | 55ma            |                          |
| D20   | D21#   | I/O | AGTL+       | 55ma            |                          |
| D21   | D25#   | I/O | AGTL+       | 55ma            |                          |
| D22   | D28#   | I/O | AGTL+       | 55ma            |                          |
| D23   | D30#   | I/O | AGTL+       | 55ma            |                          |
| D24   | D35#   | I/O | AGTL+       | 55ma            |                          |
| D25   | GND    |     | Power       |                 |                          |
| D26   | D41#   | I/O | AGTL+       | 55ma            |                          |
| D27   | D45#   | I/O | AGTL+       | 55ma            |                          |
| D28   | VTT    |     | Power       |                 |                          |
| D29   | D52#   | I/O | AGTL+       | 55ma            |                          |
| D30   | VTT    |     | Power       |                 |                          |
| D31   | D58#   | I/O | AGTL+       | 55ma            |                          |
| D32   | D60#   | I/O | AGTL+       | 55ma            |                          |
| E01   | REQ0#  | I/O | AGTL+       | 55ma            |                          |
| E02   | RSP#   | I/O | AGTL+       | 55ma            |                          |
| E03   | RS2#   | I/O | AGTL+       | 55ma            |                          |
| E04   | A06#   | I/O | AGTL+       | 55ma            |                          |
| E05   | A09#   | I/O | AGTL+       | 55ma            |                          |
| E06   | VCC    |     | Power       |                 |                          |
| E07   | A17#   | I/O | AGTL+       | 55ma            |                          |
| E08   | A19#   | I/O | AGTL+       | 55ma            |                          |
| E09   | GND    |     | Power       |                 |                          |
| E10   | A26#   | I/O | AGTL+       | 55ma            |                          |
| E11   | VTT    |     | Power       |                 |                          |
| E12   | A33#   | I/O | AGTL+       | 55ma            |                          |
| E13   | GND    |     | Power       |                 |                          |
| E14   | GND    |     | Power       |                 |                          |
| E15   | D05#   | I/O | AGTL+       | 55ma            |                          |
| E16   | D08#   | I/O | AGTL+       | 55ma            |                          |
| E17   | D11#   | I/O | AGTL+       | 55ma            |                          |
| E18   | D16#   | I/O | AGTL+       | 55ma            |                          |
| E19   | GND    |     | Power       |                 |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| E20   | GND    |     | Power       |                 |                          |
| E21   | D26#   | I/O | AGTL+       | 55ma            |                          |
| E22   | VTT    |     | Power       |                 |                          |
| E23   | D31#   | I/O | AGTL+       | 55ma            |                          |
| E24   | GND    |     | Power       |                 |                          |
| E25   | D37#   | I/O | AGTL+       | 55ma            |                          |
| E26   | D42#   | I/O | AGTL+       | 55ma            |                          |
| E27   | VCC    |     | Power       |                 |                          |
| E28   | D48#   | I/O | AGTL+       | 55ma            |                          |
| E29   | D53#   | I/O | AGTL+       | 55ma            |                          |
| E30   | D56#   | I/O | AGTL+       | 55ma            |                          |
| E31   | D59#   | I/O | AGTL+       | 55ma            |                          |
| E32   | D61#   | I/O | AGTL+       | 55ma            |                          |
| F01   | GND    |     | Power       |                 |                          |
| F02   | REQ4#  | I/O | AGTL+       | 55ma            |                          |
| F03   | LOCK#  | I   | AGTL+       |                 |                          |
| F04   | REQ1#  | I/O | AGTL+       | 55ma            |                          |
| F05   | VCC    |     | Power       |                 |                          |
| F28   | VCC    |     | Power       |                 |                          |
| F29   | D62#   | I/O | AGTL+       | 55ma            |                          |
| F30   | D63#   | I/O | AGTL+       | 55ma            |                          |
| F31   | DEP7#  | I/O | AGTL+       | 55ma            |                          |
| F32   | GND    |     | Power       |                 |                          |
| G01   | GND    |     | Power       |                 |                          |
| G02   | HIT#   | I   | AGTL+       |                 |                          |
| G03   | VTT    |     | Power       |                 |                          |
| G04   | REQ2#  | I/O | AGTL+       | 55ma            |                          |
| G05   | DEFER# | I/O | AGTL+       | 55ma            |                          |
| G28   | DEP6#  | I/O | AGTL+       | 55ma            |                          |
| G29   | DEP5#  | I/O | AGTL+       | 55ma            |                          |
| G30   | VTT    |     | Power       |                 |                          |
| G31   | DEP4#  | I/O | AGTL+       | 55ma            |                          |
| G32   | DEP3#  | I/O | AGTL+       | 55ma            |                          |
| H01   | AP0#   | I/O | AGTL+       | 55ma            |                          |
| H02   | HITM#  | I   | AGTL+       |                 |                          |
| H03   | VTT    |     | Power       |                 |                          |
| H04   | REQ3#  | I/O | AGTL+       | 55ma            |                          |
| H05   | GND    |     | Power       |                 |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|---------|-----|-------------|-----------------|--------------------------|
| H28   | GND     |     | Power       |                 |                          |
| H29   | CRESET# | O   | LVTTL       | 10ma            |                          |
| H30   | DEP2#   | I/O | AGTL+       | 55ma            |                          |
| H31   | DEP1#   | I/O | AGTL+       | 55ma            |                          |
| H32   | DEP0#   | I/O | AGTL+       | 55ma            |                          |
| J01   | AP1#    | I/O | AGTL+       | 55ma            |                          |
| J02   | BR0#    | O   | AGTL+       | 55ma            |                          |
| J03   | ADS#    | I/O | AGTL+       | 55ma            |                          |
| J04   | RP#     | I/O | AGTL+       | 55ma            |                          |
| J05   | GND     |     | Power       |                 |                          |
| J28   | X0CLKFB | I   | LVTTL       |                 |                          |
| J29   | BINIT#  | I/O | AGTL+       | 55ma            |                          |
| J30   | BP0#    | I/O | OD          | 14ma            |                          |
| J31   | BP1#    | I/O | OD          | 14ma            |                          |
| J32   | GND     |     | Power       |                 |                          |
| K01   | ERR0#   | I/O | OD          | 14ma            |                          |
| K02   | ERR1#   | I/O | OD          | 14ma            |                          |
| K03   | VCC     |     | Power       |                 |                          |
| K04   | VREF    | I   | Analog      |                 |                          |
| K05   | AERR#   | I/O | AGTL+       | 55ma            |                          |
| K28   | VCC     |     | Power       |                 |                          |
| K29   | N/C     |     |             |                 |                          |
| K30   | VCCA0   |     | Power       |                 |                          |
| K31   | VCCA1   |     | Power       |                 |                          |
| K32   | VCCA2   |     | Power       |                 |                          |
| L01   | GND     |     | Power       |                 |                          |
| L02   | TRST#   | I   | LVTTL       |                 |                          |
| L03   | TCK     | I   | LVTTL       |                 |                          |
| L04   | INTREQ# | O   | LVTTL       | 10ma            |                          |
| L05   | TMS     | I   | LVTTL       |                 |                          |
| L28   | X0CLK   | O   | LVTTL       | 10ma            |                          |
| L29   | X0CLKB  | O   | LVTTL       | 10ma            |                          |
| L30   | VCC     |     | Power       |                 |                          |
| L31   | PWRGD   | I   | LVTTL       |                 |                          |
| L32   | GND     |     | Power       |                 |                          |
| M01   | TPCTL0  | I   | LVTTL       |                 |                          |
| M02   | VCC     |     | Power       |                 |                          |
| M03   | TDO     | O   | OD          | 14ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| M04   | TDI      | I   | LVTTTL      |                 |                          |
| M05   | GND      |     | Power       |                 |                          |
| M28   | GND      |     | Power       |                 |                          |
| M29   | RESET#   | I/O | AGTL+       | 55ma            |                          |
| M30   | X1CLK    | O   | LVTTTL      | 10ma            |                          |
| M31   | X1CLKB   | O   | LVTTTL      | 10ma            |                          |
| M32   | X0RSTFB# | I   | AGTL+       |                 |                          |
| N01   | VCC      |     | Power       |                 |                          |
| N02   | TPCTL1   | I   | LVTTTL      |                 |                          |
| N03   | VTT      |     | Power       |                 |                          |
| N04   | IOREQ#   | O   | LVTTTL      | 10ma            |                          |
| N05   | IOGNT#   | I   | LVTTTL      |                 |                          |
| N28   | X1CLKFB  | I   | LVTTTL      |                 |                          |
| N29   | INIT#    | OD  | 2.5V        | 14ma            |                          |
| N30   | X0RSTB#  | O   | AGTL+       | 55ma            |                          |
| N31   | VREF     | I   | Analog      |                 |                          |
| N32   | VCC      |     | Power       |                 |                          |
| P01   | VCC      |     | Power       |                 |                          |
| P02   | MD00#    | I/O | AGTL+       | 55ma            |                          |
| P03   | MD01#    | I/O | AGTL+       | 55ma            |                          |
| P04   | MD02#    | I/O | AGTL+       | 55ma            |                          |
| P05   | VCC      |     | Power       |                 |                          |
| P28   | PWRGDB   | O   | LVTTTL      | 10ma            |                          |
| P29   | X0RST#   | O   | AGTL+       | 55ma            |                          |
| P30   | X0BE1#   | I/O | AGTL+       | 55ma            |                          |
| P31   | X0BE0#   | I/O | AGTL+       | 55ma            |                          |
| P32   | VCC      |     | Power       |                 |                          |
| R01   | GND      |     | Power       |                 |                          |
| R02   | MD03#    | I/O | AGTL+       | 55ma            |                          |
| R03   | MD04#    | I/O | AGTL+       | 55ma            |                          |
| R04   | VCC      |     | Power       |                 |                          |
| R05   | VCC      |     | Power       |                 |                          |
| R28   | HCLKIN   | I   | 2.5V        |                 |                          |
| R29   | GND      |     | Power       |                 |                          |
| R30   | X0ADS#   | I/O | AGTL+       | 55ma            |                          |
| R31   | X0PAR#   | I/O | AGTL+       | 55ma            |                          |
| R32   | X0BLK#   | O   | AGTL+       | 55ma            |                          |
| T01   | MD05#    | I/O | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| T02   | MD06#    | I/O | AGTL+       | 55ma            |                          |
| T03   | MD07#    | I/O | AGTL+       | 55ma            |                          |
| T04   | MD08#    | I/O | AGTL+       | 55ma            |                          |
| T05   | VCC      |     | Power       |                 |                          |
| T28   | GND      |     | Power       |                 |                          |
| T29   | X0D03#   | I/O | AGTL+       | 55ma            |                          |
| T30   | X0D02#   | I/O | AGTL+       | 55ma            |                          |
| T31   | X0D01#   | I/O | AGTL+       | 55ma            |                          |
| T32   | X0D00#   | I/O | AGTL+       | 55ma            |                          |
| U01   | DSTBP0#  | I/O | AGTL+       | 55ma            |                          |
| U02   | DSTBN0#  | I/O | AGTL+       | 55ma            |                          |
| U03   | MD09#    | I/O | AGTL+       | 55ma            |                          |
| U04   | GND      |     | Power       |                 |                          |
| U05   | GND      |     | Power       |                 |                          |
| U28   | N/C      |     |             |                 |                          |
| U29   | X0D04#   | I/O | AGTL+       | 55ma            |                          |
| U30   | VREF     | I   | Analog      |                 |                          |
| U31   | X0D05#   | I/O | AGTL+       | 55ma            |                          |
| U32   | GND      |     | Power       |                 |                          |
| V01   | VCC      |     | Power       |                 |                          |
| V02   | MD10#    | I/O | AGTL+       | 55ma            |                          |
| V03   | MD11#    | I/O | AGTL+       | 55ma            |                          |
| V04   | GND      |     | Power       |                 |                          |
| V05   | GND      |     | Power       |                 |                          |
| V28   | VCC      |     | Power       |                 |                          |
| V29   | VCC      |     | Power       |                 |                          |
| V30   | X0XSTBN# | I   | AGTL+       |                 |                          |
| V31   | X0XSTBP# | I   | AGTL+       |                 |                          |
| V32   | GND      |     | Power       |                 |                          |
| W01   | MD12#    | I/O | AGTL+       | 55ma            |                          |
| W02   | MD13#    | I/O | AGTL+       | 55ma            |                          |
| W03   | MD14#    | I/O | AGTL+       | 55ma            |                          |
| W04   | MD15#    | I/O | AGTL+       | 55ma            |                          |
| W05   | GND      |     | Power       |                 |                          |
| W28   | VCC      |     | Power       |                 |                          |
| W29   | X0XRTS#  | I   | AGTL+       |                 |                          |
| W30   | X0HRTS#  | O   | AGTL+       | 55ma            |                          |
| W31   | X0HSTBN# | O   | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| W32   | X0HSTBP# | O   | AGTL+       | 55ma            |                          |
| Y01   | VCC      |     | Power       |                 |                          |
| Y02   | MD16#    | I/O | AGTL+       | 55ma            |                          |
| Y03   | VTT      |     | Power       |                 |                          |
| Y04   | MD17#    | I/O | AGTL+       | 55ma            |                          |
| Y05   | MD18#    | I/O | AGTL+       | 55ma            |                          |
| Y28   | GND      |     | Power       |                 |                          |
| Y29   | X0D07#   | I/O | AGTL+       | 55ma            |                          |
| Y30   | VTT      |     | Power       |                 |                          |
| Y31   | X0D06#   | I/O | AGTL+       | 55ma            |                          |
| Y32   | VCC      |     | Power       |                 |                          |
| AA01  | MD19#    | I/O | AGTL+       | 55ma            |                          |
| AA02  | MD20#    | I/O | AGTL+       | 55ma            |                          |
| AA03  | MD21#    | I/O | AGTL+       | 55ma            |                          |
| AA04  | MD22#    | I/O | AGTL+       | 55ma            |                          |
| AA05  | GND      |     | Power       |                 |                          |
| AA28  | GND      |     | Power       |                 |                          |
| AA29  | X0D11#   | I/O | AGTL+       | 55ma            |                          |
| AA30  | X0D10#   | I/O | AGTL+       | 55ma            |                          |
| AA31  | X0D09#   | I/O | AGTL+       | 55ma            |                          |
| AA32  | X0D08#   | I/O | AGTL+       | 55ma            |                          |
| AB01  | GND      |     | Power       |                 |                          |
| AB02  | MD23#    | I/O | AGTL+       | 55ma            |                          |
| AB03  | VCC      |     | Power       |                 |                          |
| AB04  | MD24#    | I/O | AGTL+       | 55ma            |                          |
| AB05  | MD25#    | I/O | AGTL+       | 55ma            |                          |
| AB28  | X0D14#   | I/O | AGTL+       | 55ma            |                          |
| AB29  | X0D13#   | I/O | AGTL+       | 55ma            |                          |
| AB30  | VCC      |     | Power       |                 |                          |
| AB31  | X0D12#   | I/O | AGTL+       | 55ma            |                          |
| AB32  | GND      |     | Power       |                 |                          |
| AC01  | GND      |     | Power       |                 |                          |
| AC02  | MD26#    | I/O | AGTL+       | 55ma            |                          |
| AC03  | VREF     | I   | Analog      |                 |                          |
| AC04  | DSTBP1#  | I/O | AGTL+       | 55ma            |                          |
| AC05  | GND      |     | Power       |                 |                          |
| AC28  | GND      |     | Power       |                 |                          |
| AC29  | X1RST#   | O   | AGTL+       | 55ma            |                          |

**Table 12-23: MIOC Pin List Sorted by Pin (Continued)**

| Pin # | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|---------|-----|-------------|-----------------|--------------------------|
| AC30  | VCC     |     | Power       |                 |                          |
| AC31  | X0D15#  | I/O | AGTL+       | 55ma            |                          |
| AC32  | VCC     |     | Power       |                 |                          |
| AD01  | DSTBN1# | I/O | AGTL+       | 55ma            |                          |
| AD02  | MD27#   | I/O | AGTL+       | 55ma            |                          |
| AD03  | MD28#   | I/O | AGTL+       | 55ma            |                          |
| AD04  | MD29#   | I/O | AGTL+       | 55ma            |                          |
| AD05  | GND     |     | Power       |                 |                          |
| AD28  | GND     |     | Power       |                 |                          |
| AD29  | X1BE1#  | I/O | AGTL+       | 55ma            |                          |
| AD30  | X1BE0#  | I/O | AGTL+       | 55ma            |                          |
| AD31  | X1RSTB# | O   | AGTL+       | 55ma            |                          |
| AD32  | X1ADS#  | I/O | AGTL+       | 55ma            |                          |
| AE01  | GND     |     | Power       |                 |                          |
| AE02  | MD30#   | I/O | AGTL+       | 55ma            |                          |
| AE03  | VTT     |     | Power       |                 |                          |
| AE04  | MD31#   | I/O | AGTL+       | 55ma            |                          |
| AE05  | MD32#   | I/O | AGTL+       | 55ma            |                          |
| AE28  | X1BLK#  | O   | AGTL+       | 55ma            |                          |
| AE29  | X1D1#   | I/O | AGTL+       | 55ma            |                          |
| AE30  | VTT     |     | Power       |                 |                          |
| AE31  | X1D00#  | I/O | AGTL+       | 55ma            |                          |
| AE32  | GND     |     | Power       |                 |                          |
| AF01  | GND     |     | Power       |                 |                          |
| AF02  | MD33#   | I/O | AGTL+       | 55ma            |                          |
| AF03  | VTT     |     | Power       |                 |                          |
| AF04  | MD34#   | I/O | AGTL+       | 55ma            |                          |
| AF05  | MD35#   | I/O | AGTL+       | 55ma            |                          |
| AF28  | VCC     |     | Power       |                 |                          |
| AF29  | X1D03#  | I/O | AGTL+       | 55ma            |                          |
| AF30  | VTT     |     | Power       |                 |                          |
| AF31  | X1D02#  | I/O | AGTL+       | 55ma            |                          |
| AF32  | GND     |     | Power       |                 |                          |
| AG01  | MD36#   | I/O | AGTL+       | 55ma            |                          |
| AG02  | MD37#   | I/O | AGTL+       | 55ma            |                          |
| AG03  | MD38#   | I/O | AGTL+       | 55ma            |                          |
| AG04  | MD39#   | I/O | AGTL+       | 55ma            |                          |
| AG05  | VCC     |     | Power       |                 |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| AG28  | VCC      |     | Power       |                 |                          |
| AG29  | VREF     | I   | Analog      |                 |                          |
| AG30  | X1D05#   | I/O | AGTL+       | 55ma            |                          |
| AG31  | X1D04#   | I/O | AGTL+       | 55ma            |                          |
| AG32  | X1RSTFB# | I   | AGTL+       |                 |                          |
| AH01  | MD40#    | I/O | AGTL+       | 55ma            |                          |
| AH02  | MD41#    | I/O | AGTL+       | 55ma            |                          |
| AH03  | MD42#    | I/O | AGTL+       | 55ma            |                          |
| AH04  | MD43#    | I/O | AGTL+       | 55ma            |                          |
| AH05  | MD44#    | I/O | AGTL+       | 55ma            |                          |
| AH06  | VCC      |     | Power       |                 |                          |
| AH07  | MD57#    | I/O | AGTL+       | 55ma            |                          |
| AH08  | MD62#    | I/O | AGTL+       | 55ma            |                          |
| AH09  | DSTBN3#  | I/O | AGTL+       | 55ma            |                          |
| AH10  | VCC      |     | Power       |                 |                          |
| AH11  | VCC      |     | Power       |                 |                          |
| AH12  | DOFF0#   | O   | AGTL+       | 55ma            |                          |
| AH13  | GND      |     | Power       |                 |                          |
| AH14  | GND      |     | Power       |                 |                          |
| AH15  | DCMPLTB# | I/O | AGTL+       | 55ma            |                          |
| AH16  | ROW#     | O   | AGTL+       | 55ma            |                          |
| AH17  | VCC      |     | Power       |                 |                          |
| AH18  | BANK1#   | O   | AGTL+       | 55ma            |                          |
| AH19  | GND      |     | Power       |                 |                          |
| AH20  | GND      |     | Power       |                 |                          |
| AH21  | MA07#    | O   | AGTL+       | 55ma            |                          |
| AH22  | VTT      |     | Power       |                 |                          |
| AH23  | MA12#    | O   | AGTL+       | 55ma            |                          |
| AH24  | GND      |     | Power       |                 |                          |
| AH25  | GND      |     | Power       |                 |                          |
| AH26  | X1D14#   | I/O | AGTL+       | 55ma            |                          |
| AH27  | VCC      |     | Power       |                 |                          |
| AH28  | X1HSTBN# | O   | AGTL+       | 55ma            |                          |
| AH29  | X1HSTBP# | O   | AGTL+       | 55ma            |                          |
| AH30  | X1XSTBN# | I   | AGTL+       |                 |                          |
| AH31  | X1XSTBP# | I   | AGTL+       |                 |                          |
| AH32  | GND      |     | Power       |                 |                          |
| AJ01  | DSTBP2#  | I/O | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| AJ02  | DSTBN2#  | I/O | AGTL+       | 55ma            |                          |
| AJ03  | VTT      |     | Power       |                 |                          |
| AJ04  | MD45#    | I/O | AGTL+       | 55ma            |                          |
| AJ05  | VTT      |     | Power       |                 |                          |
| AJ06  | MD54#    | I/O | AGTL+       | 55ma            |                          |
| AJ07  | MD58#    | I/O | AGTL+       | 55ma            |                          |
| AJ08  | GND      |     | Power       |                 |                          |
| AJ09  | MD63#    | I/O | AGTL+       | 55ma            |                          |
| AJ10  | MD67#    | I/O | AGTL+       | 55ma            |                          |
| AJ11  | MD71#    | I/O | AGTL+       | 55ma            |                          |
| AJ12  | CMND1#   | O   | AGTL+       | 55ma            |                          |
| AJ13  | DSEL0#   | O   | AGTL+       | 55ma            |                          |
| AJ14  | WDEVT#   | O   | AGTL+       | 55ma            |                          |
| AJ15  | RCMPLTB# | I   | AGTL+       |                 |                          |
| AJ16  | DCMPLTA# | I/O | AGTL+       | 55ma            |                          |
| AJ17  | BANK0#   | O   | AGTL+       | 55ma            |                          |
| AJ18  | CARD1#   | O   | AGTL+       | 55ma            |                          |
| AJ19  | GND      |     | Power       |                 |                          |
| AJ20  | MA02#    | O   | AGTL+       | 55ma            |                          |
| AJ21  | MA06#    | O   | AGTL+       | 55ma            |                          |
| AJ22  | MA09#    | O   | AGTL+       | 55ma            |                          |
| AJ23  | MA11#    | O   | AGTL+       | 55ma            |                          |
| AJ24  | GND      |     | Power       |                 |                          |
| AJ25  | GND      |     | Power       |                 |                          |
| AJ26  | GND      |     | Power       |                 |                          |
| AJ27  | X1D13#   | I/O | AGTL+       | 55ma            |                          |
| AJ28  | VTT      |     | Power       |                 |                          |
| AJ29  | X1D06#   | I/O | AGTL+       | 55ma            |                          |
| AJ30  | VTT      |     | Power       |                 |                          |
| AJ31  | X1XRTS#  | I   | AGTL+       |                 |                          |
| AJ32  | X1HRTS#  | O   | AGTL+       | 55ma            |                          |
| AK01  | VCC      |     | Power       |                 |                          |
| AK02  | MD46#    | I/O | AGTL+       | 55ma            |                          |
| AK03  | MD47#    | I/O | AGTL+       | 55ma            |                          |
| AK04  | MD48#    | I/O | AGTL+       | 55ma            |                          |
| AK05  | MD49#    | I/O | AGTL+       | 55ma            |                          |
| AK06  | MD55#    | I/O | AGTL+       | 55ma            |                          |
| AK07  | MD59#    | I/O | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| AK08  | DSTBP3#  | I/O | AGTL+       | 55ma            |                          |
| AK09  | MD64#    | I/O | AGTL+       | 55ma            |                          |
| AK10  | MD68#    | I/O | AGTL+       | 55ma            |                          |
| AK11  | VCC      |     | Power       |                 |                          |
| AK12  | VCC      |     | Power       |                 |                          |
| AK13  | PHITA#   | I   | AGTL+       |                 |                          |
| AK14  | VCC      |     | Power       |                 |                          |
| AK15  | DVALIDA# | O   | AGTL+       | 55ma            |                          |
| AK16  | VTT      |     | Power       |                 |                          |
| AK17  | VTT      |     | Power       |                 |                          |
| AK18  | VCC      |     | Power       |                 |                          |
| AK19  | VCC      |     | Power       |                 |                          |
| AK20  | VCC      |     | Power       |                 |                          |
| AK21  | MA5#     | O   | AGTL+       | 55ma            |                          |
| AK22  | VCC      |     | Power       |                 |                          |
| AK23  | VCC      |     | Power       |                 |                          |
| AK24  | GND      |     | Power       |                 |                          |
| AK25  | GND      |     | Power       |                 |                          |
| AK26  | X1D15#   | I/O | AGTL+       | 55ma            |                          |
| AK27  | GND      |     | Power       |                 |                          |
| AK28  | X1D10#   | I/O | AGTL+       | 55ma            |                          |
| AK29  | X1D09#   | I/O | AGTL+       | 55ma            |                          |
| AK30  | X1D08#   | I/O | AGTL+       | 55ma            |                          |
| AK31  | X1D07#   | I/O | AGTL+       | 55ma            |                          |
| AK32  | GND      |     | Power       |                 |                          |
| AL01  | VCC      |     | Power       |                 |                          |
| AL02  | VCC      |     | Power       |                 |                          |
| AL03  | MD50#    | I/O | AGTL+       | 55ma            |                          |
| AL04  | MD51#    | I/O | AGTL+       | 55ma            |                          |
| AL05  | GND      |     | Power       |                 |                          |
| AL06  | MD56#    | I/O | AGTL+       | 55ma            |                          |
| AL07  | MD60#    | I/O | AGTL+       | 55ma            |                          |
| AL08  | VTT      |     | Power       |                 |                          |
| AL09  | MD65#    | I/O | AGTL+       | 55ma            |                          |
| AL10  | MD69#    | I/O | AGTL+       | 55ma            |                          |
| AL11  | CMND0#   | O   | AGTL+       | 55ma            |                          |
| AL12  | RHITA#   | I   | AGTL+       |                 |                          |
| AL13  | MRESET#  | O   | AGTL+       | 55ma            |                          |

Table 12-23: MIOC Pin List Sorted by Pin (Continued)

| Pin # | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|----------|-----|-------------|-----------------|--------------------------|
| AL14  | DSEL1#   | O   | AGTL+       | 55ma            |                          |
| AL15  | VREF     | I   | Analog      |                 |                          |
| AL16  | DVALIDB# | O   | AGTL+       | 55ma            |                          |
| AL17  | PHITB#   | I   | AGTL+       | 55ma            |                          |
| AL18  | CARD0#   | O   | AGTL+       | 55ma            |                          |
| AL19  | SMIACT#  | O   | LVTTTL      | 10ma            |                          |
| AL20  | MA01#    | O   | AGTL+       | 55ma            |                          |
| AL21  | MA04#    | O   | AGTL+       | 55ma            |                          |
| AL22  | MA08#    | O   | AGTL+       | 55ma            |                          |
| AL23  | MA10#    | O   | AGTL+       | 55ma            |                          |
| AL24  | VCC      |     | Power       |                 |                          |
| AL25  | VTT      |     | Power       |                 |                          |
| AL26  | VTT      |     | Power       |                 |                          |
| AL27  | GND      |     | Power       |                 |                          |
| AL28  | GND      |     | Power       |                 |                          |
| AL29  | X1D12#   | I/O | AGTL+       | 55ma            |                          |
| AL30  | X1D11#   | I/O | AGTL+       | 55ma            |                          |
| AL31  | GND      |     | Power       |                 |                          |
| AL32  | GND      |     | Power       |                 |                          |
| AM01  | VCC      |     | Power       |                 |                          |
| AM02  | VCC      |     | Power       |                 |                          |
| AM03  | VCC      |     | Power       |                 |                          |
| AM04  | MD52#    | I/O | AGTL+       | 55ma            |                          |
| AM05  | MD53#    | I/O | AGTL+       | 55ma            |                          |
| AM06  | GND      |     | Power       |                 |                          |
| AM07  | MD61#    | I/O | AGTL+       | 55ma            |                          |
| AM08  | VTT      |     | Power       |                 |                          |
| AM09  | MD66#    | I/O | AGTL+       | 55ma            |                          |
| AM10  | MD70#    | I/O | AGTL+       | 55ma            |                          |
| AM11  | GND      |     | Power       |                 |                          |
| AM12  | CSTB#    | O   | AGTL+       | 55ma            |                          |
| AM13  | DOFF1#   | O   | AGTL+       | 55ma            |                          |
| AM14  | GND      |     | Power       |                 |                          |
| AM15  | RCMPLTA# | I   | AGTL+       |                 |                          |
| AM16  | GND      |     | Power       |                 |                          |
| AM17  | RHITB#   | I   | AGTL+       |                 |                          |
| AM18  | BANK2#   | O   | AGTL+       | 55ma            |                          |
| AM19  | GND      |     | Power       |                 |                          |

**Table 12-23: MIOC Pin List Sorted by Pin (Continued)**

| Pin # | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|-------|--------|-----|-------------|-----------------|--------------------------|
| AM20  | MA00#  | O   | AGTL+       | 55ma            |                          |
| AM21  | MA03#  | O   | AGTL+       | 55ma            |                          |
| AM22  | GND    |     | Power       |                 |                          |
| AM23  | GND    |     | Power       |                 |                          |
| AM24  | MA13#  | O   | AGTL+       | 55ma            |                          |
| AM25  | VTT    |     | Power       |                 |                          |
| AM26  | VTT    |     | Power       |                 |                          |
| AM27  | GND    |     | Power       |                 |                          |
| AM28  | GND    |     | Power       |                 |                          |
| AM29  | X1PAR# | I/O | AGTL+       | 55ma            |                          |
| AM30  | GND    |     | Power       |                 |                          |
| AM31  | GND    |     | Power       |                 |                          |
| AM32  | GND    |     | Power       |                 |                          |

**Table 12-24: PXB Pinlist Sorted by Pin**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| A01  | N/C     |     |             |                 |                          |
| A02  | N/C     |     |             |                 |                          |
| A03  | VCC     |     | Power       |                 |                          |
| A04  | VCC     |     | Power       |                 |                          |
| A05  | VCC     |     | Power       |                 |                          |
| A06  | VCC     |     | Power       |                 |                          |
| A07  | VCC     |     | Power       |                 |                          |
| A08  | VCC     |     | Power       |                 |                          |
| A09  | VCC     |     | Power       |                 |                          |
| A10  | VCC     |     | Power       |                 |                          |
| A11  | N/C     |     |             |                 |                          |
| A12  | VREF    | I   | Analog      |                 |                          |
| A13  | N/C     |     |             |                 |                          |
| A14  | VCC     |     | Power       |                 |                          |
| A15  | XD[10]# | I/O | AGTL+       | 55ma            |                          |
| A16  | VCC     |     | Power       |                 |                          |
| A17  | XHSTBN# | I   | AGTL+       |                 |                          |
| A18  | VCC     |     | Power       |                 |                          |
| A19  | XD[04]# | I/O | AGTL+       | 55ma            |                          |
| A20  | VCC     |     | Power       |                 |                          |
| A21  | XBLK#   | I   | AGTL+       |                 |                          |
| A22  | VCC     |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| A23  | N/C      |     |             |                 |                          |
| A24  | VREF     | I   | Analog      |                 |                          |
| A25  | N/C      |     |             |                 |                          |
| A26  | VCC      |     | Power       |                 |                          |
| A27  | VCCA0    |     | Power       |                 |                          |
| A28  | VCC      |     | Power       |                 |                          |
| A29  | VCC      |     | Power       |                 |                          |
| A30  | N/C      |     |             |                 |                          |
| A31  | N/C      |     |             |                 |                          |
| A32  | N/C      |     |             |                 |                          |
| B01  | N/C      |     |             |                 |                          |
| B02  | VCC      |     | Power       |                 |                          |
| B03  | VCC      |     | Power       |                 |                          |
| B04  | VCC      |     | Power       |                 |                          |
| B05  | N/C      |     |             |                 |                          |
| B06  | N/C      |     |             |                 |                          |
| B07  | N/C      |     |             |                 |                          |
| B08  | N/C      |     |             |                 |                          |
| B09  | N/C      |     |             |                 |                          |
| B10  | N/C      |     |             |                 |                          |
| B11  | N/C      |     |             |                 |                          |
| B12  | N/C      |     |             |                 |                          |
| B13  | N/C      |     |             |                 |                          |
| B14  | XD[15]#  | I/O | AGTL+       | 55ma            |                          |
| B15  | XD[11]#  | I/O | AGTL+       | 55ma            |                          |
| B16  | XD[08]#  | I/O | AGTL+       | 55ma            |                          |
| B17  | N/C      |     |             |                 |                          |
| B18  | XHRTS#   | I   | AGTL+       |                 |                          |
| B19  | XD[05]#  | I/O | AGTL+       | 55ma            |                          |
| B20  | XD[02]#  | I/O | AGTL+       | 55ma            |                          |
| B21  | XPAR#    | I/O | AGTL+       | 55ma            |                          |
| B22  | XBE[01]# | I/O | AGTL+       | 55ma            |                          |
| B23  | N/C      |     |             |                 |                          |
| B24  | N/C      |     |             |                 |                          |
| B25  | N/C      |     |             |                 |                          |
| B26  | N/C      |     |             |                 |                          |
| B27  | N/C      |     |             |                 |                          |
| B28  | VCC      |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| B29  | VCC     |     | Power       |                 |                          |
| B30  | VCC     |     | Power       |                 |                          |
| B31  | VCC     |     | Power       |                 |                          |
| B32  | N/C     |     |             |                 |                          |
| C01  | N/C     |     |             |                 |                          |
| C02  | N/C     |     |             |                 |                          |
| C03  | N/C     |     |             |                 |                          |
| C04  | N/C     |     |             |                 |                          |
| C05  | N/C     |     |             |                 |                          |
| C06  | GND     |     | Power       |                 |                          |
| C07  | GND     |     | Power       |                 |                          |
| C08  | GND     |     | Power       |                 |                          |
| C09  | N/C     |     |             |                 |                          |
| C10  | GND     |     | Power       |                 |                          |
| C11  | N/C     |     |             |                 |                          |
| C12  | GND     |     | Power       |                 |                          |
| C13  | N/C     |     |             |                 |                          |
| C14  | GND     |     | Power       |                 |                          |
| C15  | XD[12]# | I/O | AGTL+       | 55ma            |                          |
| C16  | GND     |     | Power       |                 |                          |
| C17  | XHSTBP# | I   | AGTL+       |                 |                          |
| C18  | GND     |     | Power       |                 |                          |
| C19  | XXSTBN# | O   | AGTL+       | 55ma            |                          |
| C20  | GND     |     | Power       |                 |                          |
| C21  | XADS#   | I/O | AGTL+       | 55ma            |                          |
| C22  | GND     |     | Power       |                 |                          |
| C23  | N/C     |     |             |                 |                          |
| C24  | GND     |     | Power       |                 |                          |
| C25  | XCLK    | I   | LVTTL       |                 |                          |
| C26  | GND     |     | Power       |                 |                          |
| C27  | VCCA1   |     | Power       |                 |                          |
| C28  | N/C     |     |             |                 |                          |
| C29  | N/C     |     |             |                 |                          |
| C30  | N/C     |     |             |                 |                          |
| C31  | N/C     |     |             |                 |                          |
| C32  | N/C     |     |             |                 |                          |
| D01  | N/C     |     |             |                 |                          |
| D02  | GND     |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| D03  | N/C     |     |             |                 |                          |
| D04  | VTT     |     | Power       |                 |                          |
| D05  | N/C     |     |             |                 |                          |
| D06  | N/C     |     |             |                 |                          |
| D07  | N/C     |     |             |                 |                          |
| D08  | N/C     |     |             |                 |                          |
| D09  | CRES1   | I   | Analog      |                 |                          |
| D10  | N/C     |     |             |                 |                          |
| D11  | N/C     |     |             |                 |                          |
| D12  | N/C     |     |             |                 |                          |
| D13  | N/C     |     |             |                 |                          |
| D14  | N/C     |     |             |                 |                          |
| D15  | XD[13]# | I/O | AGTL+       | 55ma            |                          |
| D16  | XD[09]# | I/O | AGTL+       | 55ma            |                          |
| D17  | XD[06]# | I/O | AGTL+       | 55ma            |                          |
| D18  | XXRTS#  | O   | AGTL+       | 55ma            |                          |
| D19  | N/C     |     |             |                 |                          |
| D20  | XD[03]# | I/O | AGTL+       | 55ma            |                          |
| D21  | XD[00]# | I/O | AGTL+       | 55ma            |                          |
| D22  | XRST#   | I   | AGTL+       |                 |                          |
| D23  | N/C     |     |             |                 |                          |
| D24  | N/C     |     |             |                 |                          |
| D25  | N/C     |     |             |                 |                          |
| D26  | N/C     |     |             |                 |                          |
| D27  | VCC     |     | Power       |                 |                          |
| D28  | VTT     |     | Power       |                 |                          |
| D29  | PWRGD   | I   | LVTTL       |                 |                          |
| D30  | N/C     |     |             |                 |                          |
| D31  | GND     |     | Power       |                 |                          |
| D32  | N/C     |     |             |                 |                          |
| E01  | N/C     |     |             |                 |                          |
| E02  | N/C     |     |             |                 |                          |
| E03  | N/C     |     |             |                 |                          |
| E04  | N/C     |     |             |                 |                          |
| E05  | N/C     |     |             |                 |                          |
| E06  | VTT     |     | Power       |                 |                          |
| E07  | N/C     |     |             |                 |                          |
| E08  | VTT     |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| E09  | CRES0    | I   | Analog      |                 |                          |
| E10  | VTT      |     | Power       |                 |                          |
| E11  | N/C      |     |             |                 |                          |
| E12  | VTT      |     | Power       |                 |                          |
| E13  | XIB      | O   | AGTL+       | 55ma            |                          |
| E14  | VTT      |     | Power       |                 |                          |
| E15  | XD[14]#  | I/O | AGTL+       | 55ma            |                          |
| E16  | VTT      |     | Power       |                 |                          |
| E17  | XD[07]#  | I/O | AGTL+       | 55ma            |                          |
| E18  | VTT      |     | Power       |                 |                          |
| E19  | XXSTBP#  | O   | AGTL+       | 55ma            |                          |
| E20  | VTT      |     | Power       |                 |                          |
| E21  | XD[01]#  | I/O | AGTL+       | 55ma            |                          |
| E22  | VTT      |     | Power       |                 |                          |
| E23  | XBE[00]# | I/O | AGTL+       | 55ma            |                          |
| E24  | VTT      |     | Power       |                 |                          |
| E25  | N/C      |     |             |                 |                          |
| E26  | VTT      |     | Power       |                 |                          |
| E27  | VCCA2    |     | Power       |                 |                          |
| E28  | N/C      |     |             |                 |                          |
| E29  | N/C      |     |             |                 |                          |
| E30  | N/C      |     |             |                 |                          |
| E31  | N/C      |     |             |                 |                          |
| E32  | N/C      |     |             |                 |                          |
| F01  | GND      |     | Power       |                 |                          |
| F02  | N/C      |     |             |                 |                          |
| F03  | VCC      |     | Power       |                 |                          |
| F04  | N/C      |     |             |                 |                          |
| F05  | GND      |     | Power       |                 |                          |
| F28  | GND      |     | Power       |                 |                          |
| F29  | PIIXOK#  | I   | LVTTL       |                 |                          |
| F30  | N/C      |     |             |                 |                          |
| F31  | N/C      |     |             |                 |                          |
| F32  | N/C      |     |             |                 |                          |
| G01  | N/C      |     |             |                 |                          |
| G02  | N/C      |     |             |                 |                          |
| G03  | N/C      |     |             |                 |                          |
| G04  | N/C      |     |             |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| G05  | N/C     |     |             |                 |                          |
| G28  | N/C     |     |             |                 |                          |
| G29  | N/C     |     |             |                 |                          |
| G30  | VCC     |     | Power       |                 |                          |
| G31  | VCC     |     | Power       |                 |                          |
| G32  | N/C     |     |             |                 |                          |
| H01  | VCC     |     | Power       |                 |                          |
| H02  | N/C     |     |             |                 |                          |
| H03  | GND     |     | Power       |                 |                          |
| H04  | N/C     |     |             |                 |                          |
| H05  | VCC     |     | Power       |                 |                          |
| H28  | N/C     |     |             |                 |                          |
| H29  | N/C     |     |             |                 |                          |
| H30  | GND     |     | Power       |                 |                          |
| H31  | N/C     |     |             |                 |                          |
| H32  | N/C     |     |             |                 |                          |
| J01  | N/C     |     |             |                 |                          |
| J02  | N/C     |     |             |                 |                          |
| J03  | N/C     |     |             |                 |                          |
| J04  | N/C     |     |             |                 |                          |
| J05  | N/C     |     |             |                 |                          |
| J28  | N/C     |     |             |                 |                          |
| J29  | N/C     |     |             |                 |                          |
| J30  | PBCLKFB | I   | LVTTTL      |                 |                          |
| J31  | N/C     |     |             |                 |                          |
| J32  | PACLKFB | I   | LVTTTL      |                 |                          |
| K01  | GND     |     | Power       |                 |                          |
| K02  | N/C     |     |             |                 |                          |
| K03  | VCC     |     | Power       |                 |                          |
| K04  | N/C     |     |             |                 |                          |
| K05  | GND     |     | Power       |                 |                          |
| K28  | GND     |     | Power       |                 |                          |
| K29  | N/C     |     |             |                 |                          |
| K30  | VCC     |     | Power       |                 |                          |
| K31  | N/C     |     |             |                 |                          |
| K32  | GND     |     | Power       |                 |                          |
| L01  | GND     |     | Power       |                 |                          |
| L02  | GND     |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| L03  | GND    |     | Power       |                 |                          |
| L04  | GND    |     | Power       |                 |                          |
| L05  | GND    |     | Power       |                 |                          |
| L28  | N/C    |     |             |                 |                          |
| L29  | N/C    |     |             |                 |                          |
| L30  | PBCLK  | O   | LVTTTL      | 10ma            |                          |
| L31  | N/C    |     |             |                 |                          |
| L32  | PACLK  | O   | LVTTTL      | 10ma            |                          |
| M01  | VCC    |     | Power       |                 |                          |
| M02  | N/C    |     |             |                 |                          |
| M03  | GND    |     | Power       |                 |                          |
| M04  | TCK    | I   | 2.5V        |                 |                          |
| M05  | VCC    |     | Power       |                 |                          |
| M28  | VCC    |     | Power       |                 |                          |
| M29  | N/C    |     |             |                 |                          |
| M30  | GND    |     | Power       |                 |                          |
| M31  | N/C    |     |             |                 |                          |
| M32  | VCC    |     | Power       |                 |                          |
| N01  | TDI    | I   | 2.5V        |                 |                          |
| N02  | TDO    | O   | OD          | 14ma            |                          |
| N03  | VCC    |     | Power       |                 |                          |
| N04  | TMS    | I   | 2.5V        |                 |                          |
| N05  | TRST#  | I   | 2.5V        |                 |                          |
| N28  | N/C    |     |             |                 |                          |
| N29  | N/C    |     |             |                 |                          |
| N30  | N/C    |     |             |                 |                          |
| N31  | N/C    |     |             |                 |                          |
| N32  | N/C    |     |             |                 |                          |
| P01  | VCC    |     | Power       |                 |                          |
| P02  | N/C    |     |             |                 |                          |
| P03  | GND    |     | Power       |                 |                          |
| P04  | N/C    |     |             |                 |                          |
| P05  | VCC    |     | Power       |                 |                          |
| P28  | GND    |     | Power       |                 |                          |
| P29  | N/C    |     |             |                 |                          |
| P30  | VCC    |     | Power       |                 |                          |
| P31  | N/C    |     |             |                 |                          |
| P32  | GND    |     | Power       |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| R01  | VCC    |     | Power       |                 |                          |
| R02  | N/C    |     |             |                 |                          |
| R03  | GND    |     | Power       |                 |                          |
| R04  | N/C    |     |             |                 |                          |
| R05  | VCC    |     | Power       |                 |                          |
| R28  | GND    |     | Power       |                 |                          |
| R29  | N/C    |     |             |                 |                          |
| R30  | VCC    |     | Power       |                 |                          |
| R31  | N/C    |     |             |                 |                          |
| R32  | GND    |     | Power       |                 |                          |
| T01  | VCC    |     | Power       |                 |                          |
| T02  | N/C    |     |             |                 |                          |
| T03  | GND    |     | Power       |                 |                          |
| T04  | N/C    |     |             |                 |                          |
| T05  | VCC    |     | Power       |                 |                          |
| T28  | GND    |     | Power       |                 |                          |
| T29  | N/C    |     |             |                 |                          |
| T30  | VCC    |     | Power       |                 |                          |
| T31  | N/C    |     |             |                 |                          |
| T32  | GND    |     | Power       |                 |                          |
| U01  | N/C    |     |             |                 |                          |
| U02  | N/C    |     |             |                 |                          |
| U03  | N/C    |     |             |                 |                          |
| U04  | N/C    |     |             |                 |                          |
| U05  | N/C    |     |             |                 |                          |
| U28  | N/C    |     |             |                 |                          |
| U29  | N/C    |     |             |                 |                          |
| U30  | VCC    |     | Power       |                 |                          |
| U31  | N/C    |     |             |                 |                          |
| U32  | GND    |     | Power       |                 |                          |
| V01  | GND    |     | Power       |                 |                          |
| V02  | N/C    |     |             |                 |                          |
| V03  | VCC5A  | I   | Power (PCI) |                 |                          |
| V04  | N/C    |     |             |                 |                          |
| V05  | GND    |     | Power       |                 |                          |
| V28  | VCC    |     | Power       |                 |                          |
| V29  | N/C    |     |             |                 |                          |
| V30  | VCC5N  |     | Power (PCI) |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| V31  | N/C      |     |             |                 |                          |
| V32  | GND      |     | Power       |                 |                          |
| W01  | PBAD[31] | I/O | PCI         |                 |                          |
| W02  | PBAD[30] | I/O | PCI         |                 |                          |
| W03  | PBAD[29] | I/O | PCI         |                 |                          |
| W04  | PBAD[28] | I/O | PCI         |                 |                          |
| W05  | GND      |     | Power       |                 |                          |
| W28  | VCC      |     | Power       |                 |                          |
| W29  | PAAD[28] | I/O | PCI         |                 |                          |
| W30  | PAAD[29] | I/O | PCI         |                 |                          |
| W31  | PAAD[30] | I/O | PCI         |                 |                          |
| W32  | PAAD[31] | I/O | PCI         |                 |                          |
| Y01  | VCC      |     | Power       |                 |                          |
| Y02  | PBAD[27] | I/O | PCI         |                 |                          |
| Y03  | GND      |     | Power       |                 |                          |
| Y04  | PBAD[26] | I/O | PCI         |                 |                          |
| Y05  | VCC      |     | Power       |                 |                          |
| Y28  | VCC      |     | Power       |                 |                          |
| Y29  | PAAD[26] | I/O | PCI         |                 |                          |
| Y30  | GND      |     | Power       |                 |                          |
| Y31  | PAAD[27] | I/O | PCI         |                 |                          |
| Y32  | VCC      |     | Power       |                 |                          |
| AA1  | PBAD[25] | I/O | PCI         |                 |                          |
| AA2  | PBAD[24] | I/O | PCI         |                 |                          |
| AA3  | PBAD[23] | I/O | PCI         |                 |                          |
| AA4  | PBAD[22] | I/O | PCI         |                 |                          |
| AA5  | PBAD[21] | I/O | PCI         |                 |                          |
| AA28 | PAAD[21] | I/O | PCI         |                 |                          |
| AA29 | PAAD[22] | I/O | PCI         |                 |                          |
| AA30 | PAAD[23] | I/O | PCI         |                 |                          |
| AA31 | PAAD[24] | I/O | PCI         |                 |                          |
| AA32 | PAAD[25] | I/O | PCI         |                 |                          |
| AB01 | GND      |     | Power       |                 |                          |
| AB02 | PBAD[20] | I/O | PCI         |                 |                          |
| AB03 | VCC5B    |     | Power (PCI) |                 |                          |
| AB04 | PBAD[19] | I/O | PCI         |                 |                          |
| AB05 | GND      |     | Power       |                 |                          |
| AB28 | GND      |     | Power       |                 |                          |

**Table 12-24: PXB Pinlist Sorted by Pin (Continued)**

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| AB29 | PAAD[19] | I/O | PCI         |                 |                          |
| AB30 | VCC5M    |     | Power (PCI) |                 |                          |
| AB31 | PAAD[20] | I/O | PCI         |                 |                          |
| AB32 | GND      |     | Power       |                 |                          |
| AC01 | PBAD[18] | I/O | PCI         |                 |                          |
| AC02 | PBAD[17] | I/O | PCI         |                 |                          |
| AC03 | PBAD[16] | I/O | PCI         |                 |                          |
| AC04 | PBAD[15] | I/O | PCI         |                 |                          |
| AC05 | PBAD[14] | I/O | PCI         |                 |                          |
| AC28 | PAAD[14] | I/O | PCI         |                 |                          |
| AC29 | PAAD[15] | I/O | PCI         |                 |                          |
| AC30 | PAAD[16] | I/O | PCI         |                 |                          |
| AC31 | PAAD[17] | I/O | PCI         |                 |                          |
| AC32 | PAAD[18] | I/O | PCI         |                 |                          |
| AD01 | VCC      |     | Power       |                 |                          |
| AD02 | PBAD[13] | I/O | PCI         |                 |                          |
| AD03 | GND      |     | Power       |                 |                          |
| AD04 | PBAD[12] | I/O | PCI         |                 |                          |
| AD05 | VCC      |     | Power       |                 |                          |
| AD28 | VCC      |     | Power       |                 |                          |
| AD29 | PAAD[12] | I/O | PCI         |                 |                          |
| AD30 | GND      |     | Power       |                 |                          |
| AD31 | PAAD[13] | I/O | PCI         |                 |                          |
| AD32 | VCC      |     | Power       |                 |                          |
| AE01 | PBAD[11] | I/O | PCI         |                 |                          |
| AE02 | PBAD[10] | I/O | PCI         |                 |                          |
| AE03 | PBAD[09] | I/O | PCI         |                 |                          |
| AE04 | PBAD[08] | I/O | PCI         |                 |                          |
| AE05 | PBAD[07] | I/O | PCI         |                 |                          |
| AE28 | PAAD[07] | I/O | PCI         |                 |                          |
| AE29 | PAAD[08] | I/O | PCI         |                 |                          |
| AE30 | PAAD[09] | I/O | PCI         |                 |                          |
| AE31 | PAAD[10] | I/O | PCI         |                 |                          |
| AE32 | PAAD[11] | I/O | PCI         |                 |                          |
| AF01 | GND      |     | Power       |                 |                          |
| AF02 | PBAD[06] | I/O | PCI         |                 |                          |
| AF03 | VCC5C    |     | Power (PCI) |                 |                          |
| AF04 | PBAD[05] | I/O | PCI         |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal     | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|------------|-----|-------------|-----------------|--------------------------|
| AF05 | GND        |     | Power       |                 |                          |
| AF28 | GND        |     | Power       |                 |                          |
| AF29 | PAAD[05]   | I/O | PCI         |                 |                          |
| AF30 | VCC5L      |     | Power (PCI) |                 |                          |
| AF31 | PAAD[06]   | I/O | PCI         |                 |                          |
| AF32 | GND        |     | Power       |                 |                          |
| AG01 | PBAD[04]   | I/O | PCI         |                 |                          |
| AG02 | PBAD[03]   | I/O | PCI         |                 |                          |
| AG03 | PBAD[02]   | I/O | PCI         |                 |                          |
| AG04 | PBAD[01]   | I/O | PCI         |                 |                          |
| AG05 | PBAD[00]   | I/O | PCI         |                 |                          |
| AG28 | PAAD[00]   | I/O | PCI         |                 |                          |
| AG29 | PAAD[01]   | I/O | PCI         |                 |                          |
| AG30 | PAAD[02]   | I/O | PCI         |                 |                          |
| AG31 | PAAD[03]   | I/O | PCI         |                 |                          |
| AG32 | PAAD[04]   | I/O | PCI         |                 |                          |
| AH01 | N/C        |     |             |                 |                          |
| AH02 | N/C        |     |             |                 |                          |
| AH03 | VCC5D      |     | Power (PCI) |                 |                          |
| AH04 | VCC        |     | Power       |                 |                          |
| AH05 | N/C        |     |             |                 |                          |
| AH06 | N/C        |     |             |                 |                          |
| AH07 | GND        |     | Power       |                 |                          |
| AH08 | PBMON[01]# | I/O | LVTTTL      | 10ma            |                          |
| AH09 | VCC        |     | Power       |                 |                          |
| AH10 | PBGNT[02]# | O   | PCI         |                 |                          |
| AH11 | GND        |     | Power       |                 |                          |
| AH12 | PBREQ[01]# | I   | PCI         |                 |                          |
| AH13 | VCC        |     | Power       |                 |                          |
| AH14 | PBDEVSEL#  | I/O | PCI         |                 |                          |
| AH15 | GND        |     | Power       |                 |                          |
| AH16 | PBCBE[00]# | I/O | PCI         |                 |                          |
| AH17 | VCC        |     | Power       |                 |                          |
| AH18 | PACBE[00]# | I/O | PCI         |                 |                          |
| AH19 | GND        |     | Power       |                 |                          |
| AH20 | PADEVSEL#  | I/O | PCI         |                 |                          |
| AH21 | VCC        |     | Power       |                 |                          |
| AH22 | PAREQ[01]# | I   | PCI         |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal     | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|------------|-----|-------------|-----------------|--------------------------|
| AH23 | GND        |     | Power       |                 |                          |
| AH24 | PAGNT[02]# | O   | PCI         |                 |                          |
| AH25 | VCC        |     | Power       |                 |                          |
| AH26 | PAMON[01]# | I/O | LVTTTL      | 10ma            |                          |
| AH27 | GND        |     | Power       |                 |                          |
| AH28 | N/C        |     |             |                 |                          |
| AH29 | VCC        |     | Power       |                 |                          |
| AH30 | VCC5K      |     | Power (PCI) |                 |                          |
| AH31 | N/C        |     |             |                 |                          |
| AH32 | N/C        |     |             |                 |                          |
| AJ01 | N/C        |     |             |                 |                          |
| AJ02 | N/C        |     |             |                 |                          |
| AJ03 | N/C        |     |             |                 |                          |
| AJ04 | VCC        |     | Power       |                 |                          |
| AJ05 | N/C        |     |             |                 |                          |
| AJ06 | N/C        |     |             |                 |                          |
| AJ07 | PBXARB#    | I   | PCI         |                 |                          |
| AJ08 | N/C        |     |             |                 |                          |
| AJ09 | PBRST#     | O   | PCI         |                 |                          |
| AJ10 | PBGNT[03]# | O   | PCI         |                 |                          |
| AJ11 | PBGNT[00]# | O   | PCI         |                 |                          |
| AJ12 | PBREQ[02]# | I   | PCI         |                 |                          |
| AJ13 | PBCBE[03]# | I/O | PCI         |                 |                          |
| AJ14 | PBTRDY#    | I/O | PCI         |                 |                          |
| AJ15 | PBLOCK#    | I/O | PCI         |                 |                          |
| AJ16 | PBCBE[01]# | I/O | PCI         |                 |                          |
| AJ17 | REQ64#     | I/O | PCI         |                 |                          |
| AJ18 | PACBE[01]# | I/O | PCI         |                 |                          |
| AJ19 | PALOCK#    | I/O | PCI         |                 |                          |
| AJ20 | PATRDY#    | I/O | PCI         |                 |                          |
| AJ21 | PACBE[03]# | I/O | PCI         |                 |                          |
| AJ22 | PAREQ[02]# | I   | PCI         |                 |                          |
| AJ23 | PAGNT[00]# | O   | PCI         |                 |                          |
| AJ24 | PAGNT[03]# | O   | PCI         |                 |                          |
| AJ25 | PARST#     | O   | PCI         |                 |                          |
| AJ26 | MODE64#    | I   | PCI         |                 |                          |
| AJ27 | PAXARB#    | I   | PCI         |                 |                          |
| AJ28 | N/C        |     |             |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal     | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|------------|-----|-------------|-----------------|--------------------------|
| AJ29 | VCC        |     | Power       |                 |                          |
| AJ30 | N/C        |     |             |                 |                          |
| AJ31 | N/C        |     |             |                 |                          |
| AJ32 | N/C        |     |             |                 |                          |
| AK01 | N/C        |     |             |                 |                          |
| AK02 | GND        |     | Power       |                 |                          |
| AK03 | N/C        |     |             |                 |                          |
| AK04 | VCC5E      |     | Power (PCI) |                 |                          |
| AK05 | N/C        |     |             |                 |                          |
| AK06 | N/C        |     |             |                 |                          |
| AK07 | VCC        |     | Power       |                 |                          |
| AK08 | N/C        |     |             |                 |                          |
| AK09 | GND        |     | Power       |                 |                          |
| AK10 | PBGNT[04]# | O   | PCI         |                 |                          |
| AK11 | VCC5F      |     | Power (PCI) |                 |                          |
| AK12 | PBREQ[03]# | I   | PCI         |                 |                          |
| AK13 | GND        |     | Power       |                 |                          |
| AK14 | PBIRDY#    | I/O | PCI         |                 |                          |
| AK15 | VCC5G      |     | Power (PCI) |                 |                          |
| AK16 | PBPAR      | I/O | PCI         |                 |                          |
| AK17 | GND        |     | Power       |                 |                          |
| AK18 | PAPAR      | I/O | PCI         |                 |                          |
| AK19 | VCC5H      |     | Power (PCI) |                 |                          |
| AK20 | PAIRDY#    | I/O | PCI         |                 |                          |
| AK21 | GND        |     | Power       |                 |                          |
| AK22 | PAREQ[03]# | I   | PCI         |                 |                          |
| AK23 | VCC5I      |     | Power (PCI) |                 |                          |
| AK24 | PAGNT[04]# | O   | PCI         |                 |                          |
| AK25 | GND        |     | Power       |                 |                          |
| AK26 | PHOLD#     | I   | PCI         |                 |                          |
| AK27 | VCC        |     | Power       |                 |                          |
| AK28 | N/C        |     |             |                 |                          |
| AK29 | VCC5J      |     | Power (PCI) |                 |                          |
| AK30 | N/C        |     |             |                 |                          |
| AK31 | GND        |     | Power       |                 |                          |
| AK32 | N/C        |     |             |                 |                          |
| AL01 | N/C        |     |             |                 |                          |
| AL02 | N/C        |     |             |                 |                          |

Table 12-24: PXB Pinlist Sorted by Pin (Continued)

| PIN# | Signal     | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|------------|-----|-------------|-----------------|--------------------------|
| AL03 | N/C        |     |             |                 |                          |
| AL04 | N/C        |     |             |                 |                          |
| AL05 | N/C        |     |             |                 |                          |
| AL06 | N/C        |     |             |                 |                          |
| AL07 | INTRQB#    | OD  | PCI         |                 |                          |
| AL08 | N/C        |     |             |                 |                          |
| AL09 | PBMON[00]# | I/O | PCI         |                 |                          |
| AL10 | PBGNT[05]# | O   | PCI         |                 |                          |
| AL11 | PBGNT[01]# | O   | PCI         |                 |                          |
| AL12 | PBREQ[04]# | I   | PCI         |                 |                          |
| AL13 | PBREQ[00]# | I   | PCI         |                 |                          |
| AL14 | PBFRAME#   | I/O | PCI         |                 |                          |
| AL15 | PBSTOP#    | I/O | PCI         |                 |                          |
| AL16 | PBSERR#    | OD  | PCI         |                 |                          |
| AL17 | ACK64#     | I/O | PCI         |                 |                          |
| AL18 | PASERR#    | OD  | PCI         |                 |                          |
| AL19 | PASTOP#    | I/O | PCI         |                 |                          |
| AL20 | PAFRAME#   | I/O | PCI         |                 |                          |
| AL21 | PAREQ[00]# | I   | PCI         |                 |                          |
| AL22 | PAREQ[04]# | I   | PCI         |                 |                          |
| AL23 | PAGNT[01]# | O   | PCI         |                 |                          |
| AL24 | PAGNT[05]# | O   | PCI         |                 |                          |
| AL25 | PAMON[00]# | I/O | PCI         |                 |                          |
| AL26 | PHLDA#     | O   | PCI         |                 |                          |
| AL27 | INTRQA#    | OD  | PCI         |                 |                          |
| AL28 | N/C        |     |             |                 |                          |
| AL29 | N/C        |     |             |                 |                          |
| AL30 | N/C        |     |             |                 |                          |
| AL31 | N/C        |     |             |                 |                          |
| AL32 | N/C        |     |             |                 |                          |
| AM01 | N/C        |     |             |                 |                          |
| AM02 | N/C        |     |             |                 |                          |
| AM03 | GND        |     | Power       |                 |                          |
| AM04 | GND        |     | Power       |                 |                          |
| AM05 | GND        |     | Power       |                 |                          |
| AM06 | N/C        |     |             |                 |                          |
| AM07 | GND        |     | Power       |                 |                          |
| AM08 | N/C        |     |             |                 |                          |

**Table 12-24: PXB Pinlist Sorted by Pin (Continued)**

| PIN# | Signal     | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|------------|-----|-------------|-----------------|--------------------------|
| AM09 | VCC        |     | Power       |                 |                          |
| AM10 | N/C        |     |             |                 |                          |
| AM11 | GND        |     | Power       |                 |                          |
| AM12 | PBREQ[05]# | I   | PCI         |                 |                          |
| AM13 | VCC        |     | Power       |                 |                          |
| AM14 | PBCBE[02]# | I/O | PCI         |                 |                          |
| AM15 | GND        |     | Power       |                 |                          |
| AM16 | PBPERR#    | I/O | PCI         |                 |                          |
| AM17 | VCC        |     | Power       |                 |                          |
| AM18 | PAPERR#    | I/O | PCI         |                 |                          |
| AM19 | GND        |     | Power       |                 |                          |
| AM20 | PACBE[02]# | I/O | PCI         |                 |                          |
| AM21 | VCC        |     | Power       |                 |                          |
| AM22 | PAREQ[05]# | I   | PCI         |                 |                          |
| AM23 | GND        |     | Power       |                 |                          |
| AM24 | N/C        |     |             |                 |                          |
| AM25 | VCC        |     | Power       |                 |                          |
| AM26 | WSC#       | O   | PCI         |                 |                          |
| AM27 | GND        |     | Power       |                 |                          |
| AM28 | GND        |     | Power       |                 |                          |
| AM29 | GND        |     | Power       |                 |                          |
| AM30 | GND        |     | Power       |                 |                          |
| AM31 | N/C        |     |             |                 |                          |
| AM32 | GND        |     | Power       |                 |                          |

**Table 12-25: MUX Pin List Sorted by Pin**

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A01  | GND    |     | Power       |                 |                          |
| A02  | Q2D23  | I/O | LVTTTL      | 10ma            |                          |
| A03  | Q1D22  | I/O | LVTTTL      | 10ma            |                          |
| A04  | Q3D21  | I/O | LVTTTL      | 10ma            |                          |
| A05  | Q3D20  | I/O | LVTTTL      | 10ma            |                          |
| A06  | GND    |     | Power       |                 |                          |
| A07  | Q3D19  | I/O | LVTTTL      | 10ma            |                          |
| A08  | VCC    |     | Power       |                 |                          |
| A09  | Q3D18  | I/O | LVTTTL      | 10ma            |                          |
| A10  | TDO    | O   | OD          | 14ma            |                          |
| A11  | VCC    |     | Power       |                 |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A12  | Q3D17  | I/O | LVTTL       | 10ma            |                          |
| A13  | VCC    |     | Power       |                 |                          |
| A14  | Q1D16  | I/O | LVTTL       | 10ma            |                          |
| A15  | GND    |     | Power       |                 |                          |
| A16  | Q1D15  | I/O | LVTTL       | 10ma            |                          |
| A17  | Q3D14  | I/O | LVTTL       | 10ma            |                          |
| A18  | Q3D13  | I/O | LVTTL       | 10ma            |                          |
| A19  | Q1D13  | I/O | LVTTL       | 10ma            |                          |
| A20  | GND    |     | Power       |                 |                          |
| B01  | Q1D25  | I/O | LVTTL       | 10ma            |                          |
| B02  | GND    |     | Power       |                 |                          |
| B03  | Q1D23  | I/O | LVTTL       | 10ma            |                          |
| B04  | VCC    |     | Power       |                 |                          |
| B05  | Q2D21  | I/O | LVTTL       | 10ma            |                          |
| B06  | GND    |     | Power       |                 |                          |
| B07  | Q2D19  | I/O | LVTTL       | 10ma            |                          |
| B08  | VCC    |     | Power       |                 |                          |
| B09  | Q2D18  | I/O | LVTTL       | 10ma            |                          |
| B10  | GND    |     | Power       |                 |                          |
| B11  | GND    |     | Power       |                 |                          |
| B12  | Q2D17  | I/O | LVTTL       | 10ma            |                          |
| B13  | VCC    |     | Power       |                 |                          |
| B14  | Q0D16  | I/O | LVTTL       | 10ma            |                          |
| B15  | GND    |     | Power       |                 |                          |
| B16  | Q2D14  | I/O | LVTTL       | 10ma            |                          |
| B17  | VCC    |     | Power       |                 |                          |
| B18  | Q0D13  | I/O | LVTTL       | 10ma            |                          |
| B19  | GND    |     | Power       |                 |                          |
| B20  | Q2D11  | I/O | LVTTL       | 10ma            |                          |
| C01  | Q3D25  | I/O | LVTTL       | 10ma            |                          |
| C02  | Q0D25  | I/O | LVTTL       | 10ma            |                          |
| C03  | Q0D24  | I/O | LVTTL       | 10ma            |                          |
| C04  | Q0D23  | I/O | LVTTL       | 10ma            |                          |
| C05  | Q0D22  | I/O | LVTTL       | 10ma            |                          |
| C06  | Q1D21  | I/O | LVTTL       | 10ma            |                          |
| C07  | Q1D20  | I/O | LVTTL       | 10ma            |                          |
| C08  | Q1D19  | I/O | LVTTL       | 10ma            |                          |
| C09  | Q1D18  | I/O | LVTTL       | 10ma            |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| C10  | TDI    | I   | LVTTTL      |                 |                          |
| C11  | TCK    | I   | LVTTTL      |                 |                          |
| C12  | Q1D17  | I/O | LVTTTL      | 10ma            |                          |
| C13  | Q3D16  | I/O | LVTTTL      | 10ma            |                          |
| C14  | Q3D15  | I/O | LVTTTL      | 10ma            |                          |
| C15  | Q1D14  | I/O | LVTTTL      | 10ma            |                          |
| C16  | Q2D13  | I/O | LVTTTL      | 10ma            |                          |
| C17  | Q3D12  | I/O | LVTTTL      | 10ma            |                          |
| C18  | Q0D12  | I/O | LVTTTL      | 10ma            |                          |
| C19  | Q1D11  | I/O | LVTTTL      | 10ma            |                          |
| C20  | Q1D10  | I/O | LVTTTL      | 10ma            |                          |
| D01  | Q3D26  | I/O | LVTTTL      | 10ma            |                          |
| D02  | VCC    |     | Power       |                 |                          |
| D03  | Q3D24  | I/O | LVTTTL      | 10ma            |                          |
| D04  | GND    |     | Power       |                 |                          |
| D05  | Q3D22  | I/O | LVTTTL      | 10ma            |                          |
| D06  | VCC    |     | Power       |                 |                          |
| D07  | Q2D20  | I/O | LVTTTL      | 10ma            |                          |
| D08  | GND    |     | Power       |                 |                          |
| D09  | Q0D18  | I/O | LVTTTL      | 10ma            |                          |
| D10  | VCC    |     | Power       |                 |                          |
| D11  | VCC    |     | Power       |                 |                          |
| D12  | Q0D17  | I/O | LVTTTL      | 10ma            |                          |
| D13  | GND    |     | Power       |                 |                          |
| D14  | Q0D15  | I/O | LVTTTL      | 10ma            |                          |
| D15  | VCC    |     | Power       |                 |                          |
| D16  | Q2D12  | I/O | LVTTTL      | 10ma            |                          |
| D17  | GND    |     | Power       |                 |                          |
| D18  | Q0D11  | I/O | LVTTTL      | 10ma            |                          |
| D19  | VCC    |     | Power       |                 |                          |
| D20  | Q3D09  | I/O | LVTTTL      | 10ma            |                          |
| E01  | Q1D27  | I/O | LVTTTL      | 10ma            |                          |
| E02  | Q2D26  | I/O | LVTTTL      | 10ma            |                          |
| E03  | Q2D25  | I/O | LVTTTL      | 10ma            |                          |
| E04  | Q2D24  | I/O | LVTTTL      | 10ma            |                          |
| E05  | Q3D23  | I/O | LVTTTL      | 10ma            |                          |
| E06  | Q2D22  | I/O | LVTTTL      | 10ma            |                          |
| E07  | Q0D21  | I/O | LVTTTL      | 10ma            |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| E08  | Q0D20  | I/O | LVTTL       | 10ma            |                          |
| E09  | Q0D19  | I/O | LVTTL       | 10ma            |                          |
| E10  | TMS    | I   | LVTTL       |                 |                          |
| E11  | TRST#  | I   | LVTTL       |                 |                          |
| E12  | Q2D16  | I/O | LVTTL       | 10ma            |                          |
| E13  | Q2D15  | I/O | LVTTL       | 10ma            |                          |
| E14  | Q0D14  | I/O | LVTTL       | 10ma            |                          |
| E15  | Q1D12  | I/O | LVTTL       | 10ma            |                          |
| E16  | Q3D11  | I/O | LVTTL       | 10ma            |                          |
| E17  | Q3D10  | I/O | LVTTL       | 10ma            |                          |
| E18  | Q0D10  | I/O | LVTTL       | 10ma            |                          |
| E19  | Q2D09  | I/O | LVTTL       | 10ma            |                          |
| E20  | Q3D08  | I/O | LVTTL       | 10ma            |                          |
| F01  | Q0D28  | I/O | LVTTL       | 10ma            |                          |
| F02  | GND    |     | Power       |                 |                          |
| F03  | Q1D26  | I/O | LVTTL       | 10ma            |                          |
| F04  | VCC    |     | Power       |                 |                          |
| F05  | Q1D24  | I/O | LVTTL       | 10ma            |                          |
| F06  | VCC    |     | Power       |                 |                          |
| F14  | VCC    |     | Power       |                 |                          |
| F15  | VCC    |     | Power       |                 |                          |
| F16  | Q2D10  | I/O | LVTTL       | 10ma            |                          |
| F17  | VCC    |     | Power       |                 |                          |
| F18  | Q1D09  | I/O | LVTTL       | 10ma            |                          |
| F19  | GND    |     | Power       |                 |                          |
| F20  | Q1D08  | I/O | LVTTL       | 10ma            |                          |
| G01  | Q2D28  | I/O | LVTTL       | 10ma            |                          |
| G02  | Q1D28  | I/O | LVTTL       | 10ma            |                          |
| G03  | Q3D27  | I/O | LVTTL       | 10ma            |                          |
| G04  | Q0D27  | I/O | LVTTL       | 10ma            |                          |
| G05  | Q0D26  | I/O | LVTTL       | 10ma            |                          |
| G06  | VCC    |     | Power       |                 |                          |
| G16  | Q0D09  | I/O | LVTTL       | 10ma            |                          |
| G17  | Q2D08  | I/O | LVTTL       | 10ma            |                          |
| G18  | Q0D08  | I/O | LVTTL       | 10ma            |                          |
| G19  | Q1D07  | I/O | LVTTL       | 10ma            |                          |
| G20  | Q2D07  | I/O | LVTTL       | 10ma            |                          |
| H01  | VCC    |     | Power       |                 |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| H02  | VCC    |     | Power       |                 |                          |
| H03  | Q0D29  | I/O | LVTTTL      | 10ma            |                          |
| H04  | GND    |     | Power       |                 |                          |
| H05  | Q2D27  | I/O | LVTTTL      | 10ma            |                          |
| H16  | Q3D07  | I/O | LVTTTL      | 10ma            |                          |
| H17  | GND    |     | Power       |                 |                          |
| H18  | Q0D07  | I/O | LVTTTL      | 10ma            |                          |
| H19  | VCC    |     | Power       |                 |                          |
| H20  | VCC    |     | Power       |                 |                          |
| J01  | Q0D30  | I/O | LVTTTL      | 10ma            |                          |
| J02  | Q3D29  | I/O | LVTTTL      | 10ma            |                          |
| J03  | Q2D29  | I/O | LVTTTL      | 10ma            |                          |
| J04  | Q1D29  | I/O | LVTTTL      | 10ma            |                          |
| J05  | Q3D28  | I/O | LVTTTL      | 10ma            |                          |
| J09  | GND    |     | Power       |                 |                          |
| J10  | GND    |     | Power       |                 |                          |
| J11  | GND    |     | Power       |                 |                          |
| J12  | GND    |     | Power       |                 |                          |
| J16  | Q3D06  | I/O | LVTTTL      | 10ma            |                          |
| J17  | Q3D05  | I/O | LVTTTL      | 10ma            |                          |
| J18  | Q0D06  | I/O | LVTTTL      | 10ma            |                          |
| J19  | Q1D06  | I/O | LVTTTL      | 10ma            |                          |
| J20  | Q2D06  | I/O | LVTTTL      | 10ma            |                          |
| K01  | Q3D30  | I/O | LVTTTL      | 10ma            |                          |
| K02  | GND    |     | Power       |                 |                          |
| K03  | Q2D30  | I/O | LVTTTL      | 10ma            |                          |
| K04  | VCC    |     | Power       |                 |                          |
| K05  | Q1D30  | I/O | LVTTTL      | 10ma            |                          |
| K09  | GND    |     | Power       |                 |                          |
| K10  | GND    |     | Power       |                 |                          |
| K11  | GND    |     | Power       |                 |                          |
| K12  | GND    |     | Power       |                 |                          |
| K16  | Q0D05  | I/O | LVTTTL      | 10ma            |                          |
| K17  | VCC    |     | Power       |                 |                          |
| K18  | Q1D05  | I/O | LVTTTL      | 10ma            |                          |
| K19  | GND    |     | Power       |                 |                          |
| K20  | Q2D05  | I/O | LVTTTL      | 10ma            |                          |
| L01  | Q2D31  | I/O | LVTTTL      | 10ma            |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| L02  | GND    |     | Power       |                 |                          |
| L03  | Q1D31  | I/O | LVTTL       | 10ma            |                          |
| L04  | VCC    |     | Power       |                 |                          |
| L05  | Q0D31  | I/O | LVTTL       | 10ma            |                          |
| L09  | GND    |     | Power       |                 |                          |
| L10  | GND    |     | Power       |                 |                          |
| L11  | GND    |     | Power       |                 |                          |
| L12  | GND    |     | Power       |                 |                          |
| L16  | Q1D04  | I/O | LVTTL       | 10ma            |                          |
| L17  | VCC    |     | Power       |                 |                          |
| L18  | Q2D04  | I/O | LVTTL       | 10ma            |                          |
| L19  | GND    |     | Power       |                 |                          |
| L20  | Q3D04  | I/O | LVTTL       | 10ma            |                          |
| M01  | Q2D32  | I/O | LVTTL       | 10ma            |                          |
| M02  | Q1D32  | I/O | LVTTL       | 10ma            |                          |
| M03  | Q0D32  | I/O | LVTTL       | 10ma            |                          |
| M04  | Q3D31  | I/O | LVTTL       | 10ma            |                          |
| M05  | Q3D32  | I/O | LVTTL       | 10ma            |                          |
| M09  | GND    |     | Power       |                 |                          |
| M10  | GND    |     | Power       |                 |                          |
| M11  | GND    |     | Power       |                 |                          |
| M12  | GND    |     | Power       |                 |                          |
| M16  | Q3D02  | I/O | LVTTL       | 10ma            |                          |
| M17  | Q1D03  | I/O | LVTTL       | 10ma            |                          |
| M18  | Q2D03  | I/O | LVTTL       | 10ma            |                          |
| M19  | Q3D03  | I/O | LVTTL       | 10ma            |                          |
| M20  | Q0D04  | I/O | LVTTL       | 10ma            |                          |
| N01  | VCC    |     | Power       |                 |                          |
| N02  | VCC    |     | Power       |                 |                          |
| N03  | Q0D33  | I/O | LVTTL       | 10ma            |                          |
| N04  | GND    |     | Power       |                 |                          |
| N05  | Q3D33  | I/O | LVTTL       | 10ma            |                          |
| N16  | Q3D01  | I/O | LVTTL       | 10ma            |                          |
| N17  | GND    |     | Power       |                 |                          |
| N18  | Q0D03  | I/O | LVTTL       | 10ma            |                          |
| N19  | VCC    |     | Power       |                 |                          |
| N20  | VCC    |     | Power       |                 |                          |
| P01  | Q2D33  | I/O | LVTTL       | 10ma            |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| P02  | Q1D33   | I/O | LVTTTL      | 10ma            |                          |
| P03  | Q0D34   | I/O | LVTTTL      | 10ma            |                          |
| P04  | Q1D34   | I/O | LVTTTL      | 10ma            |                          |
| P05  | Q3D34   | I/O | LVTTTL      | 10ma            |                          |
| P15  | VCC     |     | Power       |                 |                          |
| P16  | Q1D00   | I/O | LVTTTL      | 10ma            |                          |
| P17  | Q1D01   | I/O | LVTTTL      | 10ma            |                          |
| P18  | Q0D02   | I/O | LVTTTL      | 10ma            |                          |
| P19  | Q1D02   | I/O | LVTTTL      | 10ma            |                          |
| P20  | Q2D02   | I/O | LVTTTL      | 10ma            |                          |
| R01  | GND     |     | Power       |                 |                          |
| R02  | GND     |     | Power       |                 |                          |
| R03  | Q0D35   | I/O | LVTTTL      | 10ma            |                          |
| R04  | VCC     |     | Power       |                 |                          |
| R05  | MD31#   | I/O | AGTL+       | 55ma            |                          |
| R06  | VCC     |     | Power       |                 |                          |
| R07  | VCC     |     | Power       |                 |                          |
| R15  | VCC     |     | Power       |                 |                          |
| R16  | MD00#   | I/O | AGTL+       | 55ma            |                          |
| R17  | VCC     |     | Power       |                 |                          |
| R18  | Q2D00   | I/O | LVTTTL      | 10ma            |                          |
| R19  | GND     |     | Power       |                 |                          |
| R20  | GND     |     | Power       |                 |                          |
| T01  | Q2D34   | I/O | LVTTTL      | 10ma            |                          |
| T02  | Q1D35   | I/O | LVTTTL      | 10ma            |                          |
| T03  | Q3D35   | I/O | LVTTTL      | 10ma            |                          |
| T04  | MD32#   | I/O | AGTL+       | 55ma            |                          |
| T05  | MD29#   | I/O | AGTL+       | 55ma            |                          |
| T06  | DSTBP1# | I/O | AGTL+       | 55ma            |                          |
| T07  | MD23#   | I/O | AGTL+       | 55ma            |                          |
| T08  | MD19#   | I/O | AGTL+       | 55ma            |                          |
| T09  | N/C     |     |             |                 |                          |
| T10  | VCCA    |     | Power       |                 |                          |
| T11  | WDME#   | I   | AGTL+       | 55ma            |                          |
| T12  | CRES0   | I   | Analog      |                 |                          |
| T13  | MD15#   | I/O | AGTL+       | 55ma            |                          |
| T14  | MD09#   | I/O | AGTL+       | 55ma            |                          |
| T15  | MD07#   | I/O | AGTL+       | 55ma            |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| T16  | MD05#   | I/O | AGTL+       | 55ma            |                          |
| T17  | MD01#   | I/O | AGTL+       | 55ma            |                          |
| T18  | Q0D00   | I/O | LVTTTL      | 10ma            |                          |
| T19  | Q3D00   | I/O | LVTTTL      | 10ma            |                          |
| T20  | Q2D01   | I/O | LVTTTL      | 10ma            |                          |
| U01  | Q2D35   | I/O | LVTTTL      | 10ma            |                          |
| U02  | VCC     |     | Power       |                 |                          |
| U03  | MD33#   | I/O | AGTL+       | 55ma            |                          |
| U04  | GND     |     | Power       |                 |                          |
| U05  | VTT     |     | Power       |                 |                          |
| U06  | VCC     |     | Power       |                 |                          |
| U07  | MD21#   | I/O | AGTL+       | 55ma            |                          |
| U08  | GND     |     | Power       |                 |                          |
| U09  | VTT     |     | Power       |                 |                          |
| U10  | VCC     |     | Power       |                 |                          |
| U11  | VCC     |     | Power       |                 |                          |
| U12  | VTT     |     | Power       |                 |                          |
| U13  | GND     |     | Power       |                 |                          |
| U14  | MD13#   | I/O | AGTL+       | 55ma            |                          |
| U15  | VCC     |     | Power       |                 |                          |
| U16  | VTT     |     | Power       |                 |                          |
| U17  | GND     |     | Power       |                 |                          |
| U18  | MD02#   | I/O | AGTL+       | 55ma            |                          |
| U19  | VCC     |     | Power       |                 |                          |
| U20  | Q0D01   | I/O | LVTTTL      | 10ma            |                          |
| V01  | N/C     |     |             |                 |                          |
| V02  | MD34#   | I/O | AGTL+       | 55ma            |                          |
| V03  | MD30#   | I/O | AGTL+       | 55ma            |                          |
| V04  | MD27#   | I/O | AGTL+       | 55ma            |                          |
| V05  | VREF    | I   | Analog      |                 |                          |
| V06  | MD24#   | I/O | AGTL+       | 55ma            |                          |
| V07  | MD20#   | I/O | AGTL+       | 55ma            |                          |
| V08  | DOFF1#  | I   | AGTL+       | 55ma            |                          |
| V09  | DOFF0#  | I   | AGTL+       | 55ma            |                          |
| V10  | HCLKIN  | I   | 2.5V        |                 |                          |
| V11  | DVALID# | I   | AGTL+       | 55ma            |                          |
| V12  | LRD#    | I   | AGTL+       | 55ma            |                          |
| V13  | CRES1   | I   | Analog      |                 |                          |

Table 12-25: MUX Pin List Sorted by Pin (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| V14  | MD16#    | I/O | AGTL+       | 55ma            |                          |
| V15  | MD10#    | I/O | AGTL+       | 55ma            |                          |
| V16  | VREF     | I   | Analog      |                 |                          |
| V17  | MD08#    | I/O | AGTL+       | 55ma            |                          |
| V18  | MD06#    | I/O | AGTL+       | 55ma            |                          |
| V19  | MD03#    | I/O | AGTL+       | 55ma            |                          |
| V20  | N/C      |     |             |                 |                          |
| W01  | MD35#    | I/O | AGTL+       | 55ma            |                          |
| W02  | GND      |     | Power       |                 |                          |
| W03  | VTT      |     | Power       |                 |                          |
| W04  | VCC      |     | Power       |                 |                          |
| W05  | MD25#    | I/O | AGTL+       | 55ma            |                          |
| W06  | GND      |     | Power       |                 |                          |
| W07  | VTT      |     | Power       |                 |                          |
| W08  | VCC      |     | Power       |                 |                          |
| W09  | DSEL#    | I   | AGTL+       | 55ma            |                          |
| W10  | GND      |     | Power       |                 |                          |
| W11  | GND      |     | Power       |                 |                          |
| W12  | GDCMPLT# | I/O | AGTL+       | 55ma            |                          |
| W13  | VCC      |     | Power       |                 |                          |
| W14  | VTT      |     | Power       |                 |                          |
| W15  | GND      |     | Power       |                 |                          |
| W16  | MD11#    | I/O | AGTL+       | 55ma            |                          |
| W17  | VCC      |     | Power       |                 |                          |
| W18  | VTT      |     | Power       |                 |                          |
| W19  | GND      |     | Power       |                 |                          |
| W20  | MD04#    | I/O | AGTL+       | 55ma            |                          |
| Y01  | GND      |     | Power       |                 |                          |
| Y02  | MD28#    | I/O | AGTL+       | 55ma            |                          |
| Y03  | DSTBN1#  | I/O | AGTL+       | 55ma            |                          |
| Y04  | MD26#    | I/O | AGTL+       | 55ma            |                          |
| Y05  | MD22#    | I/O | AGTL+       | 55ma            |                          |
| Y06  | GND      |     | Power       |                 |                          |
| Y07  | MD18#    | I/O | AGTL+       | 55ma            |                          |
| Y08  | LDSTB#   | I   | AGTL+       | 55ma            |                          |
| Y09  | MRESET#  | I   | AGTL+       | 55ma            |                          |
| Y10  | VCC      |     | Power       |                 |                          |
| Y11  | WDEVT#   | I   | AGTL+       | 55ma            |                          |

**Table 12-25: MUX Pin List Sorted by Pin (Continued)**

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| Y12  | AVWP#   | I   | AGTL+       | 55ma            |                          |
| Y13  | DCMPLT# | I/O | AGTL+       | 55ma            |                          |
| Y14  | MD17#   | I/O | AGTL+       | 55ma            |                          |
| Y15  | GND     |     | Power       |                 |                          |
| Y16  | MD14#   | I/O | AGTL+       | 55ma            |                          |
| Y17  | MD12#   | I/O | AGTL+       | 55ma            |                          |
| Y18  | DSTBP0# | I/O | AGTL+       | 55ma            |                          |
| Y19  | DSTBN0# | I/O | AGTL+       | 55ma            |                          |
| Y20  | GND     |     | Power       |                 |                          |

**Table 12-26: RCG Pin List Sorted by Pin**

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| A01  | GND     |     | Power       |                 |                          |
| A02  | RASCA0# | O   | LVTTTL      | 10ma            |                          |
| A03  | CASCA0# | O   | LVTTTL      | 10ma            |                          |
| A04  | RASCB0# | O   | LVTTTL      | 10ma            |                          |
| A05  | CASCB1# | O   | LVTTTL      | 10ma            |                          |
| A06  | GND     |     | Power       |                 |                          |
| A07  | WECA#   | O   | LVTTTL      | 10ma            |                          |
| A08  | VCC     |     | Power       |                 |                          |
| A09  | WECB#   | O   | LVTTTL      | 10ma            |                          |
| A10  | ADDRD13 | O   | LVTTTL      | 10ma            |                          |
| A11  | ADDRD08 | O   | LVTTTL      | 10ma            |                          |
| A12  | ADDRD03 | O   | LVTTTL      | 10ma            |                          |
| A13  | VCC     |     | Power       |                 |                          |
| A14  | ADDRD01 | O   | LVTTTL      | 10ma            |                          |
| A15  | GND     |     | Power       |                 |                          |
| A16  | RASDD1# | O   | LVTTTL      | 10ma            |                          |
| A17  | RASDD0# | O   | LVTTTL      | 10ma            |                          |
| A18  | CASDC0# | O   | LVTTTL      | 10ma            |                          |
| A19  | CASDA1# | O   | LVTTTL      | 10ma            |                          |
| A20  | GND     |     | Power       |                 |                          |
| B01  | RASCA1# | O   | LVTTTL      | 10ma            |                          |
| B02  | GND     |     | Power       |                 |                          |
| B03  | RASCB1# | O   | LVTTTL      | 10ma            |                          |
| B04  | VCC     |     | Power       |                 |                          |
| B05  | CASCC0# | O   | LVTTTL      | 10ma            |                          |
| B06  | GND     |     | Power       |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| B07  | CASCD1# | O   | LVTTTL      | 10ma            |                          |
| B08  | VCC     |     | Power       |                 |                          |
| B09  | CASCC1# | O   | LVTTTL      | 10ma            |                          |
| B10  | GND     |     | Power       |                 |                          |
| B11  | GND     |     | Power       |                 |                          |
| B12  | ADDRD04 | O   | LVTTTL      | 10ma            |                          |
| B13  | VCC     |     | Power       |                 |                          |
| B14  | RASDC1# | O   | LVTTTL      | 10ma            |                          |
| B15  | GND     |     | Power       |                 |                          |
| B16  | RASDC0# | O   | LVTTTL      | 10ma            |                          |
| B17  | VCC     |     | Power       |                 |                          |
| B18  | CASDD1# | O   | LVTTTL      | 10ma            |                          |
| B19  | GND     |     | Power       |                 |                          |
| B20  | CASDC1# | O   | LVTTTL      | 10ma            |                          |
| C01  | ADDRC05 | O   | LVTTTL      | 10ma            |                          |
| C02  | ADDRC03 | O   | LVTTTL      | 10ma            |                          |
| C03  | ADDRC00 | O   | LVTTTL      | 10ma            |                          |
| C04  | RASCC1# | O   | LVTTTL      | 10ma            |                          |
| C05  | RASCC0# | O   | LVTTTL      | 10ma            |                          |
| C06  | RASCD0# | O   | LVTTTL      | 10ma            |                          |
| C07  | CASCB0# | O   | LVTTTL      | 10ma            |                          |
| C08  | CASCD0# | O   | LVTTTL      | 10ma            |                          |
| C09  | N/C     |     |             |                 |                          |
| C10  | ADDRD12 | O   | LVTTTL      | 10ma            |                          |
| C11  | ADDRD09 | O   | LVTTTL      | 10ma            |                          |
| C12  | ADDRD05 | O   | LVTTTL      | 10ma            |                          |
| C13  | ADDRD02 | O   | LVTTTL      | 10ma            |                          |
| C14  | ADDRD00 | O   | LVTTTL      | 10ma            |                          |
| C15  | RASDA0# | O   | LVTTTL      | 10ma            |                          |
| C16  | RASDB0# | O   | LVTTTL      | 10ma            |                          |
| C17  | WEDA#   | O   | LVTTTL      | 10ma            |                          |
| C18  | CASDB0# | O   | LVTTTL      | 10ma            |                          |
| C19  | CASDD0# | O   | LVTTTL      | 10ma            |                          |
| C20  | WEDB#   | O   | LVTTTL      | 10ma            |                          |
| D01  | ADDRC08 | O   | LVTTTL      | 10ma            |                          |
| D02  | VCC     |     | Power       |                 |                          |
| D03  | ADDRC02 | O   | LVTTTL      | 10ma            |                          |
| D04  | GND     |     | Power       |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| D05  | RASCD1# | O   | LVTTTL      | 10ma            |                          |
| D06  | VCC     |     | Power       |                 |                          |
| D07  | CASCA1# | O   | LVTTTL      | 10ma            |                          |
| D08  | GND     |     | Power       |                 |                          |
| D09  | N/C     |     |             |                 |                          |
| D10  | VCC     |     | Power       |                 |                          |
| D11  | VCC     |     | Power       |                 |                          |
| D12  | ADDRD06 | O   | LVTTTL      | 10ma            |                          |
| D13  | GND     |     | Power       |                 |                          |
| D14  | RASDB1# | O   | LVTTTL      | 10ma            |                          |
| D15  | VCC     |     | Power       |                 |                          |
| D16  | CASDA0# | O   | LVTTTL      | 10ma            |                          |
| D17  | GND     |     | Power       |                 |                          |
| D18  | CASDB1# | O   | LVTTTL      | 10ma            |                          |
| D19  | VCC     |     | Power       |                 |                          |
| D20  | N/C     |     |             |                 |                          |
| E01  | ADDRC10 | O   | LVTTTL      | 10ma            |                          |
| E02  | ADDRC07 | O   | LVTTTL      | 10ma            |                          |
| E03  | ADDRC04 | O   | LVTTTL      | 10ma            |                          |
| E04  | ADDRC01 | O   | LVTTTL      | 10ma            |                          |
| E05  | N/C     |     |             |                 |                          |
| E06  | N/C     |     |             |                 |                          |
| E07  | N/C     |     |             |                 |                          |
| E08  | N/C     |     |             |                 |                          |
| E09  | N/C     |     |             |                 |                          |
| E10  | ADDRD11 | O   | LVTTTL      | 10ma            |                          |
| E11  | ADDRD10 | O   | LVTTTL      | 10ma            |                          |
| E12  | ADDRD07 | O   | LVTTTL      | 10ma            |                          |
| E13  | RASDA1# | O   | LVTTTL      | 10ma            |                          |
| E14  | N/C     |     |             |                 |                          |
| E15  | N/C     |     |             |                 |                          |
| E16  | N/C     |     |             |                 |                          |
| E17  | N/C     |     |             |                 |                          |
| E18  | N/C     |     |             |                 |                          |
| E19  | N/C     |     |             |                 |                          |
| E20  | ADDRB12 | O   | LVTTTL      | 10ma            |                          |
| F01  | ADDRC13 |     | LVTTTL      | 10ma            |                          |
| F02  | GND     | O   | Power       |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| F03  | ADDRC06 |     | LVTTTL      | 10ma            |                          |
| F04  | VCC     | O   | LVTTTL      | 10ma            |                          |
| F05  | N/C     |     |             |                 |                          |
| F06  | VCC     |     | Power       |                 |                          |
| F14  | VCC     |     | Power       |                 |                          |
| F15  | VCC     |     | Power       |                 |                          |
| F16  | N/C     |     |             |                 |                          |
| F17  | VCC     |     | Power       |                 |                          |
| F18  | ADDRB13 | O   | LVTTTL      | 10ma            |                          |
| F19  | GND     |     | Power       |                 |                          |
| F20  | ADDRB09 | O   | LVTTTL      | 10ma            |                          |
| G01  | N/C     |     |             |                 |                          |
| G02  | ADDRC12 | O   | LVTTTL      | 10ma            |                          |
| G03  | ADDRC11 | O   | LVTTTL      | 10ma            |                          |
| G04  | ADDRC09 | O   | LVTTTL      | 10ma            |                          |
| G05  | N/C     |     |             |                 |                          |
| G06  | VCC     |     | Power       |                 |                          |
| G16  | N/C     |     |             |                 |                          |
| G17  | ADDRB11 | O   | LVTTTL      | 10ma            |                          |
| G18  | ADDRB10 | O   | LVTTTL      | 10ma            |                          |
| G19  | ADDRB06 | O   | LVTTTL      | 10ma            |                          |
| G20  | ADDRB05 | O   | LVTTTL      | 10ma            |                          |
| H01  | VCC     |     | Power       |                 |                          |
| H02  | VCC     |     | Power       |                 |                          |
| H03  | CASAC0# | O   | LVTTTL      | 10ma            |                          |
| H04  | GND     |     | Power       |                 |                          |
| H05  | CASAA1# | O   | LVTTTL      | 10ma            |                          |
| H16  | ADDRB08 | O   | LVTTTL      | 10ma            |                          |
| H17  | GND     |     | Power       |                 |                          |
| H18  | ADDRB07 | O   | LVTTTL      | 10ma            |                          |
| H19  | VCC     |     | Power       |                 |                          |
| H20  | VCC     |     | Power       |                 |                          |
| J01  | WEAA#   | O   | LVTTTL      | 10ma            |                          |
| J02  | CASAB1# | O   | LVTTTL      | 10ma            |                          |
| J03  | CASAD1# | O   | LVTTTL      | 10ma            |                          |
| J04  | WEAB#   | O   | LVTTTL      | 10ma            |                          |
| J05  | CASAC1# | O   | LVTTTL      | 10ma            |                          |
| J09  | GND     |     | Power       |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| J10  | GND     |     | Power       |                 |                          |
| J11  | GND     |     | Power       |                 |                          |
| J12  | GND     |     | Power       |                 |                          |
| J16  | ADDRB04 | O   | LVTTTL      | 10ma            |                          |
| J17  | ADDRB03 | O   | LVTTTL      | 10ma            |                          |
| J18  | ADDRB02 | O   | LVTTTL      | 10ma            |                          |
| J19  | ADDRB01 | O   | LVTTTL      | 10ma            |                          |
| J20  | ADDRB00 | O   | LVTTTL      | 10ma            |                          |
| K01  | CASAA0# | O   | LVTTTL      | 10ma            |                          |
| K02  | GND     |     | Power       |                 |                          |
| K03  | CASAB0# | O   | LVTTTL      | 10ma            |                          |
| K04  | VCC     |     | Power       |                 |                          |
| K05  | CASAD0# | O   | LVTTTL      | 10ma            |                          |
| K09  | GND     |     | Power       |                 |                          |
| K10  | GND     |     | Power       |                 |                          |
| K11  | GND     |     | Power       |                 |                          |
| K12  | GND     |     | Power       |                 |                          |
| K16  | RASBB1# | O   | LVTTTL      | 10ma            |                          |
| K17  | VCC     |     | Power       |                 |                          |
| K18  | RASBC1# | O   | LVTTTL      | 10ma            |                          |
| K19  | GND     |     | Power       |                 |                          |
| K20  | RASBD1# | O   | LVTTTL      | 10ma            |                          |
| L01  | RASAA0# | O   | LVTTTL      | 10ma            |                          |
| L02  | GND     |     | Power       |                 |                          |
| L03  | RASAC0# | O   | LVTTTL      | 10ma            |                          |
| L04  | VCC     |     | Power       |                 |                          |
| L05  | RASAD0# | O   | LVTTTL      | 10ma            |                          |
| L09  | GND     |     | Power       |                 |                          |
| L10  | GND     |     | Power       |                 |                          |
| L11  | GND     |     | Power       |                 |                          |
| L12  | GND     |     | Power       |                 |                          |
| L16  | RASBA1# | O   | LVTTTL      | 10ma            |                          |
| L17  | VCC     |     | Power       |                 |                          |
| L18  | RASBA0# | O   | LVTTTL      | 10ma            |                          |
| L19  | GND     |     | Power       |                 |                          |
| L20  | RASBC0# | O   | LVTTTL      | 10ma            |                          |
| M01  | RASAB0# | O   | LVTTTL      | 10ma            |                          |
| M02  | RASAA1# | O   | LVTTTL      | 10ma            |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| M03  | RASAB1# | O   | LVTTL       | 10ma            |                          |
| M04  | RASAC1# | O   | LVTTL       | 10ma            |                          |
| M05  | RASAD1# | O   | LVTTL       | 10ma            |                          |
| M09  | GND     |     | Power       |                 |                          |
| M10  | GND     |     | Power       |                 |                          |
| M11  | GND     |     | Power       |                 |                          |
| M12  | GND     |     | Power       |                 |                          |
| M16  | CASBA0# | O   | LVTTL       | 10ma            |                          |
| M17  | CASBB1# | O   | LVTTL       | 10ma            |                          |
| M18  | RASBB0# | O   | LVTTL       | 10ma            |                          |
| M19  | CASBB0# | O   | LVTTL       | 10ma            |                          |
| M20  | RASBD0# | O   | LVTTL       | 10ma            |                          |
| N01  | VCC     |     | Power       |                 |                          |
| N02  | VCC     |     | Power       |                 |                          |
| N03  | ADDRA01 | O   | LVTTL       | 10ma            |                          |
| N04  | GND     |     | Power       |                 |                          |
| N05  | ADDRA00 | O   | LVTTL       | 10ma            |                          |
| N16  | N/C     |     |             |                 |                          |
| N17  | GND     |     | Power       |                 |                          |
| N18  | CASBA1# | O   | LVTTL       | 10ma            |                          |
| N19  | VCC     |     | Power       |                 |                          |
| N20  | VCC     |     | Power       |                 |                          |
| P01  | ADDRA03 | O   | LVTTL       | 10ma            |                          |
| P02  | ADDRA02 | O   | LVTTL       | 10ma            |                          |
| P03  | ADDRA05 | O   | LVTTL       | 10ma            |                          |
| P04  | ADDRA04 | O   | LVTTL       | 10ma            |                          |
| P05  | N/C     |     |             |                 |                          |
| P15  | VCC     |     | Power       |                 |                          |
| P16  | N/C     |     |             |                 |                          |
| P17  | WEBA#   | O   | LVTTL       | 10ma            |                          |
| P18  | CASBC0# | O   | LVTTL       | 10ma            |                          |
| P19  | CASBD0# | O   | LVTTL       | 10ma            |                          |
| P20  | WEBB#   | O   | LVTTL       | 10ma            |                          |
| R01  | GND     |     | Power       |                 |                          |
| R02  | GND     |     | Power       |                 |                          |
| R03  | ADDRA06 | O   | LVTTL       | 10ma            |                          |
| R04  | VCC     |     | Power       |                 |                          |
| R05  | N/C     |     |             |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown  |
|------|---------|-----|-------------|-----------------|---------------------------|
| R06  | VCC     |     | Power       |                 |                           |
| R07  | VCC     |     | Power       |                 |                           |
| R15  | VCC     |     | Power       |                 |                           |
| R16  | N/C     |     |             |                 |                           |
| R17  | VCC     |     | Power       |                 |                           |
| R18  | CASBD1# | O   | LVTTTL      | 10ma            |                           |
| R19  | GND     |     | Power       |                 |                           |
| R20  | GND     |     | Power       |                 |                           |
| T01  | ADDRA08 | O   | LVTTTL      | 10ma            |                           |
| T02  | ADDRA07 | O   | LVTTTL      | 10ma            |                           |
| T03  | ADDRA10 | O   | LVTTTL      | 10ma            |                           |
| T04  | ADDRA09 | O   | LVTTTL      | 10ma            |                           |
| T05  | N/C     |     |             |                 |                           |
| T06  | N/C     |     |             |                 |                           |
| T07  | MA05#   | I   | LVTTTL      | 10ma            |                           |
| T08  | MA02#   | I   | LVTTTL      | 10ma            |                           |
| T09  | N/C     |     |             |                 |                           |
| T10  | VCCA    |     | Power       |                 |                           |
| T11  | CMND1#  | I   | AGTL+       |                 |                           |
| T12  | BANK0#  | I   | AGTL+       |                 |                           |
| T13  | N/C     |     |             |                 |                           |
| T14  | WDME#   | O   | AGTL+       | 55ma            |                           |
| T15  | LRD#    | O   | AGTL+       | 55ma            |                           |
| T16  | N/C     |     |             |                 |                           |
| T17  | VCC     |     | Power       |                 |                           |
| T18  | BANKID# | I   | LVTTTL      |                 | Requires external pull-up |
| T19  | DR50T#  | I   | LVTTTL      |                 |                           |
| T20  | CASBC1# | O   | LVTTTL      | 10ma            |                           |
| U01  | ADDRA11 | O   | LVTTTL      | 10ma            |                           |
| U02  | VCC     |     | Power       |                 |                           |
| U03  | N/C     |     |             |                 |                           |
| U04  | GND     |     | Power       |                 |                           |
| U05  | VTT     |     | Power       |                 |                           |
| U06  | VCC     |     | Power       |                 |                           |
| U07  | MA06#   | I   | LVTTTL      | 10ma            |                           |
| U08  | GND     |     | Power       |                 |                           |
| U09  | VTT     |     | Power       |                 |                           |
| U10  | VCC     |     | Power       |                 |                           |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| U11  | VCC     |     | Power       |                 |                          |
| U12  | VTT     |     | Power       |                 |                          |
| U13  | GND     |     | Power       |                 |                          |
| U14  | RHIT#   | O   | AGTL+       | 55ma            |                          |
| U15  | VCC     |     | Power       |                 |                          |
| U16  | VTT     |     | Power       |                 |                          |
| U17  | GND     |     | Power       |                 |                          |
| U18  | DR50H#  | I   | LVTTL       |                 |                          |
| U19  | VCC     |     | Power       |                 |                          |
| U20  | VCC     |     | Power       |                 |                          |
| V01  | ADDRA13 | O   | LVTTL       | 10ma            |                          |
| V02  | ADDRA12 | O   | LVTTL       | 10ma            |                          |
| V03  | CRES1   | I   | Analog      |                 |                          |
| V04  | CRES0   | I   | Analog      |                 |                          |
| V05  | VREF    | I   | Analog      |                 |                          |
| V06  | MA09#   | I   | AGTL+       |                 |                          |
| V07  | MA07#   | I   | AGTL+       |                 |                          |
| V08  | MA03#   | I   | AGTL+       |                 |                          |
| V09  | MA00#   | I   | AGTL+       |                 |                          |
| V10  | HCLKIN  | I   | 2.5V        |                 |                          |
| V11  | CSTB#   | I   | AGTL+       |                 |                          |
| V12  | BANK1#  | I   | AGTL+       |                 |                          |
| V13  | RCMPLT# | O   | AGTL+       | 55ma            |                          |
| V14  | PHIT#   | O   | AGTL+       | 55ma            |                          |
| V15  | AVWP#   | O   | AGTL+       | 55ma            |                          |
| V16  | VREF    | I   | Analog      |                 |                          |
| V17  | TRST#   | I   | LVTTL       |                 |                          |
| V18  | TCK     | I   | LVTTL       |                 |                          |
| V19  | TDO     | O   | OD          | 14ma            |                          |
| V20  | TDI     | I   | LVTTL       |                 |                          |
| W01  | N/C     |     |             |                 |                          |
| W02  | GND     |     | Power       |                 |                          |
| W03  | VTT     |     | Power       |                 |                          |
| W04  | VCC     |     | Power       |                 |                          |
| W05  | MA10#   | I   | AGTL+       |                 |                          |
| W06  | GND     |     | Power       |                 |                          |
| W07  | VTT     |     | Power       |                 |                          |
| W08  | VCC     |     | Power       |                 |                          |

Table 12-26: RCG Pin List Sorted by Pin (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| W09  | MA01#    | I   | AGTL+       |                 |                          |
| W10  | GND      |     | Power       |                 |                          |
| W11  | GND      |     | Power       |                 |                          |
| W12  | BANK2#   | I   | AGTL+       |                 |                          |
| W13  | VCC      |     | Power       |                 |                          |
| W14  | VTT      |     | Power       |                 |                          |
| W15  | GND      |     | Power       |                 |                          |
| W16  | N/C      |     |             |                 |                          |
| W17  | VCC      |     | Power       |                 |                          |
| W18  | VTT      |     | Power       |                 |                          |
| W19  | GND      |     | Power       |                 |                          |
| W20  | N/C      |     |             |                 |                          |
| Y01  | GND      |     | Power       |                 |                          |
| Y02  | N/C      |     |             |                 |                          |
| Y03  | MA13#    | I   | AGTL+       |                 |                          |
| Y04  | MA12#    | I   | AGTL+       |                 |                          |
| Y05  | MA11#    | I   | AGTL+       |                 |                          |
| Y06  | GND      |     | Power       |                 |                          |
| Y07  | MA08#    | I   | AGTL+       |                 |                          |
| Y08  | MA04#    | I   | AGTL+       |                 |                          |
| Y09  | MRESET#  | I   | AGTL+       |                 |                          |
| Y10  | VCC      |     | Power       |                 |                          |
| Y11  | ROW#     | I   | AGTL+       |                 |                          |
| Y12  | CMND0#   | I   | AGTL+       |                 |                          |
| Y13  | CARD#    | I   | AGTL+       |                 |                          |
| Y14  | GRCMPLT# | I/O | AGTL+       | 55ma            |                          |
| Y15  | GND      |     | Power       |                 |                          |
| Y16  | LDSTB#   | O   | AGTL+       | 55ma            |                          |
| Y17  | N/C      |     |             |                 |                          |
| Y18  | TMS      | I   | LVTTTL      |                 |                          |
| Y19  | N/C      |     |             |                 |                          |
| Y20  | GND      |     | Power       |                 |                          |

## 12.9.2 Pin Lists Sorted by Signal

Table 12-27: MIOC Pin List Sorted by Signal

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| B04  | A03#   | I/O | AGTL+       | 55ma            |                          |
| C04  | A04#   | I/O | AGTL+       | 55ma            |                          |
| D04  | A05#   | I/O | AGTL+       | 55ma            |                          |
| E04  | A06#   | I/O | AGTL+       | 55ma            |                          |
| A05  | A07#   | I/O | AGTL+       | 55ma            |                          |
| C05  | A08#   | I/O | AGTL+       | 55ma            |                          |
| E05  | A09#   | I/O | AGTL+       | 55ma            |                          |
| B06  | A10#   | I/O | AGTL+       | 55ma            |                          |
| C06  | A11#   | I/O | AGTL+       | 55ma            |                          |
| D06  | A12#   | I/O | AGTL+       | 55ma            |                          |
| A07  | A13#   | I/O | AGTL+       | 55ma            |                          |
| B07  | A14#   | I/O | AGTL+       | 55ma            |                          |
| C07  | A15#   | I/O | AGTL+       | 55ma            |                          |
| D07  | A16#   | I/O | AGTL+       | 55ma            |                          |
| E07  | A17#   | I/O | AGTL+       | 55ma            |                          |
| C08  | A18#   | I/O | AGTL+       | 55ma            |                          |
| E08  | A19#   | I/O | AGTL+       | 55ma            |                          |
| A09  | A20#   | I/O | AGTL+       | 55ma            |                          |
| B09  | A21#   | I/O | AGTL+       | 55ma            |                          |
| C09  | A22#   | I/O | AGTL+       | 55ma            |                          |
| D09  | A23#   | I/O | AGTL+       | 55ma            |                          |
| B10  | A24#   | I/O | AGTL+       | 55ma            |                          |
| D10  | A25#   | I/O | AGTL+       | 55ma            |                          |
| E10  | A26#   | I/O | AGTL+       | 55ma            |                          |
| B11  | A27#   | I/O | AGTL+       | 55ma            |                          |
| D11  | A28#   | I/O | AGTL+       | 55ma            |                          |
| A12  | A29#   | I/O | AGTL+       | 55ma            |                          |
| B12  | A30#   | I/O | AGTL+       | 55ma            |                          |
| C12  | A31#   | I/O | AGTL+       | 55ma            |                          |
| D12  | A32#   | I/O | AGTL+       | 55ma            |                          |
| E12  | A33#   | I/O | AGTL+       | 55ma            |                          |
| A13  | A34#   | I/O | AGTL+       | 55ma            |                          |
| B13  | A35#   | I/O | AGTL+       | 55ma            |                          |
| J03  | ADS#   | I/O | AGTL+       | 55ma            |                          |
| K05  | AERR#  | I/O | AGTL+       | 55ma            |                          |
| H01  | AP0#   | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| J01  | AP1#    | I/O | AGTL+       | 55ma            |                          |
| AJ17 | BANK0#  | O   | AGTL+       | 55ma            |                          |
| AH18 | BANK1#  | O   | AGTL+       | 55ma            |                          |
| AM18 | BANK2#  | O   | AGTL+       | 55ma            |                          |
| D13  | BERR#   | I/O | AGTL+       | 55ma            |                          |
| J29  | BINIT#  | I/O | AGTL+       | 55ma            |                          |
| C02  | BNR#    | I/O | AGTL+       | 55ma            |                          |
| J30  | BP0#    | I/O | OD          | 14ma            |                          |
| J31  | BP1#    | I/O | OD          | 14ma            |                          |
| D01  | BPRI#   | I/O | AGTL+       | 55ma            |                          |
| J02  | BR0#    | O   | AGTL+       | 55ma            |                          |
| AL18 | CARD0#  | O   | AGTL+       | 55ma            |                          |
| AJ18 | CARD1#  | O   | AGTL+       | 55ma            |                          |
| AL11 | CMND0#  | O   | AGTL+       | 55ma            |                          |
| AJ12 | CMND1#  | O   | AGTL+       | 55ma            |                          |
| C11  | CRES0   | I   | Analog      |                 |                          |
| A17  | CRES1   | I   | Analog      |                 |                          |
| H29  | CRESET# | O   | LVTTTL      | 10ma            |                          |
| AM12 | CSTB#   | O   | AGTL+       | 55ma            |                          |
| D14  | D00#    | I/O | AGTL+       | 55ma            |                          |
| A15  | D01#    | I/O | AGTL+       | 55ma            |                          |
| B15  | D02#    | I/O | AGTL+       | 55ma            |                          |
| C15  | D03#    | I/O | AGTL+       | 55ma            |                          |
| D15  | D04#    | I/O | AGTL+       | 55ma            |                          |
| E15  | D05#    | I/O | AGTL+       | 55ma            |                          |
| B16  | D06#    | I/O | AGTL+       | 55ma            |                          |
| D16  | D07#    | I/O | AGTL+       | 55ma            |                          |
| E16  | D08#    | I/O | AGTL+       | 55ma            |                          |
| B17  | D09#    | I/O | AGTL+       | 55ma            |                          |
| D17  | D10#    | I/O | AGTL+       | 55ma            |                          |
| E17  | D11#    | I/O | AGTL+       | 55ma            |                          |
| A18  | D12#    | I/O | AGTL+       | 55ma            |                          |
| B18  | D13#    | I/O | AGTL+       | 55ma            |                          |
| C18  | D14#    | I/O | AGTL+       | 55ma            |                          |
| D18  | D15#    | I/O | AGTL+       | 55ma            |                          |
| E18  | D16#    | I/O | AGTL+       | 55ma            |                          |
| B19  | D17#    | I/O | AGTL+       | 55ma            |                          |
| D19  | D18#    | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A20  | D19#   | I/O | AGTL+       | 55ma            |                          |
| B20  | D20#   | I/O | AGTL+       | 55ma            |                          |
| D20  | D21#   | I/O | AGTL+       | 55ma            |                          |
| A21  | D22#   | I/O | AGTL+       | 55ma            |                          |
| B21  | D23#   | I/O | AGTL+       | 55ma            |                          |
| C21  | D24#   | I/O | AGTL+       | 55ma            |                          |
| D21  | D25#   | I/O | AGTL+       | 55ma            |                          |
| E21  | D26#   | I/O | AGTL+       | 55ma            |                          |
| B22  | D27#   | I/O | AGTL+       | 55ma            |                          |
| D22  | D28#   | I/O | AGTL+       | 55ma            |                          |
| B23  | D29#   | I/O | AGTL+       | 55ma            |                          |
| D23  | D30#   | I/O | AGTL+       | 55ma            |                          |
| E23  | D31#   | I/O | AGTL+       | 55ma            |                          |
| A24  | D32#   | I/O | AGTL+       | 55ma            |                          |
| B24  | D33#   | I/O | AGTL+       | 55ma            |                          |
| C24  | D34#   | I/O | AGTL+       | 55ma            |                          |
| D24  | D35#   | I/O | AGTL+       | 55ma            |                          |
| C25  | D36#   | I/O | AGTL+       | 55ma            |                          |
| E25  | D37#   | I/O | AGTL+       | 55ma            |                          |
| A26  | D38#   | I/O | AGTL+       | 55ma            |                          |
| B26  | D39#   | I/O | AGTL+       | 55ma            |                          |
| C26  | D40#   | I/O | AGTL+       | 55ma            |                          |
| D26  | D41#   | I/O | AGTL+       | 55ma            |                          |
| E26  | D42#   | I/O | AGTL+       | 55ma            |                          |
| B27  | D43#   | I/O | AGTL+       | 55ma            |                          |
| C27  | D44#   | I/O | AGTL+       | 55ma            |                          |
| D27  | D45#   | I/O | AGTL+       | 55ma            |                          |
| A28  | D46#   | I/O | AGTL+       | 55ma            |                          |
| C28  | D47#   | I/O | AGTL+       | 55ma            |                          |
| E28  | D48#   | I/O | AGTL+       | 55ma            |                          |
| A29  | D49#   | I/O | AGTL+       | 55ma            |                          |
| B29  | D50#   | I/O | AGTL+       | 55ma            |                          |
| C29  | D51#   | I/O | AGTL+       | 55ma            |                          |
| D29  | D52#   | I/O | AGTL+       | 55ma            |                          |
| E29  | D53#   | I/O | AGTL+       | 55ma            |                          |
| B30  | D54#   | I/O | AGTL+       | 55ma            |                          |
| C30  | D55#   | I/O | AGTL+       | 55ma            |                          |
| E30  | D56#   | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| C31  | D57#     | I/O | AGTL+       | 55ma            |                          |
| D31  | D58#     | I/O | AGTL+       | 55ma            |                          |
| E31  | D59#     | I/O | AGTL+       | 55ma            |                          |
| D32  | D60#     | I/O | AGTL+       | 55ma            |                          |
| E32  | D61#     | I/O | AGTL+       | 55ma            |                          |
| F29  | D62#     | I/O | AGTL+       | 55ma            |                          |
| F30  | D63#     | I/O | AGTL+       | 55ma            |                          |
| A04  | DBSY#    | I/O | AGTL+       | 55ma            |                          |
| AJ16 | DCMPLTA# | I/O | AGTL+       | 55ma            |                          |
| AH15 | DCMPLTB# | I/O | AGTL+       | 55ma            |                          |
| G05  | DEFER#   | I/O | AGTL+       | 55ma            |                          |
| H32  | DEP0#    | I/O | AGTL+       | 55ma            |                          |
| H31  | DEP1#    | I/O | AGTL+       | 55ma            |                          |
| H30  | DEP2#    | I/O | AGTL+       | 55ma            |                          |
| G32  | DEP3#    | I/O | AGTL+       | 55ma            |                          |
| G31  | DEP4#    | I/O | AGTL+       | 55ma            |                          |
| G29  | DEP5#    | I/O | AGTL+       | 55ma            |                          |
| G28  | DEP6#    | I/O | AGTL+       | 55ma            |                          |
| F31  | DEP7#    | I/O | AGTL+       | 55ma            |                          |
| AH12 | DOFF0#   | O   | AGTL+       | 55ma            |                          |
| AM13 | DOFF1#   | O   | AGTL+       | 55ma            |                          |
| B14  | DRDY#    | I/O | AGTL+       | 55ma            |                          |
| AJ13 | DSEL0#   | O   | AGTL+       | 55ma            |                          |
| AL14 | DSEL1#   | O   | AGTL+       | 55ma            |                          |
| U02  | DSTBN0#  | I/O | AGTL+       | 55ma            |                          |
| AD01 | DSTBN1#  | I/O | AGTL+       | 55ma            |                          |
| AJ02 | DSTBN2#  | I/O | AGTL+       | 55ma            |                          |
| AH09 | DSTBN3#  | I/O | AGTL+       | 55ma            |                          |
| U01  | DSTBP0#  | I/O | AGTL+       | 55ma            |                          |
| AC04 | DSTBP1#  | I/O | AGTL+       | 55ma            |                          |
| AJ01 | DSTBP2#  | I/O | AGTL+       | 55ma            |                          |
| AK08 | DSTBP3#  | I/O | AGTL+       | 55ma            |                          |
| AK15 | DVALIDA# | O   | AGTL+       | 55ma            |                          |
| AL16 | DVALIDB# | O   | AGTL+       | 55ma            |                          |
| K01  | ERR0#    | I/O | OD          | 14ma            |                          |
| K02  | ERR1#    | I/O | OD          | 14ma            |                          |
| A01  | GND      |     | Power       |                 |                          |
| A02  | GND      |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A03  | GND    |     | Power       |                 |                          |
| A06  | GND    |     | Power       |                 |                          |
| A10  | GND    |     | Power       |                 |                          |
| A11  | GND    |     | Power       |                 |                          |
| A14  | GND    |     | Power       |                 |                          |
| A16  | GND    |     | Power       |                 |                          |
| A19  | GND    |     | Power       |                 |                          |
| A22  | GND    |     | Power       |                 |                          |
| A23  | GND    |     | Power       |                 |                          |
| A27  | GND    |     | Power       |                 |                          |
| B01  | GND    |     | Power       |                 |                          |
| B02  | GND    |     | Power       |                 |                          |
| B05  | GND    |     | Power       |                 |                          |
| B28  | GND    |     | Power       |                 |                          |
| C01  | GND    |     | Power       |                 |                          |
| D08  | GND    |     | Power       |                 |                          |
| D25  | GND    |     | Power       |                 |                          |
| E09  | GND    |     | Power       |                 |                          |
| E13  | GND    |     | Power       |                 |                          |
| E14  | GND    |     | Power       |                 |                          |
| E19  | GND    |     | Power       |                 |                          |
| E20  | GND    |     | Power       |                 |                          |
| E24  | GND    |     | Power       |                 |                          |
| F01  | GND    |     | Power       |                 |                          |
| F32  | GND    |     | Power       |                 |                          |
| G01  | GND    |     | Power       |                 |                          |
| H05  | GND    |     | Power       |                 |                          |
| H28  | GND    |     | Power       |                 |                          |
| J05  | GND    |     | Power       |                 |                          |
| J32  | GND    |     | Power       |                 |                          |
| L01  | GND    |     | Power       |                 |                          |
| L32  | GND    |     | Power       |                 |                          |
| M05  | GND    |     | Power       |                 |                          |
| M28  | GND    |     | Power       |                 |                          |
| R01  | GND    |     | Power       |                 |                          |
| R29  | GND    |     | Power       |                 |                          |
| T28  | GND    |     | Power       |                 |                          |
| U04  | GND    |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| U05  | GND    |     | Power       |                 |                          |
| U32  | GND    |     | Power       |                 |                          |
| V04  | GND    |     | Power       |                 |                          |
| V05  | GND    |     | Power       |                 |                          |
| V32  | GND    |     | Power       |                 |                          |
| W05  | GND    |     | Power       |                 |                          |
| Y28  | GND    |     | Power       |                 |                          |
| AA05 | GND    |     | Power       |                 |                          |
| AA28 | GND    |     | Power       |                 |                          |
| AB01 | GND    |     | Power       |                 |                          |
| AB32 | GND    |     | Power       |                 |                          |
| AC01 | GND    |     | Power       |                 |                          |
| AC05 | GND    |     | Power       |                 |                          |
| AC28 | GND    |     | Power       |                 |                          |
| AD05 | GND    |     | Power       |                 |                          |
| AD28 | GND    |     | Power       |                 |                          |
| AE01 | GND    |     | Power       |                 |                          |
| AE32 | GND    |     | Power       |                 |                          |
| AF01 | GND    |     | Power       |                 |                          |
| AF32 | GND    |     | Power       |                 |                          |
| AH13 | GND    |     | Power       |                 |                          |
| AH14 | GND    |     | Power       |                 |                          |
| AH19 | GND    |     | Power       |                 |                          |
| AH20 | GND    |     | Power       |                 |                          |
| AH24 | GND    |     | Power       |                 |                          |
| AH25 | GND    |     | Power       |                 |                          |
| AH32 | GND    |     | Power       |                 |                          |
| AJ08 | GND    |     | Power       |                 |                          |
| AJ19 | GND    |     | Power       |                 |                          |
| AJ24 | GND    |     | Power       |                 |                          |
| AJ25 | GND    |     | Power       |                 |                          |
| AJ26 | GND    |     | Power       |                 |                          |
| AK24 | GND    |     | Power       |                 |                          |
| AK25 | GND    |     | Power       |                 |                          |
| AK27 | GND    |     | Power       |                 |                          |
| AK32 | GND    |     | Power       |                 |                          |
| AL05 | GND    |     | Power       |                 |                          |
| AL27 | GND    |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| AL28 | GND     |     | Power       |                 |                          |
| AL31 | GND     |     | Power       |                 |                          |
| AL32 | GND     |     | Power       |                 |                          |
| AM06 | GND     |     | Power       |                 |                          |
| AM11 | GND     |     | Power       |                 |                          |
| AM14 | GND     |     | Power       |                 |                          |
| AM16 | GND     |     | Power       |                 |                          |
| AM19 | GND     |     | Power       |                 |                          |
| AM22 | GND     |     | Power       |                 |                          |
| AM23 | GND     |     | Power       |                 |                          |
| AM27 | GND     |     | Power       |                 |                          |
| AM28 | GND     |     | Power       |                 |                          |
| AM30 | GND     |     | Power       |                 |                          |
| AM31 | GND     |     | Power       |                 |                          |
| AM32 | GND     |     | Power       |                 |                          |
| R28  | HCLKIN  | I   | 2.5V        |                 |                          |
| G02  | HIT#    | I   | AGTL+       |                 |                          |
| H02  | HITM#   |     | AGTL+       |                 |                          |
| N29  | INIT#   | OD  | 2.5V        | 14ma            |                          |
| L04  | INTREQ# | O   | LVTTL       | 10ma            |                          |
| N05  | IOGNT#  | I   | LVTTL       |                 |                          |
| N04  | IOREQ#  | O   | LVTTL       | 10ma            |                          |
| F03  | LOCK#   | I   | AGTL+       |                 |                          |
| AM20 | MA00#   | O   | AGTL+       | 55ma            |                          |
| AL20 | MA01#   | O   | AGTL+       | 55ma            |                          |
| AJ20 | MA02#   | O   | AGTL+       | 55ma            |                          |
| AM21 | MA03#   | O   | AGTL+       | 55ma            |                          |
| AL21 | MA04#   | O   | AGTL+       | 55ma            |                          |
| AK21 | MA05#   | O   | AGTL+       | 55ma            |                          |
| AJ21 | MA06#   | O   | AGTL+       | 55ma            |                          |
| AH21 | MA07#   | O   | AGTL+       | 55ma            |                          |
| AL22 | MA08#   | O   | AGTL+       | 55ma            |                          |
| AJ22 | MA09#   | O   | AGTL+       | 55ma            |                          |
| AL23 | MA10#   | O   | AGTL+       | 55ma            |                          |
| AJ23 | MA11#   | O   | AGTL+       | 55ma            |                          |
| AH23 | MA12#   | O   | AGTL+       | 55ma            |                          |
| AM24 | MA13#   | O   | AGTL+       | 55ma            |                          |
| P02  | MD00#   | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| P03  | MD01#  | I/O | AGTL+       | 55ma            |                          |
| P04  | MD02#  | I/O | AGTL+       | 55ma            |                          |
| R02  | MD03#  | I/O | AGTL+       | 55ma            |                          |
| R03  | MD04#  | I/O | AGTL+       | 55ma            |                          |
| T01  | MD05#  | I/O | AGTL+       | 55ma            |                          |
| T02  | MD06#  | I/O | AGTL+       | 55ma            |                          |
| T03  | MD07#  | I/O | AGTL+       | 55ma            |                          |
| T04  | MD08#  | I/O | AGTL+       | 55ma            |                          |
| U03  | MD09#  | I/O | AGTL+       | 55ma            |                          |
| V02  | MD10#  | I/O | AGTL+       | 55ma            |                          |
| V03  | MD11#  | I/O | AGTL+       | 55ma            |                          |
| W01  | MD12#  | I/O | AGTL+       | 55ma            |                          |
| W02  | MD13#  | I/O | AGTL+       | 55ma            |                          |
| W03  | MD14#  | I/O | AGTL+       | 55ma            |                          |
| W04  | MD15#  | I/O | AGTL+       | 55ma            |                          |
| Y02  | MD16#  | I/O | AGTL+       | 55ma            |                          |
| Y04  | MD17#  | I/O | AGTL+       | 55ma            |                          |
| Y05  | MD18#  | I/O | AGTL+       | 55ma            |                          |
| AA01 | MD19#  | I/O | AGTL+       | 55ma            |                          |
| AA02 | MD20#  | I/O | AGTL+       | 55ma            |                          |
| AA03 | MD21#  | I/O | AGTL+       | 55ma            |                          |
| AA04 | MD22#  | I/O | AGTL+       | 55ma            |                          |
| AB02 | MD23#  | I/O | AGTL+       | 55ma            |                          |
| AB04 | MD24#  | I/O | AGTL+       | 55ma            |                          |
| AB05 | MD25#  | I/O | AGTL+       | 55ma            |                          |
| AC02 | MD26#  | I/O | AGTL+       | 55ma            |                          |
| AD02 | MD27#  | I/O | AGTL+       | 55ma            |                          |
| AD03 | MD28#  | I/O | AGTL+       | 55ma            |                          |
| AD04 | MD29#  | I/O | AGTL+       | 55ma            |                          |
| AE02 | MD30#  | I/O | AGTL+       | 55ma            |                          |
| AE04 | MD31#  | I/O | AGTL+       | 55ma            |                          |
| AE05 | MD32#  | I/O | AGTL+       | 55ma            |                          |
| AF02 | MD33#  | I/O | AGTL+       | 55ma            |                          |
| AF04 | MD34#  | I/O | AGTL+       | 55ma            |                          |
| AF05 | MD35#  | I/O | AGTL+       | 55ma            |                          |
| AG01 | MD36#  | I/O | AGTL+       | 55ma            |                          |
| AG02 | MD37#  | I/O | AGTL+       | 55ma            |                          |
| AG03 | MD38#  | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| AG04 | MD39#   | I/O | AGTL+       | 55ma            |                          |
| AH01 | MD40#   | I/O | AGTL+       | 55ma            |                          |
| AH02 | MD41#   | I/O | AGTL+       | 55ma            |                          |
| AH03 | MD42#   | I/O | AGTL+       | 55ma            |                          |
| AH04 | MD43#   | I/O | AGTL+       | 55ma            |                          |
| AH05 | MD44#   | I/O | AGTL+       | 55ma            |                          |
| AJ04 | MD45#   | I/O | AGTL+       | 55ma            |                          |
| AK02 | MD46#   | I/O | AGTL+       | 55ma            |                          |
| AK03 | MD47#   | I/O | AGTL+       | 55ma            |                          |
| AK04 | MD48#   | I/O | AGTL+       | 55ma            |                          |
| AK05 | MD49#   | I/O | AGTL+       | 55ma            |                          |
| AL03 | MD50#   | I/O | AGTL+       | 55ma            |                          |
| AL04 | MD51#   | I/O | AGTL+       | 55ma            |                          |
| AM04 | MD52#   | I/O | AGTL+       | 55ma            |                          |
| AM05 | MD53#   | I/O | AGTL+       | 55ma            |                          |
| AJ06 | MD54#   | I/O | AGTL+       | 55ma            |                          |
| AK06 | MD55#   | I/O | AGTL+       | 55ma            |                          |
| AL06 | MD56#   | I/O | AGTL+       | 55ma            |                          |
| AH07 | MD57#   | I/O | AGTL+       | 55ma            |                          |
| AJ07 | MD58#   | I/O | AGTL+       | 55ma            |                          |
| AK07 | MD59#   | I/O | AGTL+       | 55ma            |                          |
| AL07 | MD60#   | I/O | AGTL+       | 55ma            |                          |
| AM07 | MD61#   | I/O | AGTL+       | 55ma            |                          |
| AH08 | MD62#   | I/O | AGTL+       | 55ma            |                          |
| AJ09 | MD63#   | I/O | AGTL+       | 55ma            |                          |
| AK09 | MD64#   | I/O | AGTL+       | 55ma            |                          |
| AL09 | MD65#   | I/O | AGTL+       | 55ma            |                          |
| AM09 | MD66#   | I/O | AGTL+       | 55ma            |                          |
| AJ10 | MD67#   | I/O | AGTL+       | 55ma            |                          |
| AK10 | MD68#   | I/O | AGTL+       | 55ma            |                          |
| AL10 | MD69#   | I/O | AGTL+       | 55ma            |                          |
| AM10 | MD70#   | I/O | AGTL+       | 55ma            |                          |
| AJ11 | MD71#   | I/O | AGTL+       | 55ma            |                          |
| AL13 | MRESET# | O   | AGTL+       | 55ma            |                          |
| C23  | N/C     |     |             |                 |                          |
| K29  | N/C     |     |             |                 |                          |
| U28  | N/C     |     |             |                 |                          |
| AC32 | VCC     |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| AK13 | PHITA#   | I   | AGTL+       |                 |                          |
| AL17 | PHITB#   | I   | AGTL+       |                 |                          |
| L31  | PWRGD    | I   | LVTTTL      |                 |                          |
| P28  | PWRGDB   | O   | LVTTTL      | 10ma            |                          |
| AM15 | RCMPLTA# | I   | AGTL+       |                 |                          |
| AJ15 | RCMPLTB# | I   | AGTL+       |                 |                          |
| E01  | REQ0#    | I/O | AGTL+       | 55ma            |                          |
| F04  | REQ1#    | I/O | AGTL+       | 55ma            |                          |
| G04  | REQ2#    | I/O | AGTL+       | 55ma            |                          |
| H04  | REQ3#    | I/O | AGTL+       | 55ma            |                          |
| F02  | REQ4#    | I/O | AGTL+       | 55ma            |                          |
| M29  | RESET#   | I/O | AGTL+       | 55ma            |                          |
| AL12 | RHITA#   | I   | AGTL+       |                 |                          |
| AM17 | RHITB#   | I   | AGTL+       |                 |                          |
| AH16 | ROW#     | O   | AGTL+       | 55ma            |                          |
| J04  | RP#      | I/O | AGTL+       | 55ma            |                          |
| B03  | RS0#     | I/O | AGTL+       | 55ma            |                          |
| C03  | RS1#     | I/O | AGTL+       | 55ma            |                          |
| E03  | RS2#     | I/O | AGTL+       | 55ma            |                          |
| E02  | RSP#     | I/O | AGTL+       | 55ma            |                          |
| AL19 | SMIACT#  | O   | LVTTTL      | 10ma            |                          |
| L03  | TCK      | I   | LVTTTL      |                 |                          |
| M04  | TDI      | I   | LVTTTL      |                 |                          |
| M03  | TDO      | O   | OD          | 14ma            |                          |
| L05  | TMS      | I   | LVTTTL      |                 |                          |
| M01  | TPCTL0   | I   | LVTTTL      |                 |                          |
| N02  | TPCTL1   | I   | LVTTTL      |                 |                          |
| D02  | TRDY#    | I/O | AGTL+       | 55ma            |                          |
| L02  | TRST#    | I   | LVTTTL      |                 |                          |
| A30  | VCC      |     | Power       |                 |                          |
| A31  | VCC      |     | Power       |                 |                          |
| A32  | VCC      |     | Power       |                 |                          |
| B31  | VCC      |     | Power       |                 |                          |
| B32  | VCC      |     | Power       |                 |                          |
| C10  | VCC      |     | Power       |                 |                          |
| C13  | VCC      |     | Power       |                 |                          |
| C14  | VCC      |     | Power       |                 |                          |
| C19  | VCC      |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| C20  | VCC    |     | Power       |                 |                          |
| C22  | VCC    |     | Power       |                 |                          |
| C32  | VCC    |     | Power       |                 |                          |
| E06  | VCC    |     | Power       |                 |                          |
| E27  | VCC    |     | Power       |                 |                          |
| F05  | VCC    |     | Power       |                 |                          |
| F28  | VCC    |     | Power       |                 |                          |
| K03  | VCC    |     | Power       |                 |                          |
| K28  | VCC    |     | Power       |                 |                          |
| L30  | VCC    |     | Power       |                 |                          |
| M02  | VCC    |     | Power       |                 |                          |
| N01  | VCC    |     | Power       |                 |                          |
| N32  | VCC    |     | Power       |                 |                          |
| P01  | VCC    |     | Power       |                 |                          |
| P05  | VCC    |     | Power       |                 |                          |
| P32  | VCC    |     | Power       |                 |                          |
| R04  | VCC    |     | Power       |                 |                          |
| R05  | VCC    |     | Power       |                 |                          |
| T05  | VCC    |     | Power       |                 |                          |
| V01  | VCC    |     | Power       |                 |                          |
| V28  | VCC    |     | Power       |                 |                          |
| V29  | VCC    |     | Power       |                 |                          |
| W28  | VCC    |     | Power       |                 |                          |
| Y01  | VCC    |     | Power       |                 |                          |
| Y32  | VCC    |     | Power       |                 |                          |
| AB03 | VCC    |     | Power       |                 |                          |
| AB30 | VCC    |     | Power       |                 |                          |
| AC30 | VCC    |     | Power       |                 |                          |
| AF28 | VCC    |     | Power       |                 |                          |
| AG05 | VCC    |     | Power       |                 |                          |
| AG28 | VCC    |     | Power       |                 |                          |
| AH06 | VCC    |     | Power       |                 |                          |
| AH10 | VCC    |     | Power       |                 |                          |
| AH11 | VCC    |     | Power       |                 |                          |
| AH17 | VCC    |     | Power       |                 |                          |
| AH27 | VCC    |     | Power       |                 |                          |
| AK01 | VCC    |     | Power       |                 |                          |
| AK11 | VCC    |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| AK12 | VCC    |     | Power       |                 |                          |
| AK14 | VCC    |     | Power       |                 |                          |
| AK18 | VCC    |     | Power       |                 |                          |
| AK19 | VCC    |     | Power       |                 |                          |
| AK20 | VCC    |     | Power       |                 |                          |
| AK22 | VCC    |     | Power       |                 |                          |
| AK23 | VCC    |     | Power       |                 |                          |
| AL01 | VCC    |     | Power       |                 |                          |
| AL02 | VCC    |     | Power       |                 |                          |
| AL24 | VCC    |     | Power       |                 |                          |
| AM01 | VCC    |     | Power       |                 |                          |
| AM02 | VCC    |     | Power       |                 |                          |
| AM03 | VCC    |     | Power       |                 |                          |
| K30  | VCCA0  |     | Power       |                 |                          |
| K31  | VCCA1  |     | Power       |                 |                          |
| K32  | VCCA2  |     | Power       |                 |                          |
| K04  | VREF   | I   | Analog      |                 |                          |
| N31  | VREF   | I   | Analog      |                 |                          |
| U30  | VREF   | I   | Analog      |                 |                          |
| AC03 | VREF   | I   | Analog      |                 |                          |
| AG29 | VREF   | I   | Analog      |                 |                          |
| AL15 | VREF   | I   | Analog      |                 |                          |
| A08  | VTT    |     | Power       |                 |                          |
| A25  | VTT    |     | Power       |                 |                          |
| B08  | VTT    |     | Power       |                 |                          |
| B25  | VTT    |     | Power       |                 |                          |
| C16  | VTT    |     | Power       |                 |                          |
| C17  | VTT    |     | Power       |                 |                          |
| D03  | VTT    |     | Power       |                 |                          |
| D05  | VTT    |     | Power       |                 |                          |
| D28  | VTT    |     | Power       |                 |                          |
| D30  | VTT    |     | Power       |                 |                          |
| E11  | VTT    |     | Power       |                 |                          |
| E22  | VTT    |     | Power       |                 |                          |
| G03  | VTT    |     | Power       |                 |                          |
| G30  | VTT    |     | Power       |                 |                          |
| H03  | VTT    |     | Power       |                 |                          |
| N03  | VTT    |     | Power       |                 |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| Y03  | VTT     |     | Power       |                 |                          |
| Y30  | VTT     |     | Power       |                 |                          |
| AE03 | VTT     |     | Power       |                 |                          |
| AE30 | VTT     |     | Power       |                 |                          |
| AF03 | VTT     |     | Power       |                 |                          |
| AF30 | VTT     |     | Power       |                 |                          |
| AH22 | VTT     |     | Power       |                 |                          |
| AJ03 | VTT     |     | Power       |                 |                          |
| AJ05 | VTT     |     | Power       |                 |                          |
| AJ28 | VTT     |     | Power       |                 |                          |
| AJ30 | VTT     |     | Power       |                 |                          |
| AK16 | VTT     |     | Power       |                 |                          |
| AK17 | VTT     |     | Power       |                 |                          |
| AL08 | VTT     |     | Power       |                 |                          |
| AL25 | VTT     |     | Power       |                 |                          |
| AL26 | VTT     |     | Power       |                 |                          |
| AM08 | VTT     |     | Power       |                 |                          |
| AM25 | VTT     |     | Power       |                 |                          |
| AM26 | VTT     |     | Power       |                 |                          |
| AJ14 | WDEVT#  | O   | AGTL+       | 55ma            |                          |
| R30  | X0ADS#  | I/O | AGTL+       | 55ma            |                          |
| P31  | X0BE0#  | I/O | AGTL+       | 55ma            |                          |
| P30  | X0BE1#  | I/O | AGTL+       | 55ma            |                          |
| R32  | X0BLK#  | O   | AGTL+       | 55ma            |                          |
| L28  | X0CLK   | O   | LVTTL       | 10ma            |                          |
| L29  | X0CLKB  | O   | LVTTL       | 10ma            |                          |
| J28  | X0CLKFB | I   | LVTTL       |                 |                          |
| T32  | X0D00#  | I/O | AGTL+       | 55ma            |                          |
| T31  | X0D01#  | I/O | AGTL+       | 55ma            |                          |
| T30  | X0D02#  | I/O | AGTL+       | 55ma            |                          |
| T29  | X0D03#  | I/O | AGTL+       | 55ma            |                          |
| U29  | X0D04#  | I/O | AGTL+       | 55ma            |                          |
| U31  | X0D05#  | I/O | AGTL+       | 55ma            |                          |
| Y31  | X0D06#  | I/O | AGTL+       | 55ma            |                          |
| Y29  | X0D07#  | I/O | AGTL+       | 55ma            |                          |
| AA32 | X0D08#  | I/O | AGTL+       | 55ma            |                          |
| AA31 | X0D09#  | I/O | AGTL+       | 55ma            |                          |
| AA30 | X0D10#  | I/O | AGTL+       | 55ma            |                          |

Table 12-27: MIOC Pin List Sorted by Signal (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| AA29 | X0D11#   | I/O | AGTL+       | 55ma            |                          |
| AB31 | X0D12#   | I/O | AGTL+       | 55ma            |                          |
| AB29 | X0D13#   | I/O | AGTL+       | 55ma            |                          |
| AB28 | X0D14#   | I/O | AGTL+       | 55ma            |                          |
| AC31 | X0D15#   | I/O | AGTL+       | 55ma            |                          |
| W30  | X0HRTS#  | O   | AGTL+       | 55ma            |                          |
| W31  | X0HSTBN# | O   | AGTL+       | 55ma            |                          |
| W32  | X0HSTBP# | O   | AGTL+       | 55ma            |                          |
| R31  | X0PAR#   | I/O | AGTL+       | 55ma            |                          |
| P29  | X0RST#   | O   | AGTL+       | 55ma            |                          |
| N30  | X0RSTB#  | O   | AGTL+       | 55ma            |                          |
| M32  | X0RSTFB# | I   | AGTL+       |                 |                          |
| W29  | X0XRTS#  | I   | AGTL+       |                 |                          |
| V30  | X0XSTBN# | I   | AGTL+       |                 |                          |
| V31  | X0XSTBP# | I   | AGTL+       |                 |                          |
| AD32 | X1ADS#   | I/O | AGTL+       | 55ma            |                          |
| AD30 | X1BE0#   | I/O | AGTL+       | 55ma            |                          |
| AD29 | X1BE1#   | I/O | AGTL+       | 55ma            |                          |
| AE28 | X1BLK#   | O   | AGTL+       | 55ma            |                          |
| M30  | X1CLK    | O   | LVTTL       | 10ma            |                          |
| M31  | X1CLKB   | O   | LVTTL       | 10ma            |                          |
| N28  | X1CLKFB  | I   | LVTTL       |                 |                          |
| AE31 | X1D00#   | I/O | AGTL+       | 55ma            |                          |
| AE29 | X1D01#   | I/O | AGTL+       | 55ma            |                          |
| AF31 | X1D02#   | I/O | AGTL+       | 55ma            |                          |
| AF29 | X1D03#   | I/O | AGTL+       | 55ma            |                          |
| AG31 | X1D04#   | I/O | AGTL+       | 55ma            |                          |
| AG30 | X1D05#   | I/O | AGTL+       | 55ma            |                          |
| AJ29 | X1D06#   | I/O | AGTL+       | 55ma            |                          |
| AK31 | X1D07#   | I/O | AGTL+       | 55ma            |                          |
| AK30 | X1D08#   | I/O | AGTL+       | 55ma            |                          |
| AK29 | X1D09#   | I/O | AGTL+       | 55ma            |                          |
| AK28 | X1D10#   | I/O | AGTL+       | 55ma            |                          |
| AL30 | X1D11#   | I/O | AGTL+       | 55ma            |                          |
| AL29 | X1D12#   | I/O | AGTL+       | 55ma            |                          |
| AJ27 | X1D13#   | I/O | AGTL+       | 55ma            |                          |
| AH26 | X1D14#   | I/O | AGTL+       | 55ma            |                          |
| AK26 | X1D15#   | I/O | AGTL+       | 55ma            |                          |

**Table 12-27: MIOC Pin List Sorted by Signal (Continued)**

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| AJ32 | X1HRYS#  | O   | AGTL+       | 55ma            |                          |
| AH28 | X1HSTBN# | O   | AGTL+       | 55ma            |                          |
| AH29 | X1HSTBP# | O   | AGTL+       | 55ma            |                          |
| AM29 | X1PAR#   | I/O | AGTL+       | 55ma            |                          |
| AC29 | X1RST#   | O   | AGTL+       | 55ma            |                          |
| AD31 | X1RSTB#  | O   | AGTL+       | 55ma            |                          |
| AG32 | X1RSTFB# | I   | AGTL+       |                 |                          |
| AJ31 | X1XRTS#  | I   | AGTL+       |                 |                          |
| AH30 | X1XSTBN# | I   | AGTL+       |                 |                          |
| AH31 | X1XSTBP# | I   | AGTL+       |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| AL17 | ACK64#  | I/O | PCI         |                 |                          |
| E09  | CRES0   | I   | Analog      |                 |                          |
| D09  | CRES1   | I   | Analog      |                 |                          |
| AL27 | INTRQA# | OD  | PCI         |                 |                          |
| AL7  | INTRQB# | OD  | PCI         |                 |                          |
| AJ26 | MODE64# | I   | PCI         |                 |                          |
| A01  | N/C     |     |             |                 |                          |
| A02  | N/C     |     |             |                 |                          |
| A11  | N/C     |     |             |                 |                          |
| A13  | N/C     |     |             |                 |                          |
| A23  | N/C     |     |             |                 |                          |
| A25  | N/C     |     |             |                 |                          |
| A30  | N/C     |     |             |                 |                          |
| A31  | N/C     |     |             |                 |                          |
| A32  | N/C     |     |             |                 |                          |
| B01  | N/C     |     |             |                 |                          |
| B05  | N/C     |     |             |                 |                          |
| B06  | N/C     |     |             |                 |                          |
| B07  | N/C     |     |             |                 |                          |
| B08  | N/C     |     |             |                 |                          |
| B09  | N/C     |     |             |                 |                          |
| B10  | N/C     |     |             |                 |                          |
| B11  | N/C     |     |             |                 |                          |
| B12  | N/C     |     |             |                 |                          |
| B13  | N/C     |     |             |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| B17  | N/C    |     |             |                 |                          |
| B23  | N/C    |     |             |                 |                          |
| B24  | N/C    |     |             |                 |                          |
| B25  | N/C    |     |             |                 |                          |
| B26  | N/C    |     |             |                 |                          |
| B27  | N/C    |     |             |                 |                          |
| B32  | N/C    |     |             |                 |                          |
| C01  | N/C    |     |             |                 |                          |
| C02  | N/C    |     |             |                 |                          |
| C03  | N/C    |     |             |                 |                          |
| C04  | N/C    |     |             |                 |                          |
| C05  | N/C    |     |             |                 |                          |
| C09  | N/C    |     |             |                 |                          |
| C11  | N/C    |     |             |                 |                          |
| C13  | N/C    |     |             |                 |                          |
| C23  | N/C    |     |             |                 |                          |
| C28  | N/C    |     |             |                 |                          |
| C29  | N/C    |     |             |                 |                          |
| C30  | N/C    |     |             |                 |                          |
| C31  | N/C    |     |             |                 |                          |
| C32  | N/C    |     |             |                 |                          |
| D01  | N/C    |     |             |                 |                          |
| D03  | N/C    |     |             |                 |                          |
| D05  | N/C    |     |             |                 |                          |
| D06  | N/C    |     |             |                 |                          |
| D07  | N/C    |     |             |                 |                          |
| D08  | N/C    |     |             |                 |                          |
| D10  | N/C    |     |             |                 |                          |
| D11  | N/C    |     |             |                 |                          |
| D12  | N/C    |     |             |                 |                          |
| D13  | N/C    |     |             |                 |                          |
| D14  | N/C    |     |             |                 |                          |
| D19  | N/C    |     |             |                 |                          |
| D23  | N/C    |     |             |                 |                          |
| D24  | N/C    |     |             |                 |                          |
| D25  | N/C    |     |             |                 |                          |
| D26  | N/C    |     |             |                 |                          |
| D30  | N/C    |     |             |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| D32  | N/C    |     |             |                 |                          |
| E01  | N/C    |     |             |                 |                          |
| E02  | N/C    |     |             |                 |                          |
| E03  | N/C    |     |             |                 |                          |
| E04  | N/C    |     |             |                 |                          |
| E05  | N/C    |     |             |                 |                          |
| E07  | N/C    |     |             |                 |                          |
| E11  | N/C    |     |             |                 |                          |
| E25  | N/C    |     |             |                 |                          |
| E28  | N/C    |     |             |                 |                          |
| E29  | N/C    |     |             |                 |                          |
| E30  | N/C    |     |             |                 |                          |
| E31  | N/C    |     |             |                 |                          |
| E32  | N/C    |     |             |                 |                          |
| F02  | N/C    |     |             |                 |                          |
| F04  | N/C    |     |             |                 |                          |
| F30  | N/C    |     |             |                 |                          |
| F32  | N/C    |     |             |                 |                          |
| G01  | N/C    |     |             |                 |                          |
| G02  | N/C    |     |             |                 |                          |
| G03  | N/C    |     |             |                 |                          |
| G04  | N/C    |     |             |                 |                          |
| G05  | N/C    |     |             |                 |                          |
| G28  | N/C    |     |             |                 |                          |
| G29  | N/C    |     |             |                 |                          |
| G32  | N/C    |     |             |                 |                          |
| H02  | N/C    |     |             |                 |                          |
| H04  | N/C    |     |             |                 |                          |
| H28  | N/C    |     |             |                 |                          |
| H29  | N/C    |     |             |                 |                          |
| H31  | N/C    |     |             |                 |                          |
| H32  | N/C    |     |             |                 |                          |
| J01  | N/C    |     |             |                 |                          |
| J02  | N/C    |     |             |                 |                          |
| J03  | N/C    |     |             |                 |                          |
| J04  | N/C    |     |             |                 |                          |
| J05  | N/C    |     |             |                 |                          |
| J28  | N/C    |     |             |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| J29  | N/C    |     |             |                 |                          |
| J31  | N/C    |     |             |                 |                          |
| K02  | N/C    |     |             |                 |                          |
| K04  | N/C    |     |             |                 |                          |
| K31  | N/C    |     |             |                 |                          |
| L28  | N/C    |     |             |                 |                          |
| L29  | N/C    |     |             |                 |                          |
| L31  | N/C    |     |             |                 |                          |
| M02  | N/C    |     |             |                 |                          |
| M31  | N/C    |     |             |                 |                          |
| N28  | N/C    |     |             |                 |                          |
| N29  | N/C    |     |             |                 |                          |
| N30  | N/C    |     |             |                 |                          |
| N31  | N/C    |     |             |                 |                          |
| N32  | N/C    |     |             |                 |                          |
| P02  | N/C    |     |             |                 |                          |
| P04  | N/C    |     |             |                 |                          |
| P29  | N/C    |     |             |                 |                          |
| P31  | N/C    |     |             |                 |                          |
| R02  | N/C    |     |             |                 |                          |
| R04  | N/C    |     |             |                 |                          |
| R29  | N/C    |     |             |                 |                          |
| R31  | N/C    |     |             |                 |                          |
| T02  | N/C    |     |             |                 |                          |
| T04  | N/C    |     |             |                 |                          |
| T29  | N/C    |     |             |                 |                          |
| T31  | N/C    |     |             |                 |                          |
| U01  | N/C    |     |             |                 |                          |
| U02  | N/C    |     |             |                 |                          |
| U03  | N/C    |     |             |                 |                          |
| U04  | N/C    |     |             |                 |                          |
| U05  | N/C    |     |             |                 |                          |
| U28  | N/C    |     |             |                 |                          |
| U29  | N/C    |     |             |                 |                          |
| U31  | N/C    |     |             |                 |                          |
| V02  | N/C    |     |             |                 |                          |
| V04  | N/C    |     |             |                 |                          |
| V29  | N/C    |     |             |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| V31  | N/C    |     |             |                 |                          |
| AH01 | N/C    |     |             |                 |                          |
| AH02 | N/C    |     |             |                 |                          |
| AH05 | N/C    |     |             |                 |                          |
| AH06 | N/C    |     |             |                 |                          |
| AH28 | N/C    |     |             |                 |                          |
| AH31 | N/C    |     |             |                 |                          |
| AH32 | N/C    |     |             |                 |                          |
| AJ01 | N/C    |     |             |                 |                          |
| AJ02 | N/C    |     |             |                 |                          |
| AJ03 | N/C    |     |             |                 |                          |
| AJ05 | N/C    |     |             |                 |                          |
| AJ06 | N/C    |     |             |                 |                          |
| AJ08 | N/C    |     |             |                 |                          |
| AJ28 | N/C    |     |             |                 |                          |
| AJ30 | N/C    |     |             |                 |                          |
| AJ31 | N/C    |     |             |                 |                          |
| AJ32 | N/C    |     |             |                 |                          |
| AK01 | N/C    |     |             |                 |                          |
| AK03 | N/C    |     |             |                 |                          |
| AK05 | N/C    |     |             |                 |                          |
| AK06 | N/C    |     |             |                 |                          |
| AK08 | N/C    |     |             |                 |                          |
| AK28 | N/C    |     |             |                 |                          |
| AK30 | N/C    |     |             |                 |                          |
| AK32 | N/C    |     |             |                 |                          |
| AL01 | N/C    |     |             |                 |                          |
| AL02 | N/C    |     |             |                 |                          |
| AL03 | N/C    |     |             |                 |                          |
| AL04 | N/C    |     |             |                 |                          |
| AL05 | N/C    |     |             |                 |                          |
| AL06 | N/C    |     |             |                 |                          |
| AL08 | N/C    |     |             |                 |                          |
| AL28 | N/C    |     |             |                 |                          |
| AL29 | N/C    |     |             |                 |                          |
| AL30 | N/C    |     |             |                 |                          |
| AL31 | N/C    |     |             |                 |                          |
| AL32 | N/C    |     |             |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| AM01 | N/C      |     |             |                 |                          |
| AM02 | N/C      |     |             |                 |                          |
| AM06 | N/C      |     |             |                 |                          |
| AM08 | N/C      |     |             |                 |                          |
| AM10 | N/C      |     |             |                 |                          |
| AM24 | N/C      |     |             |                 |                          |
| AM31 | N/C      |     |             |                 |                          |
| K29  | N/C      |     |             |                 |                          |
| M29  | N/C      |     |             |                 |                          |
| F31  | N/C      |     |             |                 |                          |
| AG28 | PAAD[00] | I/O | PCI         |                 |                          |
| AG29 | PAAD[01] | I/O | PCI         |                 |                          |
| AG30 | PAAD[02] | I/O | PCI         |                 |                          |
| AG31 | PAAD[03] | I/O | PCI         |                 |                          |
| AG32 | PAAD[04] | I/O | PCI         |                 |                          |
| AF29 | PAAD[05] | I/O | PCI         |                 |                          |
| AF31 | PAAD[06] | I/O | PCI         |                 |                          |
| AE28 | PAAD[07] | I/O | PCI         |                 |                          |
| AE29 | PAAD[08] | I/O | PCI         |                 |                          |
| AE30 | PAAD[09] | I/O | PCI         |                 |                          |
| AE31 | PAAD[10] | I/O | PCI         |                 |                          |
| AE32 | PAAD[11] | I/O | PCI         |                 |                          |
| AD29 | PAAD[12] | I/O | PCI         |                 |                          |
| AD31 | PAAD[13] | I/O | PCI         |                 |                          |
| AC28 | PAAD[14] | I/O | PCI         |                 |                          |
| AC29 | PAAD[15] | I/O | PCI         |                 |                          |
| AC30 | PAAD[16] | I/O | PCI         |                 |                          |
| AC31 | PAAD[17] | I/O | PCI         |                 |                          |
| AC32 | PAAD[18] | I/O | PCI         |                 |                          |
| AB29 | PAAD[19] | I/O | PCI         |                 |                          |
| AB31 | PAAD[20] | I/O | PCI         |                 |                          |
| AA28 | PAAD[21] | I/O | PCI         |                 |                          |
| AA29 | PAAD[22] | I/O | PCI         |                 |                          |
| AA30 | PAAD[23] | I/O | PCI         |                 |                          |
| AA31 | PAAD[24] | I/O | PCI         |                 |                          |
| AA32 | PAAD[25] | I/O | PCI         |                 |                          |
| Y29  | PAAD[26] | I/O | PCI         |                 |                          |
| Y31  | PAAD[27] | I/O | PCI         |                 |                          |

Table 12-28: PXB Pin List Sorted by Signal (Continued)

| PIN# | Signal    | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|-----------|-----|-------------|-----------------|--------------------------|
| W29  | PAAD[28]  | I/O | PCI         |                 |                          |
| W30  | PAAD[29]  | I/O | PCI         |                 |                          |
| W31  | PAAD[30]  | I/O | PCI         |                 |                          |
| W32  | PAAD[31]  | I/O | PCI         |                 |                          |
| AH18 | PACBE[0]# | I/O | PCI         |                 |                          |
| AJ18 | PACBE[1]# | I/O | PCI         |                 |                          |
| AM20 | PACBE[2]# | I/O | PCI         |                 |                          |
| AJ21 | PACBE[3]# | I/O | PCI         |                 |                          |
| L32  | PACLK     | O   | LVTTTL      | 10ma            |                          |
| J32  | PACLKFB   | I   | LVTTTL      |                 |                          |
| AH20 | PADEVSEL# | I/O | PCI         |                 |                          |
| AL20 | PAFRAME#  | I/O | PCI         |                 |                          |
| AJ23 | PAGNT[0]# | O   | PCI         |                 |                          |
| AL23 | PAGNT[1]# | O   | PCI         |                 |                          |
| AH24 | PAGNT[2]# | O   | PCI         |                 |                          |
| AJ24 | PAGNT[3]# | O   | PCI         |                 |                          |
| AK24 | PAGNT[4]# | O   | PCI         |                 |                          |
| AL24 | PAGNT[5]# | O   | PCI         |                 |                          |
| AK20 | PAIRDY#   | I/O | PCI         |                 |                          |
| AJ19 | PALOCK#   | I/O | PCI         |                 |                          |
| AL25 | PAMON[0]# | I/O | LVTTTL      | 10ma            |                          |
| AH26 | PAMON[1]# | I/O | LVTTTL      | 10ma            |                          |
| AK18 | PAPAR     | I/O | PCI         |                 |                          |
| AM18 | PAPERR#   | I/O | PCI         |                 |                          |
| AL21 | PAREQ[0]# | I   | PCI         |                 |                          |
| AH22 | PAREQ[1]# | I   | PCI         |                 |                          |
| AJ22 | PAREQ[2]# | I   | PCI         |                 |                          |
| AK22 | PAREQ[3]# | I   | PCI         |                 |                          |
| AL22 | PAREQ[4]# | I   | PCI         |                 |                          |
| AM22 | PAREQ[5]# | I   | PCI         |                 |                          |
| AJ25 | PARST#    | O   | PCI         |                 |                          |
| AL18 | PASERR#   | OD  | PCI         |                 |                          |
| AL19 | PASTOP#   | I/O | PCI         |                 |                          |
| AJ20 | PATRDY#   | I/O | PCI         |                 |                          |
| AJ27 | PAXARB#   | I   | PCI         |                 |                          |
| AG05 | PBAD[00]  | I/O | PCI         |                 |                          |
| AG04 | PBAD[01]  | I/O | PCI         |                 |                          |
| AG03 | PBAD[02]  | I/O | PCI         |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal    | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|-----------|-----|-------------|-----------------|--------------------------|
| AG02 | PBAD[03]  | I/O | PCI         |                 |                          |
| AG01 | PBAD[04]  | I/O | PCI         |                 |                          |
| AF04 | PBAD[05]  | I/O | PCI         |                 |                          |
| AF02 | PBAD[06]  | I/O | PCI         |                 |                          |
| AE05 | PBAD[07]  | I/O | PCI         |                 |                          |
| AE04 | PBAD[08]  | I/O | PCI         |                 |                          |
| AE03 | PBAD[09]  | I/O | PCI         |                 |                          |
| AE02 | PBAD[10]  | I/O | PCI         |                 |                          |
| AE01 | PBAD[11]  | I/O | PCI         |                 |                          |
| AD04 | PBAD[12]  | I/O | PCI         |                 |                          |
| AD02 | PBAD[13]  | I/O | PCI         |                 |                          |
| AC05 | PBAD[14]  | I/O | PCI         |                 |                          |
| AC04 | PBAD[15]  | I/O | PCI         |                 |                          |
| AC03 | PBAD[16]  | I/O | PCI         |                 |                          |
| AC02 | PBAD[17]  | I/O | PCI         |                 |                          |
| AC01 | PBAD[18]  | I/O | PCI         |                 |                          |
| AB04 | PBAD[19]  | I/O | PCI         |                 |                          |
| AB02 | PBAD[20]  | I/O | PCI         |                 |                          |
| AA05 | PBAD[21]  | I/O | PCI         |                 |                          |
| AA04 | PBAD[22]  | I/O | PCI         |                 |                          |
| AA03 | PBAD[23]  | I/O | PCI         |                 |                          |
| AA02 | PBAD[24]  | I/O | PCI         |                 |                          |
| AA01 | PBAD[25]  | I/O | PCI         |                 |                          |
| Y04  | PBAD[26]  | I/O | PCI         |                 |                          |
| Y02  | PBAD[27]  | I/O | PCI         |                 |                          |
| W04  | PBAD[28]  | I/O | PCI         |                 |                          |
| W03  | PBAD[29]  | I/O | PCI         |                 |                          |
| W02  | PBAD[30]  | I/O | PCI         |                 |                          |
| W01  | PBAD[31]  | I/O | PCI         |                 |                          |
| AH16 | PBCBE[0]# | I/O | PCI         |                 |                          |
| AJ16 | PBCBE[1]# | I/O | PCI         |                 |                          |
| AM14 | PBCBE[2]# | I/O | PCI         |                 |                          |
| AJ13 | PBCBE[3]# | I/O | PCI         |                 |                          |
| L30  | PBCLK     | O   | LVTTL       | 10ma            |                          |
| J30  | PBCLKFB   | I   | LVTTL       |                 |                          |
| AH14 | PBDEVSEL# | I/O | PCI         |                 |                          |
| AL14 | PBFRAME#  | I/O | PCI         |                 |                          |
| AJ11 | PBGNT[0]# | O   | PCI         |                 |                          |

Table 12-28: PXB Pin List Sorted by Signal (Continued)

| PIN# | Signal    | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|-----------|-----|-------------|-----------------|--------------------------|
| AL11 | PBGNT[1]# | O   | PCI         |                 |                          |
| AH10 | PBGNT[2]# | O   | PCI         |                 |                          |
| AJ10 | PBGNT[3]# | O   | PCI         |                 |                          |
| AK10 | PBGNT[4]# | O   | PCI         |                 |                          |
| AL10 | PBGNT[5]# | O   | PCI         |                 |                          |
| AK14 | PBIRDY#   | I/O | PCI         |                 |                          |
| AJ15 | PBLOCK#   | I/O | PCI         |                 |                          |
| AL09 | PBMON[0]# | I/O | PCI         |                 |                          |
| AH08 | PBMON[1]# | I/O | PCI         |                 |                          |
| AK16 | PBPAR     | I/O | PCI         |                 |                          |
| AM16 | PBPERR#   | I/O | PCI         |                 |                          |
| AL13 | PBREQ[0]# | I   | PCI         |                 |                          |
| AH12 | PBREQ[1]# | I   | PCI         |                 |                          |
| AJ12 | PBREQ[2]# | I   | PCI         |                 |                          |
| AK12 | PBREQ[3]# | I   | PCI         |                 |                          |
| AL12 | PBREQ[4]# | I   | PCI         |                 |                          |
| AM12 | PBREQ[5]# | I   | PCI         |                 |                          |
| AJ09 | PBRST#    | O   | PCI         |                 |                          |
| AL16 | PBSERR#   | OD  | PCI         |                 |                          |
| AL15 | PBSTOP#   | I/O | PCI         |                 |                          |
| AJ14 | PBTRDY#   | I/O | PCI         |                 |                          |
| AJ07 | PBXARB#   | I   | PCI         |                 |                          |
| AL26 | PHLDA#    | O   | PCI         |                 |                          |
| AK26 | PHOLD#    | I   | PCI         |                 |                          |
| F29  | PIIXOK#   | I   | LVTTTL      |                 |                          |
| D29  | PWRGD     | I   | LVTTTL      |                 |                          |
| AJ17 | REQ64#    | I/O | PCI         |                 |                          |
| M04  | TCK       | I   | 2.5V        |                 |                          |
| N01  | TDI       | I   | 2.5V        |                 |                          |
| N02  | TDO       | O   | OD          | 14ma            |                          |
| N04  | TMS       | I   | 2.5V        |                 |                          |
| N05  | TRST#     | I   | 2.5V        |                 |                          |
| A03  | VCC       |     | Power       |                 |                          |
| A04  | VCC       |     | Power       |                 |                          |
| A05  | VCC       |     | Power       |                 |                          |
| A06  | VCC       |     | Power       |                 |                          |
| A07  | VCC       |     | Power       |                 |                          |
| A08  | VCC       |     | Power       |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A09  | VCC    |     | Power       |                 |                          |
| A10  | VCC    |     | Power       |                 |                          |
| A14  | VCC    |     | Power       |                 |                          |
| A16  | VCC    |     | Power       |                 |                          |
| A18  | VCC    |     | Power       |                 |                          |
| A20  | VCC    |     | Power       |                 |                          |
| A22  | VCC    |     | Power       |                 |                          |
| A26  | VCC    |     | Power       |                 |                          |
| A28  | VCC    |     | Power       |                 |                          |
| A29  | VCC    |     | Power       |                 |                          |
| B02  | VCC    |     | Power       |                 |                          |
| B03  | VCC    |     | Power       |                 |                          |
| B04  | VCC    |     | Power       |                 |                          |
| B28  | VCC    |     | Power       |                 |                          |
| B29  | VCC    |     | Power       |                 |                          |
| B30  | VCC    |     | Power       |                 |                          |
| B31  | VCC    |     | Power       |                 |                          |
| D27  | VCC    |     | Power       |                 |                          |
| F03  | VCC    |     | Power       |                 |                          |
| G30  | VCC    |     | Power       |                 |                          |
| G31  | VCC    |     | Power       |                 |                          |
| H01  | VCC    |     | Power       |                 |                          |
| H05  | VCC    |     | Power       |                 |                          |
| K03  | VCC    |     | Power       |                 |                          |
| K30  | VCC    |     | Power       |                 |                          |
| M01  | VCC    |     | Power       |                 |                          |
| M05  | VCC    |     | Power       |                 |                          |
| M28  | VCC    |     | Power       |                 |                          |
| M32  | VCC    |     | Power       |                 |                          |
| N03  | VCC    |     | Power       |                 |                          |
| P01  | VCC    |     | Power       |                 |                          |
| P30  | VCC    |     | Power       |                 |                          |
| R01  | VCC    |     | Power       |                 |                          |
| R30  | VCC    |     | Power       |                 |                          |
| T01  | VCC    |     | Power       |                 |                          |
| T30  | VCC    |     | Power       |                 |                          |
| U030 | VCC    |     | Power       |                 |                          |
| Y1   | VCC    |     | Power       |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| Y05  | VCC    |     | Power       |                 |                          |
| Y28  | VCC    |     | Power       |                 |                          |
| Y32  | VCC    |     | Power       |                 |                          |
| AD01 | VCC    |     | Power       |                 |                          |
| AD05 | VCC    |     | Power       |                 |                          |
| AD28 | VCC    |     | Power       |                 |                          |
| AD32 | VCC    |     | Power       |                 |                          |
| AH04 | VCC    |     | Power       |                 |                          |
| AH09 | VCC    |     | Power       |                 |                          |
| AH13 | VCC    |     | Power       |                 |                          |
| AH17 | VCC    |     | Power       |                 |                          |
| AH21 | VCC    |     | Power       |                 |                          |
| AH25 | VCC    |     | Power       |                 |                          |
| AH29 | VCC    |     | Power       |                 |                          |
| AJ04 | VCC    |     | Power       |                 |                          |
| AJ29 | VCC    |     | Power       |                 |                          |
| AK07 | VCC    |     | Power       |                 |                          |
| AK27 | VCC    |     | Power       |                 |                          |
| AM09 | VCC    |     | Power       |                 |                          |
| AM13 | VCC    |     | Power       |                 |                          |
| AM17 | VCC    |     | Power       |                 |                          |
| AM21 | VCC    |     | Power       |                 |                          |
| AM25 | VCC    |     | Power       |                 |                          |
| P05  | VCC    |     | Power       |                 |                          |
| R05  | VCC    |     | Power       |                 |                          |
| T05  | VCC    |     | Power       |                 |                          |
| V28  | VCC    |     | Power       |                 |                          |
| W28  | VCC    |     | Power       |                 |                          |
| V03  | VCC5A  |     | Power (PCI) |                 |                          |
| AB03 | VCC5B  |     | Power (PCI) |                 |                          |
| AF03 | VCC5C  |     | Power (PCI) |                 |                          |
| AH03 | VCC5D  |     | Power (PCI) |                 |                          |
| AK04 | VCC5E  |     | Power (PCI) |                 |                          |
| AK11 | VCC5F  |     | Power (PCI) |                 |                          |
| AK15 | VCC5G  |     | Power (PCI) |                 |                          |
| AK19 | VCC5H  |     | Power (PCI) |                 |                          |
| AK23 | VCC5I  |     | Power (PCI) |                 |                          |
| AK29 | VCC5J  |     | Power (PCI) |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| AH30 | VCC5K  |     | Power (PCI) |                 |                          |
| AF30 | VCC5L  |     | Power (PCI) |                 |                          |
| AB30 | VCC5M  |     | Power (PCI) |                 |                          |
| V30  | VCC5N  |     | Power (PCI) |                 |                          |
| A27  | VCCA0  |     | Power       |                 |                          |
| C27  | VCCA1  |     | Power       |                 |                          |
| E27  | VCCA2  |     | Power       |                 |                          |
| A12  | VREF   | I   | Analog      |                 |                          |
| A24  | VREF   | I   | Analog      |                 |                          |
| C06  | GND    |     | Power       |                 |                          |
| C07  | GND    |     | Power       |                 |                          |
| C08  | GND    |     | Power       |                 |                          |
| C10  | GND    |     | Power       |                 |                          |
| C12  | GND    |     | Power       |                 |                          |
| C14  | GND    |     | Power       |                 |                          |
| C16  | GND    |     | Power       |                 |                          |
| C18  | GND    |     | Power       |                 |                          |
| C20  | GND    |     | Power       |                 |                          |
| C22  | GND    |     | Power       |                 |                          |
| C24  | GND    |     | Power       |                 |                          |
| C26  | GND    |     | Power       |                 |                          |
| D02  | GND    |     | Power       |                 |                          |
| D31  | GND    |     | Power       |                 |                          |
| F01  | GND    |     | Power       |                 |                          |
| F05  | GND    |     | Power       |                 |                          |
| F28  | GND    |     | Power       |                 |                          |
| H03  | GND    |     | Power       |                 |                          |
| H30  | GND    |     | Power       |                 |                          |
| K01  | GND    |     | Power       |                 |                          |
| K05  | GND    |     | Power       |                 |                          |
| K28  | GND    |     | Power       |                 |                          |
| K32  | GND    |     | Power       |                 |                          |
| L01  | GND    |     | Power       |                 |                          |
| L02  | GND    |     | Power       |                 |                          |
| L03  | GND    |     | Power       |                 |                          |
| L04  | GND    |     | Power       |                 |                          |
| L05  | GND    |     | Power       |                 |                          |
| M03  | GND    |     | Power       |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| M30  | GND    |     | Power       |                 |                          |
| P03  | GND    |     | Power       |                 |                          |
| P32  | GND    |     | Power       |                 |                          |
| R03  | GND    |     | Power       |                 |                          |
| R32  | GND    |     | Power       |                 |                          |
| T03  | GND    |     | Power       |                 |                          |
| T32  | GND    |     | Power       |                 |                          |
| U32  | GND    |     | Power       |                 |                          |
| V01  | GND    |     | Power       |                 |                          |
| V32  | GND    |     | Power       |                 |                          |
| Y03  | GND    |     | Power       |                 |                          |
| Y30  | GND    |     | Power       |                 |                          |
| AB01 | GND    |     | Power       |                 |                          |
| AB05 | GND    |     | Power       |                 |                          |
| AB28 | GND    |     | Power       |                 |                          |
| AB32 | GND    |     | Power       |                 |                          |
| AD03 | GND    |     | Power       |                 |                          |
| AD30 | GND    |     | Power       |                 |                          |
| AF01 | GND    |     | Power       |                 |                          |
| AF05 | GND    |     | Power       |                 |                          |
| AF28 | GND    |     | Power       |                 |                          |
| AF32 | GND    |     | Power       |                 |                          |
| AH07 | GND    |     | Power       |                 |                          |
| AH11 | GND    |     | Power       |                 |                          |
| AH15 | GND    |     | Power       |                 |                          |
| AH19 | GND    |     | Power       |                 |                          |
| AH23 | GND    |     | Power       |                 |                          |
| AH27 | GND    |     | Power       |                 |                          |
| AK02 | GND    |     | Power       |                 |                          |
| AK09 | GND    |     | Power       |                 |                          |
| AK13 | GND    |     | Power       |                 |                          |
| AK17 | GND    |     | Power       |                 |                          |
| AK21 | GND    |     | Power       |                 |                          |
| AK25 | GND    |     | Power       |                 |                          |
| AK31 | GND    |     | Power       |                 |                          |
| AM03 | GND    |     | Power       |                 |                          |
| AM04 | GND    |     | Power       |                 |                          |
| AM05 | GND    |     | Power       |                 |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| AM07 | GND     |     | Power       |                 |                          |
| AM11 | GND     |     | Power       |                 |                          |
| AM15 | GND     |     | Power       |                 |                          |
| AM19 | GND     |     | Power       |                 |                          |
| AM23 | GND     |     | Power       |                 |                          |
| AM27 | GND     |     | Power       |                 |                          |
| AM28 | GND     |     | Power       |                 |                          |
| AM29 | GND     |     | Power       |                 |                          |
| AM30 | GND     |     | Power       |                 |                          |
| AM32 | GND     |     | Power       |                 |                          |
| P28  | GND     |     | Power       |                 |                          |
| R28  | GND     |     | Power       |                 |                          |
| T28  | GND     |     | Power       |                 |                          |
| V05  | GND     |     | Power       |                 |                          |
| W05  | GND     |     | Power       |                 |                          |
| D04  | VTT     |     | Power       |                 |                          |
| D28  | VTT     |     | Power       |                 |                          |
| E06  | VTT     |     | Power       |                 |                          |
| E08  | VTT     |     | Power       |                 |                          |
| E10  | VTT     |     | Power       |                 |                          |
| E12  | VTT     |     | Power       |                 |                          |
| E14  | VTT     |     | Power       |                 |                          |
| E16  | VTT     |     | Power       |                 |                          |
| E18  | VTT     |     | Power       |                 |                          |
| E20  | VTT     |     | Power       |                 |                          |
| E22  | VTT     |     | Power       |                 |                          |
| E24  | VTT     |     | Power       |                 |                          |
| E26  | VTT     |     | Power       |                 |                          |
| AM26 | WSC#    | O   | PCI         |                 |                          |
| C21  | XADS#   | I/O | AGTL+       | 55ma            |                          |
| E23  | XBE[0]# | I/O | AGTL+       | 55ma            |                          |
| B22  | XBE[1]# | I/O | AGTL+       | 55ma            |                          |
| A21  | XBLK#   | I   | AGTL+       |                 |                          |
| C25  | XCLK    | I   | LVTTL       |                 |                          |
| D21  | XD[00]# | I/O | AGTL+       | 55ma            |                          |
| E21  | XD[01]# | I/O | AGTL+       | 55ma            |                          |
| B20  | XD[02]# | I/O | AGTL+       | 55ma            |                          |
| D20  | XD[03]# | I/O | AGTL+       | 55ma            |                          |

**Table 12-28: PXB Pin List Sorted by Signal (Continued)**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| A19  | XD[04]# | I/O | AGTL+       | 55ma            |                          |
| B19  | XD[05]# | I/O | AGTL+       | 55ma            |                          |
| D17  | XD[06]# | I/O | AGTL+       | 55ma            |                          |
| E17  | XD[07]# | I/O | AGTL+       | 55ma            |                          |
| B16  | XD[08]# | I/O | AGTL+       | 55ma            |                          |
| D16  | XD[09]# | I/O | AGTL+       | 55ma            |                          |
| A15  | XD[10]# | I/O | AGTL+       | 55ma            |                          |
| B15  | XD[11]# | I/O | AGTL+       | 55ma            |                          |
| C15  | XD[12]# | I/O | AGTL+       | 55ma            |                          |
| D15  | XD[13]# | I/O | AGTL+       | 55ma            |                          |
| E15  | XD[14]# | I/O | AGTL+       | 55ma            |                          |
| B14  | XD[15]# | I/O | AGTL+       | 55ma            |                          |
| B18  | XHRTS#  | I   | AGTL+       |                 |                          |
| A17  | XHSTBN# | I   | AGTL+       |                 |                          |
| C17  | XHSTBP# | I   | AGTL+       |                 |                          |
| E13  | XIB     | O   | AGTL+       | 55ma            |                          |
| B21  | XPAR#   | I/O | AGTL+       | 55ma            |                          |
| D22  | XRST#   | I   | AGTL+       |                 |                          |
| D18  | XXRTS#  | O   | AGTL+       | 55ma            |                          |
| C19  | XXSTBN# | O   | AGTL+       | 55ma            |                          |
| E19  | XXSTBP# | O   | AGTL+       | 55ma            |                          |

**Table 12-29: MUX Pin List Sorted by Signal**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|-----------------------|
| Y12  | AVWP#   | I   | AGTL+       |                 |                       |
| T12  | CRES0   | I   | Analog      |                 |                       |
| V13  | CRES1   | I   | Analog      |                 |                       |
| Y13  | DCMPLT# | I/O | AGTL+       | 55ma            |                       |
| V09  | DOFF0#  | I   | AGTL+       |                 |                       |
| V08  | DOFF1#  | I   | AGTL+       |                 |                       |
| W09  | DSEL#   | I   | AGTL+       |                 |                       |
| Y19  | DSTBN0# | I/O | AGTL+       | 55ma            |                       |
| Y03  | DSTBN1# | I/O | AGTL+       | 55ma            |                       |
| Y18  | DSTBP0# | I/O | AGTL+       | 55ma            |                       |
| T06  | DSTBP1# | I/O | AGTL+       | 55ma            |                       |
| V11  | DVALID# | I   | AGTL+       |                 |                       |
| T09  | N/C     |     |             |                 |                       |

Table 12-29: MUX Pin List Sorted by Signal (Continued)

| PIN# | Signal   | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|-----------------------|
| W12  | GDCMPLT# | I/O | AGTL+       | 55ma            |                       |
| A01  | GND      |     | Power       |                 |                       |
| A06  | GND      |     | Power       |                 |                       |
| A15  | GND      |     | Power       |                 |                       |
| A20  | GND      |     | Power       |                 |                       |
| B02  | GND      |     | Power       |                 |                       |
| B06  | GND      |     | Power       |                 |                       |
| B10  | GND      |     | Power       |                 |                       |
| B11  | GND      |     | Power       |                 |                       |
| B15  | GND      |     | Power       |                 |                       |
| B19  | GND      |     | Power       |                 |                       |
| F02  | GND      |     | Power       |                 |                       |
| F19  | GND      |     | Power       |                 |                       |
| H04  | GND      |     | Power       |                 |                       |
| H17  | GND      |     | Power       |                 |                       |
| J09  | GND      |     | Power       |                 |                       |
| J10  | GND      |     | Power       |                 |                       |
| J11  | GND      |     | Power       |                 |                       |
| J12  | GND      |     | Power       |                 |                       |
| N04  | GND      |     | Power       |                 |                       |
| N17  | GND      |     | Power       |                 |                       |
| R01  | GND      |     | Power       |                 |                       |
| R02  | GND      |     | Power       |                 |                       |
| R19  | GND      |     | Power       |                 |                       |
| R20  | GND      |     | Power       |                 |                       |
| W06  | GND      |     | Power       |                 |                       |
| W10  | GND      |     | Power       |                 |                       |
| W11  | GND      |     | Power       |                 |                       |
| W15  | GND      |     | Power       |                 |                       |
| W19  | GND      |     | Power       |                 |                       |
| Y01  | GND      |     | Power       |                 |                       |
| Y06  | GND      |     | Power       |                 |                       |
| Y15  | GND      |     | Power       |                 |                       |
| Y20  | GND      |     | Power       |                 |                       |
| D04  | GND      |     | Power       |                 |                       |
| D08  | GND      |     | Power       |                 |                       |
| D13  | GND      |     | Power       |                 |                       |
| D17  | GND      |     | Power       |                 |                       |

Table 12-29: MUX Pin List Sorted by Signal (Continued)

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| K02  | GND    |     | Power       |                 |                       |
| K09  | GND    |     | Power       |                 |                       |
| K10  | GND    |     | Power       |                 |                       |
| K11  | GND    |     | Power       |                 |                       |
| K12  | GND    |     | Power       |                 |                       |
| K19  | GND    |     | Power       |                 |                       |
| L02  | GND    |     | Power       |                 |                       |
| L09  | GND    |     | Power       |                 |                       |
| L10  | GND    |     | Power       |                 |                       |
| L11  | GND    |     | Power       |                 |                       |
| L12  | GND    |     | Power       |                 |                       |
| L19  | GND    |     | Power       |                 |                       |
| M09  | GND    |     | Power       |                 |                       |
| M10  | GND    |     | Power       |                 |                       |
| M11  | GND    |     | Power       |                 |                       |
| M12  | GND    |     | Power       |                 |                       |
| U04  | GND    |     | Power       |                 |                       |
| U08  | GND    |     | Power       |                 |                       |
| U13  | GND    |     | Power       |                 |                       |
| U17  | GND    |     | Power       |                 |                       |
| W02  | GND    |     | Power       |                 |                       |
| V10  | HCLKIN | I   | 2.5V        |                 |                       |
| Y08  | LDSTB# | O   | AGTL+       | 55ma            |                       |
| V12  | LRD#   | I   | AGTL+       |                 |                       |
| R16  | MD00#  | I/O | AGTL+       | 55ma            |                       |
| T17  | MD01#  | I/O | AGTL+       | 55ma            |                       |
| U18  | MD02#  | I/O | AGTL+       | 55ma            |                       |
| V19  | MD03#  | I/O | AGTL+       | 55ma            |                       |
| W20  | MD04#  | I/O | AGTL+       | 55ma            |                       |
| T16  | MD05#  | I/O | AGTL+       | 55ma            |                       |
| V18  | MD06#  | I/O | AGTL+       | 55ma            |                       |
| T15  | MD07#  | I/O | AGTL+       | 55ma            |                       |
| V17  | MD08#  | I/O | AGTL+       | 55ma            |                       |
| T14  | MD09#  | I/O | AGTL+       | 55ma            |                       |
| V15  | MD10#  | I/O | AGTL+       | 55ma            |                       |
| W16  | MD11#  | I/O | AGTL+       | 55ma            |                       |
| Y17  | MD12#  | I/O | AGTL+       | 55ma            |                       |
| U14  | MD13#  | I/O | AGTL+       | 55ma            |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal  | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|-----------------------|
| Y16  | MD14#   | I/O | AGTL+       | 55ma            |                       |
| T13  | MD15#   | I/O | AGTL+       | 55ma            |                       |
| V14  | MD16#   | I/O | AGTL+       | 55ma            |                       |
| Y14  | MD17#   | I/O | AGTL+       | 55ma            |                       |
| Y07  | MD18#   | I/O | AGTL+       | 55ma            |                       |
| T08  | MD19#   | I/O | AGTL+       | 55ma            |                       |
| V07  | MD20#   | I/O | AGTL+       | 55ma            |                       |
| U07  | MD21#   | I/O | AGTL+       | 55ma            |                       |
| Y05  | MD22#   | I/O | AGTL+       | 55ma            |                       |
| T07  | MD23#   | I/O | AGTL+       | 55ma            |                       |
| V06  | MD24#   | I/O | AGTL+       | 55ma            |                       |
| W05  | MD25#   | I/O | AGTL+       | 55ma            |                       |
| Y04  | MD26#   | I/O | AGTL+       | 55ma            |                       |
| V04  | MD27#   | I/O | AGTL+       | 55ma            |                       |
| Y02  | MD28#   | I/O | AGTL+       | 55ma            |                       |
| T05  | MD29#   | I/O | AGTL+       | 55ma            |                       |
| V03  | MD30#   | I/O | AGTL+       | 55ma            |                       |
| R05  | MD31#   | I/O | AGTL+       | 55ma            |                       |
| T04  | MD32#   | I/O | AGTL+       | 55ma            |                       |
| U03  | MD33#   | I/O | AGTL+       | 55ma            |                       |
| V02  | MD34#   | I/O | AGTL+       | 55ma            |                       |
| W01  | MD35#   | I/O | AGTL+       | 55ma            |                       |
| Y09  | MRESET# | I   | AGTL+       |                 |                       |
| Y10  | VCC     |     | Power       |                 |                       |
| V20  | N/C     |     |             |                 |                       |
| V01  | N/C     |     |             |                 |                       |
| T18  | Q0D00   | I/O | LVTTTL      | 10ma            |                       |
| U20  | Q0D01   | I/O | LVTTTL      | 10ma            |                       |
| P18  | Q0D02   | I/O | LVTTTL      | 10ma            |                       |
| N18  | Q0D03   | I/O | LVTTTL      | 10ma            |                       |
| M20  | Q0D04   | I/O | LVTTTL      | 10ma            |                       |
| K16  | Q0D05   | I/O | LVTTTL      | 10ma            |                       |
| J18  | Q0D06   | I/O | LVTTTL      | 10ma            |                       |
| H18  | Q0D07   | I/O | LVTTTL      | 10ma            |                       |
| G18  | Q0D08   | I/O | LVTTTL      | 10ma            |                       |
| G16  | Q0D09   | I/O | LVTTTL      | 10ma            |                       |
| E18  | Q0D10   | I/O | LVTTTL      | 10ma            |                       |
| D18  | Q0D11   | I/O | LVTTTL      | 10ma            |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| C18  | Q0D12  | I/O | LVTTL       | 10ma            |                       |
| B18  | Q0D13  | I/O | LVTTL       | 10ma            |                       |
| E14  | Q0D14  | I/O | LVTTL       | 10ma            |                       |
| D14  | Q0D15  | I/O | LVTTL       | 10ma            |                       |
| B14  | Q0D16  | I/O | LVTTL       | 10ma            |                       |
| D12  | Q0D17  | I/O | LVTTL       | 10ma            |                       |
| D09  | Q0D18  | I/O | LVTTL       | 10ma            |                       |
| E09  | Q0D19  | I/O | LVTTL       | 10ma            |                       |
| E08  | Q0D20  | I/O | LVTTL       | 10ma            |                       |
| E07  | Q0D21  | I/O | LVTTL       | 10ma            |                       |
| C05  | Q0D22  | I/O | LVTTL       | 10ma            |                       |
| C04  | Q0D23  | I/O | LVTTL       | 10ma            |                       |
| C03  | Q0D24  | I/O | LVTTL       | 10ma            |                       |
| C02  | Q0D25  | I/O | LVTTL       | 10ma            |                       |
| G05  | Q0D26  | I/O | LVTTL       | 10ma            |                       |
| G04  | Q0D27  | I/O | LVTTL       | 10ma            |                       |
| F01  | Q0D28  | I/O | LVTTL       | 10ma            |                       |
| H03  | Q0D29  | I/O | LVTTL       | 10ma            |                       |
| J01  | Q0D30  | I/O | LVTTL       | 10ma            |                       |
| L05  | Q0D31  | I/O | LVTTL       | 10ma            |                       |
| M03  | Q0D32  | I/O | LVTTL       | 10ma            |                       |
| N03  | Q0D33  | I/O | LVTTL       | 10ma            |                       |
| P03  | Q0D34  | I/O | LVTTL       | 10ma            |                       |
| R03  | Q0D35  | I/O | LVTTL       | 10ma            |                       |
| P16  | Q1D00  | I/O | LVTTL       | 10ma            |                       |
| P17  | Q1D01  | I/O | LVTTL       | 10ma            |                       |
| P19  | Q1D02  | I/O | LVTTL       | 10ma            |                       |
| M17  | Q1D03  | I/O | LVTTL       | 10ma            |                       |
| L16  | Q1D04  | I/O | LVTTL       | 10ma            |                       |
| K18  | Q1D05  | I/O | LVTTL       | 10ma            |                       |
| J19  | Q1D06  | I/O | LVTTL       | 10ma            |                       |
| G19  | Q1D07  | I/O | LVTTL       | 10ma            |                       |
| F20  | Q1D08  | I/O | LVTTL       | 10ma            |                       |
| F18  | Q1D09  | I/O | LVTTL       | 10ma            |                       |
| C20  | Q1D10  | I/O | LVTTL       | 10ma            |                       |
| C19  | Q1D11  | I/O | LVTTL       | 10ma            |                       |
| E15  | Q1D12  | I/O | LVTTL       | 10ma            |                       |
| A19  | Q1D13  | I/O | LVTTL       | 10ma            |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| C15  | Q1D14  | I/O | LVTTL       | 10ma            |                       |
| A16  | Q1D15  | I/O | LVTTL       | 10ma            |                       |
| A14  | Q1D16  | I/O | LVTTL       | 10ma            |                       |
| C12  | Q1D17  | I/O | LVTTL       | 10ma            |                       |
| C09  | Q1D18  | I/O | LVTTL       | 10ma            |                       |
| C08  | Q1D19  | I/O | LVTTL       | 10ma            |                       |
| C07  | Q1D20  | I/O | LVTTL       | 10ma            |                       |
| C06  | Q1D21  | I/O | LVTTL       | 10ma            |                       |
| A03  | Q1D22  | I/O | LVTTL       | 10ma            |                       |
| B03  | Q1D23  | I/O | LVTTL       | 10ma            |                       |
| F05  | Q1D24  | I/O | LVTTL       | 10ma            |                       |
| B01  | Q1D25  | I/O | LVTTL       | 10ma            |                       |
| F03  | Q1D26  | I/O | LVTTL       | 10ma            |                       |
| E01  | Q1D27  | I/O | LVTTL       | 10ma            |                       |
| G02  | Q1D28  | I/O | LVTTL       | 10ma            |                       |
| J04  | Q1D29  | I/O | LVTTL       | 10ma            |                       |
| K05  | Q1D30  | I/O | LVTTL       | 10ma            |                       |
| L03  | Q1D31  | I/O | LVTTL       | 10ma            |                       |
| M02  | Q1D32  | I/O | LVTTL       | 10ma            |                       |
| P02  | Q1D33  | I/O | LVTTL       | 10ma            |                       |
| P04  | Q1D34  | I/O | LVTTL       | 10ma            |                       |
| T02  | Q1D35  | I/O | LVTTL       | 10ma            |                       |
| R18  | Q2D00  | I/O | LVTTL       | 10ma            |                       |
| T20  | Q2D01  | I/O | LVTTL       | 10ma            |                       |
| P20  | Q2D02  | I/O | LVTTL       | 10ma            |                       |
| M18  | Q2D03  | I/O | LVTTL       | 10ma            |                       |
| L18  | Q2D04  | I/O | LVTTL       | 10ma            |                       |
| K20  | Q2D05  | I/O | LVTTL       | 10ma            |                       |
| J20  | Q2D06  | I/O | LVTTL       | 10ma            |                       |
| G20  | Q2D07  | I/O | LVTTL       | 10ma            |                       |
| G17  | Q2D08  | I/O | LVTTL       | 10ma            |                       |
| E19  | Q2D09  | I/O | LVTTL       | 10ma            |                       |
| F16  | Q2D10  | I/O | LVTTL       | 10ma            |                       |
| B20  | Q2D11  | I/O | LVTTL       | 10ma            |                       |
| D16  | Q2D12  | I/O | LVTTL       | 10ma            |                       |
| C16  | Q2D13  | I/O | LVTTL       | 10ma            |                       |
| B16  | Q2D14  | I/O | LVTTL       | 10ma            |                       |
| E13  | Q2D15  | I/O | LVTTL       | 10ma            |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| E12  | Q2D16  | I/O | LVTTL       | 10ma            |                       |
| B12  | Q2D17  | I/O | LVTTL       | 10ma            |                       |
| B09  | Q2D18  | I/O | LVTTL       | 10ma            |                       |
| B07  | Q2D19  | I/O | LVTTL       | 10ma            |                       |
| D07  | Q2D20  | I/O | LVTTL       | 10ma            |                       |
| B05  | Q2D21  | I/O | LVTTL       | 10ma            |                       |
| E06  | Q2D22  | I/O | LVTTL       | 10ma            |                       |
| A02  | Q2D23  | I/O | LVTTL       | 10ma            |                       |
| E04  | Q2D24  | I/O | LVTTL       | 10ma            |                       |
| E03  | Q2D25  | I/O | LVTTL       | 10ma            |                       |
| E02  | Q2D26  | I/O | LVTTL       | 10ma            |                       |
| H05  | Q2D27  | I/O | LVTTL       | 10ma            |                       |
| G01  | Q2D28  | I/O | LVTTL       | 10ma            |                       |
| J03  | Q2D29  | I/O | LVTTL       | 10ma            |                       |
| K03  | Q2D30  | I/O | LVTTL       | 10ma            |                       |
| L01  | Q2D31  | I/O | LVTTL       | 10ma            |                       |
| M01  | Q2D32  | I/O | LVTTL       | 10ma            |                       |
| P01  | Q2D33  | I/O | LVTTL       | 10ma            |                       |
| T01  | Q2D34  | I/O | LVTTL       | 10ma            |                       |
| U01  | Q2D35  | I/O | LVTTL       | 10ma            |                       |
| T19  | Q3D00  | I/O | LVTTL       | 10ma            |                       |
| N16  | Q3D01  | I/O | LVTTL       | 10ma            |                       |
| M16  | Q3D02  | I/O | LVTTL       | 10ma            |                       |
| M19  | Q3D03  | I/O | LVTTL       | 10ma            |                       |
| L20  | Q3D04  | I/O | LVTTL       | 10ma            |                       |
| J17  | Q3D05  | I/O | LVTTL       | 10ma            |                       |
| J16  | Q3D06  | I/O | LVTTL       | 10ma            |                       |
| H16  | Q3D07  | I/O | LVTTL       | 10ma            |                       |
| E20  | Q3D08  | I/O | LVTTL       | 10ma            |                       |
| D20  | Q3D09  | I/O | LVTTL       | 10ma            |                       |
| E17  | Q3D10  | I/O | LVTTL       | 10ma            |                       |
| E16  | Q3D11  | I/O | LVTTL       | 10ma            |                       |
| C17  | Q3D12  | I/O | LVTTL       | 10ma            |                       |
| A18  | Q3D13  | I/O | LVTTL       | 10ma            |                       |
| A17  | Q3D14  | I/O | LVTTL       | 10ma            |                       |
| C14  | Q3D15  | I/O | LVTTL       | 10ma            |                       |
| C13  | Q3D16  | I/O | LVTTL       | 10ma            |                       |
| A12  | Q3D17  | I/O | LVTTL       | 10ma            |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| A09  | Q3D18  | I/O | LVTTL       | 10ma            |                       |
| A07  | Q3D19  | I/O | LVTTL       | 10ma            |                       |
| A05  | Q3D20  | I/O | LVTTL       | 10ma            |                       |
| A04  | Q3D21  | I/O | LVTTL       | 10ma            |                       |
| D05  | Q3D22  | I/O | LVTTL       | 10ma            |                       |
| E05  | Q3D23  | I/O | LVTTL       | 10ma            |                       |
| D03  | Q3D24  | I/O | LVTTL       | 10ma            |                       |
| C01  | Q3D25  | I/O | LVTTL       | 10ma            |                       |
| D01  | Q3D26  | I/O | LVTTL       | 10ma            |                       |
| G03  | Q3D27  | I/O | LVTTL       | 10ma            |                       |
| J05  | Q3D28  | I/O | LVTTL       | 10ma            |                       |
| J02  | Q3D29  | I/O | LVTTL       | 10ma            |                       |
| K01  | Q3D30  | I/O | LVTTL       | 10ma            |                       |
| M04  | Q3D31  | I/O | LVTTL       | 10ma            |                       |
| M05  | Q3D32  | I/O | LVTTL       | 10ma            |                       |
| N05  | Q3D33  | I/O | LVTTL       | 10ma            |                       |
| P05  | Q3D34  | I/O | LVTTL       | 10ma            |                       |
| T03  | Q3D35  | I/O | LVTTL       | 10ma            |                       |
| C11  | TCK    | I   | LVTTL       |                 |                       |
| C10  | TDI    | I   | LVTTL       |                 |                       |
| A10  | TDO    | O   | OD          | 14ma            |                       |
| E10  | TMS    | I   | LVTTL       |                 |                       |
| E11  | TRST#  | I   | LVTTL       |                 |                       |
| A08  | VCC    |     | Power       |                 |                       |
| A11  | VCC    |     | Power       |                 |                       |
| A13  | VCC    |     | Power       |                 |                       |
| B04  | VCC    |     | Power       |                 |                       |
| B08  | VCC    |     | Power       |                 |                       |
| B13  | VCC    |     | Power       |                 |                       |
| B17  | VCC    |     | Power       |                 |                       |
| F04  | VCC    |     | Power       |                 |                       |
| F06  | VCC    |     | Power       |                 |                       |
| F14  | VCC    |     | Power       |                 |                       |
| F15  | VCC    |     | Power       |                 |                       |
| F17  | VCC    |     | Power       |                 |                       |
| G06  | VCC    |     | Power       |                 |                       |
| H01  | VCC    |     | Power       |                 |                       |
| H02  | VCC    |     | Power       |                 |                       |

Table 12-29: MUX Pin List Sorted by Signal (Continued)

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| H19  | VCC    |     | Power       |                 |                       |
| H20  | VCC    |     | Power       |                 |                       |
| N19  | VCC    |     | Power       |                 |                       |
| N20  | VCC    |     | Power       |                 |                       |
| P15  | VCC    |     | Power       |                 |                       |
| R04  | VCC    |     | Power       |                 |                       |
| R06  | VCC    |     | Power       |                 |                       |
| R07  | VCC    |     | Power       |                 |                       |
| R15  | VCC    |     | Power       |                 |                       |
| R17  | VCC    |     | Power       |                 |                       |
| W08  | VCC    |     | Power       |                 |                       |
| W13  | VCC    |     | Power       |                 |                       |
| W17  | VCC    |     | Power       |                 |                       |
| D02  | VCC    |     | Power       |                 |                       |
| D06  | VCC    |     | Power       |                 |                       |
| D10  | VCC    |     | Power       |                 |                       |
| D11  | VCC    |     | Power       |                 |                       |
| D15  | VCC    |     | Power       |                 |                       |
| D19  | VCC    |     | Power       |                 |                       |
| K04  | VCC    |     | Power       |                 |                       |
| K17  | VCC    |     | Power       |                 |                       |
| L04  | VCC    |     | Power       |                 |                       |
| L17  | VCC    |     | Power       |                 |                       |
| N01  | VCC    |     | Power       |                 |                       |
| N02  | VCC    |     | Power       |                 |                       |
| U02  | VCC    |     | Power       |                 |                       |
| U06  | VCC    |     | Power       |                 |                       |
| U10  | VCC    |     | Power       |                 |                       |
| U11  | VCC    |     | Power       |                 |                       |
| U15  | VCC    |     | Power       |                 |                       |
| U19  | VCC    |     | Power       |                 |                       |
| W04  | VCC    |     | Power       |                 |                       |
| T10  | VCCA   |     | Power       |                 |                       |
| V05  | VREF   | I   | Analog      |                 |                       |
| V16  | VREF   | I   | Analog      |                 |                       |
| W07  | VTT    |     | Power       |                 |                       |
| W14  | VTT    |     | Power       |                 |                       |
| W18  | VTT    |     | Power       |                 |                       |

**Table 12-29: MUX Pin List Sorted by Signal (Continued)**

| PIN# | Signal | I/O | Driver Type | Driver Strength | Input Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|-----------------------|
| U05  | VTT    |     | Power       |                 |                       |
| U09  | VTT    |     | Power       |                 |                       |
| U12  | VTT    |     | Power       |                 |                       |
| U16  | VTT    |     | Power       |                 |                       |
| W03  | VTT    |     | Power       |                 |                       |
| Y11  | WDEVT# | I   | AGTL+       |                 |                       |
| T11  | WDME#  | I   | AGTL+       |                 |                       |

**Table 12-30: RCG Pin List Sorted by Signal**

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| N05  | ADDRA00 | O   | LVTTTL      | 10ma            |                          |
| N03  | ADDRA01 | O   | LVTTTL      | 10ma            |                          |
| P02  | ADDRA02 | O   | LVTTTL      | 10ma            |                          |
| P01  | ADDRA03 | O   | LVTTTL      | 10ma            |                          |
| P04  | ADDRA04 | O   | LVTTTL      | 10ma            |                          |
| P03  | ADDRA05 | O   | LVTTTL      | 10ma            |                          |
| R03  | ADDRA06 | O   | LVTTTL      | 10ma            |                          |
| T02  | ADDRA07 | O   | LVTTTL      | 10ma            |                          |
| T01  | ADDRA08 | O   | LVTTTL      | 10ma            |                          |
| T04  | ADDRA09 | O   | LVTTTL      | 10ma            |                          |
| T03  | ADDRA10 | O   | LVTTTL      | 10ma            |                          |
| U01  | ADDRA11 | O   | LVTTTL      | 10ma            |                          |
| V02  | ADDRA12 | O   | LVTTTL      | 10ma            |                          |
| V01  | ADDRA13 | O   | LVTTTL      | 10ma            |                          |
| J20  | ADDRB00 | O   | LVTTTL      | 10ma            |                          |
| J19  | ADDRB01 | O   | LVTTTL      | 10ma            |                          |
| J18  | ADDRB02 | O   | LVTTTL      | 10ma            |                          |
| J17  | ADDRB03 | O   | LVTTTL      | 10ma            |                          |
| J16  | ADDRB04 | O   | LVTTTL      | 10ma            |                          |
| G20  | ADDRB05 | O   | LVTTTL      | 10ma            |                          |
| G19  | ADDRB06 | O   | LVTTTL      | 10ma            |                          |
| H18  | ADDRB07 | O   | LVTTTL      | 10ma            |                          |
| H16  | ADDRB08 | O   | LVTTTL      | 10ma            |                          |
| F20  | ADDRB09 | O   | LVTTTL      | 10ma            |                          |
| G18  | ADDRB10 | O   | LVTTTL      | 10ma            |                          |
| G17  | ADDRB11 | O   | LVTTTL      | 10ma            |                          |
| E20  | ADDRB12 | O   | LVTTTL      | 10ma            |                          |
| F18  | ADDRB13 | O   | LVTTTL      | 10ma            |                          |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown  |
|------|----------|-----|-------------|-----------------|---------------------------|
| C03  | ADDRRC00 | O   | LVTTTL      | 10ma            |                           |
| E04  | ADDRRC01 | O   | LVTTTL      | 10ma            |                           |
| D03  | ADDRRC02 | O   | LVTTTL      | 10ma            |                           |
| C02  | ADDRRC03 | O   | LVTTTL      | 10ma            |                           |
| E03  | ADDRRC04 | O   | LVTTTL      | 10ma            |                           |
| C01  | ADDRRC05 | O   | LVTTTL      | 10ma            |                           |
| F03  | ADDRRC06 | O   | LVTTTL      | 10ma            |                           |
| E02  | ADDRRC07 | O   | LVTTTL      | 10ma            |                           |
| D01  | ADDRRC08 | O   | LVTTTL      | 10ma            |                           |
| G04  | ADDRRC09 | O   | LVTTTL      | 10ma            |                           |
| E01  | ADDRRC10 | O   | LVTTTL      | 10ma            |                           |
| G03  | ADDRRC11 | O   | LVTTTL      | 10ma            |                           |
| G02  | ADDRRC12 | O   | LVTTTL      | 10ma            |                           |
| F01  | ADDRRC13 | O   | LVTTTL      | 10ma            |                           |
| C14  | ADDRRD00 | O   | LVTTTL      | 10ma            |                           |
| A14  | ADDRRD01 | O   | LVTTTL      | 10ma            |                           |
| C13  | ADDRRD02 | O   | LVTTTL      | 10ma            |                           |
| A12  | ADDRRD03 | O   | LVTTTL      | 10ma            |                           |
| B12  | ADDRRD04 | O   | LVTTTL      | 10ma            |                           |
| C12  | ADDRRD05 | O   | LVTTTL      | 10ma            |                           |
| D12  | ADDRRD06 | O   | LVTTTL      | 10ma            |                           |
| E12  | ADDRRD07 | O   | LVTTTL      | 10ma            |                           |
| A11  | ADDRRD08 | O   | LVTTTL      | 10ma            |                           |
| C11  | ADDRRD09 | O   | LVTTTL      | 10ma            |                           |
| E11  | ADDRRD10 | O   | LVTTTL      | 10ma            |                           |
| E10  | ADDRRD11 | O   | LVTTTL      | 10ma            |                           |
| C10  | ADDRRD12 | O   | LVTTTL      | 10ma            |                           |
| A10  | ADDRRD13 | O   | LVTTTL      | 10ma            |                           |
| V15  | AVWP#    | O   | AGTL+       | 55ma            |                           |
| T12  | BANK0#   | I   | AGTL+       |                 |                           |
| V12  | BANK1#   | I   | AGTL+       |                 |                           |
| W12  | BANK2#   | I   | AGTL+       |                 |                           |
| T18  | BANKID#  | I   | LVTTTL      |                 | Requires external pull-up |
| Y13  | CARD#    | I   | AGTL+       |                 |                           |
| K01  | CASAA0#  | O   | LVTTTL      | 10ma            |                           |
| H05  | CASAA1#  | O   | LVTTTL      | 10ma            |                           |
| K03  | CASAB0#  | O   | LVTTTL      | 10ma            |                           |
| J02  | CASAB1#  | O   | LVTTTL      | 10ma            |                           |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| H03  | CASAC0# | O   | LVTTTL      | 10ma            |                          |
| J05  | CASAC1# | O   | LVTTTL      | 10ma            |                          |
| K05  | CASAD0# | O   | LVTTTL      | 10ma            |                          |
| J03  | CASAD1# | O   | LVTTTL      | 10ma            |                          |
| M16  | CASBA0# | O   | LVTTTL      | 10ma            |                          |
| N18  | CASBA1# | O   | LVTTTL      | 10ma            |                          |
| M19  | CASBB0# | O   | LVTTTL      | 10ma            |                          |
| M17  | CASBB1# | O   | LVTTTL      | 10ma            |                          |
| P18  | CASBC0# | O   | LVTTTL      | 10ma            |                          |
| T20  | CASBC1# | O   | LVTTTL      | 10ma            |                          |
| P19  | CASBD0# | O   | LVTTTL      | 10ma            |                          |
| R18  | CASBD1# | O   | LVTTTL      | 10ma            |                          |
| A03  | CASCA0# | O   | LVTTTL      | 10ma            |                          |
| D07  | CASCA1# | O   | LVTTTL      | 10ma            |                          |
| C07  | CASCB0# | O   | LVTTTL      | 10ma            |                          |
| A05  | CASCB1# | O   | LVTTTL      | 10ma            |                          |
| B05  | CASCC0# | O   | LVTTTL      | 10ma            |                          |
| B09  | CASCC1# | O   | LVTTTL      | 10ma            |                          |
| C08  | CASCD0# | O   | LVTTTL      | 10ma            |                          |
| B07  | CASCD1# | O   | LVTTTL      | 10ma            |                          |
| D16  | CASDA0# | O   | LVTTTL      | 10ma            |                          |
| A19  | CASDA1# | O   | LVTTTL      | 10ma            |                          |
| C18  | CASDB0# | O   | LVTTTL      | 10ma            |                          |
| D18  | CASDB1# | O   | LVTTTL      | 10ma            |                          |
| A18  | CASDC0# | O   | LVTTTL      | 10ma            |                          |
| B20  | CASDC1# | O   | LVTTTL      | 10ma            |                          |
| C19  | CASDD0# | O   | LVTTTL      | 10ma            |                          |
| B18  | CASDD1# | O   | LVTTTL      | 10ma            |                          |
| Y12  | CMND0#  | I   | AGTL+       |                 |                          |
| T11  | CMND1#  | I   | AGTL+       |                 |                          |
| V04  | CRES0   | I   | Analog      |                 |                          |
| V03  | CRES1   | I   | Analog      |                 |                          |
| V11  | CSTB#   | I   | AGTL+       |                 |                          |
| U18  | DR50H#  | I   | LVTTTL      |                 |                          |
| T19  | DR50T#  | I   | LVTTTL      |                 |                          |
| A01  | GND     |     | Power       |                 |                          |
| A06  | GND     |     | Power       |                 |                          |
| A15  | GND     |     | Power       |                 |                          |

**Table 12-30: RCG Pin List Sorted by Signal (Continued)**

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| A20  | GND    |     | Power       |                 |                          |
| B02  | GND    |     | Power       |                 |                          |
| B06  | GND    |     | Power       |                 |                          |
| B10  | GND    |     | Power       |                 |                          |
| B11  | GND    |     | Power       |                 |                          |
| B15  | GND    |     | Power       |                 |                          |
| B19  | GND    |     | Power       |                 |                          |
| F02  | GND    |     | Power       |                 |                          |
| F19  | GND    |     | Power       |                 |                          |
| H04  | GND    |     | Power       |                 |                          |
| H17  | GND    |     | Power       |                 |                          |
| J09  | GND    |     | Power       |                 |                          |
| J10  | GND    |     | Power       |                 |                          |
| J11  | GND    |     | Power       |                 |                          |
| J12  | GND    |     | Power       |                 |                          |
| N04  | GND    |     | Power       |                 |                          |
| N17  | GND    |     | Power       |                 |                          |
| R01  | GND    |     | Power       |                 |                          |
| R02  | GND    |     | Power       |                 |                          |
| R19  | GND    |     | Power       |                 |                          |
| R20  | GND    |     | Power       |                 |                          |
| W06  | GND    |     | Power       |                 |                          |
| W10  | GND    |     | Power       |                 |                          |
| W11  | GND    |     | Power       |                 |                          |
| W15  | GND    |     | Power       |                 |                          |
| W19  | GND    |     | Power       |                 |                          |
| Y01  | GND    |     | Power       |                 |                          |
| Y06  | GND    |     | Power       |                 |                          |
| Y15  | GND    |     | Power       |                 |                          |
| Y20  | GND    |     | Power       |                 |                          |
| D04  | GND    |     | Power       |                 |                          |
| D08  | GND    |     | Power       |                 |                          |
| D13  | GND    |     | Power       |                 |                          |
| D17  | GND    |     | Power       |                 |                          |
| K02  | GND    |     | Power       |                 |                          |
| K09  | GND    |     | Power       |                 |                          |
| K10  | GND    |     | Power       |                 |                          |
| K11  | GND    |     | Power       |                 |                          |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal   | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|----------|-----|-------------|-----------------|--------------------------|
| K12  | GND      |     | Power       |                 |                          |
| K19  | GND      |     | Power       |                 |                          |
| L02  | GND      |     | Power       |                 |                          |
| L09  | GND      |     | Power       |                 |                          |
| L10  | GND      |     | Power       |                 |                          |
| L11  | GND      |     | Power       |                 |                          |
| L12  | GND      |     | Power       |                 |                          |
| L19  | GND      |     | Power       |                 |                          |
| M09  | GND      |     | Power       |                 |                          |
| M10  | GND      |     | Power       |                 |                          |
| M11  | GND      |     | Power       |                 |                          |
| M12  | GND      |     | Power       |                 |                          |
| U04  | GND      |     | Power       |                 |                          |
| U08  | GND      |     | Power       |                 |                          |
| U13  | GND      |     | Power       |                 |                          |
| U17  | GND      |     | Power       |                 |                          |
| W02  | GND      |     | Power       |                 |                          |
| Y14  | GRCMPLT# | I/O | AGTL+       | 55ma            |                          |
| V10  | HCLKIN   | I   | 2.5V        |                 |                          |
| Y16  | LDSTB#   | O   | AGTL+       | 55ma            |                          |
| T15  | LRD#     | O   | AGTL+       | 55ma            |                          |
| V09  | MA00#    | I   | AGTL+       |                 |                          |
| W09  | MA01#    | I   | AGTL+       |                 |                          |
| T08  | MA02#    | I   | AGTL+       |                 |                          |
| V08  | MA03#    | I   | AGTL+       |                 |                          |
| Y08  | MA04#    | I   | AGTL+       |                 |                          |
| T07  | MA05#    | I   | AGTL+       |                 |                          |
| U07  | MA06#    | I   | AGTL+       |                 |                          |
| V07  | MA07#    | I   | AGTL+       |                 |                          |
| Y07  | MA08#    | I   | AGTL+       |                 |                          |
| V06  | MA09#    | I   | AGTL+       |                 |                          |
| W05  | MA10#    | I   | AGTL+       |                 |                          |
| Y05  | MA11#    | I   | AGTL+       |                 |                          |
| Y04  | MA12#    | I   | AGTL+       |                 |                          |
| Y03  | MA13#    | I   | AGTL+       |                 |                          |
| Y09  | MRESET#  | I   | AGTL+       |                 |                          |
| T17  | VCC      |     | Power       |                 |                          |
| P16  | N/C      |     |             |                 |                          |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| R05  | N/C     |     |             |                 |                          |
| R16  | N/C     |     |             |                 |                          |
| T05  | N/C     |     |             |                 |                          |
| T06  | N/C     |     |             |                 |                          |
| T09  | N/C     |     |             |                 |                          |
| T13  | N/C     |     |             |                 |                          |
| T16  | N/C     |     |             |                 |                          |
| E05  | N/C     |     |             |                 |                          |
| E06  | N/C     |     |             |                 |                          |
| E07  | N/C     |     |             |                 |                          |
| E08  | N/C     |     |             |                 |                          |
| E09  | N/C     |     |             |                 |                          |
| E14  | N/C     |     |             |                 |                          |
| E15  | N/C     |     |             |                 |                          |
| E16  | N/C     |     |             |                 |                          |
| F05  | N/C     |     |             |                 |                          |
| F16  | N/C     |     |             |                 |                          |
| G05  | N/C     |     |             |                 |                          |
| G16  | N/C     |     |             |                 |                          |
| N16  | N/C     |     |             |                 |                          |
| P05  | N/C     |     |             |                 |                          |
| Y10  | VCC     |     | Power       |                 |                          |
| C09  | N/C     |     |             |                 |                          |
| D09  | N/C     |     |             |                 |                          |
| D20  | N/C     |     |             |                 |                          |
| E17  | N/C     |     |             |                 |                          |
| E18  | N/C     |     |             |                 |                          |
| E19  | N/C     |     |             |                 |                          |
| G01  | N/C     |     |             |                 |                          |
| W1   | N/C     |     |             |                 |                          |
| W16  | N/C     |     |             |                 |                          |
| W20  | N/C     |     |             |                 |                          |
| Y02  | N/C     |     |             |                 |                          |
| U03  | N/C     |     |             |                 |                          |
| Y17  | N/C     |     |             |                 |                          |
| Y19  | N/C     |     |             |                 |                          |
| V14  | PHIT#   | O   | AGTL+       | 55ma            |                          |
| L01  | RASAA0# | O   | LVTTL       | 10ma            |                          |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal  | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|---------|-----|-------------|-----------------|--------------------------|
| M02  | RASAA1# | O   | LVTTTL      | 10ma            |                          |
| M01  | RASAB0# | O   | LVTTTL      | 10ma            |                          |
| M03  | RASAB1# | O   | LVTTTL      | 10ma            |                          |
| L03  | RASAC0# | O   | LVTTTL      | 10ma            |                          |
| M04  | RASAC1# | O   | LVTTTL      | 10ma            |                          |
| L05  | RASAD0# | O   | LVTTTL      | 10ma            |                          |
| M05  | RASAD1# | O   | LVTTTL      | 10ma            |                          |
| L18  | RASBA0# | O   | LVTTTL      | 10ma            |                          |
| L16  | RASBA1# | O   | LVTTTL      | 10ma            |                          |
| M18  | RASBB0# | O   | LVTTTL      | 10ma            |                          |
| K16  | RASBB1# | O   | LVTTTL      | 10ma            |                          |
| L20  | RASBC0# | O   | LVTTTL      | 10ma            |                          |
| K18  | RASBC1# | O   | LVTTTL      | 10ma            |                          |
| M20  | RASBD0# | O   | LVTTTL      | 10ma            |                          |
| K20  | RASBD1# | O   | LVTTTL      | 10ma            |                          |
| A02  | RASCA0# | O   | LVTTTL      | 10ma            |                          |
| B01  | RASCA1# | O   | LVTTTL      | 10ma            |                          |
| A04  | RASCB0# | O   | LVTTTL      | 10ma            |                          |
| B03  | RASCB1# | O   | LVTTTL      | 10ma            |                          |
| C05  | RASCC0# | O   | LVTTTL      | 10ma            |                          |
| C04  | RASCC1# | O   | LVTTTL      | 10ma            |                          |
| C06  | RASCD0# | O   | LVTTTL      | 10ma            |                          |
| D05  | RASCD1# | O   | LVTTTL      | 10ma            |                          |
| C15  | RASDA0# | O   | LVTTTL      | 10ma            |                          |
| E13  | RASDA1# | O   | LVTTTL      | 10ma            |                          |
| C16  | RASDB0# | O   | LVTTTL      | 10ma            |                          |
| D14  | RASDB1# | O   | LVTTTL      | 10ma            |                          |
| B16  | RASDC0# | O   | LVTTTL      | 10ma            |                          |
| B14  | RASDC1# | O   | LVTTTL      | 10ma            |                          |
| A17  | RASDD0# | O   | LVTTTL      | 10ma            |                          |
| A16  | RASDD1# | O   | LVTTTL      | 10ma            |                          |
| V13  | RCMPLT# | O   | AGTL+       | 55ma            |                          |
| U14  | RHIT#   | O   | AGTL+       | 55ma            |                          |
| Y11  | ROW#    | I   | AGTL+       |                 |                          |
| V18  | TCK     | I   | LVTTTL      |                 |                          |
| V20  | TDI     | I   | LVTTTL      |                 |                          |
| V19  | TDO     | O   | OD          | 14ma            |                          |
| Y18  | TMS     | I   | LVTTTL      |                 |                          |

Table 12-30: RCG Pin List Sorted by Signal (Continued)

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| V17  | TRST#  | I   | LVTTL       |                 |                          |
| D11  | VCC    |     | Power       |                 |                          |
| D15  | VCC    |     | Power       |                 |                          |
| D19  | VCC    |     | Power       |                 |                          |
| K04  | VCC    |     | Power       |                 |                          |
| K17  | VCC    |     | Power       |                 |                          |
| L04  | VCC    |     | Power       |                 |                          |
| L17  | VCC    |     | Power       |                 |                          |
| N01  | VCC    |     | Power       |                 |                          |
| N02  | VCC    |     | Power       |                 |                          |
| U02  | VCC    |     | Power       |                 |                          |
| U06  | VCC    |     | Power       |                 |                          |
| U10  | VCC    |     | Power       |                 |                          |
| U11  | VCC    |     | Power       |                 |                          |
| U15  | VCC    |     | Power       |                 |                          |
| U19  | VCC    |     | Power       |                 |                          |
| U20  | VCC    |     | Power       |                 |                          |
| W04  | VCC    |     | Power       |                 |                          |
| A08  | VCC    |     | Power       |                 |                          |
| A13  | VCC    |     | Power       |                 |                          |
| B04  | VCC    |     | Power       |                 |                          |
| B08  | VCC    |     | Power       |                 |                          |
| B13  | VCC    |     | Power       |                 |                          |
| B17  | VCC    |     | Power       |                 |                          |
| F04  | VCC    |     | Power       |                 |                          |
| F06  | VCC    |     | Power       |                 |                          |
| F14  | VCC    |     | Power       |                 |                          |
| F15  | VCC    |     | Power       |                 |                          |
| F17  | VCC    |     | Power       |                 |                          |
| G06  | VCC    |     | Power       |                 |                          |
| H01  | VCC    |     | Power       |                 |                          |
| H02  | VCC    |     | Power       |                 |                          |
| H19  | VCC    |     | Power       |                 |                          |
| H20  | VCC    |     | Power       |                 |                          |
| N19  | VCC    |     | Power       |                 |                          |
| N20  | VCC    |     | Power       |                 |                          |
| P15  | VCC    |     | Power       |                 |                          |
| R04  | VCC    |     | Power       |                 |                          |

**Table 12-30: RCG Pin List Sorted by Signal (Continued)**

| Pin# | Signal | I/O | Driver Type | Driver Strength | Internal Pullup/Pulldown |
|------|--------|-----|-------------|-----------------|--------------------------|
| R06  | VCC    |     | Power       |                 |                          |
| R07  | VCC    |     | Power       |                 |                          |
| R15  | VCC    |     | Power       |                 |                          |
| R17  | VCC    |     | Power       |                 |                          |
| W08  | VCC    |     | Power       |                 |                          |
| W13  | VCC    |     | Power       |                 |                          |
| W17  | VCC    |     | Power       |                 |                          |
| D02  | VCC    |     | Power       |                 |                          |
| D06  | VCC    |     | Power       |                 |                          |
| D10  | VCC    |     | Power       |                 |                          |
| T10  | VCCA   |     | Power       |                 |                          |
| V05  | VREF   | I   | Analog      |                 |                          |
| V16  | VREF   | I   | Analog      |                 |                          |
| W07  | VTT    |     | Power       |                 |                          |
| W14  | VTT    |     | Power       |                 |                          |
| W18  | VTT    |     | Power       |                 |                          |
| U05  | VTT    |     | Power       |                 |                          |
| U09  | VTT    |     | Power       |                 |                          |
| U12  | VTT    |     | Power       |                 |                          |
| U16  | VTT    |     | Power       |                 |                          |
| W03  | VTT    |     | Power       |                 |                          |
| T14  | WDME#  | O   | AGTL+       | 55ma            |                          |
| J01  | WEAA#  | O   | LVTTL       | 10ma            |                          |
| J04  | WEAB#  | O   | LVTTL       | 10ma            |                          |
| P17  | WEBA#  | O   | LVTTL       | 10ma            |                          |
| P20  | WEBB#  | O   | LVTTL       | 10ma            |                          |
| A07  | WECA#  | O   | LVTTL       | 10ma            |                          |
| A09  | WECB#  | O   | LVTTL       | 10ma            |                          |
| C17  | WEDA#  | O   | LVTTL       | 10ma            |                          |
| C20  | WEDB#  | O   | LVTTL       | 10ma            |                          |

## 12.9.3 Package information

### 12.9.3.1 324 BGA Package Information

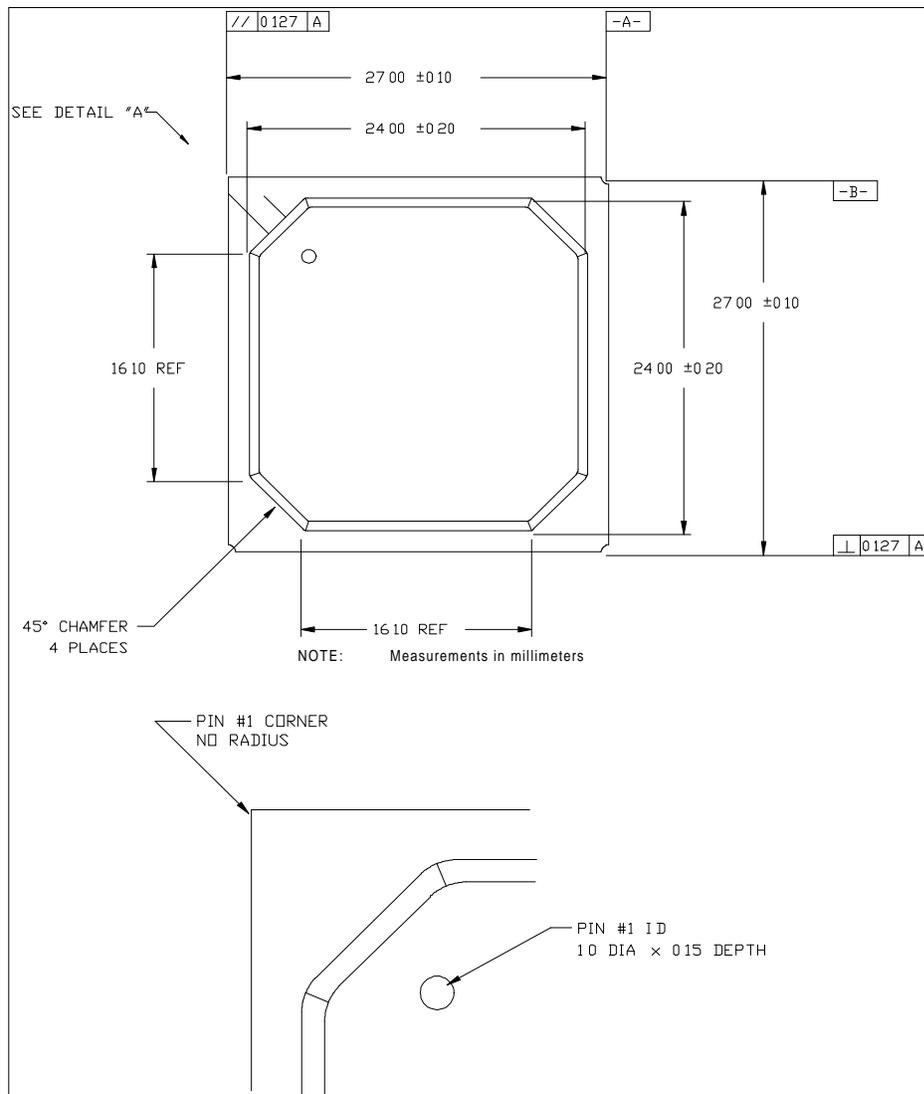


Figure 12-15: 324 BGA Dimension Top View

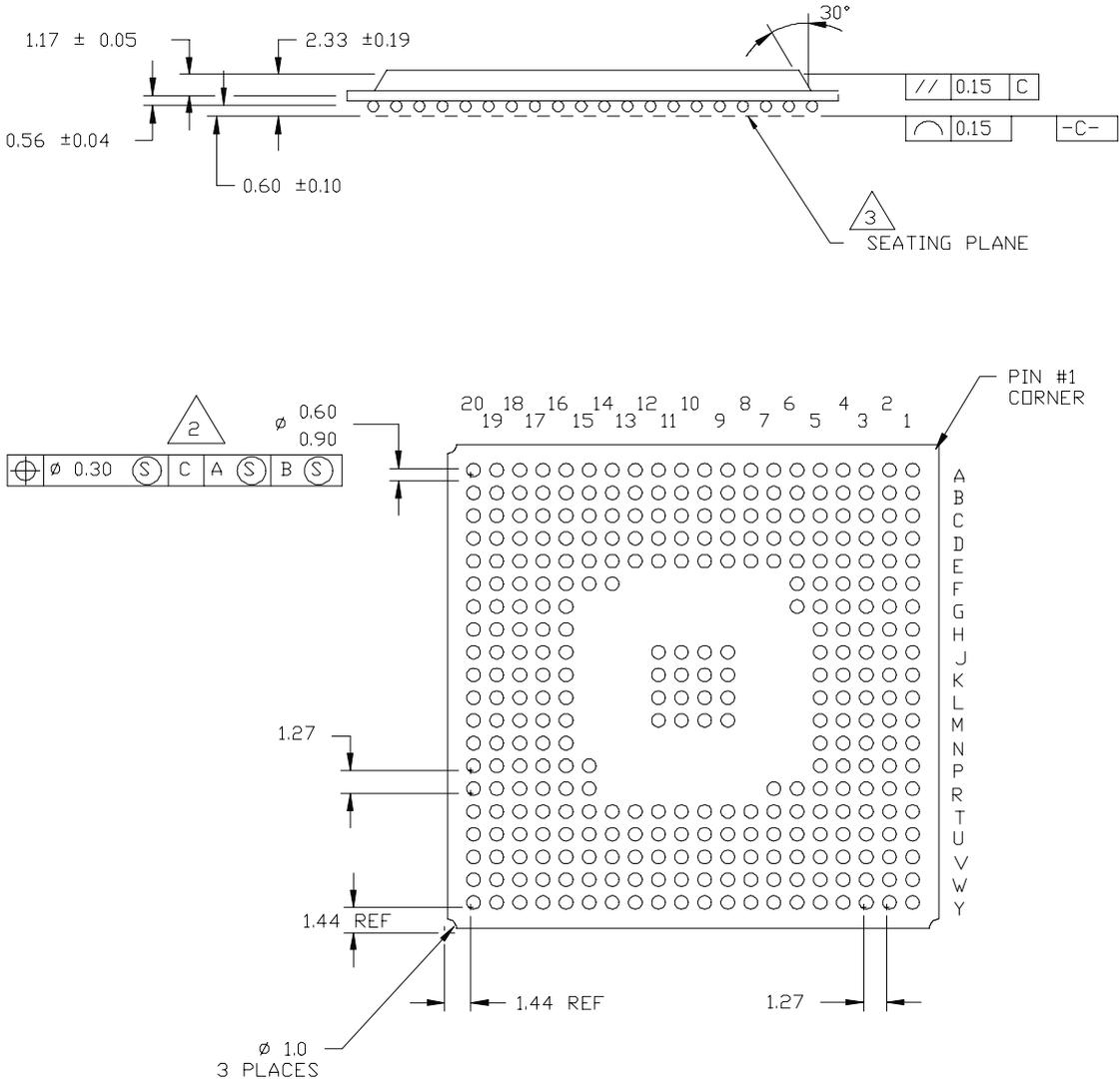
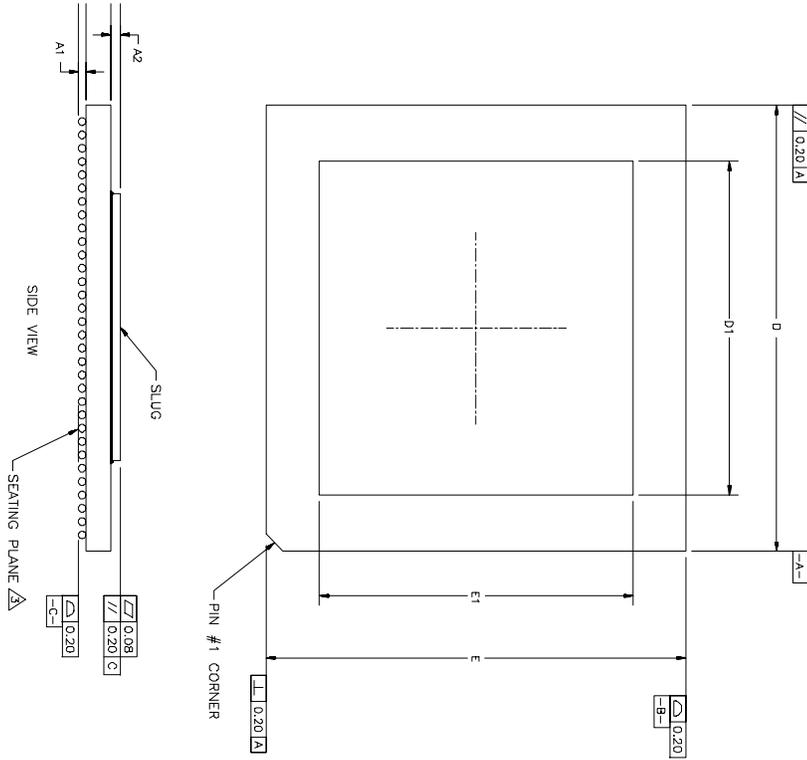
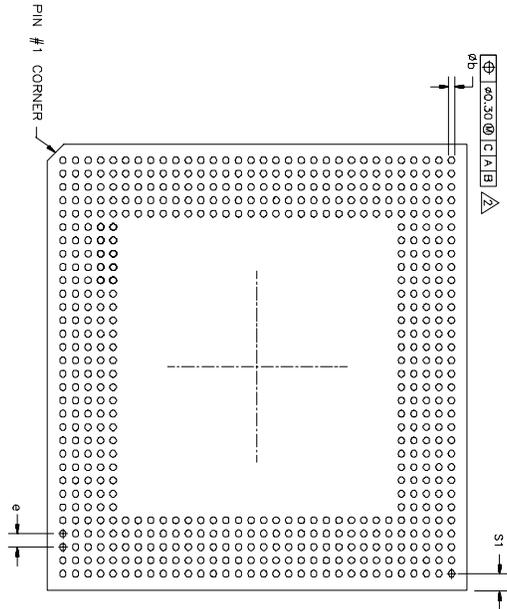


Figure 12-16: 324 BGA Dimensions Bottom View

12.9.3.2 540 PBGA Package Information



- NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
  2. DIMENSIONS IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM  $C$ .
  3. PRIMARY DATUM  $C$  AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
  4. ALL DIMENSIONS ARE IN MILLIMETERS



**Table 12-31: 540 PBGA dimensions**

| Package Dimensions |          |       |
|--------------------|----------|-------|
| Packages           |          |       |
|                    | 540 LD   |       |
| Symbol             | Min      | Max   |
| A                  | 3.59     | 4.10  |
| A <sub>1</sub>     | 0.40     | 0.70  |
| A <sub>2</sub>     | 0.95     | 1.10  |
| b                  | 0.60     | 0.90  |
| c                  | 2.00     | 2.30  |
| D                  | 42.30    | 42.70 |
| D <sub>1</sub>     | -        | 27.70 |
| E                  | 42.30    | 42.70 |
| E <sub>1</sub>     | -        | 27.70 |
| e                  | 1.27     |       |
| N                  | 540      |       |
| S <sub>1</sub>     | 1.56 REF |       |

**NOTE:** Measurement in millimeters

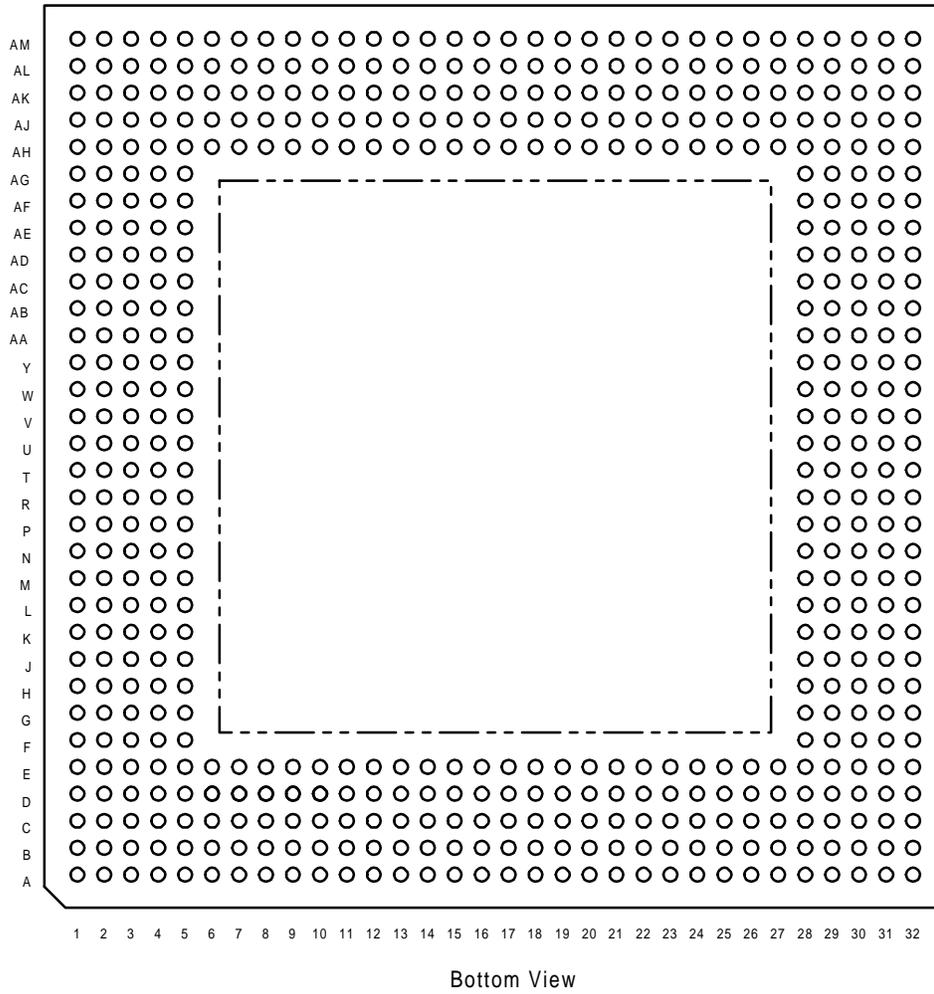


Figure 12-17: 540 PBGA Pin Grid





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