# i860™ Processor Performance

**Release 1.0**

**March 1989**

**Intel Corporation**

# Contents



# Figures



# Tables

# i860™ Processor Performance

**Release 1.0**

**March 1989**

**Intel Corporation**

# Contents



# Figures



# Tables

# 1 The i860™ Processor

The i860 processor is a highly integrated 64-bit RISC processor. Integrated on-chip are the integer execution unit, pipelined floating-point adder and multiplier units, 3-D graphics unit, four-KByte instruction cache, eight-KByte data cache and paging unit. Up to three operations can simultaneously take place in the integer, floating-point adder and multiplier units. The internal instruction bus is 64 bits wide while the internal cache bus is 128 bits wide. The parallel architecture provides unprecedented and balanced performance in integer, floating-point and 3-D graphics operations. The block diagram of the i860 processor is shown in Figure 1. The current maximum operating frequency of the i860 processor is 40 MHz.

# 2 Introduction

Benchmark programs evaluate the performance of not only a given architecture but also a host of other tightly coupled hardware/software constituents. Operating system, compilers, libraries, system workload, memory design and I/O subsystem each play a key role. It is not unusual for sub-optimizations in these external elements to undermine the performance of the underlying processor architecture. It is certainly the case for the i860 processor since the compilers and libraries used are in their preliminary form and the memory subsystem is less than optimized. In addition, there are a few errata impacting the performance identified on the first stepping of the i860 processor silicon on which all the measured benchmark results were obtained. Despite all of these performance detriments, the i860 processor still outperforms all other high performance microprocessors. Future improvements on the clock frequency of the i860 processor, the compiler, vectorizer, vector libraries and memory subsystem will further increase the performance of the i860 processor.

Popular benchmarks are the Dhrystone and Stanford Integer Suite for integer performance evaluation, and the Linpack and Whetstone for floating-point performance evaluation. For programs which are highly vectorizable, the vector processing capability of the i860 processor really distinguishes the processor from other RISC processors, as illustrated later by the vectorized Linpack results. In fact, the vector performance of the i860 processor approaches that of the supercomputers and mainframes with vector hardware.

Integer performance comparisons are made to that of VAX 11/780 under UNIX (BSD 4.3). There is not a single machine for floating-point comparisons.

# 3 Performance Summary

The measured, simulated and projected performance numbers are presented in this section. The i860 processor performance is then compared with that of other processors.

## 3.1 i860 Processor Benchmark Results

Benchmark results for the 40 MHz i860 processor are summarized in Table 1. All the benchmarks were run on a 33.3 MHz system and the numbers for 40 MHz were calculated by

Table 1. i860™ Processor Benchmark Results at 40 MHz

| Benchmarks | Measured Results | Simulated Results | Projected Results |
|---|---|---|---|
| **Dhrystone(KDhry/sec)** | | | |
| Version 1.1 | 82.9 | 86.2 | 90.0 |
| Version 2.1 | 78.1 | N.A. | 85.0 |
| **Stanford Integer(MIPS)** | N.A. | 32.1 | 33.2 |
| **Whetstone (MWhet/sec)** | | | |
| Single Precision | 30.8 | 30.6 | 32.0 |
| Double Precision | 24.0 | 23.3 | 25.0 |
| **Linpack(MFLOPS)** | | | |
| Fortran Double | N.A. | 7.3 | 10.0 |
| Coded Double | N.A. | 13.2 | 13.2 |

### 3.2 Performance Comparisons

The benchmark results are compared with that for other processors in Figures 2 and 3. The data on the MIPS R3000, Motorola 88000 and Sun SPARC are published data. The i860™ processor outperforms all other microprocessors in every benchmark category.

## 4 Benchmarking Methodology

All available performance results on the i860 processor are presented. The results from versions 1.1 and 2.1 of Dhrystone are presented, although version 1.1 results tends to be better and hence are still quoted by the industry. Also, the Linpack results for both the (assembly) coded and vectorized Fortran BLASes are provided.

Unless otherwise stated, all data are actual data obtained on the benchmarking system. Simulation results are meant only to provide the complete performance comparisons and to reflect what the i860 processor can do. More benchmark results will be incorporated in the next release of this document as soon as they become available.

Specific benchmark configurations and conditions will be fully described to facilitate performance comparison and verification.

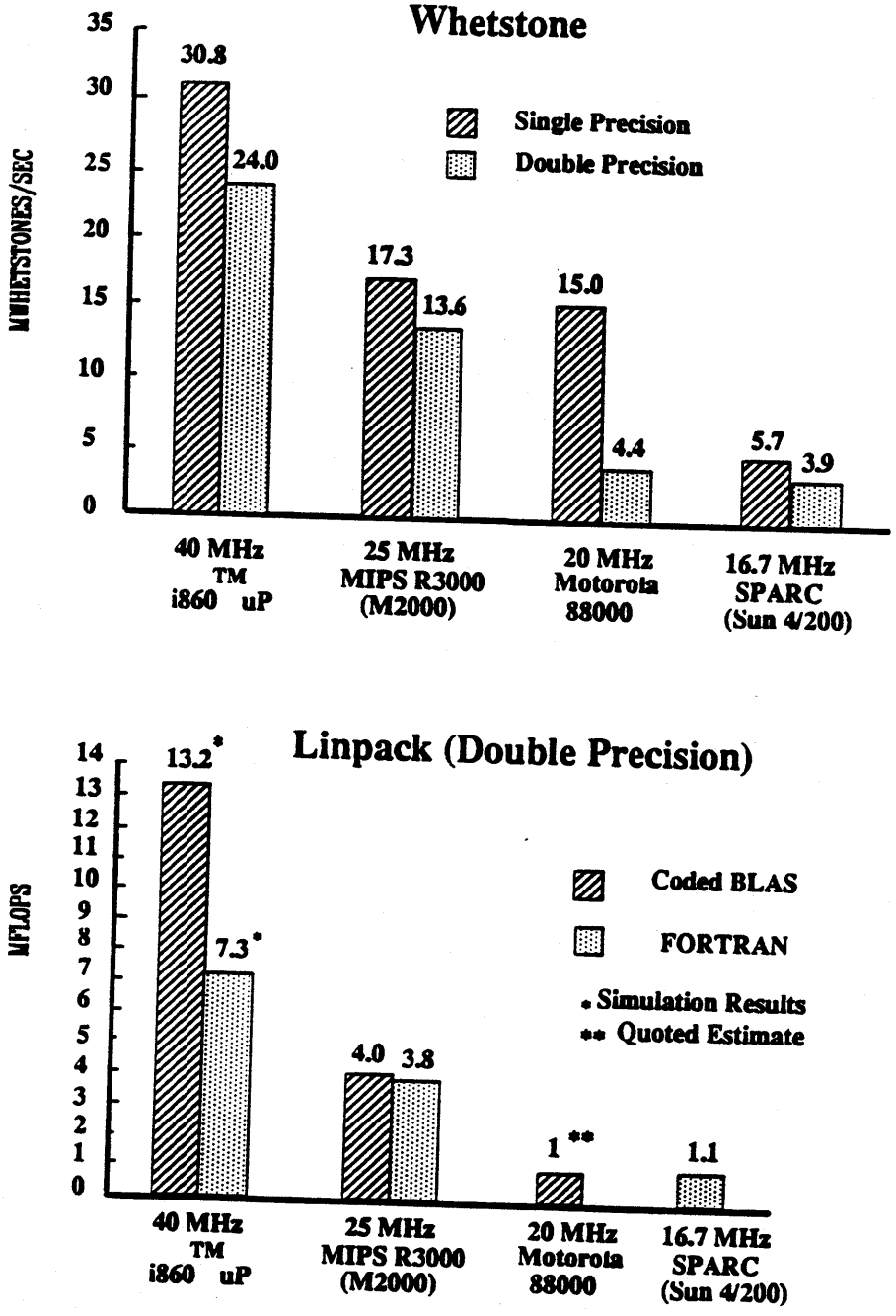


**Figure 3**: Summary of Floating-Point Benchmark Results

### 5.2 Compilation and Run-Time Conditions

**Host Link.** The benchmarking system runs under OS/2 ver 1.10 with the communications software, Host Link to connect to the 386 microprocessor based host machine. The communications software resides on both the host and the i860 processor based add-in card. The Host Link software also provides similar operating environment on the simulation vehicle.

**Compilers.** Compilation Optimizations are as follows:

| Benchmark | Compiler Version | Options |
|---|---|---|
| Dhrystone | Green Hills Fortran 1.8.5 | Note 1 |
| Stanford | Green Hills C 1.8.5 | Note 1 |
| Whetstone | Green Hills Fortran 1.8.5 | Note 2 |
| Linpack | Green Hills Fortran 1.8.5 | Note 1 |

Note 1: –OLM –X405 –X370 –X393 –X422
Note 2: –OLM –X405 –X370 –X393 –X422 –X425
–X425 generates less optimal code to work around errata on early steppings. The measured performance would be negatively impacted by the workarounds. However, simulation was performed without workaround code for the errata.

Refer to compiler documents provided by the compiler vendors for option explanations.

**Vectorizer.** The PSR (Pacific Sierra Research) Fortran vectorizer (version 2.25N1) functions as a preprocessor to vectorize code. An equivalent Fortran program containing calls to vector libraries is produced. The vectorizer is used to vectorize the benchmarks (for example, Linpack) prior to normal compilation.

**Libraries.** PSR math libraries are used. The libraries are written in assembly code. Beta site release dated Feb 2, 1989 was used.

### 5.3 Timing Measurements and Host Link Overheads

The timing mechanism on the benchmarking system is implemented via timer interrupts (every 13.3 ms) to the i860 processor. Interrupt overheads in the Host Link are impossible to single out and are hence embedded in the measured results. As much as 5% performance degradation due to the overheads has been identified in benchmarks such Stanford Integer Suite, and Linpack.

## 6 Benchmark Results

The benchmark results are discussed below. Brief description of the benchmarks is also given. Performance numbers for other processors on the market are published data.

Table 2. Dhrystone Benchmark Results

| Dhry's /Sec | Rel. | System |
|---|---|---|
| 1,571 | 0.9 | VAX 11/780, 4.3BSD [MIPS 88] |
| 1,757 | 1.0 | VAX 11/780, VAX/VMS 4.2 [Intergraph 86] |
| 3,850 | 2.2 | Sun-3/100 [Muchnick 88] |
| 6,374 | 3.6 | Sun-3/260, 25MHz 68020, SunOS 3.2 |
| 6,423 | 3.7 | VAX 8600, 4.3BSD |
| 6,440 | 3.7 | IBM 4381-2, UTS V, cc 1.11 |
| 6,896 | 3.9 | Intergraph InterPro 32C, SYSV R3 3.0.0, Green hills,-O |
| 7,109 | 4.0 | Apollo DN4000 -O |
| 7,140 | 4.1 | Sun-3/200 [Munchnick 88] |
| 7,249 | 4.2 | Convex C-1 XP 6.0, vc 1.1 |
| 7,409 | 4.2 | VAX 8600, VAX/VMS in [Intergraph 86] |
| 7,655 | 4.4 | Alliant FX/8 [Alliant 86] |
| 8,309 | 4.7 | InterPro-326, 30MHz Clipper, Green Hills [Intergraph 86] |
| 9,436 | 5.4 | Convergent Server PC, 20MHz, 80386, GreenHills |
| 9,920 | 5.6 | HP 9000/840S [HP87] |
| 10,416 | 5.9 | VAX 8550, VAX/VMS 4.5, cc 2.2 |
| 10,787 | 6.1 | VAX 8650, VAX/VMS, [Intergraph 86] |
| 11,215 | 6.4 | HP 9000/840, HP-UX, full optimization |
| 12,639 | 7.2 | HP 9000/825S [HP 87] |
| 13,000 | 7.4 | MIPS M/500, 8MHz R2000, -O3 |
| 13,157 | 7.5 | HP 825SRX [Sun 87] |
| 14,109 | 8.0 | Sun-4/110 [Sun 88] |
| 14,195 | 8.1 | Multiflow Trace 7/200 [Multiflow] |
| 14,820 | 8.4 | CRAY 1S |
| 15,007 | 8.5 | IBM 3081, UTS SUR2.5, cc 1.5 |
| 15,576 | 8.9 | HP 9000/850 [HP 87] |
| 18,530 | 10.5 | CRAY X-MP |
| 19,000 | 10.8 | Sun-4/200, 16.7MHz SPARC [Muchnick 88], -O3 |
| 19,800 | 11.3 | MIPS M/800, 12.5MHz R200, -O3 |
| 23,430 | 13.3 | HP 835S [RISC Mgmt 88] |
| 23,700 | 13.5 | MIPS M/1000, 15MHz R2000, -O3 |
| 27,400 | 15.6 | MIPS M/120-5, 16.7MHz R2000, -O3 |
| 28,846 | 16.4 | Amdahl 5860, UTS-V, cc1.22 |
| 31,250 | 17.8 | IBM 3090/200 |
| 34,000 | 19.4 | Motorola 88000, 20MHz unknown configuration [RISC Mgmt 88] |
| 35,653 | 20.3 | AMD 2900, 25MHz, 2 8K caches (simulation) [AMD 88] |
| 42,300 | 24.1 | MIPS M/2000, 25MHz R3000, -O3 |
| 43,668 | 24.9 | Amdahl 5890/300E, cc-O |
| 53,108 | 30.2 | CCI Power 7/64 (simulation) [Simpson 88] |
| **69,000** | **39.3** | **i860 uP @ 33.3MHz (Measured)** |
| **82,900** | **47.2** | **i860 uP @ 40MHz (Scaled from 33.3MHz)** |

The single- and double-precision results obtained on the benchmarking system are 30.8 and 24.0 MWhet/sec respectively. Some improvements in the performance are expected with errata fixes and future release of the compilers and libraries. The projected single and double precision

Table 4. Whetstone Benchmark Results

| DP KWips | SP Kwips | System |
|---|---|---|
| 410 | 500 | VAX 11/780, 4.3BSD, f77 [MIPS 88] |
| 715 | 1,083 | VAX 11/780, LLL compiler [MIPS 88] |
| 830 | 1,250 | VAX 11/780 VAX/VMS [Intergraph 86] |
| 924 | 1,039 | Sun-3/160C, 68881 [Wilson 88] |
| 1,230 | 1,250 | Sun-3/260, 25MHz 68020, 20MHz 68881 |
| 1,581 | 1,886 | Apollo DN4000, 25MHz 68020, 25MHz 68881[Wilson 88] |
| 1,730 | 1,860 | Intel 80386+80387, 20MHz, 64K cache, Greenhills |
| 1,740 | 2,980 | Intergraph InterPro-32C 30MHzClipper[Intergraph 86] |
| 1,863 | 2,433 | Sun-3/260, 25MHz 68020, 20MHz 68881 |
| 2,092 | 3,115 | HP 9000/840S [HP 87] |
| 2,433 | 3,521 | HP 9000/825S [HP 87] |
| 2,590 | 4,170 | Intel 80386+Weitek 1167, 20MHz, Greenhill |
| 2,673 | 3,569 | Sun-3/260, Weitek FPA [Wilson 88] |
| 2,670 | 4,590 | VAX 8600, VAX/VMS [Intergraph 86] |
| 2,907 | 4,202 | HP 9000/850S [HP 87] |
| 2,940 | 4,215 | Sun-4/110 [Sun 88] |
| 3,885 | 5,663 | Sun-4/200,16.7MHz SPARC, Weitek 1164/5 [Wilson 1988] |
| 3,950 | 6,670 | VAX 8700, VAX/VMS, Pascal(?) [McInnis 87] |
| 4,000 | 6,900 | VAX 8650, VAX/VMS [Intergraph 86] |
| 4,120 | 4,930 | Alliant FX/8 (1CE) [Alliant 86] |
| 4,200 | - | Convex C-1 XP [Multiflow] |
| 4,220 | 5,430 | MIPS M/500 |
| 4,400 | 15,000 | Motorola 20MHz 88000 [RISC Mgmt 88, Simpson 88] |
| 6,600 | - | HP 835S [RISC Mgmt, 88] |
| 6,930 | 8,570 | MIPS M/800 |
| 7,960 | 10,280 | MIPS M/1000 |
| 9,100 | 11,400 | MIPS M/120-5 |
| 12,605 | - | Multiflow Trace 7/200 [Multiflow] |
| 13,600 | 17,300 | MIPS M/2000-8, 25MHz R3000/R3010 |
| 14,069 | - | CCI Power 7/64 (simulation) [Simpson 88] |
| **20,000** | **25,641** | **i860 uP @ 33.3MHz (Measured)** |
| **24,000** | **30,800** | **i860 uP @ 40MHz (Scaled from 33.3MHz)** |
| 25,000 | - | IBM 3090-200 [Multiflow] |
| 35,000 | - | Cray X-MP/12 |

vector statement is executed approximately $n^3/3 + n^2$ times where n is equal to the matrix order. Therefore, the inner loop dominates the total execution time.

Table 5. 100 x 100 Linpack Benchmark Results

| DP Fortran | DP Coded | System |
|---|---|---|
| .10 | - | Sun-3/160, 16.7MHz (Rolled BLAS) |
| .11 | - | Sun-3/260, 25MHz 68020+20MHz 68881 (Rolled BLAS) |
| .13 | .16 | DEC Micro VAX II, VAX/VMS |
| .14 | - | Appollo DN4000, 25MHz (68020+68881) [ENEWS 87] |
| .14 | - | VAX 11/780, 4.3BSD, LLL Fortran [ours] |
| .14 | .17 | VAX 11/780, VAX/VMS |
| .20 | - | 80386+80387, 20MHz, 64K cache, Greenhills |
| .29 | .49 | Intergraph IP-32C, 30Mz Clipper [Intergraph 86] |
| .38 | - | 80386 +Weitek 1167, 20MHz,64K cache, Greenhills |
| .41 | - | Sun-3/160, Weitek FPA (Rolled BLAS) |
| .41 | .45 | DEC Micro VAX 3200/3500/3600, VAX/VMS |
| .45 | .54 | HP9000 Model 840S [HP 87] |
| .46 | - | Sun-3/260, Weitek FPa (Rolled BLAS) |
| .49 | .66 | VAX 8600, VAX/VMS 4.5 |
| .49 | .54 | HP 9000/825S [HP 87] |
| .57 | .72 | HP9000 Model 850S [HP 87] |
| .60 | .72 | MIPS M/500, f77 1.21 |
| .65 | .76 | VAX 8500, VAX/VMS |
| .70 | .96 | VAX 8650, VAX/VMS |
| .78 | - | IBM 9370-90, VS FORT 1.3.0 |
| .86 | - | Sun-4/110 [Sun 88] |
| .99 | 1.2 | VAX 8550/8700/8800, VAX/VMS |
| 1.1 | - | SUN 4/200 16.7MHz SPARC (Rolled BLAS) w/ Weitek 1164/5 [SUN 87a] |
| 1.2 | 1.3 | MIPS M/800, f77 1.31 |
| 1.5 | 1.7 | ELXSI 6420 |
| 1.5 | 1.6 | MIPS M/1000, f77 1.31 |
| 1.6 | 2.0 | Alliant FX-1 (1 CE) [Alliant 86] |
| 2.1 | - | IBM 3081K H enhanced opt-3 |
| 2.1 | 2.2 | MIPS M/120-5, f77 1.31 |
| 3.0 | 3.3 | CONVEX C-1/XP, Fort 2.0 (Rolled BLAS) |
| 3.6 | 3.9 | MIPS M/2000-8 25MHz R3000/R3010 f77 1.31 |
| 3.8 | 4.0 | MIPS M/2000-8 25MHz R3000/R3010, f77 1.40 (Rolled BLAS) |
| 6.0 | - | Multiflow Trace 7/200 Fortran 1.4 (Rolled BLAS) |
| 7.6 | 11.0 | Alliant FX-8, 8 CEs, FX Fortran, v2.0.1.9 |
| 6.1 | 11.0 | i860 uP @ 33.3MHz Vector (Simulation) |
| 7.3 | 13.2 | i860 uP @ 40MHz Vector (Simulation) |
| 12 | 23 | CRAY 1S CFT (Rolled BLAS) |
| 52 | 61 | ETA10-E (1 proc, 10.5ns) |
| 56 | 60 | CRAY X-MP/4 CFT (Rolled BLAS) |

[Serlin 87]
O. Serlin, "Editor's Notebook," Supermicro, issue no. 69, July 1987.

[Serlin 86]
O. Serlin, "Mips, Dhrystones, and Other Tales," Datamation, June 1986.

[Simpson 88]
D. Simpson, "OEMS Cheer Motorola's 88000," p.83-91, Mini-Micro System, Aug. 1988.

[Sun 87]
Sun Microsystems, Sun-4 Product Introduction Material, Jul. 1987.

[Sun 87a]
Sun Microsystems, "Sun-4/200 Benchmarks," June 1987.

[Sun 88]
Sun Microsystems, "Sun-4/110 Preliminary Benchmark Results," WSD Performance Group, 1/28/88.

[Weicker 84]
R. Weicker, "Dhrystone: A Synthetic Systems Programming Benchmark," Communications of the ACM, Vol. 27, No. 10, Oct. 1984.

[Weicker 88]
R. Weicker, "Dhrystone Benchmark: Rationale for Version2 and Measurement Rules," May 17, 1988.

[Wilson 88]
D. Wilson, "The Sun 4/260 RISC-Based Technical Workstation," p91-101, UNIX Review, Jul. 1988.