Mobile Intel® Pentium® 4 Processor-M and Intel® 845MP/845MZ Chipset Platform

Design Guide

April 2002

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Revision History

Rev.	Description	Date
001	Initial Release	March 2002
002	Updates include: • Added 845MZ product information	April 2002

1. Introduction

This design guide provides Intel's design recommendations for systems based on the Mobile Intel® Pentium® 4 Processor-M and the Intel® 845MP/845MZ chipset. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processor or 845MP/845MZ chipset.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two following categories.

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

Note: The guidelines recommended in this document are based on experience and preliminary simulation work performed at Intel while developing Mobile Intel Pentium 4 Processor-M and 845MP/845MZ chipset-based systems. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics are provided in Section 13. The schematics are a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform, component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1. Related Documentation

Reference the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact the field representative for information on how to obtain Intel issued documentation.

Document	Document Number/Source
Intel® 845MP/845MZ Chipset: 82845MP/845MZ Memory Controller Hub Mobile (MCH-M) Datasheet	250687-002
Mobile Intel® Pentium® 4 Processor-M in the 478 Pin Package Datasheet	250686-002
Mobile Intel® Pentium® 4 Processor-M in the 478 Pin Package Thermal Design Guidelines	Contact your Field Representative
Mobile Intel® 845MP/845MZ Chipset Thermal and Mechanical Design Guidelines	Contact your Field Representative
Mobile Intel® Pentium® 4 Processor-M in the 478 pin package Processor Signal Integrity Models	Contact your Field Representative
Mobile Intel® Pentium® 4 Processor-M VR Down Design Guidelines	Contact your Field Representative
mPGA478 Socket Design Guidelines	249890
Intel® PC DDR-SDRAM Specification	http://developer.intel.com/technology/memory/ddr/specs/ddr_specs.htm
Accelerated Graphics Port Interface Specification Rev 2.0	http://www.agpforum.org/
Low Pin Count Interface Specification Rev 1.0	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI Local Bus Specification Rev. 2.1	www.pcisig.com
PCI-PCI Bridge Specification Rev. 1.0	www.pcisig.com
PCI Bus Power Management Interface Specification Rev. 1.0	www.pcisig.com
Universal Serial Bus 1.1 Specification	http://www.usb.org/developers/docs.html
Advanced Configuration and Power Interface Specification (ACPI) Rev. 1.0b	http://www.teleport.com/~acpi/
PC'01 Specification	www.microsoft.com
PC 99 System Design Guide, Revision 1.0	http://www.microsoft.com/hwdev/pc99.htm
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm
Intel® 82801CAM I/O Controller Hub 3 (ICH3-M) Specification Update	http://developer.intel.com/design/chipsets/datashts/290716.htm
Intel® 82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Preview Datasheet	(Order# A00358-004), available at *http://www-niooem.jf.intel.com/components.htm* and on IBL
Intel® 82562ET LAN on Motherboard Design Guide (AP-414)	Contact your Field Representative

Document	Document Number/Source
Intel® 82562ET/EM PCB Design Platform LAN Connect (AP-412)	Contact your Field Representative

1.2. Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

Table 1. Conventions and Terminology

Convention/ Terminology	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers by the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. Backward Crosstalk—coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. Forward Crosstalk—coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. Even Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Convention/ Terminology	Definition
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, and any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. Maximum and Minimum Flight Time—Flight time variations can be caused by many different variables. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions. Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is observable only in simulation.
Pin	The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin.
Processor	In this document "processor" refers to the Mobile Intel Pentium 4 Processor-M in the 478-pin package based on 0.13-micron (130 nanometer) technology.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the Mobile Intel® Pentium® 4 Processor-M. It may also be termed "system bus" in implementations where the System Bus is routed to other components. The P6 bus was the microprocessor bus of the Mobile Intel Pentium Pro processor, Mobile Intel® Pentium® II processor, and Mobile Intel® Pentium® III processors. The System Bus is not compatible with the P6 bus.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Convention/ Terminology	Definition
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal that falls below V_{SS} at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VREF Guardband	A guardband defined above and below V_{REF} to provide a more realistic model accounting for noise such as V_{TT} and V_{REF} variation.

1.3. Mobile Intel® Pentium® 4 Processor-M in 478- Pin Package

The Mobile Intel Pentium 4 Processor-M in the 478-pin package is the next generation, IA-32 processor. This processor has a number of features that significantly increase its performance from previous IA-32 generation processors. The new Intel NetBurst™ micro-architecture includes a number of new features as well as some improvements on existing features.

Intel NetBurst micro-architecture features include hyper-pipelined technology, rapid execution engine, 400-MHz system bus, and execution trace cache. Compared to previous generation processors, the hyper pipelined technology doubles the pipeline depth in the mobile Pentium 4 Processor-M in the mobile and allows the processor to reach much higher core frequencies. The rapid execution engine allows the 2 integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400-MHz system bus is a quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12-k decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

Improved features within the Intel NetBurst micro-architecture include the advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is 512, on-die level 2, cache with an increased bandwidth over previous micro-architectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. Finally, SSE2 adds 144 new instructions for double precision floating point, SIMD integer, and memory management.

The mobile Pentium 4 Processor-M in the 478-pin package supports uniprocessor configurations only. The mobile Pentium 4 Processor-M includes a Thermal monitor that allows systems to be designed for anticipated processor thermals as opposed to worst case with no performance degradation expected.

Table 2. Mobile Pentium 4 Processor-M in the 478-Pin Package Feature Set Overview

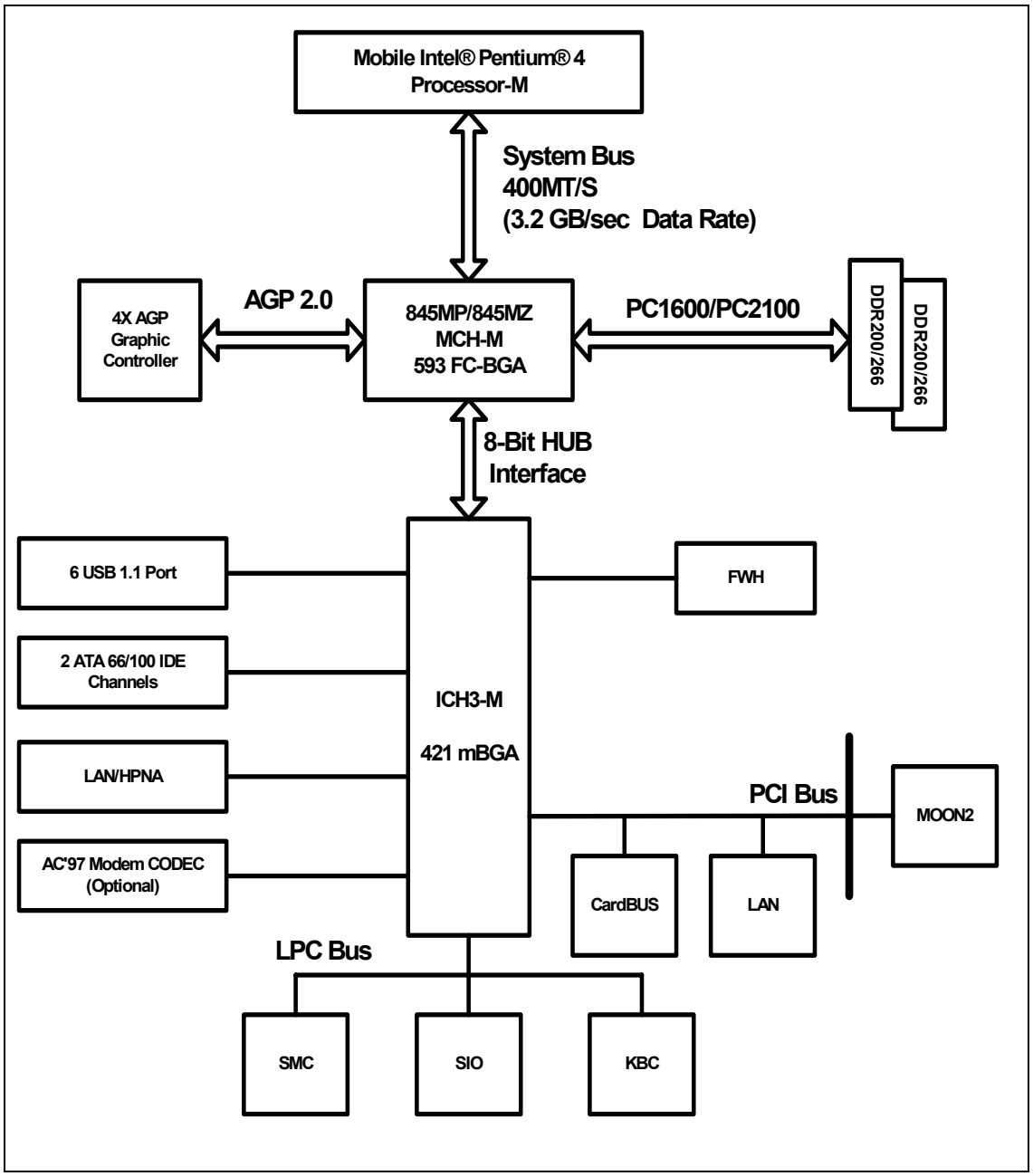
Feature	Mobile Intel Pentium 4 Processor-M in the 478 Pin Package
L1 Cache	12 KB on-die
L2 Cache	512 KB on-die
L3 Cache	None
Data Transfer Rate	3.2 GB/sec
Manageability Features	Thermal Monitor
Package Pin Configuration	478 pin, 0.050” Micro-FCPGA

1.4. Intel 845MP/845MZ Chipset

The Intel 845MP/845MZ chipset consists of the following main components: Mobile Intel Memory Controller Hub (MCH-M) and the Mobile Intel I/O Controller Hub 3 (ICH3-M). All these components are interconnected via an Intel proprietary interface called hub interface. The hub interface is designed into the Intel 845MP/845MZ chipset to provide efficient communication between components.

Additional hardware platform features include AGP 4x mode, PC2100/PC1600 DDR System memory, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN* and Universal Serial Bus 1.1. The platform is also ACPI-compliant and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN* connect, the platform supports Wake-on-LAN* for remote administration and troubleshooting.

Figure 1. Typical System Block Diagram



1.4.1. Intel Memory Controller Hub (MCH-M)

The Intel 845MP/845MZ MCH-M component provides the processor interface, DDR interface, AGP interface and hub interface in an Intel 845MP/845MZ chipset platform.

The Intel MCH-M is in a 593-ball BGA package and has the following functionality:

- Supports a single Processor with a data transfer rate of 400 MHz
- Supports DDR-SDRAM at 100/133-MHZ operation (DDR200/266)

- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5-V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability
- 8-bit, 66-MHz,, 4x hub interface to the Intel ICH3-M

1.4.1.1. Processor System Bus Support

- AGTL+ bus driver technology (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)
- Supports Uniprocessor (UP) systems
- 400 MT/s PSB support
- Optimized for Mobile Intel Pentium 4 Processor-M in 478-pin Micro-FCPGA package
- 12 deep in-order queue
- Supports in-order and dynamic deferred transactions
- Low Vtt

1.4.1.2. Integrated System Memory DRAM Controller

- Supports up to 2 SO-DIMMs
- Up to 1 GB using 64-Mb, 128-Mb, 256-Mb, 512-Mb technology
- 200/266 MHz DDR interface
- 64-bit data interface
- PC2100 and PC1600 system memory interface
- Supports x16 DDR device widths with Dynamic Powerdown Support for suspend to RAM (STR) and S3
- Supports up to 16 simultaneous open pages
- Refresh Mechanism: CAS-before-RAS only
- Support for DIMM Serial Presence Detect (SPD) scheme via SMBus interface STR power management support via self refresh mode using CKE

1.4.1.2.1. Accelerated Graphics Port (AGP) Interface

- Supports AGP 2.0 data transfers
- Supports a single AGP (4X/2X/1X) device (either via a connector or on the motherboard)
- AGP 1.5-V Connector support only
- Synchronously coupled to the host with 1:2 clock ratio
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP semantic traffic to the DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches

- AGP BUSY protocol.
- AGP Clamping and sense amp control
- Supports 32-deep AGP address queue.

1.4.1.3. Packaging/Power

- 593-pin, FC-BGA package
- 1.5 V (±5%) core and mixed 3.3 V, 1.5 V, 1.8 V, and AGTL+ I/O

1.4.1.4. I/O Controller Hub (ICH3-M)

ICH3-M provides the I/O subsystem with access to the rest of the system:

- Upstream Accelerated Hub Architecture interface at 266 MB/s for access to the MCH-M
- PCI 2.2 interface (6 PCI Req/Grant Pairs)
- Bus Master IDE controller (supports Ultra ATA 100/66/33)
- USB 1.1 Controller
- SMBus Controller
- FWH Interface
- LPC Interface
- AC'97 2.1 Interface
- Integrated System Management Controller
- Alert-On-LAN
- IRQ Controller

1.4.1.4.1. Packaging/Power

- 421 BGA
- 3.3-V core and 1.8-V and 3.3-V standby

1.4.1.5. Firmware Hub (FWH)

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPIs

1.4.1.5.1. Packaging/Power

- 32-Pin PLCC
- 3.3-V core and 3.3 V/12 V for fast programming
- Register-based locking

1.4.2. Bandwidth Summary

Table 3 lists the bandwidths of critical 845MP/845MZ chipset platform interfaces.

Table 3. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus	100	4	8	3200
AGP	66	4	4	1066
Hub Interface	66	4	1	266
PCI	33	1	4	133
DDR-SDRAM 200/266 MHz	100/133	2/2	8/8	1600/2100

2. General Design Considerations

This section documents motherboard layout and routing guidelines for Intel 845MP/845MZ platforms. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 Ω ± 15%) is the "nominal" trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace that is based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

2.1. Nominal Board Stackup

The Intel 845MP/845MZ Chipset platform requires a board stackup yielding a target impedance of 55 Ω ± 15% with a 5-mil wide external trace and a 4-mil wide internal trace width for all interfaces.

3. Processor System Bus Design Guidelines

3.1. Introduction

Intel's Mobile Pentium 4 Processor-M is the first mobile Intel processor with the Intel NetBurst micro-architecture. The Mobile Pentium 4 Processor-M utilizes Micro Flip-Chip Pin Grid Array (Micro-FCPGA) package technology, and plugs into a 478-pin, surface-mount, Zero Insertion Force (ZIF) socket, which is referred to as the mPGA478M socket. The Mobile Pentium 4 Processor-M maintains full compatibility with IA-32 software. The Mobile Pentium processor's 400-MT/s Intel NetBurst micro-architecture system bus utilizes a split-transaction, deferred reply protocol like the Mobile Intel Pentium 4 Processor-M. The following layout guidelines support designs using the Mobile Intel Pentium 4 Processor-M and the Intel 845MP/845MZ chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most PSB signals. The exception to these are RESET#, BPM[5:0]# signals which requires a 51.1 Ω ± 1% pull-up , and BR0 signal requires 220 Ω ± 5% pull-up to Vtt on the processor end of the transmission line.

3.2. Processor System Bus (PSB) Routing Guidelines

Table 4 summarizes the layout recommendations for mobile Pentium 4 Processor-M in the 478-pin package configurations and expands on specific design issues and their recommendations.

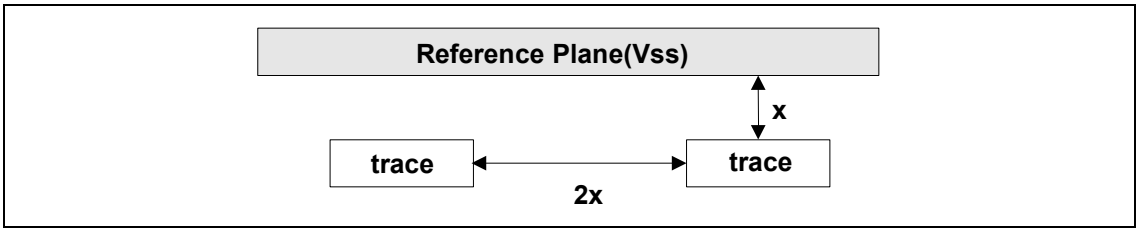
Table 4. System Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Greater than or equal to 2:1 edge-to-edge spacing versus trace to reference plane height ratio. See Figure 1 for an illustration of this recommendation.
Data Line lengths (agent to agent spacing)	1.5 inches– 10 inches from - pin to pin. Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.100 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals in the same source synchronous group should be routed on the same layer and referenced to Vss.
DSTBn/p[3:0]#	A data strobe and its complement should be routed within ±0.025 inches of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. DSTBn/p# should be routed on the same layer as their associated data group and referenced to Vss.
Address line lengths(agent to agent spacing)	1.5 inches – 10 inches from pin-to-pin address signals of the same source synchronous group should be routed to the same Pad-to-Pad length within± 0.200 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).
ADSTBn/p[1:0]#	An address strobe and its complement should be routed within ± 0.200 inches of the same Pad-to-Pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).
Common Clock line lengths	No length compensation is necessary.
Topology	Stripline
Routing priorities	All associated signals and strobes should be routed on same layer for entire length of bus. All signals should be referenced to Vss. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be Vss and the layers must all be of the same configuration (all stripline or all microstrip for example).
Clock keepout zones	A spacing requirement of 16-20 mils should be maintained around all clocks.
Trace Impedance	55 ohms ± 15%
Source Synchronous routing restriction	There are no length-matching routing restrictions between (or

Parameter	Processor Routing Guidelines
	within) either the source-synchronous data or address groups. As long as the strobe and associated line length routing guidelines are met for each group, there is no need to length-match between the groups. For example, one data group may be routed to the minimum allowable length while another data group could be routed to the maximum allowable length. Simulations have verified that the PSB will still function correctly even under this extreme condition.

Refer to the *Intel® 845MP or 845MZ Chipset Memory Controller Hub Mobile (MCH-M) Datasheet* for MCH-M package dimensions and refer to the *Intel® Mobile Pentium® 4 Processor-M in the 478 Pin Package Signal Integrity Models* for Processor package dimensions.

Figure 2. Cross-Sectional View of 2:1 Ratio



NOTE: This is the edge-to-edge trace spacing versus trace to reference plane height.

A trace spacing to height above reference plane ratio of 2 to 1 ensures a low crosstalk coefficient. All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the Processor have been created with the assumption of 2:1 trace spacing to height above reference plane ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

3.2.1. Return Path Evaluation

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs etc. Think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

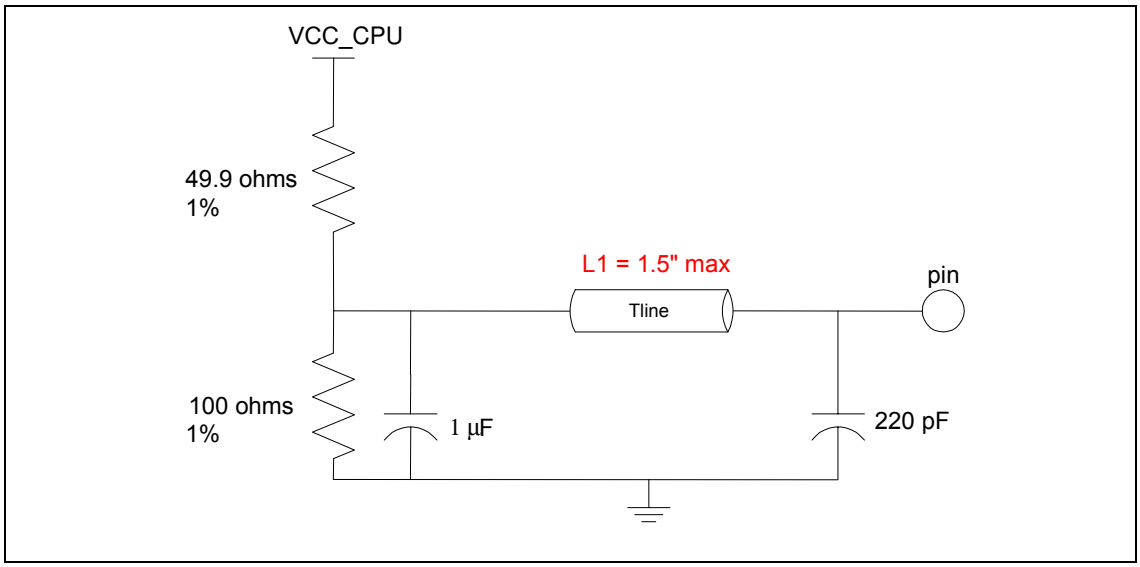
The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain Vss as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

3.2.2. GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage only needs to be supplied to one of the four pins. The other three pins can be left unconnected.

Figure 3. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1-µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin
- Decouple the pin with a high frequency capacitor (such as a 220 pF 603) as close to the pin as possible
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7-mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the system bus signals).

3.3. Processor Configuration

3.3.1. Mobile Intel Pentium 4 Processor-M in the 478 -Pin Package Configuration

This section provides more details for routing Mobile Intel Pentium 4 Processor-M based systems. For proper operation of the processor and the Intel 845MP/845MZ chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations

are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the system bus in your platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup and other parameters can be made that improve system performance.

Refer to the *Mobile Intel® Pentium® 4 Processor-M Datasheet* for a system bus signal list, signal types and definitions.

3.4. General Topology and Layout Guidelines

The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with very preliminary Intel 845MP/845MZ Chipset package models.

3.4.1. Design Recommendations

Below are the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

DATA:

Data signals of the same source synchronous group should be routed to the same **pad-to-pad** length within ± 0.100 inches of the associated strobes. As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 0.100 inches) from the **pad** of the processor to the **associated pad** of the chipset.

Equation 1. Calculation to Determine Package Delta Addition to Motherboard Length for UP Systems

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

Refer to the *Intel® 845MP or 845MZ Chipset Memory Controller Hub Mobile (MCH-M) datasheet* for MCH-M package dimensions and refer to the *Intel® Mobile Pentium® 4 Processor-M in the 478 Pin Package/ Signal Integrity Models* for package dimensions.

* Strobe package length is the average of the strobe pair.

ADDRESS:

Address signals follow the same rules as data signals except they should be routed to the same **pad-to-pad** length within ± 0.200 inches of the associated strobes. Address signals may change layers if the reference plane remains Vss.

STROBE:

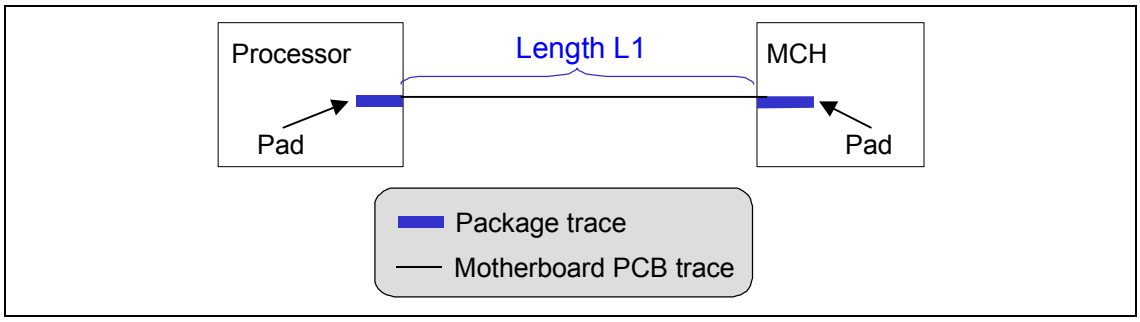
A strobe and its complement should be routed to a length equal to their corresponding data group's mean **pad-to-pad** length ± 0.025 inches

COMMON CLOCK:

Common clock signals should be routed to a minimum pin-to-pin motherboard length of **1.5** inches and a maximum motherboard length of **10.0** inches.

Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. There is no guarantee of a relationship of dielectric thickness, line width, and velocity between layers.

Figure 4. Processor Topology



3.4.2. Source Synchronous (SS) Signals

Table 5. Processor System Bus Data Signal Routing Guidelines

Signal Names		Topology	Routing Length (pin-to-pin) L1		Nominal Impedance (ohms)	Width & spacing (mils)
CPU	Intel 845MP/845MZ		Max (inches)	Min (inches)		
D[63:0]#	HD[63:0]#	Stripline	10.0	1.5	55 ±15%	4 & 8
DBI[3:0]#	DBI[3:0]	Stripline	10.0	1.5	55 ±15%	4 & 8
DSTP[3:0]#	HDSTP[3:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8
DSTBN[3:0]#	HDSTBN[3:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8

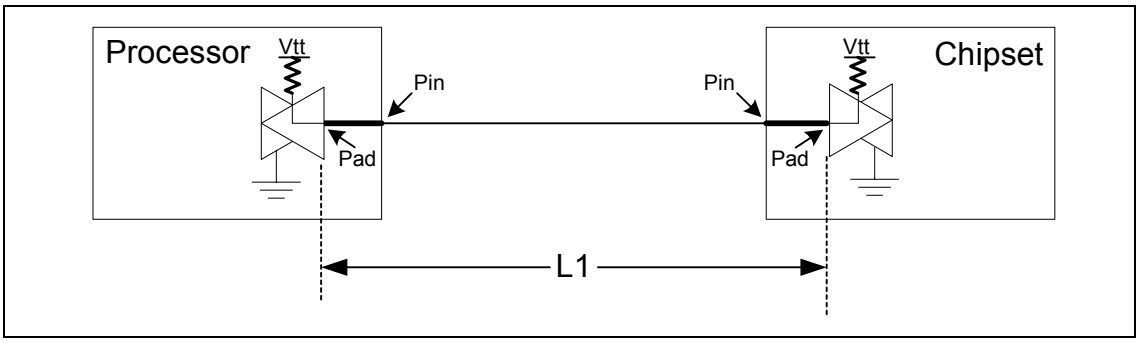
NOTE: The Data signals within each group must be routed to within ± 0.100 inches of its associated “reference” strobe. The complement strobe must be routed to within ± 0.025 inches of the associate “reference” strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

Table 6. Processor System Bus Address Signal Routing Guidelines

Signal Names		Topology	Routing Length (pin-to-pin) L1		Nominal Impedance (ohms)	Width & Spacing (mils)
CPU	Intel 845MP/845MZ		Max (inches)	Min (inches)		
A[35:3]#	HA[35:3]#	Stripline	10.0	1.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8
ADSTB[1:0]#	HADSTB[1:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8

NOTE: The Address signals within each group must be routed to within ± 0.200 of its associated strobe. . All traces within each signal group must be routed on the same layer (required). Intel recommends that the length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

Figure 5. SS Topology for Address and Data



3.4.3. Common Clock (CC) AGTL+ Signals

Table 7. Processor System Bus Control Signal Routing Guidelines

Signal Names		Topology	Routing Trace Length (Pin-to-Pin)		Nominal Board Impedance (ohms)	Width & spacing (mils)
CPU	Intel 845MP/845MZ		Max (inches)	Min (inches)		
RESET#	CPURST#	Stripline	10.0	1.5	55 ± 15%	4 & 8
BR0#	BR0#	Stripline	10.0	1.5	55 ± 15%	4 & 8
BNR#	BNR#	Stripline	10.0	1.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8
BPRI#	BPRI#	Stripline	10.0	1.5	55 ± 15%	4 & 8
DEFER#	DEFER#	Stripline	10.0	1.5	55 ± 15%	4 & 8
LOCK#	HLOCK#	Stripline	10.0	1.5	55 ± 15%	4 & 8
TRDY#	HTRDY#	Stripline	10.0	1.5	55 ± 15%	4 & 8
DRDY#	DRDY#	Stripline	10.0	1.5	55 ± 15%	4 & 8
ADS#	ADS#	Stripline	10.0	1.5	55 ± 15%	4 & 8
DBSY#	DBSY#	Stripline	10.0	1.5	55 ± 15%	4 & 8
HIT#	HIT#	Stripline	10.0	1.5	55 ± 15%	4 & 8
HITM#	HITM#	Stripline	10.0	1.5	55 ± 15%	4 & 8
RS[2:0]#	RS[2:0]#	Stripline	10.0	1.5	55 ± 15%	4 & 8

NOTE: Trace width of 4 mils and trace spacing of 8 mils within signal groups. Entire trace for each signal routed on one layer (recommended) RESET# and BR0# are CC AGTL+ signals without ODT (On die termination). For these signals Rtt should be placed near CPU: L2<= 0.5 inches. Rtt = 51.1 ±1%. Routing these signals to 4.0 inches ± 0.5 inches should maximize the setup and hold margin parameters while adhering to expected mobile solution design constraints.

3.4.3.1. CC Topology with ODT

ODT Compensation Resistors:

Pentium 4: R_comp = 51.1 ± 1% ohms (Pins L24 and P1 – Pulled to ground through resistor)

Intel 845MP/845MZ: R_comp = 24.9 ± 1% ohms (Pins AC2 and AC13 - Pulled to ground through resistor)

Figure 6. CC Topology With ODT

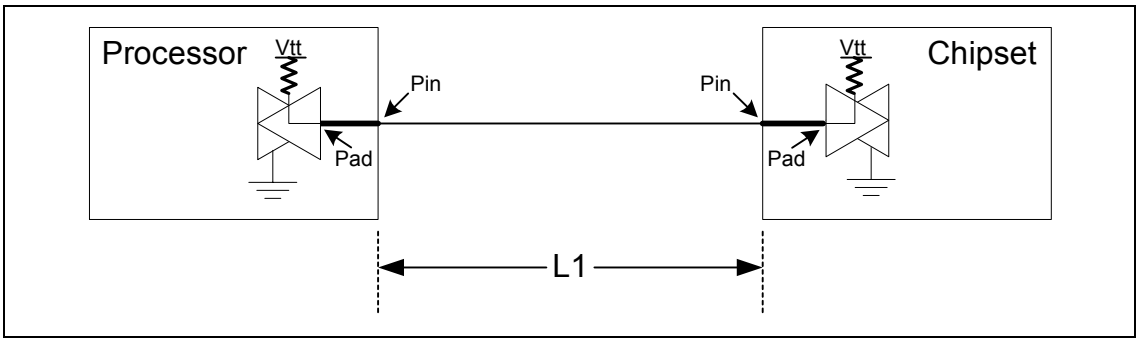
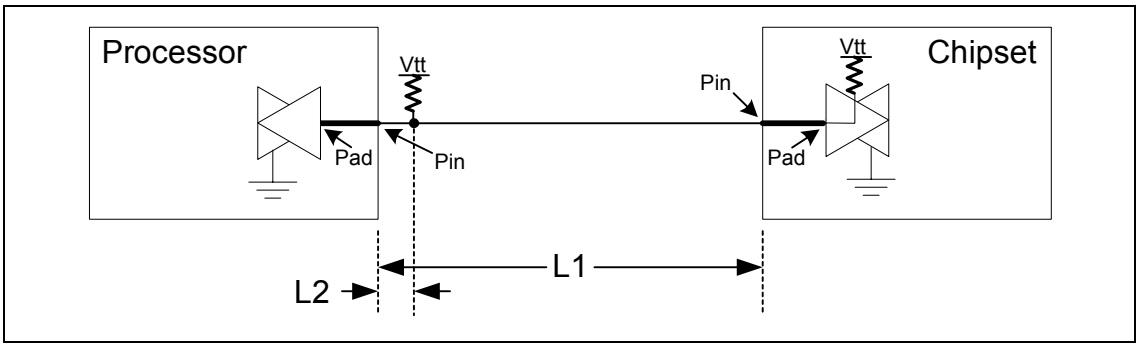


Figure 7. CC Topology Without ODT



3.4.4. PWRGOOD and Asynchronous AGTL+ Signals

Table 8. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU IO Type	Output	Output Buffer Type	Output Power Well	Input	Input Power Well
FERR#	Floating point error	1	O	CPU	OD AGTL+	N/A	ICH3-M	Main I/O (3.3V)
IERR#	Internal error	1	O	CPU	OD AGTL+	N/A	System Receiver	Vcc_Receiver
PROCHOT#	Thermal sensor	1	O	CPU	OD AGTL+	N/A	System Receiver	Vcc_Receiver
THRMTRIP#	Thermal sensor	1	O	CPU	OD AGTL+	N/A	System Receiver	Vcc_Receiver
LINT1/INTR	Local interrupts	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
LINT0/NMI	Local interrupts	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
DPSLP#	Deep sleep	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
SLP#	Sleep	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
STPCLK#	Processor stop clock	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
IGNNE#	Ignore next numeric error	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
SMI#	System management interrupt	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
A20M#	Address 20 mask	2	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU	N/A
INIT#	Processor initialize	2B	I	ICH3-M	CMOS	CPU I/O (VCC_CPU)	CPU, FWH	N/A, 3.3 V
CPUPREF#	GHI#	2	1	ICH3-M	OD CMOS	N/A	CPU	N/A
PWRGOOD	System power good	2A	I	ICH3-M	OD CMOS	N/A	CPU	N/A

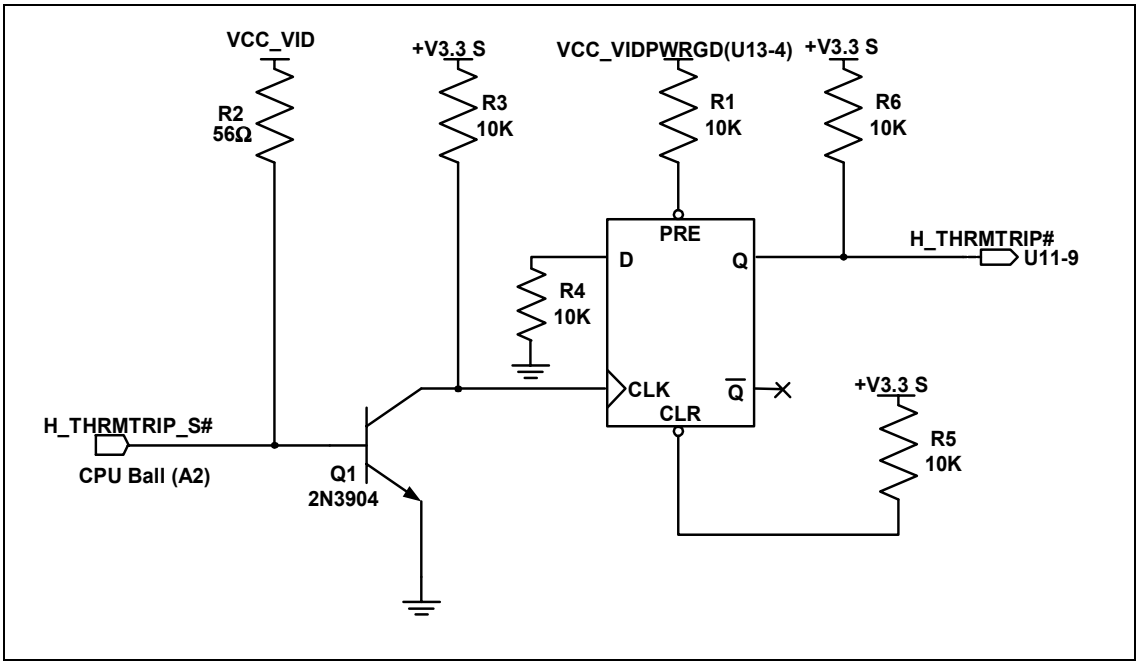
All signals must meet the AC and DC specifications as documented in the *Mobile Intel® Pentium® Processor-M Datasheet*. In addition, several design guidelines should be implemented when designing your platform with these signals. They are:

- Although the asynchronous signals are not high frequency in nature, they nevertheless need to be protected from crosstalk and other sources of noise in the same fashion as the common-clock and source-synchronous signals. Therefore, the same line-to-line spacing ratio of 2:1. Figure 2 need also apply.
- Due to the long trace lengths usually associated with these signals, Intel recommends that no electrical stubs exist and that probing be done at the via nearest to the receiver in order to maintain signal integrity. These signals should also remain ground-referenced the entire length of the trace.
- If probing is required, active FET probes are recommended as they have a much lower effective capacitance than passive probes. This, again, is to maintain proper signal integrity and to prevent any outside influences that may detrimentally affect the system.
- On critical signals, such as DPSLP#, which is used for internal clock control, it may be desirable to implement additional precautions, such as ground shielding traces or wider keepout zones in order to assure proper functionality.

3.4.4.1. CPU THRMTRIP# Circuit Recommendation

The following sections describe the topologies and layout recommendations for the miscellaneous signals. In the Figure 8 the circuit effectively latches the low state of THRMTRIP# via the D Flip-Flop once the processor has driven THRMTRIP# to a low state. Operation can be restored if the system power is cycled (power off/on system). R6 is included if the designer wishes to disable THRMTRIP# and remove R2, R3, Q1, R4, U1, R1, and R5 and can be included as a no-stuff. Please refer to customer reference board schematics in Section 13 for all referenced connections.

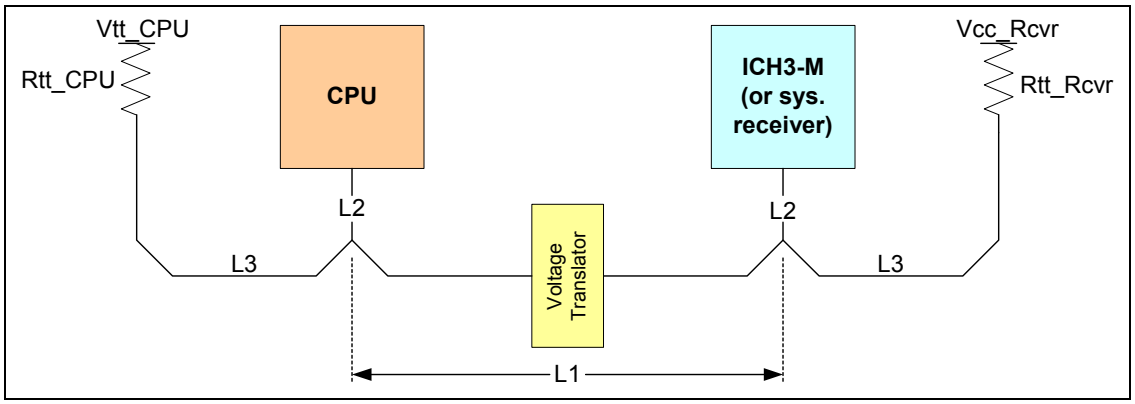
Figure 8. THRMTRIP# Circuit Recommendation



3.4.4.1.1. Topology #1: Asynchronous AGTL+ Signals Driven by the Processor; FERR#, IERR#, PROCHOT# and THRMTRIP#

These signals should adhere to the following routing and layout recommendations. Figure 9 illustrates the recommended topology. If THRMTRIP# and PROCHOT# are routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Figure 9. Routing Illustration for FERR#, IERR#, PROCHOT#, and THRMTRIP#



Note: If the design is not using the recommended THRMTRIP# latch circuit in Figure 9, THRMTRIP# can be routed through a Voltage Translator to a system logic that can provide the equivalent latching function.

Table 9. Layout Recommendations for Miscellaneous Signals – Topology 1

L1	L2	L3	Rtt
1.5" - 14.0"	1.1" max	3.0" max	Rtt_CPU = 56 ohms ± 5%
			Rtt_Rcvr = 300 ohms ± 5%

3.4.4.1.2. Topology #2, #2A: PWRGOOD and Asynchronous AGTL+ Signals Driven by ICH3-M

Top. #2 signals: LINT1/INTR, LINT0/NMI, CPUPERF#, DPSLP#, SLP#, STPCLK#, IGNNE#, SMI# and A20M#.

Top. #2A signal: PWRGOOD.

These signals should adhere to the following routing and layout recommendations. Figure 10 illustrates the recommended topology.

Figure 10. Routing Illustration for LINT1/INTR, LINT0/NMI, DPSLP#, SLP#, STPCLK#, IGNNE#, SMI# and A20M#, CPUPERF#, and PWRGOOD- Topology 2, 2A

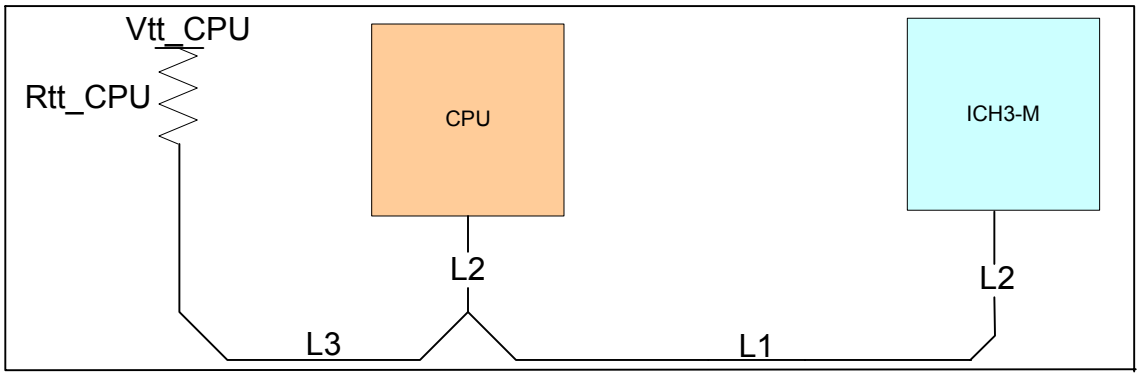


Table 10. Layout Recommendations for Miscellaneous Signals – Topology 2, 2A

L1	L2	L3	Rtt
1.5" - 14.0"	1.1" max	3.0" max	Rtt_#2 = 200 ohms ± 5%
			Rtt_#2A = 300 ohms ± 5%

3.4.4.1.3. Topology #2B: PWRGOOD and Asynchronous AGTL+ Signals Driven by ICH3-M to Both CPU and FWH; INIT#

These signals should adhere to the following routing and layout recommendations. Figure 11 illustrates the recommended topology.

Figure 11. Routing Illustration INIT#

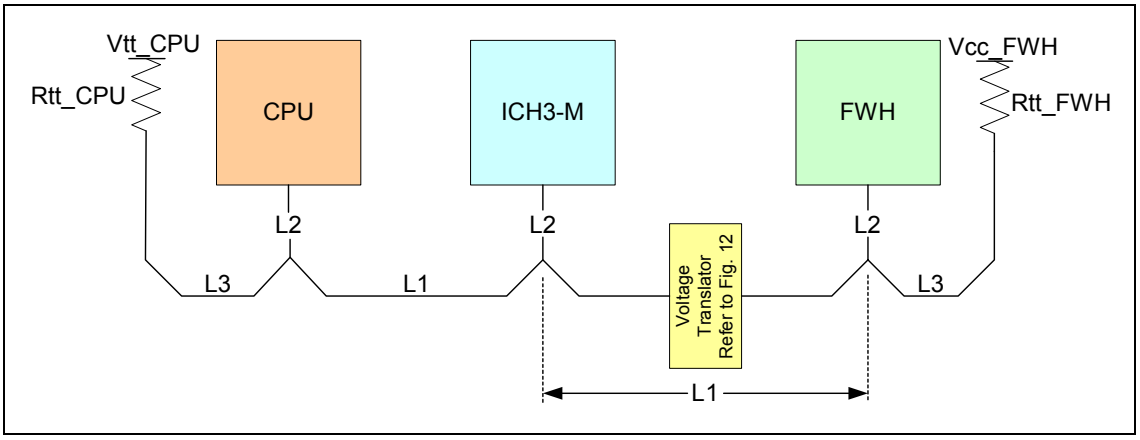


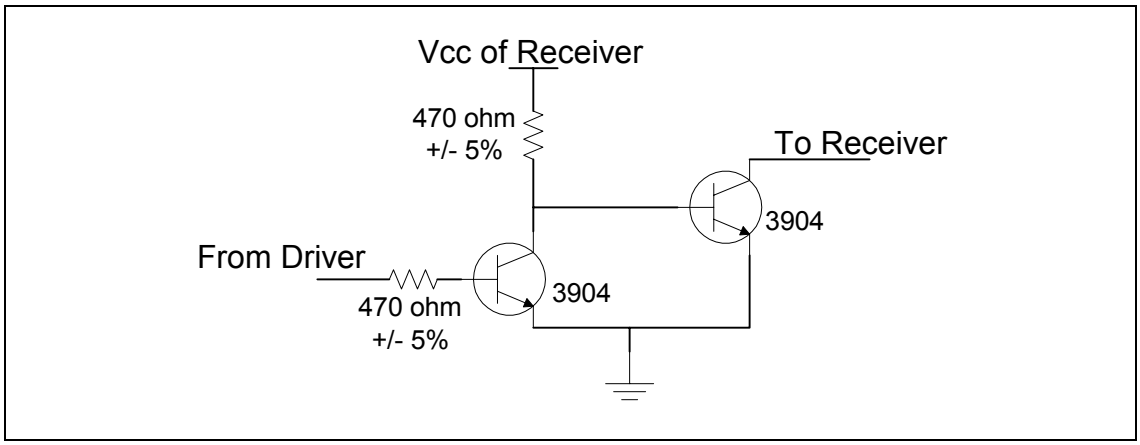
Table 11. Layout Recommendations for Miscellaneous Signals – Topology 2B

L1	L2	L3	Rtt
1.5" - 14.0"	1.1" max	3.0" max	Rtt_CPU = 200 Ω ± 5%
			Rtt_FWH= 300 Ω ± 5%

3.4.4.2. Voltage Translator Circuit

This recommended Voltage translator circuit should be applied to topologies #1 and #2B shown in Section 3.4.4.1.1 and 3.4.4.1.3.

Figure 12. Voltage Translator Circuit of Topology#1 and #2B



3.5. ITP Debug Port

Note: The Debug Port design information has been moved! This includes all information necessary to develop a Debug Port on this platform, including electrical specifications, mechanical requirements, and all In-Target Probe (ITP) signal layout guidelines. Please reference the *Intel® Pentium® 4 Debug Port Design Guide* and the *ITP700 Debug Port Design Guide*, which can be found on http://developer.intel.com/design/Xeon/guides/249679.htm, for the design of your platform. Refer to the *ITP700 Debug Port Design Guide* for further information Debug Tools Specifications.

3.5.1.1. Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Mobile Intel Pentium 4 Processor-M system. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Mobile Pentium 4 Processor-M system, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Mobile Pentium 4 Processor-M that use LAI: mechanical and electrical.

3.5.1.1.1. Mechanical Considerations

The LAI is installed between the processor socket and the Mobile Pentium 4 processor. The LAI pins plug into the socket, while the Mobile Pentium 4 Processor-M in the 478-pin package plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Mobile Pentium 4 Processor-M and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space

normally occupied by the Mobile Pentium 4 Processor-M heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

3.5.1.1.2. Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

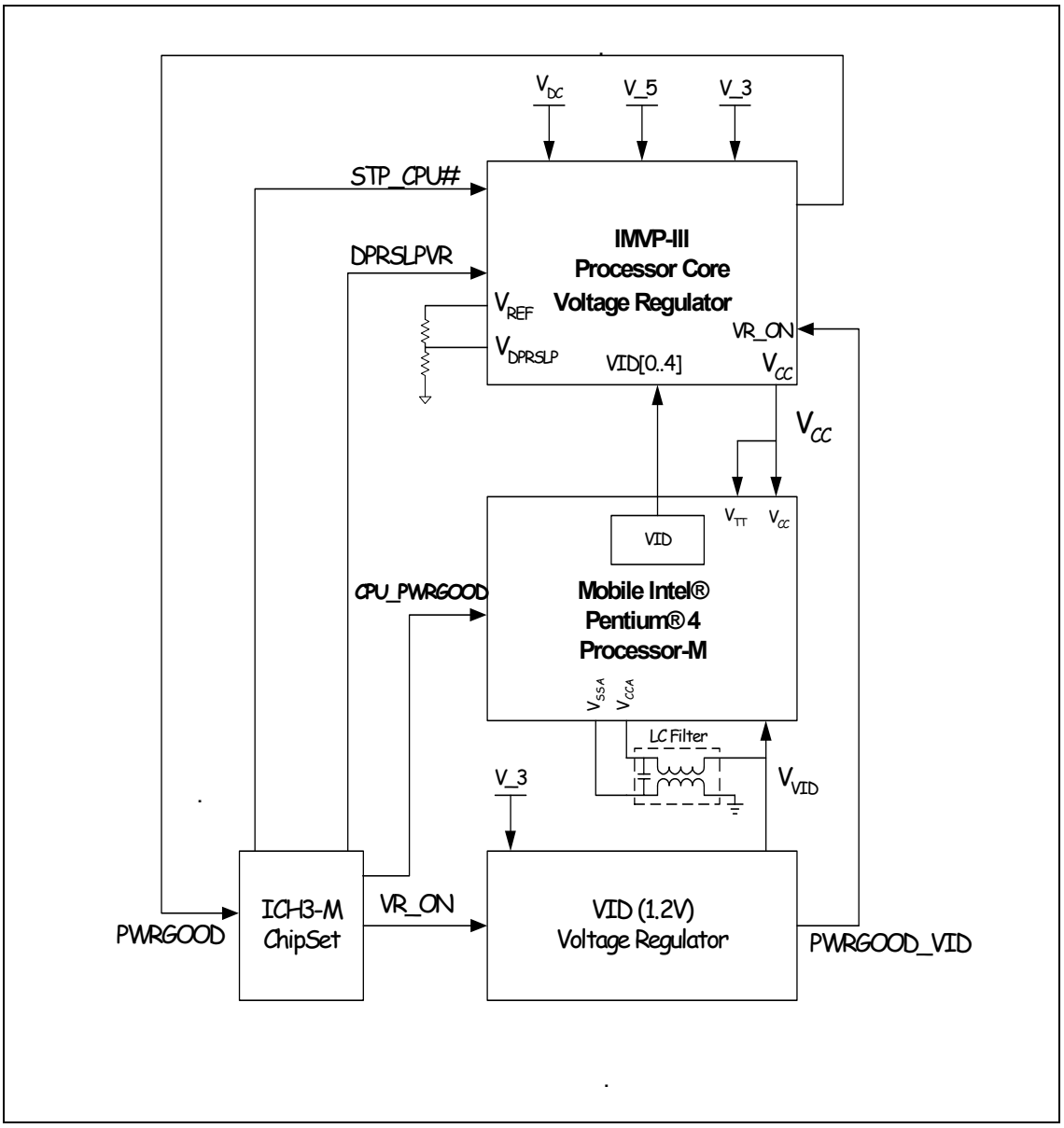
4. Processor Power Requirements

4.1. General Description

The *IMVP-III Design Guide* defines the electrical requirements for the DC-to-DC Voltage Regulator for the Mobile Pentium 4 Processor-M that features Intel SpeedStep® technology in a Micro-FCPGA package. Please contact your Field Representative for more information.

4.2. Power Delivery Architectural Block Diagram

Figure 13. Voltage Regulator Block Diagram



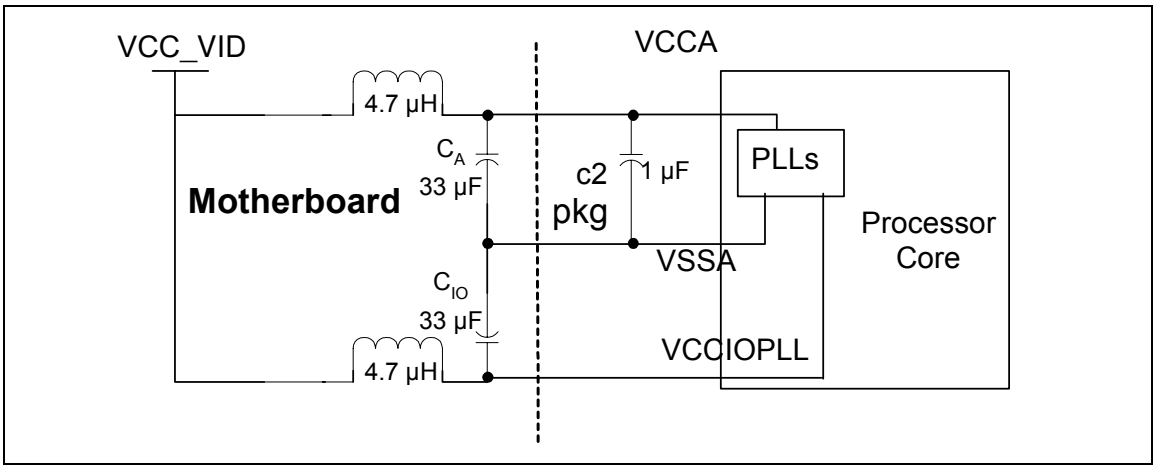
4.3. Processor Phase Lock Loop Design Guidelines

4.3.1. Filter Specifications for VCCA, VCCIOPLL, and VSSA

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low pass filtered from VCC_VID. The

general desired filter topology is shown in Figure 14. Not shown in the core is parasitic routing and excluded from the external circuitry are parasitics associated with each component.

Figure 14. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity this document will address the recommendation for the V_{CCA} filter design. The same characteristics and design approach is applicable for the $V_{CCIOPLL}$ filter design.

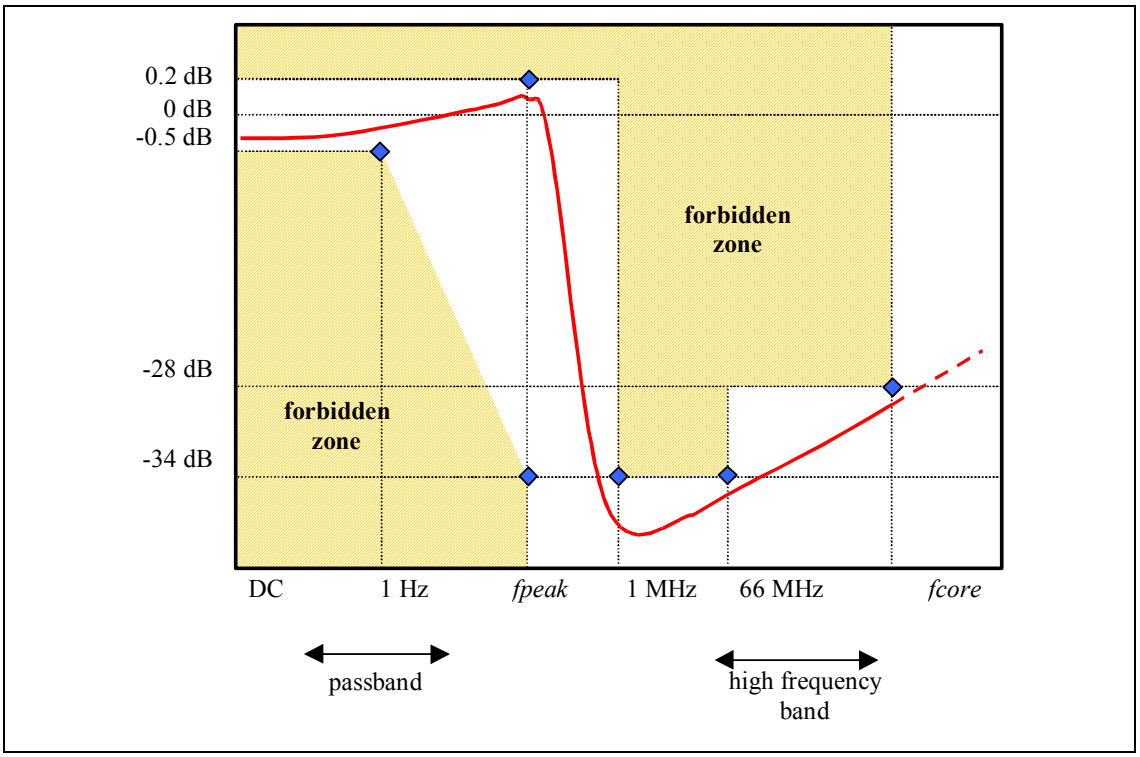
Note: The 1-µF package capacitor in Figure 14 does not exist on the Mobile Intel Pentium 4 Processor-M in the 478-pin package. It is present for the Mobile Intel Pentium 4 Processor-M only.

The AC low-pass recommendation, with input at VCC_VID and output measured across the capacitor (C_A or C_{IO} in Figure 14), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in Figure 15.

Figure 15. Filter Recommendation



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore* (core frequency).
3. *fpeak*, if existent, should be less than 0.05 MHz.

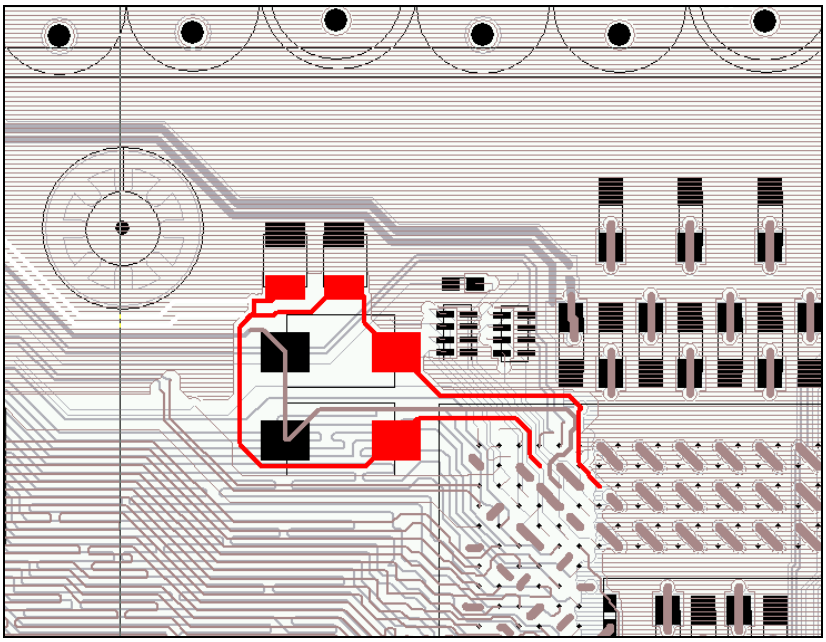
Other recommendations:

- Capacitors for the filter can be any value between 22 µF and 100 µF as long components with ESL ≤ 5 nH and ESR < 0.3 Ω are used.
- Values of either 4.7 µH or 10 µH may be used for the inductor.
- Use shielded type inductors to minimize magnetic pickup
- Filter should support DC current > 60 mA
- DC voltage drop from VCC_CPU to VCCA should be < 60 mV
- In order to maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_VID to the processor socket should be a maximum of 1 µ.

Other routing requirements:

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 16
- VCCA route should be parallel and next to VSSA route (minimize loop area)
- A minimum of a 12-mil trace should be used to route from the filter to the processor pins.
- L should be close to C

Figure 16. Example Component Placement for PLL Filter



4.4. Voltage and Current

A mobile processor core regulator supplies the required voltage and current to a single processor. Refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* (contact your Field Representative) for the load line specification and implementation features.

4.4.1. Voltage Identification

Refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* (contact your Field Representative) for the load line specification and implementation features.

4.4.2. V_{CC} Power Sequencing

4.4.2.1. Core Converter Soft Start Timer

The main purpose of a soft start timer is to control the ramp-up time of the core voltage in order to reduce the initial in-rush current on the supply input voltage (battery) rail. The soft start circuit must not allow the V_{CC} power plane voltage to rise too fast.

4.4.2.2. Power On/Off Sequencing

For more information please refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* for the actual specifications (contact your Field Representative).

Figure 17. Power On Sequencing Diagram

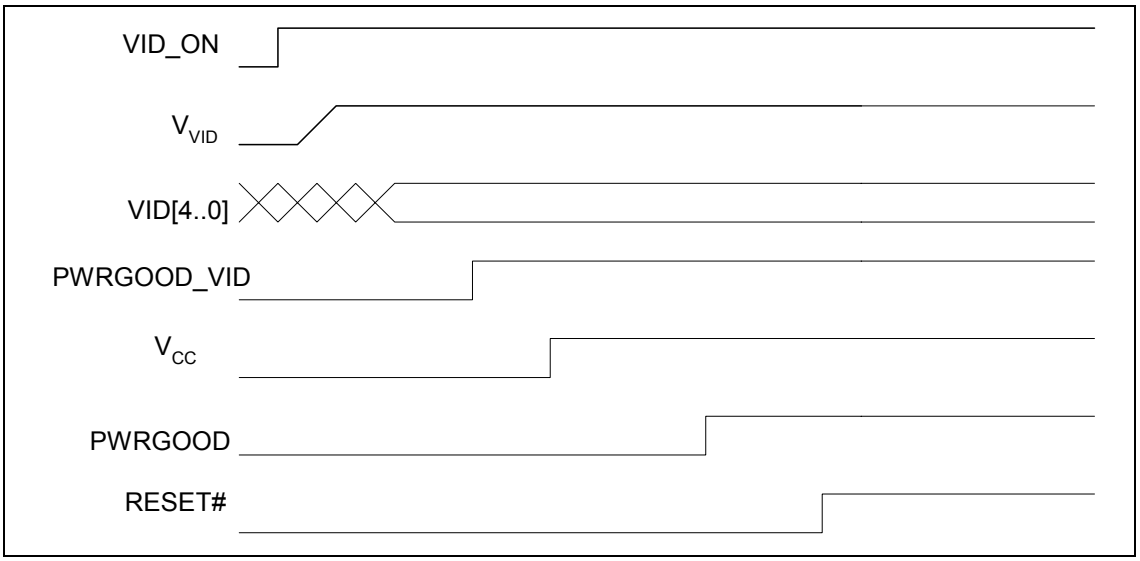
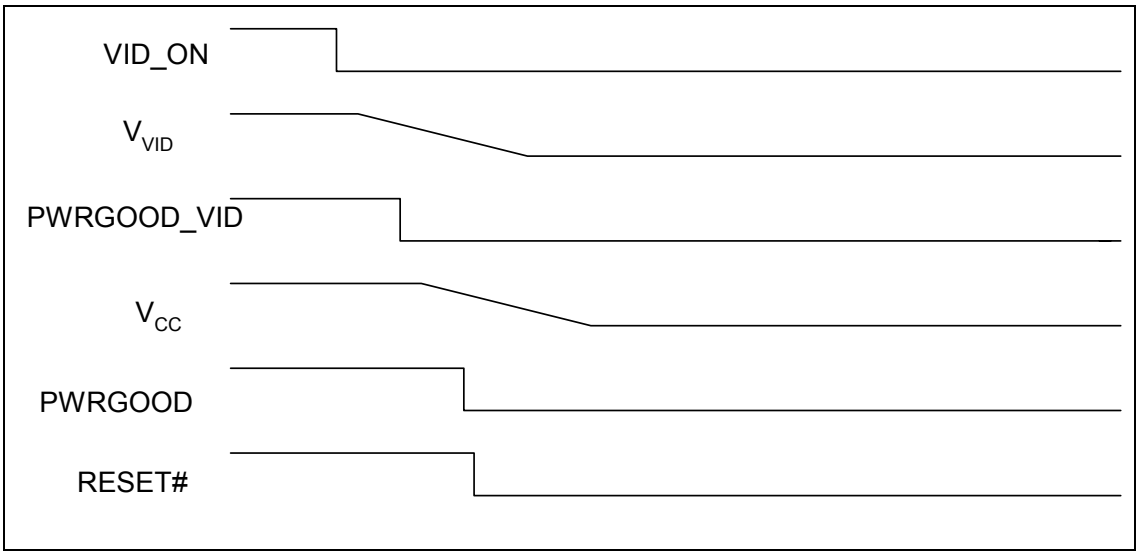


Figure 18. Power Off Sequencing Diagram



4.5. Voltage Regulator Design Recommendations

For more information please refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* for the actual specifications (contact your Field Representative). The following section describes some guidelines for the design of the voltage regulator in terms of design topology and component selection. This is done to ensure design and component compatibility.

4.6. Processor Decoupling Recommendation

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerance at the processor socket pins. To meet the transient

response of the processor, it is necessary to properly place bulk and high frequency capacitors close to the processor power and ground pins.

4.6.1. Transient Response

The inductance of the motherboard power planes slows the voltage regulator's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more stray inductance is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, areas closer to the load have less room for capacitor placement. Therefore, tradeoffs must be made.

The processor causes very large switching transients. These sharp surges of current occur at the transition between low power states and the normal operating states. It is the responsibility of the system designer to provide adequate high frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage capacitors supply current during longer lasting changes in current demand.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can respond. A typical voltage converter has a reaction time on the order of 1 to 100 µs while the processor's current steps are on the order of 30 to 40 ns. High Frequency decoupling is typically done with ceramic capacitors with a very low ESR. Because of there low ESR, these capacitors can act very quickly to supply current at the beginning of a transient event. However, because the ceramic capacitors are small, i.e. they can only store a small amount of charge, Bulk capacitors are needed too. Bulk capacitors are typically polarized with high capacitance values and unfortunately higher ESRs. The higher ESR of the Bulk capacitor limits how quickly it can respond to a transient event. The Bulk and HF capacitors working together can supply the charge needed to stay in regulator before the regulator can react during a transient.

A load change transient occurs when coming out of or entering a low power state. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the processor enters different power modes by stopping and starting it's internal clock. The processor current requirements can change by as much as 70% (±10%) of the maximum current very quickly.

4.6.2. Processor Voltage Plane

Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone. Intel recommends that all layers of the stack-up be used for processor power and ground routing.

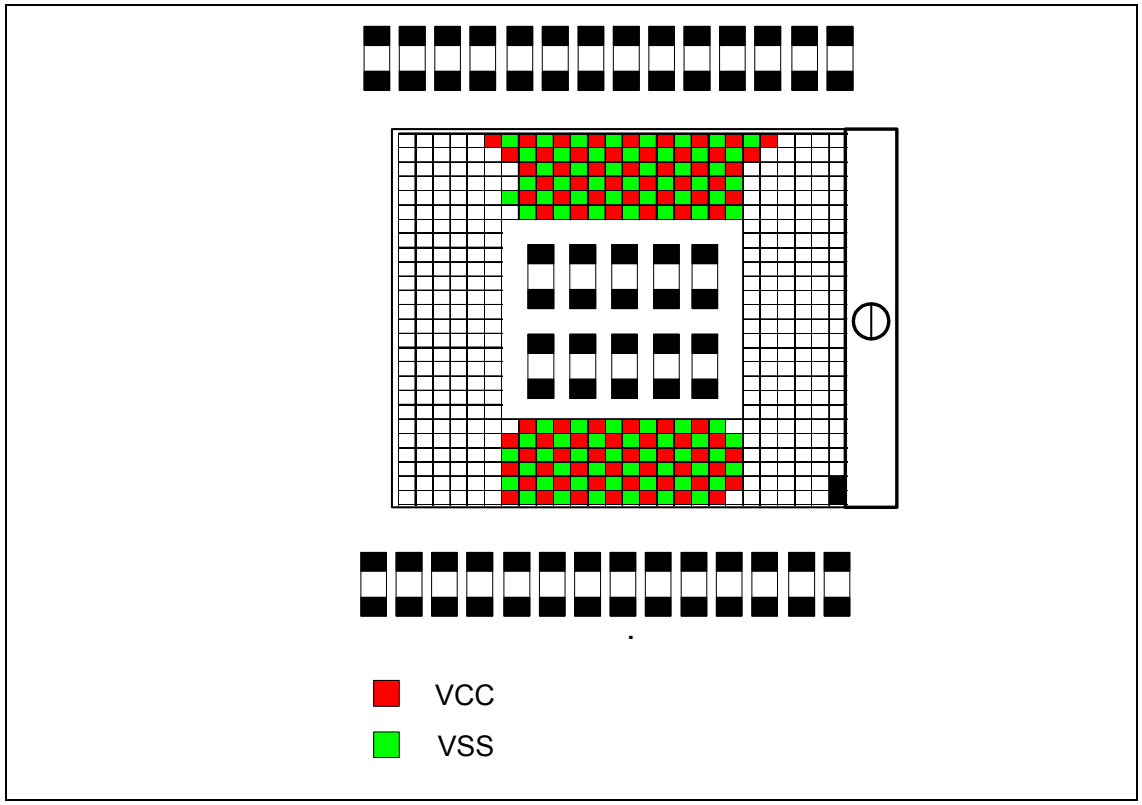
Due to the fact that the processor voltage is unique to most system designs, a voltage island is the most cost-effective means of distributing power to the processor. This island from the source of power to the load should not have any breaks so as to minimize inductance in the plane. It should also completely surround all of the pins of the source and all of the pins in the power pin area of the processor.

The bulk capacitors and the high frequency capacitors should be placed as close to the processor as possible and in the path of current flow. The processor socket has 478 pins with 50-mil pitch. The routing of these signals, power, and ground pins will require many vias. These vias cause a "Swiss Cheese" effect in the power and ground planes beneath the processor resulting in increased inductance and resistance of these planes. This increase in impedance can choke off the high current carrying channel of the voltage regulator. In order to provide the best path through the via field, it is recommended that vias are shared for every two processor ground pins.

4.6.3. High Frequency Decoupling

System motherboards should include high frequency decoupling capacitors as close to the socket power and ground pins as possible. A total of thirty-eight 10.0-µF, X5R/X7R, 1206 package, ceramic capacitors are recommended to provided high frequency decoupling for the processor. Ten of these 1206 capacitors should be placed in the socket cavity area. Fourteen of these 1206 capacitors should be placed on the north side of the cavity and fourteen of these 1206 capacitors should be placed on the south side of the cavity. See Figure 19 for an example on placement of the high frequency decoupling capacitors.

Figure 19. Processor High Frequency Decoupling Placement Example



4.6.4. Bulk Decoupling

System motherboards should include bulk-decoupling capacitors as close to the processor socket power and ground pins as possible (<1.0 inch). The maximum Equivalent Series Resistance (ESR) should be equal to or less than 2.5 mΩ.

4.7. Thermal Power Dissipation

Power dissipation has traditionally been a thermal/mechanical challenge for mobile system designers. The amount of current required from the processor power delivery circuit and the heat generated by processors has increased as processor frequencies go up and the silicon process geometry shrinks. The package of any integrated device can only dissipate so much heat into the surrounding environment. The temperature of a device, such as a processor power delivery circuit-switching transistor, is a balance of

heat being generated by the device and its ability to shed heat either through radiation into the surrounding air or by conduction into the circuit board. Increased power will effectively raise the temperature of the processor power delivery circuit's. Switching transistor die temperatures can exceed the recommended operating value if the heat cannot be removed from the package effectively.

As the current demands for higher frequency and performance processors increase, the amount of power dissipated, *i.e.*, heat generated, in the processor power delivery circuit is becoming of concern for mobile system. The high input voltage, low duty factor inherent in mobile power supply designs leads to increasing power dissipation losses in the output stage of the traditional buck regulator topology that is used in the mobile industry today.

These losses can be attributed to three main areas of the processor power delivery circuit: the switching MOSFET dissipates a significant amount of power during switching of the top control MOSFET; power dissipation resulting from drain to source resistance ($R_{DS(ON)}$) DC losses across the bottom synchronous MOSFET; and the power dissipation generated through the magnetic core and windings of the main power inductor.

There has been significant improvement in the switching MOSFET technology to lower gate charge of the control MOSFET allowing them to switch faster thus reducing switching losses. Improvements in lowering the $R_{DS(ON)}$ parametric of the synchronous MOSFET have resulted in reduced DC losses. The Direct Current Resistance (DCR) of the power inductor has been reduced, as well, to lower the amount of power dissipation in the circuit's magnetic.

These technology improvements by themselves are not sufficient to effectively remove the heat generated during the high current demand and tighter voltage regulation required by today's mobile processors. There are several mechanisms for effectively removing heat from the package of these integrated devices. Some of the most common methods are listed below.

- Attaching a heat spreader or heat pipe to the package with a low thermal co-efficient bonding material
- Adding and/or increasing the copper fill area attached to high current carrying leads
- Adding or re-directing air flow to flow across the device
- Utilize multiple devices in parallel, as allowed, to reduce package power dissipation
- Utilizing newer/enhanced technology and devices to lower heat generation but with equal or better performance

For the mobile designer, these options are not always available or economically feasible. The most effective method of thermal spreading and heat removal, from these devices, is to generate airflow across the package AND add copper fill area to the current carrying leads of the package.

The processor power delivery topology can also be modified to improve the thermal spreading characteristic of the circuit and dramatically reduce the power dissipation requirements of the switching MOSFET and inductor. This topology referred to as multi-phase, provides an output stage of the processor regulator consisting of several smaller buck inductor phases that are summed together at the processor. Each phase can be designed to handle and source a much smaller current. This can reduce the size, quantity, and rating of the components needed in the design. This can also decrease the cost and PCB area needed for the total solution. The implementation options for this topology are discussed in the next section.

4.8. Voltage Regulator Topology

For more information please refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* for the actual specifications (contact your Field Representative).

4.9. Voltage Regulator Layout Recommendations

For more information please refer to the *IMVP-III Mobile Processor Core Voltage Regulator Specification Design Guide* for the actual specifications (contact your Field Representative).

Table 12. Intel Mobile Pentium 4 Processor-M and Intel 845MP/845MZ Chipset Package Lengths

Processor lengths			MCH-M Lengths		
Signal	**Processor ball**	**Length (inches)**	**Signal**	**MCH-M ball**	**Length (inches)**
Address Group 0					
ADSTB#[0]	L5	0.219	HADSTB0#	R5	0.530
A#[03]	K2	0.392	HA03#	T4	0.518
A#[04]	K4	0.281	HA04#	T5	0.434
A#[05]	L6	0.170	HA05#	T3	0.728
A#[06]	K1	0.435	HA06#	U3	0.577
A#[07]	L3	0.330	HA07#	R3	0.551
A#[08]	M6	0.157	HA08#	P7	0.359
A#[09]	L2	0.374	HA09#	R2	0.643
A#[10]	M3	0.328	HA10#	P4	0.533
A#[11]	M4	0.261	HA11#	R6	0.397
A#[12]	N1	0.406	HA12#	P5	0.463
A#[13]	M1	0.420	HA13#	P3	0.576
A#[14]	N2	0.362	HA14#	N2	0.660
A#[15]	N4	0.252	HA15#	N7	0.407
A#[16]	N5	0.204	HA16#	N3	0.570
REQ#[0]	J1	0.447	HREQ0#	U6	0.402
REQ#[1]	K5	0.232	HREQ1#	T7	0.350
REQ#[2]	J4	0.294	HREQ2#	R7	0.393
REQ#[3]	J3	0.357	HREQ3#	U5	0.475
REQ#[4]	H3	0.360	HREQ4#	U2	0.599
Address Group 1					
ADSTB#[1]	R5	0.220	HADSTB1#	N6	0.438
A#[17]	T1	0.477	HA17#	K4	0.550
A#[18]	R2	0.399	HA18#	M4	0.580
A#[19]	P3	0.316	HA19#	M3	0.648
A#[20]	P4	0.257	HA20#	L3	0.604
A#[21]	R3	0.333	HA21#	L5	0.521
A#[22]	T2	0.394	HA22#	K3	0.624
A#[23]	U1	0.470	HA23#	J2	0.685
A#[24]	P6	0.160	HA24#	M5	0.509
A#[25]	U3	0.399	HA25#	J3	0.636
A#[26]	T4	0.294	HA26#	L2	0.648

Processor lengths			MCH-M Lengths		
Signal	**Processor ball**	**Length (inches)**	**Signal**	**MCH-M ball**	**Length (inches)**
A#[27]	V2	0.423	HA27#	H4	0.634
A#[28]	R6	0.177	HA28#	N5	0.472
A#[29]	W1	0.491	HA29#	G2	0.792
A#[30]	T5	0.232	HA30#	M6	0.449
A#[31]	U4	0.293	HA31#	L7	0.365
Data Group 0					
DSTBN#[0]	E22	0.465	HDSTBN0#	AD4	0.759
DSTBP#[0]	F21	0.362	HDSTBP0#	AD3	0.801
D#[00]	B21	0.434	HD00#	AA2	0.649
D#[01]	B22	0.494	HD01#	AB5	0.564
D#[02]	A23	0.559	HD02#	AA5	0.531
D#[03]	A25	0.634	HD03#	AB3	0.678
D#[04]	C21	0.407	HD04#	AB4	0.628
D#[05]	D22	0.411	HD05#	AC5	0.635
D#[06]	B24	0.565	HD06#	AA3	0.623
D#[07]	C23	0.495	HD07#	AA6	0.468
D#[08]	C24	0.537	HD08#	AE3	0.802
D#[09]	B25	0.612	HD09#	AB7	0.495
D#[10]	G22	0.298	HD10#	AD7	0.609
D#[11]	H21	0.231	HD11#	AC7	0.548
D#[12]	C26	0.616	HD12#	AC6	0.579
D#[13]	D23	0.485	HD13#	AC3	0.709
D#[14]	J21	0.209	HD14#	AC8	0.590
D#[15]	D25	0.572	HD15#	AE2	0.856
DBI#[0]	E21	0.309	DBI0#	AD5	0.637
Data Group 1					
DSTBN#[1]	K22	0.312	HDSTBN1#	AE6	0.693
DSTBP#[1]	J23	0.313	HDSTBP1#	AE7	0.638
D#[16]	H22	0.281	HD16#	AG5	0.845
D#[17]	E24	0.481	HD17#	AG2	0.904
D#[18]	G23	0.365	HD18#	AE8	0.663
D#[19]	F23	0.428	HD19#	AF6	0.759
D#[20]	F24	0.449	HD20#	AH2	0.965
D#[21]	E25	0.521	HD21#	AF3	0.798

Processor lengths			MCH-M Lengths		
Signal	**Processor ball**	**Length (inches)**	**Signal**	**MCH-M ball**	**Length (inches)**
D#[22]	F26	0.521	HD22#	AG3	0.898
D#[23]	D26	0.605	HD23#	AE5	0.709
D#[24]	L21	0.187	HD24#	AH7	0.863
D#[25]	G26	0.535	HD25#	AH3	0.904
D#[26]	H24	0.412	HD26#	AF4	0.794
D#[27]	M21	0.171	HD27#	AG8	0.789
D#[28]	L22	0.254	HD28#	AG7	0.785
D#[29]	J24	0.410	HD29#	AG6	0.785
D#[30]	K23	0.323	HD30#	AF8	0.711
D#[31]	H25	0.481	HD31#	AH5	0.892
DBI#[1]	G25	0.458	DINVB_1	AG4	0.888
Data Group 2					
DSTBN#[2]	K22	0.252	HDSTBN2#	AE11	0.595
DSTBP#[2]	J23	0.264	HDSTBP2#	AD11	0.532
D#[32]	M23	0.291	HD32#	AC11	0.514
D#[33]	N22	0.227	HD33#	AC12	0.565
D#[34]	P21	0.179	HD34#	AE9	0.652
D#[35]	M24	0.361	HD35#	AC9	0.566
D#[36]	N23	0.273	HD36#	AE10	0.605
D#[37]	M26	0.448	HD37#	AD9	0.635
D#[38]	N26	0.431	HD38#	AG9	0.724
D#[39]	N25	0.386	HD39#	AC10	0.543
D#[40]	R21	0.161	HD40#	AE12	0.558
D#[41]	P24	0.332	HD41#	AF10	0.666
D#[42]	R25	0.373	HD42#	AG11	0.703
D#[43]	R24	0.320	HD43#	AG10	0.705
D#[44]	T26	0.411	HD44#	AH11	0.754
D#[45]	T25	0.378	HD45#	AG12	0.669
D#[46]	T22	0.219	HD46#	AE13	0.563
D#[47]	T23	0.269	HD47#	AF12	0.596
DBI#[2]	P26	0.438	DINVB_2	AH9	0.775
Data Group 3					
DSTBN#[3]	W22	0.302	HDSTBN3#	AC15	0.443
DSTBP#[3]	W23	0.303	HDSTBP3#	AC16	0.395

Processor lengths			MCH-M Lengths		
Signal	**Processor ball**	**Length (inches)**	**Signal**	**MCH-M ball**	**Length (inches)**
D#[48]	U26	0.424	HD48#	AG13	0.668
D#[49]	U24	0.329	HD49#	AH13	0.712
D#[50]	U23	0.269	HD50#	AC14	0.412
D#[51]	V25	0.386	HD51#	AF14	0.548
D#[52]	U21	0.174	HD52#	AG14	0.621
D#[53]	V22	0.246	HD53#	AE14	0.520
D#[54]	V24	0.343	HD54#	AG15	0.612
D#[55]	W26	0.457	HD55#	AG16	0.610
D#[56]	Y26	0.460	HD56#	AG17	0.619
D#[57]	W25	0.429	HD57#	AH15	0.703
D#[58]	Y23	0.339	HD58#	AC17	0.399
D#[59]	Y24	0.386	HD59#	AF16	0.580
D#[60]	Y21	0.214	HD60#	AE15	0.534
D#[61]	AA25	0.422	HD61#	AH17	0.672
D#[62]	AA22	0.268	HD62#	AD17	0.419
D#[63]	AA24	0.387	HD63#	AE16	0.503
DBI#[3]	V21	0.202	DINVB_3	AD15	0.431

5. Double Data Rate Synchronous DRAM (DDR-SDRAM) System Memory Design Guidelines

5.1. Introduction

The Intel 845MP/845MZ chipset Double Data Rate (DDR) SDRAM system memory interface consists of 120 CMOS signals. These CMOS signals have been divided into several signal groups: Data, Command, Control, Feedback, and Clock signals. Table 13 summarizes the different signal groupings. Refer to the *Intel® 845MP/845MZ Chipset Memory Controller Hub-Mobile (MCH-M) Datasheet* for details on the signals listed.

Table 13. Intel 845MP/845MZ DDR Signal Groups

Group	Signal Name	Description
Data	SDQ[63:0]	Data Bus
	SCB[7:0]	Check Bits for ECC Function
	SDQS[8:0]	Data Strobes
Command	SMA[12:0]	Memory Address Bus
	SBS[1:0]	Bank Select
	SRAS#	Row Address Select
	SCAS#	Column Address Select
	SWE#	Write Enable
Control	SCKE[3:0]	Clock Enable - (One per Device Row)
	SCS#[3:0]	Chip Select - (One per Device Row)
Feedback	RCVENOUT#	Output Feedback Signal
	RCVENIN#	Input Feedback Signal
Clocks	SCK[5:0]	DDR-SDRAM Differential Clocks - (3 per SO-DIMM)
	SCK#[5:0]	DDR-SDRAM Inverted Differential Clocks - (3 per SO-DIMM)

Caution: The Intel 845MP/845MZ chipset does not support data masking. The system memory DQM[7:0] pins on the DDR SO-DIMM's must be tied to ground.

5.2. DDR System Memory Topology and Layout Design Guidelines

The Intel 845MP/845MZ chipset Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology.

This section contains information and details on the DDR topologies, the DDR layout and routing guidelines, and the DDR power delivery requirements that will provide for a robust DDR solution on a Intel 845MP/845MZ based design.

The MCH-M AGP ST[0] signal is sampled by the MCH-M on power-on to indicate at what system memory mode, DDR, the MCH-M should configure and operate. An internal MCH-M pull-up resistor on this signal sets the default system memory configuration to PC133 SDRAM. To enable the MCH-M to operate in DDR mode an external pull-down resistor to ground is required on ST[0]. The recommended pull-down resistor is 2 KΩ.

The DDR bus has been designed to route in two ground referenced internal layers. DDR System Memory Topologies for all signal groups have a relatively high via usage, please take this in consideration for the board layout as the vias and the anti-pad for the via could restrict power delivery to the SO-DIMMs.

5.2.1. Data Signals – SDQ[63:0], SDQS[8:0], SCB[7:0]

The MCH-M data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits for Error Checking and Correction (ECC), and 9 data strobe signals. There is an associated data strobe (DQS) for each data (DQ) and check bit (CB) group. This section summarizes the DQ/CB to DQS matching.

The data signals include SDQ[63:0], SDQS[8:0], and SCB[7:0]. The data signals should transition from an external layer to an internal signal layer under the MCH-M. Keep to the same internal layer until transitioning back to an external layer at the series resistor. After the series resistor, the signal route should transition from the external layer to the same internal layer and route to SO-DIMM0. At SO-DIMM0 the signal should transition to an external layer and connect to the appropriate pad of the connector. At the SO-DIMM0 transition continue the signal route on the same internal layer to SO-DIMM1. Transition back out to an external layer and connect to the appropriate pad of SO-DIMM1 and the parallel termination resistor.

Data Signals (SDQ[63:0],SDQS[8:0],SCB[7:0]) need to be routed on the same inner signal layer. In addition, match routing topology and via placement for all signals in a given byte lane including the associated strobe. External trace lengths should be minimized. To facilitate simpler routing, swapping of the byte lane and the associated strobe is allowed. Bit swapping within the byte lane is also allowed. Intel suggests that the parallel termination be placed on both sides of SO-DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals can not be placed within the same R pack as the command and control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Figure 20. Data Signal Routing Topology

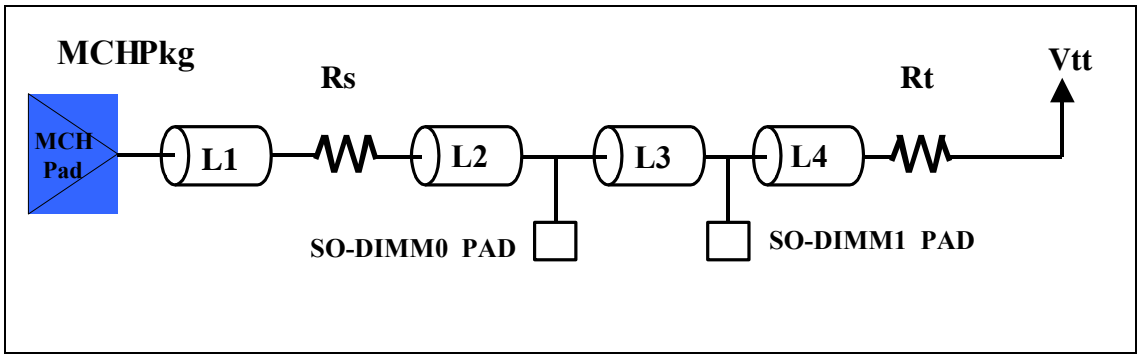


Table 14. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	Data – SDQ[63:0], SCB[7:0], SDQS[8:0]	
Topology	Daisy Chain	Figure 20 Figure 23
Reference Plane	Ground Referenced	
Characteristic Trace Impedance (Zo)	55 Ω ±15%	
Trace Width	Inner layer: 4 mils Outer layer: 5 mils	
Trace to space ratio	• 1:2 (e.g. 4 mil trace 8 mil space)	
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils minimum	
Trace Length L1– MCH-M die pad to Series Termination Resistor Pad	Min = 2.0” Max = 3.5”	Figure 20
Trace Length L2 – Series Termination Resistor Pad to First SO-DIMM Pad	Max = 0.75”	Figure 20
Trace Length L3 – SO-DIMM Pad to SO-DIMM Pad	Max = 1.25”	Figure 20
Trace Length L4 – Last SO-DIMM Pad to Parallel termination Resistor Pad	Max = 0.8”	Figure 20
Series Resistor (Rs)	22 Ω ± 5% (see note below)	Figure 20
Termination Resistor (Rtt)	56 Ω ± 5% (see note below)	Figure 20
Maximum Recommended motherboard via Count per signal	**5 vias**	
Length Matching Requirements	• SDQ[63:0], SCB[7:0] to SDQS[8:0] • SDQS[8:0] to SCK/SCK#[5:0] • See Section 5.2.1.1 for details • See Section 5.2.1.2 for details	Figure 21, Figure 22

NOTES:
1. Recommended resistor values may change in a later revision of the design guide.
2. The overall maximum and minimum lengths to the SO-DIMM must comply with clock length matching requirements.

5.2.1.1. Data to Strobe Length Matching Requirements

The data signals SDQ[63:0] and the check bit signals [7:0] are grouped by byte lane and associated with a data strobe, SDQS[7:0]. The data signals and check bit signals must be length matched to their associated strobe within ± 25mils. For SO-DIMM0 this length matching includes the MCH-M package length and the motherboard trace length to the pads of the SO-DIMM0 connector (MCH-M package + L1 + L2). For SO-DIMM1 this length matching includes the MCH-M package length and the motherboard trace length to the pads of the SO-DIMM1 connector (MCH-M package + L1 + L2 + L3).

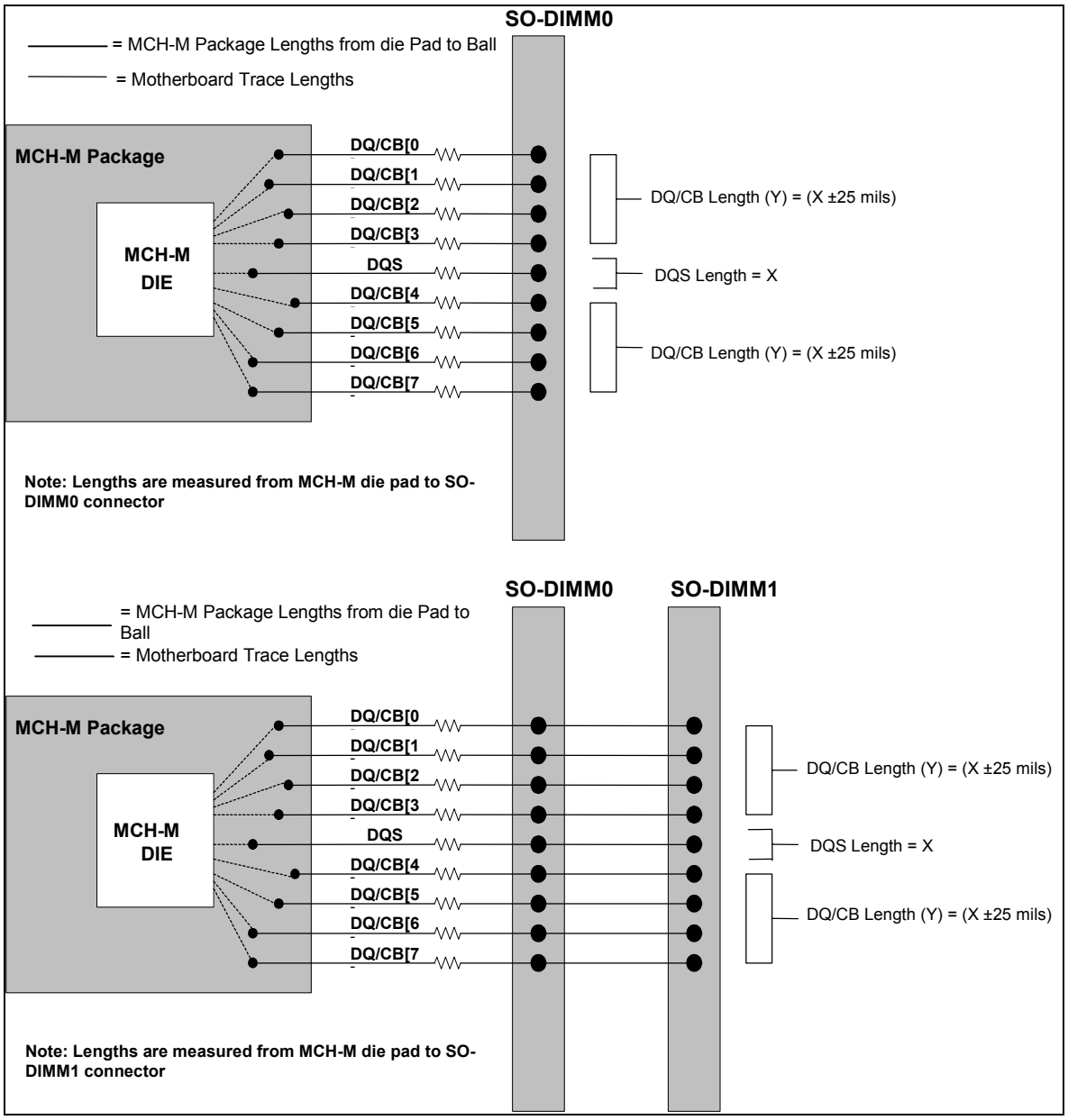
- Associated SDQS Length = X
- SDQ/SCB Byte Group Length = Y, where (X – 25 mils) ≤ Y ≤ (X + 25 mils)
- Length X and Y include the compensated MCH-M Package Length + the Motherboard Trace Length

No length matching is required from the second SO-DIMM to the parallel termination resistors. The table and diagram below depict the length matching requirements between the DQ, CB, and DQS signals.

Table 15. DQ/CB to DQS Length Mismatch Mapping

Signal	Length Mismatch	Relative To
SDQ[7:0]	±25 mils	SDQS0
SDQ[15:8]	±25 mils	SDQS1
SDQ[23:16]	±25 mils	SDQS2
SDQ[31:24]	±25 mils	SDQS3
SDQ[39:32]	±25 mils	SDQS4
SDQ[47:40]	±25 mils	SDQS5
SDQ[55:48]	±25 mils	SDQS6
SDQ[63:56]	±25 mils	SDQS7
SCB[7:0]	±25 mils	SDQS8

Figure 21. DQ/CB to DQS Trace Length Matching Requirements



5.2.1.2. Strobe to Clock Length Matching Requirements

The data strobe signals must be 1.0 inch to 2.0 inches shorter than their associated differential clock pairs.

Length matching equation for SO-DIMM0:
X_1=SCK/SCK#[2:0]
Y_1=SDQS[8:0] = MCH-M package + L1 + L2 of Figure 21 where,

$(X_1 – 2.0”) \leq Y_1 \leq (X_1 – 1.0”)$

Length matching equation for SO-DIMM1:
X_2=SCK/SCK#[5:3]
Y_2= SDQS[8:0] = MCH-M Package + L1 + L2 + L3 of Figure 21 where,

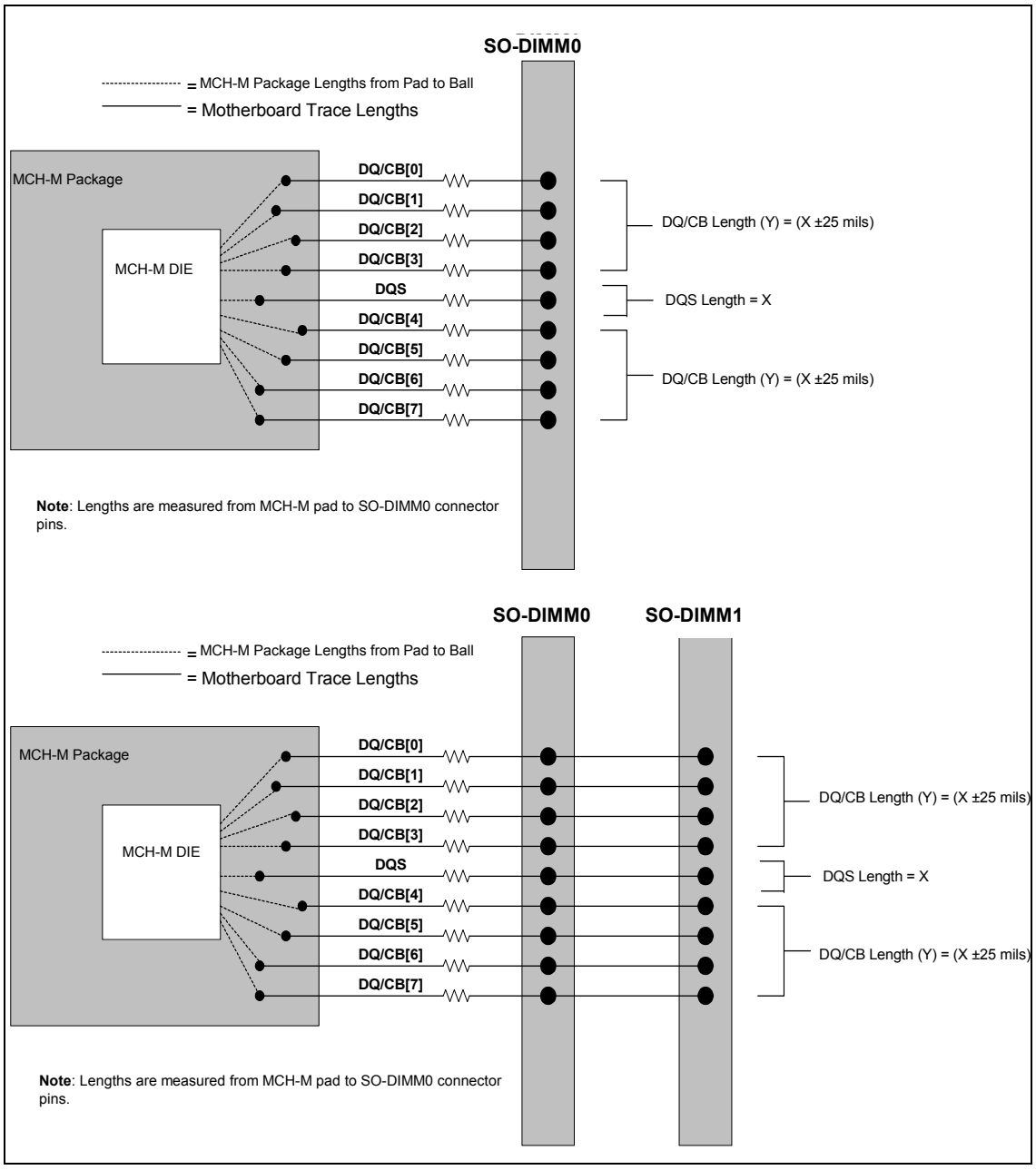
$(X_2 – 2.0”) \leq Y_2 \leq (X_2 – 1.0”)$

For example if the total clock length of SCK/SCK#[2:0](X_1) is 3.5 inches then the length of all data strobe signal routing to SO-DIMM0 must be between 1.5 inches to 2.5 inches, if SCK/SCK#[5:3](X_2) is 4.5 inches then the length of all control signal route to SO-DIMM1 must be between 2.5 inches to 3.5 inches.

- The MCH-M package lengths for clocks and strobes **must** be taken into account for routing length matching.
- Refer to Section Table 23 or the *Pentium® 4 Processor-M in the 568 Pin Package* and *845MP/845MZ Chipset Platform Trace Length Calculator* for package trace length data.

Figure 22 depicts the length matching requirements between the data strobe signals and the clock signals.

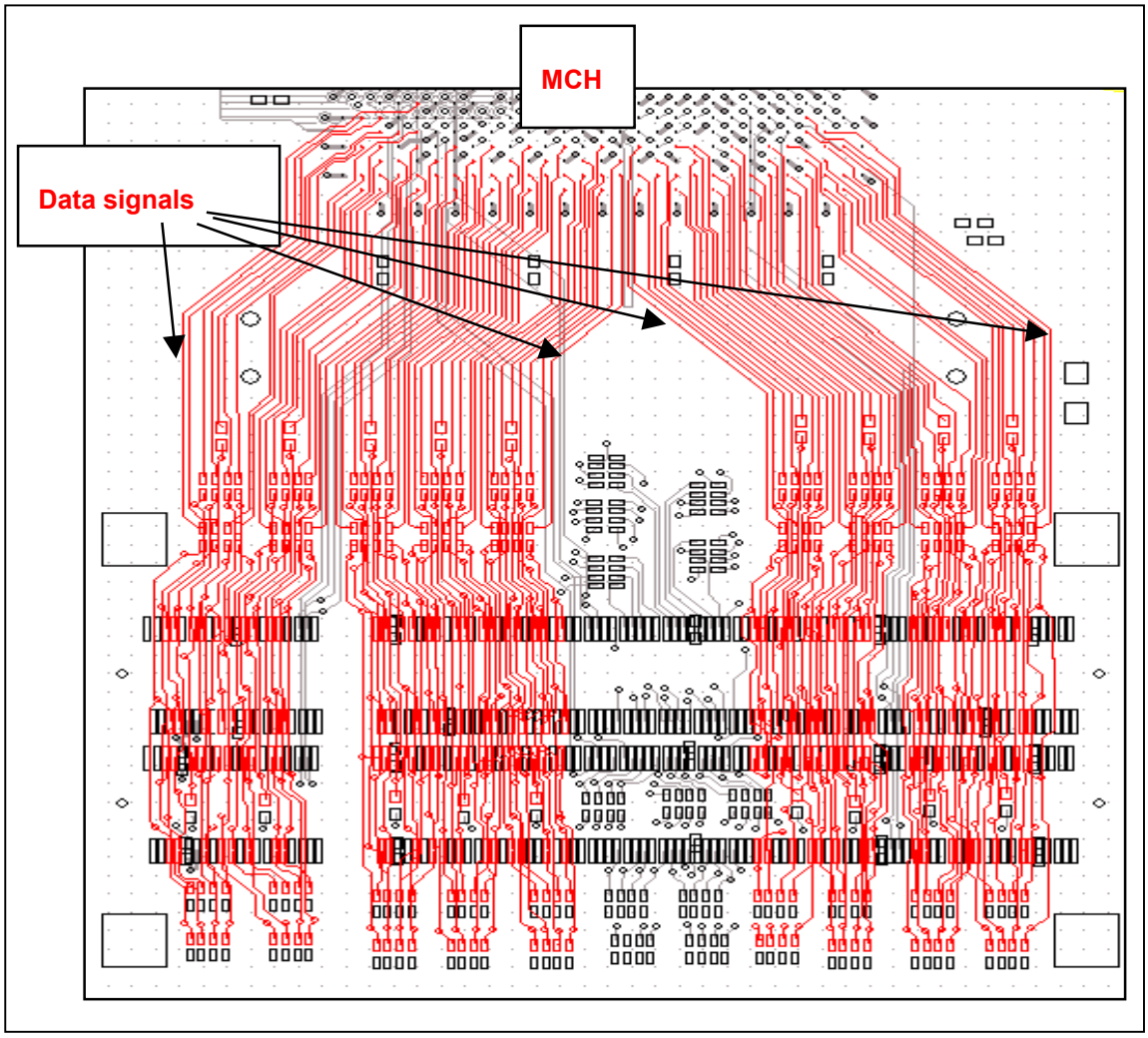
Figure 22. SDQS to SCK/SCK# Trace Length Matching Requirements



5.2.1.3. Data Routing Example

Figure 23 is an example of a board routing for the data signal group. Data routing is shown in red. The majority of the Data signal route is on an internal layer, both external layers can used for parallel termination R-pack placement.

Figure 23. Data Signal Group Routing Example



5.2.2. Control Signals – SCKE[3:0], SCS#[3:0]

The MCH-M control signals, SCKE[3:0] and SCS#[3:0], are common clocked signals. They are "clocked" into the DDR SDRAMs using clock signals SCK/SCK#[5:0]. The MCH-M drives the control and clock signals together, with the clocks crossing in the valid control window. The MCH-M provides one chip select and one clock enable signal per SO-DIMM physical device row. Two chip-selects and two clock-enables will be routed to each SO-DIMM. Table 16 summarizes the control signal mapping.

Table 16. Control Signal SO-DIMM Mapping

Signal	Relative To	SO-DIMM Pin
SCS#[0]	SO-DIMM0	121
SCS#[1]	SO-DIMM0	122
SCS#[2]	SO-DIMM1	121
SCS#[3]	SO-DIMM1	122
SCKE[0]	SO-DIMM0	96
SCKE[1]	SO-DIMM0	95
SCKE[2]	SO-DIMM1	96
SCKE[3]	SO-DIMM1	95

Refer to Figure 24 and Figure 27 for clarification of the description below.

The control signal routing should transition from an external layer to an internal signal layer under the MCH-M. It should keep to the same internal layer until transitioning back out to an external layer(s) to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. Intel suggests that control be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors but control signals can't be placed within the same Rpacks as data, strobe or command signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals going to SO-DIMM0 or SO-DIMM1.

Figure 24. SO-DIMM0, 1 Control Signal Routing Topology

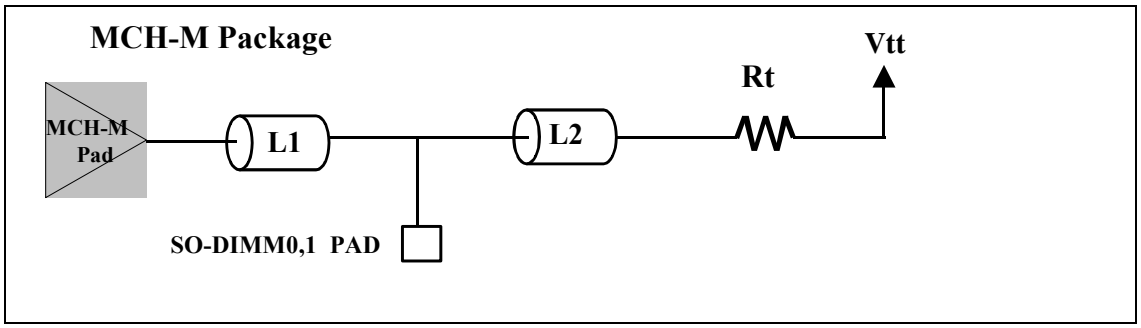


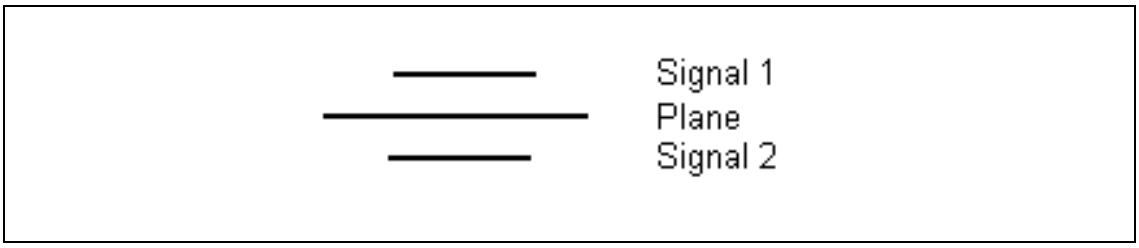
Table 17. Control Signal Group Routing Guidelines1

Parameter	Routing Guidelines	Figure
Signal Group	Control – SCS#[3:0], SCKE[3:0]	
Topology	Point to Point Parallel Termination	Figure 24, Figure 27
Reference Plane	Ground Referenced[2]	
Characteristic Trace Impedance (Zo)	55 Ω ± 15%	
Trace Width	Inner Layer= 4 mils Outer Layer= 5 mils	
Trace to space ratio	1:2 (e.g. 4mil trace 8mil space)	
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils	
Trace Length L1 – MCH-M Control Signal Ball to SO-DIMM Pad	Min = 0.5” Max= 5.0”	Figure 24
Trace Length L2 – SO-DIMM Pad to Rtt Pad	Max = 2.0”	Figure 24
Parallel Termination Resistor (Rtt)	56 Ω +/- 5% (see note below)	Figure 24
Maximum Recommended motherboard via Count per signal	3 vias[3]	Figure 27
Length Matching Requirements	SCS#/SCKE[3:0] to SCK/SCK#[5:0] See section 0 for details	Figure 26

NOTES:
1. Recommendations may change in a later revision of the design guide based on a post silicon simulation analysis.
2. Where ever possible control signal should be routed on adjacent layers to the referenced plane. See Figure 25 below for example, the control signal routing should only route on Signal 1 and Signal 2 layer where Signal 1 may be external (microstrip) and Signal 2 may be internal (stripline) or where Signal 1 is internal (stripline) and Signal 2 is external (microstrip).
3. It is possible to route control using 2 vias if one via is shared that connect to SO-DIMM and parallel termination resistor.

Note: The overall maximum and minimum lengths to the SO-DIMM must comply with clock length matching requirements.

Figure 25. Referencing Plane Stack-up



5.2.2.1. Control Group Signal Length Matching Requirements

The control signals must be 1.0 inch to 3.0 inches shorter than their associated differential clocks pair.

Note that these requirements may change in a later revision of the design guide based on a post silicon simulation analysis.

Length matching equation for SO-DIMM0:
X_1=SCK/SCK#[2:0]
Y_1=SCS#[1:0] and SCKE[1:0] = L1 of Figure 26 where,

$(X_1 – 3.0”) \leq Y_1 \leq (X_1 – 1.0”)$

Length matching equation for SO-DIMM1:
X_2=SCK/SCK#[5:3]
Y_2=SCS#[3:2] and SCKE[3:2] = L1 of Figure 26 where,

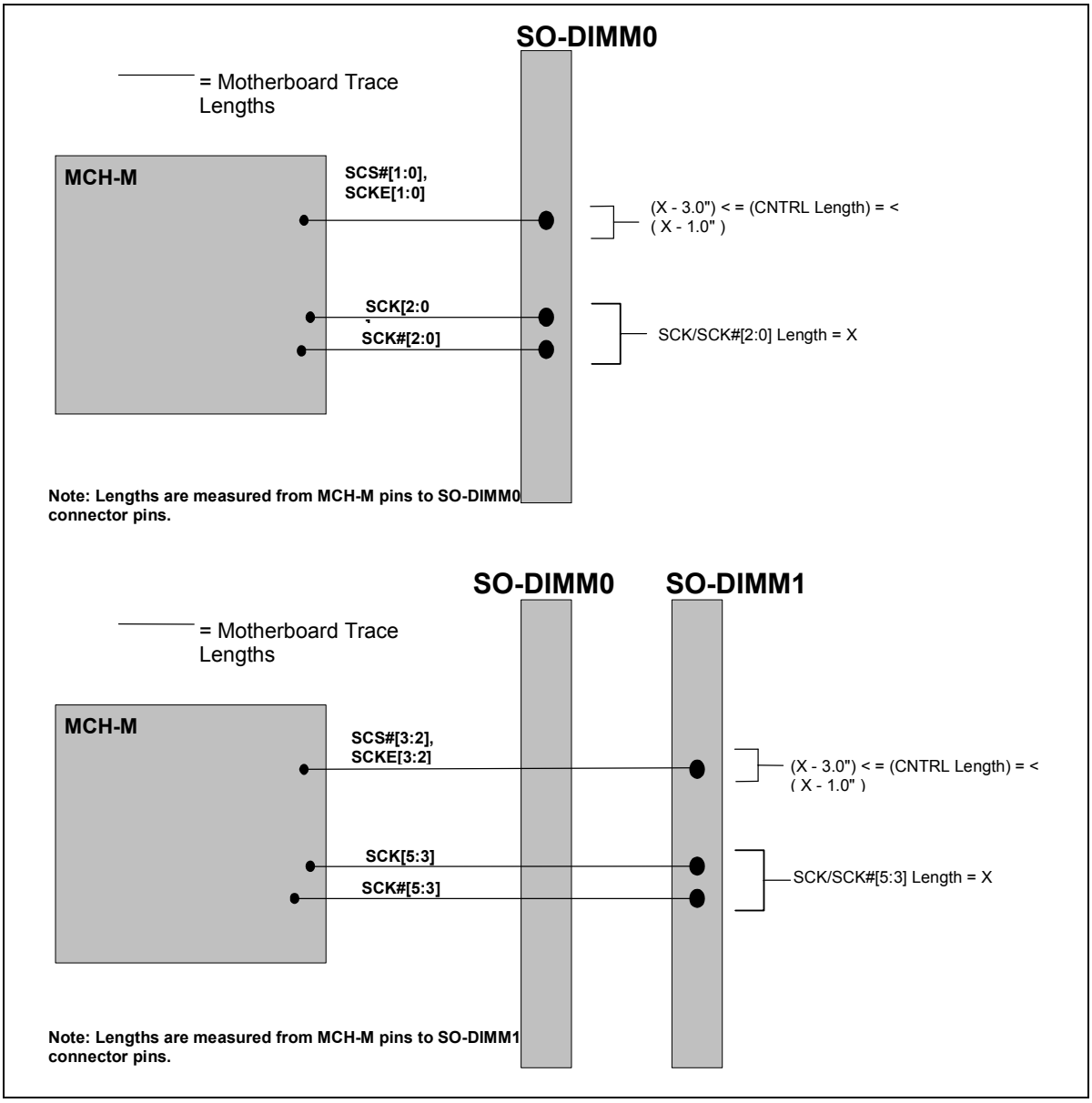
$(X_2 – 3.0”) \leq Y_2 \leq (X_2 – 1.0”)$

For example if the clock length of SCK/SCK#[2:0](X_1) is 3.5 inches then the length of all control signal routing to SO-DIMM0 must be between 0.5 inches to 2.5 inches, if SCK/SCK#[5:3](X_2) is 4.5 inches then the length of all control signal route to SO-DIMM1 must be between 1.5 inches to 3.5 inches.

- The MCH-M package lengths don’t need to be taken into account for routing purpose.

Figure 26 depicts the length matching requirements between the control signals and the clock signals.

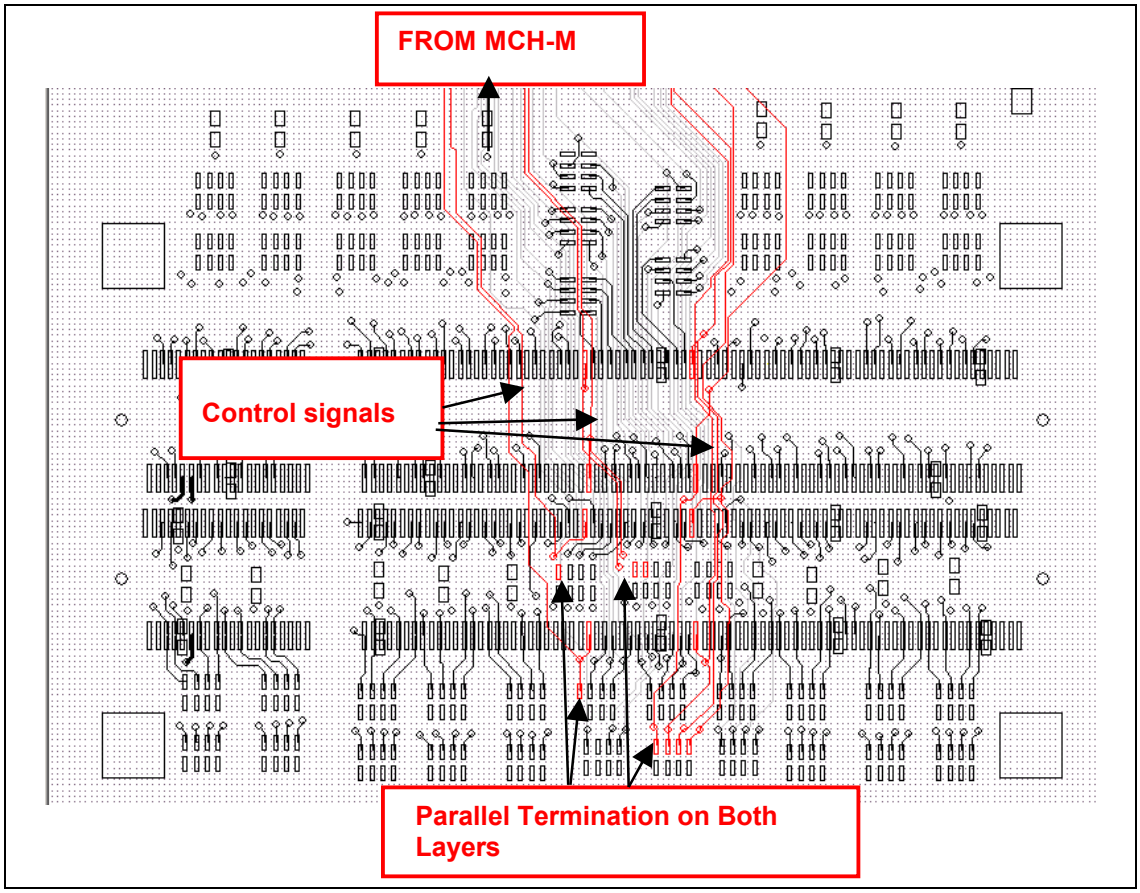
Figure 26. Control Signal to SCK/SCK# Trace Length Matching Requirements



5.2.2.2. Control Routing Example

Figure 27 is an example of a board routing for the control signal group.

Figure 27. Control Routing Example



Control routing is shown in red. The majority of the control signal route is on an internal layer, both external layers are used for parallel termination R-pack placement.

5.2.3. Command Signals – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

There are two supported topologies for the command signal group. This section has been divided into two subsection; Topology 1 and Topology 2. Topology 2 is the topology that best allows for placement of the SO-DIMMs back to back in the butterfly configuration, thus minimizing the SO-DIMM footprint area. Mixing topology 1 and topology 2 is "OK", as long as designer follows this document's guidelines.

The MCH-M command signals; SMA[12:0], SBS[1:0], SRAS#, SCAS#, and SWE#; are common clocked signals. They are "clocked" into the DDR SDRAMs using the clock signals SCK/SCK#[5:0]. The MCH-M drives the command and clock signals together, with the clocks crossing in the valid command window.

5.2.3.1. Command Topology 1 Solution

5.2.3.1.1. Routing description for Command Topology 1

Refer to Figure 28 and Figure 31 for clarification of the description below. The command signal routing should transition from an external layer to an internal signal layer under the MCH-M. Keep to the same internal layer until transitioning back to an external layer immediately prior to connecting the appropriate pad of the SO-DIMM0 connector. At the SO-DIMM0 layer transition continue the signal route on the same internal layer to the series resistor Rd2d, collocated to SO-DIMM1. At this resistor the signal should transition to an external layer immediately prior to the pad of Rd2d. After the series resistor, Rd2d, continue the signal route on the external layer landing on the appropriate connector pad of SO-DIMM1. After SO-DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

External trace lengths should be minimized. It is suggested that the parallel termination(Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is suggested that command be routed on same internal layer.

Resistor packs are acceptable for the series (Rd2d) and parallel (Rt) command termination resistors but command signals can't be placed within the same Rpacks as data, strobe or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1 for topology 1.Collocating the series resistor, Rd2d, and SO-DIMM1 allows for the elimination of one via from the signal route.

Figure 28. Command Signal Routing Topology 1

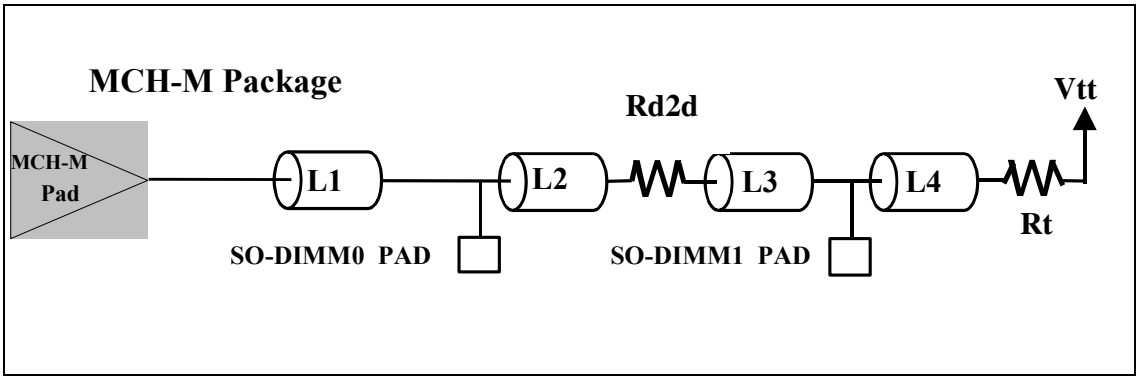


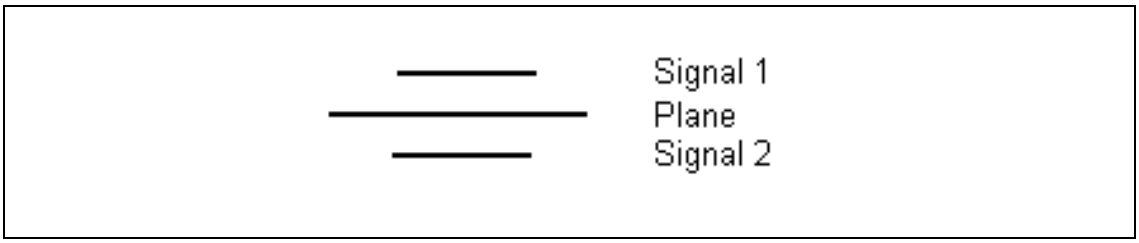
Table 18. Command Signal Group Routing Guidelines[1]

Parameter	Routing Guidelines	Figure
Signal Group	Command – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#	
Topology	Daisy Chain	Figure 28, Figure 31
Reference Plane	Ground Referenced[2]	
Characteristic Trace Impedance (Zo)	55Ω ±15%	
Trace Width	Inner layers= 4 mils Outer layer= 5 mils	
Trace to space ratio	1:2 (e.g. 4mil trace 8mil space)	
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils	
Trace Length L1 – MCH-M Command Signal ball to Rs Pad	Min = 1.0” Max= 4.0”	Figure 28
Trace Length L2 + L3 – SO-DIMM0 Pad to Rd2d Pad; Rd2d Pad to SO-DIMM1 pad	Max=1.3”	Figure 28
Trace Length L4 – SO-DIMM1 Pad to Rt Pad	Max =0.8”	Figure 28
Series Resistor (Rd2d) SO-DIMM0 to SO-DIMM1	10 Ω ± 5%	Figure 28
Parallel Termination Resistor (Rt)	56 Ω ± 5%	Figure 28
Maximum Recommended motherboard via Count per signal	5 vias3	Figure 31
Length Matching Requirements	CMD to SCK/SCK#[5:0] See 5.2.3.1.2 for details	Figure 30

NOTES:
1. Recommendation may change in a later revision of the design guide based on a post silicon simulation analysis.
2. Where ever possible command signals should be routed on adjacent layers to the referenced plane. See Figure 29 below for example, the command signal routing should only route on Signal 1 and Signal 2 layer where Signal 1 may be external (microstrip) and Signal 2 may be internal (stripline) or where Signal 1 is internal(stripline) and Signal 2 is external(microstrip). The ground plane is shared between Signal 1 and Signal2.
3. It is possible to route using 3 vias if one via is shared that connects to SO-DIMM1 and the parallel termination resistor.

Note: The overall maximum and minimum lengths to the SO-DIMM must comply with clock length matching requirements.

Figure 29. Referencing Plane Stack-up



5.2.3.1.2. Command Group Signal Length Matching Requirements

The command signals must be 1.0 inch to 3.0 inches shorter than their associated differential clock pairs SCK/SCK#[5:0].

Note that these requirements may change in a later revision of the design guide based on a post silicon simulation analysis.

Length matching equation for SO-DIMM0:
X_1=SCK/SCK#[2:0]
Y_1=L1 of Figure 30 where,

(X_1 – 3.0”) ≤ Y_1 ≤ (X_1 – 1.0 inch)

Length matching equation for SO-DIMM1:
X_2=SCK/SCK#[5:3]
Y_2=L1+L2+L3 of Figure 30where,

(X_2 – 3.0 inches) ≤ Y_2 ≤ (X_2 – 1.0 inch). For example if the clock length of SCK/SCK#[2:0](X_1) is 5.0 inches then the length of all command signal routing to SO-DIMM0 must be between 2.0 inches to 4.0 inches, if SCK/SCK#[5:3](X_2) is 5.5 inches then the length of command signal routing to SO-DIMM1 must be between 2.5 inches to 4.5 inches.

Caution: The MCH-M package lengths do not need to be taken into account for routing purposes. Figure 30 below depicts the length matching requirements between the command signals and the clock signals.

Figure 30. Command Signal to SCK/SCK# Trace Length Matching Requirements

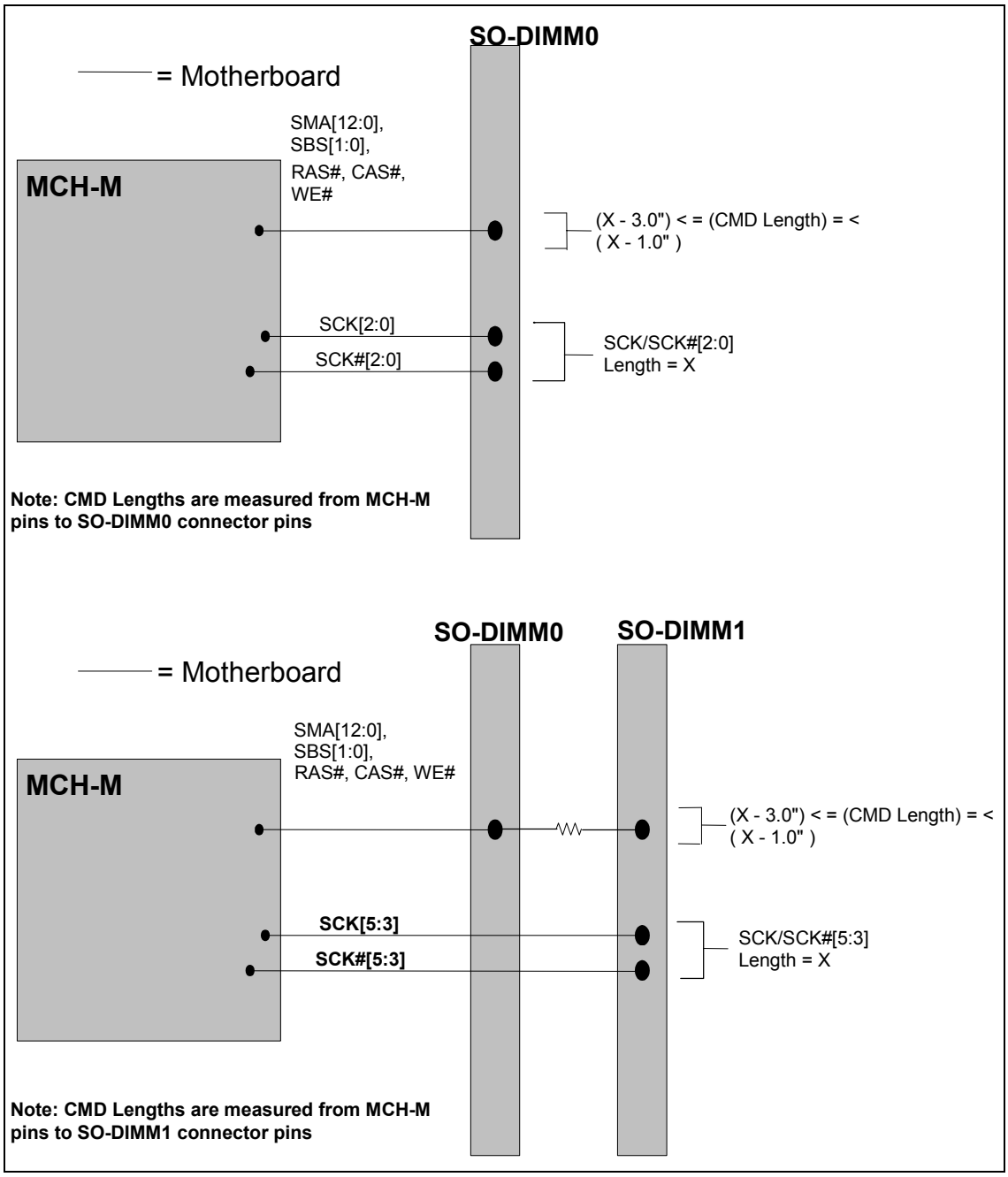
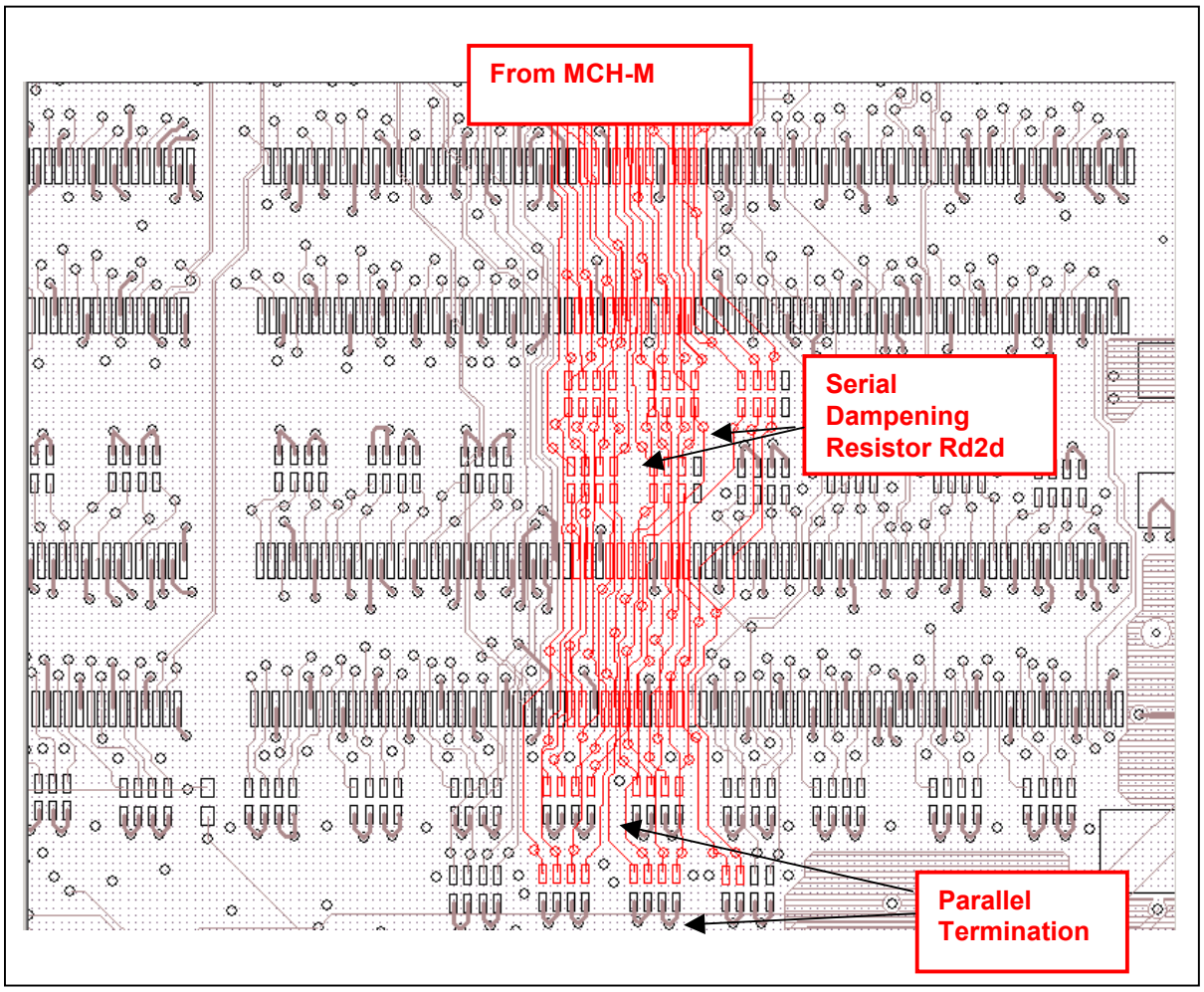


Figure 31. Command Routing Example for Topology 1



NOTE: Red signals are command routing. The majority of the command signal route is on an internal layer.

5.2.3.2. Command Topology 2 Solution

5.2.3.2.1. Routing Description for Command Topology 2

Refer to Figure 32 and Figure 33 for clarification of the description below.

The command signal routing should transition from an external layer to an internal signal layer under the MCH-M. Keep to the same internal layer until transitioning back to an external layer at the series resistor Rd2d. At this point there is a T in the topology. One leg of the T will route through Rd2d and either transition back to the same internal layer or stay external and landing on the appropriate connector pad of SO-DIMM0. If it was necessary to return to the internal layer the signal should return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM0. The other leg of the T will continue on the same internal layer and return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM1. If possible stay on the external layer and connect to the parallel termination resistor or if the parallel termination resistor is on the opposite side of the board from the SO-DIMM1 connector then share the via and route to the parallel termination resistor. If sharing the via or using the opposite side of the board is not possible, continue on the same internal layer and route to the external layer immediately prior to the termination resistor.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

Resistor packs are acceptable for the series (Rd2d) and parallel (Rt) command termination resistors but command signals can't be placed within the same Rpacks as data, strobe or control signals.

The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals going to SO-DIMM0 and SO-DIMM1.

Figure 32. Command Signal Routing Topology

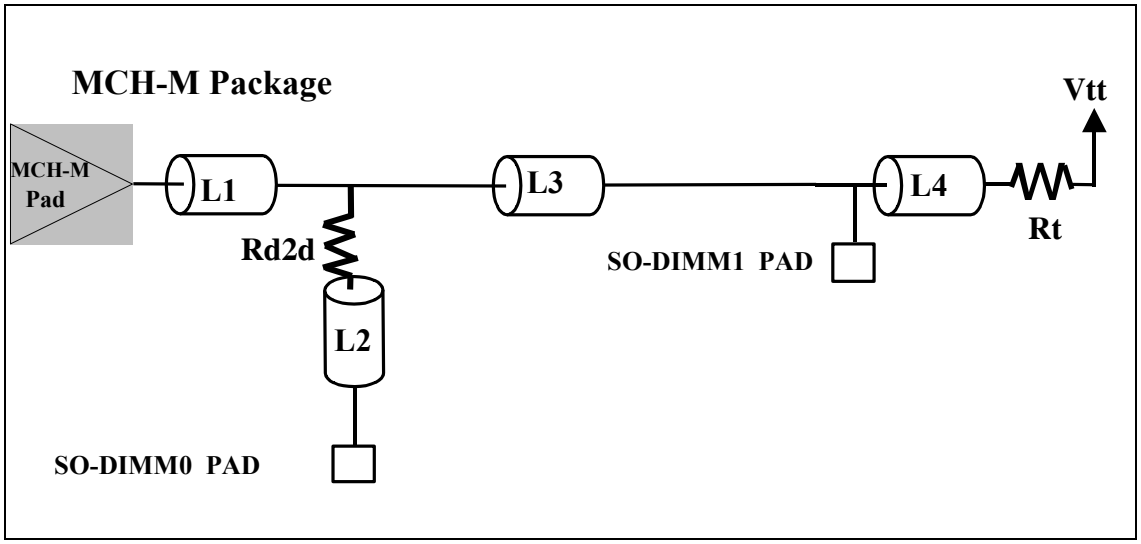


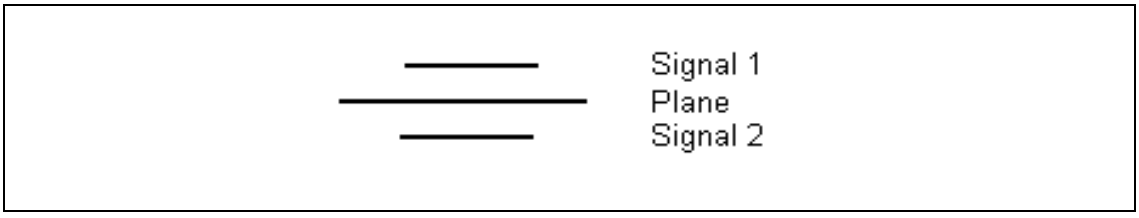
Table 19. Command Signal Group Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	Command – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#	
Topology	T Topology	Figure 32, Figure 35
Reference Plane	Ground Referenced[2]	
Characteristic Trace Impedance (Zo)	55 Ω ± 15%	
Trace Width	Inner layers= 4 mils Outer layer= 5 mils	
Trace to space ratio	1:2 (e.g. 4mil trace 8mil space)	
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils	
Trace Length L1 – MCH-M Command Signal ball to Rs Pad	Min = 0.5” Max= 5.0”	Figure 32
Trace Length L2 – Rd2d Pad to SO-DIMM0 Pad	Max = 1.0”	Figure 32
Trace Length L3 – Rd2d Pad to SO-DIMM1	Min = 0.4” Max=1.75”	Figure 32
Trace Length L4 – SO-DIMM1 Pad to Rt Pad	Max = 0.25”	Figure 32
Series Dampening Resistor (Rd2d)	10 Ω (see note below)[1]	Figure 32
Parallel Termination Resistor (Rt)	56 Ω ± 5%[1]	Figure 32
Maximum Recommended motherboard via Count per signal	**6 vias**[3]	Figure 35
Length Matching Requirements	CMD to SCK/SCK#[5:0] See 5.2.3.2.2 for details	Figure 34

NOTES:
1. Recommendation may change in a later revision of the design guide based on a post silicon simulation analysis.
2. Wherever possible command signals should be routed on adjacent layers to the referenced plane. See Figure 33 for example. The command signal routing should only route on Signal 1 and Signal 2 layer where Signal 1 may be external (microstrip) and Signal 2 may be internal (stripline) or where Signal 1 is internal (stripline) and Signal 2 is external (microstrip).
3. It is possible to route using 3 vias if one via is shared that connect to SO-DIMM0 and Rd2d resistor.

Note: The overall maximum and minimum lengths to the SO-DIMM must comply with clock length matching requirements.

Figure 33. Referencing Plane Stack-up



5.2.3.2.2. Command Group Signal Length Matching Requirements

The command signals, must be 1.0 inch to 3.0 inches shorter than their associated differential clock pairs SCK/SCK#[5:0].

Note that these requirements may change in a later revision of the design guide based on a post silicon simulation analysis.

Length matching equation for SO-DIMM0:
X_1=SCK/SCK#[2:0]
Y_1=L1 +L2 of Figure 34 where,

$(X_1 – 3.0”) \leq Y_1 \leq (X_1 – 1.0 \text{ inch})$

Length matching equation for SO-DIMM1:
X_2=SCK/SCK#[5:3]
Y_2=L1+L3 of Figure 34 where,

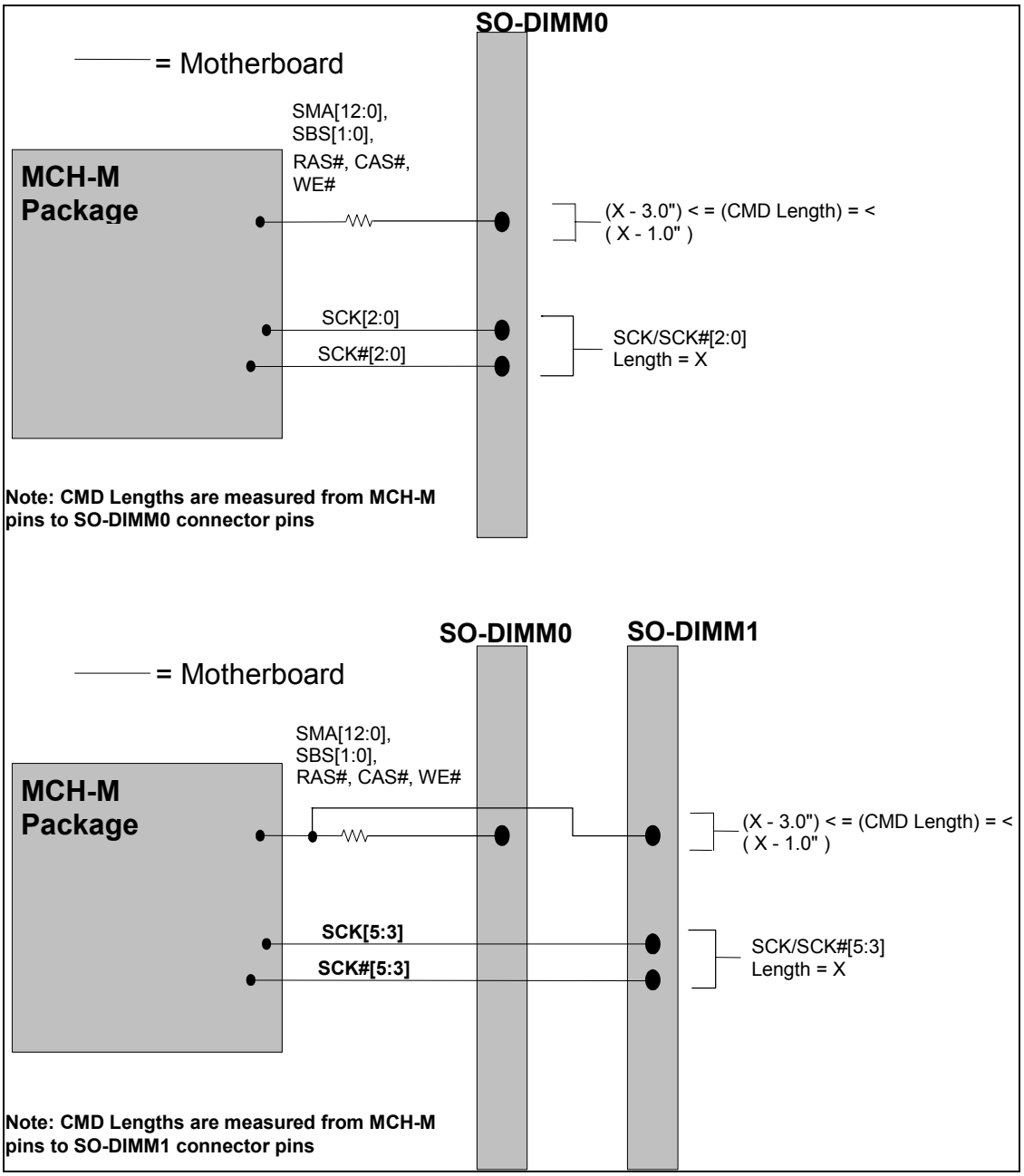
$(X_2 – 3.0”) \leq Y_2 \leq (X_2 – 1.0 \text{ inch})$

For example if the clock length of SCK/SCK#[2:0](X_1) is 3.0 inches then the length of all command signal routing to SO-DIMM0 must be between 0.75 inches to 2.0 inches, if SCK/SCK#[5:3](X_2) is 3.5 inches then the length of all command signal routing to SO-DIMM0 must be between 0.5 inches to 2.5 inches. The minimum length of 0.75 inches for command signal routing is the shortest possible length to SO-DIMM0.

Caution: The MCH-M package lengths don’t need to be taken into account for routing purposes.

The diagram below depicts the length matching requirements between the command signals and the clock signals.

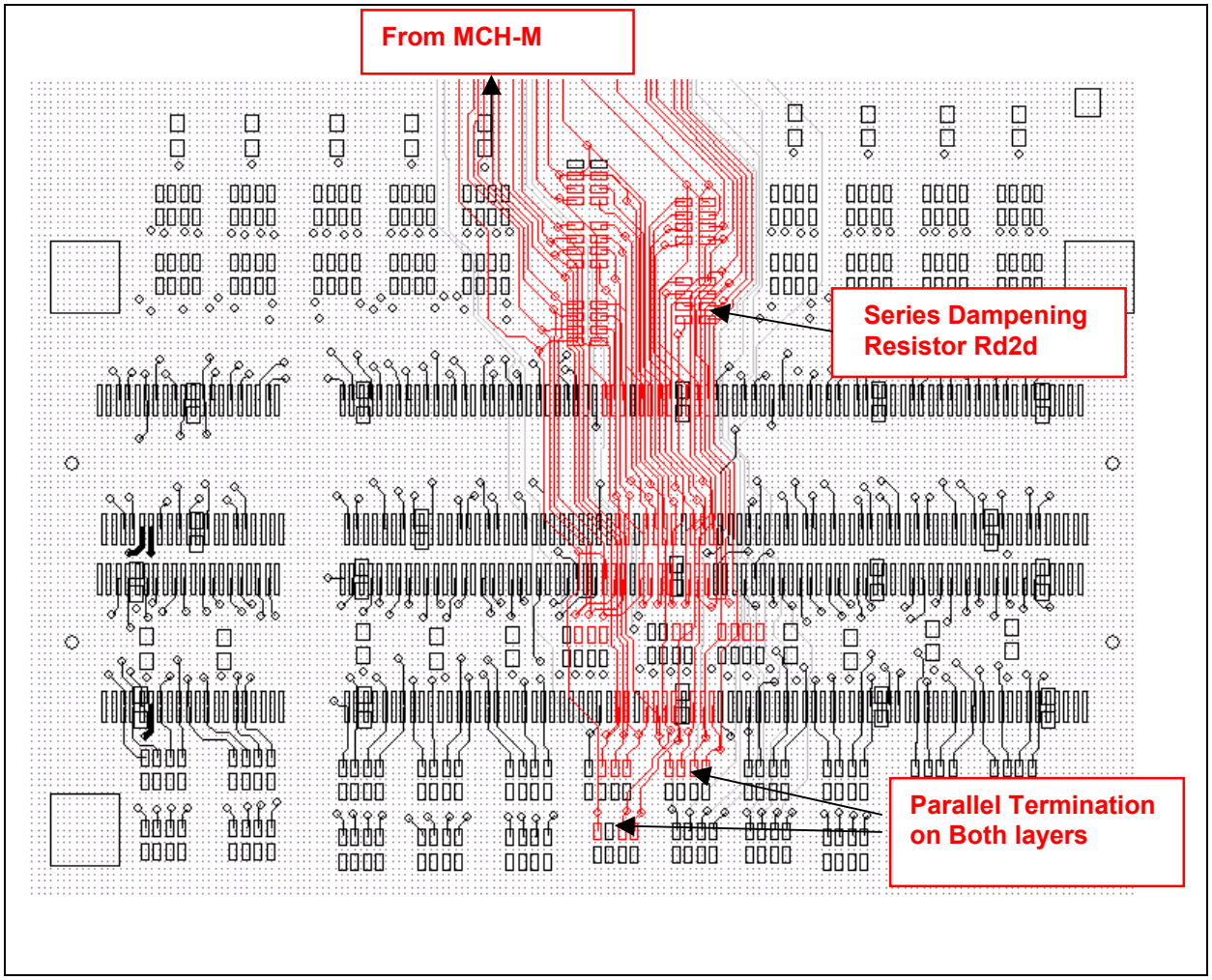
Figure 34. Command Signal to SCK/SCK# Trace Length Matching Requirements



5.2.3.2.3. Command Routing Example for Topology 2 Solution

Figure 35 is an example of a board routing for the command signal group.

Figure 35. Command Routing Example for Topology 2



NOTE: Red signals are command routing. The majority of the command signal route is on an internal layer; both external layers are used for parallel termination R-pack placement. Note that the series dampening R-packs are rotated to allow for improved power distribution.

5.2.4. Clock Signals – SCK[5:0], SCK#[5:0]

The clock signal group includes the differential clock pairs SCK[5:0] and SCK#[5:0]. The MCH-M generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The MCH-M only supports unbuffered DDR SO-DIMMs, three differential clock pairs are routed to each SO-DIMM connector. Table 20 summarizes the clock signal mapping.

Table 20. Clock Signal Mapping

Signal	Relative To
SCK[2:0], SCK#[2:0]	SO-DIMM0
SCK[5:3], SCK#[5:3]	SO-DIMM1

Note: One to one mapping of the clocks from the MCH-M to the SO-DIMM is not required. For example, it is not necessary that SCK0 from the MCH-M routes to the same number clock on the SO-DIMM0 connector, which is CK0 in the PC2100 and PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification. However CKn and CKn# may not be swapped from the MCH-M to the SO-DIMMs. The changing of clock numbering from MCH-M to SO-DIMMs may require a BIOS change.

The clock signal routing should transition from an external layer to an internal signal layer under the MCH-M and route as a differential pair referenced to ground for the entire length to their associated SO-DIMM connector pads. Immediately prior to the SO-DIMM connector the signals should transition to an external layer to connect the appropriate pad of the connector.

External trace lengths should be minimized. All internal and external signal routing should be ground referenced to keep the path of the return current continuous.

The diagrams and table below depict the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 36. DDR Clock Routing Topology (SCK/SCK#[2:0])

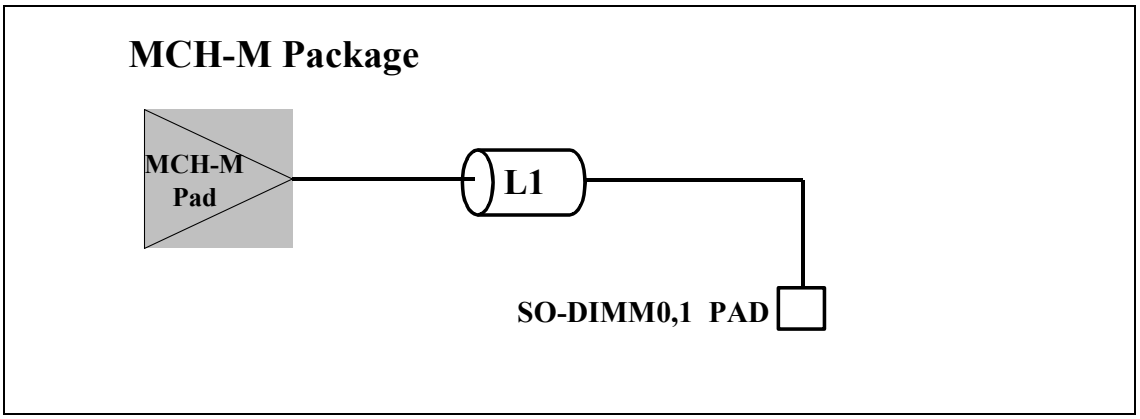
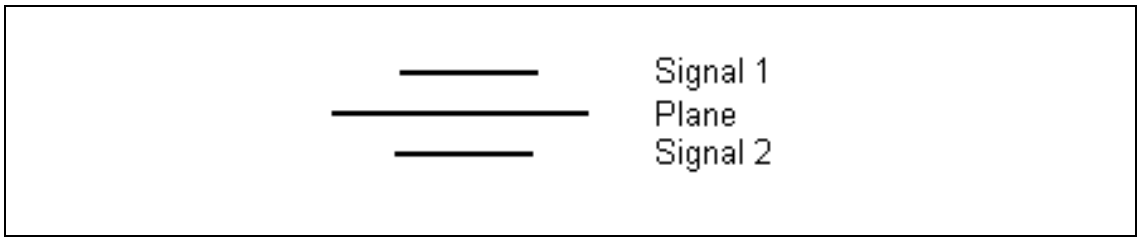


Table 21. Clock Signal Group Routing Guidelines[1]

Parameter	Routing Guidelines	Figure
Signal Group	Clock – SCK[5:0], SCK#[5:0]	
Topology	Differential Pair Point to Point	Figure 35
Reference Plane	Ground Referenced[2]	
Characteristic Trace Impedance (Zo)	Single Ended =55 Ω ± 15%	
Trace Width	Inner layers= 4 mils Outer layer= 5 mils	
Differential Trace Spacing	Inner layers= 4 mils Outer layer= 5 mils	
Group Spacing	Isolation spacing from another DDR signal group = 20 mils Isolation spacing from non-DDR related signals = 20 mils	
Serpentine Spacing	12 mils minimum	
Trace Length L1 – MCH-M Signal ball to Associated SO-DIMM0 Connector Pad	Min = 1.5” Max= 8.0”	Figure 35
Maximum Recommended motherboard via Count **per signal**	**2 vias**	
Length Matching Requirements	SCK / SCK# The three SO-DIMM0 Clock pairs are equal in length plus tolerance, and the three SO-DIMM1 Clock pairs are equal in length plus tolerance. See Section 5.2.4.1 for details	Figure 38, Figure 39
Clock pair to pair tolerance	± 25 mils	
SCK to SCK# tolerance	± 10 mils	

NOTES:
1. Recommendation may change in a later revision of the design guide based on a post silicon simulation analysis.
2. Wherever possible the clock signals should be routed on adjacent layers to the referenced ground plane. See Figure 37 for example. The clock signal routing should only route on Signal 1 and Signal 2 layer where Signal 1 may be external (microstrip) and Signal 2 may be internal (stripline) or where Signal 1 is internal (stripline) and Signal 2 is external (microstrip).

Figure 37. Ground Referencing Plane Stack-up



5.2.4.1. Clock Group Signal Length Matching Requirements

The MCH-M provides three differential clock pair signals for each SO-DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. The differential pairs for one SO-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]
SCK[2] / SCK#[2]

The differential pairs for the second SO-DIMM are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]
SCK[5] / SCK#[5]

The SCK and SCK# lengths must include both the MCH-M Package Length plus the Motherboard Trace Length.

Clock length matching is required between clock pairs to their specified SO-DIMM connector. The differential clock pairs must be matched to ± 25 mils including MCH-M package lengths. Each SCK to SCK# pair must be matched to ±10 mils including MCH-M package lengths.

Please note that the differential clocks must be 1.0 inch to 2.0 inches longer than the data and data strobe signals, and 1.0 inch to 3.0 inches longer then the control and command signals. For information covering the data and data strobe to clock length matching requirements reference 5.2.1.1, for information covering the control signal to clock length matching requirements reference 5.2.2.1, and for information covering the command signal to clock length matching requirements reference Section 5.2.3.1.2 and 5.2.3.2.2-update link. The diagrams below depict the clock length matching requirements. Refer to the *Pentium® 4 Processor-M in the 568 Pin Package* and *Intel® 845MP/845MZ Chipset Platform Trace Length Calculator* for package trace length data.

Figure 38. SCK to SCK# Trace Length Matching Requirements

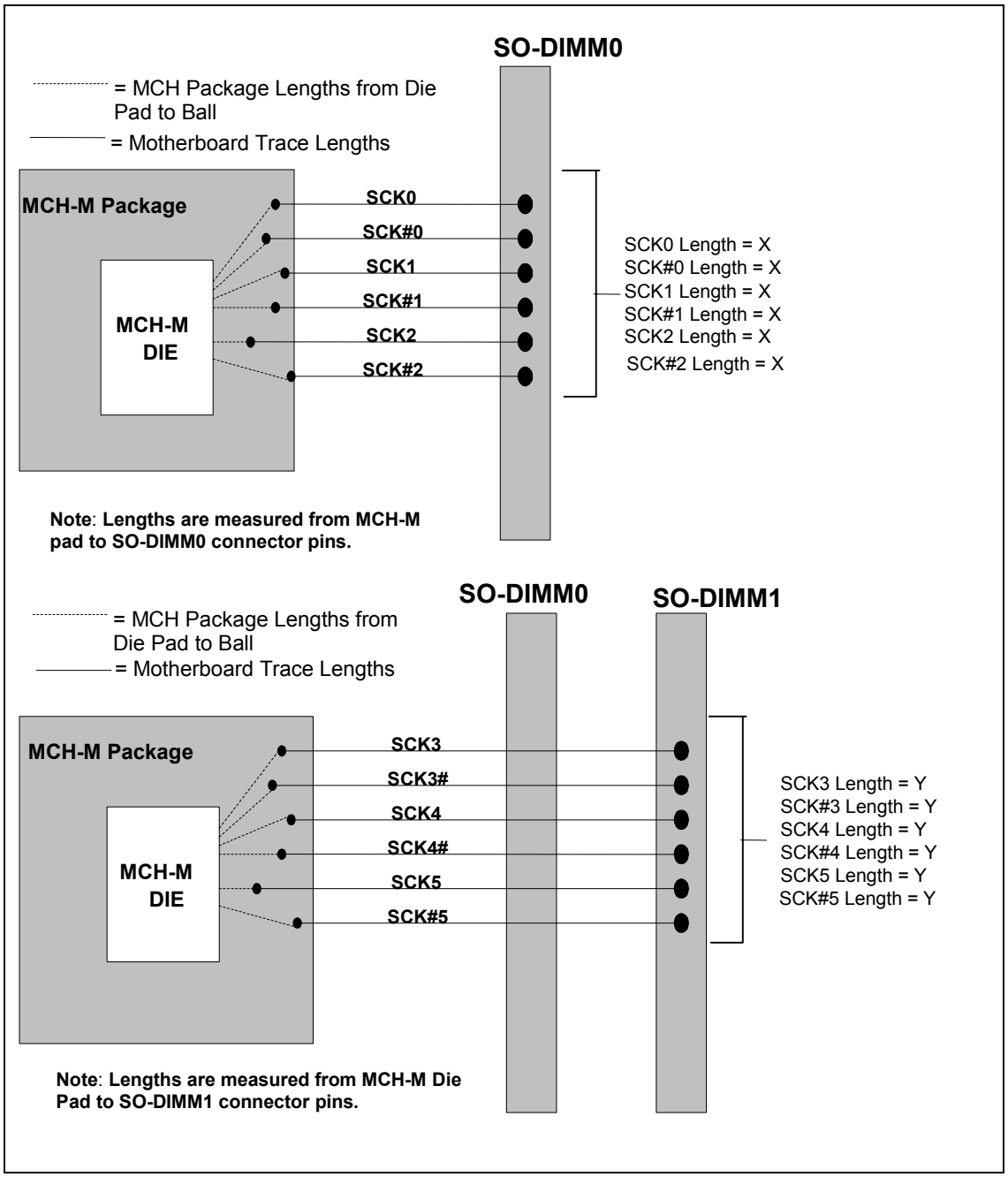
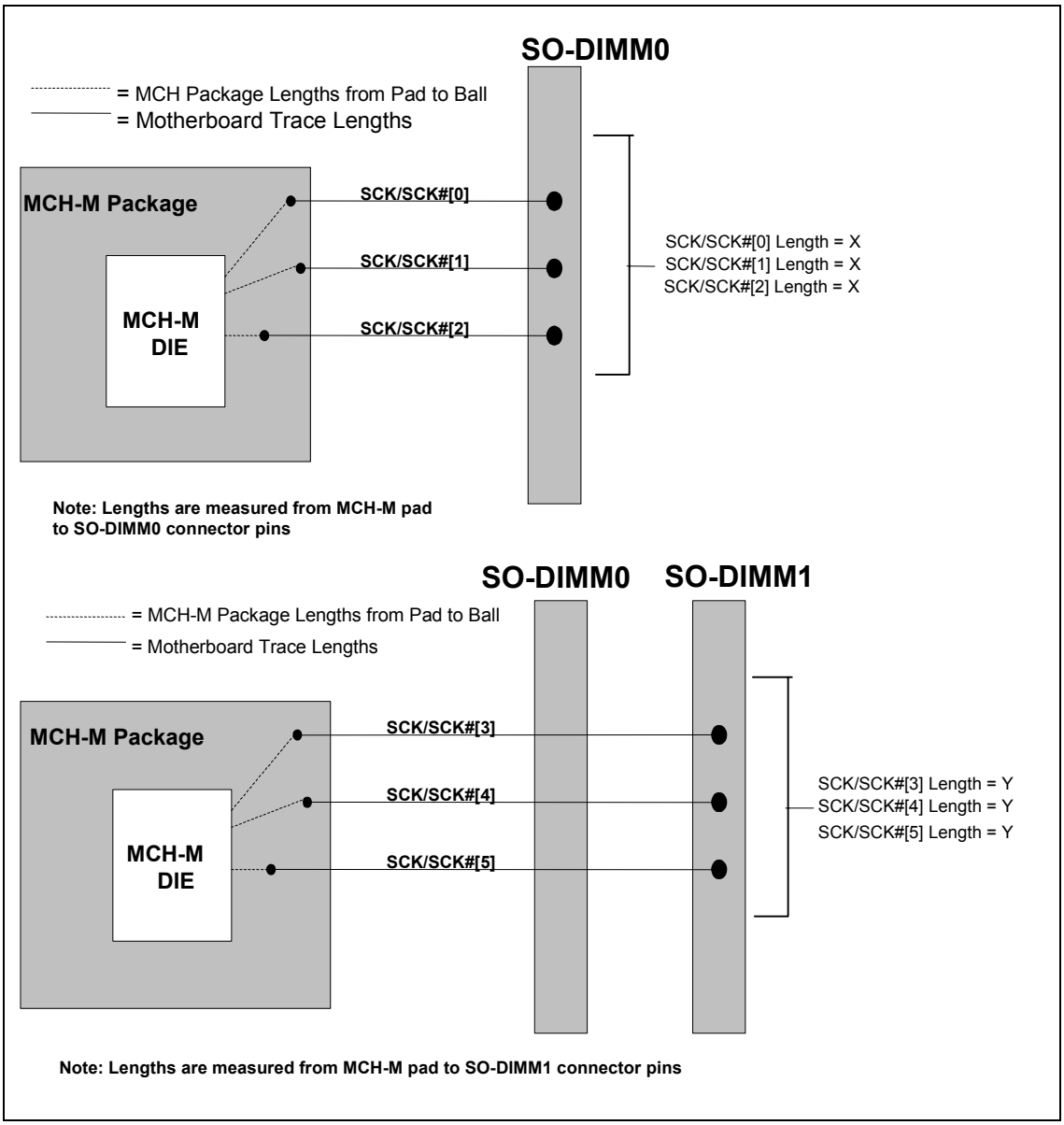


Figure 39. Clock Pair Trace Length Matching Requirements



5.2.5. Feedback - RCVENOUT#, RCVENIN#

The MCH-M provides a feedback signal called “receive enable” (RCVEN#), which is used to gate the strobe inputs for read data. There are two pins on the MCH-M to facilitate the use of RCVEN#. The RCVENOUT# pin is an output of the MCH-M and the RCVENIN# pin is an input to the MCH-M. RCVENOUT# must connect to RCVENIN#.

The RCVEN# signal must be routed on the same layer as the system memory clocks. It should transition from the top signal layer to an inner signal layer under the MCH-M, routed referenced to ground for the entire length, and then transition from the inner signal layer back to the top signal layer under the MCH-M.

External trace lengths should be minimized. All internal and external signals should be ground referenced to keep the path of the return current continuous.

The diagrams and table below depicts the recommended topology and layout routing guidelines for the DDR-SDRAM feedback signal.

Figure 40. DDR Feedback (RCVEN#) Routing Topology

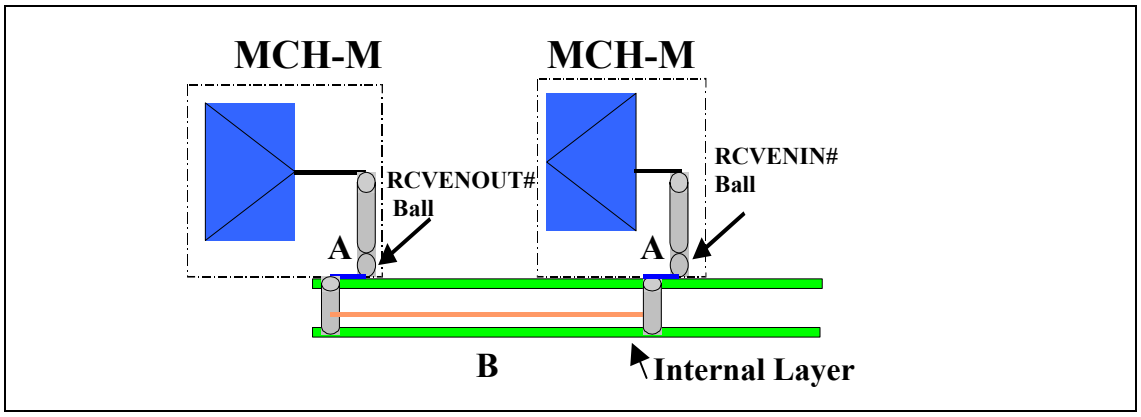


Table 22. DDR Feedback Signal Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	Feedback – RCVENOUT# and RCVENIN#	
Topology	Point to Point	
Reference Plane	Ground Referenced	
Characteristic Trace Impedance (Zo)	55 Ω ± 15%	
Trace Width	Inner layers= 4 mils Outer layers= 5mils	
Group Spacing	Isolation spacing from another DDR signal group = 10 mils Isolation spacing from non-DDR related signals = 10 mils	
Trace Length A – MCH-M Signal Ball to MCH-M Signal Via	Max = 40 mils	Figure 40
Total Length A + B – MCH-M RCVENOUT# Signal Ball to MCH-M RCVENIN# Signal Ball	Must equal 1000 mils ± 10 mils	Figure 40
Maximum via Count per signal	2	
Length Matching Requirements	None	

Table 23. MCH-M DDR Signal Package Lengths

DDR Data Signals					
Data Signal	MCH-M Ball	Package Length (inches)	Data Signal	MCH-M Ball	Package Length (inches)
SDQ0	G28	0.716	SDQ36	B13	0.639
SDQ1	F27	0.699	SDQ37	C13	0.552
SDQ2	C28	0.874	SDQ38	C11	0.588
SDQ3	E28	0.754	SDQ39	D10	0.626
SDQ4	H25	0.532	SDQ40	E10	0.533
SDQ5	G27	0.666	SDQ41	C9	0.605
SDQ6	F25	0.592	SDQ42	D8	0.587
SDQ7	B28	0.892	SDQ43	E8	0.522
SDQ8	E27	0.797	SDQ44	E11	0.523
SDQ9	C27	0.833	SDQ45	B9	0.715
SDQ10	B25	0.812	SDQ46	B7	0.706
SDQ11	C25	0.753	SDQ47	C7	0.643
SDQ12	B27	0.886	SDQ48	C6	0.7
SDQ13	D27	0.867	SDQ49	D6	0.664
SDQ14	D26	0.773	SDQ50	D4	0.76
SDQ15	E25	0.645	SDQ51	B3	0.922
SDQ16	D24	0.722	SDQ52	E6	0.64
SDQ17	E23	0.602	SDQ53	B5	0.846
SDQ18	C22	0.699	SDQ54	C4	0.81
SDQ19	E21	0.566	SDQ55	E5	0.67
SDQ20	C24	0.785	SDQ56	C3	0.859
SDQ21	B23	0.781	SDQ57	D3	0.811
SDQ22	D22	0.64	SDQ58	F4	0.723
SDQ23	B21	0.711	SDQ59	F3	0.814
SDQ24	C21	0.627	SDQ60	B2	0.949
SDQ25	D20	0.555	SDQ61	C2	0.893
SDQ26	C19	0.587	SDQ62	E2	0.865
SDQ27	D18	0.522	SDQ63	G5	0.689
SDQ28	C20	0.615	SCB0	C16	0.57
SDQ29	E19	0.487	SCB1	D16	0.526
SDQ30	C18	0.579	SCB2	B15	0.623
SDQ31	E17	0.521	SCB3	C14	0.533
SDQ32	E13	0.432	SCB4	B17	0.621

DDR Data Signals					
Data Signal	**MCH-M Ball**	**Package Length (inches)**	**Data Signal**	**MCH-M Ball**	**Package Length (inches)**
SDQ33	C12	0.543	SCB5	C17	0.583
SDQ34	B11	0.596	SCB6	C15	0.54
SDQ35	C10	0.59	SCB7	D14	0.503
DDR Data Strobe Signals			**DDR Clock Signals**		
Data Signal	**MCH-M Ball**	**Package Length (inches)**	**Data Signal**	**MCH-M Ball**	**Package Length (inches)**
SDQS0	F26	0.651	SCK0	E14	0.453
SDQS1	C26	0.775	SCK#0	F15	0.432
SDQS2	C23	0.738	SCK1	J24	0.454
SDQS3	B19	0.636	SCK#1	G25	0.587
SDQS4	D12	0.493	SCK2	G6	0.551
SDQS5	C8	0.596	SCK#2	G7	0.543
SDQS6	C5	0.776	SCK3	G15	0.371
SDQS7	E3	0.821	SCK#3	G14	0.349
SDQS8	E15	0.52	SCK4	E24	0.610
			SCK#4	G24	0.548
			SCK5	H5	0.589
			SCK#5	F5	0.693

6. AGP Port Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification, Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide (*Intel® 845MP/845MZ Chipset Platform Design Guide*) focuses only on specific Intel 845MP/845MZ chipset platform recommendations.

6.1. AGP Interface

The *AGP Interface Specification Revision 2.0* enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5-volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in Revision 2.0 of the *AGP Interface Specification*.

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, the data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15 ns (66-MHz clock) or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time; not the clock cycle time. During 2X operation, the data is sampled twice during a 66-MHz clock cycle, therefore, the data cycle time is 7.5 ns.

In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5-V operation, $V_{il_{max}}$ is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

A single AGP connector is supported by the Intel 845MP/845MZ chipset MCH-M AGP interface. LOCK# and SERR#/PERR# are not supported. The AGP buffers operate in only one mode.

1.5-V drive, not 3.3-V safe. This mode is compliant with the AGP 2.0 spec. The Intel 845MP/845MZ chipset can make use of a 1.5V only AGP connector.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The Intel 845MP/845MZ chipset MCH-M supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization

The AGP interface is clocked from the 66-MHz clock (pin 3V66). The AGP interface is synchronous to the host and system memory interfaces with a clock ratio of 1:2 (66 MHz: 133 MHz) and to the hub interface with a clock ratio of 1:1 (66 MHz : 66 MHz).

6.2. AGP 2.0

The *AGP Interface Specification*, rev. 2.0, enhances the functionality of the original *AGP Interface Specification* (rev. 1.0) by allowing 4X data transfers (i.e., 4 data samples per clock) and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle; therefore, the data cycle time is 7.5 ns. In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

6.2.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. The signal groups are documented in the following table.

Table 24. AGP 2.0 Signal Groups

1x Timing Domain	2x/4x Timing Domain	Miscellaneous Signals
AGPCLK PIPE# RBF# WBF# ST[2:0] G_FRAME# G_IRDY# G_TRDY# G_STOP# G_DEVSEL# G_REQ# G_GNT# G_PAR	SET #1 G_AD[15:0] G_CBE[1:0]# AD_STB0 AD_STB0# SET #2 G_AD[31:16] G_CBE[3:2]# AD_STB1 AD_STB1# SET #3 SBA[7:0] SB_STB SB_STB#	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

These signals are used in 4X AGP mode ONLY.

Table 25. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section, the term data refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term strobe refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB#. When the term data is used, it refers to one of the three sets of data signals, as in Table 24. When the term strobe is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

6.3. AGP Routing Guidelines

6.3.1. 1X Timing Domain Routing Guidelines

6.3.1.1. Trace Length Requirements for the AGP 1X

This section contains information on the 1X Timing Domain Routing Guidelines. The AGP 1X timing domain signals (refer to Table 24) has a maximum trace length of 9.5 inches. The target impedance is 55 ohm, with plus and minus fifteen percent tolerance. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 25. In addition to this maximum trace length requirement (refer to Table 27 and Table 28) these signals must meet the trace spacing and trace length mismatch requirements in Sections 6.3.1.2 and 6.3.1.3.

Table 26. Layout Routing Guidelines for AGP 1X Signals

1X signals	Max. length (inches)	Width (mils)	Space (mils)
CLK_AGP_SLT	10	4	4
AGP_PIPE#	10	4	4
AGP_RBF#	10	4	4
AGP_WBF#	10	4	4
AGP_ST[2:0]	10	4	4
AGP_FRAME#	10	4	4
AGP_IRDY#	10	4	4
AGP_TRDY#	10	4	4
AGP_STOP#	10	4	4
AGP_DEVSEL#	10	4	4
AGP_REQ#	10	4	4
AGP_GNT#	10	4	4
AGP_PAR	10	4	4

6.3.1.2. Trace Spacing Requirements

AGP 1X timing domain signals (refer to Table 27) can be routed with 4-mil minimum trace separation.

6.3.1.3. Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

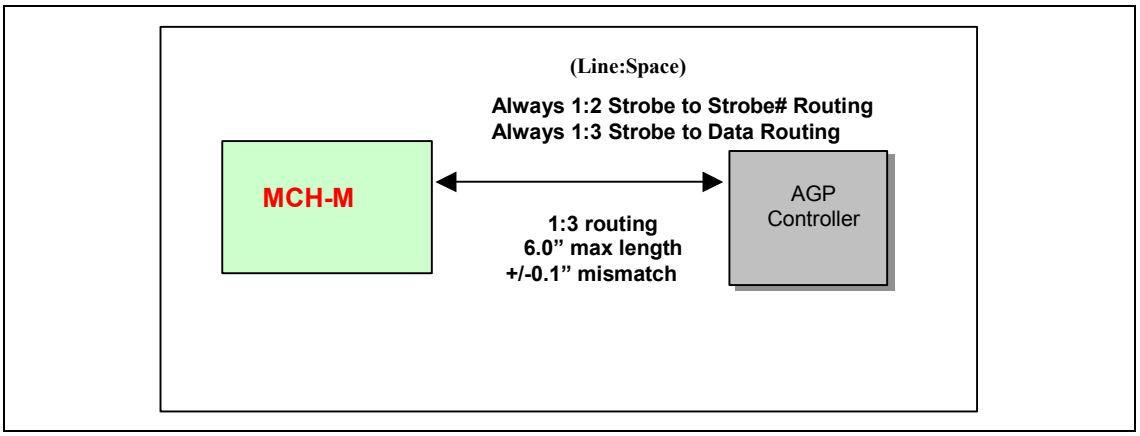
6.3.2. 2X/4X Timing Domain Routing Guidelines

6.3.2.1. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 25. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Sections 6.3.2.2 and 6.3.2.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces. Simulations in mobile environment support this rule.

Figure 41. AGP Layout Guidelines



If the AGP interface is less than 6.0 inches, a 1:2 trace spacing is required for 2X/4X lines. These 2X/4X signals must be matched their associated strobe within ± 0.1 inches. This is for designs that require less than 6 inches between the graphics device and the MCH-M.

Reduce line length mismatch to ensure added margin. In order to reduce trace to trace coupling (cross talk), separate the traces as much as possible.

6.3.2.2. Trace Spacing Requirements

AGP 2X/4X timing domain signals (refer to Table 25) must be routed as documented in Table 28. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the MCH-M. The routing must widen to the requirement in Table 28 within 0.3 inches of the MCH-M package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

Table 27. Layout Routing Guidelines for AGP 2X/4X Signals

Signal	Maximum Length (inch)	Trace Space (mils) (4 mil traces)	Length Mismatch (inch)	Relative To	Notes
2X/4X Timing Domain Set#1	6	8	± 0.1	AGP_ADSTB0 and AGP_ADSTB0#	AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils)
2X/4X Timing Domain Set#2	6	8	± 0.1	AGP_ADSTB1 and AGP_ADSTB1#	AGP_ADSTB1, AGP_ADSTB1# must be the same length ±10 mils)
2X/4X Timing Domain Set#3	6	8	± 0.1	AGP_SBSTB and AGP_SBSTB #	AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils)

6.3.2.3. Trace Length Mismatch Requirements

The length-matching requirement depends on the maximum AGP trace length. If there are no AGP 2X/4X traces longer than 6.0 inches, then signals must be matched within ± 0.1 inches.

Table 28. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Minimum Trace Length	Maximum Trace Length
< 6 in	1:2	X	X – 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. That is, if AD_STB0 and ADSTB0# are 5 inches, then AD[15:0] and C/BE[1:0] must be between 4.9 inches and 5.1 inches. However AD_STB1 and ADSTB1# can be 3.5 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.4 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

All signals should be routed as striplines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin. Table 29 shows AGP 2.0 routing summary.

Table 29. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (4 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	10 in	4 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	8 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	8 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	8 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
Miscellaneous	10 in	8 mils	No Requirement	N/A	PCI_PME#, AGP_PERR#, AGP_SERR#

NOTE: Each strobe pair must be separated from other signals by at least 15 mils.

6.3.3. AGP Clock Skew

The maximum total AGP clock skew, between the Intel 845MP/845MZ and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1-ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

6.3.4. AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel 845MP/845MZ chipset (MCH-M). The following guidelines are not intended to replace thorough system validation on Intel 845MP/845MZ chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the MCH-M. These should be placed within 70 mils of the outer row of balls on the MCH-M for VDDQ decoupling. The closer the placement, the better the performance.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- In order to add the decoupling capacitors within 70 mils of the MCH-M and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1-inch max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four

layer PCB design, the signals transition from one side of the board to the other. One extra 0.01-µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

6.3.5. AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the MCH-M to an AGP connector controller), using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_TRDY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, Intel strongly recommends that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all Intel 845MP/845MZ chipset designs.

6.3.6. Pull-ups

AGP control signals require pull-up resistors to VDDQ on the motherboard to ensure they contain stable values when no agent is actively driving the bus. Intel 845MP/845MZ MCH-M has integrated the following pull-up resistors, however, the following signals may still require pull-up resistors:

- 1X Timing Domain Signals:
  - FRAME#
  - TRDY#
  - IRDY#
  - DEVSEL#
  - STOP#
  - SERR#
  - PERR#
  - RBF#
  - PIPE#
  - REQ#
  - WBF#
  - GNT#
  - ST[2:0]
  - PAR

It is critical that these signals be pulled up to 1.5 V.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept at less than 0.5 inches, to avoid signal reflections from the stub.

The strobe signals require pull-ups/pull-downs on the motherboard to ensure that they contain stable values when no agent is driving the bus.

INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

The 2X/4X Timing Domain Signals are:

- AD_STB[1:0] (pull up to 1.5 V)
- SB_STB (pull up to1.5 V)

- AD_STB[1:0]# (pull down to ground)
- SB_STB# (pull down to ground)

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1 inch, to avoid signal reflections from the stub.

The pull-up/pull-down resistor value requirements are shown in Table 30.

Table 30. AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 KΩ	16 KΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ.

The MCH-M ST[0] signal needs a site for an external pull-down resistor to ground.

6.3.7. AGP VDDQ and Vref

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. AGP specifies VCC voltage plane as ALWAYS 3.3 V. VDDQ is the interface voltage. The external graphics controller may ONLY power the MCH-M AGP I/O buffers with the 1.5-V VDDQ power pins.

In AGP 1.0 implementations, VDDQ was also 3.3 V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ as both are tied to the 3.3-V power plane on the motherboard. AGP 2.0 requires that these power planes are separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5 V) operation. The VCC and VDDQ power supplies are such that the VDDQ voltage level is never more than 0.5 V above the VCC voltage level.

6.3.8. Vref Generation for AGP 2.0(2X & 4X)

6.3.8.1. 3.3-V AGP Interface (AGP 2x)

The 3.3-V AGP interfaces will use only one Vref. That is, only one resistor divider on the AGP controller that will divide VDDQ down to Vref for MCH-M and AGP controller. For Intel 845MP/845MZ platforms, only 1.5-V interface will be supported.

6.3.8.2. 1.5-V AGP interface (AGP 2x & 4x)

In order to account for potential differences between VDDQ and GND at the MCH-M and graphics controller, both devices use *source generated Vref*. That is, the Vref signal is generated at the graphics controller and *sent* to the MCH-M, and another Vref is generated at the MCH-M and *sent* to the graphics controller.

Both the graphics controller and the MCH-M are required to generate Vref. The voltage divider networks consist of AC and DC elements.

The Vref divider network should be placed as close to the *AGP* interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

All resistors used in above reference generation schemes should have ± 1% tolerance.

6.3.9. Compensation

The MCH-M AGP interface supports resistive buffer compensation (RCOMP). For Printed Circuit Boards with Characteristics impedance of 55 Ω, tie the AGP_RCOMP pin to a 36.5 Ω, 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈0.5 inches) trace.

7. MCH-M PLL Requirements

7.1. MCH-M PLL Power Delivery

VCCA1 and VSSA1, and VCCA0 and VSSA0 are power sources required by the MCH-M's PLL clock generators.

Figure 42. Intel 845MP/845MZ PLL0 Filter

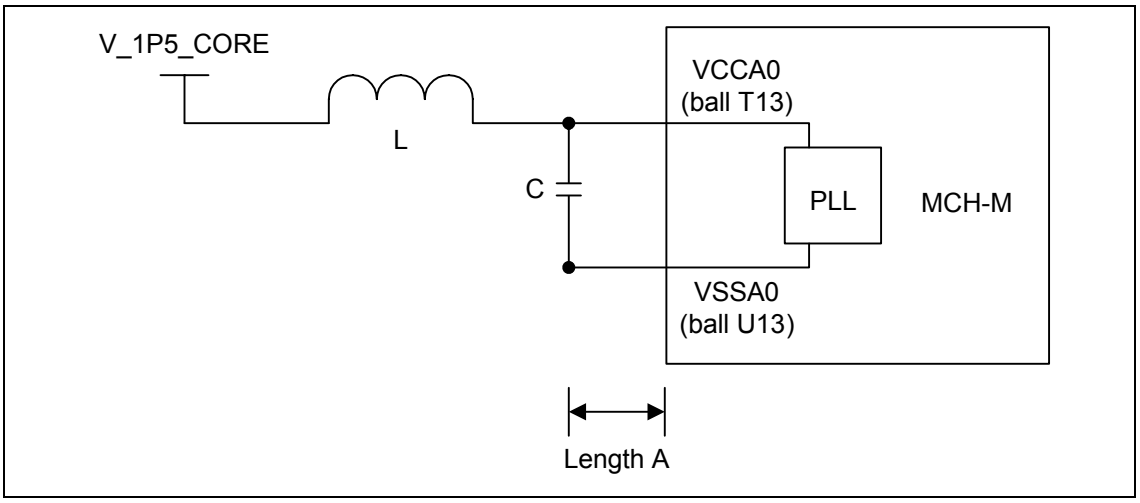


Table 31. PLL0 Filter Routing Guidelines

Parameter	Routing Guidelines
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – A	1.5"
Capacitor – C	33 µF
Inductor – L	4.7 µH

Figure 43. Intel 845MP/845MZ PLL1 Filter

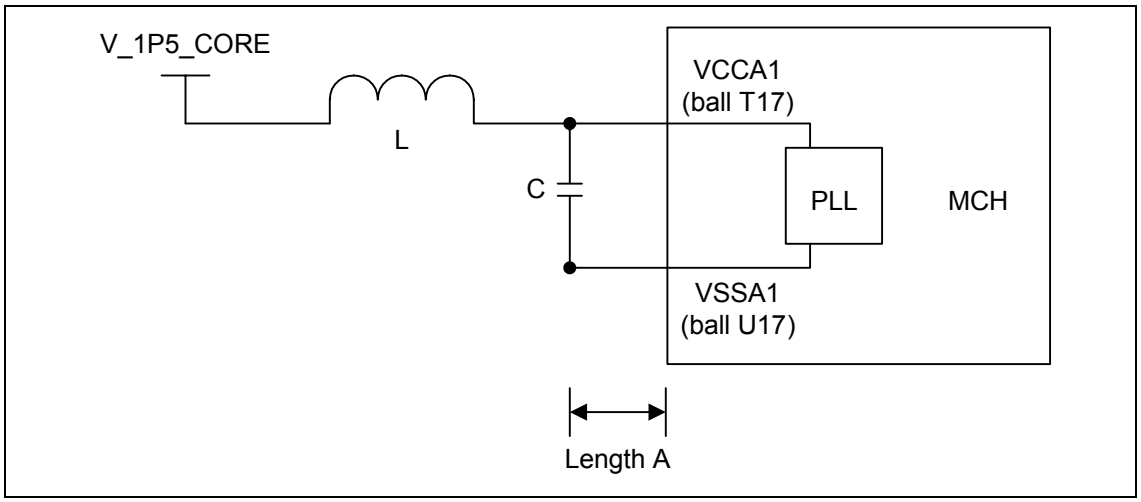


Table 32. PLL1 Routing Guidelines

Parameter	Routing Guidelines
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – A	1.5”
Capacitor – C	33 µF
Inductor – L	4.7 µH

Table 33. Recommended Inductor Components for MCH-M PLL Filter

Value	Tolerance	SRF	Rated I	DCR
4.7µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max)
4.7µH	10%	47 MHz	30 mA	0.7 Ω (±50%)
4.7µH	30%	35 MHz	30 mA	0.3 Ω max

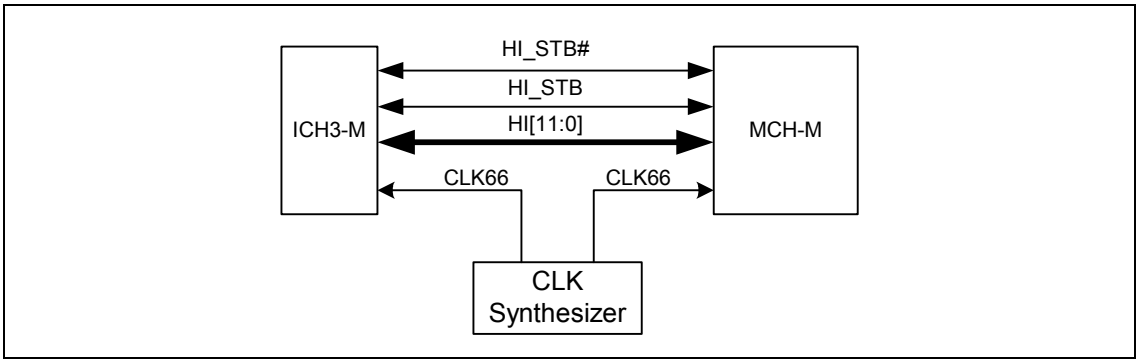
Table 34. Recommended Capacitor Components for MCH-M PLL Filter

Value	ESL	ESR
33 µF	2.5 nH	0.225 Ω
33 µF	2.5 nH	0.2 Ω

8. Hub Interface

The MCH-M and ICH3-M ballout assignments have been optimized to simplify the Hub Interface routing between these devices. Intel recommends that the Hub Interface signals be routed directly from the MCH-M to ICH3-M with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer. The Hub Interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB).

Figure 44. Hub Interface Routing Example



8.1. Hub Interface Routing Guidelines

This section documents the routing guidelines for the 10-bit hub interface. This hub interface connects the ICH3-M and the MCH-M. The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

The trace impedance must equal 55 Ω ± 15%.

Table 35. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HICOMP Resistor Value	HICOMP Resistor Tied to
ICH3-M	55 ohms ±15%	36.5 Ω ± 1%	VSS
MCH-M	55 ohms ± 15%	36.5 Ω ± 1%	Vcc1_8

8.2. Hub Interface Data Signals

These data signal traces should be routed 4 mils wide with 8 mils trace spacing (4 on8) and 12 mils spacing from other signals. In order to break out of the MCH-M and ICH3-M packages, the hub interface data signals can be routed 5-mils wide 5-mils spacing. The signal must be separated to 5-mils width with 10-mils spacing within 300 mils from the package.

The maximum hub interface data signal trace length is six inches. Each data signal must be matched within ± 200 mils of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

Table 36. Hub Interface Signals

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HUB_PD[10:0]	6	4	8	±200	Differential HUB_PSTRB pair	12	
HUB_PSTRB and HUB_PSTRB#	6	4	8	±200	Data lines	12	HUB_PSTRB and HUB_PSTRB# must be the same length (±10 mils)

8.3. Hub Interface Strobe Signals

The hub interface strobe signals should be routed as a differential pair, 4-mils wide with 8-mils trace spacing (4 on 8) and 12-mils spacing from other signals. This strobe pair should have a minimum of 12 mils spacing from any adjacent signals. The maximum length for the strobe signals is six inches. Each strobe signal must be the same length, and each data signal must be matched to within ± 200 mils of the strobe signals.

8.4. HUBREF Generation/Distribution

HUBREF is the hub interface reference voltage. Depending on the buffer mode, the HUBREF voltage requirement must be set appropriately for proper operation. See the table below for the HUBREF voltage specifications and the associated resistor recommendations for the voltage divider circuit.

Table 37. Hub Interface HUBREF Generation Circuit Specifications

HUBREF Voltage Specification (V)	Recommended Resistor Values for the HUBREF Divider Circuit (Ohm)
½ VCC1_8 ± 4%	R1 = R2 = 301 ± 1%

The single HUBREF divider should not be located more than four inches away from either the MCH-M or ICH3-M. If the single HUBREF divider is located more than four inches away, locally generated hub interface reference dividers should be used instead. The reference voltage generated by a single HUBREF divider should be bypassed to ground with a 0.1-µF capacitor (C1) and at each component with a 0.01-µF capacitor (C2) located close to the component HUBREF pin Figure 45. If the reference voltage is generated locally, the bypass capacitor (0.01 µF) needs to be close to the component HUBREF pin Figure 46.

Figure 45. Single HUBREF Voltage Divider

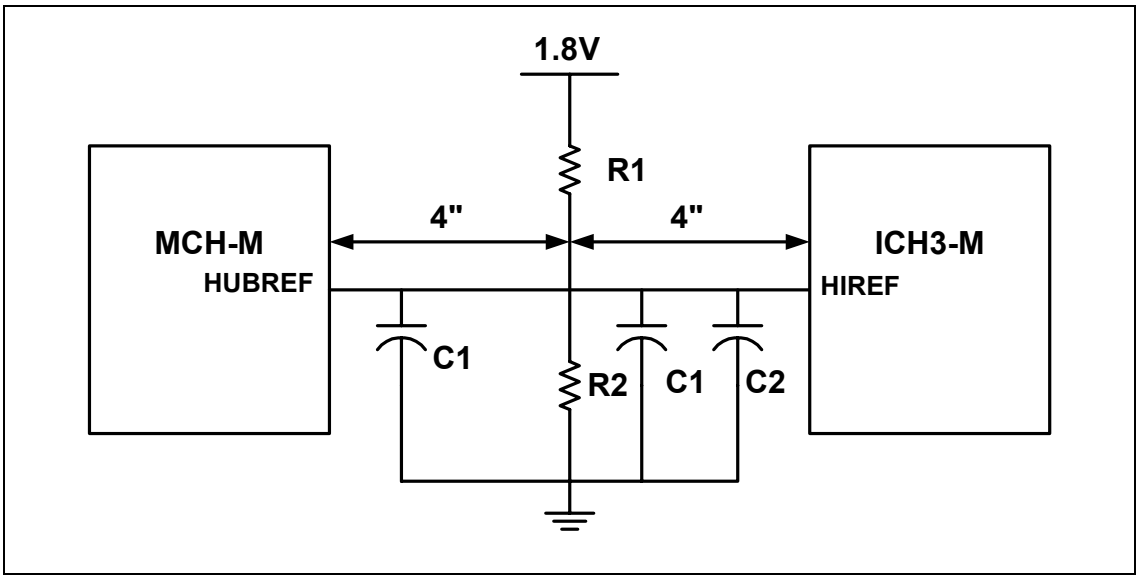
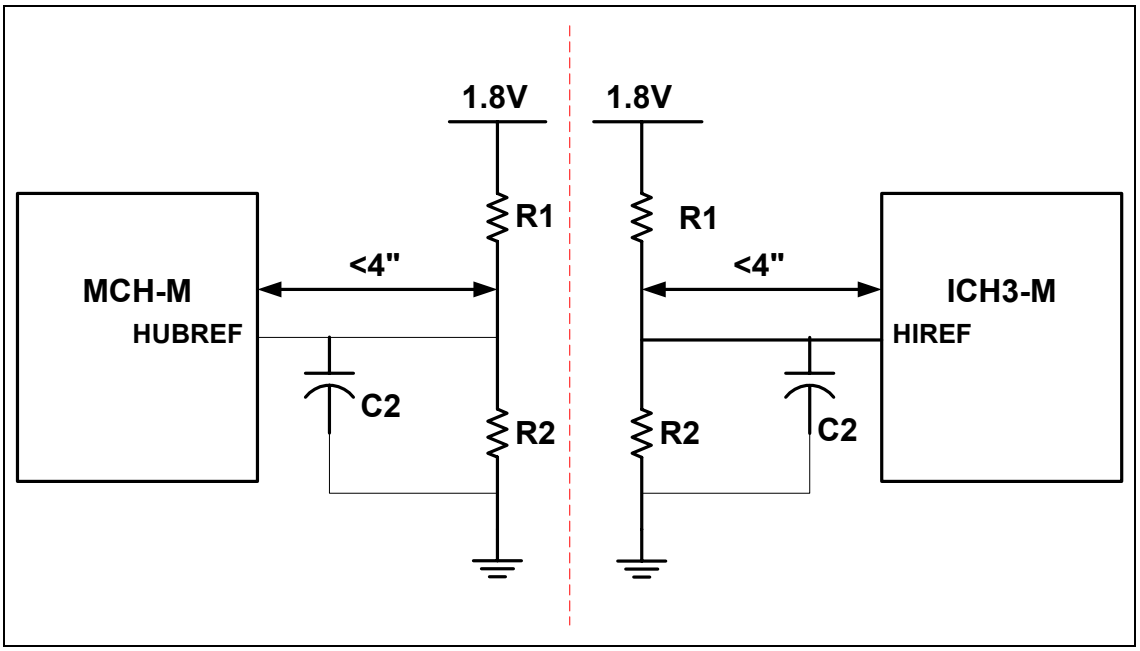


Figure 46. Locally Generated HUBREF Divider



NOTE: There is no C1.

8.5. Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH3-M and MCH-M). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 side of the capacitors to the VCC1_8 power balls. Similarly, if layout allows, metal fingers running on the VCC1_8 side of the board should connect the groundside of the capacitors to the VSS power balls.

9. I/O Subsystem

9.1. IDE Interface

This section contains guidelines for connecting and routing the ICH3-M IDE interface. The ICH3-M has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH3-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Additional series termination resistors may be needed; the designer should verify motherboard signal integrity through simulation. Zero Ohm series resistors can be added into the design as a stuffing option to address possible noise issues on the motherboard.

The IDE interface can be routed with 4-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH3-M to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inches shorter than the longest IDE signal (on that channel). See Table 38.

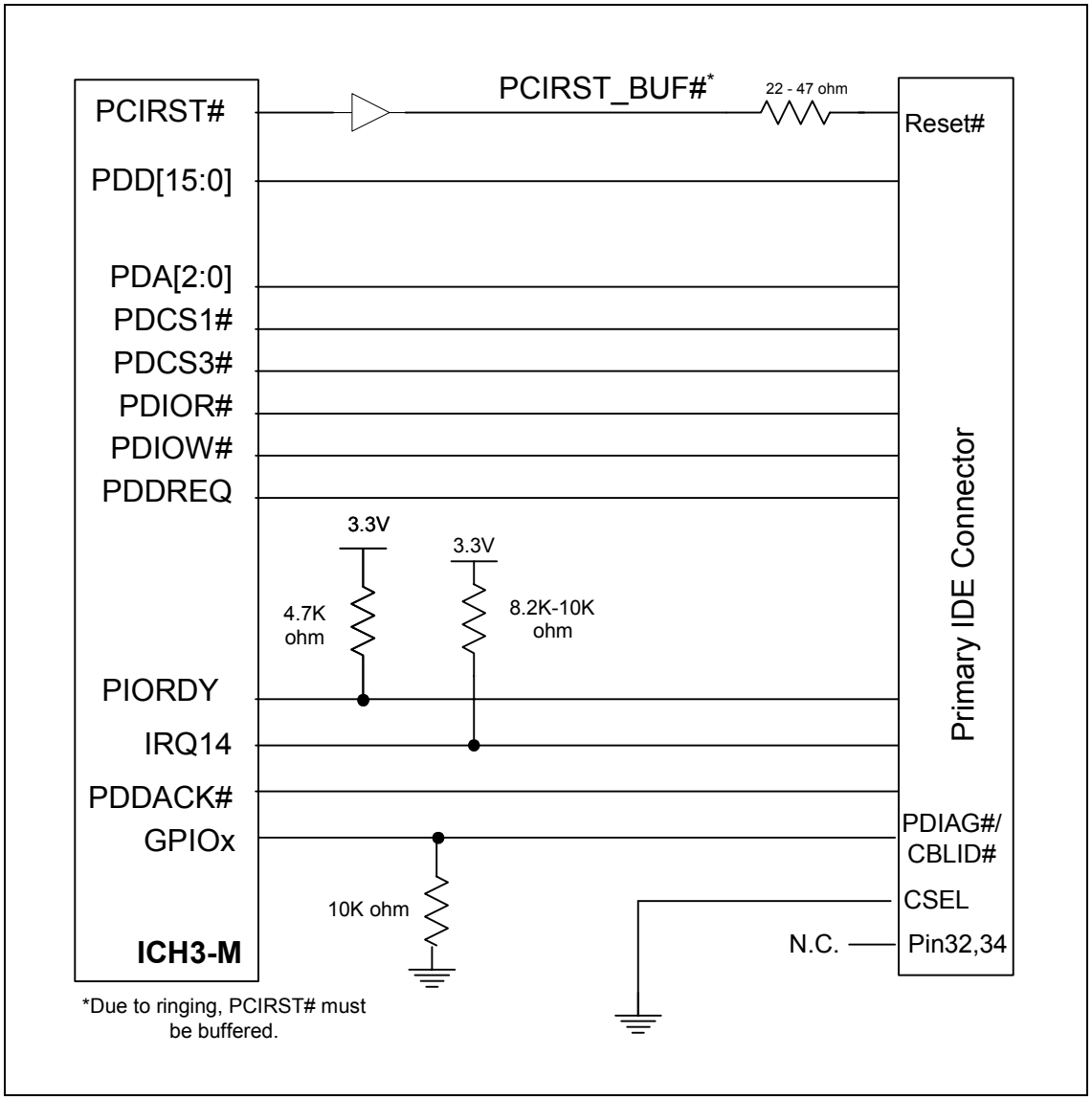
Table 38. IDE Signals

Signal	Max length (inch)	Width (mils)	Space (mils)	Relative Mismatch max length (mils)	Relative To	Space with other signals (mils)
Signal Group#ide1 IDE_PDD[15:0] IDE_SDD[15:0] IDE_PDA2 IDE_PDCS3# IDE_PATADET IDE_SATADET IDE_SEC_RST# IDE_PRI_RST# IDE_PDA0 IDE_PDA1 IDE_PDCS1# IDE_PDDACK# IDE_PDDREQ IDE_PDIOW# IDE_SDA0 IDE_SDA1 IDE_SDA2 IDE_SDCS1#	8	4	7	±250	Shortest and longest IDE signal in same channel	8

Signal	Max length (inch)	Width (mils)	Space (mils)	Relative Mismatch max length (mils)	Relative To	Space with other signals (mils)
IDE_SDCS3# IDE_SDDACK# IDE_SDDREQ IDE_SDIOW#						
Signal Group#ide2 IDE_PIORDY IDE_PDIOR# IDE_SIORDY IDE_SDIOR#	8	4	7	± 5	IDE_PIORDY with IDE_PDIOR# And IDE_SIORDY with IDE_SDIOR#	8
Other signals INT_IRQ1 IDE_PDACTIVE# INT_IRQ15 IDE_SDACTIVE#						

9.1.1. Primary IDE Connector Requirements

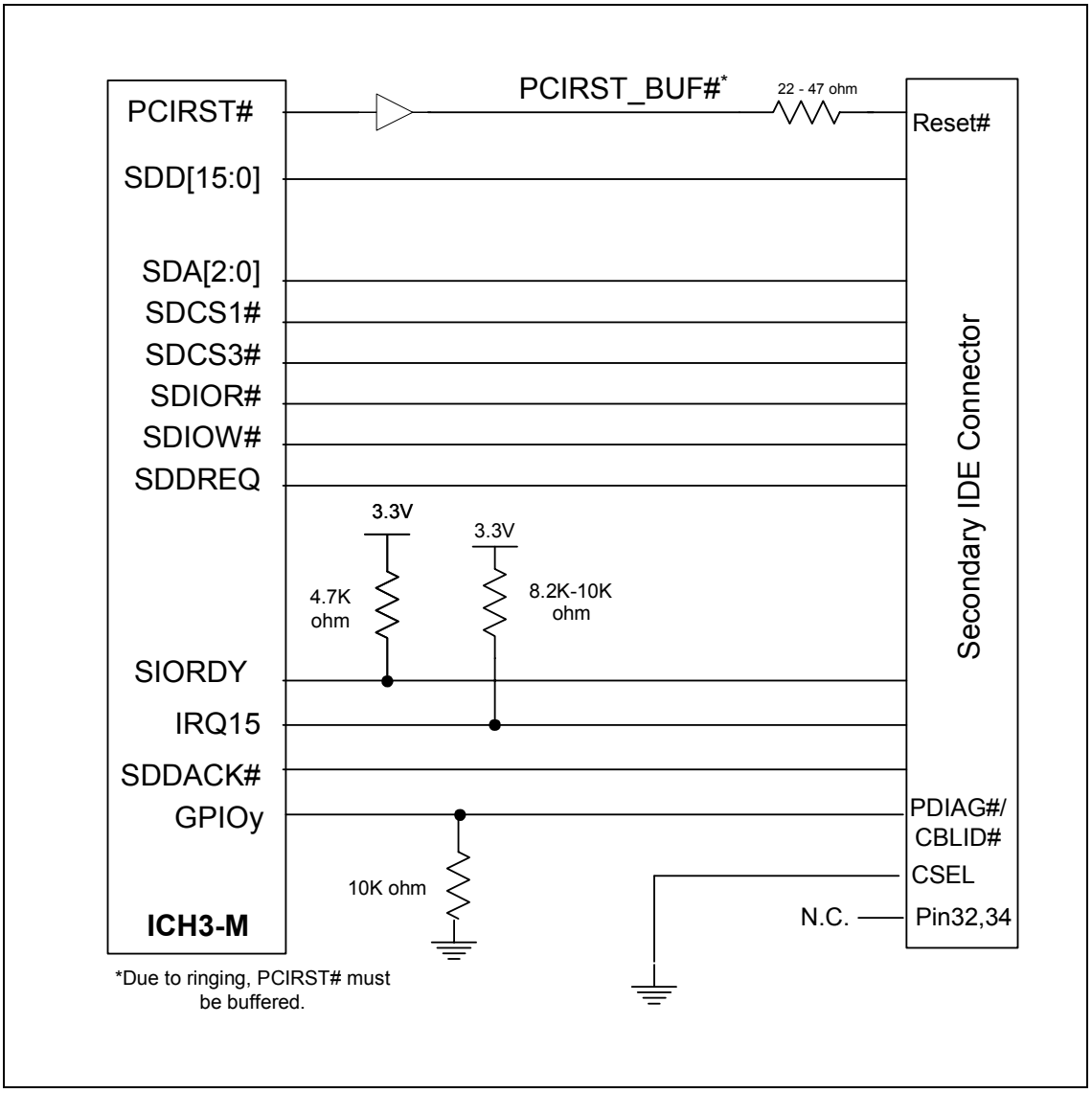
Figure 47. Connection Requirements for Primary IDE Connector



- 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to Vcc3_3.
- A 4.7-kΩ pull-up resistor to Vcc3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- A 10-kΩ pull-down resistor to ground is required on the PDIAG#/CBLID# signal. This is to prevent the GPI pin from floating if a device is not present on the Primary IDE interface.

9.1.2. Secondary IDE Connector Requirements

Figure 48. Connection Requirements for Secondary IDE Connector



- 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to Vcc3_3.
- A 4.7-KΩ pull-up resistor to Vcc3_3 is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

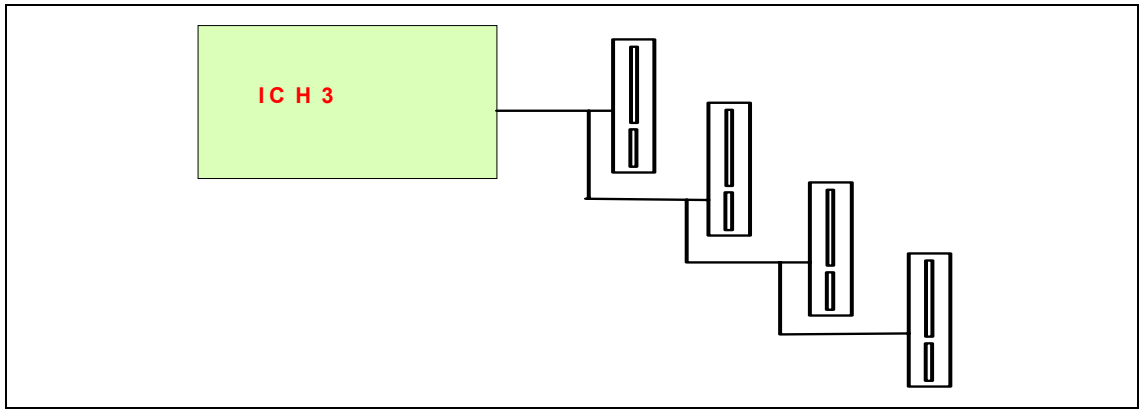
- A 10-kΩ pull-down resistor to ground is on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the Secondary IDE interface.

9.2. PCI

The ICH3-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH3-M is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH3-M supports six PCI Bus masters (excluding the ICH3-M), by providing six REQ#/GNT# pairs. In addition, the ICH3-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 49. PCI Bus Layout Example



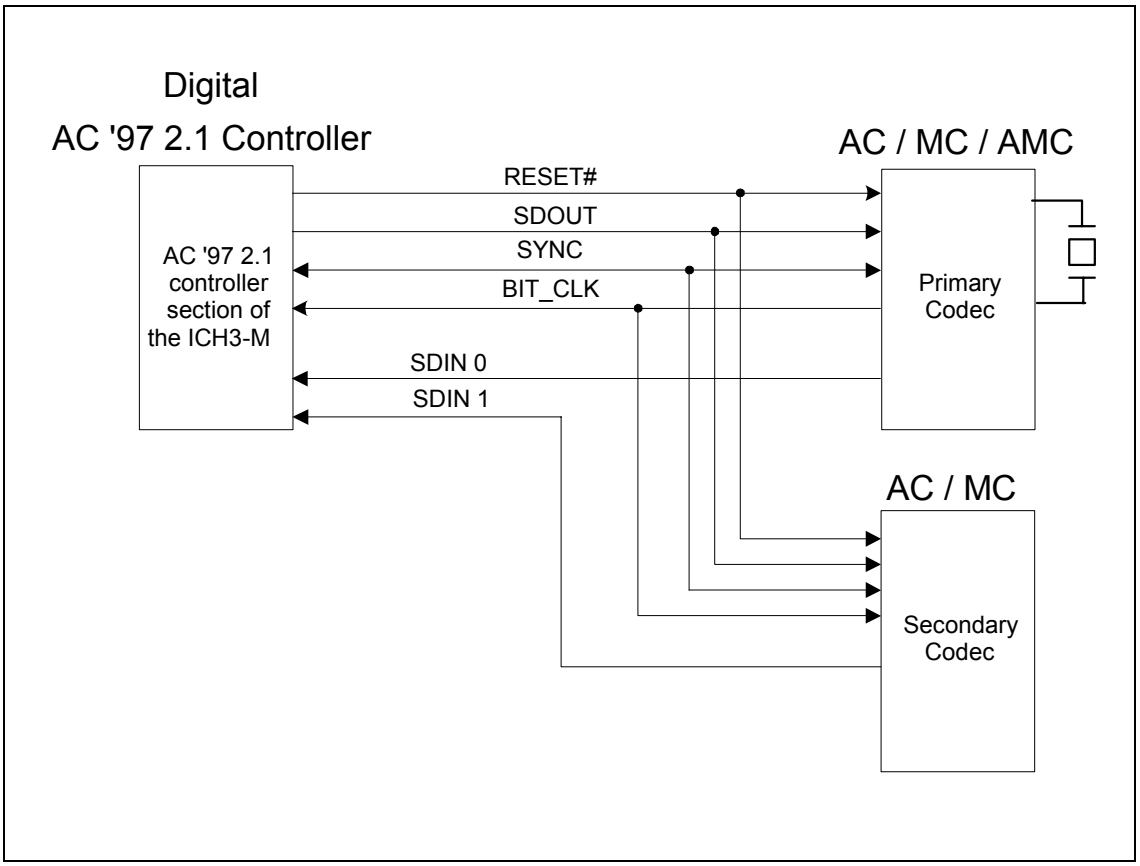
9.3. AC'97

The ICH3-M implements an AC'97 2.1 compliant digital controller. Any Codec attached to the ICH3-M AC-link must be AC'97 2.1 compliant as well. Please contact your Codec IHV for information on 2.1 compliant products. The AC'97 2.1 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH3-M AC-link allows a maximum of two Codecs to be connected. The following figure shows a two-Codec topology of the AC-link for the ICH3-M.

Figure 50. ICH3-M AC'97 – Codec Connection



9.3.1. Four-Layer Layout Example

Using the assumed 4-layer stack-up, the AC'97 interface can be routed using 5-mil traces with 5-mil space between the traces. Maximum length between ICH3-M to CODEC/CNR is 14 inches in a "T" topology. Trace impedance should be $Z_0 = 55\ \Omega \pm 15\%$.

Clocking is provided from the primary Codec on the link via BITCLK, and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary Codec vendor for crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary Codec to the digital controller (ICH3-M), and any other Codec present. That clock is used as the time base for latching and driving data.

The ICH3-M supports wake on ring from S1-S5 via the AC'97 link. The Codec asserts AC_SDINn to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem Codec.

The ICH3-M has weak pull-downs/pull-ups that are only enabled when the AC-Link Shut Off bit in the ICH3-M is set or if both function 5 and function 6 of device 31 are disabled (hidden). This will keep the link from floating when the AC-link is off, or there are no Codecs present.

If the Shut-off bit is not set, or if neither function 5 nor function 6 of device 31 are disabled (hidden), it implies that there is a Codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the Codec and ICH3-M respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

9.3.2. AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different Codec configurations. Please refer to Intel's White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser) for Intel's recommended Codec configurations (available at the URL given in Section 9.3).

To support more than two channels of audio output, the ICH3-M allows for a configuration where two audio Codecs work concurrently to provide surround sound capabilities. To maintain data-on-demand capabilities, the ICH3-M AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached Codecs. It is assumed that both Codecs will be programmed to the same sample rate and that the Codecs have identical (or at least compatible) FIFO depth requirements. Intel recommends that the Codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

9.3.3. Valid Codec Configurations

Table 39. Codec Configurations

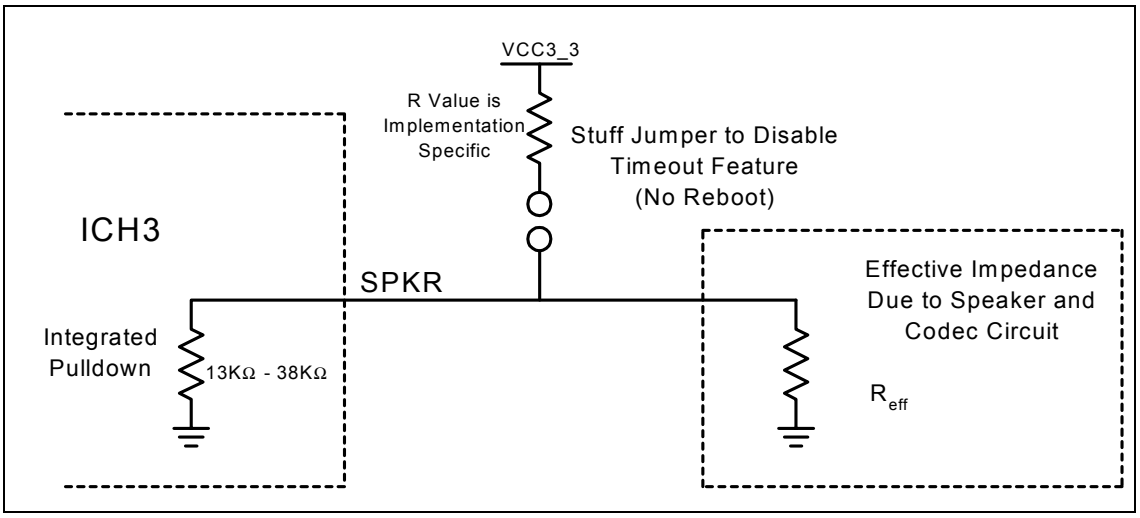
Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of Codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

9.3.4. SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH3-M sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see the following figure). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH3-M's integrated pull-down resistor will be read as logic high (0.5 Vcc3_3 to Vcc3_3 + 0.5 V).

Figure 51. Example Speaker Circuit



9.3.5. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.

- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary Codec on the link via BITCLK, and it is derived from a 24.576-MHz crystal or oscillator. Refer to the primary Codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary Codec to the digital controller (ICH3-M) and by any other Codec present. The clock is used as the time base for latching and driving data.

9.3.6. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH3-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH3-M platform.

- Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH3-M supports wake-on-ring from S1-S5 states via the AC'97 link. The Codec asserts AC_SDIN*n* to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no Codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.4. USB Guidelines and Recommendations

9.4.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth plane closest to the ground plane, and allowing a higher component density on the first plane. For mobile motherboards, with different stackup, all USB signals should be ground referenced when using the appropriate layer for routing.

- Place the ICH3-M and major components on the unrouted board first. With minimum trace lengths, route high-speed clock, periodic signals and USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pairs and any connector leaving the PCB (i.e. I/O connectors, control and signal headers, or power connectors).

- USB signals should be ground referenced.
- Route USB signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
- Stubs on USB signals should be avoided, as stubs have an effect on signal quality. If a stub is necessary in the design, no stub should be greater than 200 mils.
- Route all traces over continuous planes, (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. This increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
- Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.
- Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

9.4.2. USB Trace Separation

Use the following separation guidelines.

- Recommended trace width and separation is 4-mil trace with a 6-mil space (90-Ω differential impedance).

The goal is to have a 90-Ω differential impedance and the spacing may need to be different depending on the stackup.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90-Ω differential impedance.
- Use at a minimum 20-mil spacing between USB signal pair and other traces on the PCB. This helps to prevent crosstalk. If possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk.

9.4.3. USB Trace Length Matching

Use the following trace length matching guidelines.

- USB signal pair traces should be trace length matched.

Table 40. USB Signals

Signal	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
USB Signals Group USB_PN0 to USB_PN5 USB_PP0 to USB_PP5	4	6	± 75	Signal differential pair	20	Clock and PCI should be 50 mils away from USB signals (min)

9.4.4. Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

9.4.4.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This can be true of USB signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them.
- Avoid routing of USB signals 50-mil of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

9.4.4.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guideline for the GND plane.

- Avoid anti-etch on the GND plane.

9.4.4.3. EMI Recommendation

Recommended a 45-pF capacitor for each data line for its USB EMI solution.

9.5. IOAPIC (I/O Advanced Programmable Interrupt Controller)

Intel 845MP/845MZ platform does not support IOAPIC when C2/C3/C4 states are enabled.

Mobile Systems not using the IOAPIC should disable IOAPIC functionality through the system BIOS.

9.5.1. IOAPIC Disabling Options

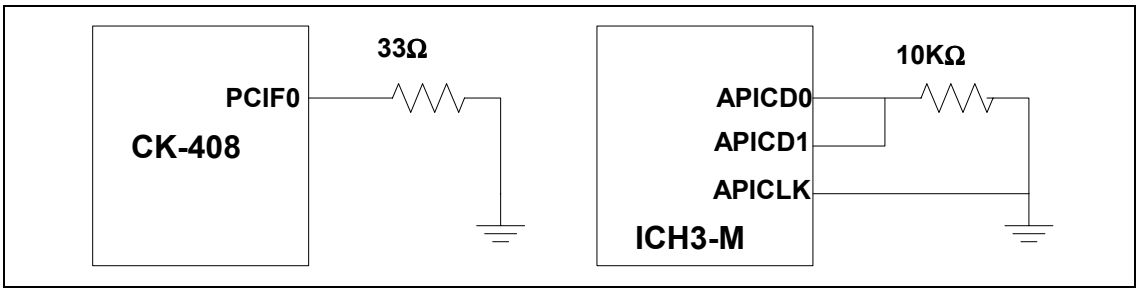
9.5.1.1. Recommended Implementation

Intel recommends that IOAPIC be disabled in software while the connections to the board are as shown in Figure 52. Software can be used to turn off PICCLK from clock generator.

To disable IOAPIC in BIOS:

- ICH3-M: D31:F0; Offset: D1; bit 0 (0=disable);
- Mobile Pentium 4 Processor-M: MSR 1Bh bit 11 (0 = disable)

Figure 52. Minimum IOAPIC Disable Topology



9.5.2. PIRQ Routing Example

PCI interrupt request signals E-H are new to the ICH3-M. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, a system can be designed to minimize sharing of PCI interrupt request lines.

Due to different system configurations, IRQ line routing to the PCI slots ("swizzling") should be made to minimize the sharing of interrupts between both internal ICH3-M functions and PCI functions. The figure below shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

Figure 53. Example PIRQ Routing

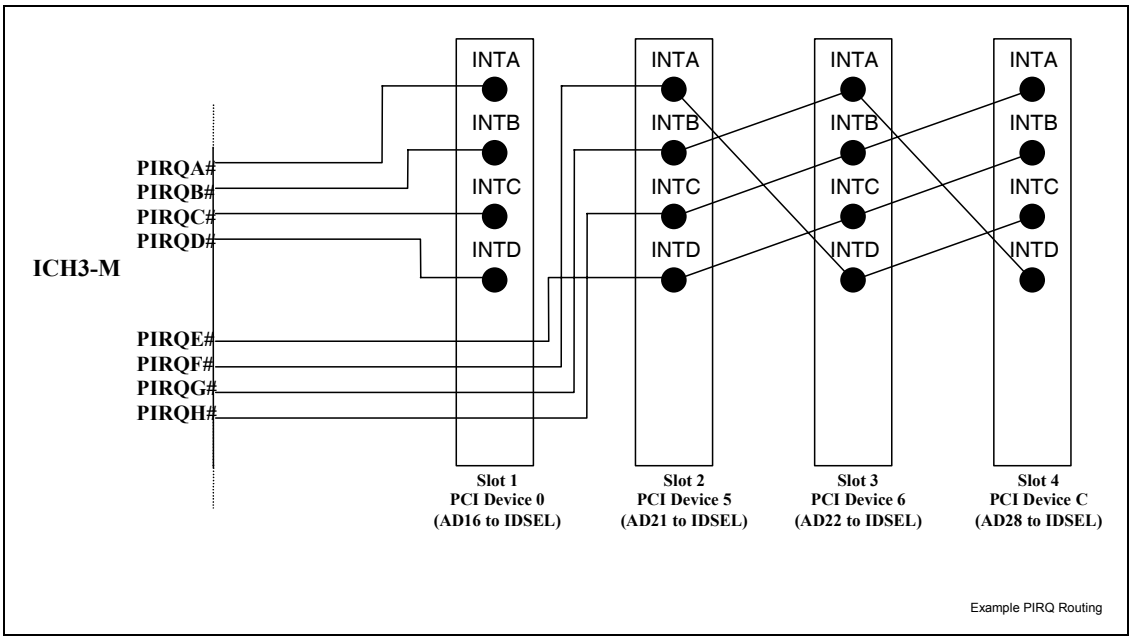


Figure 53 is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH3-M's internal device/functions (but at a higher latency cost).

9.6. SMBus 2.0/SMLink Interface

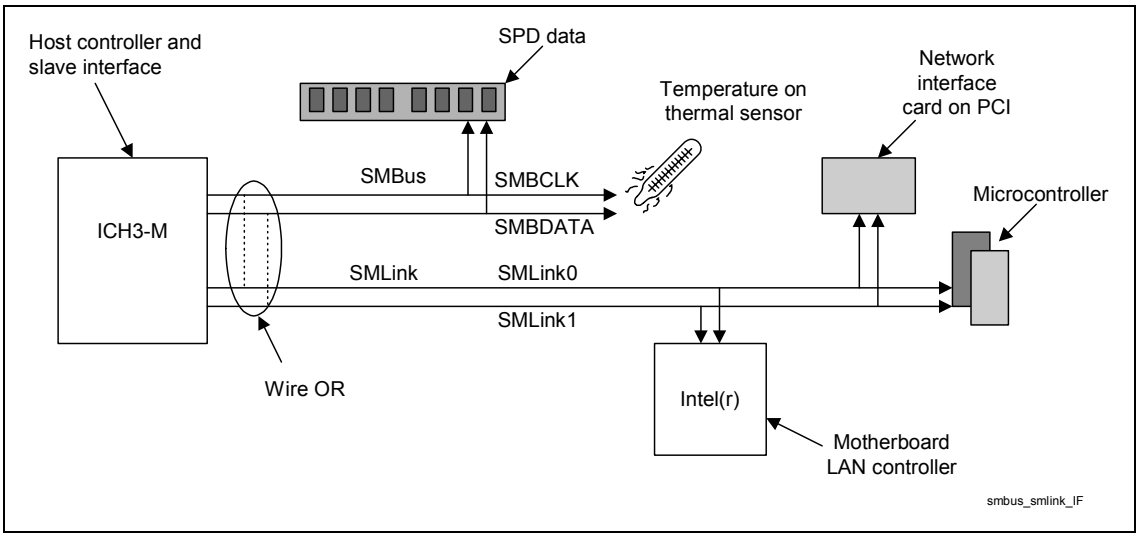
The SMBus interface on the ICH3-M is the same as that on the ICH2-M. It uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH3-M. If the SMBus is used only for the RAMBUS SPD EEPROMs (one on each RIMM*), both signals should be pulled up with a 4.7-kΩ resistor to 3.3 V.

The ICH3-M incorporates a SMLink interface supporting AOL*, AOL2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* (AOL*) functionality, the ICH3-M transmits heartbeat and event messages over the interface. When using the 82562EM Platform LAN Connect Component, the ICH3-M's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, AOL2*-enabled LAN Controller (i.e. Gamla) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH3-M SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (such as Gamla) to access targets on the SMBus as well as the ICH3-M Slave interface. Additionally, the ICH3-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

Figure 54. SMBUS 2.0/SMLink Interface



NOTE: Intel does not support external access of the ICH3-M's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH3-M's SMBus Slave Interface by the ICH3-M's SMBus Host Controller.

9.6.1. SMBus Architecture and Design Considerations

9.6.1.1. SMBus Design Considerations

There are several possibilities for designing an SMBus using the ICH3-M. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where either Vcc_Core or Vcc_Suspend powers all devices, and a mixed design where some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on the following:

- Are there devices that must run in STR?
- Amount of Vcc_Suspend current available, i.e. minimizing load of Vcc_Suspend.

9.6.1.2. General Design Issues/Notes

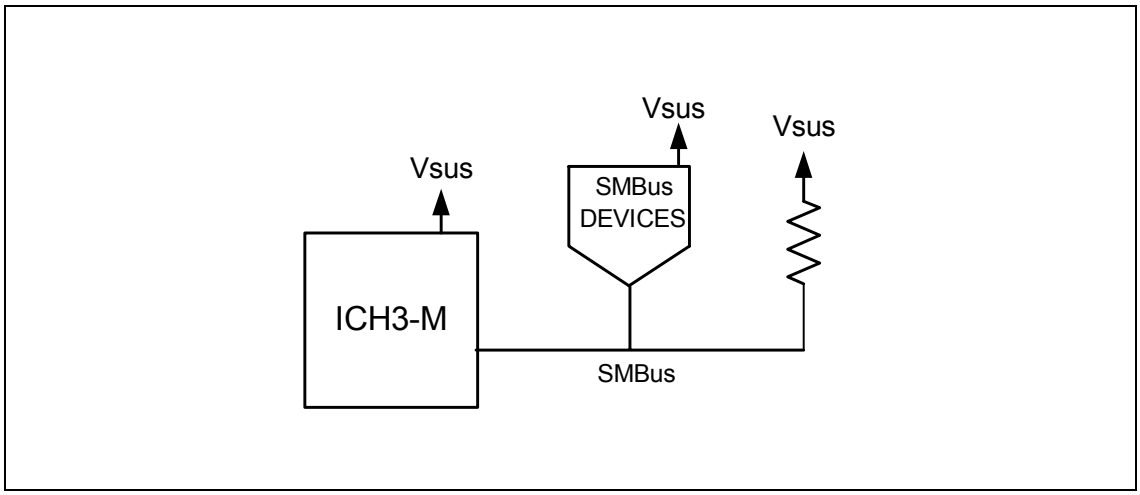
Regardless of the architecture used, there are some general considerations.

The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 KΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH3-M and other devices.

9.6.1.3. The Unified Vcc_ Suspend Architecture

In this design all SMBus devices are powered by the Vcc_Suspend supply. Consideration must be made to provide enough Vcc_Suspend current while in STR.

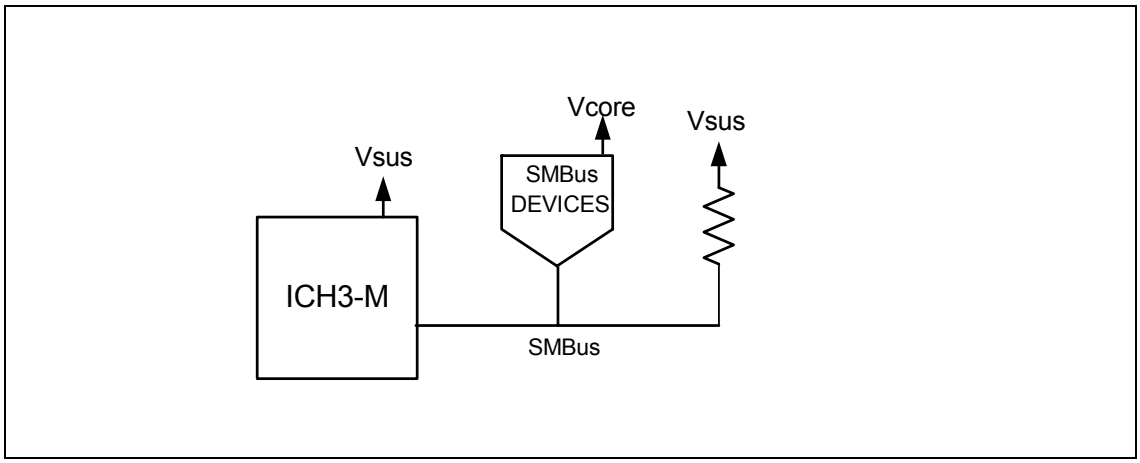
Figure 55. Unified Vcc_Suspend Architecture



9.6.1.4. The Unified Vcc_Core Architecture

In this design, all SMBUS devices are powered by the Vcc_Core supply. This architecture allows none of the devices to operate in STR, but minimizes the load on Vcc_Suspend.

Figure 56. Unified Vcc_Core Architecture

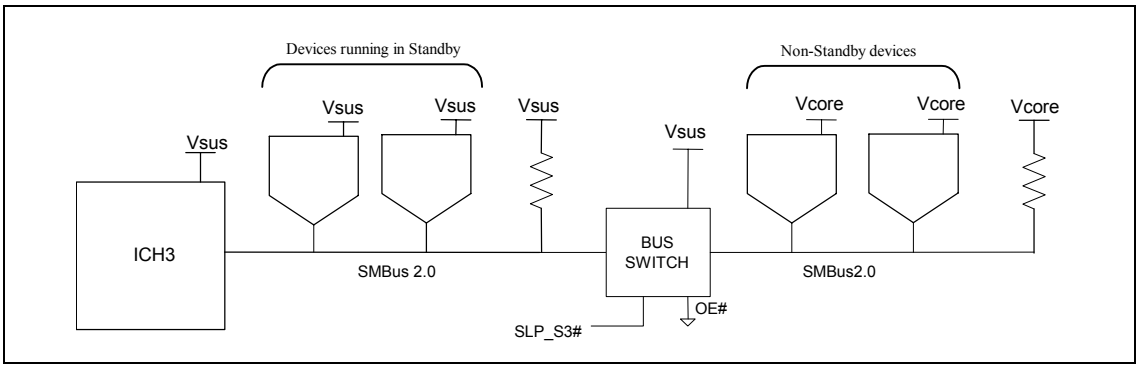


NOTES:
1. The SMBus device needs to be back-drive safe while its supply (Vcore) is off and Vcc_Suspend is still powered.
2. In suspended modes where Vcc_Core is OFF & Vcc_Suspend is on, the Vcc_Core node will be very near ground. In this case the input leakage of the ICH3-M will be approximately 10 µA.

9.6.1.5. Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes Vcc_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies.

Figure 57. Mixed Vcc_Suspend/Vcc_Core Architecture



Added Considerations for Mixed Architecture:

- The bus switch must be powered by Vcc_Suspend
- If there are 5-V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3-V signal levels.
- Devices that are powered by the Vcc_Suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

9.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent (contact your Field Representative for more information).

9.7.1. FWH Decoupling

A 0.1-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

9.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH3-M hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH3-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from of a PCI card that positively decodes these memory cycles (In order to boot off a PCI card it is necessary to keep the ICH3-M in subtractive decode mode). If a PCI boot card is inserted and the ICH3-M is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB. Once booted from the PCI card, you could potentially program the FWH in circuit and program the ICH3-M CMOS.

9.8. FWH Signaling Voltage Compatibility

Depending on the V_CPU_IO of the processor and the manufacturer of the FWH, there may be signaling voltage compatibility issues with the ICH3-M. The range of acceptable V_CPU_IO for the ICH3-M is 1.2 V to 2.5 V. If the processor core voltage is not within this range, translation logic will be required on the processor side before even considering the FWH.

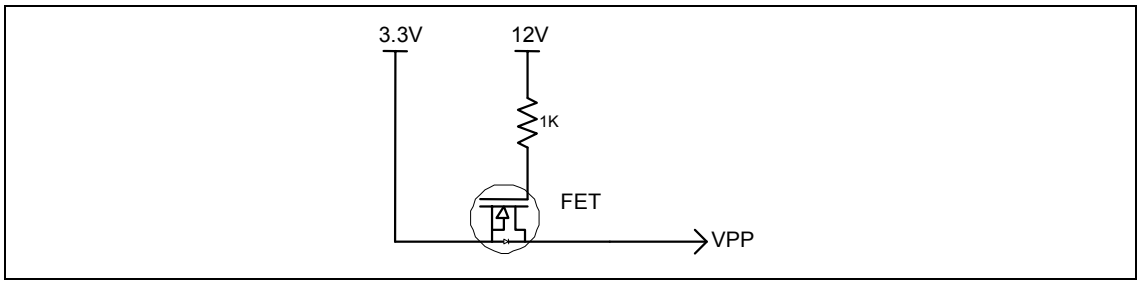
Furthermore, the FWH INIT signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT signal is active low. Therefore, the inactive state of the ICH3-M INIT signal needs to be at a value slightly higher than the V_{IH} min FWH INIT pin specification. The ICH3-M inactive state of this signal is governed by the formula V_CPU_IO - 0.13 V. Therefore if the V_CPU_IO of the processor is 1.5 V and the V_{IH} min spec of the FWH INIT input signal is 1.35 V, there would be no compatibility issue because 1.5 V - 0.13 V = 1.37 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.4 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into account noise that may be encountered on INIT. Care must be taken to ensure that the VIM min specification is met with ample noise margin.

9.8.1. FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports Vpp of 3.3 V or 1 2 V. If Vpp is 12 V the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V Vpp for 80 hours. The 12V Vpp would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 58. FWH VPP Isolation Circuitry



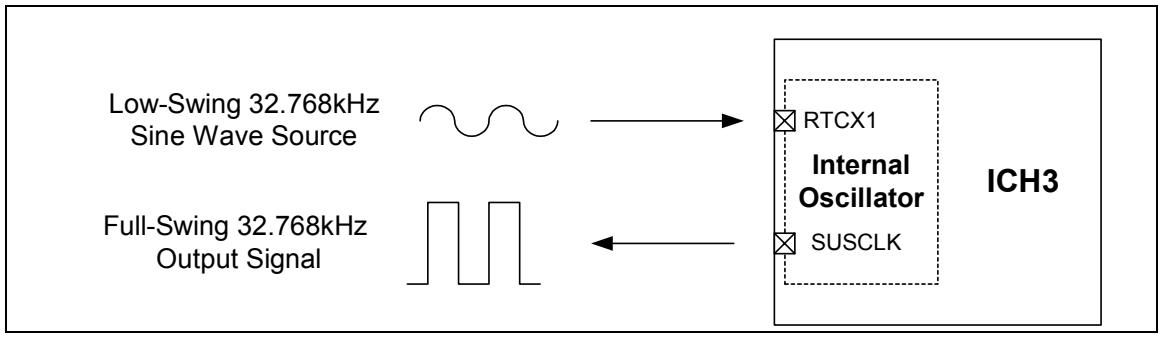
9.9. RTC

The ICH3-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH3-M uses a crystal circuit to generate a low-swing, 32-kHz,input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH3-M, the

RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICHn is called SUSCLK. This is illustrated in Figure 59.

Figure 59. RTCX1 and SUSCLK Relationship in ICH3-M



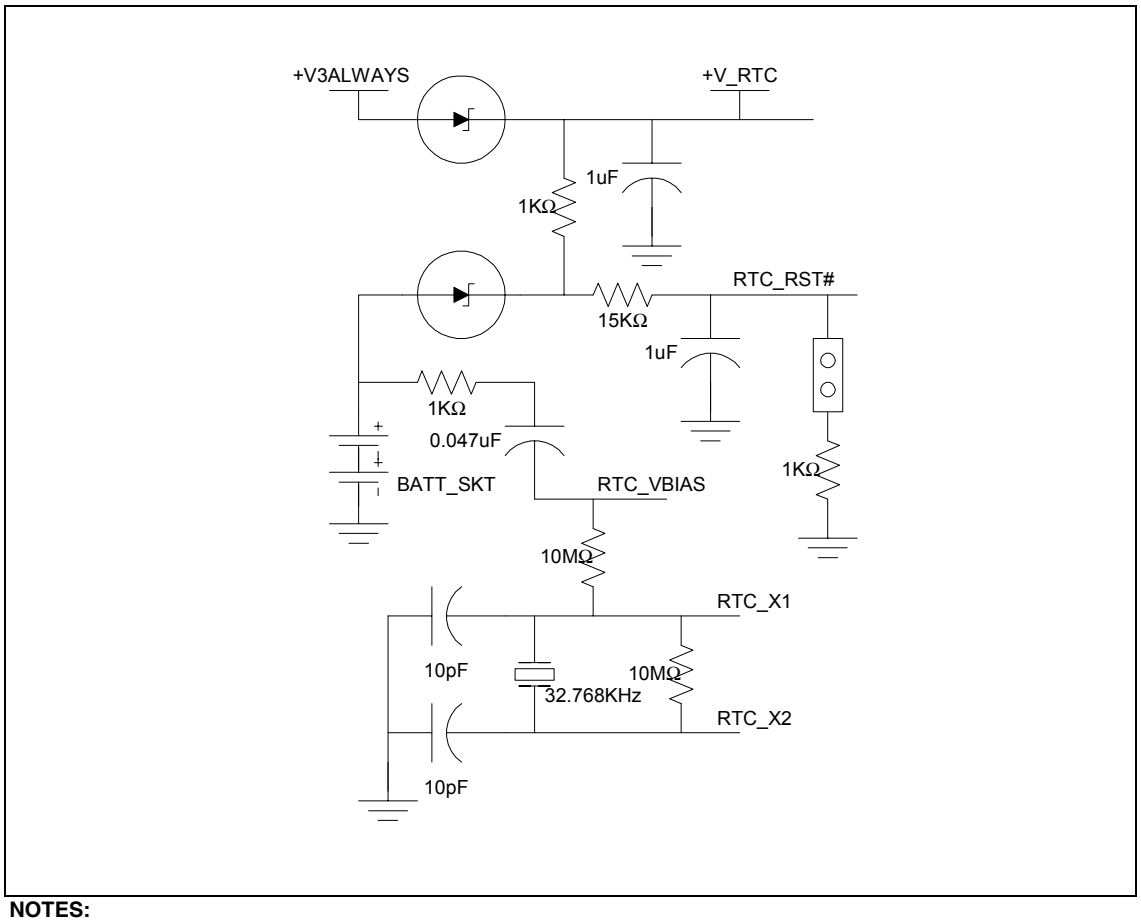
For further information on the RTC, please consult Application Note *AP-728 ICH/ICH2/ICH2M/ICH3S/ICH3M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*.

This section will present the recommended hookup for the RTC circuit for the ICH3-M.

9.9.1. RTC Crystal

The ICH3-M RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. The following figure documents the external circuitry that comprises the oscillator of the ICH3-M RTC.

Figure 60. External Circuitry for the ICH3-M RTC

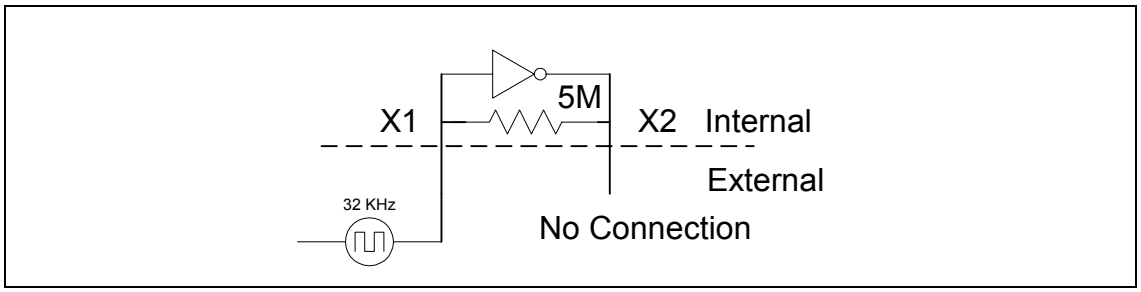


NOTES:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C2 and C3 are 18 pF.)
2. V_{CCRTC}: Power for RTC Well.
3. RTCX2: Feedback for the external crystal.
4. RTCX1: Input to the internal oscillator.
5. V_{BIAS}: RTC BIAS Voltage – This ball is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.

Note: Even if the ICH3-M internal RTC is not used, it is still necessary to supply clock inputs to X1 and X2 of the ICH3-M because other signals are gated off that clock in suspend modes. However, in this case, the frequency (32.768 kHz) of the clock inputs is not critical; a lower-cost crystal can be used or a single clock input can be driven into X1 with X2 left as no connect; Figure 61 illustrates this. **This is not a validated configuration with ICH3-M.**

Figure 61. RTC Connections When Not Using Internal RTC



9.9.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C3 needs to be 0.047 µF, and the capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package.

The following equation can be used to choose the external capacitance values:

Equation 2. RTC External Capacitor Equation

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

C_{load} = Crystal's load capacitance. This value can be obtained from crystal's specification.

C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH3-M. These values can be obtained in the ICH3-M's datasheet.

C_{trace1}, C_{trace2} = Trace length capacitances measured from crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value is approximately equal to:
C_{trace} = trace length * 2 pF / inch (dependent upon board characteristics)

$C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

Example 1:

According to a required 12-pF load capacitance of a typical crystal that is used with the ICH3-M, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25^0 C) to yield a 32.768-kHz oscillation.

At 0^0 C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25^0 C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1 , C_2 are chosen to be 6.8 pF instead of 10 pF. This will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0°C. The 6.8-pF value of C1 and C2 is the **practical value**.

Note that the temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0°C (25° below room temperature) is the same when operating at 50°C (25°C above room temperature).

9.9.3. RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Don't route switching signals under the external components (unless on the other side of the board).
- The oscillator Vcc should be clean; use a filter, such as an RC lowpass, or a ferrite inductor.

9.9.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH3-M is not powered by the system.

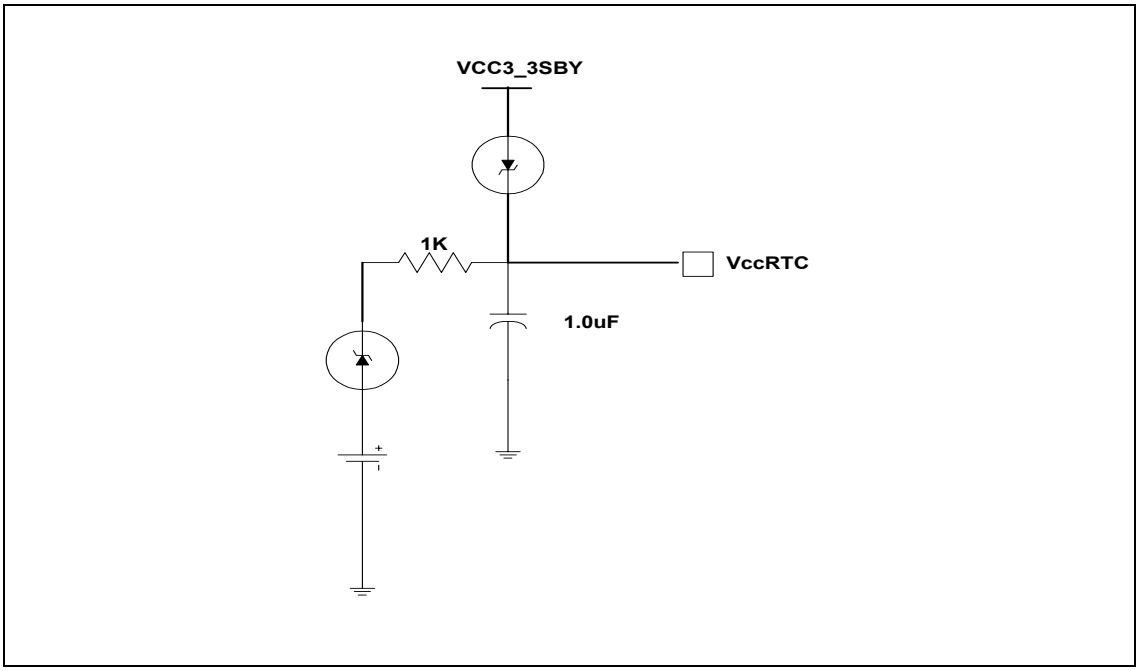
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

Equation 3. RTC External Battery Life Equation

170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. . The battery voltage of the RTC must be greater than 2V at all time to ensure the accuracy of the RTC clock. The battery must be connected to the ICH3-M via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH3-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. The following figure is an example of a diode circuit that is used.

Figure 62. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.9.5. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Don't route any switching signals under the external components (unless on the other side of the ground plane).

9.9.6. VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 60) therefore it is self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200-mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note that VBIAS is also very sensitive to environmental conditions.

9.9.7. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50-Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH3-M's RTC Clock (see Application Note AP-728 for further details).

9.9.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER# and PWROK) must be either pulled up to V_{CC}RTC or pulled down to ground while in G3 state. RTCRST# when configured meets this requirement. RSMRST# should have a weak external pull-down (8-22 KΩ) to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down of 8-22 KΩ. The details are shown in the figure below. The arrows in bold indicate the leakage paths if appropriate pull-ups and pull-downs are not present.

9.10. Internal LAN Layout Guidelines

The ICH3-M provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 41. Integrated LAN Capability

Platform LAN Connect component	Connection	Features
82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection
82562EH	1 Mb HomePNA* LAN	1 Mb HomePNA* connection

Intel developed a dual footprint for 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate Platform LAN Connect component to meet the market need.

Figure 63. ICH3-M/LAN Connect Section (Dual Footprint Option)

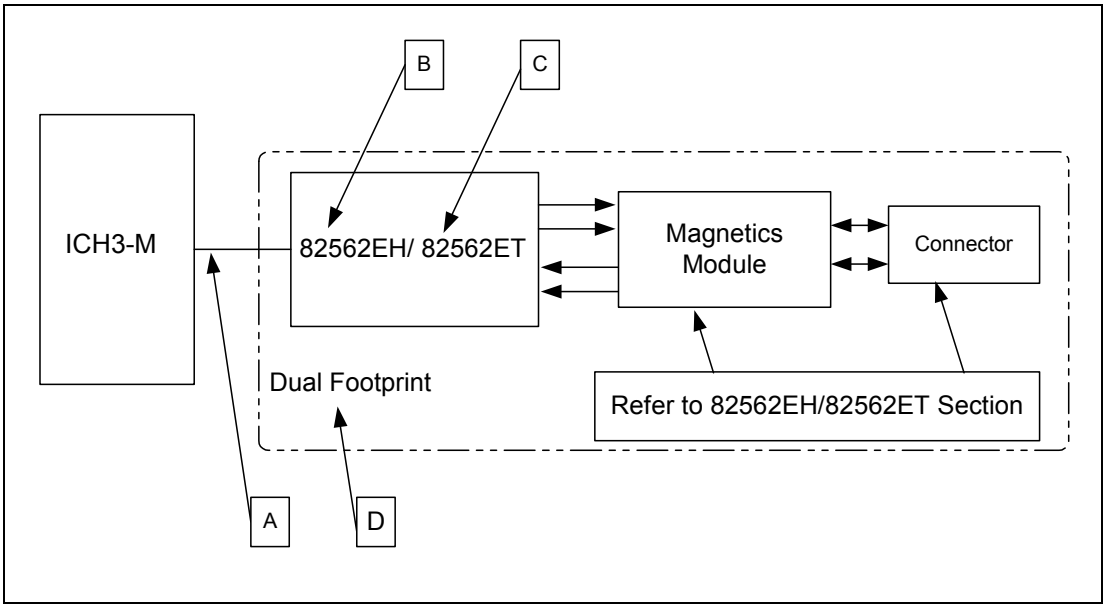


Table 42. LAN Design Guide Section Reference

Layout Section	Figure 13-22 Reference	Design Guide Section
ICH3-M – LAN Interconnect	A	ICH3-M – LAN Interconnect Guidelines
General Routing Guidelines	B,C,D	
82562EH	B	
82562ET /82562EM	C	
Dual Layout Footprint	D	

9.10.1. ICH3-M – LAN Interconnect Guidelines

This section contains guidelines to the design of motherboards and riser cards to comply with LAN Connect. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH3-M to LAN component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed. Dual footprint guidelines are found in Figure 63.

Bus Topologies

The LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH3-M and the LAN component
- Dual Footprint
- LOM/CNR Implementation

9.10.1.1. Point-to-point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EH, 82562ET, or CNR is installed.

Figure 64. Single Solution Interconnect

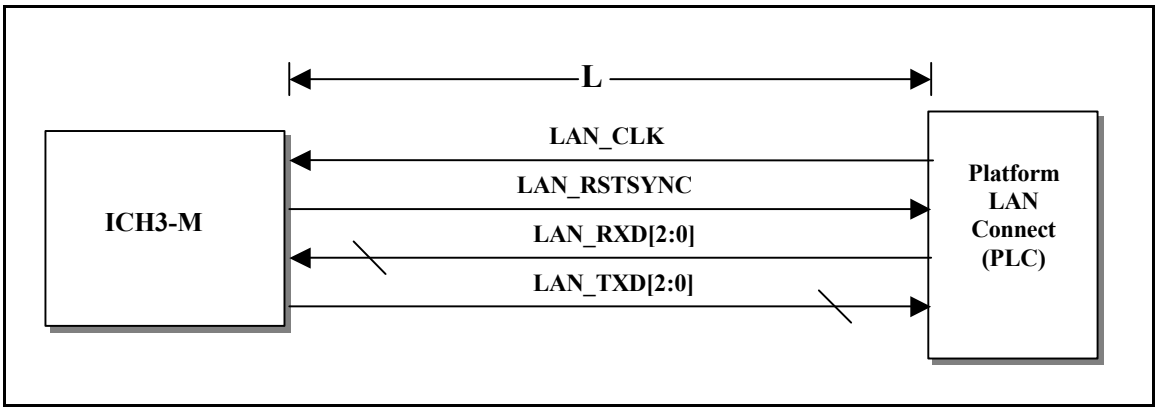


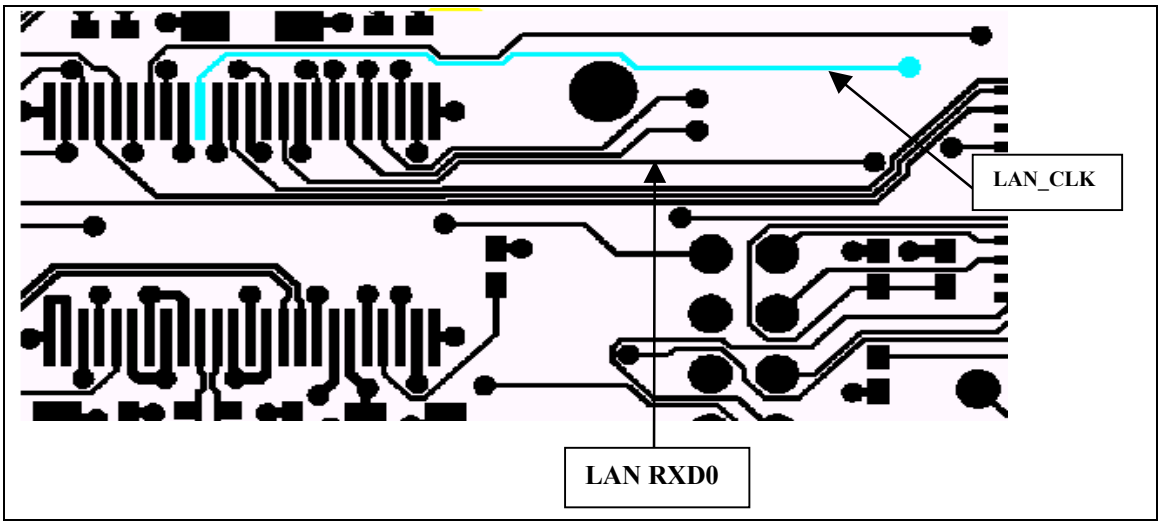
Table 43. LAN Design Guide Point-to-Point Length Requirements

Length Requirements From the Previous Figure	
Configuration:	A
82562EH	L = 4.5” to 10” (Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] not connected)
82562ET	L = 3.5” to 10”
CNR	L = 3” to 9” (0.5” to 3” on card)

9.10.1.2. Signal Routing and Layout

LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 65. LAN_CLK Routing Example



9.10.1.3. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

9.10.1.4. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the daughtercard. An impedance of 60 Ω ±10% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.10.1.5. Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33-Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.10.2. General LAN Routing Guidelines and Considerations

9.10.2.1. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.5-mil stackup.

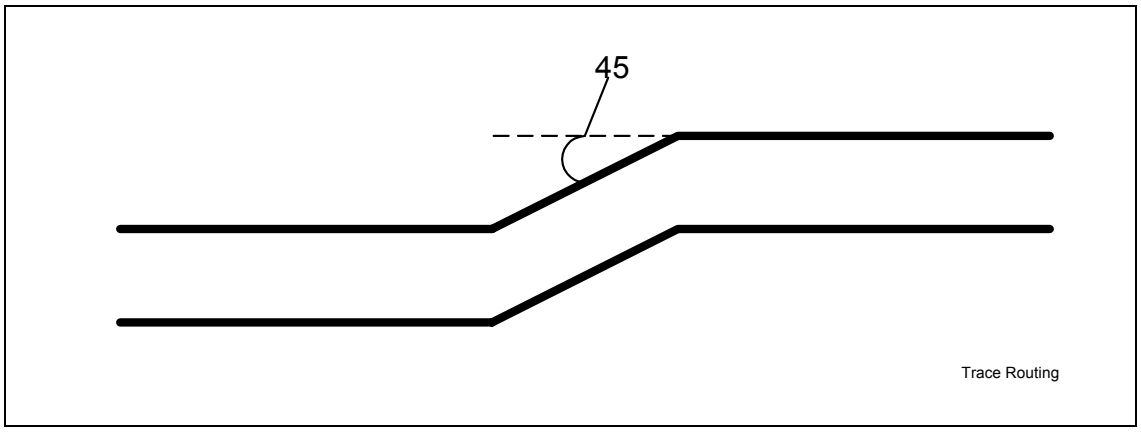
- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inches (clock trace must be longest). See Table 44 below for summary of recommendations
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, Intel recommends using two 45° bends instead.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Table 44. LAN Signals

Signal	Max length (inch)	Width (mils)	Space btwn diff pair (mils)	Space btwn trans. recv. diff pair or other signals(mils)	Mismatch relative max. (mils)	Relative To	Notes
Signals Group#lan1 LAN_RXD0 to LAN_RXD2 LAN_TXD0 to LAN_TXD2 LAN_RST	10 (min 3.5)	4	*4	8	-500	LAN_JCLK	Diff. Pair must be the same length (±10 mils)
Signals Group#lan2 TDP (pin9, J23A) TDN (pin10, J23A) LAN_RDP LAN_RDN LAN_JCL	4	4	7	100	+/-10	Signals Group#lan2 diff pair	Diff. Pair must be the same length (±10 mils)
LAN_JCLK	10 (min 3.5)	4	none	16	+500	Signals Group#lan1	LAN_JCLK is equal to Signals Group#lan 1 or longer by 500 mil (max)

NOTE: *This parameter is not for diff pairs, it is the space between datalines.

Figure 66. Trace Routing



9.10.2.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers

are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 ohms. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 ohms, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetic/edge of the board.

9.10.2.1.2. Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phone line and Ethernet) and other nets, but group associated differential pairs together.

  NOTE: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize cross talk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

9.10.2.2. Power and Ground Connections

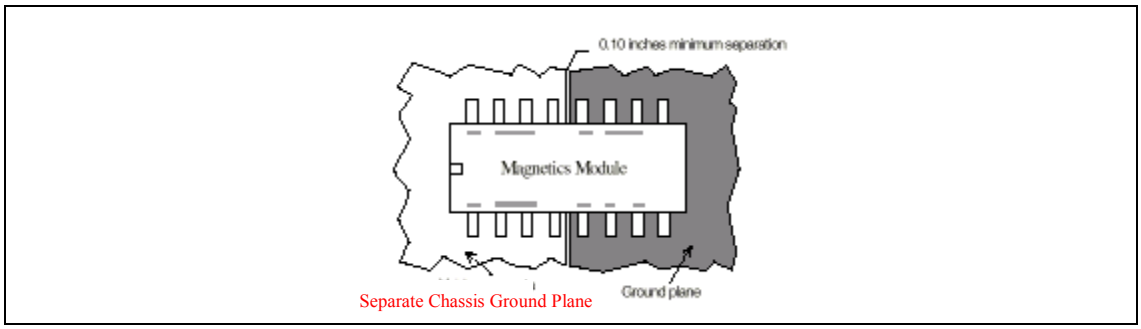
Some rules and guidelines to follow for power and ground connections:

- All Vcc pins should be connected to the same power supply.
- All Vss pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended
- Place decoupling as close as possible to power pins.

9.10.2.2.1. General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetic module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 67. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetic module.
- Create a spark gap between pins 2 through 5 of the Phone line connector(s) and shield ground of 1.6 mm (59.0 mil). This is a **critical** requirement needed to past FCC part 68 testing for phone line connection. Note: For worldwide certification, a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6 mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5-mm spacing.

9.10.2.3. A Four-Layer Board Design (Example)

9.10.2.3.1. Top Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

9.10.2.3.2. Ground Plane

A layout split (100 mils) of the ground plane under the magnetic module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

9.10.2.3.3. Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill "island", separated from digital power, RC filtered from the digital power.

9.10.2.3.4. Bottom Layer Routing

The digital high-speed signals that include all of the LAN interconnect interface signals are routed on the bottom layer.

9.10.2.4. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetic or between the magnetic and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetic should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetic, the RJ-45/11, and the PLC.
- Use of an inferior magnetic module. The magnetic modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetic modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)

- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Please follow the appropriate reference schematic or Ap-Note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetic modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Ap-Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetic center-taps.
- Incorrect differential trace impedances. It is important to have ~100 ohms impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 ohms and 85 ohms, even when the designers think they've designed for 100 ohms. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 ohms. A 10-ohm to 15-ohm drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetic) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. [6 pF to 12-pF values have been used on past designs with reasonably good success.] These caps are not necessary, unless there is some overshoot in 100-Mbps mode.

It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.

† Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.10.3. 82562EH Home/PNA* Guidelines

9.10.3.1. Related Docs

- *82562EH HomePNA* 1 Mb/s Physical Layer Interface – Product Preview Datasheet*
- *RS-82562EH 1Mb/s Home PNA LAN Connect Option Application Note*

Both of the above documents are available at:
http://developer.intel.com/design/network/home/82562eh.htm

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.10.2. Additional guidelines for implementing an 82562EH Home/PNA* Platform LAN Connect component are provided below.

9.10.3.2. Power and Ground Connections

Some rules to follow for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.
- The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS, and VCCA, and VSSA power supplies.

9.10.3.3. Guidelines for 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA* LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA* LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.10.3.4. Crystals and Oscillators

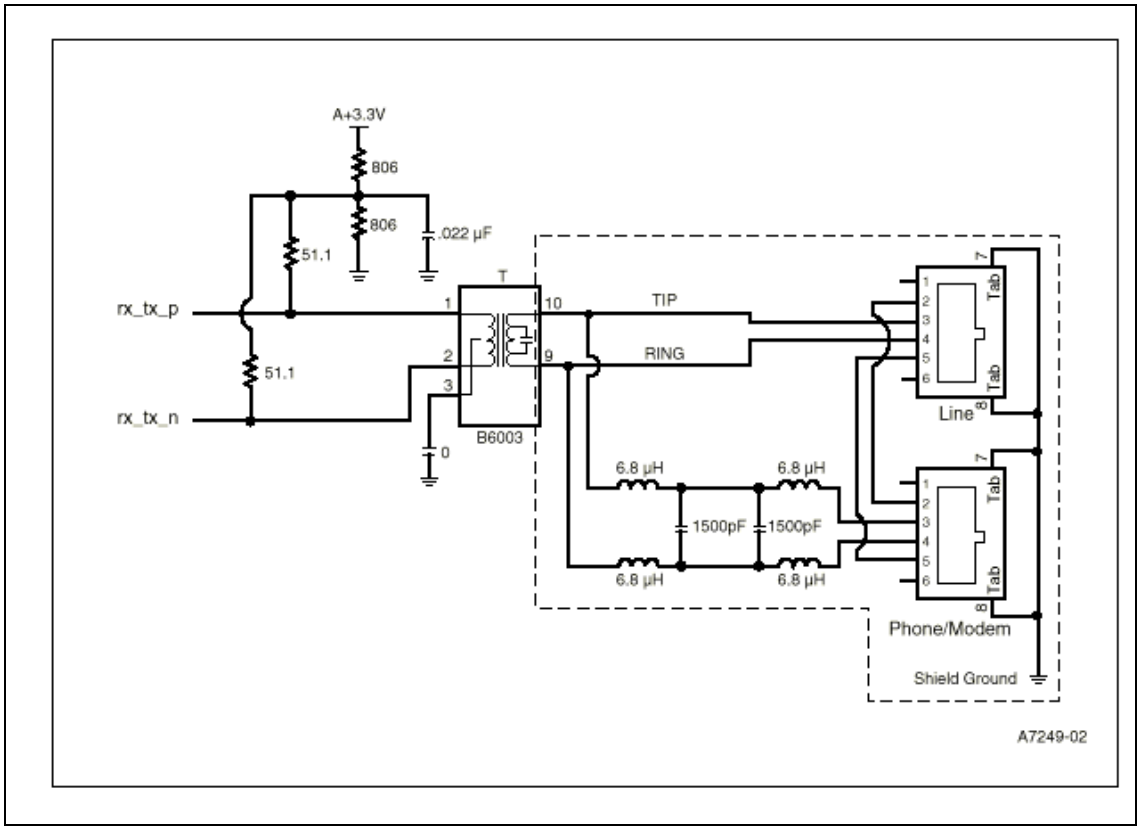
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA* magnetic module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

9.10.3.5. Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1-Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1-Ω resistors is connected to a voltage divider network. The opposite end of one 806-Ω resistor is tied to VCCA (3.3 V), and the opposite end of the other 806-Ω resistor and the cap are connected to ground. The termination is shown in the following figure.

Figure 68. 82562EH Termination



The filter and magnetic component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA* LAN interface.

One RJ-11 jack (labeled “LINE” in the above figure) allows the node to be connected to the phoneline, and the second jack (labeled “PHONE” in the above figure) allows other downline devices to be connected at the same time. This second connector is not required by HomePNA*. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA* to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Please refer to the HomePNA* website: www.homepna.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA* certifications.

9.10.3.6. Critical Dimensions

There are three dimensions to consider during layout. Distance ‘A’ from 82562EH to the magnetic module, distance ‘B’ from the line RJ11 connector to the magnetic module, and distance ‘C’ from the phone RJ11 to the LPF (if implemented).

Figure 69. Critical Dimensions for Component Placement

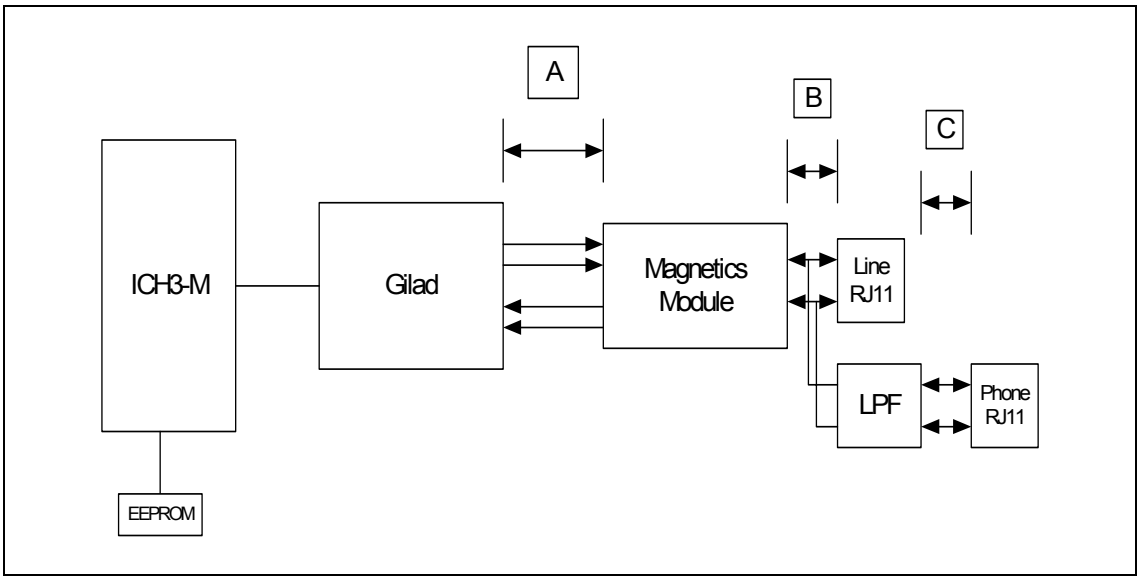


Table 45. 82562EH Home/PNA* Critical Dimensions for Component Placement

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

9.10.3.6.1. Distance from Magnetic Module to Line RJ11

This distance 'B' should be given highest priority and should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.10.3.6.2. Distance from 82562EH to Magnetic Module

Due to the high-speed of signals present, distance 'A' between the 82562EH and the magnetic should also be less than 1 inch, but should be second priority relative to distance form connects to the magnetic module.

And in general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

9.10.3.6.3. Distance from LPF to Phone RJ11

This distance 'C' should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.10.4. 82562ET / 82562EM Guidelines

9.10.4.1. Related Docs

- *82562ET LAN on Motherboard Design Guide (AP-414): OR-2336*
- *82562ET/EM PCB Design Platform LAN Connect (AP-412): OR-2059*
- *82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Datasheet (Order# A00358-004), available at http://www-niooem.jf.intel.com/components.htm and on IBL*

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.10.2. Additional guidelines for implementing an 82562ET or 82562EM Platform LAN Connect component are provided below.

9.10.4.2. Guidelines for 82562ET / 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.10.4.3. Crystals and Oscillators

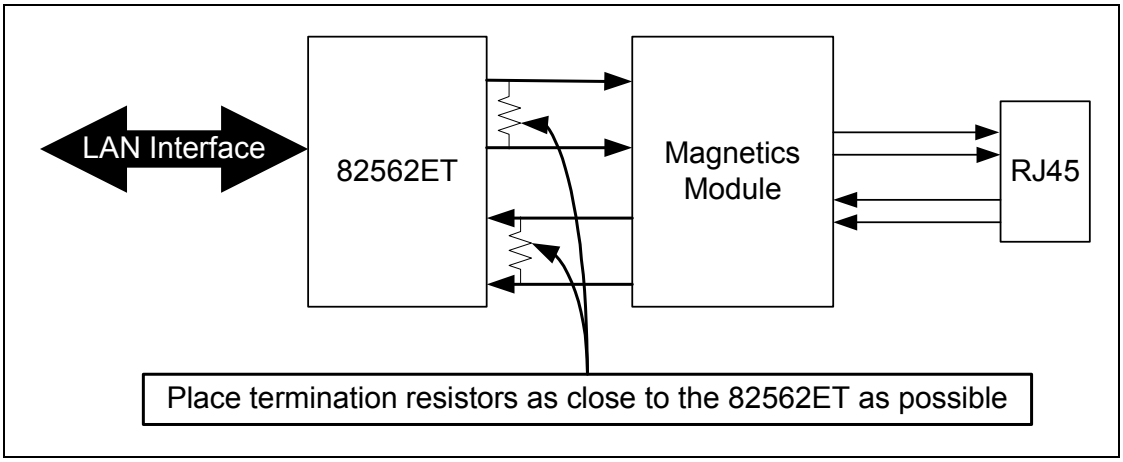
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetic module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.10.4.4. 82562ET/82562EM Termination Resistors

The 100-Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 100-Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN Connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. 82562ET), including the wire impedance reflected through the transformer.

Figure 70. 82562ET/82562EM Termination



9.10.4.5. Critical Dimensions

There are two dimensions to consider during layout. Distance ‘B’ from the line RJ45 connector to the magnetic module and distance ‘A’ from the 82562ET or 82562EM to the magnetic module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). See Figure 71 below.

Figure 71. Critical Dimensions for Component Placement

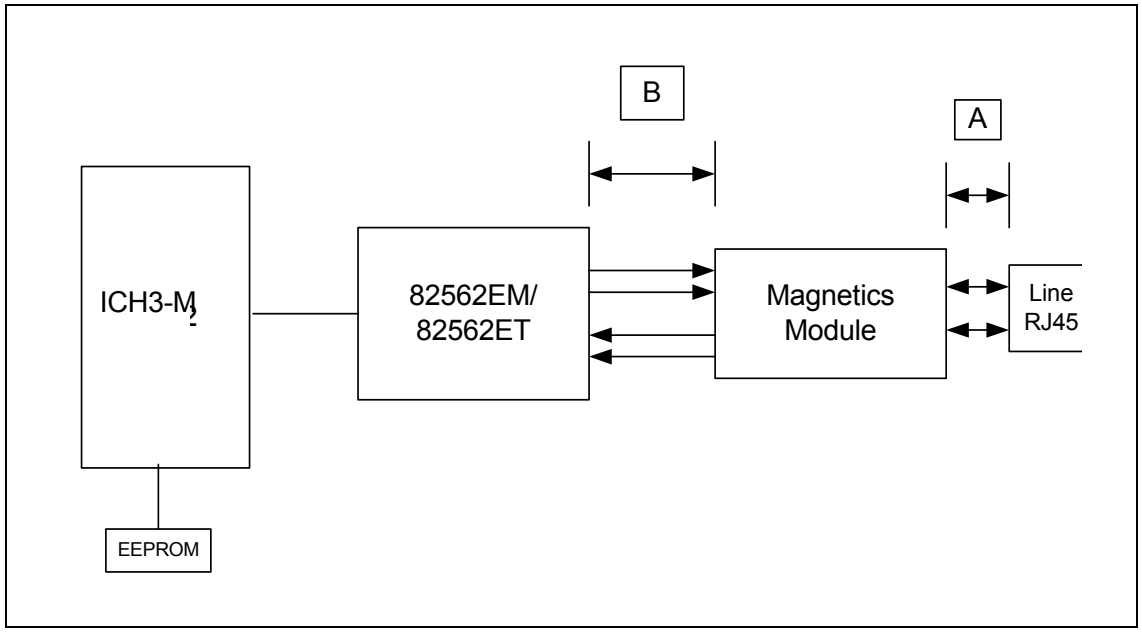


Table 46. 82562ET / 82562EM Critical Dimensions for Component Placement

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.10.4.5.1. Distance from Magnetic Module to RJ45

The distance A in the above figure should be given the highest priority in board layout. The distance between the magnetic module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω. However, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 will as short as possible should be a priority.

Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105-110 Ω should compensate for second order effects.

9.10.4.5.2. Distance from 82562ET to Magnetic Module

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.10.4.6. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly.

The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

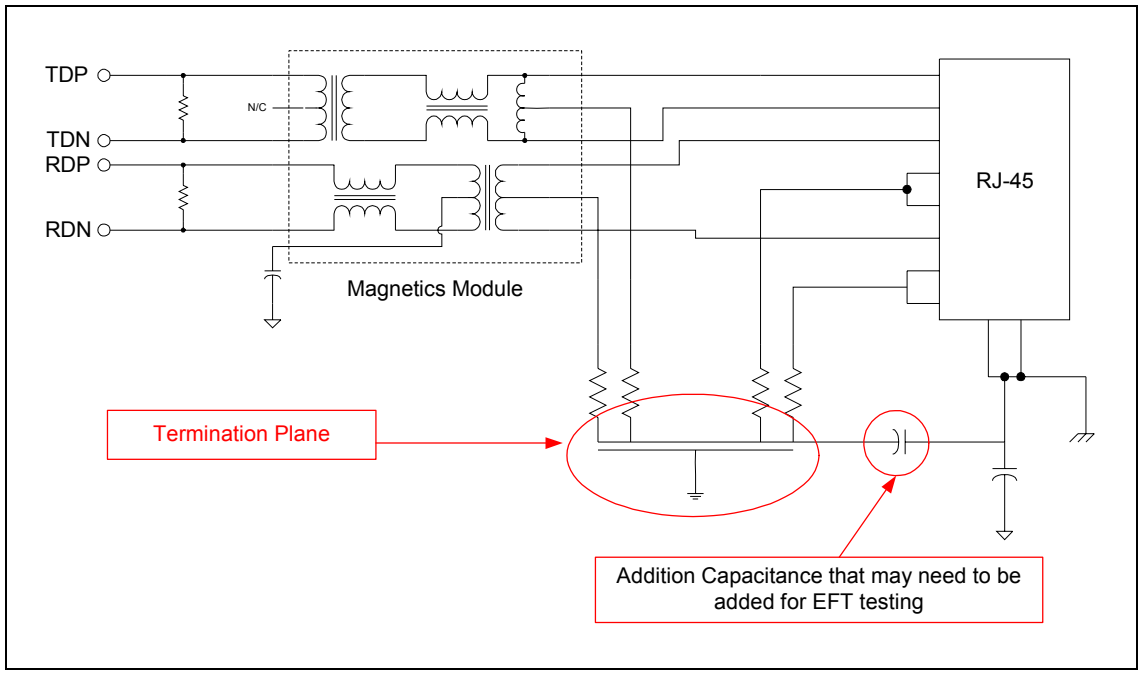
9.10.4.6.1. Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and the magnetic module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane and couples capacitively to the ground plane creating the required 1500 pF of capacitance. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused balls is then carried to the plane.

9.10.4.6.2. Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 72. Termination Plane



9.10.5. 82562ET/82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components while having only one motherboard design. The following are guidelines for the 82562ET/82562EH Dual Footprint option.

The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in the below two figures.

Figure 73. Dual Footprint LAN Connect Interface

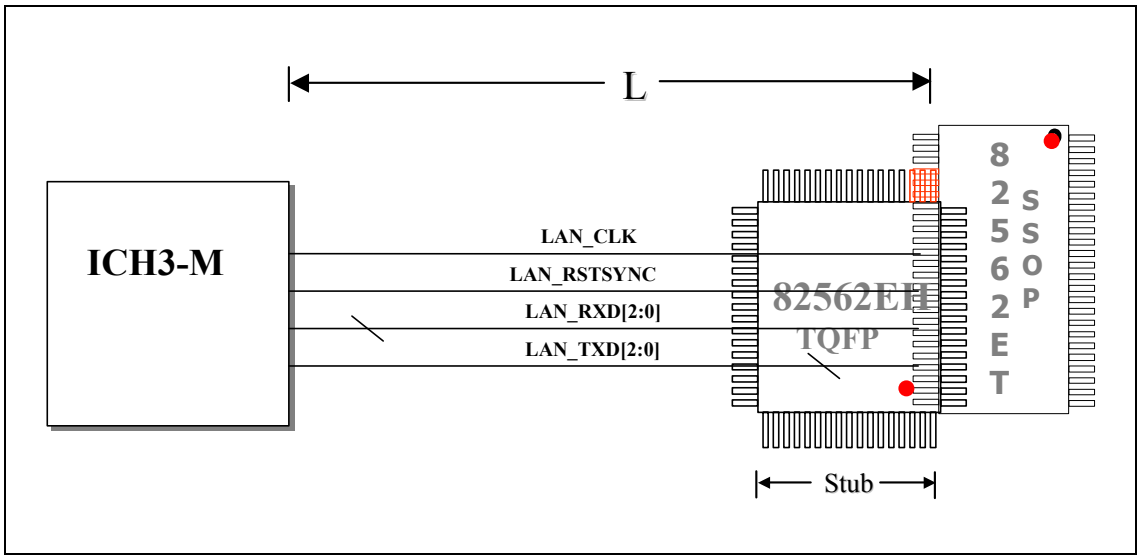
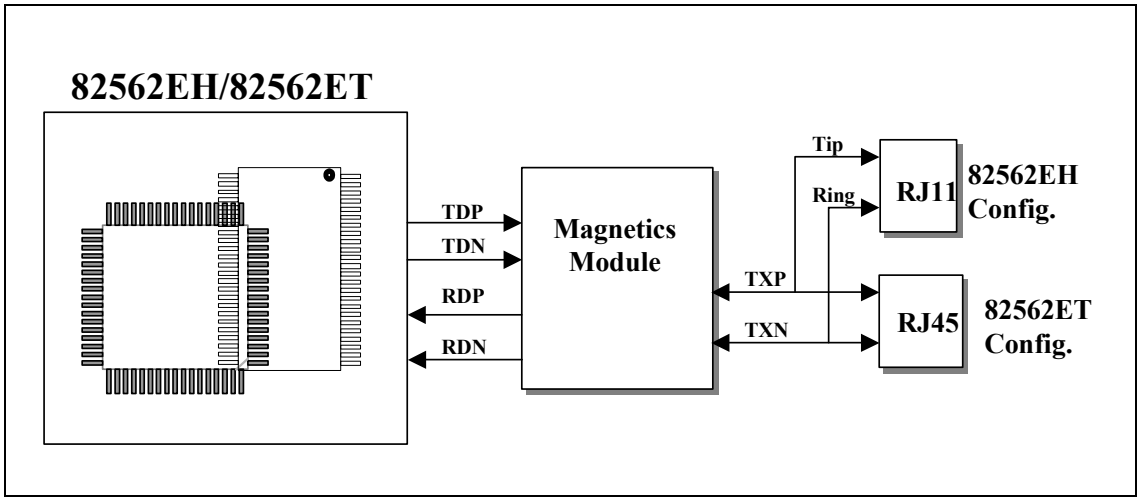


Figure 74. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 0.5 inches to 6.5 inches
- Stub < 0.5 inches
- Either 82562EH or 82562ET/82562EM can be installed. Not both
- 82562ET pins 28, 29, and 30 overlap with 82562EH pins 17, 18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- The 82562EH and 82562ET configurations share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip.

- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22-Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e. magnetic module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e. RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0-Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetic to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

10. Platform Clock Routing Guidelines

10.1. Clock Generation

Only one clock generator component is required in an Intel 845MP/845MZ chipset-based system. Clock synthesizers that meet the Intel CK-408 Clock Synthesizer/Driver Specification are suitable for an Intel 845MP/845MZ chipset based system. For more information on CK-408 compliance, refer to the CK-408 Clock Synthesizer/Driver Specification Document. The following tables and figure list and detail the Intel 845MP/845MZ clock groups, the platform system clock cross-reference, and the platform clock distribution:

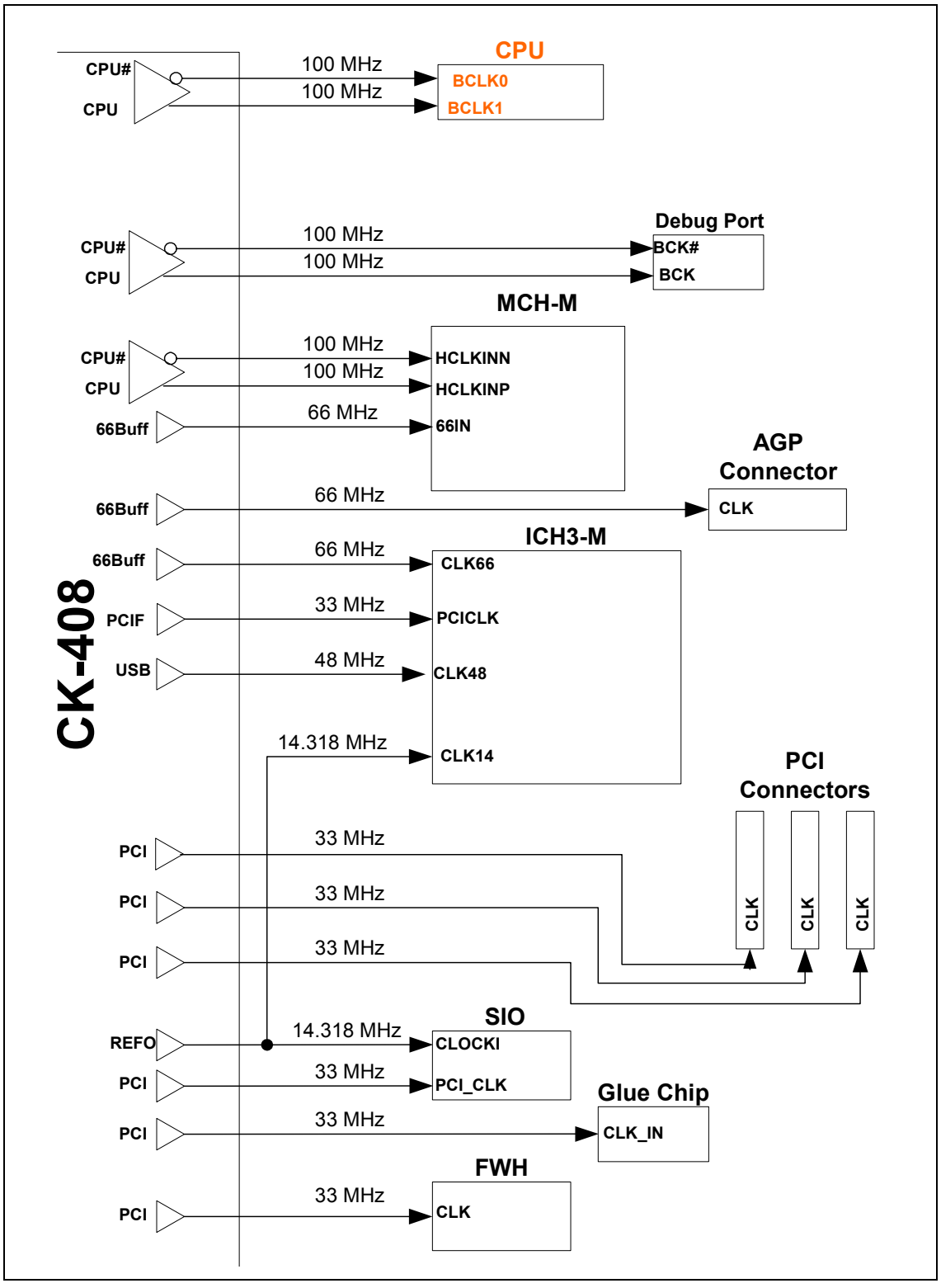
Table 47. Intel 845MP/845MZ Clock Groups

Clock Name	Frequency	Receiver
Host_CLK	100 MHz	CPU, Debug Port, and MCH-M
CLK66	66 MHz	MCH-M and Intel ICH3-M
AGPCLK	66 MHz	AGP Connector or AGP Device
CLK33	33 MHz	Intel ICH3-M, SIO, Glue Chip, and FWH
CLK14	14.318 MHz	Intel ICH3-M and SIO
PCICLK	33 MHz	PCI Connector
USBCLK	48 MHz	Intel ICH3-M
APIC_CLK	33 MHz	Intel ICH3-M (not used on 845MP/845MZ platform)

Table 48. Platform System Clock Cross-reference

Clock Group	CK-408 Pin	Component	Component Pin Name
HOST_CLK	CPU#	CPU	BCLK[0]
	CPU	CPU	BCLK[1]
	CPU#	Debug Port	BCLK[0]
	CPU	Debug Port	BCLK[1]
	CPU#	MCH-M	BCLK[0]
	CPU	MCH-M	BCLK[1]
CLK66	66BUFF	MCH-M	66IN
		ICH3-M	CLK66
AGPCLK	66BUFF	AGP Connector or AGP Device	CLK
CLK33	PCIF	ICH3-M	PCICLK
	PCI	SIO	PCI_CLK
	PCI	Glue Chip	CLK_IN
	PCI	FWH	CLK
CLK14	REF0	ICH3-M	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
USBCLK	USB	ICH3-M	CLK48
APICCLK	PCIF	ICH3-M	APICCLK

Figure 75. Processor BCLK Topology



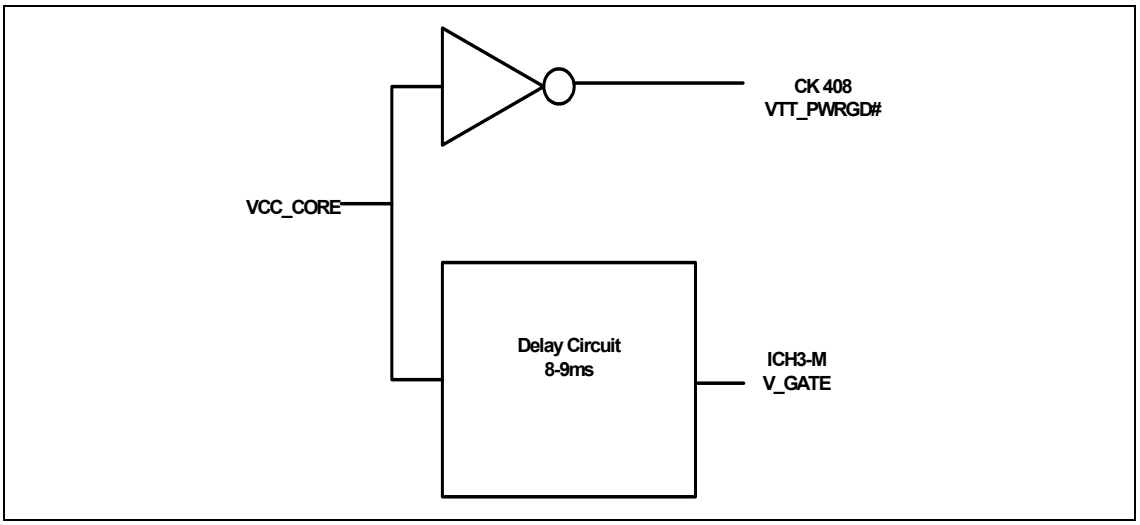
NOTE: Debug Port must always be BCLK3.

10.2. Clock Control

10.2.1. CK-408 Delay Circuit Recommendation

Ensure the processor gets power before receiving the clock. Follow Figure 76.

Figure 76. ICH3-M Follows the CK-408 Power-up



10.2.2. SLP_S1#

When asserted SLP_S1# indicates that the system is in the S1-M power state. SLP_S1# needs to be connected to clock generator PWRDWN# to shut off the system clocks in S1-M state. While entering S3 state, SLP_S1# initially asserts, but then goes high briefly when PCIRST# asserts, and then fades to low/off when the ICH3-M main I/O power rail is switched off. The duration of SLP_S1# going high is platform dependent since it is related to turning off of the ICH3-M main I/O power rail.

If SLP_S1# is directly connected to the PWRDWN# pin of a CK-408 compatible clock generator, then during S3 entry, the clock generator's outputs may be momentarily turned ON when SLP_S1# deasserts (due to PCIRST# assertion); and then turned OFF when the ICH3-MM main I/O power rail is switched off (causing SLP_S1# to fade to low/off) or when power to the clock generator is turned off, whichever occurs first. The clock restart and the subsequent clock stop are not guaranteed to be clean.

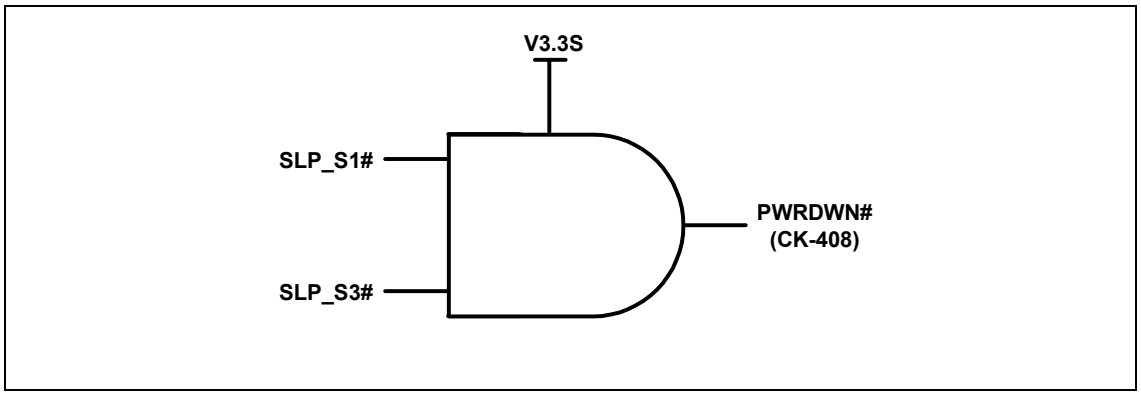
In systems that incorporate any peripherals which are not reset during S3 and which do not use SUS_STAT# as an indicator of clock validity, ensure that the PWRDWN# pin of the CK-408-compatible clock generator is not deasserted during S3 entry for a long enough duration such that the system clocks can restart.

10.2.3. SLP_S3#

When asserted SLP_S3# indicates that the system is in the S3 power state.

If systems have problem with clocks being turned on during S1M to S3 transition, the designer can use following recommendation. SLP_S3# pin be connected to clock generator PWRDWN# in combination with the SLP_S1# signal to shut off the system clocks in S3 and during S1M to S3 transition.

Figure 77. PWRDWN# to CK-408



NOTES:
1. CK-408 Minimum power up latency should be ≥ 100 µS to guarantee functionality of "AND logic". In systems that incorporate any peripherals which are not reset during S3 and which do not use SUS_STAT# as an indicator of clock validity, ensure that the PWRDWN# pin of the CK-408-compatible clock generator is not deasserted during S3 entry for a long enough duration such that the system clocks can restart.
2. If platform does not support S1M state, designer may connect SLP_S3 to PWRDWN# pin of CK-408.

10.3. Clock Group Topology and Layout Routing Guidelines

10.3.1. HOST_CLK Clock Group

The clock synthesizer provides four sets of 100-MHz differential clock outputs. The 100-MHz differential clocks are driven to the Processor the Intel 845MP/845MZ and the processor debug port as shown in figure below.

The clock driver differential bus output structure is a "Current Mode Current Steering" output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

Note: Designer should use one or the other topologies for CPU, MCH-M, and ITP. Make sure to route all clocks pairs in the same fashion (layer, layer transition, same number of via).

10.3.1.1. End Of Line Termination Topology

The recommended termination for the differential bus clock is a "End of Line Termination." Refer to Figure 78 for an illustration of this terminology scheme. Parallel Rt 55-Ω resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitic, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be between 20 and 33 Ohms. Simulations have shown that Rs values above 33 Ohms provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin #43) connected to HIGH – making the multiplication factor as 6.

- Iref pin (pin # 42) is connected to ground through a 475-Ohm (±1 % tol.) resistor – making the Iref as 2.32 mA.

Figure 78. End of Line Termination Topology

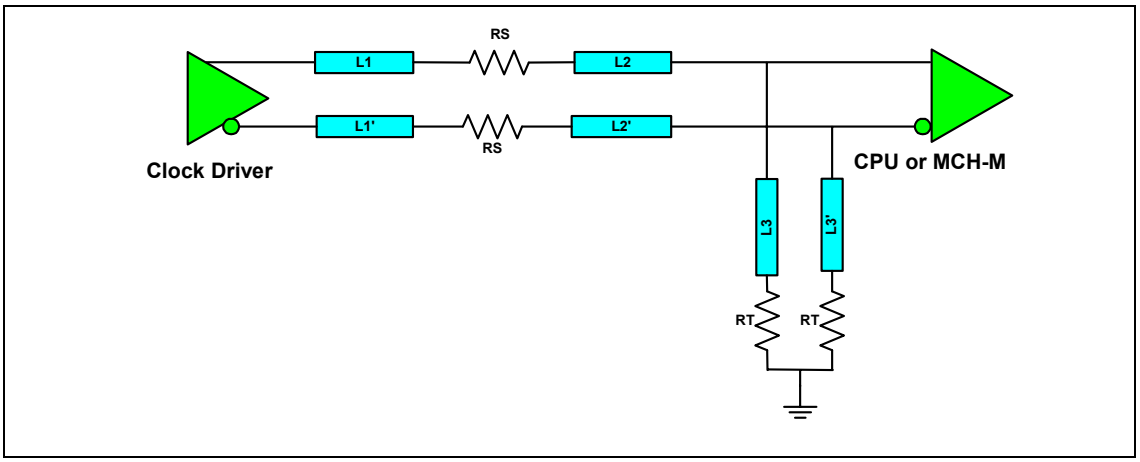


Table 49. End of Line Termination Topology BCLK [1:0]# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
BCLK Skew between agents	400 ps totalBudget:150 ps for Clock driver250 ps for interconnect		1, 2, 3, 4
Differential pair spacing	S max.	Figure 80	5, 6
Spacing to other traces	4 S- 5 S mils	Figure 80	--
Line width	4.0 mils	Figure 80	7
Systemboard Impedance – Differential	100Ω± 15%	--	8
Systemboard Impedance – odd mode	55Ω ±15%	--	9
Processor routing length – L1, L1': Clock driver to Rs	0.5” max	Figure 79	13
Processor routing length – L2, L2'	0 – 0.2"	Figure 79	13
Processor routing length – L3, L3’: RS-RT node to Rt	0 - 0.5"	Figure 79	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 8"	Figure 79	
MCH-M routing length – L1, L1’: Clock Driver to RS	0.5” max	Figure 79	13
MCH-M routing length – L2, L2'	2– 8"	Figure 79	13
MCH-M routing length – L3, L3’: RS-RT node to Rt	0 – 0.2"	Figure 79	13
Clock driver to Processor and clock driver to Chipset length matching (L1+L2)	+260 mils -190 mils	Figure 79	10
BCLK0 – BCLK1 length matching	±10 mils		--
Rs Series termination value	33 Ω ± 5%		11
Rt Shunt termination value	55 Ω ± 1% (for 55 Ω MB impedance)		12

10.3.1.2. Source Shunt Termination Topology

The recommended termination for the differential bus clock is a “Source Shunt Termination.” Refer to Figure 79 for an illustration of this terminology scheme. Parallel Rt 49.9 resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver’s output parasitic, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be between 20 and 33 Ohms. Simulations have shown that Rs values above 33 ohms provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin #43) connected to HIGH – making the multiplication factor as 6.
- Iref pin (pin # 42) is connected to ground through a 475-Ohm (± 1 % tol.) resistor – making the Iref as 2.32 mA.

Figure 79. Source Shunt Termination Topology

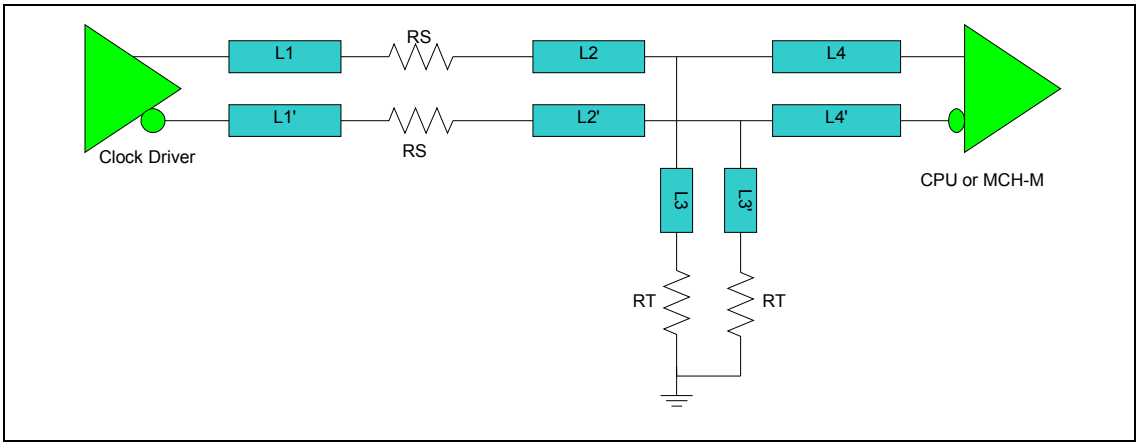


Table 50. Source Shunt Termination Topology BCLK [1:0]# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
BCLK Skew between agents	400 ps totalBudget:150 ps for Clock driver250 ps for interconnect		1, 2, 3, 4
Differential pair spacing	S max.	Figure 80	5, 6
Spacing to other traces	4 S- 5 S mils	Figure 80	--
Line width	4.0 mils	Figure 80	7
Systemboard Impedance – Differential	100Ω ± 15%	--	8
Systemboard Impedance – odd mode	55 Ω ± 15%	--	9
Processor routing length – L1, L1': Clock driver to Rs	0.5” max	Figure 79	13
Processor routing length – L2, L2'	0 – 0.2"	Figure 79	13
Processor routing length – L3, L3': RS-RT node to Rt	0 - 0.5"	Figure 79	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 8"	Figure 79	
MCH-M routing length – L1, L1': Clock Driver to RS	0.5” max	Figure 79	13
MCH-M routing length – L2, L2'	0 – 0.2"	Figure 79	13
MCH-M routing length – L3, L3': RS-RT node to Rt	0 – 0.2"	Figure 79	13
MCH-M routing length – L4, L4': RS-RT Node to Load	2 – 8"	Figure 79	
Clock driver to Processor and clock	+260 mils	Figure 79	10

Layout Guideline	Value	Illustration	Notes
driver to Chipset length matching (L1+L2+L4)	-190 mils		
BCLK0 – BCLK1 length matching	± 10 mils		--
Rs Series termination value	33 Ω ± 5%		11
Rt Shunt termination value	55 Ω ± 1% (for 55 Ω MB impedance)		12

NOTES:

1. This number does not include clock driver common m.
2. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
7. Set line width to meet correct systemboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stackup.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the systemboard trace length for the chipset will be longer than that for the processor. Details of this additional length will be included in a future revision of the processor package files.
11. Rs values between 20 Ω – 33 Ω have been shown to be effective.
12. Rt shunt termination value should match the systemboard impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.
14. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.

BCLK General Routing Guidelines:

1. When routing the 100-MHz differential clocks do not split up the two halves of a differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.
2. If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
3. Do not place Vias between adjacent complementary clock traces, and avoid differential Vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential Vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

EMI constraints:

- Clocks are a significant contributor to EMI and should be treated with care. Following recommendations can aid in EMI reduction:
- Maintain uniform spacing between the two halves of differential clocks

Route clocks on physical layer adjacent to the VSS reference plane only

Figure 80. Clock Skew as Measured from Agent to Agent

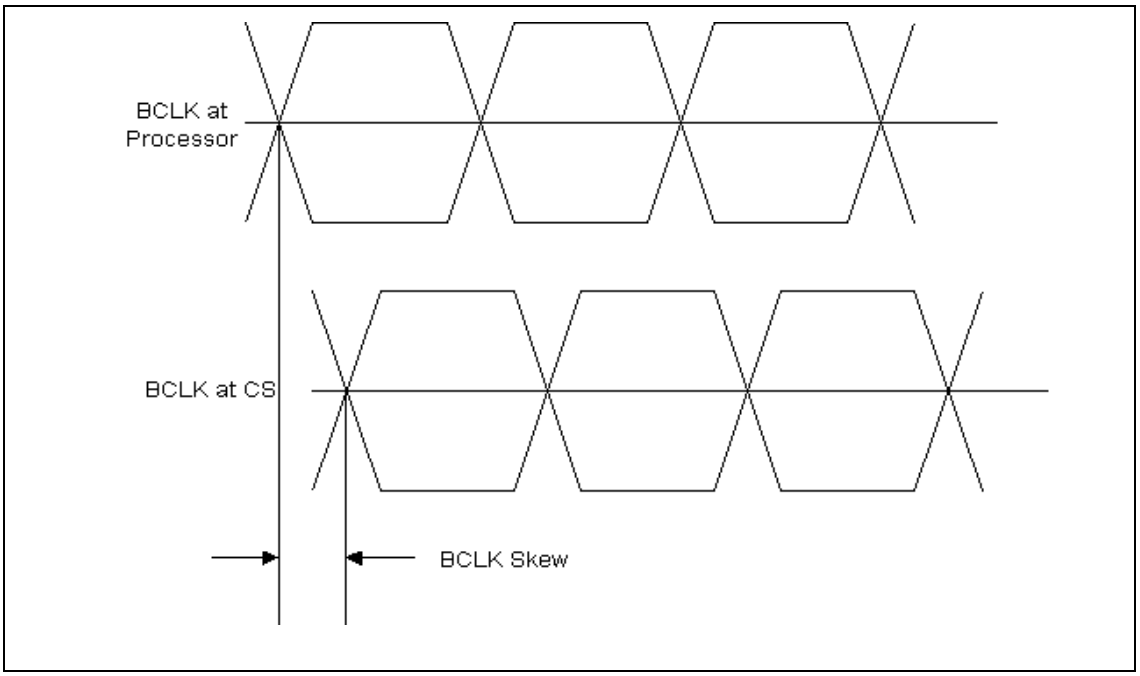
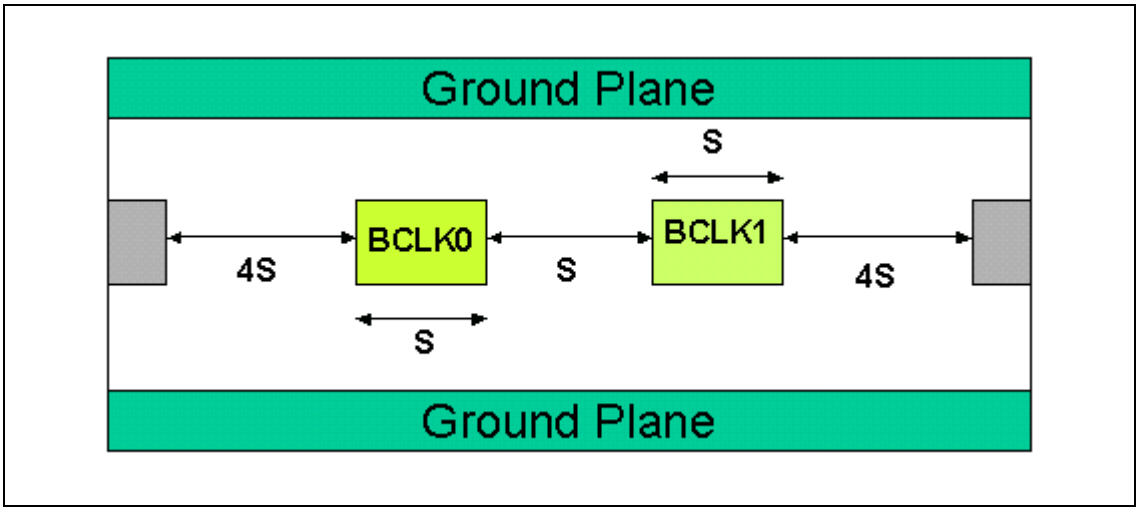


Figure 81. Trace Spacing



10.3.2. CLK66 Clock Group

The driver is the clock synthesizer 66-MHz clock output buffer and the receiver is the 66- MHz clock input buffer at the MCH-M and the Intel ICH3-M. Note that the goal is to have as little skew between the clocks within this group.

Figure 82. Topology for CLK66

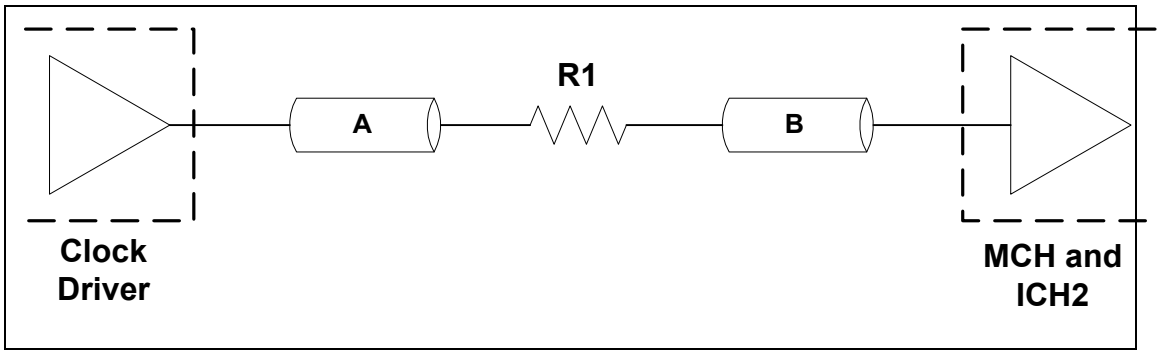


Table 51. CLK66 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK66
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	55 Ohms ± 15%
Trace Width	4 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	0.00” to 0.50”
Trace Length – B	4.00” to 8.50”
Resistor	R1 = 33 Ohms +/- 1%
Skew Requirements	All the clocks in the CLK66 group should have minimal skew (~ 0) between each other with tolerance of 500 pS
Clock Driver to MCH-M	X
Clock Driver to ICH	X ± 100 mils

If the trace length from the clock driver to the MCH-M is X, the trace length from clock to ICH must be X ± 100 mils.

10.3.3. AGPCLK Clock Group

The driver is the clock synthesizer 66-MHz clock output buffer and the receiver is the 66-MHz clock input buffer at the AGP device. Note that the goal is to have minimal (~ 0) skew between this clock and the clocks in the clock group CLK66.

Figure 83. Topology for AGPCLK to AGP Connector

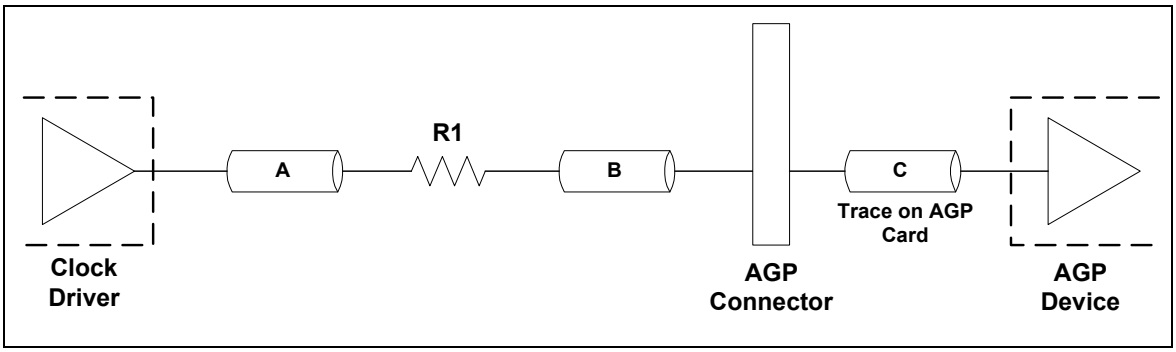


Figure 84. Topology for AGPCLK to AGP Device Down

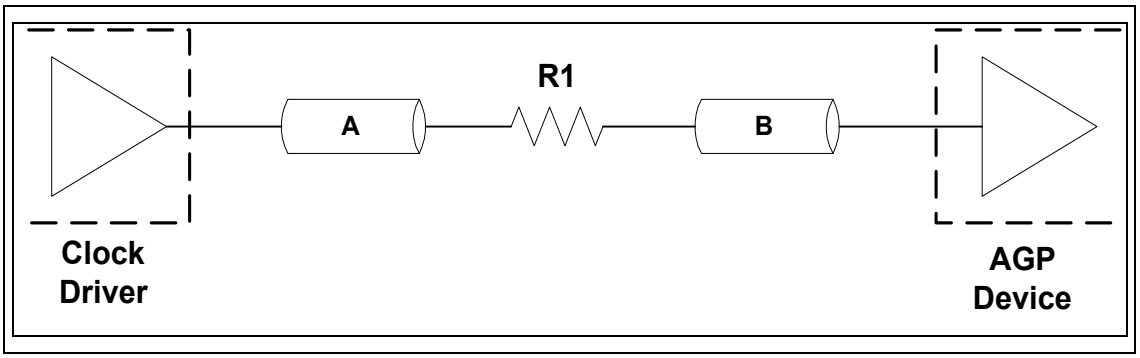


Table 52. AGPCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	AGPCLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	55 Ohms ± 15%
Trace Width	4 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	0.00” to 0.50”
Trace Length – B	(CLK66 Trace B) – 4”
Trace Length – C	Routed 4” per the AGP Specification
Resistor	R1 = 33 Ohms ± 1%
Skew Requirements	Should have minimal (~ 0) skew between the AGPCLK and the clocks in the CLK66 clock group.

10.3.4. CLK33 Clock Group

The driver is the clock synthesizer 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at the Intel ICH3-M, FWH, Glue Chip, and SIO. Note that the goal is to have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.

Figure 85. Topology for CLK33

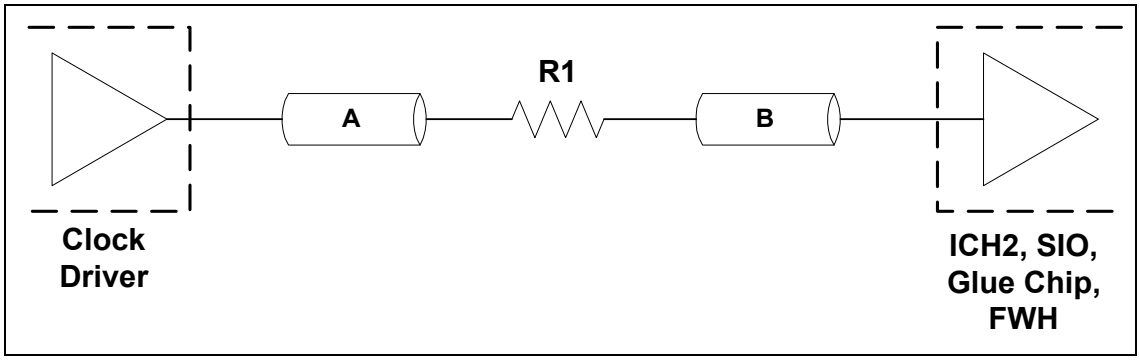


Table 53. CLK33 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	55 Ohms ± 15%
Trace Width	4 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	Same as CLK66 Trace A This trace must be exactly length matched to CLK66 Trace A
Trace Length – B	Same as CLK66 Trace B This trace must be exactly length matched to CLK66 Trace B
Resistor	R1 = 33 ohms ±1%
Skew Requirements	Should have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.

10.3.5. CLK14 Clock Group

The driver is the clock synthesizer 14.318-MHz clock output buffer and the receiver is the 14.318-MHz clock input buffer at the ICH3-M and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other, however each of the clocks in this group are asynchronous to clocks of any other group.

Figure 86. Topology for CLK14

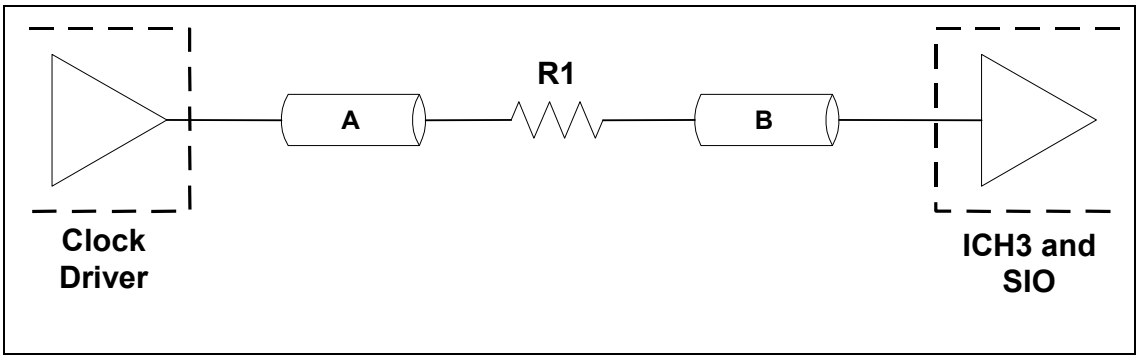


Table 54. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ohms ± 15%
Trace Width	5 mils
Trace Spacing	10 mils
Spacing to other traces	10 mils
Trace Length – A	0.00” to 0.50”
Trace Length – B	4.00” to 8.50”
Resistor	R1 = 33 Ohms ±1%
Skew Requirements	Should have minimal skew (~ 0) between each other, however each of the clocks in this group is asynchronous to clocks of any other group.

10.3.6. PCICLK Clock Group

The driver is the clock synthesizer 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at the PCI devices on the PCI cards. Note that the goal is to have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ±1 ns skew between the clocks of this group and that of group CLK33.

Figure 87. Topology for PCICLK to PCI Device Down

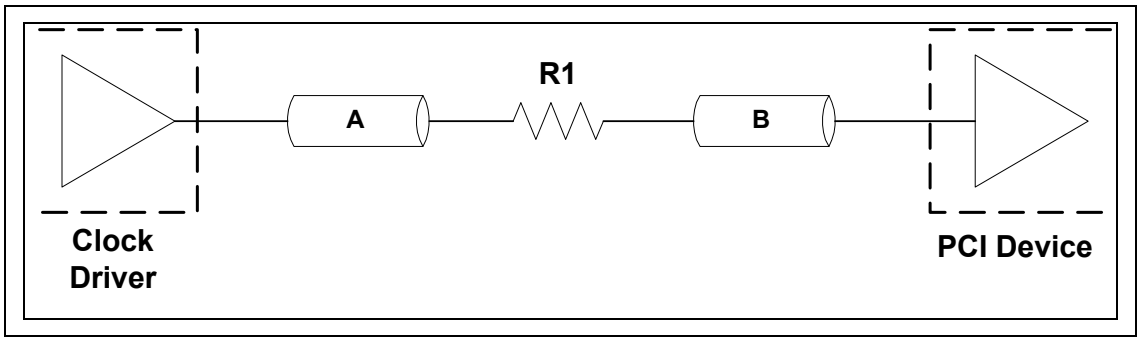


Table 55. PCICLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ohms ± 15%
Trace Width	5 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	Same as CLK33 Trace A This trace must be exactly length matched to CLK33 Trace A
Trace Length – B	Same as CLK33 Trace B This trace must be exactly length matched to CLK33 Trace B
Resistor	R1 = 33 Ohms ± 1%
Skew Requirements	Should have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ±1 ns skew between the clocks of this group and that of group CLK33.

Figure 88. Topology for PCICLK to PCI Slot

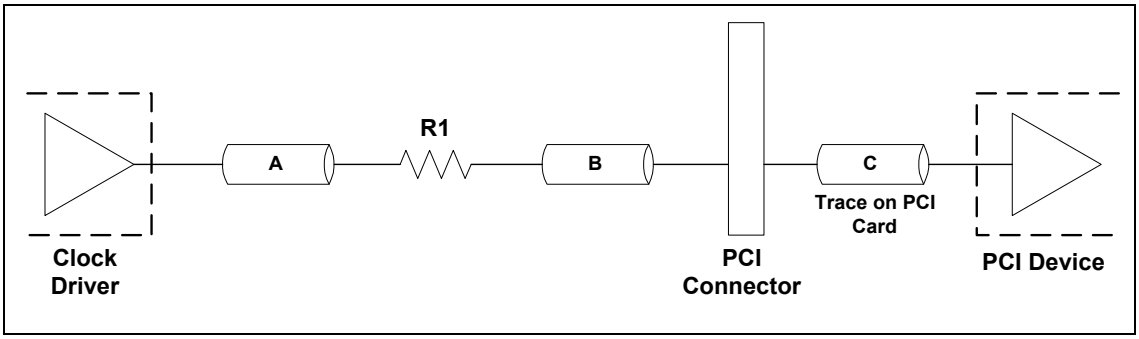


Table 56. PCICLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	50 Ohms ± 15%
Trace Width	5 mils
Trace Spacing	10 mils
Spacing to other traces	10 mils
Trace Length – A	Same as CLK33 Trace A This trace must be exactly length matched to CLK33 Trace A
Trace Length – B	(Routed equal to CLK33 Trace B) – 2.5”
Trace Length – C	Routed 2.50” per the PCI Specification
Resistor	R1 = 33 Ohms ± 1%
Skew Requirements	Should have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ±1 ns skew between the clocks of this group and that of group CLK33.
Maximum via Count per signal	1

10.3.7. USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer and the receiver is the USB clock input buffer at the Intel ICH3-M. Note that this clock is asynchronous to any other clock on the board.

Figure 89. Topology for USB_CLOCK

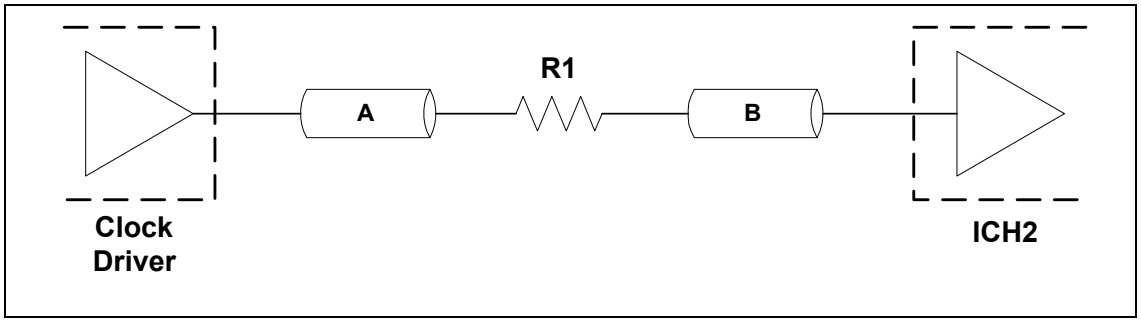


Table 57. USBCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	50 Ohms ± 15%
Trace Width	5 mils
Trace Spacing	-
Spacing to other traces	20 mils
Trace Length – A	0.00” – 0.50”
Trace Length – B	3.00” – 12.00”
Resistor	R1 = 33 Ohms ± 1%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum via Count per signal	2

11. Platform Power Guidelines

11.1. Definitions

Suspend-To-RAM (STR):

In the STR state, the system state is stored in main memory and all unnecessary systemlogic is turned off. Only main memory and logic required to *wake* the system remain powered.

Full-power operation:

During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (PROCESSOR stop-grant state) state.

Suspend operation:

During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).

Core power rail:

A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply.

Standby power rail:

A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: 5 V_{SB} (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail:

A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 V_{SB} is usually derived (on the motherboard) from 5V_{SB} using a voltage regulator.

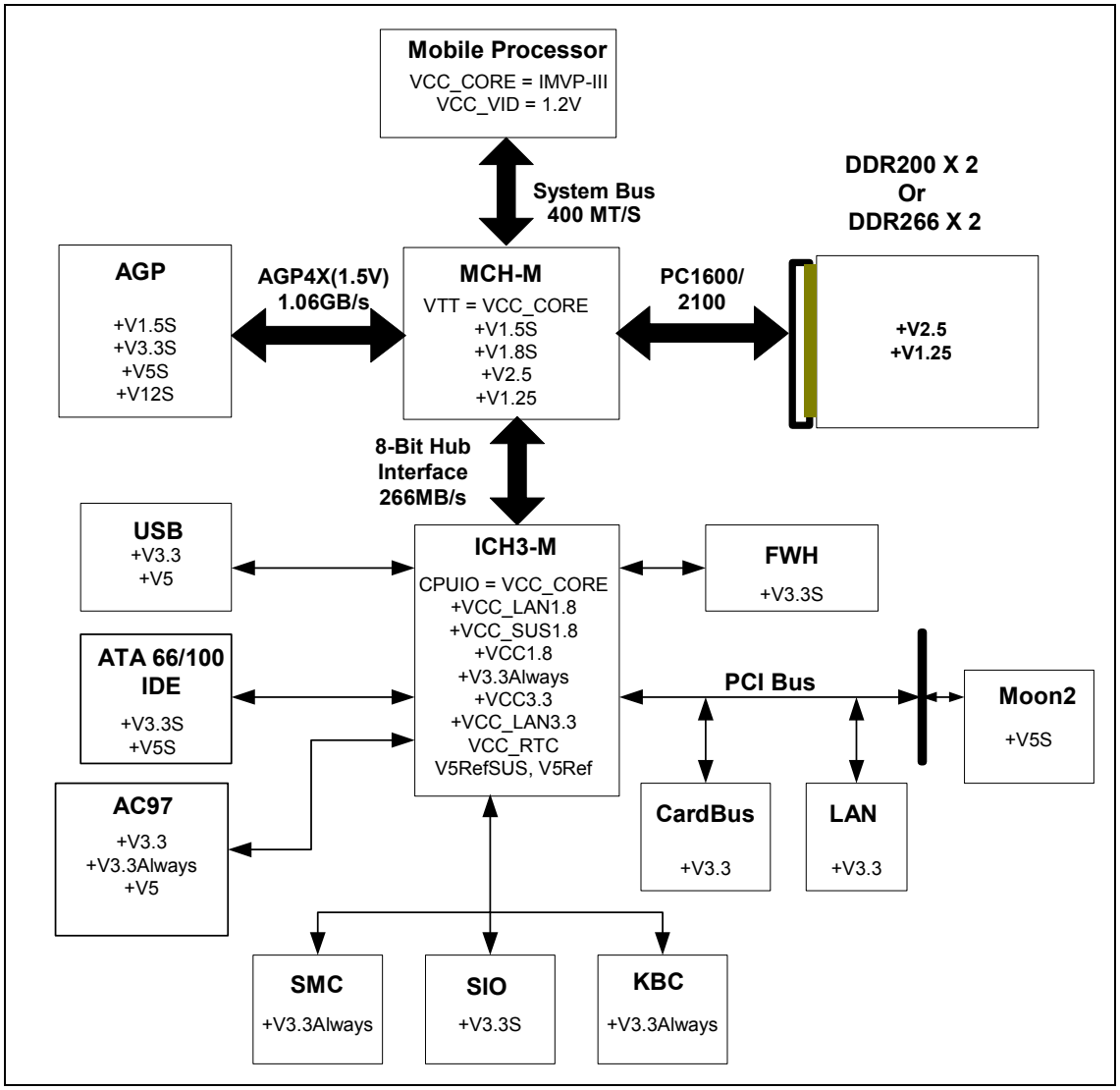
Dual power rail:

A *dual* power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

11.2. Platform Power Requirements

11.2.1. Platform Power Delivery Architectural Block Diagram

Figure 90. Platform Power Delivery Block Diagram



11.3. Voltage Supply

11.3.1. Power Management States

Table 58. Power Management States

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S5#	+V*ALW	+V*	+V*S	CLOCKS
FULL ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power on Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	LOW
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

11.3.2. Power Supply Rail Descriptions

Table 59. Power Supply Rail Descriptions (* Currents are Estimates Only)

Signal Names	Voltage (V)	Current (A)*	Tolerance	Enable	Description
+V1_25	1.25	± 2.0	± 2% DC	SLP_S5# HIGH	845MP/845MZ MCH-M DDR Reference & Termination. SLP_S5# for VTT is “ON”, SLP_S3# for VTT “OFF”
+V1_5S	1.5	3.5	± 5%	SLP_S3# HIGH	845MP/845MZ MCH-M Core & AGP, AGP VDDQ
+V1_8ALWAYS	1.8	0.21	± 5%	+VDC ON	ICH3-M
+V1_8	1.8	0.5	± 5%	SLP_S5# HIGH	ICH3-M
+V1_8S	1.8	0.8	± 5%	SLP_S3# HIGH	ICH3-M, 845MP/845MZ MCH-M
+V2_5	2.5	6.1	± 5%	SLP_S5# HIGH	845MP/845MZ MCH-M DDR I/O, DDR SO-DIMM
+V3ALWAYS	3.3	0.4	± 5%	+VDC ON	ICH3-M, SMC/KBC, AC97
+V3	3.3	0.9	± 5%	SLP_S5# HIGH	ICH3-M, Cardbus, AC97, RS232
+V3S	3.3	7.0	± 5%	SLP_S3# HIGH	ICH3-M, CK-408, AGP Core, DDR SO-DIMM, FWH, SIO, AC97
+V5	5.0	9.0	± 5%	SLP_S5# HIGH	USB, AC97, HDD,+V2_5, AGP, +V1_25, DVD/CDROM,
+V5S	5.0	1.0	± 5%	SLP_S3# HIGH	ICH3-M, AGP I/O, MSE/KBD, FDD, HDD, DV/CDROM
+V12S	12.0	0.2	± 5%	SLP_S3# HIGH	AGP, Cardbus
+VCC_CORE	IMVP-III	40.0	IMVP-III	+VCC_VID HIGH	See IMVP-III *Mobile Processor Core Voltage Regulator Specification* Design Guide for details.
+VCC_VID	1.2	0.300	± 5% DC	VR_ON	Reference voltage for processor

Signal Names	Voltage (V)	Current (A)*	Tolerance	Enable	Description
			± 9% AC		PLL and VID circuitry.

11.3.3. Power Supply Control Signals

11.3.3.1. SLP_S3#

SLP_S3# is a signal coming from the ICH3-M. Deassertion of SLP_S3# enables the outputs for the following rails: +V1.25, +V1_5S, +V1_8S, +V3_3S, +V5S, and +V12S. SLP_S3# will be asserted when the system enters S3/S4/S5 or powers off. SLP_S3# is deasserted when the system boots up or exits from S3, S4, and S5.

11.3.3.2. SLP_S5#

SLP_S5# is a signal coming from the ICH3-M. Deassertion of SLP_S5# enables the outputs for the following rails: +V1_8, +V2_5, +V3_3, and +V5. SLP_S5# will be asserted when the system enters S4/S5 or powers off. SLP_S5# is deasserted when the system boots up or exits from S4 and S5.

11.4. Platform Power Sequencing Requirements

11.4.1. Processor Power Sequencing

11.4.1.1. Core Converter Soft Start Timer

Refer to 4.4.2.2.

11.4.2. ICH3-M Power Sequencing

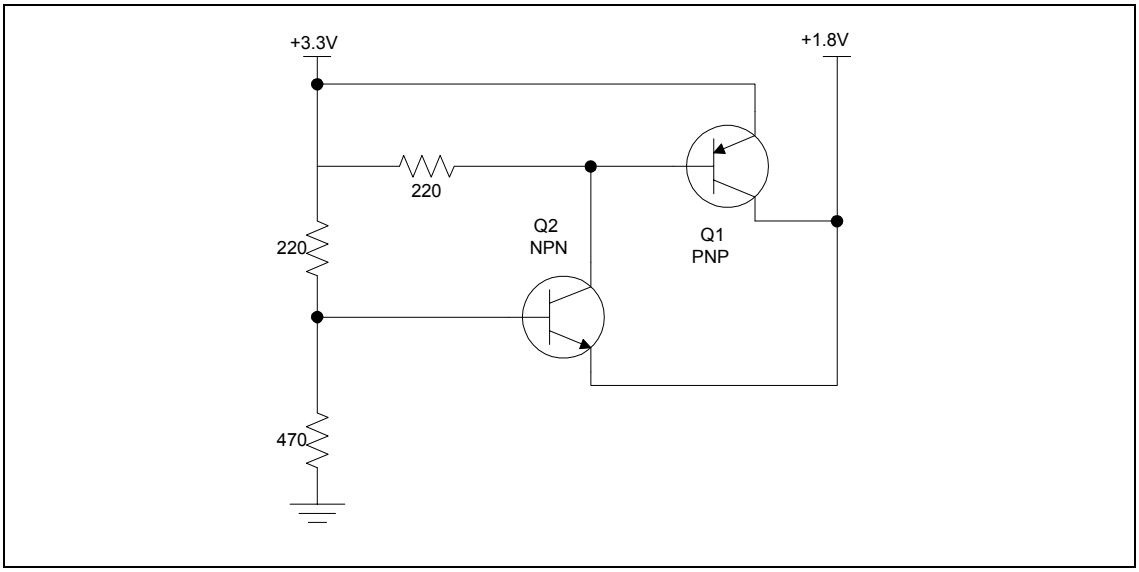
11.4.2.1. 1.8 V/3.3 V Sequencing

The ICH3-M has three pairs of associated 1.8-V and 3.3-V supplies. These are +V1.8ALWAYS & +V3ALWAYS, +V1.8 & +V3, and +V1.8S & +V3S. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.8-V supply may come up before the 3.3 V supply without violating this rule. One serious consequence of violation of this "2 V Rule" is electrical overstress of oxide layers, resulting in component damage. The majority of the ICH3-M I/O buffers are driven by the 3.3-V supplies, but are controlled by logic that is powered by the 1.8-V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3-V supply comes up first. In this case, the I/O buffers will be in an undefined state until the 1.8-V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH3-M may unexpectedly drive these signals if the 3.3-V supply is active while the 1.8-V supply is not.

Figure 91 is an example power-on sequencing circuit that ensures the “2 V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8-V supply tracks the 3.3-V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying

the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3-V supply into 1.8-V plane when the 1.8-V plane reaches 1.8 V.

Figure 91. Example 1.8-V/3.3-V Power Sequencing Circuit



When analyzing systems that may be "marginally compliant" to the 2 V Rule, please pay close attention to the behavior of the ICH3-M's RSMRST#, PWROK, and LAN_RST# in ICH3-M signals, since these signals control internal isolation logic between the various power planes:

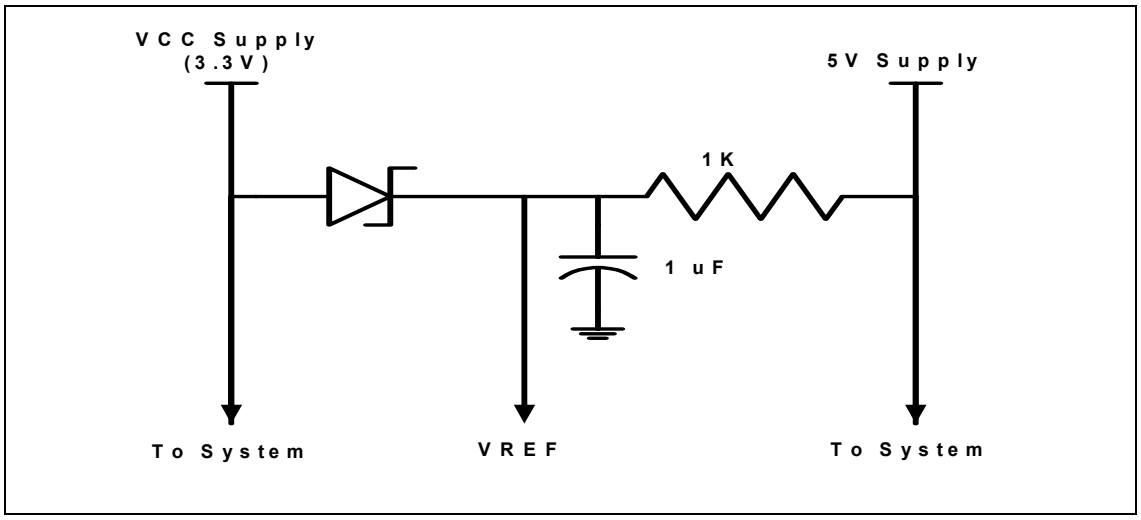
- RSMRST# controls isolation between the RTC well and the Resume wells
- PWROK controls isolation between the Resume wells and Main wells
- LAN_RST# controls isolation between the LAN wells and the Resume wells (applies only to ICH3-M)

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

11.4.2.2. 3.3-V/V5REF and 3.3SUS/V5REF_SUS Sequencing

V5REF is the reference voltage for 5-V tolerance on inputs to the ICH3-M. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. The rule must be followed in order to ensure the safety of the ICH3-M. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 92 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule. This rule also applies to the standby rails, but in most platforms, the VCCSUS3_3 rail is derived from the VCCSUS5 rail and therefore, the VCCSUS3_3 rail will always come up after the VCCSUS5 rail. As a result, V5REF_SUS will always be powered up before VCCSUS3_3. In platforms that do not derive the VCCSUS3_3 rail from the VCCSUS5 rail, this rule must be comprehended in the platform design.

Figure 92. Example 3.3-V/V5REF Sequencing Circuitry



In compliance with USB 2.0 specification requirements for continuous short conditions, V5REF_Sus pins must be connected to 5 V. 5VREF_Sus affects 5-V tolerance for all USB signals, both over-current and data pins. USB 2.0 specification requires that USB controller to withstand a continuous short between the USB 5-V connector supply to a USB signal at the connector for 24 hours. Figure 93 and Figure 94 provide options for connecting V5REF_Sus to 5 volts on mobile platforms. Figure 93 is for platforms that support +V5_Always (5 V always ON). Figure 94 represents a connection to V5REF_Sus for platforms that do not support +V5_Always.

Figure 93. V5REF_Sus Option 1: +V5_Always Available in Platform

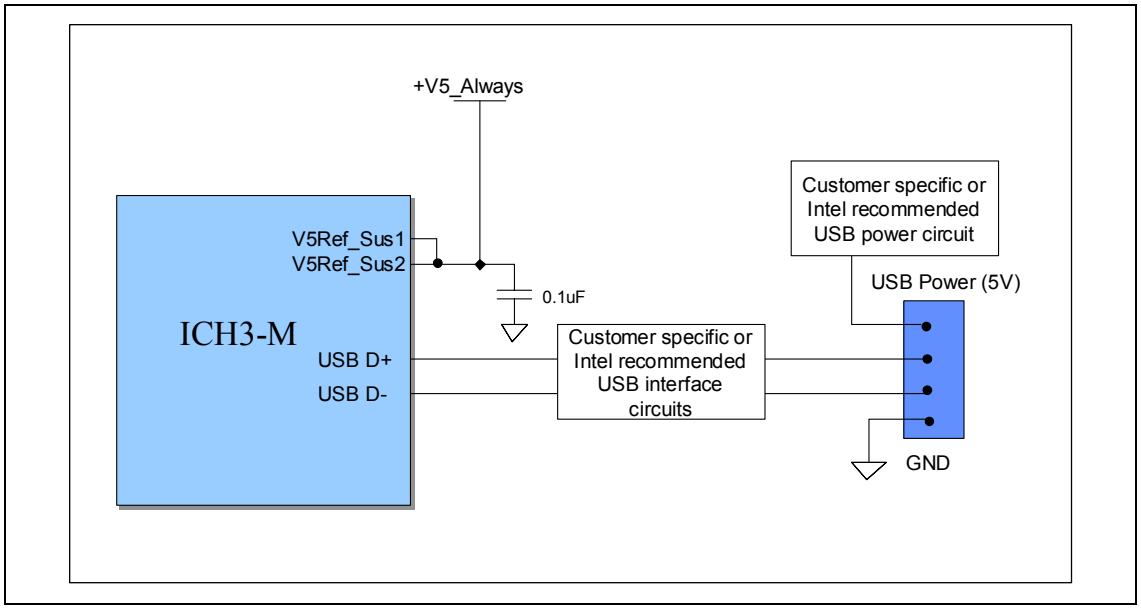
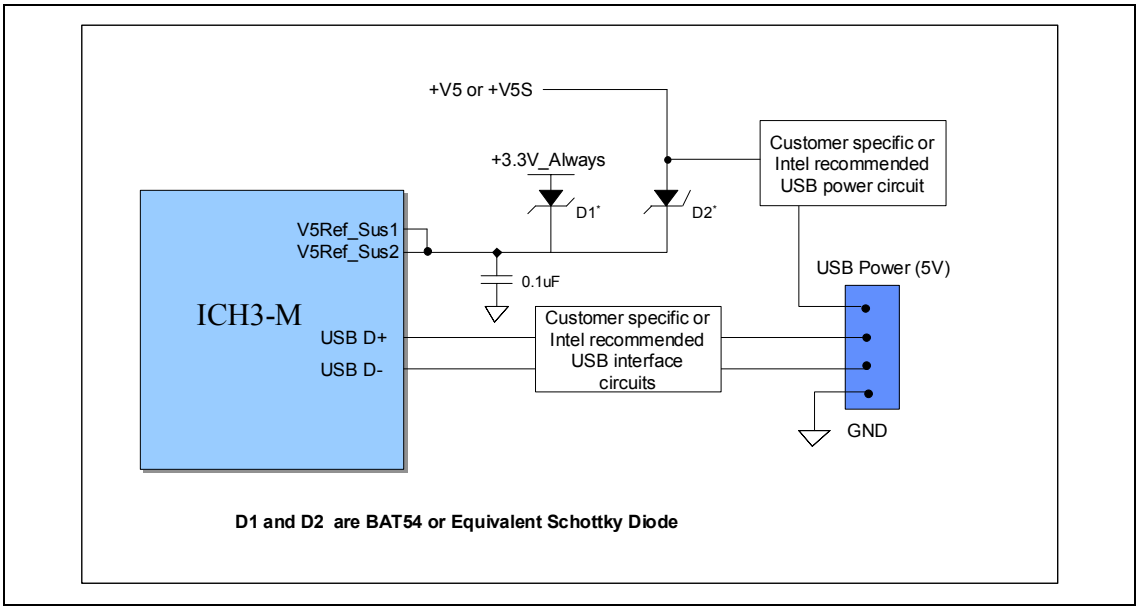


Figure 94. V5REF_Sus Option 1: +V5_Always Not Available in Platform



11.4.3. MCH-M Power Sequencing Requirements

There are no MCH-M power sequencing requirements. All MCH-M power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice would have all MCH-M power rails come up as close in time as practical, with the core voltage (1.5 V) coming up first.

11.4.4. DDR Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ are driven from a single power converter output.
- VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)
- VREF tracks VDDQ/2
- A minimum resistance of 42 Ohm (22 Ohm series resistor + 22 Ohm parallel resistor -5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, then the following table must be adhered to during power up:

Table 60. Power-up Initialization Sequence (Should Above Listed Requirements Not be Met)

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
$V_{DD}Q$	After or with V_{DD}	< V_{DD} + 0.3 V
V_{TT}	After or with $V_{DD}Q$	< $V_{DD}Q$ + 0.3 V
V_{REF}	After or with $V_{DD}Q$	< $V_{DD}Q$ + 0.3 V

11.5. Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerances for each component. To meet the component transient load steps, it is necessary to properly place bulk and high frequency capacitors close to the component power and ground pins.

11.5.1. Transient Response

The inductance of the motherboard power planes slows the voltage regulator's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed the more stray inductance is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, areas closer to the load have less room for capacitor placement. Therefore tradeoffs must be made. It is the responsibility of the system designer to provide adequate high frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage capacitors supply current during longer lasting changes in current demand.

High Frequency decoupling is typically done with ceramic capacitors with a very low ESR. Because of there low ESR, these capacitors can act very quickly to supply current at the beginning of a transient event. However, because the ceramic capacitors are small, i.e. they can only store a small amount of charge, Bulk capacitors are needed too. Bulk capacitors are typically polarized with high capacitance values and unfortunately higher ESRs. The higher ESR of the Bulk capacitor limits how quickly it can respond to a transient event. The Bulk and HF capacitors working together can supply the charge needed to stay in regulator before the regulator can react during a transient. The bulk capacitors and the high frequency capacitors should be placed as close to the load as possible and in the path of current flow.

Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Power should never be distributed by traces alone. Intel recommends that all layers of the stack-up be used for power and ground routing.

11.5.2. Processor Decoupling Recommendations

See Processor Power Delivery Design Recommendations.

11.5.3. ICH3-M Decoupling Recommendations

11.5.3.1. 1.8-V Power Supply Rails

Seven 0.1 µF, 0603, X7R capacitors and one 22.0 µF, X5R capacitors should be placed between the VCCPHL and VCCCORE supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

Eight 0.1 µF, 0603, X7R capacitors and one 22.0 µF, X5R capacitors should be placed between the VCCPUSB and the VCCPSUS supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

Two 0.1 µF, 0603, X7R capacitors and one 4.7 µF, X5R capacitors should be placed between the VCCPAUX supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

11.5.3.2. 3.3-V Power Supply Rails

Twelve 0.1 µF, 0603, X7R capacitors and one 22.0 µF, X5R capacitors should be placed between the VCCPPCI supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

Three 0.1 µF, 0603, X7R capacitors and one 10.0 µF, X5R capacitors should be placed between the VCCSUS supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

Two 0.1 µF, 0603, X7R capacitors and one 22 µF, X5R capacitors should be placed between the VCCAUX supply pins and the VSS ground pins. Place the all capacitors as close to the ICH3-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

11.5.4. MCH-M Decoupling Recommendations

11.5.4.1. VCC_CORE, VTT Processor System Bus, VTT

Ten 0.1 µF, 0603, X7R capacitors and three 10.0 µF, 1206, X5R capacitors should be placed between the VTTFSB supply pins and the VSS ground pins. Place the all capacitors as close to the MCH-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

11.5.4.2. 1.5-V AGP/CORE

Six 0.1 µF, 0603, X7R capacitors and two 10.0 µF, 1206, X5R capacitors should be placed between the VCCAGP/VCCCORE supply pins and the VSS ground pins. Place the all capacitors as close to the MCH-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

11.5.4.3. 1.8-V Hub Interface

Three 0.1 µF, 0603, X7R capacitors and one 10.0 µF, 1206, X5R capacitors should be placed between the VCCHL supply pins and the VSS ground pins. Place the all capacitors as close to the MCH-M package as possible, but ensure the 0603 capacitors are the closest to the package. Connections should be done to minimize loop area and loop inductance of these capacitors.

11.5.5. 2.5-V MCH-M System Memory High Frequency Decoupling

Every MCH-M ground and power ball in the system memory interface should have its own via. For 2.5-V high frequency decoupling, a minimum of six 0603 0.1-µF high frequency capacitors is required, and must be within 150 mils of the MCH-M package. The six capacitors should be evenly distributed along

the MCH-M DDR system memory interface and must be placed perpendicular to the MCH-M with the power (2.5 V) side of the capacitors facing the MCH-M. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5-V power ball on the outer row of balls on the MCH-M. Each capacitor should have their 2.5-V via placed directly over and connected to a separate 2.5 V copper finger, and they should be as close to the capacitor pad as possible, within 25 mils. The ground end of the capacitors must connect to the ground flood and to the ground plane through a via. This via should be as close to the capacitor pad as possible, within 25mils with as thick a trace as possible.

11.5.6. 2.5-V MCH-M System Memory Low Frequency Bulk Decoupling

The MCH-M system memory interface requires low frequency bulk decoupling. Place two 100-µF electrolytic capacitors between the MCH-M and the first SO-DIMM connector. The power end of the capacitors must connect to 2.5 V, and the ground end of the capacitors must connect to ground. Also, the output of the 2.5-V regulator must have enough bulk decoupling to ensure the stability of this regulator. The amount of bulk decoupling required at the output of the 2.5 V regulator will vary according to the needs of different OEM design targets.

11.5.7. 2.5-V SO-DIMM System Memory High Frequency Decoupling

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 0.1 uF high-frequency bypass capacitors are required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors should connect to 2.5 V and ground. The ground trace should connect to a via that transitions to the ground flood and to the ground plane. The ground via should be placed as close to the ground pad as possible. The 2.5-V trace should connect to a via that transitions to the 2.5 V copper flood and to the 2.5-V plane. It should connect to the closet 2.5-V SO-DIMM pin on either the first or second SO-DIMM connector, with a wide trace. The capacitors 2.5 V traces should be distributed as evenly as possible amongst the two SO-DIMMs.

11.5.8. 2.5-V SO-DIMM System Memory Low Frequency Decoupling

The DDR SO-DIMMs require low frequency bulk decoupling. Place a total of four 100-µF capacitors, one at each corner of each SO-DIMM connector. The power end of the capacitors must connect to a 2.5-V plane, and the ground end of the capacitors must connect to ground plane. The output of the 2.5-V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 2.5-V regulator will vary according to the needs of different OEM design targets.

11.5.9. 1.25-V DDR VTT High Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603 0.1-µF capacitor per two DDR signals. These decoupling capacitors connect directly to the VTT Island and to ground, and must be spread-out across the termination Island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible. The ground end of the capacitors must connect to the ground flood on layer two and to the ground plane on layer three through a via. Finally, the distance from any DDR termination resistor pin to a VTT capacitor pin must not exceed more then 100 mils.

11.5.10. 1.25-V DDR VTT Low Frequency Bulk Decoupling Requirements

The VTT Termination Island requires low frequency bulk decoupling. Place one 220-µF electrolytic capacitor at each end of the termination island. The power end of the capacitors must connect to the Vtt termination island directly, and the ground end of the capacitors must connect to ground. Also, the output of the 1.25-V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25-V regulator will vary according to the needs of different OEM design targets.

11.5.11. 1.5-V AGP Decoupling

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel 845MP/845MZ chipset (MCH-M). The following guidelines are not intended to replace thorough system validation on Intel 845MP/845MZ chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the MCH-M. These should be placed within 70 mils of the outer row of balls on the MCH-M for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- In order to add the decoupling capacitors within 70 mils of the MCH-M and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1-inch max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01-µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

11.5.12. 1.8-V Hub Interface Decoupling

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH3-M and MCH-M). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the +V1.8 side of the capacitors to the +V1.8 power pins. Similarly, if layout allows, metal fingers running on the +V1.8 side of the board should connect the groundside of the capacitors to the VSS power pins.

11.5.13. 3.3-V FWH Decoupling

A 0.1-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

11.5.14. 3.3-V General LAN Decoupling

- All Vcc pins should be connected to the same power supply.
- All Vss pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended
- Place decoupling as close as possible to power pins.

11.6. 3.3-V Clock Driver Decoupling

The decoupling caps should be connected taking care to connect the Vdd pins directly to the Vdd side of the caps. However, the Vss pins should not be connected directly to the Vss side of the caps. Instead they should be connected to the ground flood under the part that is viaed to the ground plane. This is done to avoid Vdd glitches propagating out, getting coupled through the decoupling caps to the Vss pins. This method has been shown to provide the best clock performance.

The decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

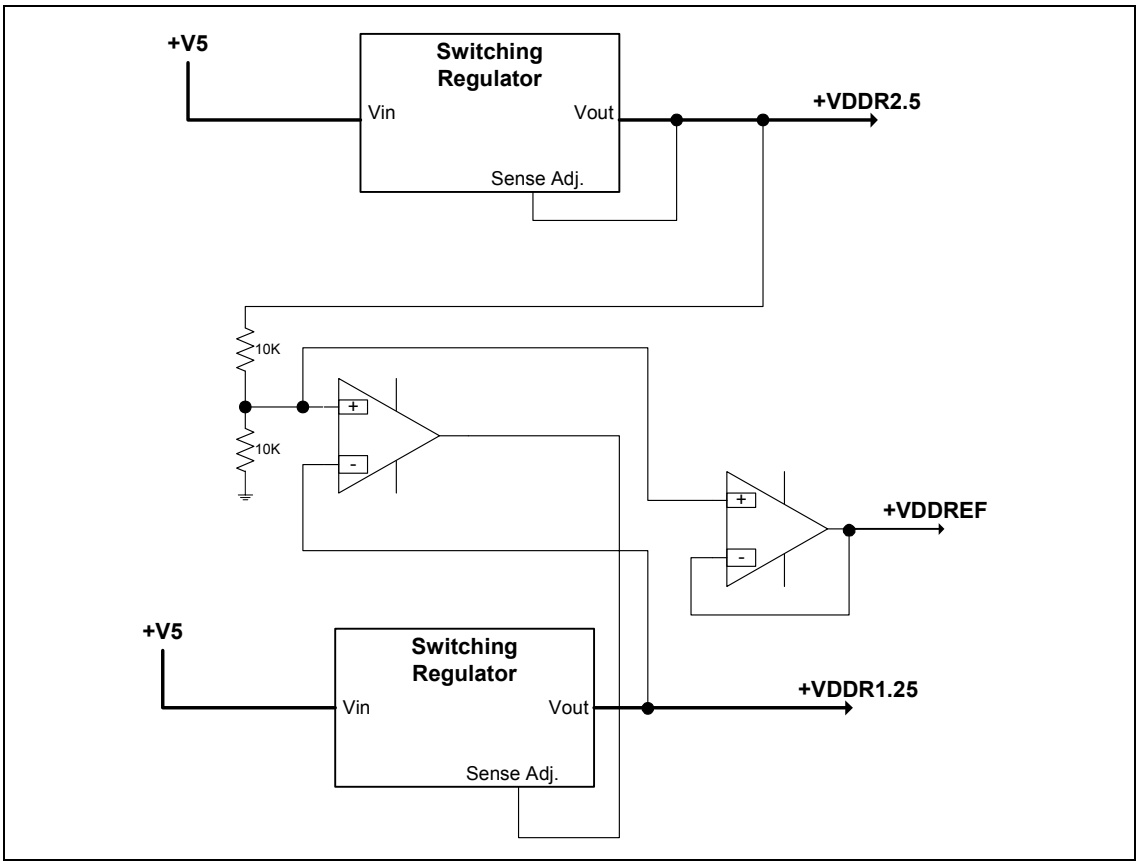
- One 10-µf bulk decoupling cap in a 1206 package placed close to the Vdd generation circuitry.
- Six 0.1-µf high frequency decoupling caps in a 0603-package placed close to the Vdd pins on the Clock driver.
- Three 0.1-µf high frequency decoupling caps in a 0603-package placed close to the VddA pins on the Clock driver.
- One 10-µf bulk decoupling cap in a 1206-package placed close to the VddA generation circuitry

11.7. DDR Power Delivery Design Guidelines

The following sections summarize the DDR system voltage and current requirements as of the release this document. This document is not the original source for these specifications. For more information refer to Section 1.1Related Documentation.

The following guidelines are recommended for a MCH-M DDR system memory design. The main focus of these MCH-M guidelines is to minimize signal integrity problems and improve the power delivery of the MCH-M system memory interface and the DDR SO-DIMMs.

Figure 95. DDR Power Delivery Block Diagram



11.7.1. DDR Memory Bypass Capacitor Guidelines

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5-V discontinuity a minimum of nine, 0603, 0.1-µF, high-frequency bypass capacitors are required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors should connect to 2.5 V and ground. The ground via should be placed as close to the ground pad as possible. The 2.5-V trace should connect to a via that transitions to the 2.5-V copper flood and it should connect to the closet 2.5-V SO-DIMM pin on either the first or second SO-DIMM connector, with a wide trace. The capacitors 2.5-V traces should be distributed as evenly as possible amongst the two SO-DIMMs. Finally, the 2.5-V via should be placed as close to the 2.5-V pad as possible.

11.7.2. 2.5-V Power Delivery Guidelines

The 2.5-V power for the MCH-M system memory interface and the DDR-SO-DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5-V copper flooding to ensure proper MCH-M and SO-DIMM power delivery. This 2.5-V flood must extend from the MCH-M 2.5-V power vias all the way to the 2.5-V DDR voltage regulator and its bulk capacitors, located at the end of the DDR channel beyond the second SO-DIMM connector. The 2.5-V DDR voltage regulator must connect to the 2.5-V flood with a minimum of six vias, and the SO-DIMM connector 2.5-V pins as well as the MCH-M 2.5-V power vias must connect to the 2.5-Vcopper flood. The copper flooding to the MCH-M should include at least seven fingers to allow for the routing of the

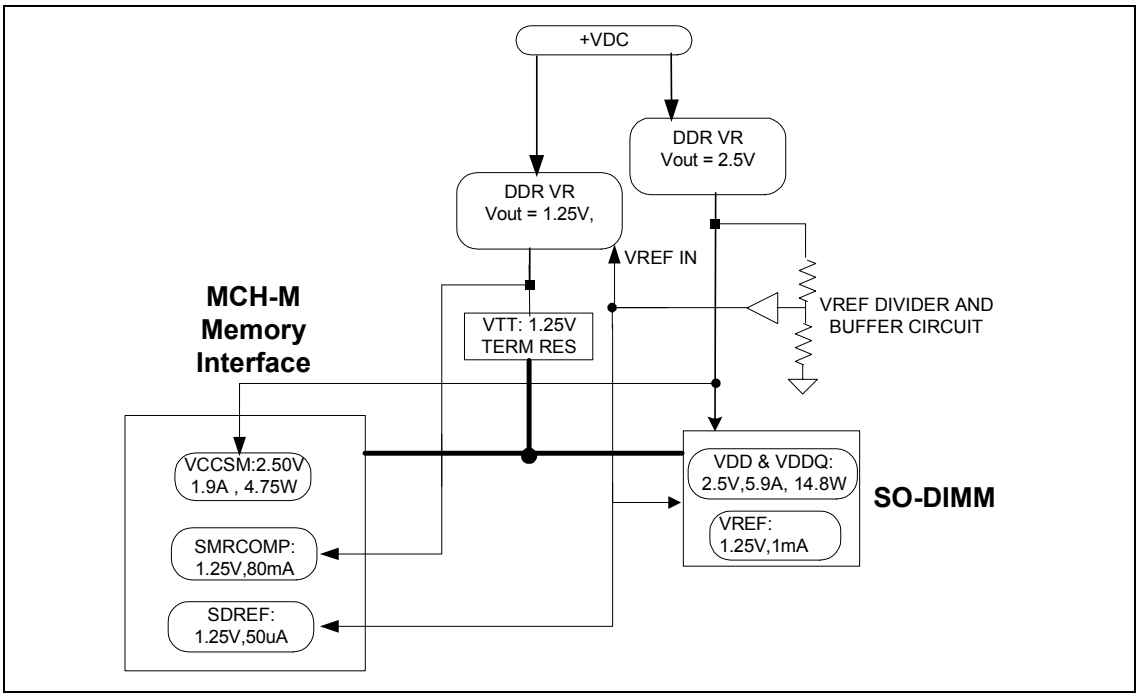
DDR signals and for optimal MCH-M power delivery. The copper fingers must be kept as wide as possible in order to keep the loop inductance path from the 2.5-V voltage regulator to the MCH-M at a minimum. In the areas where the copper flooding necks down around the MCH-M make sure to keep these neck down lengths as short as possible. The 2.5-V copper flooding under the SO-DIMM connectors must encompass all the SO-DIMM 2.5-V pins and must be solid except for the small areas where the clocks are routed within the SO-DIMM pin field where they connect to their specified SO-DIMM pins.

Additionally, a small 2.5-V cooper flood shape should be placed under the MCH-M, to encompass and increase the copper flooding to the back row of 2.5-V MCH-M pins. This flood must not be placed under any of the DDR signals. In order to maximize the copper flooding these signals should be kept as short as possible in order to reduce the amount of serpentining needed in this area on the bottom layer. Also, a minimum of 12-mil isolation spacing should be maintained between the copper flooding and the DDR signals. Finally, the six MCH-M 2.5V high frequency decoupling capacitors, located on the top signal layer, should have their 2.5-V via placed directly over and connected to a separate 2.5-V copper finger. Refer to Section 11.5 for decoupling capacitors.

11.7.3. Intel 845MP/845MZ Chipset DDR Reference Board Power Delivery

Figure 96 shows the power delivery architecture for the Intel 845MP/845MZ Chipset DDR memory subsystem. This power delivery example provides support for the suspend-to-RAM (STR) and the full Power-on State.

Figure 96. Intel 845MP/845MZ Chipset DDR Power Delivery Example



NOTES:

1. Designer must follow following recommendations.
2. VDD & VDDQ (2.5 V) must stay on to drive CKE signals in S3 state.
3. During S3 state VTT and SMRCOMP can be turned off.
4. VTT must have smooth soft start to prevent glitches.
5. VREF(DDR) & SDREF(MCH-M) must stay on to acknowledge the state of CKE signals in S3 state.

Following requirements must be met in order to turn off DDR Vtt in the S3 power state:

MCH-M VCCSM (2.5 V) and SDREF must stay on to drive CKE signals in S3. DDR Vtt must have a smooth soft start to prevent glitches that can affect CKE pins being driven low. DDR Vtt must be stable and within voltage tolerance specification before ICH deasserts reset (PCIRST) to the MCH-M. Optional: Vtt to SMRCOMP can be off in S3 following the same above requirements. Please note MCH-M will enable a weak pull-up when reset is asserted, so the command signals should all be high during S3.

11.7.4. DDR Reference Voltage

The table below has grouped the voltage and current specifications together for each the MCH-M, memory and termination voltage. There are 7 voltages specified here for a DDR VR system. Although, there are only 2 unique voltage regulators for 2.5 V and 1.25 V nominal, each specific power rail described here has a unique specification. Described below are the memory components themselves first

(the top 3 listed) and the MCH-M requirements (next row of 3) and finally the termination voltage and current requirements.

For convenience, tolerances are given in both % and Volts though validation should be done using the spec exactly as it is written. The voltage specs are clearly defined under “Specification Definition”. If this states a tolerance in terms of volts (as Vref says ± 0.050 V) then that specific voltage tolerance should be used, not the a percentage of the measured value. Likewise, percentages should be used where stated. If not stated then either way if fine.

Voltage specs are defined as either “Absolute” or “Relative”. These are described below:

Type Of Specification	Description
Absolute Specification	This is a standard specification most commonly used. This means that the voltage limits are based on a fixed nominal voltage and have a symmetric ± tolerance added to determine the acceptable voltage range. For example, Vdd’s spec does not depend on any other voltage levels. It is simply 2.5 V ± 8%.
Relative Specification	This is a specification whose nominal value is not fixed but is relative to or is a function of another voltage. This means that the other voltage must be measured to know what the nominal value is and then the symmetrical ± tolerance added to that measured value. For example, Vref’s spec depends on the actual value of Vdd to determine Vdd/2 and then tolerance ±0.050 V from this calculated value.

From the table below, it can be seen that only the 2.5-V supply is fixed an absolute specification, whereas all of the 1.25-V nominal supplies are relative to the 2.5-V supply directly or another 1.25-V supply which is then relative to the 2.5-V supply. Due to these 1.25-V relative specifications, it becomes very important that the 1.25-V supply can track the variations in the 2.5V supply and respond according to the 2.5 V variations. This can be implemented as shown in the block diagram in Figure 96 where the 2.5-V output is divided in half and used to generate the 1.25-V reference into the 1.25-V VR controller design. In this manner, the 1.25-V VR will respond proportionally to variations in the 2.5-V supply improving the voltage margin of the relative supply requirements and overall memory system stability.

It should be noted that at launch, all of specifications in this document were current, however it is the current specifications are considered to be higher than actually expected and will be reduced in future specifications.

Table 61. DDR SDRAM Memory Voltage & Current Specification

Name	"Vdd"	"Vddq"	"Vref"	Description
PURPOSE	CORE SUPPLY VOLTAGE, STATIC	I/O SUPPLY VOLTAGE , STATIC	I/O REFERENCE SUPPLY VOLTAGE, STATIC	
SPECIFICATION DEFINITION	Vdd	Vddq	Vref = (Vdd/2) ±0.050 V	((2.5 V+/-8%)/2) ±0.050 V
VOLTAGE Nominal (V)	2.500	2.500	1.250	
TOLERANCE (±%)	8.0%	8.0%	4.0%	
TOLERANCE (±-V)	0.200	0.200	0.050	
MAX ABSOLUTE SPEC VALUE (V)	2.700	2.700	1.400	((2.5 V+8%)/2)+0.050 V
MIN ABSOLUTE PEC VALUE (V)	2.300	2.300	1.100	((2.5 V-8%)/2)-0.050 V
MAX RELATIVE SPEC (calculated from measured "Vdd" value)	na	na	(measuredVdd/2)+0.050 V	
MIN RELATIVE SPEC (calculated from measured "Vdd" value)	na	na	(measuredVdd/2)-0.050 V	
	Idd (max)	Iddq (max)	Iref (max)	
ABSOLUTE MAXIMUM CURRENT REQUIREMENTS	5.000	0.920	0.001	

Table 62. MCH-M DDR Voltage and Current Specifications

Name	"VCCSM"	"SDREF"	"Vtt"= "SMRCOMP"	Description
PURPOSE	MCH-M DDR SUPPLY VOLTAGE (I/O), STATIC	MCH-M REFERENCE SUPPLY VOLTAGE, STATIC	SMRCOMP TERMINATION SUPPLY VOLTAGE, STATIC	
DEFINITION	VCCSM	SDREF=(VCCSM/2) ±2%	Vtt = ("Vref")+/-0.040V	(((2.5 V+/-8%)/2)+/-0.050 V)+/-0.040)
VOLTAGE Nominal (V)	2.500	1.250	1.250	
TOLERANCE (±%)	5.0%	2.0%	3.2%	
TOLERANCE (±V)	0.125	0.025	0.040	
MAX ABSOLUTE SPEC VALUE (V)	2.625	1.339	1.440	(((2.5 V+8%)/2) + 0.050 V)+0.040)
MIN ABSOLUTE SPEC VALUE (V)	2.375	1.164	1.060	(((2.5 V-8%)/2) -0.050 V)-0.040)
MAX RELATIVE SPEC (calculated from measured "VCCSM" value)	na	(measuredVCCSM/2)+ 2%	(measured Vref)+0.04V	
MIN RELATIVE SPEC (calculated from measured "VCCSM" value)	na	(measuredVCCSM/2) - 2%	(measured Vref)-0.040V	
	Ivccsm (max)	Isdref (max)	Ittrc (max)	
ABSOLUTE MAXIMUM CURRENT REQUIREMENTS	1.900	0.010	0.040	

Table 63. Termination Voltage and Current Specifications

Name	"Vtt"	Description
PURPOSE	TERMINATION SUPPLY VOLTAGE, STATIC	
DEFINITION	Vtt = ("Vref")± 0.040 V	(((2.5 V+/-8%)/2) ± 0.050 V) ±0.040
VOLTAGE Nominal (V)	1.250	
TOLERANCE (±%)	3.2%	
TOLERANCE (±V)	0.040	
MAX ABSOLUTE SPEC VALUE (V)	1.440	(((2.5 V+8%)/2)+0.050 V)+0.040
MIN ABSOLUTE SPEC VALUE (V)	1.060	(((2.5 V-8%)/2)-0.050 V)-0.040
MAX RELATIVE SPEC (calculated from measured "VCCSM" value)	(measured Vref)+0.040 V	
MIN RELATIVE SPEC (calculated from measured "VCCSM" value)	(measured Vref)-0.040 V	
	Itt (max)	
ABSOLUTE MAXIMUM CURRENT REQUIREMENTS	2.400	

11.7.4.1. VREF Generation

It may also be noted in Figure 95 that when the 1.25-V reference is generated from the 2.5-V supply a buffer is used. A buffer has also been used to provide this reference to the system for the MCH-M and memory. Specifically, this is the “VREF” signal to the memory and the “SDREF” signal to the MCH-M. Our reference design utilizes this buffer to provide the necessary current to these devices, which the simple resistor divider is not capable of providing. This “SDREF” voltage to the MCH-M has the tightest tolerance in the memory system of ± 2%. Using common 1% resistors consumes 1% of this 2% tolerance. This means SDREF must now be controlled to a 1% tolerance (i.e. be able to divide VCCSM/2 within 1%). A simple resistor divider is not a voltage regulator and is most definitely not a current source. Any current drawn across the resistor divider used to generate this 1.25-V reference will cause a voltage drop across the top resistor that distorts or biases this reference to a lower voltage.

Table 64. MCH-M DDR I/O

NAME	VCCSM[1]	SDREF
PURPOSE	MCH-M DDR SUPPLY VOLTAGE (I/O), STATIC	MCH-M REFERENCE SUPPLY VOLTAGE, STATIC
	VCCSM	SDREF =(VCCSM± 5%) / 2
VOLTAGE Nominal (V)	2.500 "± 5%"	1.250 "± 2%"
TOLERANCE (+/-V)	0.125	0.025
Vmax(V)	2.625	1.275
Vmin(V)	2.375	1.225
	Ivccsm (max)	Isdref (max)
Imax	1.400	0.010

NOTE: MCH-M VREF REQUIREMENTS: the MCH-M core is called "VCCSM" =+2.5 V ±5%. SDREF is ("VCCSM"± 5%) /2 ±2%. This means that whether the 2.5v is 5% high or low, we need to be able to divide that voltage by 2 with a 2% accuracy. This basically means to use 1% resistors, or better.

As shown in Table 64, the max current required by the MCH-M for the SDREF input is 0.010 A. This is too big of a load for a resistor divider. Some sample calculations are shown in the table below. It is not possible to maintain regulation within 2% using a resistive divider without using a resistor so small that the 2.5-V current requirement becomes prohibitive. Hence, a buffer is required due to the 10-mA current requirement of the MCH-M SDREF.

Table 65. Effects of Varying Resistor Values in the Divider Circuit

Rdivider (ohms)	Leakage (A)	Rtop Vdroop (V)	I(2.5) total=2.5v/2R (A)
1	0.01	0.01	1.25
10	0.01	0.1	0.125
100	0.01	1	0.0125
1000	0.01	10	0.00125
10000	*0.01*	*100*	0.000125
100000	0.01	1000	1.25E-05
1000000	0.01	10000	1.25E-06

Rdivider: This is the resistor value selected to form the divider. Assumes both top and values are equal as required for divide by 2.

Leakage: This is the amount of leakage current which needs to sourced from the 2.5-V supply, across the divider's top resistor (Rtop) and out to the MCH-M SDREF input or the DDR VREF input. This current does not go across the bottom resistor.

Rtop Vdroop: This is the resulting voltage droop across Rtop as a result of the leakage current.

I(2.5) total=2.5 V/2R This is the total current through divider. This is calculated to consider the amount of current & power used as a DC current through the divider.

The implementation of a buffer is also required by the DDR. The same VREF may be used for both MCH-M and the DDR as well.

11.7.4.2. DDR VREF Requirements

Making the same calculations for the DDR loading, results to find the max Vref load of 1 mA, a divider is STILL NOT feasible here as the load of 1 mA causes unacceptable drop across even small Rs, which waste power.

Table 66. MCH-M VREF Calculation

NAME	*Vdd*	*Vref*
PURPOSE	CORE SUPPLY VOLTAGE , STATIC	I/O REFERENCE SUPPLY VOLTAGE, STATIC
	Vdd	*Vref = (Vdd=/-8%) / 2*
VOLTAGE Nominal (V)	*2.500*(+/-8%)	*1.250*
TOLERANCE (+/-V)	0.200	0.050
Vmax(V)	2.700	1.300
Vmin(V)	2.300	1.200
	Idd	Iref
Section 11.7.3	*5.000*	*0.001*

Note: The DDR core is called "Vdd" =+2.5 V +/-8% (= ±0.2 V). VREF is ("Vdd"+/-8%)/2 ±50 mV. This means that whether the 2.5 V is 8% high or low, we need to be able to divide ***that voltage*** by 2 within a 50-mV accuracy. This basically means to use 1% resistors, or better.

Table 67. Reference Distortion Due to Load Current

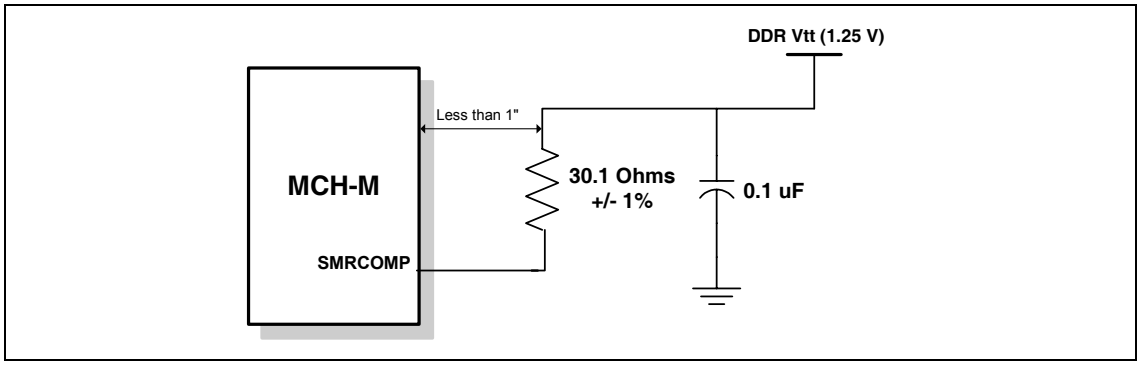
R(ohms)	I(A)	Vdroop(V)	I2.5 total=2.5v/2R(A)
1	0.001	0.001	1.25
10	0.001	0.01	0.125
100	0.001	0.1	0.0125
1000	0.001	1	0.00125
10000	0.001	*10*	0.000125
100000	0.001	100	1.25E-05
1000000	0.001	1000	1.25E-06

Note: As for the MCH-M, a calculation can be made for the DDR. This shows that even with the slight load of 1 mA by the DDR it is still not feasible to use a simple resistor divider. Using the max leakage specs provided today and trying to maintain an error of less than 1%(12.5 mV) one needs to decrease the resistor values such that the current just to source the divider becomes unacceptable. A divider alone does not become an acceptable solution until current requirements are in the 100-µA range. Today, it is not possible to guarantee this type of current requirement for these applications. Hence, the use of a buffer is highly recommended for these reference voltage requirements.

11.7.5. DDR SMRCOMP Resistive Compensation

The MCH-M uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR system memory (SMRCOMP) must be connected to the DDR termination voltage (1.25 V) through a 30 Ω ±1% resistor and one 0603 0.1-µF decoupling capacitor to ground. Place the resistor and capacitor as close to the MCH-M as possible, within 1.0 inch of the MCH-M package. The compensation signal and the VTT trace should be routed with as wide a trace as possible, minimum of 12-mils wide and isolated from other signals with a minimum of 10-mils spacing.

Figure 97. SMRCOMP Recommendation



11.7.6. DDR VTT Termination

All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the MCH-M. Place a solid 1.25-V (VTT) termination island on the top signal layer, just beyond the last SO-DIMM connector. The VTT Termination Island must be at least 50-mils wide. Use this termination island to terminate all DDR signals, using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK are from the same DDR signal group. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer.

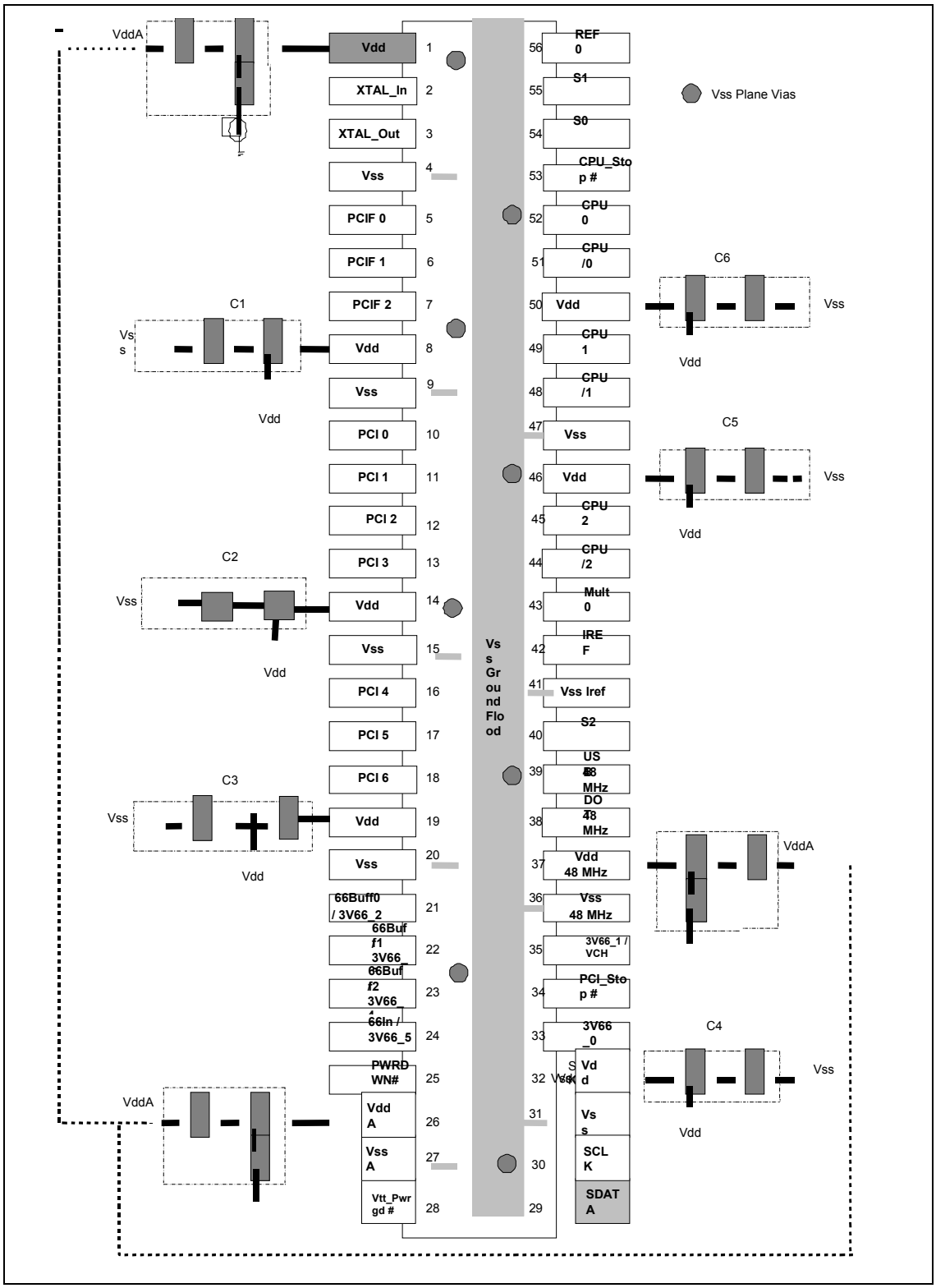
11.8. Clock Driver Power Delivery Design Guidelines

Special care must be taken to provide a quiet VddA supply to the Ref Vdd, VddA and the 48MHz Vdd. These VddA signals are especially sensitive to switching noise induced by the other Vdd's on the cock chip. They are also sensitive to switching noise generated elsewhere in the system such as CPU VRM. The CLC Pie filter should be designed to provide the best reasonable isolation. Intel recommends that a solid ground plane be underneath the clock chip on layer 2. (Assuming top trace is layer 1). It is also recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the Vss pins.

For ALL power connections to planes, decoupling caps and vias , the MAXIMUM trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance. The decoupling caps should be connected as shown in the illustration taking care to connect the Vdd pins directly to the Vdd side of the caps. However the Vss pins should not be connected directly to the Vss side of the caps. Instead they should be connected to the ground flood under the part that is viaed to the ground plane. This is done to avoid Vdd glitches propagating out, getting coupled through the decoupling caps to the Vss pins. This method has been shown to provide the best clock performance.

The ground flood should be viaed through to the ground plane with no less than 12-16 vias under the part. It should be well connected. For all power connections, heavy duty and/or dual vias should be used. It is imperative that the standard signal vias and small traces not be used for connecting decoupling caps and ground floods to the power and ground planes. VddA should be generated by using a CLC filter. This VddA should be connected to the Vdd side of the three capacitors that require it using a hefty trace on the top layer. This trace should be routed from the CLC filter using a star topology.

Figure 98. Decoupling Capacitors Placement and Connectivity



12. System Design Checklist

12.1. Host Interface

Table 68. Resistor Recommendations

Mobile Intel Pentium 4-M – Resistor Recommendations				
Signal	**System Pull-up/ Pull-down**	**Ω**	**Notes**	**✓**
H_A[35:3]#	Connect A[31:3]# to MCH-M. Leave A[35:32]# as No Connect		A[35:32]# are not supported by the chipset. Has internal pull-up to VCC_CORE	
H_RESET#	Pull-up to VCC_CORE	51 Ω ±1%	Place resistor < 0.1" from CPU interface	
H_IERR#	Pull-up to VCC_CORE	10 kΩ	Required pull-up for noise reduction	
H_FERR#	Pull-up to VCC_CORE		Use Voltage Translation Circuit	
COMP[1:0]	Pull-down to GND	51.1 Ω ±1%	Individual pull-down resistor	
CPU_VR_VID [4:0]	Pull-up to V3.3S	1 kΩ		
TESTHI0/BYPASSEN# TESTHI1/H_ODT TESTHI2/H_MCLK0 TESTHI3/ H_MCLK1 TESTHI4/ H_MCLK2 TESTHI5/ H_MCLK3 TESTHI8/H_BR3# TESTHI9/H_BR2# TESTHI10/H_BR1#	Pull-up to VCC_CORE		The TESTHI pins should be tied to the processor VCC using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 ohm, then a value between 40Ω and 60Ω is required. The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group: 1) TESTHI[1:0] 2) TESTHI[5:2] 3) TESTHI[10:8]	
TESTHI6/ITPCLKOUT0 TESTHI7/ITPCLKOUT1			These pins as differential clock for an ITP port designed on the motherboard. if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to VCC using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1-KΩ resistors is required. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC will prevent use of debug interposers.	

Mobile Intel Pentium 4-M – Resistor Recommendations				
Signal	**System Pull-up/ Pull-down**	**Ω**	**Notes**	**✓**
			This implementation is strongly discouraged for system boards that do not implement an onboard debug port. As an alternative, group 2 (TESTHI[5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor VCC. This has no impact on system functionality. TESTHI[0] may also be tied directly to processor VCC if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0] pins, direct tie to VCC is strongly discouraged for system boards that do not implement an onboard debug port.	
MCERR#	NC			
AP[1:0]	NC			
BINIT#	NC			
DP[3:0]	NC			
RSP#	NC			
H_A20M#	Pull-up to VCC_CORE	200 Ω		
H_IGNNE#	Pull-up to VCC_CORE	200 Ω		
H_INTR	Pull-up to VCC_CORE	200 Ω		
H_NMI	Pull-up to VCC_CORE	200 Ω		
H_STPCLK#	Pull-up to VCC_CORE	200 Ω		
H_SMI#	Pull-up to VCC_CORE	200 Ω		
H_DPSLP#	Pull-up to VCC_CORE	200 Ω		
H_CPUSLP#	Pull-up to VCC_CORE	200 Ω		
H_INIT#	Pull-up to VCC_CORE	200 Ω		
H_BR0#	Pull-up to VCC_CORE	220 Ω		
H_BPM[5:0]	Pull-up to VCC_CORE	51 Ω		
PM_CPUPERF#	Terminate to VCC_CORE	200 Ω		
H_PWRGD	Pull-up to	300 Ω		

Mobile Intel Pentium 4-M – Resistor Recommendations				
Signal	System Pull-up/ Pull-down	Ω	Notes	✓
	VCC_CORE			

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

12.2. In Target Probe (ITP)

Table 69. In Target Probe (ITP)

Mobile Intel Pentium 4 Processor-M – ITP (In Target Probe)					
Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes	✓
ITP_TDI	Pull-up to VCC_CORE	150 Ω			
ITP_TDO	Pull-up to VCC_CORE	75 Ω			
ITP_TRST#	Pull-down to GND	680 Ω		If ITP/TAP unused pull-down with 1.5 kΩ	
ITP_PREQ#	Pull-up to VCC_CORE	51 Ω			
ITP_PRDY#	Pull-up to VCC_CORE	51 Ω	240 Ω	Place resistor < 1” from port; Debug port must be at end of trace; See Spec. Update for latest details	
ITP_D_TMS	Pull-up to VCC_CORE	39 Ω		Place resistor < 1” from port; Debug port must be at end of trace	
ITP_D_TCK	Pull-down to GND	27.4 Ω		Place resistor < 1” from port; Debug port must be at end of trace	
ITP_RST#	Pull-up to VCC_CORE	51 Ω +± 1%		Place resistor < 1” from port; Debug port must be at end of trace	
DBRESET#	Pull-up to V3.3	150 Ω			
ITP_POWERON	Pull-up to VCC_CORE	1.5 kΩ			

12.3. Thermal Sensor

Table 70. Thermal Sensor Signals

Mobile Intel Pentium 4 Processor-M – Thermal Sensor				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
ADD[1:0]	Pull-up to V3.3S	1 kΩ		
STBY#	Pull-up to V3.3S	10 kΩ		
SMBDATA	Pull-up to V3.3S	10 kΩ		
SMBCLK	Pull-up to V3.3S	10 kΩ		
THRM_ALERT#	Pull-up to V3.3S	10 kΩ	To enable alert, ALERT# can be connected to THRM# on ICH-M	
DXP, DXN			Route both signals on same layer	

12.4. PLL[2:1] PLC Filter

Table 71. PLL[2:1] RLC Filter

Mobile Intel Pentium 4 Processor-M – PLL[2:1] RLC Filter			
Device	**Value**	**Notes**	**✓**
L	4.7 µH at 80 mA or 10 µH at 60 mA	Rated for DC current > 60 mA	
C	22-100 µF	ESR<0.3 Ω ESL<5 nH Tolerance ± 20%	

12.5. Decoupling Recommendation

Table 72. Decoupling Recommendation

Mobile Intel Pentium 4 Processor-M – High Frequency Decoupling Recommendations*					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
+VCC_CORE	See Processor Power Delivery Design Recommendations	10 µF_6.3 V	38	Use 2-3 vias per pad for reduced inductance during layout. Placement should be near processor for all	

NOTE: *All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution.

12.6. CK-408 Clock Checklist

Table 73. Resistor Recommendation

Checklist Items	Recommendations	Reason/Impact
66_BUFF0	Connect to MCH-M. Series resistor of 33 Ω ± 1%	Refer to the reference schematics.
66_BUFF1	Connect to ICH3-M. Series resistor of 33 Ω ± 1%	Refer to the reference schematics.
66_BUFF2	Connect to AGP. Series resistor of 33 Ω ± 1%	Refer to the reference schematics.
66_INPUT	No Connect.	Refer to the reference schematics.
CPU0		Refer to the reference schematics.
CPU0#		Refer to the reference schematics.
CPU1		Refer to the reference schematics.
CPU1#		Refer to the reference schematics.
CPU2		Refer to the reference schematics.
CPU2#		Refer to the reference schematics.
CPU_STOP#	Connect to ICH3-M STPCPU#	Internal Pull-up
DOT_48 MHz	No Connect	Refer to the reference schematics.
IREF	Terminate to ground through a 475 Ω ± 1% resistor.	Refer to the reference schematics.
MULT0	Brought in through V3.3S coming through a series resistor of 10 kΩ ± 5%	Refer to the reference schematics.
PCI [6:0]	Series resistor of 33 Ω ± 1%	Refer to the reference schematics.
PCIF [2:0]	Series resistor of 33 Ω ± 1%	Refer to the reference schematics.
PCI_STOP# **	Connect to ICH3-M STPPCI#	Refer to the reference schematics.
PWRDWN#	Connect to ANDED SLP_S1# and SLP_S3# powered by non-switch +V3.3.	Refer to the reference schematics.
REF0	Series resistor of 33 Ω ± 5%	Refer to the reference schematics.
SEL_0	Pull up to VCC3_CLK with a 1 K resistor.	Refer to the reference schematics.
SEL_1	Pull down to GND with 1 K resistor.	Refer to the reference schematics.

Checklist Items	Recommendations	Reason/Impact
SEL_2	Pull down to ground through a1 K ± 5% resistor.	Refer to the reference schematics.
SCLK	Connect to SO-DIMMs.	Refer to the reference schematics.
SDATA	Connect to SO-DIMMs.	Refer to the reference schematics.
USB_48MHZ	Connect to ICH3-M. 33 Ω ±5% series resistor	Refer to the reference schematics.
VDD	Connect to VCC3_CLK and decouple with 0.1 µF ±5% value.	Refer to the reference schematics.
VDD_48MHZ	Connect to VCC3_CLK and decouple with 0.1 µF ±5% value.	Refer to the reference schematics.
VDDA	Connect to VCC3_CLK and decouple with 0.1 µF ±5% value.	Refer to the reference schematics.
VSS	Connect to ground.	Refer to the reference schematics.
VSS_48MHZ	Connect to ground.	Refer to the reference schematics.
VSS_IREF	Connect to ground.	Refer to the reference schematics.
VTT_PWRGD#	Connect to inverted and delayed VCC_CORE pwrgd	
XTAL_IN		Refer to the reference schematics.
XTAL_OUT		Refer to the reference schematics.

12.7. DDR SO-DIMM0 Connector

Table 74. DDR S0-DIMM0 Recommendations

Checklist Items	Recommendations	Reason/Impact
S#[0]	Connect to SCS#[0] pin on MCH-M Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
S#[1]	Connect to SCS#[1] pin on MCH-M Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CKE[0]	Connect to the MCH-M SCKE[0] pin Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CKE[1]	Connect to the MCH-M SCKE[1] pin Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
A[12:0]	Connect to the MCH-M SMA[12:0] pins Connect to SO-DIMM1 with a 10 Ω ± 5% resistor	Refer to the reference schematics.
RAS#	Connect to the MCH-M SRAS# pin Connect to SO-DIMM1 with a 10 Ω ± 5% resistor	Refer to the reference schematics.
CAS#	Connect to the MCH-M SCAS# pin Connect to SO-DIMM1 with a 10 Ω ± 5% resistor	Refer to the reference schematics.
WE#	Connect to the MCH-M SWE# pin Connect to SO-DIMM1 with a 10 Ω ± 5% resistor	Refer to the reference schematics.
BA[1:0]	Connect to the MCH-M SBS[1:0] pins Connect to SO-DIMM1 with a 10Ω ± 5% resistor	Refer to the reference schematics.
DQ[63:0]	Connect to MCH-M SDQ[63:0] signals through 22 ohm ± 5% series resistors Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25V DDR Termination Voltage)	Refer to the reference schematics.
CB[7:0]	Connect to MCH-M SCB[7:0] signals through 22 ohm ± 5% series resistors Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	For systems not implementing ECC SO-DIMMS CB[7:0] can be left as no connect
DQS[8:0]	Connect to MCH-M SDQS[8:0] signals through 22 ohm ± 5% series resistors Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	For systems not implementing ECC SO-DIMMS DQS[8] can be left as no connect

Checklist Items	Recommendations	Reason/Impact
DM[8:0] / DQS[17:9]	Connect to Ground	Refer to the reference schematics.
CK[2:0]	Connect to the MCH-M SCK[2:0] pins	Refer to the reference schematics.
CK#[2:0]	Connect to the MCH-M SCK#[2:0] pins	Refer to the reference schematics.
SA[2:0]	Connect to ground.	Refer to the reference schematics.
SDA SCL	Connect to SMB_DATA and SMB_CLK with 10 KΩ resistor pull-ups to +V3.3Always	Refer to the reference schematics.
VDD	Connect to DDR 2.5 V	Refer to the reference schematics.
VDDQ	Connect to DDR 2.5 V	Refer to the reference schematics.
VREF	Connect to DDR Reference Voltage (Vref) Connect to a 0.1 µF capacitor tied to ground	Refer to the reference schematics.
VSS	Connect to ground.	Refer to the reference schematics.
VDDSPD	Serial EEPROM positive power supply (wired to a separate pin at the connector, which supports operation from a minimum of 2.3 V to a maximum of 3.6 V). This pin is isolated from the Vdd/Vddq supply voltages. Recommend connecting this to 3.3VAlways	Refer to the reference schematics.
VDDID	No Connect.	Refer to the reference schematics.

12.8. DDR SO-DIMM1 Connector

Table 75. DDR S0-DIMM0 Recommendations

Checklist Items	Recommendations	Reason/Impact
S#[0]	Connect to SCS#[2] pin on MCH-M Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
S#[1]	Connect to SCS#[3] pin on MCH-M Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CKE[0]	Connect to the MCH-M SCKE[2] pin Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CKE[1]	Connect to the MCH-M SCKE[3] pin Connect to a 56 ohm ± 5% parallel termination resistor tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
A[12:0]	Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
RAS#	Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CAS#	Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
WE#	Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
BA[1:0]	Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
DQ[63:0]	Connect to the MCH-M SDQ[63:0] pins through 22 ohm ± 5% series resistors described in Sect. 6 Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	Refer to the reference schematics.
CB[7:0]	Connect to the MCH-M SCB[7:0] pins through 22 ohm ± 5% series resistors described in Sect. 6 Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage)	For systems not implementing ECC SO-DIMMS CB[7:0] can be left as no connect
DQS[8:0]	Connect to the MCH-M SDQS[8:0] pins through 22 ohm ± 5% series resistors described in Section 6. Connect to a 56 ohm ± 5% parallel termination resistors tied to Vtt (1.25 V DDR Termination Voltage).	For systems not implementing ECC, SO-DIMMS DQS[8] can be left as no connect.
DM[8:0] / DQS[17:9]	Connect to Ground	Refer to the reference schematics.
CK[2:0]	Connect to the MCH-M SCK[5:3] pins	Refer to the reference schematics.
CK#[2:0]	Connect to the MCH-M SCK#[5:3] pins	Refer to the reference schematics.

Checklist Items	Recommendations	Reason/Impact
SA[2:0]	Connect SA2 and SA1 to ground Connect SA0 to V3.3S	Refer to the reference schematics.
SDA SCL	Connect to SMB_DATA and SMB_CLK with 10KΩ resistor pull-ups to +V3.3Always	Refer to the reference schematics.
VDD	Connect to DDR 2.5 V	Refer to the reference schematics.
VDDQ	Connect to DDR 2.5 V	Refer to the reference schematics.
VREF	Connect to DDR Reference Voltage (Vref) Connect to a 0.1-µF capacitor tied to ground	Refer to the reference schematics.
VSS	Connect to ground.	Refer to the reference schematics.
VDDSPD	Serial EEPROM positive power supply (wired to a separate pin at the connector, which supports operation from a minimum of 2.3 V to a maximum of 3.6 V). This pin is isolated from the Vdd/Vddq supply voltages. Recommend connecting this to 3.3VAlways	Refer to the reference schematics.
VDDID	No Connect.	Refer to the reference schematics.

Table 76. DDR Extra

Checklist Items	Recommendations	Reason/Impact
RCVENOUT#	Connect to MCH-M RCVENIN# pin	
RCVENIN#	Connect to MCH-M RCVENOUT# pin	
VCCSM[38:0]	Connect MCH-M VCCSM pins to 2.5 V	
SDREF	Connect to DDR Reference Voltage (Vref) Connect to a 0.1-µF capacitor tied to ground	

12.9. MCH-M Signals

Table 77. Processor System Bus Signals

MCH-M – Processor System Bus (PSB) Signals				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
H_D#[63:0], H_A#[31:3], H_REQ#[4:0], H_RS#[2:0]			Route all signals between processor and MCH-M with board trace impedance	
H_RESET#			Route all signals between processor and MCH-M with 55 Ω ± 1% trace impedance; Also drives H_RESETX w/ 0 Ω series damping	
H_ADS#, H_BNR#, H_BPRI#, H_DBSY#, H_DEFER#, H_DRDY#, H_HIT#, H_HITM#, H_LOCK#, H_TRDY#			Route all signals between processor and MCH-M with 55 Ω ± 1% trace impedance	
H_XRCOMP H_YRCOMP	Connect to GND	24.9 Ω ±1%	Referencing a 50-Ω buffer impedance	
SCK6/CLK6, SCK#6/CLK7, SCK7/CLK10, SCK#7/CLK11, SCK8/CLK9, SCK#8/CLK8			No Connect No Connect No Connect No Connect No Connect No Connect	
HXSWING				
HYSWING				

NOTE: Please refer to Customer Reference Board schematic for SCKE[3:0] connection. Also SCS#[5:4] are NC. Intel does not support SCS[5:4].

Table 78. Miscellaneous Signals

MCH-M – Miscellaneous Signals				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
AGP_RCOMP	Connect to GND	36.5 Ω ± 1%	For AGP devices Referencing a 55-Ω board impedance	
HUB_RCOMP	Pull-up to VCC1_8	36.5 Ω ± 1%	Referencing a 55-Ω board impedance	
SMRCOMP	Connect to DDR Termination Voltage (Vtt) through a 30.1 Ω ± 1% pull-up resistor. Connect to a 0.1-µF capacitor tied to ground.			

Table 79. Decoupling Recommendation

MCH-M – High Speed Decoupling Recommendations					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
HUB_VREF	Decouple to GND	0.01 µF	1	Place close to MCH-M	
SM_VREF	Decouple to GND	0.1 µF	1	Place as close as possible to the MCH-M SDREF Input (J21/J9)	
+VCC_CORE (VTTFSB)	Decouple to GND Decouple to GND	0.1 µF 10.0 µF	10 3	Distribute as close as possible to MCH-M VTTFSB Quadrant	
+V1.5S_MCH (VCCAGP)	Decouple to GND Decouple to GND	0.1 µF 10.0 µF 100 µF	6 2 1	Distribute as close as possible to MCH-M AGP/Core Quadrant	
+V1.8S_MCH (VCCHL)	Decouple to GND Decouple to GND	0.1 µF 10 µF	3 1	Distribute as close as possible to MCH-M Hub Interface Quadrant	
+V2.5 for MCH	Decouple to GND	0.1 µF 22.0 µF 100 µF 150 µF	6(min) 2 3	Distribute as close as possible to MCH-M System Memory Quadrant;	
+V2.5 for DDR	Decouple to GND	0.1 µF 100 µF 150 µF	9(min) 4 5	One 0.1 µF cap per power pin. Place each cap close to DDR pin.	
+V1.25V	Decouple to GND	0.1 µF	54(min)	Place one cap close to every 2 pull up resistors termination.	

NOTE: Please check on Low Frequency Decoupling values for the 2.5 DDR and 2.5 MCH-M.

Table 80. Reference Voltage Dividers

MCH-M – Reference Voltage Dividers*					
Signal	**System Pull-up/Pull-down**	**Ω**	**F**	**Notes**	**✓**
SM_VREF					
HUB_VREF	Voltage divider with w/ cap and 0 Ω in parallel to bottom resistor	301 Ω ± 1% (both)	0.01 µF	Place divider pair in middle of bus. Divided voltage is [1/2]*1.8 V.	

12.10. AGP

Table 81. Resistor Recommendation

AGP – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
AGP_SBSTB# AGP_ADSTB[1:0]#				Have internal pull-downs.	
ST[0]	Pull-down to GND	2 kΩ		ST[0] signal pulled low indicates that system memory is DDR SDRAM	
ST[2:1]	Pull-up to V1.5S	8.2 kΩ		It is required that ST[2:1] have site for external pull-down resistor to ground, but the resistor should not be populated.	
AGP_PERR# AGP_SERR#	Pull-up to V1-5S	8.2 kΩ			
AGP_PIPE# AGP_GNT# AGP_ADSTB[1:0] AGP_SBSTB AGP_FRAME# AGP_TRDY# AGP_STOP# AGP_DEVSEL# AGP_IRDY# AGP_RBF# AGP_REQ# AGP_WBF#				Have internal pull-ups.	
AGP_BUSY#	Pull-up to V3_3S_ICH	10 kΩ		Connect to ICH AGP_BUSY# pin AGPBUSy# must be connected to AGP Graphics controller supporting AGP Busy/Stop protocol	
STP_AGP#				Connect to ICH C3_STAT# pin	

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Table 82. Decoupling Recommendation

AGP– High Speed Decoupling Recommendations*					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
AGP_VREF	Decouple to GND	0.1 µF	2	Place one capacitor near MCH-M and one near AGP connector	
+V1-5S_AGP	Decouple to GND	150 µF 0.1 µF 22 µF	2 7 1	Distribute as close as possible to AGP connector VDDQ and VDDQ1.5 Quadrants	
+V3S_AGP	Decouple to GND	100 µF 0.1 µF 22 µF	1 3 2	Distribute as close as possible to AGP connector VCC3.3 Quadrant	
+V5S_AGP	Decouple to GND	0.1 µF 22 µF	2 1	Distribute as close as possible to AGP connector V5.0 Pins	
+V12S	Decouple to GND	0.1 µF	1	Distribute as close as possible to AGP connector 12 V Pin	

Table 83. Reference Voltage Dividers

AGP– Reference Voltage Dividers*				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
AGP_VREF		1 kΩ (Each resistor in divider)	Place in between video controller and MCH-M. (1/2)VDDQ to video controller and MCH-M.	

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution.

12.11. ICH3-M Checklist

Table 84. PCI Resistor Recommendation

ICH3-M – PCI Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
PCI_FRAME#, PCI_IRDY#, PCI_TRDY#, PCI_STOP#	Pull-up to V3.3S	8.2 kΩ		Alternative system can be 2.7 kΩ pull-up to V5S	
PCI_PERR#, PCI_SERR#, PCI_DEVSEL#, PCI_LOCK#	Pull-up to V3.3S	8.2 kΩ		Alternative system can be 2.7 kΩ pull-up to V5S	
PCI_GPIO0/ REQA#, PCI_GPIO1/ REQB#/REQ5#, PCI_REQ#[4:0]	Pull-up to V3.3S	8.2 kΩ		Alternative system can be 2.7 kΩ pull-up to V5S	
PCI_RST#			22 Ω or 33 Ω	Should be buffered to form IDE_RST# for improved signal integrity	
PCI_PME#				Has integrated pull-up	
PCI_GNT#[4:0]	External pull-up not required. If external resistors implemented, they must be pulled up to V3.3S				
PCI_GPIO16/ GNTA#, PCI_GPIO17/ GNTB#/GNT5#				Has integrated pull-up; GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull down resistor can be added to manually enable the function.	
INT_IRQ[15:14], INT_SERIRQ	Pull-up to V3.3S	8.2 kΩ		Open drain signal.	
INT_PIRQ[D:A]#	Pull-up to V3.3S	8.2 kΩ		Alternative system can be 2.7 kΩ pull-up to V5S	
INT_PIRQ[H:E]#/ GPIO[5:2]	Pull-up to V3.3S	8.2 kΩ		Alternative system can be 2.7 kΩ pull-up to V5S	
INT_APICD[1:0]	Connect to GND	10 kΩ		Connect both signals through one 10 kΩ resistor	
INT_APICCLK	Connect to GND				

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Table 85. System Management Interface (SM-BUS)

ICH3-M – System Management Interface				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
SM_LINK[1:0]	Pull-up to V3_3ALWAYS	4.7 kΩ		
SM_INTRUDER#	Pull-up to V3_3ALWAYS	100 kΩ	Pull signal to VCCRTC (VBAT) if not needed	
SMB_ALERT#/ GPIO11	Pull-up to V3_3ALWAYS	10 kΩ	Pull-up only if using this signal as SMB_ALERT#	
SMB_CLK, SMB_DATA	Pull-up to V3_3ALWAYS	10 kΩ		

Table 86. AC '97 Interface

ICH3-M – AC '97 Interface					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
AC_BITCLK				Has internal pull-down 20 kΩ enabled only when AC_SHUT bit is set to 1	
AC_SYNC			33 Ω	No extra pull-down resistors required. Some implementations add termination for signal integrity.	
AC_SDATAIN [1:0]				External pull-down not required	
AC_SDATAOUT				Has internal pull-down 20 kΩ enabled only when AC_SHUT bit is set to 1	

Table 87. Power Management Interface

ICH3-M – Power Management Interface					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
PM_CLKRUN#/ GPIO24	Pull-up to V3.3S	10 kΩ			
PM_RI#	Pull-up to V3_3ALWAYS	8.2 kΩ			
PM_THRM#	Pull-up to V3.3S	8.2 kΩ		Pull-up required only if temperature sensor not used; Alternative system can be 2.7 kΩ to V5S; External pull-up/down not required if connecting to temperature sensor	

ICH3-M – Power Management Interface					
Signal	**System** **Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
DPRSLPVR , PM_SLP_S3#, PM_SLP__S5#				External pull-up/down not required.	
PM_PWRBTN#				Has integrated pull-up of 24 kΩ	
PM_LANPWROK , PM_RSMRST#				Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_8 have reached their nominal voltages Refer to the reference schematics.	
PWROK	This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both V_{CC}3_3 and V_{CC}1_8 have reached their nominal voltages.	8 KΩ-22 KΩ		RTC well input requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3.	

Table 88. LPC Interface

ICH3-M – LPC Interface				
Signal	System Pull-up/Pull-down	Ω	Notes	✓
LPC_AD[3:0], LPC_DRQ#[1:0]			Has integrated weak internal pull-up	

Table 89. USB Interface

ICH3-M – USB Interface					
Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes	✓
USB_RBIAS	Pull-down to GND	18.2 Ω ± 1%		22.6 Ω for ICH3-M B0 ES Samples only	
HUB_VREF					

12.12. HUB Interface

Table 90. Decoupling Recommendation

ICH3-M – Hublink Decoupling Recommendations*					
Signal	Configuration	F	Qty	Notes	✓
HUB_VREF	Pull-down to GND	0.01 µF	1 ea.		
HUB_VSWING	Pull-down to GND	0.1 µF	1 ea.		

Table 91. Reference Recommendation

ICH3-M – Hublink Reference Voltage Dividers*				
Signal	System Pull-up/Pull-down	Ω	Notes	✓
HUB_VSWING	Voltage divider w/ bottom resistor parallel to RC in series (0.1 µF)	301 Ω ±1% (for both)	Place divider pair in middle of bus; Range for voltage divider resistors: 100 Ω – 1 kΩ	

NOTE: *All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution.

Table 92. RTC Circuitry

ICH3-M – RTC Circuitry Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
CLK_VBIAS	Connect 10 MΩ across to CLK_RTCX1 and 0.047 µF decoupling cap in series with 1 kΩ	10 MΩ 1 kΩ	Cap for noise immunity This DC Voltage is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. VBIAS should be at least 200 mV DC.	
CLK_RTCX1, CLK_RTCX2	Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor and use 12 pF decoupling caps at each signal.	10 MΩ	Refer to reference schematics. RTCX1 may optionally be driven by an external oscillator, instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3-V source. Circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.	

NOTES:

1. Connect supply clock inputs to X1 and X2 of the ICH3-M because other signals are gated off that clock in suspend modes. However, in this case, the frequency (32.768 kHz) of the clock inputs is not critical; a lower-cost crystal can be used or a single clock input can be driven into X1 with X2 left as no connect
2. To maintain RTC accuracy, the external capacitor C3 needs to be 0.047 µF and capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Table 93. LAN Interface

ICH3-M – LAN Interface Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
LAN_JCLK			No resistor required; If LAN interface not used, leave unconnected (NC)	
LAN_RXD[2:0]			No resistor required, has integrated weak internal pull-up; If LAN interface not used, leave unconnected (NC)	
LAN_TXD[2:0], LAN_RSTSYNC	See notes		Connect to LAN_TXD on Platform LAN Connect Device. If LAN interface not used, leave unconnected (NC).	

Table 94. Decoupling Recommendation

ICH3-M – High Speed Decoupling Recommendations					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
+VCC_CORE	Pull-down to GND	0.1 µF 1.0 µF, 16 V	2 1	Place close to ICH3-M VCCPCPU pins as possible.	
+V1.8S	Pull-down to GND	0.1 µF 22 µF 100 µF	7 1 1	Place as close as possible to the ICH3-M VCCPHL and VCCCORE Quadrants	
+V1.8Always	Pull-down to GND	0.1 µF 10 µF	3 1	Place as close as possible to the ICH3-M VCCSUS Quadrant and one between balls C23 and B23	
+V1.8	Pull-down to GND	0.1 µF 22 µF	2 1	Place as close as possible to the ICH3-M VCCAUX Quadrant	
+V3.3S	Pull-down to GND Pull-down to GND	0.1 µF 22 µF	12 2	Place as close as possible to the ICH3-M VCCPPCI Quadrant	
+V3.3Always	Pull-down to GND	0.1 µF 22 µF	8 1	Place as close as possible to the ICH3-M VCCPUSB and VCCPSUS Quadrants	
+V3.3	Pull-down to GND	0.1 µF 4.7 µF 22 µF	2 1 1	Place as close as possible to the ICH3-M VCCPAUX Quadrant	

Table 95. Reference Voltage Dividers

ICH3-M – Reference Voltage Dividers*				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
+V5S_ICHREF	Pull-up to V5S	Note		

NOTE: *All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution.

Table 96. ICH3-M Miscellaneous Signals

ICH3-M – Reference Voltage Dividers*				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
SPKR			Has integrated pull-down; Integrated pull-down is only enabled at boot/reset for strapping functions, otherwise disabled	

12.13. USB Checklist

Table 97.Resistor Recommendations

USB – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
USB_PN[5:0], USB_PP[5:0]				Place near ICH3-M	
USB_OC[5:0]	Pull-up to V3.3Always	10 kΩ		Pull-up voltage rail will depend on usage	

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Table 98. Decoupling Recommendations

USB – Decoupling Recommendations*					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
USBPWRCONN [D:A]	Pull-down to GND	0.1 µF 100 µF_16V	1 ea.		
+V5_USB[2:1]	Pull-down to GND	0.01 µF	1 ea.		

NOTE: *All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution.

12.14. FWH Checklist

Table 99. Resistor Recommendations

FWH – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
FGPI[4:0]				Configuration different depending on implementation. Terminate to GND with 10 kΩ resistor if not used.	
INIT#	Pull-up to V3_3S	See note		Configuration depends on FWH implementation	
IC	Pull-down to GND	10 kΩ			

12.15. LAN/HomePNA Checklist

Table 100. LAN – Resistor Recommendations

LAN – Resistor Recommendations*					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
RBIAS100	Pull-down to GND	619 Ω +/-1%			
RBIAS10	Pull-down to GND	549 Ω +/-1%			
TDP, TDN		100 Ω +/-1%		Crossover resistor	
RDP, RDN		124 Ω +/-1%		Crossover resistor	
RJ45_7, RJ45_4	Pull-down	75 Ω +/-1%			
RJ45_SPDLED#, RJ45_ACTLED#			470 Ω		
ISOL_TCK, ISO_TI, ISOL_EX, TESTEN	Pull-up to V3.3	10 kΩ			

12.16. EEPROM Interface

Table 101. EEPROM Interface Recommendation

Checklist Items	Recommendations	Reason/Impact
EE_DOUT	Prototype Boards should include a placeholder for a pull-down resistor* on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.	ICH3-M contains integrated pull-up resistor for this Signal. Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH3-M perspective.)
EE_DIN	No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector.	ICH3-M contains integrated pull-up resistor for this Signal. Connected to EEPROM data output signal. (Output from EEPROM perspective and input from ICH3-M perspective.)

NOTE: * If resistor is stuffed the value is 1 Kohm 5%

12.17. Interrupt Interface

Table 102. Interrupt Interface Recommendation

Checklist Items	Recommendations	Reason/Impact
PIRQ[D:A]#	These signals require a pull-up resistor. Recommend a 2.7 KΩ pull-up resistor to VCCV_{CC}5 or 8.2 KΩ to V_{CC}CC3_.3.	In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register.
PIRQ[H:E]#/GPIO[5:2]	These signals require a pull-up resistor. Recommend a 2.7 KΩ pull-up resistor to VCCV_{CC}5 or 8.2 KΩ to V_{CC}CC3_.3.	In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register.
SERIRQ	External weak (8.2 KΩ) pull-up resistor to V_{CC}CC3_.3 is recommended.	Open drain signal

12.18. GPIO

Table 103. GPIO Recommendation

Checklist Items	Recommendations	Reason/Impact
GPIO Balls	**GPIO[7, 5:0]:** • These balls are in the Main Power Well. Pull-ups must use the $V_{CC}3\_3$ plane. • Unused core well inputs must be pulled up to $V_{CC}3\_3$. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO[1] can be used as PCI REQ[5]#. • GPIO[5:2] can be used as PIRQ[H:E]#. • These signals are 5V tolerant **GPIO[8] & [13:11]:** • These balls are in the Resume Power Well. Pull-ups go to $V_{CC}Sus3\_3$ plane. • Unused resume well inputs must be pulled up to $V_{CC}Sus3\_3$. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5V tolerant. • GPIO[11] can be used as SMBALERT#. **GPIO[24:16]:** • Fixed as output only. Can be left NC. • In Main Power Well ($V_{CC}3\_3$). • GPIO[22] is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO[17] can be used as PCI GNT[5]#. • GPIO[18] / STP_PCI# • GPIO[19] / SLP_S1# • GPIO[20] / STP_CPU# • GPIO[21] can be used as C3_STAT# • GPIO[22] / CPUPERF# • GPIO[23] / SSMUXSEL **GPIO[28,27,25,24]:** • I/O balls. Default as outputs. Can be left NC. • GPIO[24]/CLKRUN# • From resume power well ($V_{CC}Sus3\_3$). • GPIO[24] / CLKRUN#† (Note: use pull-up to $V_{CC}3\_3$ if this signal is pulled-up) **GPIO[43:32]:** • I/O balls. From main power well ($V_{CC}3\_3$). Default as outputs when enabled as GPIOs.	*Ensure ALL unconnected signals are OUTPUTS ONLY!* These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register. Main power well GPIO are 5 V tolerant, except for GPIO[43:32]. Resume power well GPIOs are not 5 V tolerant. Muxed pins with Power Management functionality are used for their respective power management functions

12.19. CPU Signals

Table 104. CPU Signals

Signal Group	Recommendation	Reason
FERR#,IERR#,PROCHOT#, *THRMTRIP#	**Translation circuit is required between CPU and ICH3 Pullup at Rtt_CPU=56_5% Pullup at Vcc_Rcvr=300_5%	Voltage translation
LINT1/INTR, LINT0/NMI, DPSLP#, SLP#, STPCLK#, IGNNE#, SMI#, A20M#, CPUPERF#	Pullup 200 Ohm_5% to Vtt_CPU	VCC_CORE<1.3 V
PWRGOOD	Pullup 300 Ohm_5% to Vtt_CPU	VCC_CORE<1.3 V
INIT#	**Translation circuit is required between ICH3 and FWH Pullup at Rtt_CPU=200_5% Rtt_FWH=300_5%	

12.20. IDE Checklist

Table 105. IDE Checklist

Checklist Items	Recommendations	Reason/Impact
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 KΩ pull-down resistor. Refer to ATA ATAPI-4 specification.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33Ω, but can range from 31 Ω to 43 Ω.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but can range from 31 Ω ohms to 43 Ω.
PDREQ, SDREQ	No extra series termination resistors. No pull-down resistors needed.	These signals have integrated series resistors in the ICH3. These signals have integrated pull-down resistors in the ICH3-M.
PIORDY, SIORDY	No extra series termination resistors. Pull up to $VCCV_{CC}3.33\_3$ via a 4.7 KΩ resistor.	These signals have integrated series resistors in the ICH3-M.
IRQ14, IRQ15	Recommend 8.2 KΩ—10 KΩ pull-up resistors to $VCCV_{CC}3.33\_3$. No extra series termination resistors.	Open drain outputs from drive.

12.21. HomePNA - Resistor Recommendation

Table 106. HomePNA - Resistor Recommendation

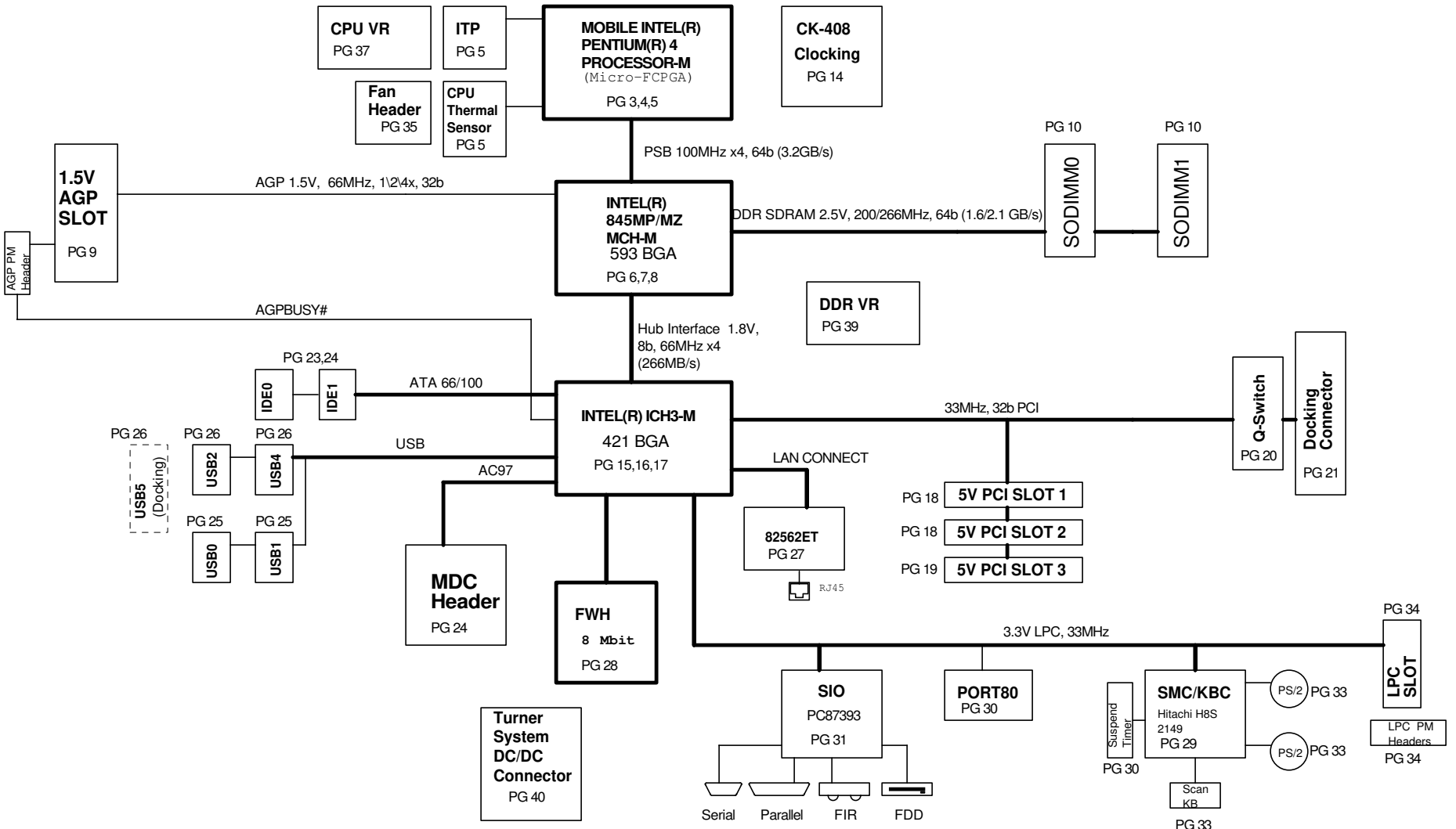
HomePNA – Resistor Recommendations*					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
TX_EN, MDC, MDIO, ISOLATE, HMII/JORD	Pull-down to GND	1 kΩ			
XO	Pull-down	121 Ω ± 1%		With crossover resistor 10 kΩ to XI	
RX_TX_P, RX_TX_N	Pull-up	51.1 Ω ± 1%			
TEST_EN	Pull-down to GND	1 K			
LEDA_L, LEDL_L	Pull-up	470 Ω			
PHAD4/GPSI	Pull-down to GND	10 kΩ			

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

13. Customer Reference Board Schematics

See the following page for the customer reference board schematics.

INTEL (R) 845MP/MZ PLATFORM SCHEMATICS



Title	BLOCK DIAGRAM
Project:	845MP/MZ Platform
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

+VDC	Primary DC system power supply (10 to 17V)
+VCC_CORE	Core voltage for CPU
+VCC_VID	1.2V For CPU PLL and VID circuitry
+V1.25	DDR Termination voltage
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.8ALWAYS	1.8V always on power rail
+V1.8	1.8V power rail (off in S4-S5)
+V1.8S	1.8V switched power rail (off in S3-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)
-V12S	-12.0V switched power rail for PCI (off in S3-S5)

PCI Devices

Device	IDSEL #	REQ/GNT #		Interrupts	PC/PCI
Slot 1	AD25	1	1	A, B, C, D	A
Slot 2	AD26	2	2	B, C, D, A	A
Slot 3	AD27	3	3	C, D, A, B E, F, G, H	A
Docking	AD28	4	4	B, C, D, A	B
AGP	(AD17 internal)			A, B	
LAN	(AD24 internal)				
USB	AD29				
Hub to PCI	AD30				
LPC bridge/IDE/AC97/SMBus	AD31				

DDR Termination:

Address/Command	MA, BS#, RAS#, CAS#, WE#	1 Series and 1 Parallel
DATA	DQS, DATA, CB	1 Series and 1 Parallel
Control	CKE, CS#	1 Series and 1 Parallel

Power States

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+V3ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	LOW
S4 (Suspend To Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

I²C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH
SO-DIMM0	1010 0000	A0	SMB_ICH
SO-DIMM1	1010 0001	A2	SMB_ICH
Thermal Diode	1001 110x	9C	SMB_THRM
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB

Net Name Suffix

\# = Active Low signal

LED	Page	Ref
Primary IDE	24	DS27
Secondary IDE	24	DS24
SMC/KBC NUMLOCK	29	DS2
SMC/KBC SCROLL LOCK	29	DS1
SMC/KBC CAPS LOCK	29	DS3
SMC/KBC INIT CLOCK	24	DS26

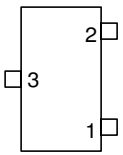
SW	Page	Ref
ON/OFF	40	SW5
LID	29	SW3
DIP SWITCH	36	SW4
RESET	40	SW6
VIRTUAL BATTERY	29	SW2

Default Jumper Settings			Page
J2	1-X	KBC 60/64 DECODE DISABLE	29
J8	1-X	INIT CLK DISABLE	30
J11	1-2	KSC DISABLE	29
J12	1-2	LAN PHYCLK Disable	27
J21	2-3	WMT-N/Northwood Select	36
J22	1-X	KSC Programming	29
J27	1-X	KSC Programming	29
J38	2-3	WMT-N/Northwood Select	36
J49	1-2	SIO Disable	31
J51	1-2	CPU VR Phase num Select	37
J75	1-X	CMOS CLEAR	16
J81	2-3	AGP Reset Default	9

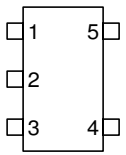
PCB Footprints

As seen from top

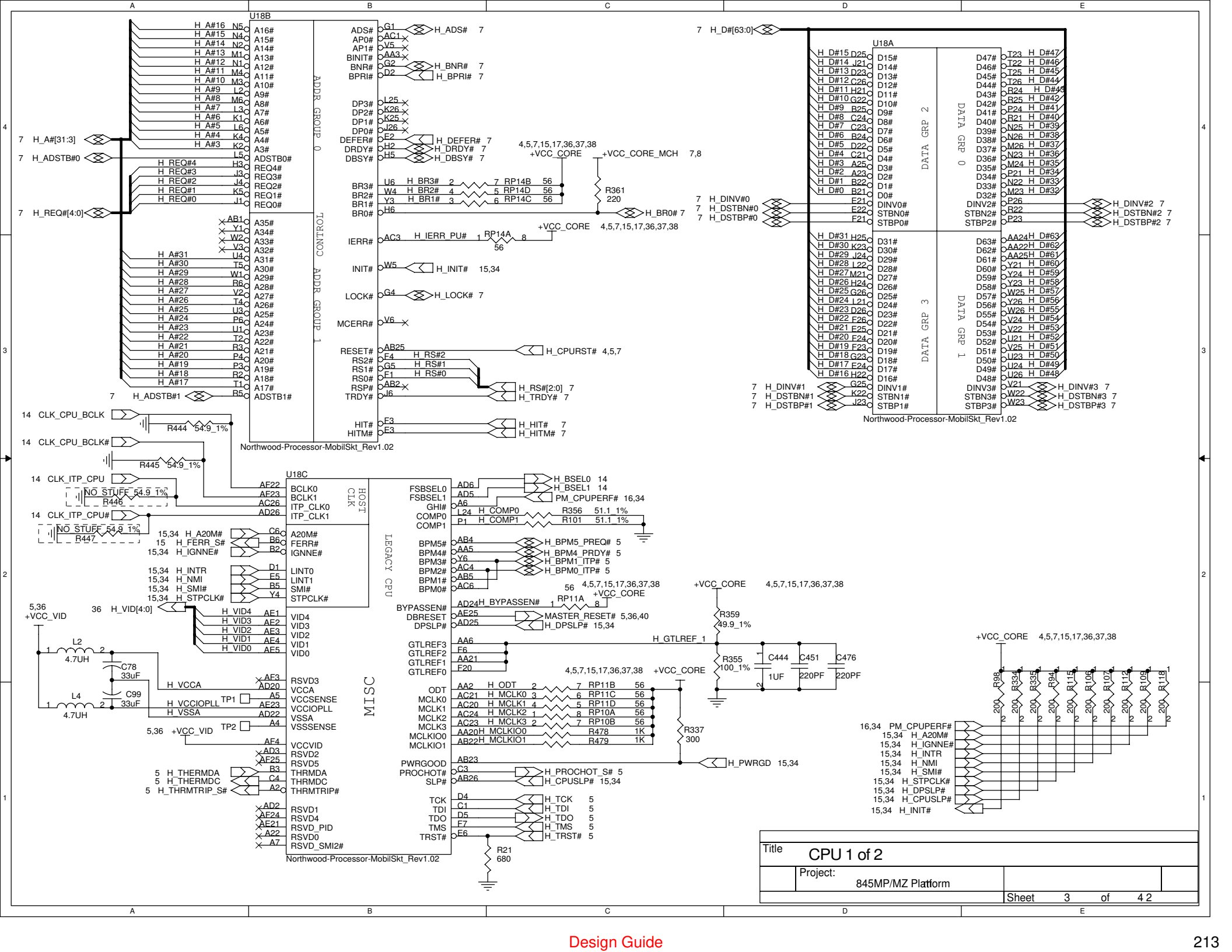
SOT-23



SOT23-5



Title	Notes and Annotations		
	Project: 845MP/MZ Platform		
		Sheet 2 of 4 2	


U18B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
Northwood-Processor-MobilSkt_Rev1.02
U18A
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
Northwood-Processor-MobilSkt_Rev1.02
U18C
HOST CLK
LEGACY CPU
MISC
Northwood-Processor-MobilSkt_Rev1.02
H_A#[31:3]
H_ADSTB#0
H_REQ#[4:0]
H_ADSTB#1
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR_PU#
H_INIT#
H_LOCK#
H_RS#[2:0]
H_TRDY#
H_CPURST#
H_HIT#
H_HITM#
H_D#[63:0]
H_DINV#0
H_DSTBN#0
H_DSTBP#0
H_DINV#1
H_DSTBN#1
H_DSTBP#1
H_DINV#2
H_DSTBN#2
H_DSTBP#2
H_DINV#3
H_DSTBN#3
H_DSTBP#3
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_ITP_CPU
CLK_ITP_CPU#
H_A20M#
H_FERR_S#
H_IGNNE#
H_INTR
H_NMI
H_SMI#
H_STPCLK#
H_VID[4:0]
+VCC_VID
H_VCCA
H_VCCIOPLL
H_VSSA
TP1
TP2
H_THERMDA
H_THERMDC
H_THRMTRIP_S#
H_BSEL0
H_BSEL1
PM_CPUPERF#
H_COMP0
H_COMP1
H_BPM5_PREQ#
H_BPM4_PRDY#
H_BPM1_ITP#
H_BPM0_ITP#
H_BYPASSEN#
MASTER_RESET#
H_DPSLP#
H_GTLREF_1
H_ODT
H_MCLK0
H_MCLK1
H_MCLK2
H_MCLK3
H_MCLKIO0
H_MCLKIO1
H_PWRGD
H_PROCHOT_S#
H_CPUSLP#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
+VCC_CORE
+VCC_CORE_MCH
Title
CPU 1 of 2
Project:
845MP/MZ Platform
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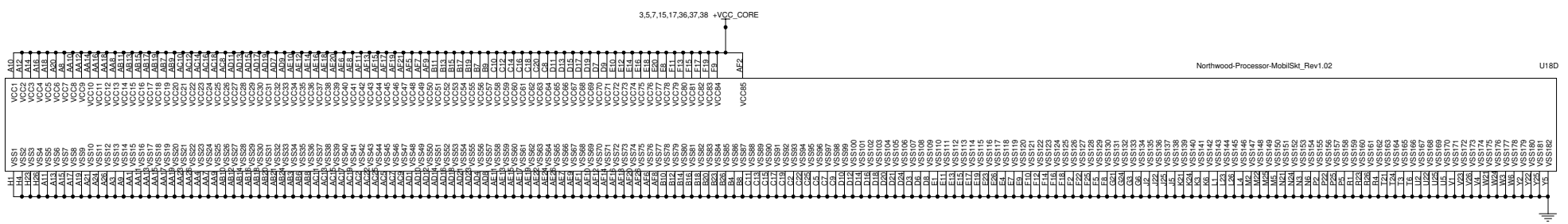
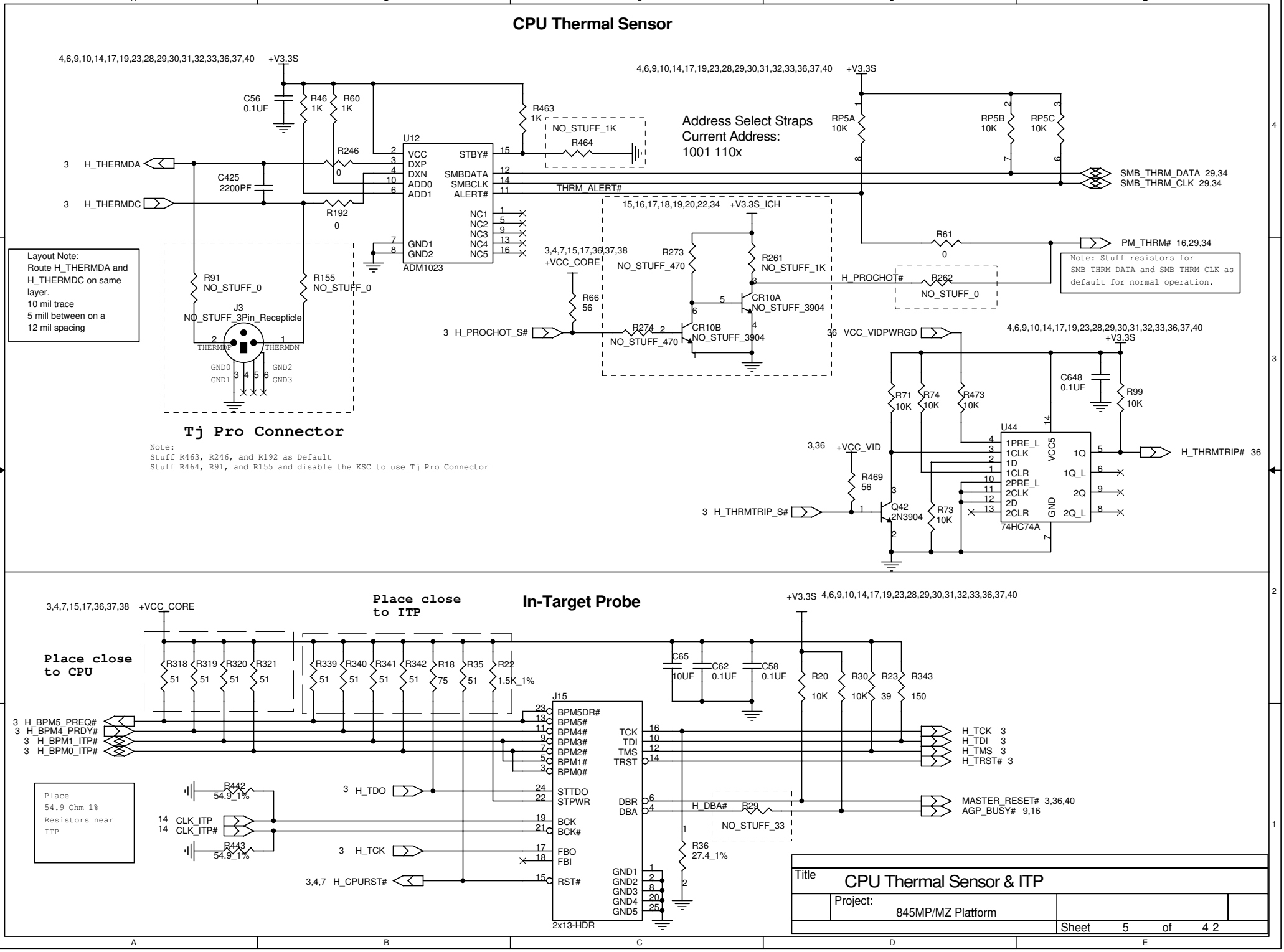


Title	CPU 1 of 2 / MCH POWER ON CONFIGURATION	
Project: 845MP/MZ Platform		
	Sheet 4 of 42	


CPU Thermal Sensor
4,6,9,10,14,17,19,23,28,29,30,31,32,33,36,37,40 +V3.3S
C56 0.1UF
R46 1K
R60 1K
R463 1K
NO_STUFF_1K
R464
U12
VCC
DXP
DXN
ADD0
ADD1
STBY#
SMBDATA
SMBCLK
ALERT#
NC1
NC2
NC3
NC4
NC5
GND1
GND2
ADM1023
R246 0
R192 0
C425 2200PF
3 H_THERMDA
3 H_THERMDC
THRM_ALERT#
Address Select Straps
Current Address:
1001 110x
RP5A 10K
RP5B 10K
RP5C 10K
SMB_THRM_DATA 29,34
SMB_THRM_CLK 29,34
15,16,17,18,19,20,22,34 +V3.3S_ICH
3,4,7,15,17,36,37,38 +VCC_CORE
R273 NO_STUFF_470
R261 NO_STUFF_1K
CR10A NO_STUFF_3904
CR10B NO_STUFF_3904
R274 NO_STUFF_470
R66 56
3 H_PROCHOT_S#
H_PROCHOT#
R262 NO_STUFF_0
R61 0
PM_THRM# 16,29,34
Note: Stuff resistors for SMB_THRM_DATA and SMB_THRM_CLK as default for normal operation.
Layout Note:
Route H_THERMDA and H_THERMDC on same layer.
10 mil trace
5 mil between on a 12 mil spacing
R91 NO_STUFF_0
R155 NO_STUFF_0
J3
NO_STUFF_3Pin_Recepticle
THERMDP
THERMDN
GND0
GND1
GND2
GND3
Tj Pro Connector
Note:
Stuff R463, R246, and R192 as Default
Stuff R464, R91, and R155 and disable the KSC to use Tj Pro Connector
36 VCC_VIDPWRGD
4,6,9,10,14,17,19,23,28,29,30,31,32,33,36,37,40 +V3.3S
C648 0.1UF
R99 10K
R71 10K
R74 10K
R473 10K
U44
1PRE_L
1CLK
1D
1CLR
2PRE_L
2CLK
2D
2CLR
VCC5
GND
1Q
1Q_L
2Q
2Q_L
74HC74A
3,36 +VCC_VID
R469 56
Q42 2N3904
R73 10K
3 H_THRMTRIP_S#
H_THRMTRIP# 36
In-Target Probe
Place close to ITP
Place close to CPU
3,4,7,15,17,36,37,38 +VCC_CORE
+V3.3S 4,6,9,10,14,17,19,23,28,29,30,31,32,33,36,37,40
R318 51
R319 51
R320 51
R321 51
R339 51
R340 51
R341 51
R342 51
R18 75
R35 51
R22 1.5K_1%
C65 10UF
C62 0.1UF
C58 0.1UF
R20 10K
R30 10K
R23 39
R343 150
J15
BPM5DR#
BPM5#
BPM4#
BPM3#
BPM2#
BPM1#
BPM0#
STTDO
STPWR
BCK
BCK#
FBO
FBI
RST#
TCK
TDI
TMS
TRST
DBR
DBA
GND1
GND2
GND3
GND4
GND5
2x13-HDR
3 H_BPM5_PREQ#
3 H_BPM4_PRDY#
3 H_BPM1_ITP#
3 H_BPM0_ITP#
3 H_TDO
3 H_TCK
3,4,7 H_CPURST#
H_TCK 3
H_TDI 3
H_TMS 3
H_TRST# 3
H_DBA# R29
NO_STUFF_33
R36 27.4_1%
MASTER_RESET# 3,36,40
AGP_BUSY# 9,16
R442 54.9_1%
R443 54.9_1%
14 CLK_ITP
14 CLK_ITP#
Place 54.9 Ohm 1% Resistors near ITP
Title
CPU Thermal Sensor & ITP
Project:
845MP/MZ Platform
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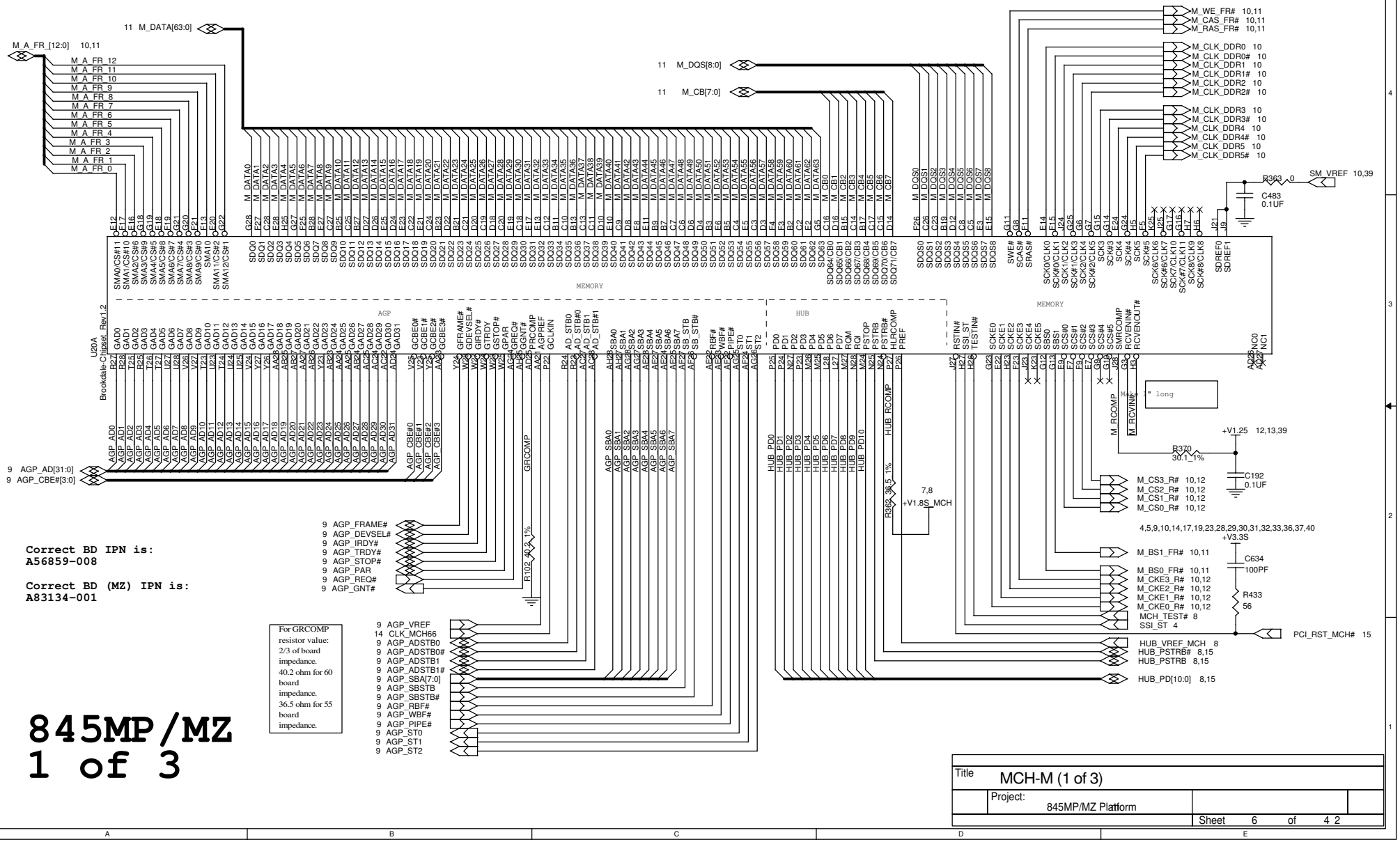
Correct BD IPN is:
A56859-008
Correct BD (MZ) IPN is:
A83134-001
845MP/MZ
1 of 3
For GRCOMP resistor value: 2/3 of board impedance. 40.2 ohm for 60 board impedance. 36.5 ohm for 55 board impedance.
Title
MCH-M (1 of 3)
Project:
845MP/MZ Platform
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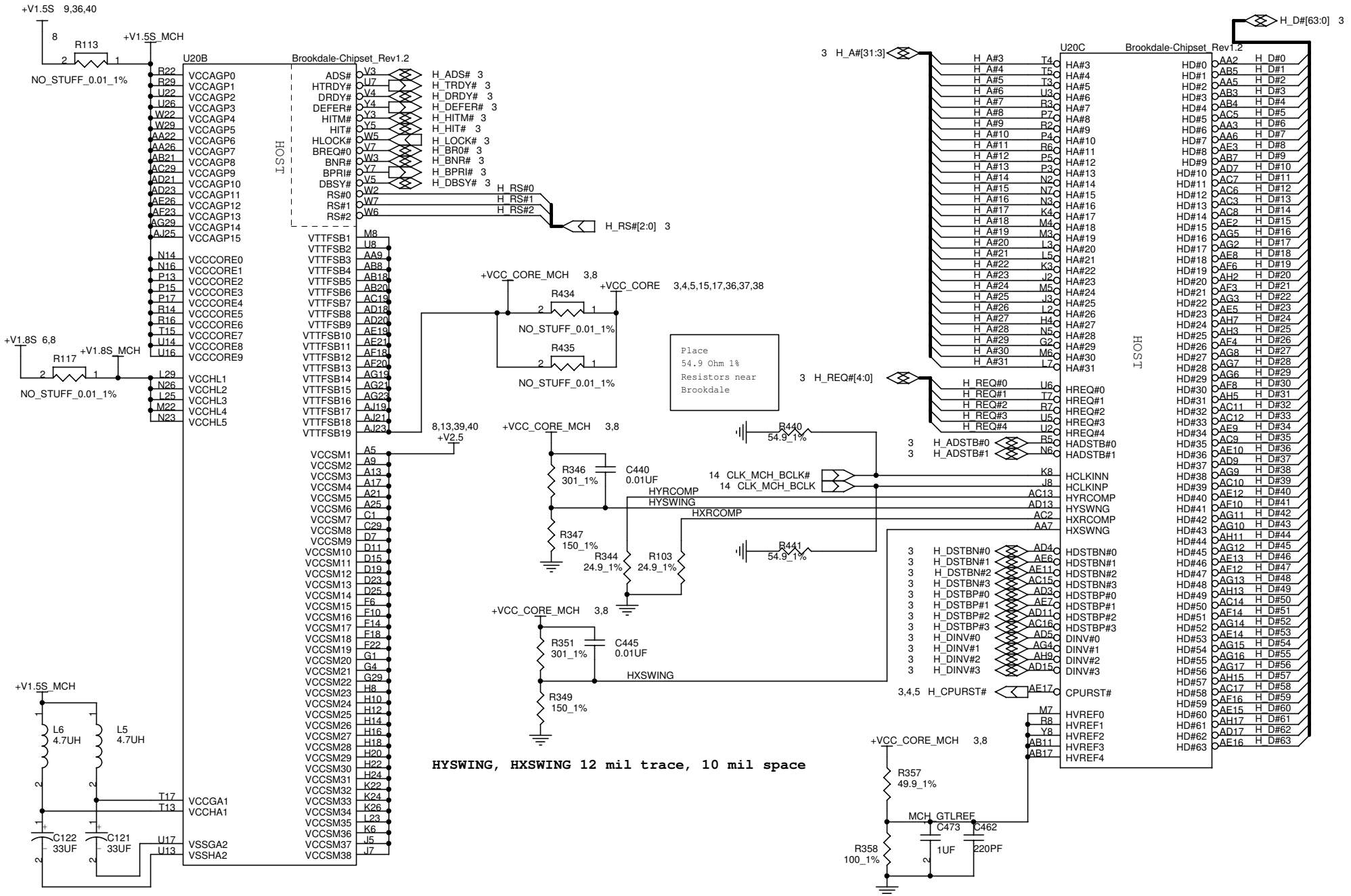
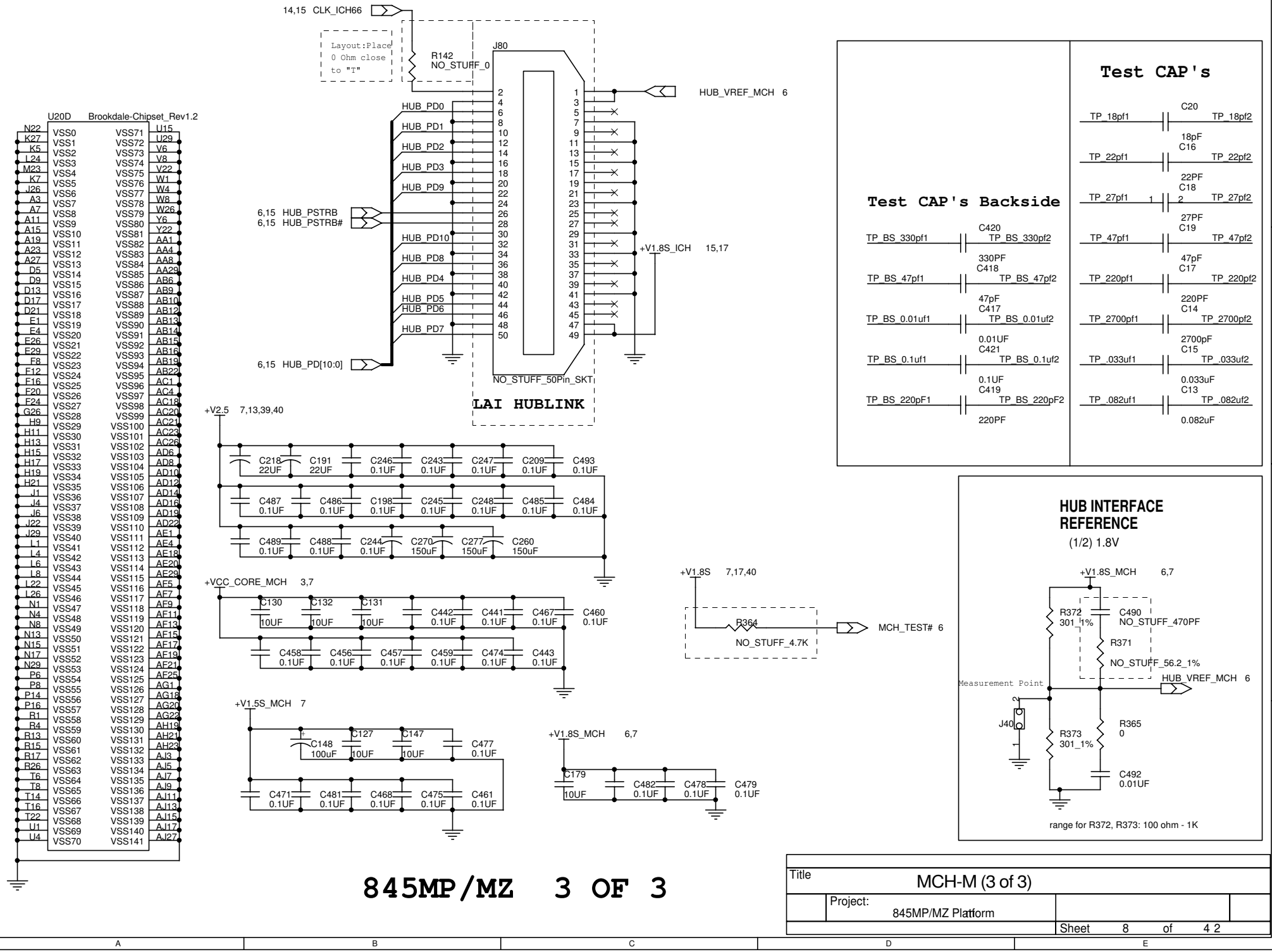
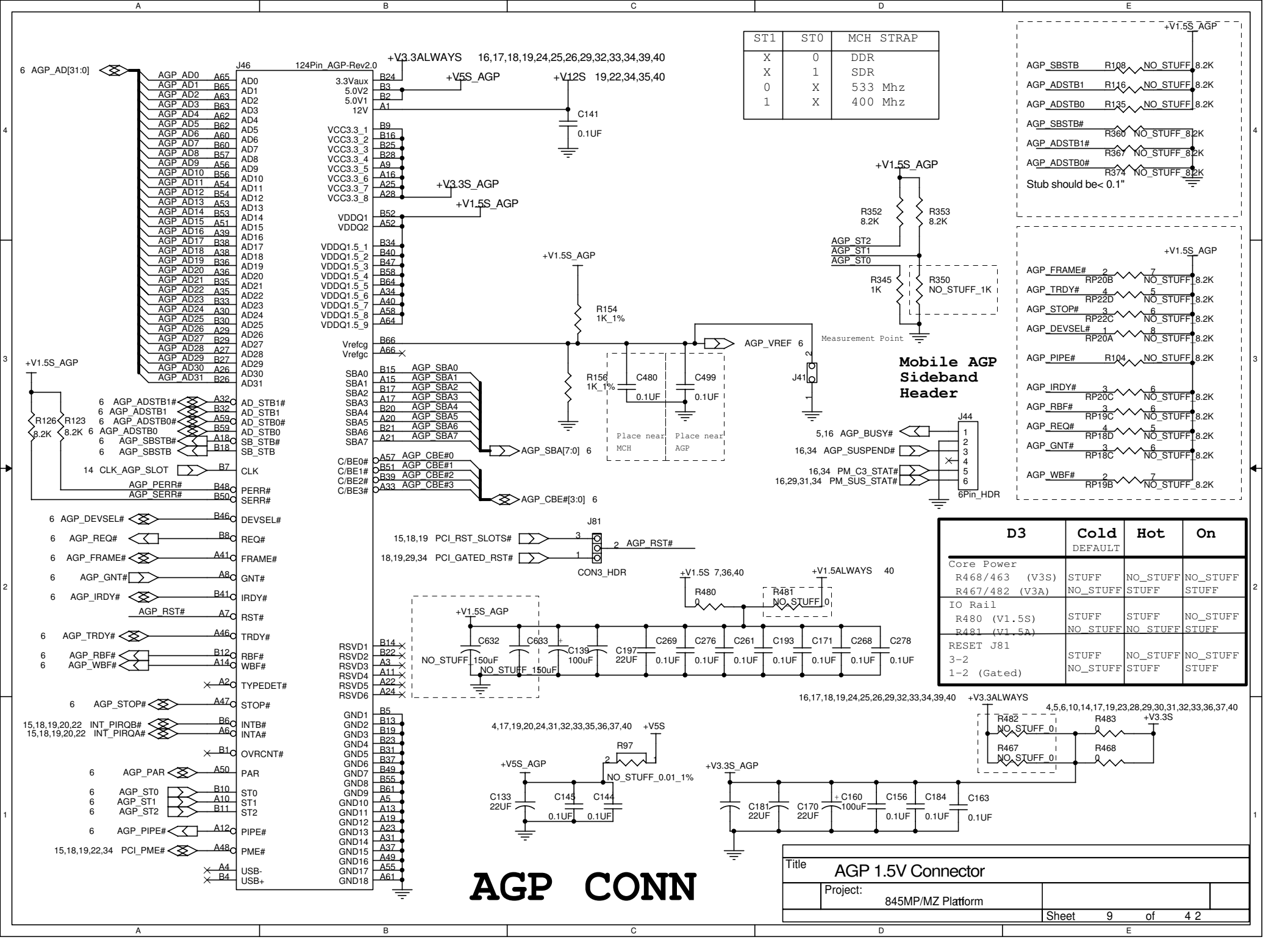
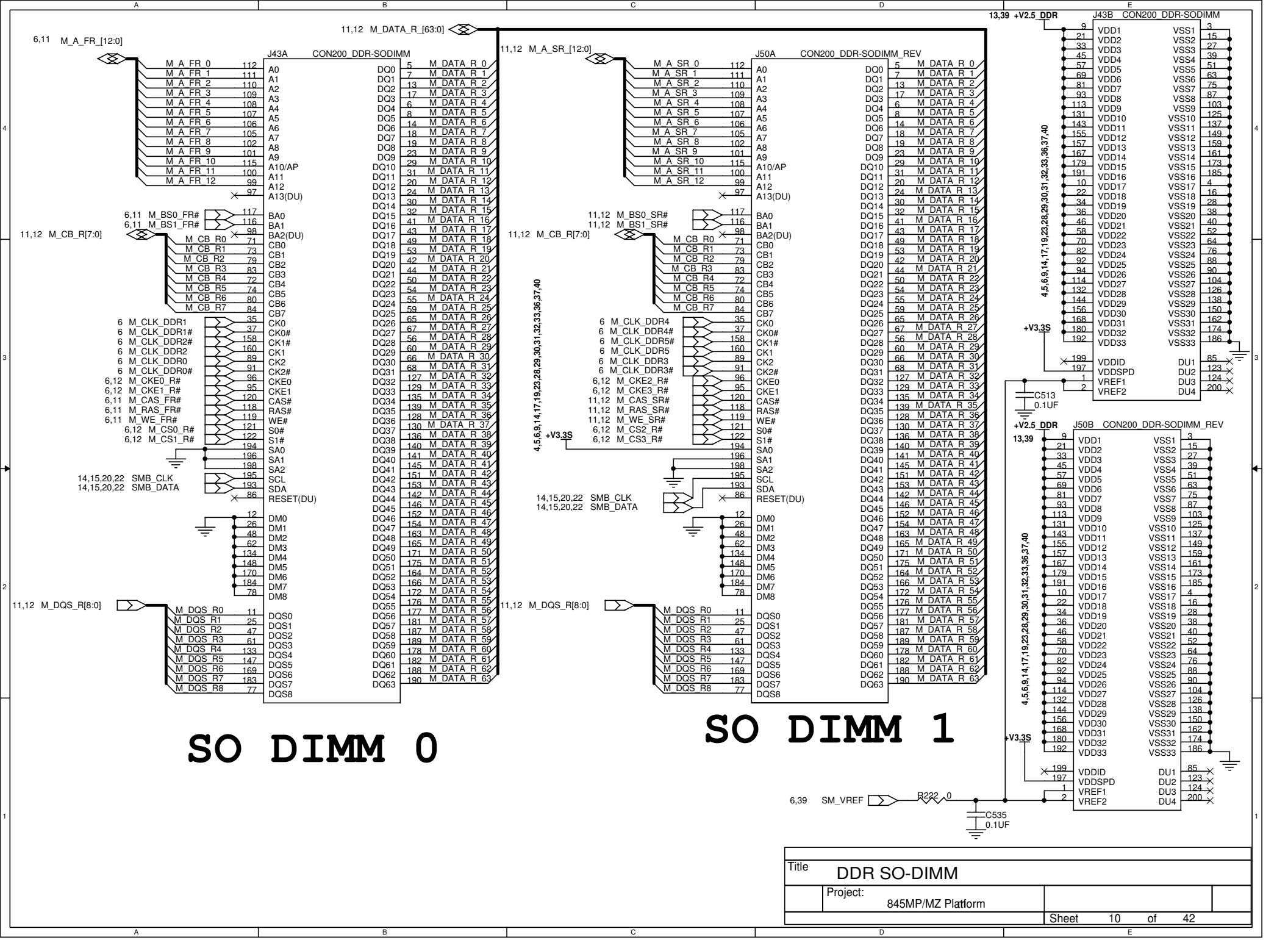
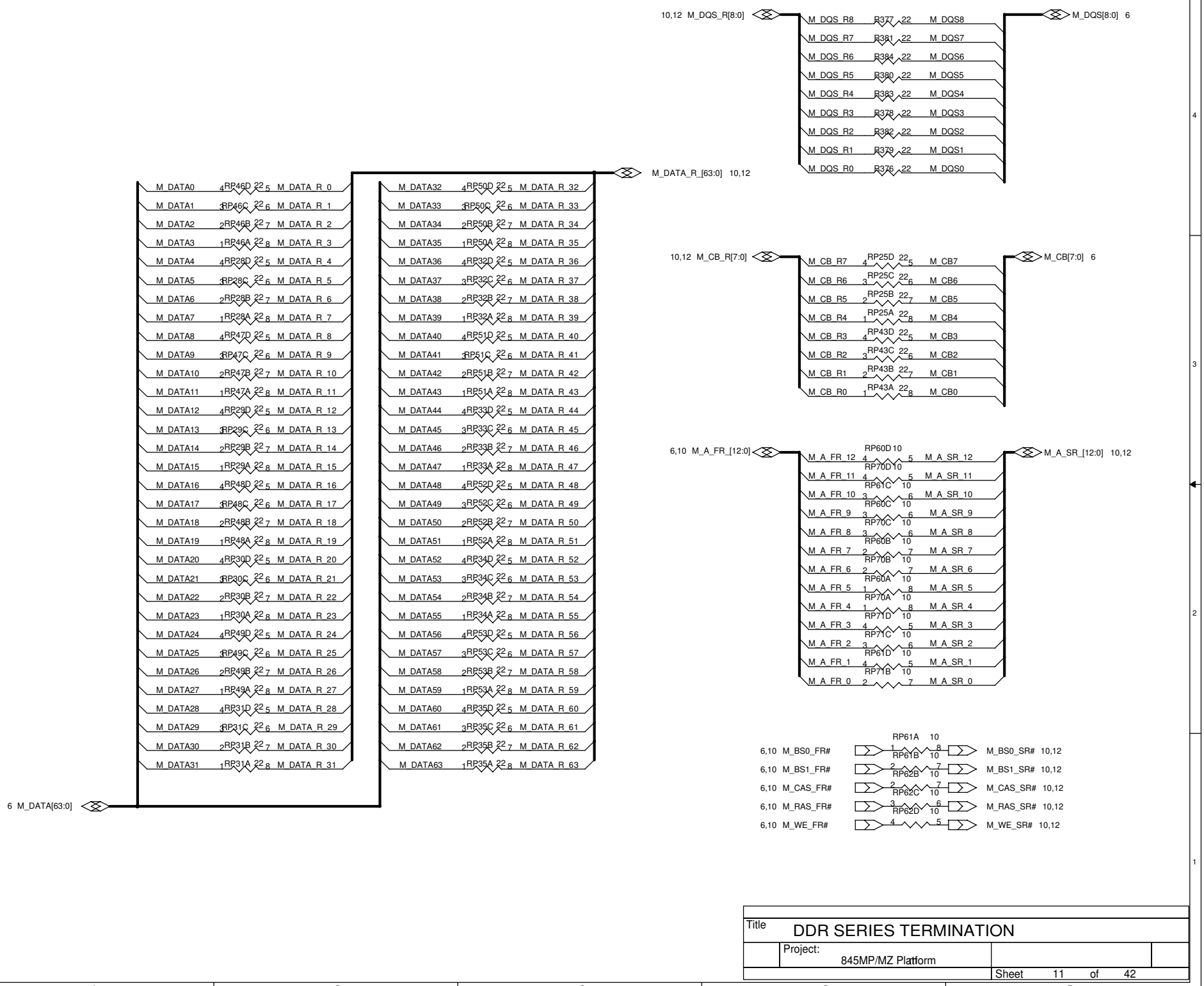
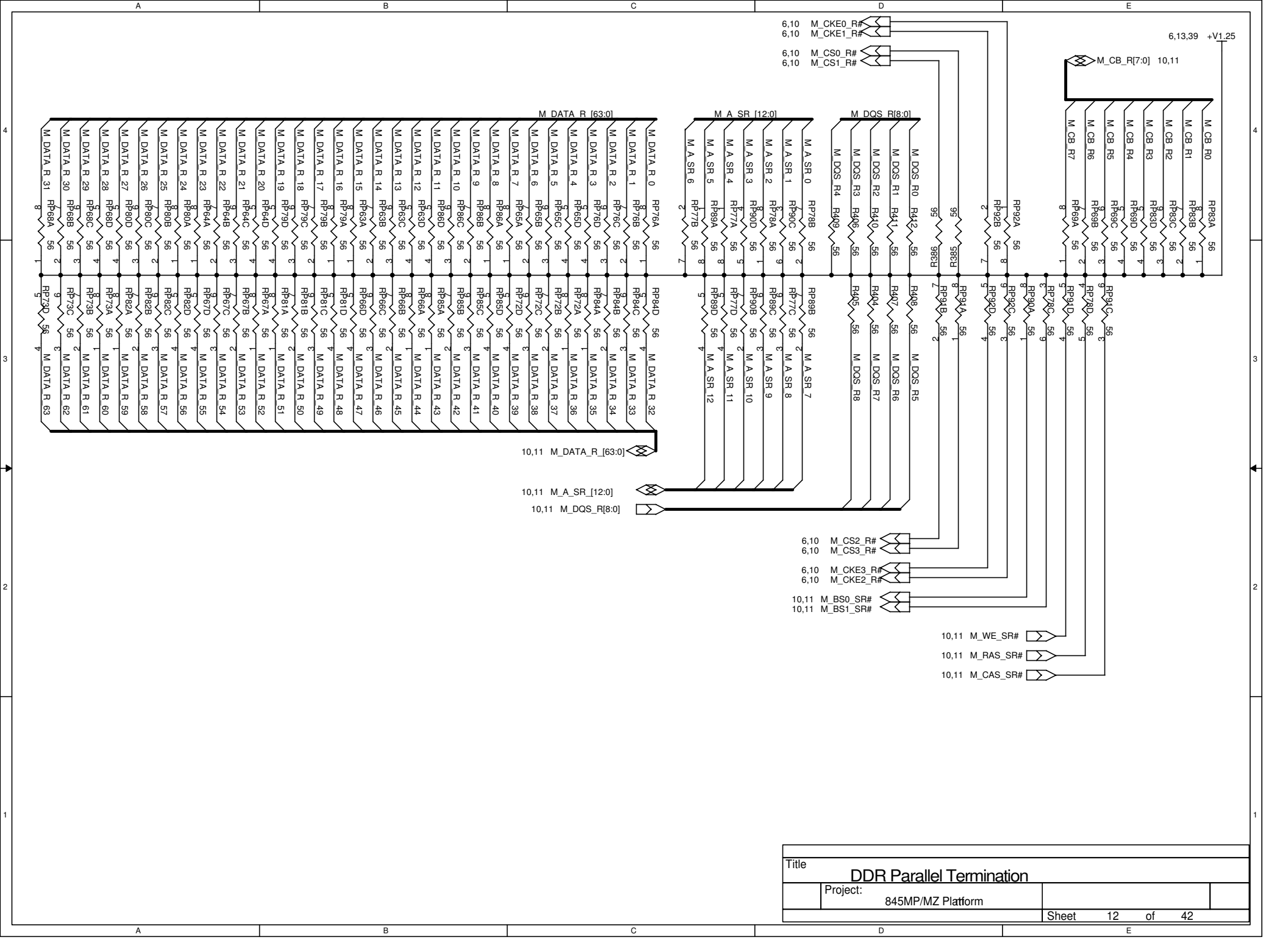

+V1.5S 9,36,40
R113
+V1.5S_MCH
NO_STUFF_0.01_1%
U20B
Brookdale-Chipset_Rev1.2
HOST
VCCAGP0
VCCAGP1
VCCAGP2
VCCAGP3
VCCAGP4
VCCAGP5
VCCAGP6
VCCAGP7
VCCAGP8
VCCAGP9
VCCAGP10
VCCAGP11
VCCAGP12
VCCAGP13
VCCAGP14
VCCAGP15
VCCCORE0
VCCCORE1
VCCCORE2
VCCCORE3
VCCCORE4
VCCCORE5
VCCCORE6
VCCCORE7
VCCCORE8
VCCCORE9
+V1.8S 6,8
R117
+V1.8S_MCH
NO_STUFF_0.01_1%
VCCHL1
VCCHL2
VCCHL3
VCCHL4
VCCHL5
+V1.5S_MCH
L6 4.7UH
L5 4.7UH
C122 33UF
C121 33UF
VCCGA1
VCCHA1
VSSGA2
VSSHA2
ADS#
HTRDY#
DRDY#
DEFER#
HITM#
HIT#
HLOCK#
BREQ#0
BNR#
BPRI#
DBSY#
RS#0
RS#1
RS#2
H_ADS# 3
H_TRDY# 3
H_DRDY# 3
H_DEFER# 3
H_HITM# 3
H_HIT# 3
H_LOCK# 3
H_BR0# 3
H_BNR# 3
H_BPRI# 3
H_DBSY# 3
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3
VTTFSB1
VTTFSB2
VTTFSB3
VTTFSB4
VTTFSB5
VTTFSB6
VTTFSB7
VTTFSB8
VTTFSB9
VTTFSB10
VTTFSB11
VTTFSB12
VTTFSB13
VTTFSB14
VTTFSB15
VTTFSB16
VTTFSB17
VTTFSB18
VTTFSB19
VCCSM1
VCCSM2
VCCSM3
VCCSM4
VCCSM5
VCCSM6
VCCSM7
VCCSM8
VCCSM9
VCCSM10
VCCSM11
VCCSM12
VCCSM13
VCCSM14
VCCSM15
VCCSM16
VCCSM17
VCCSM18
VCCSM19
VCCSM20
VCCSM21
VCCSM22
VCCSM23
VCCSM24
VCCSM25
VCCSM26
VCCSM27
VCCSM28
VCCSM29
VCCSM30
VCCSM31
VCCSM32
VCCSM33
VCCSM34
VCCSM35
VCCSM36
VCCSM37
VCCSM38
+VCC_CORE_MCH 3,8
+VCC_CORE 3,4,5,15,17,36,37,38
R434
R435
NO_STUFF_0.01_1%
NO_STUFF_0.01_1%
Place
54.9 Ohm 1%
Resistors near
Brookdale
8,13,39,40
+V2.5
+VCC_CORE_MCH 3,8
R346 301_1%
C440 0.01UF
R347 150_1%
R344 24.9_1%
R103 24.9_1%
HYRCOMP
HYSWING
HXRCOMP
+VCC_CORE_MCH 3,8
R351 301_1%
C445 0.01UF
R349 150_1%
HXSWING
HYSWING, HXSWING 12 mil trace, 10 mil space
R440 54.9_1%
R441 54.9_1%
14 CLK_MCH_BCLK#
14 CLK_MCH_BCLK
HCLKINN
HCLKINP
HYRCOMP
HYSWNG
HXRCOMP
HXSWNG
3 H_A#[31:3]
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
3 H_REQ#[4:0]
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
HREQ#0
HREQ#1
HREQ#2
HREQ#3
HREQ#4
3 H_ADSTB#0
3 H_ADSTB#1
HADSTB#0
HADSTB#1
3 H_DSTBN#0
3 H_DSTBN#1
3 H_DSTBN#2
3 H_DSTBN#3
3 H_DSTBP#0
3 H_DSTBP#1
3 H_DSTBP#2
3 H_DSTBP#3
3 H_DINV#0
3 H_DINV#1
3 H_DINV#2
3 H_DINV#3
HDSTBN#0
HDSTBN#1
HDSTBN#2
HDSTBN#3
HDSTBP#0
HDSTBP#1
HDSTBP#2
HDSTBP#3
DINV#0
DINV#1
DINV#2
DINV#3
3,4,5 H_CPURST#
CPURST#
HVREF0
HVREF1
HVREF2
HVREF3
HVREF4
+VCC_CORE_MCH 3,8
R357 49.9_1%
MCH_GTLREF
R358 100_1%
C473 1UF
C462 220PF
U20C
Brookdale-Chipset_Rev1.2
HOST
H_D#[63:0] 3
HD#0
HD#1
HD#2
HD#3
HD#4
HD#5
HD#6
HD#7
HD#8
HD#9
HD#10
HD#11
HD#12
HD#13
HD#14
HD#15
HD#16
HD#17
HD#18
HD#19
HD#20
HD#21
HD#22
HD#23
HD#24
HD#25
HD#26
HD#27
HD#28
HD#29
HD#30
HD#31
HD#32
HD#33
HD#34
HD#35
HD#36
HD#37
HD#38
HD#39
HD#40
HD#41
HD#42
HD#43
HD#44
HD#45
HD#46
HD#47
HD#48
HD#49
HD#50
HD#51
HD#52
HD#53
HD#54
HD#55
HD#56
HD#57
HD#58
HD#59
HD#60
HD#61
HD#62
HD#63
845MP/MZ 2 OF 3
Title
MCH-M (2 of 3)
Project:
845MP/MZ Platform
Sheet 7 of 42

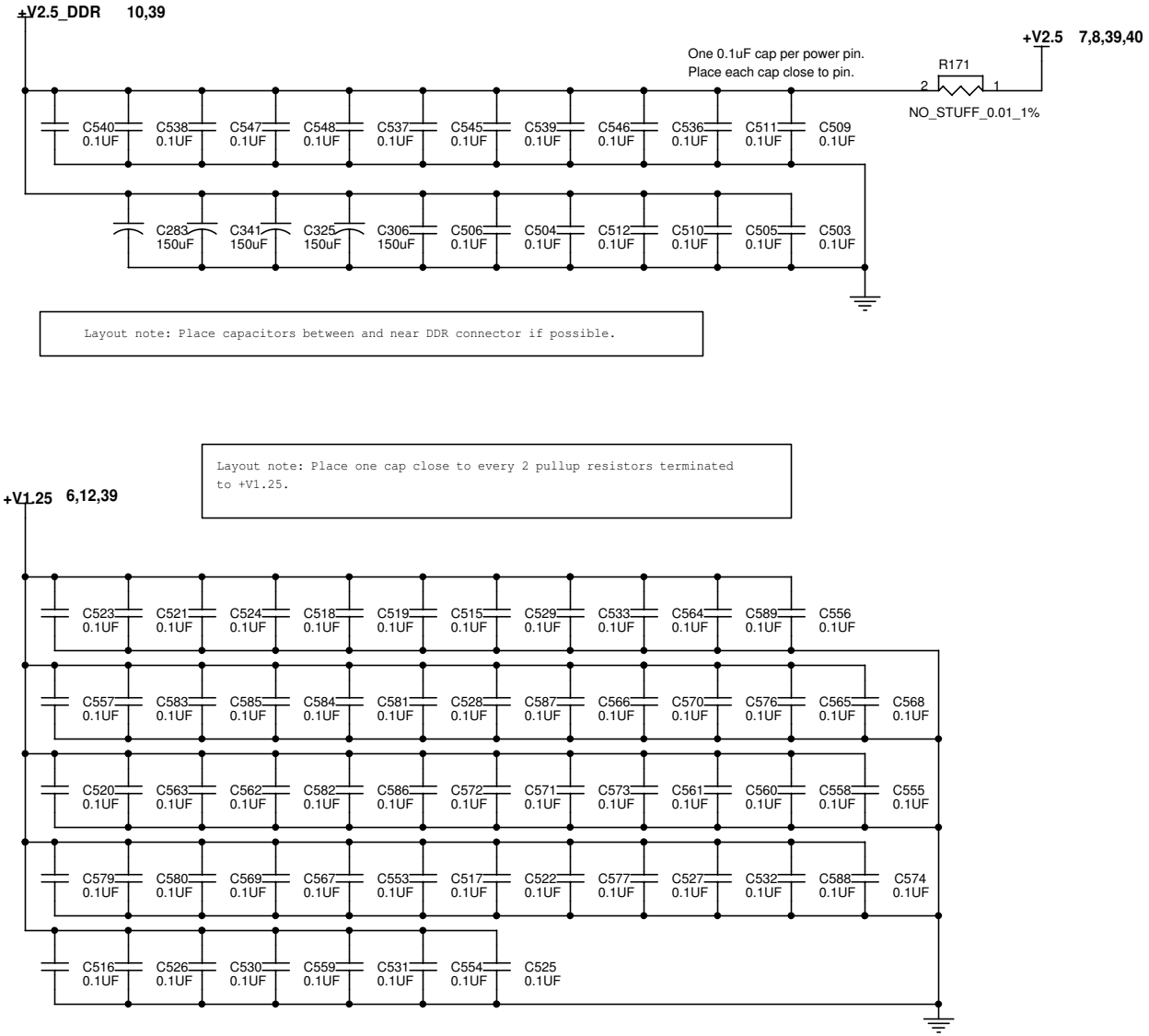

14,15 CLK_ICH66
Layout:Place 0 Ohm close to "I"
R142 NO_STUFF_0
J80
HUB_VREF_MCH 6
HUB_PD0
HUB_PD1
HUB_PD2
HUB_PD3
HUB_PD9
6,15 HUB_PSTRB
6,15 HUB_PSTRB#
HUB_PD10
HUB_PD8
HUB_PD4
HUB_PD5
HUB_PD6
HUB_PD7
+V1.8S_ICH 15,17
6,15 HUB_PD[10:0]
NO_STUFF_50Pin_SKT
LAI HUBLINK
U20D Brookdale-Chipset_Rev1.2
+V2.5 7,13,39,40
C218 22UF
C191 22UF
C246 0.1UF
C243 0.1UF
C247 0.1UF
C209 0.1UF
C493 0.1UF
C487 0.1UF
C486 0.1UF
C198 0.1UF
C245 0.1UF
C248 0.1UF
C485 0.1UF
C484 0.1UF
C489 0.1UF
C488 0.1UF
C244 0.1UF
C270 150uF
C277 150uF
C260 150uF
+VCC_CORE_MCH 3,7
C130 10UF
C132 10UF
C131 10UF
C442 0.1UF
C441 0.1UF
C467 0.1UF
C460 0.1UF
C458 0.1UF
C456 0.1UF
C457 0.1UF
C459 0.1UF
C474 0.1UF
C443 0.1UF
+V1.8S 7,17,40
R364 NO_STUFF_4.7K
MCH_TEST# 6
+V1.5S_MCH 7
C148 100uF
C127 10UF
C147 10UF
C477 0.1UF
C471 0.1UF
C481 0.1UF
C468 0.1UF
C475 0.1UF
C461 0.1UF
+V1.8S_MCH 6,7
C179 10UF
C482 0.1UF
C478 0.1UF
C479 0.1UF
Test CAP's Backside
TP_BS_330pf1
C420
TP_BS_330pf2
330PF
TP_BS_47pf1
C418
TP_BS_47pf2
47pF
TP_BS_0.01uf1
C417
TP_BS_0.01uf2
0.01UF
TP_BS_0.1uf1
C421
TP_BS_0.1uf2
0.1UF
TP_BS_220pF1
C419
TP_BS_220pF2
220PF
Test CAP's
TP_18pf1
C20
TP_18pf2
18pF
TP_22pf1
C16
TP_22pf2
22PF
TP_27pf1
C18
TP_27pf2
27PF
TP_47pf1
C19
TP_47pf2
47pF
TP_220pf1
C17
TP_220pf2
220PF
TP_2700pf1
C14
TP_2700pf2
2700pF
TP_.033uf1
C15
TP_.033uf2
0.033uF
TP_.082uf1
C13
TP_.082uf2
0.082uF
HUB INTERFACE REFERENCE
(1/2) 1.8V
+V1.8S_MCH 6,7
R372 301_1%
C490 NO_STUFF_470PF
R371
NO_STUFF_56.2_1%
Measurement Point
HUB_VREF_MCH 6
J40
R373 301_1%
R365 0
C492 0.01UF
range for R372, R373: 100 ohm - 1K
845MP/MZ 3 OF 3
Title
MCH-M (3 of 3)
Project:
845MP/MZ Platform
Sheet 8 of 42


AGP CONN
J46
124Pin_AGP-Rev2.0
Mobile AGP Sideband Header
J44
6Pin_HDR
J41
J81
CON3_HDR
Measurement Point
Place near MCH
Place near AGP
Stub should be< 0.1"
ST1 ST0 MCH STRAP
X 0 DDR
X 1 SDR
0 X 533 Mhz
1 X 400 Mhz
D3 Cold DEFAULT Hot On
Core Power
R468/463 (V3S) STUFF NO_STUFF NO_STUFF
R467/482 (V3A) NO_STUFF STUFF STUFF
IO Rail
R480 (V1.5S) STUFF STUFF NO_STUFF
R481 (V1.5A) NO_STUFF NO_STUFF STUFF
RESET J81
3-2 STUFF NO_STUFF NO_STUFF
1-2 (Gated) NO_STUFF STUFF STUFF
Title AGP 1.5V Connector
Project: 845MP/MZ Platform
Sheet 9 of 42

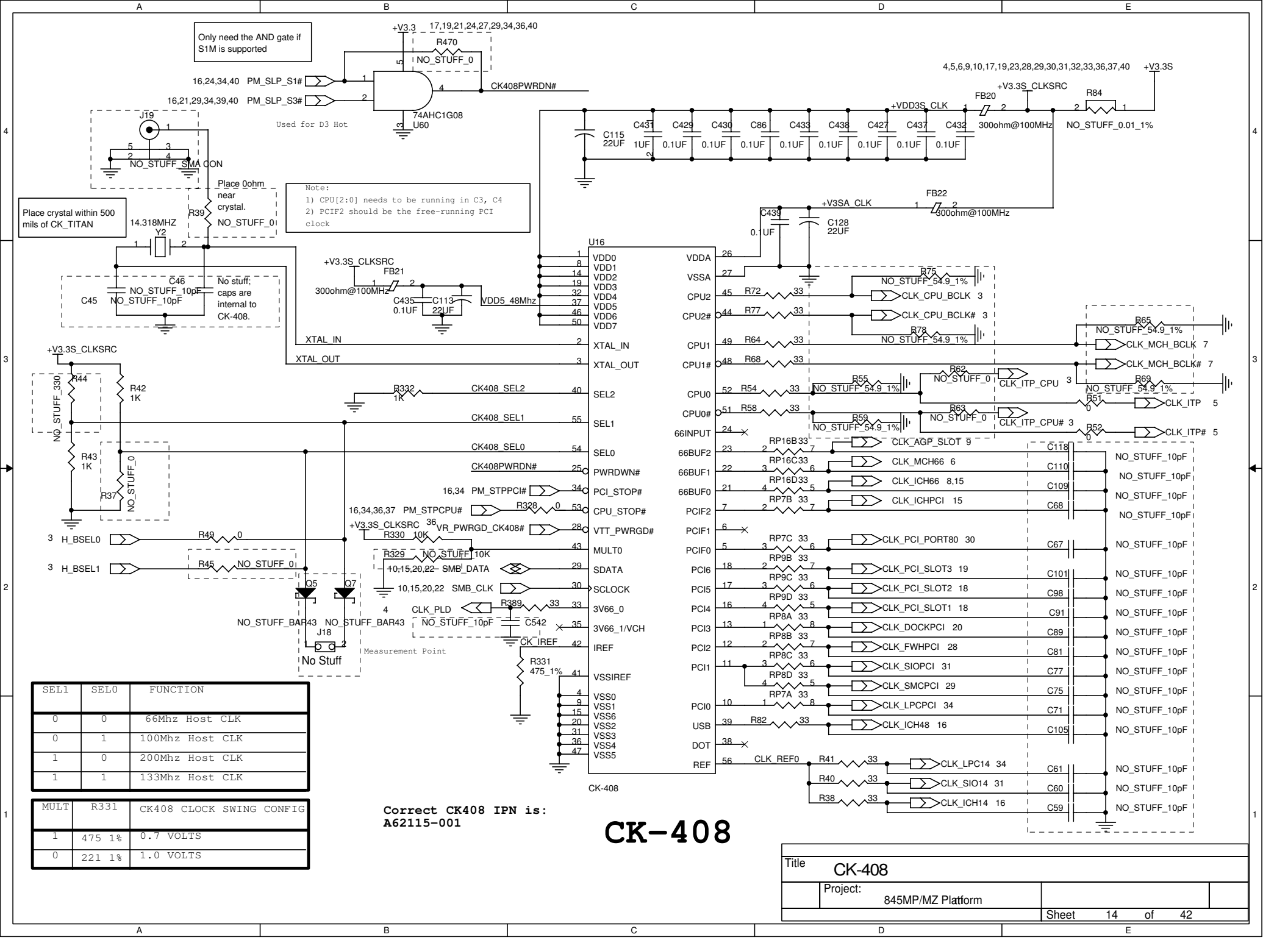

SO DIMM 0
SO DIMM 1
J43A CON200_DDR-SODIMM
J50A CON200_DDR-SODIMM_REV
J43B CON200_DDR-SODIMM
J50B CON200_DDR-SODIMM_REV
M_A_FR_[12:0]
M_A_SR_[12:0]
M_DATA_R_[63:0]
M_CB_R[7:0]
M_DQS_R[8:0]
M_BS0_FR#
M_BS1_FR#
M_BS0_SR#
M_BS1_SR#
M_CLK_DDR1
M_CLK_DDR1#
M_CLK_DDR2#
M_CLK_DDR2
M_CLK_DDR0
M_CLK_DDR0#
M_CKE0_R#
M_CKE1_R#
M_CAS_FR#
M_RAS_FR#
M_WE_FR#
M_CS0_R#
M_CS1_R#
M_CLK_DDR4
M_CLK_DDR4#
M_CLK_DDR5#
M_CLK_DDR5
M_CLK_DDR3
M_CLK_DDR3#
M_CKE2_R#
M_CKE3_R#
M_CAS_SR#
M_RAS_SR#
M_WE_SR#
M_CS2_R#
M_CS3_R#
SMB_CLK
SMB_DATA
+V2.5_DDR
+V3.3S
SM_VREF
R222 0
C513 0.1UF
C535 0.1UF
Title DDR SO-DIMM
Project: 845MP/MZ Platform
Sheet 10 of 42


10,12 M_DQS_R[8:0]
M_DQS_R8 R377 22 M_DQS8
M_DQS_R7 R381 22 M_DQS7
M_DQS_R6 R384 22 M_DQS6
M_DQS_R5 R380 22 M_DQS5
M_DQS_R4 R383 22 M_DQS4
M_DQS_R3 R378 22 M_DQS3
M_DQS_R2 R382 22 M_DQS2
M_DQS_R1 R379 22 M_DQS1
M_DQS_R0 R376 22 M_DQS0
M_DQS[8:0] 6
M_DATA_R_[63:0] 10,12
M_DATA0 RP46D 22 M_DATA_R_0
M_DATA1 RP46C 22 M_DATA_R_1
M_DATA2 RP46B 22 M_DATA_R_2
M_DATA3 RP46A 22 M_DATA_R_3
M_DATA4 RP28D 22 M_DATA_R_4
M_DATA5 RP28C 22 M_DATA_R_5
M_DATA6 RP28B 22 M_DATA_R_6
M_DATA7 RP28A 22 M_DATA_R_7
M_DATA8 RP47D 22 M_DATA_R_8
M_DATA9 RP47C 22 M_DATA_R_9
M_DATA10 RP47B 22 M_DATA_R_10
M_DATA11 RP47A 22 M_DATA_R_11
M_DATA12 RP29D 22 M_DATA_R_12
M_DATA13 RP29C 22 M_DATA_R_13
M_DATA14 RP29B 22 M_DATA_R_14
M_DATA15 RP29A 22 M_DATA_R_15
M_DATA16 RP48D 22 M_DATA_R_16
M_DATA17 RP48C 22 M_DATA_R_17
M_DATA18 RP48B 22 M_DATA_R_18
M_DATA19 RP48A 22 M_DATA_R_19
M_DATA20 RP30D 22 M_DATA_R_20
M_DATA21 RP30C 22 M_DATA_R_21
M_DATA22 RP30B 22 M_DATA_R_22
M_DATA23 RP30A 22 M_DATA_R_23
M_DATA24 RP49D 22 M_DATA_R_24
M_DATA25 RP49C 22 M_DATA_R_25
M_DATA26 RP49B 22 M_DATA_R_26
M_DATA27 RP49A 22 M_DATA_R_27
M_DATA28 RP31D 22 M_DATA_R_28
M_DATA29 RP31C 22 M_DATA_R_29
M_DATA30 RP31B 22 M_DATA_R_30
M_DATA31 RP31A 22 M_DATA_R_31
M_DATA32 RP50D 22 M_DATA_R_32
M_DATA33 RP50C 22 M_DATA_R_33
M_DATA34 RP50B 22 M_DATA_R_34
M_DATA35 RP50A 22 M_DATA_R_35
M_DATA36 RP32D 22 M_DATA_R_36
M_DATA37 RP32C 22 M_DATA_R_37
M_DATA38 RP32B 22 M_DATA_R_38
M_DATA39 RP32A 22 M_DATA_R_39
M_DATA40 RP51D 22 M_DATA_R_40
M_DATA41 RP51C 22 M_DATA_R_41
M_DATA42 RP51B 22 M_DATA_R_42
M_DATA43 RP51A 22 M_DATA_R_43
M_DATA44 RP33D 22 M_DATA_R_44
M_DATA45 RP33C 22 M_DATA_R_45
M_DATA46 RP33B 22 M_DATA_R_46
M_DATA47 RP33A 22 M_DATA_R_47
M_DATA48 RP52D 22 M_DATA_R_48
M_DATA49 RP52C 22 M_DATA_R_49
M_DATA50 RP52B 22 M_DATA_R_50
M_DATA51 RP52A 22 M_DATA_R_51
M_DATA52 RP34D 22 M_DATA_R_52
M_DATA53 RP34C 22 M_DATA_R_53
M_DATA54 RP34B 22 M_DATA_R_54
M_DATA55 RP34A 22 M_DATA_R_55
M_DATA56 RP53D 22 M_DATA_R_56
M_DATA57 RP53C 22 M_DATA_R_57
M_DATA58 RP53B 22 M_DATA_R_58
M_DATA59 RP53A 22 M_DATA_R_59
M_DATA60 RP35D 22 M_DATA_R_60
M_DATA61 RP35C 22 M_DATA_R_61
M_DATA62 RP35B 22 M_DATA_R_62
M_DATA63 RP35A 22 M_DATA_R_63
6 M_DATA[63:0]
10,12 M_CB_R[7:0]
M_CB_R7 RP25D 22 M_CB7
M_CB_R6 RP25C 22 M_CB6
M_CB_R5 RP25B 22 M_CB5
M_CB_R4 RP25A 22 M_CB4
M_CB_R3 RP43D 22 M_CB3
M_CB_R2 RP43C 22 M_CB2
M_CB_R1 RP43B 22 M_CB1
M_CB_R0 RP43A 22 M_CB0
M_CB[7:0] 6
6,10 M_A_FR_[12:0]
M_A_FR_12 RP60D 10 M_A_SR_12
M_A_FR_11 RP70D 10 M_A_SR_11
M_A_FR_10 RP61C 10 M_A_SR_10
M_A_FR_9 RP60C 10 M_A_SR_9
M_A_FR_8 RP70C 10 M_A_SR_8
M_A_FR_7 RP60B 10 M_A_SR_7
M_A_FR_6 RP70B 10 M_A_SR_6
M_A_FR_5 RP60A 10 M_A_SR_5
M_A_FR_4 RP70A 10 M_A_SR_4
M_A_FR_3 RP71D 10 M_A_SR_3
M_A_FR_2 RP71C 10 M_A_SR_2
M_A_FR_1 RP61D 10 M_A_SR_1
M_A_FR_0 RP71B 10 M_A_SR_0
M_A_SR_[12:0] 10,12
RP61A 10
6,10 M_BS0_FR#
RP61B 10
M_BS0_SR# 10,12
6,10 M_BS1_FR#
RP62B 10
M_BS1_SR# 10,12
6,10 M_CAS_FR#
RP62C 10
M_CAS_SR# 10,12
6,10 M_RAS_FR#
RP62D 10
M_RAS_SR# 10,12
6,10 M_WE_FR#
M_WE_SR# 10,12
Title
DDR SERIES TERMINATION
Project:
845MP/MZ Platform
Sheet 11 of 42


M_DATA_R [63:0]
M_A_SR [12:0]
M_DQS_R[8:0]
M_CB_R[7:0] 10,11
6,13,39 +V1.25
6,10 M_CKE0_R#
6,10 M_CKE1_R#
6,10 M_CS0_R#
6,10 M_CS1_R#
6,10 M_CS2_R#
6,10 M_CS3_R#
6,10 M_CKE3_R#
6,10 M_CKE2_R#
10,11 M_BS0_SR#
10,11 M_BS1_SR#
10,11 M_WE_SR#
10,11 M_RAS_SR#
10,11 M_CAS_SR#
10,11 M_DATA_R_[63:0]
10,11 M_A_SR_[12:0]
10,11 M_DQS_R[8:0]
Title
DDR Parallel Termination
Project:
845MP/MZ Platform
Sheet 12 of 42



Title	DDR Decoupling
Project:	845MP/MZ Platform
Sheet	13 of 42



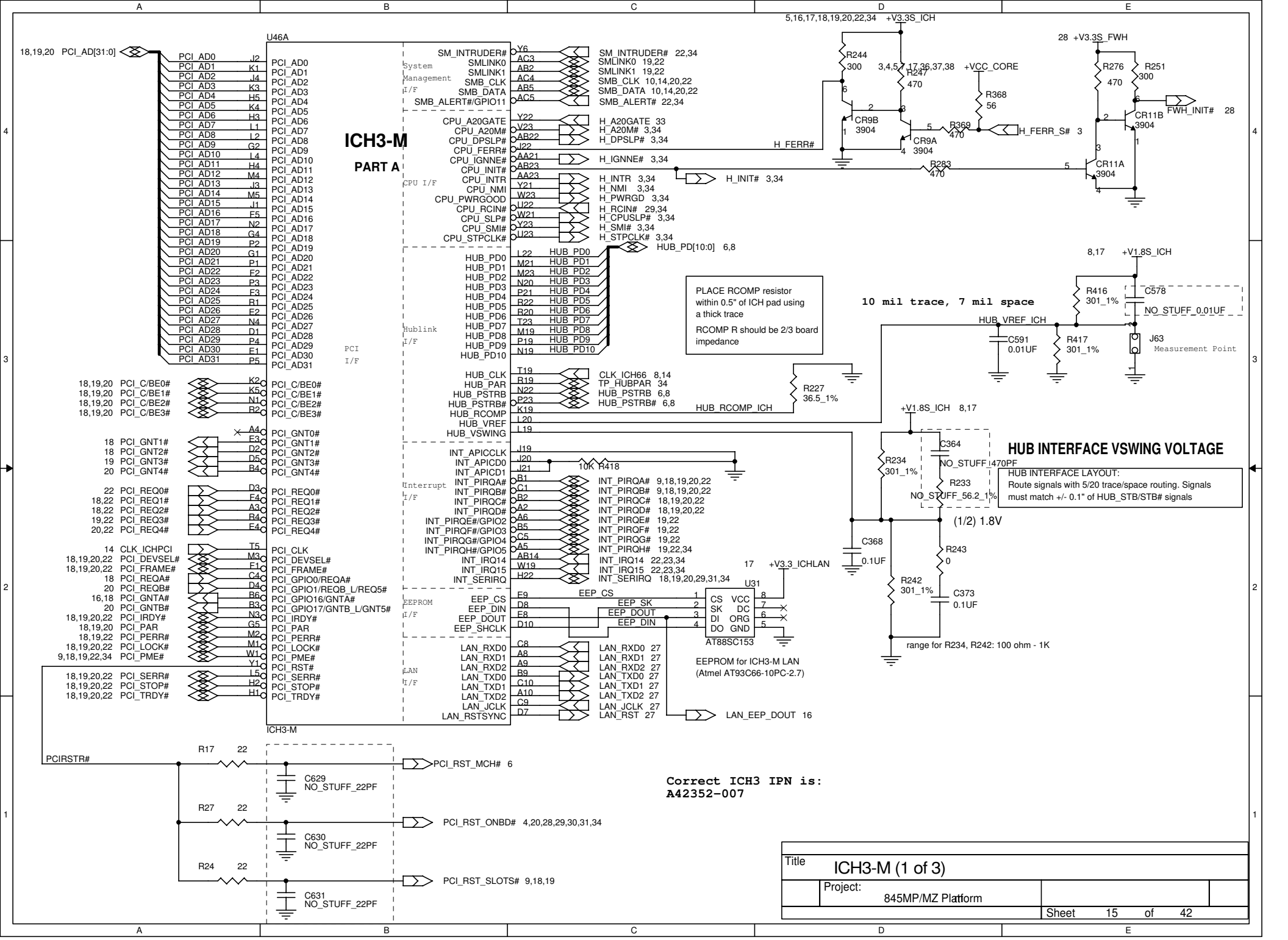
SEL1	SEL0	FUNCTION
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK

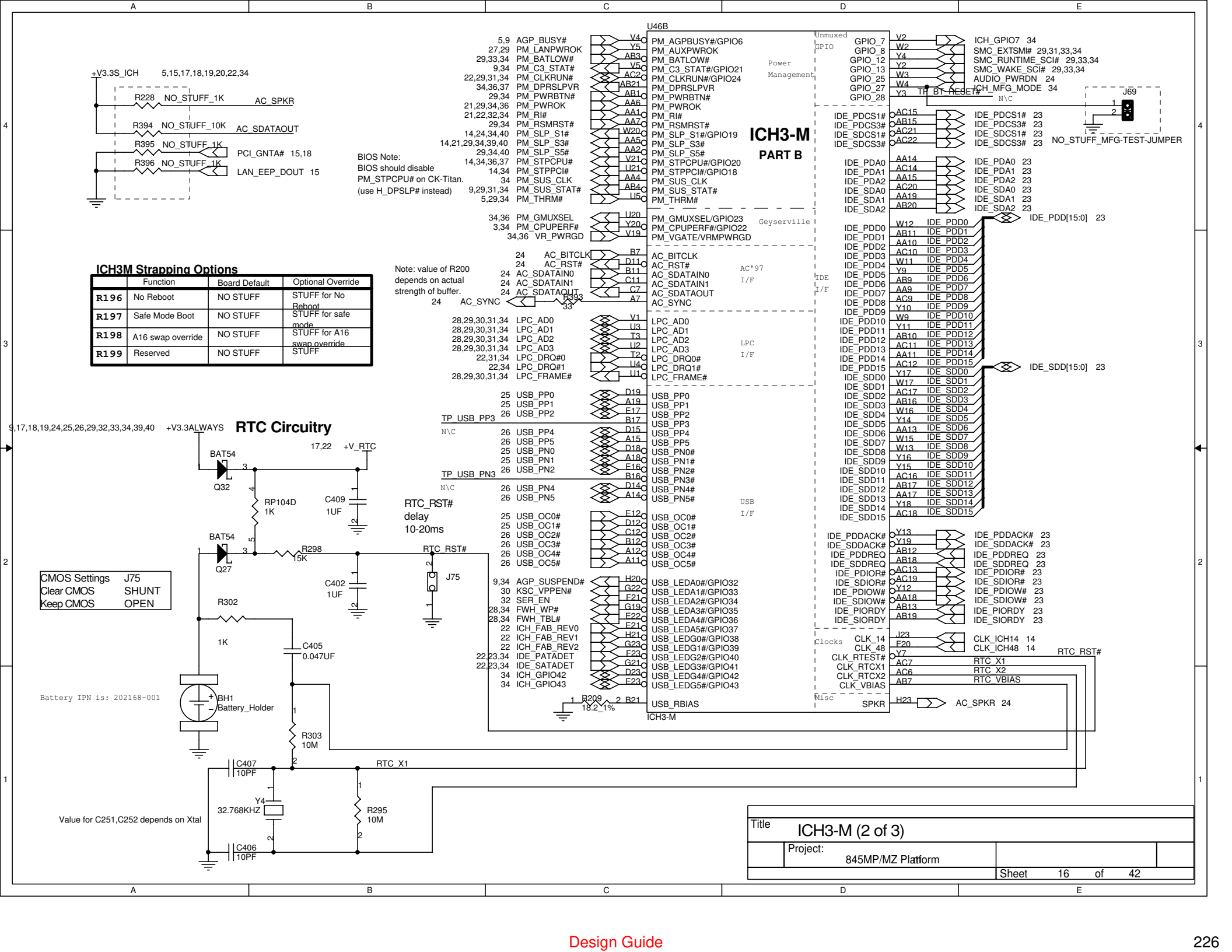
MULT	R331	CK408 CLOCK SWING CONFIG
1	475 1%	0.7 VOLTS
0	221 1%	1.0 VOLTS

Correct CK408 IPN is: A62115-001

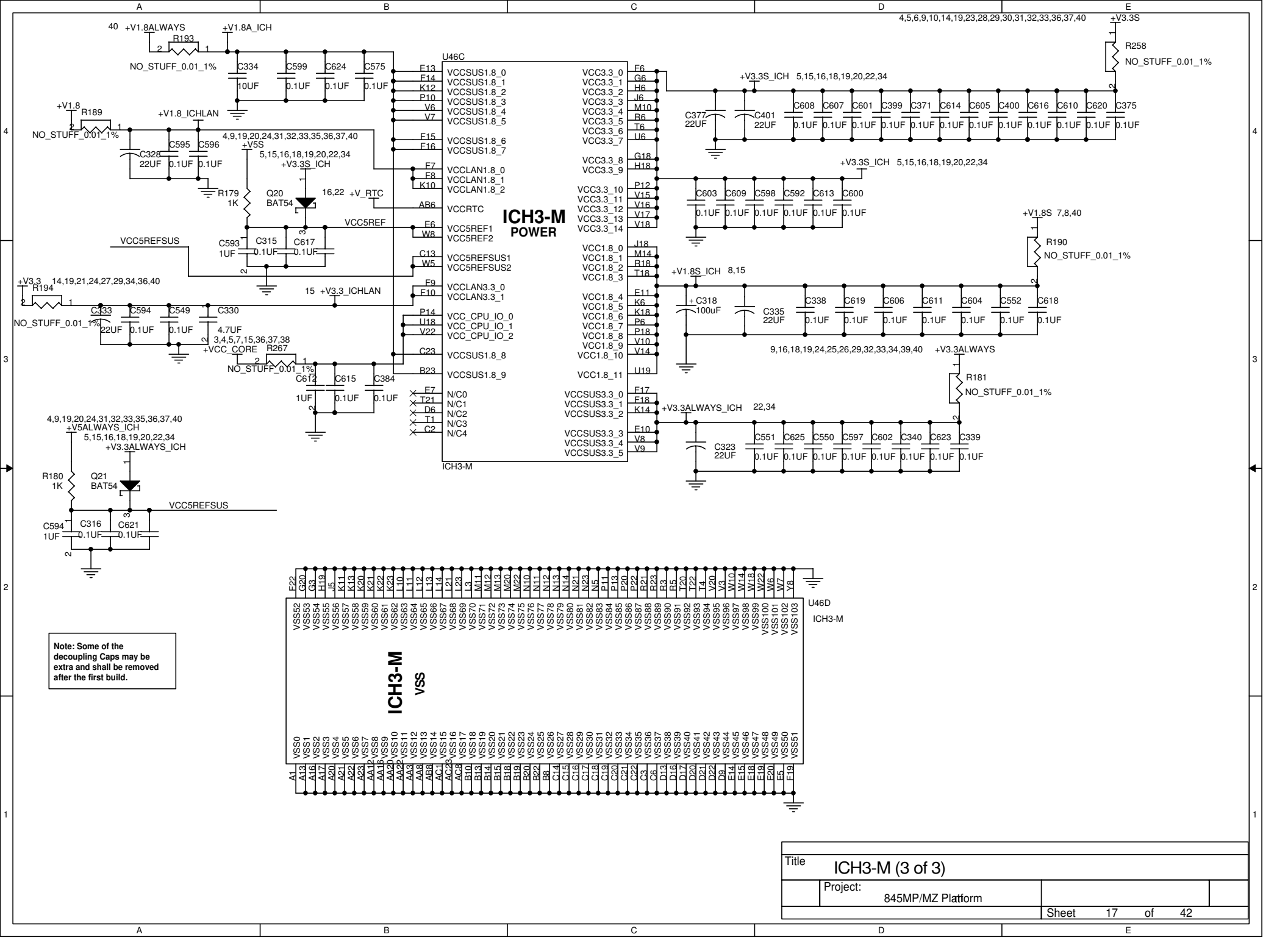
CK-408

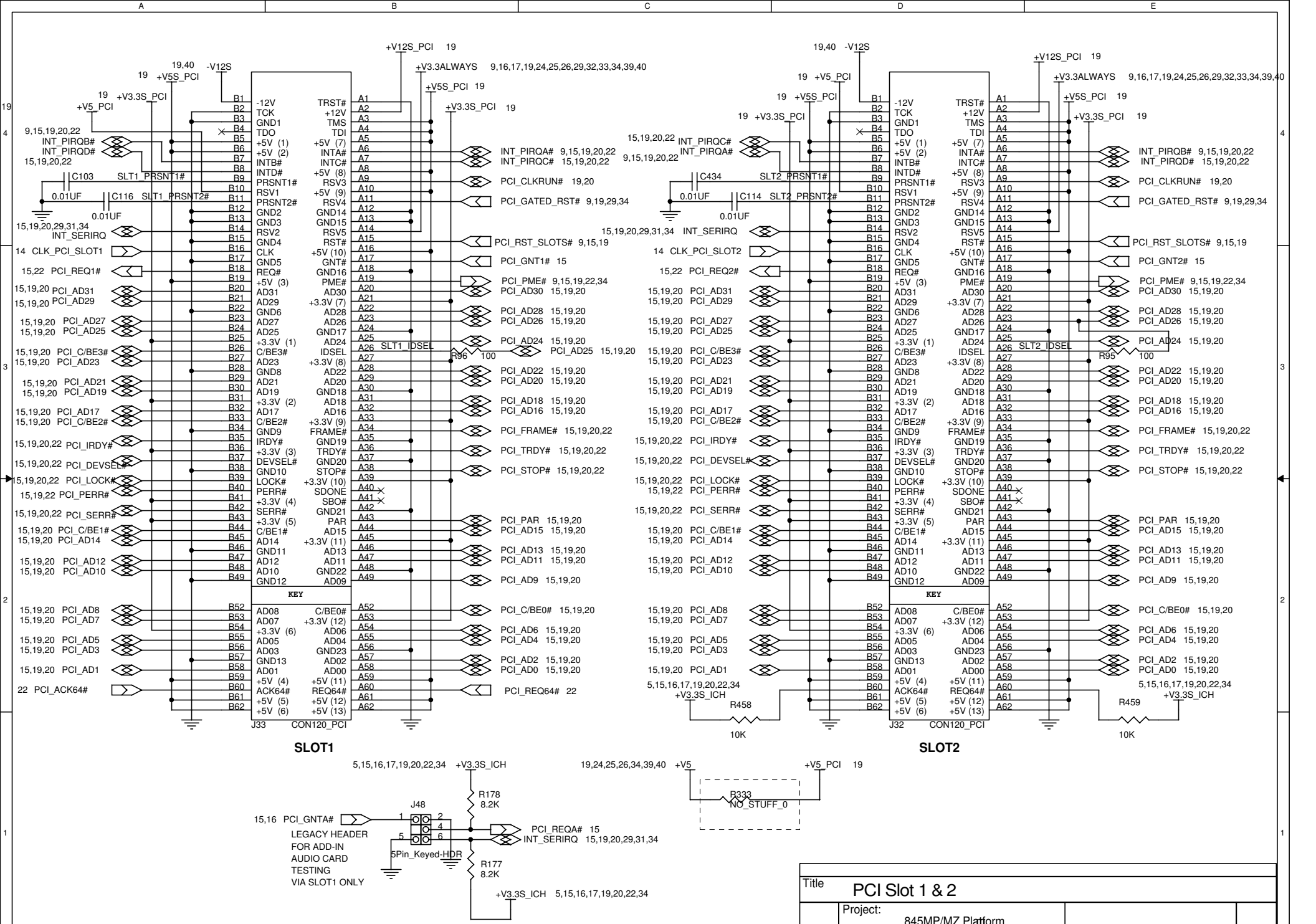
Title	CK-408	
	Project: 845MP/MZ Platform	
		Sheet 14 of 42

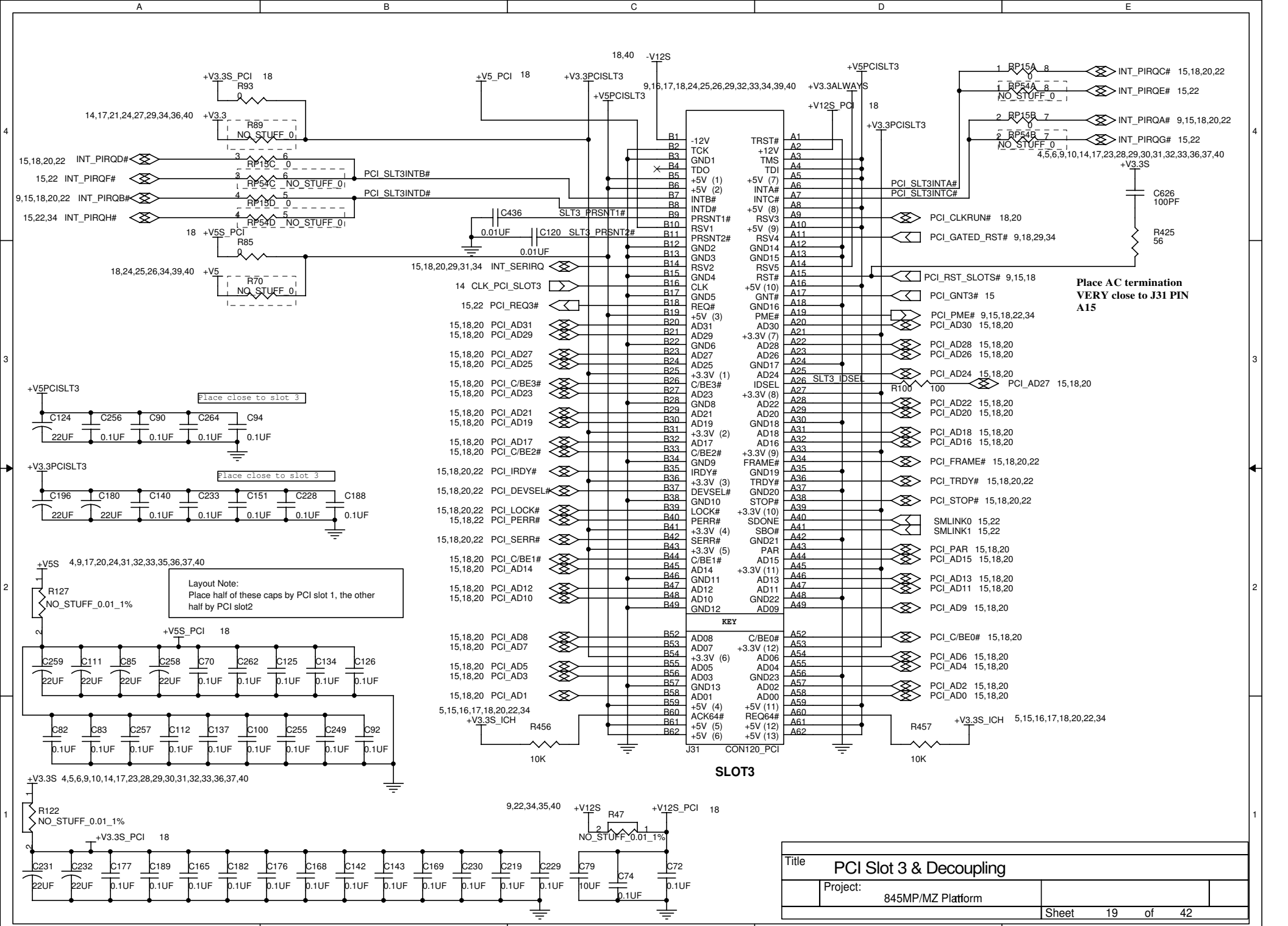

ICH3-M
PART A
U46A
ICH3-M
PCI_AD[31:0]
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
PCI_GNT0#
PCI_GNT1#
PCI_GNT2#
PCI_GNT3#
PCI_GNT4#
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
PCI_REQ3#
PCI_REQ4#
CLK_ICHPCI
PCI_DEVSEL#
PCI_FRAME#
PCI_REQA#
PCI_REQB#
PCI_GNTA#
PCI_IRDY#
PCI_PAR
PCI_PERR#
PCI_LOCK#
PCI_PME#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_CLK
PCI_RST#
PCI_GPIO0/REQA#
PCI_GPIO1/REQB_L/REQ5#
PCI_GPIO16/GNTA#
PCI_GPIO17/GNTB_L/GNT5#
PCI I/F
SM_INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11
System Management I/F
CPU_A20GATE
CPU_A20M#
CPU_DPSLP#
CPU_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_PWRGOOD
CPU_RCIN#
CPU_SLP#
CPU_SMI#
CPU_STPCLK#
CPU I/F
HUB_PD0
HUB_PD1
HUB_PD2
HUB_PD3
HUB_PD4
HUB_PD5
HUB_PD6
HUB_PD7
HUB_PD8
HUB_PD9
HUB_PD10
Hublink I/F
HUB_CLK
HUB_PAR
HUB_PSTRB
HUB_PSTRB#
HUB_RCOMP
HUB_VREF
HUB_VSWING
INT_APICCLK
INT_APICD0
INT_APICD1
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
INT_PIRQE#/GPIO2
INT_PIRQF#/GPIO3
INT_PIRQG#/GPIO4
INT_PIRQH#/GPIO5
INT_IRQ14
INT_IRQ15
INT_SERIRQ
Interrupt I/F
EEP_CS
EEP_DIN
EEP_DOUT
EEP_SHCLK
EEPROM I/F
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_JCLK
LAN_RSTSYNC
LAN I/F
H_FERR#
H_IGNNE#
H_INIT#
H_INTR
H_NMI
H_PWRGD
H_RCIN#
H_CPUSLP#
H_SMI#
H_STPCLK#
HUB_PD[10:0]
HUB_RCOMP_ICH
R227 36.5_1%
PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace
RCOMP R should be 2/3 board impedance
10 mil trace, 7 mil space
HUB_VREF_ICH
R416 301_1%
C578 NO_STUFF_0.01UF
C591 0.01UF
R417 301_1%
J63 Measurement Point
+V1.8S_ICH
HUB INTERFACE VSWING VOLTAGE
R234 301_1%
C364 NO_STUFF_470PF
R233 NO_STUFF_56.2_1%
(1/2) 1.8V
C368 0.1UF
R243 0
R242 301_1%
C373 0.1UF
range for R234, R242: 100 ohm - 1K
HUB INTERFACE LAYOUT:
Route signals with 5/20 trace/space routing. Signals must match +/- 0.1" of HUB_STB/STB# signals
+V3.3_ICHLAN
U31
CS VCC
SK DC
DI ORG
DO GND
AT88SC153
EEPROM for ICH3-M LAN
(Atmel AT93C66-10PC-2.7)
LAN_EEP_DOUT
+V3.3S_ICH
+VCC_CORE
+V3.3S_FWH
FWH_INIT#
H_FERR_S#
CR9A 3904
CR9B 3904
CR11A 3904
CR11B 3904
R244 300
R247 470
R368 56
R369 470
R276 470
R251 300
R283 470
PCIRSTR#
R17 22
R27 22
R24 22
C629 NO_STUFF_22PF
C630 NO_STUFF_22PF
C631 NO_STUFF_22PF
PCI_RST_MCH# 6
PCI_RST_ONBD# 4,20,28,29,30,31,34
PCI_RST_SLOTS# 9,18,19
Correct ICH3 IPN is:
A42352-007
Title
ICH3-M (1 of 3)
Project:
845MP/MZ Platform
Sheet 15 of 42

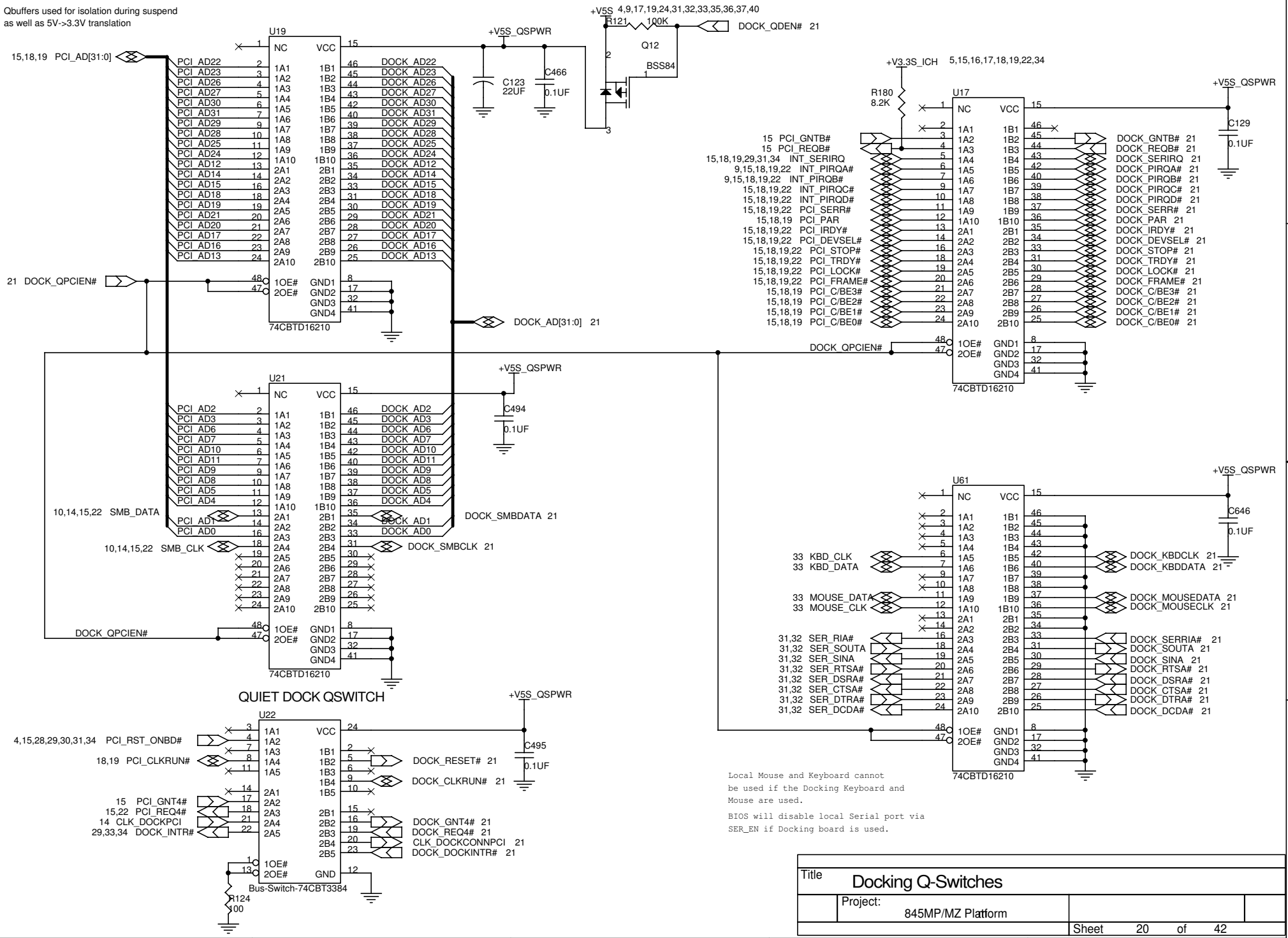


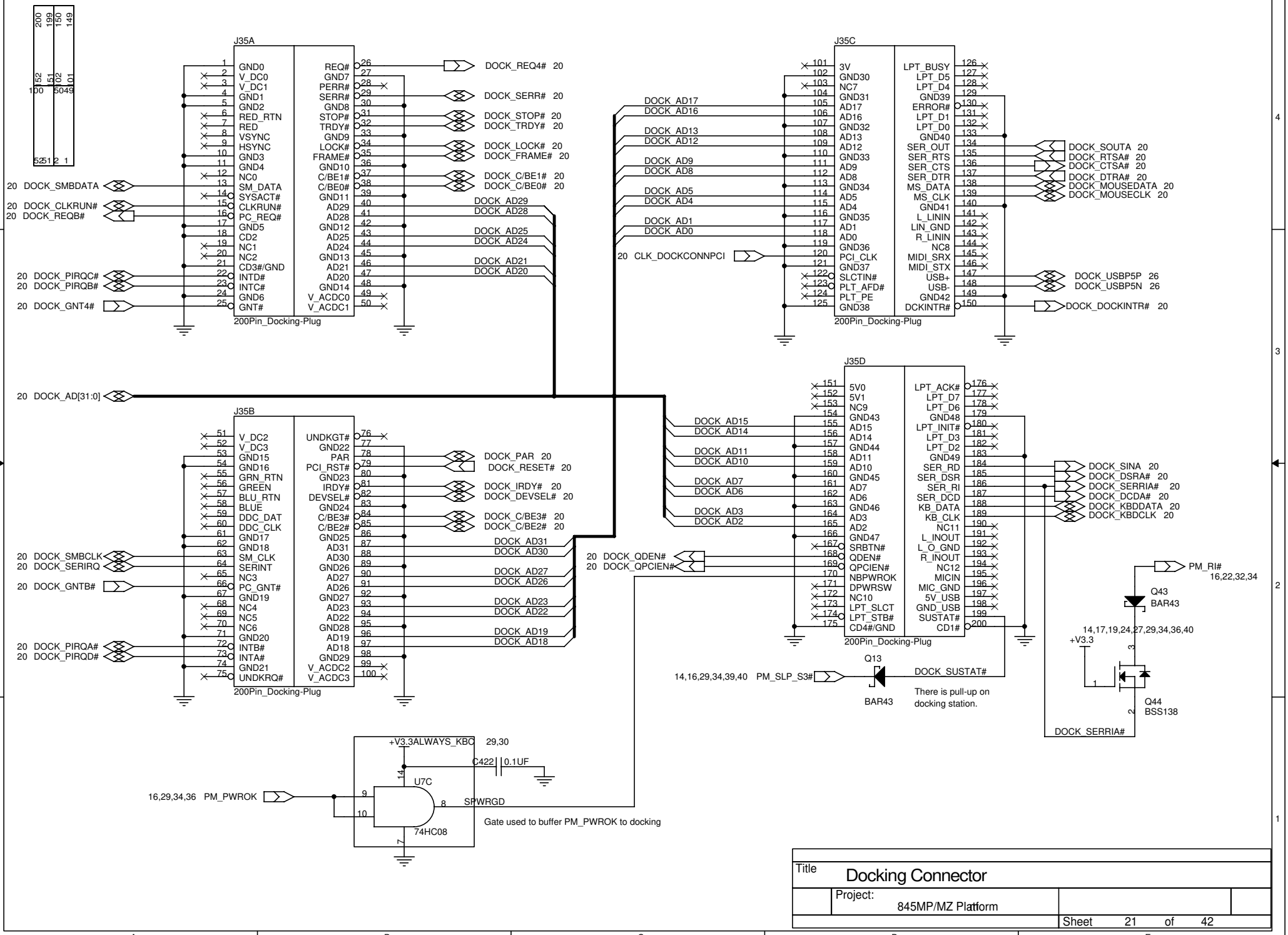
	Function	Board Default	Optional Override
R196	No Reboot	NO STUFF	STUFF for No Reboot
R197	Safe Mode Boot	NO STUFF	STUFF for safe mode
R198	A16 swap override	NO STUFF	STUFF for A16 swap override
R199	Reserved	NO STUFF	STUFF


ICH3-M
POWER
U46C
ICH3-M
U46D
ICH3-M
VSS
Note: Some of the decoupling Caps may be extra and shall be removed after the first build.
Title
ICH3-M (3 of 3)
Project:
845MP/MZ Platform
Sheet 17 of 42


SLOT1
SLOT2
J33 CON120_PCI
J32 CON120_PCI
KEY
+V12S_PCI 19
+V3.3ALWAYS 9,16,17,19,24,25,26,29,32,33,34,39,40
+V5S_PCI 19
+V3.3S_PCI 19
+V5_PCI 19
-V12S 19,40
SLT1_PRSNT1#
SLT1_PRSNT2#
SLT1_IDSEL
SLT2_PRSNT1#
SLT2_PRSNT2#
SLT2_IDSEL
C103 0.01UF
C116 0.01UF
C434 0.01UF
C114 0.01UF
R96 100
R95 100
R458 10K
R459 10K
INT_PIRQA# 9,15,19,20,22
INT_PIRQB# 9,15,19,20,22
INT_PIRQC# 15,19,20,22
INT_PIRQD# 15,19,20,22
INT_SERIRQ 15,19,20,29,31,34
PCI_CLKRUN# 19,20
PCI_GATED_RST# 9,19,29,34
PCI_RST_SLOTS# 9,15,19
PCI_GNT1# 15
PCI_GNT2# 15
PCI_REQ1# 15,22
PCI_REQ2# 15,22
PCI_PME# 9,15,19,22,34
CLK_PCI_SLOT1 14
CLK_PCI_SLOT2 14
PCI_AD31 15,19,20
PCI_AD30 15,19,20
PCI_AD29 15,19,20
PCI_AD28 15,19,20
PCI_AD27 15,19,20
PCI_AD26 15,19,20
PCI_AD25 15,19,20
PCI_AD24 15,19,20
PCI_C/BE3# 15,19,20
PCI_AD23 15,19,20
PCI_AD22 15,19,20
PCI_AD21 15,19,20
PCI_AD20 15,19,20
PCI_AD19 15,19,20
PCI_AD18 15,19,20
PCI_AD17 15,19,20
PCI_AD16 15,19,20
PCI_C/BE2# 15,19,20
PCI_FRAME# 15,19,20,22
PCI_IRDY# 15,19,20,22
PCI_TRDY# 15,19,20,22
PCI_DEVSEL# 15,19,20,22
PCI_STOP# 15,19,20,22
PCI_LOCK# 15,19,20,22
PCI_PERR# 15,19,22
PCI_SERR# 15,19,20,22
PCI_PAR 15,19,20
PCI_C/BE1# 15,19,20
PCI_AD15 15,19,20
PCI_AD14 15,19,20
PCI_AD13 15,19,20
PCI_AD12 15,19,20
PCI_AD11 15,19,20
PCI_AD10 15,19,20
PCI_AD9 15,19,20
PCI_C/BE0# 15,19,20
PCI_AD8 15,19,20
PCI_AD7 15,19,20
PCI_AD6 15,19,20
PCI_AD5 15,19,20
PCI_AD4 15,19,20
PCI_AD3 15,19,20
PCI_AD2 15,19,20
PCI_AD1 15,19,20
PCI_AD0 15,19,20
PCI_REQ64# 22
PCI_ACK64# 22
+V3.3S_ICH 5,15,16,17,19,20,22,34
R178 8.2K
R177 8.2K
J48
5Pin_Keyed-HDR
15,16 PCI_GNTA#
PCI_REQA# 15
INT_SERIRQ 15,19,20,29,31,34
LEGACY HEADER
FOR ADD-IN
AUDIO CARD
TESTING
VIA SLOT1 ONLY
19,24,25,26,34,39,40 +V5
R333
NO_STUFF_0
Title
PCI Slot 1 & 2
Project:
845MP/MZ Platform
Sheet 18 of 42


SLOT3
J31 CON120_PCI
KEY
Place close to slot 3
Place close to slot 3
Layout Note:
Place half of these caps by PCI slot 1, the other half by PCI slot2
Place AC termination VERY close to J31 PIN A15
Title
PCI Slot 3 & Decoupling
Project:
845MP/MZ Platform
Sheet 19 of 42


Qbuffers used for isolation during suspend
as well as 5V->3.3V translation
U19
74CBTD16210
U21
74CBTD16210
U17
74CBTD16210
U61
74CBTD16210
U22
Bus-Switch-74CBT3384
QUIET DOCK QSWITCH
+V5S_QSPWR
+V3.3S_ICH
+V5S
DOCK_QDEN# 21
DOCK_AD[31:0] 21
DOCK_SMBDATA 21
DOCK_SMBCLK 21
DOCK_QPCIEN#
Local Mouse and Keyboard cannot
be used if the Docking Keyboard and
Mouse are used.
BIOS will disable local Serial port via
SER_EN if Docking board is used.
Title
Docking Q-Switches
Project:
845MP/MZ Platform
Sheet 20 of 42


J35A
J35B
J35C
J35D
200Pin_Docking-Plug
20 DOCK_AD[31:0]
20 DOCK_SMBDATA
20 DOCK_CLKRUN#
20 DOCK_REQB#
20 DOCK_PIRQC#
20 DOCK_PIRQB#
20 DOCK_GNT4#
20 DOCK_SMBCLK
20 DOCK_SERIRQ
20 DOCK_GNTB#
20 DOCK_PIRQA#
20 DOCK_PIRQD#
20 DOCK_QDEN#
20 DOCK_QPCIEN#
20 CLK_DOCKCONNPCI
DOCK_REQ4# 20
DOCK_SERR# 20
DOCK_STOP# 20
DOCK_TRDY# 20
DOCK_LOCK# 20
DOCK_FRAME# 20
DOCK_C/BE1# 20
DOCK_C/BE0# 20
DOCK_PAR 20
DOCK_RESET# 20
DOCK_IRDY# 20
DOCK_DEVSEL# 20
DOCK_C/BE3# 20
DOCK_C/BE2# 20
DOCK_SOUTA 20
DOCK_RTSA# 20
DOCK_CTSA# 20
DOCK_DTRA# 20
DOCK_MOUSEDATA 20
DOCK_MOUSECLK 20
DOCK_USBP5P 26
DOCK_USBP5N 26
DOCK_DOCKINTR# 20
DOCK_SINA 20
DOCK_DSRA# 20
DOCK_SERRIA# 20
DOCK_DCDA# 20
DOCK_KBDDATA 20
DOCK_KBDCLK 20
PM_RI# 16,22,32,34
Q43 BAR43
14,17,19,24,27,29,34,36,40
+V3.3
Q44 BSS138
DOCK_SERRIA#
Q13 BAR43
14,16,29,34,39,40 PM_SLP_S3#
DOCK_SUSTAT#
There is pull-up on docking station.
+V3.3ALWAYS_KBC 29,30
C422 0.1UF
U7C 74HC08
16,29,34,36 PM_PWROK
SPWRGD
Gate used to buffer PM_PWROK to docking
Title
Docking Connector
Project:
845MP/MZ Platform
Sheet 21 of 42

Layout Note:
Signals on RPs shown below
can be swapped to aid routing.

5,15,16,17,18,19,20,34 +V3.3S_ICH

15,18,19,20 PCI_FRAME# — RP93A 1 8 8.2K
15,18,19,20 PCI_IRDY# — RP96B 2 7 8.2K
15,18,19,20 PCI_TRDY# — RP94D 4 5 8.2K
15,18,19,20 PCI_STOP# — RP94C 3 6 8.2K

15,18,19,20 PCI_SERR# — RP94B 2 7 8.2K
15,18,19,20 PCI_DEVSEL# — RP94A 1 8 8.2K
15,18,19 PCI_PERR# — RP96C 3 6 8.2K
15,18,19,20 PCI_LOCK# — RP96D 4 5 8.2K

15 PCI_REQ0# — RP93D 4 5 8.2K

15,18 PCI_REQ1# — RP93B 2 7 8.2K
15,18 PCI_REQ2# — RP75A 1 8 8.2K
15,19 PCI_REQ3# — RP96A 1 8 8.2K
15,20 PCI_REQ4# — RP93C 3 6 8.2K

Pull-ups for PCI_GNT#0 and PCI_GNT#3 are by PCI slots

15,23,34 INT_IRQ14 — RP103D 4 5 8.2K

15,23,34 INT_IRQ15 — RP103A 1 8 8.2K
9,15,18,19,20 INT_PIRQA# — RP87B 2 7 8.2K
9,15,18,19,20 INT_PIRQB# — RP87A 1 8 8.2K

15,18,19,20 INT_PIRQC# — RP87C 3 6 8.2K
15,18,19,20 INT_PIRQD# — RP87D 4 5 8.2K

15,19 INT_PIRQE# — RP42A 1 8 8.2K
15,19 INT_PIRQF# — RP42B 2 7 8.2K
15,19 INT_PIRQG# — RP42C 3 6 8.2K
15,19,34 INT_PIRQH# — RP42D 4 5 8.2K
18 PCI_REQ64# — RP21A 1 8 10K
18 PCI_ACK64# — RP21B 2 7 10K

16,23,34 IDE_PATADET — RP105A 1 8 NO_STUFF_10K
16,23,34 IDE_SATADET — RP105B 2 7 NO_STUFF_10K
16,29,31,34 PM_CLKRUN# — RP99D 4 5 10K
16,31,34 LPC_DRQ#0 — R259 NO_STUFF_10K
16,34 LPC_DRQ#1 — R260 NO_STUFF_10K

DRQ0# & DRQ1# have
weak internal
pullups

+V3.3ALWAYS_ICH 17,34

16,21,32,34 PM_RI# — RP98C 3 6 10K
15,34 SMB_ALERT# — RP101A 1 8 10K
9,15,18,19,34 PCI_PME# — R419 10K

+V_RTC 16,17

15,34 SM_INTRUDER# — R307 100K

010 = 3 binary = Sheeks Fab 3

FAB REVISION

5,15,16,17,18,19,20,34 +V3.3S_ICH

R400 NO_STUFF_10K
R401 10K
R413 10K

16 ICH_FAB_REV0
16 ICH_FAB_REV1
16 ICH_FAB_REV2

R414 1K
R415 NO_STUFF_1K
R399 NO_STUFF_1K

AOL II LAN SUPPORT

+V3.3ALWAYS_ICH 17,34

R292 4.7K
RP101B 10K
SMLINK0 15,19

9,19,34,35,40 +V12S
BSS138 Q31

SMB_CLK 10,14,15,20

17,34 +V3.3ALWAYS_ICH

R296 4.7K
RP101C 10K
SMLINK1 15,19

Q1 and Q2 connect SMLINK and SMBUS in S0 for SMBus 2.0 compliance.

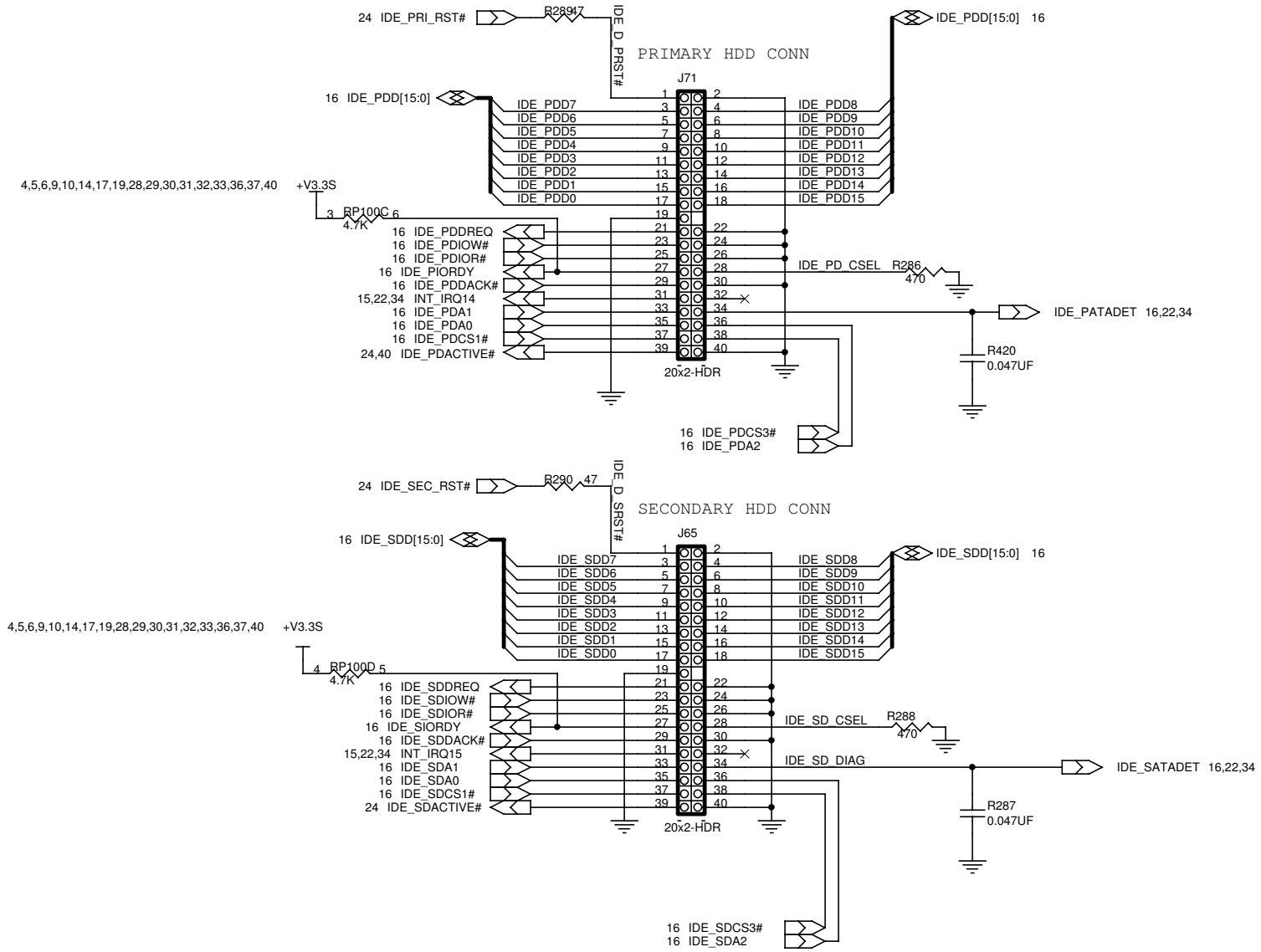
9,19,34,35,40 +V12S
BSS138 Q29

SMB_DATA 10,14,15,20

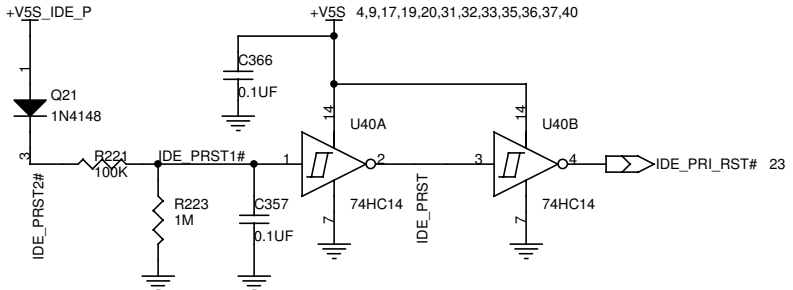
5,15,16,17,18,19,20,34 +V3.3S_ICH

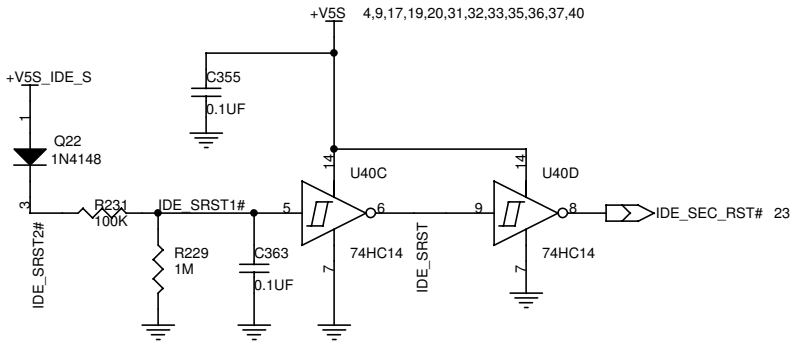
J68
CON4_HDR

Title	ICH3-M Pullups and Testpoints
Project:	845MP/MZ Platform
Sheet	22 of 42



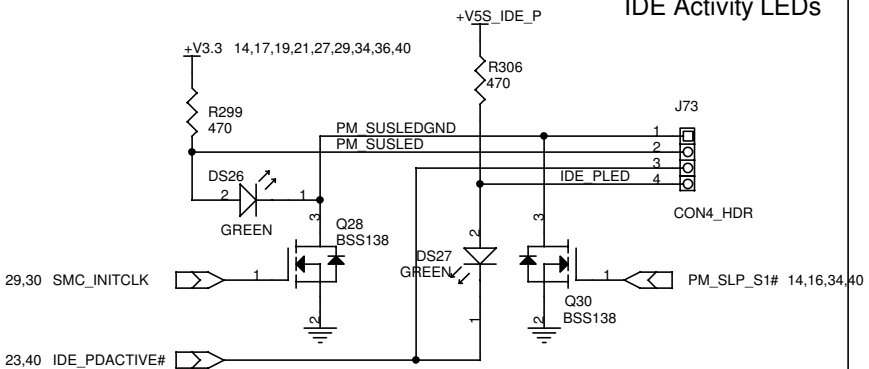
Title	IDE 1 of 2
Project:	845MP/MZ Platform
Sheet	23 of 42

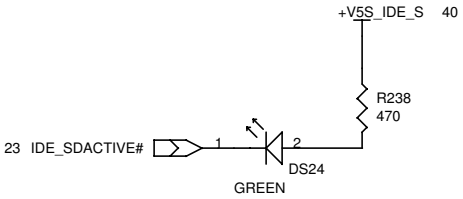




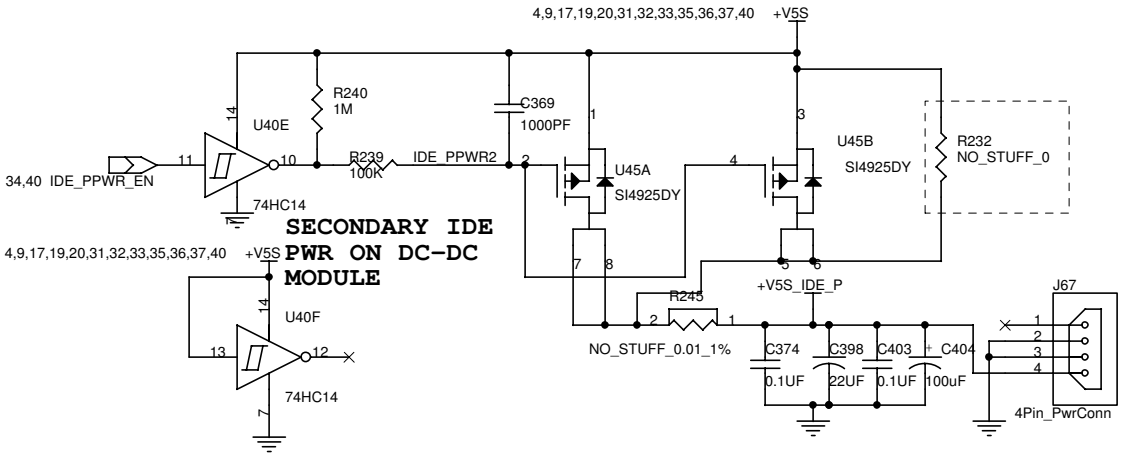
IDE Reset Circuitry

IDE Activity LEDs



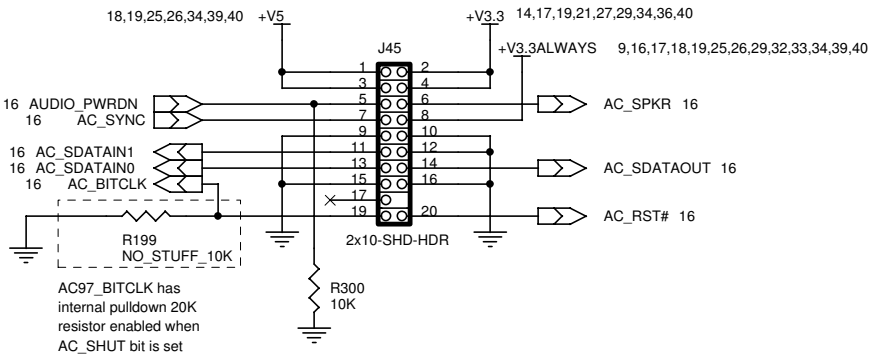


Primary IDE Power

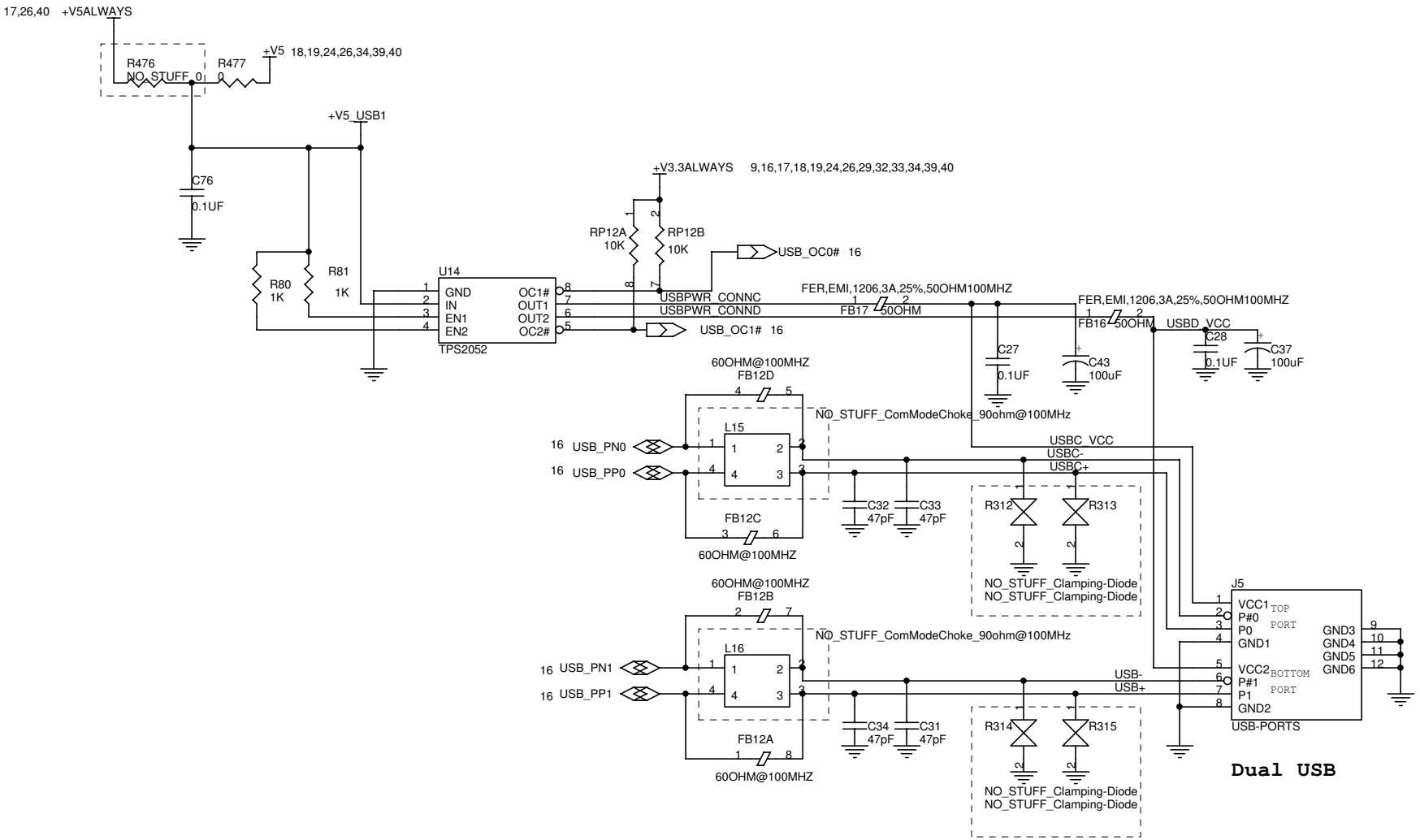


Mobile Drive Only

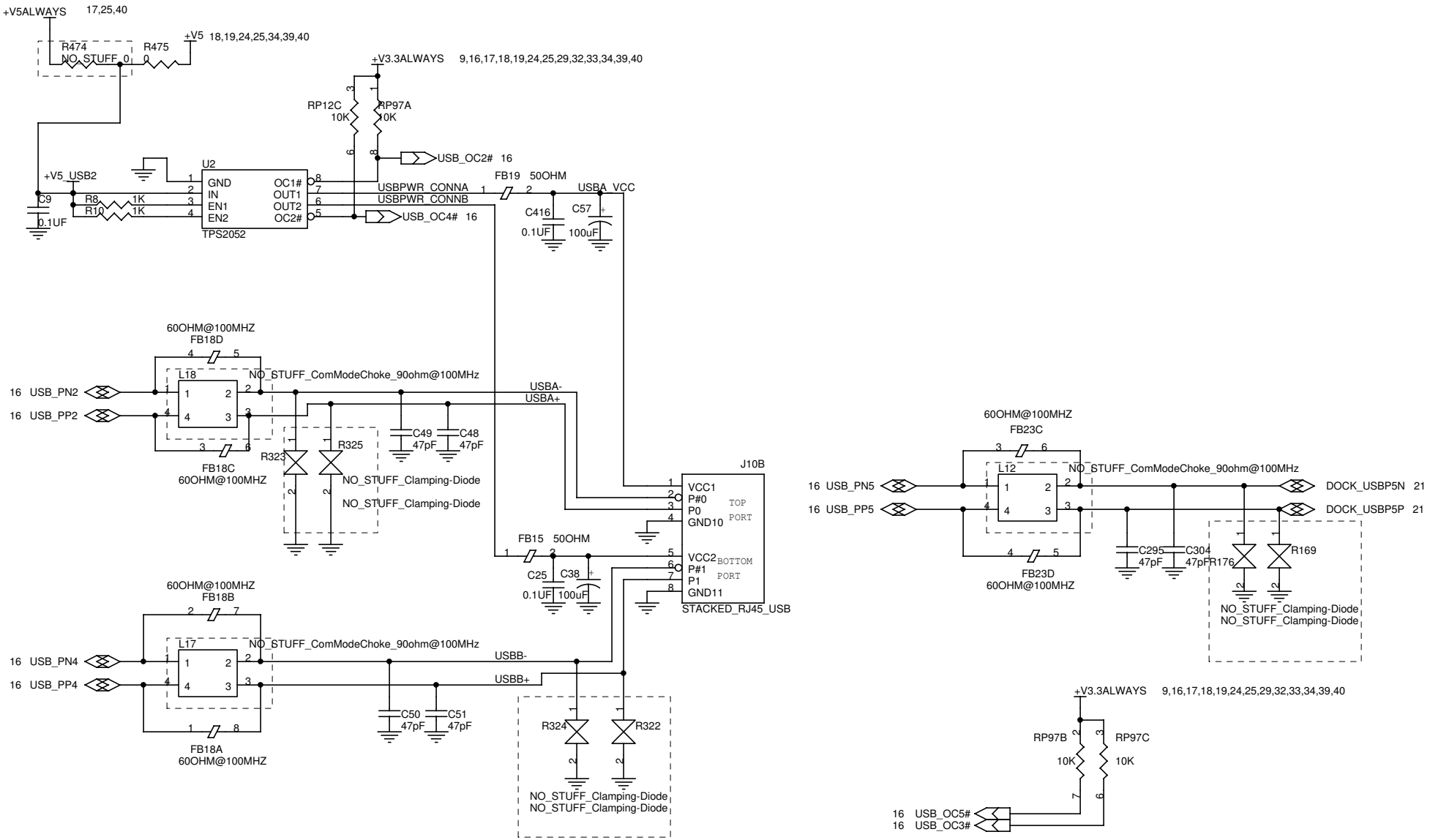
MDC INTERPOSER HEADER



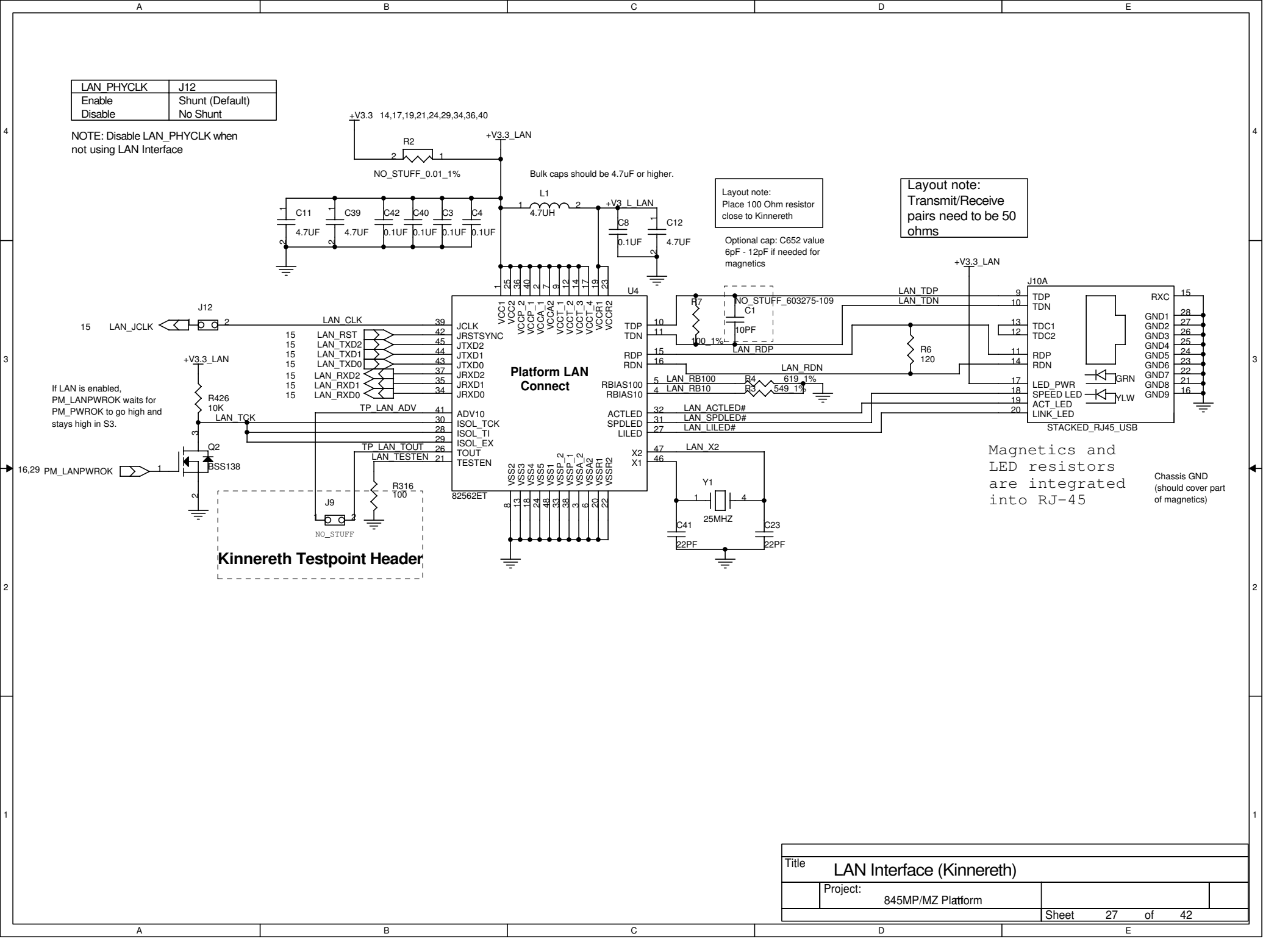
Title	IDE 2 of 2 / MDC INTERPOSER		
	Project: 845MP/MZ Platform		
		Sheet 24 of 42	

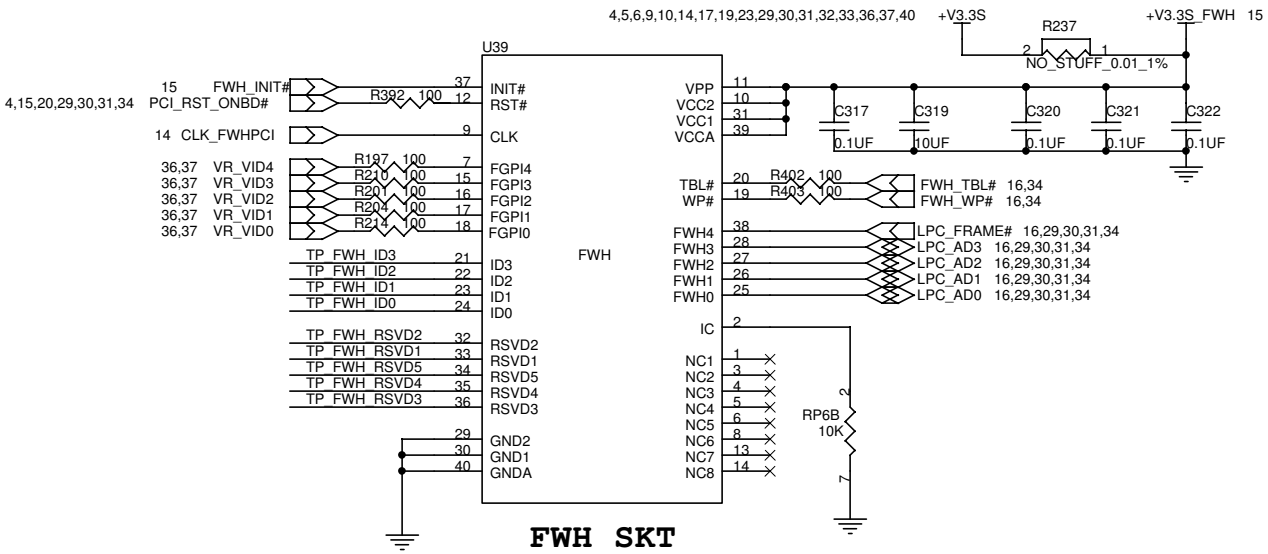


Title	USB (1 of 2)
Project:	845MP/MZ Platform
Sheet	25 of 42



Title	USB Connector (2 OF 2)
Project:	845MP/MZ Platform
Sheet	26 of 42


LAN_PHYCLK | J12
Enable | Shunt (Default)
Disable | No Shunt
NOTE: Disable LAN_PHYCLK when not using LAN Interface
+V3.3 14,17,19,21,24,29,34,36,40
+V3.3_LAN
R2
NO_STUFF_0.01_1%
Bulk caps should be 4.7uF or higher.
L1
4.7UH
+V3_L_LAN
C11 4.7UF
C39 4.7UF
C42 0.1UF
C40 0.1UF
C3 0.1UF
C4 0.1UF
C8 0.1UF
C12 4.7UF
Layout note: Place 100 Ohm resistor close to Kinnereth
Optional cap: C652 value 6pF - 12pF if needed for magnetics
Layout note: Transmit/Receive pairs need to be 50 ohms
U4
Platform LAN Connect
82562ET
JCLK
JRSTSYNC
JTXD2
JTXD1
JTXD0
JRXD2
JRXD1
JRXD0
ADV10
ISOL_TCK
ISOL_TI
ISOL_EX
TOUT
TESTEN
TDP
TDN
RDP
RDN
RBIAS100
RBIAS10
ACTLED
SPDLED
LILED
X2
X1
R7 100_1%
C1 10PF
NO_STUFF_603275-109
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN
R6 120
R4 619_1%
R3 549_1%
LAN_RB100
LAN_RB10
LAN_ACTLED#
LAN_SPDLED#
LAN_LILED#
LAN_X2
Y1 25MHZ
C41 22PF
C23 22PF
J12
15 LAN_JCLK
LAN_CLK
15 LAN_RST
15 LAN_TXD2
15 LAN_TXD1
15 LAN_TXD0
15 LAN_RXD2
15 LAN_RXD1
15 LAN_RXD0
TP_LAN_ADV
TP_LAN_TOUT
LAN_TESTEN
+V3.3_LAN
R426 10K
LAN_TCK
Q2 BSS138
16,29 PM_LANPWROK
If LAN is enabled, PM_LANPWROK waits for PM_PWROK to go high and stays high in S3.
J9
NO_STUFF
R316 100
Kinnereth Testpoint Header
J10A
TDP
TDN
TDC1
TDC2
RDP
RDN
LED_PWR
SPEED LED
ACT_LED
LINK_LED
RXC
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GRN
YLW
STACKED_RJ45_USB
Magnetics and LED resistors are integrated into RJ-45
Chassis GND (should cover part of magnetics)
Title
LAN Interface (Kinnereth)
Project:
845MP/MZ Platform
Sheet 27 of 42

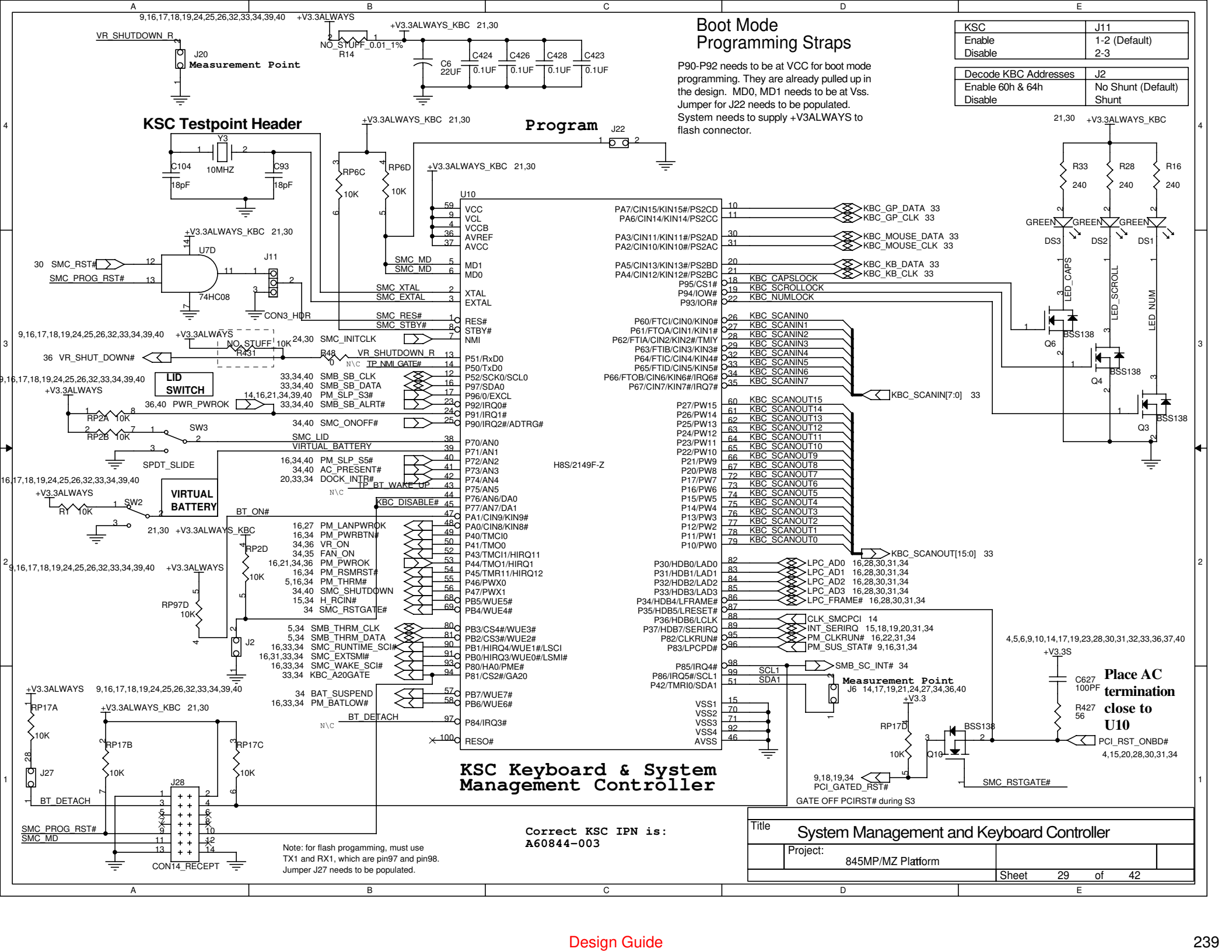


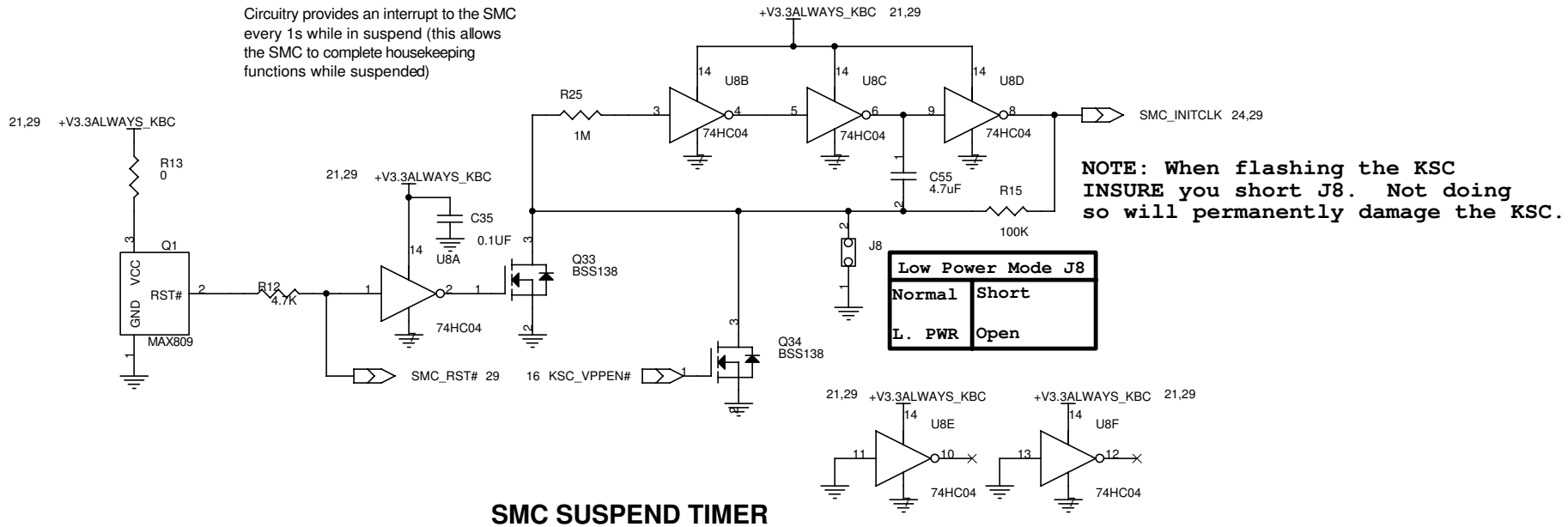
FWH SKT

FWH sits in the
FWH_TSOP_Socket

FWH IPN is:
A60882-004

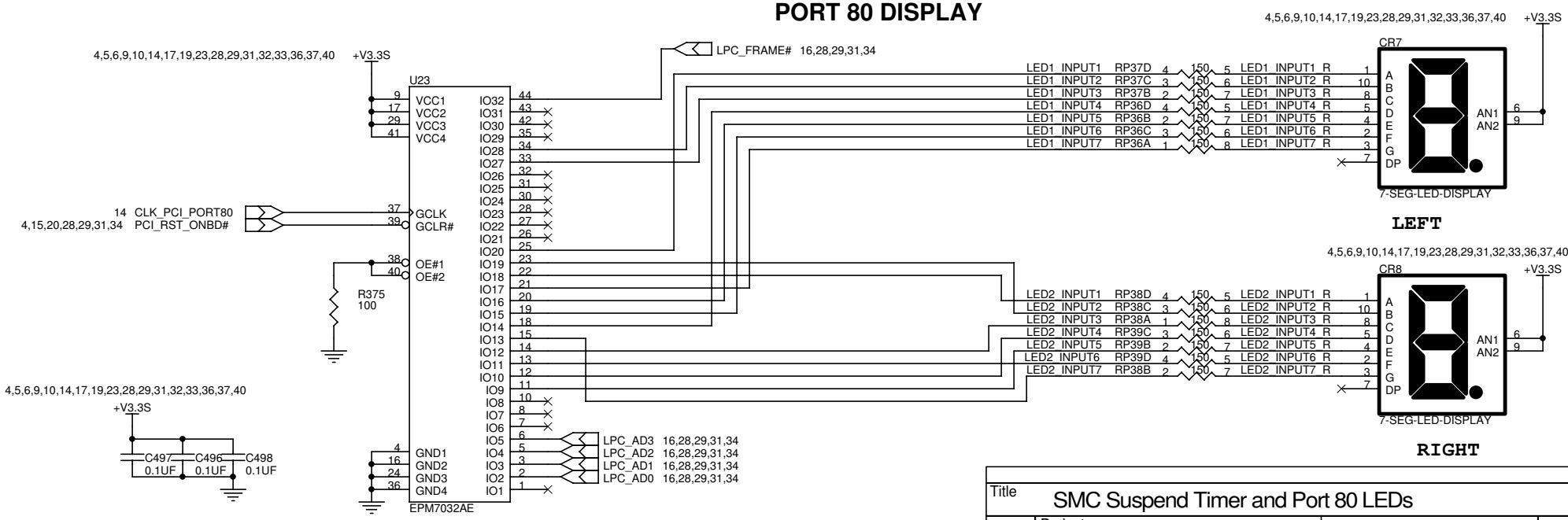
Title	FWH		
	Project: 845MP/MZ Platform		
		Sheet 28 of 42	


Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J22 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
KSC | J11
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J2
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
KSC Testpoint Header
Program
J22
U10
H8S/2149F-Z
KSC Keyboard & System Management Controller
LID SWITCH
VIRTUAL BATTERY
SPDT_SLIDE
Measurement Point
J20
J6
Place AC termination close to U10
Correct KSC IPN is: A60844-003
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98. Jumper J27 needs to be populated.
GATE OFF PCIRST# during S3
Title
System Management and Keyboard Controller
Project:
845MP/MZ Platform
Sheet 29 of 42

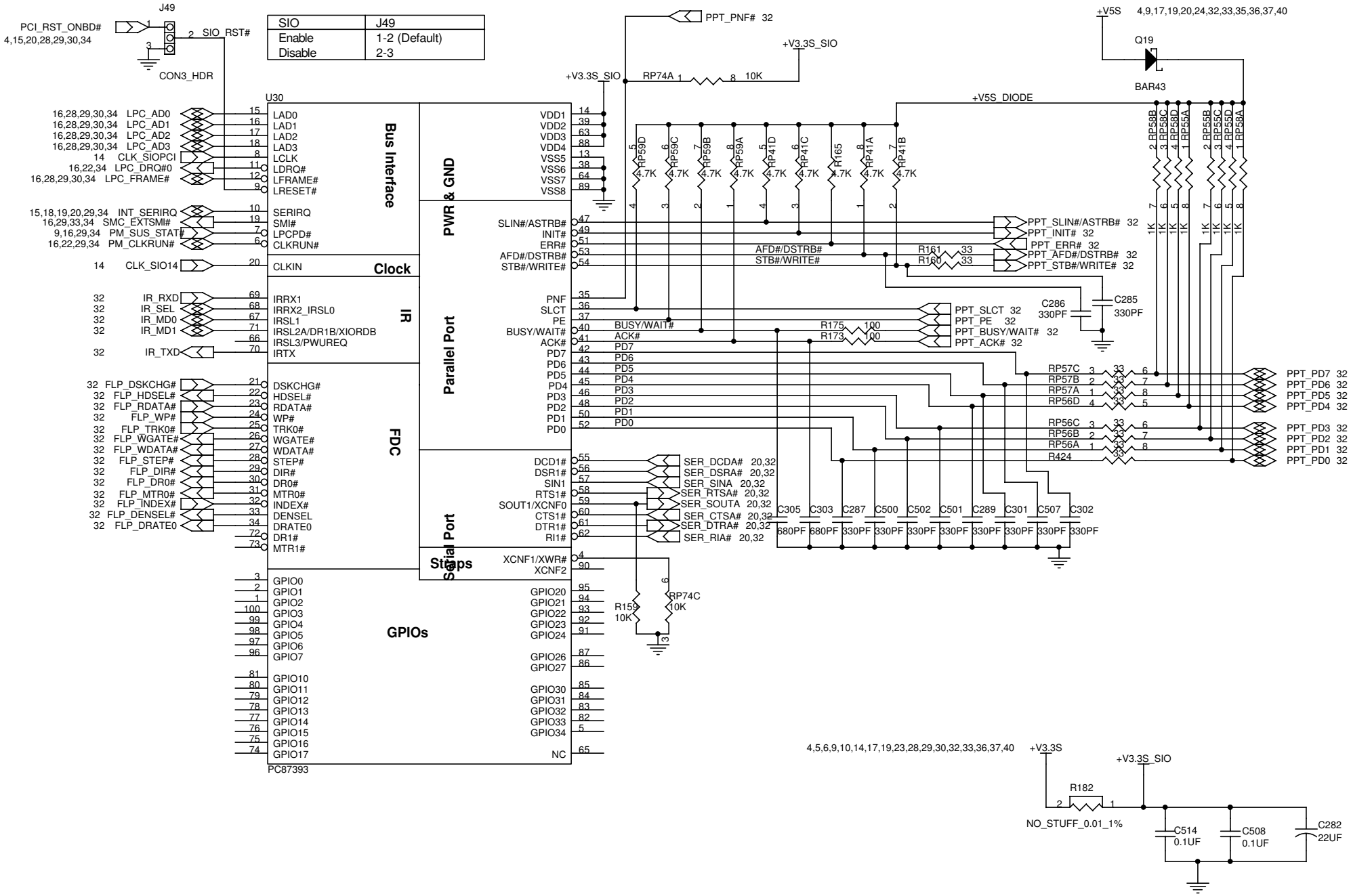


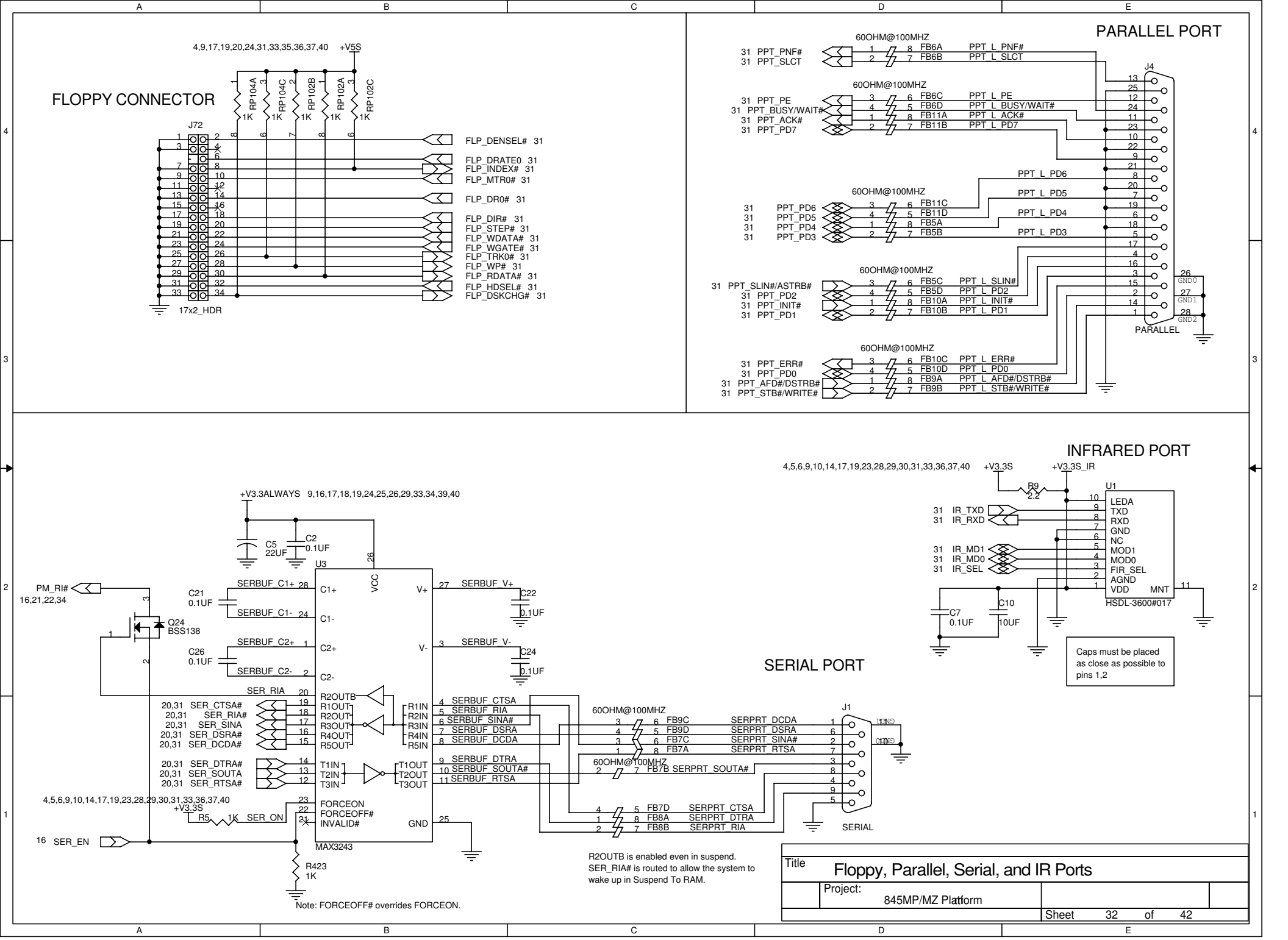
SMC SUSPEND TIMER

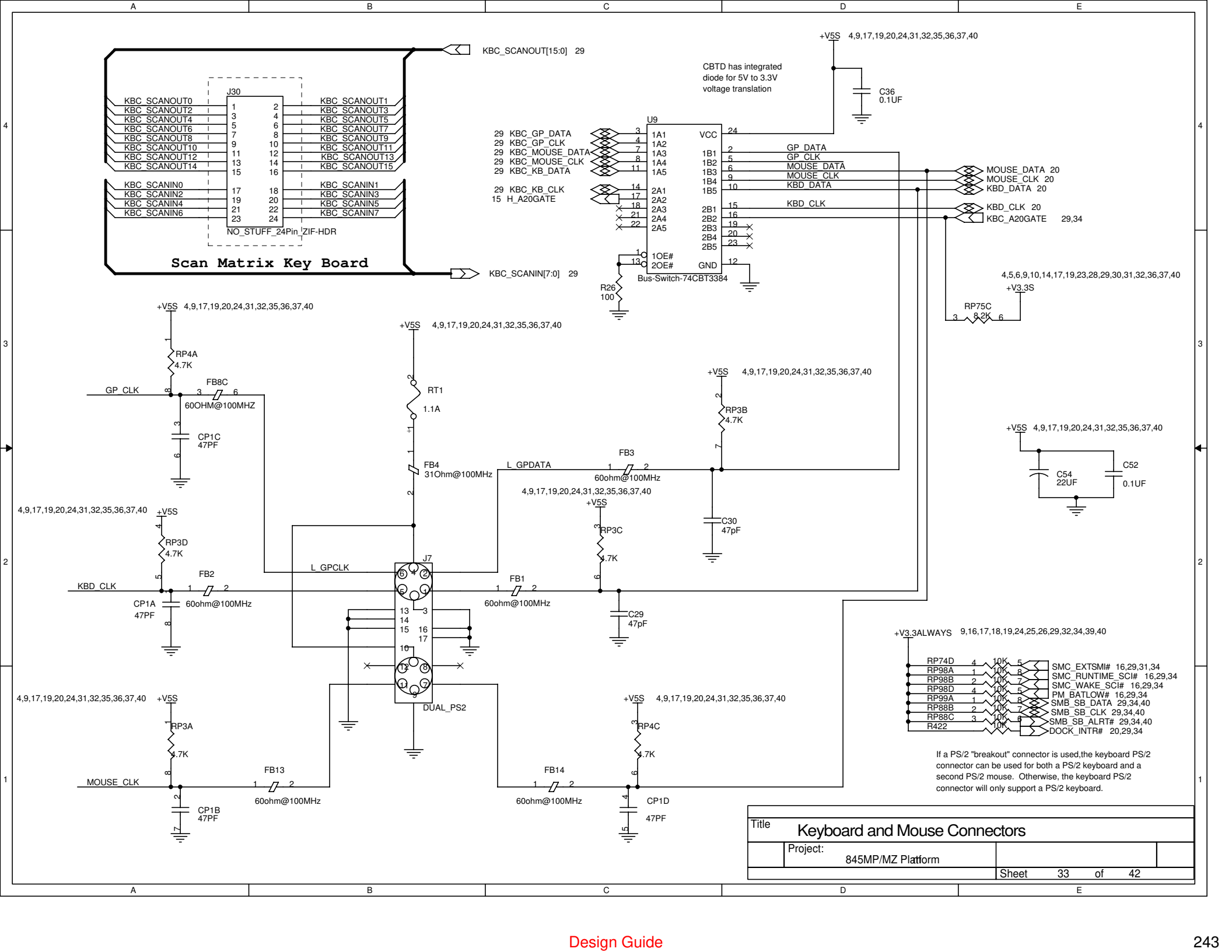
PORT 80 DISPLAY

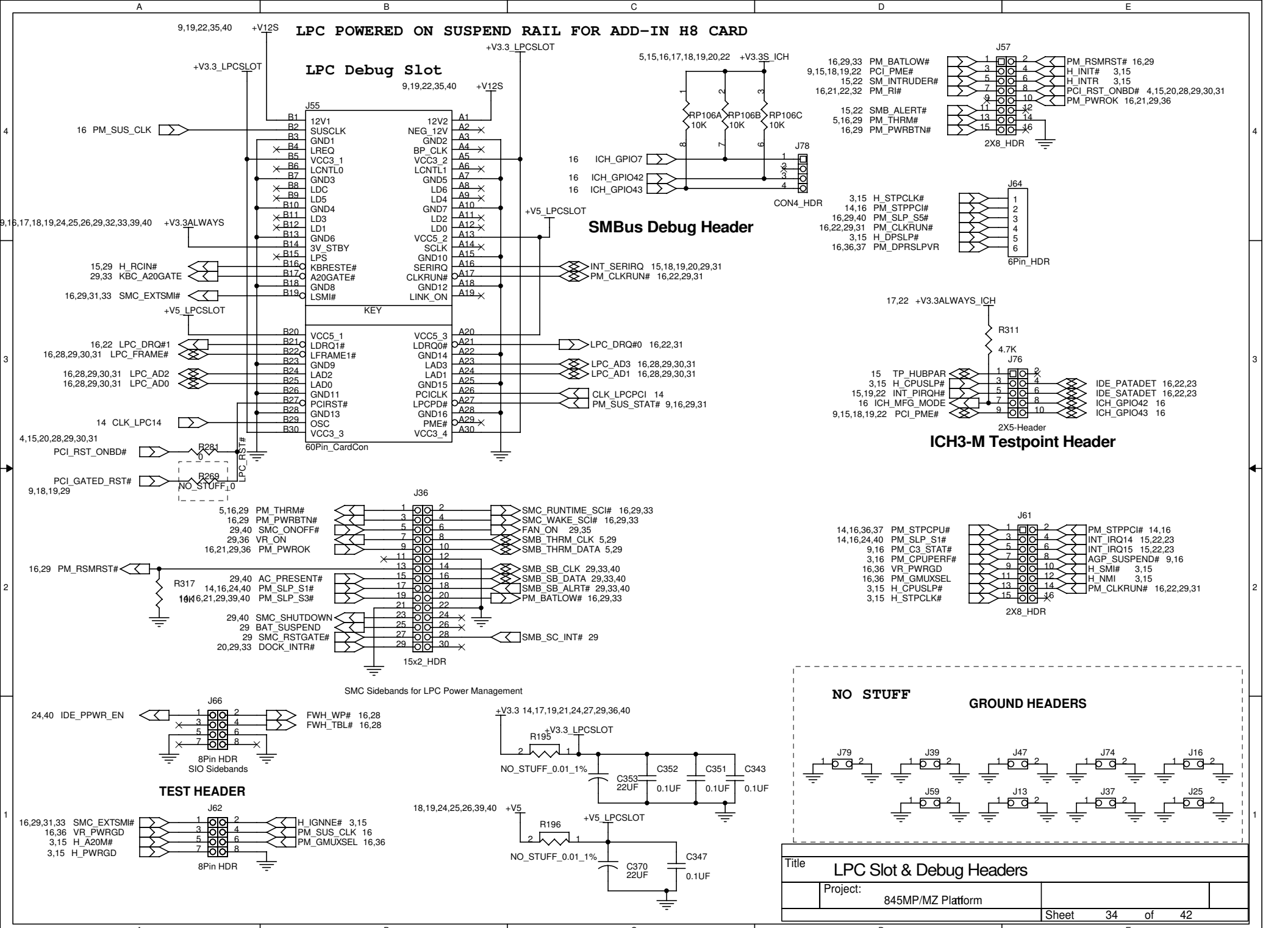


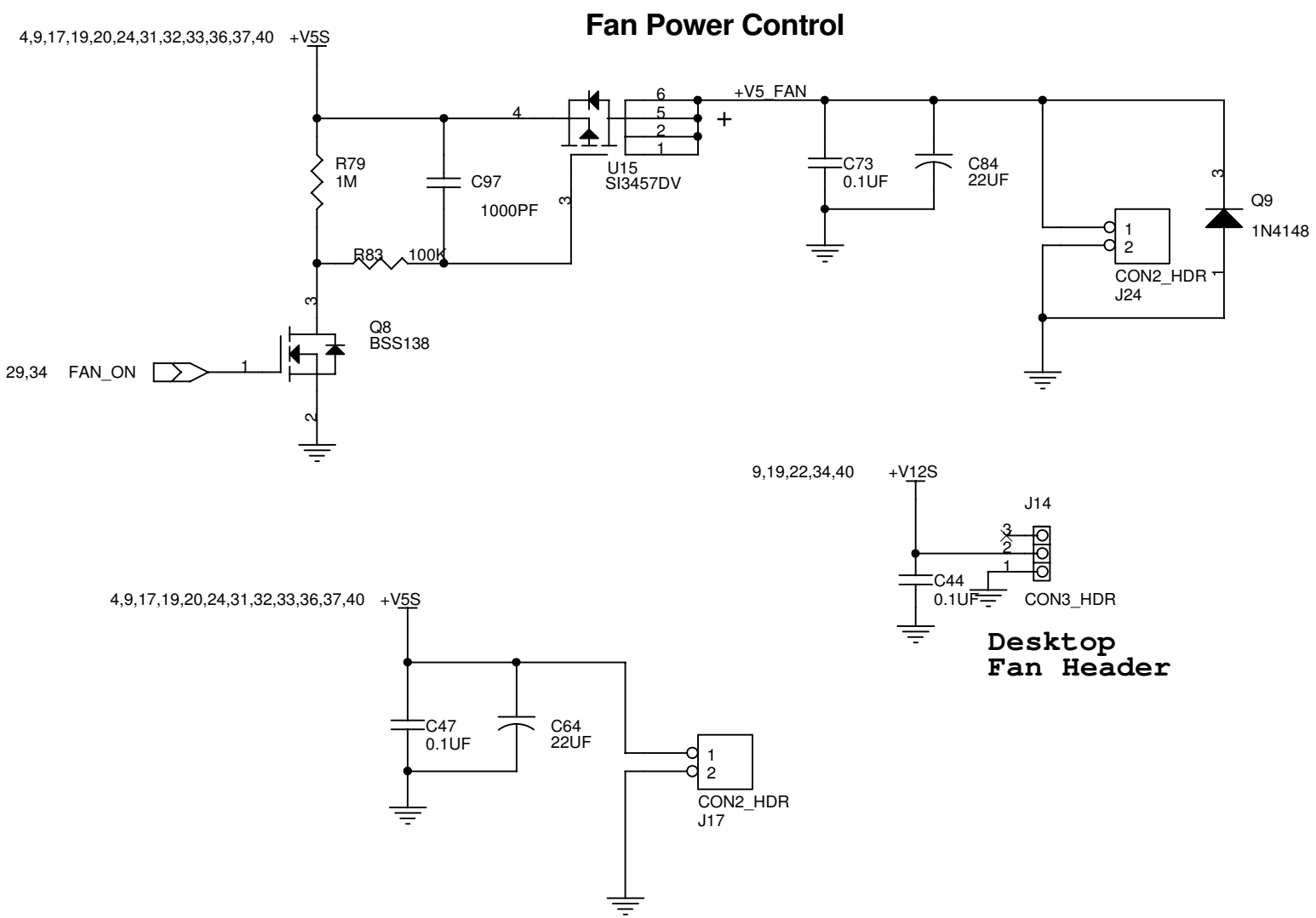
Title	SMC Suspend Timer and Port 80 LEDs
Project:	845MP/MZ Platform
Sheet	30 of 42


J49
PCI_RST_ONBD#
4,15,20,28,29,30,34
SIO_RST#
CON3_HDR
SIO | J49
Enable | 1-2 (Default)
Disable | 2-3
U30
PC87393
Bus Interface
Clock
IR
FDC
Parallel Port
Serial Port
PWR & GND
Straps
GPIOs
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
SERIRQ
SMI#
LPCPD#
CLKRUN#
CLKIN
IRRX1
IRRX2_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL
DRATE0
DR1#
MTR1#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
XCNF1/XWR#
XCNF2
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO26
GPIO27
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
NC
PPT_PNF# 32
+V3.3S_SIO
RP74A 10K
+V5S 4,9,17,19,20,24,32,33,35,36,37,40
Q19
BAR43
+V5S_DIODE
PPT_SLIN#/ASTRB# 32
PPT_INIT# 32
PPT_ERR# 32
PPT_AFD#/DSTRB# 32
PPT_STB#/WRITE# 32
PPT_SLCT 32
PPT_PE 32
PPT_BUSY/WAIT# 32
PPT_ACK# 32
PPT_PD7 32
PPT_PD6 32
PPT_PD5 32
PPT_PD4 32
PPT_PD3 32
PPT_PD2 32
PPT_PD1 32
PPT_PD0 32
SER_DCDA# 20,32
SER_DSRA# 20,32
SER_SINA 20,32
SER_RTSA# 20,32
SER_SOUTA 20,32
SER_CTSA# 20,32
SER_DTRA# 20,32
SER_RIA# 20,32
4,5,6,9,10,14,17,19,23,28,29,30,32,33,36,37,40 +V3.3S
+V3.3S_SIO
R182
NO_STUFF_0.01_1%
C514 0.1UF
C508 0.1UF
C282 22UF
Title
Super I/O Controller
Project:
845MP/MZ Platform
Sheet 31 of 42

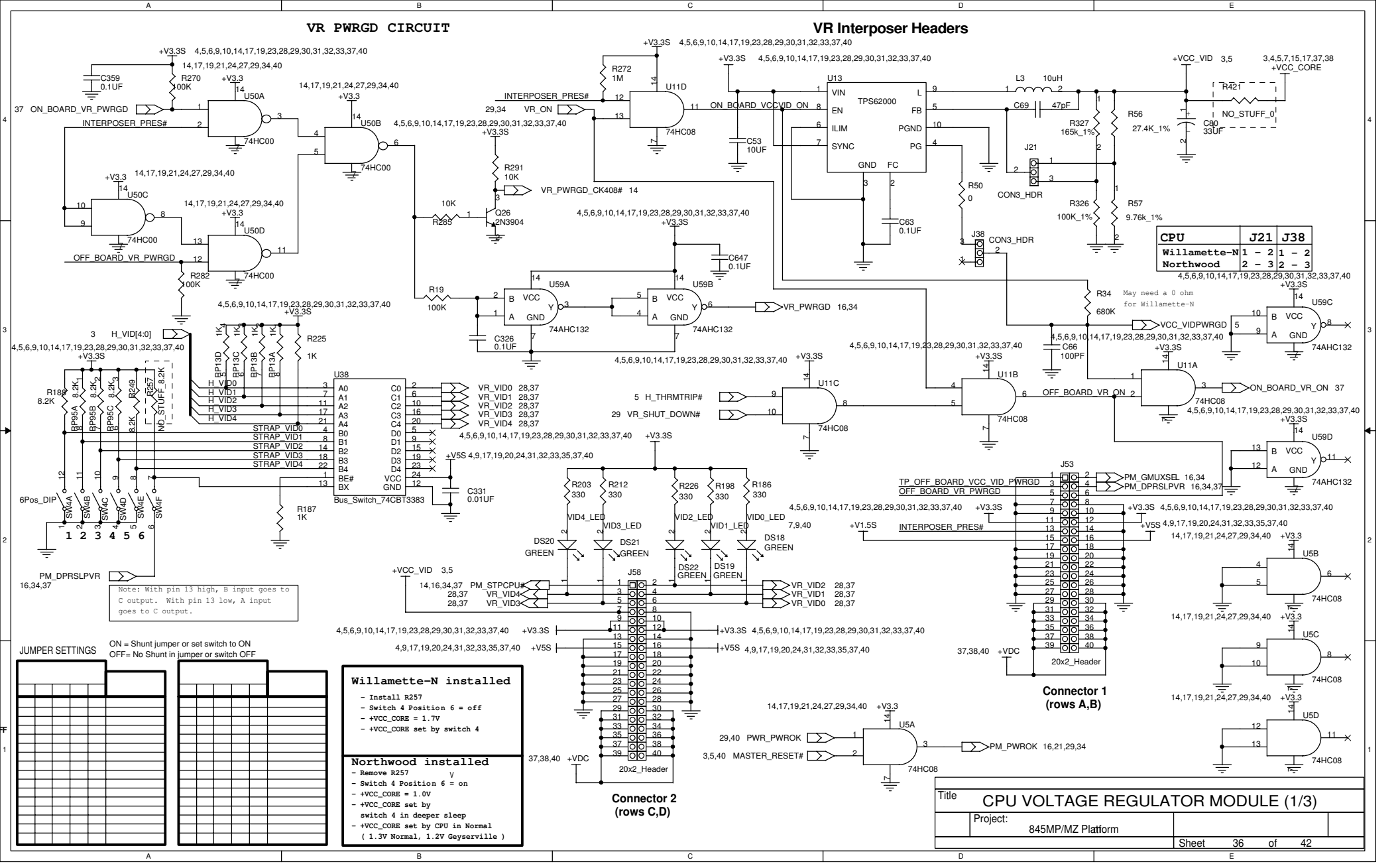

FLOPPY CONNECTOR
4,9,17,19,20,24,31,33,35,36,37,40 +V5S
RP104A 1K
RP104C 1K
RP102B 1K
RP102A 1K
RP102C 1K
J72
17x2_HDR
FLP_DENSEL# 31
FLP_DRATE0 31
FLP_INDEX# 31
FLP_MTR0# 31
FLP_DR0# 31
FLP_DIR# 31
FLP_STEP# 31
FLP_WDATA# 31
FLP_WGATE# 31
FLP_TRK0# 31
FLP_WP# 31
FLP_RDATA# 31
FLP_HDSEL# 31
FLP_DSKCHG# 31
PARALLEL PORT
60OHM@100MHZ
31 PPT_PNF#
31 PPT_SLCT
FB6A PPT_L_PNF#
FB6B PPT_L_SLCT
31 PPT_PE
31 PPT_BUSY/WAIT#
31 PPT_ACK#
31 PPT_PD7
FB6C PPT_L_PE
FB6D PPT_L_BUSY/WAIT#
FB11A PPT_L_ACK#
FB11B PPT_L_PD7
31 PPT_PD6
31 PPT_PD5
31 PPT_PD4
31 PPT_PD3
FB11C PPT_L_PD6
FB11D PPT_L_PD5
FB5A PPT_L_PD4
FB5B PPT_L_PD3
31 PPT_SLIN#/ASTRB#
31 PPT_PD2
31 PPT_INIT#
31 PPT_PD1
FB5C PPT_L_SLIN#
FB5D PPT_L_PD2
FB10A PPT_L_INIT#
FB10B PPT_L_PD1
31 PPT_ERR#
31 PPT_PD0
31 PPT_AFD#/DSTRB#
31 PPT_STB#/WRITE#
FB10C PPT_L_ERR#
FB10D PPT_L_PD0
FB9A PPT_L_AFD#/DSTRB#
FB9B PPT_L_STB#/WRITE#
J4
PARALLEL
INFRARED PORT
4,5,6,9,10,14,17,19,23,28,29,30,31,33,36,37,40
+V3.3S
+V3.3S_IR
R9 2.2
U1
HSDL-3600#017
31 IR_TXD
31 IR_RXD
31 IR_MD1
31 IR_MD0
31 IR_SEL
LEDA
TXD
RXD
GND
NC
MOD1
MOD0
FIR_SEL
AGND
VDD
MNT
C7 0.1UF
C10 10UF
Caps must be placed as close as possible to pins 1,2
+V3.3ALWAYS 9,16,17,18,19,24,25,26,29,33,34,39,40
C5 22UF
C2 0.1UF
U3
MAX3243
VCC
GND
C1+
C1-
C2+
C2-
V+
V-
R1IN
R2IN
R3IN
R4IN
R5IN
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
T1IN
T2IN
T3IN
T1OUT
T2OUT
T3OUT
FORCEON
FORCEOFF#
INVALID#
SERBUF_C1+
SERBUF_C1-
SERBUF_C2+
SERBUF_C2-
SERBUF_V+
SERBUF_V-
C21 0.1UF
C22 0.1UF
C26 0.1UF
C24 0.1UF
PM_RI#
16,21,22,34
Q24
BSS138
SER_RIA
20,31 SER_CTSA#
20,31 SER_RIA#
20,31 SER_SINA
20,31 SER_DSRA#
20,31 SER_DCDA#
20,31 SER_DTRA#
20,31 SER_SOUTA
20,31 SER_RTSA#
SERBUF_CTSA
SERBUF_RIA
SERBUF_SINA#
SERBUF_DSRA
SERBUF_DCDA
SERBUF_DTRA
SERBUF_SOUTA#
SERBUF_RTSA
4,5,6,9,10,14,17,19,23,28,29,30,31,33,36,37,40
+V3.3S
R5 1K SER_ON
16 SER_EN
R423 1K
Note: FORCEOFF# overrides FORCEON.
SERIAL PORT
60OHM@100MHZ
FB9C SERPRT_DCDA
FB9D SERPRT_DSRA
FB7C SERPRT_SINA#
FB7A SERPRT_RTSA
FB7B SERPRT_SOUTA#
FB7D SERPRT_CTSA
FB8A SERPRT_DTRA
FB8B SERPRT_RIA
J1
SERIAL
R2OUTB is enabled even in suspend.
SER_RIA# is routed to allow the system to wake up in Suspend To RAM.
Title
Floppy, Parallel, Serial, and IR Ports
Project:
845MP/MZ Platform
Sheet 32 of 42


KBC_SCANOUT[15:0] 29
J30
KBC_SCANOUT0
KBC_SCANOUT1
KBC_SCANOUT2
KBC_SCANOUT3
KBC_SCANOUT4
KBC_SCANOUT5
KBC_SCANOUT6
KBC_SCANOUT7
KBC_SCANOUT8
KBC_SCANOUT9
KBC_SCANOUT10
KBC_SCANOUT11
KBC_SCANOUT12
KBC_SCANOUT13
KBC_SCANOUT14
KBC_SCANOUT15
KBC_SCANIN0
KBC_SCANIN1
KBC_SCANIN2
KBC_SCANIN3
KBC_SCANIN4
KBC_SCANIN5
KBC_SCANIN6
KBC_SCANIN7
NO_STUFF_24Pin_ZIF-HDR
Scan Matrix Key Board
KBC_SCANIN[7:0] 29
+V5S 4,9,17,19,20,24,31,32,35,36,37,40
CBTD has integrated diode for 5V to 3.3V voltage translation
C36 0.1UF
U9
29 KBC_GP_DATA
29 KBC_GP_CLK
29 KBC_MOUSE_DATA
29 KBC_MOUSE_CLK
29 KBC_KB_DATA
29 KBC_KB_CLK
15 H_A20GATE
1A1
1A2
1A3
1A4
1A5
2A1
2A2
2A3
2A4
2A5
1OE#
2OE#
VCC
GND
1B1
1B2
1B3
1B4
1B5
2B1
2B2
2B3
2B4
2B5
Bus-Switch-74CBT3384
GP_DATA
GP_CLK
MOUSE_DATA
MOUSE_CLK
KBD_DATA
KBD_CLK
MOUSE_DATA 20
MOUSE_CLK 20
KBD_DATA 20
KBD_CLK 20
KBC_A20GATE 29,34
R26 100
4,5,6,9,10,14,17,19,23,28,29,30,31,32,36,37,40
+V3.3S
RP75C 8.2K
RP4A 4.7K
GP_CLK
FB8C 60OHM@100MHZ
CP1C 47PF
RT1 1.1A
FB4 31Ohm@100MHz
L_GPDATA
FB3 60ohm@100MHz
RP3B 4.7K
C30 47pF
C54 22UF
C52 0.1UF
RP3D 4.7K
KBD_CLK
FB2 60ohm@100MHz
CP1A 47PF
L_GPCLK
J7
DUAL_PS2
RP3C 4.7K
FB1 60ohm@100MHz
C29 47pF
+V3.3ALWAYS 9,16,17,18,19,24,25,26,29,32,34,39,40
RP74D 10K
RP98A 10K
RP98B 10K
RP98D 10K
RP99A 10K
RP88B 10K
RP88C 10K
R422 10K
SMC_EXTSMI# 16,29,31,34
SMC_RUNTIME_SCI# 16,29,34
SMC_WAKE_SCI# 16,29,34
PM_BATLOW# 16,29,34
SMB_SB_DATA 29,34,40
SMB_SB_CLK 29,34,40
SMB_SB_ALRT# 29,34,40
DOCK_INTR# 20,29,34
RP3A 4.7K
MOUSE_CLK
FB13 60ohm@100MHz
CP1B 47PF
RP4C 4.7K
FB14 60ohm@100MHz
CP1D 47PF
If a PS/2 "breakout" connector is used,the keyboard PS/2 connector can be used for both a PS/2 keyboard and a second PS/2 mouse. Otherwise, the keyboard PS/2 connector will only support a PS/2 keyboard.
Title
Keyboard and Mouse Connectors
Project:
845MP/MZ Platform
Sheet 33 of 42


LPC POWERED ON SUSPEND RAIL FOR ADD-IN H8 CARD
LPC Debug Slot
60Pin_CardCon
SMBus Debug Header
CON4_HDR
6Pin_HDR
2X8_HDR
ICH3-M Testpoint Header
2X5-Header
15x2_HDR
SMC Sidebands for LPC Power Management
8Pin HDR
SIO Sidebands
TEST HEADER
NO STUFF
GROUND HEADERS
LPC Slot & Debug Headers
Project:
845MP/MZ Platform
Sheet 34 of 42

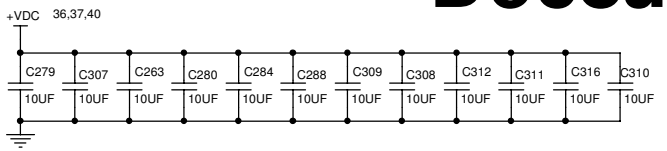


Title	System Management and Keyboard Controller IC
Project:	845MP/MZ Platform
Sheet	35 of 42


VR PWRGD CIRCUIT
VR Interposer Headers
U50A
U50B
U50C
U50D
74HC00
U11D
74HC08
U13
TPS62000
U59A
U59B
74AHC132
U59C
U59D
U11A
U11B
U11C
U38
Bus_Switch_74CBT3383
U5A
U5B
U5C
U5D
J21
CON3_HDR
J38
J53
J58
20x2_Header
Connector 1
(rows A,B)
Connector 2
(rows C,D)
Q26
2N3904
DS20
DS21
DS22
DS18
DS19
GREEN
SW4A
SW4B
SW4C
SW4D
SW4E
SW4F
6Pos_DIP
JUMPER SETTINGS
ON = Shunt jumper or set switch to ON
OFF= No Shunt in jumper or switch OFF
Willamette-N installed
- Install R257
- Switch 4 Position 6 = off
- +VCC_CORE = 1.7V
- +VCC_CORE set by switch 4
Northwood installed
- Remove R257
- Switch 4 Position 6 = on
- +VCC_CORE = 1.0V
- +VCC_CORE set by
switch 4 in deeper sleep
- +VCC_CORE set by CPU in Normal
(1.3V Normal, 1.2V Geyserville)
CPU | J21 | J38
Willamette-N | 1 - 2 | 1 - 2
Northwood | 2 - 3 | 2 - 3
Note: With pin 13 high, B input goes to C output. With pin 13 low, A input goes to C output.
May need a 0 ohm for Willamette-N
Title
CPU VOLTAGE REGULATOR MODULE (1/3)
Project:
845MP/MZ Platform
Sheet 36 of 42

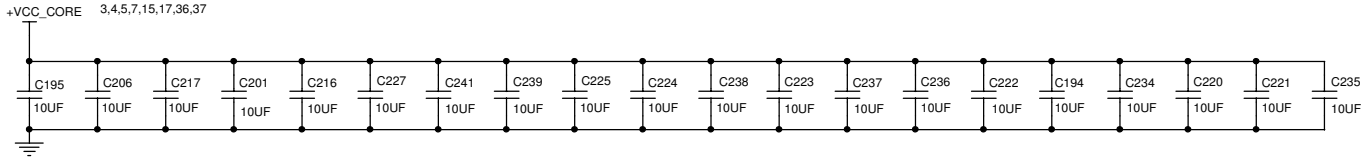
Decoupling

VR Input Decoupling

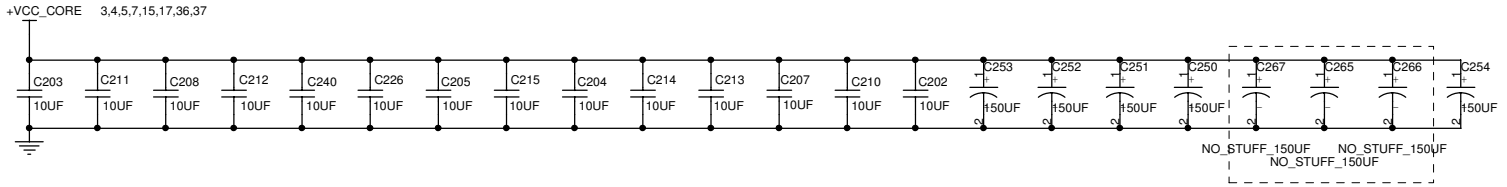


Bulk decoupling values are tuned to Intels IMVP II 5Phase VR design. Circuits using other converter topologies may have different requirements.

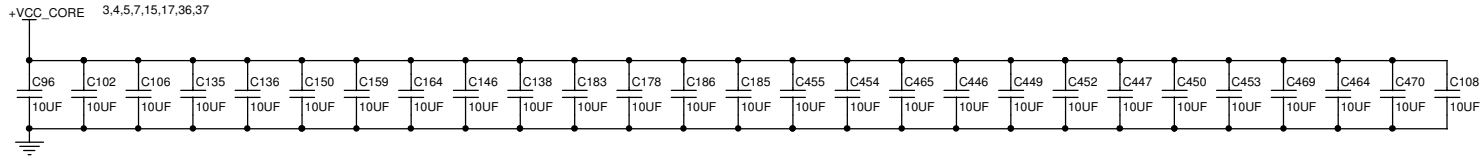
V_CORE Bulk Decoupling



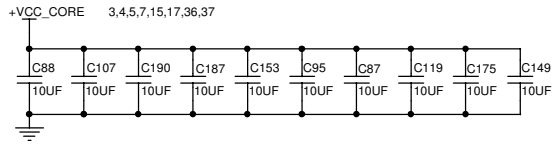
V_CORE Bulk Decoupling (Optional)

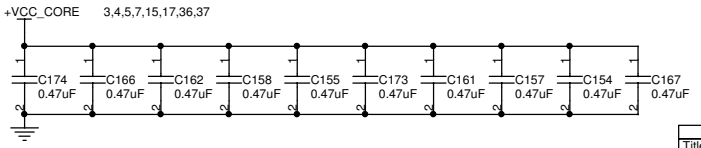


High Frequency Decoupling (Place underneath Processor)

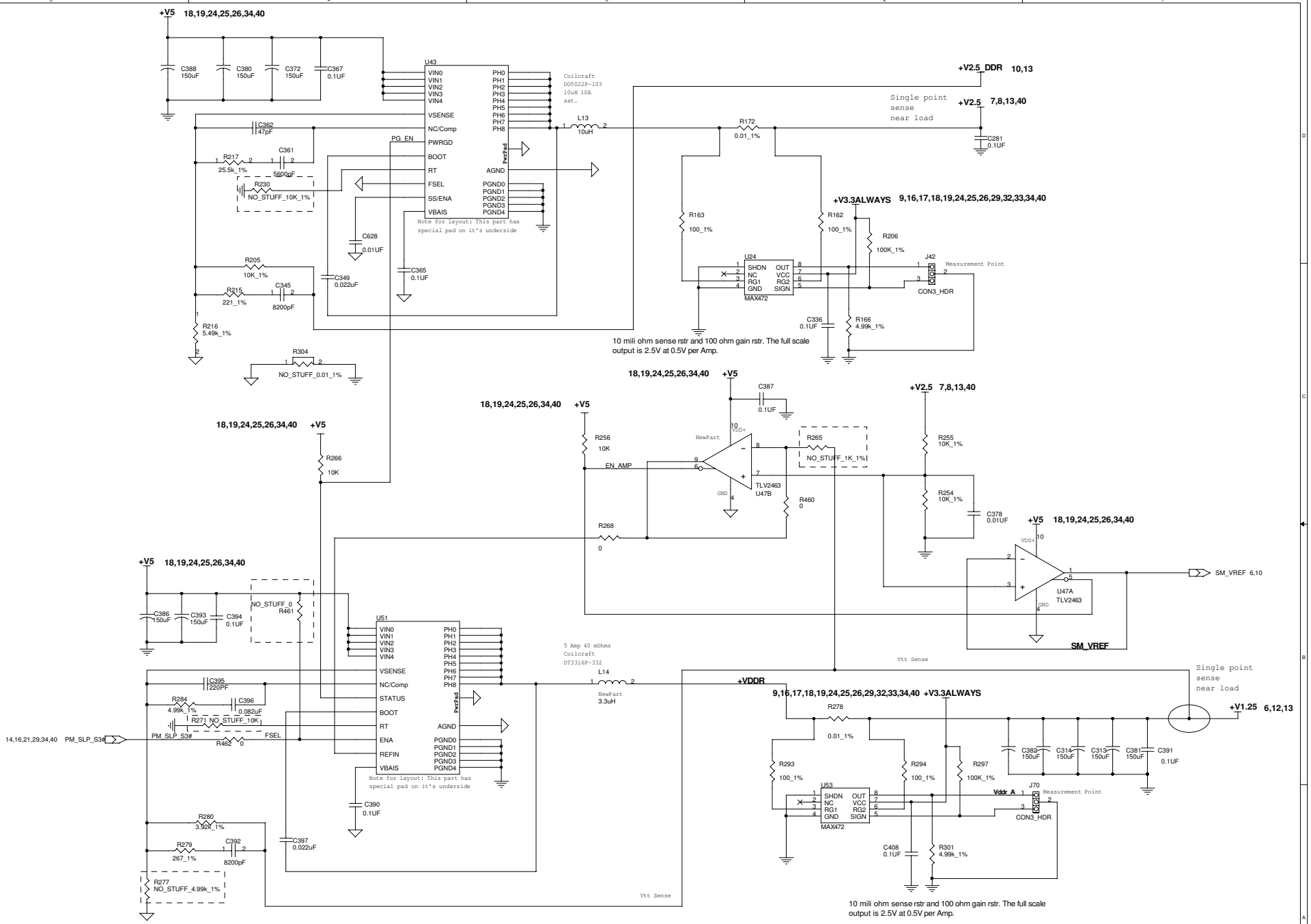


Mid Frequency Decoupling (Place around Processor)





Title	Decoupling
Project:	845MP/MZ Platform
Sheet	38 of 42



DDR VR

Title	DDR_VR
Project:	845MP/MZ Platform
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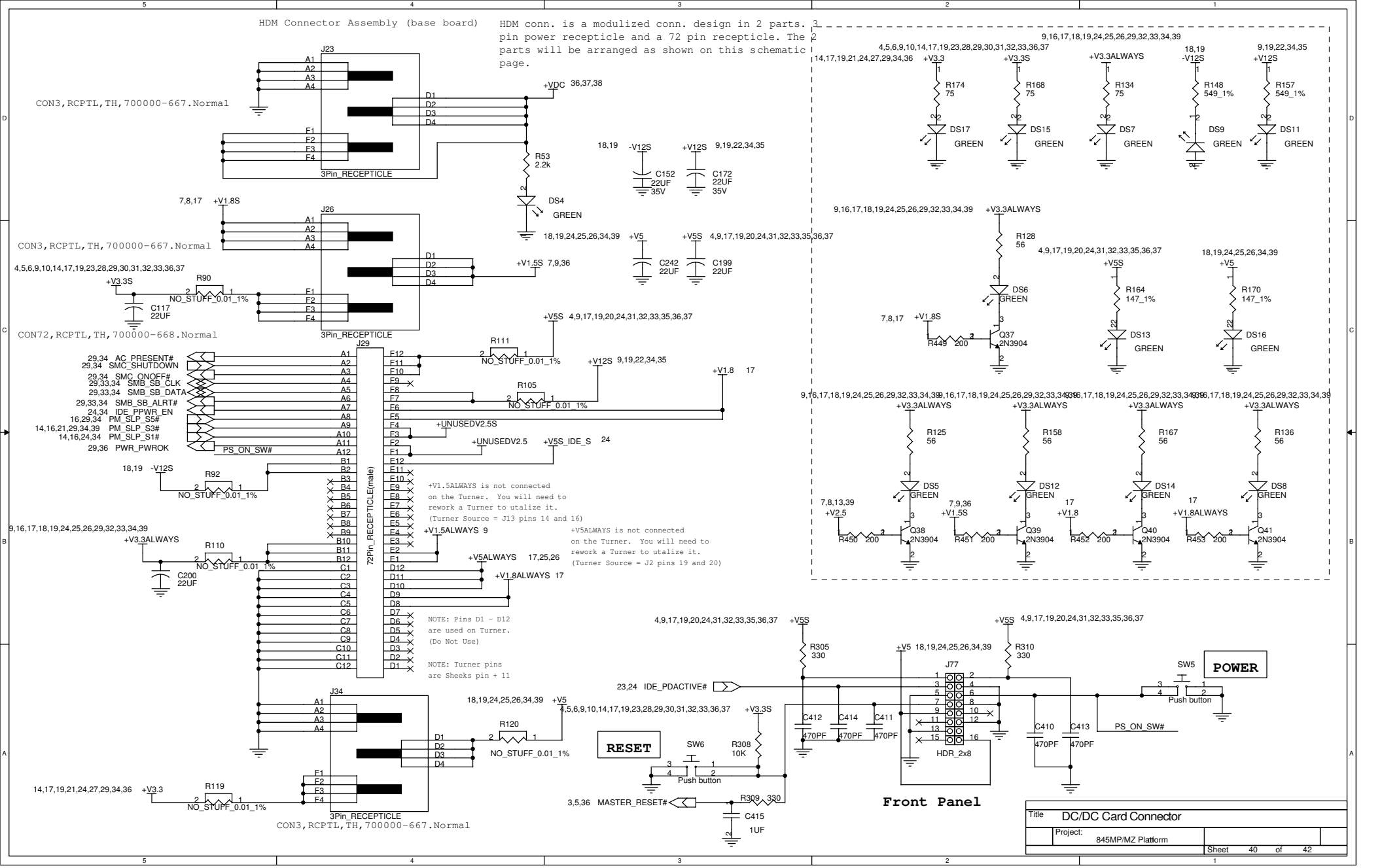
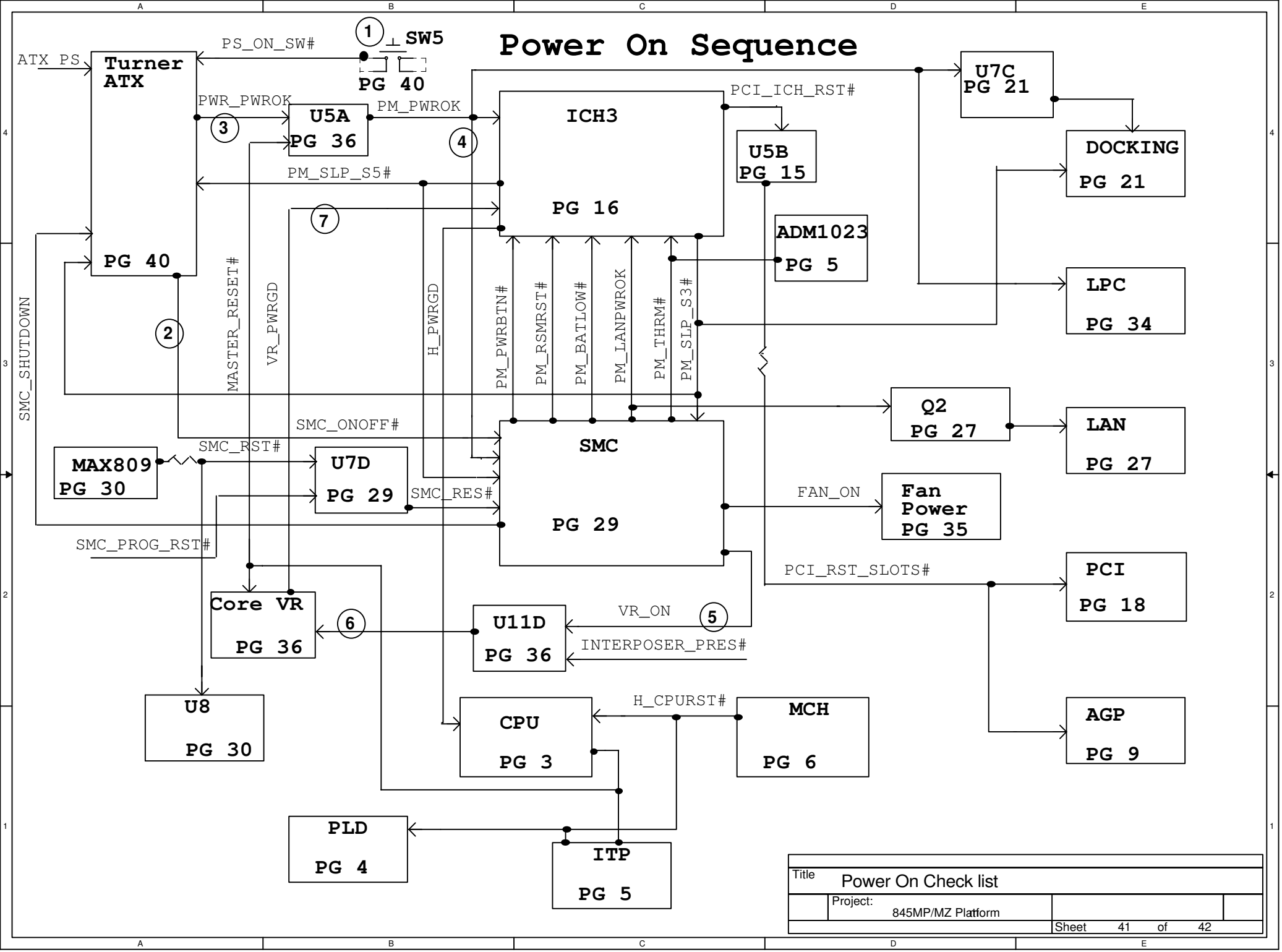
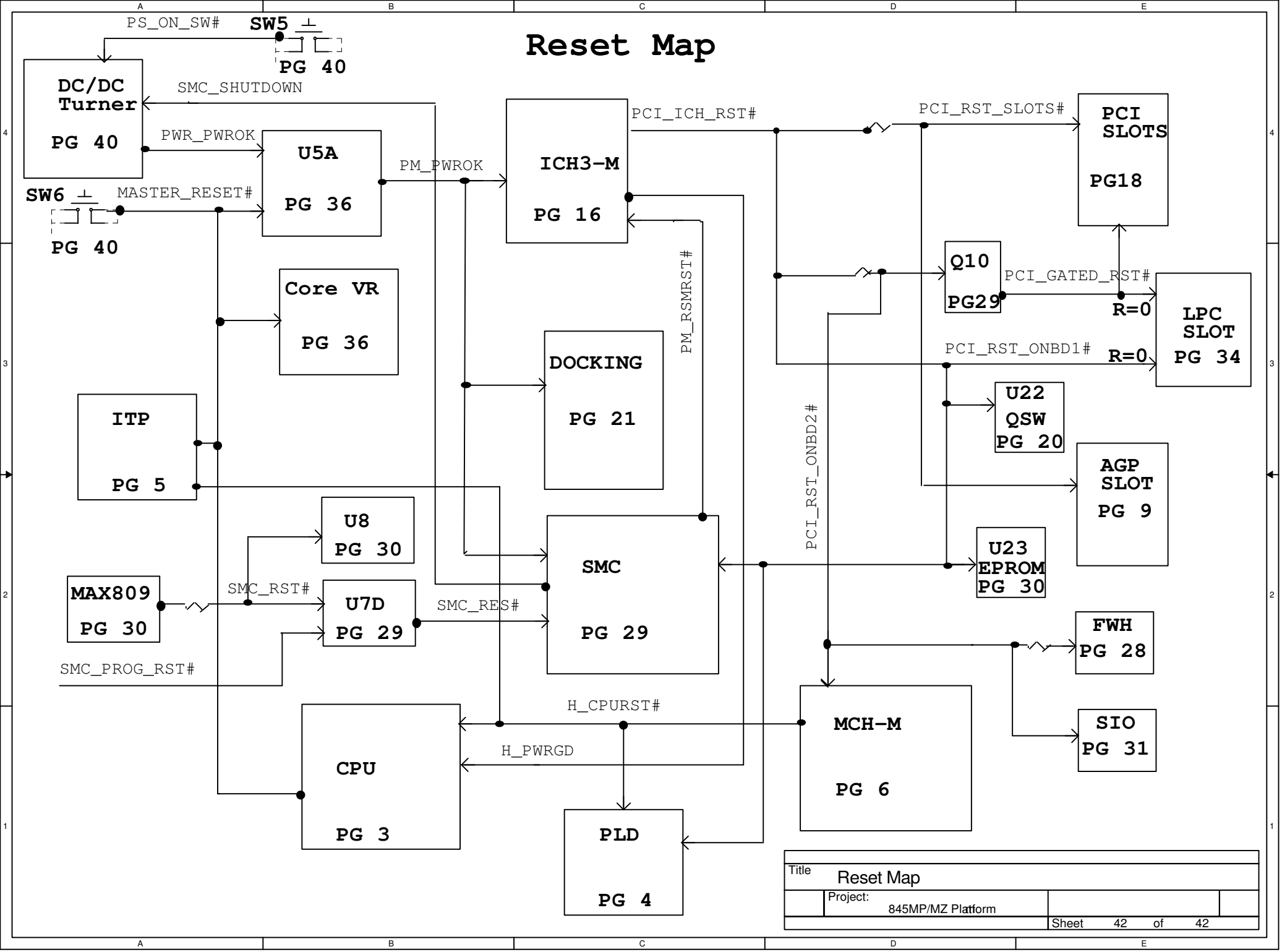

HDM Connector Assembly (base board)
HDM conn. is a modulized conn. design in 2 parts. 3 pin power recepticle and a 72 pin recepticle. The parts will be arranged as shown on this schematic page.
CON3,RCPTL,TH,700000-667.Normal
CON72,RCPTL,TH,700000-668.Normal
3Pin_RECEPTICLE
72Pin_RECEPTICLE(male)
+VDC 36,37,38
+V1.8S 7,8,17
+V1.5S 7,9,36
+V5S 4,9,17,19,20,24,31,32,33,35,36,37
+V5 18,19,24,25,26,34,39
+V3.3S 4,5,6,9,10,14,17,19,23,28,29,30,31,32,33,36,37
+V3.3ALWAYS 9,16,17,18,19,24,25,26,29,32,33,34,39
-V12S 18,19
+V12S 9,19,22,34,35
+V1.8 17
+V1.8ALWAYS 17
+V1.5ALWAYS 9
+V5ALWAYS 17,25,26
+UNUSEDV2.5S
+UNUSEDV2.5
+V5S_IDE_S 24
PS_ON_SW#
+V1.5ALWAYS is not connected on the Turner. You will need to rework a Turner to utalize it. (Turner Source = J13 pins 14 and 16)
+V5ALWAYS is not connected on the Turner. You will need to rework a Turner to utalize it. (Turner Source = J2 pins 19 and 20)
NOTE: Pins D1 - D12 are used on Turner. (Do Not Use)
NOTE: Turner pins are Sheeks pin + 11
RESET
POWER
Push button
Front Panel
HDR_2x8
DS17 GREEN
DS15 GREEN
DS7 GREEN
DS9 GREEN
DS11 GREEN
DS6 GREEN
DS13 GREEN
DS16 GREEN
DS5 GREEN
DS12 GREEN
DS14 GREEN
DS8 GREEN
Q37 2N3904
Q38 2N3904
Q39 2N3904
Q40 2N3904
Q41 2N3904
Title DC/DC Card Connector
Project: 845MP/MZ Platform
Sheet 40 of 42


Power On Sequence
ATX PS
Turner ATX
PG 40
PS_ON_SW#
SW5
PG 40
PWR_PWROK
U5A
PG 36
PM_PWROK
ICH3
PG 16
PCI_ICH_RST#
U5B
PG 15
U7C
PG 21
DOCKING
PG 21
PM_SLP_S5#
ADM1023
PG 5
LPC
PG 34
SMC_SHUTDOWN
MASTER_RESET#
VR_PWRGD
H_PWRGD
PM_PWRBTN#
PM_RSMRST#
PM_BATLOW#
PM_LANPWROK
PM_THRM#
PM_SLP_S3#
Q2
PG 27
LAN
PG 27
SMC_ONOFF#
SMC_RST#
MAX809
PG 30
U7D
PG 29
SMC_RES#
SMC
PG 29
FAN_ON
Fan Power
PG 35
SMC_PROG_RST#
PCI_RST_SLOTS#
PCI
PG 18
Core VR
PG 36
U11D
PG 36
VR_ON
INTERPOSER_PRES#
U8
PG 30
H_CPURST#
CPU
PG 3
MCH
PG 6
AGP
PG 9
PLD
PG 4
ITP
PG 5
Title
Power On Check list
Project:
845MP/MZ Platform
Sheet 41 of 42


Reset Map
PS_ON_SW#
SW5
PG 40
DC/DC Turner
PG 40
SMC_SHUTDOWN
PWR_PWROK
U5A
PG 36
PM_PWROK
ICH3-M
PG 16
PCI_ICH_RST#
PCI_RST_SLOTS#
PCI SLOTS
PG18
SW6
MASTER_RESET#
PG 40
Core VR
PG 36
PM_RSMRST#
Q10
PG29
PCI_GATED_RST#
R=0
LPC SLOT
PG 34
PCI_RST_ONBD1#
R=0
DOCKING
PG 21
ITP
PG 5
U22
QSW
PG 20
AGP SLOT
PG 9
PCI_RST_ONBD2#
U8
PG 30
SMC
PG 29
U23
EPROM
PG 30
MAX809
PG 30
SMC_RST#
U7D
PG 29
SMC_RES#
FWH
PG 28
SMC_PROG_RST#
H_CPURST#
MCH-M
PG 6
SIO
PG 31
H_PWRGD
CPU
PG 3
PLD
PG 4
Title
Reset Map
Project:
845MP/MZ Platform
Sheet 42 of 42