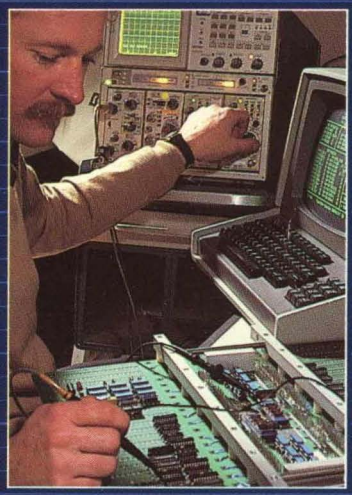
INTERSIL Application Handbook

Excellence in Signal Processing and Control Integrated Circuits



GE Semiconductor

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Application Handbook
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DATA ACQUISITION SYSTEMS

Introduction

Data acquisition and conversion systems interface between the real world of physical parameters, which are analog, and the artificial world of digital computation and control. With current emphasis on digital systems, the interfacing function has become an important one; digital systems are used widely because complex circuits are low cost, accurate, and relatively simple to implement. In addition, there is rapid growth in use of minicomputers and microcomputers to perform difficult digital control and measurement functions.

Computerized feedback control systems are used in many different industries today in order to achieve greater productivity in our modern industrial society. Industries which presently employ such automatic systems include steel making, food processing, paper production, oil refining, chemical manufacturing, textile production, and cement manufacturing.

The devices which perform the interfacing function between analog and digital worlds are analog-to-digital (A/D) and digital-to-analog (D/A) converters, which together are known as data converters. Some of the specific applications in which data converters are used include data telemetry systems, pulse code modulated communications, automatic test systems, computer display systems, video signal processing systems, data logging systems, and sampled-data control systems. In addition, every laboratory digital multimeter or digital panel meter contains an A/D converter.

Besides A/D and D/A converters, data acquisition and distribution systems may employ one or more of the following circuit functions:

Basic Data Distribution Systems

Transducers
Amplifiers
Filters
Nonlinear Analog Functions
Analog Multiplexers
Sample-Holds

The interconnection of these components is shown in the diagram of the data acquisition portion of a computerized feedback control system in Figure 1.

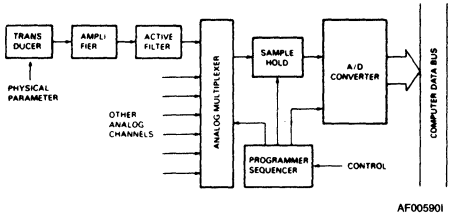


Figure 1: Data Acquisition System

The input to the system is a *physical parameter* such as temperature, pressure, flow, acceleration, and position, which are analog quantities. The parameter is first converted into an electrical signal by means of a *transducer*; once in electrical form, all further processing is done by electronic circuits.

Next, an *amplifier* boosts the amplitude of the transducer output signal to a useful level for further processing. Transducer outputs may be microvolt or millivolt level signals which are then amplified to 1 to 10 volt levels. Furthermore, the transducer output may be a high impedance signal, a differential signal with common-mode noise, a current output, a signal superimposed on a high voltage, or a combination of these. The amplifier, in order to convert such signals into a high level voltage, may be one of several specialized types.

The amplifier is frequently followed by a low pass *active filter* which reduces high frequency signal components, unwanted electrical interference noise, or electronic noise from the signal. The amplifier is sometimes also followed by a special *nonlinear analog function* circuit which performs a nonlinear operation on the high level signal. Such operations include squaring, multiplication, division, RMS conversion, log conversion, or linearization.

The processed analog signal next goes to an *analog multiplexer* which sequentially switches between a number of different analog input channels. Each input is in turn connected to the output of the multiplexer for a specified period of time by the multiplexer switch. During this connection time a *sample-hold* circuit acquires the signal voltage and then holds its value while an *analog-to-digital converter* converts the value into digital form. The resultant digital word goes to a computer data bus or to the input of a digital circuit.

Thus the analog multiplexer, together with the sample-hold, time shares the A/D converter with a number of analog input channels. The timing and control of the complete data acquisition system is done by a digital circuit called a *programmer-sequencer,* which in turn is under control of the computer. In some cases the computer itself may control the entire data acquisition system.

While this is perhaps the most commonly used data acquisition system configuration, there are alternative ones. Instead of multiplexing high-level signals, low-level multiplexing is sometimes used with the amplifier following the multiplexer. In such cases just one amplifier is required, but its gain may have to be changed from one channel to the next during multiplexing. Another method is to amplify and convert the signal into digital form at the transducer location and send the digital information in serial form to the computer. Here the digital data must be converted to parallel form and then multiplexed onto the computer data bus.

Basic Data Acquisition System

The data distribution portion of a feedback control system, illustrated in Figure 2, is the reverse of the data acquisition system. The computer, based on the inputs of the data acquisition system, must close the loop on a

process and control it by means of output control functions. These control outputs are in digital form and must therefore be converted into analog form in order to drive the process. The conversion is accomplished by a series of *digital-to-analog converters* as shown. Each D/A converter is coupled to the computer data bus by means of a register which stores the digital word until the next update. The registers are activated sequentially by a *decoder and control circuit* which is under computer control.

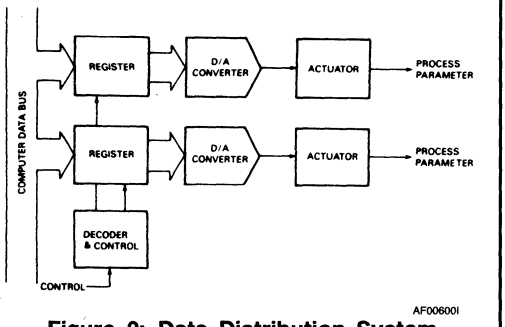


Figure 2: Data Distribution System

The D/A converter outputs then drive *actuators* which directly control the various process parameters such as temperature, pressure, and flow. Thus the loop is closed on the process and the result is a complete automatic process control system under computer control.

QUANTIZING THEORY

Introduction

Analog-to-digital conversion in its basic conceptual form is a two-step process: quantizing and coding. Quantizing is the process of transforming a continuous analog signal into a set of discrete output states. Coding is the process of assigning a digital code word to each of the ouput states. Some of the early A/D converters were appropriately called quantizing encoders.

Quantizer Transfer Function

The nonlinear transfer function shown in Figure 3 is that of an ideal quantizer with 8 output states; with output code words assigned, it is also that of a 3-bit A/D converter. The 8 output states are assigned the sequence of binary numbers from 000 through 111. The analog input range for this quantizer is 0 to +10V.

There are several important points concerning the transfer function of Figure 3. First, the *resolution* of the quantizer is defined as the number of output states expressed in bits; in this case it is a 3-bit quantizer. The number of output states for a binary coded quantizer is 2^n, where n is the number of bits. Thus, an 8-bit quantizer has 256 output states and a 12-bit quantizer has 4096 output states.

As shown in the diagram, there are $2^n - 1$ analog decision points (or threshold levels) in the transfer function. These points are at voltages of +0.625, +1.875, +3.125, +4.375, +5.625, +6.875, and +8.125. The decision points must be precisely set in a quantizer in order to divide the analog voltage range into the correct quantized values.

The voltages +1.25, +2.50, +3.75, +5.00, +6.25, +7.50, and +8.75 are the center points of each output code word. The analog decision point voltages are precisely halfway between the code word center points. The quantizer staircase function is the best approximation which can be made to a straight line drawn through the origin and full scale point; notice that the line passes through all of the code word center points.

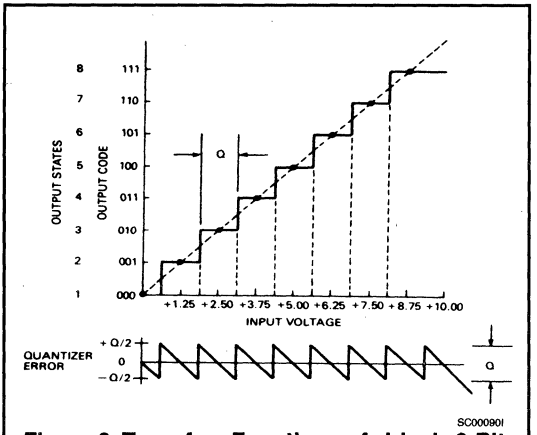


Figure 3: Transfer Function of Ideal 3-Bit Quantizer

Quantizer Resolution and Error

At any part of the input range of the quantizer, there is a small range of analog values within which the same output code word is produced. This small range is the voltage difference between any two adjacent decision points and is known as the analog quantization size, or *quantum,* Q. In Figure 3, the quantum is 1.25V and is found in general by dividing the full scale analog range by the number of ouput states. Thus

$$Q = \frac{FSR}{2^n}$$

where FSR is the full scale range, or 10V in this case. Q is the smallest analog difference which can be resolved, or distinguished, by the quantizer. In the case of a 12-bit quantizer, the quantum is much smaller and is found to be

$$Q = \frac{FSR}{2^n} = \frac{10V}{4096} = 2.44mV$$

If the quantizer input is moved through its entire range of analog values and the difference between ouput and input is taken, a sawtooth error function results, as shown in Figure 3. This function is called the quantizing error and is the irreducible error which results from the quantizing process. It can be reduced only by increasing the number of output states (or the resolution) of the quantizer, thereby making the quantization finer.

For a given analog input value to the quantizer, the output error will vary anywhere from 0 to ±Q/2; the error is zero only at analog values corresponding to the code center points. This error is also frequently called *quantization uncertainty* or *quantization noise.*

The quantizer output can be thought of as the analog input with quantization noise added to it. The noise has a peak-to-peak value of Q but, as with other types of noise, the average value is zero. Its RMS value, however, is useful in analysis and can be computed from the triangular waveshape to be $Q/2\sqrt{3}$.

SAMPLING THEORY

Introduction

An analog-to-digital converter requires a small, but significant, amount of time to perform the quantizing and coding operations. The time required to make the conversion depends on several factors: the converter resolution, the conversion technique, and the speed of the components employed in the converter. The conversion speed required for a particular application depends on the time variation of the signal to be converted and on the accuracy desired.

Aperture Time

Conversion time is frequently referred to as *aperture time.* In general, aperture time refers to the time uncertainty (or time window) in making a measurement and results in an amplitude uncertainty (or error) in the measurement if the signal is changing during this time.

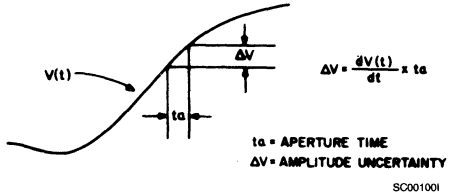


Figure 4: Aperture Time and Amplitude Uncertainty

As shown in Figure 4, the input signal to the A/D converter changes by ΔV during the aperture time t_a in which the conversion is performed. The error can be considered an amplitude error or a time error; the two are related as follows

$$\Delta V = t_a \frac{dV(t)}{dt}$$

where dV(t)/dt is the rate of change with time of the input signal.

It should be noted that ΔV represents the maximum error due to signal change, since the actual error depends on how the conversion is done. At some point in time within t_a, the signal amplitude corresponds exactly with the ouput code word produced.

For the specific case of a sinusoidal input signal, the maximum rate of change occurs at the zero crossing of the waveform, and the amplitude error is

$$\Delta V = t_a \frac{d}{dt} (A \sin \omega t)_{t=0} = t_a A \omega$$

The resultant error as a fraction of the peak to peak full scale value is

$$\epsilon = \frac{\Delta V}{2A} = \pi f t_a$$

From this result the aperture time required to digitize a 1 kilohertz signal to 10 bits resolution can be found. The resolution required is one part in 2^{10} or 0.001.

$$t_a = \frac{\epsilon}{\pi f} = \frac{0.001}{3.14 \times 10^3} = 320 \times 10^{-9}$$

The result is a required aperture time of just 320 nanoseconds!

One should appreciate the fact that 1kHz is not a particularly fast signal, yet it is difficult to find a 10 bit A/D converter to perform this conversion at any price! Fortunately, there is a relatively simple and inexpensive way around this dilemma by using a sample-hold circuit.

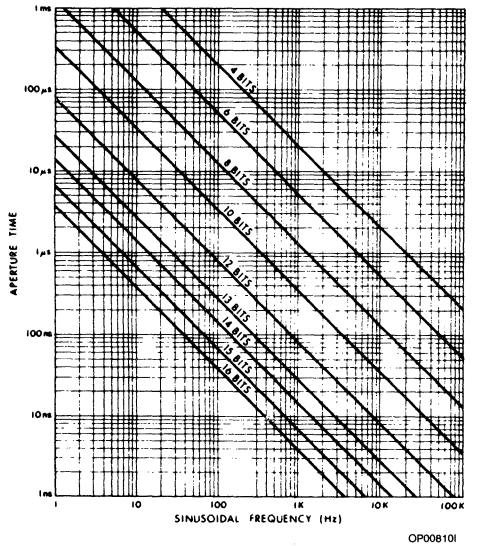


Figure 5: Graph for Aperture Error for Sinusoidal Signals

Sample-Holds and Aperture Error

A sample-hold circuit samples the signal voltage and then stores it on a capacitor for the time required to perform the A/D conversion. The aperture time of the A/D converter is therefore greatly reduced by the much shorter aperture time of the sample-hold circuit. In turn, the aperture time of the sample-hold is a function of its bandwidth and switching time.

Figure 5 is a useful graph of Equation 5. It gives the aperture time required for converting sinusoidal signals to a maximum error less than one part in 2^n where n is the resolution of the converter in bits. The peak to peak value of the sinusoid is assumed to be the full scale range of the A/D converter. The graph is most useful in selecting a sample-hold by aperture time or an A/D converter by conversion time.

Sampled-Data Systems and the Sampling Theorem

In data acquisition and distribution systems, and other sampled-data systems, analog signals are sampled on a

periodic basis as illustrated in Figure 6. The train of sampling pulses in 6(b) represents a fast-acting switch which connects to the analog signal for a very short time and then disconnects for the remainder of the sampling period.

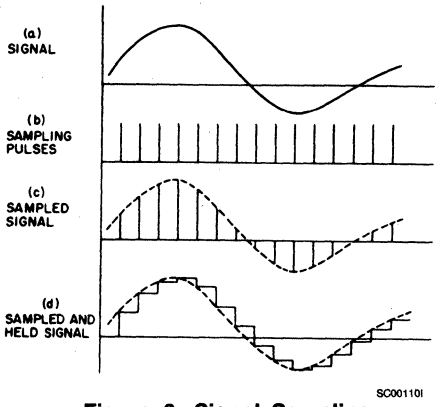


Figure 6: Signal Sampling

The result of the fast-acting sampler is identical with multiplying the analog signal by a train of sampling pulses of unity amplitude, giving the modulated pulse train of Figure 6(c). The amplitude of the original signal is perserved in the modulation envelope of the pulses. If the switch type sampler is replaced by a switch and capacitor (a sample-hold circuit), then the amplitude of each sample is stored between samples and a reasonable reconstruction of the original analog signal results, as shown in 6(d).

The purpose of sampling is the efficient use of data processing equipment and data transmission facilities. A single data transmission link, for example, can be used to transmit many different analog channels on a sampled basis, whereas it would be uneconomical to devote a complete transmission link to the continuous transmission of a single signal.

Likewise, a data acquisition and distribution system is used to measure and control the many parameters of a process control system by sampling the parameters and updating the control inputs periodically. In data conversion systems it is common to use a single, expensive A/D converter of high speed and precision and then multiplex a number of analog inputs into it.

An important fundamental question to answer about sample-data systems is this: "How often must I sample an analog signal in order not to lose information from it?" It is obvious that all useful information can be extracted if a slowly varying signal is sampled at a rate such that little or no change takes place between samples. Equally obvious is the fact that information is being lost if there is a significant change in signal amplitude between samples.

The answer to the question is contained in the well-known Sampling Theorem which may be stated as follows: *If a continuous, bandwidth-limited signal contains no frequency components higher than fc, then the original signal can be recovered without distortion if it is sampled at a rate of at least 2fc samples per second.*

Frequency Folding and Aliasing

The Sampling Theorem can be demonstrated by the frequency spectra illustrated in Figure 7. Figure 7(a) shows the frequency spectrum of a continuous bandwidth-limited analog signal with frequency components out to fc. When this signal is sampled at a rate fs, the modulation process shifts the original spectrum out of fs, 2fs, 3fs, etc. in addition to the one at the origin. A portion of this resultant spectrum is shown in Figure 7(b).

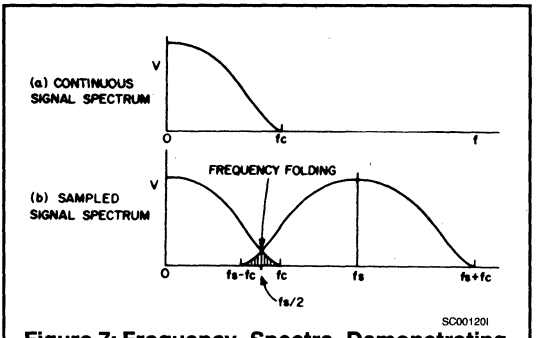


Figure 7: Frequency Spectra Demonstrating the Sampling Theorem

If the sampling frequency fs is not high enough, part of the spectrum centered about fs will fold over into the original signal spectrum. This undesirable effect is called *frequency folding*. In the process of recovering the original signal, the folded part of the spectrum causes distortion in the recovered signal which cannot be eliminated by filtering the recovered signal.

From the figure, if the sampling rate is increased such that fs – fc > fc, then the two spectra are separated and the original signal can be recovered without distortion. This demonstrates the result of the Sampling Theorem that fs > 2fc. Frequency folding can be eliminated in two ways: first by using a high enough sampling rate, and second by filtering the signal before sampling to limit its bandwidth to fs/2.

One must appreciate the fact that in practice there is always some frequency folding present due to high frequency signal components, noise, and non-ideal pre-sample filtering. The effect must be reduced to negligible amounts for the particular application by using a sufficiently high sampling rate. The required rate, in fact, may be much higher than the minimum indicated by the Sampling Theorem.

The effect of an inadequate sampling rate on a sinusoid is illustrated in Figure 8; an *alias frequency* in the recovered signal results. In this case, sampling at a rate slightly less than twice per cycle gives the low frequency sinusoid shown by the dotted line in the recovered signal. This alias frequency can be significantly different from the original frequency. From the figure it is easy to see that if the sinusoid is sampled at least twice per cycle, as required by the Sampling Theorem, the original frequency is preserved.

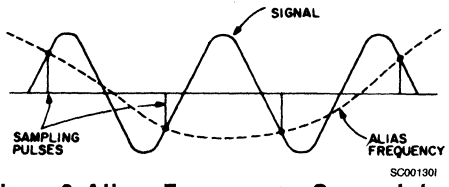


Figure 8: Alias Frequency Caused by Inadequate Sampling Rate

CODING FOR DATA CONVERTERS

Natural Binary Code

A/D and D/A converters interface with digital systems by means of an appropriate digital code. While there are many possible codes to select, a few standard ones are almost exclusively used with data converters. The most popular code is *natural binary*, or *straight binary*, which is used in its fractional form to represent a number

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ . \ . \ . \ + a_n 2^{-n}$$

where each coefficient "a" assumes a value of zero or one. N has a value between zero and one.

A binary fraction is normally written as 0.110101, but with data converter codes the decimal point is omitted and the code word is written 110101. This code word represents a fraction of the full scale value of the converter and has no other numerical significance.

The binary code word 110101 therefore represents the decimal fraction (1 x 0.5) + (1 x 0.25) + (1 x 0.125) + (1 x 0.0625) + (0 x 0.03125) + (1 x 0.015625) = 0.828125 or 82.8125% of full scale for the converter. If full scale is +10V, then the code word represents +8.28125V. The natural binary code belongs to a class of codes known as positive weighted codes since each coefficient has a specific weight, none of which is negative.

The leftmost bit has the most weight, 0.5 of full scale, and is called the *most significant bit,* or MSB; the rightmost bit has the least weight, 2^{-n} of full scale, and is therefore called the *least significant bit*, or LSB. The bits in a code word are numbered from left to right from 1 to n.

The LSB has the same analog equivalent value as Q discussed previously, namely

$$\text{LSB (Analog Value)} = \frac{\text{FSR}}{2^n}$$

Table 1 is a useful summary of the resolution, number of states, LSB weights, and dynamic range for data converters from one to twenty bits resolution.

Table 1: Resolution Number of States, LSB Weight, and Dynamic Range for Data Converters

RESOLUTION BITS n	NUMBER OF STATES 2^n	LSB WEIGHT 2^{-n}	DYNAMIC RANGE dB
0	1	1	0
1	2	0.5	6
2	4	0.25	12
3	8	0.125	18.1
4	16	0.0625	24.1
5	32	0.03125	30.1
6	64	0.015625	36.1
7	128	0.0078125	42.1
8	256	0.00390625	48.2
9	512	0.001953125	54.2
10	1 024	0.0009765625	60.2
11	2 048	0.00048828125	66.2
12	4 096	0.000244140625	72.2
13	8 192	0.0001220703125	78.3
14	16 384	0.00006103515625	84.3
15	32 768	0.000030517578125	90.3
16	65 536	0.0000152587890625	96.3
17	131 072	0.00000762939453125	102.3
18	262 144	0.000003814697265625	108.4
19	524 288	0.0000019073486328125	114.4
20	1 048 576	0.0000009536743164062 5	120.4

The *dynamic range* of a data converter in dB is found as follows:

$$DR(dB) = 20\log 2^n = 20n\log 2$$
$$= 20n(0.301) = 6.02n$$

where DR is dynamic range, n is the number of bits, and 2^n the number of states of the converter. Since 6.02dB corresponds to a factor of two, it is simply necessary to multiply the resolution of a converter in bits by 6.02. A 12-bit converter, for example, has a dynamic range of 72.2dB.

An important point to notice is that the maximum value of the digital code, namely all 1's, does not correspond with analog full scale, but rather with one LSB less than full scale, or FS $(1 - 2^{-n})$. Therefore a 12 bit converter with a 0 to +10V analog range has a maximum code of 1111 1111 1111 and a maximum analog value of +10V $(1 - 2^{-12})$ = +9.99756V. In other words, the maximum analog value of the converter, corresponding to all one's in the code, never quite reaches the point defined as analog full scale.

Other Binary Codes

Several other binary codes are used with A/D and D/A converters in addition to straight binary. These codes are *offset binary, two's complement, binary coded decimal* (BCD), and their complemented versions. Each code has a specific advantage in certain applications. BCD coding for example is used where digital displays must be interfaced such as in digital panel meters and digital multimeters. Two's complement coding is used for computer arithmetic logic operations, and offset binary coding is used with bipolar analog measurements.

Not only are the digital codes standardized with data converters, but so are the analog voltage ranges. Most converters use unipolar voltage ranges of 0 to +5V and 0 to +10V although some devices use the negative ranges 0 to −5V and 0 to −10V. The standard bipolar voltage ranges are ±2.5V, ±5V and ±10V. Many converters today are pin-programmable between these various ranges.

Table 2: Binary Coding for 8 Bit Unipolar Converters

FRACTION OF FS	+10V FS	STRAIGHT BINARY	COMPLEMENTARY BINARY
+FS−1 LSB	+9.961	1111 1111	0000 0000
+¾ FS	+7.500	1100 0000	0011 1111
+½ FS	+5.000	1000 0000	0111 1111
+¼ FS	+2.500	0100 0000	1011 1111
+⅛ FS	+1.250	0010 0000	1101 1111
+1 LSB	+0.039	0000 0001	1111 1110
0	0.000	0000 0000	1111 1111

Table 2 shows straight binary and complementary binary codes for unipolar 8 bit converter with a 0 to +10V analog FS range. The maximum analog value of the converter is +9.961V, or one LSB less than +10V. Note that the LSB size is 0.039V as shown near the bottom of the table. The *complementary binary* coding used in some converters is simply the logic complement of straight binary.

When A/D and D/A converters are used in bipolar operation, the analog range is offset by half scale, or by the MSB value. The result is an analog shift of the converter transfer function as shown in Figure 9. Notice for this 3-bit A/D converter transfer function that the code 000 corresponds with −5V, 100 with 0V, and 111 with +3.75V. Since the ouput coding is the same as before the analog shift, it is now appropriately called offset binary coding.

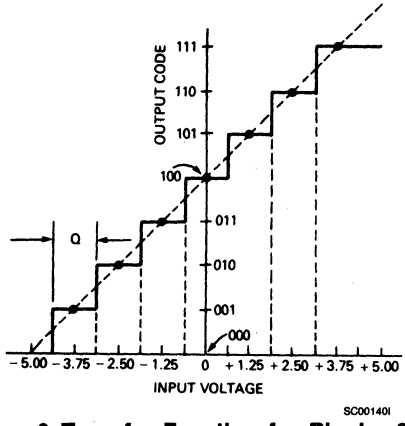


Figure 9: Transfer Function for Bipolar 3-Bit A/D Converter

Table 3 shows the offset binary code together with *complementary offset binary, two's complement, and sign-magnitude binary* codes. These are the most popular codes employed in bipolar data converters.

FRACTION OF FS	±5V FS	OFFSET BINARY	COMP. OFF BINARY	TWO'S COMPLEMENT	SIGN −MAG BINARY
+FS−1 LSB	+4.9976	1111 1111	0000 0000	0111 1111	1111 1111
+¼ FS	+3.7500	1110 0000	0001 1111	0110 0000	1110 0000
+½ FS	+2.5000	1100 0000	0011 1111	0100 0000	1100 0000
+¾ FS	+1.2500	1010 0000	0101 1111	0010 0000	1010 0000
0	0.0000	1000 0000	0111 1111	0000 0000	1000 0000
−¼ FS	−1.2500	0110 0000	1001 1111	1110 0000	0010 0000
−½ FS	−2.5000	0100 0000	1011 1111	1100 0000	0100 0000
−¾ FS	−3.7500	0010 0000	1101 1111	1010 0000	0110 0000
−FS+1 LSB	−4.9976	0000 0001	1111 1110	1000 0001	0111 1111
−FS	−5.0000	0000 0000	1111 1111	1000 0000	—

***NOTE:** Sign Magnitude Binary has two code words for zero as shown here.

Table 3: Popular Bipolar Codes Used with Data Converters

	SIGN—MAG BINARY
0+	1000 0000 0000
0	0000 0000 0000

The two's complement code has the characteristic that the sum of the positive and negative codes for the same analog magnitude always produces all zero's and a carry. This characteristic makes the two's complement code useful in arithmetic computations. Notice that the only difference between two's complement and offset binary is the complementing of the MSB. In bipolar coding, the MSB becomes the sign bit.

The sign-magnitude binary code, infrequently used, has identical code words for equal magnitude analog values except that the sign bit is different. As shown in Table 3 this code has two possible code words for zero: 1000 0000 or 0000 0000. The two are usually distinguished as 0+ and 0−, respectively. Because of this characteristic, the code has maximum analog values of ± (FS − 1 LSB) and reaches neither analog +FS or −FS.

BCD Codes

Table 4 shows BCD and complementary BCD coding for a 3 decimal digit data converter. These are the codes used with integrating type A/D converters employed in digital panel meters, digital multimeters, and other decimal display applications. Here four bits are used to represent each decimal digit. BCD is a positive weighted code but is relatively inefficient since in each group of four bits, only 10 out of a possible 16 states are utilized.

Table 4: BCD and Complementary BCD Coding

FRACTION OF FS	+10V FS	BINARY CODED DECIMAL	COMPLEMENTARY BCD
+FS−1 LSB	+9.99	1001 1001 1001	0110 0110 0110
+¾ FS	+7.50	0111 0101 0000	1000 1010 1111
+½ FS	+5.00	0101 0000 0000	1010 1111 1111
+¼ FS	+2.50	0010 0101 0000	1101 1010 1111
+⅛ FS	+1.25	0001 0010 0101	1110 1101 1010
+1 LSB	+0.01	0000 0000 0001	1111 1111 1110
0	0.00	0000 0000 0000	1111 1111 1111

The LSB analog value (or quantum, Q) for BCD is

$$\text{LSB (Analog Value)} = Q = \frac{FSR}{10^d}$$

where FSR is the full scale range and d is the number of decimal digits. For example if there are 3 digits and the full scale range is 10V, the LSB value is

$$\text{LSB (Analog Value)} = \frac{10V}{10^3} = .01V = 10mV$$

BCD coding is frequently used with an additional overrange bit which has a weight equal to full scale and produces a 100% increase in range for the A/D converter. Thus for a converter with a decimal full scale of 999, an overrange bit provides a new full scale of 1999, twice that of the previous one. In this case, the maximum output code is 1 1001 1001 1001. The additional range is commonly referred to as ½ digit, and the resolution of the A/D converter in this case is 3½ digits.

Likewise, if this range is again expanded by 100%, a new full scale of 3999 results and is called 3¾ digits resolution. Here two overrange bits have been added and the full scale output code is 11 1001 1001 1001. When BCD coding is used for bipolar measurements another bit, a sign bit, is added to the code and result is *sign-magnitude BCD* coding.

AMPLIFIERS AND FILTERS

Operational and Instrumentation Amplifiers

The front end of a data acquisition system extracts the desired analog signal from a physical parameter by means of a transducer and then amplifies and filters it. An amplifier and filter are critical components in this initial signal processing.

The amplifier must perform one or more of the following functions: boost the signal amplitude, buffer the signal, convert a signal current into a voltage, or extract a differential signal from common mode noise.

To accomplish these functions requires a variety of different amplifier types. The most popular type of amplifier is an *operational amplifier* which is a general purpose gain block with differential inputs. The op amp may be connected in many different closed loop configurations, of which a few are shown in Figure 10. The gain and bandwidth of the circuits shown depend on the external resistors connected around the amplifier. An operational amplifier is a good choice in general where a single-ended signal is to be amplified, buffered, or converted from current to voltage.

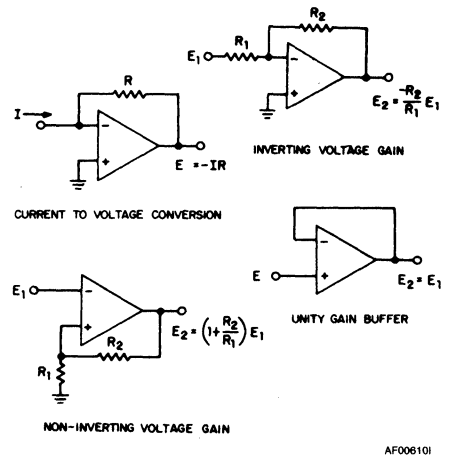


Figure 10: Operational Amplifier Configurations

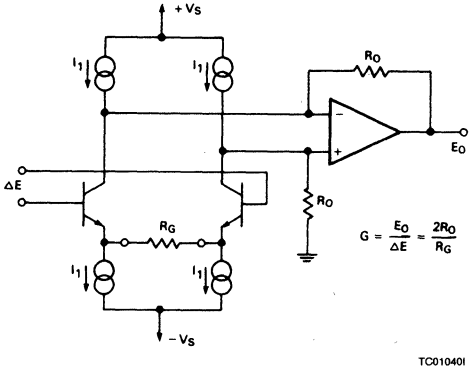


Figure 11: Simplified Instrumentation Amplifier Circuit

In the case of differential signal processing, the *instrumentation amplifier* is a better choice since it maintains high impedance at both of its differential inputs and the gain is set by a resistor located elsewhere in the amplifier circuit. One type of instrumentation amplifier circuit is shown in Figure 11. Notice that no gain-setting resistors are connected to either of the input terminals. Instrumentation amplifiers have the following important characteristics.

1. High impedance differential inputs.
2. Low input offset voltage drift.
3. Low input bias currents.
4. Gain easily set by means of one or two external resistors.
5. High common-mode rejection ratio.

Common Mode Rejection

Common-mode rejection ratio is an important parameter of differential amplifiers. An ideal differential input amplifier responds only to the voltage difference between its input

terminals and does not respond at all to any voltage that is common to both input terminals (common-mode voltage). In nonideal amplifiers, however, the common-mode input signal causes some output response even though small compared to the response to a differential input signal.

The ratio of differential and common-mode responses is defined as the common-mode rejection ratio. *Common-mode rejection ratio of an amplifier is the ratio of differential voltage gain to common-mode voltage gain and is generally expressed in dB.*

$$CMRR = 20\log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common-mode voltage gain. CMRR is a function of frequency and therefore also a function of the impedance balance between the two amplifier input terminals. At even moderate frequencies CMRR can be significantly degraded by small unbalances in the source series resistance and shunt capacitance.

Other Amplifier Types

There are several other special amplifiers which are useful in conditioning the input signal in a data acquisition system. An *isolation amplifier* is used to amplify a differential signal which is superimposed on a very high common-mode voltage, perhaps several hundred or even several thousand volts. The isolation amplifier has the characteristics of an instrumentation amplifier with a very high common-mode input voltage capability.

Another special amplifier, the *chopper stabilized amplifier*, is used to accurately amplify microvolt level signals to the required amplitude. This amplifier employs a special switching stabilizer which gives extremely low input offset voltage drift. Another useful device, the *electrometer amplifier*, has ultra-low input bias currents, generally less than one picoampere and is used to convert extremely small signal currents into a high level voltage.

Filters

A *low pass filter* frequently follows the signal processing amplifier to reduce signal noise. Low pass filters are used for the following reasons: to reduce man-made electrical interference noise, to reduce electronic noise, and to limit the bandwidth of the analog signal to less than half the sampling frequency in order to eliminate frequency folding. When used for the last reason, the filter is called a *presampling filter or anti-aliasing filter.*

Man-made electrical noise is generally periodic, as for example in power line interference, and is sometimes reduced by means of a special filter such as a *notch filter.* Electronic noise, on the other hand, is random noise with noise power proportional to bandwidth and is present in transducer resistances, circuit resistances, and in amplifiers themselves. It is reduced by limiting the bandwidth of the system to the minimum required to pass desired signal components.

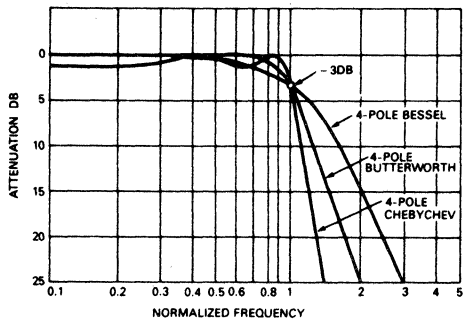


Figure 12: Some Practical Low Pass Filter Characteristics

No filter does a perfect job of eliminating noise or other undesirable frequency components, and therefore the choice of a filter is always a compromise. Ideal filters, frequently used as analysis examples, have flat passband response with infinite attenuation at the cutoff frequency, but are mathematical filters only and not physically realizable.

In practice, the systems engineer has a choice of cutoff frequency and attenuation rate. The attenuation rate and resultant phase response depend on the particular filter characteristic and the number of poles in the filter function. Some of the more popular filter characteristics include Butterworth, Chebychev, Bessel, and elliptic. In making this choice, the effect of overshoot and nonuniform phase delay must be carefully considered. Figure 12 illustrates some practical low pass filter response characteristics.

Passive RLC filters are seldom used in signal processing applications today due chiefly to the undesirable characteristics of inductors. Active filters are generally used now since they permit the filter characteristics to be accurately set by precision, stable resistors and capacitors. Inductors, with their undesirable saturation and temperature drift characteristics, are thereby eliminated. Also, because active filters use operational amplifiers, the problems of insertion loss and output loading are also eliminated.

SETTLING TIME

Definition

A parameter that is specified frequently in data acquisition and distribution systems is *settling time.* The term settling time originates in control theory but is now commonly applied to amplifiers, multiplexers, and D/A converters.

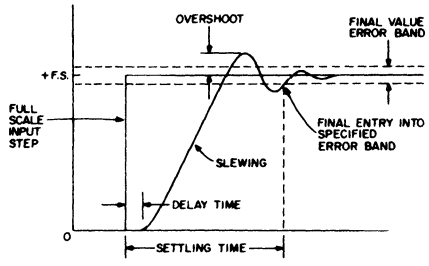


Figure 13: Amplifier Settling Time

Settling time is defined as *the time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value.* The method of application of the input step may vary depending on the type of circuit, but the definition still holds. In the case of a D/A converter, for example, the step is applied by changing the digital input code whereas in the case of an amplifier the input signal itself is a step change.

The importance of settling time in a data acquisition system is that certain analog operations must be performed in sequence, and one operation may have to be accurately settled before the next operation can be initiated. Thus a buffer amplifier preceding an A/D converter must have accurately settled before the conversion can be initiated.

Settling time for an amplifier is illustrated in Figure 13. After application of a full scale step input there is a small delay time following which the amplifier output slews, or changes at its maximum rate. *Slew rate* is determined by internal amplifier currents which must charge internal capacitances.

As the amplifier output approaches final value, it may first overshoot and then reverse and undershoot this value before finally entering and remaining within the specified error band. Note that settling time is measured to the point at which the amplifier output *enters* and *remains* within the error band. This error band in most devices is specified to either ±0.1% or ±0.01% of the full scale transition.

Amplifier Characteristics

Settling time, unfortunately, is not readily predictable from other amplifier parameters such as bandwidth, slew rate, or overload recovery time, although it depends on all of these. It is also dependent on the shape of the amplifier open loop gain characteristic, its input and output capacitance, and the dielectric absorption of any internal capacitances. An amplifier must be specifically designed for optimized settling time, and settling time is a parameter that must be determined by testing.

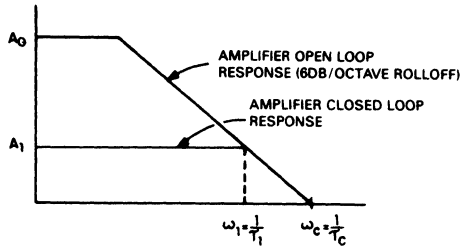


Figure 14: Amplifier Single-Pole Open Loop Gain Characteristic

One of the important requirements of a fast settling amplifier is that it have a single-pole open loop gain characteristic, i.e., one that has a smooth 6dB per octave gain roll-off characteristic to beyond the unity gain cross-over frequency. Such a desirable characteristic is shown in Figure 14.

It is important to note that an amplifier with a single-pole response can never settle faster than the time indicated by the number of closed loop time constants to the given accuracy. Figure 15 shows output error as a function of the number of time constants τ where

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f}$$

and f is the closed loop 3dB bandwidth of the amplifier.

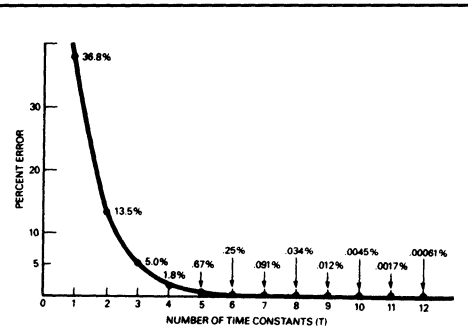


Figure 15: Output Settling Error as a Function of Number of Time Constants

Actual settling time for a good quality amplifier may be significantly longer than that indicated by the number of closed loop time constants due to slew rate limitation and overload recovery time. For example, an amplifier with a closed loop bandwidth of 1MHz has a time constant of 160nsec. which indicates a settling time of 1.44μsec. (9 time constants) to 0.01% of final value. If the slew rate of this amplifier is 1V/μsec., it will take more than 10μsec. to settle to 0.01% for a 10V change.

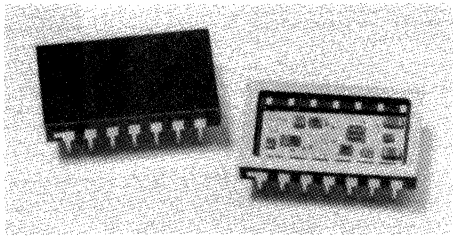


Figure 16: Ultra-Fast Settling Hybrid Operational Amplifier

If the amplifier has a nonuniform gain roll-off characteristic, then its settling time may have one of two undesirable qualities. First, the output may reach the vicinity of the error band quickly but then take a long time to actually enter it; second, it may overshoot the error band and then oscillate back and forth through it before finally entering and remaining inside it.

Modern fast settling operational amplifiers come in many different types including modular, hybrid, and monolithic amplifiers. Such amplifiers have settling times to 0.1% or 0.01% of 2μsec. down to 100nsec. and are useful in many data acquisition and conversion applications. An example of an ultra-fast settling operational amplifier of the hybrid type is shown in Figure 16.

DIGITAL-TO-ANALOG CONVERTERS

Introduction

Digital-to-analog converters are the devices by which computers communicate with the outside world. They are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digitally controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters. D/A converters are also referred to as DAC's and are termed *decoders* by communications engineers.

The transfer function of an ideal 3-bit D/A converter is shown in Figure 17. Each input code word produces a single, discrete analog output value, generally a voltage. Over the output range of the converter 2^n different values are produced including zero; and the output has a one-to-one correspondence with input, which is not true for A/D converters.

There are many different circuit techniques used to implement D/A converters, but a few popular ones are widely used today. Virtually all D/A converters in use are of the *parallel type* where all bits change simultaneously upon application of an input code word; *serial type* D/A converters, on the other hand, produce an analog output only after receiving all digital input data in sequential form.

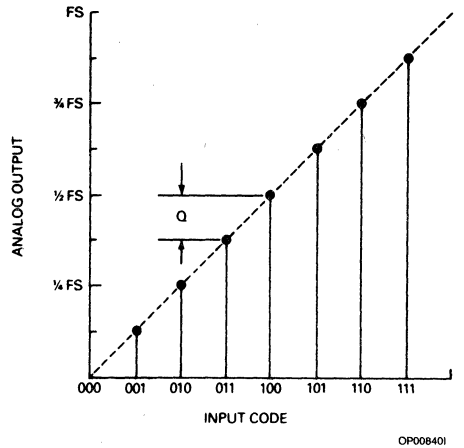


Figure 17: Transfer Function of Ideal 3-bit D/A Converter

Weighted Current Source D/A Converter

The most popular D/A converter design in use today is the weighted current source circuit illustrated in Figure 18. An array of switched transistor current sources is used with binary weighted currents. The binary weighting is achieved by using emitter resistors with binary related values of R, 2R, 4R, 8R, ... 2^nR. The resulting collector currents are then added together at the current summing line.

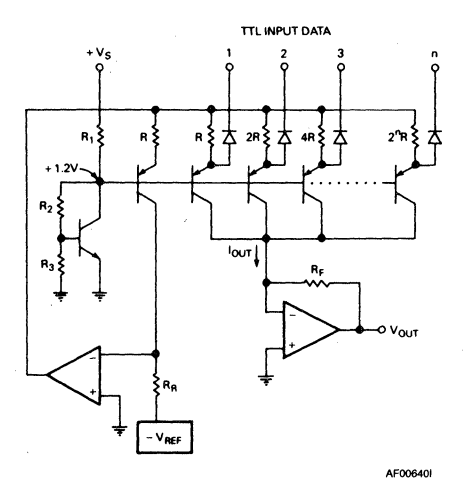


Figure 18: Weighted Current Source D/A Converter

The current sources are switched on or off from standard TTL inputs by means of the control diodes connected to each emitter. When the TTL input is high the current source is on; when the input is low it is off, with the current flowing through the control diode. Fast switching speed is achieved because there is direct control of the transistor current, and the current sources never go into saturation.

To interface with standard TTL levels, the current sources are biased to a base voltage of +1.2V. The emitter currents are regulated to constant values by means of the control amplifier and a precision voltage reference circuit together with a bipolar transistor.

The summed output currents from all current sources that are on go to an operational amplifier summing junction; the amplifier converts this output current into an output voltage. In some D/A converters the output current is used to directly drive a resistor load for maximum speed, but the positive output voltage in this case is limited to about +1 volt.

The weighted current source design has the advantages of simplicity and high speed. Both PNP and NPN transistor current sources can be used with this technique although the TTL interfacing is more difficult with NPN sources. This technique is used in most monolithic, hybrid, and modular D/A converters in use today.

A difficulty in implementing higher resolution D/A converter designs is that a wide range of emitter resistors is required, and very high value resistors cause problems with both temperature stability and switching speed. To overcome these problems, weighted current sources are used in identical groups, with the output of each group divided down by a resistor divider as shown in Figure 19.

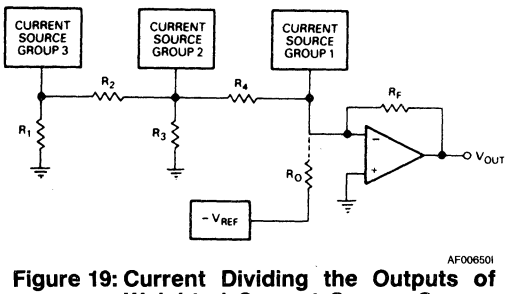


Figure 19: Current Dividing the Outputs of Weighted Current Source Groups

The resistor network, R_1 through R_4, divides the output of Group 3 down by a factor of 256 and the output of Group 2 down by a factor of 16 with respect to the output of Group 1. Each group is identical, with four current sources of the type shown in Figure 18, having binary current weights of 1, 2, 4, 8. Figure 19 also illustrates the method of achieving a bipolar output by deriving an offset current from the reference circuit which is then subtracted from the output current line through resistor R_O. This current is set to exactly one half the full scale output current.

R-2R D/A Converter

A second popular technique for D/A conversion is the R-2R ladder method. As shown in Figure 20, the network consists of series resistors of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a single-pole double-throw electronic switch which connects the resistor to either ground or the output current summing line.

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point A looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

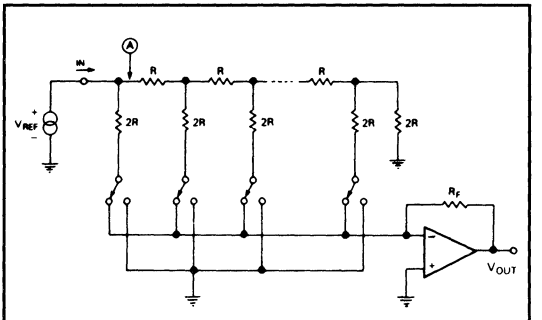


Figure 20: R-2R Ladder D/A Converter

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

$$I_{OUT} = \frac{V_{REF}}{R}\left[1/2 + 1/4 + 1/8 \ldots\ldots \frac{1}{2^n}\right]$$

which is a binary series. The sum of all currents is then

$$I_{OUT} = \frac{V_{REF}}{R}\left(1 - 2^{-n}\right)$$

where the 2^n term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

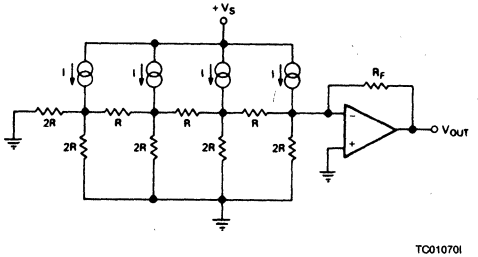
The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A converters by using laser-trimmed thin film resistor networks.

Multiplying and Deglitched D/A Converters

The R-2R ladder method is specifically used for *multiplying type* D/A converters. With these converters, the reference voltage can be varied over the full range of $\pm V_{max}$ with the output the product of the reference voltage and the digital input word. Multiplication can be performed in 1, 2, or 4 algebraic quadrants.

If the reference voltage is unipolar, the circuit is a one-quadrant multiplying DAC; if it is biplolar, the circuit is a two-quadrant multiplying DAC. For four-quadrant operation the two current summing lines shown in Figure 20 must be subtracted from each other by operational amplifiers.

In multiplying D/A converters, the electronic switches are usually implemented with CMOS devices. Multiplying DAC's are commonly used in automatic gain controls, CRT character generation, complex function generators, digital attenuators, and divider circuits.



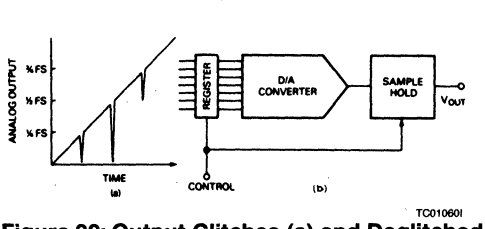
TC01070I

Figure 21: D/A Converter Employing R-2R Ladder with Equal Value Switched Current Sources

Another important D/A converter design takes advantage of the best features of both the weighted current source technique and the R-2R ladder technique. This circuit, shown in Figure 21, uses equal value switched current sources to drive the junctions of the R-2R ladder network. The advantage of the equal value current sources is obvious since all emitter resistors are identical and switching speeds are also identical. This technique is used in many ultra-high speed D/A converters.

One other specialized type D/A converter used primarily in CRT display systems is the *deglitched* D/A converter. All D/A converters produce output spikes, or *glitches*, which are most serious at the major output transitions of 1/4 FS, 1/2 FS, and 3/4 FS as illustrated in Figure 23(a).

Glitches are caused by small time differences between some current sources turning off and others turning on. Take, for example, the major code transition at half scale from 0111 . . . . 1111 to 1000 . . . . 0000. Here the MSB current source turns on while all other current sources turn off. The small difference in switching times results in a narrow half scale glitch. Such a glitch produces distorted characters on CRT displays.



TC01060I

Figure 22: Output Glitches (a) and Deglitched D/A Converter (b)

Glitches can be virtually eliminated by the circuit shown in Figure 23(b). The digital input to a D/A converter is controlled by an input register while the converter output goes to a specially designed sample-hold circuit. When the digital input is updated by the register, the sample-hold is switched into the hold mode. After the D/A has changed to its new output value and all glitches have settled out, the sample-hold is then switched back into the tracking mode. When this happens, the output changes smoothly from its previous value to the new value with no glitches present.

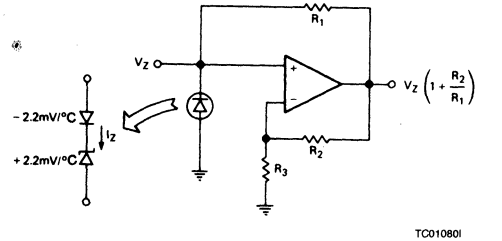
VOLTAGE REFERENCE CIRCUITS

An important circuit required in both A/D and D/A converters is the voltage reference. The accuracy and stability of a data converter ultimately depends upon the reference; it must therefore produce a constant output voltage over both time and temperature.

The compensated zener reference diode with a buffer-stabilizer circuit is commonly used in most data converters today. Although the compensated zener may be one of several types, the compensated *subsurface*, or *buried*, zener is probably the best choice. These new devices produce an avalanche breakdown which occurs beneath the surface of the silicon, resulting in better long-term stability and noise characteristics than with earlier surface breakdown zeners.

These reference devices have reverse breakdown voltages of about 6.4 volts and consist of a forward biased diode in series with the reversed biased zener. Because the diodes have approximately equal and opposite voltage changes with temperature, the result is a temperature stable voltage. Available devices have temperature coefficients from 100ppm/°C to less than 1ppm/°C.

Some of the new IC voltage references incorporate active circuitry to buffer the device and reduce its dynamic impedance; in addition, some contain temperature regulation circuitry on the chip to achieve ultra-low tempcos.



TC01080I

Figure 23: A Precision, Buffered Voltage Reference Circuit

A popular buffered reference circuit is shown in Figure 23; this circuit produces an output voltage higher than the reference voltage. It also generates a constant, regulated current through the reference which is determined by the three resistors.

Some monolithic A/D and D/A converters use another type of reference device known as the *bandgap reference*. This circuit is based on the principle of using the known, predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon. This reference gives excellent results for the lower reference voltages of 1.2 or 2.5 volts.

ANALOG-TO-DIGITAL CONVERTERS

Counter Type A/D Converter

Analog-to-digital converters, also called ADC's or *encoders*, employ a variety of different circuit techniques to implement the conversion function. As with D/A converters, however, relatively few of these circuits are widely used today. Of the various techniques available, the choice depends on the resolution and speed required.

One of the simplest A/D converters is the *counter*, or *servo*, type. This circuit employs a digital counter to control the input of a D/A converter. Clock pulses are applied to the counter and the output of the D/A is stepped up one LSB at a time. A comparator compares the D/A output with the analog input and stops the clock pulses when they are equal. The counter output is then the converted digital word.

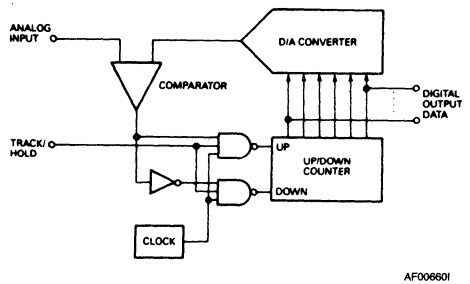


Figure 24: Tracking Type A/D Converter

While this converter is simple, it is also relatively slow. An improvement on this technique is shown in Figure 24 and is known as a *tracking* A/D converter, a device commonly used in control systems. Here an up-down counter controls the DAC, and the clock pulses are directed to the pertinent counter input depending on whether the D/A output must increase or decrease to reach the analog input voltage.

The obvious advantage of the tracking A/D converter is that it can continuously follow the input signal and give updated digital output data if the signal does not change too rapidly. Also, for small input changes, the conversion can be quite fast. The converter can be operated in either the track or hold modes by a digital input control.

Successive-Approximation A/D Converters

By far, the most popular A/D conversion technique in general use for moderate to high speed applications is the *successive-approximation* type A/D. This method falls into a class of techniques known as *feedback type* A/D converters, to which the counter type also belongs. In both cases a D/A converter is in the feedback loop of a digital control circuit which changes its output until it equals the analog input. In the case of the successive-approximation converter, the DAC is controlled in an optimum manner to complete a conversion in just n-steps, where n is the resolution of the converter in bits.

The operation of this converter is analogous to weighing an unknown on a laboratory balance scale using standard weights in a binary sequence such as 1, ½, ¼, ⅛ . . . . . 1/n kilograms. The correct procedure is to begin with the largest standard weight and proceed in order down to the smallest one.

The largest weight is placed on the balance pan first; if it does not tip, the weight is left on and the next largest weight is added. If the balance does tip, the weight is removed and the next one added. The same procedure is used for the next largest weight and so on down to the smallest. After the nth standard weight has been tried and a decision made, the weighing is finished. The total of the standard weights remaining on the balance is the closest possible approximation to the unknown.

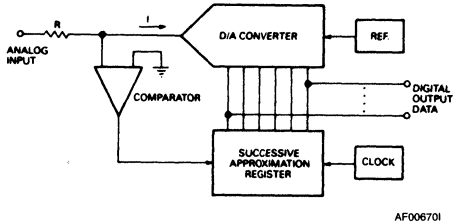


Figure 25: Successive Approximation A/D Converter

In the successive-approximation A/D converter illustrated in Figure 25, a successive-approximation register (SAR) controls the D/A converter by implementing the weighing logic just described. The SAR first turns on the MSB of the DAC and the comparator tests this output against the analog input. A decision is made by the comparator to leave the bit on or turn it off after which bit 2 is turned on and a second comparison made. After n-comparisons the digital output of the SAR indicates all those bits which remain on and produces the desired digital code. The clock circuit controls the timing of the SAR. Figure 26 shows the D/A converter output during a typical conversion.

The conversion efficiency of this technique means that high resolution conversions can be made in very short times. For example, it is possible to perform a 10 bit conversion in 1μsec. or less and a 12 bit conversion in 2μsec. or less. Of course the speed of the internal circuitry, in particular the D/A and comparator, are critical for high speed performance.

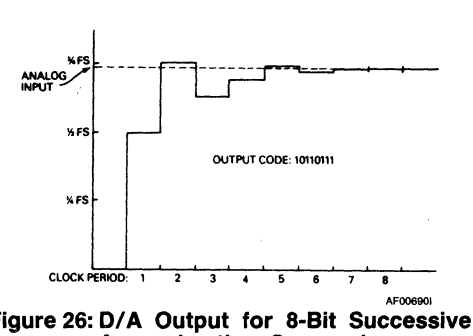


Figure 26: D/A Output for 8-Bit Successive Approximation Conversion

The Parallel (Flash) A/D Converter

For ultra-fast conversions required in video signal processing and radar applications where up to 8 bits resolution is required, a different technique is employed; it is known as the *parallel* (also *flash*, or *simultaneous*) method and is illustrated in Figure 27.

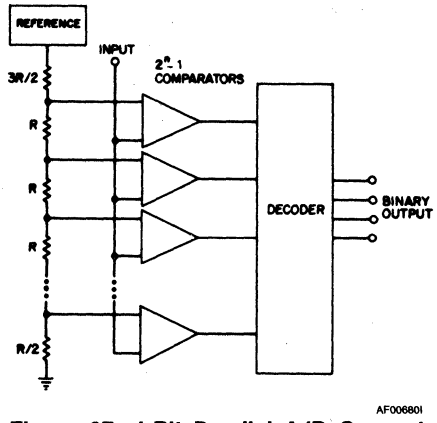


Figure 27: 4-Bit Parallel A/D Converter

This circuit employs 2^n-1 analog comparators to directly implement the quantizer transfer function of an A/D converter.

The comparator trip-points are spaced 1 LSB apart by the series resistor chain and voltage reference. For a given analog input voltage all comparators biased below the voltage turn on and all those biased above it remain off. Since all comparators change state simultaneously, the quantization process is a one-step operation.

A second step is required, however, since the logic output of the comparators is not in binary form.

Therefore an ultra-fast decoder circuit is employed to make the logic conversion to binary. The parallel technique reaches the ultimate in high speed because only two sequential operations are required to make the conversion.

The limitation of the method, however, is in the large number of comparators required for even moderate resolutions. A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stages as shown in Figure 28.

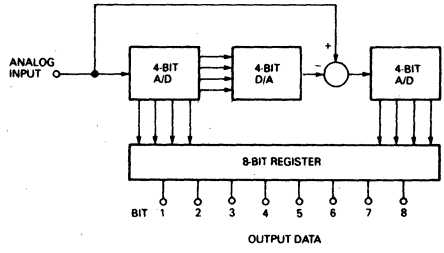


Figure 28: Two-Stage Parallel 8-Bit A/D Converter

The result of the first 4-bit conversion is converted back to analog by means of an ultra-fast 4-bit D/A and then subtracted from the analog input. The resulting residue is then converted by the second 4-bit A/D, and the two sets of data are accumulated in the 8-bit output register.

Converters of this type achieve 8-bit conversions at rates of 20 MHz and higher, while single stage 4-bit conversions can reach 50 to 100MHz rates.

INTEGRATING TYPE A/D CONVERTERS

Indirect A/D Conversion

Another class of A/D converters known as integrating type operates by an indirect conversion method. The unknown input voltage is converted into a time period which is then measured by a clock and counter. A number of variations exist on the basic principle such as *single-slope*, *dual-slope*,and *triple-slope* methods. In addition there is another technique — completely different — which is known as the *charge-balancing* or *quantized feedback* method.

The most popular of these methods are dual-slope and charge-balancing; although both are slow, they have excellent linearity characteristics with the capability of rejecting input noise. Because of these characteristics, integrating type A/D converters are almost exclusively used in digital panel meters, digital multimeters, and other slow measurement applications.

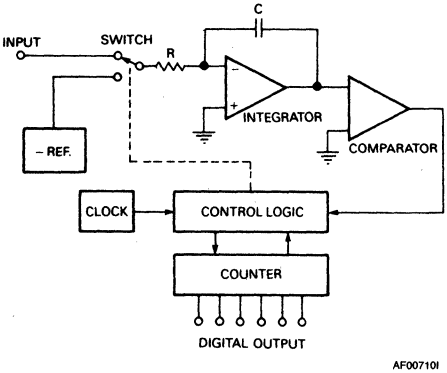


Figure 29: Dual Slope A/D Converter

Dual-Slope A/D Conversion

The dual-slope technique, shown in Figure 29, is perhaps best known. Conversion begins when the unknown input voltage is switched to the integrator input; at the same time the counter begins to count clock pulses and counts up to overflow. At this point the control circuit switches the integrator to the negative reference voltage which is integrated until the output is back to zero. Clock pulses are counted during this time until the comparator detects the zero crossing and turns them off.

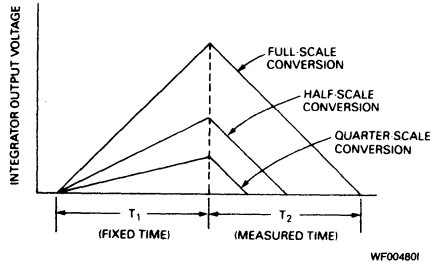


Figure 30: Integrator Output Waveform for Dual Slope A/D Converter

The counter output is then the converted digital word. Figure 30 shows the integrator output waveform where T_1 is a fixed time and T_2 is a time proportional to the input voltage. The times are related as follows:

$$T_2 = T_1 \frac{E_{IN}}{V_{REF}}$$

The digital output word therefore represents the ratio of the input voltage to the reference.

Dual-slope conversion has several important features. First, conversion accuracy is independent of the stability of the clock and integrating capacitor so long as they are constant during the conversion period. Accuracy depends only on the reference accuracy and the integrator circuit linearity. Second, the noise rejection of the converter can be infinite if T_1 is set to equal the period of the noise. To reject 60Hz power noise therefore requires that T_1 be 16.667msec.

Charge-Balancing A/D Conversion

The charge-balancing, or quantized feedback, method of conversion is based on the principle of generating a pulse train with frequency proportional to the input voltage and then counting the pulses for a fixed period of time. This circuit is shown in Figure 31. Except for the counter and timer, the circuit is a *voltage-to-frequency* (V/F) converter which generates an output pulse rate proportional to input voltage.

The circuit operates as follows. A positive input voltage causes a current to flow into the operational integrator through R_1. This current is integrated, producing a negative going ramp at the output. Each time the ramp crosses zero the comparator output triggers a precision pulse generator which puts out a constant width pulse.

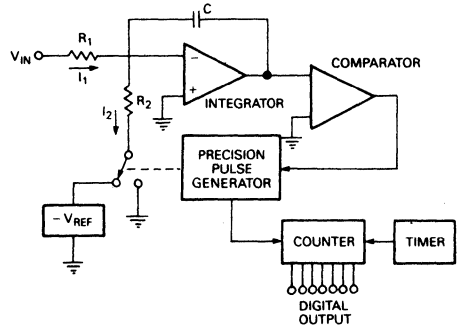


Figure 31: Charge-Balancing A/D Converter

The pulse output controls switch S_1 which connects R_2 to the negative reference for the duration of the pulse. During this time a pulse of current flows out of the integrator summing junction, producing a fast, positive ramp at the integrator output. This process is repeated, generating a train of current pulses which exactly balances the input current — hence the name charge balancing. This balance has the following relationship:

$$f = \frac{1}{\tau} \frac{V_{IN}}{V_{REF}} \frac{R_2}{R_1}$$

where τ is the pulse width and f the frequency.

A higher input voltage therefore causes the integrator to ramp up and down faster, producing higher frequency output pulses. The timer circuit sets a fixed time period for counting. Like the dual-slope converter, the circuit also integrates input noise, and if the timer is synchronized with the noise frequency, infinite rejection results. Figure 32 shows the noise rejection characteristic of all integrating type A/D converters with rejection plotted against the ratio of integration period to noise period.

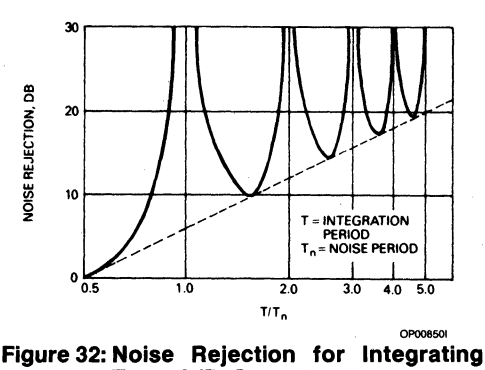


Figure 32: Noise Rejection for Integrating Type A/D Converters

ANALOG MULTIPLEXERS

Analog Multiplexer Operation

Analog multiplexers are the circuits that time-share an A/D converter among a number of different analog channels. Since the A/D converter in many cases is the most expensive component in a data acquisition system, multiplexing analog inputs to the A/D is an economical approach. Usually the analog multiplexer operates into a sample-hold circuit which holds the required analog voltage long enough for A/D conversion.

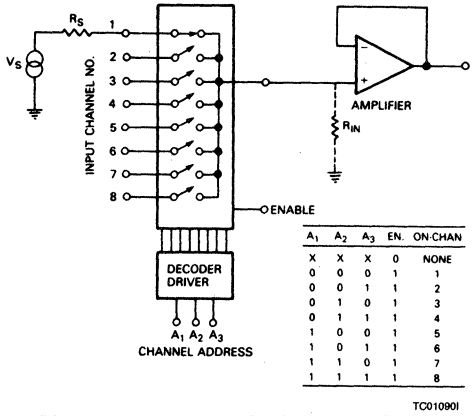


Figure 33: Analog Multiplexer Circuit

As shown in Figure 33, an analog multiplexer consists of an array of parallel electronic switches connected to a common output line. Only one switch is turned on at a time. Popular switch configurations include 4, 8, and 16 channels which are connected in single (single-ended) or dual (differential) configurations.

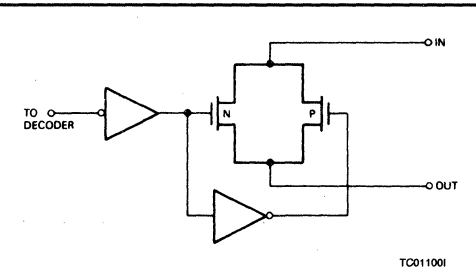


Figure 34: CMOS Analog Switch Circuit

The multiplexer also contains a decoder-driver circuit which decodes a binary input word and turns on the appropriate switch. This circuit interfaces with standard TTL inputs and drives the multiplexer switches with the proper control voltages. For the 8-channel analog multiplexer shown, a one-of-eight decoder circuit is used.

Most analog multiplexers today employ the CMOS switch circuit shown in Figure 34. A CMOS driver controls the gates of parallel-connected P-channel and N-channel MOSFET's. Both switches turn on together with the parallel connection giving relatively uniform on-resistance over the required analog input voltage range. The resulting on-resistance may vary from about 50 ohms to 2K ohms depending on the multiplexer; this resistance increases with temperature.

Analog Multiplexer Characteristics

Because of the series resistance, it is common practice to operate an analog multiplexer into a very high load resistance such as the input of a unity gain buffer amplifier shown in the diagram. The load impedance must be large compared with the switch on-resistance and any series source resistance in order to maintain high transfer accuracy. *Transfer error* is the input to output error of the multiplexer with the source and load connected; error is expressed as a percent of input voltage.

Transfer errors of 0.1% to 0.01% or less are required in most data acquisition systems. This is readily achieved by using operational amplifier buffers with typical input impedances from 10^8 to 10^{12} ohms. Many sample-hold circuits also have very high input impedances.

Another important characteristic of analog multiplexers is *break-before-make* switching. There is a small time delay between disconnection from the previous channel and connection to the next channel which assures that two adjacent input channels are never instantaneously connected together.

Settling time is another important specification for analog multiplexers; it is the same definition previously given for amplifiers except that it is measured from the time the channel is switched on. *Throughput rate* is the highest rate at which a multiplexer can switch from channel to channel with the output settling to its specified accuracy. *Crosstalk* is the ratio of output voltage to input voltage with all channels connected in parallel and off; it is generally expressed as an input to output attenuation ratio in dB.

As shown in the representative equivalent circuit of Figure 35, analog multiplexer switches have a number of leakage currents and capacitances associated with their operation. These parameters are specified on data sheets and must be considered in the operation of the devices. Leakage currents, generally in picoamperes at room temperature, become troublesome only at high temperatures. Capacitances affect crosstalk and settling time of the multiplexer.

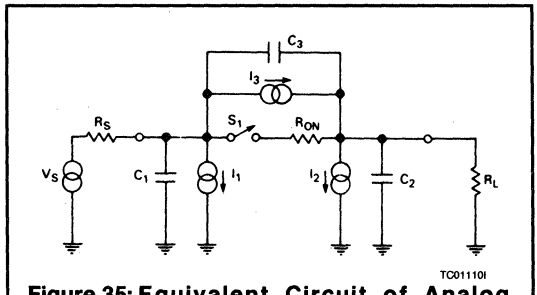


Figure 35: Equivalent Circuit of Analog Multiplexer Switch

Analog Multiplexer Applications

Analog multiplexers are employed in two basic types of operation: high-level and low-level. In *high-level multiplexing*, the most popular type, the analog signal is amplified to the 1 to 10V range ahead of the multiplexer. This has the advantage of reducing the effects of noise on the signal during the remaining analog processing. In *low-level multiplexing* the signal is amplified after multiplexing; therefore great care must be exercised in handling the low-level signal up to the multiplexer. Low-level multiplexers generally use two-wire differential switches in order to minimize noise pick-up. Reed relays, because of essentially zero series resistance and absence of switching spikes, are frequently employed in low-level multiplexing systems. They are also useful for high common-mode voltages.

A useful specialized analog multiplexer is the *flying-capacitor* type. This circuit, shown as a single channel in Figure 36 has differential inputs and is particularly useful with high common-mode voltages. The capacitor connects first to the differential analog input, charging up to the input voltage, and is then switched to the differential output which goes to a high input impedance instrumentation amplifier. The differential signal is therefore transferred to the amplifier input without the common mode voltage and is then further processed up to A/D conversion.

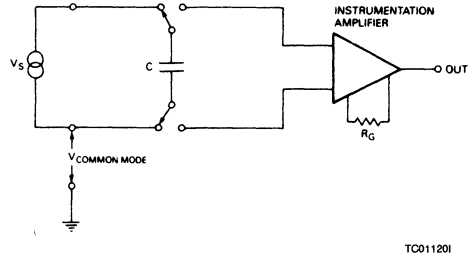


Figure 36: Flying Capacitor Multiplexer Switch

In order to realize large numbers of multiplexed channels, you can connect analog multiplexers in parallel using the enable input to control each device. This is called *single-level multiplexing*. You can also connect the output of several multiplexers to the inputs of another to expand the number of channels; this method is *double-level multiplexing*.

SAMPLE-HOLD CIRCUITS

Operation of Sample-Holds

Sample-hold circuits, discussed earlier, are the devices which store analog information and reduce the aperture time of an A/D converter. A sample-hold is simply a voltage-memory device in which an input voltage is acquired and then stored on a high quality capacitor. A popular circuit is shown in Figure 37.

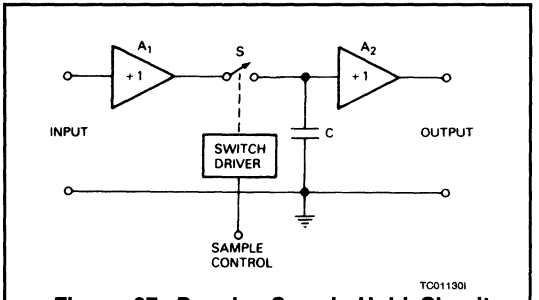


Figure 37: Popular Sample-Hold Circuit

A_1 is an input buffer amplifier with a high input impedance so that the source, which may be an analog multiplexer, is not loaded. The output of A_1 must be capable of driving the hold capacitor with stability and enough drive current to charge it rapidly. S_1 is an electronic switch, generally an FET, which is rapidly switched on or off by a driver circuit which interfaces with TTL inputs.

C is a capacitor with low leakage and low dielectric absorption characteristics; it is a polystyrene, polycarbonate, polypropylene, or teflon type. In the case of hybrid sample-holds, the MOS type capacitor is frequently used.

A_2 is the output amplifier which buffers the voltage on the hold capacitor. It must therefore have extremely low input bias current, and for this reason an FET input amplifier is required.

There are two modes of operation for a sample-hold: *sample* (or tracking) *mode*, when the switch is closed; and *hold mode*, when the switch is open. Sample-holds are usually operated in one of two basic ways. The device can continuously track the input signal and be switched into the hold mode only at certain specified times, spending most of the time in tracking mode. This is the case for a sample-hold employed as a deglitcher at the output of a D/A converter, for example.

Alternatively, the device can stay in the hold mode most of the time and go to the sample mode just to acquire a new input signal level. This is the case for a sample-hold used in a data acquisition system following the multiplexer.

The Sample-Hold as a Data Recovery Filter

A common application for sample-hold circuits is *data recovery*, or *signal reconstruction, filters*. The problem is to reconstruct a train of analog samples into the original signal; when used as a recovery filter, the sample-hold is known as a *zero-order hold*. It is a useful filter because it fills in the space between samples, providing data smoothing.

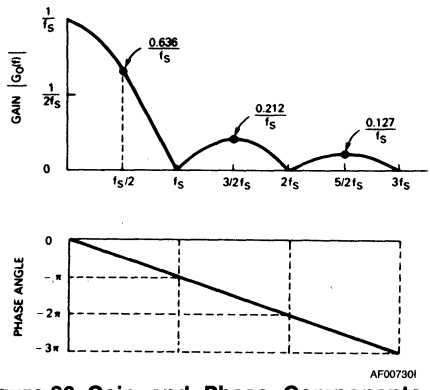


Figure 38: Gain and Phase Components of Zero-Order Hold Transfer Function

As with other filter circuits, the gain and phase components of the transfer function are of interest. By an analysis based on the impulse response of a sample-hold and use of the Laplace transform, the transfer function is found to be

$$G_0(f) = \frac{1}{f_S}\left[\frac{\sin\pi\left(\frac{f}{f_S}\right)}{\pi\left(\frac{f}{f_S}\right)}\right]\epsilon^{-j\pi f/f_S}$$

where f_S is the sampling frequency. This function contains the familiar (sin x)/x term plus a phase term, both of which are plotted in Figure 38.

The sample-hold is therefore a low pass filter with a cut-off frequency slightly less than $f_S/2$ and a linear phase response which results in a constant delay time of T/2, where T is the time between samples. Notice that the gain function also has significant response lobes beyond f_S. For this reason a sample-hold reconstruction filter is frequently followed by another conventional low pass filter.

Other Sample-Hold Circuits

In addition to the basic circuit of Figure 37, there are several other sample-hold circuit configurations which are frequently used. Figure 39 shows two such circuits which are closed loop circuits as contrasted with the open loop circuit of Figure 37. Figure 39(a) uses an operational integrator and another amplifier to make a fast, accurate inverting sample-hold. A buffer amplifier is sometimes added in front of this circuit to give high input impedance. Figure 39(b) shows a high input impedance non-inverting sample-hold circuit.

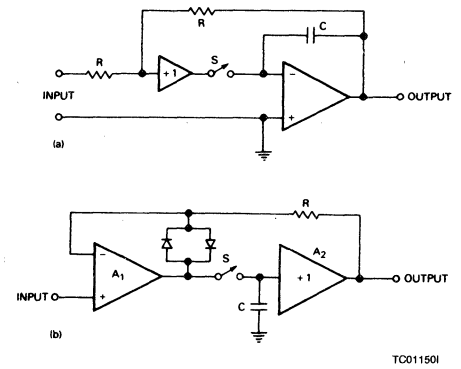


Figure 39: Two Closed Loop Sample-Hold Circuits

The circuit in Figure 37, although generally not as accurate as those in Figure 39, can be used with a diode-bridge switch to realize ultra-fast acquisition sample-holds.

Sample-Hold Characteristics

A number of parameters are important in characterizing sample-hold performance. Probably most important of these is *acquisition time.* The definition is similar to that of settling time for an amplifier. It is the time required, after the sample-command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band around final value.

Several hold-mode specifications are also important. *Hold-mode droop* is the output voltage change per unit time when the sample switch is open. This droop is caused by the leakage currents of the capacitor and switch, and the output amplifier bias current. *Hold-mode feedthrough* is the percentage of input signal transferred to the output when the sample switch is open. It is measured with a sinusoidal input signal and caused by capacitive coupling.

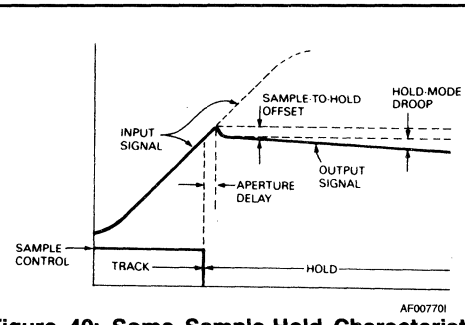


Figure 40: Some Sample-Hold Characteristics

The most critical phase of sample-hold operation is the transition from the sample mode to the hold mode. Several important parameters characterize this transition. *Sample-to-hold offset* (or step) *error* is the change in output voltage from the sample mode to the hold mode, with a constant input voltage. It is caused by the switch transferring charge onto the hold capacitor as it turns off.

Aperture delay is the time elapsed from the hold command to when the switch actually opens; it is generally much less than a microsecond. *Aperture uncertainty* (or *aperture jitter*) is the time variation, from sample to sample, of the aperture delay. It is the limit on how precise is the point in time of opening the switch. Aperture uncertainty is the time used to determine the aperture error due to rate of change of the input signal. Several of the above specifications are illustrated in the diagram of Figure 40.

Sample-hold circuits are simple in concept, but generally difficult to fully understand and apply. Their operation is full of subtleties, and they must therefore be carefully selected and then tested in a given application.

SPECIFICATION OF DATA CONVERTERS

Ideal vs. Real Data Converters

Real A/D and D/A converters do not have the ideal transfer functions discussed earlier. There are three basic departures from the ideal: offset, gain, and linearity errors. These errors are all present at the same time in a converter; in addition they change with both time and temperature.

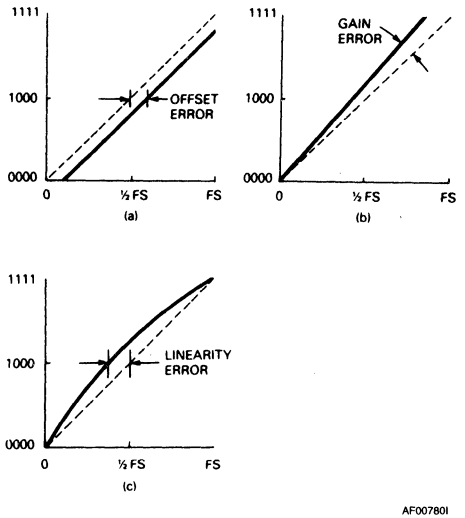


Figure 41: Offset (a), Gain (b), and Linearity (c) Errors for an A/D Converter

Figure 41 shows A/D converter transfer functions which illustrate the three error types. Figure 41(a) shows *offset error*, the analog error by which the transfer function fails to pass through zero. Next, in Figure 41(b) is *gain error*, also called *scale factor error*; it is the difference in slope between the actual transfer function and the ideal, expressed as a percent of analog magnitude.

In Figure 41(c) *linearity error*, or nonlinearity, is shown; this is defined as the maximum deviation of the actual transfer function from the ideal straight line at any point along the function. It is expressed as a percent of full scale or in LSB size, such as ± ½ LSB, and assumes that offset and gain errors have been adjusted to zero.

Most A/D and D/A converters available today have provision for external trimming of offset and gain errors. By careful adjustment these two errors can be reduced to zero, at least at ambient temperature. Linearity error, on the other hand, is the remaining error that cannot be adjusted out and is an inherent characteristic of the converter.

Data Converter Error Characteristics

Basically there are only two ways to reduce linearity error in a given application. First, a better quality higher cost converter with smaller linearity error can be procured. Second, a computer or microprocessor can be programmed to perform error correction on the converter. Both alternatives may be expensive in terms of hardware or software cost.

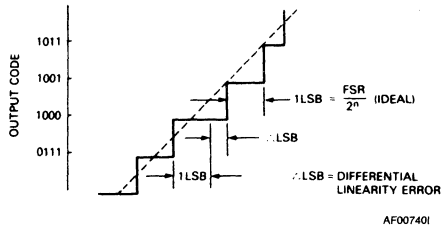


Figure 42: Defining Differential Linearity Error

The linearity error discussed above is actually more precisely termed *integral linearity error*. Another important type of linearity error is known as *differential linearity error*. This is defined as the maximum amount of deviation of any quantum (or LSB change) in the entire transfer function from its ideal size of $FSR/2^n$. Figure 42 shows that the actual quantum size may be larger or smaller than the ideal; for example, a converter with a maximum differential linearity error of ± ½LSB can have a quantum size between ½LSB and 1 ½LSB anywhere in its transfer function. In other words, any given analog step size is (1 ± ½) LSB. Integral and differential linearities can be thought of as macro- and micro-linearities, respectively.

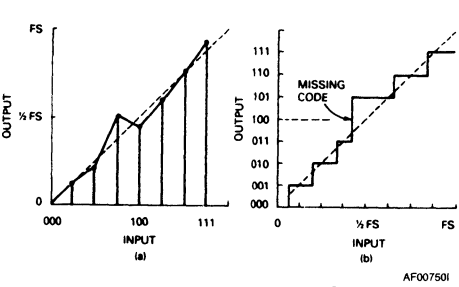


Figure 43: Nonmonotonic D/A Converter (a) and A/D Converter with Missing Code (b)

Two other important data converter characteristics are closely related to the differential linearity specification. The first is *monotonicity*, which applies to D/A converters. Monotonicity is the characteristic whereby the output of a

circuit is a continuously increasing function of the input. Figure 43(a) shows a *nonmonotonic* D/A converter output where, at one point, the output decreases as the input increases. A D/A converter may go nonmonotonic if its differential linearity error exceeds 1 LSB; if it is always less than 1 LSB, it assures that the device will be monotonic.

The term *missing code*, or *skipped code*, applies to A/D converters. If the differential linearity error of an A/D converter exceeds 1 LSB, its output can miss a code as shown in Figure 43(b). On the other hand, if the differential linearity error is always less than 1 LSB, this assures that the converter will not miss any codes. Missing codes are the result of the A/D converter's internal D/A converter becoming nonmonotonic.

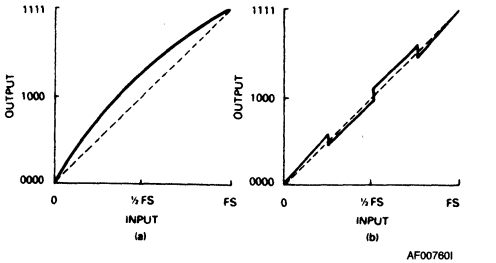


Figure 44: Linearity Characteristics of Integrating (a) and Successive Approximation (b) A/D Converters

For A/D converters the character of the linearity error depends on the technique of conversion. Figure 44(a), for example, shows the linearity characteristic of an integrating type A/D converter. The transfer function exhibits a smooth curvature between zero and full scale. The predominant type of error is integral linearity error, while differential linearity error is virtually nonexistent.

Figure 44(b), on the other hand, shows the linearity characteristic of a successive approximation A/D converter; in this case differential linearity error is the predominant type, and the largest errors occur at the specific transitions at ½, ¼, and ¾ scale. This result is caused by the internal D/A converter nonlinearity; the weight of the MSB and bit 2 current sources is critical in relation to all the other weighted current sources in order to achieve ±½ LSB maximum differential linearity error.

Temperature Effects

Ambient temperature change influences the offset, gain, and linearity errors of a data converter. These changes over temperature are normally specified in ppm of full scale range per degree Celsius. When operating a converter over significant temperature change, the effect on accuracy must be carefully determined. Of key importance is whether the device remains monotonic, or has no missing codes, over the temperatures of concern. In many cases the total error change must be computed, i.e., the sum of offset, gain, and linearity errors due to temperature.

The characteristic of monotonicity, or no missing codes, over a given temperature change can be readily computed from the *differential linearity tempco* specified for a data converter. Assuming the converter initially has ½LSB of differential linearity error, the change in temperature for an increase to 1 LSB is therefore

$$\Delta T = \frac{2^{-n} \cdot 10^6}{2\ DLT}$$

where n is the converter resolution in bits and DLT is the specified differential linearity tempco in ppm of FSR/°C. ΔT is the maximum change in ambient temperature which assures that the converter will remain monotonic, or have no missing codes.

SELECTION OF DATA CONVERTERS

One must keep in mind a number of important considerations in selecting A/D or D/A converters. An organized approach to selection suggests drawing up a checklist of required characteristics. An initial checklist should include the following key items:

1. Converter type
2. Resolution
3. Speed
4. Temperature coefficient

After the choice has been narrowed by these considerations, a number of other parameters must be considered. Among these are analog signal range, type of coding, input impedance, power supply requirements, digital interface required, linearity error, output current drive, type of start and status signals for an A/D, power supply rejection, size, and weight. One should list these parameters in order of importance to efficiently organize the selection process.

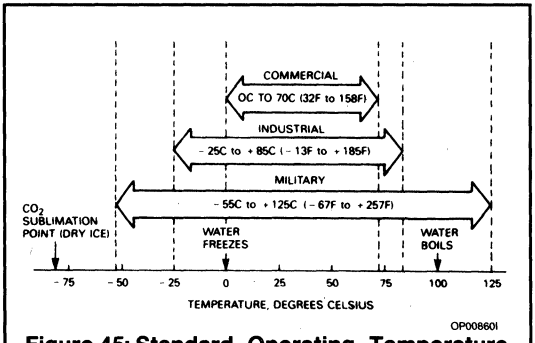


Figure 45: Standard Operating Temperature Ranges for Data Converters

In addition, the required operating temperature range must be determined; data converters are normally specified for one of three basic ranges known in the industry as commercial, industrial, or military. These temperature ranges are illustrated in Figure 45. Further, the level of reliability must be determined in terms of a standard device, a specially screened device, or a military standard 883 device.

And finally, not to be forgotten are those important specifications, price and delivery, to which the reputation of the manufacturer must be added.

AO20
A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing

The purpose of this application bulletin is to show that any competent engineer can design a complex data acquisition system as a series of manageable building blocks. It also explains the wide range of LSI devices that have recently become available, with moderate ad-mixtures of suitable MSI and SSI and discrete devices.

THE FUNDAMENTALS

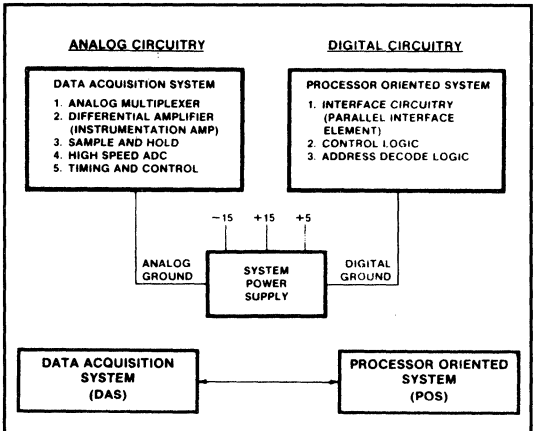


Figure 1: Basic Building Blocks of Data Acquisition System

The first thing to consider when designing a Data Acquisition System (DAS) to interface to a Processor Oriented System (POS), is to recognize the physical handicaps which arise when mating the two in the same surroundings. The two biggest influences on an unhappy relationship are the analog and digital ground routing in the DAS, and noise emissions from the POS. Since the DAS depends on the accuracy of voltage levels, it is imperative to maintain that accuracy within an environment of large digital ground currents and noise. Not only must care be taken when laying out the PC board, the analog section must be as isolated as possible from its digital neighbor. The isolation can be obtained by physical separation and lots of ground plane; both analog and digital.

The analog and digital ground routing should be two separate networks originating at the system power supply as one common ground. Figure 2 shows an example of an ideal grounding scheme for an analog and digital system. It is important to ensure that the analog ground path back to the system power supply contains little or no varying currents and at the same time is as physically short and hefty as possible. This is necessary in order to keep a constant analog ground reference throughout the entire system. The separation between analog and digital ground networks should not stop at the system bus but should continue on every card in the system. Clamping diodes may be installed between the two grounds on cards containing both analog and digital circuitry, to help prevent damage to circuitry in the event of accidental separation (excess potential difference) between the two grounds.

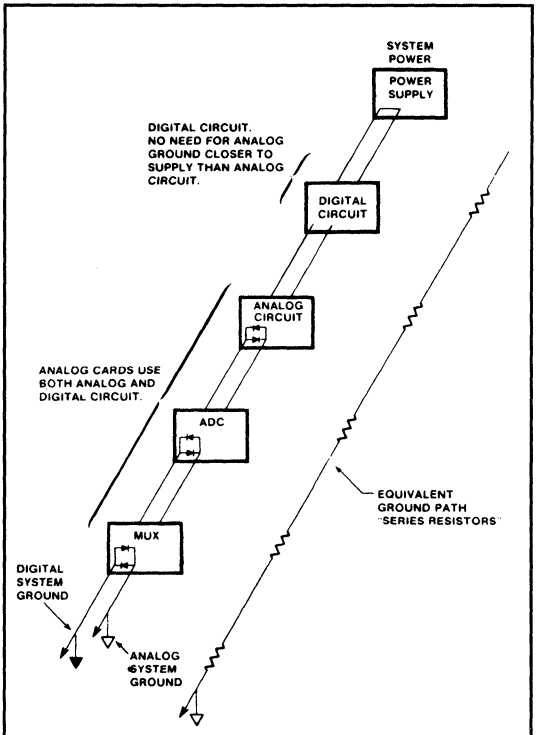


Figure 2: Ideal Grounding Scheme For An Analog and Digital System

HIGH SPEED DATA ACQUISITION — A BLOCK APPROACH

Figure 3 illustrates the basic building blocks which make up the Data Acquisition System (DAS). Starting with the input, an analog multiplexer is needed to direct the various channels of analog information to the analog to digital converter. Before reaching the A/D converter the analog inputs will usually require some sort of signal conditioning; the second block of the DAS (the differential amplifier) performs this function. The differential amplifier or instrumentation amplifier may be assigned the task of summing a pair of analog inputs together in a differential fashion with electrically programmable gain and filtering or may function as a non-inverting buffer stage for a single multiplexer channel. The complexity of this block will depend largely on the application and the types of inputs to be digitized. Once the input signal has been conditioned for the A/D converter, it may pass through a sample and hold amplifier before

reaching the A/D converter input. The sample and hold amplifier block is a prerequisite for the successive-approximation technique of Analog to Digital conversion. This is due to the nature of the conversion process, and will be discussed in more detail later.

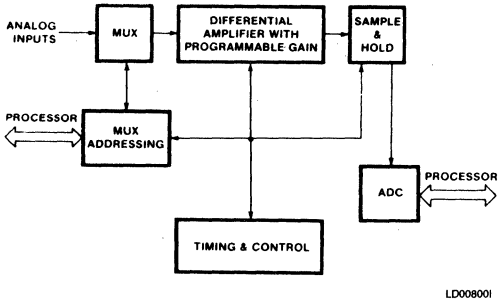


Figure 3: Functional Diagram — High Speed Data Acquisition System

The analog to digital converter is the heart of the DAS and its architecture is solely dependent on the through-put rate required. Although the successive-approximation approach is emphasized in this bulletin, greater resolution and accuracy may be obtained with the slower dual slope technique as this system block. The last block to be considered is the timing and control section. In any DAS system there is a definite order in which events should take place. To illustrate this point, consider the normal sequence of events following a start of conversion command in a DAS. First an input channel must be selected for digitizing at the analog multiplexer, and a programmed gain set up. Next, before a "hold" command is issued, a time delay must be initiated, to allow for the settling time of both the diff-amp and sample/hold amplifier. Finally, the A/D converter is strobed and the conversion complete signal is monitored until the end of conversion takes place. With the end of conversion comes the final digitized analog input value available at the output of the A/D converter in binary form.

PLACEMENT CONSIDERATIONS

When examining the architecture of the Data Acquisition System one may wonder why the system blocks are configured the way they are. It is readily apparent why the analog multiplexer is the input block and the A/D converter is the output block but what about the placement of the differential amplifier and the sample and hold amplifier? The answer to this question becomes apparent when studying the effect of the offset errors introduced by each block.

When considering the overall data acquisition function, the final offset trim can best be made by nulling the system offset error at the analog input of the A/D converter; this single offset adjustment requires that all offset errors introduced into the system prior to the A/D converter be constant with any gain setting of the differential amplifier. Since the multiplexer contributes no offset error and the sample and hold amplifier does, placing the sample and hold amplifier in front of the differential amplifier would cause the total offset error seen by the A/D converter to be a function of the gain setting in the differential amplifier block. Not only would this placement of the sample and hold amplifier require the DAS to have more than one offset adjustment, it would also require it to have two sample and hold amplifiers when the system is configured for differential measurements. Inserting the differential amplifier in front of the sample and hold and behind the multiplexer eliminates these problems.

MULTIPLEXER CONSIDERATIONS

When choosing an LSI device for the front end of a Data Acquisition System there are several inherent properties of the device which must be considered before the successful mating of its inputs with external circuitry can be achieved.

Input Impedance

The high input impedance of many analog multiplexing devices can be deceptive because of the dynamic properties that limit the maximum usable source impedance to a relatively low value. Figure 4 shows an impedance model for a typical IC multiplexer. At the bottom of Figure 4 is the equivalent circuit for an ON channel which consists of the ON-resistance of the channel, in series with a 35pF capacitor forming a low pass filter. This capacitance becomes an important consideration when determining the maximum usable source impedance of the data acquisition system. Since the through-put rate of the Data Acquisition System is dependent upon the individual settling times of each block, it is essential to keep the multiplexer settling time to a minimum.

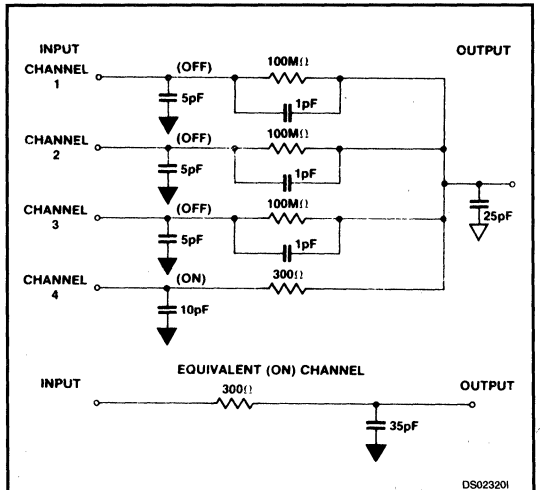


Figure 4: Analog Multiplexer Equivalent Circuit for Source Impedance Calculations

With a settling time of approximately five to eight micro seconds for the differential amplifier and sample and hold amplifier, it would be beneficial to keep the multiplexer's maximum settling time for any channel under one micro second. With this in mind, and using the model in Figure 4, the maximum usable source impedance can be calculated as follows.

Assuming the resolution and accuracy of the system to be 12 bits, a settling time of 9.2τ ($\tau = (R_{SOURCE} + r_{DS(ON)})C_{MUX}$) is required to settle an input signal to 1/2 of the least significant bit (LSB) or .01%. Therefore, with an output capacitance of 35pF and on ON resistance of 300Ω, the settling time is (9.2) (R_{SOURCE} + 300) (35×10^{-12}). Substituting 1 microsecond for the settling time and solving for R_{SOURCE}, the maximum usable source impedance is 2.9kΩ. A more exact determination of the maximum usable source impedance can be made by adding the capacitance of external components, particularly those of the sample-hold circuit, and printed circuit traces before making the calculation.

Leakage

A very influential contributor to the DC errors in the front end of a data acquisition system is the multiplexer leakage current over temperature. Even though at room temperature the leakage current may be only a few nano-amps, at 70°C it may increase to several micro-amps. This characteristic of the multiplexer must be considered when a wide temperature operating range is required of the data acquisition system.

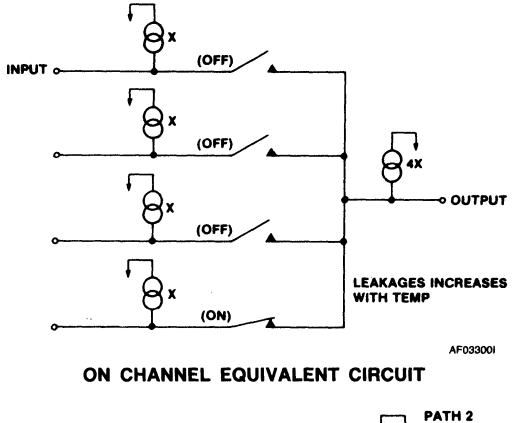


Figure 5: Analog Multiplexer Equivalent Circuit for Leakage Current Considerations

At the bottom of Figure 5 is a model of an ON channel of a multiplexer, for leakage current considerations. It can be seen that the leakage current has two paths to follow; either through the input or output of the multiplexer. This current, which is the sum of the individual channel leakages, will almost always flow through the input into the source impedance of the external circuitry. This is because of the high input impedance of the differential amplifier which follows the multiplexer. With the leakage current taking the path of least resistance into the source impedance at the multiplexer input, another error is introduced into the data acquisition function. This is an offset error, which varies with temperature and has a magnitude equal to the product of the leakage current and the source impedance. To illustrate the magnitude of this error, consider a 16 channel multiplexer whose selected channel has an input impedance of 3kΩ. Assuming the device is spec'd at 70°C to have 500nA of leakage per channel, the total leakage current would be 8μA. Now with 3kΩ at the input, the 8μA of leakage will introduce 24mV of offset error; equivalent to ten LSBs for a 12 bit system if the input range is 0–10 volts.

Since this characteristic of the analog multiplexer can contribute a significant offset error to the system over temperature, the multiplexer selection must be carefully made when considering overall system performance.

Latchup

Another consideration which must be made when selecting a multiplexer is whether or not the device will be subject to latchup. Latchup is an SCR type of action which the multiplexer may enter when one of the 15V power supplies powering the device, especially the +15V supply, falls below the selected channel's input level.

To illustrate this point, consider an OFF channel of a CMOS multiplexer (Figure 6). The input to this OFF channel is −10V, and the output is at +10V, probably held there by another ON channel. Now if the +15V supply were to drop below 9.3V for any reason, the SCR action would take place, freezing this channel ON. The input would then be effectively shorted to the multiplexer output and to the selected ON channel, not to mention the power supply. This is an undesirable condition which may occur at power on, during a power supply "glitch" or during momentary shut down of a power supply, etc. Not only is this an unhealthy mode for the multiplexer, but undoing it requires that all power to the device is turned off and then back on in the proper sequence. This means that when a multiplexer with this possible condition is selected for the front end of a DAS, special circuitry must be implemented to prevent the SCR action from taking place at power on or during power failure.

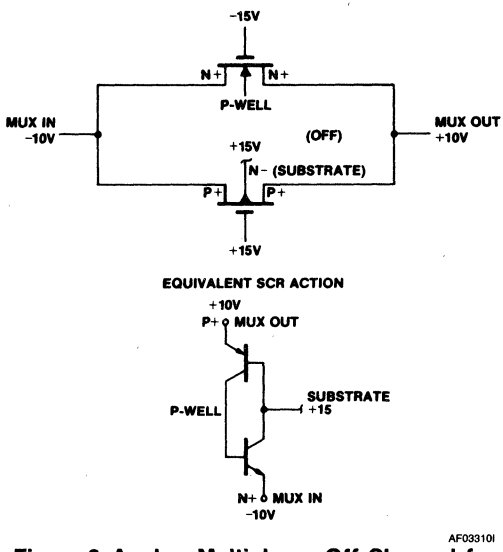


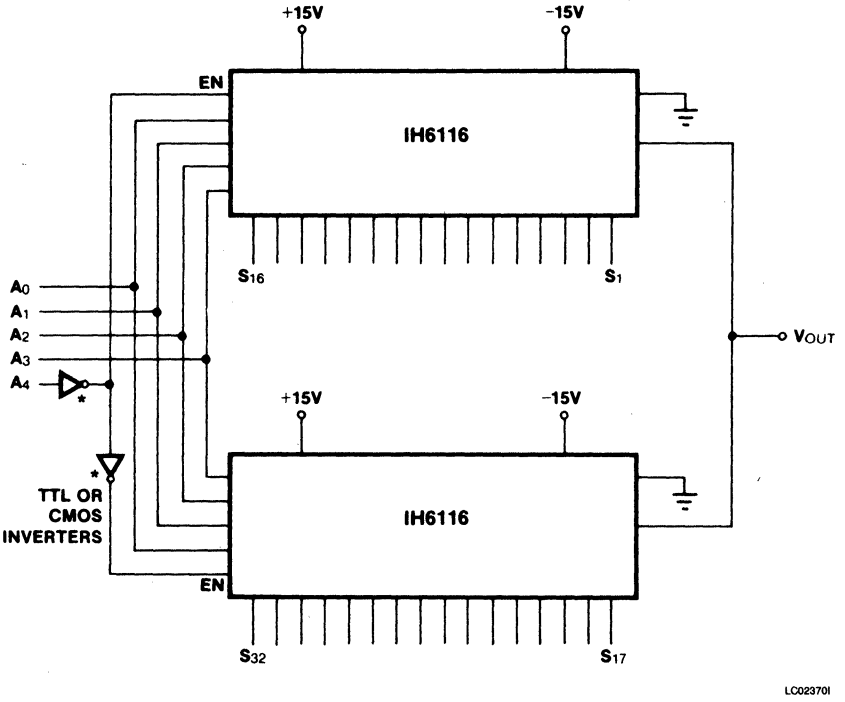
Figure 6: Analog Multiplexer Off Channel for Latchup Considerations

The best way to eliminate this problem is to select a device which has no latchup problems. See Intersil Application Bulletin A006 for a description of some latchup proof analog multiplexers and switches.

Cascading

As a general rule, the cascading of multiplexers is easily accomplished. (See Figure 7.) When the outputs of two multiplexers are connected together to form one larger multiplexer, the output capacitance and the leakage current doubles. If the DAS were originally tuned for maximum through-put rate and input source impedance with one multiplexer in the system, cascading two or more multiplexers in this fashion could degrade system performance drastically. This problem can be somewhat overcome by adding a third tier of submultiplexing, as shown in Figure 8. Both leakage current and output capacity are reduced significantly, however channel ON resistance and switching times are now increased. This increase is generally insignificant when compared to that of Figure 7, and will not usually hinder system throughput performance. The benefits obtained by submultiplexing in this way will substantially increase with the number of channels to be accessed.

1 OUT OF 32 CHANNEL MULTIPLEXER USING 2 IH6116'S



*TTL inverter must have resistor pullup to drive EN input.

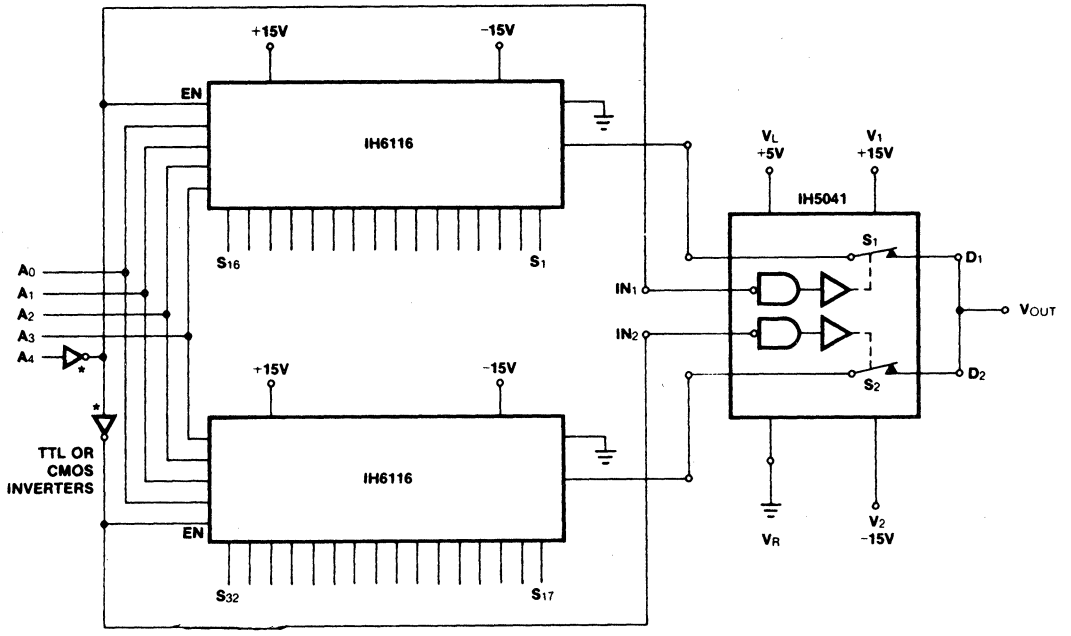
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 7: Easy Cascading Of Two Multiplexers Can Be Accomplished By Connecting In Parallel

1 OUT OF 32 CHANNEL MULTIPLEXER USING 2 IH6116S AND AN IH5041 FOR SUBMULTIPLEXER



*TTL gate must have resistor pullup to +5V to drive "EN" input.

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 8: Using Another Tier Of Submultiplexing To Reduce The Effects Of Output Capacitance and Leakage Current

Single Ended or Differential

The selection of either a single ended or differential multiplexer for the front end of the DAS is dependent upon the application. Since the 16 channel IC multiplexer is the basic building block, the designer must decide whether to go with 16 single ended or 8 dual differential inputs. The types of analog inputs to be digitized will dictate which type is used.

If the transducer circuitry to be monitored is far enough away from the DAS to allow excessive interference pickup on the return cable, the need for a shielded twisted pair and a differential front end becomes likely. With the differential front end, the common mode "noise" signal on the twisted pair will be rejected at the differential amplifier provided that its magnitude does not exceed the input voltage range of the DAS. If the magnitude of noise is greater than the input range, the signal to be digitized will be lost. There are several methods for overcoming this problem. First, the "noise" source could be eliminated; second, the cable length from the transducer to the DAS could be shortened; third, a very expensive high voltage differential amplifier could be used to buffer the multiplexer; finally, local conversion of transducer signals could be established to allow transmission of digital (serial) signals over long distance to the central processor instead of the low level analog signals produced by most transducers.

Even though the first and second solutions would eliminate the noise magnitude problems, implementing either of these two solutions would probably require the moving of some heavy piece of equipment away from the cable (a generator for example) or closer to the DAS (a smelting pot for example).

Therefore, a choice between solutions three and four must be made. After examining the cost for each solution, the local conversion technique is usually most viable.

THE DIFFERENTIAL AMPLIFIER

The differential amplifier becomes an essential part of the DAS when low level transducer signals must be recovered from noise. The complexity of this block may vary from a single op-amp buffer all the way to a software programmable signal conditioner for several different types of transducers (pressure, temperature, flow, etc.).

Before deciding on the configuration needed for a particular application, there are a few parameter prerequisites which must be met, no matter how simple or complex this block of the DAS is. First, the differential amplifier circuitry following the multiplexer must have a high input impedance. This is necessary to avoid the effects of the unpredictable multiplexer channel ON-resistance. This resistance, which varies with everything (voltage, current, temperature, etc.), must not be a part of the overall data acquisition function; in other words, if the resistance of the ON-channel were to double for some reason, there should be no noticeable change at the output of the differential amplifier. Next, the common mode rejection ratio of the differential amplifier should be better than 80db. This insures that for ±10 volts of common mode input noise only 1mV could slip through to the output. (Again, we are assuming a 12 bit system.) Another important factor, especially in DASs of 12 bits or more, is the stability of critical components over temperature. Maintaining 12 bits of absolute accuracy over any reasonable temperature range can be very expensive, and this aspect of the system's design must be thoroughly examined before specifying any critical components.

Programmable Gain Changing Provisions

The provision of programmable gain at the input stage of a DAS should be considered only after it has been determined that a single, optimum gain setting will not give satisfactory performance. Not only is it expensive to incorporate software programmable gain into a DAS, it almost always ends up being the greatest single source of errors within the system.

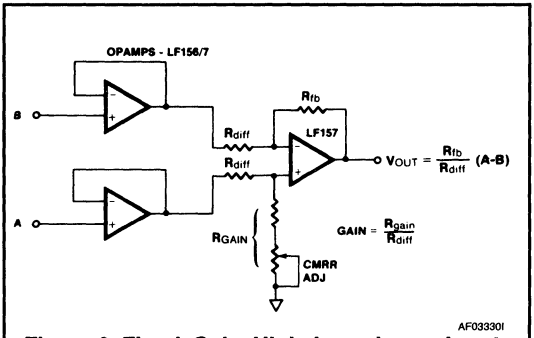
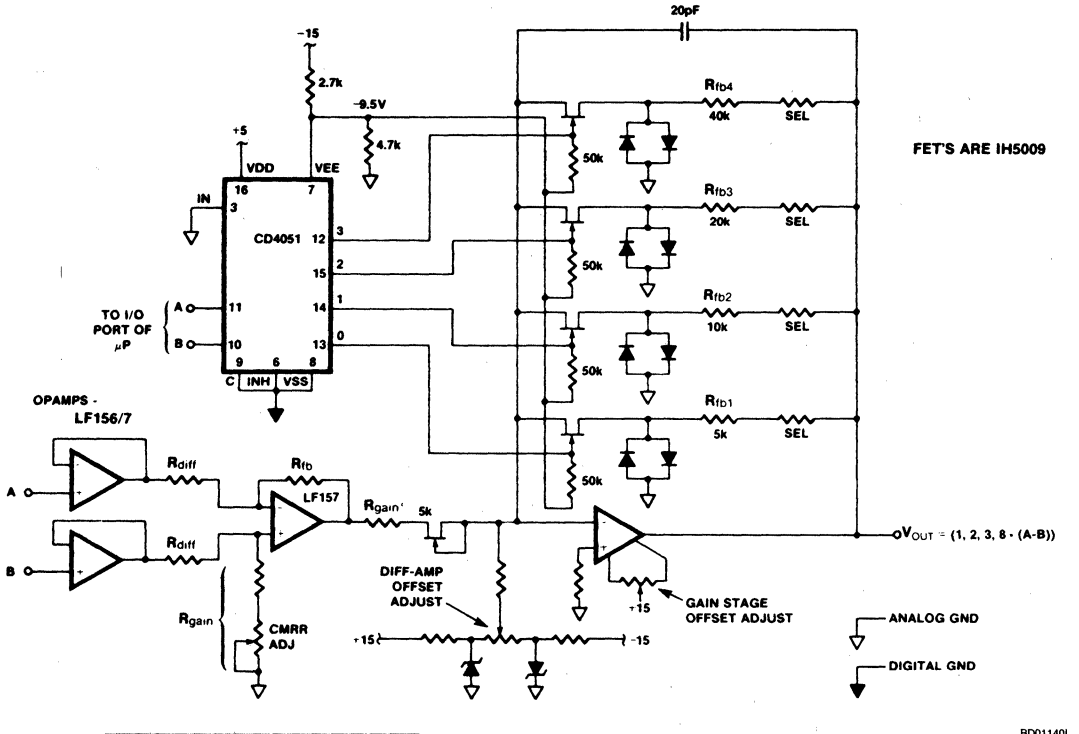


Figure 9: Fixed Gain High Impedance Input. Differential Amplifier with CMRR Fine Adjustment

Figure 9 shows all that is required for a fixed gain high input impedance differential amplifier; Figure 10 shows the same differential amplifier with the software programmable gain feature. The actual differential amplifier is made up of two LF156s, for input buffers, and one LF157 (better CMRR) for the differential stage. Since better than .005% ratio matching of the gain resistors would be needed to obtain a CMRR of 80db, a potentiometer is used for fine tuning the CMRR at low frequencies. The high frequency CMRR is dependent entirely on the op amp selected for the differential stage, and for the LF157 this is 90dB at 1kHz.



b	a	GAIN
0	0	X1
0	1	X2
1	0	X4
1	1	X8

Figure 10: Programmable Gain Differential Input Amplifier

Considering the difficulty in maintaining a high degree of common mode rejection, the addition of a programmable gain feature should not be included within the differential amplifier stage itself, but rather be a separate stage following the differential amplifier, as shown in Figure 10. This particular programmable gain circuit employs a CD4051 (CMOS Analog Multiplexer) as a two to four line decoder, with appropriate FET drive for switching between feedback resistors to program the gain to any one of four values. The problems associated with a circuit of this type are rather obvious. First, it was previously determined that one offset adjustment for the entire DAS would be advantageous. Not only does the programmable gain stage require offset adjustment, but both the offset of the gain op amp and the offset of the differential stage must be nulled. This is to prevent the offset error of the system up to this point from becoming a function of the programmed gain. Probably the biggest disadvantage in using a programmable gain stage is the initial calibration required; in addition to the two offset adjustments, there are four gain adjustments which must be carefully made by selecting FETs and feedback resistors. The calibration of this gain state is not only troublesome, but is also very time consuming and, for a high volume production environment, not very appealing.

SAMPLE AND HOLD AMPLIFIER

Successive approximation is the most popular technique for high speed analog to digital conversion. This technique requires that the analog input signal remain constant during the entire conversion process, and for this reason, a sample and hold amplifier is needed to buffer the successive approximation A/D converter. Like the other blocks of the DAS, the proper selection of sample and hold circuitry is necessary to insure maximum system performance.

Aperture Time

Aperture time is defined as the time required by the sample and hold to switch from a tracking mode into a hold mode, once a hold command is given. The aperture time is also the characteristic of the sample and hold circuitry which limits the maximum input frequency or slew rate for

which the DAS can accurately sample. For example, in a 12 bit system with a 10 volt full scale input range and an aperture time of 100ns, the maximum input slew rate would be 10mV/μs, or 300Hz (dV/dt = 2πVpk maximum slew rate of a sine function). This is due to the input changing more than 1/2 LSB after the command to sample is given, and before the sample is taken. Even though the aperture time limits the maximum input frequency for real time event recording (exact input value at t = Xμs after starting the event), higher frequency input may be sampled at system accuracies. Applications do exist where aperture time errors are not important, since the sampling of the input data is not referenced to a point in time. An example of this would be the recording of a high speed event (vibration analysis) for graphical analysis. The only requirement is that the sampled data be equally spaced with respect to time. If the aperture uncertainty (the difference in aperture time from sample to sample) is small in comparison to the aperture time, the aperture time is really nothing but a time delay from the time when the command to sample was given to the time when the actual sample was taken. Thus the aperture error can effectively be nulled by taking the sample one aperture time period before the time when it would normally have been taken.

Acquisition Time

This is defined as the time required for the sample and hold amplifier to slew and settle to the input signal when switched from hold to sample mode. Along with the settling time of the Differential Amplifier, the acquisition time of the sample and hold also effects the maximum throughput rate of the DAS. For this reason it is important to select a sample and hold amplifier with an acquisition time as low as possible ($\leq 5\mu$s). If the sample and hold amplifier to be used is an IC type, the input step magnitude for which the acquisition time is specified should conform to the input requirements of the sample and hold block. Figure 11 shows the various relationships between the acquisition time and the other parameters of the sample and hold amplifier.

Feed Through

When the Sample and Hold Amplifier is in the hold mode, the amount of input voltage change seen at the output is considered the feed through. Feed through is caused by the stray capacitance from the analog input of the sample and hold to the top of the sampling capacitor (across the input switch; see Figure 11). This capacitance forms a capacitive voltage divider with the sampling capacitor, and allows a fraction of the input signal to feed through to the output when the input switch is open and the sample and hold is in the hold mode. The effect of the stray capacitance can be minimized by careful printed circuit layout and by selecting a larger value of sampling capacitor, however tradeoffs between the amount of feed through and the acquisition time may have to be made when selecting the sampling capacitor, because of the change in the AC characteristics of the sample and hold circuitry.

Charge Injection

Charge injection results in an error to the sampled value when switching from the sample mode to the hold mode. A voltage step is created on the sampling capacitor by the charge injected through the capacitance between the gate of the input switch and the sampling capacitor (see Figure 11). Circuit board strays may also contribute to this capacitance. Again this effect may be minimized by careful printed circuit layout and a larger value of sampling capacitor. However, although the charge injected causes a voltage step on the sampling capacitor, and therefore is a source of error, the fact that it is relatively constant in magnitude means that it can be nulled as a system offset if not too severe.

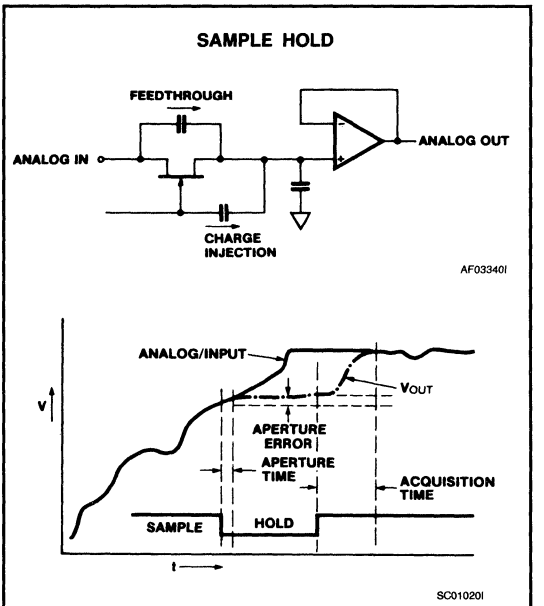


Figure 11: Properties of the Sample and Hold Displayed Graphically

Droop Rate

Droop Rate is the rate at which the sampled voltage decays at the output of the sample and hold amplifier during the hold mode. The rate of decay is proportional to the sum of the sample and hold leakage and bias currents which may either charge or discharge the sampling capacitor during the hold period. To calculate the maximum droop rate simply divide 1/10 LSB of the A/D converter's lowest input range by its conversion time. This will result in a maximum value of droop rate, and at the same time not produce any significant error which could degradate system accuracy.

ANALOG TO DIGITAL CONVERTER

The successive approximation technique of analog to digital conversion is by far the most popular technique for high speed, high accuracy, microprocessor compatible analog to digital converters. Conversion times as low as two microseconds with twelve bits of resolution and accuracy are obtainable.

Figure 12 shows a block diagram of the successive approximation analog to digital converter (ADC). The basic ADC loop consists of a successive approximation register (SAR), a current output digital to analog converter (DAC) and a comparator. To initiate a conversion, the start conversion input is pulsed and the conversion sequence

begins. The SAR initially sets up one "0" and the rest "1's" on its outputs, equivalent to half-scale minus a least significant bit (LSB). Assuming unipolar operation, the digitizing of the analog input signal proceeds as follows. The initial setting of the SAR outputs programs the DAC to half-scale minus an LSB, and that value of current flows into the DAC. The magnitude of the input will determine the polarity of the comparator output, greater than half scale being positive. This in turn signals the SAR to make a decision on the most significant bit (MSB) with the arrival of the first pulse from the system clock. On the rising edge of the first clock pulse the SAR programs the MSB to its final value, and at the same time sets the second bit to a logic low. This allows the SAR to make a decision on the second bit, and set up for the third bit on the rising edge of the second clock pulse. This process will continue in descending bit order until the LSB has been programmed. At that time the conversion complete signal will change states, signifying an end of conversion, with the final digitized input remaining latched at the outputs of the SAR.

ADC DESIGN

The two primary factors which control the complexity of the ADC design are accuracy and speed. The accuracy specification directly specifies the resolution (accuracy) required of the ADC, however the throughput rate does not directly specify the speed. To calculate the conversion time required, subtract from the inverse of the throughput rate (in hertz) the sum of the settling times of all blocks up to the ADC. For example, assume that the throughput requirement for a DAS is 30 kilo-samples per second. If the multiplexer, differential amplifier and sample and hold amplifier have a combined settling time of 8 microseconds, the ADC would have to convert in 25 microseconds or less to maintain the 30 kilohertz throughout rate. It turns out that the design of 12 bit or less converters with conversion times greater than 25 microseconds is relatively easy. However, as the conversion time drops below 20 microseconds, the difficulty of design seems to increase, somewhat exponentially.

Loop Speed

Several things limit minimum conversion times. Looking at Figure 12, the slowest point in the loop is the node where the DAC output, comparator input and analog input join together. To understand why this is so, it is necessary to remember what is happening at this node during the conversion process. During a conversion, the SAR programs the DAC output current in an attempt to equal the current through the input resistor, by the time the conversion ends. While the successive approximation process is taking place, the difference between the two currents (which will vary in magnitude throughout the conversion) will charge the nodal capacitance which drives the comparator's output to the proper polarity to signal the SAR. The comparator's speed problem (due to lack of overdrive) evolves when this current difference is very small (LSB levels), and insufficient time is available before the next clock pulse for the nodal capacitance to charge to a voltage large enough to switch the comparator.

The inadequate overdrive results in a conversion error. The use of a high speed comparator and a high current DAC will help eliminate this problem, which is quite severe in sub 20μs converters.

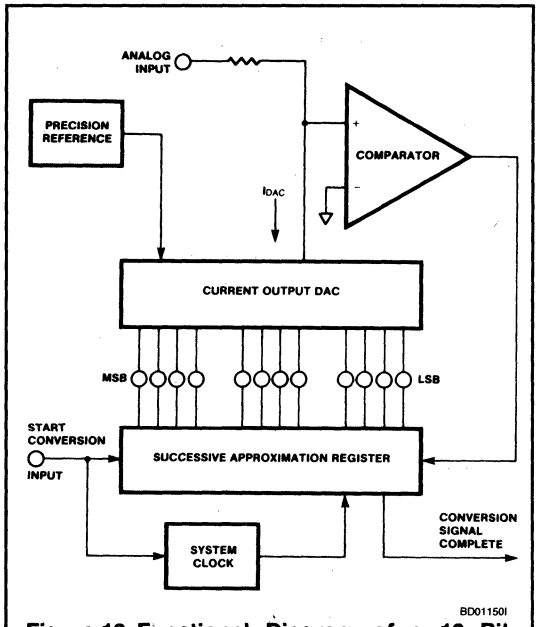


Figure 12: Functional Diagram of a 12 Bit Successive Approximation Analog to Digital Converter

The Comparator

The loop comparator must be able to switch fast with very little overdrive. A very fast comparator is the National Semiconductor LM361, with a switching time of typically 14ns with 5mV of overdrive. Not only is it fast, it is also very expensive; however, for sub 20μs conversion times such speed is a must. Figure 13 shows a comparator scheme using an LM301 op-amp in a feed forward configuration, combined with an LM311 comparator to bring high speed at low cost. This particular comparator, along with a fast settling current output DAC, will provide 12 bit analog to digital conversion with conversion times as low as 25μs.

Probably the most difficult aspect of using a high speed comparator in a successive approximation loop is the problem of maintaining frequency stability while operating within the linear region of the comparator (when very low overdrive is present at comparator inputs). Since the comparator is operating at a high gain-band-width with minimal feedback compensation, even small amounts of parasitic feedback will cause oscillations. To avoid this, careful PC layout must be observed. Lots of analog and digital ground planes and extensive bypassing of the supplies is recommended. Comparator output to input isolation, along with analog and digital signal isolation, should also be considered during PC layout. It is also a wise idea to buffer the load driven by the comparator output with a discrete transistor, thereby eliminating thermal feedback effects which could cause instability.

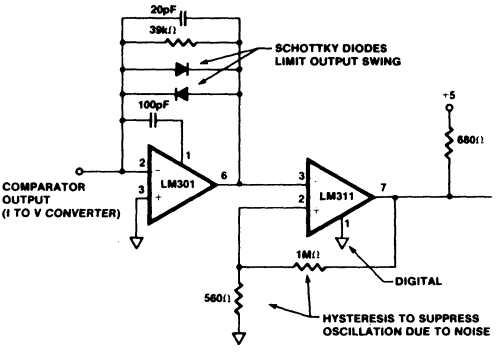


Figure 13: Cheap High Speed Comparator

The Digital to Analog Converter

The DAC within the system ADC is the one element of the entire DAS which is most responsible for maintaining overall system accuracy. The DAC, therefore, must not only be fast settling, but it must also be linear, monotonic and stable over temperature.

What type of DAC should be used in the system ADC? Again it depends on the DAS throughput requirements. For sub 25μs conversion times, the author recommends a multiple IC high current DAC (see A010 for such a device) along with a high speed comparator like the LM361. However, for conversion times greater than 25μs the system DAC can be implemented very easily with a monolithic current output type device. The Intersil AD7541 is an excellent example of a laser trimmed monolithic multiplying current output DAC with true 12-bit accuracy and resolution. Once the monolithic DAC is selected, all that is usually required to make it play is power and a reference. The reference must be added externally to get the required temperature stability, since on board monolithic references are generally very poor in this regard. The most widely used reference device is a temperature compensated zener diode along with an op-amp for gain buffering.

Successive Approximation Logic

Figure 14 shows how to combine a standard TTL 7400 quad-NAND gate with a 12-bit successive-approximation register to obtain all the necessary logic to support a 12-bit A/D converter. NAND gates B, C, and D form an oscillator circuit, controlled by the SAR signals, start (S) and conversion complete (CC). The Start Conversion input requires a positive pulse, buffered and inverted by gate A. On the positive transition of this pulse, gate C will provide the CP input of the SAR with a positive transition. This initializes the SAR by setting the CC output (conversion complete) signal to a logic one state, and the bit outputs to a condition of one zero and the rest ones, the MSB being equal to zero. The RC delay between the output of gate A and the input of gate C insures that the S input will have the necessary set up time before the CP input is clocked by the rising edge of the start conversion pulse. As soon as the start conversion input pulse returns to a logic low the conversion will begin. It is important to note the conversion complete signal (CC) represents the conversion time of the ADC plus the pulse width of the start conversion input pulse. Once the conversion process starts, gates B, C and D will provide the SAR with a series of clock pulses at a frequency set by the clock timing capacitor. The hysteresis effect of the 200Ω and 2kΩ resistors around gates C and D help provide a fast, clean clock for the CP input of the SAR. As soon as the twelfth clock pulse strobes the CP input, the SAR responds by making a decision on the twelfth bit and resetting the CC signal to a logic low signifying an end of conversion.

A serial form of the conversion is also available at the serial data output (DO). Used along with a delayed clock signal as a strobe, this output feature provides one means of transmitting the digitized analog input signal over long distances with only three wires.

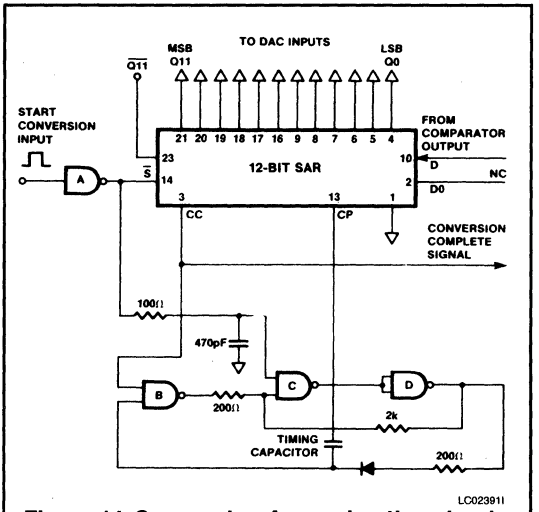


Figure 14: Successive-Approximation Logic for A 12 Bit Analog to Digital Converter

Other Considerations

The A/D converter can be set up to operate in any one of many input range configurations. The three most popular are Straight Binary, Offset Binary and Twos-Complement Binary. Straight Binary is the unipolar input range, for which inputs of zero and full scale volts result in output codes of all zeros and all ones respectively. Figure 12 shows the Straight Binary configuration where the value of the input resistor is selected to produce the desired input range with respect to the full scale current of the DAC. Offset Binary can be obtained from the Straight Binary configuration of Figure 12 by adding half scale current to the summing input of the comparator in the form of a current source or a resistor to a positive reference. The only difference between Offset Binary and Straight Binary is a negative shift in the input range of half scale volts. This input shift, or offset, allows both positive and negative inputs to be digitized (Bipolar input range). An input voltage of minus full scale results in an output code of all zeros and plus full scale results in all ones. Twos-complement Binary is almost identical to Offset Binary, the only difference being the Twos-complement code has an inverted MSB. To obtain a

twos-complement operation from Figure 12, set up for the offset binary configuration as previously described then read the digital output using an inverted MSB. The AM2504 successive-approximation register makes this easy by providing both MSB polarities. The MSB (pin 21) must be connected to the DAC for the successive-approximation process to work but, for twos-complemented Binary, "$\overline{\text{MSB}}$" is read as the most significant bit of the digital output word.

An interesting feature of the AM2504 SAR is the ease with which it can be short-cycled. Short cycling of the SAR is the process of reducing both the resolution and conversion time of the ADC by using the new LSB + 1 bit as conversion complete signal for the SAR logic, instead of the CC output of the SAR. This permits the original 12-bit DAS to operate at a much higher throughput rate, albeit with less resolution. In many instances, not all of the DAS transducer inputs will require the 12 bits of resolution and accuracy available, and when this is the case the throughput rate can be optimized by software control of the ADC resolution and clock frequency. During the conversion process the 12-bit ADC requires the comparator input to settle in ten time constants (1/2 LSB), which is equal in time to one period of the ADC's clock (assuming the clock is set to a maximum frequency while still maintaining 12-bits of accuracy). Short cycling the 12-bit converter to 8-bits would decrease the minimum conversion time by 58%, since only 6.2 time constants are now required for the comparators input to settle to .2% or 1/2 LSB at 8-bits ($8 \times 6.2\tau$ instead of $12 \times 10\tau$).

ANALOG SECTION AS A WHOLE

Figure 15 shows the complete analog section of a 12-bit, binary, 2's complement DAS with the timing and control necessary to interface the analog components to each other and to a microprocessor.

The front end of the DAS is configured differentially using a dual eight input IC multiplexer (IH6216) and three LM156 op-amps. Following the differential amplifier is the programmable gain stage discussed earlier, with a low pass filter on the output feeding the IH5110 sample and hold amplifier. The output of the IH5110 is connected to the comparator input (– input LM301) through the internal 10K feedback resistor of the 7541 multiplying D/A converter. The AD7541, along with a ±10 Volt reference and successive approximation logic, make up the 2's complement A/D converter.

A conversion is initiated by programming the multiplexer and programmable gain stage before strobing the 74123 dual one-shot. This can be accomplished by simply outputting one word to the port of the microprocessor which is responsible for the control of the DAS. The time delay created by the 74123 allows the front end of the DAS to settle before the strobing of the A/D converter; this time delay can also be implemented in software, thus eliminating the need for the 74123. As soon as the A/D converter is strobed, the conversion complete signal (busy signal) of the AM2504 SAR commands the IH5110 sample and hold amplifier to enter the HOLD mode and the actual conversion process begins. The microprocessor, after allowing for the set up time of the conversion complete signal (settling time incorporated by the 74123), should monitor the conversion complete signal for the end of conversion. This can also be monitored using the microprocessor's interrupt facilities. With the end of conversion, the digitized analog input signal is available for the microprocessor to input by tri-stating the outputs of the AM2504 SAR onto the microprocessor's bus.

MICROPROCESSOR INTERFACING

Figure 16 shows a method for interfacing the DAS to a microprocessor. There are three basic building blocks which make up the parallel interface. They are the data bus buffers, address decode logic and handshake and control circuitry. In order for the microprocessor to communicate effectively with the DAS, these three blocks are always needed, and may be implemented by merely using a single LSI parallel interface element (provided by each microprocessor manufacturer) or by using several MSI discrete logic packages. No matter which way is chosen, the interfacing is relatively easy, assuming there is some prior knowledge of the microprocessor to be interfaced. Figure 17 shows a block diagram of the DAS to 8080 CPU interface.

Data Bus Buffering

The characteristic which is responsible for the dynamic flow of data into and out of the microprocessor also requires that its data bus be buffered for both directions of data flow to and from external devices. This means that an external device must latch data from the bus at the appropriate time, and enable data to the bus at the appropriate time. The use of Three-State buffers for enabling data onto the bus, and D-type latches for removing data from the bus, permit this type of data transfer if their respective enable and clock control lines are activated at the right times by the handshake and control circuitry. Depending on the type of logic used in the microprocessor system and the number of loads on the bus, the logic family to be used in the DAS interface can be determined. Figure 18 shows the first part of the design of a discrete logic interface between the DAS and the Intel 8080 microprocessor. In the upper right hand corner of the figure are the two sets of octal three-state buffers and the octal latch used by the CPU to obtain communication with the DAS through the bidirectional data bus, DB0–DB7. The CPU executes a data transfer by supplying the hand shake and control circuitry of the interface with the proper signals to allow the selected buffer or latch to be enabled.

Examples of three-state buffers include the TTL 80T9X and 74LS36X series and the CMOS 80C9X series; all have six buffers per package in different polarities and three-state configurations. Also available are 8-bit CMOS latch/buffers 74C373 and 74C374 which are very attractive for 8-bit CMOS applications, and the 74LS374 for heavier loads.

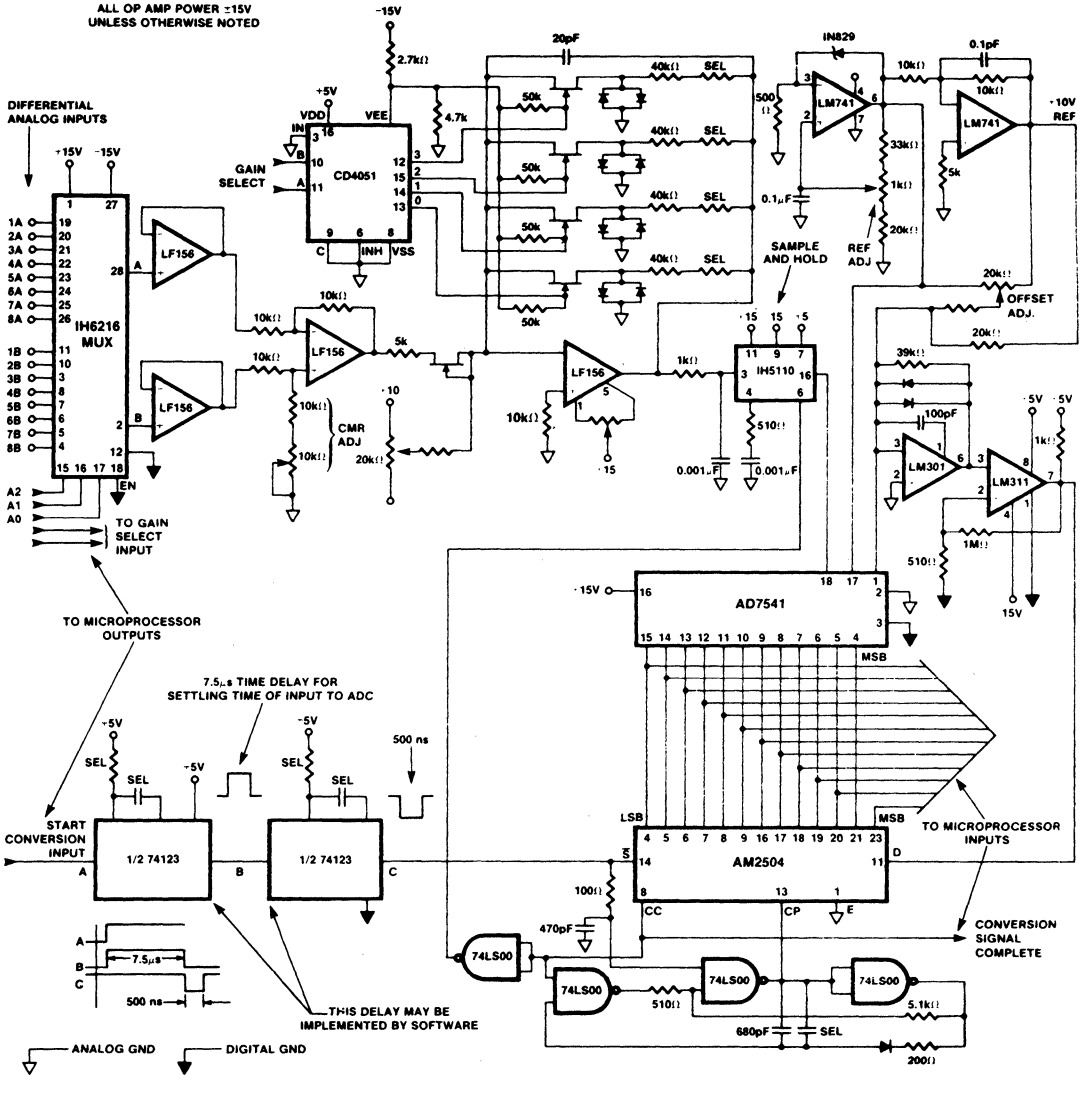


Figure 15: Complete A/D Conversion System

Address Decoding

In a control system environment, where many processes are being controlled using a single microprocessor as the controller, the requirements of the system are such that the microprocessor must communicate with several different I/O devices over the same data lines. When interfacing hardware to a data bus with this type of structure, the microprocessor must have the ability to enable, or "address", a specific I/O device for data transfer through the bus. This brings about the need for address decoding hardware at the interface itself. The type and quantity of circuitry used for this task depends primarily on the architecture of the overall system. Since the addressing capabilities of the microprocessor may overwhelmingly exceed the actual number of unique addresses used within a system, the amount of discrete logic necessary for address decoding at each interface may be kept to a minimum by initially allocating only the number of microprocessor address lines

which are actually needed to satisfy the system's I/O requirements.

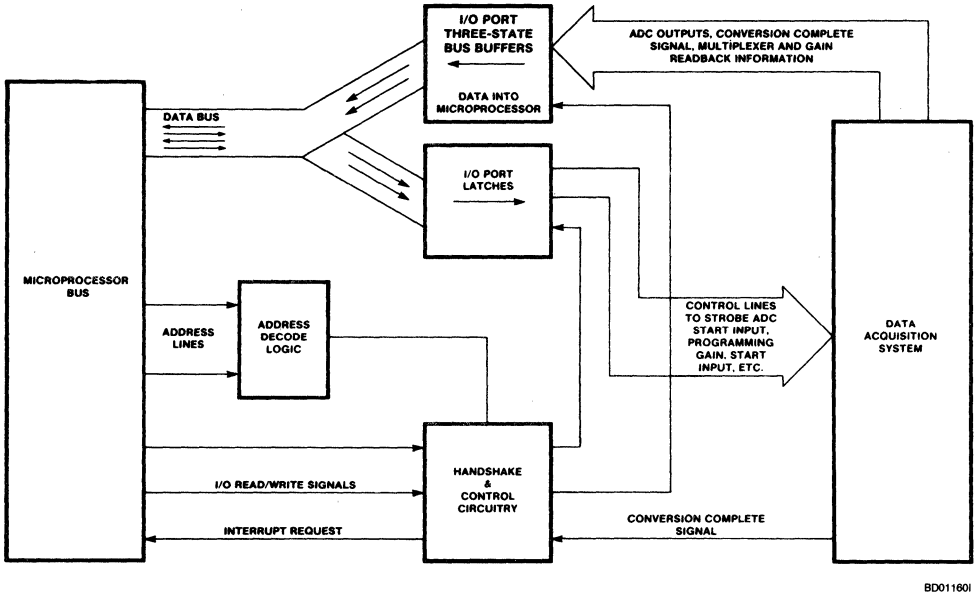


Figure 16: Functional Diagram Multiprocessor to Data Acquisition

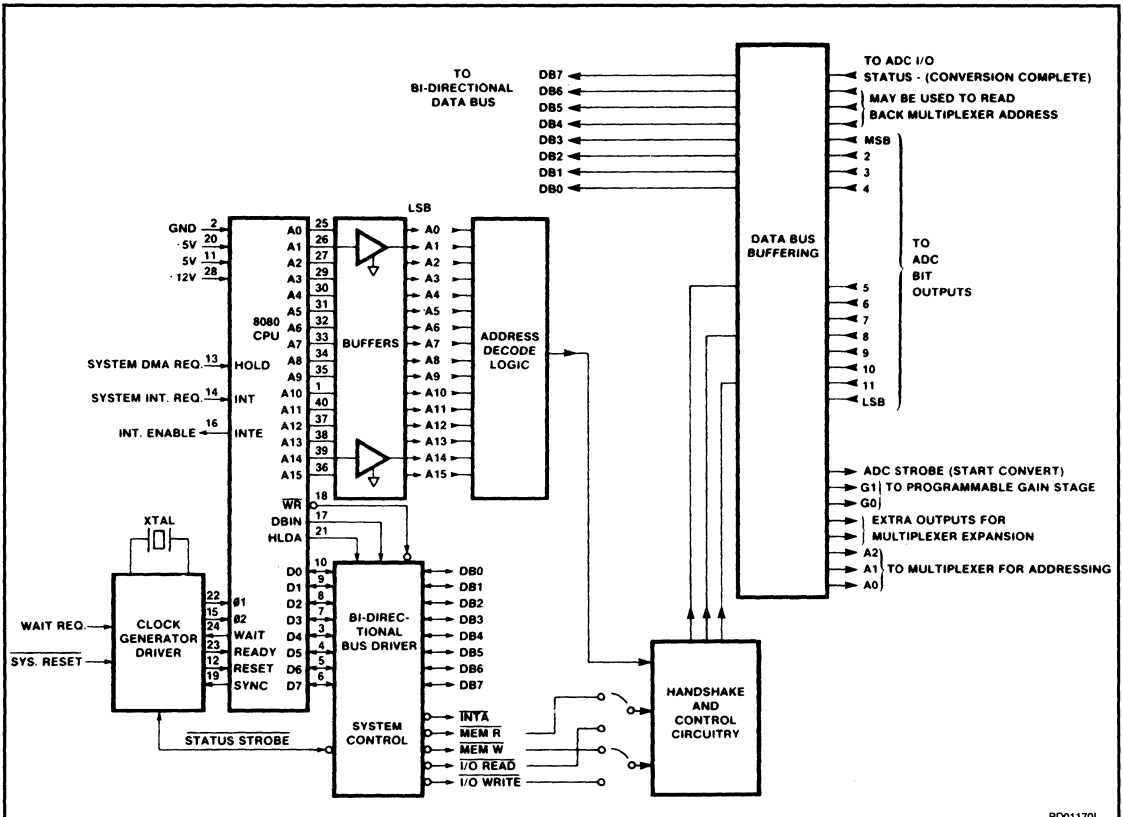


Figure 17: Functional Diagram for Interface Of DAS to 8080 CPU

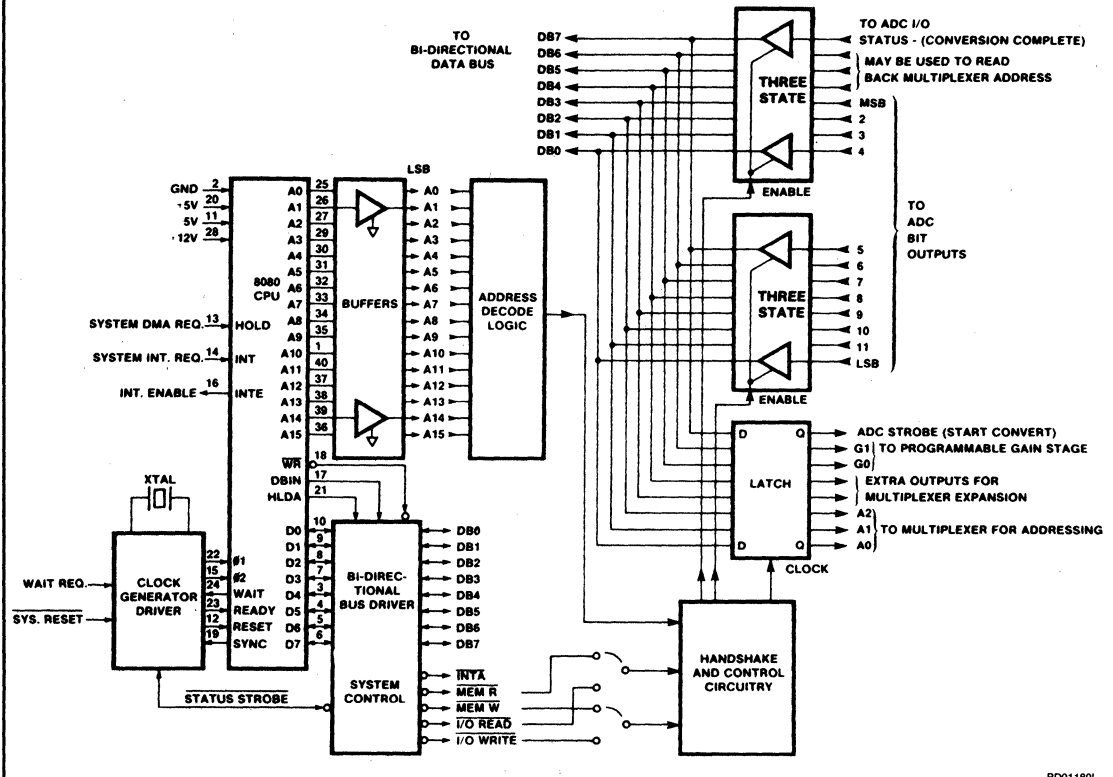


Figure 18: DAS to 8080 Interface Showing Circuitry Necessary

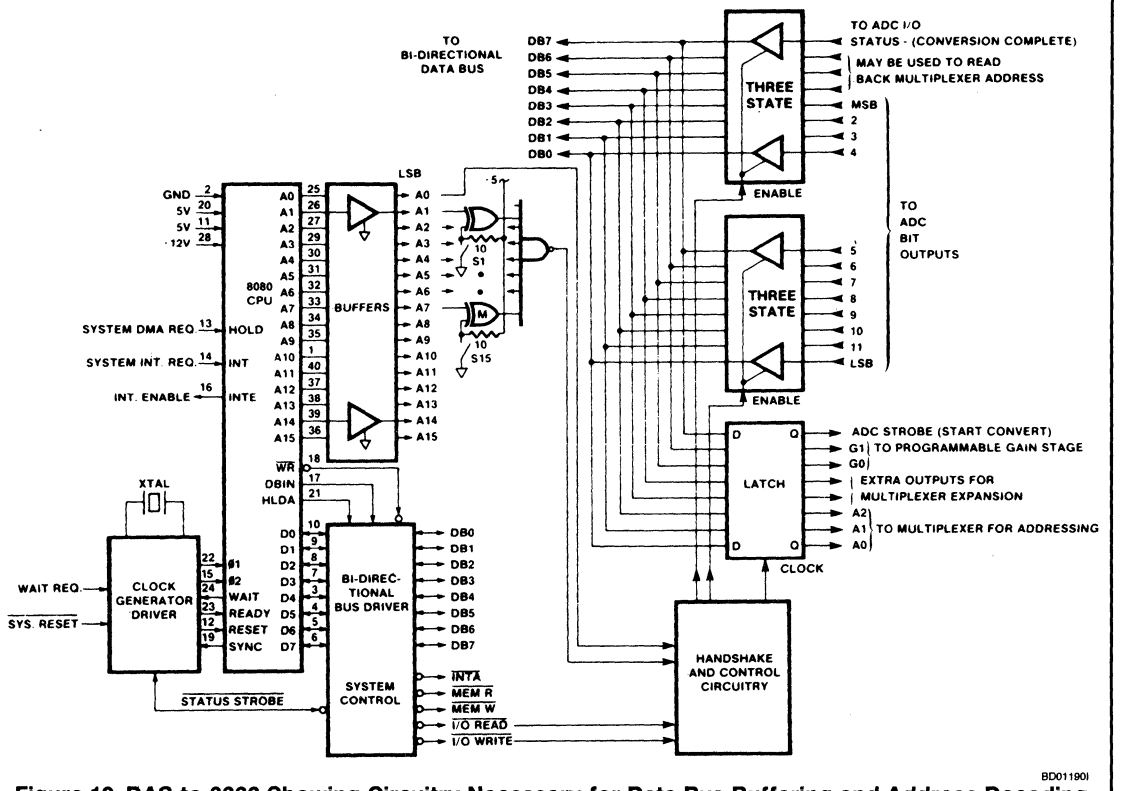


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Figure 19: DAS to 8080 Showing Circuitry Necessary for Data Bus Buffering and Address Decoding for Programmed I/O

There are basically two techniques for I/O addressing: Programmed I/O and memory mapped I/O. Programmed I/O refers to specific instructions and microprocessor signals set aside by the manufacturer for the special purpose of communicating with I/O devices. The Intel 8080, for example, has an input and output instruction which uses the eight lower address lines (A0–A7), together with two special read ($\overline{I/OR}$) or write ($\overline{I/OW}$) signals to control all I/O access to the CPU. Figure 19 illustrates this type of address decoding, which uses exclusive-OR logic to buffer the address lines into an eight input NAND gate. The exclusive-OR gates can be programmed for polarity (inverting or noninverting), thus allowing for jumper selectable addressing of the particular device onto the microprocessor data bus. It is important to note that the two signals which control the read ($\overline{I/OR}$) and write ($\overline{I/OW}$) operations from the microprocessor are active only during the execution of either the input or output instructions of the 8080 instruction set. Thus the memory addressing capabilities of the microprocessor are not affected since the memory read/write control is activated by two completely different control signals: Memory Read ($\overline{MEMR}$) and Memory Write ($\overline{MEMW}$). In memory mapped I/O, this is not the case. The same control lines used to control memory access, (again $\overline{MEMR}$) and ($\overline{MEMW}$), are also used to control the I/O transfer, see Figure 20. The address decoding shown here is an extension of the previously described decoding of Figure 19, the only difference being the number of address lines decoded. The extra address lines are needed because the I/O address now looks like a memory address to the CPU, and with the normal microprocessor memory mapped in the lower addresses of the usable addressing range the I/O addresses are partitioned above the memory, starting at a point greater than the highest memory address. The benefits of memory mapped I/O over programmed I/O are realized when considering the software required to access the I/O device under each configuration. When using programmed I/O there are only two instructions available to access the device, while memory mapped I/O makes available all of the memory reference instructions. With the 8080 CPU this means that two 8-bit ports, or both 8-bit words forming the ADC and control information may be read directly into the H and L registers using the single LHLD instruction. The significance of this feature is obvious: software I/O transfers can be made faster and more efficiently, and operations such as incrementing a multiplexer address can be accomplished directly with one instruction, rather than the three or four required in programmed I/O. The key to this efficiency is the fact that data to and from the I/O device does not have to pass through the

accumulator when communicating with the I/O device, as it does in programmed I/O.

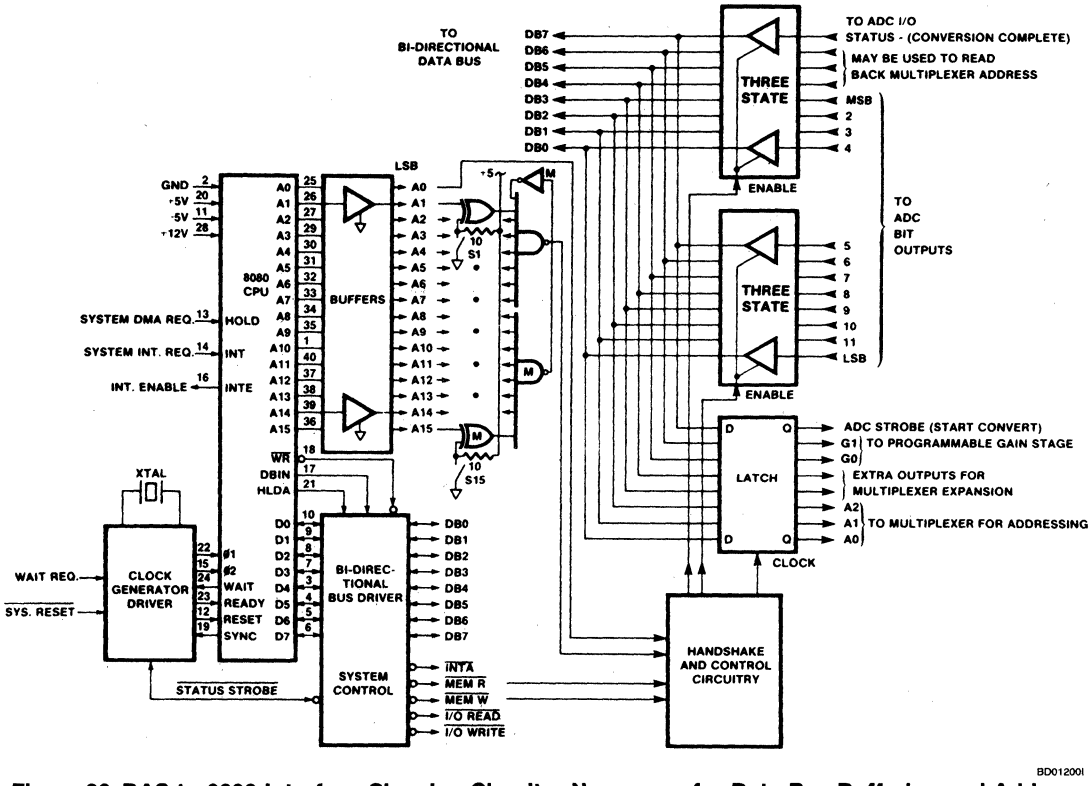


Figure 20: DAS to 8080 Interface Showing Circuitry Necessary for Data Bus Buffering and Address Decoding for Memory Mapped I/O

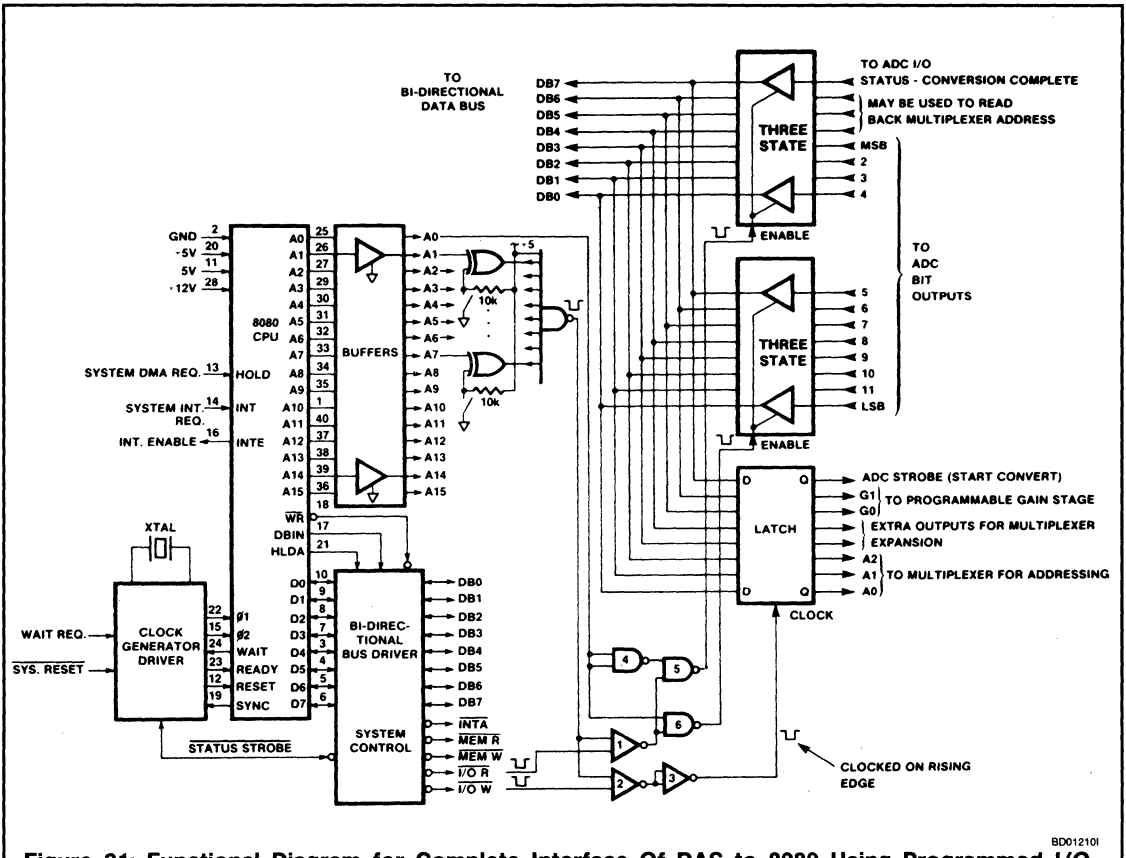


Figure 21: Functional Diagram for Complete Interface Of DAS to 8080 Using Programmed I/O

Handshake and Control Circuitry

The handshake and control circuitry is shown in Figures 21 and 22 for both the programmed I/O interface (Figure 21) and the memory mapped I/O interface (Figure 22). The circuitry required for the handshake and control block consists of only a few gates and is identical for either interface. NOR gates 1 and 2 are fed by the two read/write signals $\overline{I/OR}$ and $\overline{I/OW}$ for the programmed I/O interface, and $\overline{MEMR}$ and $\overline{MEMW}$ for the memory mapped I/O interface. They enable either a write into the latch, or a read from one of the three-state buffer groups, but only if the output of the address decode circuitry is enabled, or gate D's output is at a logic low level. During a read instruction, the selected interface, via the A0 address line, will select the three-state group controlled by gate 6 (if A0 = high level) to enable data onto the data bus. The use of the least significant address lines for control (in this case A0) provides an easy way to select between multiple ports on the same interface.

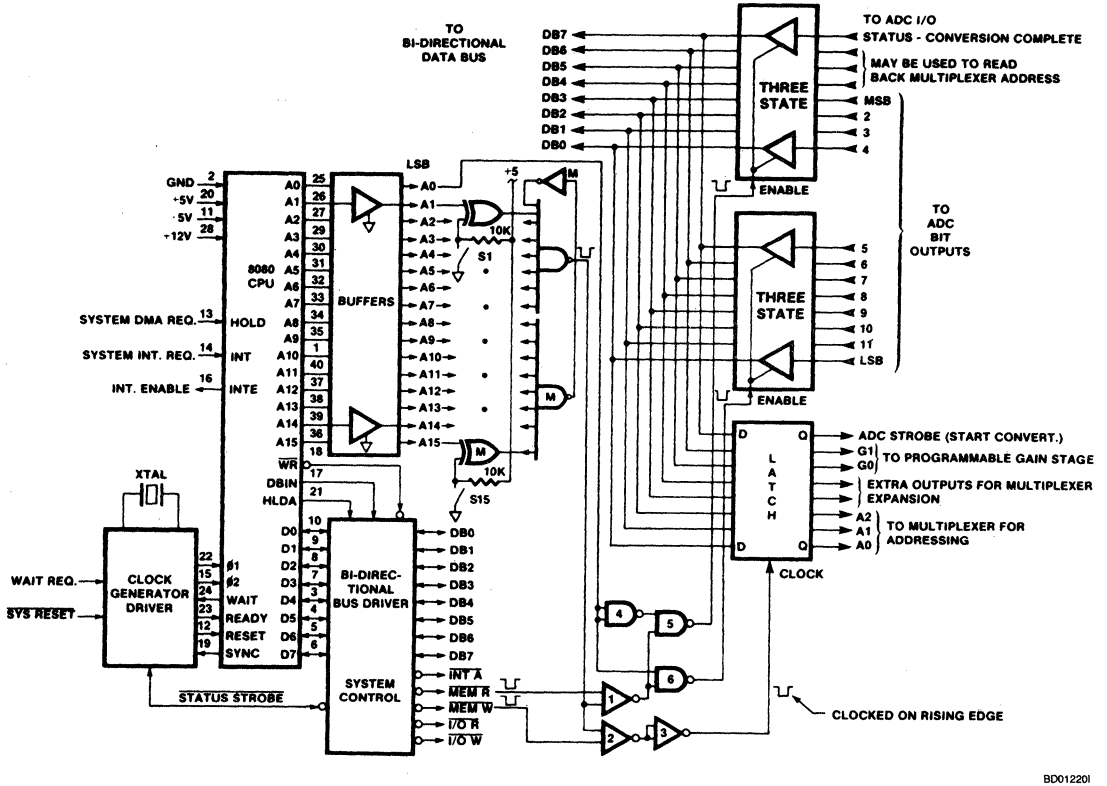


Figure 22: Functional Diagram for Complete Interface Of DAS to 8080 Using Memory Mapped I/O

Interrupts

Figure 23 shows the previously described Programmed I/O Interface with the necessary circuitry for an interrupt driven interface. As shown, only one interface to the microprocessor can be interrupt driven in a system that may have several I/O devices processing data. Figure 23 shows the Q output of the interrupt latch being tied directly to the interrupt request input (INT) of the 8080. As soon as the STATUS signal makes the transition to a logic one (positive transition), signifying an end of conversion of the DAS's ADC, the Q output of the interrupt latch is clocked high. This immediately generates an interrupt request at the 8080 INT input, and assuming that the microprocessor strobed the ADC some time ago and is now currently executing an instruction for some other routine in memory, program execution will jump to the interrupt service routine for the interrupting device at the end of the current instruction execution.

Usually the interrupt service routine is set up to service a device when the CPU cannot afford to spend the time monitoring the device's data ready flags. The service routine for the interface in Figure 23 should include reading the status information and most significant ADC MSBs via gate 5 and will thus clear the interrupt request to the 8080 before the interrupt service routine is over. This is important because if the interrupt request is not removed before a return to normal program execution occurs, the interrupt service routine will be immediately re-entered.

When configuring a system with several interrupt driven interfaces, there is a need for additional hardware between the interrupt latch output of the interface and the interrupt request input of the 8080. The multiple interrupt hardware is generally never located on a single device interface, and is beyond the scope of this application note.

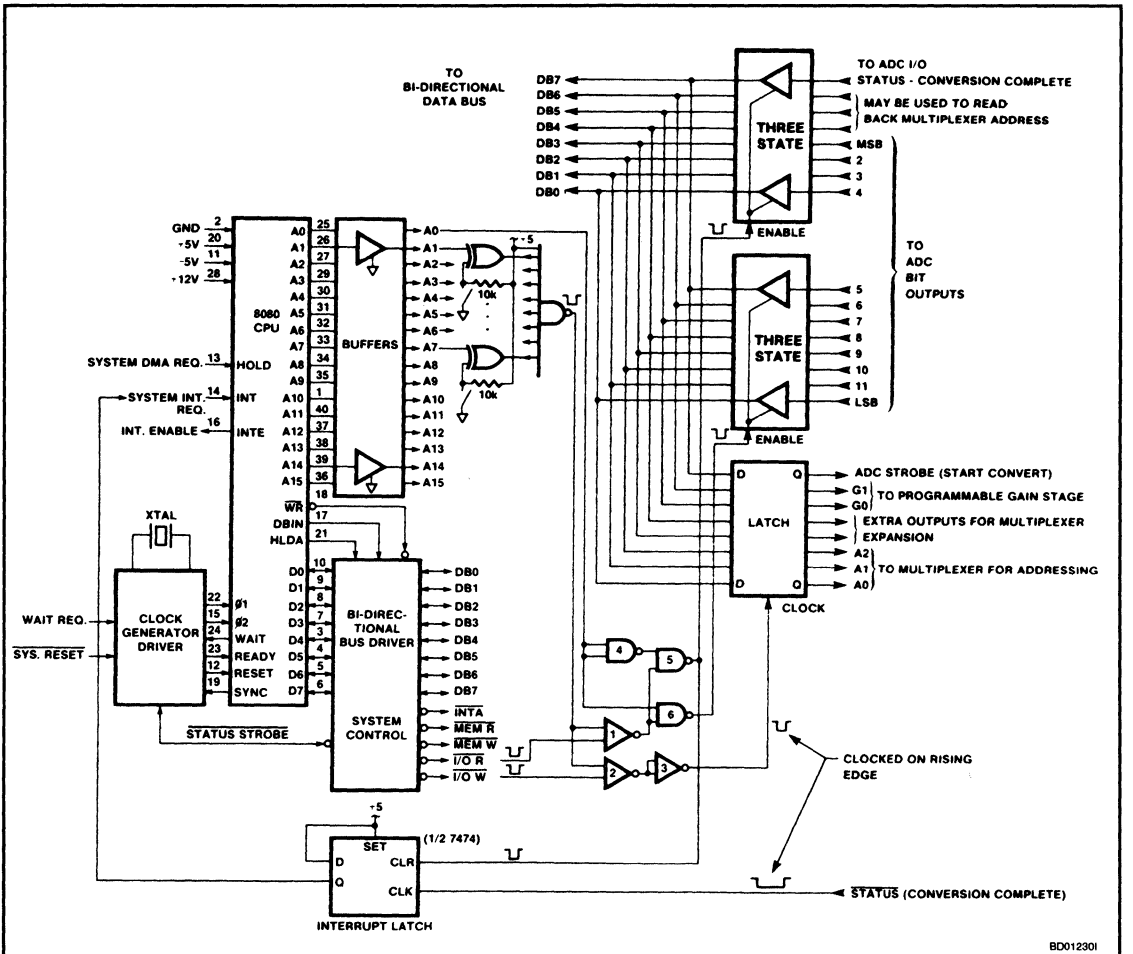
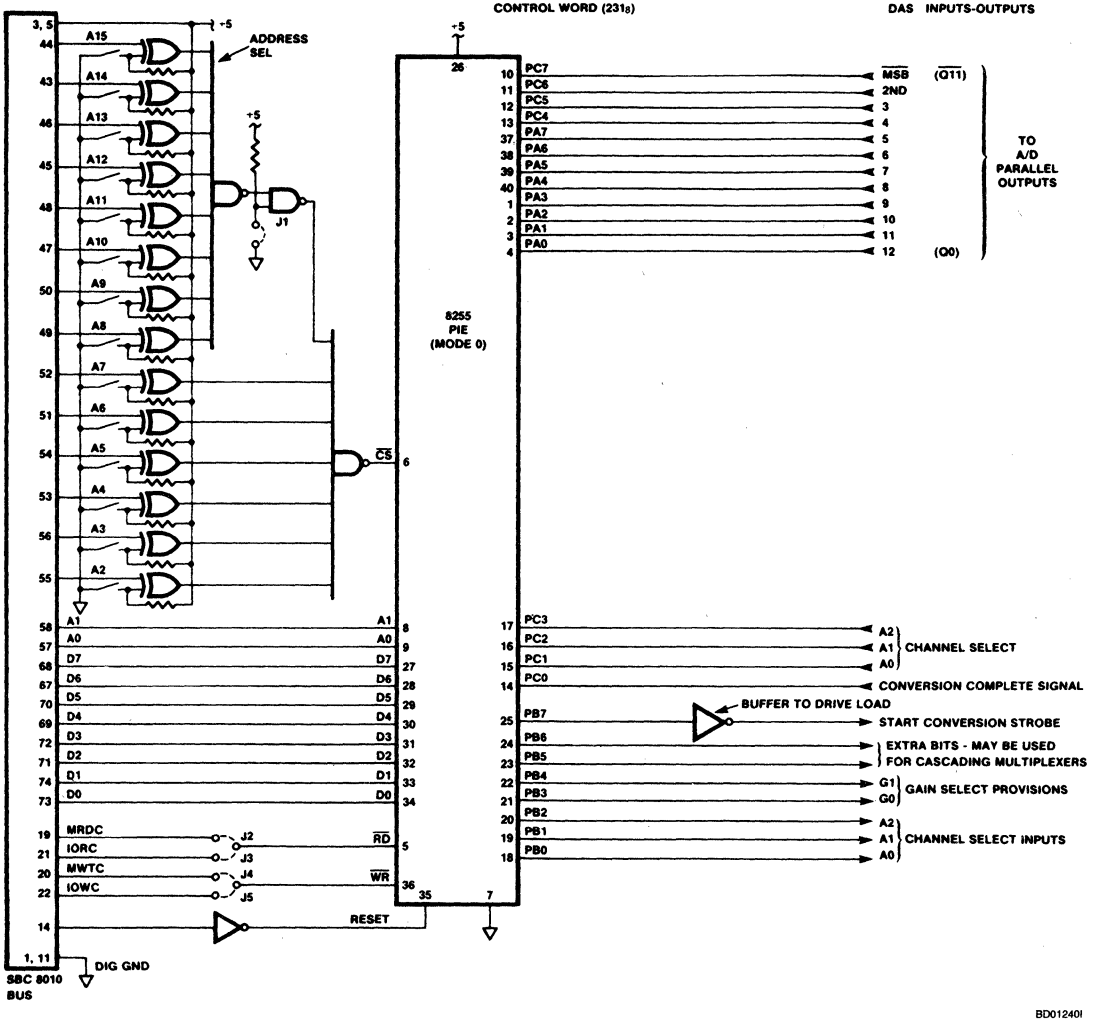


Figure 23: Block Diagram for Complete Interface of DAS to 8080 Using Programmed I/O and Interrupt Driven

INTERFACE TO THE SBC-80/10 BUS

Figure 24 shows a complete interface for a DAS using the 8255 parallel interface element, which will plug directly into the SBC 80/10 bus. The 8255, when used in mode 0, will replace the three-state buffers, latch and handshake and control circuitry of Figure 23, and provide a simplified interface. When using the 8255, or any other parallel interface element to directly drive a data bus, care must be taken not to overload the three-state drive capabilities of its outputs, otherwise the interface will not drive the bus and improper transfer of data will occur. For a heavily loaded bus, which can be considered more than three TTL loads when connecting the data lines of the 8255 directly to the bus, the 8255 must itself be buffered by three-state buffers. The enable lines for these buffers would then be driven by the same read/write signals which enter the 8255 at pins 5 and 36 respectively. By initializing the 8255 with a control word of 231_8 in mode 0, the I/O pins will be programmed as shown in Figure 24, with PB0–PB7 as outputs and all others as inputs.



NOTE: 1. FOR PROGRAMMED I/O CONNECT J1, J3 AND J5
2. FOR MEMORY MAPPED I/O CONNECT J2 AND J4

Figure 24: Interface to SBC 80/10 Bus

SUMMARY

Although a wide variety of circuits have been presented, the actual requirements for a specific application will dictate the selections which must be made from them. Again, an accurate 12 bit system has been covered at every stage, and would be adequate for any less accurate system. Some improvements in speed or economy could be achieved by the redesign of the building blocks under the guidelines explored here, but at the cost of lowered accuracy. Increases in accuracy, correspondingly, would necessitate redesign, or at least reformulation, of most of the blocks as required.

Nevertheless, it should be clear that the cookbook approach, in a building block orientation as presented here, is capable of achieving an altogether satisfactory design of a high speed data acquisition and microprocessor interface system. And for those who hate cooking, many of the more complex blocks are available as modules (generally designed as described here, and using the same components), simplifying the process considerably. For the ultimate in "table service", complete systems can be purchased, including all the elements described here. But that is outside the purview of a cookbook.

Some other applications bulletins that may be found useful are listed here:

A003 "Understanding and Applying the Analog Switch", by Dave Fullagar.
A004 "The IH5009 Series of Low Cost Analog Switches".
A006 "A New CMOS Analog Gate Technology", by Dave Fullagar.
A016 "Selecting A/D Converters", by Dave Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4-1/2 Digit Panel Meter Demonstrator/ Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar & Michael Dufort.
A025 "Building a Remote Data Logging Station", by Peter Bradshaw.
A028 "Building an Autoranging DMM with the ICL7103A/ 8052A A/D Converter Pair", by Larry Goff.
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw.
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.
R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection", by Dick Wilenken.
R011 "Switching Signals with Semiconductors", by Paresh Manair.

A001
Glossary of Data Conversion Terms

This glossary defines the most often used terms in the field of data conversion technology. Each of the terms has been described or referred to elsewhere in this book.

ABSOLUTE ACCURACY: The worst-case input to output error of a data converter referred to the NBS standard volt.

ACCURACY: The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy.*

ACQUISITION TIME: For a sample-hold, the time required, after the sample command is given, for the hold capacitor to charge to a full scale voltage change and then remain within a specified error band around final value.

ACTIVE FILTER: An electronic filter which uses passive circuit elements with active devices such as gyrators or operational amplifiers. In general, resistors and capacitors are used but no inductors.

ACTUATOR: A device which converts a voltage or current input into a mechanical output.

ADC: Abbreviation for analog-to-digital converter. See *A/D converter.*

A/D CONVERTER: Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

ALIAS FREQUENCY: In reconstructed analog data, a false lower frequency component which is the result of insufficient sampling rate, i.e., less than that required by the sampling theorem.

ALIASING: See *Alias Frequency.*

ANALOG MULTIPLEXER: An array of switches with a common output connection for selecting one of a number of analog inputs. The output signal follows the selected input within a small error.

ANTI-ALIAS FILTER: See *Pre-Sampling Filter.*

APERTURE DELAY TIME: In a sample-hold, the time elapsed from the hold command to the actual opening of the sampling switch.

APERTURE JITTER: See *Aperture Uncertainty Time.*

APERTURE TIME: The time window, or time uncertainty, in making a measurement. For an A/D converter it is the conversion time; for a sample-to-hold it is the signal averaging time during the sample-to-hold transition.

APERTURE UNCERTAINTY TIME: In a sample-hold, the time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample.

AUTO-ZERO: A stabilization circuit which servos an amplifier or A/D converter input offset to zero during a portion of its operating cycle.

BANDGAP REFERENCE: A voltage reference circuit which is based on the principle of the predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon (≈1.22V).

BANDWIDTH: The frequency at which the gain of an amplifier or other circuit is reduced by 3dB from its DC value; also the range of frequencies within which the attenuation is less than 3dB from the center frequency value.

BCD: See *Binary Coded Decimal.*

BINARY CODE: See *Natural Binary Code.*

BINARY CODED DECIMAL (BCD): A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

BIPOLAR MODE: For a data converter, when the analog signal range includes both positive and negative values.

BIPOLAR OFFSET: The analog displacement of one half of full scale range in a data converter operated in the bipolar mode. The offset is generally derived from the converter reference circuit.

BREAK-BEFORE-MAKE SWITCHING: A characteristic of analog multiplexers in which there is a small time delay between disconnection from the previous channel and connection to the next channel. This assures that no two inputs are ever momentarily shorted together.

BUFFER AMPLIFIER: An amplifier employed to isolate the loading effect of one circuit from another.

BURIED ZENER REFERENCE: See *Subsurface Zener Reference.*

BUSY OUTPUT: See *Status Output.*

BUTTERFLY CHARACTERISTIC: An error versus temperature graph in which all errors are contained within two straight lines which intersect at room temperature, or approximately 25°C.

CHARGE BALANCING A/D CONVERTER: An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called *quantized-feedback.*

CHARGE DUMPING: See *Charge Transfer.*

CHARGE INJECTION: See *Charge Transfer.*

CHARGE TRANSFER: In a sample-hold, the phenomenon of moving a small charge from the sampling switch to the hold capacitor during switch turn-off. This is caused by the switch control voltage change coupling through switch capacitance to the hold capacitor. Also called *charge dumping* or *charge injection.*

CHOPPER-STABILIZED AMPLIFIER: An operational amplifier which employs a special DC modulator-demodulator circuit to reduce input offset voltage drift to an extremely low value.

CLOCK: A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

CLOCK RATE: The frequency of the timing pulses of the clock circuit in an A/D converter.

COMMON-MODE REJECTION RATIO: For an amplifier, the ratio of differential voltage gain to common-mode voltage gain, generally expressed in dB.

$$CMRR = 20\log_{10}\frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common mode voltage gain.

COMPANDING CONVERTER: An A/D or D/A converter which employs a logarithmic transfer function to expand or compress the analog signal range. These converters have large effective dynamic ranges and are commonly used in digitized voice communication systems.

COMPLEMENTARY BINARY CODE: A binary code which is the logical complement of straight binary. All 1's become 0's and vice versa.

CONVERSION TIME: The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full scale analog input change.

CONVERSION RATE: The number of repetitive A/D or D/A conversions per second for a full scale change to specified resolution and linearity.

COUNTER TYPE A/D CONVERTER: A feedback method of A/D conversion whereby a digital counter drives a D/A converter which generates an output ramp which is compared with the analog input. When the two are equal, a comparator stops the counter and output data is ready. Also called a *servo type* A/D converter.

CREEP VOLTAGE: A voltage change with time across an open capacitor caused by dielectric absorption. This causes sample-hold output error.

CROSSTALK: In an analog multiplexer, the ratio of output voltage to input voltage with all channels connected in parallel and off. It is generally expressed as an input to output attenuation ratio in dB.

DAC: Abbreviation for digital-to-analog converter. See *D/A Converter.*

D/A CONVERTER: Digital-to-analog converter. A circuit which converts a digital code word into an output analog (continuous) voltage or current.

DATA ACQUISITION SYSTEM: A system consisting of analog multiplexers, sample-holds, A/D converters, and other circuits which process one or more analog signals and convert them into digital form for use by a computer.

DATA AMPLIFIER: See *Instrumentation Amplifier.*

DATA CONVERTER: An A/D or D/A Converter.

DATA DISTRIBUTION SYSTEM: A system which uses D/A converters and other circuits to convert the digital outputs of a computer into analog form for control of a process or system.

DATA RECOVERY FILTER: A filter used to reconstruct an analog signal from a train of analog samples.

DATA WORD: A digital code-word that represents data to be processed.

DECAY RATE: See *Hold-Mode Droop.*

DECODER: A communications term for D/A converter.

DEGLITCHED DAC: A D/A converter which incorporates a deglitching circuit to virtually eliminate output spikes (or glitches). These DAC's are commonly used in CRT display systems.

DEGLITCHER: A special sample-hold circuit used to eliminate the output spikes (or glitches) from a D/A converter.

DIELECTRIC ABSORPTION: A voltage memory characteristic of capacitors caused by the dielectric material not polarizing instantaneously. The result is that not all the energy stored in a charged capacitor can be quickly recovered upon discharge, and the open capacitor voltage will creep. See also *Creep Voltage.*

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

DIGITIZER: A device which converts analog into digital data; an A/D converter.

DOUBLE-LEVEL MULTIPLEXING: A method of channel expansion in analog multiplexers whereby the outputs of a group of multiplexers connect to the inputs of another multiplexer.

DROOP: See *Hold-Mode Droop.*

DUAL SLOPE A/D CONVERTER: An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

DYNAMIC ACCURACY: The total error of a data converter or conversion system when operated at its maximum specified conversion rate or throughput rate.

DYNAMIC RANGE: The ratio of full scale range (FSR) of a data converter to the smallest difference it can resolve. In terms of converter resolution:

$$\text{Dynamic Range (DR)} = 2^n$$

It is generally expressed in dB:

$$DR = 20\log_{10}2^n = 6.02n$$

where n is the resolution in bits.

EFFECTIVE APERTURE DELAY: In a sample-hold, the time difference between the hold command and the time at which the input signal equalled the held voltage.

ELECTROMETER AMPLIFIER: An amplifier characterized by ultra-low input bias current and input noise which is used to measure currents in the picoampere region and lower.

ENCODER: A communications term for an A/D converter.

E.O.C.: End of Conversion. See *Status Output.*

ERROR BUDGET: A systematic listing of errors in a circuit or system to determine worst case total or statistical error.

EXTRAPOLATIVE HOLD: See *First-Order Hold.*

FEEDBACK TYPE A/D CONVERTER: A class of analog-to-digital converters in which a D/A converter is enclosed in the feedback loop of a digital control circuit which changes the D/A output until it equals the analog input.

FIRST-ORDER HOLD: A type of sample-hold, used as a recovery filter, which uses the present and previous analog samples to predict the slope to the next sample. Also called an *extrapolative hold.*

FLASH TYPE A/D CONVERTER: See *Parallel A/D Converter.*

FLYING-CAPACITOR MULTIPLEXER: A multiplexer switch which employs a double-pole, double-throw switch connected to a capacitor. By first connecting the capacitor to the signal source and then to differential amplifier, a signal with a high common-mode voltage can be multiplexed to a ground-referenced circuit.

FRACTIONAL-ORDER HOLD: A type of sample-hold, used as a recovery filter, which uses a fixed fraction of the difference between the present and previous analog samples to predict the slope to the next sample.

FREQUENCY FOLDING: In the recovery of sampled data, the overlap of adjacent spectra caused by insufficient sampling rate. The overlapping results in distortion in the recovered signal which cannot be eliminated by filtering the recovered signal.

FREQUENCY-TO-VOLTAGE (F/V) CONVERTER: A device which converts an input pulse rate into an output analog voltage.

FSR: Full Scale Range.

FULL POWER FREQUENCY: The maximum frequency at which an amplifier, or other device, can deliver rated peak-to-peak output voltage into rated load at a specified distortion level.

FULL SCALE RANGE (FSR): The difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

F/V CONVERTER: See *Frequency-To-Voltage Converter.*

GAIN-BANDWIDTH PRODUCT: The product of gain and small signal bandwidth for an operational amplifier or other circuit. This product is constant for a single-pole response.

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

HIGH-LEVEL MULTIPLEXING: An analog multiplexing circuit in which the analog signal is first amplified to a higher level (1 to 10 volts) and then multiplexed. This is the preferred method of multiplexing to prevent noise contamination of the analog signal.

HOLD CAPACITOR: A high quality capacitor used in a sample-hold circuit to store the analog voltage. The capacitor must have low leakage and low dielectric absorption. Types commonly used include polystyrene, teflon, polycarbonate, polypropylene, and MOS.

HOLD-MODE: The operating mode of a sample-hold circuit in which the sampling switch is open.

HOLD-MODE DROOP: In a sample-hold, the output voltage change per unit of time with the sampling switch open. It is commonly expressed in V/sec. or $\mu V/\mu$ sec.

HOLD-MODE FEEDTHROUGH: In a sample-hold, the percentage of input sinusoidal or step signal measured at the output with the sampling switch open.

HOLD-MODE SETTLING TIME: In a sample-hold, the time from the hold-command transition until the output has settled within a specified error band.

HYSTERESIS ERROR: The small variation in analog transition points of an A/D converter whereby the transition level depends on the direction from which it is approached. In most A/D converters this hysteresis is very small and is caused by the analog comparator.

IDEAL FILTER: A low pass filter with flat passband response, infinite attenuation at the cutoff frequency, and zero response past cutoff; it also has linear phase response in the passband. Ideal filters are mathematical filters frequently used in textbook examples but not physically realizable.

INDIRECT TYPE A/D CONVERTER: A class of analog-to-digital converters which converts the unknown input voltage into a time period and then measures this period.

INFINITE-HOLD: A sample-hold circuit which converts an analog voltage into digital form which is then held indefinitely, without decay, in a register.

INPUT DYNAMIC RANGE: In an amplifier, the maximum permissible peak-to-peak voltage across the input terminals which does not cause the output to slew rate limit or distort. Mathematically it is found as

$$\text{IDR (Input Dynamic Range)} \frac{\text{SR}}{\pi \text{GB}}$$

where SR is the slew rate and GB is gain bandwidth.

INSTRUMENTATION AMPLIFIER: An amplifier circuit with high impedance differential inputs and high common-mode rejection. Gain is set by one or two resistors which do not connect to the input terminals.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTEGRATING A/D CONVERTER: One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

INTERPOLATIVE HOLD: See *Polygonal Hold.*

ISOLATION AMPLIFIER: An amplifier which is electrically isolated between input and output in order to be able to amplify a differential signal superimposed on a high common-mode voltage.

LEAST SIGNIFICANT BIT (LSB): The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{\text{FSR}}{2^n}$$

where FSR is full scale range and n is the resolution in bits.

LINEARITY ERROR: See *Integral Linearity Error* and *Differential Linearity Error.*

LONG TERM STABILITY: The variation in data converter accuracy due to time change alone. It is commonly specified in percent per 1000 hours or per year.

LOW-LEVEL MULTIPLEXING: An analog multiplexing system in which a low amplitude signal is first multiplexed and then amplified.

LSB: Least Significant Bit.

LSB SIZE: See *Quantum.*

MAJOR CARRY: See *Major Transition.*

MAJOR TRANSITION: In a data converter, the change from a code of 1000 . . . 000 to 0111 . . . 1111 or vice-versa. This transition is the most difficult one to make from a linearity standpoint since the MSB weight must ideally be precisely one LSB larger than the sum of all other bit weights.

MISSING CODE: In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a nonmonotonic D/A converter inside the A/D.

MONOTONICITY: For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Nonmonotonicity* may occur if the converter differential linearity error exceeds ±1 LSB.

MOST SIGNIFICANT BIT (MSB): The leftmost bit in a data converter code. It has the largest weight, equal to one half of full scale range.

MSB: Most Significant Bit.

MULTIPLYING D/A CONVERTER: A type of digital-to-analog converter in which the reference voltage can be varied over a wide range to produce an analog output which is the product of the input code and input reference voltage. Multiplication can be accomplished in one, two, or four algebraic quadrants.

MUX: Abbreviation for multiplexer. See *Analog Multiplexer.*

NATURAL BINARY CODE: A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

NEGATIVE TRUE LOGIC: A logic system in which the more negative of two voltage levels is defined as a logical 1 (true) and the more positive level is defined as a logical 0 (false).

NOISE REJECTION: The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

NONMONOTONIC: A D/A converter transfer characteristic in which the output does not continuously increase with increasing input. At one or more points there may be a dip in the output function.

NORMAL-MODE REJECTION: The attenuation of a specific frequency or band of frequencies appearing directly across two electrical terminals. In A/D converters, normal-mode rejection is determined by an input filter or by integration of the input signal.

NOTCH FILTER: An electronic filter which attenuates or rejects a specific frequency or narrow band of frequencies with a sharp cutoff on either side of the band.

NYQUIST THEOREM: See *Sampling Theorem.*

OFFSET BINARY CODE: Natural binary code in which the code word 0000....0000 is displaced by one-half analog full scale. The code represents analog values between −FS and +FS (full scale). The code word 1000....0000 then corresponds to analog zero.

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

OFFSET ERROR: The error at analog zero for a data converter operating in the bipolar mode.

ONE'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all one's.

PARALLEL TYPE A/D CONVERTER: An ultrafast method of A/D conversion which uses an array of $2^n - 1$ comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

PARALLEL TYPE D/A CONVERTER: The most commonly used type of D/A converter in which upon application of an input code, all bits change simultaneously to produce a new output.

PASSIVE FILTER: A filter circuit using only resistors, capacitors, and inductors.

POLYGONAL HOLD: A type of sample-hold, used as a signal recovery filter, which produces a voltage output which is a straight line joining the previous sample value to the present sample. This results in an accurate signal reconstruction but with a one sample-period output delay.

POSITIVE TRUE LOGIC: A logic system in which the more positive of two voltage levels is defined as a logical 1 (true) and the more negative level is defined as a logical 0 (false).

POWER SUPPLY SENSITIVITY: The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

PRECISION: The degree of repeatability, or reproducibility of a series of successive measurements. Precision is affected by the noise, hysteresis, time, and temperature stability of a data converter or other device.

PRE-SAMPLING FILTER: A low pass filter used to limit the bandwidth of a signal before sampling in order to assure that the conditions of the Sampling Theorem are met. Therefore frequency folding is eliminated or greatly diminished in the recovered signal spectrum.

PROGRAMMABLE GAIN AMPLIFIER: An amplifier with a digitally controlled gain for use in data acquisition systems.

PROGRAMMER-SEQUENCER: A digital logic circuit which controls the sequence of operations in a data acquisition system.

PROPAGATION TYPE A/D CONVERTER: A type of A/D conversion method which employs one comparator per bit to achieve ultra-fast A/D conversion. The conversion propagates down the series of cascaded comparators.

QUAD CURRENT SWITCH: A group of four current sources weighted 8-4-2-1 which are switched on and off by TTL inputs. They are used to implement A/D and D/A converter designs up to 16 bits resolution by using multiple quads with current dividers between each quad.

QUANTIZATION NOISE: See *Quantization Error.*

QUANTIZATION UNCERTAINTY: See *Quantization Error.*

QUANTIZED FEEDBACK A/D CONVERTER: See *Charge Balancing A/D Converter.*

QUANTIZER: A circuit which transforms a continuous analog signal into a set of discrete output states. Its transfer function is the familiar staircase function.

QUANTIZING ERROR: The inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process. The quantized value is uncertain by up to ±Q/2 where Q is the quantum size. This error can be reduced only by increasing the resolution of the converter. Also called *quantization uncertainty or quantization noise.*

QUANTUM: The analog difference between two adjacent codes for an A/D or D/A converter. Also called *LSB size.*

R-2R LADDER NETWORK: An array of matched resistors with series values of R and shunt values of 2R in a standard ladder circuit configuration.

RATIOMETRIC A/D CONVERTER: An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the reference.

RECONSTRUCTION FILTER: See *Data Recovery Filter.*

RECOVERY FILTER: See *Data Recovery Filter.*

REFERENCE CIRCUIT: A circuit which produces a stable output voltage over time and temperature for use in A/D and D/A converters. The circuit generally uses an operational amplifier with a precision Zener or bandgap type reference element.

RELATIVE ACCURACY: The worst case input to output error of a data converter, as a percent of full scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

RESOLUTION: The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

SAMPLE-HOLD: A circuit which accurately acquires and stores an analog voltage on a capacitor for a specified period of time.

SAMPLE-HOLD FIGURE OR MERIT: The ratio of capacitor charging current in the sample-mode to the leakage current off the capacitor in the hold-mode.

SAMPLE-MODE: The operating mode of a sample-hold circuit in which the sampling switch is closed.

SAMPLER: An electronic switch which is turned on and off at a fast rate to produce a train of analog sample pulses.

SAMPLE-TO-HOLD OFFSET ERROR: For a sample-hold, the change in output voltage from the sample-mode to the hold-mode, with constant input voltage. This error is caused by the sampling switch transferring charge onto the hold capacitor as it opens.

SAMPLE-TO-HOLD STEP: See *Sample-to-Hold Offset Error.*

SAMPLE-TO-HOLD TRANSIENT: A small spike at the output of a sample-hold when it goes into the hold mode. It is caused by feedthrough from the sampling switch control voltage.

SAMPLING THEOREM: A theorem due to Nyquist which says if a continuous bandwidth-limited signal contains no frequency components higher than f_c, then the original signal can be recovered without distortion if it is sampled at a rate of at least $2f_c$ samples per second.

SAR: Successive approximation register. A digital control circuit used to control the operation of a successive approximation A/D converter.

SCALE FACTOR ERROR: See *Gain Error.*

SERIAL TYPE D/A CONVERTER: A type of digital-to-analog converter in which the digital input data is received in sequential form before an analog output is produced.

SERVO-TYPE A/D CONVERTER: See *Counter-Type A/D Converter.*

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and D/A converters.

SHORT CYCLING: The termination of an A/D conversion process at a resolution less than the full resolution of the converter. This results in a shorter conversion time for reduced resolution in A/D converters with a short cycling capability.

SIGNAL RECONSTRUCTION FILTER: A low pass filter used to accurately reconstruct an analog signal from a train of analog samples.

SIGN-MAGNITUDE BCD: A binary coded decimal code in which a sign bit is added to distinguish positive from negative in bipolar operation.

SIGN-MAGNITUDE BINARY CODE: The natural binary code to which a sign bit is added to distinguish positive from negative in bipolar operation.

SIMULTANEOUS SAMPLE-HOLD: A system in which a series of sample-hold circuits are used to sample a number of analog channels, all at the same instant. This requires one sample-hold per analog channel.

SIMULTANEOUS TYPE A/D CONVERTER: See *Parallel Type A/D Converter.*

SINGLE-LEVEL MULTIPLEXING: A method of channel expansion in analog multiplexers whereby several multiplexers are operated in parallel by connecting their outputs together. Each multiplexer is controlled by a digital *enable* input.

SINGLE-SLOPE A/D CONVERTER: A simple A/D converter technique in which a ramp voltage generated from a voltage reference and integrator is compared with the analog input voltage by a comparator. The time required for the ramp to equal the input is measured by a clock and counter to produce the digital output word.

SKIPPED CODE: See *Missing Code.*

SLEW RATE: The maximum rate of change of the output of an operational amplifier or other circuit. Slew rate is limited by internal charging currents and capacitances and is generally expressed in volts per microsecond.

SPAN: For an A/D or D/A converter, the full scale range or difference between maximum and minimum analog values.

START-CONVERT: The input pulse to an A/D converter which initiates conversion.

STATIC ACCURACY: The total error of a data converter or conversion system under DC input conditions.

STATUS OUTPUT: The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called *busy output* or *end of conversion* output.

STRAIGHT BINARY CODE: See *Natural Binary Code.*

SUBSURFACE ZENER REFERENCE: A compensated voltage reference diode in which avalanche breakdown occurs below the surface of the silicon in the bulk region rather than at the surface. This results in lower noise and higher stability. The reversed biased diode is temperature compensated by a series connected, forward biased signal diode.

SUCCESSIVE APPROXIMATION A/D CONVERTER: An A/D conversion method that compares in sequence a series of binary weighted values with the analog input to produce an output digital word in just n steps, where n is the resolution in bits. The process is efficient and is analogous to weighing an unknown quantity on a balance scale using a set of binary standard weights.

TEMPERATURE COEFFICIENT: The change in analog magnitude with temperature, expressed in ppm/°C.

THREE-STATE OUTPUT: A type of A/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An *enable* control turns the output on or off.

THROUGHPUT RATE: The maximum repetitive rate at which a data conversion system can operate to give specified output accuracy. It is determined by adding the various times required for multiplexer settling, sample-hold acquisition, A/D conversion, etc. and then taking the inverse of total time.

TRACK-AND-HOLD: A sample-hold circuit which can continuously follow the input signal in the sample-mode and then go into hold-mode upon command.

TRACKING A/D CONVERTER: A counter-type analog-to-digital converter which can continuously follow the analog input at some specified maximum rate and continuously update its digital output as the input signal changes. The circuit uses a D/A converter driven by an up-down counter.

TRANSDUCER: A device which converts a physical parameter such as temperature or pressure into an electrical voltage or current.

TRANSFER FUNCTION: The input to output characteristic of a device such as a data converter expressed either mathematically or graphically.

TRIPLE-SLOPE A/D CONVERTER: A variation on the dual slope type A/D converter in which the time period measured by the clock and counter is divided into a coarse (fast slope) measurement and a fine (slow slope) measurement.

TWO'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all zero's plus a carry.

TWO-STAGE PARALLEL A/D CONVERTER: An ultra-fast A/D converter in which two parallel type A/D's are operated in cascade to give higher resolution. In the usual case a 4-bit parallel converter first makes a conversion; the resulting output code drives an ultra-fast 4-bit D/A, the output of which is subtracted from the analog input to form a residual. This residual then goes to a second 4 bit parallel A/D. The result is an 8 bit word converted in two steps.

UNIPOLAR MODE: In a data converter, when the analog range includes values of one polarity only.

V/F CONVERTER: See *Voltage-to-Frequency Converter.*

VIDEO A/D CONVERTER: An ultra-fast A/D converter capable of conversion rates of 5MHz and higher. Resolution is usually 8 bits but can vary depending on the application. Conversion rates of 20MHz and higher are common.

VOLTAGE DECAY: See *Hold-Mode Droop.*

VOLTAGE REFERENCE: See *Reference Circuit.*

VOLTAGE-TO-FREQUENCY (V/F) CONVERTER: A device which converts an analog voltage into a train of digital pulses with frequency proportional to the input voltage.

WEIGHTED CURRENT SOURCE D/A CONVERTER: A digital-to-analog converter design based on a series of binary weighted transistor current sources which can be turned on or off by digital inputs.

ZERO DRIFT: The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.

ZERO ERROR: The error at analog zero for a data converter operating in the unipolar mode.

ZERO-ORDER HOLD: A name for a sample-hold circuit used as a data recovery filter. It is used to accurately reconstruct an analog signal from a train of analog samples.

Chapter 2
A/D & D/A Converters

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Selecting A/D Converters

One of the popular pastimes of the nineteen sixties was to predict the explosive growth of digital data processing, fed by the newly-developed semiconductor MSI circuits, and the subsequent demise of analog circuitry. The first part of this prediction has certainly come true — the advent of the microprocessor has caused, and will continue to cause, a revolution in digital processing which was unthinkable 10 years ago. But far from causing the demise of analog systems, the reverse has occurred. Nearly all the data being processed (with the notable exception of financial data) consists of physical parameters of an analog nature — pressure, temperature, velocity, light intensity and acceleration to name but a few. In every instance this analog information must be converted into its digital equivalent, using some form of A/D converter. Converter products are thus assuming a key role in the realization of data acquisition systems.

Increased use of microprocessors has also caused dramatic cost reductions in the digital components of a typical system. The $8000 mini-computer of a few years ago is being replaced by a $475 dedicated microprocessor board. This trend is also being reflected in the analog components. No longer is it possible to justify buying a $400 data acquisition module when a dedicated system, adequate for the task under consideration, can be put together for $50.

Thus many engineers, who in the past have had limited exposure to analog circuitry, are having to come to grips with the characteristics of A/D converters, sample & holds, multiplexers and operational amplifiers. Contrary to the propaganda put out by many of the specialty module houses, there is nothing mysterious about these components or the way they interface with one another. Now that many of them are available as one or two chip MSI circuits, a block diagram may be turned into a working piece of hardware with relative ease.

The purpose of this note is to compare and contrast the more popular A/D designs, and provide the reader with sufficient information to select the most appropriate converter for his or her needs.

THE IMPORTANT PARAMETERS

Let's begin by taking a look at some actual systems, since this will illustrate the diversity of performance required of A-to-D converters.

Case 1: A seismic recording truck is situated over a potential natural gas site. Some 32 recording devices are laid out over the surrounding area. An explosive charge is detonated and in a matter of seconds it is all over. During that time it is necessary to scan each recorder every 100 microseconds. Speed is clearly the most important requirement. In this instance, 12 bit accuracy is not required; and, since the truck contains many thousands of dollars of electronics, cost is not a critical parameter. The A/D will be a high speed successive approximation design.

Case 2: A semiconductor engineer is measuring the 'thermal profile' of a furnace. It is necessary to make measurements accurate to a few tenths of a degree Centigrade, which is equivalent to a few microvolts of thermocouple output. Sampling rates of a few readings per second are adequate and costs should be kept low. The integrating ('dual slope', 'triphasic', 'quad slope', depending on which manufacturer you go to) A/D is the only type capable of the required precision/cost combination. It has the added advantage of maintaining accuracy in a noisy environment.

Case 3: A businessman is talking to his sales office in Rome. Assuming the phone company is not on strike, his voice will be sampled at a 10kHz rate, or thereabouts, in order not to lose information in the audio frequency range up to 5kHz. This requires a medium accuracy (8 bit) A/D with a cycle time of 100 microseconds or less. In this application the integrating type is not fast enough, so it is necessary to use a slow (for this approach) successive approximation design.

These examples serve to introduce both the two most popular conversion techniques (successive approximation and integrating) and the three key parameters of a converter, i.e. speed, accuracy and cost. In fact the first choice in selecting an A/D is between successive approximation and integrating, since greater than 95% of all converters fall into one of these two categories.

If we look at the whole gamut of available converters, with conversion speeds ranging from 100ms to less than 1μs, we see that these two design approaches divide the speed spectrum into two groups with almost no overlap. (Table 1) However, before making a selection solely on the basis of speed, it is important to have an understanding of how the converters work, and how the data sheet specifications relate to the circuit operation.

TABLE 1

TYPE OF CONVERTER	RELATIVE SPEED	CONVERSION TIME			
		8 BITS	10 BITS	12 BITS	16 BITS
integrating	slow	20ms	30ms	40ms	250ms
	medium	1ms	5ms	20ms	—
	fast	0.3ms	1ms	5ms	—
successive approximation	general purpose	30μs	40μs	50μs	—
	high performance	10μs	15μs	20μs	400μs
	fast	5μs	10μs	12μs	—
	high speed	2μs	4μs	6μs	—
	ultra-fast	0.8μs	1μs	2μs	—

THE INTEGRATING CONVERTER

Summary of Characteristics

As the name implies, the output of an integrating converter represents the integral or average value of an input voltage over a fixed period of time. A sample-and-hold circuit, therefore, is not required to freeze the input during the measurement period, and noise rejection is excellent.

Equally important, the linearity error of integrating converters is small since they use time to quantize the answer — it is relatively easy to hold short-term clock jitter to better than 1 in 10^6.

The most popular integrating converter uses the dual-slope principle, a detailed description of which is given in Ref. 1.

Its advantages and disadvantages may be summarized as follows:

Advantages:

Inherent accuracy
Non-critical components
Excellent noise rejection
No sample & hold required
Low cost
No missing codes

Disadvantages:

Low speed (typically 3 to 100 readings/sec)

In a practical circuit, the primary errors (other than reference drift) are caused by the non-ideal characteristics of analog switches and capacitors. In the former, leakage and charge injection are the main culprits; in the latter, dielectric absorption is a source of error. All these factors are discussed at length in Ref. 1.

A well-designed dual slope circuit such as Intersil's ICL7135 is capable of 4½ digit performance (±1 in ±20,000) with no critical tweaks or close tolerance components other than a stable reference.

Timing Considerations

In a typical circuit, such as the ICL7135 referred to above, the conversion takes place in three phases as shown in Figure 1. Note that the input is actually integrated or averaged over a period of 10,000 clock pulses (or 83.3 ms with a 120kHz clock) within a conversion cycle of 40,000 clock pulses in total. Also note that the actual business of looking at the input signal does not begin for 10,000 clock pulses, since the circuit first goes into an auto-zero mode. For a 3½ digit product, such as the ICL7106 or ICL7107, the measurement period is 1000 clock pulses (or 8.33ms with a 120kHz clock).

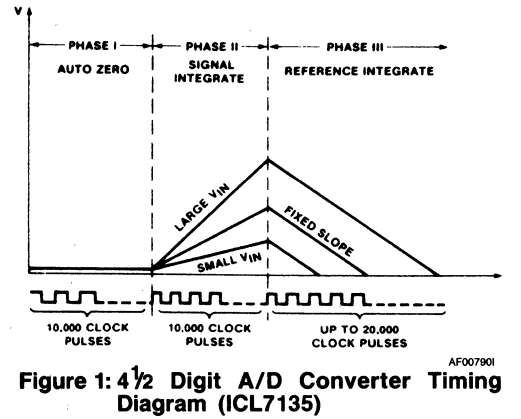

Figure 1: 4½ Digit A/D Converter Timing Diagram (ICL7135)

These timing characteristics give the dual slope circuit both its strengths and its weaknesses. By making the signal integrate period an integral number of line frequency periods, excellent 60Hz noise rejection can be obtained. And of course integrating the input signal for several milliseconds smoothes out the effect of high frequency noise.

But in many applications such as transient analysis or sampling high frequency waveforms, averaging the input over several milliseconds is totally unacceptable. It is of course feasible to use a sample & hold at the input, but the majority of systems that demand a short measurement window also require high speed conversions.

THE SUCCESSIVE APPROXIMATION CONVERTER

How it works

The heart of the successive approximation A/D is a digital-to-analog converter (DAC) in a feedback loop with a comparator and some clever logic referred to as a "successive approximation register" (SAR). Figure 2 shows a typical system. The DAC output is compared with the analog input, progressing from the most significant bit (MSB) to the least significant bit (LSB) one bit at a time. The bit in question is set to one. If the DAC output is less than the input, the bit in question is left at one. If the DAC output is greater than the input, the bit is set to zero. The register then moves on to the next bit. At the completion of the conversion, those bits left in the one state cause a current to flow at the output of the DAC which should match I_{IN} within ±½ LSB. Performing an 'n' bit conversion requires only 'n' trials, making the technique capable of high speed conversion.

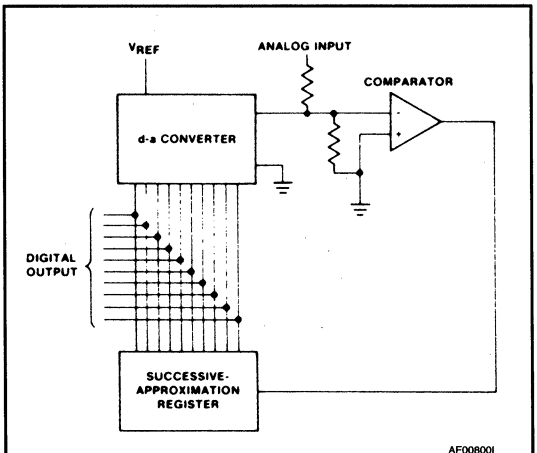

Figure 2: Successive Approximation A/D Converter

The advantages and disadvantages of successive approximation converters may be summarized as follows:

Advantages:
Hi Speed
(Typically 100,000 conversions/sec)

Disadvantages:
Several critical components
Can have missing codes
Requires sample and hold
Difficult to auto-zero
High cost

Error Sources

The error source in the successive approximation converter are more numerous than in the integrating type, with contributions from both the DAC and the comparator. The DAC generally relies on a resistor ladder and current or voltage switches to achieve quantization. Maintaining the correct impedance ratios over the operating temperature range is much more difficult than maintaining clock pulse uniformity in an integrating converter.

The data sheet for a hypothetical A/D might contain the following accuracy related specifications:

Resolution	: 10 Bits
Quantization Uncertainty	: ±½ LSB
Relative Accuracy	: ±½ LSB
Differential Non Linearity	: ±½ LSB
Gain Error	: Adjustable to zero at 25°C
Gain Temp. Coeff.	: ±10 ppm of Full Scale Reading/°C
Offset Error	: Adjustable to zero at 25°C
Offset Temp. Coeff.	: ±20 ppm of Full Scale Reading/°C

Now, referring to the definition of terms on the last page of this Application Note, what does this tell us about the product? First of all, being told that the *quantization uncertainty* is ±½ LSB is like being told that binary numbers are comprised of ones and zeros — it's part of the system. The *relative accuracy* of ±½ LSB, guaranteed over the temperature range, tells us that after removing gain and offset errors, the transfer function never deviates by more than ±½ LSB from where it should be. That's a good spec., but note that gain and offset errors have been adjusted prior to making the measurement. Over a finite temperature range, the temperature coefficients of gain and offset must be taken into account.

The *differential non-linearity* of ±½ LSB maximum is also guaranteed over temperature: this ensures that there are no missing codes.

The *gain temperature coefficient* is 10ppm of FSR per °C, or 0.001% per °C. Now 1 LSB in a 10 bit system is 1 part in 1024, or approximately 0.1%. So a 50°C temperature change from the temperature at which the gain was adjusted (i.e. from +25°C to +75°C) could give rise to ±½ LSB error. This error is separate from, and in the limit could add to, the relative accuracy spec.

The *offset temperature coefficient* of 20 ppm per °C give rise to ±1 LSB error (over a +25°C to +75°C range) by the same reasoning applied to the gain tempco. The reference contributes an error in direct proportion to its percentage change over the operating temperature range.

We can summarize the effect of the major error sources:

Relative Accuracy	±½ LSB or ±.05%
Gain Temp. Coefficient	±½ LSB or ±.05%
Offset Temp. Coefficient	±1 LSB or ±0.1%

A straight forward RMS summation shows that the A/D is 10 bits ±1¼ LSB over a 0°C to +75°C temperature range. However it is over-optimistic to RMS errors with such a small number of variables, and yet we do know that the error cannot exceed ±2 LSB. A realistic estimate might place the accuracy at 10 bits ±1½ LSB.

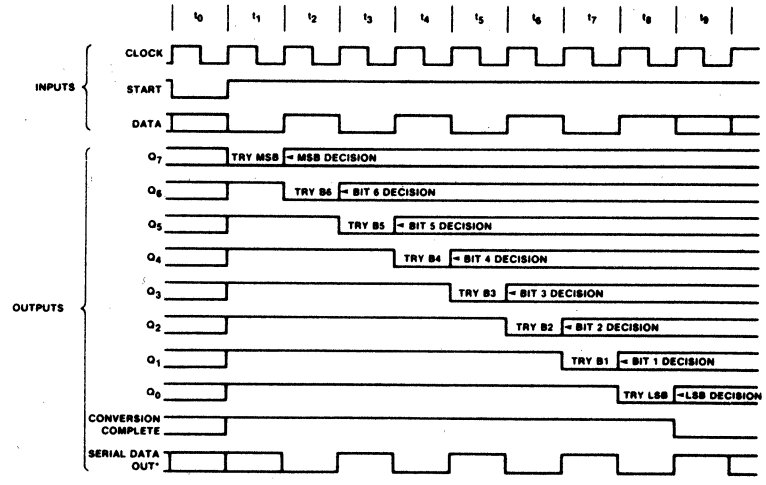

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Figure 3: Typical Timing Diagram for Successive Approximation Converter

Timing Considerations

All successive approximation converters have essentially similar timing characteristics, Figure 3. Holding the start input Low for at least a clock period initiates the conversion. The MSB is set low and all the other bits high for the first trial. Each trial takes one clock period, proceeding from the MSB to the LSB. Note that, in contrast to the integrating converter, a serial output arises naturally from this conversion technique.

Although the successive approximation A/D is capable of very high conversion speeds, there is an important limitation on the slew rate of the input signal. Unlike integrating designs, no averaging of the input signal takes place. To maintain accuracy to 10 bits, for example, the input should not change by more than $\pm$½ LSB during the conversion period. Figure 4(a) shows maximum allowable dV/dt as a function of sampling (or aperture) time for various conversion resolutions. Now for a sinusoidal waveform represented by Esin ωt, the maximum rate of change of voltage $\Delta e/\Delta t$ is $2\pi f E$. The amplitude of one ½ LSB is $E/2^n$, since the pk-pk amplitude is 2E. So the change in input amplitude Δe is given by:

$$\Delta e = E/2^n = 2\pi f E \Delta T, \text{ where } \Delta T = \text{conversion time}$$

$$f\max = \frac{1}{2}\pi \Delta T 2^n$$

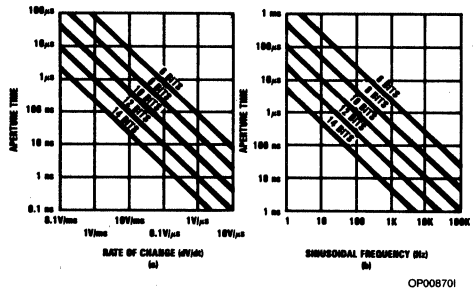

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Figure 4: Maximum input signal rate change (a) and sinewave frequency (b) as a function of sampling or aperture time for $\pm$½ LSB accuracy in 'n' bits.

This is the highest frequency that can be applied to the converter input without using a sample and hold. For n = 10 bits, $\Delta T = 10\mu s$, f max = 15.5Hz. Frequencies this low often come as a surprise to first time users of so-called high speed A/D converters, and explain why the majority of non-integrating converters are preceded by a sample & hold. Figure 4(b) plots equation (1) for a range of ΔT values. Note that when a sample & hold is used, ΔT is the aperture time of the S & H. With the help of a $5 sample & hold such as Intersils's IH5110 (worst case aperture time = 200 ns), f max in the above example becomes 780Hz.

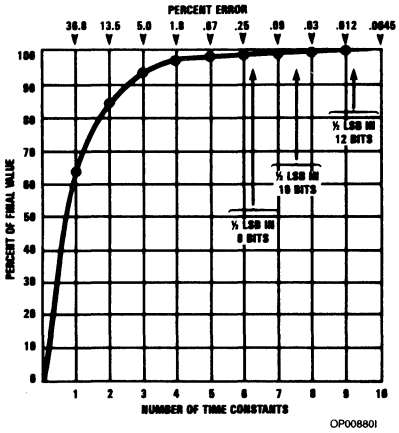

Figure 5: Voltage across a capacitor (as % of final value) as a function of time (# of time constants)

Consideration must also be given to the input stage time constant of both the sample & hold, if there is one, and the converter. The number of time constants taken to charge a capacitor within a given percentage of full scale is shown in Figure 5. For example, consider a product with a 10pF input capacitance driven by a signal source impedance of 100kΩ. For 12 bit accuracy, at least 9 time constants, or 9μs, should be allowed for charging.

CONVERTER CHECKLIST

In selecting a converter for a specific application, it will be helpful to go through the following checklist, matching required performance against data sheet guarantees:

a) How many bits?

b) What is total error budget over the temperature range?

c) What is full scale reading and magnitude of LSB? Make sure that the 95% noise is substantially less than the magnitude of the LSB. If no noise specifications are given, assume that the omission is intentional!

d) What input characteristics are required? With most successive approximation converters, the input resistance is low (≅5kΩ) since one is looking into the comparator summing junction. In a well designed dual slope circuit, there should be a high input resistance buffer ($R_{in} \simeq 10^{12}\Omega$) included within the auto-zero loop.

e) What aperture time (or measurement window) is required?
If an averaged value of the input signal (over some milliseconds) is acceptable, use an integrating converter. Refer to Figure 4 for systems where an averaged value of the input is not acceptable. Remember most successive approximation systems rely on a sample & hold to 'freeze' the input while the conversion is taking place. Thus the sample & hold characteristics should be matched to the input signal slew rate, and the A/D converter characteristics matched to the required conversion rate.

f) What measurement frequency is required? This will determine the maximum allowable conversion time (including auto-zero time for integrating types).

g) Is microprocessor compatibility important? Some A/D's interface easily with microprocessors; others do not. Ref. 2 explores the microprocessor interface in considerable depth.

h) Does the converter form part of a multiplexed data acquisition system?
Note that some integrating converters assess polarity based on the input voltage during the previous conversion cycle. Such designs are clearly unsuitable for multiplexed inputs where the signal polarity bears no relationship to the previously measured value. They can also give trouble with inputs hovering around zero.

i) Is 60Hz rejection important?
If the line frequency rejection capabilities of the integrating converter are important, make sure that the duration of the measurement (input integrate) period is a fixed number of clock pulses. In some designs, the input integration time is programmed by the auto-zero information, making rejection of specific frequencies impossible.

MULTIPLEXED DATA SYSTEMS

The foregoing discussion has summarized the characteristics of A/D converters as stand-alone components. However, one of the most important applications for A/Ds is as part of a multiplexed data acquisition system. Traditionally, systems of this type have used analog signal transmission between the transducer and a central multiplexer/converter console. (Figure 6a) To sample 100 data points 25 times per second requires a 100 input analog multiplexer and an A/D capable of 2500 conversions per second. A successive approximation converter would be the obvious choice.

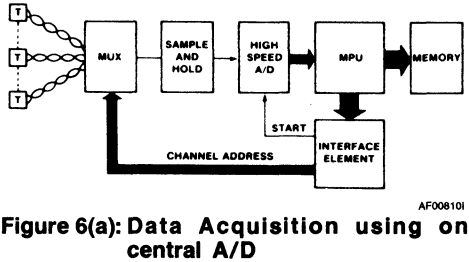

Figure 6(a): Data Acquisition using one central A/D

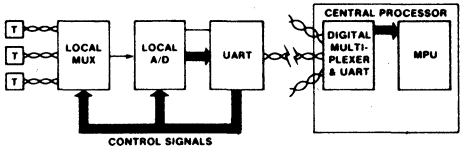

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Figure 6(b): Data Acquisition using several local A/Ds

Another approach, which becomes attractive with the availability of low cost IC converters, is to use localized A/D conversion with digital transmission back to a central console. In the limit one could use a converter per transducer, but it is often more economical to have a local conversion station servicing several transducers (Figure 6b). Several advantages result from this approach. Firstly, digital transmission is more satisfactory in a noisy environment, and lends itself to optical isolation techniques better than analog transmission. Secondly, using local conversion stations significantly reduces the number of interconnects back to the central processor. When one considers that the instrumentation for a typical power plant uses 4.5 million feet of cable, this can result in real cost savings. Finally, by sharing the conversion workload among several A/Ds, it is frequently possible to switch from a successive approximation to a dual slope design.

DEFINITION OF TERMS

Quantization Error. This is the fundamental error associated with dividing a continuous (analog) signal into a finite number of digital bits. A 10 bit converter, for example, can only identify the input voltage to 1 part in 2^{10}, and there is an unavoidable output uncertainty of $\pm 1/2$ LSB (Least Significant Bit). See Figure 7.

Linearity. The maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity is usually expressed as a fraction of LSB size. The linearity of a good converter is $\pm 1/2$ LSB. See Figure 8.

Differential Non-Linearity. This describes the variation in the analog value between adjacent pairs of digital numbers, over the full range of the digital output. If each transition is equal to 1 LSB, the differential non-linearity is clearly zero. If the transition is 1 LSB $\pm 1/2$ LSB, then there is a differential linearity error of $\pm 1/2$ LSB, but no possibility of missing codes. If the transition is 1 LSB ± 1 LSB, then there is the possibility of missing codes. This means that the output may jump from, say 011 . . . . 111 to 100 . . . . 001, missing out 100 . . . . 000. See Figure 9.

Relative Accuracy. The input to output error as a fraction of full scale, with gain and offset errors adjusted to zero. Relative accuracy is a function of linearity, and is usually specified at less than $\pm 1/2$ LSB.

Gain Error. The difference in slope between the actual transfer function and the ideal transfer function, expressed as a percentage. This error is generally adjustable to zero by adjusting the input resistor in a current-comparing successive approximation A/D. See Figure 10.

Gain Temperature Coefficient. The deviation from zero gain error on a 'zeroed' part which occurs as the temperature moves away from 25°C. See Figure 10.

Offset Error. The mean value of input voltage required to set zero code out. This error can generally be trimmed to zero at any given temperature, or is automatically zeroed in the case of a good integrating design.

Offset Temperature Coefficient. The change in offset error as a function of temperature.

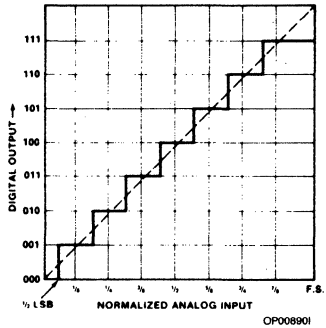

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Figure 7: Ideal A/D conversion

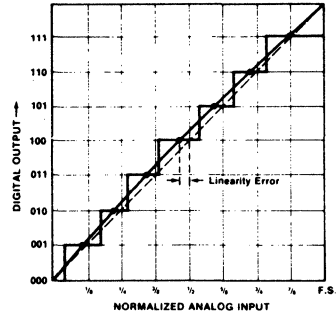

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Figure 8: Linearity Error

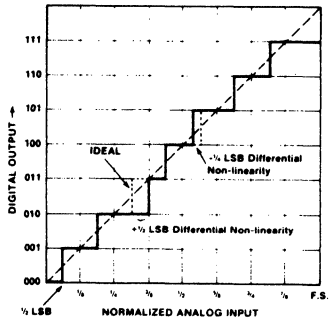

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Figure 9: Differential Non-linearity

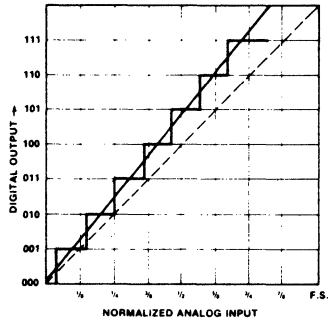

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Figure 10: Gain Error

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Know Your Converter Codes

When you work with A/D and D/A converters, there are many input and output codes to choose from. Here are some characteristics of each.

The right digital code can help simplify system design when analog-to-digital and digital-to-analog converters are used in the system.

While some custom A/D and D/A converters use special codes, off-the-shelf units employ one of a few common codes adopted by the industry as "standard" (Table 1). Understanding which code to use, and where, is the key to a simpler system design. And the added benefits with a standard code include lower cost of the converter and a wider choice of vendors.

Many designers are perplexed about application. There are unipolar codes — straight binary, complementary binary and binary coded decimal (BCD). There are bipolar codes — sign-magnitude binary, sign-magnitude BCD, offset binary, one's complement and two's complement. Other decimal codes include excess-three, 2421, 5421, 5311 and 74-2-1. And there are also reflective codes — such as the Grey code; and error-detecting codes — like the Hamming.

Table 1: Summary of Coding for A/D and D/A Converters

D/A CONVERTERS	A/D CONVERTERS
UNIPOLAR	
Straight binary	Straight binary
BCD	BCD
Complementary binary	Straight bin, invert, analog
Complementary BCD	BCD, inverted analog
BIPOLAR	
Offset binary	Offset binary
Complementary off, binary	Two's complement
Two's complement	Offset bin, invert, analog
	Two's compl, invert, analog
	Sign + mag. binary
	Sign + mag. BCD

All codes used in converters are based on the binary numbering system. Any number can be represented in binary by the following

$$N = a_n 2^n + a_{n-1} 2^{n-1} + \ldots + a_2 2^2 + a_1 2^1 + a_0 2^0,$$

where each coefficient a assumes a value of one or zero. A fractional binary number can be represented as

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots + a_n 2^{-n}.$$

A specific binary fraction is then written, for example, as 0.101101. In most converters it is this fractional binary number that is used for the basic converter code. Conventionally the fractional notation is assumed and the decimal point dropped.

The left-most digit has the most weight, 0.5, and is commonly known as the most-significant-bit (MSB). Thus the right-most digit would have the least weight, $1/2^n$, and is called the least-significant-bit (LSB).

This coding scheme is convenient for converters, since the full-scale range used is simply interpreted in terms of a fraction of full scale. For instance, the fractional code word 101101 has a value of (1 x 0.5) + (0 x 0.25) + (1 x 0.125) + (1 x 0.0625) + (0 x 0.03125) + (1 x 0.015625), or 0.703125 of full-scale value. If all the bits are ONEs, the result is not full scale but rather $(1 - 2^{-n})$ x full scale. Thus a 10-bit D/A converter with all bits ON has an input code of 1111 1111 11. If the unit has a +10-V full-scale output range, the actual analog output value is

$$(1 - 2^{-10}) \times 10V = +9.990235V.$$

The quantization size, or LSB size, is full scale divided by 2^n — which in this case is 9.77mV.

Analyzing Digital Codes

The four most common unipolar codes are straight binary, complementary binary, binary-coded decimal (BCD) and complementary BCD. Of these four, the most popular is straight-binary, positive-true. Positive-true coding means that a logic ONE is defined as the more positive of the two voltage levels for the logic family.

Negative-true logic defines things the other way — the more negative logic level is called ONE and the other level ZERO. Thus, for standard TTL, positive true logic makes the +5-V output logic ONE and 0V a ZERO. In negative true logic the +5V is ZERO and 0V is ONE.

All four of the codes are defined (Table 2) in terms of the fraction of their full-scale values. Full-scale ranges of +5 and +10V are shown with 12-bit codes.

D/A and A/D converters: The operating basics

The basic transfer characteristic of an ideal D/A converter forms the plot shown in Figure A. The D/A takes an input digital code and converts it to an analog output voltage or current. This form of discrete input and discrete output (quantized) gives the transfer function a straight line through the tops of the vertical bars. In general the analog values are completely arbitrary and a large number of binary digital codes can be used. Analog full-scale can be defined as 25.2 to 85.7V as easily as 0 to 10V.

In practice, though, the industry has settled on several codes and very simple ranges for most major applications. For instance, the transfer characteristics in Figure A are for a D/A converter that uses a 3-bit unipolar binary code and an output defined only in terms of its full-scale value.

Table 2: Unipolar Codes–12 Bit Converter
Straight binary and complementary binary

SCALE	+ 10V FS	+ 5V FS	STRAIGHT BINARY			COMPLEMENTARY BINARY		
+ FS–1 LSB	+ 9.9976	+ 4.9988	1111	1111	1111	0000	0000	0000
+ 7/8 FS	+ 8.7500	+ 4.3750	1110	0000	0000	0001	1111	1111
+ 3/4 FS	+ 7.5000	+ 3.7500	1100	0000	0000	0011	1111	1111
+ 5/8 FS	+ 6.2500	+ 3.1250	1010	0000	0000	0101	1111	1111
+ 1/2 FS	+ 5.0000	+ 2.5000	1000	0000	0000	0111	1111	1111
+ 3/8 FS	+ 3.7500	+ 1.8750	0110	0000	0000	1001	1111	1111
+ 1/4 FS	+ 2.5000	+ 1.2500	0100	0000	0000	1011	1111	1111
+ 1/8 FS	+ 1.2500	+ 0.6250	0010	0000	0000	1101	1111	1111
0 + 1 LSB	+ 0.0024	+ 0.0012	0000	0000	0001	1111	1111	1110
0	0.0000	0.0000	0000	0000	0000	1111	1111	1111

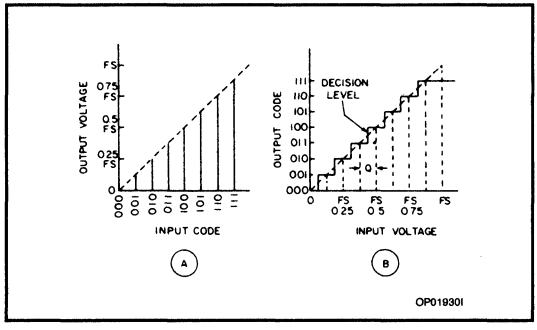
BCD and complementary BCD

SCALE	+ 10V FS	+ 5 V FS	BINARY CODED DECIMAL			COMPLEMENTARY BCD		
+ FS–1 LSB	+ 9.99	+ 4.95	1001	1001	1001	0110	0110	0110
+ 7/8 FS	+ 8.75	+ 4.37	1000	0111	0101	0111	1000	1010
+ 3/4 FS	+ 7.50	+ 3.75	0111	0101	0000	1000	1010	1111
+ 5/8 FS	+ 6.25	+ 3.12	0110	0010	0101	1001	1101	1010
+ 1/2 FS	+ 5.00	+ 2.50	0101	0000	0000	1010	1111	1111
+ 3/8 FS	+ 3.75	+ 1.87	0011	0111	0101	1100	1000	1010
+ 1/4 FS	+ 2.50	+ 1.25	0010	0101	0000	1101	1010	1111
+ 1/8 FS	+ 1.25	+ 0.62	0001	0010	0101	1110	1101	1010
0 + 1 LSB	+ 0.01	+ 0.00	0000	0000	0001	1111	1111	1110
0	0.00	0.00	0000	0000	0000	1111	1111	1111

The ideal A/D converter (Figure B) has a staircase transfer characteristic. Here an analog input voltage or current is converted into a digital word. The analog input is quantized into n levels for a converter with n bits resolution. For the ideal converter, the true analog value corresponding to a given output code word is centered between two decision levels. There are $2^N - 1$ analog decision levels. The quantization size, Q, is equal to the full-scale range of the converter divided by 2^n.

For the ideal D/A converter, there is a one-to-one correspondence between input and output, but for the A/D there is not, because any analog input within a range of Q will give the same output code word. Thus, for a given code word, the corresponding input analog value could have errors of from 0 to ±Q/2. This quantization error can be reduced only by an increase in converter resolution.

Although the analog input or output ranges are arbitrary, some of the standardized ranges include 0 to +5, 0 to +10, 0 to 5 and 0 to 10V for unipolar converters, and 2.5 to +2.5, 5 to 5 and 10 to +10V for bipolar units. Many units on the market are programmable types in which external pin connections determine the range of operation.



Complementary-binary, positive-true coding is also used in D/A converters. This scheme is used because of the weighted current source configuration employed in many converter designs.

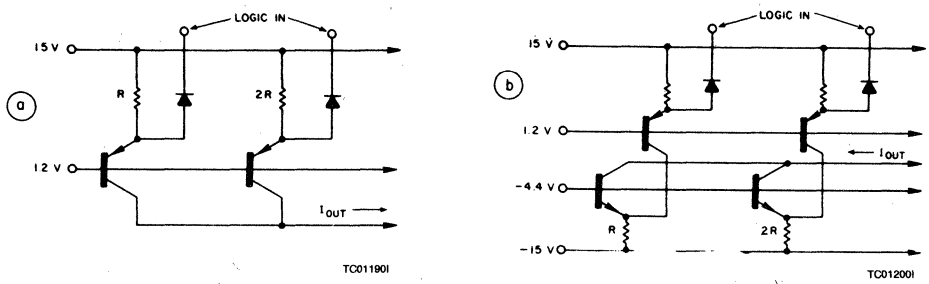


Figure 1: Weighted current-source configurations for straight binary (a) and complementary binary (b) coding generate output current in different directions. The resistor weighting determines the output code.

Figure 1 shows two commonly used weighted-current-source designs. The pnp version (Figure 1a) delivers a positive output current with straight binary positive-true coding. When the logic input is ONE, or +5V, the current source is on, since the input diode is back-biased. Thus the current from each ON weighted current source is summed at the common-collector connection and flows to the output. A ZERO input holds the cathode of the input diode at ground and steals the emitter current from the transistor, keeping it off.

The use of an npn current source (Figure 1b) produces a negative output current with complementary binary positive-true coding. The pnp transistors operate in the same way as before, but each collector is connected to the emitter of an npn weighted current source, which is turned on or off by the pnp transistor. This basic method finds common use in IC quad current-source circuits.

Complementary binary, positive-true, coding is identical to straight binary negative true; these are just two definitions of the same code. Straight-binary, negative-true, coding is commonly used to interface equipment with many minicomputer input output busses. Unipolar A/D converters most frequently use the straight binary positive-true coding. They also use straight-binary inverted-analog where the full-scale code word corresponds to the negative full scale analog value.

Another popular code used in many converters is BCD. Table 2 shows three-decade BCD and complementary BCD codes used with converters that have full-scale ranges of +5 or +10V. BCD is an 8421 weighted code, with four bits used to code each decimal digit. This code is relatively inefficient, since only 10 of the 16 code states for each decade are used. It is, however, a very useful code for interfacing decimal displays and switches with digital systems.

With D/A converters, it is especially convenient to have input decimal codes for use with such equipment as digitally programmed power supplies. And, with A/D converters, BCD is particularly popular for the dual-slope type for direct connection to numeric displays.

BCD coding in converters can be achieved in two ways: binary-to-BCD code conversion or direct weighting of internal resistor ladders and current sources. Today it is almost always done by resistor weighting schemes (Figure 2). Each of the weighted resistors gets switched to a voltage source and thus generates the weighted current for the amplifier. Figure 2a shows an 8-bit binary ladder network. Due to temperature-tracking constraints, groups of four resistors are used. Then the total resistance variation won't exceed 8-to-1.

In between the groups of four resistors is a current divider composed of two resistors that give a division ratio of 16 to 1 between resistor quads. The BCD ladder configuration is similar, with the same values in each of the groups of four resistors. In this case, however, the current divider has a ratio of 10 to 1 between resistor quads. Thus, because of the difference in internal weighting, BCD-coded converters cannot be pin-strapped for another code; they must be ordered only for BCD use.

CODES CAN BE MADE BIPOLAR

Most converters have provision for both unipolar and bipolar operation by external pin connection. The unipolar analog range is offset by one-half of full scale, or by the value of MSB current source, to get bipolar operation (Figure 3). The current source, equal to the MSB current, is derived from the internal voltage reference, so it will track the other weighted current sources with temperature.

For bipolar operation, this current source is connected to the converter's comparator input. Since the current flows in a direction opposite from that of the other weighted sources, its value is subtracted from the input range. With the weighted currents flowing away from the comparator input, the normal input voltage range is positive. Thus the offsetting can change a 0 to +10-V input range into a -5 to +5-V bipolar range.

If the analog range is offset for a converter with straight binary coding, the new coding becomes offset binary. This is the simplest code for a converter to implement, since no change in the coding is required. Table 3 shows offset binary coding for a bipolar converter with a ±5-V input range. All ZEROs in the code correspond to minus full scale. The code word that was originally half-scale becomes the analog zero, 1000 0000 0000. And all ONEs correspond to +5V less one LSB. Successive-approximation A/D converters also have a serial, straight-binary output. This serial output is the result of the sequential conversion process, and it also becomes offset binary when the converter is connected for bipolar operation.

Three other types of binary codes are shown in Table 3, along with the offset binary. Of all four, the two most commonly used are offset binary and two's complement. Some converters use the sign-magnitude binary, but the one's complement is rarely used.

The two's complement code is the most popular because most digital arithmetic is performed in it; thus most interfacing problems are eliminated. The easiest way to characterize the two's-complement code is to look at the sum of a positive and negative number of the same magnitude; the result is all ZEROs plus a carry.

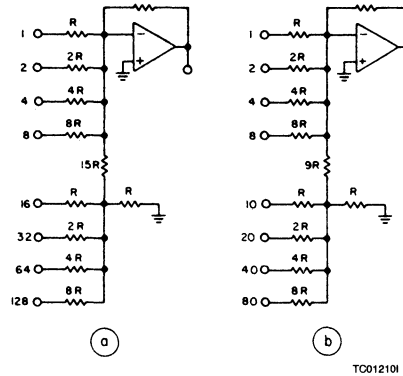


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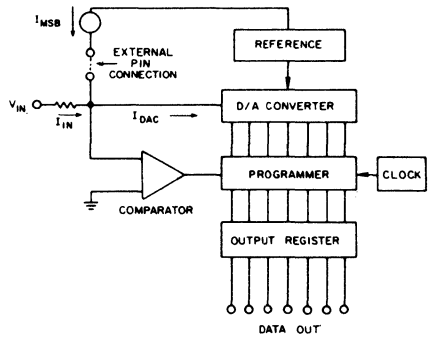
Figure 2: Binary (a) and BCD (b) ladder networks in D/A converters use the same weighting in the resistor quads but different divider ratios.



TC01220I

Figure 3: Most A/D converters for bipolar operation are offset by a current equal to the value of the MSB. The half-scale then becomes 100 . . . 0.

2

Table 3: Bipolar Codes-12 Bit Converter

SCALE	≠5VFS	OFFSET BINARY	TWO'S COMPLEMENT	ONE'S COMPLEMENT	SIGN-MAG BINARY
+FS-1LSB	+4.9976	1111 1111 1111	0111 1111 1111	1111 1111 1111	1111 1111 1111
+3/4fs	+3.7500	1110 0000 0000	0110 0000 0000	0110 0000 0000	1110 0000 0000
+1/2FS	+2.5000	1100 0000 0000	0100 0000 0000	0100 0000 0000	1100 0000 0000
+1/4FS	+1.25000	1010 0000 0000	0010 0000 0000	0010 0000 0000	1010 0000 0000
0	0.0000	1000 0000 0000	0000 0000 0000	0000 0000 0000*	1000 0000 0000*
-1/4FS	-1.2500	0110 0000 0000	1110 0000 0000	1101 1111 1111	0010 0000 0000
-1/2FS	-2.500	0100 0000 0000	1100 0000 0000	1011 1111 1111	0010 0000 0000
-3/4FS	-3.7500	0010 0000 0000	1010 0000 0000	1001 1111 1111	0110 0000 0000
-FS+1 LSB	-4.9976	0000 0000 0001	1000 0000 0000	1000 1111 1111	
-FS	-5.0000	0000 0000 0000	1000 0000 0000	—	—

***NOTE:** One's complement and sign magnitude binary have words for zero as given below: these are designated zero plus two code words zero as given below: these are designated zero plus and zero minus:

	ONE'S COMPLEMENT	SIGN-MAG BINARY
0+	0000 0000 0000	1000 0000 0000
0-	1111 1111 1111	0000 0000 0000

Table 4: Inverted Analog Offset Binary Coding Comparison

SCALE	NORMAL ANALOG OFFSET BINARY	INVERTED ANALOG OFFSET BINARY	NORMAL ANALOG COMP. OFFSET BINARY
+FS		0000 0000 0000	
+FS- 1 LSB	1111 1111 1111	0000 0000 0001	0000 0000 0000
+1/2 FS	1100 0000 0000	0100 0000 0000	0011 1111 1111
0	1000 0000 0000	1000 0000 0000	0111 1111 1111
-1/2 FS	0100 0000 0000	1100 0000 0000	1011 1111 1111
-FS + 1 LSB	0000 0000 0001	1111 1111 1111	1111 1111 1110
-FS	0000 0000 0000		1111 1111 1111

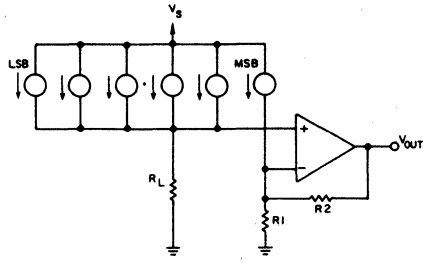


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Figure 4: For two's complement coding in a D/A, the MSB current-source must go to the opposite terminal from the other weighted sources to avoid output glitches.

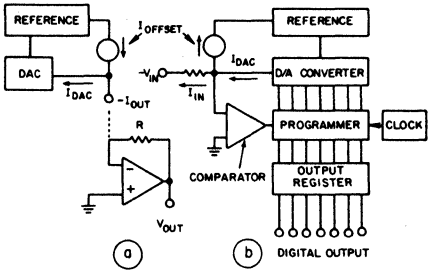

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Figure 5: The inverted-analog D/A converter (a) and the inverted-analog A/D converter (b) have negative-going analog output and input values, respectively.

Visually the only difference between two's complement and offset binary is the left-most bit. In two's complement code it is the complement of the left-most bit in offset binary.

This left-most bit is normally called the MSB; in offset binary it is, in effect, the sign bit, and is so called in the other codes. Thus two's-complement coding is derived from offset binary when the sign bit is complemented and brought out as an additional output.

Coding has its Limitations

Both two's-complement and offset-binary codes have magnitudes (if we temporarily forget about the sign bit) that increase from minus full scale to zero, and, with a sign change, from zero to plus full scale. Both codes have a single definition of zero. On the other hand, one's-complement and sign-magnitude codes have magnitudes that increase from zero to plus full scale and from zero to minus full scale. Both of these codes have two code words for zero, as shown in Table 3. Because of the extra code word used for zero, the range of these codes is one LSB less than for offset-binary and two's-complement coding.

For positive numbers, one-complement is the same as two's-complement. The negative number in one's-complement is obtained when the positive number is complemented. Sign-magnitude coding is identical to offset binary for positive numbers; negative numbers are obtained by use of the positive number with a complemented sign bit.

D/A converters don't usually use two's complement coding. This is because it's hard to invert the MSB weighted current source. If the logic input is inverted, there is an extra digital delay in switching the current source, and this causes large output transients when the current is switched on and off.

The other alternative is to change the direction of the MSB current instead of inverting the digital input. This is also difficult to do and can introduce switching delays.

One satisfactory way of inverting the MSB is shown in Figure 4. Here a voltage output D/A converter that uses two's-complement coding has the MSB current switched into the negative amplifier input terminal, while the other weighted currents are switched into the load resistor and positive input terminal. Thus opposite-polarity output voltages are produced, and there are no additional switching delays in the MSB.

One other code in Table 1 is the sign-magnitude BCD. This code, used mostly in dual-slope A/D converters, usually requires 13 bits for a three-decade digital display. Of the 13 bits, 12 are for the BCD code and one for the sign bit. An additional output bit for an overrange indication is generally supplied.

Another scheme in Table 1 is inverted analog code. This is also called negative reference coding. While most converters use zero to plus full scale as analog values; the inverted configuration uses zero to minus full scale values. The coding then increases in magnitude when the analog level increases in magnitude from zero to minus full scale. For bipolar coding, normal analog has an increasing code as the analog value goes from minus full scale to plus full scale; inverted analog coding does the opposite — the

code increases as the analog value goes from plus full scale to minus.

Why the need for this code? Figure 5a shows a D/A converter that delivers a negative output current. With bipolar operation and use of the offset current source, the converter provides a code ZERO that corresponds to plus full scale output current. However, if a current-to-voltage converter is used at the output, an inversion takes place, and a normal analog output voltage results.

In Figure 5b, a D/A converter with positive output current is used in an A/D converter. Since the D/A output current is summed with the offset and input current at the comparator input, a negative input voltage is needed to balance these currents. The analog input thus goes from plus full scale to minus full scale for an increasing output code. Normal analog coding is achieved by use of an inverting amplifier ahead of the analog input terminal.

Inverted analog coding is compared with the normal offset binary coding in Table 4. This comparison shows that if the inverted analog offset binary code is rotated around the zero of the analog voltage, a normal analog offset binary output results. If inverted analog offset binary is compared with normal analog complementary offset binary, the two codes will appear identical except for an offset of one LSB. The relationship between these two codes can be expressed as:

Normal analog complementary binary
+ 1 LSB = Inverted analog offset binary.

Therefore a converter that uses one of these codes can also be used for the other with an external offset adjustment of 1 LSB.

AO42
Interpretation of Data Converter Accuracy Specifications

Cognizance of accuracy factors involved when interfacing data converters into system applications permits designers to meet overall error budget constraints. Transfer functions; quantization noise; offset, gain, and linearity errors; and temperature effects must be interpreted to satisfy specification requirements

Analog-to-digital and digital-to-analog converters are widely utilized to interface between the physical world of analog measurements and the computational world of digital computers. Dating from the early 1950s, the application of data converters has increased enormously as the use of minicomputers and microcomputers has grown. Typical applications of data converters involve the areas of process control and measurement where the inputs and outputs of the system must be in analog form, yet the computation and control functions are performed digitally. In such a system, input variables such as temperature, flow, pressure, and velocity must be converted into electrical form by a transducer, then amplified and converted into digital form by an analog-to-digital converter for the computer to process.

Since the computer not only measures and determines the state of a process, but also controls it, its computations must be employed to close the loop around the system. This is done by causing the computer to actuate inputs to the process itself, thus controlling its state. Because the actuation is done by analog control parameters, the output of the digital computer must be converted into analog form by a digital-to-analog converter. Such a closed loop feedback control system is shown in Figure 1.

Interfacing by analog-to-digital (A/D) and digital-to-analog (D/A) converters performs a vital role. At the present time, it is estimated that at least 15% of all microcomputers function in such control and measurement applications where data converters are required; this percentage is expected to grow to about 40% within a few years. For the designer of such computer controlled systems, it is fortunate that a broad choice of data converters exists. In fact, a virtual supermarket of A/D and D/A converters of all prices, sizes, and performance specifications is available. This spectrum of converters encompasses those from simple 8-bit monolithic devices costing a few dollars, through better performing hybrid devices with higher resolution, to higher cost discrete module converters with the best performance characteristics.

Design selection involves not only price and size, but also many facets of performance: resolution, linearity, temperature coefficient, speed, and various self-contained options. In the realm of A/D converters (ADCs), there is also the choice between basic conversion methods, such as successive approximation, dual-slope integrating, and parallel (or flash) techniques. Furthermore, there exists a choice between three competing technologies: monolithic, hybrid, and modular, each with its own specific advantages. Since A/D and D/A converters are basically analog circuits that have digital inputs or outputs, the computer systems engineer who may be mostly familiar with digital techniques must become familiar with the many analog specifications describing data converter performance in order to choose the correct converter for a specific requirement.

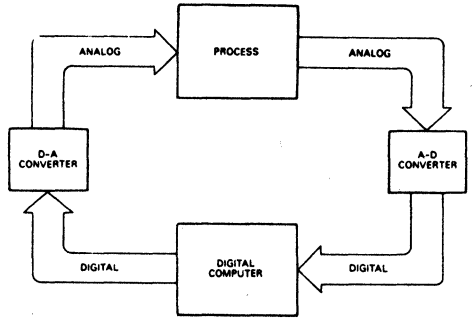

Figure 1: Computer controlled feedback control system. Computer closes loop around process to control its state. However, two interfaces are required: A/D converter and D/A converter

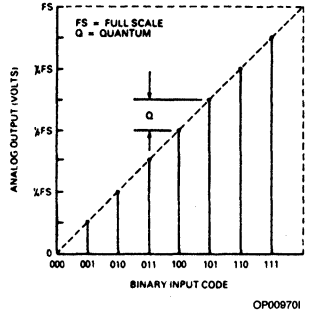

Figure 2: Ideal DAC transfer function. This I/O graph is shown for 3-bit DAC which has one-to-one correspondence between input and output

DATA CONVERTER TRANSFER FUNCTIONS

Figure 2 shows the transfer function of an ideal 3-bit D/A converter (DAC). This converter is assumed to be of the parallel type, as are virtually all DACS in use today. A

parallel DAC responds simultaneously to all digital input lines whereas a serial DAC responds sequentially to each digital input. The transfer function representing a 3-bit DAC is a discontinuous function; its analog output voltage or current changes only in discrete analog steps, or quanta, rather than continuously. However, a one-to-one correspondence exists between the binary input code and the analog output value. For each input code there is one, and only one, possible output value. Analog step magnitude, or quantum, is shown as Q.

The horizontal axis is the input binary code, in this case a 3-bit code, increasing from 000 to 111. The number of output states, or quanta, is 2^n, where n is the number of bits in the code. For a 3-bit DAC, the number of states is 2^3 or 8; for a 12-bit DAC, the number of states is 2^{12} or 4096.

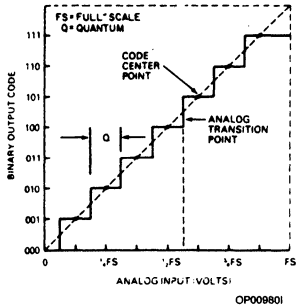

Figure 3: Ideal ADC transfer function. I/O graph illustrates 3-bit ADC which has quantized characteristic

Figure 3 illustrates the transfer function for an ideal 3-bit ADC. This transfer function is also discontinuous but without the one-to-one correspondence between input and output. An ADC produces a quantized output from a continuously variable analog input. Therefore, each output code word corresponds to a small range (Q) of analog input values. The ADC also has 2^n output states and $2^n - 1$ transition points between states; Q is the analog difference between these transition points.

For both ADCs, Q represents the smallest analog difference that the converter can resolve. Thus, it is the resolution of the converter expressed in analog units. Resolution for an A/D or D/A converter, however, is commonly expressed in bits, since this defines the number of states of the converter. A converter with a resolution of 12 bits, then, ideally resolves 1 part in 4096 of its analog range.

For an ideal ADC or DAC, Q has the same value anywhere along the transfer function. This value is Q = FSR 2^n, where FSR is the converter's full-scale range — the difference between the maximum and minimum analog values. For example, if a converter has a unipolar range of 0 to 10V or a bipolar range of −5 to 5V, FSR in both cases is 10V. Q is also referred to as one least significant bit (LSB), since it represents the smallest code change the converter can produce, with the last bit in the code changing from 0 to 1 or 1 to 0.

Notice in the transfer functions of both A/D and D/A converters that the output never reaches full scale. This results because full scale is a nominal value that remains the same regardless of the resolution of the converter. For example, assume that a DAC has an output range of 0 to 10V; then 0V is nominal full scale. If the converter has an 8-bit resolution, its maximum output is 255/256 x 10 V = 9.961V. If the converter has 12-bit resolution, its maximum output voltage is 4095/4096 x 10 V = 9.9976V.

In both cases, maximum output is one bit less than indicated by the nominal full-scale voltage. This is true because analog zero is one of the 2^n converter states; therefore, there are only $2^n - 1$ steps above zero for either an A/D or D/A converter. To actually reach full scale would require $2^n + 1$ states, necessitating an additional coding bit. For simplicity and convenience then, data converters always have the analog range defined as nominal full scale rather than actual full scale for the particular resolution implemented.

In the transfer functions of Figures 2 and 3, a straight line is passed through the output values in the case of the DAC and through the code center points in the case of the ADC. For the ideal converter, this line passes precisely through zero and full scale. Table 1 summarizes the characteristics of the ideal A/D or D/A converter for the most commonly applied resolutions.

QUANTIZATION NOISE AND DYNAMIC RANGE

Even an ideal A/D or D/A converter has an irreducible error, which is quantization uncertainty or quantization noise. Since a data converter cannot distinguish an analog difference less than Q, its output at any point may be in error by as much as ±Q/2.

Figure 4(a) shows an ideal ADC and an ideal DAC that digitize and then reconstruct an analog slow-voltage ramp signal. The ADC and output register are both triggered together so that the DAC is updated in synchronism with the A/D conversions. The DAC output ramp is identical with the analog input ramp except for the discrete steps in its output (not counting time delay). If the output ramp is subtracted from the input ramp as shown, the difference is the quantization noise — a natural result of the conversion process. This noise [Figure 4(b)] is simply the difference between the transfer function and the straight line shown in Figure 3. Quantization noise from an ideal conversion is therefore a triangular waveform with a peak-to-peak value of Q.

TABLE 1
SUMMARY OF DATA CONVERTER CHARACTERISTICS

RESOLUTION (n)	STATES (2^n)	BINARY WEIGHT (2^{-n})	Q FOR 10 V FS	S/N RATIO (dB)	DYNAMIC RANGE (dB)	MAX OUTPUT FOR 10 V FS (V)
4	16	0.0625	0.625 V	34.9	24.1	9.3750
6	64	0.0156	0.156 V	46.9	36.1	9.8440
8	256	0.00391	39.1 mV	58.9	48.2	9.9609
10	1024	0.000977	9.76 mV	71.0	60.2	9.9902
12	4096	0.000244	2.44 mV	83.0	72.2	9.9976
14	16384	0.0000610	610 μV	95.1	84.3	9.9994
16	65536	0.0000153	153 μV	107.1	96.3	9.9998

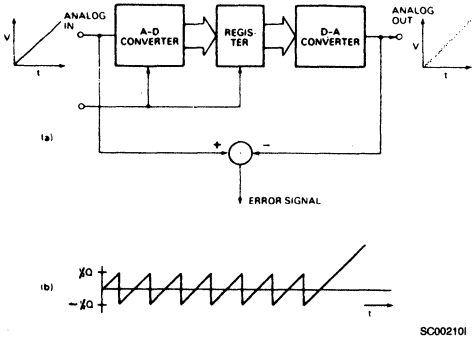

Figure 4: Signal digitization and reconstruction (a) and quantization noise (b). Quantization noise is shown as difference between input and output for ideal data conversion system

As with most noise sources, the average value is zero, but the rms value is determined from the triangular shape to be E_n (rms) = $Q/\sqrt{12}$. Thus, a data conversion system can be thought of as a simple signal processor that adds noise to the original signal by virtue of the quantization process. Since this noise is an inherent part of the conversion process, it cannot be eliminated except with a converter of infinite resolution. The best that can be done, even with ideal converters, is to reduce it to a level consistent with desired system accuracy. This is done by using a converter with sufficiently high resolution.

In many computerized signal processing applications, it is necessary to determine the signal-to-noise (S/N) ratio, which is a power ratio expressed in decibels. It can be found from the ratio of peak-to-peak signal to rms noise as follows.

$$\text{S/N Ratio (dB)} = 10 \log \left[\frac{2^n Q}{Q/\sqrt{12}}\right]^2$$

$$= 20 \log 2^n + 20 \log \sqrt{12}$$

$$= 6.02n + 10.8 \qquad (1)$$

The S/N ratio increases by a factor of about 6dB for each additional bit of resolution.

Dynamic range of a data converter, another useful term, is found from the ratio of FSR to Q. This ratio is the same as the number of converter states.

$$\text{Dynamic Range (dB)} = 20 \log 2^n = 20n \log 2 = 6.02n \qquad (2)$$

Therefore, simply multiplying the number of bits of resolution by 6dB gives the dynamic range. S/N ratio and dynamic range are summarized for the most popular resolutions in Table 1.

NON-IDEAL DATA CONVERTERS

Real A/D and D/A converters exhibit a number of departures from the ideal transfer functions just described. These departures include offset, gain, and linearity errors (Figure 5), all of which appear simultaneously in any given data converter. In addition, the errors change with both time and temperature. In Figure 5(a), the ADC transfer function is shifted to the right from the ideal function. This offset error is defined as the analog value by which the transfer function fails to pass through zero; it is generally specified in millivolts or in percent of full scale.

In Figure 5(b), the converter transfer function has a slope difference from the ideal function. This gain, or scale factor, error is defined as the difference in full-scale values between the ideal and actual transfer functions when the offset error is zero; gain error is expressed in percent.

An ADC transfer function in Figure 5(c) exhibits linearity error, a curvature from the ideal straight line. Linearity error, or nonlinearity, is the maximum deviation of the transfer function from a straight line drawn between zero and full scale; it is expressed in percent or in LSBs (such as $\pm 1/2$ LSB). Figure 5(d) shows the total error of a non-ideal ADC, which contains offset, gain, non-linearity, and quantization errors. Compare this curve with that of Figure 4(b).

Fortunately, most A/D and D/A converters on the market today have provision for trimming out the initial offset and gain errors. By means of two simple external potentiometer adjustments, the offset and gain errors can be virtually reduced to zero or within the limits of measurement accuracy. Then, only the linearity error remains.

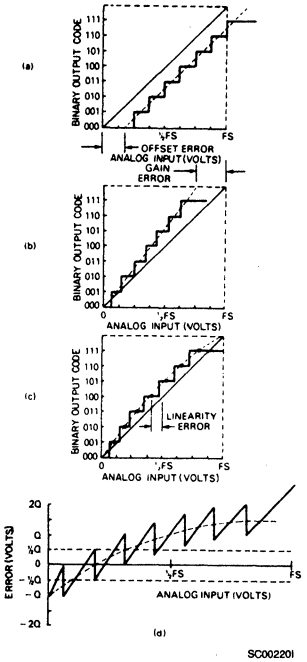

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Figure 5: Errors in nonideal A/D converters. Transfer functions are shown for ADCs with offset error (a), gain error (b), and linearity error (c). ADC with all three errors present will have quantization error as shown in (d)

NONLINEARITY

Linearity error is the most difficult error to deal with since it cannot be eliminated by adjustment. Like quantization error, it is an irreducible error. Basically, there are just two methods to reduce linearity error, both of which are expensive: either use a higher quality converter with better linearity, or perform a digital error correction routine on the data using a computer. The latter, of course, may not be feasible in many applications. There is some merit in using a more expensive converter, however. For example, suppose that an ultra-linear 8-bit ADC is required. Most good quality converters have linearity errors specified to less than ± ½ LSB. If a more expensive 12-bit ADC is employed with only 8 output bits used, then its linearity error of ± ½ LSB out of 12 bits is the same as ± 1/32 LSB out of 8 bits. This converter, therefore, becomes an ultralinear 8-bit ADC and probably at not too great an additional cost.

Actually, two types of linearity errors existing in A/D and D/A converters are integral linearity error and differential linearity error. Integral linearity error in Figure 5(c) is due to the curvature of the transfer function, resulting in departure from the ideal straight line. The definition given for integral linearity error as the maximum deviation of the transfer function from a straight line between zero and full scale is a conservative one used by most data converter manufacturers. It is an "end-point" definition, as contrasted with the normal definition of linearity error as the maximum deviation from the "best-fit" straight line.

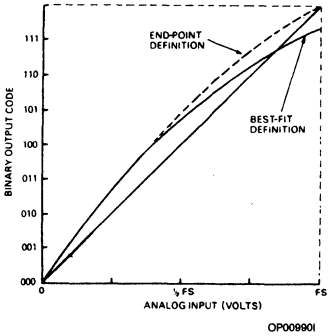

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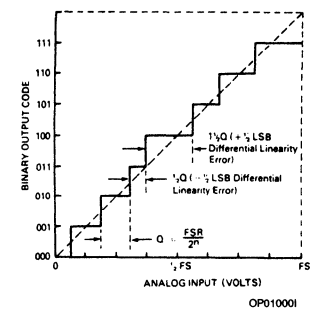
Figure 6: Comparison of linearity error definitions. Curves illustrate end-point and best-fit definitions of linearity error in an ADC

Since determining the best-fit straight line for data converters can be a tedious process when calibrating the device, most manufacturers have opted for the more conservative definition. This means that the converter must be aligned accurately at zero and at full scale to realize the specified linearity. The end-point definition can mean a linearity that is twice as good as a best-fit definition, as illustrated in Figure 6. Notice that the curvature may be twice as great with the best-fit straight line definition.



OP01000I

Figure 7: Definition of differential linearity error. This transfer function illustrates ± ½ LSB differential linearity errors. Differential linearity error of zero means that every step in transfer function has size of precisely Q

Differential linearity error is the amount of deviation of any quantum from its ideal value. In other words, it is the deviation in the analog difference between two adjacent codes from the ideal value of FSR/2^n. If a data converter has ± ½ LSB maximum differential linearity error, then the actual size of any quantum in its transfer function is between ½ LSB and 1 ½ LSB; each analog step is 1 ± ½ LSB.

Figure 7 illustrates the definition. The first two steps shown are the ideal value $Q = FSR/2^n$. The next step is only ½Q, and above this is 1½Q. These two steps are at the limit of the specification of ±½ LSB maximum differential linearity error. Most data converters today are specified in terms of both integral and differential linearity error. In production testing of data converters, quanta sizes are measured over the converter's full-scale range.

Two other important terms are commonly used in conjunction with the differential linearity error specification. The first is monotonicity, which applies to DACs. A monotonic DAC has an analog output that is a continuously increasing function of the input. The DAC transfer function shown in Figure 8(a) is monotonic even though it has a large differential linearity error. The transfer function of Figure 8(b), on the other hand, is nonmonotonic since the output actually decreases at one point. In terms of differential linearity error, a DAC may go nonmonotonic if the differential linearity error is greater than ±1 LSB at some point; if the differential linearity error is less than ±1 LSB, it assures that the output is monotonic.

The term missing, or skipped, code applies to ADCs. When the differential linearity error of an ADC is greater than ±1 LSB, the output may have a missing code; if the differential linearity error is less than ±1 LSB, it assures that there are no missing codes. Figure 9(a) shows the transfer function of an ADC with a large differential linearity error but with no missing codes. In Figure 9(b), however, the differential linearity error causes a code to be skipped in the output.

For ADCs, the linearity characteristic depends on the technique of A/D conversion used; each converter type exhibits its own specific nonlinearity characteristic. Figure 10 illustrates the nonlinearity characteristics of the two most popular types of ADCs: successive approximation and dual-slope integrating. With the successive approximation ADC, and also with other feedback type ADCs that use a parallel input DAC in the feedback loop, differential linearity error is the dominant type of nonlinearity. This is due to the parallel input DAC, which is made up of weighted current sources. The worst differential linearity errors occur at the major code transitions, such a ¼, ½, and ¾ scale. If these differential linearity errors are small, then the integral linearity error will also be small.

The difficulty at the major transition points is that, for example, the most significant bit current source is turning on while all other current sources are turning off. This subtraction of currents must be accurate to ±½ LSB and is a severe constraint in high resolution DACs. This means that the weighted current sources must be precisely trimmed in manufacturing. The most difficult transition is at ½ scale, where all bits change state (eg, for an 8-bit converter, 01111111 to 10000000), and the worst differential linearity error generally occurs here.

The next most difficult transitions occur at ¼ scale and ¾ scale, where all but one of the bits change state (eg, for an 8-bit converter, 00111111 to 01000000 and 10111111 to 11000000, respectively). Relatively smaller differential linearity errors may also occur at the ⅛, ⅜, ⅝, and ⅞ scale transitions, and so on. Figure 10(a) shows a successive approximation ADC transfer function, illustrating exaggerated differential linearity errors at ¼, ½, and ¾ scale. If these errors are properly trimmed out in manufacturing, then both differential and integral linearity errors will be less than ±½ LSB.

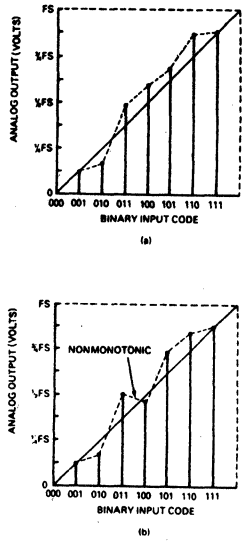


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Figure 8: Monotonic (a) and nonmonotonic (b) DAC outputs. Monotonicity means output is continuously increasing function of input

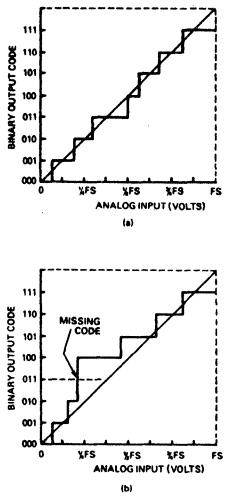

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Figure 9: No missing code (a) and missing code (b) in ADC output. Differential linearity error of less than ±1 LSB assures that there are no missing codes in transfer function

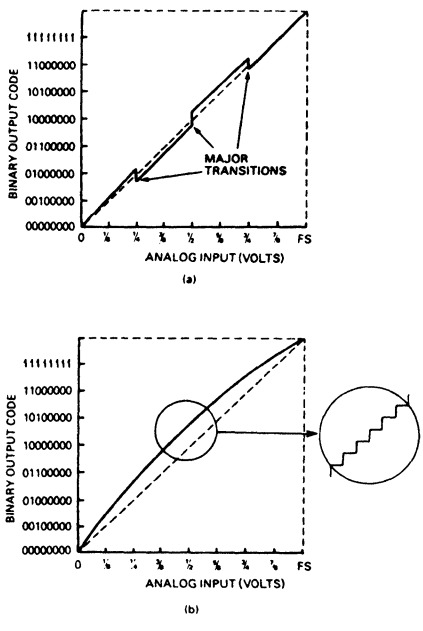

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Figure 10: Linearity characteristic of successive approximation (a) and dual slope integrating (b) ADCs. Transfer function of successive approximation converter exhibits mostly differential linearity error while that of integrating converter shows mostly integral linearity error

Figure 10(b) shows a dual-slope integrating ADC transfer function. In this case, the predominant nonlinearity is the integral linearity error; differential linearity error is almost nonexistent in integrating type ADCs, which also includes charge balancing ADCs. The curvature of the transfer function is caused by a nonideal integrator circuit. Differential linearity is determined by the time between clock pulses in the converter, and this is constant within any conversion cycle.

TEMPERATURE INDUCED ERRORS

Ambient temperature changes cause variations in offset, gain, and linearity errors. If a converter is operated at a constant temperature within its specified operating temperature range, offset and gain errors can be zeroed by external adjustment at that temperature. But if the converter must operate with changing ambient temperature, then the problem becomes acute.

Offset change with temperature is generally specified in microvolts per degree Celsius, or in parts per million of full scale per degree Celsius. Gain temperature coefficient is specified in parts per million per degree Celsius, and linearity error change with temperature is expressed in parts per million of full scale per degree Celsius.

Effective approaches to minimizing gain and offset changes with temperature are available. If a converter operates most of the time at a given temperature, then its offset and gain should be zeroed at that temperature. If, however, the ambient temperature varies between two temperatures, the converter should be calibrated midway between those two temperatures. Another approach to minimizing changes with temperature is to use a converter with a low temperature coefficient to meet the desired specification. Data converters with low temperature coefficients are, of course, more expensive, but this may be the most economical solution to the problem when all design factors are considered. Another method of minimizing gain error is based on the fact that many data converters with internal references have provision for connecting an external reference. In such a case, it is possible to connect a lower temperature coefficient external reference to the converter. This can be particularly effective where a number of converters are used together and one reference is used for all of them.

Linearity error temperature coefficient is the most troublesome specification, since it resists correction. In many applications, it is desired that the converter be monotonic, or have no missing codes, over the desired operating temperature range. From the converter differential linearity temperature coefficient, it is useful to determine the temperature range over which the converter will have guaranteed monotonicity or no missing codes. Using a conservative approach, it is assumed that the converter has a maximum initial differential linearity error of ±½ LSB. Then, if the differential linearity error changes by not more than an additional ½ LSB, a DAC will remain monotonic and an ADC will have no missing codes.

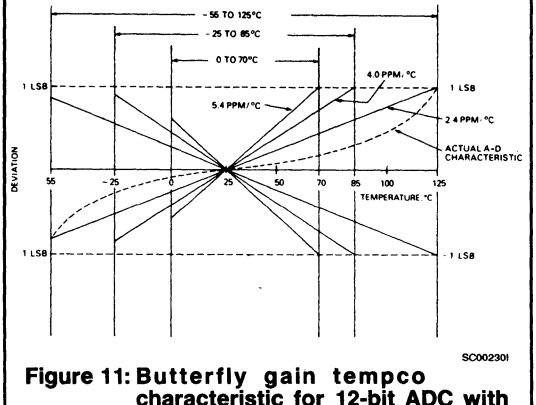

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Figure 11: Butterfly gain tempco characteristic for 12-bit ADC with ±1 LSB maximum gain error. Converter is calibrated for zero gain error at 25°C. Limits shown are for ±1 LSB error out of 12 bits over designated temperature range

With a 12-bit ADC for example, ½ LSB is equal to 120ppm. If the operating temperature range is 0 to 70°C and the converter is calibrated at 25°C, the maximum temperature change is 70°C – 25°C, or 45°C. To guarantee

no missing codes, the differential linearity temperature coefficient must be 120ppm/45°C = 2.7ppm/°C of full scale, maximum. An even lower differential linearity temperature coefficient is required to assure no missing codes if the operating temperature range is the full −55°C to 125°C military range. Performing a similar computation gives 120ppm/100°C = 1.2ppm/°C of full scale, maximum, for the differential linearity temperature coefficient.

Gain temperature coefficient is commonly specified by the butterfly limits shown in Figure 11. All the lines pass through zero at 25°C, where it is assumed that the initial measurement is made. The graph of Figure 11 shows the maximum gain temperature coefficient required for a ±1 LSB gain error for a 12-bit A/D or D/A converter over three different temperature ranges. Observe that the gain deviation curve must be within the bounds shown to meet the specification of ±1 LSB maximum change. The dotted curve shows an actual converter gain deviation that would qualify as a gain temperature coefficient of ±2.4ppm/°C over the −55 to 125°C operating temperature range. This represents a very low temperature coefficient for an actual converter since most available devices fall in the range of 5 to 50ppm/°C.

ERROR BUDGET SUMMARY

A common mistake in specifying data converters is to assume that the relative accuracy of a converter is determined only by the number of resolution bits. In fact, achievable relative accuracy is likely to be far different from the implied resolution, depending on the converter specifications and operating conditions. This simply means that the last few resolution bits may be meaningless in terms of realizable accuracy.

The best way to attack this design problem is with a systematic error budget. An error budget partitions all possible errors by source to arrive at a total error. In a given system, this must be done not only for the A/D or D/A converter, but also for the other circuits, such as transducer, amplifier, analog multiplexer, and sample and hold.

As an example, using the accuracy specifications for a typical 12-bit ADC (Table 2), an error budget can be determined based on the following assumptions: operating temperature range of 0°C to 50°C, maximum power supply voltage change of 1% with time and temperature, and maximum converter change of 0.02% with time. Table 3 shows the resulting error budget with a total worst case error of 0.1135%. It is improbable that the errors will all add in one direction. Statistical (rms) addition of the errors yields a lower value of 0.0581%; this, on the other hand, may be too optimistic since the number of error sources is small. At any rate, the maximum error will be somewhere between 0.0581% and 0.1135%, a significant difference from what might be assumed as a 12-bit or 0.024% converter. The ideal relative accuracy has been degraded by one to two resolution bits.

In applying data converters, best results are achieved by reading the data sheet carefully for accuracy specifications, computing total error by the error budget method, and then carefully aligning and testing the converter in its actual application.

TABLE 2
ACCURACY SPECIFICATIONS FOR 12-BIT ADC

CHARACTERISTIC	VALUE
Resolution	12 Bits
Differential Linearity Error	±½ LSB max
Differential Linearity Tempco	±2ppm/°C of FSR max
Gain Tempco	±20ppm/°C max
Offset Tempco	±5ppm/°C of FSR max
Power Supply Sensitivity	0.002%/%

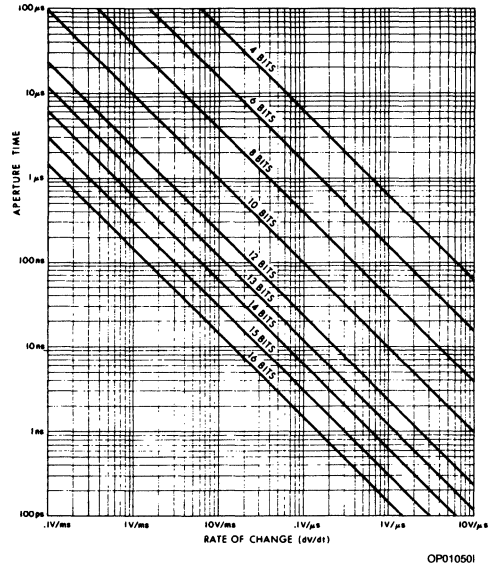
TABLE 3
ERROR BUDGET FOR 12-BIT ADC

SPECIFICATION	ERROR (%)
Quantization Error (±½ LSB)	0.012
Differential Linearity Error (±½ LSB)	0.012
Differential Linearity Error over Temp (2 ppm/°C x 25)	0.005
Gain Change over Temp (20ppm/°C x 25)	0.05
Zero Change over Temp (5ppm/°C x 25)	0.0125
Change with Power Supply (1 x 0.002%)	0.002
Long Term Change	0.02
Total Error, Worst Case	0.1135
Total Statistical (rms) Error	0.0581

Graphs give aperture time required for A/D conversion

The time required for an analog-to-digital converter to make a conversion is known as "aperture time," and depends on both the resolution and the particular conversion method employed. For commercially available A/D converters that use the successive approximation method, the aperture time may be 40 microseconds for a relatively low-cost 12-bit converter, or as little as 4μs for a more expensive high-speed 12-bit converter. In many cases a sample-hold circuit is used ahead of an A/D converter to effectively reduce the aperture times; the sample-hold can take a very fast sample of the analog signal and then hold the value while the A/D operation is performed. (The time interval during which the signal-hold circuit turns off is then the aperture time, and determines the conversion accuracy. The time for actual A/D conversion can be longer.)

It is important for the designer to know what aperture time is required to keep the system error to a tolerable value in terms of the resolution of his A/D converter. The maximum aperture time that allows 1-bit accuracy in conversion of an analog signal to 4 bits, 6 bits, . . . or 16 bits is given here in two useful graphs. The graph in Figure 12(a) shows this aperture time as a function of signal rate of change, for signals that are 10 volts full scale or peak to peak. Figure 12(b) gives the aperture time as a function of the frequency of a sinusoidal signal.



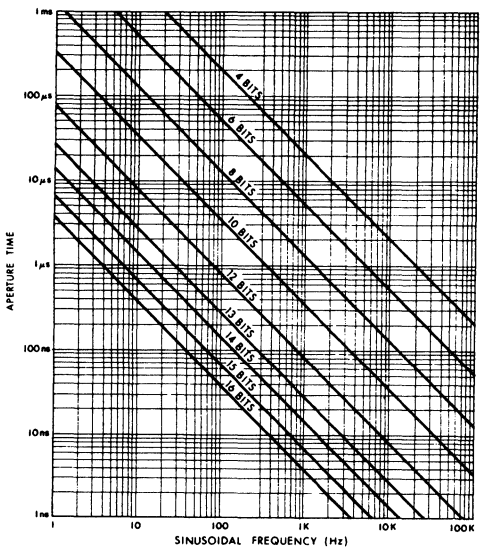


Figure 12: Sampling time. Aperture time for 1-bit accuracy at various resolutions in A/D conversion are shown here. Graph (a) gives aperture time as a function of signal rate of change for signals that are 10 volts full scale or 10 volts peak to peak. Graph (b) gives aperture time as a function of frequency for sinusoidal signals. Aperture times for larger allowed error can be found by reading on line for lower resolution, e.g., a 2-bit error and 8-bit resolution requires the same time as a 1-bit error and 7-bit resolution. Equations for these graphs are found in text.

The two graphs are derived with reference to Figure 13, which shows a time-varying signal and the amplitude uncertainty ΔV associated with an aperture time t_A

$$t_A = \Delta V/(dV/dt)$$

If the fractional error e is the ratio of ΔV to full-scale voltage V_{FS},

$$t_A = (\epsilon\ V_{FS})/(dV/dt)$$

If ΔV is held to 1 bit, and V_{FS} is resolved into n bits, then $\epsilon = 1/(2^n)$, and

$$t_A = V_{FS}/2^n(dV/dt)$$

This is the equation for the family of lines in Figure 1(a), with $V_{FS} = 10$ volts and $n = 4,6,\ldots 16$.

For a sinusoidal signal, which has a maximum rate of change at its zero crossing,

$$\Delta V = t_A[d/dt(1/2)(V \sin \omega t)]_{t-0} = \omega V t_A/2$$

where V is peak-to-peak signal value. This gives

$$t_A = (2\Delta V)/(\omega V) = \epsilon/\pi f = 1/(2^n \pi f)$$

for a 1-bit error and n-bit resolution. This is the equation for the family of lines in Figure 12(b).

If the allowed error is to be 2 bits instead of 1 bit, then $\epsilon = 2/(2^n)$, so aperture times are doubled. An error of 3 bits gives $\epsilon = 4/(2^n)$, and so on; thus a 1-bit increase in error is equivalent to a 1-bit decrease in resolution on the graphs.

As an example of the usefulness of these graphs, assume that a 1-kilohertz sinusoidal signal is to be digitized to a resolution of 10 bits. What aperture time must be used to give less than 1 bit of error? The answer, readily found from Figure 12(b), is 320 nanoseconds. For 1/2 bit error the aperture time would have to be 160ns. This is surprising, because a 1-kHz signal is really not very fast, and a 10-bit/320-ns converter is not to be found commercially available as a module. Therefore, a sample-hold circuit would be required ahead of a slower A/D converter.

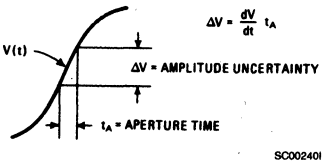


Figure 13: Error. Possibility of error in A/D conversion depends upon aperture time. The greater t_A is, the greater the uncertainty in value of an analog voltage that has been converted to digital level.

DO'S AND DON'TS OF APPLYING A/D CONVERTERS

In many applications, the limitation in the performance of any system lies in how the individual components are used. The Analog-to-Digital Converter (A/D) can also be considered as a component and, therefore, proper design procedures are necessary in order to obtain the optimum accuracy. Intersil IC A/D converters are inherently extremely accurate devices. To obtain the optimum performance from them, care should be taken in the hook-up and external components used. Test equipment used in system evaluation should be substantially more accurate and stable than the system needs to be. The following sections illustrate DO's and DON'Ts to obtain the best results from any system.

DON'T INTRODUCE GROUND LOOP ERRORS

Plan your grounding carefully. Probably the most common source of error in any Analog-Digital system is improper grounding. Let's look at Figure 14. All the grounds are tied together, so everything should be alright, right? WRONG! Almost everything is wrong with this connection.

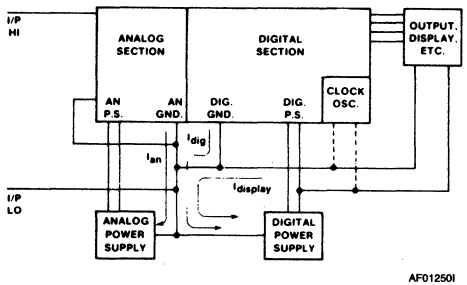


Figure 14: Don't hook it up like this!

The power supply currents for the analog and digital sections, together with the output or display currents, all flow through a lead common to the input. Let us analyze some of the errors we have introduced. The average currents flowing in the resistance of the common lead will generate a D.C. offset voltage. Even the autozero circuit of an integrating A/D converter cannot remove this error. But, in addition, this current will have several varying components. The clock oscillator, and the various digital circuits driven from it, will show supply current variation at the clock frequency, and usually at submultiple also. For a successive approximation converter, these will cause an additional effective offset. For an integrating converter, at least the higher frequency components should average out. In some converters, the analog supply currents will also vary with the clock (or a submultiple) frequency. If the display is multiplexed, that current will vary with the multiplex frequency, usually some fraction of the clock frequency. For an integrating converter, both digital and analog section currents will change as the converter goes from one phase of conversion to another. (Currents of this type injected into an autozero loop are particularly obstinate). Another serious source of variation is the change in digital and display section currents with the result value. This frequently shows up as an oscillating result, and/or missing results; one value being displayed displaces the effective input to a new value, which is converted and displayed, leading to a different displacement, a new value and so on. This sequence usually closes after two or three values, which are displayed in sequence.

A more subtle source of errors in this circuit comes from the clock oscillator frequency. For an integrating converter, variations in clock frequency during a single conversion cycle due to varying digital supply voltage or supply currents, or ground loops to a timing capacitor, will lead to incorrect results.

Figure 15 shows a much better arrangement. The digital and analog grounds are connected by a line carrying only the interface currents between sections, and the input section is also tied back by a low-current line. The display-current loop will not affect the analog section and the clock section is isolated by a decoupling capacitor. Note that external reference return currents and any other analog system currents must also be returned carefully to analog ground.

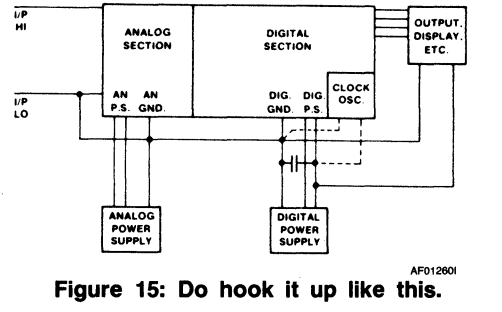


Figure 15: Do hook it up like this.

DON'T COUPLE DIGITAL SIGNALS INTO ANALOG LINES

Although Intersil's A/D converter circuits have been designed to minimize the internal coupling of digital signals into analog lines, the external capacitive coupling is controlled by the user. For the best results, it is advisable to keep analog and digital sections separated on PC boards. A few examples of the results of capacitive coupling follow.

On dual slope converters, the "busy" line swings from one state to the other at the end and beginning of the autozero cycle. Capacitive coupling from this line to the autozero or integrating capacitors will induce an effective input offset voltage. A similar effect occurs with the "Measure/Zero" line on charge-balancing converters and for a successive approximation converter with coupling between "End of Conversion" and a sample-and-hold capacitor. For a multiplexed display device, coupling between the multiplex or "digit" lines and these capacitors can lead to non-linearity of the converter. And coupling from any digital line into a high-impedance input line can lead to errors in any system.

DO USE ADEQUATE QUALITY COMPONENTS

For successive approximation converters, the resistors used must have excellent time and temperature stability to maintain accuracy. Any adjustment potentiometers, etc. must be of compatible quality (note that in some trimpots, the slider position moves with temperature!)

For dual slope converters, the component selection is less critical. Long term drifts in the integrating resistor and the capacitors are not important. However, any resistive divider used on the reference, especially if it is adjustable, must be of sufficient stability not to degrade system accuracy. Dielectric absorption in the integrating capacitor is important (see reference 1) and the integrating resistor must have a negligible voltage coefficient to ensure linearity. Noisy components will lead to noisy performance, whether in the integrator, autozero or clock circuits.

DO USE A GOOD REFERENCE

Good references are like good wines; nobody is quite sure how to make them but generally the older the technology used, the better the result, and the proof lies in the tasting (or testing). Thus, it is hard to beat the old temperature compensated zener with the current flow adjusted to the optimum for each diode. If you aren't into Zinfandel Superior Premier Cru (1972), the Intersil 8052 has a fairly good reference built in. In either case, the division down from what you get to the required reference voltage requires care also (see above). And it is a fundamental fact that no converter can be better than its reference voltage.

DO WATCH OUT FOR THERMAL EFFECTS

All integrated circuits have thermal time constants of a few milliseconds to dissipation changes in the die. These can cause changes in such parameters as offset voltages and V_{be} matching. For example, the power dissipation in an 8018 quad current switch depends on the digital value. Although the die is carefully designed to minimize the effects of this, the resultant temperature changes will affect the matching between current switch values to a small degree. Inappropriate choice of supply voltages and current levels can enhance these differences, leading to errors. Similarly, the power dissipated in a dual-slope converter circuit depends on the comparator polarity and hence varies during the conversion cycle. Offset voltage variations due to this cannot be autozero'd out, and so can lead to errors. Again a poor choice of comparator loading or swing will enhance this (normally) minor effect. The power dissipation in an output display could be coupled into the sensitive analog sections of a converter, leading to similar problems. And thermal gradients between IC packages and PC boards can lead to thermo-electric voltage errors in very sensitive systems.

DO USE THE MAXIMUM INPUT SCALE

To minimize all other sources of error, it is advisable to use the highest possible full scale input voltage. This is particularly important with successive approximation converters, where offset voltage errors can quickly get above 1LSB, but even for integrating-type converters, noise and the various other errors discussed above will increase in importance for lower-than-maximum full scale ranges. Preconverter gain is usually preferable for small original signals. All Intersil's integrating converters have a digital output line that can be used to extend auto-zero to preconditioning circuits (being careful not to couple the digital signal into the analog system, of course).

Also, DO CHECK THESE AREAS

Tie digital inputs down (or up) if you are not using them. This will avoid stray input spikes from affecting operation. Bypass all supplies with a large and a small capacitor close to the package. Limit input currents into any I.C. pin to values within the maximum rating of the device (or a few mA if not specified) to avoid damaging the device. Ensure that power supplies do not reverse polarity or spike to high values when turned on or off. Remember that many digital gates take higher-than-normal supply currents for inputs between defined logic levels. And remember also that gates can look like amplifiers under these circumstances. An example is shown in Figure 16, where stray and internal input-to-output capacitance is multiplied by the gain of the gate just at the threshold causing a large effective load capacitance on the 8052 comparator (see reference 1 for the effects of this.) A noninverting gate here could lead to oscillations.

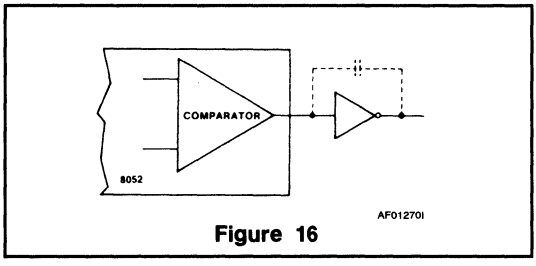


Figure 16

EXTERNAL ADJUSTMENT PROCEDURE

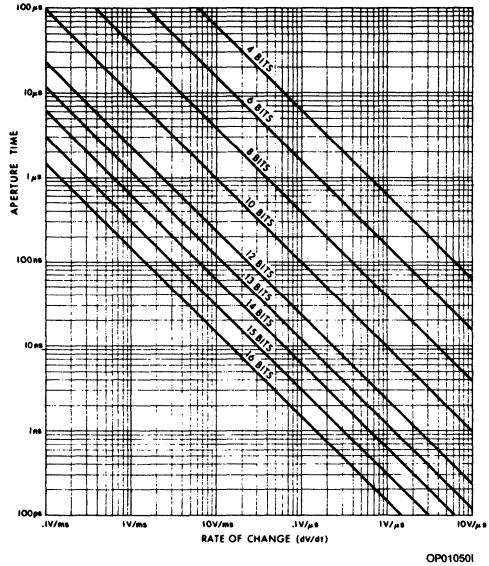
Most of the A/D converters now offered by Intersil do not require an offset adjustment. They have internal autozero circuits which typically give less than 10μV of offset. Therefore, the only optional adjustment required to obtain optimum accuracy in a given application is the full scale or gain reading.

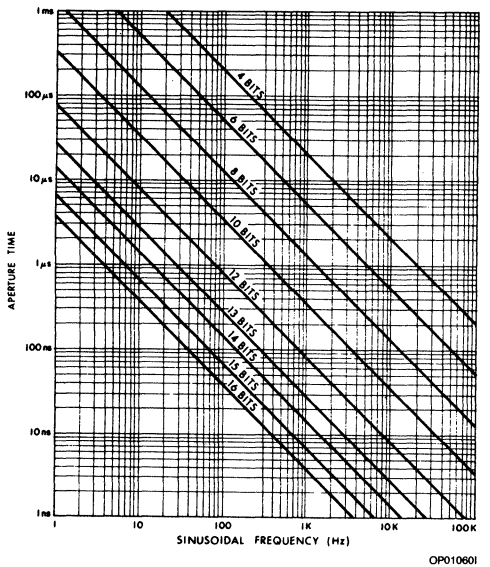
With the A/D converter in a continuous mode of conversion, the following procedure is recommended: The full scale adjustment is made by setting the input voltage to precisely ½ LSB less than full scale or ½ LSB down from nominal full scale. (Note that the nominal full scale is actually never reached but is always one LSB short). Adjust the full scale control until the converter output just barely switches from full output to one count less than full output.

A057
Graphs Give Aperture Time Required for A/D Conversion

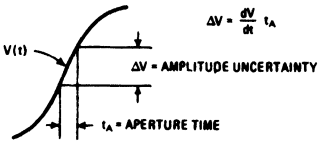
The time required for an analog-to-digital converter to make a conversion is known as "aperture time," and depends on both the resolution and the particular conversion method employed. For commercially available A/D converters that use the successive approximation method, the aperture time may be 40 microseconds for a relatively low-cost 12-bit converter, or as little as 4μs for a more expensive high-speed 12-bit converter. In many cases a sample-hold circuit is used ahead of an A/D converter to effectively reduce the aperture times; the sample-hold can take a very fast sample of the analog signal and then hold the value while the A/D operation is performed. (The time interval during which the signal-hold circuit turns off is then the aperture time, and determines the conversion accuracy. The time for actual A/D conversion can be longer.)

It is important for the designer to know what aperture time is required to keep the system error to a tolerable value in terms of the resolution of his A/D converter. The maximum aperture time that allows 1-bit accuracy in conversion of an analog signal to 4 bits, 6 bits, . . . or 16 bits is given here in two useful graphs. The graph in Fig. 1(a) shows this aperture time as a function of signal rate of change, for signals that are 10 volts full scale or peak to peak. Fig. 1(b) gives the aperture time as a function of the frequency of a sinusoidal signal.





1. Sampling time. Aperture time for 1-bit accuracy at various resolutions in A/D conversion are shown here. Graph (a) gives aperture time as a function of signal rate of change for signals that are 10 volts full scale or 10 volts peak to peak. Graph (b) gives aperture time as a function of frequency for sinusoidal signals. Aperture times for larger allowed error can be found by reading on line for lower resolution, e.g., a 2-bit error and 8-bit resolution requires the same time as a 1-bit error and 7-bit resolution. Equations for these graphs are found in text.



2. Error. Possibility of error in A/D conversion depends upon aperture time. The greater t_A is, the greater the uncertainty in value of an analog voltage that has been converted to digital level.

The two graphs are derived with reference to Fig. 2, which shows a time-varying signal and the amplitude uncertainty ΔV associated with an aperture time t_A

$$t_A = \Delta V/(dV/dt)$$

If the fractional error ϵ is the ratio of ΔV to full-scale voltage V_{FS},

$$t_A = (\epsilon\ V_{FS})/(dV/dt)$$

If ΔV is held to 1 bit, and V_{FS} is resolved into n bits, then $\epsilon = 1/(2^n)$, and

$$t_A = V_{FS}/2^n(dV/dt)$$

This is the equation for the family of lines in Fig. 1(a), with $V_{FS} = 10$ volts and $n = 4, 6, \ldots 16$.

For a sinusoidal signal, which has a maximum rate of change at its zero crossing,

$$\Delta V = t_A[d/dt(1/2)(V \sin \omega t)]_{t\text{-}0} = \omega V t_A/2$$

where V is a peak-to-peak signal value. This gives

$$t_A = (2\Delta V)/(\omega V) = \epsilon/\pi f = 1/(2^n \pi f)$$

for a 1-bit error and n-bit resolution. This is the equation for the family of lines in Fig. 1(b).

If the allowed error is to be 2 bits instead of 1 bit, then $\epsilon = 2/(2^n)$, so aperture times are doubled. An error of 3 bits gives $\epsilon = 4/(2^n)$, and so on; thus a 1-bit increase in error is equivalent to a 1-bit decrease in resolution on the graphs.

As an example of the usefulness of these graphs, assume that a 1-kilohertz sinusoidal signal is to be digitized to a resolution of 10 bits. What aperture time must be used to give less than 1 bit of error? The answer, readily found from Fig. 1(b), is 320 nanoseconds. For 1/2 bit error the aperture time would have to be 160ns. This is surprising, because a 1-kHz signal is really not very fast, and a 10-bit/320-ns converter is not to be found commercially available as a module. Therefore, a sample-hold circuit would be required ahead of a slower A/D converter.

AO17
The Integrating A/D Converter

Integrating A/D converters have two characteristics in common. First, as the name implies, their output represents the integral or average of an input voltage over a fixed period of time. Compared with techniques which require that the input is "frozen" with a sample-and-hold, the integrating converter will give repeatable results in the presence of high frequency* noise. A second and equally important characteristic is that they use time to quantise the answer, resulting in extremely small nonlinearity errors and no possibility of missing output codes. Furthermore, the integrating converter has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise, for example in laboratory instruments. (Figure 1)

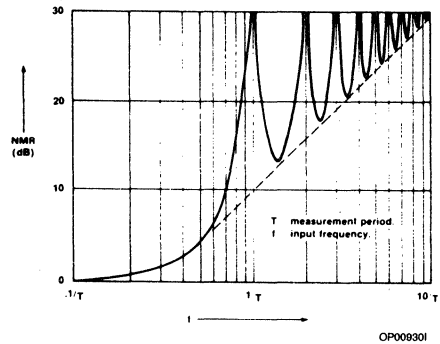


Figure 1: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

In addition, a competitive instrument-quality product should have the following features:

1. Single Reference Voltage. This is strictly a convenience to the user, but since many designs are available with single references that contribute negligible error, products requiring dual references are rapidly becoming obsolete.
2. Auto Zero. This eliminates one trim-pot and a troublesome calibration step. Furthermore, it allows the manufacturer to use op-amps with up to 10mV offset while still achieving system offsets of only a few microvolts.
3. High Input Impedance. Recently developed monolithic FET technology allows input impedances of 1000 Mohm and leakages of a few pico amps to be achieved fairly readily.

The unique characteristics of the integrating converter have made it the natural choice for panel meters and digital voltmeter applications. For this reason, overall useage of integrating converters exceeds the combined total of all other conversion methods. Furthermore, the availability of low cost one chip converters will encourage digitizing at the sensor in applications such as process control. This represents a radical departure from traditional data logging techniques which in the past have relied heavily on the transmission of analog signals. The availability of one chip microprocessor system (with ROM and RAM on chip) will give a further boost to the 'conversion at the sensor' concept by facilitating local data processing. The advantage of local processing is that only essential data, such as significant changes or danger signals, will be transmitted to the central processor.

*relative to the measurement period.

THE DUAL SLOPE TECHNIQUE — THEORY & PRACTICE

The most popular integrating converter is the "dual-slope" type, the basic operating principles of which will be described briefly. However, most of the comments relating to linearity, noise rejection, auto-zero capability, etc., apply to the whole family of integrating designs including charge balancing, triple ramps, and the 101 other techniques that have appeared in the literature. A simplified dual slope converter is shown in Figure 2.

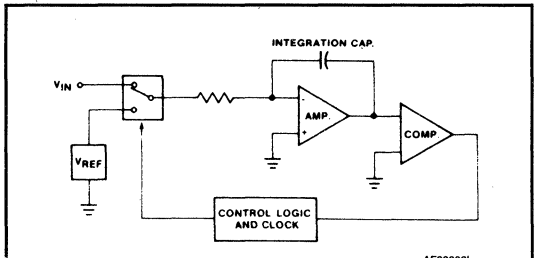


Figure 2: Simplified Dual-Slope Converter

The conversion takes place in three distinct phases (Figure 3).

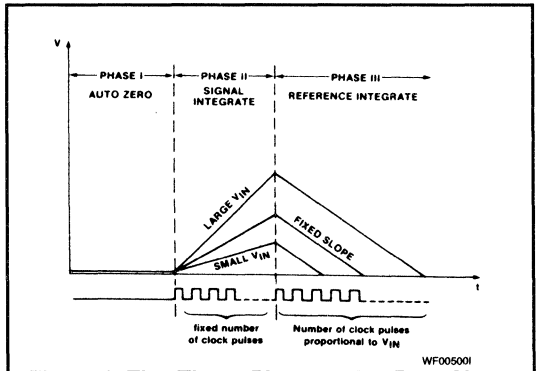


Figure 3: The Three Phases of a Dual-Slope Conversion

Phase 1, Auto Zero: During auto zero, the errors in the analog components (buffer offset voltages, etc.) will be automatically nulled out by grounding the input and

closing a feedback loop such that error information is stored on an "auto-zero" capacitor.

Phase 2, Signal Integrate: The input signal is integrated for a fixed number of clock pulses. For a 3½-digit converter, 1,000 pulses is the usual count; for a 4½-digit converter, 10,000 is typical. On completion of the integration period, the voltage V in Figure 3 is directly proportional to the input signal.

Phase 3, Reference Integrate: At the beginning of this phase, the integrator input is switched from V_{IN} to V_{REF}. The polarity of the reference is determined during Phase 2 such that the integrator discharges back towards zero. The number of clock pulses counted between the beginning of this cycle and the time when the integrator output passes through zero is a digital measure of the magnitude of V_{IN}.

The beauty of the dual slope technique is that the theoretical accuracy depends only on the absolute value of the reference and the equality of the individual clock pulses within a given conversion cycle. The latter can easily be held to 1 part in 10^6, so in practical terms the only critical component is the reference. Changes in the value of other components such as the integration capacitor or the comparator input offset voltage have no effect, provided they don't change during an individual conversion cycle. This is in contrast to Successive Approximation converters which rely on matching a whole string of resistor values for quantisation.

In a very real sense the designer is presented with a near perfect system; his job is to avoid introducing additional error sources in turning this text-book circuit into a real piece of hardware.

From the foregoing discussion, it might be assumed that designing a high performance dual-slope converter is as easy as falling off the proverbial log. This is not true, however, because in a practical circuit a host of pitfalls must be avoided. These include the non-ideal characteristics of FET switches and capacitors, and the switching delay in the zero crossing detector.

ANALYZING THE ERRORS

At this point it is instructive to perform a detailed error analysis of a representative dual slope circuit, Intersil's, ICL7135. This is a 4½-digit design, as shown in Figure 4. The error analysis which follows relates to this chip — however, the principles behind the analysis apply to most integrating converters.

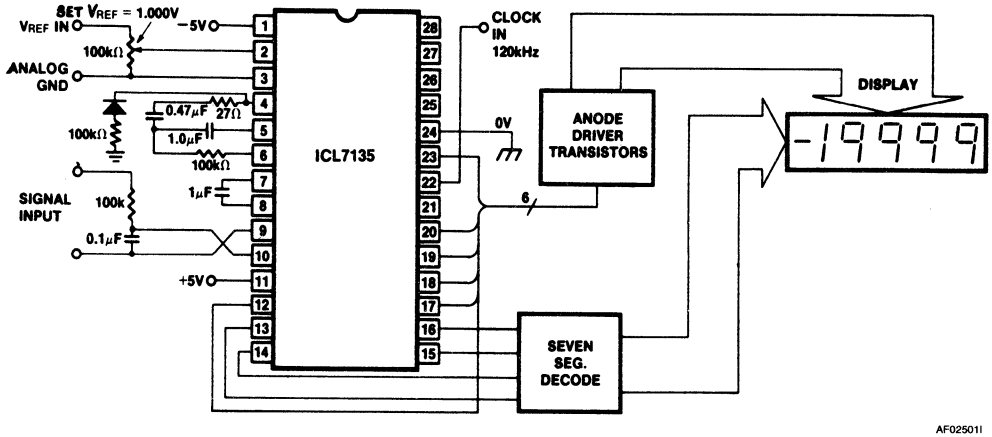


Figure 4: The ICL7135 Functional Diagram

The analog section of the converter is shown in Figure 5. Typical values are shown for 120kHz clock and 3 measurements/second. Each measurement is divided into three parts. In part 1, the auto-zero FET switches 1, 2 and 3 are closed for 10,000 clock pulses. The reference capacitor is charged to V_{REF} and the auto-zero capacitor is charged to the voltage that makes dV/dt of the integrator equal to zero. In each instance the capacitors are charged for 20 or more time-constants such that the voltage across them is only limited by noise.

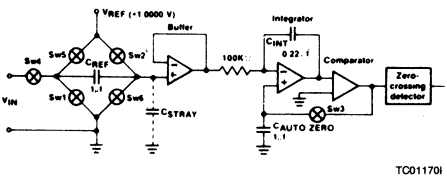


Figure 5: Analog Section of a Dual Slope Converter

In the second phase, signal integrate, switches 1, 2 and 3 are opened and switch 4 is closed for 10,000 clock pulses. The integrator capacitor will ramp up at a rate that is proportional to V_{IN}. In the final phase, de-integrate, switch 4 is opened and, depending on the polarity of the input signal, switch 5 or 6 is closed. In either case the integrator will ramp down at a rate that is proportional to V_{REF}. The amount of time, or number of clock pulses, required to bring the integrator back to its auto-zero value is 10,000 $(\frac{V_{IN}}{V_{REF}})$. Of course, this is a description of the "ideal" cycle. Errors from this ideal cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption).
6. Charge lost by C_{REF} in charging C_{stray}.

Each of these errors will be analyzed for its error contribution to the converter.

Capacitor Droop Due to Leakage

Typical leakage (I_{Doff}) of the switches at normal operating voltage is 1 pA each and 2pA at each input of the buffer and integrator op amps. In terms of offset voltage caused by capacitor droop, the effect of the auto-zero and reference capacitors is differential, i.e., there is no offset if they droop an equal amount. A conservative typical effect of droop on offset would be 2pA discharging 1μF for 83 milliseconds (10,000 clock periods), which amounts to an averaged equivalent of .083μV referred to the input. The effect of the droop on roll-over error (difference between equal positive and negative voltages near full scale) is slightly different. For a negative input voltage, switch 5 is closed for the de-integrate cycle. Thus the reference capacitor and auto-zero capacitor operate differentially for the entire measurement cycle. For a positive voltage, switch 6 is closed and the differential compensation of the reference capacitor is lost during de-integrate. A typical contribution to roll-over error is 3 pA discharging 1μF capacitor for 166 milliseconds, equivalent to .249μV when averaged. These numbers are certainly insignificant for room temperature leakages but even at 100°C the contributions should be only 15 μV and 45 μV respectively. A roll-over error of 45 μV is less than 0.5 counts on this 20,000 count instrument.

Charge "Suck-Out" When the Switches Turn-Off

There is no problem in charging the capacitors to the correct value when the switches are on. The problem is getting the switches off without changing this value. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its value. The net charge injection of switch 3 turning-off can be measured indirectly by noting the offset resulting by using a .01μF auto-zero capacitor instead of 1.0μF. For this condition the offset is typically 250μV, and since the signal ramp is a straight line instead of a parabola the main error is due to charge injection rather than leakage. This given a net injected charge of 2.5 picocouloumbs or an equivalent C_{gd} of 0.16pF. The effect of switches 1, 2, 4, 5 and 6 are more complicated since they depend on timing and some switches are going on while others are going off. A substitution of an .01μF capacitor for reference capacitor gives less than 100 μV offset error. Thus, a conservative typical offset error for a 1.0μF capacitor is 2.5μV. There is no contribution to roll-over error (independent of offset). Also this value does not change significantly with temperature.

Non-Linearity of Buffer and Integrator

In this converter, since the signal and reference are injected at the same point, the gain of the buffer and integrator are not of first-order importance in determining accuracy. This means that the buffer can have a very poor CMRR over the input range and still contribute zero error as long as it is constant, i.e., offset changes linearly with common mode voltage. The first error term is the non-linear component of CMRR. Careful measurement of CMRR on 30 buffers indicated roll-over errors from 5 to 30μV. The contribution of integrator non-linearity is less than 1μV in each case.

High Frequency Limitations of Amplifiers

For a zero input signal, the buffer output will switch from zero to V_{REF} (1.0 volt) in 0.5μseconds with an approximately linear response. The net result is to lose 0.25μseconds of de-integrate period. For a 120kHz clock, this is 3% of a clock pulse or 3μV. This is not an offset error since the delay is equal for both positive and negative references. The net result is the converter would switch from 0 to 1 at 97μV instead of 100μV in the ideal case.

A much larger source of delay is the comparator which contributes 3μseconds. At first glance, this sounds absolutely ridiculous compared to the few tens of nano-seconds delay of modern IC comparators. However, they are specified with 2 to 10mV of overdrive. By the time the ICL7135 comparator gets 10mV of overdrive, the integrator will have

been through zero-crossing for 20 clock pulses! Actually, the comparator has a 300MHz gain-bandwidth product which is comparable to the best IC's. The problem is that it must operate on 30μV of overdrive instead of 10mV. Again, this delay causes no offset error but means the converter switches from 0 to 1 at 60μV, from 1 to 2 at 160μV, etc. Most users consider this switching at approximately $\frac{1}{2}$ LSB more desirable than the "so-called ideal" case of switching at 100μV. If it is important that switching occur at 100μV, the comparator delay may be compensated by including a small value resistor ($\simeq$20Ω) in series with the integration capacitor. (Further details of this technique are given on page 4 under the heading "Maximum Clock Frequency".) The integrator time delay is less than 200 nsecond and contributes no measurable error.

Integrating Capacitor Dielectric Absorption

Any integrating A/D assumes that the voltage change across the capacitor is exactly proportional to the integral of the current into it. Actually, a very small percentage of this charge is "used up" in rearranging charges within the capacitor and does not appear as a voltage across the capacitor. This is dielectric absorption. Probably the most accurate means of measuring dielectric absorption is to use it in a dual-slope A/D converter with $V_{IN} \equiv V_{REF}$. In this mode, the instrument should read 1.0000 independent of other component values. In very careful measurements where zero-crossings were observed in order to extrapolate a fifth digit and all delay errors were calculated out, polypropylene capacitors gave the best results. Their equivalent readings were 0.99998. In the same test polycarbonate capacitors typically read 0.9992, polystrene 0.9997. Thus, polypropylene is an excellent choice since they are not expensive and their increased temperature coefficient is of no consequence in this circuit. The dielectric absorption of the reference and auto-zero capacitors are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used if very accurate readings are not required for the first few seconds of recovery.

Charge Lost by C_{REF} in Charging C_{stray}.

In addition to leakage and switching charge injection, the reference capacitor has a third method of losing charge and, therefore, voltage. It must charge C_{stray} as it swings from 0 to V_{IN} to V_{REF}. (Figure 5). However, C_{stray} only causes an error for positive inputs. To see why, let's look firstly at the sequence of events which occurs for negative inputs. During auto-zero C_{REF} and C_{stray} are both charged through the switches. When the negative signal is applied,. C_{REF} and C_{stray} are in series and act as a capacitance divider. For C_{stray} = 15pF, the divider ratio is 0.999985. When the positive reference is applied through switch #5, the same divider operates. As mentioned previously, a constant gain network contributes no error and, thus, negative inputs are measured exactly.

For positive inputs, the divider operates as before when switching from auto-zero to V_{IN}, but the negative reference is applied by closing switch #6. The reference capacitor is not used, and therefore the equivalent divider network is 1.0000 instead of .999985. At full scale, this 15μV/V error gives a 30μV rollover error with the negative reading being 30μV too low. Of course for smaller C_{stray}, the error is proportionally less.

Summary

Error analysis of the circuit using typical values shows four types of errors. They are (1) an offset error of 2.5μV due to charge injection, (2) a full scale rollover error of 30μV due to C_{stray}, (3) a full scale rollover error of 5 to 30μV due to buffer non-linearity and (4) a delay error of 40μV for the first count. These numbers are in good agreement with actual results observed for the ICL7135. Due to peak-to-peak noise of 20μV around zero, it is possible only to say that any offsets are less than 10μV. Also, the observed rollover error is typically $\frac{1}{2}$ count (50μV) with the negative reading larger than the positive. Finally, the transition from a reading of 0000 to 0001 occurs at 50μV.

These figures illustrate the very high performance which can be expected from a well designed dual-slope circuit-performance figures which can be achieved with no tricky 'tweaking' of component values. Furthermore, the circuit includes desirable convenience features such as auto-zero, auto-polarity and a single reference.

MAXIMUM CLOCK FREQUENCY

Because of the 3μs delay in the comparator, the maximum recommended clock frequency is 160kHz. In the error analysis it was shown that under these conditions half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 at 50μV, from 1 to 2 at 150μV, etc. As was noted earlier, most users consider this transition at midpoint to be desirable. However, if the clock frequency is increased appreciably above 160kHz, the instrument will flash 1 on noise peaks even when the input is shorted.

The clock frequency may be extended above 160kHz, however, by using a low value resistor in series with the integration capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase (Figure 6). By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument.

NOISE

The peak-to-peak noise around zero is approximately 20μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 40μV.

Since much of the noise originates in the auto-zero loop, some improvement in noise can be achieved by putting gain in the buffer. A gain of about 5X is optimum. Too much gain will cause the auto-zero switch to misbehave, because the amplified Vos of the buffer will exceed the switch operating range.

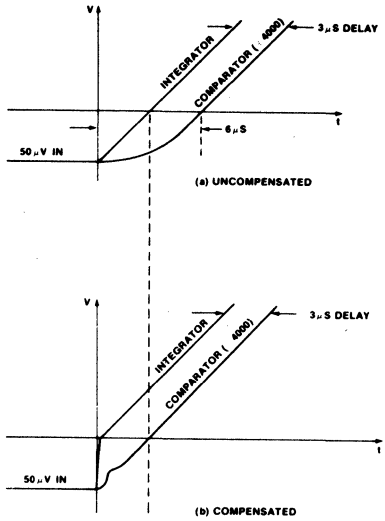


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Figure 6: Integrator and Comparator Outputs for Uncompensated (a) and Compensated (b) System

AO47
Games People Play with Intersil's A/D Converters

INTRODUCTION

This application note is a collection of application circuits, mostly small or special purpose circuits that could not justify publication in this form alone, but together constitute a useful compendium. The circuits have been loosely categorized into three groups for convenience in reference, as follows:

Input Games: Circuits which alter the input signal(s) in some (preferably) unusual or non-obvious way, to achieve an unexpected or non-standard function.

Converter Games: Circuits involving some alteration to the operation of the converter, to achieve some result other than the normal direct linear voltage conversion.

Output Games: Games played with the output of the converter, to alter or add to the display, or add a computer interface or alarm, for example.

Mixed Games: Games that cannot easily be categorized into one of the other types, or that involve more than one of the above activities.

Since many of the circuits are based on only a few of the wide range of available Intersil converters, a Schedule (Table) is provided to show to which converter circuits the applications relate, either directly or with modifications. It is assumed throughout that the "normal" operation of the devices is known to and understood by the reader. If this is not the case, the perusal of the relevant data sheet(s) and of the other application notes listed at the end of this one is recommended.

Evaluation Kits are available for the ICL7106, 7107, 7126, 7135, and 7136, containing the IC, a PC board, the required basic passive components, and in some cases a display, in others various ancillary ICs, together with the required instructions, etc. Most of the simpler circuits shown here can be easily built on the appropriate EV/Kit with a little component juggling and occasional trace cutting. Several of the kits have "breadboarding" areas to facilitate the addition of extra components.

The circuits shown here come from various and sundry sources. Many came directly from users of the devices, and many others from questions or suggestions from them, still others came from our engineering and applications people around the world.

Enough of this! Without more ado, LET THE GAMES BEGIN!

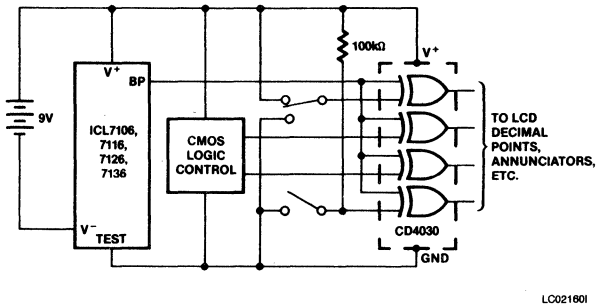
2

Table 1:— SCHEDULE OF GAMES (a.k.a. Table of Contents)

		APPLICABLE DEVICES (ICL)										
NO.	TITLE	7104	7106	7107	7109	7116	7117	7126	7135	7136	7137	CATEGORY OF GAME
1	LCD Annunciators		Y			Y		Y		Y		Output
2	Decimal Point Drive		Y			Y		Y		Y		Output
3	Low Battery Detector		Y	Y		Y	Y	Y		Y	Y	Output
4	Blank Display on Low Battery		Y	Y		Y	Y	Y		Y	Y	Output
5	LED Brightness Control			Y			Y				Y	Output
6	Leading Zero Blanking		Y	Y		Y	Y	Y	m	Y	Y	Output
7	Instant Continuity on Ohms		Y	m	m	m	m	Y	m	Y	m	Output
8	High Voltage Display Driving		Y	Y		Y	Y	Y		Y	Y	Output
9	DVM Circuits		Y	Y		Y	Y	Y	Y	Y	Y	Input
10	Battery Operated Tachometer	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Input
11	Examining your Navel	m	Y	Y	Y	m	m	Y	m	Y	Y	Input
12	Measuring h_{fe}		Y	Y	Y			Y	m	Y	Y	Input
13	Running off 1.5V Battery		Y	m	m	Y	m	Y	m	Y	m	Mixed
14	Conversion Status Signal		Y	Y				Y		Y	Y	Output
15	Switching Preamp		Y			Y		Y		Y		Input
16	Capacitance Meter		Y	m	m	Y	m	Y	m	Y	m	Input
17	Eliminating Overrange Hangover	Y										Converter
18	Auto-Tare Circuit	m			Y							Converter
19	3¾-Digit Meter (LCD/LED/VF)	m			Y							Converter
20	¼ Count Resolution Meter	m			m				Y			Converter
21	A Logarithmic A/D Converter		Y	Y	Y	Y	Y	Y	Y	Y	Y	Converter
22	No-Ref-Cap Circuits	m	Y	Y	Y	Y	Y	Y	Y	Y	Y	Converter
23	Low Noise Preamp Circuit		Y	Y	Y	m	m	Y				Converter
24	Current I/P Converter Circuit		Y	Y	Y	m	m	Y				Converter
25	BCD Output from 7-Segment O/P		Y	Y		Y	Y	Y		Y	Y	Output

Note: "Y" means that the circuit is shown for the device listed (although frequently some component values may need alteration), whereas "m" signifies that some modification is required to use that device. The "ICL7104" is to be considered a chip pair, with the required ICL8052 or ICL8068 not listed, but assumed.

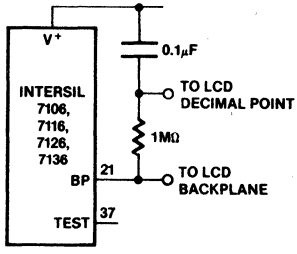
LCD Annunciators



LC02160I

Figure 1: Logic-Controlled LCD Annunciators. These circuits can be used to show any desired messages on the same display as the digital output

Decimal Point Drive



LC02170I

Figure 2: DC-less Decimal Point Drive. Although the circuit of Figure 1 can provide fixed annunciator drive, it is relatively expensive. A crude drive method (shown in A023) is to tie the LCD segment to COMMON, but this applies a significant DC voltage to the display which can lead to problems. In any case it cannot be used if COMMON is grounded externally, etc. This circuit, suggested by a French correspondent, avoids those problems, and acts as a rough "low-battery" detector also. Note that by the time the segment disappears, the reference voltage on COMMON has altered significantly, and that the detection point is a function of the individual display

Low Battery Detector

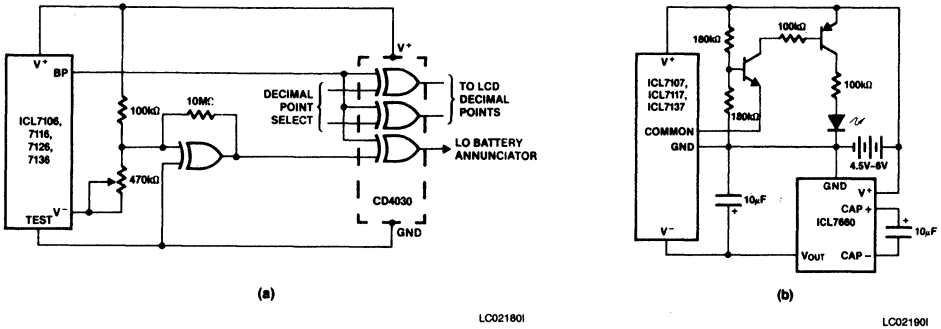


Figure 3: Low Battery Detector. The threshold is set by the resistor ratio against the internal logic regulator in each case. The remaining gates can be used for annunciator drivers, etc. as shown

Blank Display on Low Battery

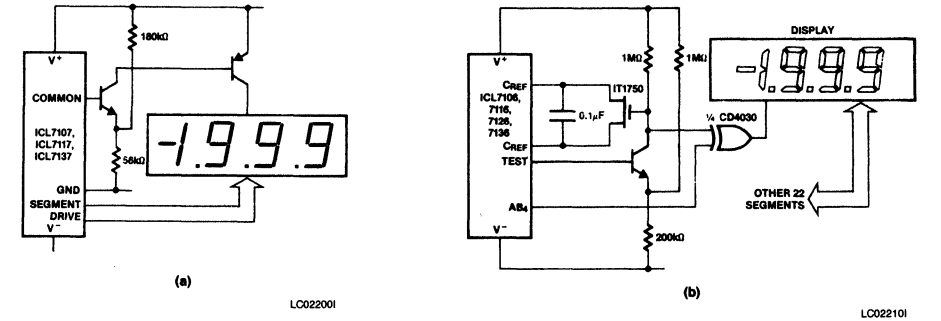


Figure 4: Blank Display on Low Battery. Sometimes no reading is better than a (possibly) bad one. The same type of circuit can be used to cover other conditions also. The LCD circuit forces an "overrrange" reading by shorting the reference input, and inverts the "1", leaving only a possible polarity indication

LED Brightness Control

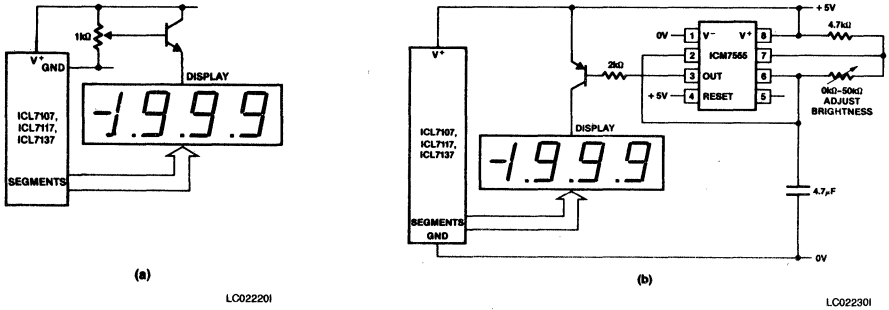
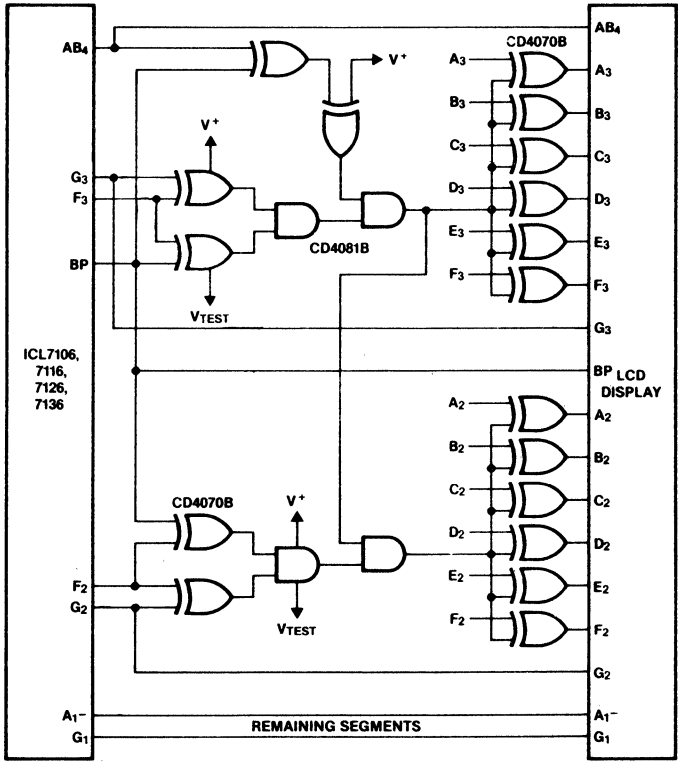


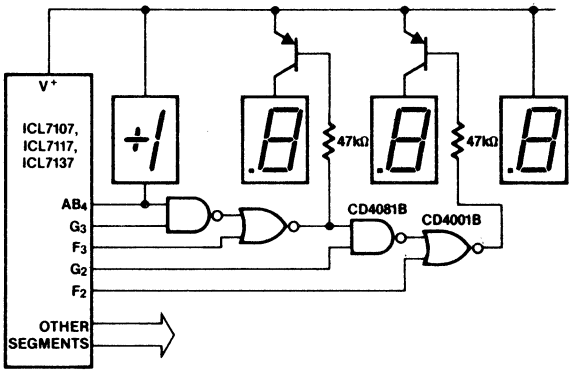
Figure 5: Controlling LED Brightness. The circuit in (a) applies a variable voltage to the anodes of the LEDs, and can lead to mismatch problems, while that of (b) uses a timer circuit to control the duty cycle, needing good supply bypassing. A counter driven by the oscillator could be used instead of a timer

Leading Zero Blanking



(a)

LC022401

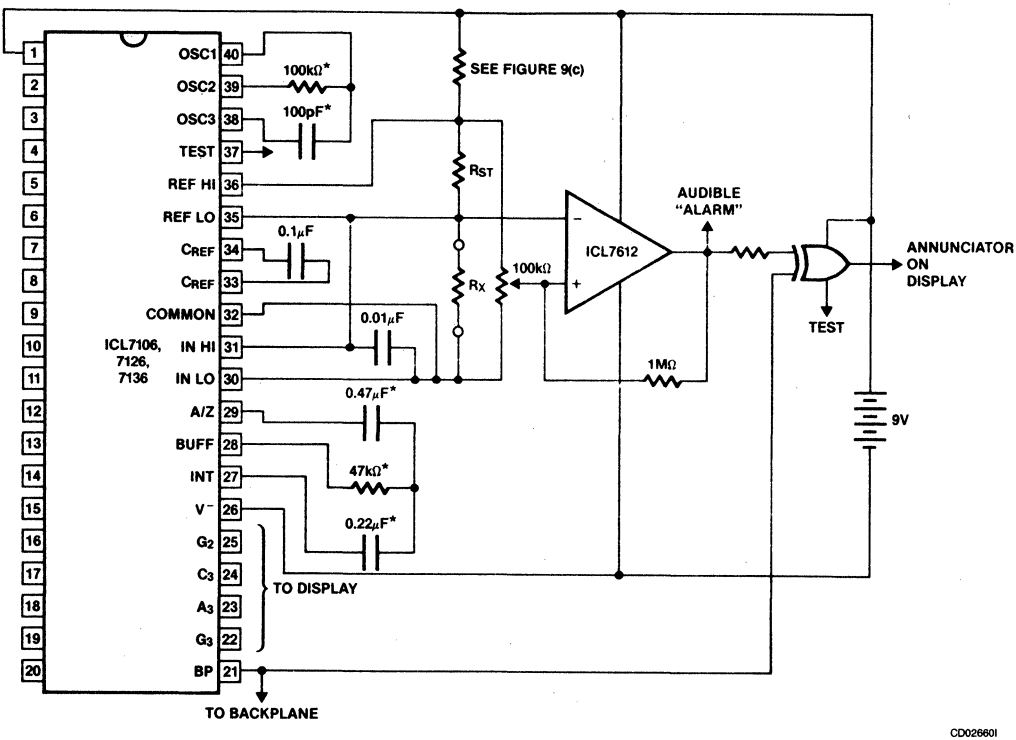


(b)

LC022501

Figure 6: Leading Zero Blanking for the ICL71X6 and 71X7. The circuits detect the "segment f and not-segment g" condition, and blank the display accordingly

Instant Continuity on Ohms



*ICL7106 only. See data sheets or A052 for correct values of these components.

Figure 7: Instant Continuity when Measuring Resistance. The output can be used to drive an audible alarm, etc. if desired. The continuity annuciator or audible signal will indicate regardless of normal measurement cycle if input is less than set proportion of full-scale input. For use with ICL7107 or ICL7109, different annunciator connection will be needed, of course. To use with ICL7116, 7117, or 7135 reverse positions of known R_{ST} and unknown R_X, swap IN HI and REF HI, IN LO and REFLO, and invert sense of output. The ICL7135 will also need a supply to drive the resistors

High Voltage Display Driving

A vacuum-fluorescent display panel can be activated by three DI805A high voltage drivers which are directly driven by an ICL71X7 3½-digit A/D converter. The ICL71X7 normally drives a common-anode LED display and its outputs pull-down to turn on a segment. The DI805A acts as an inverter in this application to illuminate display segments when its inputs are pulled down. Note the grid and filament connections to the display panel in Figure 8(a).

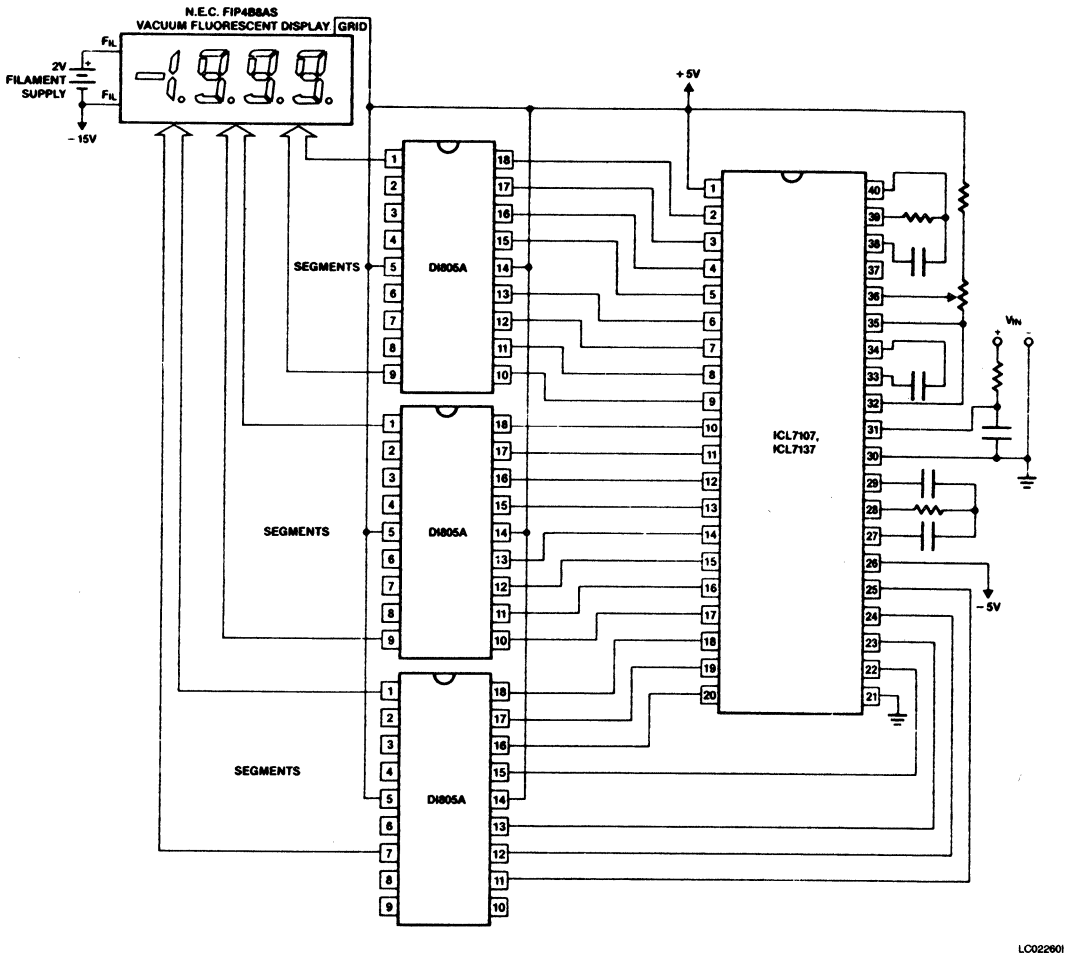


Figure 8(a): Vacuum Fluorescent Display Interface

A gas-discharge type display is shown in Figure 8(b) being activated by three DI220 display driver circuits which are driven by an ICL71X6 A/D converter. The ICL71X6 is designed to drive an LCD display. In this application, the BackPlane signal is buffered by a PNP emitter-follower and, when low, enables the high voltage drivers by providing a ground return for them. A high level on the input to the DI220 when BackPlane is low will turn on a display segment. Thus, only when a segment line is out of phase with BackPlane will the segment be on. In this mode, the display will be operating at 50% duty cycle.

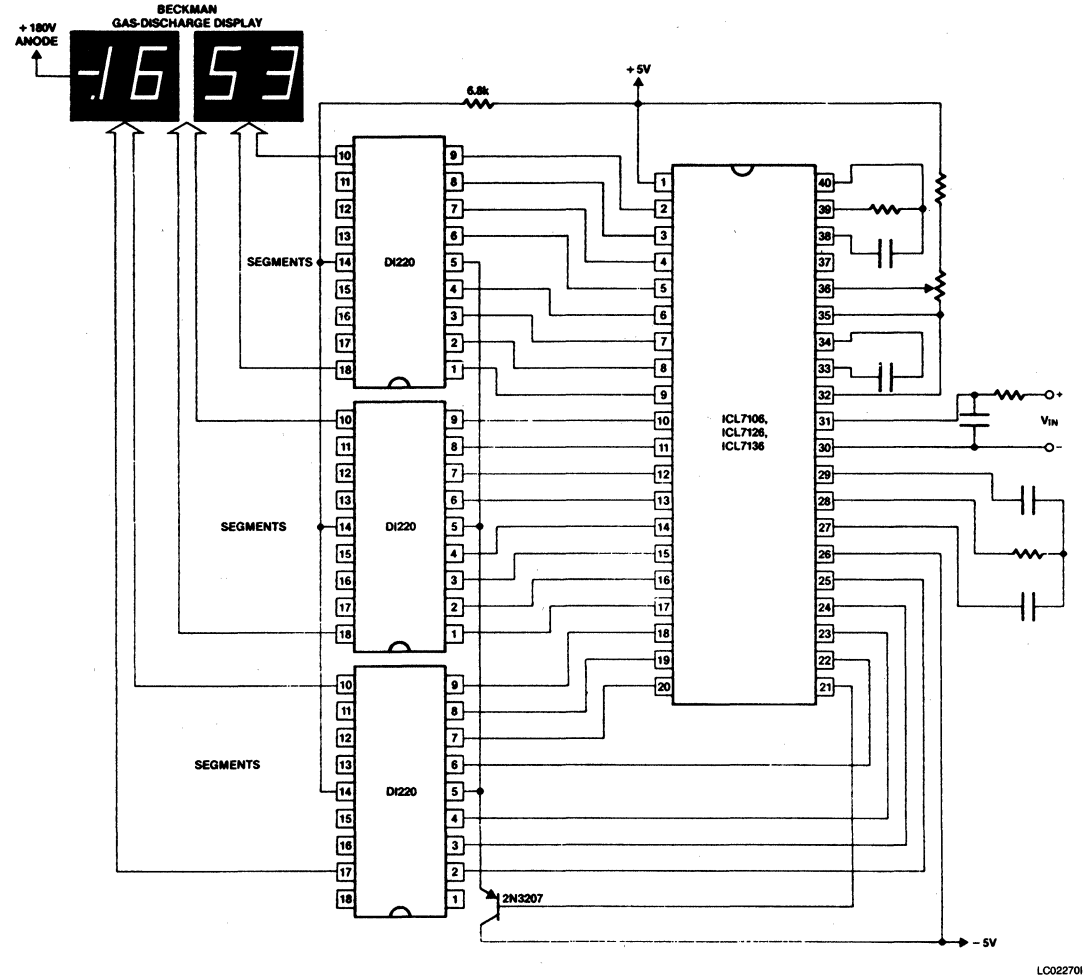
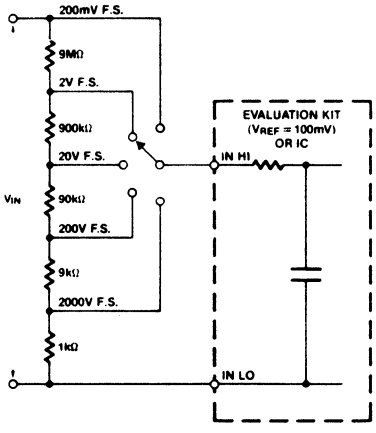


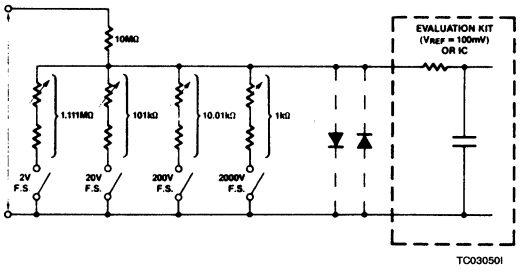
Figure 8(b): A Gas-Discharge Plasma Type Display

DVM Circuits



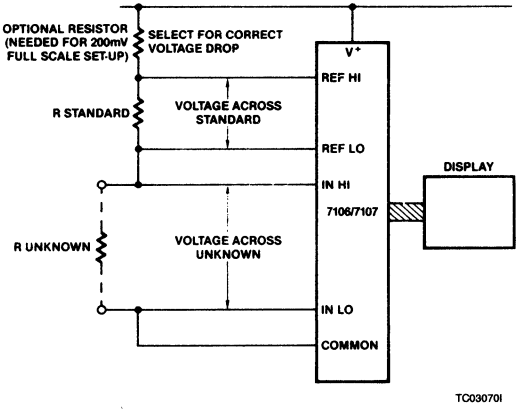
*CAUTION: High voltages can be lethal. Proper operating precautions must be observed by the user. Intersil assumes no liability for unsafe operation.

(a) Multirange Voltmeter

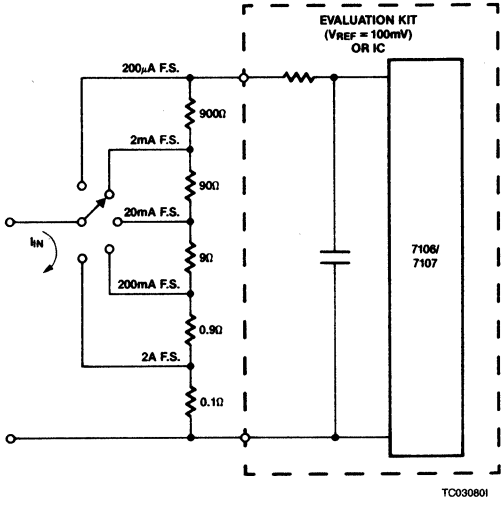


*200mV F.S. for all switches open

(b) Multirange Voltmeter, Alternative Arrangement



(c) Resistance Measurement. The optional resistor can be replaced by a diode string



(d) Multirange Current Meter

Figure 9: DVM Circuits. Voltage and current measurements for metering. For auto-ranging circuits see A046 for the 3½-digit devices, and A028 for the 4½-digit parts

Battery Operated Tachometer

The problem of getting a reading in RPM from an input frequency is solved by the use of a frequency-to-voltage converter at the front end of an A/D converter.

The frequency-to-voltage conversion is accomplished by a CMOS timer which generates a constant pulse width waveform at its output and a micropower CMOS op amp which integrates the timer pulses. Operating the timer from the internal reference voltage of the A/D converter eliminates the need for a second reference because of the rail-to-rail output swing of the timer.

The input to the A/D converter is given by:

$$V_{IN} = \left(\frac{RPM}{60}\right)(t_{pw})\ (V_R)\ (E)\ \left(\frac{R_4}{R_3}\right)$$

Where t_{pw} = timer pulse width = 1.1 R_2C_2

V_R = ICL7106 Reference Voltage = 2.8V

E = Number of events per revolution = 2 for this example

The reading of the A/D converter is given by:

$$n = \left(\frac{V_{IN}}{V_R}\right)\left(\frac{R_8 + R_7}{R_{8A}}\right)$$

$$n = \left(\frac{RPM}{60}\right)(1.1\ R_2C_2)\ (E)\ \left(\frac{R_4}{R_3}\right)\left(\frac{R_8 + R_7}{R_{8A}}\right)$$

The factor E relates to the number of pulses per revolution from a magnetic or optical sensor, the number of blades on a propeller, or the number of point closures per revolution in an automotive application. R_6 is needed only if the A/D converter is adjusted for 200mV full-scale.

Examining your Navel (alias Looking at the Beam in your Own Eye . . .)

One common application question concerns using an ICL7106/7 family device to monitor its own supplies. Obviously this won't work at all if the supply gets too low, but above this level the circuits of Figure 11 will do just that. The ICL7107 circuits can also be used for the ICL7109 and ICL7135.

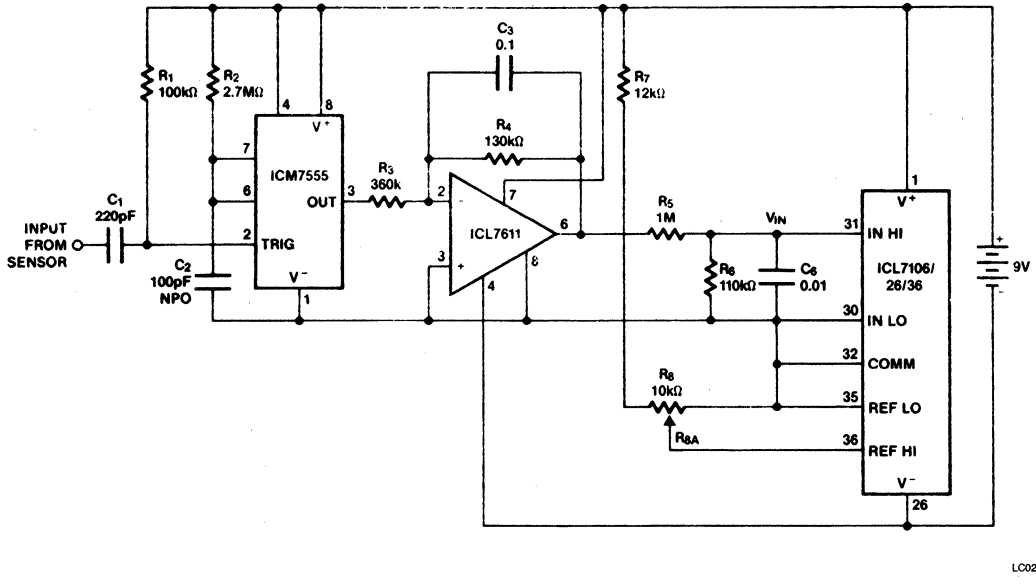
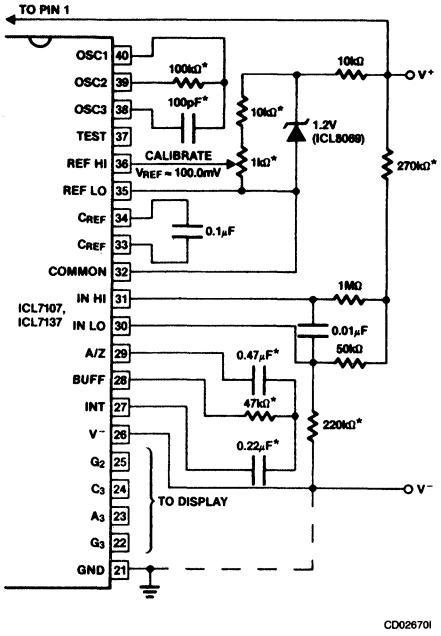
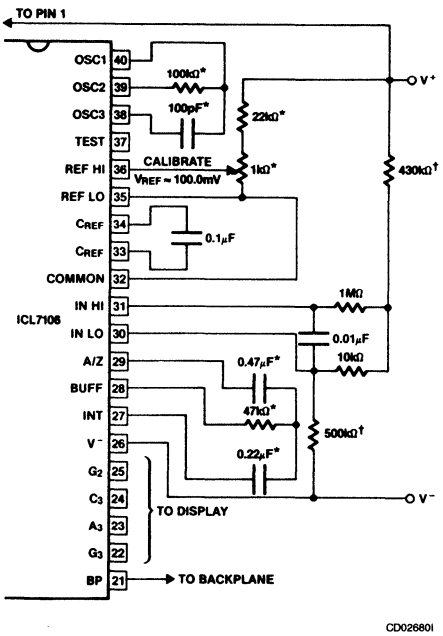


Figure 10: Tachometer using ICL7106 Family A/D





†These resistor dividers should be set up so that at "end-of-life" for the supply, IN LO is about 2.8V below V^+, and correct division occurs to IN HI-IN LO.

*ICL7106/7 only. See data sheet for values for other parts.

Figure 11(a): Voltage Monitor, LED Version using 7107. Dotted connection should be used for supplies of 4V-6V. For higher supplies, provide regulated 5V between V^+ and GND.

Figure 11(b): Voltage Monitor, LCD Version, for Voltages over 6.5V (to 15V max). Circuit uses internal reference. For < 6V, use ICL8069 reference.

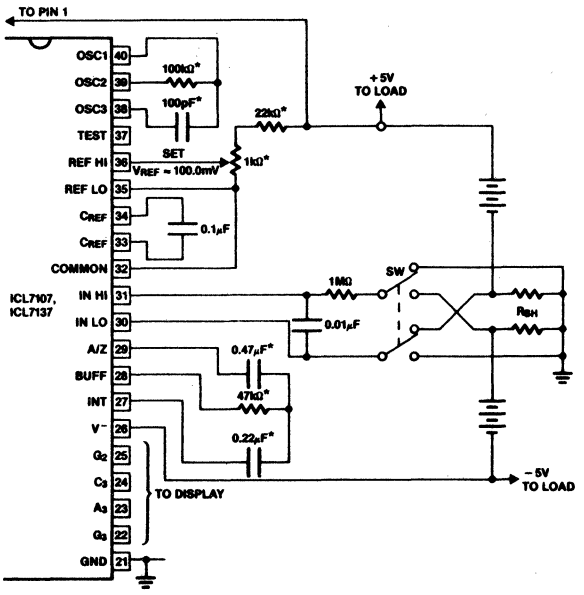
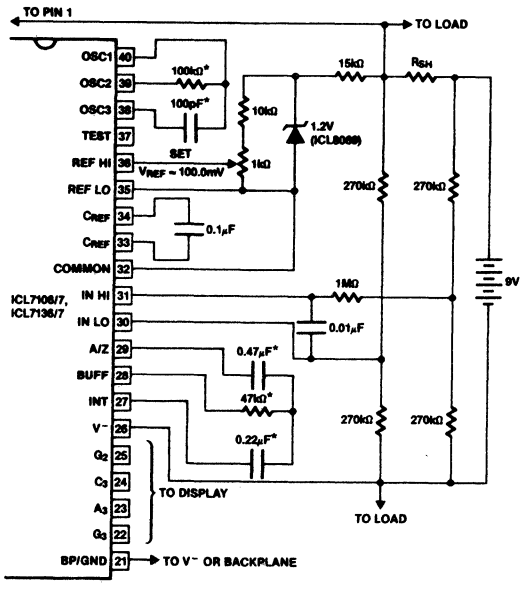


Figure 11(c): Split Supply Current Monitor with 7107, using the Internal Reference. Values for R_{SH} depend on current to be measured, should drop 100mV at half full-scale



*ICL7106/7 only. See data sheet for values for other parts.

Figure 11(d): Single Supply Current Monitor using External Reference. Circuit can use ICL7106 or 7107. Resistor dividers must match very accurately to ensure accuracy. R_{SH} depends on current to be monitored, division ratio of dividers

Measuring h_{fe}

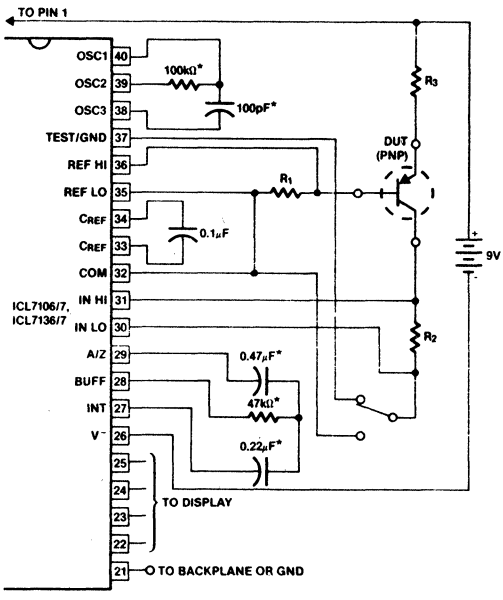
The circuit of Figure 12 sets the emitter current of the DUT via R_3, and measures the ratio of the resultant base and collector currents, monitored in R_1 and R_2 at the REFerence and INput terminals respectively. A fixed voltage and R_3 set the emitter current, hence the slightly smaller collector current and the input voltage, while the reference voltage varies as $\sim \frac{1}{h_{fe}}$.

Although high betas cause overrange readings, the circuit is not actually overloaded, while with low betas the high reference gives a short de-integrate cycle, but still accurate readings.

For the resistor values shown, full-scale is 199.9: increasing R_1 by a factor of 10 will give 1999 full-scale. R_1 and R_2 should be 0.1% or better, but R_3 is not critical. Although Figure 12 shows separate NPN and PNP circuits, they could be combined with a range-switching arrangement. Minor component value changes will accommodate the ICL7126/7136.

Running off 1.5V Battery (with aid of Voltage Converters)

Two ICL7660 voltage converters quadruple the 1.5V single cell battery voltage into 6V, sufficient to power the ICL7126/7136 A/D converter and an ICL8069 voltage reference. The latter is needed because the internal reference needs over 6.5V to operate correctly. The battery current is typically less than 3mA, and batteries up to 3.5V may be used. CR_1 may be required for batteries over 3.0V. The ICL7106 and ICL7116 can use the same circuit, but with higher battery drain. A similar arrangement can also be used with the ICL7109 and ICL7135, and also the ICL7107/7117 although LED display currents are usually too high.



(a)

CD02710I

$I_E(I_C)$	1μA	10μA	100μA	1mA
R_1	20M	2M	200k	20k
R_2	200k	20k	2k	200Ω
R_3	2M	200k	20k	2k

*ICL7106/7 only. See data sheet for values for other parts.

Figure 12: Digital h_{fe} Tester. The switch shown in the PNP version (a) permits testing at V_{CD}~0.5V or ~3.5V. This cannot be done on the NPN tester (b), however, without exceeding the common-mode range of the input

Conversion Status Signal

Many applications of the ICL7106/7 family would be facilitated by a signal similar to the BUSY or STATUS signal on such converters as the ICL7109 and 7135. The simple circuit shown here will accurately signal the end of conversion, for use in multiplexing, auto-ranging, etc. Note that it will only work with the reference input near V^+ and with reference voltages of less than a few hundred mV. Also the reference is disturbed by the current drawn, so ratiometric use is not recommended, and the beginning of conversion signal will be appreciably delayed. The good news is that the roll-over error discussed in A032 for reference not at COMMON does not apply to this circuit. See A046 for a variant of this.

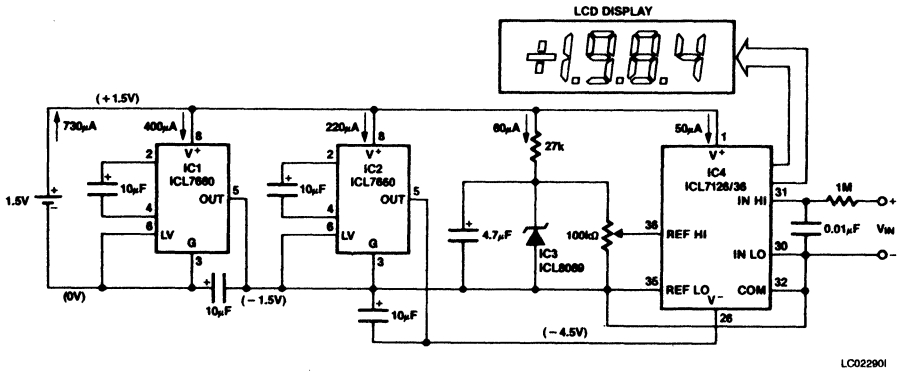
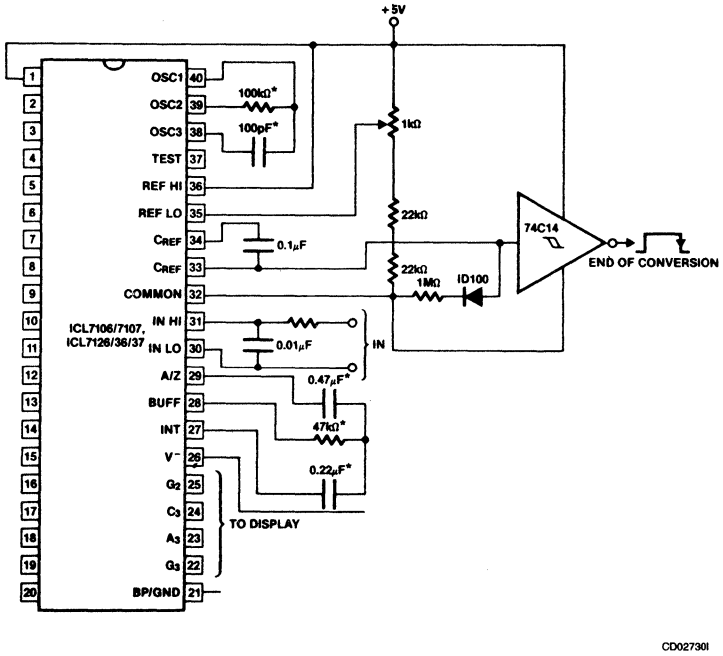


Figure 13: Using ICL7660 to Run ICL7126/36 from 1.5V Battery

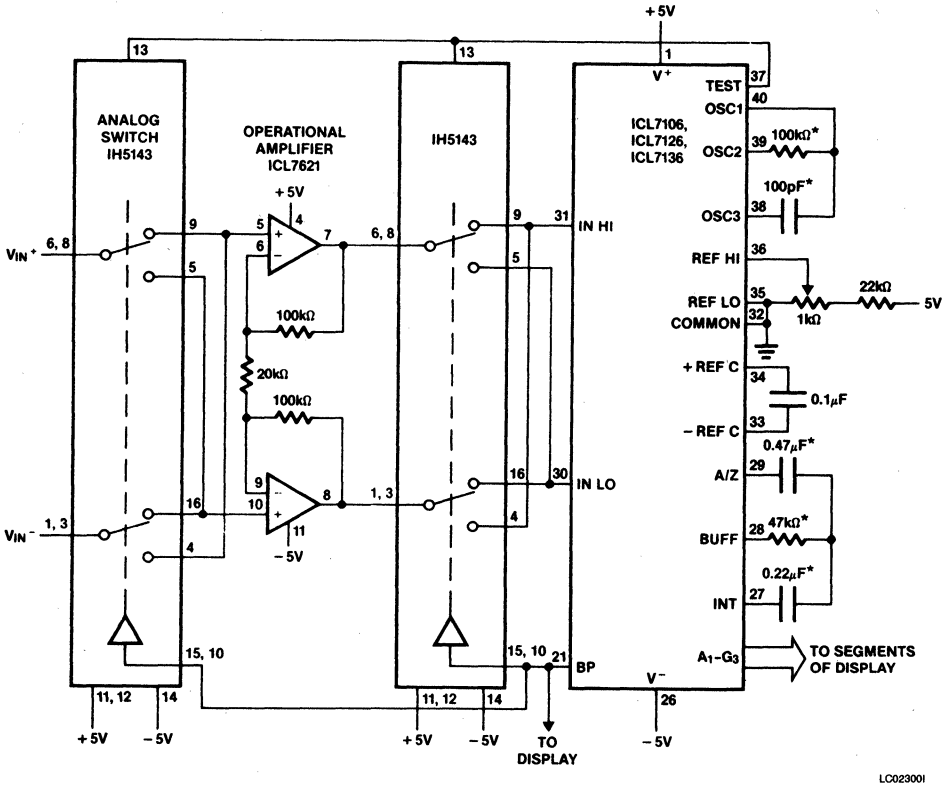


*ICL7106/7 only. See data sheet for values for other parts.

Figure 14: Simple End-of-Conversion Detector

Switching Preamp

The low-signal resolution of even the best A/D converters is limited by the effective noise voltage at the inputs, generally dominated for the ICL7106/7 family by the noise voltage trapped on the auto-zero capacitor. Low cost preamplifiers usually contribute wildly excessive offset errors, but the circuit here uses the backplane drive output of an ICL7106 (or 7116, 7126, or 7136) to synchronously switch a differential amplifier through a pair of polarity reversing analog switches. The input always sees the signal in the same polarity and magnitude, but the preamp offset is inverted with a 50% duty cycle at the A/D input so that it averages zero over the integrate cycle. The switching is performed at a 60Hz rate, and performs excellently down to 20mV full-scale (10µV/count).



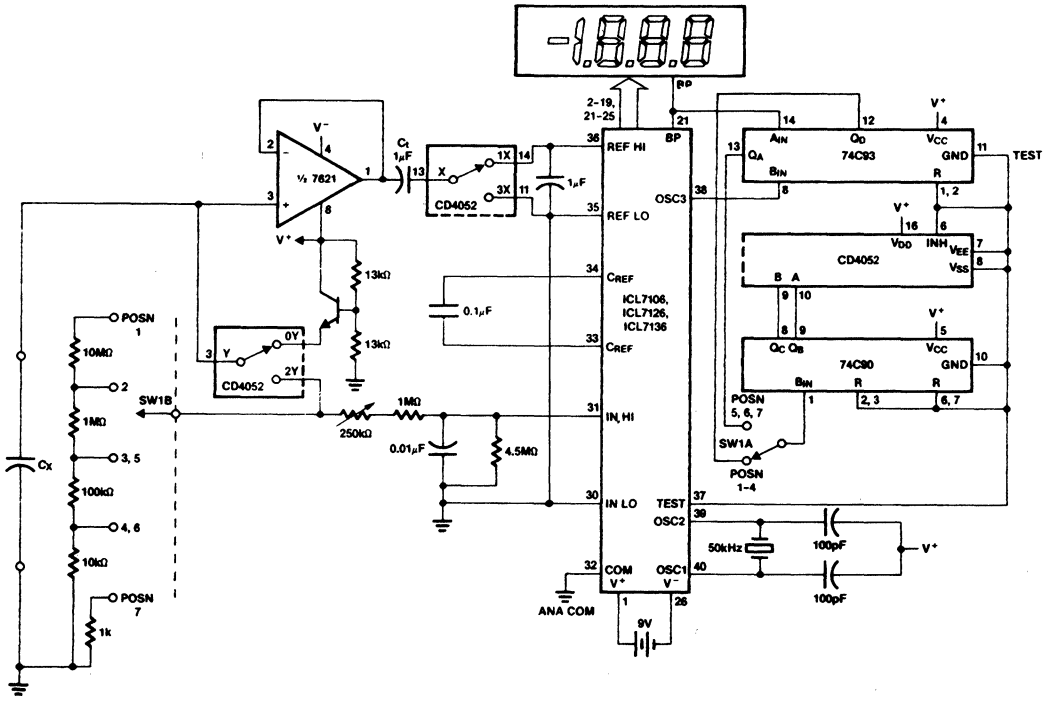
*ICL7106/7 only. See data sheets or A052 for correct values of these components.

Figure 15: Switching Preamp with Gain of 10

Most low cost dual amplifiers are suitable, but it is important that the negative and positive slew rates be reasonably close. Op amps with crossover distortion (such as the LM124/324) should not be used. See Figure 23 and also application notes A030 and A053 for alternative preamplifier circuits.

Capacitance Meter Based on 3½-Digit A/D

The circuit charges and discharges a capacitor at a crystal-controlled rate, and stores on a sample-and-difference amplifier the change in voltage achieved. The current that flows during the discharge cycle is averaged, and ratiometrically measured in the A/D using the voltage change as a reference. Range switching is done by changing the cycle rate and the current metering resistor. The cycle rate is synchronized with the conversion rate of the A/D by using the internal OSCillator (externally divided) and the (internally divided) BackPlane signals. For convenience in timing, the switching cycle takes 5 counter states, although only four switch configurations are used. Capacitances up to 200μF can be measured, and the resolution on the lowest range is down to 0.1pF.



LC02310I

	SWITCH 1A	SWITCH 1B	MAX C	COUNTER/SWITCH PHASES		
1	10MΩ	6kHz	200pF	0Y	00	Charge C_X
2	1MΩ	6kHz	2nF	1Y	01	ΔV_{CX} on C_{REF}
3	100kΩ	6kHz	20nF	2Y	10	Discharge C_X thru R_{net}
4	10kΩ	6kHz	0.2μF	3X	11	Reset C_t to zero
5	100kΩ	60Hz	2μF			
6	10kΩ	60Hz	20μF			
7	1kΩ	60Hz	200μF			

Figure 16: Capacitance Meter Built on 3½-Digit Meter

Eliminating Overrange Hangover of Dual-Slope A/D Converters

Intersil's two chip 4½-digit and 14-16-bit dual-slope A/D converters have eliminated most of the hassle of building accurate data acquisition systems, DVMs, DPMs, etc. However, the published standard hook-up circuits can, under some circumstances, give inaccurate readings. The most annoying of these is after an overload, when the residual voltage on the integrator is transferred, as a transient, to the auto-zero system, which then in turn has to settle back down. The effect is described in A030. In any system with a multiplexed input, having succeeding channels disturbed by an overload condition on one channel can be a severe problem.

This "hangover" can be eliminated by adding a simple 2 IC circuit to zero the integrator output at the beginning of the auto-zero cycle, as shown in Figure 17(a) for the ICL8052/71(C)03 device, and Figure 17(b) for the ICL8052/7104-16 device. The circuit works by connecting the comparator output to an inverting input on the buffer during the first portion of the auto-zero time, and then (as normally) to the auto-zero capacitor for the remainder [Figure 17(c)]. Half of the ICM7556 controls the timing, the other half forming the clock oscillator, and the ICL8053 performs the switching. This circuit is used, rather than other more normal switch devices, because of its low charge injection into the auto-zero capacitor.

The Zero Integrator time can be set initially at 1/3 to 1/2 the minimum auto-zero time, but if an "optimum" adjustment is required, look at the comparator output with a scope under worst-case overload conditions. The output of the delay timer should stay low until after the comparator has come off the rail, and is in the linear region (usually fairly noisy).

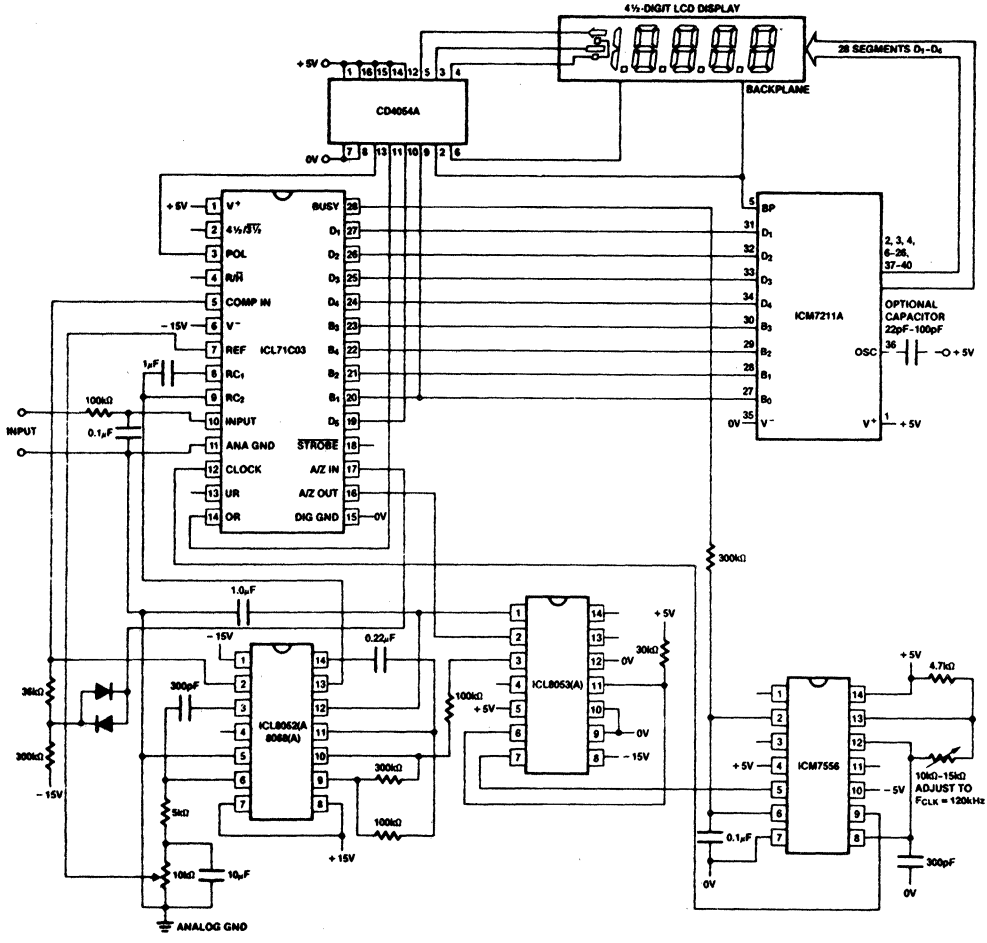
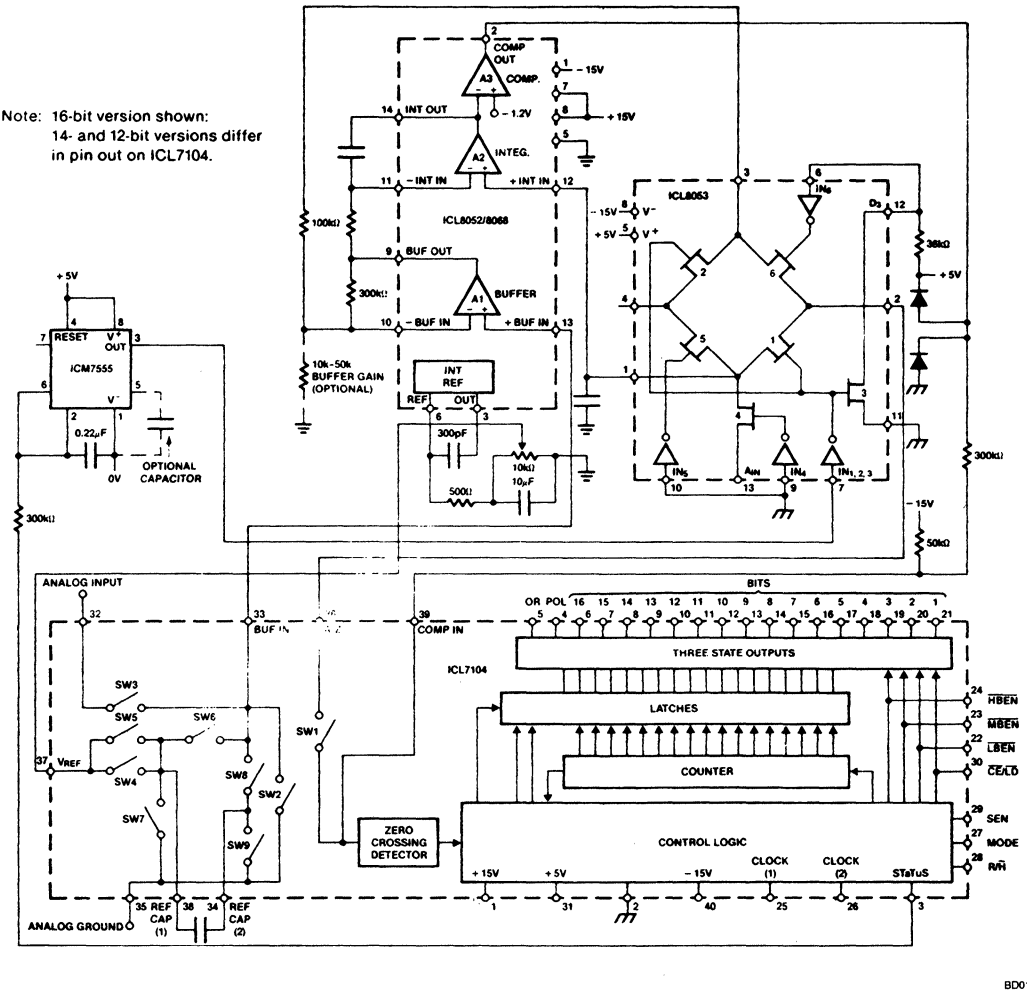


Figure 17(a): 4½-Digit LCD DPM with Zero Integrator Phase



*Note: 16-bit version shown: 14- and 12-bit versions differ in pin out on ICL7104.

Figure 17(b): 8052A (8068A)/7104 16-/14-/12-Bit A/D Converter Functional Block Diagram with Gross Overrange Protection Zero Integrator Phase Circuit

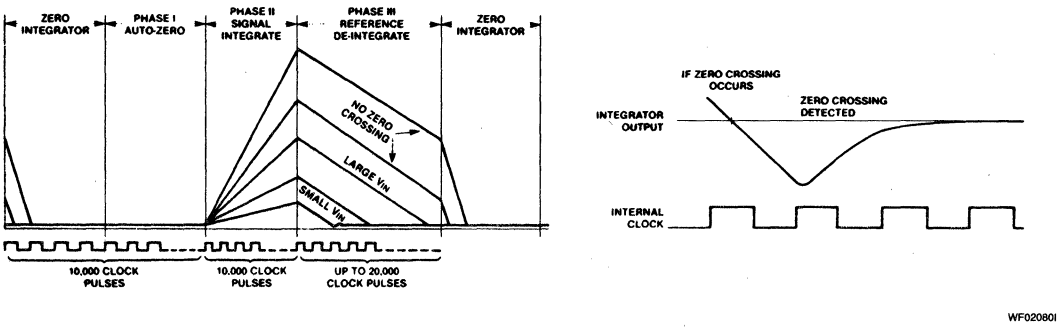


Figure 17(c): 4½-Digit A/D Converter Timing Diagrams

Under non-overload conditions, a small "zero integrator" phase is desirable, but the full time given here is not necessary. A P-channel MOSFET across the timing resistor can be used to reduce the time constant if overrange has not occurred. Alternatively, a 3-diode network can be used, or a 2-input OR gate, as in Figure 17(d).

The delay circuit also introduces a delay from the beginning of the conversion interval before the Zero Integrator phase is enabled; this delay should not exceed the input integrate time. If circuit modifications are made, this should be checked.

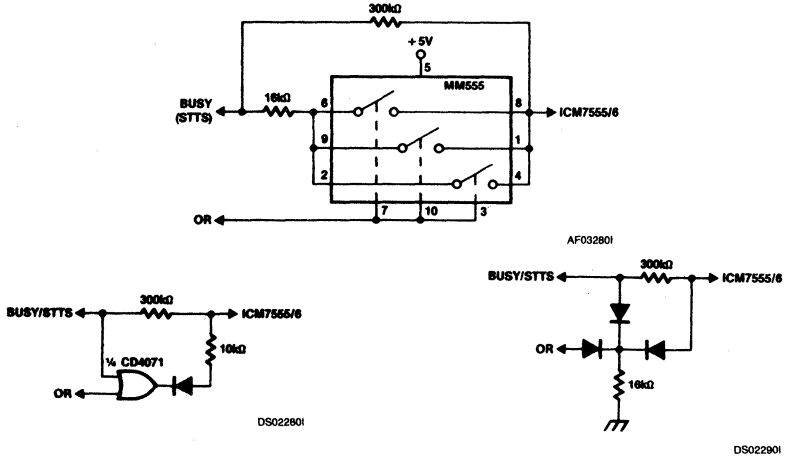


Figure 17(d): Timing Gross Overvoltages

A/D Converter and Counter make Auto-Tare Weighing Electronics

Using Intersil's ICL7109 12-bit A/D and ICM7217 4 decade display driving counter, this circuit provides simple pushbutton tare for a weighing machine and requires only a single 5V supply. With any tare weight on the scale, the press of a button zeroes the display, which then reads weight added or removed.

Operated in its handshake mode, the ICL7109 dual-slope converter gives a $\overline{\text{HBEN}}$ pulse at pin 19 one clock period after detection of zero crossing. By the nature of dual-slope conversion the zero crossing, hence the $\overline{\text{HBEN}}$ pulse, will move N clock periods later as the input is increased N bit values, and vice versa [see Figure 18(b)]. Each conversion cycle lasts 8192 clock periods.

The 7109 input can be derived from a bridge connected load cell powered from the same 5V supply as the ICL7109 and its reference, so the ratiometric operation of the 7109 rejects supply variations.

The ICM7217 4 decade bidirectional counter has display latches enabled by $\overline{\text{STORE}}$ (pin 19) which drive a multiplexed LED display. The $\overline{\text{ZERO}}$ output (pin 2) indicates the zero state of the counter, which also has a $\overline{\text{RESET}}$ input (pin 14). A separate compare register is preloaded via diodes from the display digit selects to the BCD port when Load Register (pin 11) is high. $\overline{\text{EQUAL}}$ (pin 3) goes low when register and counter are equal.

At power-up, the 10μF capacitor on Load Register (pin 11) preloads the compare register to 4096. The counter UP/$\overline{\text{DOWN}}$ line is controlled by a flip-flop (½ 74LS74) alternately set and reset by $\overline{\text{ZERO}}$ and $\overline{\text{EQUAL}}$ so the counter cycles up and down between zero and 4096, taking 8192 clock periods per cycle.

With a steady weight on the scale, the $\overline{\text{HBEN}}$ pulse from the 7109 activates the $\overline{\text{STORE}}$ input of the 7217 every 8192 clock periods to give a steady, but initially random display. When the TARE switch is closed, the counter is reset by $\overline{\text{HBEN}}$, zeroing the display. Even when the TARE switch is opened, the display remains zero because, with an unchanged weight, $\overline{\text{HBEN}}$ enables the display latches each time the counter passes zero [solid line in Figure 18(b)].

If weight corresponding to N bit values is added to the scale, $\overline{\text{HBEN}}$ moves N counts later, hence N will be latched and displayed [dotted line in Figure 18(b)]. Conversely, if N bit values of weight are removed, −N is displayed (dashed line in Figure 2). The minus sign is obtained by latching the state of the UP/$\overline{\text{DOWN}}$ line at HBEN in the second flip-flop.

The only restriction is that the converter input must not change polarity. If necessary, the POL output (pin 3) of the 7109 can be latched to warn of such an erroneous condition.

For more than 4096 count resolution, the 7109 can be replaced by the ICL8052A/ICL7104 2-chip converter set with up to 16-bit resolution. The ICM7217 counter is cascadable. The system can clearly also operate with force balance type weighing systems or other types of input signal.

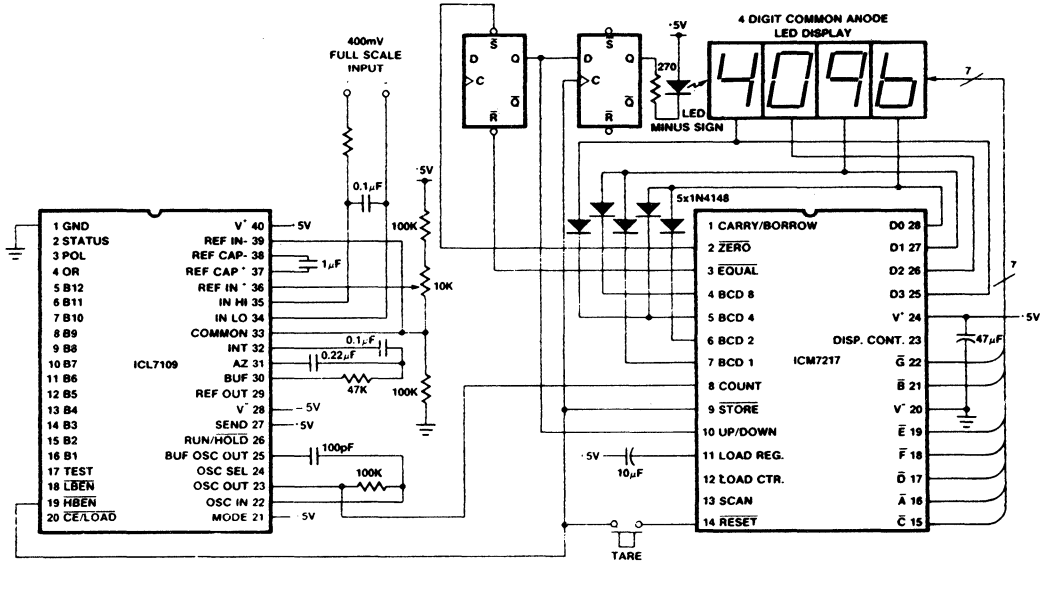


Figure 18(a): Auto-Tare Weighing System for A/D Converter

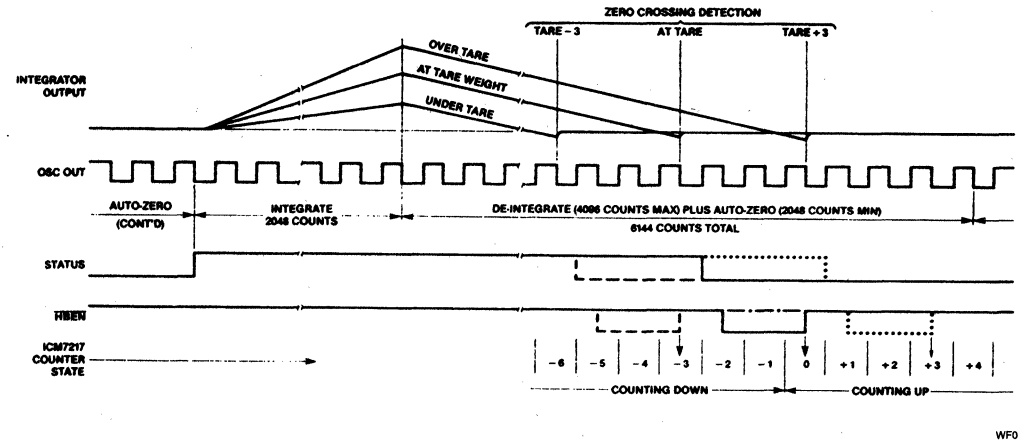


Figure 18(b): Auto-Tare Weighing System Waveforms

3¾-Digit (± 4095 Count) Meter with LED, LCD or VF Display

Using an ICL7109 12-bit A/D, an ICM7224, 7225 or 7236 counter/display driver and two 4000 series CMOS chips you can build a 3¾-digit (4095 count) auto polarity digital meter. The choice of counter determines the choice of display. ICM7224 drives liquid crystal displays, ICM7225 drives common anode LEDs and ICM7236 drives bright, green vacuum fluorescents.

Figure 19(a) shows the system schematic. The ICL7109 is run in its handshake mode (MODE wired high). The analog input is completely conventional and the analog connections are not shown in detail. Waveforms are shown in Figure 19(b).

The ICL7109 takes 8192 clock cycles to complete a conversion, 2048 for auto-zero, 2048 for signal integrate and 4096 for reference de-integrate. STATUS goes high at the beginning of signal integrate and comes low 1½ cycles after the zero crossing, giving a total of 2050 + N pulses of the clock while status is high, where N is the digital reading of the A/D. Therefore, by counting clock pulses while STATUS is high and subtracting 2050, the reading can be obtained.

The ICM7224/7225/7236 display driving counters have identical input configurations. They contain a 4½ decade counter with CLOCK, $\overline{\text{RESET}}$ and $\overline{\text{COUNT INHIBIT}}$ inputs and separate display latches activated by $\overline{\text{STORE}}$. These latches in turn drive, via decoders, non-multiplexed 7-segment displays.

When STATUS goes low, RESET of the CD4040 is taken high and the bi-stable composed of gates 3 and 4 is set, taking $\overline{\text{COUNT INHIBIT}}$ low. At the beginning of integrate STATUS goes high, removing RESET from the CD4040 and allowing it to start counting. Gate 3 detects the count of 2050 and resets the bi-stable, removing $\overline{\text{COUNT INHIBIT}}$ and allowing the counter to count clock pulses. When STATUS goes low after zero crossing the bi-stable is again set, and further counting inhibited. The counter has now counted any pulses over 2050, hence now contains the required reading. This is transferred to the display latches by $\overline{\text{HBEN}}$ from the 7109. The counter is reset by $\overline{\text{LBEN}}$ and the circuit is now ready for the next conversion cycle. The binary outputs of the 7109 are not used.

Of course, other counters can be used instead of the ICM7224/7225/7236, but these are extremely convenient in their ability to drive displays directly. The ICM7217 could be used with LED displays and its compare register could also be employed to provide an over or under limit indication.

Should greater resolution (up to 65536 counts) be required, the ICL7109 may be replaced by the ICL8052/8068 + ICL7104 14- or 16-bit converters, which have the same output interface as the 7109. The ICM7224/25/36 counters are cascadable. In this case the CD4040 counter chain would have to be extended to the appropriate length for 14- or 16-bit operation, as in these cases 8194 and 32770 counts respectively would have to be subtracted.

Because the display drive is non-multiplexed, it is convenient to mount the counter/display driver package on the same board as the displays. Only 4 signal connections (i.e., COUNT, $\overline{\text{COUNT INHIBIT}}$, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$) are then required from the main circuit board to the display board. Moreover, by interchanging display boards LED, LCD or Vacuum Fluorescent meters could be made using the same main circuit board.

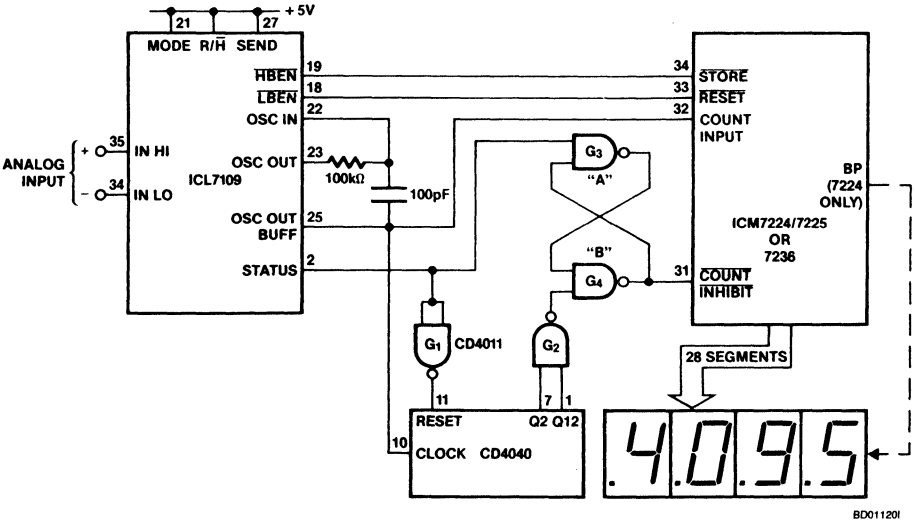


Figure 19(a): Block Schematic

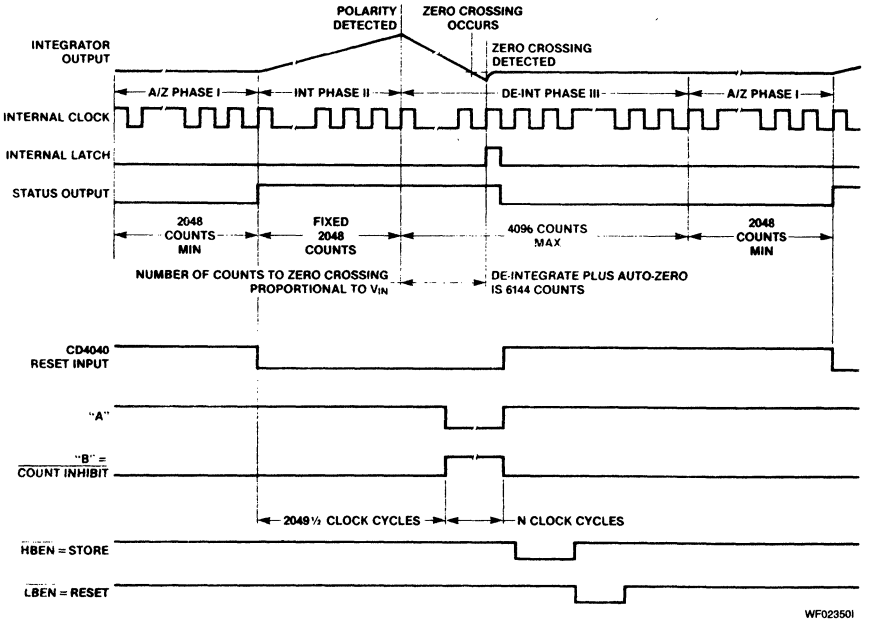
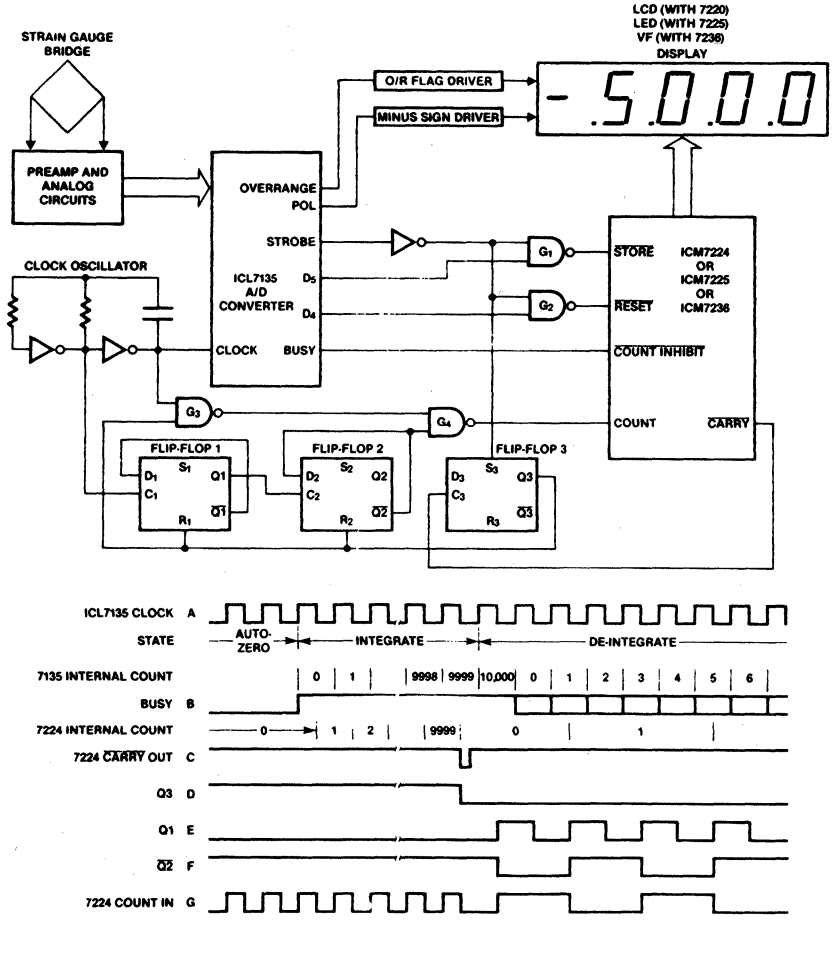


Figure 19(b): Operating Waveforms

5000 Count Weighing with ¼ Count Resolution

Low cost digital scales are readily built using a strain gauge transducer, and ICL7650 chopper stabilized CMOS amplifier, a dual-slope A/D converter such as Intersil's ICL7106/7 (3½-digit), ICL7109 (12-bit binary) or ICL7135 (4½-digit) single chip CMOS devices, plus, if necessary, a display driver. To be approved for trade, however, the electronics must resolve to ¼ of a displayed increment. This can be simply arranged by replacing the display driver with a display driving counter and a handful of standard SSI CMOS.

The ICL7135 4½-digit dual-slope A/D chip has 3 phases of operation: auto-zero, integrate and de-integrate. In the auto-zero phase, offsets are measured and nulled and the BUSY output is low. During integrate, the BUSY output goes high and the ICL7135 integrates the input signal for 10,000 clock cycles. During de-integrate, the reference is integrated until the integrator returns to its starting point (or zero crossing). If N is the digital reading, de-integrate lasts N + 1 clock cycles (the extra one is due to the fact that de-integrate actually ends on the next positive clock edge after zero crossing), and at the end of this, BUSY returns low. BUSY is therefore high for a total of 10,001 + N clock cycles, and clearly the reading can be determined by counting clock cycles while BUSY is high and subtracting 10,001.



DS023001

Figure 20: 5000 Count Meter with Internal ¼ Count Resolution

In our case, we wish to display N/4, so that the 20,000 count conversion will yield a full-scale reading of 5000. This is done by delaying for 10,001 clock cycles after BUSY goes high, then enabling a counter clocked at 1/4 the 7135 clock rate. When BUSY goes low this counter is halted, its contents transferred to the display, and reset ready for the next cycle. A small refinement is that the counter should increment at values of 2, 6, 10 etc., rather than at 4, 8, 12 etc. so that quantization error is symmetrical about the reading. A useful economy is to use the same counter for the initial 10,000 clock cycles and for the final counting. Suitable counters are Intersil's ICM7224 (driving LCD display), ICM7225 (driving LED display) or ICM7236 (driving VF display). Apart from the display drivers, these are identical 4 1/2-decade counters.

The circuit works like this; during auto-zero, when BUSY is low, the counter is disabled via its $\overline{\text{COUNT INHIBIT}}$ input. Flip-flop 3 is set, so that its Q output holds flip-flops 1 and 2 reset and gate 3 is enabled, passing 7135 clock pulses to the counter.

At the beginning of integrate, BUSY goes high and the counter begins to increment. Notice that the counter and flip-flops are incremented on the falling edge of clock, while the ICL7135 increments on the rising edge, avoiding race conditions. After 10,000 counts, the falling edge of $\overline{\text{CARRY}}$ clocks flip-flop 3 to its reset state. Flip-flops 1 and 2 are now enabled to divide the input clock by 4, while G_3 blocks direct clock input to the counter, which has now rolled to zero.

The preset conditions of flip-flops 1 and 2 are such that the first rising edge of Q2 comes 3 clock cycles later, so the counter increments to 1 just before the ICL7135 increments to 2, and so on. At the end of de-integrate BUSY comes low, freezing the counter. The $\overline{\text{STROBE}}$ output of the ICL7135 consists of 5 pulses, one coincident with each digit select, during the first multiplexed output scan cycle after de-integrate ends. $\overline{\text{STROBE}}$ is used to set flip-flop 3, restoring initial conditions ready for the next conversion. $\overline{\text{STROBE}}$ gated with D_5 stores the counter contents in the display register, then $\overline{\text{STROBE}}$ with D_4 resets the counter. Notice that the normal BCD outputs of the 7135 are unused.

A Logarithmic A/D Converter

An ordinary single chip DVM can be easily converted to display the logarithm of the ratio of 2 input voltages V_1 and V_2. The main restriction on operation is that $V_1 \geq V_2$.

Figure 21(a) shows the configuration. The modifications from the standard connection are the potential divider (ratio K) on the reference input, the signal input being the difference between V_1 and V_2, and the addition of resistor R_p in parallel with the integrator capacitor. The time constant of the integrator capacitor and R_p is given by:

$$\tau = C_{INT}R_p.$$

Referring to the waveforms of Figure 21(b), let us first calculate the final integrator voltage, V_{INT}. The aiming potential of the exponential is given by:

$$V_{ASSYMPTOTE} = \frac{R_p}{R_{INT}} (V_1 - V_2)$$

and the final integrator voltage is therefore:

$$V_{INT} = \frac{R_p}{R_{INT}} (V_1 - V_2) \left(1 - e^{\frac{-T}{\tau}}\right)$$

where T is the fixed integration period.

During de-integrate, the total swing of the exponential is given by:

$$V_{TOTAL} = V_{INT} + V_{REF} \frac{R_p}{R_{INT}}$$

and remembering that $V_{REF} = KV_2$, the total exponential swing is:

$$V_{TOTAL} = \frac{R_p}{R_{INT}} (V_1 - V_2) \left(1 - e^{\frac{-T}{\tau}}\right) + \frac{R_p}{R_{INT}} KV_2.$$

The integrator will actually cross zero when the exponential has reached

$$V_{FINAL} = V_{REF} \frac{R_p}{R_{INT}} = \frac{R_p}{R_{INT}} KV_2.$$

Therefore, the time to zero crossing is given by:

$$T_{DE\text{-}INT} = \tau \ln \left(\frac{V_{TOTAL}}{V_{FINAL}}\right)$$

$$= \tau \ln \left(\frac{\frac{R_p}{R_{INT}} (V_1 - V_2) \left(1 - e^{\frac{-T}{\tau}}\right) + \frac{R_p}{R_{INT}} KV_2}{\frac{R_p}{R_{INT}} KV_2} \right)$$

$$= \tau \ln \left(\frac{(V_1 - V_2) \left(1 - e^{\frac{-T}{\tau}}\right) + KV_2}{KV_2} \right)$$

Now, if we are sneaky, and make $K = \left(1 - e^{\frac{-T}{\tau}}\right)$,

$$T_{DE\text{-}INT} = \tau \ln \frac{K(V_1 - V_2) + KV_2}{KV_2} = \tau \ln \frac{V_1}{V_2}$$

Now let us make $\tau = \frac{T}{2.3}$

where T is the integration period:

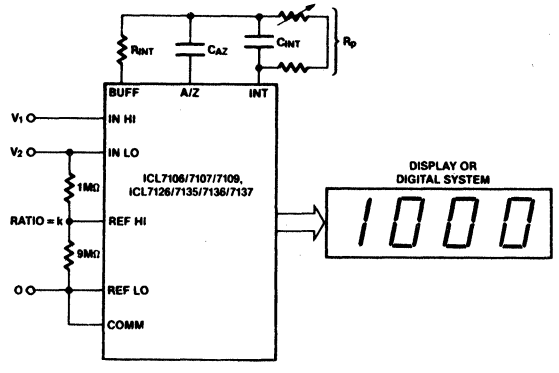
$$\text{Now } T_{DE\text{-}INT} = \frac{T}{2.3} \ln \frac{V_1}{V_2} = T \log_{10} \frac{V_1}{V_2}$$

so that the DVM will read 1,000 ($T_{DE\text{-}INT} = T$) when $V_1/V_2 = 10$, which is correct. The divider ratio, K, is:

$$K = \left(1 - e^{\frac{-T}{\tau}}\right) = 1 - e^{-2.3} = 1 - 0.1 = 0.9$$

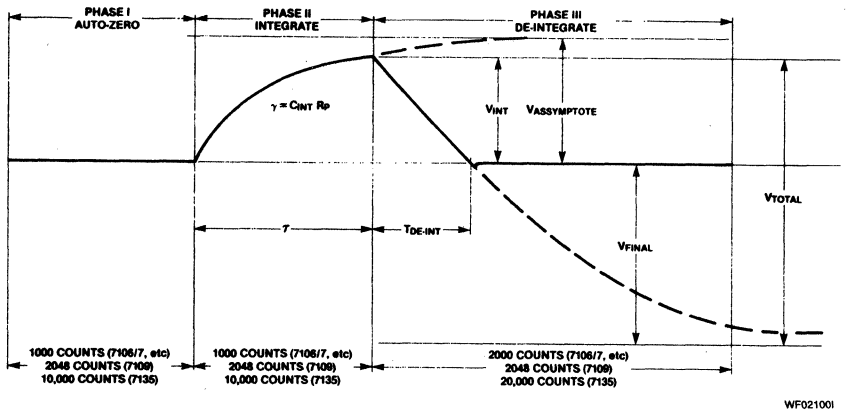
which makes sense when you realize that the final integrator voltage during the integrate phase must reach 0.9 of the assymptote level.

Theoretically, the full-scale of the system is $V_1/V_2 = 100$ (i.e., when the log = 2) but noise will probably limit this to lower values. Note also that the accuracy of the system is no longer independent of passive component variations. The simplest set-up procedure is to ensure K = 0.9 (preferably using a pretrimmed divider) then, with $V_1 = 10V_2$, adjust R_p until the reading is 1.000. Examples of the use of logarithmic readings are photographic and chemical densitometry and colorimetry and audio decibel scales.



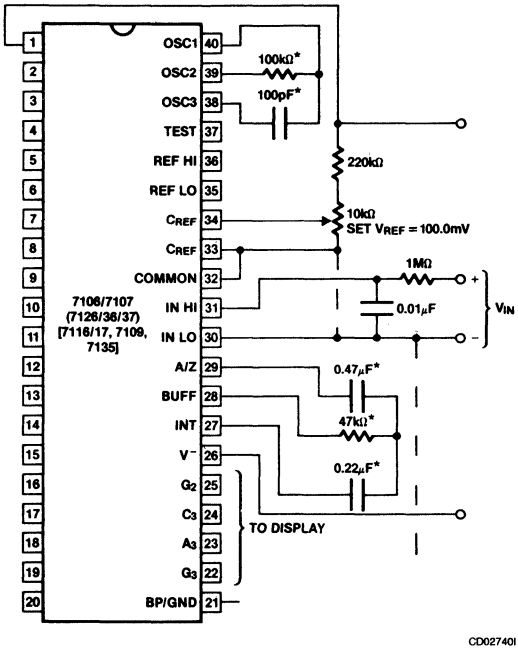
LC02340I

Figure 21(a): Circuit Modifications for Logarithmic Operation. For ICL7116, ICL7117, and ICL7135, REF LO is already connected to ANALOG COMMON



WF02100I

Figure 21(b): Integrator Output Waveforms with Respect to Integrator Non-Inverting Input



*ICL7106/7 only. See data sheet for values for other parts.

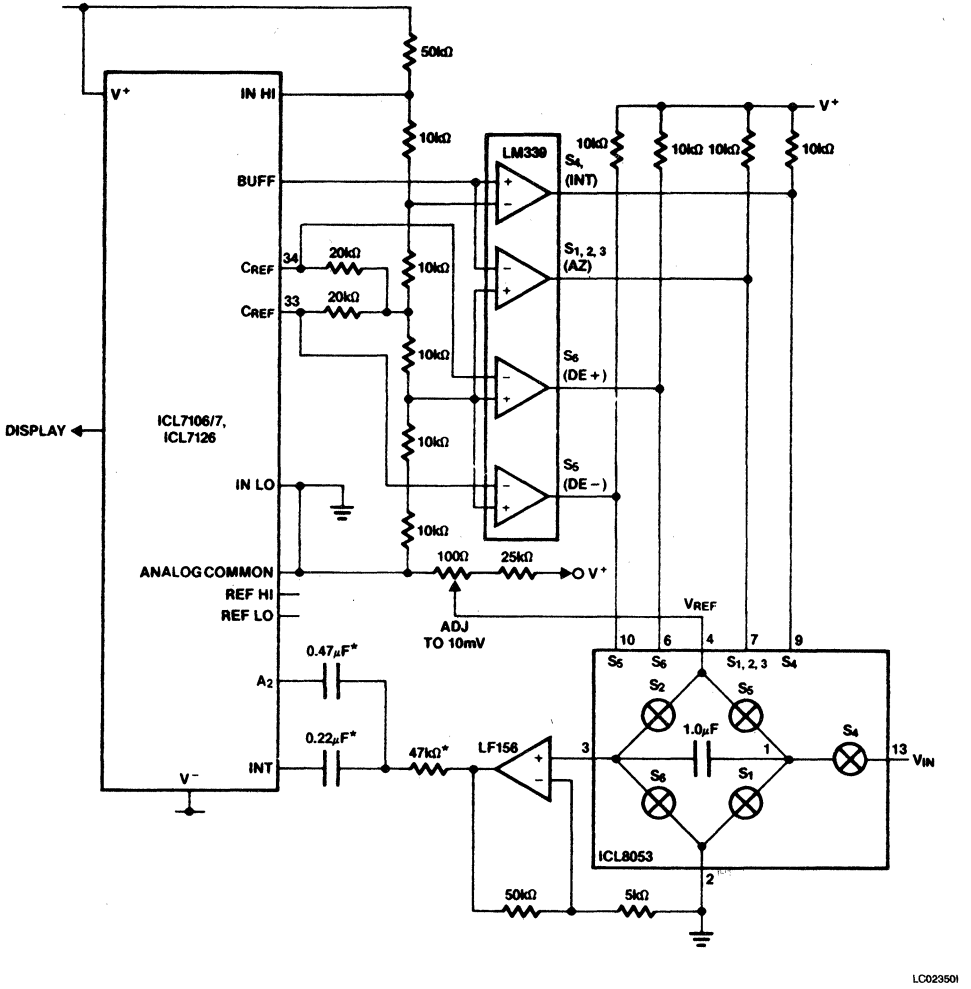
Figure 22: A "No-Ref-Cap" Circuit. This circuit gives correct negative readings but very high (or O/R) readings for positive inputs

No-Ref-Cap Circuits

In many cases, the polarity of the input voltage is always known, or a different reference is required for different polarities. In other applications, it may be desirable for the reference voltage to vary in some manner during the conversion, for instance to achieve some nonlinear conversion function. In all these cases, the reference capacitor is undesirable or un-needed. Figure 22 shows the way in which it can be removed, and the desired reference voltage fed directly into the C_{REF} pins(s). Note that the reference source may be shorted out in some phases of the conversion, so a current-limiting impedance must be provided.

Low Noise Preamp Circuit

The noise performance of the ICL7106/7/9 family is controlled by the noise trapped on the auto-zero capacitor at the beginning of the integrate phase. This noise depends (in a complicated way) on the input noise of the buffer amplifier. If the built-in buffer is replaced by a low noise op amp, the noise performance could be improved, especially if gain can be introduced into this buffer, as can be done with the 2-chip devices. Figure 23 shows a way of doing this, the main losses being in higher input current and the lack of a true differential input. The switch network of the original is replaced by an ICL8053 driven in synchronism with the internal counter by using the original switch network-buffer combination, fed by resistive dividers, and a quad comparator to detect the various phases as shown.



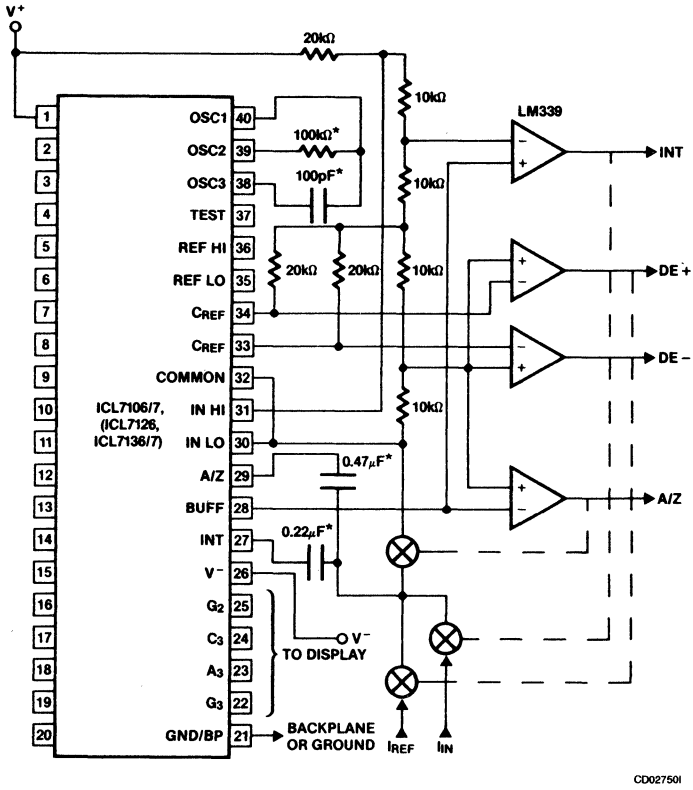
LF156, LM339, 8053 run off V^+ and V^-, 10V. These values should be changed for ICL7126.

Figure 23: Using an External Low-Noise Preamp with the ICL7106/7/26

Current I/P Converter Circuit

The normal voltage conversion circuits convert the differential input and reference voltages into corresponding currents in the integrating capacitor. In cases where the input signal is fundamentally a current in the appropriate range, it may make more sense to integrate it directly, rather than convert it to a voltage first, especially if the reference value is a current also.

The circuit of Figure 24 injects the currents directly into the integrator input. The sources are switched in synchronism with the internal conversion phase by using the buffer amplifier and the voltage switching network in combination with a quad comparator, in the same manner as in Figure 23. The normal auto-zero operation still occurs, provided the input is grounded during the appropriate phase.

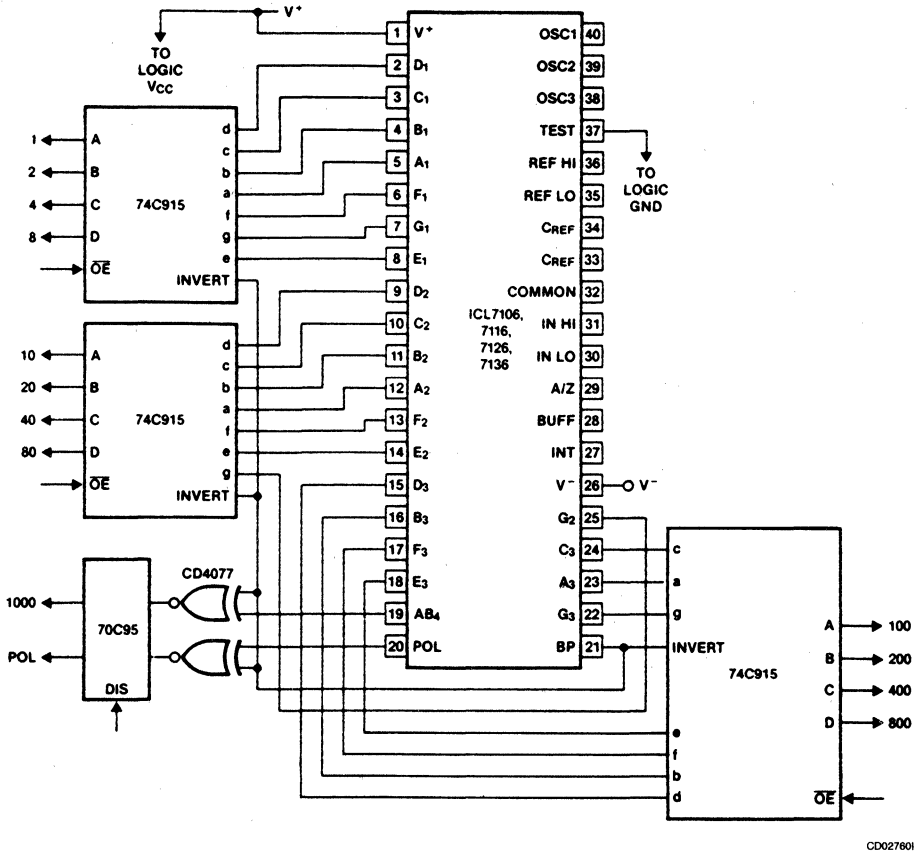


*See A052 for calculation on these values.

Figure 24: Current I/P Converter Circuit

BCD Output from 7-Segment O/P Drive

Frequently it is necessary to provide a BCD output in addition to display driving, for peripheral output on panel meters, or for special decoding of upper/lower limit values, etc. The circuits shown here use a standard CMOS gate circuit to convert the 7-segment output of either LCD or LED drivers to BCD.



*For ICL7107/7117, tie "INVERT" high, use OV supply for logic GND, and omit EX-NOR gates.

Figure 25: BCD Output from 7-Segment O/P Drive

OTHER APPLICATIONS BULLETINS

Some other applications bulletins that may be found useful are listed here:

A016 Selecting A/D Converters.
A017 The Integrating A/D Converter.
A018 Do's and Dont's of Applying A/D Converters.
A019 4-½ Digit Panel Meter Demonstrator/ Instrumentation Boards.
A023 Low Cost Digital Panel Meter Designs.
A025 Building a Remote Data Logging Station.
A028 Building an Autoranging DMM with the ICL7103A/ 8052A A/D Converter Pair.
A030 The ICL7104 — A Binary Output A/D Converter for Microprocessors.
A032 Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family.
A046 Building a Battery Operated Auto-Ranging DVM with the ICL7106.
A051 Principals and Applications of the ICL7660 Voltage Converter.
A052 Tips for Using Single-Chip 3½-Digit A/D Converters.
A053 The ICL7650: A New Era in Glitch-Free Chopper Stabilized Amplifiers.
R005 Interfacing Data Converters and Microprocessors.

AO52

Tips for Using Single-Chip 3-½ Digit A/D Converters

by Dan Watson

INTRODUCTION

Since their introduction, the single-chip 3-½ digit A/D converters have been widely accepted and used in a variety of digital instrumentation applications. As the number of applications for these low-cost circuits increases so does the number of specific questions about their operation.

The products covered are Intersil's full line of single-chip 3-½ digit A/D converters.

They are:

- ICL7106, ICL7116 for liquid crystal displays (LCD)
- ICL7107, ICL7117 for light emitting diode displays (LED)
- ICL7126 micropower version for LCD

A great deal of versatility has been designed into these devices. All have differential inputs for signal and reference. This permits applications where input and reference are not referred to ground; it also allows the ratio of two signals to be digitally displayed. The devices also feature wide operating ranges for power supply voltage and conversion time.

The first part of this application note will address the most commonly asked questions, the second part consists of a troubleshooting guide, the third section shows normal waveforms, and the fourth gives formulae for component values.

COMMONLY ASKED QUESTIONS

Power Supply

Q: What is the minimum battery voltage from which the ICL7106 or ICL7126 can operate?

A: If the internal voltage reference of the circuit is used, the ICL7106 and ICL7126 will operate down to approximately 6.5 Volts. When the battery voltage drops below that level the internal voltage reference will degrade, directly affecting converter accuracy.

If an external voltage reference such as the ICL8069 is used, a lower operating voltage can be used. Care must be taken to ensure that the input common-mode voltage range is not exceeded and that the integrator output swing is kept within its linear region. (See appropriate discussion in data sheets for specifics.) If these parameters are kept in check the ICL7106 and ICL7126 will operate accurately with a battery voltage as low as 4 Volts.

Q: How can the ICL7106 be used with fixed system power supplies?

A: The ICL7106 has been designed to be used with a 9 Volt battery. When ±15 Volt supplies are used, they should be converted to ±5 Volts with simple three terminal regulators such as μA7805 and μA7905, or the new low power ICL7663 and ICL7664. If only a +5 Volt supply is available, an ICL7660 voltage converter circuit can be used to generate −5 Volts at 20mA from the +5 Volt supply. See Figures 1 and 2.

Once a proper dual polarity power supply has been set up, the ICL7106 will make A/D conversions from input voltages referred to power supply ground. Figures 3 and 4 show the use of the ICL7106 with internal and external voltage reference. Note the 27kΩ pull up resistor on analog COMMON (pin 32) when using an external reference.

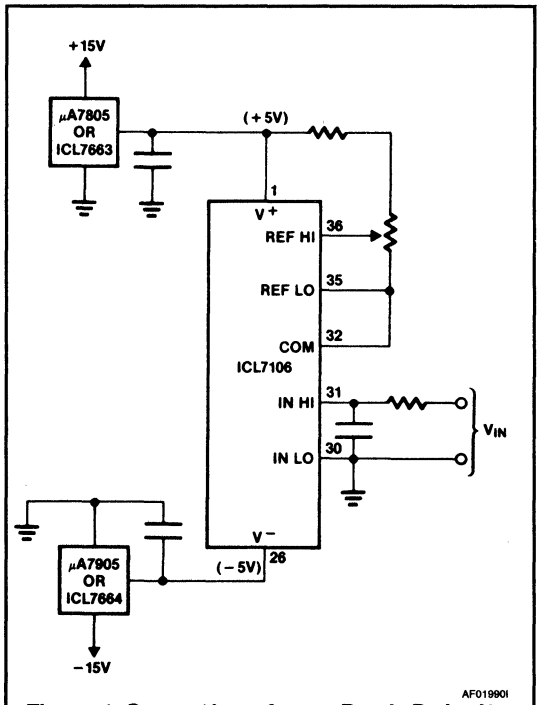


Figure 1: Operation from Dual Polarity Supplies with Internal Voltage Reference

Q: How well regulated must the power supply for the ICL7107 be?

A: The ICL7107, ICL7106, and ICL7126 have power supply rejection ratios of 86dB typically, and a power supply with 50mV load regulation or better is recommended. High frequency signals and spikes on the power supplies can get into the A/D system, and should be bypassed to ground.

Q: How long will an ICL7106 and an ICL7126 operate from a standard 9 Volt battery?

A: A standard carbon-zinc 9 Volt battery will provide 200 continuous hours of operation for the ICL7106 and 8,000 continuous hours for the ICL7126.

Q: How much power supply current is needed to operate the ICL7107?

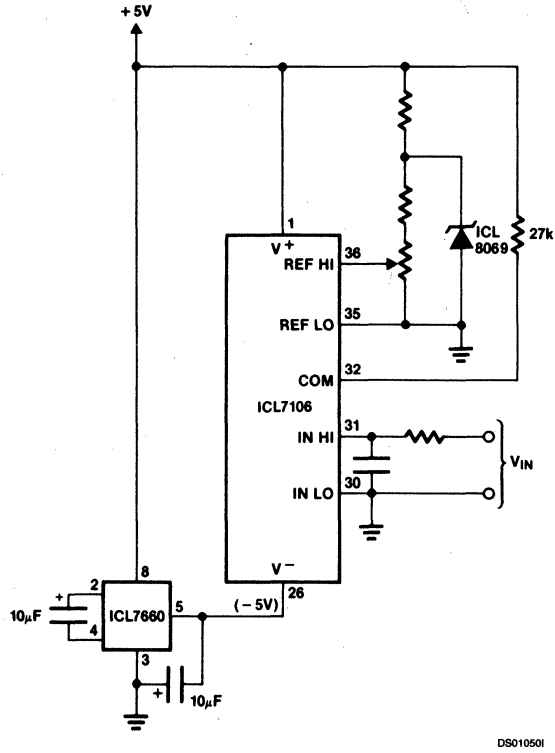


Figure 2: Operation from +5V Supply with External Voltage Reference

A: The supply current from the positive power supply varies from 72mA to 200mA depending upon the combination of display segments lighted. The ICL7107 (without display current) requires typically 1.5mA from the positive supply and 300μA from the negative supply.

Q: What is the maximum power supply voltage for the ICL7106 and ICL7107?

A: The ICL7106 has an absolute maximum battery voltage rating of 15 Volts from V^+ (pin 1) to V^- (pin 26). The ICL7107 has an absolute maximum rating of 6 Volts from V^+ to ground (pin 21) and −9 Volts from V^- to ground. If the positive voltage to the ICL7107 is greater than 6 Volts, excessive power dissipation will result. To increase LED brightness, use external drivers such as SN7407 or discrete transistors; see ICL7107 data sheet Figure 22.

Display

Q: How can the displayed reading of the ICL7106 or ICL7107 be held for a time rather than continuously updated?

A: The ICL7106 and ICL7107 are designed to continuously update the display as each conversion is completed. For applications where it is desirable to hold the displayed reading, either the ICL7116 (LCD) or the ICL7117 (LED) should be used. These parts are the same as the ICL7106 and ICL7107 except that they have built-in display hold function and slightly different pinout configurations. When the HLD terminal (pin 1) is connected to V^+, the displayed reading is frozen and the converter continues in its cycle; when the HLD pin is connected to TEST or Digital Ground (7117 only) the display updates with each conversion. The pinout differences are as follows:

1. Pin 1 is the HLD pin.
2. Pin 35 is the positive power supply pin.
3. REFerence LO is internally connected to the analog COMMON point. REFerence LO does not connect to a package pin separately.

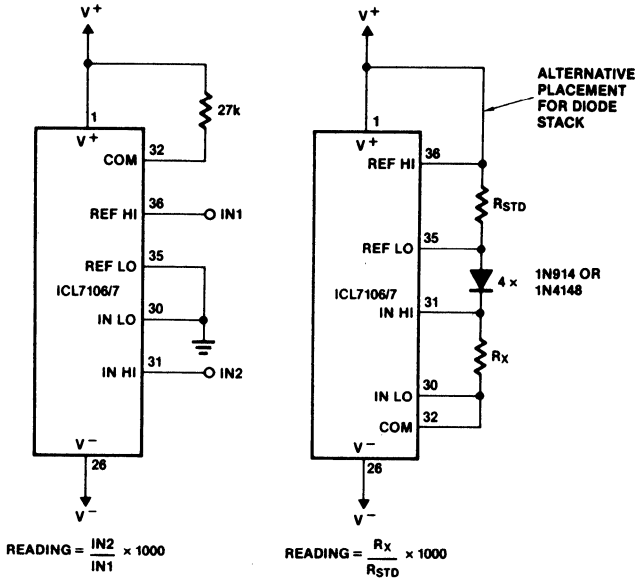


Figure 3: Examples of Ratiometric Operation

Q: What types of displays should be used with the ICL7106?

A: The ICL7106 drive signal is approximately 3.5Vrms with a backplane frequency of 60Hz, and will drive almost any size character liquid crystal display. The 0.5" variety is the most common and inexpensive. Suitable displays include the 6FE0203-E from AND, the SX140 from Crystaloid, the 3902-315 from Hamlin, and the 7543-W-2 from LXD.

Q: What types of displays should be used with the ICL7107?

A: Almost any common anode seven-segment LED display will work with the ICL7107. The ICL7107 drives the LEDs with current-limited outputs of 7mA to 8mA per segment; this will automatically compensate the LEDs for different V-I characteristics. For more contrast, use displays that are more efficient. Suitable displays include the Hewlett Packard 5082-7736/30, the ITAC MAN3730/10, the Litronix DL701/7 and the Monsanto 4630/10.

Timing

Q: How fast can the ICL7106 or ICL7107 be operated?

A: The maximum oscillator frequency of the ICL7107 and ICL7106 should normally be considered to be 240kHz. This frequency is the highest frequency that will reject 60Hz noise in the integrator (200kHz for 50Hz rejection). Since the signal integrate phase of the conversion cycle is 1000 clock pulses long, and one cycle of 60Hz lasts 16 2/3ms, the internal clock frequency is:

$$\frac{1000}{0.01667} = 60\text{kHz}$$

The internal clock is generated by dividing the oscillator frequency by four, therefore, the oscillator frequency will be 240kHz. This corresponds to 15 conversions per second. In applications where 50Hz or 60Hz rejection is not required, the devices may be operated up to 30 readings per second (480kHz). At this high speed, however, the devices may tend to read one count high.

Ratiometric Operation

Q: What is ratiometric operation and how can the ICL7107 or ICL7106 be operated in that manner?

A: In a ratiometric application the ICL7106 and ICL7107 will display a reading which is proportional to the ratio of two inputs. In this mode, one signal is connected between INPUT HI and INPUT LO, and the other signal is connected between REF HI and REF LO. For signals which share a common connection, INPUT LO and REF LO should be connected together, see Figure 3. When the two input signals are equal, the reading will be 1000. The maximum readable ratio of two inputs is 1.999.

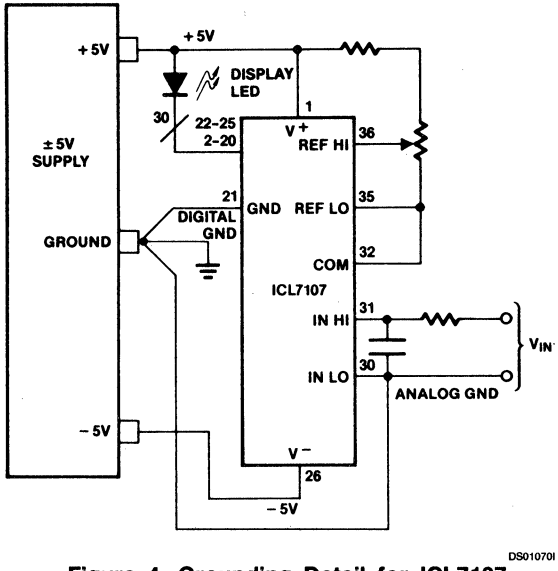


Figure 4: Grounding Detail for ICL7107

Temperature

Q: What variation in reading can be expected with the ICL7106 or ICL7107 when used over the temperature range of 0°C to +70°C?

A: To determine temperature stability of the circuit, analyze each of the three sources of drift.

1. Offset drift is specified to be 1μV/°C maximum. For a 70°C change in temperature, a 70μV change in offset will occur. If the A/D is set for a 200mV full-scale, each count corresponds to 100μV. The change in offset for a 70°C change in temperature will be 70/100 or 0.7 counts maximum. In practice, offset drift is likely to be much less than this.
2. Scale factor is specified to be 5ppm/°C maximum. A 70°C change in temperature corresponds to a change in scale factor of 0.035%. The corresponding change in reading will be 0.035% of 2000 counts, or 0.7 counts maximum. In practice, scale factor drift is likely to be much less than this.
3. The temperature coefficient of the internal voltage reference is specified to be 80ppm/°C typically. A 70°C change in temperature will cause a change in reading of 0.56%. The change in reading from this will be 0.56% of 2000 counts or 11.2 counts typically. This is clearly the major source of error in absolute measurements.

Since using the internal reference of the ICL7106 can result in a change in reading of 11.2 + 0.7 + 0.7 = 12.6 counts over a change in temperature of 70°C, the use of an external reference is recommended.

Using an external reference such as the ICL8069, the change in reading can be kept to 2.8 counts maximum. Such an external reference is recommended for the ICL7107 because of the chip heating caused by power dissipation. This power dissipation is due to the LED drivers, and is not a significant factor when using the ICL7106 over a limited temperature range.

One other effect of increasing temperature on the ICL7106 or ICL7107 is the increase of input leakage currents. This has negligible effect on performance in most applications when recommended component values are used. In more critical applications, increasing the value of C_{REF} and C_{AZ} will minimize these effects.

Components

Q: Can the ICL7126 plug directly into a socket previously occupied by an ICL7106?

A: The ICL7126 and ICL7106 have identical pinout configurations, however some external component values will have to be re-calculated in order to use the ICL7126.

1. The oscillator capacitor (pin 38) should be no more than 50pF, and the oscillator frequency adjusted to 60kHz or less.
2. The current through the reference voltage divider (V^+ to COMMON pin 32) should be limited to 10μA.
3. The integrating capacitor (pin 27) and resistor (pin 28) values should be re-calculated. See component selection question or Component Formulae section of this note for further details.
4. The auto-zero capacitor (pin 29) should be 0.33μF for 0.2 Volt full-scale, or 0.033μF for 2 Volt full-scale operation.

Q: What types and values of external passive components should be used with the ICL7106, ICL7107, and ICL7126?

A: The oscillator, integrator, and voltage reference divider resistors may be carbon or metal film resistors with a tolerance of 5%, the oscillator capacitor should be a dipped

mica or ceramic type with 10% tolerance, and the reference and auto-zero capacitors should be either polystyrene or mylar types with 20% tolerance. The integrating capacitor should be polypropylene, with polystyrene and polycarbonate as second and third choices, respectively. The integrating capacitor must have good dielectric absorption characteristics for the A/D converters to have optimum linearity.

The values for these components depend on the type of converter used. See the Component Formulae section of this application note. These formulas will give an approximate value that is best for a given A/D converter. The actual component value should be the closest standard value that is available.

TROUBLESHOOTING GUIDE

When problems occur with the application of Intersil's family of 3½ digit A/D converters, they can usually be divided into three categories. These categories are:

1. Accuracy problems
2. Display problems
3. Functional problems

This portion of this application note will deal with specific problems in these three areas.

Accuracy Problems

1. Problem: Above a certain input voltage level, the displayed reading does not linearly track the input.

Action: Observe the waveform at the output of the integrator stage (pin 27) of the A/D converter. There should be no clipping at the positive and negative peaks of the ramped waveform. The value of R_{INT} or C_{INT} may be too small, or the oscillator frequency may be too low, allowing the integrator to saturate. See previous section on component value selection.

2. Problem: For a constant input voltage, there is a difference in the absolute value of the reading when only the polarity is reversed.

Action: This problem is called "rollover error" and is usually eliminated by proper selection of the integrating capacitor connected to pin 27. A capacitor with good dielectric absorption characteristics is required; polypropylene or polystyrene are the best types of capacitors to use here. Another possible source is that C_{REF} is too small, or that there is excessive stray capacitance to ground from its pins (see A032).

3. Problem: For a constant input level, the displayed reading varies as the positive power supply voltage varies.

Action: The connection to analog COMMON (pin 32) should be checked. If the internal voltage reference is used, analog COMMON should **not** be grounded, but rather should be connected to REF LO (pin 35), as shown in Figure 1.

4. Problem: The displayed reading of the ICL7106 or ICL7107 is not constant for constant input, and changes several counts from one reading to the next.

Action: The connection to analog COMMON should be checked. If an external voltage reference is used, the COMMON pin should have a pull-up resistor of 27kΩ connected between it and the positive power supply, as shown in Figure 2.

5. Problem: With the voltage inputs shorted together, there is an offset reading of several counts.

Action: The size of the reference capacitor is too small, or the type of capacitor is too leaky. Use a mylar capacitor of 1μF in most applications. Only in applications where input and reference voltage are referred to ground as a common point will a 0.1μF capacitor be satisfactory.

6. Problem: The evaluation kit has been carefully assembled and displays an offset error of several counts when inputs are shorted together.

Action: Proper cleaning of the printed circuit board after assembly should eliminate any leakage paths.

Display Problems

7. Problem: The displayed reading of the ICL7107 is not stable and changes every conversion cycle.

Action: The connections to power supply ground and signal grounds must be carefully routed to avoid noise problems. Digital ground (pin 21) carries all the LED return current, and should only be connected to INput LO (pin 30) at the power supply terminals. Figure 4 shows how this grounding should be done to keep the LED current from generating a noisy input voltage.

8. Problem: As power is applied to the ICL7107 with constant input voltage, the reading changes with time and only after a few minutes is stable.

Action: This is caused by the use of the internal reference of the ICL7107 in applications where external LED displays are also being driven. The power dissipated by the LED drivers causes internal chip heating which causes the internal voltage reference to drift. This can be avoided by using an external voltage reference such as the ICL8069, which is considerably more stable than the internal reference of the ICL7107. See Figure 2 for connections.

9. Problem: The LED display driven by the ICL7107 is not bright enough.

Action: The ICL7107 will typically drive 8mA per segment. This current cannot be varied upward, and will be the same regardless of the size and type of display. To increase brightness, the user should either pick the most efficient display available or use external drivers such as 7407 open collector buffers.

10. Problem: The LCD display connected to an ICL7106 is weak and occasionally displays incomplete characters.

Action: Low power supply or battery voltage will cause the LCD display to have low contrast. Temperature extremes below 0°C will also cause problems with LCD displays.

11. Problem: There is permanent distortion or "burning" of the LCD display after prolonged use.

Action: LCD display damage is caused when there is DC drive to a segment or decimal point. Holding the TEST pin (pin 37) high for a long period may also cause display damage.

Functional Problems

12. Problem: When power is applied to the A/D converter it displays 1666 steadily and does not change.

Action: This is an indication that the oscillator is not functioning. Check oscillator components and printed circuit board for leakage paths around pins 38, 39, and 40.

13. Problem: The overrange condition (+ or −1 and blank) is continually shown regardless of input voltage.

Action: Check to see if input voltage between pins 30 and 31 is greater than twice the reference voltage. Also check

to see that the reference voltage (between pins 35 and 36) or C_{REF} is not shorted out in some way.

14. Problem: Excess power supply current is drawn after the TEST pin is pulled high and then low.

Action: Make sure that when the TEST pin is dropped it is allowed to float and not returned to the negative power supply level.

NORMAL WAVEFORMS

Integrator output and buffer amplifier waveforms are shown in Figures 6 and 7 for the two most common configurations of the ICL7106, ICL7107, and ICL7126. Figure 5 shows battery operation with COMMON (pin 32) shorted to INput LO (pin 30). In this case, all voltage measurements are made with respect to COMMON, which is internally set to 2.8 Volts below V^+ terminal (pin 1). During the auto-zero phase of the conversion cycle both INTegrator and BUFFer amplifier outputs are at V_{COM}, the voltage on pin 32. When the integrate portion of the cycle begins, the buffer is switched to the input voltage, V_{IN}, and its output goes to a level equal to $V_{COM} + V_{IN}$. In Figures 6 and 7, the solid line shows the negative input voltage, and the dotted line represents the positive input voltage. During this phase the integrator will ramp in a direction opposite to the input voltage polarity. During the third (de-integrate) phase of the conversion cycle the reference capacitor (pins 33 and 34) is switched between COMMON and the BUFFer amplifier input with the right polarity to make the integrator ramp back to its starting voltage, V_{COM}.

Dual power supply operation is shown in Figure 1 for the ICL7106 and in Figure 4 for the ICL7107, with INput LO connected to ground in both cases. Figure 7 shows the INTegrator and BUFFer amplifier outputs at V_{COM} during the auto-zero part of the conversion cycle, just as in the case of Figures 5 and 6. When the integrate phase starts, the buffer and integrator are switched so that their inputs are referred to ground rather than V_{COM}. The BUFFer OUTput goes to a voltage corresponding to V_{IN}, and the integrator begins ramping from ground in a direction opposite to the input voltage polarity. During the third phase of the cycle, deintegration takes place with respect to V_{COM} and the conversion is complete when the INTegrator output equals V_{COM}.

Figures 8 and 9 show normal clock (OSC 3) and LCD driver waveforms (ICL7106 and ICL7126). Note that in Figures 6 and 7, the buffer and integrator input offset voltages (typically about 20mV) have been neglected. These will move the baselines by the corresponding amount, but will not affect the actual waveforms themselves.

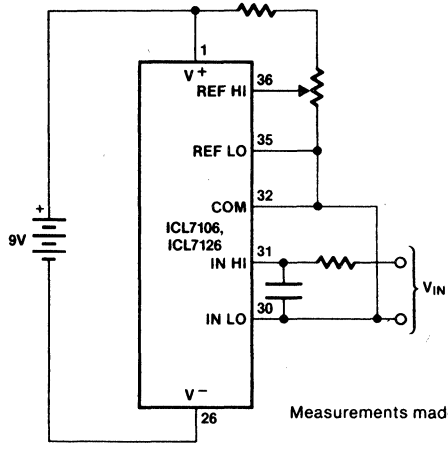


Figure 5: Operation from 9 Volt Battery with Internal Voltage Reference

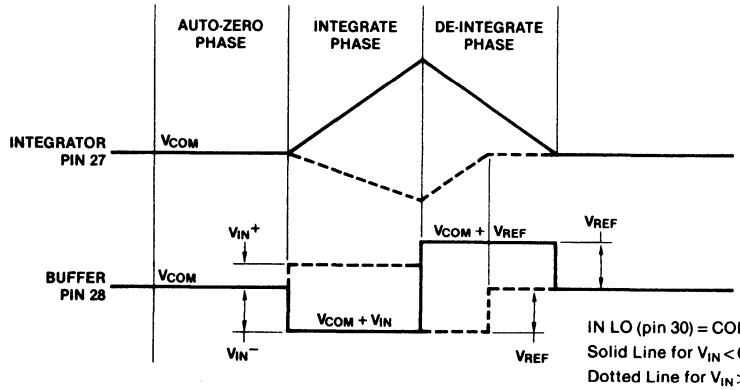


Figure 6: Integrator and Buffer Waveforms for Circuit of Figure 5

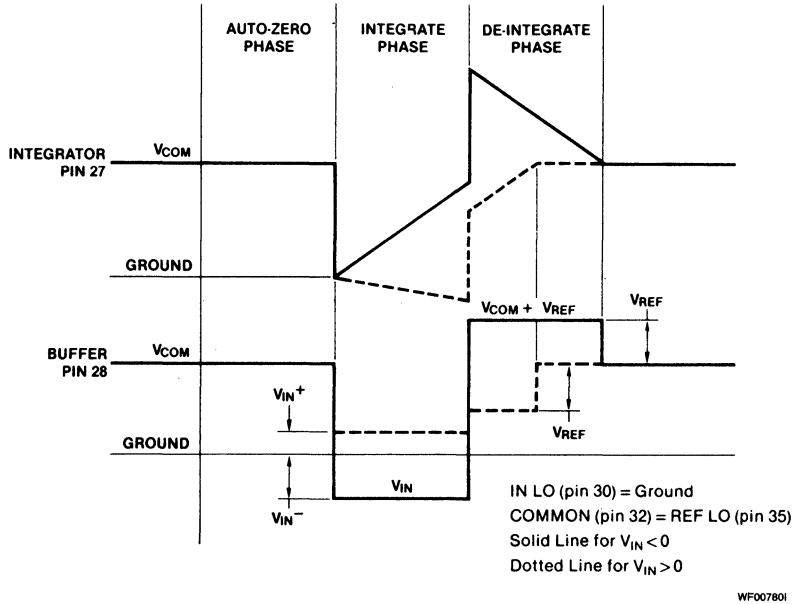


Figure 7: Integrator and Buffer Waveforms for ICL7106, ICL7126 Connected as in Figure 1, or ICL7107 Connected as in Figure 4

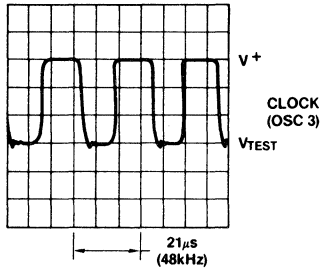


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Figure 8: Clock Waveform on OSC 3 (Pin 38) R = 100kΩ and C = 100pF

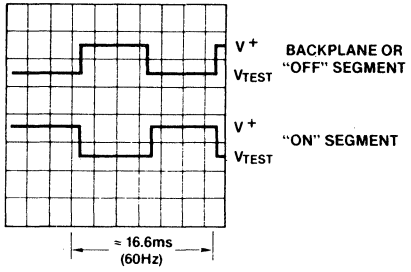

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Figure 9: LCD Drive Waveforms for ICL7106 and ICL7126

COMPONENT FORMULAE

Integrator Resistor and Capacitor (R_{INT}, C_{INT})

$$R_{INT} = \frac{\text{Full-scale input voltage}}{I_{INT}}$$

$$C_{INT} = \frac{4000 \times I_{INT}}{\text{Integrator swing} \times f_{osc}}$$

where I_{INT} is integrator drive current and f_{osc} is oscillator frequency.

For ICL7106, ICL7107 $I_{INT} = 4\mu A$
For ICL7126 $I_{INT} = 1\mu A$

Full-scale input voltage is normally that input voltage that will just read (−)1999 or overrange. However, if a more restrictive input (and reading) range is in use, the larger of this maximum input voltage or the reference voltage may be used instead.

Integrator swing for ICL7106 and ICL7126 battery operation is 2 Volts. Integrator swing for ±5 Volt supply operation 3.5 Volts.

Auto-Zero Cap(C_{AZ})

RANGE	ICL7106 ICL7107	ICL7126
200mV scale	0.47μF	0.33μF
2.0V scale	0.047μF	0.033μF

The value for C_{AZ} should be approximately twice the value for C_{INT}. Increasing C_{AZ} will reduce noise, but slow down recovery from overload or start-up. See A032 for more details.

Oscillator Frequency

$$f_{OSC} = \frac{0.45}{R_{OSC} \times C_{OSC}} \text{ (approximately)}$$

where $R_{OSC} > 50k\Omega$ and $C_{OSC} > 50pF$ for ICL7106, ICL7107 and where C_{OSC}~50pF and $f_{OSC} \leq 60kHz$ for ICL7126.

Note that changing the oscillator frequency may require a change in the value of C_{INT} and C_{AZ}. Also note that the internal clock frequency is equal to one-fourth of the oscillator frequency.

Reference Cap (C_{REF})

Use 1.0μF for high input to reference common-mode voltages or 2.0 Volt full-scale input range.

Use 0.1μF for low input to reference common-mode voltages.

OTHER PRODUCTS

Much of the discussion given here is also relevant to other A/D converters, such as the ICL7109 and ICL7135, which have an analog section almost identical to that of the ICL7106/7 etc., and even to chip pairs such as the ICL8052/ICL71C03 and ICL8052/ICL7104.

OSCILLATOR FREQUENCY (kHz)	CONVERSIONS PER SECOND	FREQUENCY REJECTED (Hz)
240	15	60
200	12.5	50
120	7.5	60
100	6.25	50
80	5	60
66.66	4.16	50
60	3.75	60
50	3.12	50
48	3	60
40	2.5	50 & 60
34.28	2.14	60
33.33	2.08	50
30	1.87	60
25	1.56	50
24	1.5	60
20	1.25	50 & 60

OTHER APPLICATIONS BULLETINS

Some other applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.

A052

A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family", by Peter Bradshaw.

A046 "Building a Battery Operated Auto-Ranging DVM with the ICL7106", by Larry Goff.

A051 "Principals and Applications of the ICL7660 Voltage Converter" by Peter Bradshaw and Dave Bingham.

AO43
Video Analog-to-Digital Conversion

Calls for virtuoso performances. And the plot really thickens when you have to produce high resolution.

Accurately digitizing analog signals containing high frequencies, demands ultrahigh-speed, or video, A/D converters. Such a converter is essential to diverse uses like radar-signature or transient analysis, high-speed digital-data transmission, video densitometry, and digital television. In television alone, a speedy converter can help enhance images, correct time-base errors, convert standards, synchronize or store frames, reduce noise, and record TV.

Most video A/D converters work in the 1-to-20MHz range. But at these speeds, resolution can be a problem. Fortunately, 8 bits and fewer most often suffice in ultrafast A/D applications.

Higher resolutions are hard (and expensive) to come by, particularly at 10 to 20MHz. In this ultrahigh-speed range, 4 bits is about the practical limit for a single-stage converter. However, you can cascade A/D stages for more than 4 bits.

Below 5MHz, you can retain the "one bit at a time" concept of the familiar successive-approximation converter, while reducing the time delays inherent in converting each bit. The "propagation" (or variable-reference-cascade) converter of Figure 1 does just this.

COMPARATORS STAR IN PROPAGATION A/D'S

The critical parts of the circuit are the comparators, which must be very fast, and the switches, which must be not only very fast but also capable of withstanding the reference voltage. A propagation A/D converter uses one comparator per bit. Furthermore, each bit is converted in sequence, beginning with the most significant. With a −5 V reference, the circuit of Figure 1 handles inputs from 0 to +10V.

Comparator A_1 makes its decision at a +5V input: when the analog-input voltage exceeds +5V, the output is true. The threshold of comparator A_2 is set for an input of either +2.5 or +7.5V, depending on the output of comparator A_1. If the analog input voltage exceeds +7.5V, comparator A_2 also goes true. If, however, the analog input voltage is between +5 and +7.5V, the output becomes ZERO; an input between +2.5 and +5V produces a ONE. And for less than 2.5-V input, the output becomes ZERO.

As you can see, then, the output of comparator A_1 sets the threshold of comparator A_2 via electronic switch S_1. S_1 switches one end of the resistive divider at comparator A_2 to ground when the output of comparator A_1 is ZERO, and to the −5V reference when it is ONE. Therefore, the threshold of the second comparator is set for either of two analog-input-voltage levels: +2.5 or +7.5V.

This process continues for comparators A_3 and A_4. Each succeeding threshold is set by the result of all previous comparator decisions. Thus, comparator A_3 has four possible threshold levels, +1.25, +3.75, +6.25, or +8.75V. Similarly, comparator A_4 has eight possible threshold levels (for a summary of each comparator's threshold levels, see Table 1).

Obviously, a propagation-type converter becomes more complex as its resolution increases beyond 4 bits. Higher resolution requires not only more resistors — to set the new threshold levels — but also higher-value resistors. The resistor values go up in a 1, 2, 4, 8, . . . binary sequence. So as the number of bits increases, the resistors soon take on values so large as to affect the conversion time for the less-significant bits. The fault lies with slow settling of the currents switched through the resistors. The time constants, caused by switch plus stray capacitances and the high-value resistors, cause the delays.

Still, you can achieve 50-ns per bit conversions with a propagation-type converter. After a new input is applied to the converter, the resulting digital output word propagates rapidly down the converter-output lines, as each comparator and switch change states. Instead of simply allowing the circuit to propagate naturally, you can also operate it in a clocked mode by using sampling (gated) comparators, rather than the usual ungated kind.

But 5-MHz and higher conversion rates, together with the complexity required for higher than 4-bit resolution, severely limit the video uses of propagation-type analog-to-digital converters.

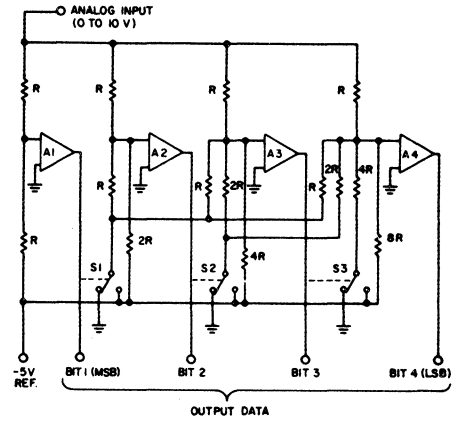

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Figure 1: A propagation-type A/D converter uses one comparator per bit, with each bit converted in sequence. At best, this type of A/D runs at 5MHz for up to four bits.

TABLE 1. COMPARATOR THRESHOLDS FOR A 4-BIT PROPAGATION-TYPE A/D CONVERTER

SCALE	COMPARATOR NUMBER			
	1	2	3	4
FS–1 LSB			+8.750	+9.375
3/4 FS		+7.500		+8.125
1/2 FS	+5.000		+6.250	+6.875
				+5.625
1/4 FS		+2.500	+3.750	+4.375
				+3.125
1 LSB			+1.250	+1.875
				+0.625

QUANTIZER PLAYS THE LEAD

Fortunately, a much faster technique is available. Parallel conversion (also called flash, or simultaneous) is more popular because it is faster than propagation. A parallel-type A/D converter is simply a quantizer circuit followed by a decoder circuit. As a matter of fact these two functions are fundamental to all A/D converters. The difference is that these functions are clearly separate in a parallel A/D.

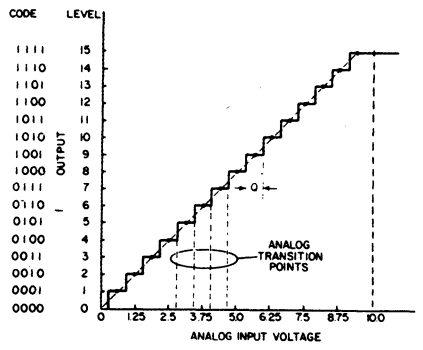

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Figure 2: The quantizer transfer function for a 4-bit parallel-type converter shows how the analog input is broken into 16 different levels. Each word of digitally coded output signals represents a range, Q, of input voltage.

The quantizer section of a parallel converter is defined by its transfer function, which is shown for a 4-bit quantizer, in Figure 2. The quantizer breaks up the continuous-analog input (horizontal axis) into discrete-output levels (vertical axis).

In Figure 2, the output is divided into 16 different states, or 2^n levels, where n is the number of bits. Along the horizontal axis of the transfer function are 2^n-1 or 15 analog-transition points which represent the voltage levels that define the edges between adjacent output states or codes.

There is no one-to-one correspondence between input and output for the quantizer, which assigns one output code word to a small range, or band, of analog-input values. The size of this band is the quantum, Q, and is equal to the full-scale-analog range divided by the number of output states:

$$Q = \frac{FSR}{2^n}$$

In Figure 2, where the full-scale-input range is 10V,

$$Q = \frac{10}{2^4}$$

$$= \frac{10}{16}$$

$$= 0.625V.$$

TABLE 2. PARALLEL 3-BIT A/D CODING

SCALE (FRACTION OF FULL SCALE)	7-LINE EQUALLY WEIGHTED CODE WITH OVERRANGE	BINARY CODE
+9/8	11111111	1000
	01111111	0111
+3/4	00111111	0110
	00011111	0101
+1/2	00001111	0100
	00000111	0011
+1/4	00000011	0010
	00000001	0001
0	00000000	0000

Figure 2 shows levels of 0 through 15 at the output. When binary-code words are assigned to these output states, as shown in the leftmost column, the transfer function becomes that of a complete A/D converter rather than just a quantizer alone.

The binary codes are assigned by a circuit that decodes the quantizer-output logic. Though you can select any code, the code shown, natural binary, is most used. Notice that the analog center of each code word — the exact analog value — is depicted by a dot on the transfer-function graph.

The transfer function in Figure 2 depicts an ideal quantizer or A/D converter. A real device, of course, has errors in offset, scale-factor (gain) and linearity.

Figure 3 shows a circuit implementation of a 3-bit parallel A/D converter. Usually, the quantizer portion of such a circuit consists of a bank of 2^n-1 high-speed comparators. But, in Figure 3, 2^n or 8, comparators are used, because this circuit also provides an overrange output that can be used for expansion.

The bank of comparators has 2^n analog-transition points. These are directly set by biasing one side of the comparator

inputs from a reference with a series string of equal-value resistors, R. The Q for this circuit depends on the value of R, the reference voltage, and the total resistance:

$$Q = \frac{(V_{REF}R)}{R_{TOTAL.}}$$

The bottom and top resistors in the string have values of R/2, which correspond to the values of the first and last analog-transition points. These transitions are at Q/2 and FS−m(Q/2), respectively.

Without the overrange output, the last analog transition point would be at FS−(3Q/2). The value of the top resistor would then be 3R/2.

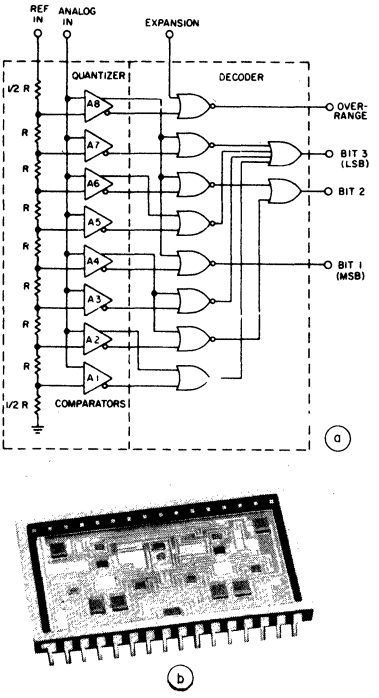

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Figure 3: The circuit for a parallel 3-bit A/D converter (a) has just two basic sections: the quantizer and the decoder. The transition points in the quantizer are set by biasing each comparator, through a resistive divider and reference. The complete 3-bit analog-to-digital converter comes packaged as a thin-film hybrid (b).

ENTER THE DECODER

The parallel converter's decoder section is a rather straightforward logic circuit. It translates the logic outputs from the comparators into the most commonly used code, natural binary.

Table 2 shows the coding for quantizer and decoder outputs. In this quantizer-output code, the seven comparator-output lines (eight, counting the overrange comparator) are equally weighted. This equally weighted code is simple and unambiguous, but inefficient — only one output line changes at a time from all-ZERO to all-ONE outputs. Except for not being cyclical, the quantizer code is like the Johnson code used in shift counters. Like the quantizer code, Johnson code proceeds from all-ZEROs to all-ONEs, but then cycles back to all ZEROs.

In the decoder, simple NOR and OR gates perform the logic according to the following equations:

$$\text{Bit } 1 = A_4$$

$$\text{Bit } 2 = A_6 + A_2 \cdot \overline{A_4}$$

$$\text{Bit } 3 = A_7 + (A_5 \cdot \overline{A_6}) + (A_3 \cdot \overline{A_4}) + (A_1 \cdot \overline{A_2}),$$

where the A_n's are the numbered-comparator outputs in Figure 3, Bit 1 is the MSB and Bit 3 is the LSB. The AND function in the equations is replaced by a NOR in the actual circuit. The OR function can be implemented by tying together the appropriate outputs of wire-ORed ECL logic.

With ultrafast analog comparators, parallel conversion offers the ultimate conversion speed. Since the comparators all change state simultaneously, the quantizer output is available after just one propagation time. Of course, the decoder adds more delay, but high-speed Schottky-TTL or ECL circuits can minimize the decoding time.

In 3-bit form with an additional comparator, for overrange, the parallel converter in Figure 3 can be expanded for higher resolution. You can connect two converters, combine into one flash converter to get often-needed 4-bit resolution. Likewise you can connect four such circuits for 5-bit resolution — and so forth. In this way, these circuits can be used as "building blocks" for ultrafast A/D converters. Conversion rates of 50MHz, for 3, 4, or 5-bit A/D's, are possible using the commercial hybrid version of these expandable parallel converters.

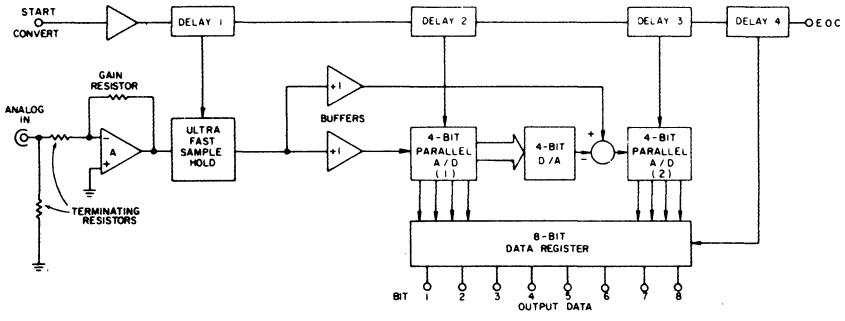


Figure 4: Two-stage parallel A/D converters can develop 8-bit resolutions at 20MHz. Though conversion 1 begins at the Start-Convert pulse and ends 65 nanoseconds later, subsequent conversions take only 50 nanoseconds.

COMPARATOR PLAYS A COMPLEX ROLE

The most critical component in a parallel A/D converter — as in a propagation converter — is the comparator. It not only determines the speed of the converter but also the accuracy. Ultrafast sampling comparators like the 685, 686 and the dual 687 are excellent for this function.

A sampling comparator has two Latch-Enable inputs that switch it into either a Compare or Latched mode. In the latter, the comparator's digital output is locked until the next comparison is made.

Whether or not you use a sampling comparator, you must consider the propagation delay for small overdrive. This is important because the analog full-scale-signal range is generally small for ultrafast A/D converters — commonly between 1 and 4V. The comparator must change state rapidly for a Q/2 analog-input change. For a 4-bit converter with a 1-V input range, this represents an overdrive of 31mV; for an 8-bit converter with the same input range, the over-drive is just 2mV.

The analog-input characteristics of a comparator are important because they affect conversion accuracy. Input-offset voltage and input-bias current are usually the most significant of these parameters. The offset voltage directly affects the accuracy of the quantizer's analog-transition points; the input-bias current also affects the accuracy through the effective input resistance of the comparator.

Since an ultrafast comparator generally has bias currents as high as 10μA, its inputs must look into low resistances. Fortunately, for small-signal ranges like 1 to 4V, each resistance in the series network can be kept low. In an actual 3-bit parallel hybrid converter, laser-trimmed, thin-film-resistor networks make the transition points stable and accurate.

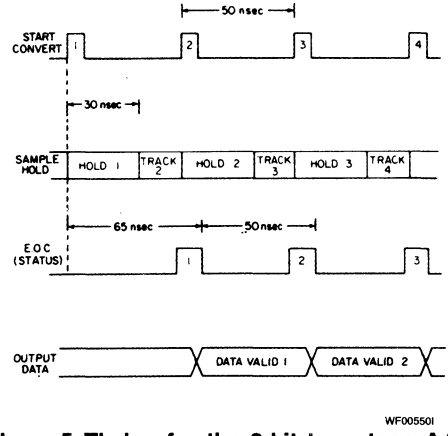


Figure 5: Timing for the 8-bit two-stage A/D converter allows for two modes in the sample-and-hold circuit — Hold and Track. These occur between successive Start-Converts. The second and succeeding conversions take 50ns.

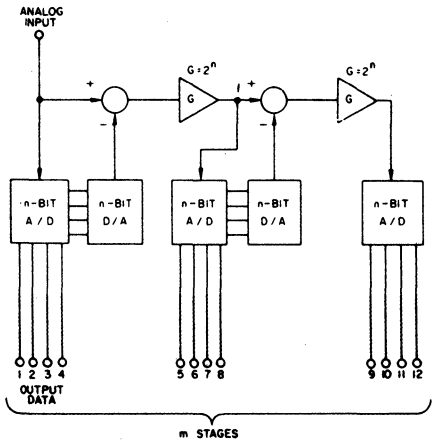


Figure 6: A generalized n-bit, m-stage A/D converter develops an output with n x m bits of resolution. In each stage, except the first, the analog result of the subtraction is amplified by a circuit whose gain is 2^n.

One comparator parameter that greatly affects speed is input capacitance. For example, the analog-input line to a 4-bit A/D with overrange feeds 15 parallel-comparator inputs. It must be driven from a low-impedance source to retain high speed. Therefore, either a high-speed input-buffer amplifier or a sample-and-hold circuit drives the input.

Parallel A/D conversion suffers from one significant drawback; more resolution than four bits requires many comparators. The number (N_C) increases exponentially with n, the number of bits:

$$N_C = 2^n - 1$$

An 8-bit converter, for example, requires 255 comparators. That many comparators vastly complicates bias-current and input-capacitance problems — to say nothing of the high power dissipation they produce. Another problem, of course, is how to position so many comparators while minimizing lead lengths.

COMING ONSTAGE — THE TWO-STAGE A/D

As a result, the practical limit of parallel A/D converters is usually 4 bits. Higher-resolution designs use a two-stage parallel technique that is really a combination of the parallel and propagation techniques. It cascades two 4-bit conversions.

This two-stage method is illustrated in Figure 4, which shows the block diagram of a complete 8-bit, 20-MHz converter, including buffer amplifiers and a sample-and-hold. Starting at the input, amplifier A terminates the analog input with the proper impedance and scales the signal for the sample-and-hold circuit. During its conversion to digital form, the ultrafast sample-and-hold acquires and holds the analog-input.

The sample-and-hold output goes into two unity-gain buffer amplifiers, one of which buffers the input to parallel 4-bit A/D converter 1. This A/D converts the input level, then stores the digital result in half of the output-data register. In addition, 15 undecoded comparator-output lines drive a 15-line, equally-weighted digital-to-analog converter. This D/A, in turn, generates an analog voltage that is subtracted from the other buffered-input signal.

The subtraction result, a residual signal, goes to the input of the second parallel 4-bit A/D, the output of which goes to the other half of the output-data register. The input signal is therefore sampled and converted to digital form in two 4-bit steps.

Four digital delays time the converter as shown in Figure 5. A pulse at the Start-Convert input begins the timing sequence. The Start-Convert pulse puts the sample-and-hold into the Hold mode for 30ns. During this time, the first 4-bit conversion is made and the second 4-bit converter quantizes the residual signal. While the second A/D conversion is decoded and transferred to the data register, the sample-and-hold goes into the Track mode to acquire the next value.

When the conversion is done and the 8-bit word is ready in the output register, the delay circuit generates and End of Conversion (or Status) pulse. In the timing diagram, numbers 1, 2, 3 and 4 indicate the relationship of the signals for the first, second, third and fourth conversions. The delay from the leading edge of the Start-Convert pulse to the falling edge of the Status pulse is 65ns — the delay for the first conversion. After the first conversion, new output data arrive every 50ns — a rate of 20MHz.

A two-stage parallel A/D converter is practically the only device used for ultrafast conversion at 8-bit resolution. Moreover, just about all new 8-bit converters have built-in sample-and-holds to shorten the effective aperture time of the conversion from the 50ns of the converter in Figure 4, to a fraction of an ns.

While the 8-bit A/D in Figure 4 is functionally simple, it's actually difficult to develop. In fact, it usually takes longer to develop than today's other types of A/D's. More engineering time can go into just determining circuit and ground-plane layout than into any other part of the development.

BEHIND THE SCENES — A HYBRID

At least one commercial 8-bit converter uses thin-film hybrid components as building blocks, which organize the critical-circuit functions into miniature packages. For example, each 4-bit A/D shown in Figure 4 can be implemented with two hybrid 3-bit expandable decoded A/D's. Also, the 15-line D/A converter, the sample-and-hold and the input-buffer amplifier can be readily hybridized. The remaining noncritical circuit elements can be made from standard monolithic devices and passive components.

The hybrid circuits' stable thin-film resistors can be laser-trimmed for optimum linearity. The entire circuit of Figure 4 fits on a single circuit card, so laying out critical components is less formidable.

Propagation and parallel two-stage are specific examples of a more general conversion method by which m stages of n bits each, make an A/D converter with m x n bits of

resolution (see Figure 6). In each case, the residual analog signal from the subtraction is boosted for the next stage by an amplifier with gain of 2^n. This technique can produce a 12-bit A/D converter using three parallel 4-bit A/D stages.

SLOWER A/D CONVERTERS ARE ALIVE AND WELL

The two most popular techniques for A/D conversion are dual-slope (a) and successive-approximation (b). Together these methods probably account for over 98% of all analog-to-digital converters in use.

Dual-slope conversion, an indirect method, converts the analog-input voltage into a time period. Then a digital clock and counter measure the interval. For only serial-output data, a simple gate replaces the counter. The method is simple, accurate, and inexpensive, but suffers one major drawback: Conversion is usually slow — often taking milliseconds.

Successive approximation A/D converters, on the other hand, can be much faster. They can convert to 12 bits in 2 to 50μs and to 8 bits in 400ns to 20μs. Also, every conversion is completed in a fixed number (n) of clock periods, where n is the resolution in bits.

Successive-approximation, a direct method, puts a D/A converter inside a feedback loop containing both analog and digital elements. The successive-approximation register controls the D/A converter, and the comparator and clock, in turn, control the register.

A conversion consists of turning on, in sequence, each bit of the D/A converter, starting with the most significant. During each clock period, the analog input and the D/A output are compared. The comparison determines whether to leave each bit on or turn it off.

So, after n clock periods, each bit has been turned on, a comparison has been made, each bit's logic state has been decided and the conversion is complete. Clock periods usually last from just fractions of a microsecond to several μs. Each clock period must allow time for comparator switching, changing successive-approximation-register states and D/A converter switching plus settling. Settling time for the D/A converter takes a large part of the clock period because the output must settle to within half the least-significant bit before the comparison starts.

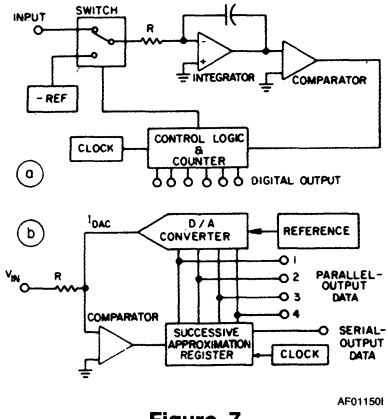


Figure 7

A045
QUAD Current Switches For D/A Conversion

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 1. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see Figure 2. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

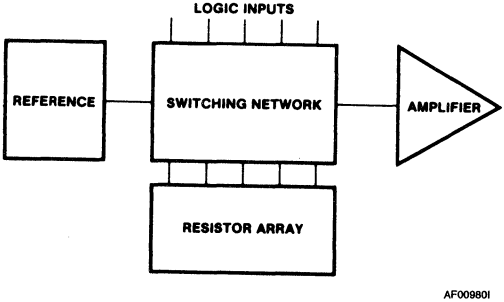


Figure 1: Elements of a D/A Converter

LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Figure 2: Truth Table

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Truth Table) each output corresponding to a particular logic input word.

Note that **maximum output** of the quad switch is $1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} = 1 - \frac{7}{8} = 1.875$ mA. If this series of bits were continued as $\frac{1}{16} + \frac{1}{32} + \frac{1}{64} \ldots\ldots \frac{1}{2n-1}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be $\frac{4095}{4096} \times 10V$. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output**.

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within $\pm \frac{1}{2}$ LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within $\pm \frac{1}{2}$ LSB of an N bit converter. Since the 8018A family has been designed with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the

settling time can be calculated and related to the measured rise time as shown in Figure 3.

Bits of Resolution	±1/2 LSB Error % Full Scale	Number of Time Constants	Number of Rise Time
8	.2 %	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2
Rise Time (10%-90%) = 2.2 $R_L C_{eff}$			

Figure 3: Setting Time vs. Rise Time Resistor Load

CIRCUIT OPERATION

An example of a practical circuit for the quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage and low input bias current is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80k resistor in the emitter of Q_6. Since this resistor is connected to −15V, this puts the emitter of Q_6 at nearly −5V and the common base line at one V_{BE} more positive at −4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to −15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40k in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20k and 10k in the emitters of Q_9 and Q_{10} contribute 0.5mA and 1mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, expansion to 8 and 12 bit is easily achieved with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16\ (1 + 1/2 + 1/4 + 1/8) + 1/256(1 + 1/2 + 1/4 + 1/8) = 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80k resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

2

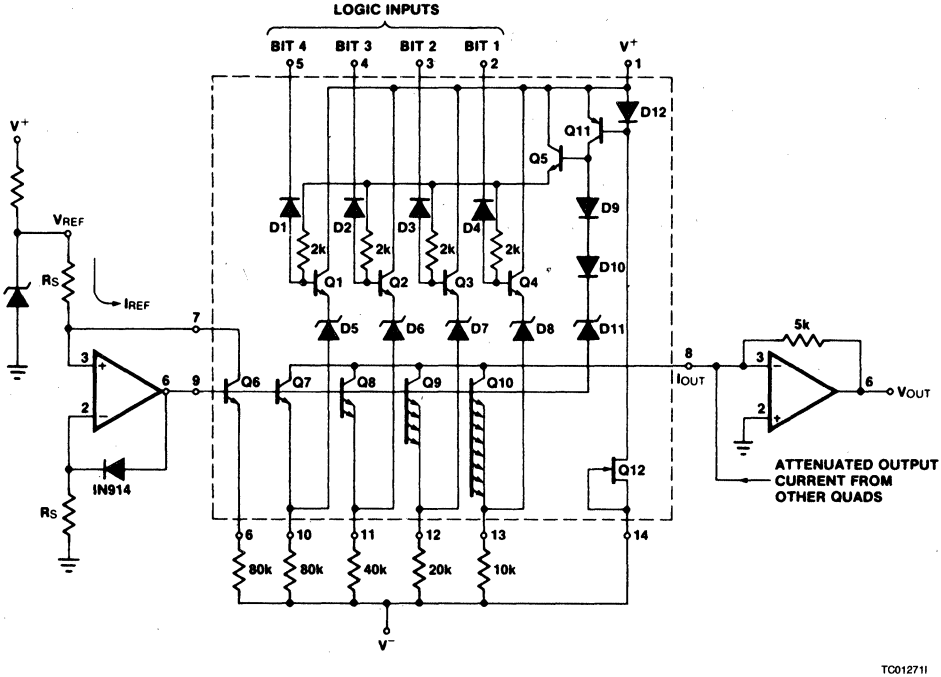


Figure 4: Typical Circuit

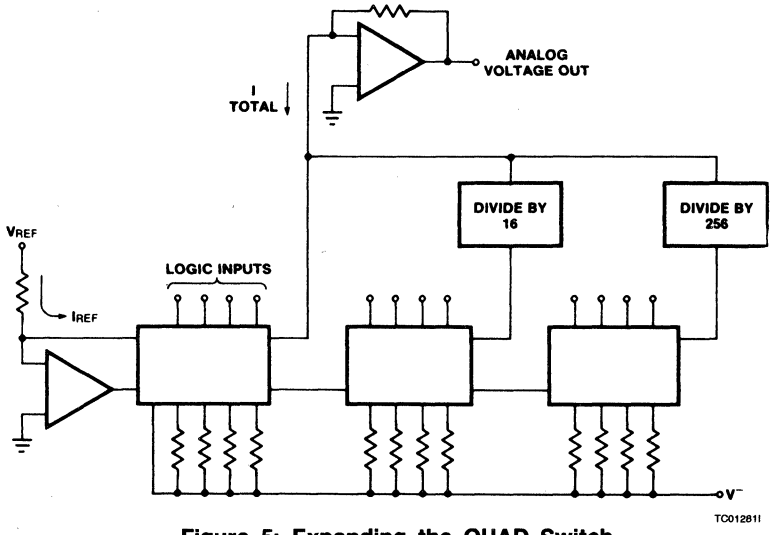


Figure 5: Expanding the QUAD Switch

GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the switch currents are determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

The zener current will be typically 1mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

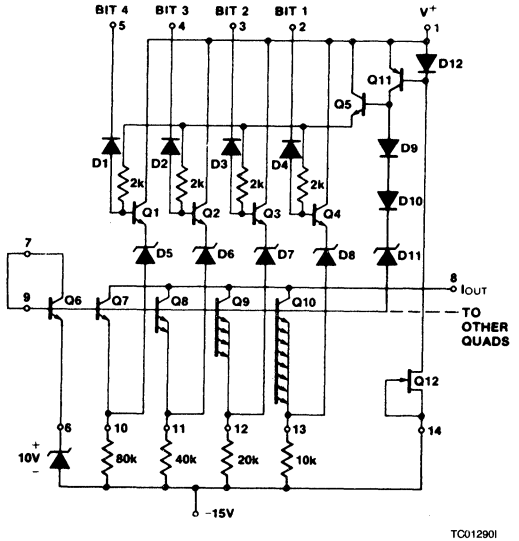


Figure 6: Simple Zener Reference

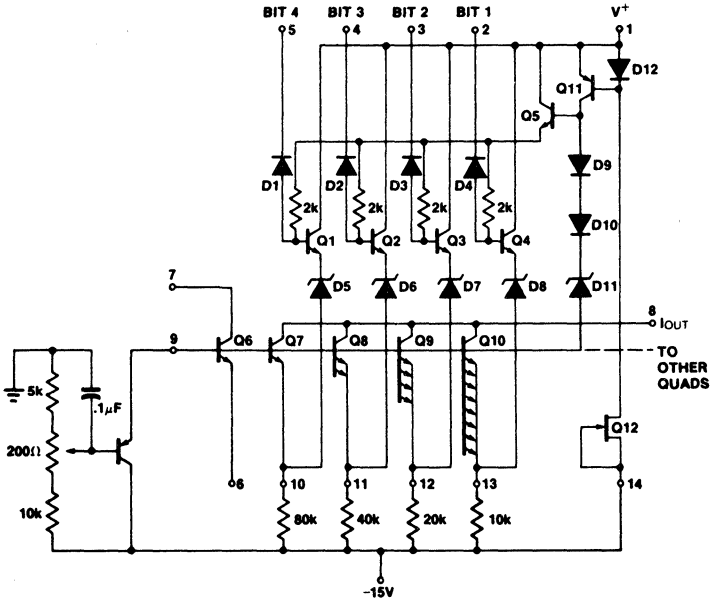
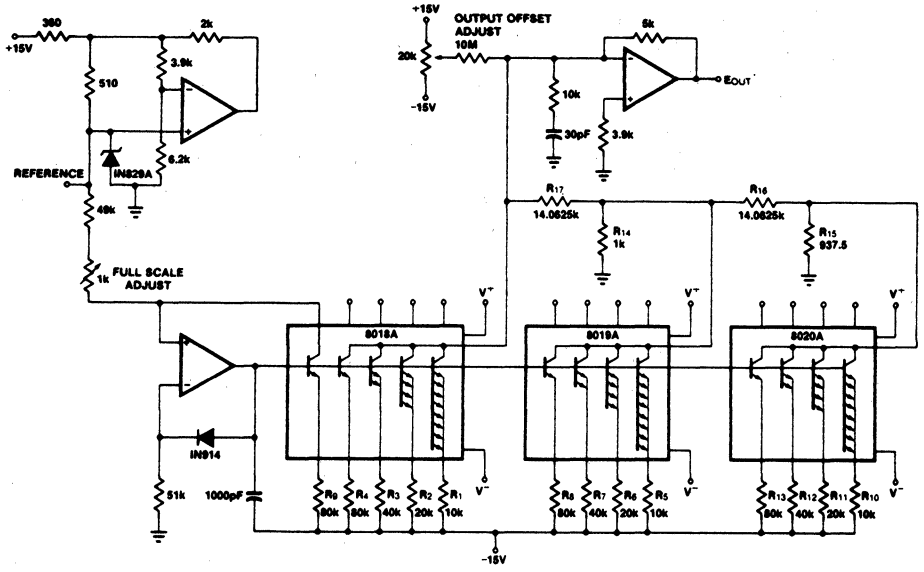


Figure 7: PNP Reference



TOLERANCE TABLE					
R_1	10k	0.1% ABS	R_{10}	10k	0.5% ABS
R_2	20k	0.0122%	R_{11}	20k	Ratio to $_{10}$ 1%
R_3	40k	0.0244%	R_{12}	40k	Ratio to $_{10}$ 1%
R_4	80k	0.0488%	R_{13}	80k	Ratio to $_{10}$ 1%
R_5	10k	0.096%	R_{14}	1k	1% ABS
R_6	20k	0.196%	R_{15}	937.5Ω	1% ABS
R_7	40k	0.391%	R_{16}	14.0625k	RATIO to R_{15} 1%
R_8	80k	0.781%	R_{17}	14.0265k	RATIO to R_{14} 0.1%
R_9	80k	0.1%			

NOTE: All resistors ratio to R_1 unless otherwise noted.

Figure 8

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a 0.01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than 0.01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

PRACTICAL D/A CONVERTERS

The complete circuit for a high performance 12 bit D/A converter is shown in Figure 8. This circuit uses the "full compensation reference" described above to set the base line drive at the proper level, the temperature compensated zener is stabilized using an op-amp as a regulated supply, and the circuit provides a very stable, precise voltage reference for the D/A converter. The 16:1 and 256:1 resistor divider values are shown for a straight binary system; for a binary coded decimal system the dividers would be 10:1 and 100:1 (BCD is frequently encountered in building programmable voltage sources).

The analog output current of the current switches is converted to an output voltage using an op-amp as shown. The output amplifier must have low input bias current (small compared with the LSB current), low offset voltage and offset voltage drift, high slew rate and fast settling time. The input compensation shown helps improve pulse response by providing a finite impedance at high frequencies for a point that is virtual ground at DC.

An alternative bias scheme is shown in Figure 9. In this case, the bias at the common base line is fixed by inverting op-amp A_4, the gain of which is adjusted to give −5.0 volts at the emitter of the reference transistor. With the bias at the common base line fixed, the regular circuit of A_1 uses the internal reference transistor and drives the bus connecting all the precision resistors. This isolates the precision resistors from V^- fluctuations. Zener D_3 and constant current source Q_1 keep the regulation op-amp in mid-range. There are several alternative bias schemes depending on power supplies available. If −20 volts is used for V^-, the bottom of the precision resistor will be at −15 and operation will be the same as the standard circuit. If only −15V is available for V^- the gain of the output transconductance amplifier can be increased by 30% to allow use of a smaller switching currents with 7 volts across the precision resistors.

MULTIPLYING DAC

The circuit of Figure 9 is also convenient to use as a one quadrant multiplying D/A converter. In a multiplying DAC, the analog output is proportional to the product of a digital number and an analog signal. The digital number drives the logic inputs, while the analog signal replaces the constant reference voltage, and produces a current to set up the regulating op-amp. To vary the magnitude of currents being switched, the voltage across all the 10k, 20k, 40k and 80k resistors must be modulated according to the analog input.

CALIBRATING THE 12 BIT D/A CONVERTER

1. With all logic inputs high (ones) adjust the output amplifier offset for zero volts out.
2. Put in the word 0000 1111 1111 (Quad 1 maximum output Quad 2 and 3 off) and adjust full scale pot for V_O of 15/16 (10V) where full scale output is to be 10 volts.
3. Put in the word 1111 0000 1111 and trim the Quad 2 divider for V_O of 15/256 (10V). This adjustment compensates for V_{BE} mismatches between quads.
4. Put in the word 1111 1111 0000 and trim the Quad 3 divider for V_O of 15/4096 (10V).
5. Finally, with all bits ON (all 0's) readjust the full scale factor pot for

$$V_O = 4095/4096 \text{ (10V)}$$

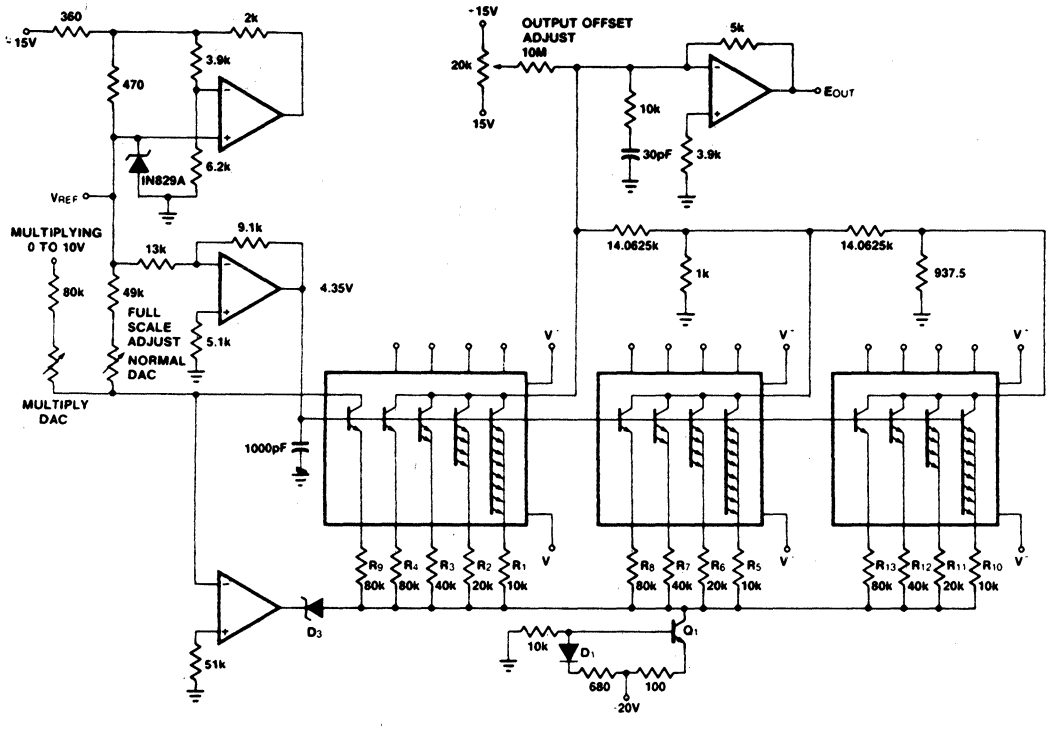

360
-15V
2k
3.9k
470
6.2k
IN829A
VREF
MULTIPLYING
0 TO 10V
80k
49k
FULL
SCALE
ADJUST
NORMAL
DAC
MULTIPLY
DAC
9.1k
13k
5.1k
4.35V
1000pF
51k
D3
-15V
OUTPUT OFFSET
ADJUST
10M
20k
15V
5k
10k
30pF
3.9k
EOUT
14.0625k
1k
14.0625k
937.5
V-
R9 80k
R4 80k
R3 40k
R2 20k
R1 10k
R8 80k
R7 40k
R6 20k
R5 10k
R13 80k
R12 40k
R11 20k
R10 10k
10k
D1
Q1
680
100
-20V
TC013211

Figure 9

AO46
Building a Battery Operated Auto Ranging DVM with the ICL7106

INTRODUCTION

In the field of DVM design, three areas are being addressed with vigor: size, power dissipation, and novelty. The handheld portable multimeter has gained in popularity since low power dissipation devices enabled battery operation, LSI A/D converters reduced IC count, and novelties such as conductance, automatic range scaling, and calculating were included to entice the user.

This application note describes a technique for auto-ranging a battery operated DVM suitable for panel meter applications. Also, circuit ideas will be presented for conductance and resistance measurement, 9 volt battery and 5 volt supply operations, and current measurement.

SECTION 1: AUTO RANGING CIRCUITRY

The control signals necessary for auto-ranging are over-range, under-range, and clock. The over-range and under-range inputs control the direction of a scale shift, becoming active at the completion of an invalid conversion and remaining active until a valid conversion occurs. The clock input controls the timing of a scale shift. This signal should occur only once per conversion cycle, during a time window which will not upset an ongoing conversion and must be disabled after valid conversions.

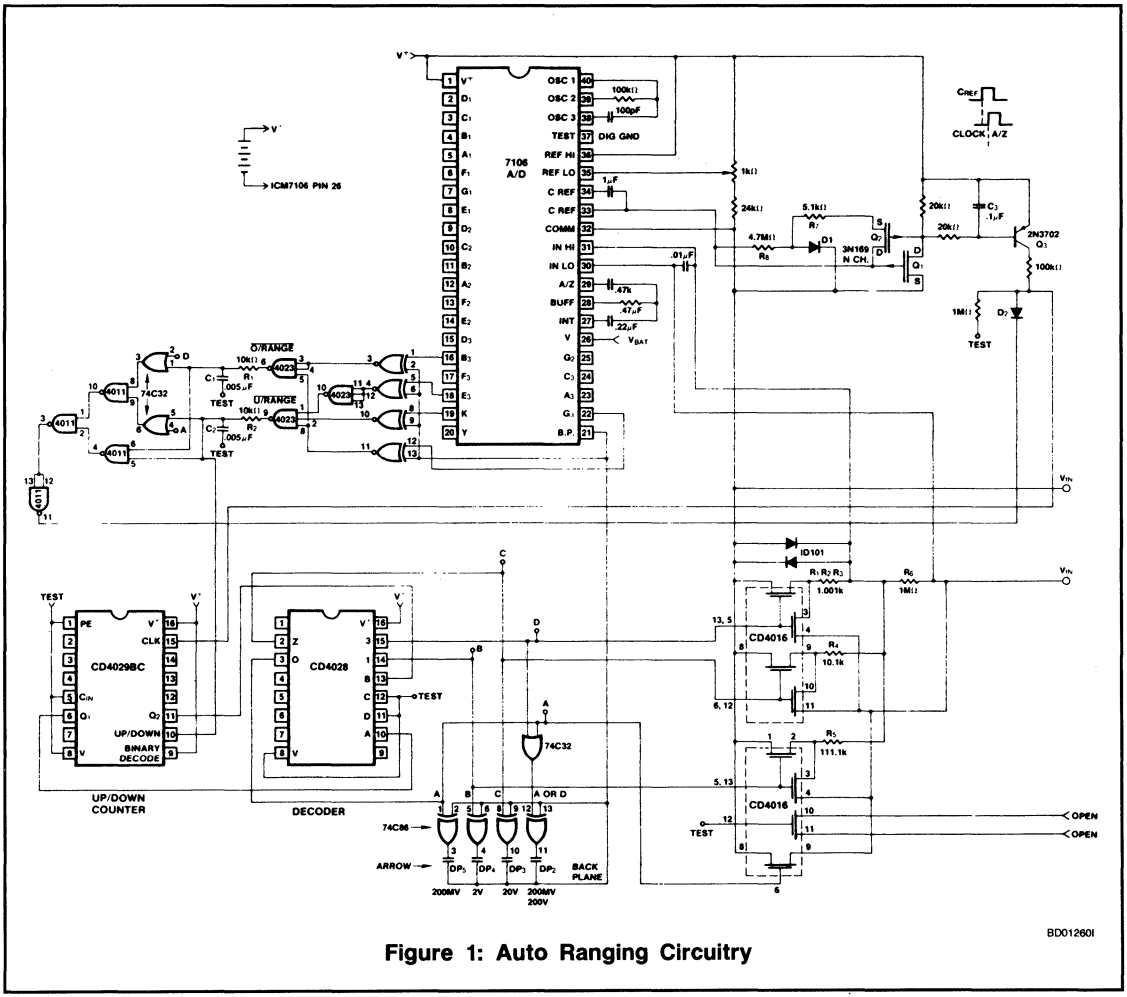


Figure 1: Auto Ranging Circuitry

In the circuit of Figure 1, inverted over-range ($\overline{O/R}$) and under-range ($\overline{U/R}$) are generated by detecting the display reading. The 7106 turns the most significant digit on and blanks the rest to indicate an over-range. An under-range occurs if the display reads less than 0100. R_1C_1 and R_2C_2 are required to deglitch $\overline{O/R}$ and $\overline{U/R}$.

The next step in the logic disables $\overline{O/R}$ and $\overline{U/R}$ prior to shifting into non-existent ranges. $\overline{O/R}$ is disabled when in the 200 volt range, while $\overline{U/R}$ is disabled when in the 200mV range.

The next level of gating disables the clock if the conditions are as described above and a valid conversion state exists. Clock is enabled only when a range shift is called for and there exists a valid range to shift into.

The 4029 is a four bit up/down counter, used as a register to hold the present state and as a counter to shift the scale as directed by the control inputs. The 4028 is a BCD to decimal decoder interfacing the 4029 and ladder switches. An additional exclusive OR gate package is added to drive the appropriate decimal point.

SECTION 2: INPUT DIVIDER NETWORK

A simplified drawing of the divider network is shown in Figure 2. This configuration was chosen for simplicity and implementation using analog switches. The low leakage ID101's are used for input protection, and the second set of switches to IN LO reduces the net error due to switch resistance. This can be seen calculating IN HI and IN LO voltages for the two equivalent circuits.

For equivalent circuit A,

$$V_{MEAS} = V_{IN\ HI} = \left(\frac{R_S + R/K}{R_S + R + R/K}\right)V_{IN} \qquad (1)$$

where R_S = switch resistance, R = input resistance (1MΩ), and 1 + K is the desired divider ratio.

Ideally V_{INHI} should be

$$V_{IDEAL} = \left(\frac{R/K}{R/K + R}\right)V_{IN} = \left(\frac{1}{1 + K}\right)V_{IN} \qquad (2)$$

Therefore the percent error is

$$\left[\frac{\text{Ideal} - \text{actual}}{\text{ideal}}\right]100, \qquad (3)$$

$$\text{or } \left(1 - (1 + K)\ \frac{R_S + R/K}{R_S + R/K + R}\right)100 \qquad (4)$$

The worst case error occurs at (1 + K) = 1000. For this example, the error due to a 1kΩ switch resistance is 99.7%.

IN HI for equivalent circuit B is the same as EQ(1) above. However, IN LO for circuit B is

$$\left(\frac{R_S}{R_S + R + R/K}\right)V_{IN}, \qquad (5)$$

and combining EQ(1) and (5)

$$V_{MEAS} = V_{INHI} - V_{INLO} = \left(\frac{R/K}{R_S + R + R/K}\right)V_{IN} \qquad (6)$$

The percent error is equal to

$$\left(1 - (1 + K)\ \frac{R/K}{R + R_S + R/K}\right)100 \qquad (7)$$

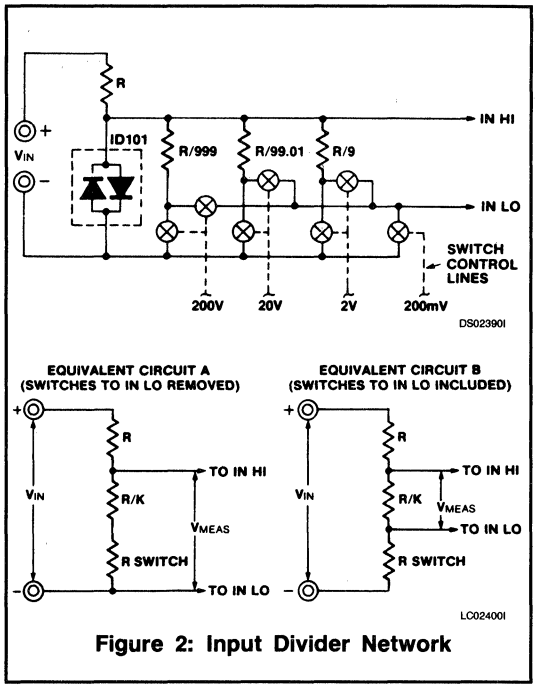


Figure 2: Input Divider Network

Using the same values for R_S, (1 + K), and R, the worst case error is 0.1%. This error can be further improved if lower $r_{DS(on)}$ switches are used. From the results calculated above, the worst case conversion error due to switch resistance will be one count of the least significant digit for a full scale input, and a slight adjustment to R itself will correct the remaining error on all scales.

SECTION 3: RANGING CLOCK CIRCUIT

Two N-channel MOSFET's, a PNP transistor and a handful of passive components combine to generate the clock signal used to gate the auto-ranging logic. A closer look a the inner workings of the ICL7106 will help clarify the discussion of this circuit. The analog section of the ICL7106 is shown in Figure 3.

It can be shown that C_{REF} low (pin 33 of ICL7106) will sit at $-V_{REF}$ for DE+ and at common for DE−, with DE+ designating the deintegrate phase for a positive input signal and DE− referring to a negative input signal. During the auto-zero phase, C_{REF} low is tied to an external reference through pin 35, which in Figure 1 is V_{REF} below the positive supply. The net result is that C_{REF} low is above COMMON during auto-zero, is left to float during signal integrate, and is at or below COMMON during deintegrate. R_8 and D_1 are added externally to pull C_{REF} to COMMON during integrate, with Q_2 and R_1 included to speed this action. The signal at C_{REF} low is now a square wave that is high during auto-zero and low at all other times. Q_1 and Q_3 amplify and level shift this waveform for logic level compatability. This clock signal is gated through D_2 and controls the timing of the auto-ranging circuitry. C_3 is added to delay the clock, eliminating disparity with $\overline{O/R}$ and $\overline{U/R}$ (see Figure 4 for timing diagram).

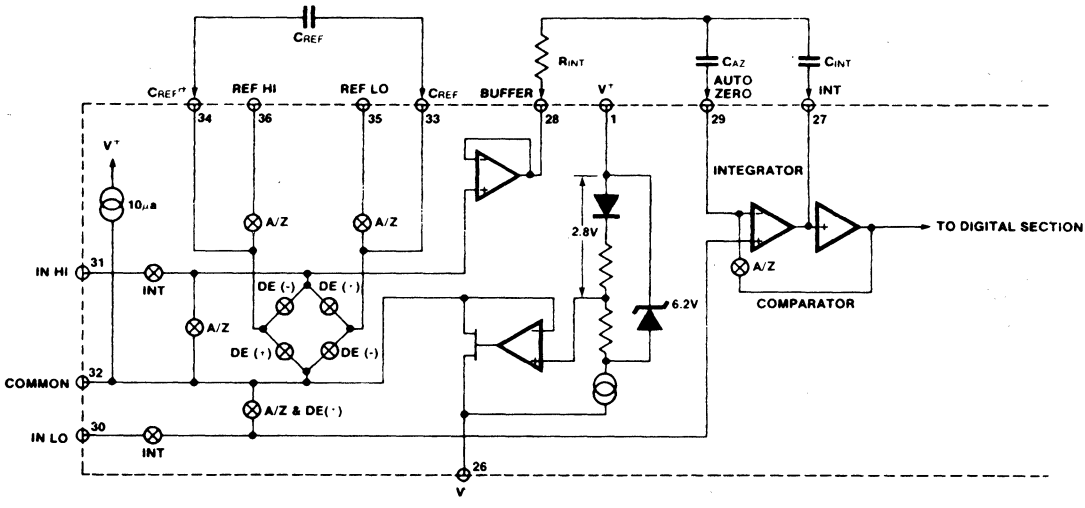


Figure 3: Analog Section of ICL7106

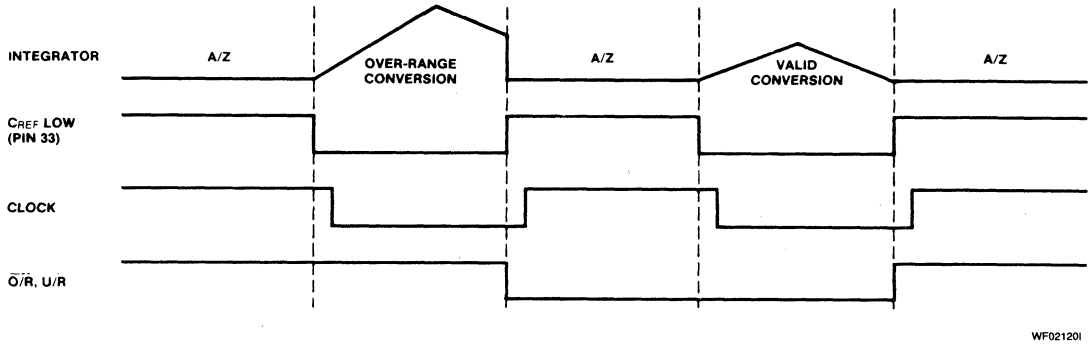


Figure 4: Timing Diagram

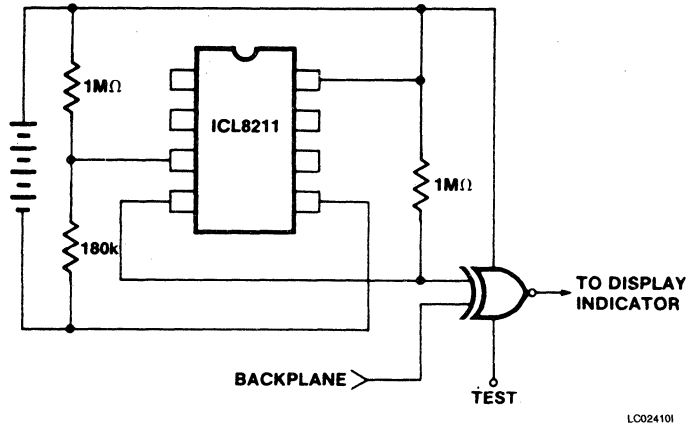


Figure 5: Low Voltage Detector

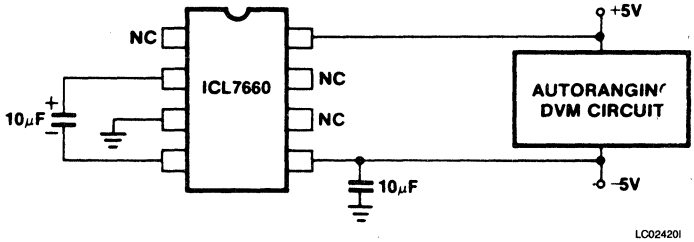


Figure 6: Generating ±5 Volts from +5 Volts

SECTION 4: SUPPLY REQUIREMENTS

The circuit of Figure 1 operates on a standard 9V transistor battery. CMOS logic and a CMOS A/D converter (ICL7106) are used to extend battery life; the approximate power drain for this circuit is 8mW. The circuit of Figure 5 can also be added to detect low supply voltage.

The circuit of Figure 6 can be used to generate ±5 volts from a single 5 volt supply. The ICL7660 is a voltage converter which takes a 5 volt input and produces a −5 volt output. With respect to common mode signals, the circuit of Figure 1 will have infinite common mode handling capability if operated from a floating nine volt battery. However if powered by a fixed supply such as in Figure 6, the common mode capability of the converter will be limited to approximately ±2 volts, if COMMON is disconnected from $-V_{IN}$.

SECTION 5: RESISTANCE, TRANSCONDUCTANCE AND CURRENT CIRCUITS

The purpose of this section is to show the simplicity of measuring transconductance (1/R) and resistance with the ICL7106. The circuit of Figure 7 requires only one precision resistor per decade range of interest. The conversion output is described by the formula

$$\left(\frac{R_X}{R_{STD}}\right)1000$$

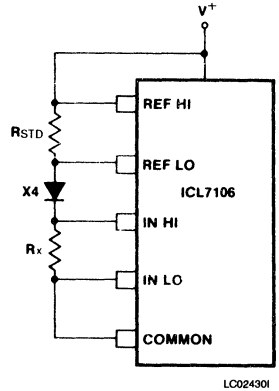


Figure 7: Transconductance and Resistance Measurement

For transconductance measurement, merely switch R_{STD} and R_X. This scheme makes the measurement of large resistors, in conductance form, convenient and easy. This is also convenient for leakage measurements.

A simple current meter can be built using the circuit of Figure 8. The low leakage of the ICL7106 (10pA/max) makes possible the measurement of currents in the mid pico-Amp range. However, the switch leakage current will limit the accuracy of the resistor network and may degrade converter resolution.

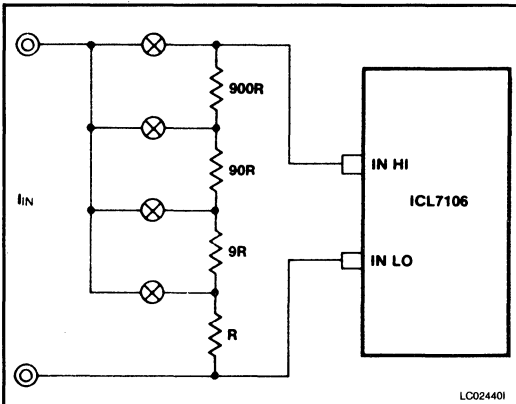


Figure 8: Current Meter

SECTION 6: USING THE ICL7126 AND ICL7107

With a few modifications the circuit of Figure 1 can easily be adapted for use with either the low power 7126 or the 7107. Using the 7126 simply requires a change in the values of the integrating and auto-zero components. Refer to the ICL7126 data sheet for details.

The ICL7107 is an LED version of the ICL7106, and is a bit trickier to use in this application. First the overrange/underrange logic must be changed slightly. Simply replace the quad exclusive-NOR with an LM339; connect the outputs, as before, to the 4023 triple 3-input NAND. Second, the 7107 requires +5V and −5V rather than the +9V battery used in figure 1. If battery operation is desired, the negative supply can be derived from 4 Ni-cad cells in series and an ICL7660. (See figure 9.) Note that both supplies float with respect to the input terminals. (Logic supplies are V^+ and DIG. GND.)

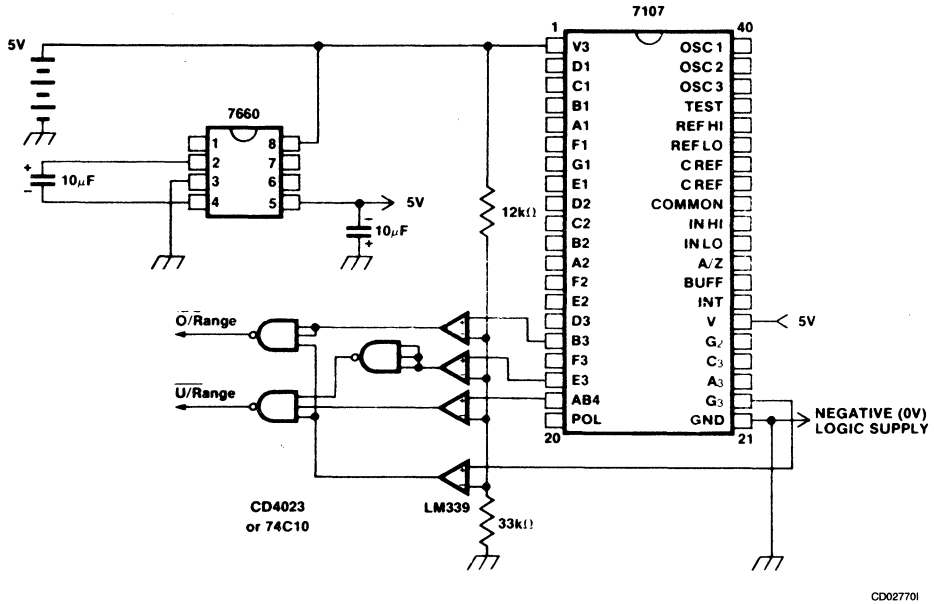


Figure 9: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading

A023
Low Cost Digital Panel Meter Designs

Including Complete Instruction for Intersil's LCD and LED Kits

Intersil's 7106 and 7107 are the first ICs to contain all the active circuitry for a 3½ digit panel meter on a single chip. The 7106 is designed to interface with a liquid crystal display (LCD) while the 7107 is intended for light-emitting diode (LED) displays. In addition to a precision dual slope converter, both circuits contain BCD to seven segment decoders, display drivers, a clock and a reference. To build a high performance panel meter (with auto zero and auto polarity features) it is only necessary to add display, 4 resistors, 4 capacitors, and an input filter if required (Figure 1 and 2).

COST ADVANTAGES OF 7106 AND 7107

Until recently, the make or buy decision for any A-to-D system was dominated by the engineering costs. Even a simple panel meter, built from off-the-shelf digital and linear ICs, required at least six months of engineering effort for completion. However, the advent of truly single chip panel meter functions (Intersil's 7106 and 7107) has reduced the design effort on the part of the user to zero. The make or buy decision becomes a simple question of dollars and cents.

At the time of writing, a 3½ digit LED display panel meter can be built for $18 in production (5,000) quantities. This figure includes labor at $3 per hour with 300% overhead. The cost breakdown is as follows:

ICL7107 (@5000 pcs)	$5.95
LEDs (4)	3.00
Capacitors (5)	.58
Resistors (4)	.12
Potentiometer	.60
Circuit Board	1.00
Misc Hardware	.75
TOTAL COMPONENTS	**$12.00**
Labor (1/2 hour at $3/hour, 300% overhead)	**6.00**
TOTAL COST	**$18.00** including assembly and test

A 3½ digit LCD panel meter, using the 7106, is $3 to $4 more expensive. This is due to the greater cost of the display.

These cost figures are considerably lower than the least expensive of the ready-built panel meters. However, the cost is not the only advantage; the do-it-yourself approach allows greater flexibility. Off-the-shelf panel meters have form factors which are frequently inconvenient, whereas a single IC design takes up a minimum of circuit board real estate. Consider the advantages for field servicing a military radar, for example, if each complex circuit card had its own built-in voltmeter and miniature switch. Fault finding would be greatly simplified by making critical voltages throughout the system instantly accessible.

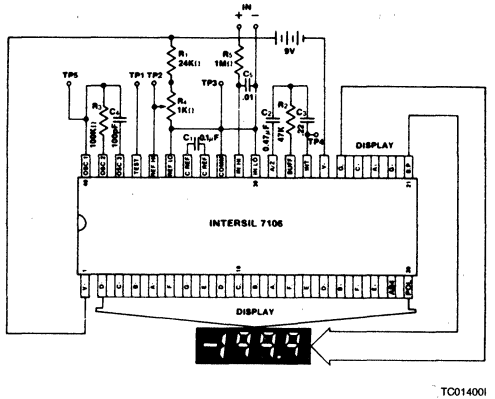


Figure 1: LCD Digital Panel Meter Using ICL7106

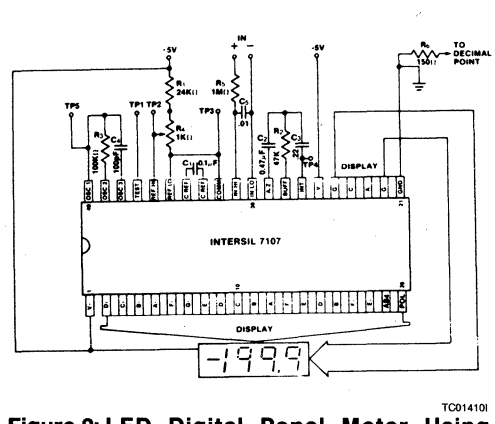


Figure 2: LED Digital Panel Meter Using ICL7107

THE EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½ digit panel meter.

With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

Assembly Instructions

The circuit board layouts and assembly drawings for both kits are given in the Appendices. The boards are single-sided to minimize cost and simplify assembly. Jumpers are used to allow maximum flexibility. For example, provision has been made for connecting an external clock (Test Point #5). Provision has also been made for separating REF Lo from COMMON when using an external reference zener. In a production instrument, the board area could be reduced dramatically. Aside from the display, all the components can easily be placed in less than 4 square inches of board space.

Molex* pins are used to provide a low cost IC socket; one circuit board can thus be used to evaluate several ICs. (Strips of 20 pins should be soldered onto the P.C. boards; the top of the strip holding the pins together can then be broken off by bending it back and forth using needle-nose pliers). Solder terminals are provided for the five test points, and for the ±5V input on the 7107 kit.

Full Scale Reading - 200mV or 2.000V?

The component values supplied with the kit are those specified in the schematics of Figure 1 or Figure 2. They have been optimized for 200.0mV full scale reading. The complete absence of last digit jitter on this range illustrates the exceptional noise performance of the 7106 and 7107. In fact, the noise level (not exceeded 95% of time) is about 15μV, a factor of 10 less than some competitive one chip panel meters.

To modify the sensitivity of 2.000 volts full scale, the integrator time constant and the reference should be changed by substituting the component values given in the Table below. The auto-zero capacitor (C_2) should also be changed. These additional components are not supplied in the kits. In addition, the decimal point jumper should be changed so the display reads 2.000.

Table 1: Component Values for Full Scale Options

COMPONENT (type)	200.0 mV Full Scale	2.000 V Full Scale
C_2 (mylar)	0.47μF	.047μF
R_1	24KΩ	1.5Ω*
R_2	47Ω	470KΩ

*Changing R_1 to 1.5KΩ will reduce the battery life of the 7106 kit. As an alternative, the potentiometer can be changed to 25KΩ.

Liquid Crystal Display (7106)

Liquid crystal displays are generally driven by applying a symmetrical square wave to the back-plan (B.P.). To turn on a segment, a waveform 180° out of phase with B.P. (but of equal amplitude) is applied to that segment. Note that excessive D.C. voltages (> 50mV) will permanently damage the display if applied for more than a few minutes. The 7106 generates the segment drive waveform internally, but the user should generate the decimal point front plane drive by inverting the B.P. (pin 21) output.** In applications where the decimal point remains fixed, a simple MOS inverter can be used (Figure 3). For instruments where the decimal point must be shifted, a quad exclusive OR gate is recommended (Figure 4). Note that in both instances, TEST (pin 37, TP1) is used as V- for the inverters. This pin is capable of sinking about 1mA, and is approximately 5 volts below V+. The B.P. output (pin 21) oscillates between V+ & TEST.

**In some displays, a satisfactory decimal point can be achieved by tying the decimal front plan to COMMON (pin 32). This pin is internally regulated at about 2.8 volts below V+. Prolonged use of this technique, however, may permanently burn-in the decimal, because COMMON is not exactly midway between B.P. high and B.P. low.

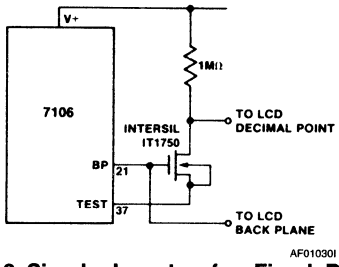


Figure 3: Simple Inverter for Fixed Decimal Point

Before soldering the display onto the circuit board, make sure that it is inserted correctly. Many LCD packages do not have pin #1 marked, but the segments of an unenergized display can be seen by viewing with reflected light. The package orientation should correspond with that shown in Appendix I.

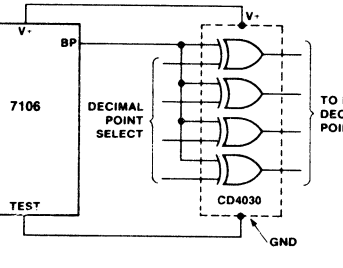


Figure 4: Exclusive 'OR' Gate for Decimal Point Drive

Light Emitting Diode Display (7107)

The 7107 pull-down FETs will sink about 8mA per segment. Using standard common anode 0.3" or 0.43" red LEDs, this drive level produces a bright display suitable for almost any indoor application. However, additional brightness can be achieved through the use of Hewlett Packard high-efficiency LEDs. Note that the display contrast can be increased substantially by using a red filter. Ref. 4 discusses filter techniques and lists manufacturers of suitable materials.

*Molex is a registered trademark of Molex Corporation, Lisle, Illinois 60532.

A fixed decimal point can be turned on by tying the appropriate cathode to ground through a 150Ω resistor. The circuit boards supplied with the kit will accommodate either H.P. 0.3" displays or the popular MAN 3700 types. The difference between the two is that the H.P. has the decimal point cathode on pin 6, whereas the MAN 3700 uses pin 9. Due to the limited space on the circuit board, not all decimal points are brought to jumper pads; it may be necessary to wire directly from the 150Ω resistor to the display. For multiple range instruments, a 7400 series CMOS quad gate or buffer should be used. The majority of them are capable of sinking about 8mA.

Capacitors

The integration capacitor should be a low dielectric-loss type. Long term stability and temperature coefficient are unimportant since the dual slope technique cancels the effect of these variations. Polypropylene capacitors have been found to work well; they have low dielectric loss characteristics and are inexpensive. However, that is not to say that they are the only suitable types. Mylar capacitors are satisfactory for C_1 (reference) and C_2 (auto-zero).

For a more detailed discussion of recommended capacitor types, the reader is referred to page 3 of Reference 2.

The Clock

A simple RC oscillator is used in the kit. It runs at about 48kHz and is divided by 4 prior to being used as the system clock (Figure 5). The internal clock period is thus 83.3μS, and the signal integration period (1000 clock pulses) is 83.3mS. This gives a measurement frequency of 3 readings per second since each conversion sequence requires 4000 clock pulses. Setting the clock oscillator at precisely 48kHz will result in optimum line frequency (60Hz) noise rejection, since the integration period is an integral number of line frequency period (see Ref. 2 for discussion). Countries with 50Hz line frequencies should set the clock at 50kHz.

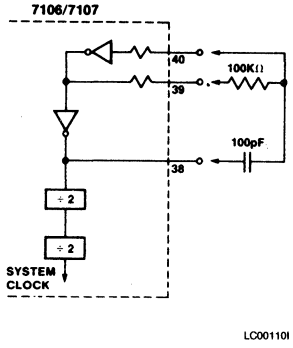


Figure 5: 7106/7107 Internal Oscillator/Clock

An external clock can also be used. In the 7106, the internal logic is referenced to TEST. External clock waveforms should therefore swing between TEST and V+ (Figure 6a). In the 7107, the internal logic is referenced to GND so any generator whose output swings from ground to +5V will work well (Figure 6b)

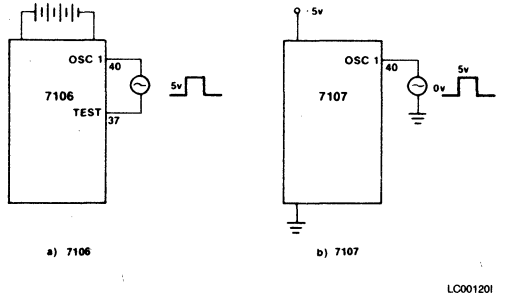


Figure 6: External Clock Options

The Reference

For 200.0mV full scale, the voltage applied between REF Hi and REF Lo should be set at 100.0mV. For 2.000V full scale, set the reference voltage at 1.000V. The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range V− to V+.

The voltage between V+ and COMMON is internally regulated at about 2.8 volts. This reference is adequate for many applications and is used in the evaluation kits. It has a typical temperature coefficient of 100ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to its higher thermal resistance, plastic parts are poorer in this respect than ceramic. The user is cautioned against extrapolating from the performance of the kit, which is supplied with a ceramic 7107, to a system using the plastic part. The combination of reference TC, internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μV pk-pk.

The linearity in going from a high dissipation count such as 1000 (19 segments on) to a low dissipation count such as 1111 (8 segments on) can also suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. These problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added as shown in Figures 7(a) or 7(b).

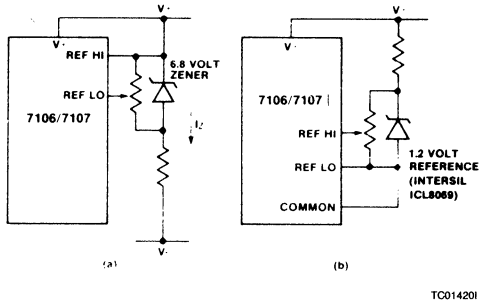


Figure 7: Using an External Reference

Power Supplies

The 7106 kit is intended to be operated from a 9 volt dry cell. INPUT Lo is shorted to COMMON, causing V+ to sit 2.8 volts positive with respect to INPUT Lo, and V− 6.2 volts negative with respect to INPUT Lo.

The 7107 kit should be operated from ±5 volts. Noisy supplies should be bypassed with 6.8μF capacitors to ground at the point where the supplies enter the board. INPUT Lo has an effective common mode range with respect to GND of a couple of volts.

The precise value is determined by the point at which the integrator output ramps within ~.3V of one or other of the supply rails. This is governed by the integrator time constant, the magnitude and polarity of the input, the common mode voltage, and the clock frequency: for further details, consult the data sheet. Where the voltage being measured is floating with respect to the supplies, INPUT Lo should be tied to some voltage within the common mode range such as GROUND or COMMON. If a −5 volt supply is unavailable, a suitable negative rail can be generated locally using the circuit shown in Figure 8.

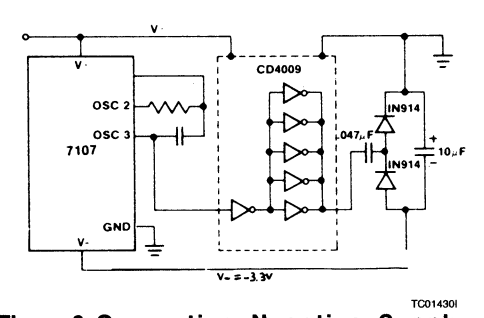


Figure 8: Generating Negative Supply From +5V

Input Filters

One of the attractive features of the 7106 and 7107 is the extremely low input leakage current, typically 1pA at 25°C. This minimizes the errors caused by high impedance passive filters on the input. For example, the simple RC (1MΩ/.01μF) combination used in the evaluation kits introduces a negligible 1μV error.

PRELIMINARY TESTS

Auto Zero

With power on and the inputs shorted, the display should read zero. The negative sign should be displayed about 50% of the time, an indication of the effectiveness of the auto-zero system used in the 7106 and 7107. Note that some competitive circuits flash negative on every alternate conversion for inputs near zero. While this may look good to the uninitiated, it is not a true auto zero system!

Over-range

Inputs greater than full scale will cause suppression of the three least significant digits; i.e. only 1 or −1 will be displayed.

Polarity

The absence of a polarity signal indicates a positive reading. A negative reading is indicated by a negative sign.

Further evaluation should be performed with the help of a precision DC voltage calibrator such as Fluke Model 343A. Alternatively a high quality 4½ digit DVM can be used, provided its performance has been measured against that of a reliable standard.

DPM COMPONENTS: SOURCES OF SUPPLY

It has already been shown that the 7106 and 7107 require an absolute minimum of additional components. The only critical ones are the display and the integration capacitor.

The following list of possible suppliers is intended to be of assistance in putting a converter design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

Liquid Crystal Displays

a) LXD Inc., Cleveland, Ohio, 216/831-8100
b) Hamlin Inc., Lake Mills, Wisconsin, 414/648-2361
c) IEE Inc., Van Nuys, California, 213/787-0311
d) Shelley Associates, Irvine, California, 714/549-3414
e) Crystaloid Electronics, Stow, Ohio, 216/688-1180

LED Displays (Common Anode)

a) Hewlett Packard Components, Palo Alto, California, 415/493-1212
b) Itac Inc., Santa Clara, California, 408/985-2290
c) Litronix Inc., Cupertino, California, 408/257-7910
d) Monsanto Inc., Palo Alto, California, 415/493-3300

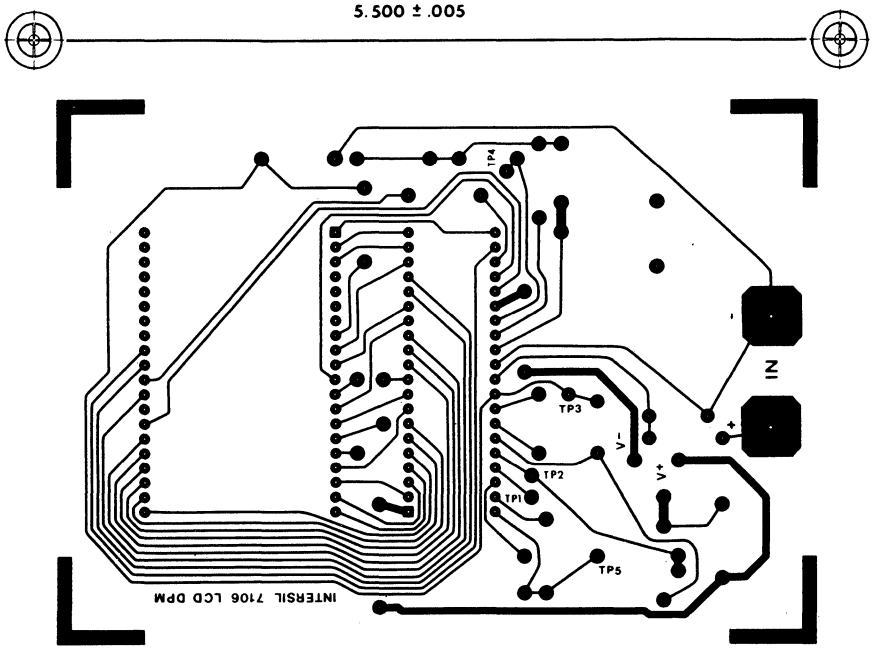
Polypropylene Capacitors

a) Plessey Capacitors, West Lake Village, California, 213/889-4120
b) IMB Electronic Products, Santa Fe Springs, California, 213/921-3407
c) Elcap Components, Santa Ana, California, 714/979-4440
d) TRW Capacitors, Ogallala, Nebraska, 308/284-3611

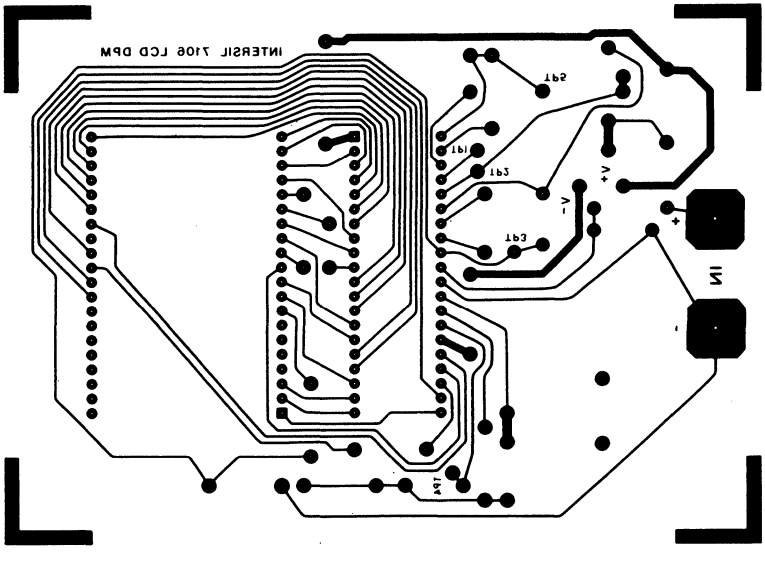
CAUTION: Potential trouble areas when constructing the evaluation kits.

1. **Certain LCD displays have a protective plastic sheet covering the plastic top. This sheet may be removed after installing the display to maximize display viewing.**
2. **Solder flux or other impurities on PC board may cause leakage paths between IC pins and board traces reducing performance and should be removed with rubbing alcohol or some other suitable cleaning agent. Displays should be removed when cleaning as damage could result to them.**
3. **Blue PC board material (PC75) has been treated with a chemical which may cause surface leakage between the input traces. It is suggested that the board be scribed between the input traces and adjacent traces to eliminate this surface leakage.**
4. **In order to ensure that unused segments on the LCD displays do not turn on, tie them to the backplane pin (pin 21).**

APPENDIX I: 7106 Printed Circuit Board Layout and Component Placement



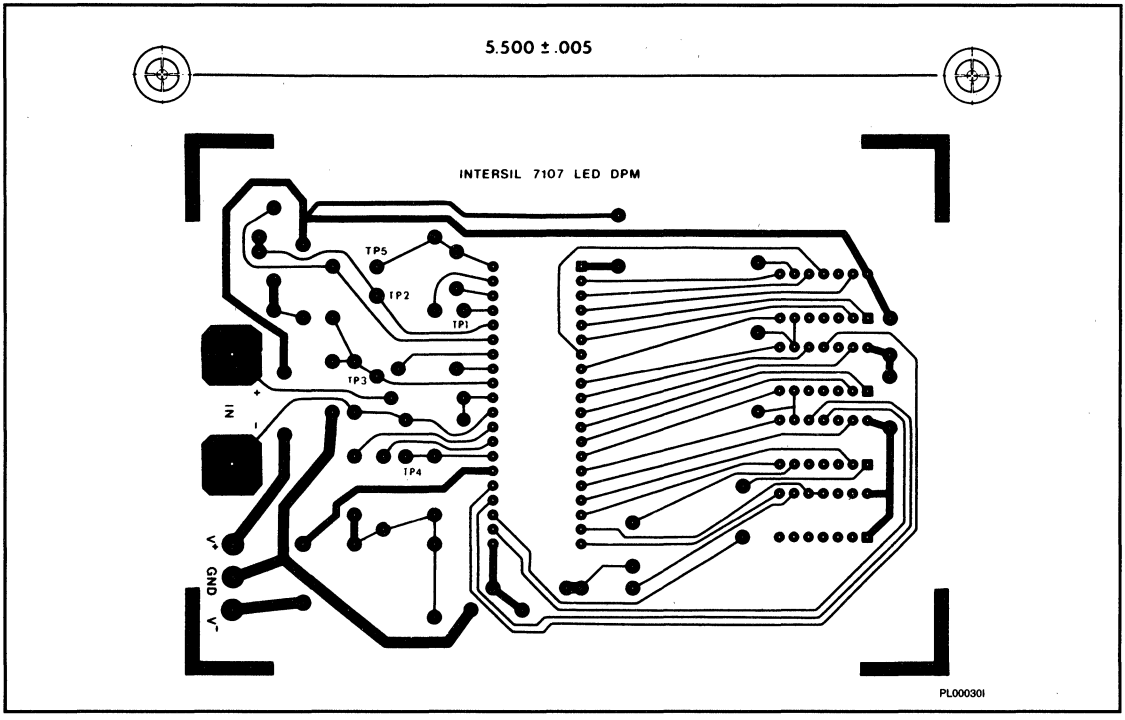
PL000101

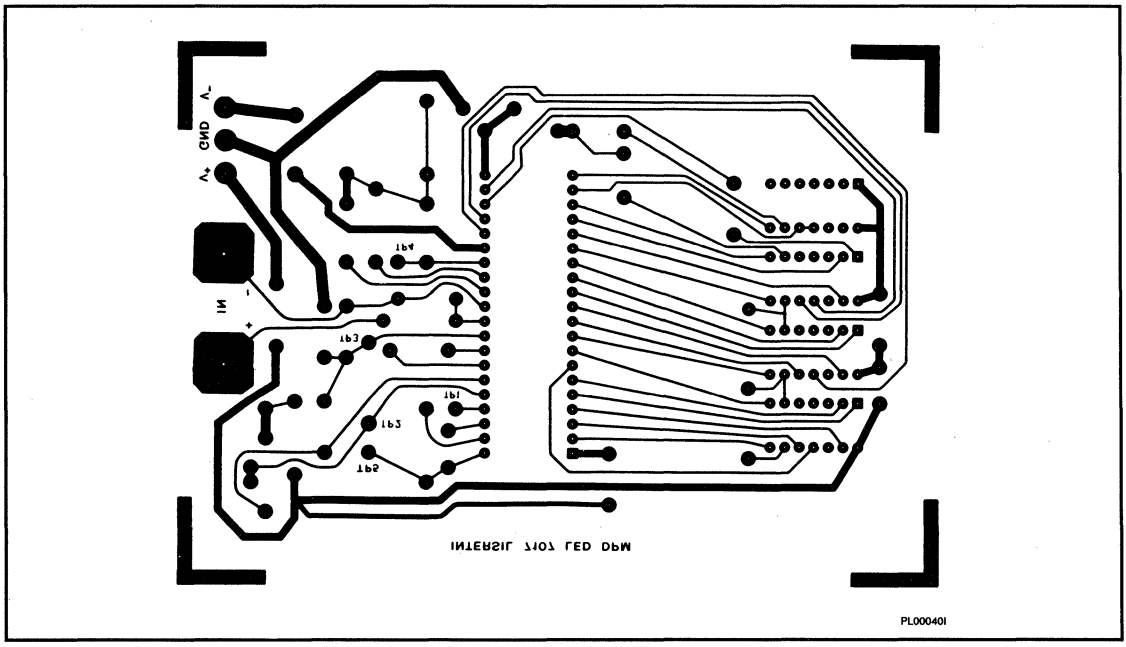


PL000201

† Jumper to display decimal for temporary decimal point. See text.

APPENDIX II: 7107 Printed Circuit Board Layout and Component Placement





* Jumpers can be inserted here to short IN LO to GND or COMMON.

† Jumpers to decimal point if required.

A049
Applying the 7109 A/D Converter

This article examines the operation and applications of the ICL7109 monolithic, CMOS, 12 bit, integrating analogue to digital converter which was introduced to the market early in 1979.

Figure 1 shows the equivalent circuit of the ICL 7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 2. They are Auto-Zero (AZ), Signal Integrate (INT) and Deintegrate (DE).

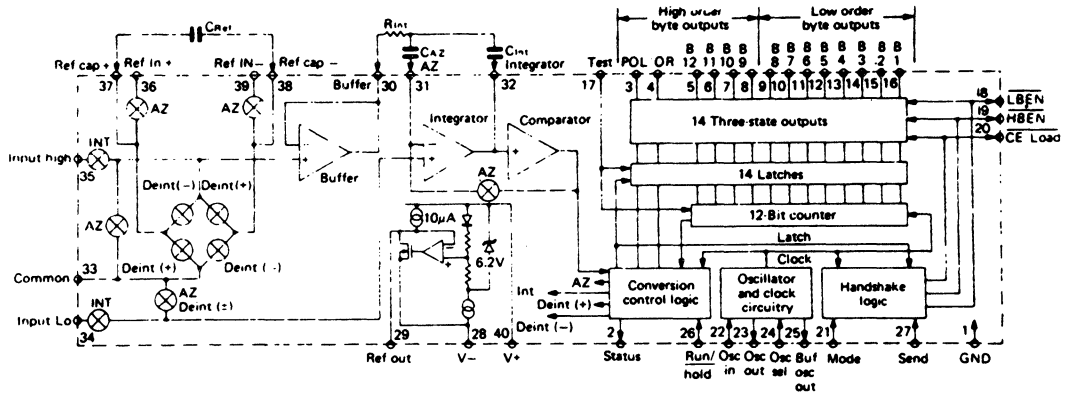


Figure 1

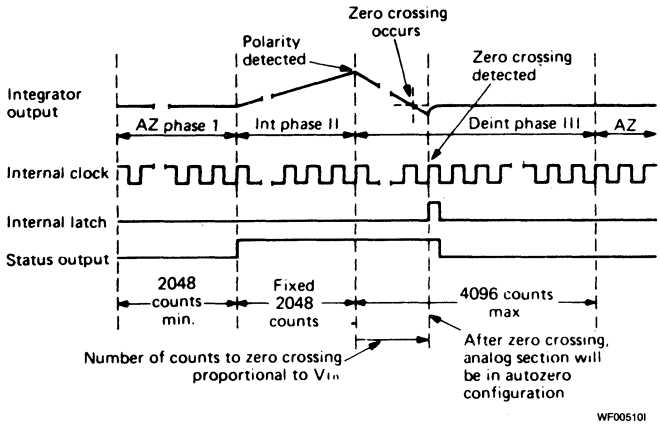


Figure 2

Auto-zero phase. During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analogue common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the *AZ* accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal integrate phase. During signal integrate the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined.

Deintegrate phase. The final phase is deintegrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range the system has a c.m.r.r. of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to ensure that integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near fullscale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

The ICL7109 has, however, been optimised for operation with analogue common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative, maximising the performance of the analogue section.

DIIFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The ICL7109 provides a reference output (pin 29) which may be used with a resistive divider to generate a reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm.

Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error. For this reason, an external high-quality reference should be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made. The internal reference may then be used as a pre-regulator for an external reference, such as the ICL8069 bandgap reference diode.

DIGITAL SECTION

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic.

The MODE is used to control the output mode of the converter.

Direct mode. When the MODE pin is left at a low level, the data outputs (bits 1 to 8 low order byte, bits 9 to 12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, and enables the converter to be interfaced directly, either as I/O or by memory mapping, to any microprocessor system with an 8-bit, 12-bit or 16-bit word length.

Handshake mode. The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM 6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimise the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE input. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed. The MODE terminal may also be used to trigger entry into the handshake mode on demand.

In this mode, the SEND input is connected to the UART TBRE output so that the ICL7109 can detect when the UART is ready for more data. The $\overline{\text{CE/LOAD}}$ pin becomes an output strobe and is connected to the UART TBRL input to clock data into the UART $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ also become outputs which identify the high and low bytes respectively. Figure 3 shows the output sequence.

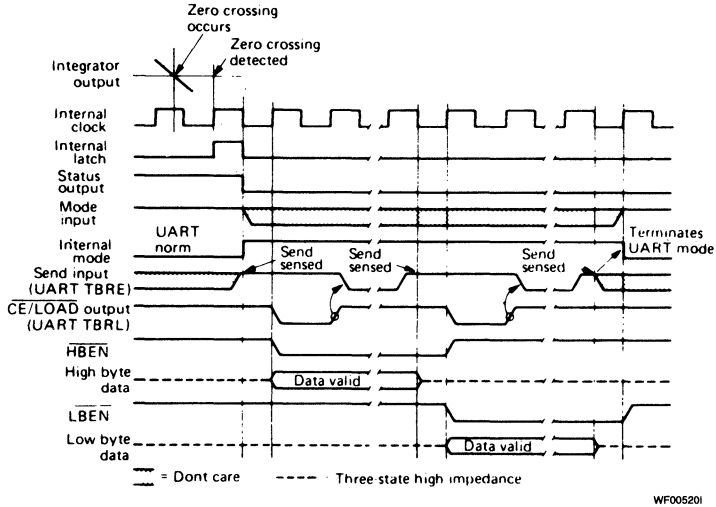


Figure 3

Assuming the UART transmitter buffer register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The CE/LOAD and HBEN terminals will go low after SEND is sensed, and the high order byte outputs become active. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART transmitter buffer register. The UART TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the transmitter register and cleared the transmitter buffer register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the HBEN output returns high. At the same time, the CE/LOAD and LBEN outputs go low, and the low order byte outputs become active. Similarly, when the CE/LOAD returns high at the end of one clock period, the low order data is clocked into the UART transmitter buffer register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, the the CE/LOAD, HBEN, and LBEN terminals return high and stay active (as long as MODE stays high).

STATUS OUTPUT

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches (See Figure 2 for details of this timing). This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

When RUN/HOLD is held high or left open (it has an internal pull-up resistor) the 7109 converts continuously, taking 8192 clock cycles for each conversion. If RUN/HOLD is taken low, the current conversion is completed and the 7109 then remains in Auto Zero state until RUN/HOLD is taken high. A single, positive pulse on RUN/HOLD will cause one conversion only to take place and is a simple way of providing a "convert on command".

From the foregoing, it will be seen that the ICL7109 is a converter offering unusual flexibility in both input and output interfacing. Let us first see how flexible input interface leads to a number of applications.

BRIDGE MEASUREMENTS

The differential input of an ICL7109 lends itself to measurement of error voltages in resistance bridges, as the common mode voltage is immaterial. Moreover, because the 7109 is ratiometric, if the reference input to the chip is derived from the bridge supply, changes in the supply will not upset the output reading. A typical example is a bridge connected load cell.

Some strain gauge bridges have very low output voltages. The input noise of the ICL7109 is about 15μV peak to peak, so that if a bridge with say 5μV per count were used the output reading would jitter. This problem can be solved in two ways. The first is to use a low drift, low offset amplifier, such as the ICL7650 chopper stabilized operational amplifier, before the converter. An alternative is to have the microprocessor take the average of several conversions. (Usually 2, 4, 8 or 16 so that the division sum is a simple right shift of the binary word).

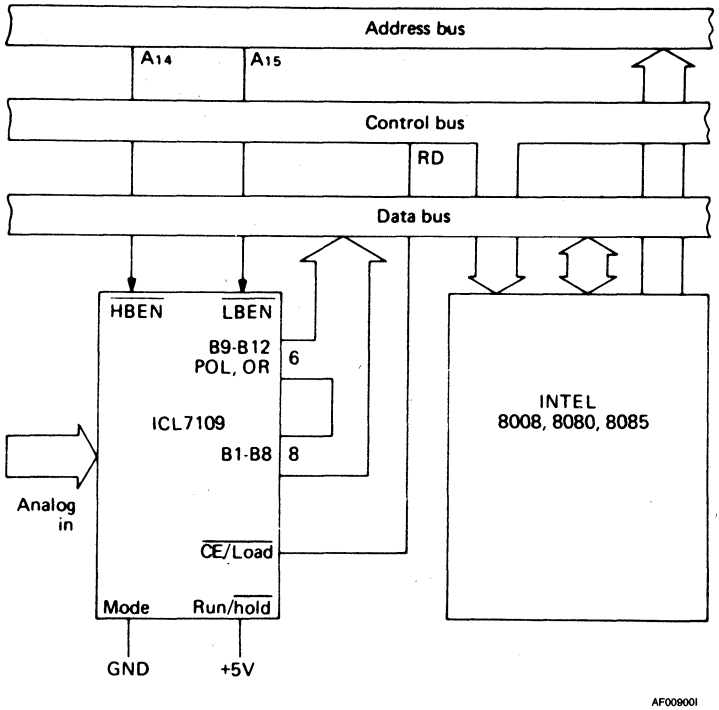


Figure 4

OFFSET ZERO MEASUREMENTS

By hooking Input Low of the 7109 to some voltage other than signal ground, measurements with an offset zero are easily possible. Consider a temperature measurement scheme using the −2mV/°C temperature coefficient of the V_{be} of a silicon transistor. By connecting one input pin to the transistor and the other to a variable voltage source the 7109 can be made to read zero at 0°C, even though the transistor V_{be} is still about 0.65V. Because the temperature coefficient of the transistor is negative, IN HI and IN LO have been interchanged so that the output goes positive for increasing temperature.

These are just a few examples of how the fully differential, fully ratiometric inputs of the ICL7109 can simplify the design of input circuitry. Now let us pass on to output configurations.

DIRECT PARALLEL PROCESSOR INTERFACES

The separately tri-state byte wide outputs of the ICL7109 make it ideal for interfacing to 8-bit microprocessor busses. Figure 4 shows a direct memory mapped interface to an 8-bit Intel 8085 processor bus. In this case linear addressing is used to select the two data bytes.

SERIAL INTERFACE

The ICL7109 is easily combined with a UART, and if necessary an analogue multiplexer, to provide a complete remote serial data acquisition station (Figure 5). The UART at the processor end of the serial link sends a digital word to the remote UART This word specifies the multiplexer address, and at the same time the remote UART Data Ready flag takes the $\overline{\text{RUN/HOLD}}$ line of the 7109 high to initiate a conversion. The appropriate input is therefore selected and converted and when conversion is complete the 7109 enters its handshake sequence, transmitting the converted data over the serial link. The $\overline{\text{HBEN}}$ output from the 7109 also clears the UART Data Ready flag so that RUN/HOLD returns low and no further conversions take place.

Optoisolators can optionally be put in the serial lines to allow for large common mode voltage differences between processor and remote station. Because all components in the remote station are low power CMOS, the generation of isolated supplies is simplified.

REPLACING V TO F CONVERTERS

A popular method of making a low cost serial interface, particularly where opto-isolation is required, is to use a V to F converter. Such an approach has its problems, as V to Fs need accurate and stable analogue components to operate correctly. They also do not generally have zero offset, scale factor drift and linearity commensurate with 12-bit accuracy applications.

The ICL7109 has a much more flexible input interface and better performance at a cost comprable with V to F converters. The STATUS output remains high for a period of

N + 2049½ clock cycles, where *N* is the digital reading. (See Figure 2). Therefore if the BUF OSC OUT from the 7109 is gated with STATUS a pulse train results which can be passed through an opto-isolator and counted by a processor to determine the digital reading, in much the same way as it would with a V to F converter. The processor only needs a simple software timeout loop to determine when the pulse train has ended. There are no critical timing requirements such as are encountered when using a V to F converter.

Alternatively, the STATUS and BUF OSC OUT lines can be separately opto-isolated and fed to a hardware counter system, if display of data is required. A suitable counter/display system uses the ICM7217 4 decade counter.

The 2049½ pulses are subtracted by presetting the counter to 7950, the tens complement of 2050. This technique has been used to make d.v.m.s with high voltage input isolation.

CONVERSION SPEED

The ICL7109 is an integrating (dual slope) converter and as such is not intended for very fast applications. The data sheet specifications are quoted at 7.5 conversions per second (corresponding to an internal clock frequency of about 61.5kHz, or a clock period of 16.3μs).

The speed of a dual slope converter is principally limited by the response time of the comparator, bearing in mind that the input to the comparator is a shallow ramp rather than a nice clean voltage step. In the ICL7109 the comparator gain/bandwidth product is about 200MHz, giving a delay of about 4μs. For this delay to represent a ½ count error the clock period would be 8μs, giving 15 conversions per second.

The logic of the ICL7109 is capable of operating at up to 500kHz, however, which would give about 60 conversions per second. At this speed the comparator delay will result in a zero offset. Linearity and resolution are, however, unaffected. (Remember that as the clock frequency is increased, the integrator and auto zero capacitors should be reduced in proportion). In many systems it is a simple matter for the microprocessor to subtract the zero offset.

An alternative technique is to compensate the zero offset by placing a small resistor in series with the integrator capacitor. Because the current in the integrator capacitor is constant during deintegrate, this resistor produces a "lead" on the ramp which can be calculated as follows.

Slope of the ramp, $\frac{dv}{dt} = \frac{I}{C}$

Offset voltage of ramp, $\Delta V = IR$

Time lead of ramp,

$$\Delta t = \Delta V, \frac{dt}{dV} = IR, \frac{C}{I} = RC$$

Therefore:- $R = \frac{\Delta t}{C}$, *where* $\Delta t = 4\mu s$.

By this means, the zero offset is cancelled (the system works for both input polarities). One error is being offset with another, and the two may not track with temperature, so this method is not to be relied on for wide temperature range applications.

The ICL7109 has shown itself to be one of the most versatile and cost effective A/D converters on the market, replacing existing 12-bit converters, as well as creating new applications which previously had been the domain of V to F converters and other devices.

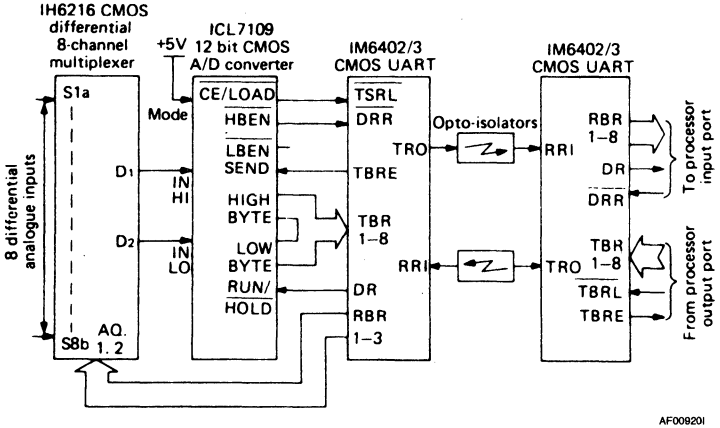


Figure 5

AO32
Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family

INTRODUCTION

Most of Intersil's one chip A/D converters offer differential input, differential reference and separable analog and digital ground references. The price of all this freedom, of course, is technical vigilance, and this note is intended as a defense manual against the potholes and landmines it makes accessible. The discussion is based on the ICL7106/7, but applies in large part to the ICL7116/7, the ICL7126, the ICL7109, and to a lesser extent to the ICL7135.

GENERAL DESCRIPTION

Figure 1 shows the Block Diagram of the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

Auto-Zero Phase

During Auto-Zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal INTegrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between INHI and INLO for a fixed time. This differential voltage can be within a wide common mode range — within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, INLO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is DE-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$1000 \left(\frac{V_{in}}{V_{ref}}\right).$$

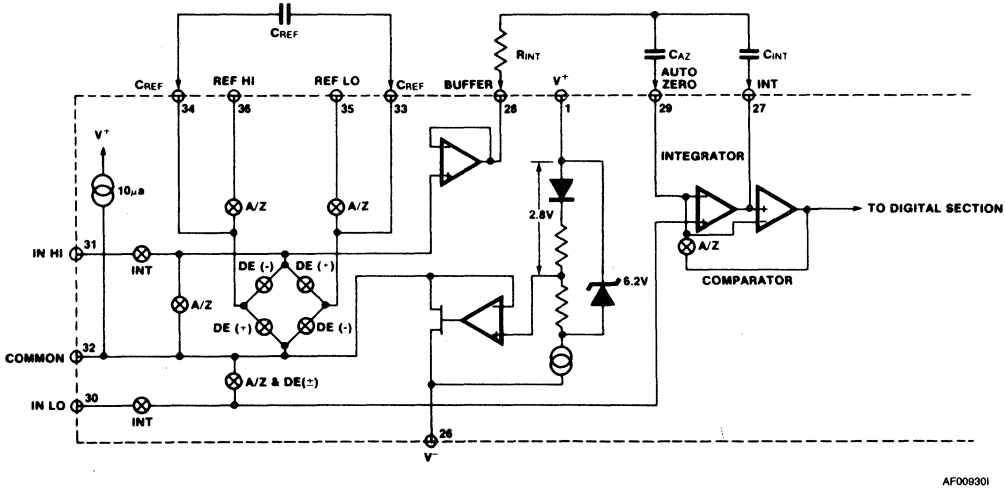


Figure 1: Analog Section of 7106/7107

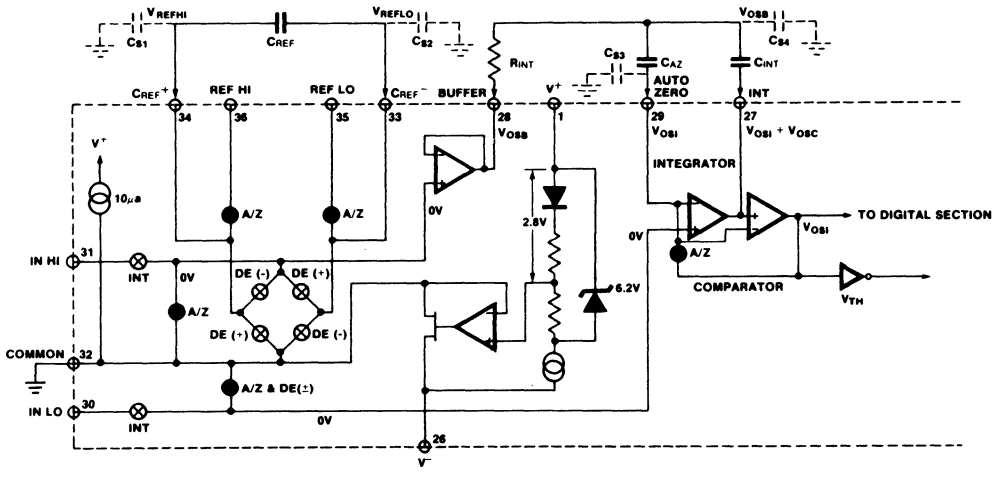


Figure 2: Auto-Zero Phase, with Offset Voltages and Stray Capacitances

CMRR AND COMMON MODE VOLTAGE EFFECTS

There are three basic voltages applied to the ICL7106/7, etc. which can give "common mode voltage" consequences. These are indicated in Figures 2, 3, and 4 which show the analog section in the phases described above. The choices are 1 of reference voltage source to COMMON, 2) of input voltage source to COMMON, and 3) of COMMON to (digital) supply voltage.

During Auto-Zero, the outputs of the buffer, integrator, and comparator are all within various offset voltages of analog COMMON. These are marked on Figure 2, which shows the Auto-Zero phase. For the remainder of the discussion, these offset voltages will be ignored, since they are merely added to other voltage changes described. The non-inverting inputs of the buffer and integrator are also tied to analog COMMON, so it is convenient to describe all these voltages with respect to COMMON.

Reference Common Mode Voltage to COMMON

The reference capacitor is recharged during the Auto-Zero time; the stray capacitance shown in Figure 2 as CS1 and CS2 will also be charged. During DE-integrate (Figure 4) the reference capacitor is switched so that one or the other of its terminals is at analog COMMON. This will cause charge-sharing with the stray capacitances on the other terminal. In particular, a common mode voltage on the reference input (with respect to COMMON) will give a roll-over error, since the effective DE-integrate reference will be higher in one polarity than the other. The ideal here is for $(V_{REFHI} + V_{REFLO}) = 2\ V_{ANCOM}$, at least for equal stray capacitances, but this is inconvenient in most applications. The roll-over error contribution at full scale (ignoring a second order term) is

$$2000\ \frac{(V_{REFLO}\ C_{S1} + V_{REFHI}\ C_{S2})}{V_{REF}\ C_{REF}} \simeq$$

$$2000\ \frac{V_{CM}\ (C_{S1} + C_{S2})}{V_{REF}\ C_{REF}}\ \text{(counts)}$$

For $C_{REF} = 0.1\ \mu F$, $C_S = 15pF$, $V_{CM}/V_{REF} = 10$, this can give two counts of error, but if $V_{REFLO} = 0$, and C_{S2} is 5pF, the error is 0.1 counts, lost in the noise level. In the latter case (a very common application condition) C_{S1} does not contribute any errors, so putting the "outside foil" of the reference capacitor to this side will minimize roll-over. Also increasing C_{REF} (without corresponding increases in C_S) will reduce rollover. Note that stray capacitance to the buffer output is also unimportant if either REFHI or REFLO is at COMMON.

Input Voltage to COMMON

First, the direct CMRR of the buffer and integrator op amps will themselves lead to a scale factor error and an offset if INLO is not at analog COMMON. Higher order CMRR terms are generally negligible, and this first order term is very small for most devices. It can be adjusted out in most applications with a reference voltage adjustment. More serious is the effect of stray capacitance to ground of the integrating and auto-zero capacitors, and the AZ pin, C_{S4} and C_{S3} in Figure 2. The AZ pin will swing from COMMON to INLO (Figure 3) and C_{S3} will have to be charged through C_{AZ}, giving an error voltage on C_{AZ}, during the integrate phase, of:

$$\Delta\ V_{AZ} = V_{INLO}\ \frac{C_{S3}}{C_{AZ}}$$

This acts as an offset voltage referred to the input, and is most serious for small ratios of full-scale input voltage to common mode voltage: For $C_{AZ} = 0.47\ \mu F$, $C_{S3} = 10pF$, $V_{INLO} = 2V$, the offset will be $40\mu V$, or 0.4 counts for 200mV full scale input. This charge is recovered in the transition back to COMMON for DE-integrate (Figure 4), so the offset is not continued in this phase. The same charge, together with that due to C_{S4}, also flows through the integrating capacitor. Ignoring second-order terms, the error

voltage on the integrator output during the integrate phase will be:

$$\Delta V_{INT} = V_{INLO}\left(\frac{C_{S3}}{C_{AZ}} + \frac{C_{S3}+C_{S4}}{C_{INT}}\right)$$

However, the charge transferred through the integrating capacitor is also recovered for DE-integrate and does not cause any errors, except for inputs near zero. The decision as to the polarity of the input signal, and the required DE-integrate reference polarity is made precisely at the end of the integrate phase, and for small input signals the error charge on the integrating capacitor due to charging strays can exceed the true signal charge, leading to an incorrect choice of polarity. Thus, the return of the error charge at the beginning of DE-integrate will lead at once to a zero crossing and a result of zero with the wrong polarity. This shows up as a series of readings such as (in a bad case) −4, −3, +0, +0, +0, +0, +1, +2, +3, +4 for INLO negative (Figure 5). The magnitude of this effect is dependent on the full scale integrator swing, and is given by:

$$\Delta \text{ pol.} = 2000\left(\frac{V_{INLO}}{V_{INTFS}}\right)\left(\frac{C_{S3}}{C_{AZ}} + \frac{C_{S3}+C_{S4}}{C_{INT}}\right)(\text{in counts})$$

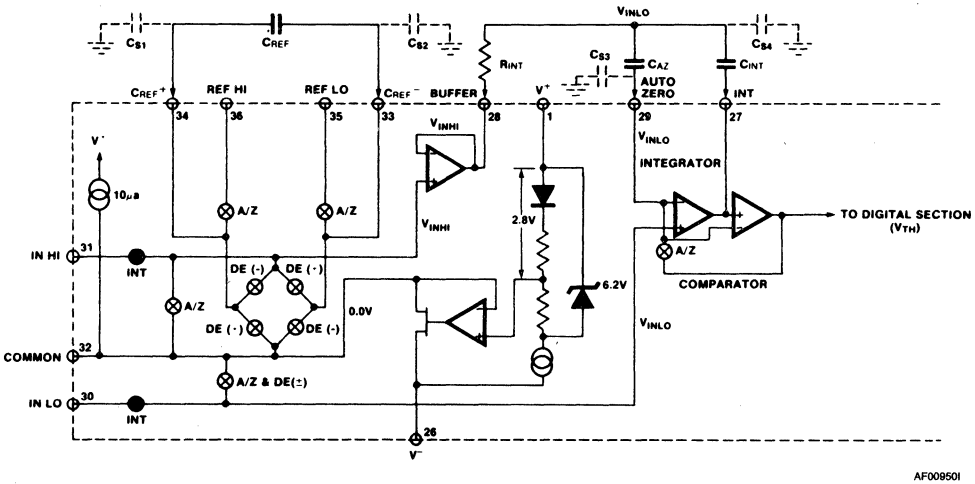


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Figure 3: Integrate Phase. All voltages shown with respect to COMMON

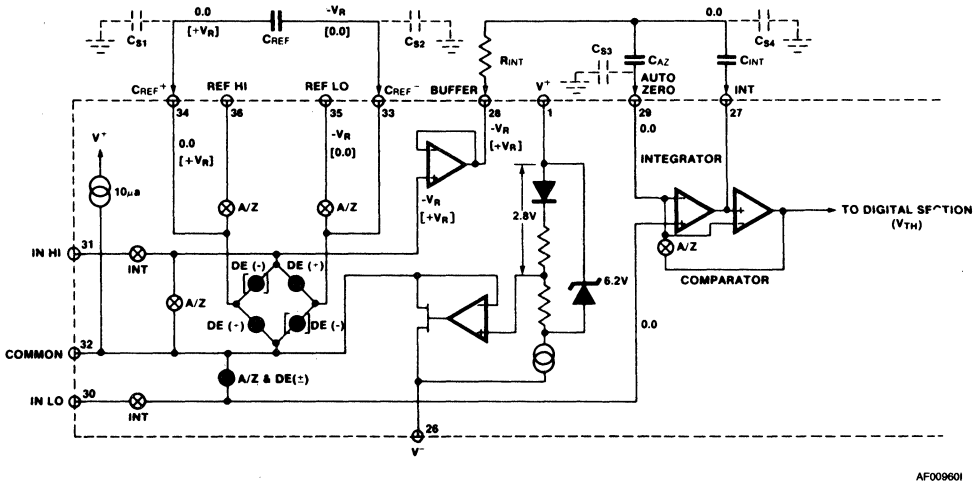

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Figure 4: DE-integrate Phase. Voltages shown with respect to COMMON, for positive input. [ ] shows values for negative input

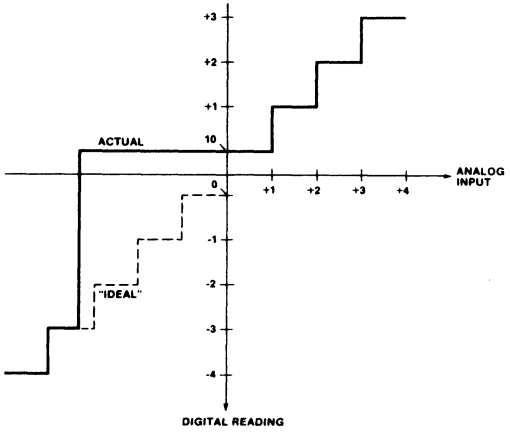

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Figure 5: "GAP" in Readings due to $V_{INLO} \neq$ COMMON (a bad case shown)

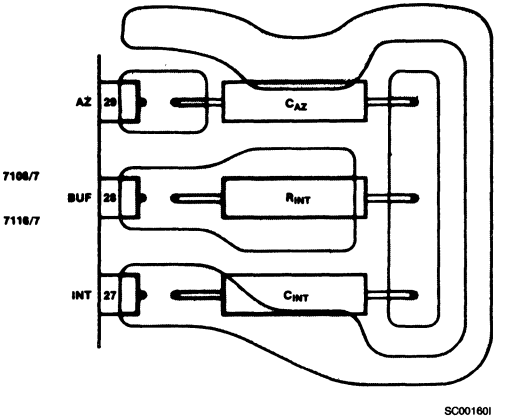

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Figure 6: Reducing Stray Capacitances C_{S3} and C_{S4}

For C_{INT} = .22μF, C_{S4} = 10pF, V_{INTFS} = +2V, and other values as before, this amounts to about 0.23 counts, but for C_{AZ} = 0.047μF (recommended for 2.0V F.S.) Δ pol is 0.6 counts. A small increase in stray capacitance or reduction of integrator swing will give a significant "gap" in the readings, as shown in Figure 5. This effect, the only one causing significant nonlinearity, can be reduced by guarding the integrating and auto-zero capacitors and resistor with either BUFFer out or INTegrator out pins in so far as possible. This can readily be done on a PC board by simple extension of the traces leading from those pins to the three components, as suggested in Figure 6. Note that excessive capacitance across R_{INT} will increase the width of the zero reading (see A017 for a discussion of a similar effect), while capacitance across C_{AZ} and C_{INT} has no effect on the circuit.

Analog COMMON to Digital Supply Voltages

The COMMON line on the ICL7106/7 family of devices provides a convenient ground-return point in many applications; particularly with floating (battery) supplies. However, in a fixed supply environment, improved integrator swing (improving many system parameters) can be achieved if COMMON is pulled more negative, and the circuit has been set up to allow this. The effects described above are all independent of the actual level of COMMON, but the next one is not!

The DE-integrate phase should ideally terminate when the output of the comparator returns to the value it had during Auto-Zero (analog COMMON), but will actually terminate when the output passes through the logic threshold of the zero-crossing gate and flip-flop combination. The "free" analog COMMON voltage is very close to the logic threshold, giving a negligible error, but if analog COMMON is pulled negative, zero crossing will be detected late for positive inputs, (reading high) and early for negative inputs (reading low), this leads to a (positive) offset. The polarity detection sees the same influence, so no nonlinearity results. The magnitude of this offset depends on comparator gain (typically 7-8K, but as low as 3K in some devices) and F.S. integrator swing;

$$\text{OFFSET (COMMON)} = 2000 \left(\frac{V_{COMMON} - V_{TH}}{V_{INTFS}\ A_{AVCOMP}} \right)$$

With a 2V swing and 3K gain, this will contribute 1/3 count per COMMON negative volt. This can be used to measure comparator gain, at least with moderate accuracy, which is otherwise hard to do. Obviously, the offset can be minimized by maximizing the integrator swing. The comparator gain varies from device to device, and is limited also by the need to keep the comparator fast. Various improvements in this gain have been made, and will probably continue to be made in the future, but this offset should be considered carefully if COMMON is to be moved away from its "free" location, or if the logic supplies are altered.

The Auto-Zero Loop Residual

During the Auto-Zero phase, the converter self-corrects for all the offset voltages in the buffer, integrator, and comparator.

This section covers a normally undetectable, but under some circumstances significant, error generated in the auto-zero system. A similar effect which occurs in the 2-chip systems has been discussed previously (see A030, Appendix A), but the details and remedies are sufficiently different to warrant a separate discussion.

The relevant circuit to be discussed is shown in Figure 7 and the major cycle waveforms in Figure 8. Let us first assume that the prior auto-zero cycle has been indefinitely long, or is otherwise ideal, so that the conversion starts with no residual error on the auto-zero capacitor. The integrate and DE-integrate cycles will be classically perfect to the point at which a zero-crossing actually occurs (at the output of the integrator). However, from this point two delays occur; first the comparator output is delayed (due to comparator delay) and secondly the zero-crossing is not registered until the next appropriate clock edge. (For further

discussion of this, see Application Note A017). At this point, the circuit is returned to the auto-zero connection (logic and switch delays may be absorbed in comparator delay as far as our discussion is concerned). The net result is that the integrator output voltage will have passed the zero-crossing point by an amount given by

$$V_{Ires} = \pm V_{IFS}\left(\frac{c_D + c_X}{c_{FS}}\right)$$

where $0 \leq c_X \leq 1$ is the variable delay, c_D is the fixed delay, c_{FS} is the full scale count in units of clock pulse periods, and V_{IFS} is the full scale integrator swing in volts.

Note: In all subsequent discussions, "C" indicates a capacitor, while "c" denotes a number (not necessarily an integer) of counts.

The range of this residual voltage corresponds to the integrator swing per count, and is independent of input value, except for polarity.

Note, however, that we have assumed a zero-crossing actually occurred. If the input is overloaded (past full scale), DE-integrate will terminate with a substantial residual voltage remaining on the integrator capacitor. The maximum value of this residual depends on the total possible swings of buffer and integrator, as compared to the "full scale" values used. In general, we may treat this case as corresponding to a large negative value of c_X.

The immediate effect of closing the auto-zero loop may be seen by examining Figure 7. We may consider the comparator as acting as an op-amp. Under these conditions: the voltage across the auto-zero impedance is high, and the (nonlinear) impedance is low; on the other hand, the initial voltage across the integrating resistor is zero.

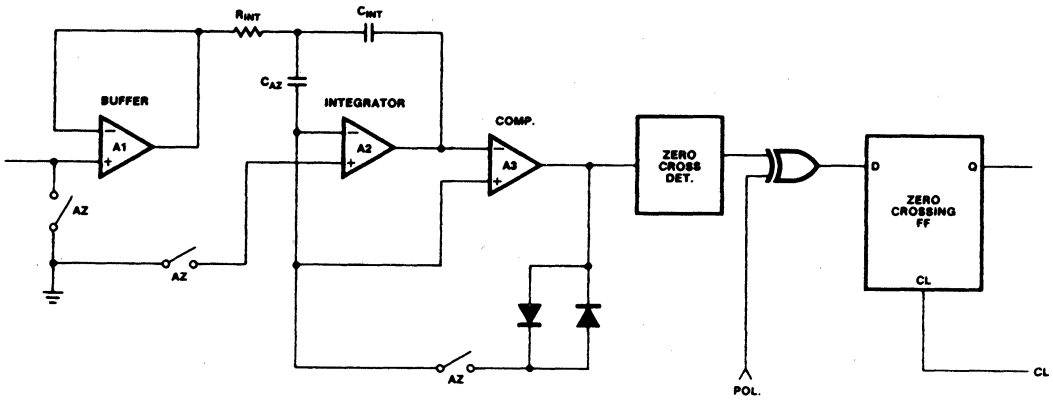

Figure 7: The Analog System (simplified to show only Auto-Zero connections)

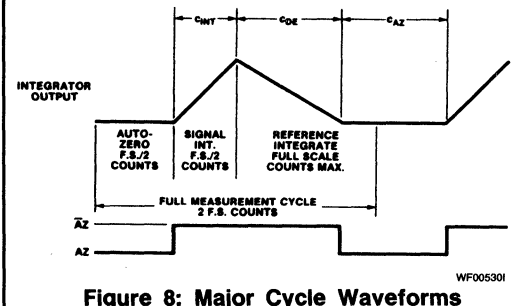

Figure 8: Major Cycle Waveforms

Thus, the auto-zero capacitor will be charged rapidly to exactly cancel the residual voltage, as shown in Figure 9. The output of the integrator is now at the correct position, but the auto-zero and integrator capacitors have shared the original error. The junction point of the two capacitors and resistor has been moved by a portion of the original residual voltage, given by:

$$V_{AZI} = V_{Ires}\left(\frac{C_{INT}}{C_{AZ} + C_{INT}}\right) \qquad \textbf{(4.1)}$$

This voltage will decay with a time constant controlled by the integrating resistor and the two capacitors, while the auto-zero capacitor is easily kept in step owing to the high comparator gain. Thus, at the end of the auto-zero time, $t_{AZ} = c_{AZ}\ t_{cp}$., the residual will be reduced to:

$$V_{AZres} = V_{AZI}\ \exp\left(\frac{(-c_{AZ})\ (t_{cp})}{R_{INT}(C_{INT} + C_{AZ})}\right)$$

$$= V_{Ires}\left(\frac{C_{INT}}{C_{AZ} + C_{INT}}\right)\exp\left(\frac{(-c_{AZ})\ (t_{cp})}{R_{INT}\ (C_{INT} + C_{AZ})}\right)$$

For the residual left after a zero-crossing, we may further refine this to:

$$V_{AZres} = V_{IFS}\left(\frac{c_X + c_D}{CFS}\right)\frac{C_{INT}}{(C_{AZ} + C_{INT})} \qquad (4.2)$$

$$\exp\left(\frac{-c_{AZ}\, t_{cp}}{R_{INT}\,(C_{INT} + C_{AZ})}\right)$$

For the overrange case, we may again assume a large negative c_X value.

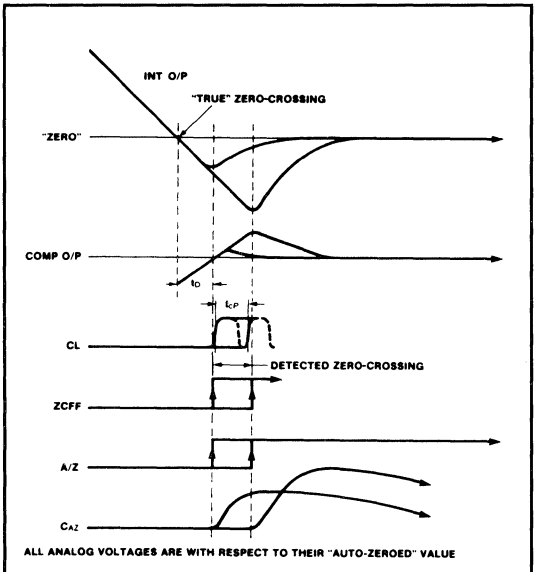

Figure 9: Waveforms at Beginning of Auto-Zero Interval

Now $R_{INT}\, C_{INT}$ is controlled by the buffer swing, V_{BFS}, the integrator swing, V_{IFS}, and the integration time $t_{INT} = c_{INT}\, t_{cp}$, so that

$$V_{BFS}/R_{INT} \cdot t_{INT} = C_{INT}\, V_{IFS},$$

$$\text{or } R_{INT}\, C_{INT} = c_{INT}\frac{V_{BFS}}{V_{IFS}}\, t_{cp}$$

Also we may write $C_{AZ} = a\, C_{INT}$, for convenience, and will then obtain

$$V_{AZres} = V_{Ires}\left(\frac{1}{1+a}\right)\exp\left(\frac{-c_{AZ}\, V_{IFS}}{c_{INT}\, V_{BFS}\,(1+a)}\right) \qquad (4.3)$$

This residual voltage on the auto-zero capacitor effectively increases the magnitude of the input voltage as seen on the output of the buffer. Thus, converting this voltage to count-equivalents.

$$c_{AZres} = \frac{V_{AZres}}{V_{BFS}} \cdot CFS = \frac{V_{IFS}}{V_{BFS}}\frac{(c_X + c_D)}{(1+a)} \qquad (4.4)$$

$$\exp\left(-\frac{c_{AZ}}{c_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+a}\right)$$

Since this voltage also subtracts from the reference, its effect at the input is magnified in the ratio

$$c_{INres} = c_{AZres}\left(\frac{c_{INT} + c_{DE}}{c_{INT}}\right) \text{ so that}$$

$$c_{INres} = \left(1 + \frac{c_{DE}}{c_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)\frac{(c_X + c_D)}{(1+a)} \qquad (4.5)$$

$$\exp\left(-\frac{c_{AZ}}{c_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+a}\right)$$

Note that c_{DE} is equal to the displayed result, except for overrange conditions, when it is equal to c_{FS} and the first bracket becomes 3. Also, $c_{AZ} = c_{INT}$; and this expression, so substituted, determines the overrange residual performance.

For the normal in-range condition, two things should be noted here. First, this residual acts to increase the input voltage magnitude, and secondly, a small increase in input voltage tends to decrease the magnitude of the residual until the result count changes. These effects lead to "stickyness" in the readings; suppose, in a noise-free system, that the input voltage is at a level where the residual's a minimum, the detected zero-crossing follows the true one as closely as possible. A minute increase in input voltage will cause the zero-crossing to be detected one pulse later and the residual to jump to its maximum value. The effect of this is a small increase in the apparent input voltage; thus if we now remove the minute increase, the residual voltage effect will maintain the new higher reading; in fact we will have to reduce the input voltage by an amount commensurate with the effective residual voltage to force the reading to drop back to the lower value. In more detail, we should consider the equilibrium conditions on the auto-zero capacitor. Clearly, the voltage added at the end of reference integrate must just balance that which decays away during the auto-zero interval. So far the relationships we have developed have assumed a zero residual before the conversion, but in the equilibrium condition the residual given by equation (4.4) remains, and at the end of conversion, the new amount, given by equation (4.1), is added to this, so we start the "auto-zero decay" interval with

$$c_{AZI} = c_{AZres} + \frac{V_{IFS}}{V_{BFS}}\frac{(c_X + c_D)}{(1+a)} \qquad (4.6)$$

By combining equations (4.4) and (4.6) we find, for the equilibrium condition,

$$c_{AZres} = \pm\frac{V_{IFS}}{V_{BFS}}\frac{(c_X + c_D)}{(1+a)}$$

$$\left[\exp\left(+\frac{c_{AZ} V_{IFS}}{c_{INT} V_{BFS}\,(1+a)}\right) - 1\right]^{-1}$$

Once again, the effect of this at the input is multiplied by the ratio of total input integrate times, so that, under equilibrium conditions,

$$C_{INres} = \pm\frac{V_{IFS}}{V_{BFS}}\left(1 + \frac{c_{DE}}{c_{INT}}\right)\frac{(c_X + c_D)}{(1+a)} \qquad (4.7)$$

$$\left[\exp\left(\frac{C_{AZ}V_{IFS}}{C_{INT}\ V_{BFS}(1+a)}\right)-1\right]^{-1}$$

Those expert at skipping to the end of the difficult bit will recognize that as the final equation, in terms of complexity. So let us now see what it means. Clearly, the error term is greater, the larger c_{DE}/c_{INT}, and the smaller c_{AZ}/c_{INT}. For the devices considered here (except some applications of the ICL7109) these are both worst case near full scale input, where $c_{DE}/c_{INT} \approx 2$ and $c_{AZ}/c_{INT} \approx 1$.

Substituting these, we find the worst case

$$C_{INres} \simeq \pm\frac{V_{IFS}}{V_{BFS}}\ (3)\ \frac{(c_X + c_D)}{(1+a)}\left[\exp\left(\frac{V_{IFS}}{V_{BFS}(1+a)}\right)-1\right]^{-1} \quad \textbf{(4.8)}$$

Recall that c_D is fixed; and c_X must be between 0 and 1. The expression is now a function purely of the ratio of integrator and buffer full scale swings, and the ratio of auto-zero and integrator capacitors, a. The effect of the latter ratio is mixed; a larger value reduces the initial error, but increases the time — constant for its decay. The relationship is plotted in Figure 10 and shows the desirability of keeping the integrator swing higher than the buffer swing. Note also that a lower capacitance ratio a always improves the residual. However, both noise and the common-mode effects discussed in Section 3 above require a large auto-zero capacitor, and a compromise must be reached. In general, if the full scale input is small, a large C_{AZ} is needed, but for larger full scale inputs, a smaller value is best. Note also that the comparator delay (c_D in equation (4.8)) is also effectively enhanced. This has the effect of shrinking the zero somewhat more than normally occurs. Since this term changes sign with polarity, the converter will have a tendency to keep the current sign at zero input.

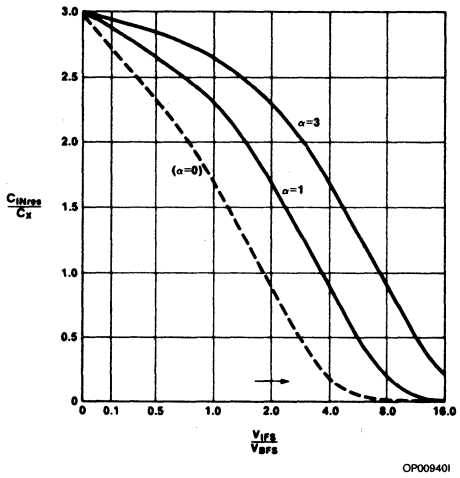

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Figure 10: Auto-Zero Loop Residual vs. Integrator/Buffer Swing and Capacitor Ratios (worst case)

The effects of noise should be mentioned here. The worst case value of residual shown in Figure 10 assumes a very gradual approach to equilibrium, and any noise spike causing the reading to flash to the next value will destroy this carefully established residual value! Thus, for any system with noise of 1/3 count or more, the effect is greatly reduced, and even 1/10 count of noise will restrict the actual hysteresis value found in practice. The detailed analysis of the auto-zero residual problem in the presence of appreciable noise is left as an exercise for the masochist.

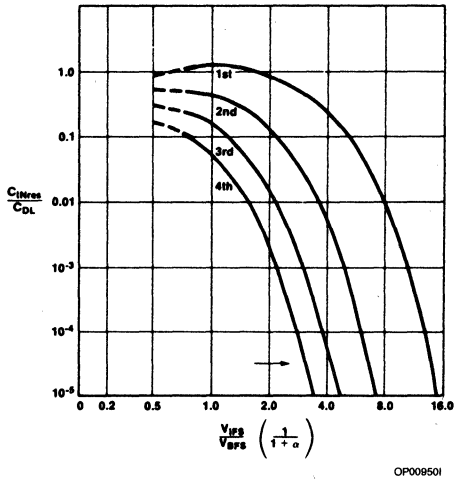

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Figure 11: Auto-Zero Loop Residual vs. Integrator/Buffer Swing for Overload and Capacitor Ratio

For overrange conditions, the controlling equation is (4.5) with the appropriate substitutions for the count ratios. Specifically, putting c_{OR} for the count-equivalent value of the overrange above full scale, and ignoring c_D, we obtain:

$$C_{INres} = 3\left(\frac{V_{IFS}}{V_{BFS}}\right)\left(\frac{C_{OR}}{1+a}\right)\exp\left[-\frac{V_{IFS}}{V_{BFS}}\cdot\frac{1}{1+a}\right] \quad \textbf{(4.9)}$$

This is plotted in Figure 11, and shows the very strong dependence on the integrator to buffer swing ratio. The direction is the opposite of that for the post-zero-crossing residual, as well as being normally much larger. A positive overrange on one reading will tend to make the next reading(s) too negative, and vice versa. The influence on second and even subsequent readings after an overrange can also be appreciable in some cases. The miss-charge trapped on the auto-zero capacitor during the first conversion after an overrange will still be there at the end. If this conversion is in-range, we may ignore c_X and c_D and just consider the continuation of the exponential decay during the following Auto-Zero phase: Thus, at the beginning of the second conversion, the residual will have been reduced to:

$$C_{AZres\ 2} = C_{AZres}\ \exp\left[-\frac{C_{AZ}}{C_{INT}}\cdot\frac{V_{IFS}}{V_{BFS}}\cdot\frac{1}{1+a}\right]$$

where C_{AZres} is given by equation (4.4). This will be similar for subsequent in-range conversions. The effect at the input is again increased by the time ratio of DE-integrate and INTegrate, and so we may write, for the effective error at the input on the nth conversion after the overrange:

$$C_{INresn} = \left(1 + \frac{C_{DE}}{C_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)\left(\frac{C_{OR}}{1+a}\right)\left[\exp\left(-\frac{C_{AZ}}{C_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+a}\right)\right]^n \quad \textbf{(4.10)}$$

This also is plotted in Figure 11, for various values of n against $\frac{V_{IFS}}{V_{BFS}} \frac{1}{1+a}$, for worst case conditions (an overload followed by several full scale conversions).

The residual can be reduced for devices, such as the ICL7109, which provide indications of overrange conversions and auto-zero phase (OR and STATUS in the ICL7109) by reducing the integrator time constant during all or part of the Auto-Zero phase after an overrange conversion. This can be done by shorting out all or part of the integrating resistor R_{INT} by a suitable analog switch. A circuit to do this is shown in Figure 12 for the ICL7109. Care should be taken to ensure that the switch does not cause errors due to charge injection into the capacitors when going OFF. Alternatively the clock can be slowed down or stopped, or Run/$\overline{\text{Hold}}$ used to extend the Auto-Zero phase under the same conditions. These techniques are much harder to apply to devices such as the ICL7106/7 which do not provide the necessary signals. Generally, however, these devices are not used in multiplexing applications.

SUMMARY

This note has described the most common behavior patterns that cause concern and/or confusion among users of the ICL7106/7 and similar products, and their origins. Hopefully, it will help alleviate or eliminate any consequent applications problems with this family of devices. Naturally, some parts will not show all of the effects; for instance, the ICL7116/7 and ICL7135 cannot suffer from large common-mode voltages between reference and COMMON, because no such voltage can be applied, and the ICL7135 has a modified auto-zero sequence that alters the residual effects in the Auto-Zero Loop Residual Section.

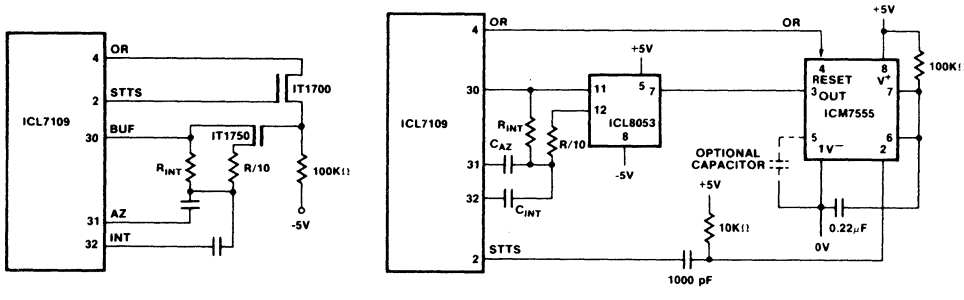


Figure 12: Circuits to Reduce Overrange Residual on ICL7109

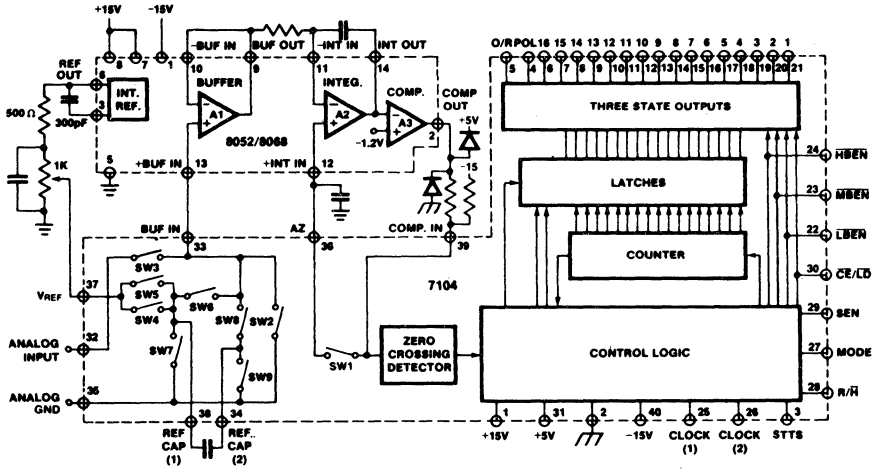
A030
ICL7104 A Binary Output A/D Converter for μProcessors

INTRODUCTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7104-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-zero, Auto-polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external auto-zero capability in preconditioning circuitry, synchronizing external multiplexers, etc., etc. The basic schematic connections are shown in Figure 1.

The chip pair operates as a dual-slope integrating converter. The conversion takes place in three stages, each with their own configuration. In the first, or auto-zero phase (this is also the "idle" condition), the converter self-corrects for all the offset voltages in the buffer, integrator, and comparator. During the second, or input integrate phase, the converter integrates the input signal for a fixed time (2^{15} clock pulses for the -16 part, 2^{13} for -14, 2^{11} for -12). The converter then determines the (average) polarity of the input, and during the third, or deintegrate (alias reference integrate) phase, integrates the reference voltage in the opposite polarity, until the circuit returns to the initial condition. This point is known as the zero-crossing, and terminates the conversion process. The time (number of clock pulses) required to reach zero-crossing is proportional to the ratio of the input signal to the reference. A more detailed discussion of the operation of the dual-slope converter is given in Application Note A017 "The Integrating A/D Converter." Figure 2 shows the basic waveforms of the Integrator.

This application note will first cover the digital interface of the ICL8052(ICL8068)-ICL7104 chip pair to digital systems of various kinds, including microprocessors, using the three state output capabilities (covered in Section 2) and the handshake system built into the 7104 (Section 3). Finally, some (mainly) analog techniques to enhance the system performance in certain applications are covered in Section 4. An Appendix covers a normally undetectable but under some circumstances significant error generated in the auto-zero system.



	OPTION	AZ MIN.	INTEG.	DEINTEG.
	16 BIT	32K	32K	0-64K
PINS 23, 12, 13 NOT CONN.	14 BIT	8K	8K	0-16K
PINS 23, 10, 11, 13, 12 NOT CONN.	12 BIT	2K	2K	0-4K

Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter

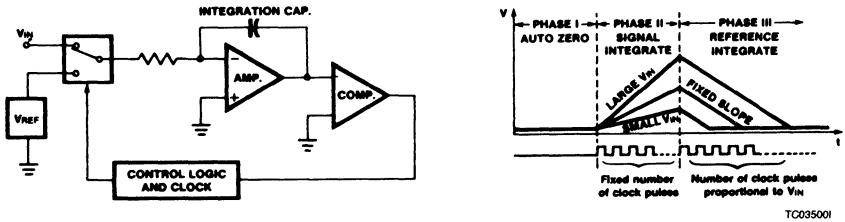


Figure 2: Simplified Dual-Slope Converter and the Three Phases of a Dual-Slope Conversion

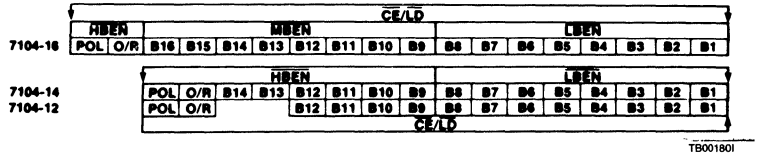


Figure 3: Three State Formats via Disable Pins

DIGITAL INTERFACE

(Without Internal Handshake)

The output format of the ICL7104 is extremely versatile, and includes a full internal handshake capability, which is discussed in the next section. Here we will be concerned only with the "normal" three state output lines. To disable the handshake circuitry, the MODE pin (pin 27) should be tied low (to digital gnd).

In this mode, the most useful output-timing signal is the STaTuS(STTS) line (pin 3), which goes high at the beginning of the signal integrate phase. When zero crossing occurs (or overload detection), new data is latched on the next clock pulse, and ½ clock pulse later, the STTS line goes low. Thus, the new data is stable on this transition. The Run/$\overline{\text{Hold}}$ pin (R/$\overline{\text{H}}$) (pin 28) is also useful for controlling conversions. A more detailed description of the operation of this pin is given in Section 4.B, but it will suffice to say here that if it is high, conversions will be performed continuously, while if it is low, the current conversion will be completed, but no others will start until it goes high again. There are 18 data output lines (16 and 14 on the 14-bit and 12-bit versions), including the polarity and over-range lines. These lines are grouped in sets of no more than 8 for three stated enable purposes, in the format shown in Figure 3, under the control of the byte and chip disable lines shown. To enable any byte, both the chip disable and the corresponding byte disable lines must be low. If all four (three for 7104-14 and -12) disable lines are tied low, all the data output lines will be asserted full time, thus giving a latched parallel output. For a three state parallel output, the three (two) byte disable lines should be tied low, and the chip disable line will act as a normal three state control line, as shown in Figure 4. This technique assumes the use of an 18 (16, 14) bit wide bus, fairly common among minicomputers and larger computers, but still rare among microprocessors (note that "extra" bits can sometimes be sensed as condition flags, etc.). For small words, the bit groups can be enabled individually or in pairs, by tying the chip disable line low, and using the byte disable lines either individually or in any combination as three state control lines, as shown in Figure 5. Several devices can be three stated to one bus by the technique suggested in Figure 6, comparable to row and column selection in memory arrays.

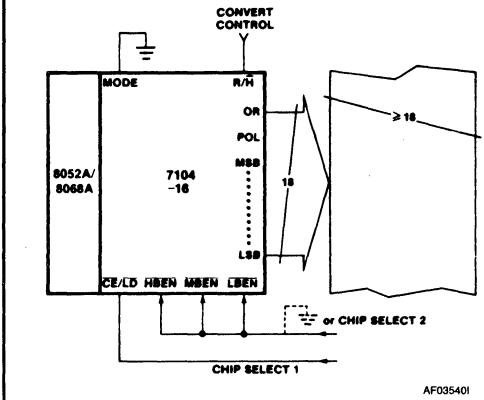


Figure 4: Full 18 Bit Three State Output

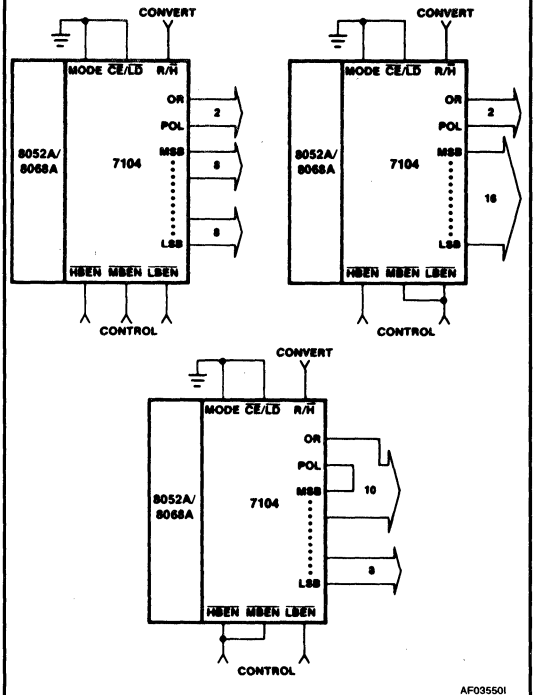


Figure 5: Various Combinations of Byte Disables

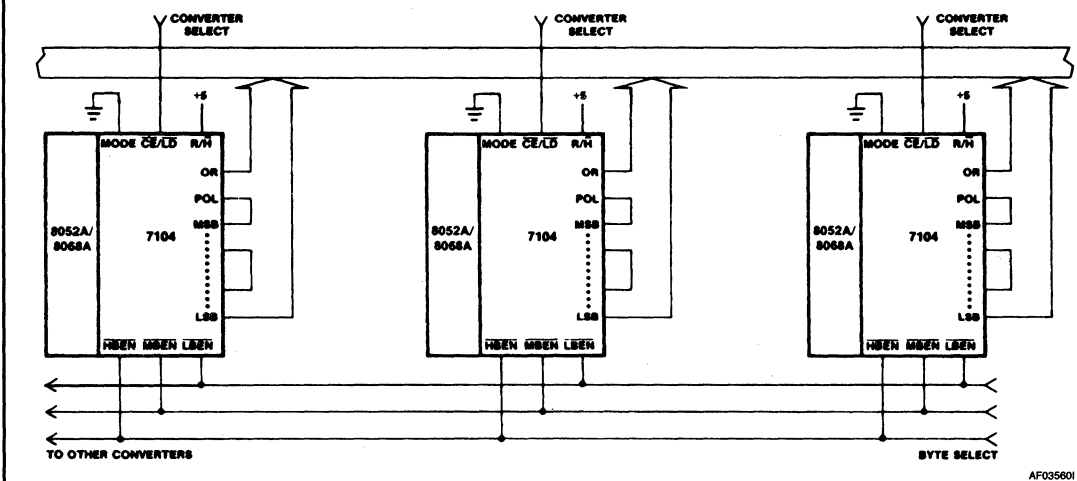


Figure 6: Three Stating Several 7104's to a Small Bus

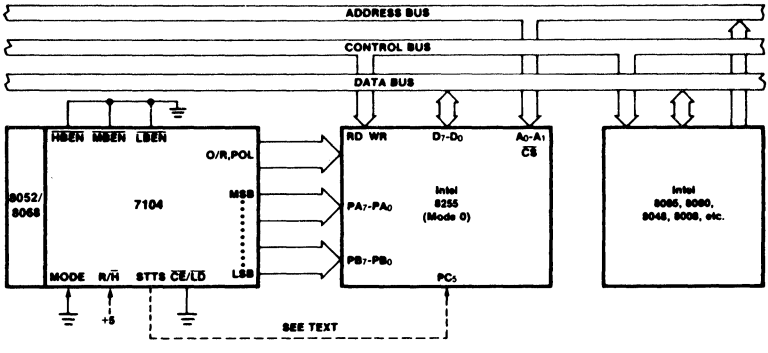


Figure 7: Full Time Parallel/Interface 8052(8068)-7104 to MCS-48, 80/85 Families

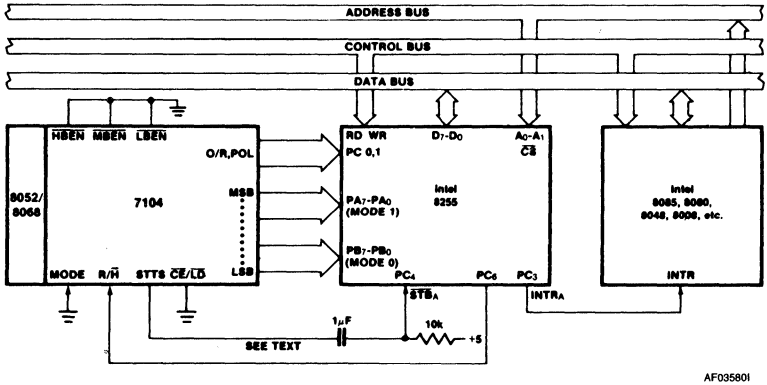


Figure 8: Full Time Parallel Interface 8052(8068)-7104 to *MCS-48, 80/85 Families with Interrupt

Some practical interface circuits utilizing the parallel and three state output capabilities of the ICL7104 are shown in Figures 7 through 13. Figure 7 shows a straightforward application to the Intel *MCS-48, 80, and 85 systems via an 8255 PPI, using full-time parallel output. The I/O ports of an 8155 can be used in the same way. This interface can be used in a read-anytime mode, although there can be timing problems here, since a read performed as new data is being latched in the ICL7104 may lead to scrambled data. (Note that this will occur only very rarely, in proportion to the ratio of setup-skew to conversion times). One way to overcome this problem is to read back the STTS line as well, and if it is high, read the data again after a delay exceeding ½ (converter) clock cycle. If STTS is now low, the second reading is correct, if it is still high, the first reading was correct (note that data never changes when STTS is low, and it goes low ½ clock cycle after data update occurs). Alternatively, the problem is completely avoided by using a read-after-update mode, as shown in Figure 8. Here the high to low transition of STTS triggers a "read data" operation through the MCS-8 Interrupt system. This application also shows the R/$\overline{H}$ pin being used to initiate conversions under software control. If continuous conversions are desired, R/$\overline{H}$ may be held high, and if the maximum possible conversion rate is desired, R/$\overline{H}$ may be tied to clock out (see Section 4.B below).

*MCS is a registered trademark of Intel Corporation, Santa Clara, Ca.

A similar interface to the Motorola MC6800 system is shown in Figure 9. Since the maximum input-port count here is only 16, while the 16-bit ICL7104 has 18 outputs, control register A is used to input the two extra bits. The high to low transition of the STTS pin enables the two high bits, clocking the two interrupt flags in Control Register A if they are negative. A pullup resistor is needed on CA1, though CA2 has one internally. The same transition causes an interrupt via Control Register B's CB1 line. It is important to ensure that the software interrupt routine reads control register A before reading data port A, since the latter operation will clear the interrupt flags. Note that CB2 controls the R/$\overline{H}$ pin through control register B, allowing software initiation of conversions in this system also. Naturally, the 14 and 12 bit versions of the ICL7104 avoid this problem since 16 or fewer bits need to be read back. Since the MOS Technology MC650X microprocessors are bus-compatible with the MC6800's the same circuit can be used with them also.

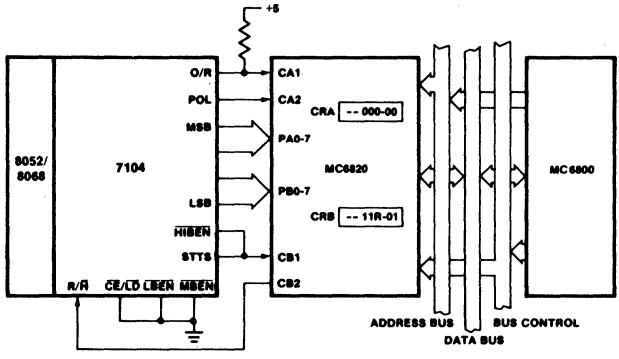


Figure 9: Parallel Interface from 7104 to MC 6800 Family (also MCS650X Family)

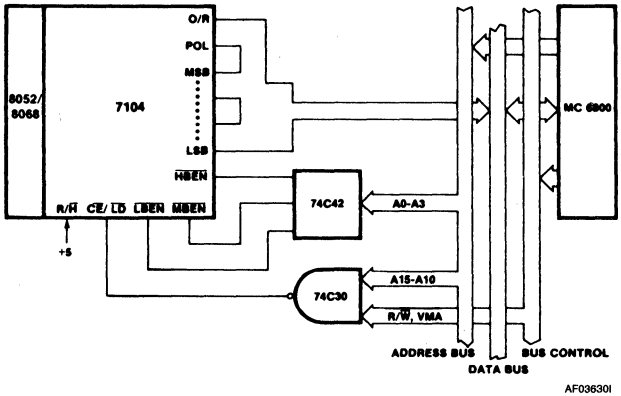


Figure 10: Direct 8052(8068)/7104 to MC6800 Microprocessor Interface

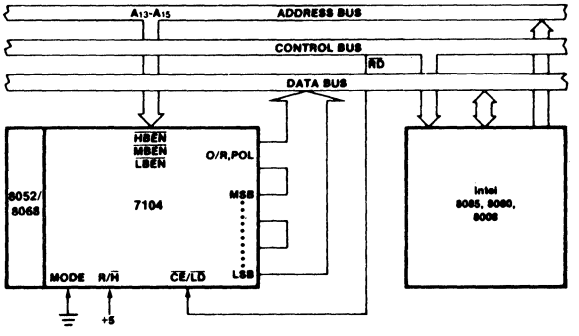


Figure 11: Direct Connection of 8052(8068)/7104 to MCS-80/85 System

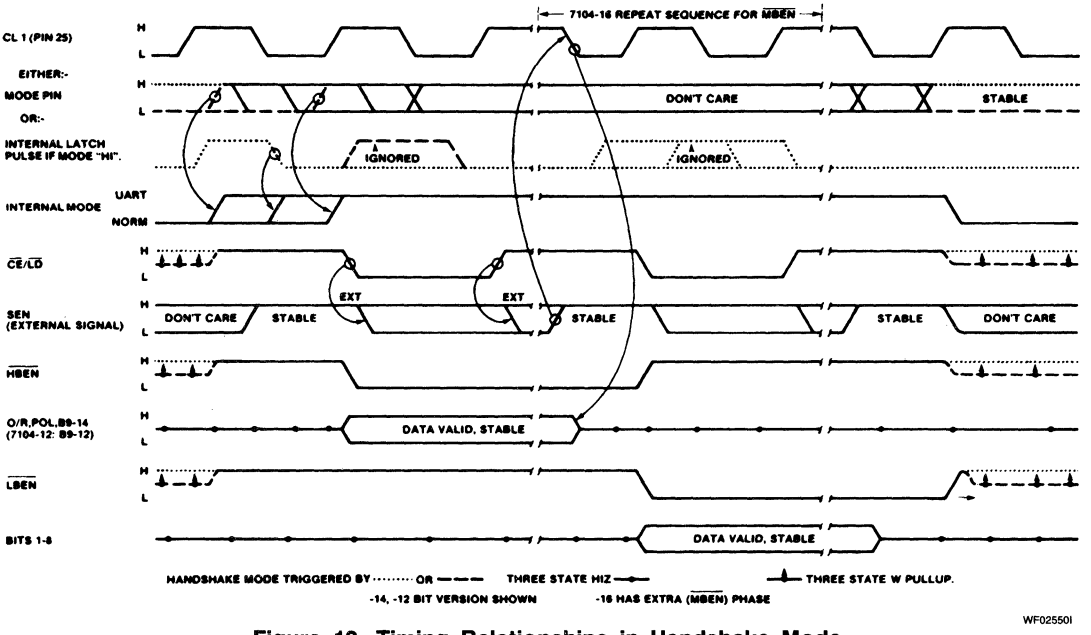


Figure 12: Timing Relationships in Handshake Mode

It is possible using the three state output capability, to connect the ICL7104 directly onto many microprocessor busses. Examples of this are shown in Figures 10 and 11. It is necessary to consider the system timing in this kind of application, and careful study should be made of the required set-up times from the microprocessor data sheets.

Note also the drive limitations on long busses. Generally this type of circuit is only favored if the memory peripheral address density is low, so that simple redundant address decoding can be used. Interrupt handling can require multiple external components also, and use of an interface device is normally advisable if this is needed.

HANDSHAKE MODE INTERFACE

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the

handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

During handshake operations, the various "disable" pins become output pins, generating signals used for the handshake operation. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CL1 (pin 25) clock edge, the corresponding byte disable line goes low, and the Chip Disable/Load line (pin 30) ($\overline{CE}/\overline{LD}$) goes low for one full clock pulse only, returning high.

On the next falling CL1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte disable pin will be cleared high, and (unless finished) the $\overline{CE}/\overline{LD}$ and the next byte disable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte disable pin is low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip disables will be three stated off, if the MODE pin is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 12.

This configuration allows ready interface with a wide variety of external devices. For instance, external latches can be clocked on the rising edge of $\overline{CE}/\overline{LD}$, and the byte disables can be used to drive either load enables, or provide data identification flags, as shown in Figure 13.

More usefully, the handshake mode can be used to interface with an 8-bit microprocessor of the MCS-8 group (eg. 8048, 8080, 8085, etc.) as shown in Figure 14. The handshake operation with the 8255 Programmable Peripheral Interface (PPI) is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send ENable pin, and driving its strobe with the $\overline{CE}/\overline{LD}$ line. The internal control register of the PPI should be set in mode 1 for the port used. If the 7104 is in handshake mode, and the 8255 IBF is low, the next word will be presented to the chosen port, and strobed. The strobe will cause IBF to rise, locking the three stated byte on. The PPI will cause a program interrupt in the MCS-8 system, which will result (after the appropriate program steps have been executed) in a "read" operation. The byte will be read, and the IBF reset low. This will cause the current byte disable to be dropped, and the next (if any) selected, strobed, etc., as before. The interface circuit as shown has the MODE pin tied to a control line on the PPI. If this bit is set always high (or mode is tied high separately), every conversion will be fed into the system (provided that the three interrupt sequences take less time than one conversion) as three 8-bit bytes; if this bit is normally left low, setting it high will cause a data transmission on demand. The interrupt routine can be used to reset the bit, if desired. Note also that the R/$\overline{H}$ pin is also shown tied to a control bit so that conversions can be performed either continuously or on demand under software control. Note that one port is not used here, and can service another peripheral device. The same arrangement can again be used with an 8155 I/O port and control lines.

Similar methods can be used with other microprocessors, such as the MC6800 or MCS650X family, as shown in Figure 15, and the Intel MCS4/40 family, as shown in Figure 16. These both operate almost identically to the method described above, except that in the former both R/$\overline{H}$ and MODE are shown tied high, to avoid using a full port for only two lines. Any 8-bit or wider microprocessor (or minicomputer), or narrower devices with 8-bit wide ports (most 4-bit devices have 8-bit wide ports available) can be interfaced in a handshake mode with a minimum of additional hardware, frequently none at all.

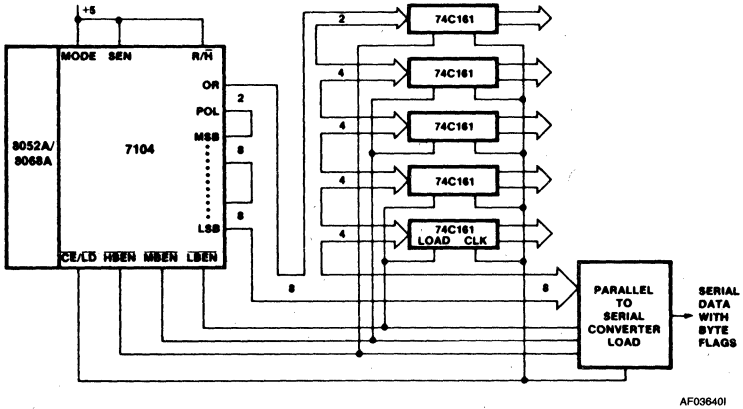


Figure 13: Use of Byte Disable Lines as Flags or for Loading

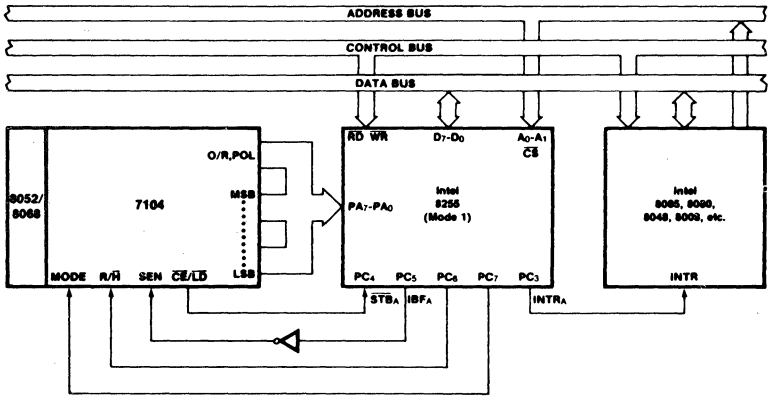


Figure 14: 8052A(8068A)-7104 to MCS-48, -80, or -85 Handshake Interface

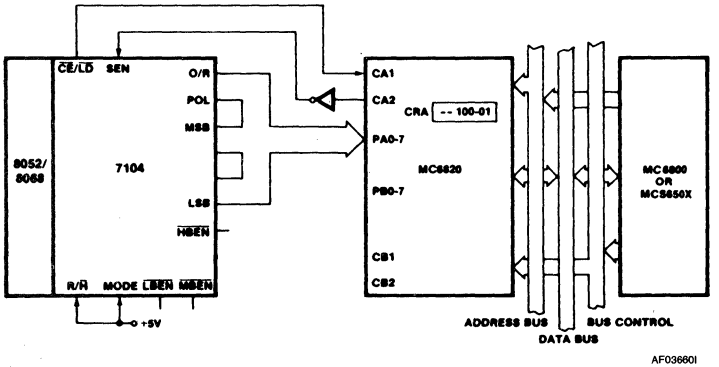


Figure 15: 8052(8068)/7104 to MC6800 or MC650X Microprocessor With Handshake

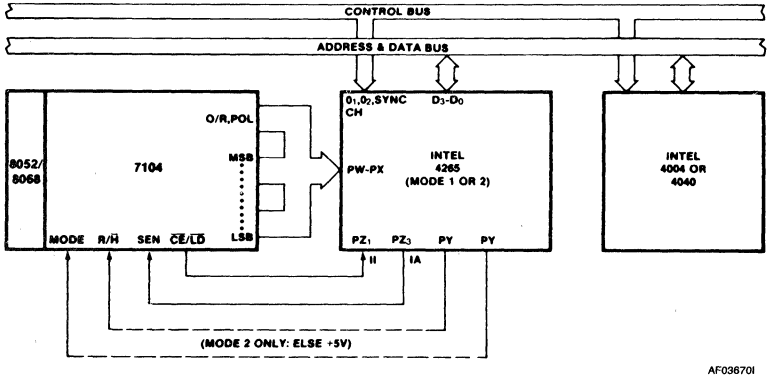


Figure 16: 8052A-7104 to MCS4/40 Microprocessor With Handshake

The handshake mode can also be used to interface with industry-standard UARTs, such as the Intersil IM6402/3 and the Western Digital TR1602. One method is shown in Figure 17. The arrangement here is such that if the UART receives any word serially down the Receiver Register Input line (RRI) the Data Received flag (DR) will be set. Since this is tied to the MODE pin, the current result will be loaded, full handshake style as before, into the transmitter buffer register, via the Transmitter Buffer Register Empty flag (TBRE) and the TBR=usL=kooad lines. The UART will thus transmit the full 18 (16, 14) bit result in 3 (2, 2) 8-bit words, together with the requisite start, stop and parity bits, serially down the Transmitter Register Output (TRO) line. The DR flag is reset via DR$\overline{R}$eset, here driven by a byte disable line. If we use DR to drive R/$\overline{H}$ instead, and use the received data word to drive a multiplexer, as shown in Figure 18, the multiplexer address sent to the UART will be selected, and a conversion initiated of the corresponding analog input. The result will be returned serially if the MODE pin is tied high. Thus a complete remote data logging station for up to 256 separate input lines can be controlled and readback through a three line interface. By adding a duplex or modem, telephone or radio link control is possible. (For a fuller discussion of this technique, see Application Note A025, Building A Remote Data Logging Station).

Alternatively, the data word could be used to select one of several A/D converters, as shown in Figure 19. The unselected A/Ds all have three stated disable lines as well as data lines, so provided only one device is selected at a time, no conflicts will occur. (Note that byte disable lines are internally pulled-up when not active, so $\overline{CE}/\overline{LD}$ has no effect on unselected converters). Naturally, care must be taken to avoid double selection errors in the data word, or an address decoder used. This technique could also be used to poll many stations on a single set of lines, provided that the TRO outputs are either three state or open collector/drain connections, since only that UART receiving an address that will trigger an attached converter will transmit anything.

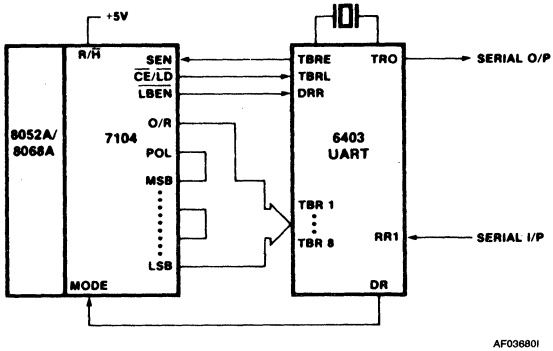


Figure 17: 8052(8068)/7104 Serial Interface Using UART

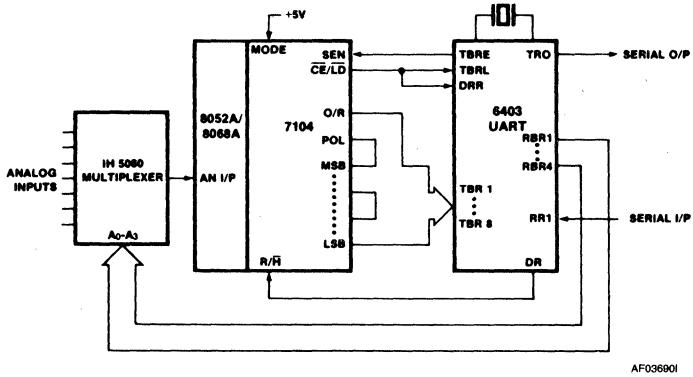


Figure 18: 8052(8068)/7104 Serial Interface Using UART and Analog Multiplexer

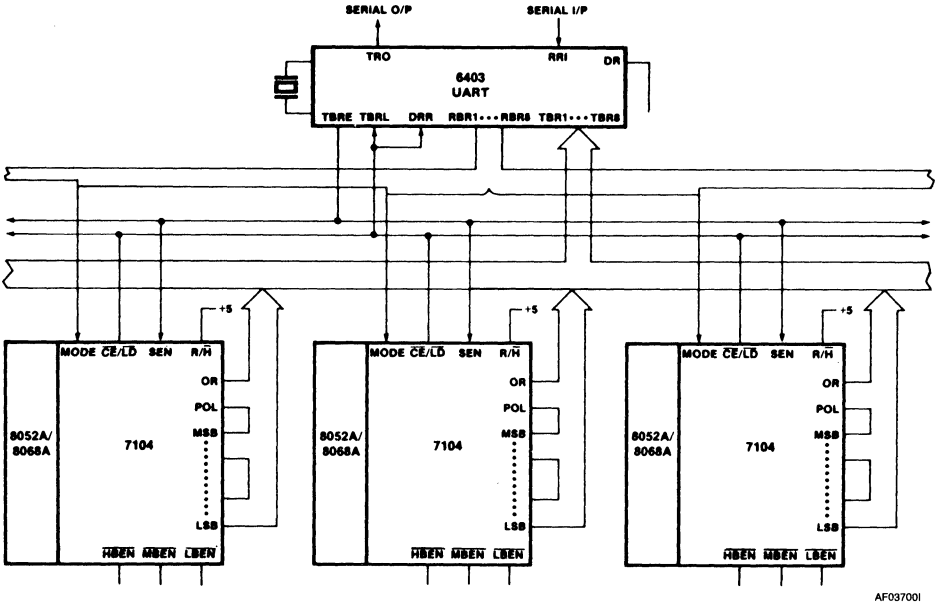


Figure 19: Multiplexing Converters Through the Mode Pin

MISCELLANEOUS TECHNIQUES FOR PERFORMANCE ENHANCEMENT

This section covers a few techniques, primarily analog, that can be used to enhance the performance of the ICL8052 (ICL8068)/ICL7104 chip pair for certain applications. Section 4.A. deals with buffer gain, for sensitivity increases of up to about 5 or 10 to 1, Section 4.B. with a special interconnection to allow the maximum rate of conversion with lower-valued inputs, and Section 4.C. external auto-zero for extending the benefits of auto-zero operation to preamplifiers, etc., to cover specialized signal processing or sensitivity enhancement by 10-100 to 1.

Buffer Gain

One of the significant contributions to the effective input noise voltage of a dual slope integrator is the so called auto-zero noise. At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. Although the open loop band width of the auto-zero loop is not wide, the gain from the input is very high, and the resulting closed loop band width to buffer noise is fairly wide. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system (see also the appendix). The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 22. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. Considerable care has been taken with the internal design of the ICL7104 and the ICL8068 to minimize the internal thermoelectric effects, but device dissipation should be minimized, and the effects of heat from adjacent (and not-so adjacent) components must be considered to achieve full performance at this sensitivity level.

Minimal Auto-Zero Time Operation

The R/$\overline{H}$ pin (pin 28) can be used in two basic modes. If it is held high, the ICL7104-16 will perform a complete conversion cycle in 131K clock counts (strictly 2^{17}), regardless of the result value (for the −14, 2^{15} counts, −12, 2^{13} counts).

If, however, the R/$\overline{H}$ pin (ever) goes low between the time of the zero-crossing and the end of a full $2^{16}/^{14}/^{12}$ count reference integrate phase, that phase is immediately terminated. If it is then held low, the 7104 will ensure a minimum auto-zero count (of $2^{15}/^{13}/^{11}$ counts) and then wait in auto-zero until the R/$\overline{H}$ pin goes high. On the other hand, if it goes high immediately subsequent to this minimal auto-zero count, the 7104 will start the next conversion after the least permissible time in auto-zero; i.e., at the maximum possible rate. The necessary "activity" on the R/$\overline{H}$ pin can be readily provided by tying it to the clock out pin (pin 26). Obviously under these conditions, the conversion cycle time depends on the result. Also note the scale factor and auto-zero effects covered in the Appendix.

External Auto-Zero

In many systems, signal conditioning is required in front of the converter for preamplification, filtering, etc., etc. With the exception of buffer gain, discussed in Section 4.A. above, it is generally not possible to include these conditioning circuits in the auto-zero loop. However, a sample-and-difference circuit keyed to the auto-zero phase can be used to eliminate offset and similar errors in preamplifiers, multiplexers, etc. A suitable circuit for a simple system is shown in Figure 21. The ICL8053 is used as a switch here primarily because of its extremely low charge injection (typically well below 10pC), even though it does limit the analog swing to ±4V. The use of an IH191 or IH5043 avoids this restriction, but increases the charge injection. The circuit of Figure 22 includes some balancing, but still injects typically 60pC (or 150pC for a DG191). Note that all these circuits have some sensitivity to stray capacitance at the converter input node. The amplifying or conditioning stages indicated in both these circuits must be capable of passing the chopping frequency with small enough delay, rise time, and overshoot to lead to insignificant error. Filtering should be done before or after the switching devices. Note also that although the input signal is still integrated over the normal time period, the input reference level is not. The time constant of the hold capacitor charging circuit should take noise and interference effects into consideration.

For a multiplexed input system, an arrangement similar to that of Figure 23 may be needed with individual preconditioning amplifiers, and Figure 24 with a common preconditioning amplifier. Note that in both of these cases, the capacitor may be charged to different voltages on each channel. By putting a capacitor in each line of Figure 23, the capacitor charging transients are eliminated, but the multiplexer capacitance becomes an important source of stray capacitance.

SUMMARY

The list of applications presented here is not intended to be nor can it be, exhaustive, but is intended to suggest the wide range of possible applications of the ICL8052(ICL8068)/ICL7104 chip pair in A/D conversion in a digital environment. Many of the ideas suggested here may be used in combination; in particular, all the digital concepts discussed in Sections 2 and 3 can be used with any of the analog techniques outlined in Section 4, and many of the uses of the R/$\overline{H}$ and MODE pins can be mixed.

Some other applications bulletins that may be found useful are listed here:

A016 Selecting A/D Converters
A017 The Integrating A/D Converter
A018 "Do's and Dont's of Applying A/D Converters"
A025 Building a Remote Data Logging Station
R005 Interfacing Data Converters & Microprocessors Electronics, Dec. 9, 1976.

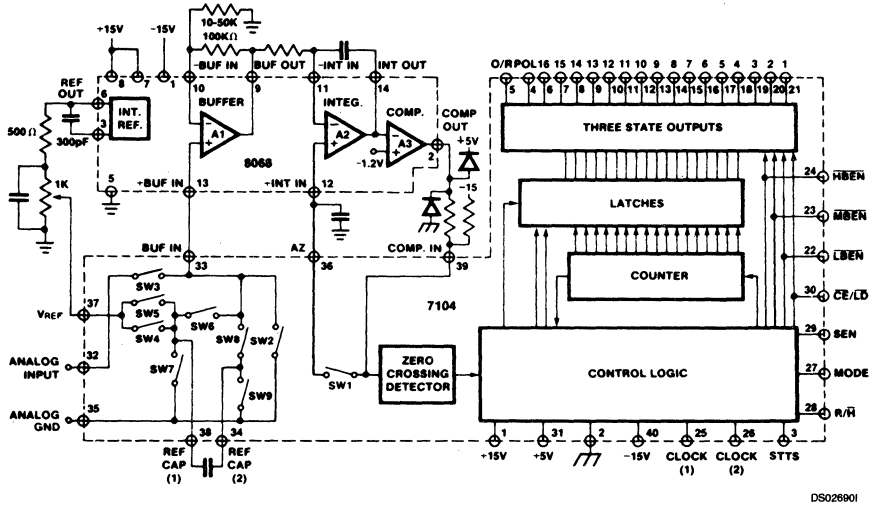
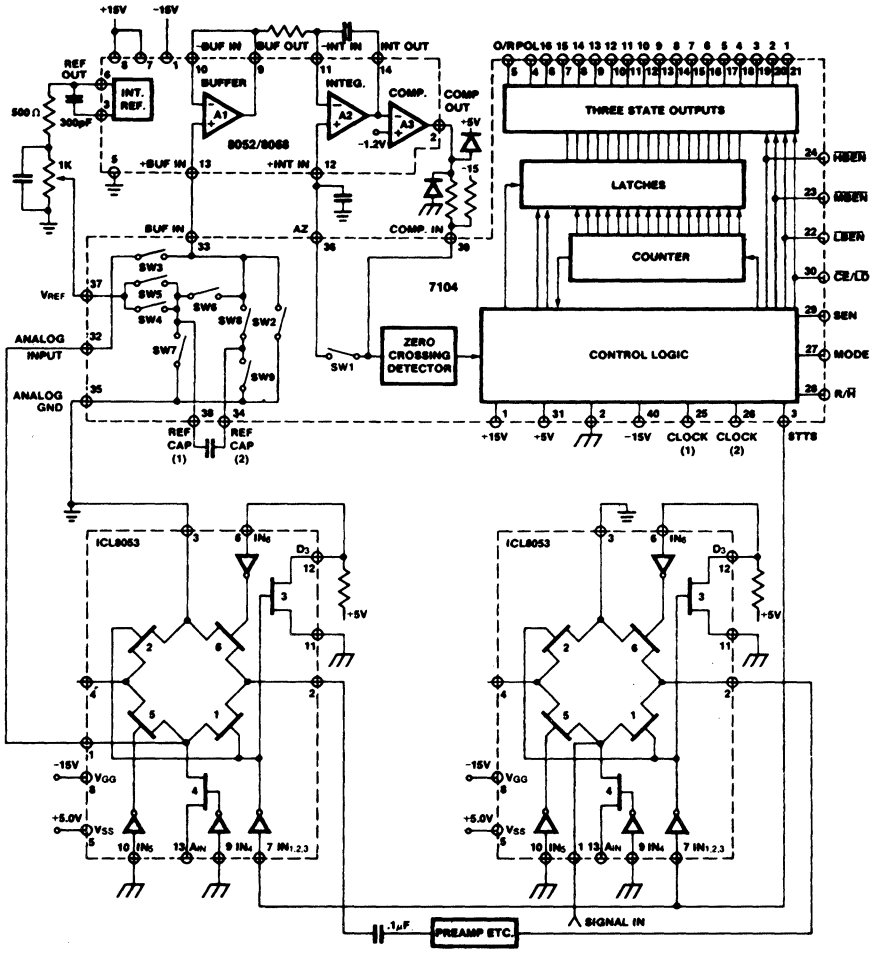


Figure 20: 8068/7104 Converter With Buffer Gain



DS02700I

Figure 21: External Auto-Zero System Using 8053 Switches

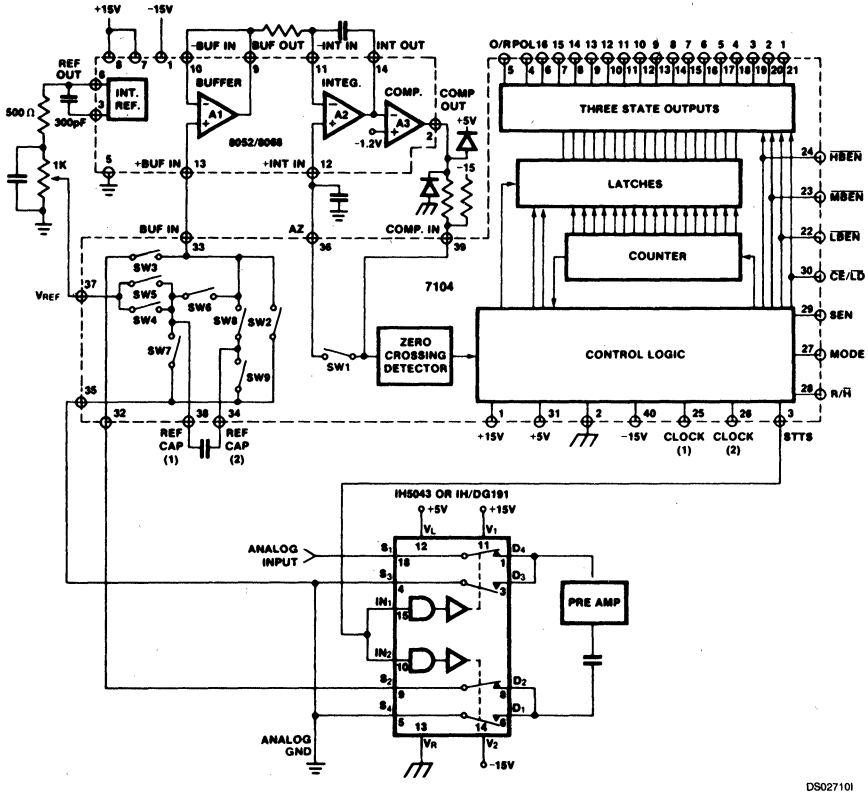


Figure 22: External Auto-Zero System for Large Signals Using IH5043 or Equivalent

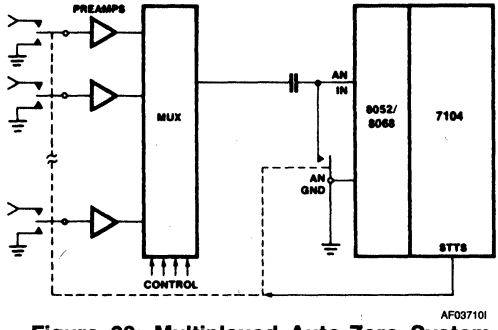


Figure 23: Multiplexed Auto-Zero System With Individual Preamps

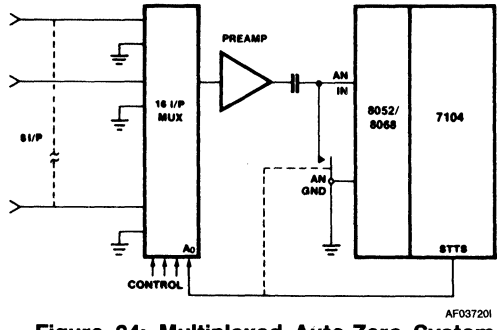


Figure 24: Multiplexed Auto-Zero System With Common Preamp

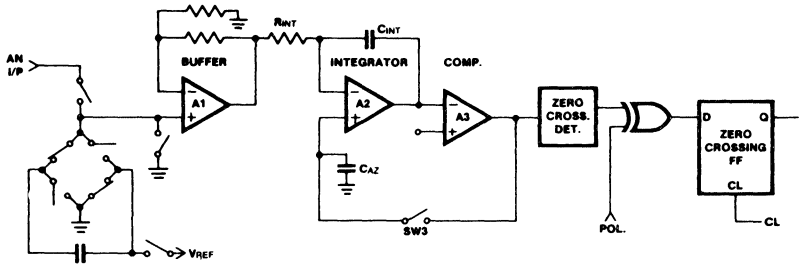


Figure A1: The Analog System

APPENDIX A: The Auto-zero Loop Residual; A Relatively Complete Discussion for those with Strong Heads

The relevant circuit to be discussed is shown in Figure A1 and the major cycle waveforms in Figure A2. Let us first assume that the prior auto-zero cycle has been indefinitely long, or is otherwise ideal, so that the conversion starts with no residual error on the auto-zero capacitor. The integrate and deintegrate cycles will be classically perfect to the point at which a zero crossing actually occurs (at the output of the integrator). However, from this point two delays occur; first the comparator output is delayed (due to comparator delay) and secondly the zero crossing is not registered until the next appropriate clock edge. (For further discussion of this, see Application Note A017). At this point, the circuit is returned to the auto-zero connection (logic and switch delays may be absorbed in comparator delay as far as our discussion is concerned). The net result is that the integrator output voltage will have passed the zero-crossing point by an amount given by

$$V_{Ires} = \pm V_{IFS}\left(\frac{C_D + C_X}{C_{FS}}\right) \text{ where } 0 \le C_X \le 1 \qquad \textbf{(A1)}$$

is the variable delay, where C_D is the fixed delay, C_{FS} is the full scale count in units of clock pulse periods, and V_{IFS} is the full scale integrator swing in volts.

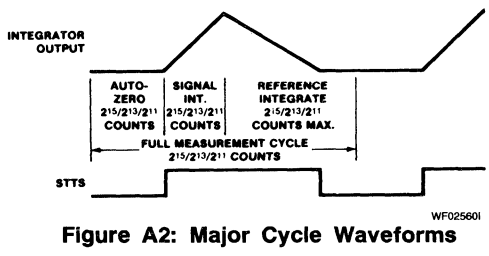


Figure A2: Major Cycle Waveforms

The range of this residual voltage corresponds to the integrator swing per count, and in independent of input value, except for polarity. The immediate effect of closing the auto-zero loop may be seen by examining Figure A3. We may consider the comparator as acting as an op-amp under these conditions: the voltage across the auto-zero impedance is high, and the (nonlinear) impedance is low; on the other hand, the initial voltage across the integrating resistor is zero. Thus the auto-zero capacitor will be charged rapidly to exactly cancel the residual voltage, as shown in Figure A4.

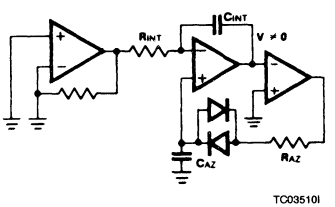


Figure A3: Analog System During Auto-Zero

The output of the integrator is now at the correct position, but the two inputs are not. The residual voltage will decay away with a time constant controlled by the integrating resistor and capacitor, while the auto-zero capacitor is easily kept in step owing to the high comparator gain. Thus at the end of the auto-zero time, $t_{AZ} = C_{AZ}\, t_{cp}$, the residual will be reduced to:

$$V_{AZres} = V_{Ires}\ \exp\left(\frac{-C_{AZ}\ t_{cp}}{R_{INT}\ C_{INT}}\right)$$

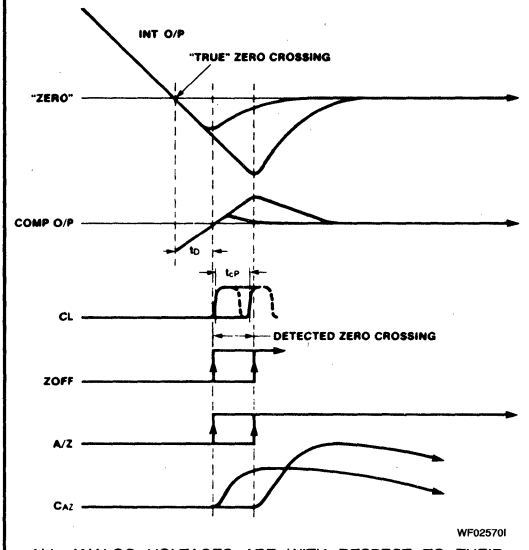
$$= V_{IFS}\ (C_X + C_D)\frac{1}{C_{FS}}\ \exp\left(\frac{-C_{AZ}\ t_{cp}}{R_{INT}\ C_{INT}}\right) \qquad \textbf{(A2)}$$

Now $R_{INT}C_{INT}$ is controlled by the buffer swing, V_{BFS}, the integrator swing, V_{IFS}, and the integration time $t_{INT} = C_{INT}\ t_{cp}$, so that

$$V_{BFS}/R_{INT}\cdot t_{INT} = C_{INT}\ V_{IFS}, \text{ or } R_{INT}\ C_{INT}$$

$$= C_{INT}\ \frac{V_{BFS}}{V_{IFS}}\ t_{cp}$$

$$\text{and } V_{AZres} = V_{Ires}\left(\exp -\frac{C_{AZ}V_{IFS}}{C_{INT}V_{BFS}}\right) \qquad \textbf{(A3)}$$



ALL ANALOG VOLTAGES ARE WITH RESPECT TO THEIR "AUTO-ZEROED" VALUE

Figure A4: Waveforms at Beginning of Auto-Zero Interval

This residual voltage on the auto-zero capacitor effectively increases the magnitude of the input voltage as seen on the output of the buffer. Thus, converting this voltage to count-equivalents,

$$C_{AZres} = \frac{V_{AZres}}{V_{BFS}} \cdot C_{FS}$$

$$= \frac{V_{IFS}}{V_{BFS}} (C_X + C_D) \exp\left(-\frac{C_{AZ}}{C_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}}\right) \quad \textbf{(A4)}$$

Since this voltage also subtracts from the reference, its effect at the input is magnified in the ratio

$$C_{INres} = C_{AZres}\left(\frac{C_{INT} + C_{DE}}{C_{INT}}\right) \text{ so that}$$

$$C_{INres} = \left(1 + \frac{C_{DE}}{C_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)(C_X + C_D) \exp\left(-\frac{C_{AZ}}{C_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}}\right) \quad \textbf{(A5)}$$

Note that C_{DE} is equal to the displayed result.

Two things should be noted here. First, this residual acts to increase the input voltage magnitude, and secondly, a small increase in input voltage tends to decrease the magnitude of the residual (until the result count changes). These effects lead to "stickiness" in the readings; suppose, in a noise-free system, that the input voltage is at a level where the residual is a minimum; the detected zero crossing follows the true one as closely as possible. A minute increase in input voltage will cause the zero crossing to be detected one pulse later, and the residual to jump to it's maximum value. The effect of this is a small increase in the apparent input voltage; thus if we now remove the minute increase, the residual voltage effect will maintain the new higher reading; in fact we will have to reduce the input voltage by an amount commensurate with the effective residual voltage to force the reading to drop back again to the lower value. In more detail, we should consider the equilibrium conditions on the auto-zero capacitor. Clearly, the voltage added at the end of reference integrate must just balance that which decays away during the auto-zero interval. So far the relationships we have developed have assumed a zero residual before the conversion, but clearly in the equilibrium condition the residual given by equation (A4) remains, and at the end of conversion, the new amount, given by equation (A1), is added to this, so we start the "auto-zero decay" interval with

$$C_{Ires} = C_{AZres} + \frac{V_{IFS}}{V_{BFS}} (C_X + C_D) \quad \textbf{(A6)}$$

By combining equations (A4) and (A6) we find, for the equilibrium condition,

$$C_{AZres} = \pm\frac{V_{IFS}}{V_{BFS}} (C_X + C_D) \left[\exp\left\{+\frac{C_{AZ}V_{IFS}}{C_{INT}V_{BFS}}\right\} - 1\right]^{-1}$$

Once again, the effect of this at the input is multiplied by the ratio of total input integrate times, so that, under equilibrium conditions,

$$C_{INres} = \pm\frac{V_{IFS}}{V_{BFS}}\left(1 + \frac{C_{DE}}{C_{INT}}\right)(C_X + C_D)\left[\exp\left\{\frac{C_{AZ}\ V_{IFS}}{C_{INT}V_{BFS}}\right\} - 1\right]^{-1} \quad \textbf{(A7)}$$

Those expert at skipping to the end of the difficult bit will recognize that as the final equation, in terms of complexity. So let us now see what it means. Clearly, the error term is greater, the larger $\frac{C_{DE}}{C_{INT}}$, and the smaller $\frac{C_{AZ}}{C_{INT}}$. For the ICL7104 combinations, (and also the ICL7103, and the data sheet systems for the ICL8053 pairs), these are both worst case near full scale input, where $\frac{C_{DE}}{C_{INT}} \approx 2$ and $\frac{C_{AZ}}{C_{INT}} \approx 1$. (Note that the minimum auto-zero time technique of section 4B will make $\frac{C_{AZ}}{C_{INT}} = 1$ for all input values). Substituting these, we find the worst case

$$C_{INres} \simeq \pm\frac{V_{IFS}}{V_{BFS}} (3)(C_X + C_D) \left[\exp\left(\frac{V_{IFS}}{V_{BFS}}\right) - 1\right]^{-1} \quad \textbf{(A8)}$$

Recall the C_D is fixed; and C_X must be between 0 and 1. The expression is now a function purely of the ratio of integrator and buffer full scale swings; the relationship is plotted in Figure A5, and shows the desirability of keeping the integrator swing higher than the buffer swing. Note also that the comparator delay (C_D in equation (A8)) is also effectively enhanced. This has the effect of shrinking the zero somewhat more than normally occurs. Since this term changes sign with polarity, the converter will have a tendency to keep the current sign at zero input.

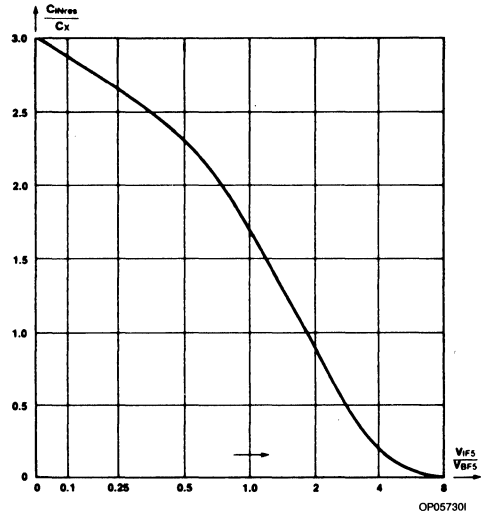


Figure A5: Auto-Zero Loop Residual vs. Integrator/Buffer Swing Ratio

The effects of noise should be mentioned here. The worst case value of residual shown in Figure A5 assumes a very gradual approach to equilibrium, and any noise spike causing the reading to flash to the next value will destroy all this carefully established residual value! Thus for any system with noise of ~ 1/3 count or more, the effect is greatly reduced, and even 1/10 count of noise will restrict the actual hysteresis value found in practice. The detailed analysis of the auto-zero residual problem in the presence of appreciable noise is left as an exercise for the masochist.

AO21
Power D/A Converters Using The IH8510

THE POWER D/A CONVERTER

Intersil has introduced a family of power amplifiers — the IH8510 family. These power amplifiers have been specifically designed to drive D.C. servo motors, D.C. linear and rotary actuators, electronic orifice valves and X-Y printer motors. There are three versions presently offered — the IH8510 is specified at 1 amp continuous output with up to ±35V power supplies; the IH8520 is specified at 2 amps continuous output at up to ±35V; finally the IH8530 is a 3 amp version with the same power supply range.

The amplifiers are linear mode types and are basically a power version of the popular 741 differential op amp. The parts are available in 8-pin TO-3 packages. Using ±30V power supplies, the amplifiers are capable of delivering up to ±26V swings into a 10Ω load. The parts are biased Class AB, and have typical no-load quiescent current of 20mA. Frequency response, input offset voltage, input offset, and bias currents are the same as the 741 op amp. All three models can withstand indefinite shorts to ground on the output. When driving a D.C. motor, the amplifiers can also withstand the surges caused by motor lock-up and motor reversal (i.e., while running in one direction, the voltage is suddenly reversed).

The linear nature of these power amplifiers allows them to fit in very well with another Intersil product family — the D/A converter. Intersil has low cost DAC's available — the 7520 series. When a DAC and a power amplifier are combined, one has a very useful building block for control functions, i.e., a digitally programmable power driver. This power DAC can interface directly with microprocessors, UARTS, computers, etc.

DESIGN DETAILS

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 1. The IH8510 power amplifier described in the introduction is driven by the Intersil 7520 monolithic D/A converter.

The 7520 contains the R/2R ladder network and the feedback resistor for proper scaling of the reference input voltage (±10V) and also the SPDT switches (CMOS) for each bit. Figure 2 shows a part of the system (first 4 bits). Note that a permanently biased "on" switch is in series with the 10KΩ feedback resistor. The $R_{DS(on)}$ of this "on" FET is 0.5 x $R_{DS(on)}$ of the Most Significant Bit (MSB) switch to maintain MSB accuracy (gain accuracy) at 25°C and over the temperature range. Since the FET switches are on the same I.C. chip, the temperature tracking is excellent. Actually, the 7520 specifies the temperature coefficient at 2ppm/°C maximum.

The circuit configuration is such that the SPDT switches in series with each 20KΩ resistor never see more than ±25mV; this minimizes DAC errors caused by $I_{D(off)}$ and $I_{D(on)}$ leakages. It also allows the DAC switch to handle ±10V references with only a single +15V power supply. The size of each DAC switch is scaled so that it does not distort the gain for each bit, i.e., the MSB switch $R_{DS(on)}$ is 25Ω; the next switch $R_{DS(on)}$ is 50Ω; the next is 100Ω, etc.

A summing amplifier is shown between the 7520 and the IH8510 in Figure 1. This apparently redundant amplifier is used to separate the gain block containing the 7520 on-chip resistors from the power amplifier gain stage whose gain is set only by external resistors. This approach minimizes drift since the resistor pairs will track properly.

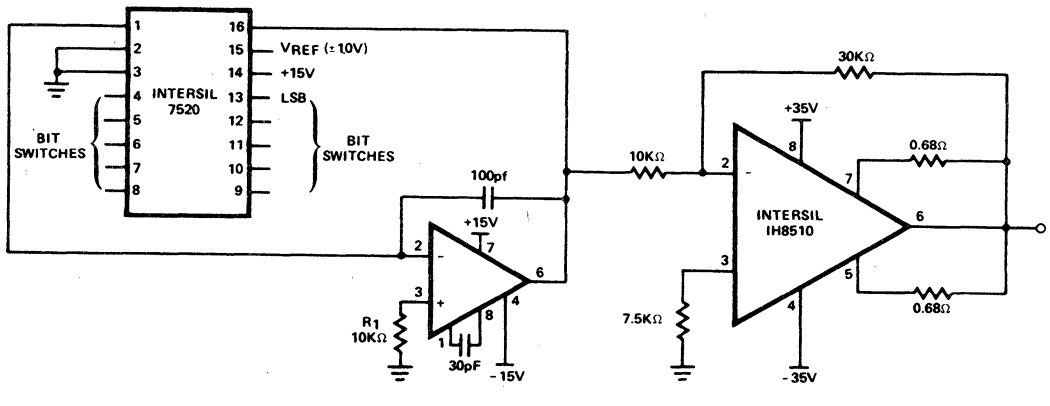


Figure 1: The Basic Power DAC

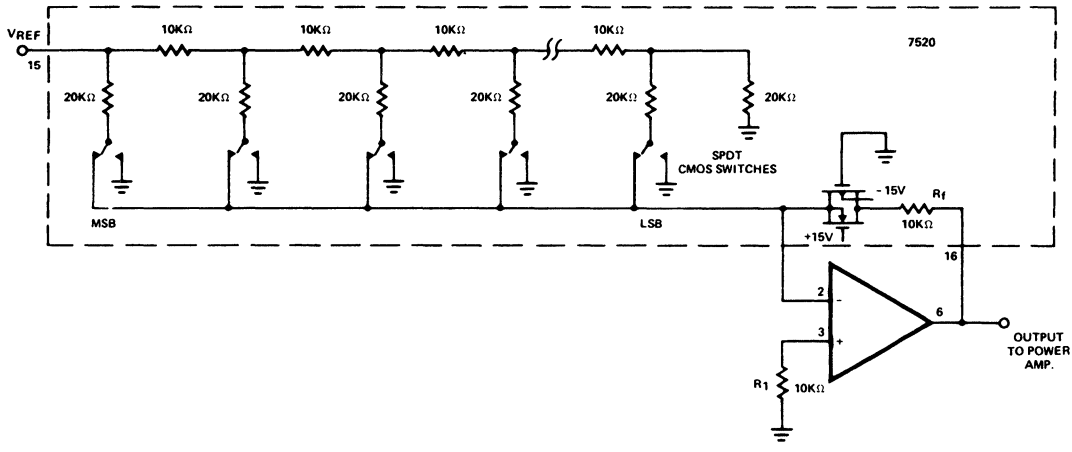


Figure 2: D/A Converter Details

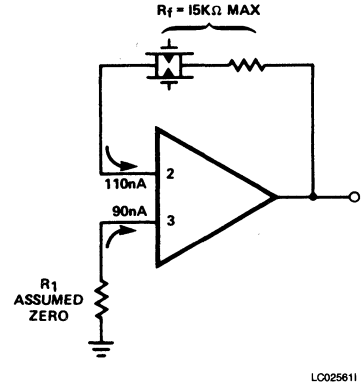


Figure 3: Worst Case Error Due to Input Current

One of the decisions the user will have to make is the choice of summing amplifier. For 8 bit accuracy with 25 volt output swings, a ½ LSB is equivalent to approximately 50mV. The worst case errors introduced by the op-amp (i.e., the cummulative effects of I_B, and I_{OS}, and $\Delta V_{OS}/\Delta T$) should therefore be significantly less than 50mV.

The initial offset voltage of the buffer amplifier adds to that of the IH8510, and is multiplied by three before appearing at the output. Depending on the application, it may be desirable to null out this offset. The nulling should be done at the buffer in the manner recommended for the amplifier being used.

In the majority of DAC applications, a full scale output adjustment is necessary. For example, set point controllers in servo systems are typically required to have an error no greater than 0.3% of full scale reading. This can be achieved by either adjusting the reference voltage up or down from a nominal 10.000V, or by using a potentiometer in the amplifier feedback network, as shown in Figure 4. The potentiometer should be a low temperature coefficient type.

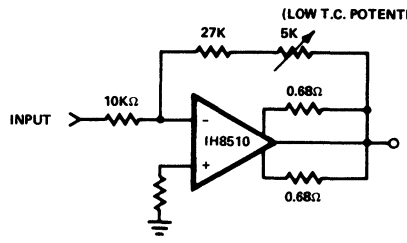


Figure 4: Full Scale Gain Adjustment

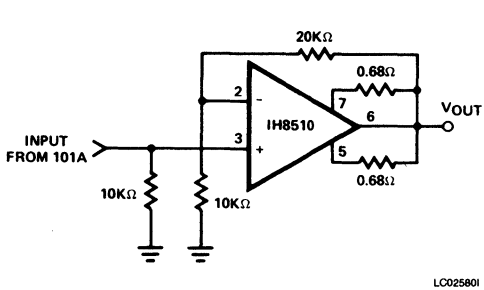


Figure 5: Non-inverting Gain Connection

A final important note on the 7520 interface concerns the connection between Pin 1 of the DAC and the summing

junction of the amplifier with an AC gain of 50,000 or better, so stray capacitance should be minimized otherwise instabilities and poor noise performance will result.

The 0.68Ω resistors from Pins 5 and 7 to Pin 6 are used to set current limits for the power amp. These are safe area limiting structures which follow a definite V_{OUT}/I_{OUT} profile. This is shown in Figure 6.

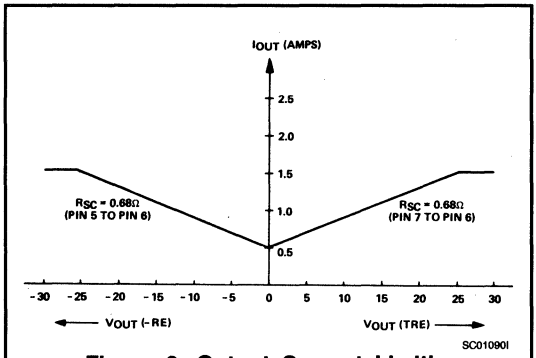


Figure 6: Output Current Limiting

Notice that maximum output current is obtained when $V_{OUT} = +25V \rightarrow 30V$, for either polarity of V_{OUT}; current falls off as V_{OUT} decreases to limit the internal power dissipation. When driving 24V to 28V DC motors or actuators, the power amp delivers full power. Since I_{OUT} is a maximum for this range, the internal power limiting does not affect normal performance. For example, consider driving a 24V DC motor at 1.5 amps delivered current. The internal power dissipation is (30V – 24V) x 1.5 amps = 9 watts.

Now the load is also taking 1.5 amps x 24V = 36 watts. The amplifier efficiency $= \frac{36 \text{ watts}}{46 \text{watts}} = 80\%$. Now, if the output is mistakenly shorted to ground (through motor failure) then $I_{OUT(max)}$ goes to 0.5 amps and the power dissipation equals 30V x 0.5 amps = 15 watts. As long as the amplifier is heat-sinked to dissipate this 15 watts, no damage will result and proper performance will return when the fault is corrected. A significant advantage of the IH8510 family is that the case is electrically isolated and is not tied to any pin. This means that multiple IH8510's can be mounted on the same heat sink.

The IH8510 family design is shown in Figure 7. It consists of a 741 op amp driving a custom chip (called the IH8063). The 8063 is a 60V circuit which boosts the voltage and current outputs of the 741 to drive internal power transistors. It also contains plus and minus regulators to lower the ±30V input voltages to ±15V for safe 741 operation.

COST OF THE POWER DAC SYSTEM

The complete, operational system is shown in Figure 4. At the time of writing, the 7520 sells for $10 in small quantities, and the 301A is in the 50¢ area. The IH8510 sells for $15 each in small quantities, so the system cost is as follows:

7520 DAC (Intersil)	$10.00
5KΩ 50ppm pot (full scale trim)	2.00
op amp	.50
100pF capacitors	.20
Miscellaneous resistors	1.10
0.68Ω 5 watt resistors	.50
IH8510 power amplifier (Intersil)	15.00
	$29.30

To obtain a D.C. reference for the DAC, one can buy a 10V reference or use a circuit such as that shown in Figure 8.

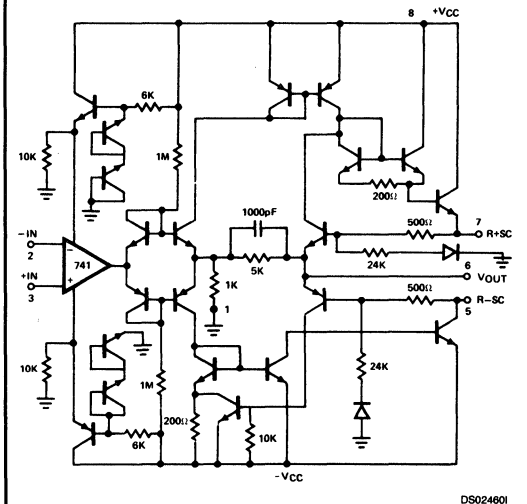


Figure 7: IH8510 Schematic

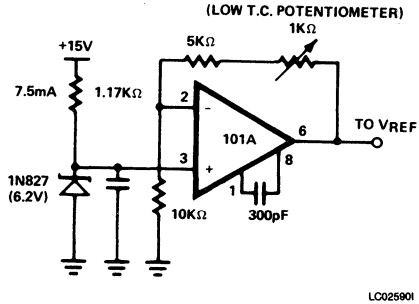


Figure 8: Buffered DAC Reference

APPLICATIONS

Motor Control

An important application for power D/A converters is in precision motor control systems (position controllers). Digitally controlled constant torque is best facilitated using the power DAC circuit shown in Figure 9. The desired torque is set by closing the appropriate DAC switches; this sets the DC output of the DAC. Torque is directly proportional to motor current, and the motor current is directly proportional to the voltage across R_S, i.e.,

$$\text{Torque} = KI_m = \frac{-KV_1}{R_S}$$

By setting the DAC input switches 2^0, 2^1, 2^2, etc., any desired torque can be obtained and a torque versus time profile can be established. Torque versus time profiles are important in controlling the acceleration and deceleration of motors and may be used to provide dynamic breaking for different load conditions. The digital control could be performed by a microprocessor or a programmable logic array.

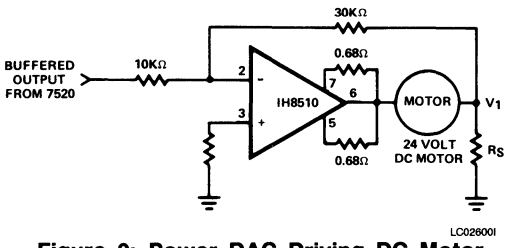


Figure 9: Power DAC Driving DC Motor

Programmable Power Supply

Another big application for power DACs is the digitally controlled power supply. It is probably that the coarse and fine control adjustment knobs on power supplies will be replaced in the future by digit switches. With this, the user does not need to use a $3\frac{1}{2}$ digit DVM just to set a power supply. An 8-bit power DAC allows the supply to be set instantly and provided remote control automatically. The practical problem one runs into here is the maximum load capacity the power DAC can drive without oscillating. Power supplies often use 0.1μF to 100μF decoupling capacitors to ground; this will cause most op amps to oscillate, including the 8510. The only answer for this application is to reduce the bandwith to gain C_L drive capability. Of course, the lower the bandwith, the bigger the value of C_L to keep the output impedance to a certain minimum value; thus there is a compromise involved here. This compromise is not unique to the 8510; the amplifiers in typical series pass regulators must also be designed to handle capacitance loads without misbehaving. Another possible solution is to isolate the amplifier output from the load by using a series inductor. Thus, when large decoupling capacitors to ground are used, the amplifier still sees at least the inductance as a load.

A059
Digital Panel Meter Experiments for the Hobbyist

Digital displays have many advantages over their analog counter parts. They are more accurate, and more rugged since there are no moving parts. Equally important, unskilled operators can record accurate data due to the unambiguous nature of the readout. But ready-built digital panel meters (DPMs) are costly and, until recently, designing one's own from scratch was an ambitious undertaking.

Intersil's ICL7106 and ICL7107 one chip panel meter ICs have changed all that. By adding only a display and less than 10 passive components, anyone can build a high performance DPM for less than the cost of a good moving-coil meter. All that is needed is Ohm's Law and a soldering iron! The hobbyist can have digital display of his aquarium temperature or the speed of his sailboat, the serviceman can build his own test equipment, and the student of physics can measure his plasma potential.

The starting point for designs such as these is one of Intersil's digital panel meter kits. Two kits are offered. One uses a liquid crystal display (LCD), and is intended to be powered by a 9V "transistor radio" battery. The other uses light emitting diode (LED) displays, and will usually be driven by an external power supply. The kits include all the components necessary to build a 200mV full scale panel meter, including the IC, circuit board, display, passive components and miscellaneous hardware. They are available from Intersil's distributors; the LCD kit (part #ICL7106 EV/KIT) sells for $29.95, the LED kit (part #ICL7107EV/KIT) sells for $24.95. Figure 1 shows what the kits look like after assembly. Included in the kit is a detailed Application Note (#A023) entitled **Low Cost Digital Panel Meter Designs**, which includes assembly instructions and schematics. For reference, the circuit diagram of each kit is repeated in Appendix I.

The following discussion uses the assembled panel meter as a basic building block and explains how it can be used to make fundamental electrical measurements of voltage, current, and resistance. Very little circuit design knowledge is assumed; the discussion is primarily directed towards engineers, technicians, students and hobbyists from fields other than electronics.

DC VOLTAGE MEASUREMENTS

The most frequently measured electrical parameter is voltage. In the majority of applications, it is desirable to have the displayed reading correspond directly to the voltage being measured. Since the maximum value that can be displayed on the digital readout is 1999, voltmeters with full-scale readings of 199.9mV, 1.999V, 19.99V, etc., are easily made. The user must determine the full-scale reading that is most appropriate for his application. Then a reference voltage, and in some instances an input attenuator, must be selected.

The relationship between the full-scale input voltage and the reference voltage is very simple:

$$V_{IN}\ (\text{full-scale}) = 1.999 \times V_{REF}$$

There is, however, a restriction on the magnitude of V_{REF}. It is not possible, for example, to measure a 199.9 volt signal by using a 100 volt reference - the integrated circuit chip would be damaged by voltages of this magnitude. The reference voltage should be between +100mV and +1 volt, and to achieve the one-to-one relationship between V_{IN} and the displayed value, it should be exactly +100.0mV or +1.000V. The evaluation kits are supplied with the components necessary to build a 200mV (or, to be precise, a 199.9mV) full-scale panel meter. The kit application note (A023) explains how to change the sensitivity from 200mV to 2V full scale.

To measure voltages greater than 2 volts, an input attenuator is needed as shown in Figure 2.

Now the full-scale sensitivity is given by:

$$V_{IN}\ (\text{full-scale}) = 1.999\ V_{REF} \times \frac{R_2}{(R_1 + R_2)}$$

For a panel meter which is to be used on a single fixed range, it is not necessary to buy .05% (1 in 2000) or better resistors. Any small variations in the ratio $R_2/R_1 + R_2$) can be compensated by tweaking the reference voltage. It is important, however, that the ratio remains fixed for the calibration period of the instrument. Metal film resistors with good long-term drift characteristics should be used. It is also important to use low temperature coefficient types, otherwise small temperature changes will effect the full scale accuracy to an undesirable extent.

The input attenuator obviously reduces the input resistance of the circuit from $> 10^{12}$ ohms to $(R_1 + R_2)$. This places an upper limit of about 10MΩ on the input resistance that can readily be achieved when using an attenuator before the A/D input current causes off-set errors.

MULTI-RANGE DVM's

Multiple range voltmeters are frequently required and are easy to implement using the ICL7106 or ICL7107. The full scale voltage is selected via a rotary or push-button switch, or possibly an analog gate. Two schemes are commonly used, as shown in Figure 3a and 3b.

The circuit of Figure 3a has the advantage that any switch contact resistance appears in series with the ICL7106/ICL7107 input. Since the input resistance is $> 10^{12}\Omega$, errors due to the switch are negligible. Another advantage is that precision voltage attenuators (R_1 through R_5) are available from a number of manufacturers. Allen Bradley, for example, makes thin film network which contains 1K, 9K, 90K, 900K and 9MΩ resistors in one package (FN207) — ideal for a five-range voltmeter. Most hobbyists, however, will find that it is less expensive to use medium precision resistors in series with potentiometers for the attenuator. Then the schematic of Figure 3b has some advantages because the resistors in the attenuator are non-interactive. Setting up the 10:1 attenuator, for example, has no influence on the 100:1, the 1000:1, etc. The circuit of Figure 3b is also more amenable to solid state range switching. An analog switch or FETs may be used in place of the mechanical switch. Then, by adding a couple of zener diodes (or ordinary silicon diodes in the case of a 200mV F.S. panel meter) the solid state switch is totally protected against overvoltages. By contrast, the configuration of Figure 3a exposes the switch to the full-input voltage, which may be several hundred volts. However, in 3b the switch

resistance forms part of the attenuator and could contribute an error.

So far we have only discussed full-scale voltages of 200mV or greater. On the 200mV scale, the least significant digit represents 100μV steps. To resolve smaller signals, it is necessary to use an operational amplifier prior to the ICL7106/ICL7107 inputs. It is quite feasible to do this, provided one realizes that the autozeroing circuitry within the panel meter cannot take care of the op-amp offset or voltage drift. In a 741 the drift may amount to as much as 15μV/°C, while a 308A will have no more than 5μV/°C.

The initial offset can of course be zeroed in the usual way. Figure 4 shows a circuit with ±20mV full-scale and an input resistance greater than 10MΩ.

AC VOLTAGE MEASUREMENTS

The ICL7106 and ICL7107 will not measure AC voltages directly; an AC to DC converter is needed. The least expensive way to build such a converter is to use an op-amp and some diodes in a half or full wave rectifying circuit. The type of circuit shown in Figure 5 has been used extensively in commercial 3½ digit DVM's. It has high input impedence (10MΩ), good bandwidth (20Hz to 5kHz) and introduces no DC errors since the CA 3140 is capacitively coupled to the ICL7106/ICL7107.

It should be realized, however, that this circuit is responding to the average value of the applied waveform. The majority of AC voltmeters, on the other hand, are required to read RMS values. For a sinusoidal waveform, the relationship between the average value and the RMS value is fixed. Thus by altering the gain of the AC or DC converter (the 2kΩ potentiometer Figure 5), the output can be adjusted to read RMS. But the more the measured waveform deviates from a sinewave, the greater will be the error. Other waveforms with fixed form-factors can be measured in a similar manner, provided the relationship between the average and the RMS value is known.

In applications where the AC waveforms being measured have widely varying form-factors, a true RMS converter should be used. National's LH0022 and Analog Devices' Model 536 are suitable. In any event, the subject of AC and DC converters is a complex one. The reader wishing to pursue the subject in greater depth is referred to Reference 1.

RESISTANCE MEASUREMENTS

The best way to measure resistance is to use the so-called ratiometric technique. The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input (between IN HI and IN LO), and the voltage across the known resistor applied to the reference input (between REF HI and REF LO). If the unknown equals the standard, the integrate and de-integrate ramps will be of equal slope and the display will read 1000. In general the displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

Figure 6 shown a typical resistance measurement circuit. Note that due to its ratiometric nature, the technique does not require an accurately defined reference voltage. The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

CURRENT MEASUREMENTS

Current must be converted into voltage through the use of a shunt resistor. The relationship between the current and the displayed reading for the circuit of Figure 7 is given by the following expression:

$$\text{Displayed reading} = \frac{I_{IN} \times R_S}{V_{REF}} \times 1000$$

In most current measurement applications, it is preferable to use a reference voltage of 100mV. This minimizes the shunt resistance and, therefore, the voltage dropped across the shunt. A multirange current meter is shown in Figure 8. Note that although the input current passes through the selector switch, IR drops across the switch do not contribute to the measured voltage.

ARBITRARY SCALE FACTORS

We have already noted that one of the advantages of a digital display is the unambiguous nature of the read-out. When measuring other physical parameters, such as temperature, it is equally desirable to display 78.0°C, for example, as 78.0. With the ICL7106 or ICL7107 this can readily be achieved, even though the temperature sensing element may be a diode which changes −2.1mV/°C.

For scale factors between 100mV and 1mV per least significant digit (LSD), simply determine the reference voltage required from the following equation:

V_{REF} = (Voltage change represented by 1 LSD) x 10^3

For example, in the temperature-sensing diode discussed above, we may want the least significant digit to represent 0.1°C, which would correspond to a voltage change across the diode of 210μV. To achieve this sensitivity, the reference should be set at 210μV x 1000 = 210mV.

For scale factors greater than 1mV/LSD, the most straight forward approach is to use an input attenuator in conjunction with a 1 volt reference. For example, consider a 0 to 2000lb. weighing machine with a transducer that puts out 3.7mV per pound. An input attenuation network that reduces the input signal to 1mV/lb will give the desired scale factor.

TEMPERATURE MEASUREMENT

Many of the points discussed in the foregoing sections can be illustrated by considering the design of a digital thermometer. We have already seen how a diode-connected transistor can be used as the sensing element since V_{BE} has a temperature coefficient of about −2.1mV/°C. Setting the reference at around 210mV will give the desired scale factor of 0.1°C per count.

The other problem that must be considered is the zero adjustment. At 0°C and 100μA bias current, the diode will have a forward voltage of about 550mV. In order for the meter to read zero at 0°C, we must set up a fixed 550mV (approx.) source that can be used to offset the diode drop. Since the voltage between V+ and common is internally regulated at about 2.8 volts in the ICL7106 and ICL7107, this is easily achieved. In the circuit of Figure 9, R_5 should be adjusted to give 000.0 output reading with Q_1 at 0°C. Then R_4 should be adjusted to give 100.0 reading with Q_1 at 100°C.

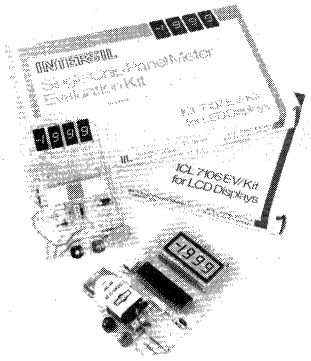


Figure 1: Digital Panel Meter Kits for the Experimenter

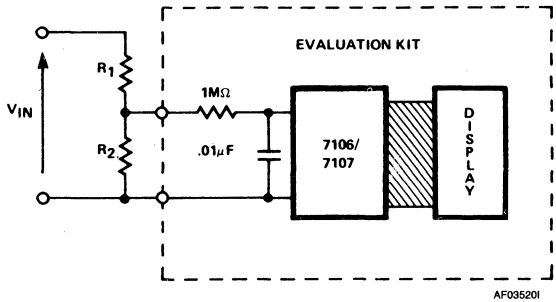
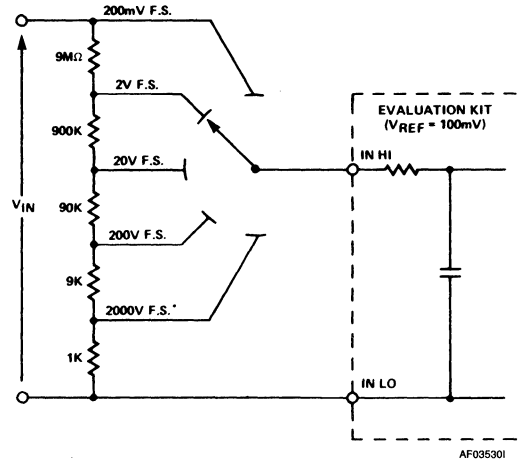


Figure 2: Input Attenuator for $V_{IN} \geq 2.0V$



*CAUTION: High voltages can be lethal. Proper operating precautions must be observed by the user. Intersil assumes no liability for unsafe operation.

Figure 3(a): Multirange Voltmeter

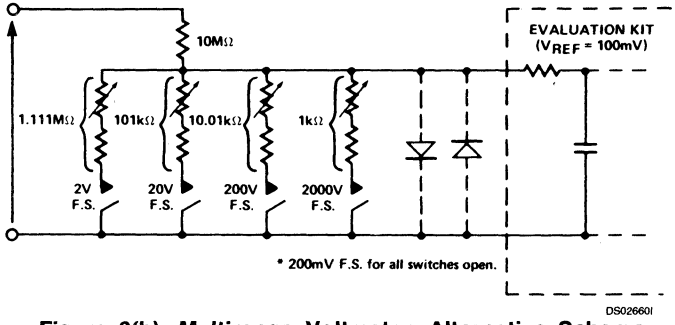
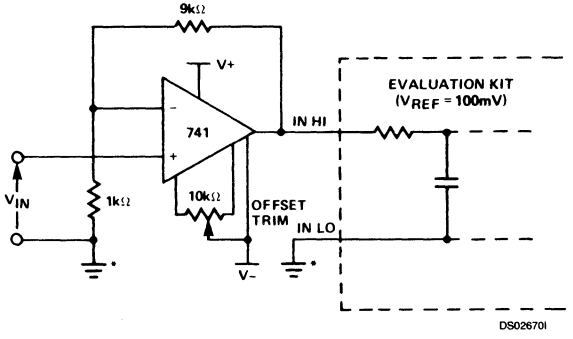
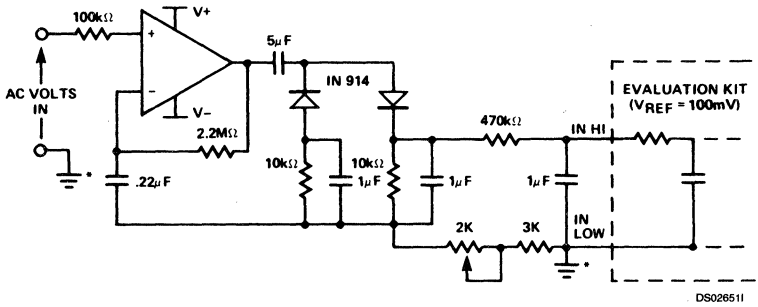


Figure 3(b): Multirange Voltmeter, Alternative Scheme



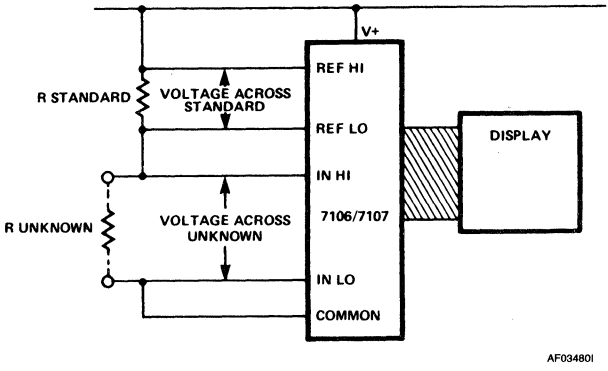
GND* = IN THE ABSENCE OF SPLIT SUPPLY OPERATION, "TEST" (PIN 37) CAN BE USED AS GROUND.

Figure 4: 20mV Full Scale



GND* = IN THE ABSENCE OF SPLIT SUPPLY OPERATION, "TEST" (PIN 37) CAN BE USED AS GROUND.

Figure 5: AC to DC Converter



(* REQUIRES SOME MODIFICATION TO THE KIT)

Figure 6: Resistance Measurement*

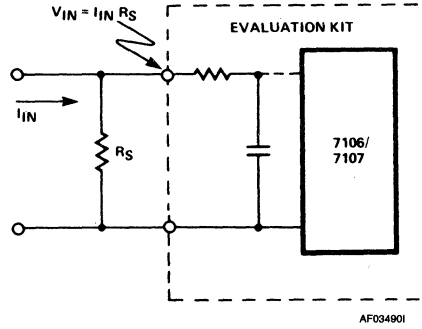


Figure 7: Current Measurement

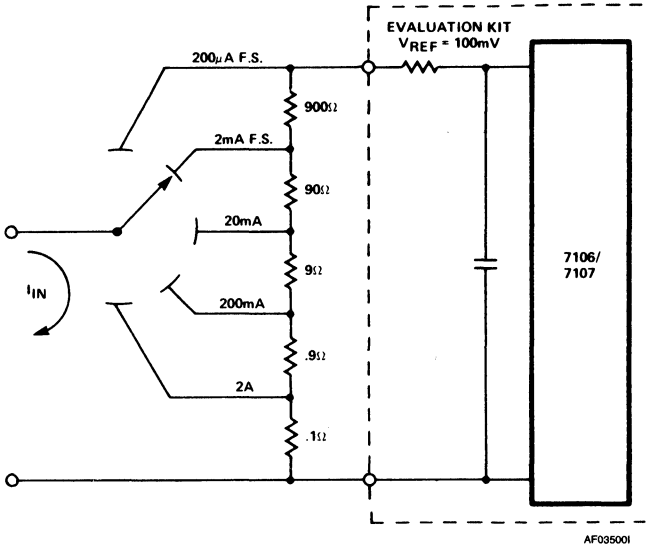
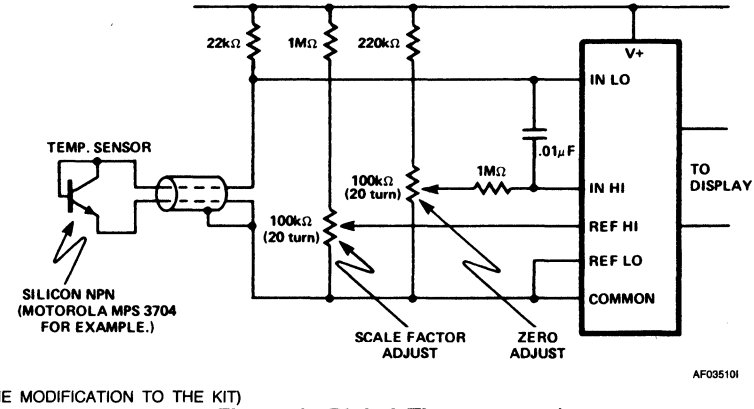


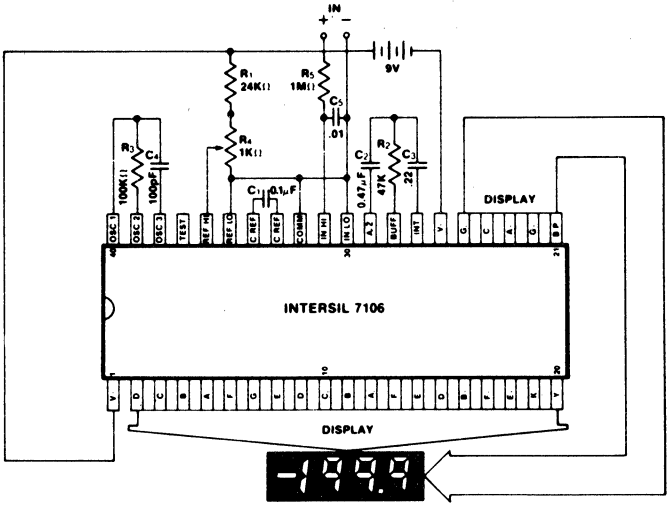
Figure 8: Multirange Current Meter



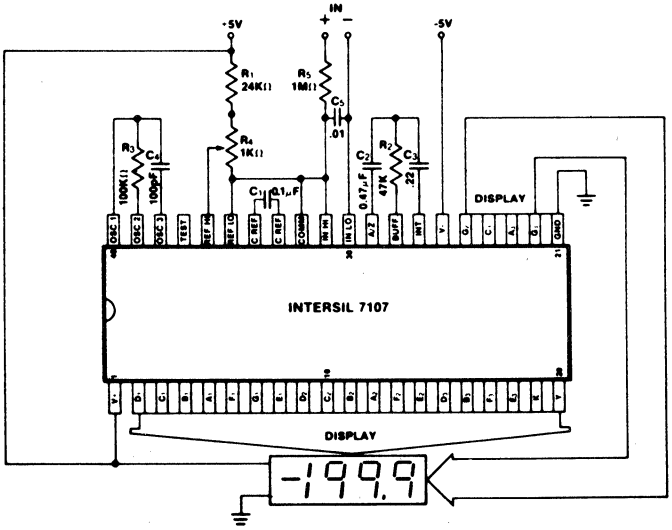
(* REQUIRES SOME MODIFICATION TO THE KIT)

Figure 9: Digital Thermometer*

APPENDIX 1—EVALUATION KIT SCHEMATICS



ICL7106 WITH LIQUID CRYSTAL DISPLAY



ICL7107 WITH LED DISPLAY

Chapter 3
Sample & Hold Circuits

AO08
Analyzing the Dynamic Accuracy of Simultaneous Sample-and-Hold Circuits

In most simultaneous data-acquisition systems a large number of analog input channels are strobed at precise time intervals and then sequentially digitized by an analog-to-digital converter. To check the multichannel sample-and-hold circuits there are some simple tests the user can perform to verify correct circuit operation.

To start the error analysis, several assumptions can safely be made: All static errors have been eliminated —

- The offset error.
- The gain error.
- The hold step error.

Input voltage. V_{in}, to the sample-and-hold equals the output voltage, V_{out}, from the sample-and-hold. V_{in} is any dc voltage between ±10V. The offset error is V_{out} when $V_{in} = 0$, while the gain error is the maximum value of the offset error divided by V_{in} maximum (10V).

LOOKING AT THE DYNAMIC ERRORS

Normally, one sample-and-hold circuit is used for each A/D converter with any multiplexing between input channels done previously. However, for a large number of channels this leads to errors due to the different conversion times of the various channels. In a simultaneous sample-and-hold configuration, a number of input analog channels are strobed at a precise time and the held voltages are sequentially converted to digital form.

At this point the most basic test that can be performed is to simultaneously apply the same voltage waveform to all inputs. Now, if we look at the output for each channel, the digital words representing each voltage should be identical. If the system fails this basic test, the user must search the specification sheets and the circuits themselves for the error sources.

The three major sources of dynamic errors can be traced to the following:

- A change in the gain during the sample mode as a function of frequency.
- A nonzero hold step as a function of frequency (hold-step error).
- A shift in the effective beginning of the hold-step as a function of V_{out}, dV_{out}/dt, or frequency (aperture-shift error).

The aperture-shift error can be caused by a slowly opening switch or by a pole at the unity-gain −3dB point (f_{co}) of the unity-gain sample amplifier. The error advances the effective time of the switch opening to a time prior to its actually reaching open circuit. For applications of simultaneous sample-and-hold circuits both the f_{co}'s and the switch opening times, must be matched.

THE TRANSFER FUNCTION DURING SAMPLE

Gain in the sample stage can be represented by a linear transfer function — at least for amplitudes small enough that the amplifier slew-rate doesn't affect the results. Thus, a simple low-pass function with a pole at f_{co}, say 1MHz, can be represented by the following:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\,\frac{f}{10^6}}$$

The graph of this typical low-pass filter is shown in Figure 1a. It has unity-gain transmission and a 1-MHz −3dB point.

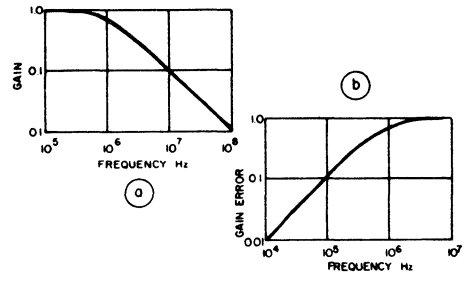


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Figure 1: Plots of a sample pole transfer function (a) and of the gain-error (b) are shown with a 1-MHz cutoff frequency.

Usually, though, it proves more useful to plot small deviations from unity gain as shown in Figure 1b. The formula used for this gain-error plot is

$$\text{Gain error} = \frac{V_{out}}{V_{in}} - 1 = \frac{-j\,\frac{f}{10^6}}{1 + j\,\frac{f}{10^6}}$$

While not usually seen in this form, this type of frequency-response plot is quite valid. From the equation we see, for example, that a circuit band-width of 1MHz, an input of 10V at a frequency of 1kHz results in an error of 0.001 or 10mV.

By now finding the response of the circuit to a ramp of K V/sec, we can try to match transfer functions of all the channels of the sample-and-hold stages. The gain-error transfer function is put into the s domain using LaPlace transforms and becomes

$$\text{Gain error} = \frac{\frac{-s}{2\pi \times 10^6}}{1 + \frac{s}{2\pi \times 10^6}}$$

The ramp is also transformed, and becomes K/s^2.

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THE SAMPLE-AND-HOLD: WHAT IS IT AND WHERE IS IT USED?

A sample-and-hold (S/H) circuit holds or "freezes" a changing analog input signal voltage. Usually, the voltage thus frozen is then converted into another form, either by a voltage-controlled oscillator, an analog-to-digital (A/D) converter or some other device.

The simplified block diagram of a lossless (ideal) S/H circuit is shown in Figure 1. Here the amplifiers are assumed to be ideal — with infinite input impedances and bandwidths, zero output impedances and unity gains. The electronic switch is also considered ideal — with infinite speed, zero impedance in the sample position and infinite impedance in the hold position. Also, the sampling capacitor, C, is assumed to have no leakage or dielectric absorption.

Depending upon cost, the user has three basic methods to choose from when setting up a multiple-signal data-acquisition system. The most basic but also the most expensive scheme is the one shown in Figure 2a. This circuit uses an individual S/H and A/D converter for each sensor line. Figure 2b is a low cost alternative in which all the sensor lines are first multiplexed and then fed into a single S/H and A/D converter. Another method, falling between those of Figures 2a and 2b in cost and performance is shown in figure 2c. Here, the sensor signals are first sampled and then multiplexed and sent to a single A/D converter.

If the S/H circuits were ideal, the only significant errors would occur in the multiplexer or the A/D converters. In a real world situation, of course, the S/H circuits introduce some serious errors into the conversion circuit.

The circuits of Figures 2a and 2c require additional qualities from the S/H circuits that are not needed for the system of Figure 2b. Precise matching of the aperture delays and bandwidths is required.

Taking the inverse transform of the product we get

$$\frac{K}{2\pi \times 10^6}[1 + e-(2^{\pi} \times 10^6)t]$$

as the output error for a ramp input.

The two terms in the result represent a gain error. This error is due to the ramp as a constant $K/2\pi fxx$ and a delay of 1 $2\pi fxx$ seconds. The delay in the output can be considered as an advance in the transition time of sample-to-hold states — but this is not usually done. The inverse transfer function can always be applied after the data has been digitized. However, for multichannel simultaneous sample-and-hold applications it is unnecessarily complicated to keep track of, say, 32 different transfer functions. The solution to this problem is to match all the transfer functions so that the units will deliver identical outputs for the same input waveform.

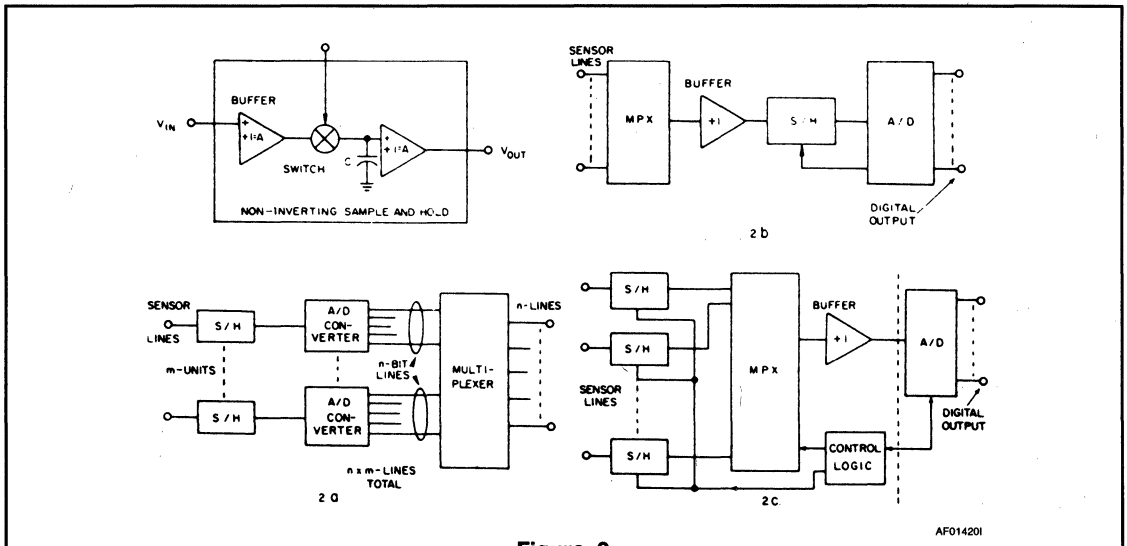

Figure 2

OTHER ERROR SOURCES EXIST

Examination of the output voltage near the time of the sample-to-hold transition shows the errors caused by both a hold step and an aperture shift (Figure 3).

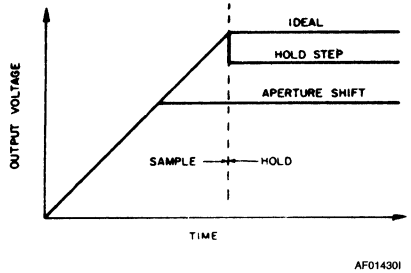

Figure 3: Dynamic errors caused by the hold step and the aperture shift are hard to distinguish.

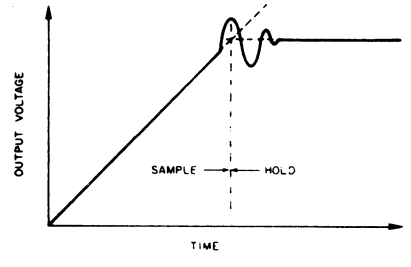

Figure 4: By extrapolating the two straight line segments to meet each other, you can find the effective time at which the hold period starts.

The hold-step error appears as a sudden change in the sample capacitor voltage at the time of hold. If such an error exists only for a fast ramp input, a probable cause is dielectric absorption in the capacitor.

The aperture shift is a variation, in either direction, of the point in time at which hold occurs. It is also known as aperture uncertainty. As a function of input rate it is somewhat difficult to measure.

To measure aperture uncertainty, use an oscilloscope with a sampling amplifier or with a sensitive, wideband input having good recovery. Then observe the sample-and-hold output for an input slope of 0.5 or 1V/μs. The resulting straight lines can then be extrapolated to a point where they meet, and the effective hold instant can be found, as shown in Figure 4. A change of this point with the input waveform, or randomly, is called aperture jitter.

A similar type of measurement uses a scope's differential input. All static and dynamic errors, including linear ones, due to the transfer function can be measured by observing $V_{out} - V_{in}$ as shown in Figure 5. The slope during the hold period can be extrapolated back to zero to find the effective time when hold starts. With a single-pole transfer function, the value of $V_{out} - V<in>$ during sample for an input ramp is proportional to the slope of the waveform. But as shown in Figure 6, to a first-order approximation, the start of hold is unaffected.

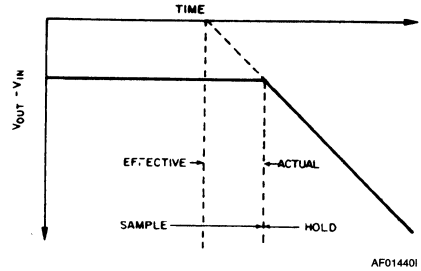

Figure 5: If you use a different scope input, the effective point of hold initiation can be found by extrapolating back to the zero point.

But, there is zero aperture uncertainty with the transfer function representation, thus the effective time of hold initiation occurs before the switch opens! The amount of this shift can be determined as a function of bandwidth. A transfer function with an f_{CO} of 1MHz can be represented by an RC low-pass filter with a resistor of 159Ω and a capacitor of 100pF. An input ramp of 1V/s will cause a capacitor current of 1mA (CV/t) which in turn causes a resistor drop of 159mV. Thus the effective time of hold occurs 159mV/V/μs or 159ns before the actual switch opening.

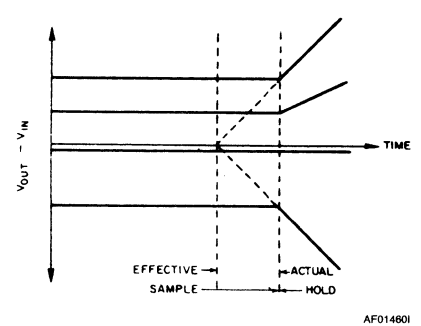

Figure 6: The effective start time for hold is not affected by the scope of the input ramp-for a first-order analysis.

The two measurements described are difficult to perform without high performance test equipment. Therefore, most manufacturers' specifications of aperture delay and uncertainty tend to be primarily concerned with the variation of switch resistance after the logic input changes to the hold state. Figure 7 shows a typical logic switch resistance change during the sample-to-hold transition.

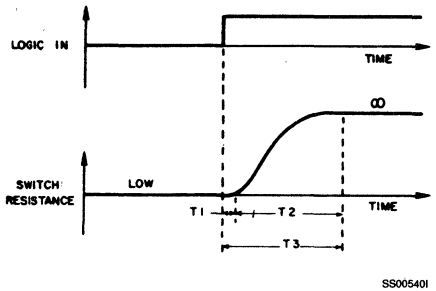

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Figure 7: A typical analog switch introduces a delay in the sample-hold transition.

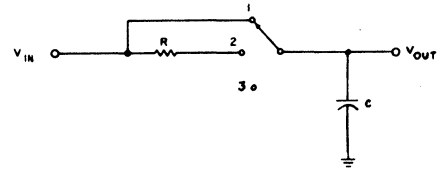

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Figure 8: An ideal slow opening switch can be modeled by using a sample RC network and a three position switch.

The time T_1 is known as the switching delay or aperture delay and is characteristic of any practical switch. Switching time, T_2, usually is measured from the 10 to 90% points (as for logic circuits) and is sometimes called aperture time. The total switching time, T_3, is also referred to as either the aperture time or aperture delay. If the rise time of the switch varies with the input voltage waveform, or just randomly, the change in T_1 is called the aperture jitter.

To further complicate matters, some definitions do not use switch resistance. Diode-bridge switches are characterized by stored charge and not by changes in resistance. The switch must then be viewed as a black box — apply a ramp voltage to it, open the switch and determine the effective time of opening by observing V_{out} and extrapolating the straight lines as previously described. A second method relying on diode reverse-recovery measurements can be used but is not as accurate.

The example shown in Figure 8 can demonstrate that the effective switch opening time occurs before the switch resistance reaches infinity. Let V_{in} be a ramp of K V/μs. If, at time t = 0, the switch goes from position 1 to 2, then 1 μs later it goes to position 3, the effective time of hold can be seen from Figure 9 to occur while the switch is in position 2. The aperture-time advance is fixed for an input ramp but will have jitter for waveforms that have curvature. The effective hold initiation will occur between instants T_1 and T_3. This is why $T_2 - T_1 = T_2$ is often specified as the aperture time.

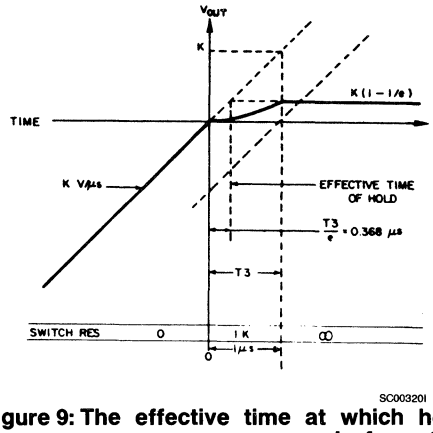

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Figure 9: The effective time at which hold commences occurs before the switch is fully opened.

AO09
Pick Sample-Holds By Accuracy and Speed and Keep Hold Capacitors in Mind

When it comes to selecting a sample-hold device, fortunately there's a fine assortment available: monolithic, hybrid and modular types can all give good performance. There are different degrees of good performance, of course, and for the most part the sample-hold that's finally selected will depend on the degree of speed and accuracy needed. Depending on the type of sample-hold and its application, it may need an external hold capacitor. This capacitor should be chosen with as much care as the sample-hold itself, for its quality directly affects the performance of the sample-hold. There will be more about selecting hold capacitors, but first, it's a good idea to consider error analysis, which is vital in appraising the total error contribution of a sample-hold to a system.

In a given system, of course, the sample-hold is but one of the many sources of error that may also include an amplifier, filter, multiplexer, and A/D converter. Achieving total system accuracy on the border of 0.01% is by no means a trivial task, but quite the opposite. It pays to take a somewhat pessimistic approach in adding up the errors, and follow this by thorough testing of the sample-hold's accuracy in the system. In many cases the results will be a pleasant surprise, because a conservatively-specified device has been chosen. In other cases, it won't be a shock to discover that the analysis is about right because the sample-hold that was selected has been specified right at the edge of its performance.

The best way to handle error analysis is with a systematic listing like the one in Table 1, which gives errors for a fast, accurate system with 0.01% error as a design goal. The errors are computed for an assumed operating temperature range of 0 to 50°C and take into account all of the specifications discussed in this series.

What seems to be a large total error in Table 1 shouldn't be alarming. The sample-hold evaluated, designed for use in 12-bit systems, has been conservatively specified. If all the errors add in the same direction, the total error is ±0.036%, but this is an unlikely possibility. Adding the errors statistically (RMS) gives a better figure of ±0.017%, which is a good bit closer to the goal. Since most of the errors are specified as maximums, the typical statistical error is actually close to 0.01%.

Speed and accuracy are the two foremost considerations in choosing a sample-hold, and the key to proper selection is an error analysis that takes the desired sampling rate into account. The circuit configuration, a subject discussed in Part 1 of this series, affects performance in certain applications, so it should be kept in mind as well.

CONSIDER MONOLITHICS FIRST

In general, a monolithic device should be considered first, since it will result in the lowest-cost design if moderate performance is acceptable. Moderate performance implies about 4μs acquisition time to 0.1% and 5 to 25μs to 0.01%. Monolithic devices use external hold capacitors, so one will need to be selected.

Hybrid microcircuit sample-holds offer a step up in performance without a major increase in size. Acquisition times of 5μs down to 1μs, to 0.01% accuracy are available, and even faster acquisition times for 0.1% can be obtained. Most hybrid sample-holds include an internal hold capacitor, so there's no need to select one unless additional capacitance is needed. Many hybrids use MOS-type hold capacitors which offer exceptionally good performance.

Both the newer monolithic as well as hybrid devices equal or surpass the performance of many of the early low-cost modular sample-holds, but they can't match the newer, high-performance modular types. These new modules offer some difficult-to-achieve speed and accuracy specifications such as 350-ns maximum acquisition time to 0.01%, or 50ns to 0.1%.

Table 1: Error Analysis of An Accurate, High Speed Sample-Hold

SOURCE OF ERROR	ERROR CONTRIBUTION	COMMENTS
Acquisition error	0.01%	Maximum error specified for rated acquisition time.
Gain error	0.00	Externally adjustable to zero.
Offset error	0.00	Externally adjustable to zero.
Nonlinearity	0.005%	Maximum specified.
Droop error	0.01%	For 10μs hold time. Using 25°C droop of 20μV/μs max. and multiplying by 10 to give droop of 1mV at 50°C. This is 0.01% for 10V full scale.
Gain change	0.004%	Using specified 15 ppm/°C max., x maximum temperature change of 25°C.
Offset change	0.008%	Using specified 30μV/°C max., x max. temperature change of 25°C.
Dielectric absorption	0.003%	Estimated error voltage during hold time using curve of Fig. 2.
Total	0.036%	
RMS Total	0.017%	

Once a sample-hold has been selected, it may need a hold capacitor. These capacitors have somewhat unusual requirements. Some parameters, such as tempco of capacitance, matter very little, while others, such as dielectric absorption, are very important. Dielectric absorption affects the accuracy of the held voltage, although insulation resistance is quite important as well, for the same reason.

When high accuracy is needed, the range of satisfactory capacitor dielectrics narrows down to those in Table 2, which gives the important specs for them. Note that insulation resistance, which is quite high at 25°C, drops drastically at higher temperatures, such as 125°C. That's because insulation resistance decreases exponentially with temperature.

IT WON'T STAY PUT

If a capacitor is charged to a given voltage, discharged by shorting it, and then open-circuited again, its voltage will begin to creep up from zero toward the original voltage. The capacitor exhibits a "voltage memory" characteristic known as dielectric absorption, which occurs because the dielectric material doesn't polarize instantaneously — molecular dipoles need time to align themselves in an electric field. As a result, not all the energy stored in a charged capacitor can be quickly recovered upon discharge.

One way to measure dielectric absorption is to charge the capacitor to some voltage for 5 minutes, discharge it through a 5-Ω resistor for 5 seconds, then disconnect it. Measure the capacitor voltage five minutes later. The ratio of the measured voltage to the charging voltage, expressed in percent, is the dielectric absorption.

Even though the time scale in a sample-hold is usually far shorter than 5 min, dielectric absorption is still a source of error and should be taken into account. Assume the hold capacitor has been resting at a given voltage V_O when a different voltage is sampled and held. Once hold mode begins, the voltage on the capacitor will begin to creep back toward V_O. Thus, the dielectric absorption causes an error as illustrated in Figure 1a.

Figure 1b shows a first-order approximation model of an imperfect capacitor, emphasizing dielectric absorption. Resistor R_1 represents the insulation resistance and r_d and c_d represent the source of the dielectric absorption. (Actually, to model the absorption accurately, there should be a number of additional, parallel r_dc_d circuits with different values.)

After capacitor C in the model has been rapidly discharged from a previous voltage and then open-circuited, the long time constant of r_dc_d causes some of the charge on c_d to transfer slowly to C, which develops a small voltage.

An accurate approximation to this "creep" voltage caused by dielectric absorption is shown in Figure 2. The curve is a natural log function of the shortening time, or sampling time (t_s). If the output creep voltage is measured at time $2t_s$, the voltage will be ΔV. If it is measured at $4t_s$, it will be 2 ΔV and at $8t_s$, 3 ΔV. The equation for the curve is

$$V_C = \Delta V \ln \frac{t}{t_s}$$

where t_s is the sample time and t is the total time, or sample time plus hold time ($t_s + t_h$).

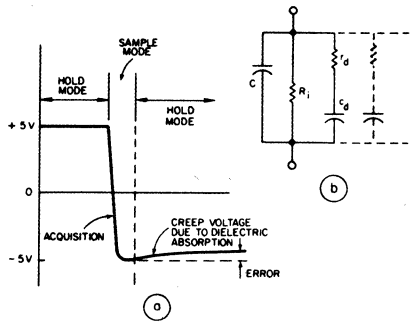

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Figure 1: In this example of dielectric absorption error, the hold capacitor has been sitting at +5V for some time. Although given enough time to settle completely during sampling, in hold mode, the capacitor's voltage creeps back toward +5V. An imperfect capacitor with dielectric absorption can be modeled (b) by a perfect capacitor C, the insulation resistance R, and the long-time-constant components r_d and C_d, which simulate dielectric absorption.

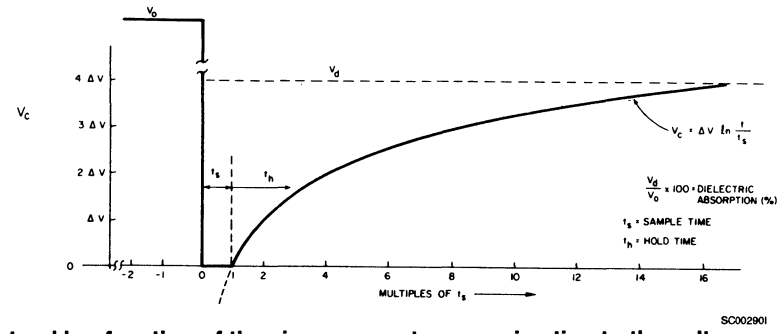

Figure 2: A natural log function of time is an accurate approximation to the voltage creep caused by dielectric absorption. Before sampling, the capacitor has been holding a voltage V_0. A new sample charges the capacitor to a new voltage (zero, in this case, for simplicity), for period t_s. Once in hold mode, the capacitor reaches a voltage ΔV at time 2t, and continues to creep toward V_0 according to the logarithmic expression.

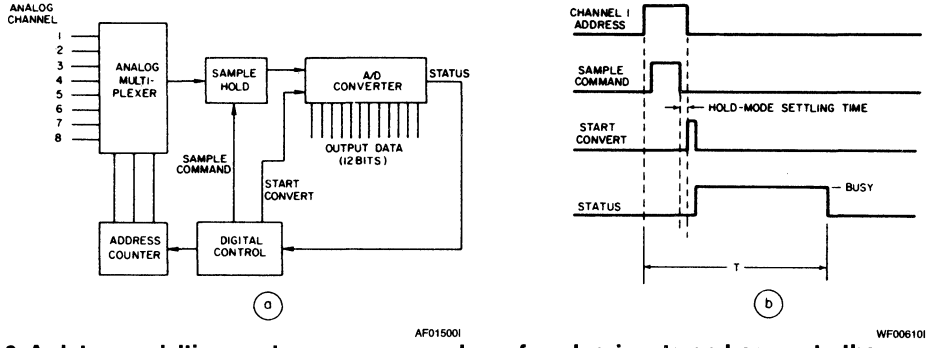

Figure 3: A data-acquisition system scans a number of analog inputs and converts them, one at a time, to digital form (a). The sample-hold provides an unchanging input to the converter until its conversion is complete. When it's finished, the STATUS line goes low to permit the next input in sequence to be converted (b).

This equation is a good model, providing $V_C << V_0$. It does not hold for extremely long time periods, however, since V_C goes to infinity for infinite time. As shown, V_d represents the voltage measured to determine dielectric absorption at a specific time, which is a large multiple of t_s.

Capacitors can be measured and fitted to this curve. First, determine the value of ΔV from the measured dielectric absorption. The standard tests for dielectric absorption normally specify $t_h >> t_s$, which is the correct way to make them. Since the equation is logarithmic, there is no asymptote to the curve, which continues to rise. For all practical purposes, however, a hold time much longer than the sample time will give a value for dielectric absorption that's far out on the curve.

Assume that the dielectric absorption is measured as 0.02% for a point at which $t_h = 15t_s$ or $t = 16t_s$. Then

$$\Delta V = \frac{2 \times 10^{-4}\ V_0}{\ln 16}$$

$$= 7.21 \times 10^{-5}\ V_0$$

where the dielectric absorption is defined as $\frac{V_c}{V_0}$ at $t = 16t_s$.

The resulting equation for creep voltage is

$$V_C = 7.21 \times 10^{-5}\ V_0 \ln \frac{t}{t_s}$$

Table 2: Sample-Hold Capacitor Characteristics

TYPE	OPERATING TEMPERATURE RANGE (°C)	INSULATION RESISTANCE AT 25°C (MEGOHM-MICROFARADS)	INSULATION RESISTANCE AT 125°C (MEGOHM-MICROFARADS)	DIELECTRIC ABSORPTION
Polycarbonate	−55 to +125	5×10^5	1.5×10^4	0.05%
Metalized polycarbonate	−55 to +125	3×10^5	4×10^3	0.05%
Polypropylene	−55 to +105	7×10^5	5×10^3 (1)	0.03%
Metalized polypropylene	−55 to +105	7×10^5	5×10^3 (1)	0.03%
Polystyrene	−55 to +85	1×10^6	7×10^4 (2)	0.02%
Teflon	−55 to +200	1×10^6	1×10^5 >	0.01%
Metallized Teflon	−55 to +200	5×10^5	2.5×10^4 (1) At 105 C (2) At 85 C	0.02%

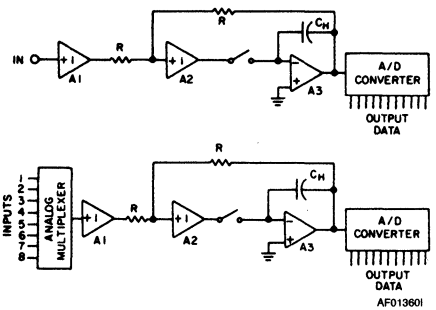

Figure 4: In a single-channel system, the settling time of the input buffer amplifier, A_1, isn't critical because the amplifier can follow changes in the signal (a). With multiplexed inputs (b), however the input buffer may take additional time to settle to the new value at the multiples's output when it switches channels.

Two factors reduce considerably the error due to dielectric absorption in typical applications of a sample-hold. First, the dielectric absorption measurement assumes a long initial charging time, say 5 minutes, whereas in a sample-hold a new voltage is held for a relatively short time. Second, the dielectric absorption is specified for a long open-circuit time compared with the shorting time, whereas in a sample-hold the hold time may be only slightly longer than the sample time.

The amount of creep voltage can also be reduced by remaining in the sample mode as long as possible relative to the hold time. The result of these factors is that a capacitor with a dielectric absorption of 0.02%, for instance, may contribute 0.005% or less error to the sample-hold, as the curve in Figure 2 shows.

At this point, there may be reason to wonder if all the care and time needed to select a sample-hold is worth it. It certainly is. There's an abundance of applications for these devices.

Take a sample

Undoubtedly one of the most common applications for a sample-hold is in data acquisition systems. A representative system would have an 8-channel multiplexer followed by a sample-hold and a 12-bit A/D converter (see Figure 3a).

A logic-control circuit steps an address counter to sequence the analog multiplexer through the eight channels of analog data. For each channel the sample-hold acquires the input signal and switches into the hold mode.

After allowing for the hold-mode settling time, a start-convert pulse initiates the A/D conversion, which is performed by successive approximation. After the conversion, the A/D converter's status output goes low.

When the conversion of this channel is finished, the analog multiplexer switches to the next channel while the output register of the A/D converter holds the digital word from the completed conversion. This word is then transferred out to a computer data bus. The sampling and conversion process is repeated for each analog channel in sequence.

From Figure 3b, T is the time required for the multiplexer and sample-hold to acquire the signal and for the A/D to convert it. Then 1/T gives the throughput rate, or the fastest rate at which the analog channels can be scanned. The rates for practical 12-bit data acquisition systems may vary from about 20kHz up to 250kHz corresponding to values of T that range from 50μs down to 4μs.

Indeed, considering the many applications for sample-holds, a good number are used in conjunction with A/D converters. This is because the sample-hold greatly reduces the converter's aperture time.

There are two important ways to use a sample-hold with an A/D converter, and each imposes a different requirement for the acquisition time. Figure 4a shows a fast inverting sample-hold used ahead of an A/D converter, which converts just one input signal. The sample-hold continuously tracks the input signal until is goes into the hold mode.

Even while in the hold mode, input-buffer amplifier A_1 continues to track the input signal and only A_2 and A_3 affect the acquisition time. Acquisition is very fast because A_1 doesn't have to settle to a new voltage for every sample.

The same sample-hold can also follow an analog multiplexer, as in Figure 4b. The required acquisition time will be longer here since A_1 must settle to a new voltage every time the multiplexer switches to a new channel. This means that the settling time of A_1 is now part of the acquisition time.

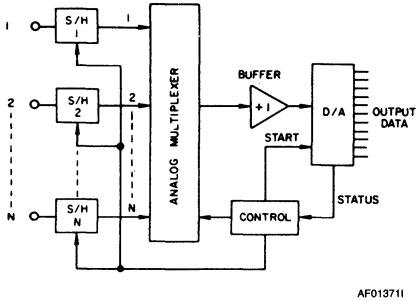

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Figure 5: A simultaneous sample-hold system such as this samples all analog inputs at the same time and holds the samples for conversion. While one of the held voltages is being converted, the others mustn't droop too much.

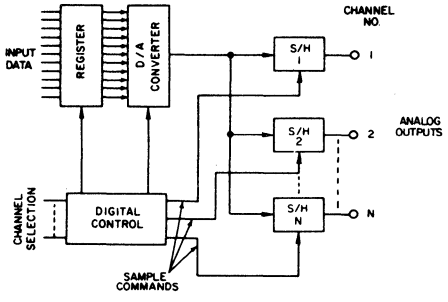

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Figure 6: Multiplexed digital data destined for a number of analog channels are reconstructed and distributed by a system like this one. Once the data for a channel have been converted, the sample-hold for that channel samples the D/A's output and retains it until the next data word for that channel comes in for conversion.

These two situations are significant because A_1's settling time may be larger than the acquisition time of the rest of the circuit. If it is, there'll be a great difference between the acquisition times of single-channel and multichannel acquisition systems.

Another important consideration in a data-acquisition system is interfacing the sample-hold to the A/D converter. A successive-approximation A/D converter, without an input buffer amplifier (which adds to the conversion time), has a resistor input that goes to an analog comparator's input terminal. Since the comparator is changing state during the successive-approximation conversion, the input impedance to the A/D changes. Since this happens at high speed, there may be errors if the sample-hold's high-frequency output impedance isn't low enough. Furthermore, most sample-holds have higher output impedance in the hold mode than in the sample mode.

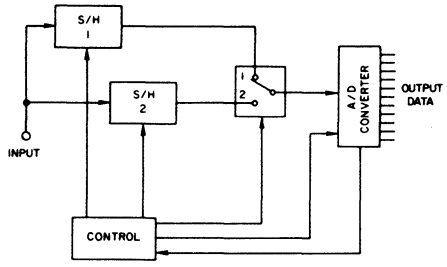

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Figure 7: In an ultra fast A/D conversion system, acquisition time in a sample-hold takes up a sizable part of the cycle. Interleaving two sample-holds like this lets one of them acquire while the other one's output is being converted.

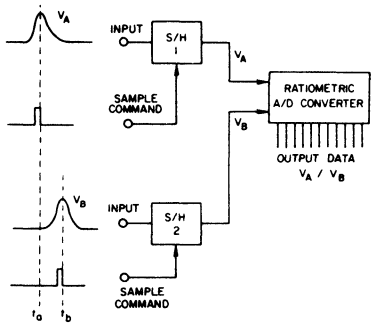

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Figure 8: Sample-holds can serve as a temporary analog signal-storage devices. The first sample-hold retains signal V_A's peak value so the converter can divide it by the peak value of input V_B, which comes by later.

Sample all at once

Another way to use sample-holds in a data-acquisition system is illustrated in the simultaneous sample-hold system of Figure 5. Here, data must be taken from all analog inputs at precisely the same time. To do this, the system

requires a sample-hold per channel ahead of the analog multiplexer.

All the sample-holds are given the hold command simultaneously; then the multiplexer sequentially switches to each sample-hold output while the A/D converter converts it into digital form. Notice that a high-impedance buffer amplifier is required between the multiplexer and the A/D converter.

For this application, select sample-hold devices that are identical and have very small aperture-uncertainty times. In addition, the aperture delay times should be adjusted so that they all go into hold mode simultaneously. Another important criterion is that the droop rate be relatively low, since the last sample-hold in the system must hold its voltage until all the other outputs have been converted.

In an application which is the reverse of data acquisition, sample-holds can send signals from a channel to many destinations in a data-distribution system. Such a system (see Figure 6) uses a single D/A converter and storage register together with a number of sample-holds to distribute data to a series of analog channels. As digital data are transferred into the D/A converter and its output changes, the appropriate sample-hold samples the new output voltage and then, once the converter's output has settled, switches into hold mode.

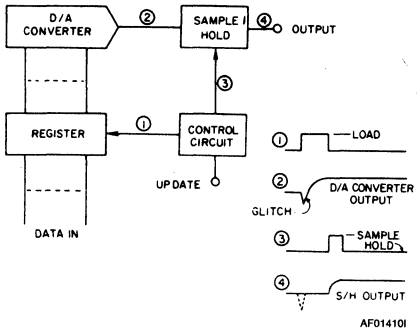


Figure 9: An output developed by many D/A converters for certain input-code transitions temporarily goes the wrong way. This transient, or "glitch", is undesirable in some applications and can be removed by sampling the converter's output after the glitch has gone by.

Each sample-hold circuit is updated in sequence as new data arrive, and holds its voltage until all the other sample-holds have been updated and the sequence returns to the first one. The sample-holds used must be chosen for the required acquisition time, which depends on the rate of updating each output, and for the desired droop error between updates.

Back on the other side of the coin, ultrafast A/D converters can benefit from working with sample-holds. Interleaving two of them, as in Figure 7, will eliminate acquisition time delay in many applications.

In such systems, the sample-hold's acquisition time can be a significant portion of the system's cycle time. With interleaved sample-holds, however, system cycle time depends only on the time required for A/D conversion.

Acquisition-time delay is eliminated by having one sample-hold acquire the next sample while the A/D is converting the output of the other sample-hold. The A/D converter, therefore, is simply switched from the output of one sample-hold to the other. The only dead time between conversions is the small delay in the analog switch.

Conversion time can be decreased further, but doing it requires a second A/D converter, with one A/D operating off each sample-hold. The sample-holds then are operated sequentially, and the outputs of the A/D's have to be digitally multiplexed. In this way the throughput time is reduced to half the conversion time of either A/D converter.

In yet another A/D application, a sample-hold can delay or "freeze" analog data that exist only briefly; this information can then be combined with later data. This circuit (see Figure 8) computes the ratio of two peaks that occur at different times, t_a and t_b.

The first sample-hold stores the peak of signal V_A so that its value will still be available to the ratiometric A/D converter when the peak of signal V_B comes by. The second sample-hold stores the peak while the ratio is being converted to digital form.

Table 3: Sample-Hold Comparison

	ACCURACY	ACQUISITION TIME	PRICE
Monolithic	0.1%	4 to 20μs	$5 to $21
	0.01%	5 to 25μs	
Hybrid	0.1%	25ns	$35 to $135
	0.01%	1 to 10μs	
Modular	0.1%	30 to 200ns	$43 to $208
	0.01%	0.25 to 5μs	

Sample-holds deglitch

The list of conversion applications for sample-holds seems almost endless. Even big problems can be solved. For example, major code transitions in a D/A converter can cause unwanted voltage spikes as large as half the full-scale output voltage. These spikes, commonly called glitches, are caused by switches in the converter that take longer to turn off than to turn on, or vice versa. The point is, in many D/A converter applications such as CRT displays and automatic testing, the converter output voltage should make a smooth, monotonic transition when it goes from one output voltage to the next.

This can be done by processing the D/A converter output with a sample-hold as shown in Figure 9. First, a digital control circuit transfers the digital data from the register to the D/A converter. With this information at its input, the D/A converter generates a new output containing glitches. Once the glitches have settled, the sample-hold takes a sample of the new analog data and returns to hold mode before the D/A output changes again. The output of the sample-hold now has a smooth, monotonic transition between the old and the new levels.

Keeping up with high-speed analog D/A outputs generally requires ultrafast sample-holds for deglitching. Usually an inverting, current-input sample-hold follows the D/A converter to permit the highest possible operating speed. In fact, some specially designed D/A converters have self-contained sample-holds for deglitching, and not surprisingly, are called deglitched D/A converters.

Putting it all together

Data conversions aren't the only applications to benefit from sample-holds. As Part 1 of this series pointed out, a zero-order hold makes an excellent data-reconstruction filter and is commonly used in pulse-amplitude modulated (PAM) systems such as the one in Figure 10. Here, time-division multiplexing is used to send a train of amplitude-modulated pulses over a transmission system, each pulse in sequence being the sample from one analog channel.

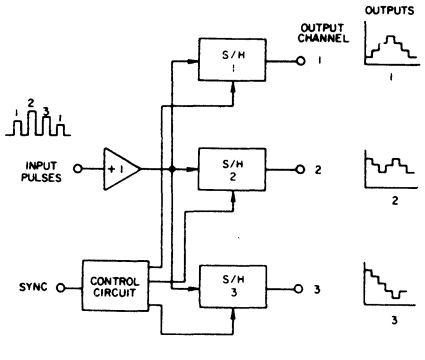


Figure 10: When analog signals are encoded by pulse-amplitude modulation and then multiplexed, they can be sorted out and reconstructed by a set of sample-holds with properly timed sample commands. The time scale of the input is shorter than that of the outputs.

To demodulate this pulse train, the control circuit synchronously switches on each sample-hold in sequence as the pulse arrives, then returns it to hold mode until the next pulse from that channel arrives. Pulse by pulse, the output of each sample-hold becomes the reconstructed analog signal of the appropriate channel. A low-pass filter can also be added to each sample-hold output to smooth the reconstructed signals further.

In some analog-circuit applications, sampling should be quick, yet the sampled value should hold steady for a long time. Such conflicting needs produce conflicting requirements on the sample-hold. The best solution to the problem is to use two cascaded sample-hold devices, as in Figure 11. The first sample-hold is a fast unit that acquires the input rapidly and accurately, while the second unit is a slow device with a very long hold time (low droop rate), perhaps on the order of minutes.

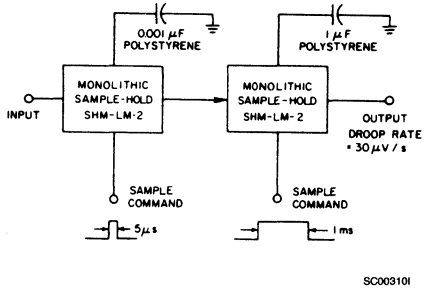


Figure 11: Cascaded sample-holds acquire a signal quickly and held it for a long time with little droop. The first one needs to hold a signal only long enough for the second to acquire it. Typical acquisition would be 5μs to 0.1% with a droop rate of 30μV/s.

Basically, the first sample-hold must acquire the signal quickly and then hold the result long enough for the second sample-hold to acquire it. The errors need to be calculated carefully to be sure of meeting the accuracy requirements. In many cases two monolithic sample-holds in cascade might do the trick. External hold capacitors can then be chosen to give the desired performance.

For example, a 0.001-μF polystyrene capacitor would be a good choice for the first sample-hold to give an acquisition time of 5μs to 0.1%. For the second one, a 1.0-μF capacitor would give an acquisition time of 10ms but a hold time of 300s to 0.1% accuracy. The resulting droop rate would be only 30μV/s, which is quite low, indeed.

AO10
Keep Track of A Sample-Hold From Mode to Mode to Locate Error Sources

A complicated process begins when a sample-hold takes a sample. The complications increase when it switches into the hold mode. To this bumper crop of complications, add the actual sample-to-hold transition itself, which, as a complex and important event, must not be overlooked. Understanding the intricate workings of this process is the basis for understanding the sources of error in the system and how to minimize them.

In the sample mode, the sampling switch closes and the circuit charges the hold capacitor to the input voltage. With the capacitor charged, the circuit tracks the input signal as it changes. However, tracking is possible only if the signal doesn't exceed the bandwidth or slew rate limit of sample-hold. The term "sample mode" applies regardless of how long tracking continues.

The operating parameters that apply to the sample-hold in the sampling mode are specified in the same way as an operational amplifier's. Offset voltage, expressed in millivolts, may be referred to either the input or output, and is usually adjustable to zero with an external potentiometer. DC gain, the ratio of output to input voltage at DC, is commonly either +1 or −1. With some sample-holds, adding external feedback resistors provides other gains, and some allow trimming external gain to precisely +1 or −1.

Bandwidth, the sinusoidal frequency at which gain is down by 3dB from its DC value, is measured with a small-signal sine wave below the slew rate limit. The slew rate is the fastest rate at which the sample-hold output can change. Specified in volts per microsecond, slew rate is generally determined by the charging rate of the hold capacitor.

ACQUISITION TIME COUNTS

The most important specification of the sample-hold in the sample mode is acquisition time — the time required, after the sample command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band about its final value.

As illustrated in Figure 1, the definition applies to the capacitor voltage, not the output voltage of the circuit. The reason for this will become clear shortly. The figure shows an initial switching delay following the sample command. After this delay, the hold capacitor charges at a maximum rate which is determined by its charging current.

Initially, as the capacitor voltage attempts to enter the final value error band, it slightly overshoots the band, but then enters and remains within it. The amount of overshoot, generated by a wideband input amplifier driving a capacitive load, depends on this amplifier's stability. Acquisition time is therefore measured from the beginning of the sample command transition to the point where the signal enters the error band and stays there.

Another useful definition of acquisition time is the amount of time following the sample command transition that the hold command can be given so that the hold capacitor retains the voltage change to the required accuracy. The full-scale voltage change is usually specified as a 10-V change, although other magnitudes may be specifically stated. The error band is commonly specified from 0.2% down to 0.005%, with other values possible. Within this range there are sample-holds available that provide acquisition times from about 10μs down to 20ns. Basically, acquisition time determines the maximum sampling rate at which a sample-hold can be operated.

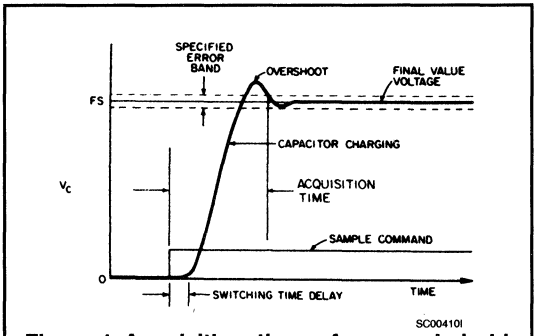


Figure 1: Acquisition time of a sample-hold starts with the sample command and ends when the voltage on the hold capacitor enters and stays in the error band. Acquisition time is defined for a full-scale voltage change, measured at the hold capacitor.

Several circuit limitations determine the achievable acquisition time for a sample-hold: the speed of the input amplifier with a capacitive load, the current available to drive the hold capacitor, the source resistance driving the hold capacitor (both amplifier output and switch), and the value of the hold capacitor. Either the input amplifier or the switch may limit the current available to drive the hold capacitor.

Figure 2 shows the relationship between the acquisition time, the current available to charge the capacitor, and the time constant associated with the hold capacitor. For example, to determine the acquisition time for a 10-V change to within 1mV, or a 0.01% error band, assume a maximum charging current from the amplifier and switch of 20mA and a capacitor value of 0.002μF. The rate of change of capacitor voltage dV_C/dt is

$$\frac{I_C}{C_H} = \frac{20 \times 10^{-3}}{2 \times 10^{-9}} = 10^7 = 10V/\mu s, \qquad (1)$$

where I_C is the charging current and C_H is the capacitance of the hold capacitor. After a 50-ns switching delay, the capacitor begins to charge at a constant rate of 10 V/μs until it approaches final value and maximum charging current is no longer required. This happens when

$$V_C = 10 - (I_C R_T) = 9.6V. \qquad (2)$$

R_T, the total resistance in the hold capacitor's charging path, is also the sum of the amplifier output resistance (R_O) and the switch series resistance (R_S).

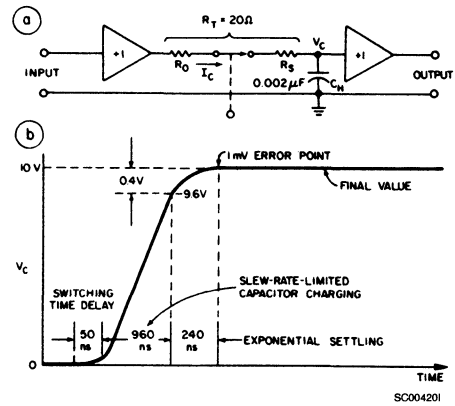


Figure 2: This equivalent circuit for determining acquisition time (a) shows the importance of the charging time constant, R_TC_H. Acquisition time is the sum of the various delays incurred in charging the hold capacitor to its final value (b), and is dominated by slew-limited charging.

The capacitor charges exponentially over the final 400mV with a time constant of

$$T = R_TC_H = 20 \times 2 \times 10^{-9} = 40 \text{ ns.} \quad (3)$$

Since the final error band is specified as 1mV, it takes six time constants to reduce the 400mV error to 1mV, or 0.25%. Six time constants give a 240-ns exponential settling time. The acquisition time is then the sum of the three times that are indicated in Figure 2b, or 0.05 + 0.96 + 0.24 = 1.25μs.

This illustrates a fast sample-hold that acquires to 0.01% accuracy and shows as well that the charging current to the capacitor must be high and the hold capacitor time constant must be low. The same acquisition time limitations apply to the other sample-hold circuits shown in Part 1 of this series, which is why a current booster amplifier is required in one case.

Direct measurement of a sample-hold's acquisition time is not always possible since in some cases the capacitor voltage is not accessible externally. If a sample-hold has an operational integrator output stage, acquisition time can be measured, but in other circuits it may not be possible because the capacitor is inside the circuit.

The two interesting cases in Figure 3 illustrate why the acquisition time is defined in terms of the hold capacitor. In Figure 3a, the output buffer has a slower response time than the input amplifier and capacitor. This lag means that when the capacitor acquires a new voltage, its final value is reached before the output of the sample-hold. The switch can be opened when the capacitor voltage has entered the specified error band even though the output voltage has not. Slightly afterward, the output amplifier settles to the correct output voltage.

Figure 3b shows the output stage of one of the popular monolithic sample-hold circuits that has a resistor in series with the hold capacitor. This resistor provides short circuit protection to the capacitor terminal. The resistor, however, causes a lag in the capacitor voltage, which means that the capacitor is not fully charged when the sample-hold output voltage has reached final value. To allow the capacitor to charge completely, the sampling switch in this circuit must remain closed longer than indicated by the output voltage. The acquisition time in this case must be measured by starting with a long sample time and then gradually reducing this time until the output starts to show an error. These cases underscore the fact that acquisition time is properly defined at the capacitor rather than at the sample-hold's output.

THEN THERE'S HOLD MODE

The second mode of operation for a sample-hold, when the sampling switch is open, is the hold mode. Two important specifications that characterize hold mode are hold mode droop, or voltage decay, and hold mode feedthrough.

Hold-mode droop, defined as the output voltage change per unit of time while in the hold mode, is commonly specified in volts per second, microvolts per microsecond, or other convenient quantities. Hold-mode droop originates as leakage from the hold capacitor (see Figure 4). The four leakage components consist of capacitor insulation leakage I_{CL}, switch leakage current I_{SL}, output amplifier bias current I_S and stray leakage I_{STRAY} from the common terminal connection. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current, I_L to hold capacitance C_H

$$\frac{dV_C}{dt} = \frac{I_l}{C_H} \quad (4)$$

If all the leakage currents don't have the same polarity, the result is somewhat lower droop rate.

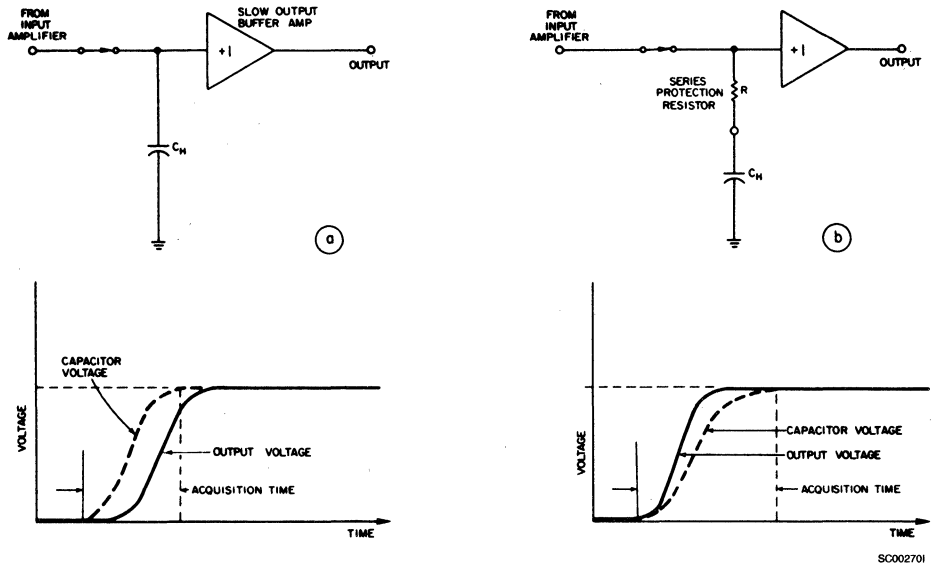


Figure 3: Acquisition time may be less than or greater than the time it takes the output voltage to settle to its final value. In (a), the capacitor reaches its final value before the output amplifier catches up. In (b), the protective resistor permits the output to settle before the capacitor reaches its final voltage.

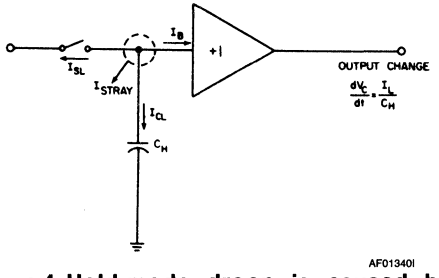
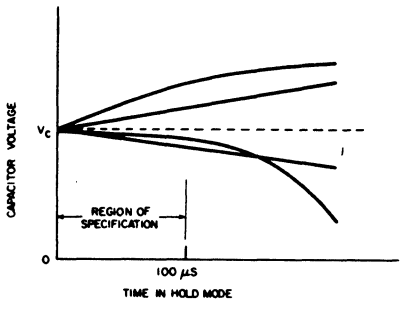


Figure 4: Hold-mode droop is caused by currents that charge or discharge the hold capacitor. These include switch-leakage, stray-leakage, amplifier-bias currents and leakage within the hold capacitor itself.



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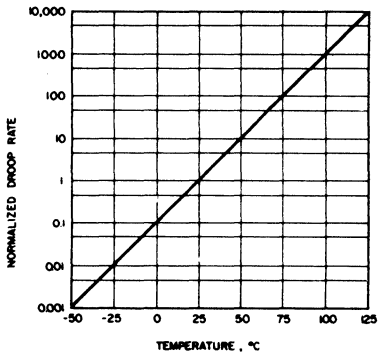

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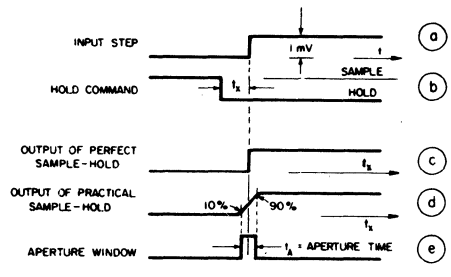
Figure 5: Droop in hold mode can be positive or negative-going, and may not be linear with time (a). Since most leakage current comes from silicon devices, droop as a function of temperature is predictable (b).

To measure hold-mode droop, simply acquire a given voltage and then while watching the output voltage on an oscilloscope, switch into the hold mode. The droop may be positive or negative and is not necessarily linear with time (See Figure 5a). Several possible droop rates are illustrated. The value measured, which appears on data sheets, is the slope right after initiation of the hold mode when the output voltage feeds an A/D converter or other circuit.

In addition, hold-mode droop changes exponentially with temperature. Most of the leakage that causes this droop comes from silicon devices. Since a device's leakage approximately doubles for every 10°C increase in temperature, hold-mode droop shares this characteristic. Figure 5b shows a normalized plot of hold-mode droop vs. temperature for virtually any sample-hold. Droop rate is specified on a data sheet at 25°C. To consider an example, a sample-hold with a droop rate of 100μV/ms at 25°C will have a rate of 3.2mV/ms at 75°C and a rate of 102mV/ms at 125°C.

For a given operating temperature, droop rate must be determined based on the required hold time in order to know the resulting error. Of course, below 25°C, droop rate improves by a factor of two for every 10°C. In cases where better droop rate is required, an extra hold capacitor must be added or a better sample-hold selected. Additional capacitance also increases the acquisition time of the circuit.

In the case of monolithic sample-holds, the hold-mode leakage is specified on the data sheet so that the required capacitor value can be figured from the relationships in equation 4.



WF00560I

Figure 6: Aperture time can be measured by repeatedly feeding a tiny step (a) to the sample-hold's input and repeatedly shifting from sample to hold (b) with a varying delay, t_X. A perfect sample-hold would have an output like (c) as a function of delay time t_X, but a real sample-hold averages this step over t_A.

Since the hold capacitor directly affects both speed and accuracy of a sample-hold, it's useful to have a figure of merit for sample-holds. Increasing the hold capacitance decreases the droop rate, but increases acquisition time. Likewise, decreasing the capacitance increases the droop rate although it does decrease the acquisition time.

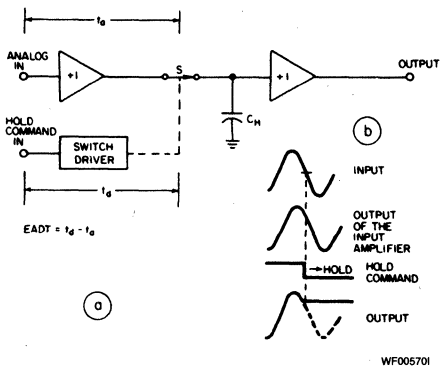


Figure 7: Effective aperture delay time is the difference between the input amplifier time delay, t_a, and the delay between the hold command and the time when the switch opens (t_d). EADT may be positive, zero, or negative. If t_a is greater than t_d, the hold capacitor sees a delayed version of the input (b), which results in holding an input voltage that occurred before the hold command.

The figure of merit is a ratio that measures the improvement in both acquisition time and droop rate together. It is a dimensionless quantity and may have values of 10^9 or more for a high quality sample-hold.

A useful figure of merit sometimes used with sample-holds is the ratio of the current available to charge the capacitor (I_C) to the leakage current from the capacitor (I_L). This ratio is approximately equal to the ratio of slew rate to droop rate:

$$\text{Figure of Merit} = \frac{I_C}{I_L} \approx \frac{\text{Slew Rate}}{\text{Droop Rate}} \qquad (5)$$

Another source of error in the hold mode is hold-mode feedthrough, or simply feedthrough, is the second specification that characterizes hold mode. This parameter is the percentage of an input sinusoidal signal that's measured at the output of a sample-hold in the hold mode.

To measure feedthrough, apply a 20-V peak-to-peak sinusoid to the input of a sample-hold while it is in the hold mode. A greatly attenuated version of the input shows up at the output, passing through switch capacitance and stray coupling capacitance. The resulting feedthrough can be measured easily with an oscilloscope. Typical values of feedthrough for a well-designed sample-hold are from 0.05% down to 0.005% of the input. Feedthrough is sometimes expressed in dB of attenuation.

Hold-mode feedthrough may vary with frequency, either increasing or decreasing at higher frequencies depending on the particular design of the sample-hold. Feedthrough is a most important specification when a sample-hold follows an analog multiplexer that switches between many different channels. Note that feedthrough can also be measured with a square-wave input rather than a sinusoid, since the square wave contains many harmonic frequencies.

A CRITICAL PARAMETER

The most critical part of sample-hold operation is during the short sample-to-hold transition when the sampling switch opens. It's during this transition period that the real subtleties of sample-hold operation appear, including one of the most important parameters associated with this period, called aperture time.

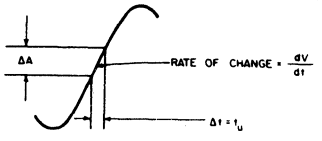


Figure 8: Timing uncertainty in the switch and driver circuit produces uncertainty in the held voltage, which for a given period of time, increases with the rate of change of the signal voltage.

Aperture time is the most misunderstood of all sample-hold specifications. There are actually several related parameters which use the word aperture as part of the specification.

The concept of aperture time in electronics relates closely to the root meaning of aperture: an opening, or hole. In electronic measurements aperture is the "opening" or "window" of time during which a signal is averaged or measured. For example, in an A/D converter, the conversion time is the time required to measure the input signal and is also known as the aperture time of the converter. In fact, a sample-hold is the device that reduces the aperture time of an A/D converter by replacing the converter's time window with the sample-hold's much shorter window.

Ideally, a sample-hold takes a point sample of the input signal, that is, an accurate sample in zero time. Since this is impossible, the sample is actually taken in the short period of time when the switch opens, during which the signal is averaged. The aperture time therefore occurs after the signal has been acquired, when the switch rapidly opens.

Aperture time is frequently, but mistakenly, defined as the turn-off time of the switch. If this were true, aperture times would be extremely small since the switch opens very quickly. The confusion stems from the fact that the switch follows on a band-limited input amplifier which, even if the switch opening were instantaneous, averages the result over a small period of time.

To interpret aperture time, as in Figure 6, assume the sample-hold receives a 1-mV input step (Figure 6a). The hold command transition (Figure 6b) can be adjusted to occur before, with or after the input step. The timing difference between the two, designated t_x, can be positive, zero, or negative. (For simplicity, assume no delay between the hold command and the opening of the sampling switch.) To make the measurement, feed the sample-hold with repeated input steps and hold commands while slowly

varying t_X. As the hold command transition effectively scans across the input step, the sample-hold's output in hold mode changes. Ideally, when hold-mode output is plotted against t_X, it should look like Figure 6c. Such an output, a perfect sample with no averaging, requires an infinite-bandwidth input amplifier in addition to an infinitely-fast switch.

Since this is not possible, the input step is averaged, or filtered, by both the switch with a non-zero opening time, and by the input amplifier, which has limited bandwidth. The actual waveform therefore looks like Figure 6d. The filtering action of the switch and input amplifier slows the rise-time of the step to t_A, which is the aperture time or aperture window of the sample-hold as shown in Figure 6e. Mathematically convolving the input step (Figure 6a) with the aperture window (Figure 6e) gives the actual output (Figure 6d).

In practice, because of amplifier and switch speed limitations, it is extremely difficult to achieve true aperture times less than a few nanoseconds.

DELAYED WINDOW

Aperture delay time, another frequently used term concerning the sample-to-hold transition, is generally defined as the elapsed time between the hold command and the opening of the switch. Aperture delay time, a pure time delay, can be compensated out by advancing or delaying the hold command. Furthermore, this specification is difficult to measure, if not impossible, since the precise time when the switch turns off cannot be determined directly.

A more useful specification might be called effective aperture delay, and defined as the time difference between the hold command and the time at which the input signal and the held voltage were equal. In other words, effective aperture delay relates the hold command to the point on the input signal which was held (see Figure 7).

Effective aperture delay really points out the difference between the two delay times shown in Figure 7. The first is the analog delay through the input amplifier, while the second is the digital delay to the switch opening (Figure 7a). Effective aperture delay (EAD) is then equal to $(t_d - t_a)$.

Notice that either a positive, negative, or zero value may be obtained depending on which delay is larger. Figure 7b illustrates negative effective aperture delay. In this instance, time lag in the input amplifier has resulted in holding an input voltage which occurred before the hold command. Knowing effective aperture delay time then is more useful than knowing aperture delay time.

A related specification, aperture uncertainty time, or aperture jitter, is the uncertainty in the time at which the switch opens. Actually, it's the time variation in aperture delay time. If the sampling switch receives the hold command for a series of samples at the same point on a waveform, it will hold slightly different values each time.

Aperture uncertainty time originates in the digital driver circuit and switch. The hold command has a finite risetime and must pass through one or more logic thresholds that have voltage noise. These transitions therefore generate time uncertainties. The significance of aperture uncertainty time is that it causes an amplitude uncertainty in the held output of the sample-hold. This amplitude error, ΔA, shown in Figure 8, equals the product of the rate of change of the input signal dV/dt, and the aperture uncertainty t_u.

This product is the basis of a graph (Figure 9) that gives aperture uncertainty vs. signal rate of change for various accuracies. The accuracy is based on 10-volt full scale signals. The surprising fact is that moderate speed signals produce relatively large errors even with small aperture uncertainties. For example, if the aperture uncertainty is 10ns and the input signal rate of change is 1V/μs, the amplitude error is 0.1% for 10V full scale. Reducing this error to 0.01% means that the aperture uncertainty time has to be reduced to just 1ns.

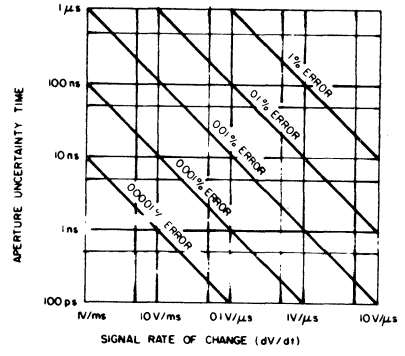


Figure 9: To obtain the error due to aperture uncertainty time for a given signal rate of change, a full-log plot is helpful. This plot assumes a 10-V full-scale signal.

Aperture uncertainty time is generally quite small in well-designed sample-holds since it's possible to achieve values of a few nanoseconds down to tens of picoseconds. As a rough rule of thumb, the aperture uncertainty tends to be 10% or less of the aperture delay time; in some designs it can be as low as 0.1%.

Sample-to-hold offset error develops when the switch opens, as a direct result of a phenomenon called charge dumping or charge transfer.

There are two types of sample-hold switches; one operates at virtual ground (Figure 10a), while the other operates at the signal voltage (Figure 10b). Every electronic switch has a capacitance associated with it. In this case it is C_{dg}, the drain-to-gate capacitance of the junction FET switches shown. This capacitance couples the switch-control voltage on the gate to the hold capacitor.

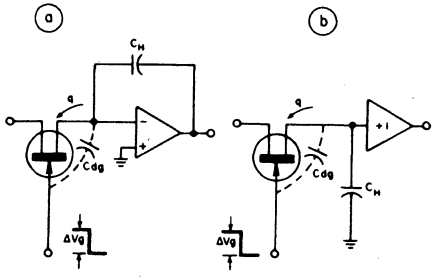


Figure 10: Drain-to-gate capacitance, C_{dg}, transfers some charge, q, when a FET sampling switch opens. The resulting voltage step on the hold capacitor, C_H, is small if C_H is large. The switch in the first circuit (a) operates at virtual ground.

Since the switch-control voltage must generally be rather large, a significant charge transfers from the hold capacitor to the gate-drive circuit when the switch is turned off. This charge is

$$q = C_{dg}\Delta V_g \qquad (6)$$

where ΔV_g is the change in gate voltage. The error this produces on the hold capacitor is then

$$V_C = \frac{q}{C_H} = \frac{C_{dg}}{C_H}\Delta V_g \qquad (7)$$

This error typically might be 10mV assuming 2pF for C_{gh}, a 10-V ΔV_g, and a 0.002μF hold capacitor. Sample-to-hold offset error is one of the undesirable, inherent characteristics of sample-hold circuits. It should be looked for and recognized. The charge transfer that causes this error is expressed in picocoulombs and in practical circuits it may vary from 50pC down to 0.1pC. Since monolithic sample-hold circuits require external hold capacitors, their voltage error must be determined by equation 7. Sample-holds with internal capacitors have a specified sample-to-hold offset voltage. This offset, of course, can be decreased by adding an external capacitor to increase the total hold capacitance.

Note that the two switch configurations in Figure 10 have somewhat different charge transfer characteristics. In the virtual ground switch the charge transfer is constant regardless of the signal voltage, since the gate voltage change is always the same. In the other switch, however, the gate voltage change varies with the signal voltage. This causes the charge transfer to vary with signal level. Furthermore, the drain-to-gate capacitance also varies with the signal voltage, so that the charge transfer itself is nonlinear and even has a "gain error."

SOME HAVE CURVED ERRORS

The output error caused by charge transfer differs for the two types of switches (Figure 11). The virtual ground switch produces a constant offset error vs. signal voltage, while the floating switch produces a nonlinear error vs. signal voltage. Charge transfer is obviously a limiting factor in a high-accuracy, high-speed sample-hold. It works against attaining both these characteristics simultaneously. Some sample-holds have unique switch designs that minimize or compensate for this charge transfer. In some of them, an externally-adjustable compensation circuit minimizes the charge transfer. If the sample-to-hold offset error is constant with signal voltage, then the error is relatively easy to handle since it can be zeroed with a simple offset adjustment.

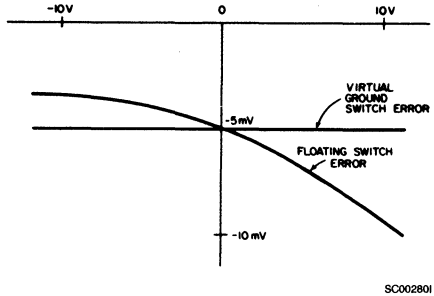


Figure 11: Sample-to-hold offset error varies with input signal voltage if the sampling switch floats with the signal, but is unaffected by variations in signal voltage if the switch operates at virtual ground.

Another effect of the sample-to-hold transition is a small transient in the output just after going into the hold mode — the hold mode settling time (Figure 12b). This is the time it takes the output of the sample-hold to settle within the specified error band after the hold command transition. Notice that the hold mode settling time includes aperture delay time. Figure 12 shows the small output transient caused by the rapid switch turn-off at the input to the buffer amplifier.

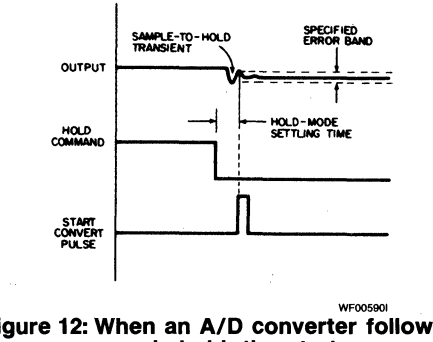


Figure 12: When an A/D converter follows a sample-hold, the start-conversion pulse must be delayed until the output of the sample-hold has had enough time to settle within the error band and stay there.

This transient occurs after the output settles to a new value that includes the sample-to-hold offset. Hold mode settling time may be a few nanoseconds to a microsecond or so, depending on the particular sample-hold. It is an important specification because an a/d conversion that follows sampling and holding cannot begin until hold-mode settling is complete without causing a conversion error. As Figure 12 shows, the pulse that starts the converter is generated after the sample-hold output has settled within the specified error band.

KNOW THE LINGO

Acquisition time: How long it takes after the sample command is given, for the hold capacitor to be charged to a full-scale voltage change and to remain within a specified error band around its final value.

Aperture delay time: The time elapsed from the hold command to the opening of the switch.

Aperture jitter: Also called "aperture uncertainty time," it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture time: The averaging time of a sample-hold during the sample-to-hold transition.

Bandwidth: The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Effective aperture delay: The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of merit: The ratio of the available charging current during sample mode to the leakage current during the hold mode.

Hold-mode droop: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-mode feedthrough: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in the hold mode.

Hold-mode settling time: The time from the hold-command transition until the output of the sample-hold has settled within the specified error band. It includes aperture delay time.

Sample-to-hold offset error: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor from the switch as it opens.

Slew rate: The fastest rate at which the sample-hold output can change. It's specified in V/μs.

AO11
Designing With A Sample-Hold Won't Be A Problem if You Use The Right Circuit

Sample-hold circuits are widely used in analog signal-processing and data-conversion systems to store an analog voltage accurately over periods ranging from less than a microsecond up to several minutes. This capability suits them to numerous applications including data-distribution systems, data-acquisition systems, simultaneous sample-hold systems, A/D converter front ends, sampling oscilloscopes and DVMs, signal reconstruction filters, and analog computation circuits.

Although sample-holds are conceptually simple, their application is full of subtleties. In general, applications that need only slow to moderate speed and moderate accuracy generate few problems, but high-speed, high-accuracy applications are the ones that need careful design. An example of the latter is taking a 10-V sample in one microsecond or less with 0.01% accuracy.

To select the right sample-hold for a particular job, and apply it properly as well, requires understanding the intricacies of its design and operation.

BASICALLY SPEAKING

A sample-hold circuit is fundamentally a "voltage memory" device that stores a given voltage on a high-quality capacitor. The circuit can take a voltage sample and then "freeze" it for some specified period, while some other circuit or system uses the voltage.

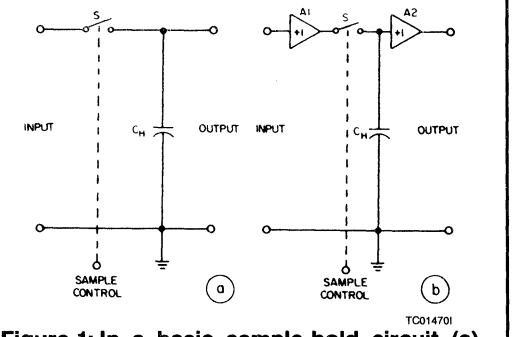


Figure 1: In a basic sample-hold circuit (a), the switch closes to sample the input voltage. When the switch opens, the capacitor holds the voltage. A practical circuit (b) has unity-gain buffers to charge the capacitor without loading the source and to drive normal loads without changing the voltage stored by the capacitor.

Figure 1a shows a sample-hold circuit in conceptual form. An electronic switch is connected to a hold capacitor so that when the switch closes, the capacitor charges to the input voltage. When the switch opens, the capacitor retains this charge and thus holds the desired voltage for a specified period.

There are three important sets of terminals in a sample-hold circuit: the analog input, the analog output, and the sample control terminals. Figure 1b shows a practical circuit that includes input and output buffer amplifiers and a switch-driver circuit. The sample control input closes the switch for sample mode, or opens it for hold mode.

The sample-hold input terminals are usually the input of a high-impedance buffer amplifier since in most applications, such as operating at the output of an analog multiplexer, the source shouldn't be loaded. Likewise, the output has a low impedance so that the sample-hold can drive a load such as an A/D converter input. The output buffer amplifier must also present a very high input impedance, and very low bias current, to the hold capacitor so that its charge doesn't leak off too rapidly. In virtually all sample-hold designs, therefore, this amplifier has a junction-FET input stage. Similarly, the switch must be fast and have very low off-state leakage.

SAMPLE-HOLD: AN ENERGY STORAGE CIRCUIT

All sample-holds are basically accurate energy storage circuits. Since the hold capacitor is a key component in an accurate sample-hold, a fundamental question to be answered is: Why use a capacitor to store the energy?

It turns out that certain types of capacitors very nearly approach the ideal. They have extremely low leakage, and therefore very high equivalent parallel resistance. This resistance, commonly specified in megohm-microfarads and known as insulation resistance, is the parallel resistance of a one-microfarad capacitor and is numerically equal to the self-discharge time constant of the capacitor in seconds.

To find the parallel resistance for other capacitor values, divide the insulation resistance in megohm-microfarads by the capacitance in microfarads. Since the parallel resistance can be quite high for smaller value capacitors, most manufacturers specify a maximum "need not exceed" value, generally twice the insulation resistance. This means only that the parallel resistance is not measured or guaranteed by the manufacturer. It may well be as high as calculated.

The self-discharge time constant is the length of time required for an open-circuited capacitor to discharge to 36.8% of its charged voltage. High-quality capacitors used in sample-holds have insulation resistance as high as 10^6 megohm-microfarads, equivalent to a self-discharge time constant of one million seconds, or 11-1/2 days. In other words, this is only 1% droop in almost three hours.

To get back to why capacitors are used for the energy storage, they approach the ideal much more closely than the alternative, which is an inductor. The figure of merit for an energy-storage element is its self-discharge time constant. A high quality short-circuited inductor is hard pressed to give a self-discharge time constant (L/R) as high as 10 seconds, while a capacitor can give a time constant (RC) of

10^6 seconds. (The only exception, a superconducting inductor, would, of course, be better than a high quality capacitor, but it would be difficult to package in an ordinary sample-hold circuit!)

Capacitors of certain types are therefore clearly superior to inductors when it comes to approaching the ideal. Acceptable types of capacitors include polystyrene, polycarbonate, polypropylene, and Teflon. In addition, MOS capacitors are excellent for hybrid circuit sample-holds.

Two other storage elements useful in specialized sample-holds are an electrochemical cell such as the Plessey Electro-Products E-Cell, and a register that holds the voltage digitally.

Sample-hold circuits are variously called zero-order-holds, track-and-holds, or sample-and-hold amplifiers. Although these terms are generally used interchangeably today, some technical distinctions should be pointed out.

Strictly speaking, a sample-hold takes a very fast sample and then goes into the hold mode. This means that the switch closes for only a very short period of time, usually because a pulse transformer drives the switch. A track and hold circuit, on the other hand, can track the input with the switch closed indefinitely and then go into the hold mode upon command.

A zero-order hold may be either a sample-hold or track-and-hold. When a device is called a zero-order hold, that means it's used as a signal recovery filter. There are various types of sample-hold recovery filters such as zero-order holds, first-order holds, fractional-order holds, and polygonal holds.

The term "sample-and-hold amplifier" can refer to either a sample-hold or a track-and-hold, and originates from the fact that operational amplifiers are used to make sample-hold circuits.

Although there's a technical distinction between the terms sample-hold and track-and-hold, it's automatically assumed that both functions are included in the term "sample-hold," as just about all sample-holds can also track and hold. The few circuits that can only sample for a short time, and cannot track the input, are clearly labeled this way.

To appreciate the difference between true sample-hold operation and track-and-hold operation, see Figure 2. In Figure 2a, a sample-hold periodically takes a sample of the input, a sinusoid in this case, and holds it for the rest of the time. In Figure 2b, a track-and-hold tracks the input for part of the time and holds it for the rest. Here, the track time and hold time are equal.

ZERO-ORDER HOLD

An important sample-hold application is reconstructing, or recovering, an analog signal that has been transmitted as a train of pulse samples, like those in Figure 3a. To reconstruct the original signal waveform, a sample-hold, or zero-order hold, retains the peak value of a sample until the next one arrives, thus filling in the spaces between them, as in Figure 3b. The result is a reasonable reconstruction of the original signal before it was converted to a pulse train. Ideally, the average of the reconstructed waveform, shown dashed in Figure 3b, is a near-replica of the original waveform, delayed by half the sampling period, T.

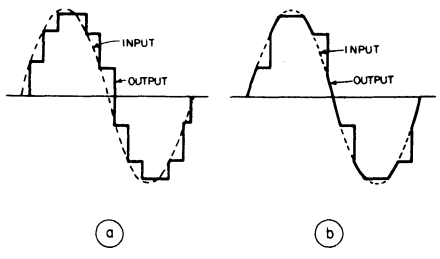


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Figure 2: A sample-hold can operate in two different ways. It can take a quick sample of the input and return right back to hold mode (a), or it can track the input for part of the time and hold it for the rest (b).

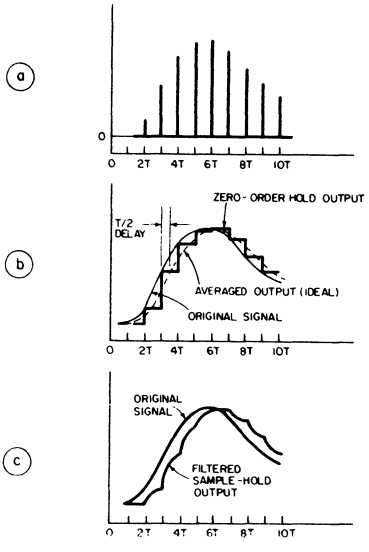

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Figure 3: A zero-order hold reconstructs an analog signal that's been transmitted as a series of pulse-samples (a). It does so by holding the amplitude of each pulse to fill in the spaces between them (b). Practical averaging uses a low-pass filter (c) that has more delay than the ideal averaging shown in (b).

If the staircase waveform of the output is objectionable, a low-pass filter following the zero-order hold will smooth the waveform further. This filter will add further phase delay, but the resulting reconstruction of the original signal is much better, as Figure 3c shows. The cutoff frequency of this filter must be determined from the sampling rate and the

bandwidth of the signal to be recovered. The lower the cutoff frequency, the better the smoothing.

The zero-order hold is a type of filter. As with other types of filters, its gain-phase characteristics are important to know. These gain and phase terms are plotted in Figure 4. The zero-order hold is obviously not an ideal filter with its (sinx)/x amplitude response. Nevertheless, it reconstructs signals respectably. Its gain is slightly more than 3dB down at a frequency of $f_S/2$, and it again goes to zero at integral multiples of the sampling frequency, f_S. There are some undesirable gain peaks at frequencies of 3/2 f_S, 5/2 f_S, etc. These peaks are frequently attenuated by a low-pass filter following the zero-order hold. A zero-order hold as a filter has a perfectly linear phase response (Figure 4b), which results in the constant phase delay of T/2 for the output signal.

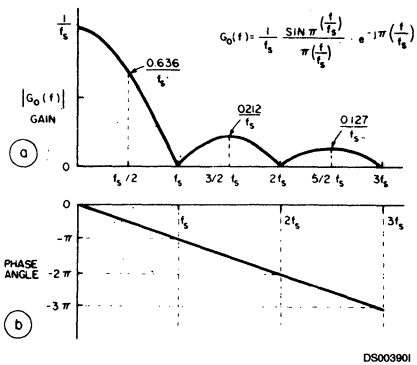

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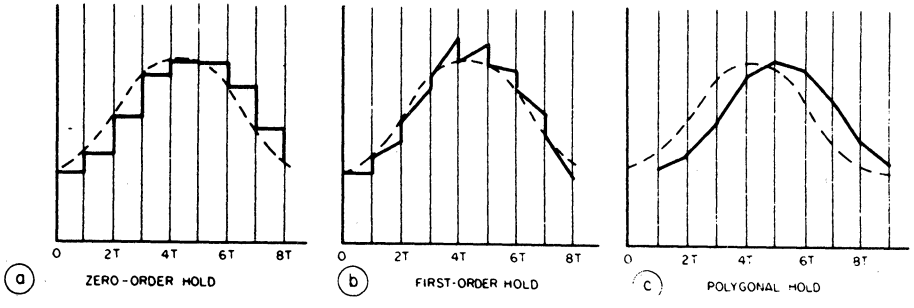
Figure 4: The gain response of a zero-order hold (a) in terms of the sampling frequency f_S takes the form of the absolute value of (sin x)/x. The phase response (b) is linear because of the constant time delay.

There are also more-sophisticated recovery filters than the zero-order hold circuit. These higher-order hold circuits, known as first-order holds, second-order holds, etc., reconstruct a signal more accurately than a zero-order hold (Figure 5). A first-order hold does this by retaining the value of the previous sample as well as the present one. It then extrapolates from existing data to predict the slope to the next sample, which hasn't arrived yet (Figure 5b). When a new sample comes in, it generates a slope proportional to the difference between this sample and the previous one. If the slope of the original signal hasn't changed much, the resulting error is small; for a constant slope, the error is zero. When the original signal reverses its slope quickly, the output "goes the wrong way," causing a fairly large error for one sample period.

An interpolative first-order hold, also called a polygonal hold, reconstructs the original signal much more accurately. This circuit also generates a line segment with a slope proportional to the difference between consecutive samples, but rather than extrapolate into the future, it interpolates between samples already received. Its accuracy is achieved at the expense of a delay of one sample period, which is necessary because a new sample must arrive before the line segment can be generated by starting from the previous sample.



SC002601

Figure 5: Three types of holds reconstruct an original signal (dashed curve) differently. The output of a zero-order hold (a) is steady between samples. A first-order hold (b) extrapolates a new slope that's proportional to the difference between the two most-recent samples. Its output error is zero during constant-slope portions of the signal. The polygonal hold (c) interpolates between the two most recent samples.

LOTS OF CIRCUIT VARIETY

Sample-holds come in many different circuit configurations, each suited to different speed and accuracy requirements. It's important to know the common configurations and how they operate to choose the proper type and apply it properly.

One configuration is popular because it's accurate and simple. This circuit, shown in Figure 6a, has a gain of −1 since $R_1 = R_2$; however, making R_2 larger than R_1 gives inverting gains larger than one. When the switch closes, hold capacitor C_H charges to the negative of the input voltage. The switch opens after the capacitor has acquired this voltage to the desired accuracy.

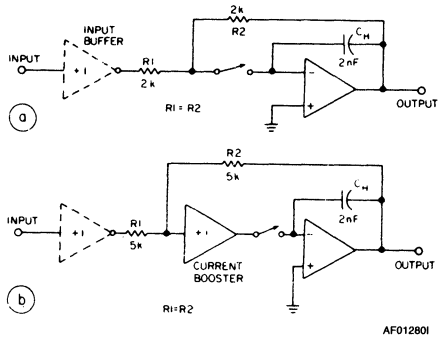


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Figure 6: This type of inverting, closed-loop circuit is both accurate and simple. The charge time constant, R_2C_H, of the basic circuit (a) is much too long for some applications. The current booster in (b) speeds up charging considerably. The input resistance, R_1, may be too low for some sources; the buffer raises it a great deal.

Although potentially very accurate, this circuit is not a fast sample-hold. The capacitor charges slowly since it has a time constant of R_2C_H; with practical values such as R_2 = 2k and C_H = 2nF, the time constant is 4μs. To reach a value within 0.01% of the input requires about nine time constants, or in this case, 36μs.

Speed can be improved considerably, as shown in Figure 6b, by adding an amplifier with current gain, inside the feedback loop. The operational amplifier must also be able to supply this current to the capacitor. Since these amplifiers have low output resistance, the circuit's time constant is much lower. For example, with the same valued capacitor and an amplifier output resistance of 20Ω, the time constant is only 40ns rather than 4μs. Now, only the amplifiers' output current capability limits charging.

With a maximum output current of 20mA from this amplifier to charge the capacitor and a 40-ns time constant, the capacitor takes just 1.2μs to charge to within 0.01% of final value. This is much faster than the 36μs for the previous circuit. Note that in the latter case, Figure 6b, R_1 and R_2 can be larger since R_2 no longer determines the charging time constant.

An input buffer amplifier improves this circuit further by boosting the input resistance to a much higher value than that of the input resistor R_1. In fact, the input resistance can be as high as 10^8 to 10^{12} ohms. Such high resistances are required when a sample-hold follows an analog multiplexer. In this case the buffer amplifier must be fast, since its settling time becomes part of the time required to charge the holding capacitor. The buffer can also be added to the circuit of Figure 6a. Both sample-holds in Figure 6 are referred to as closed loop, since the capacitor charging takes place within a closed loop circuit.

Figure 7 shows a noninverting closed-loop sample-hold in which A_1, that is serving as both an input buffer amplifier and an error-correcting amplifier, compares the output voltage to the input voltage, then charges the holding capacitor until this error is reduced to zero. Amplifier A_1 also gives this circuit a high input resistance.

Thanks to the error-correcting feedback in this sample-hold, A_2 need not be very accurate so long as its gain is roughly unity. Resistor R isolates the output of A_2 from the input of A_1 during hold mode.

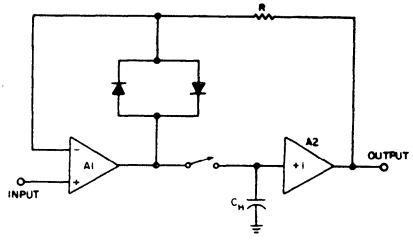

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Figure 7: Closed-loop sample-holds can also be noninverting. In this configuration, A_1 is both an input buffer and an error-correcting amplifier. When the switch closes, current from A_1 charges the hold capacitor until the output equals the input. The pair of diodes clamps A_1's output to keep it stable when the switch is open.

This circuit is both fast and accurate; how fast it charges the capacitor depends on the speed of A_1 and its output current capability. Two back-to-back diodes clamp A_1's output to its negative input so that A_1 remains closed-loop stable when the switch is opened. Note that in this circuit the switch must float up and down with the input voltage, whereas in the circuits of Figure 6 the switch always operates at virtual ground.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

Figure 8 shows another type of sample-hold circuit, which is versatile and can be operated in a number of closed loop configurations. This circuit is an operational integrator that can be enclosed in the feedback loop of A_1. In this case, however, A_1 is an operational transconductance amplifier; that is, one that produces an output current proportional to

its input voltage. The current charges the holding capacitor while the integrator's input remains at virtual ground.

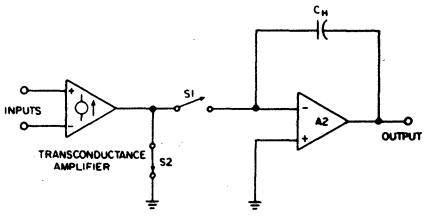

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Figure 8: Several closed-loop sample-hold configurations can be built around this circuit, shown without its feedback connections. Basically, it's an operational integrator driven by an operational transconductance amplifier, A_1.

In this circuit, the two switches operate out of phase. Switch S_1 closes to sample, then S_2 closes to reduce hold-mode feedthrough when S_1 opens again.

This circuit can be connected in different ways as a closed-loop sample-hold: Figure 9a shows the most commonly used connection, a noninverting sample-hold with a gain of +1; Figure 9b shows the noninverting connection with gain, and Figure 9c shows the inverting connection with gain.

Both of the switches in these circuits operate at virtual ground, an advantage in driving the switch and producing an accurate output voltage. This circuit has been successfully used in monolithic, hybrid, and modular sample-hold devices.

Another popular noninverting, unity-gain circuit is shown in Figure 10. It's basically the same as the one shown in Figure 1b, with two unity-gain buffer amplifiers. This type of open-loop sample-hold is commonly used in ultra-fast designs. In this case, a pulse transformer drives a fast diode bridge switch.

Normally, the supply voltage back-biases the diodes. Sampling is done by a fast-rise command pulse that turns on the diodes to charge the hold capacitor from the input buffer. Using ultra-fast buffer amplifiers and an appropriate diode-gate switch, such sample-holds can charge the hold capacitor to a full-scale change in as little as 30 nanoseconds. Because of the open-loop configuration, there is no problem with phase delays from output to input caused by a feedback loop. This means that the circuit is both fast and stable.

The input buffer in this circuit is difficult to design, for it must be both fast and stable while driving the hold capacitor load. Sampling switches, however, cause no such problems.

The basic sampling switch circuits commonly use junction FETs, MOSFETs, D-MOS FETs, and diode-gate switches. All of these can be both fast and accurate. The FET-type switches have the advantage of zero offset since they are purely resistive in the closed state. The diode-gate switch does have an offset voltage, however, which is minimized by properly matching the diode forward-voltage drops.

THE INFINITE-HOLD CIRCUIT

All sample-hold circuits have the problem that once they are in the hold mode, the charge will gradually leak off the hold capacitor due to switch leakage, capacitor leakage, and output amplifier bias current. It was mentioned previously that a digital register can store a number equivalent to a voltage value as long as necessary.

The "infinite hold" circuit uses this principle to store a voltage value for any required time without any drift due to leakage. The circuit, shown in Figure 11, is basically a tracking A/D converter, with its output from the analog feedback line rather than from the counter. It consists of a D/A converter, up-down counter, clock, and analog comparator. The circuit operates by directing clock pulses into the up or down count inputs of the bidirectional binary counter that controls a D/A converter.

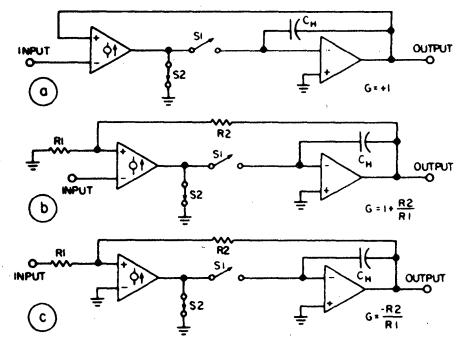

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Figure 9: Here are three different ways to connect the input and feedback to the partial circuit in Figure 8. The circuit in (c) has unity gain if the input (R_1) and feedback (R_2) resistors have equal values.

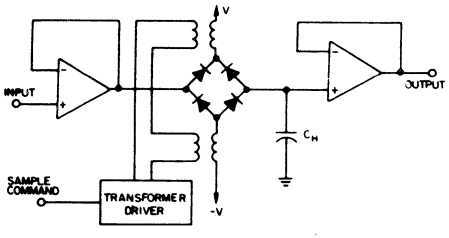

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Figure 10: Ultra-fast sample-holds often use a circuit like this. It has a diode-bridge switch and operates open-loop. The diodes are biased off until a sample command arrives; then the pulse transformer's output turns on the diodes, which connect the input buffer amplifier to the hold capacitor. A 30-ns full-scale change is possible.

An analog comparator tests the output voltage of the D/A converter against the input voltage and directs the clock pulses to the counter so that the converter's output voltage changes toward the input. When the input voltage is reached, the circuit oscillates within one count of the input value. When the sample command goes low, the counter retains its contents indefinitely until the next sample is taken.

This circuit is not particularly fast since it must go to each new value one count at a time until the input voltage is reached. Different counting techniques will speed it up, however. Its accuracy depends on the resolution of the D/A converter; ±0.01% accuracy requires at least 12 bits.

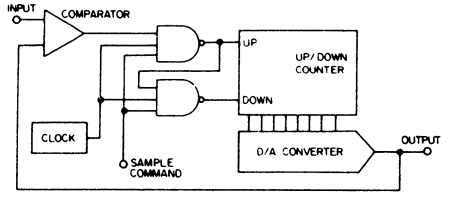

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Figure 11: Sometimes called an "infinite hold," this circuit can hold a sample indefinitely without the droop that happens with capacitor storage. It's an A/D converter with its output taken from the analog feedback line. A high on the sample command line lets the output follow the input. A low freezes the count inputs, so the count doesn't change.

KNOW YOUR CIRCUIT

Sample-hold: The generic term used for track-and-hold, zero-order hold, or sample-and-hold amplifier, it describes basically a circuit that acquires an analog input voltage and accurately stores it for a specified period of time.

Track-and-hold: A sample-hold circuit that can continuously follow the input signal until switched into the hold mode.

Signal-recovery filter: A circuit that reconstructs an analog signal from a train of analog samples.

Zero-order hold: A sample-hold circuit used as a signal recovery filter. So called because its output represents the first term of a power series approximation to the input.

First-order hold or extrapolative hold: A complex signal-recovery filter that predicts the next sample value by generating an output slope equal to the slope of a line segment connecting previous and present samples. In a sense, it works toward the future.

Polygonal hold, or interpolative hold: A complex signal-recovery filter that generates a straight-line segment output that joins the previous sample value to the present sample. It uses available data to reconstruct the signal more accurately than other hold circuits, but with a one-sample-period delay.

Infinite hold: AN analog/digital sample-hold that digitally holds an analog voltage indefinitely without the decay of capacitor storage.

Closed-loop sample-hold: A sample-hold circuit that charges the hold capacitor within a negative feedback loop during sampling to achieve high accuracy.

Open-loop sample-hold: A sample-hold circuit that does not enclose the hold capacitor within a feedback loop.

Chapter 4
Analog Switches

AO12
Switching Signals With Semiconductors

Analog switches are fast, low cost, and work well with the high impedance of most signal circuits. Often they can replace reed relays

Until recently, signal routing and switching were controlled almost exclusively by electromechanical relays and mechanical switches. Now the electronic switch, also known as the analog switch, is being used for many such applications. Initially the electronic switch replaced relays in many applications. But design engineers soon realized that analog switches have unique characteristics that allow them to do things mechanical switches could never attempt. In particular, an ordinary electronic switch is about one thousand times as fast as a conventional relay.

Further, the electronic switch is smaller, lighter, longer lived, more reliable and often lower in cost than an equivalent relay. These characteristics have allowed the development of such things as low cost, high speed, analog-to-digital and digital-to-analog converters, fast sample-and-holds, video switching and many other circuits. Usage continues to grow and a number of different types of electronic switches have been developed for specific types of applications.

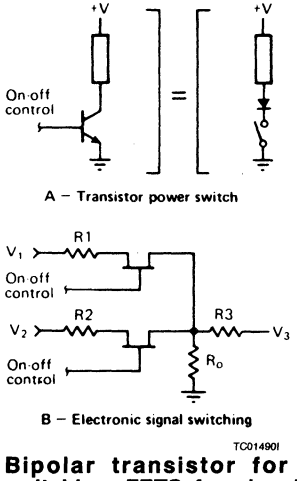


Figure 1: Bipolar transistor for power switching, FETS for signal

Transistors have been used as switches ever since they first appeared, but usually as on-off devices for controlling lights, relays, and other leads, as indicated in Figure 1A. A diode is added to the equivalent circuit to show that current can flow in only one direction. Figure 1B shows the nature of electronic switching. The signals, voltage V_1, V_2 and V_3, are usually low level and often have high impedance; they represent the flow of information rather than power. Further, the signals may be combined to produce new signals.

Analog switch vs reed relay. The reed relay is closest to the analog switch in size, speed, cost and usage; therefore it can serve as a basis for comparison. Current through the coil (Figure 2A) of the reed relay, opens or closes the associated contacts through which the signal passes.

The control input to the analog switch usually comes from TTL or CMOS logic, which the driver translates to the voltage needed to turn on or turn off the channel. The channel is a field effect transistor (FET), with the signal to be switched fed to the source while the drain is the output terminal. Depending on the voltage the driver imposes on the gate, the channel is either a very high impedance—many megohms—or well below 100ohms.

Advantages of the reed relay include the ability to handle much larger signals and a much lower resistance when on.

Some analog switches are severly limited in the magnitude and polarity of the signals they can handle. Because of the nature of semiconductors, the voltages applied to source and drain cannot be allowed to vary indiscriminately but must be held within a range established by the characteristics of the device as well as by the voltage applied to the gate by the driver. If the range is exceeded, either the channel goes to the wrong state, or some intermediate state, or the device may be destroyed.

With respect to "on" resistance, it will be a long time (if ever) before analog switches with the low "on" resistances of relays are manufactured. However, the applications that require extremely low "on" resistance are few and most signal switching is done into high impedance loads.

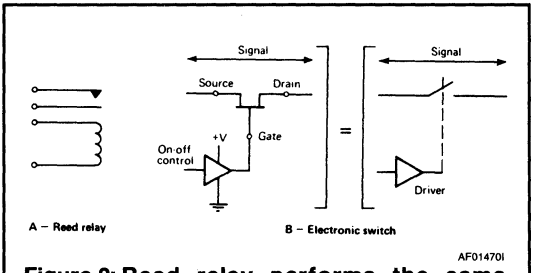
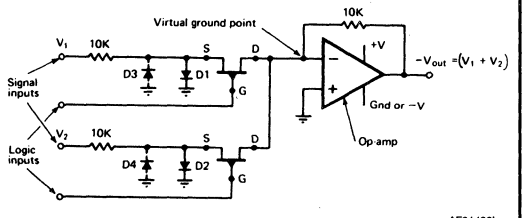


Figure 2: Reed relay performs the same function as an electronic switch

Since electronic components are much smaller than their mechanical counterparts, many more switches can be put into one package, greatly reducing parts count as well as space and volume. In addition, electronic switches have no moving parts and consequently no contact bounce. They are, however, sensitive to static electricity and thus good handling procedures should be used during assembly. The life of a solid switch is orders of magnitude greater than a relay and no maintenance is required. Driving the switch is easy since it can interface directly with TTL or CMOS logic without requiring diode protection, as a reed relay normally does. Pricing on a per channel basis is often lower for the

analog switch than the reed relay, although some high speed switches are priced higher. But the most significant advantage of the electronic switch remains its extremely fast switching speed. Its ability to switch in less than 1 microsecond has opened up possibilities that are inconceivable with a reed relay.

Switch functions duplicate those commonly found in reed relays: form A (normally closed), form B (normally open) and form C (double throw). Both single pole and multi-pole circuits are available. Semi-conductor technologies typically used include bipolar, PJFET, NJFET, MOSFET, VARAFET and CMOS.



AF01480I

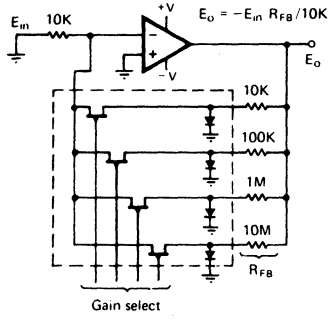
Figure 3: Output of the op-amp is determined by both the signal inputs and the logic inputs

VIRTUAL GROUND SWITCH	POSITIVE SIGNAL SWITCH
Output of switch must go into the virtual ground point of an Op Amp (unless signal is below 0.2).	Can switch positive signals only unless a translator driver is used.
No quiescent current.	No quiescent current.
Does not need driver, can be driven directly by TTL.	Does not need driver, can be driven directly by TTL.
Lowest cost.	Low cost.

The P-channel JFETS. The simplest switch to understand and operate is a Junction Field Effect Transistor having a channel doped with "positive" impurities—the PJFET. The PJFET channel is on (low resistance) in the absence of any control signal. When the voltage at the gate terminal is made more positive than either the drain or the source terminal (by a minimum amount), the switch is turned off (high resistance). This phenomenon is known as the pinching-off of the channel through which the signal is flowing, and the voltage required to do this is called the pinch-off voltage. This voltage can be obtained directly from an open collector TTL or CMOS logic operating at +5 or +15V. The PJFETS have no quiescent current and do not require external power.

PJFETS make excellent special function switches. An example is switching signals into the virtual ground (inverting) terminal of an op amp. The PJFETS in the two-input circuit of Figure 3 (Note: the arrowhead orientation signifies P-channel) can switch signals in the hundreds of volts as long as the op amp can handle such voltages. The only thing to keep in mind is that the current through each PJFET must be kept within its specified value. The solid line diodes D1 and D2 at the inputs limit the voltage at the source of the PJFET to about 0.7 volt and also shunts positive inputs to ground when the switch is off. With diodes D3 and D4 in place, the circuit can switch ±100 volts. The diodes limit the input to the PJFET to ±0.6 volt, but this is adequate since the op amp is actually forcing this point—the drains of the PJFETS—to ground.

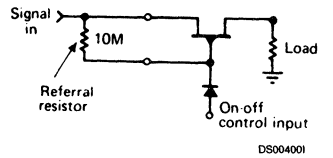
In Figure 4, PJFETS are used to switch feedback resistors to provide an amplifier with 16 different programmable gains.



AF01490I

Figure 4: Programmable gain op-amp has 16 levels of gain, from 1 to 1,000

Another special function switch built using PJFETS handles only positive signals. This switch requires an external referral resistor, Figure 5, for proper operation, but is ideal for switching into the positive terminal of an op amp.



DS004001

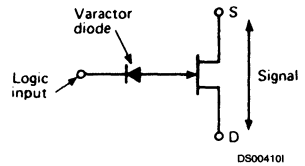
Figure 5: Analog switch handles only positive voltage signals

The N-channel JFET. An N-channel JFET—a JFET with the channel doped with "negative" impurities—is also turned on with no control signal applied, and is driven off by making the gate terminal more negative than source and drain. Since the outputs of TTL and CMOS logic gates are either a positive voltage level or near zero, a driver is required to do level shifting and generate a negative control signal. Most NJFET switches come with the drivers built in. Drivers for NJFET gates are usually bipolar, or combined bipolar/MOS: they require significant quiescent currents and therefore consume power.

The negative impurities used in NJFET channels have extra electrons, which are far more mobile than the "holes"

of PJFETS channels. As a result, the NJFETS have the lowest on resistance.

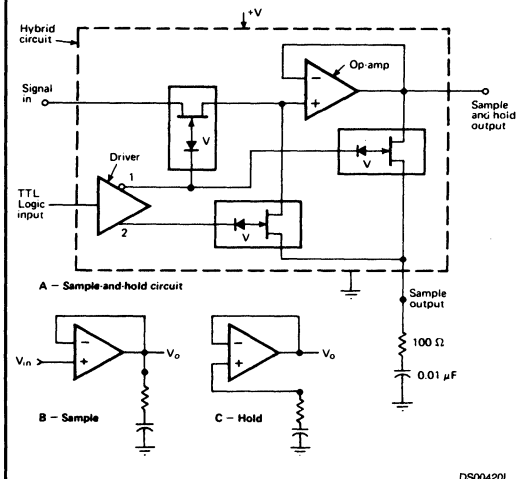
VARAFET switches. In some applications, such as sample-and-hold circuits, low charge injection is critical. For these applications the VARAFET gate, Figure 6, was developed. The gate consists of an NJFET with a varactor diode in series with the gate terminal. An NJFET by itself is not satisfactory because it will inject charge into the signal path when it is turned on and will thereby distort the output.



DS00410I

Figure 6: Use of NJFET plus varactor diode for sample-and-holds

Varactor diodes can store charge and thus they prevent most of the injected charge from entering the channel. The varactor diode also eliminates the referral components otherwise required for switching NJFET transistors. Figure 7A shows a sample-and-hold using VARAFET gates. When a sample of the analog input is wanted, the logic signal applied to the driver causes output *1* to go low and *2* to go high. This puts the circuit into the configuration shown at 7B. When this sample period is over, *1* goes low, *2* goes high, and the circuit is put in the hold mode, Figure 7C.



DS00420I

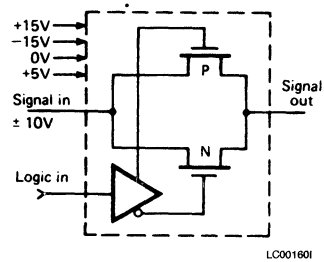
Figure 7: Sample-and-hold circuit, A, uses three VARAFETS. Circuit configuration when sampling is shown at B, and hold mode at C

MOSFET switches MOSFETS (Metal Oxide Silicon FET), unlike JFETS, are off when no control voltage is applied to the switch. They are turned on when the appropriate signal is applied to the gate terminal. MOSFET devices were among the first switches on the market but are now used in very few applications. Their only outstanding feature is more switches per package — up to six — than other technologies covered in this article.

CMOS switches. Complementary MOSFET (CMOS) switches are now beginning to dominate. In applications where the special function switches — the PJFETS, NJFETS, VARAFETS — are not needed or cannot be used. CMOS switches are the preferred devices.

CMOS switches consist of drivers and gates made from CMOS, usually on a single chip. A simplified circuit is shown in Figure 8. The on-off input signal can be obtained from a CMOS logic gate or TTL, either regular or open collector pulled to 15 volts. Switching speed is higher for 15 volt logic. When the logic input is low, both the P and N transistor are off. When the logic input is high, both transistors are on and signals up to ±10 volts can flow either way through the circuits.

A summary selection guide to analog switches is given in the table which appears at the top of these facing pages.



LC00160I

Figure 8: CMOS switches have extremely low drive and quiescent currents

4

LOWEST QUIESCENT CURRENT		HIGHEST SPEED	LOWEST $r_{DS(on)}$	
Monolithic CMOS driver gate combination (low cost).	Monolithic CMOS driver gate combination (low leakage).	Lowest charge injection. CMOS driver and VARAFET gate.	Bipolar/MOS driver with NJFET gate.	Bipolar driver with NJFET gate (low cost).
Low quiescent current.	Highest speed switch.	Lowest charge injection.	Lowest $r_{DS(on)}$	Lowest $r_{DS(on)}$
Lowest cost (for this category).	Lowest quiescent current.	Very fast.	Fast. Moderate leakage.	Only switch with true chip enable.
Good speed with moderate $r_{DS(on)}$ and leakage.	Lowest leakage resulting in lowest error.	Very low quiescent current.	High quiescent current.	Low cost.
Overvoltage protection to ±25V.	Lower cost.	Ultra low leakage.	Highest cost.	Moderate leakage quiescent current.
Can switch up to ±13V signals with ±15V supplies.	Can switch signals almost to the supply rails.		Switches ±10V signals with ±15V supplies.	Average speed.
				Switches ±10V signals with ±15V supplies, or ±12V and ±18V supplies.

AO03
Understanding and Applying the Analog Switch

INTRODUCTION

Historically the analog switch has been thought of as a solid state relay, and many of its common applications are areas where the relay dominated the scene a few years ago. Routing signals in telephone exchanges is the most obvious example. More recently, however, as creative designers are becoming aware of the unique properties of the analog switch, a new generation of applications is emerging which were simply not possible using relays. The ability to change the gain of an amplifier, or the time constant of an integrator, in less than a microsecond has far-reaching implications in real-time analog signal processing.

The purpose of this note is twofold. Firstly, to act as an introduction to analog switches to those who have hitherto only used relays. Secondly, to compare and contrast the features of the different switch families and to illustrate their use with practical applications.

RELAYS AND THE ANALOG SWITCH

Since the class of relay closest to the analog switch in terms of cost and packaging is the reed relay, the comparison which follows is confined to this type of device. Reed relays have three advantages; they are easy to apply (current through a coil opens or closes isolated contacts), they will handle signals of the order of hundreds of volts, and their ON-resistance is low. So what does the solid-state analog switch have to offer? It outperforms the mechanical relay in almost every other specification. It is much faster, does not suffer from contact bounce problems, is more rugged since there are no moving parts, has several times the number of switches per package, and is easier to drive since the switch can interface directly with TTL without requiring back-EMF diode protection, etc. The salient features of the two switch types are given in Table 1.

Analog switches can be thought of in terms of form A, B, and C relays; it is only necessary to add some external connections as shown in Table 2. The table shows devices from the IH5040 series, with the switch states for a logic "1" input. In the normal state (logic "0" input) the contact closures drawn as closed would be open and vice versa.

THE AVAILABLE SWITCH TYPES

There are basically four different switch types on the market at the present time. They may be summarized as follows:

a. Combination FET (MOS or Junction) and bipolar hybrid designs.
b. Monolithic CMOS Designs.
c. Simple low-cost JFET "virtual ground" designs.
d. Simple low-cost "positive signal" designs.

Combination FET and Bipolar Hybrid Designs

These may be described as first generation single package analog switches. In many respects they are equivalent to the μA709 in the op-amp world; both deserve credit for pioneering the concept of a complete building block in a single package, and yet both have been outdated by advancing technologies and design concepts.

This family is of hybrid construction and consists of a Bipolar, monolithic driver chip and MOSFETs or junction FETs as output devices. The driver stage is required to translate the TTL voltage levels to those suitable to drive the output stage; this is typically a 3V to +15V or a 0.8V to −15V translation.

4

TABLE 1

PARAMETER	FAMILY				
	TYPICAL REED RELAY	HYBRID FET & BIPOLAR SWITCH (IH5001)	CMOS SWITCH (IH5040)	VIRTUAL GROUND SWITCH (IH5009)	POSITIVE SIGNAL SWITCH (IH5025)
SIGNAL HANDLING (V_S = ±15V WHERE APPLICABLE)	±300V	±8V	±14V	±15V (NOTE 1)	0V TO +10V (NOTE 2)
ON RESISTANCE	0.1Ω	30Ω	75Ω	100Ω	100Ω
SPEED(t_{on}/t_{off})	1000/500μs	0.5/1.0μs	1.0/0.5μs	0.5/0.5μs	0.2/0.2μs
LOGIC COMPATIBILITY	NO	YES	YES	YES	YES
STEADY STATE QUIESCENT CURRENT (WHEN ON)	10mA @ 15V	3.5mA	10μA	NONE	NONE
COST PER CHANNEL @ 1000 PCS	< $1.00	$2.50	< $1.00	< $1.00	< $1.00

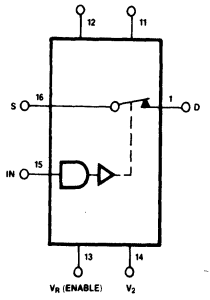
NOTE: 1. When used as recommended at the virtual ground point of an operational amplifier.
2. A method of switching +20V signals in the data sheet.

Table 2: Relay Equivalent Contact Forms

NOTE 1: Switch states are for logic "1" input

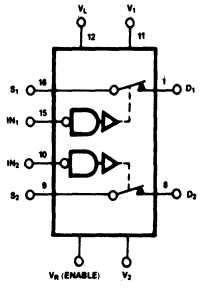
NOTE 2: Pin Connections are for DIP package

FORM A



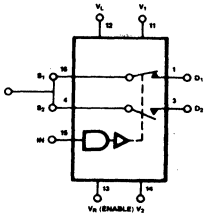
SS00560I

DUAL A



SS00570I

FORM C



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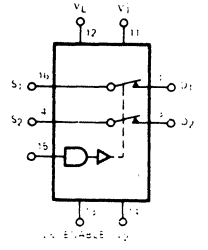
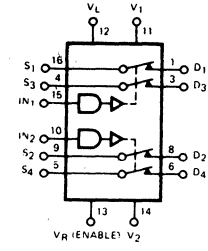


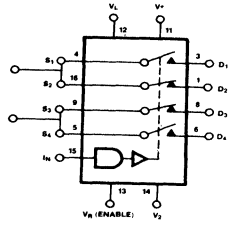
DPST

IH5044 (R_{DS} (ON) <75Ω)

SS00690I

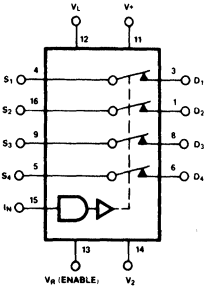


SS00600I



SS00610I

DUAL B



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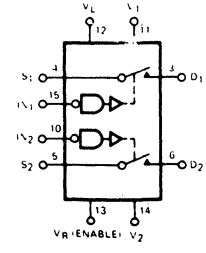
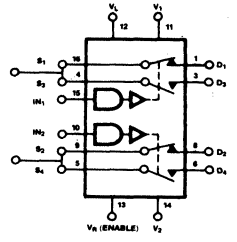


SS00630I

DUAL C



SS00640I

The DG111 through DG125 grouping has a bipolar driver and a PMOS monolithic output stage, with up to six (6) independent MOSFETs on each chip (Figure 1). These are enhancement mode MOSFETs and are turned off with no power applied. The range of switching is ±10V with +20V and −10V power supplies. Typical $R_{DS(ON)}$ is 70Ω for +10V signals, 150Ω for low level signals and about 300Ω for −10V signals. Notice the switch does not show a constant impedance as signal level is varied. To minimize this modulation effect by the signal, these parts should work into relatively high load resistances (i.e., $R_L \geq 10K\Omega$).

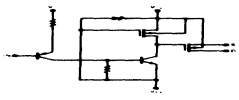
The DG126 through DG164 family, and also the IH5001 through IH5007, again have a bipolar driver chip for voltage translation, but discrete JFET chips are used as output stages here (Figure 2). Typical $R_{DS(ON)}$'s are in the 5Ω to 50Ω range (depending on Part #), and all are characterized

by a constant switch resistance. Typical analog switching levels are ±8V with ±15V supplies.

For both of the above families, the following are common characteristics:

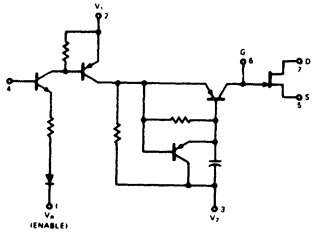
1. Construction is hybrid.
2. Switching speeds are typically 0.3μs and 1.0μs (t_{on} and t_{off})
3. Leakages are in 1nA range.
4. Charge injections are very similar.
5. Circuit power dissipation is very similar.

The new monolithic CMOS analog switches discussed in the next section will outperform these earlier hybrids in almost every parameter, will ultimately be much less costly to manufacture, and will undoubtably become the 741's and 101A's of the analog switch world.



DS006701

Figure 1: DG118 (One Channel)



DS006801

Figure 2: IH5001

Monolithic CMOS Designs

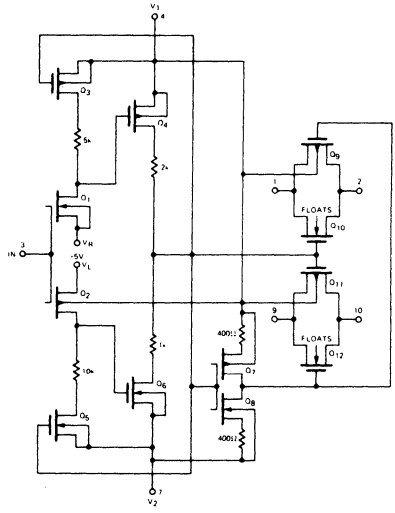
For all new designs, the CMOS switches should be considered along with the more specialized types described in c. and d. It will be shown later that the CMOS switch is extremely versatile; in fact, the only reason not to use it is in those instances where the much simpler (and less costly) specialized circuits can perform the task.

These switches are of monolithic construction and include part #'s IH5040 through IH5052. Each part is a complete driver and output stage combination and the family has the following salient features:

1. TTL compatible.
2. Switches up to ±14V with ±15V supplies.
3. Has overvoltage protection to ±25V signal inputs.
4. Draws < 100μA (1μA typ.) from ±15V supplies.
5. Break-before-make switching with typical $t_{on} \simeq$ 500ns and typical $t_{off} \simeq$ 250ns.
6. $R_{DS(on)} < 75\Omega$.
7. Improved reliability due to lower power construction and monolithic consumption.

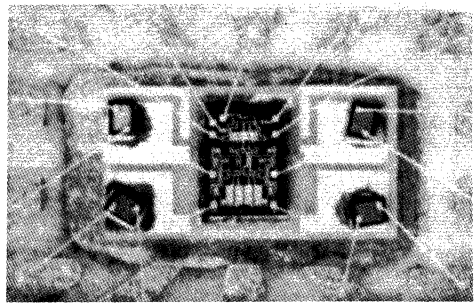
The use of CMOS processing allows the fabrication of a family of switches with superior parameters compared with the older hybrid techniques. For example, the CMOS parts can switch within 1V of power supplies (±14V with ±15V supplies) while parts in a group a) switch ±8V with ±15V or ±10V with +20V and −10V typically. Also, the CMOS quiescent current is typically microamperes instead of milliamperes; thus it is ideal for portable equipment. CMOS is compatible with any logic, while the hybrid families are strictly designed for TTL (+5V logic).

The CMOS switches are offered in a variety of switch configurations, i.e., SPST, DUAL SPST, DPST, DUAL DPST, DPDT, 4PST, etc. Each different part is merely a metal mask option of the basic CMOS device. A typical schematic is shown in Figure 3.

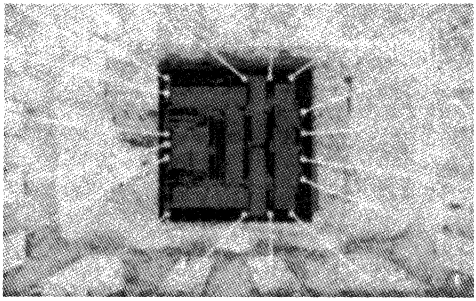


DS006901

Figure 3: IH5042 Schematic



A. Hybrid Analog Gate Using Monolithic Bipolar Drivers and FET Switches



B. MONOLITHIC CMOS ANALOG GATE

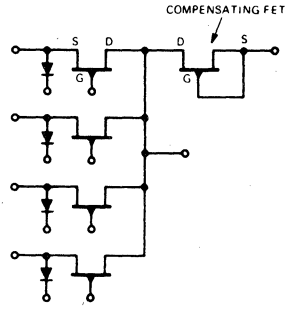
Virtual Ground Switch Family

The *Combination FET and Bipolar Hybrid Designs and Monolithic CMOS Designs* are families which feature great versatility; while there are differences in signal handling capability, speed, power consumption, etc., between the two groups, there is little doubt that both families will handle most switching needs. The disadvantage of this added versatility is the price one pays for it. If you need the flexibility to switch A.C. signals into any load, and up to ±10V amplitude, then you need either of the a) or b) groups. On the other hand, if you are switching into the inverting input of an operational amplifier, or are switching low level signals, the IH5009 through IH5024 provides the best cost performance tradeoff.

The IH5009 family came into being at Intersil to fill the need for a $1 per channel switch function. It was found that 40% of all switching applications encountered could be satisfied by a simpler switch than the driver/gate combination designs. Since the switch could be simpler, the costs were less and customer objectives could be met. This "designing for need" concept led to the P-channel JFET analog switch (IH5009 family). A P-channel was chosen as the gating element since it could be driven directly from positive going logic (TTL); thus the TTL gate acted as a driver for the FET and resulted in an immediate cost saving to end users, since previous designs had required a separate driver.

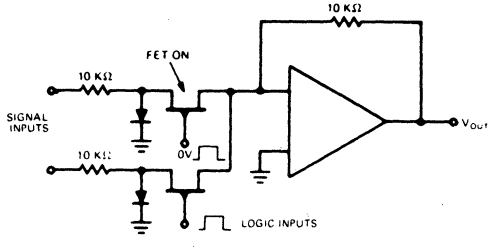
The phrase low level switching is a misnomer as applied to the IH5009 family of "virtual ground switches" (the negative feedback point of an op amp is a virtual ground). In reality, the switch could handle ±100V if one could find an op amp capable of ±100V output swings, since the signal appearing at the virtual ground is attenuated by the open loop gain. When the switch is off, it is the diodes that limit the swings, at the JFET, to levels compatible with the logic.

The diodes from the source to ground limit the swing at the JFET to +0.7V typically so the circuit operates correctly regardless of the signal voltage.



DS007001

Figure 4: IH5009 Schematic



DS007101

Figure 5: Switching At Virtual Ground of An Op-Amp (2 Channels Shown)

While the intent of the 5009 family was to reduce cost, some unique advantages accompany this reduction:

1. Since the TTL logic element is the driver, the switch is very fast; this implies that most analog switches are speed limited by the driver or translator and this is true. If the driver takes 1μs to switch from +15V to −15V then t_{off} time of driver-gate combination (N-channel) will be approximately 1μS. Only in the 5009 and the 5025 family is the FET speed capability fully utilized; this then turns out to be inherent in the design. Typical t_{on} times are 50nS and typical t_{off} times are 150nS.
2. The method of switching is current switching and the output/input relationship follows the well known inverting feedback amplifier gain equation. If the op amp has high open loop gain, the signal present at summing junction will be μV or mV and therefore, the output is just the input current times the total feedback resistance. Thus, for 0.1% or 0.01% switching accuracy, a feedback JFET is used in series with the feedback resistor (R_f); this feedback FET compensates for the error due to $I_{in} \times R_{DS}$ loss at the input (R_{DS} = "on" resistance of PJFET). In the 5009 family, a "compensating FET" is included in the package specifically for this purpose (Figure 6). The two FETs track so the gain tracks through temperature and system accuracy can be maintained.

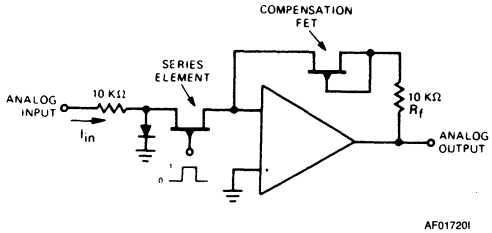


Figure 6: Use of "Compensating FET" To Reduce $R_{DS(ON)}$ Error

The 5009 series is broken up into two different groups. All the odd-numbered parts (5009, 5011, etc.) are designed to be used with TTL open collector logic (+15V power supply) while the even-numbered ones are designed to be used with +5V TTL logic. For odd-numbered parts, the JFETs have a pinch-off voltage of 4V to 10V and a maximum $R_{DS(on)}$ of 100Ω (65Ω typical) and the even numbers have a pinch-off range of 2V to 3.9V and a maximum $R_{DS(on)}$ of 150Ω (90Ω typical).

For both even and odd numbers, the match between any two channels is better than 50Ω and versions at 25Ω, 10Ω, 5Ω are available at increased cost over the basic 50Ω match. Additional information on the 5009 series is given in Intersil Application Note A004 "The IH5009 Series of Low Cost Analog Switches."

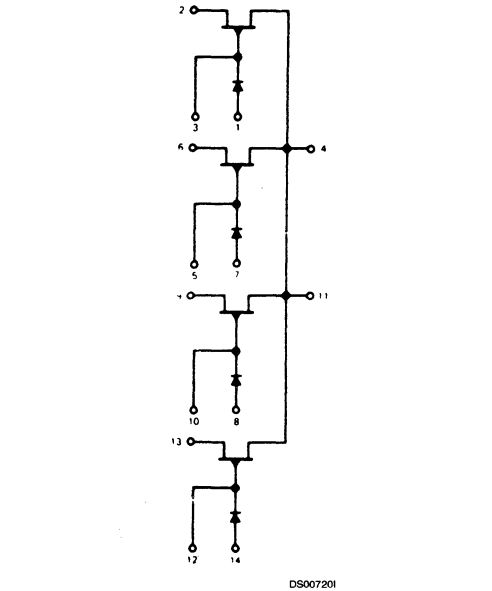


Figure 7: IH5025 Schematic

Positive Signal Switch Family

Just as the 5009 series fits a particular need for virtual ground switching applications, the IH5025 through IH5038 fits into a certain niche when only positive signals are switched. The 5025 series has been designed to switch any signal from 0V to +10V using TTL open collector logic (+15V power supply). Signals up to +25V can be switched by using a +30V supply at open collector terminal point. There is no restriction on the load, as in the 5009 family, and load resistances from 50Ω to infinity are easily handled. A typical switching circuit is shown in Figure 8 below:

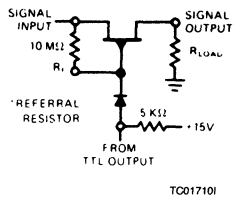


Figure 8: Typical Switching Circuit (One Channel)

Notice that no op amp is required to be part of the switching circuit, as is the case in the 5009 family. The disadvantage of this series is that negative signals cannot be switched unless external parts are added as in Figure 9.

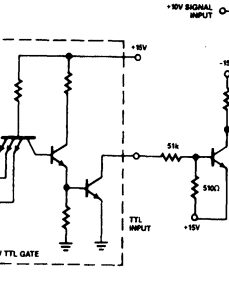


Figure 9: Switching Bipolar Signals Using The IH5025

Thus, by adding a PNP (2N3638 or 2N2907, etc.) and two resistors, the 5025 family becomes just as versatile as any other analog switch. Of course, open collector logic must still be used. When switching only positive signals, so that the circuit is driven directly from logic, speed is very fast; in fact, $t_{(on)} \approx 50ns$ and $t_{(off)} \approx 200ns$ up to $R_L = 1K$ loads ($C_L \leq 10pF$). When driving through PNP stage shown, speed is considerably reduced (to 300nS, 1 μs for $t_{(on)}$, $t_{(off)}$ respectively).

The 5025 family is broken up into 2 distinct groups, all of which have a pinch-off range of 2V to 3.9V. The odd-numbered parts have a maximum $R_{DS(on)}$ of 100Ω and the even numbers have a maximum of 150Ω; the difference between the two groups is that a larger geometry FET is used for odd-numbered parts. This larger geometry, while producing a lower on resistance, also inherently has about twice the charge injection when compared with the even-numbered parts. This is specified at 20mV maximum into 10,000pF for all parts. Typical charge injections are 7mV for even-numbered parts and 14 mV for odd-numbered parts.

As with the 5009 family, the 5025 series has a channel to channel $R_{DS(on)}$ match of 50Ω or less, with typicals running in the 25Ω area.

While the 5025 family has been targeted for use with TTL open collector logic, it can be used with 5V logic under the restraint that a maximum of 1V signal is switched. While this is rather restrictive, there are a few applications where this 1V maximum would be no problem; i.e., when switching transducer signals directly.

COMPARING THE PARAMETERS

Table 1 compares the key features of different switch types. A more detailed description of specific parameters follows:

Signal Handling

It has already been pointed out that one of the primary differences between relays and semiconductor switches is the degree of isolation between the control signal and the signal being switched. In the case of the semiconductor switch, the maximum analog signal that can be handled is related to the characteristics of the FETs or MOSFETs, and the supply voltages. When the switch itself is an N channel JFET, which in the absence of any gate bias is in the ON state, the device is held off by driving the gate towards the negative supply. Clearly, if the potential on the drain or source comes within V_p (the pinch-off voltage) of the gate, the device will turn on. With MOSFETs an analogous situation exists: The analog signal modulates the gate bias and can give rise to incorrect switch states if the recommended signal amplitudes are exceeded.

For virtual ground family (IH5009, etc.) the situation is somewhat different. The maximum signal which can be handled at the switch itself is only +700mV; however, when used as recommended at the virtual ground point of an op-amp, signals at V_{in} and V_{out} may be much larger, as previously stated (i.e., ±100V). It is worth noting that low level signals, such as those from a thermocouple, may be switches using an IH5009 without the need for an op-amp provided the amplitudes are less than 700mV.

On Resistance

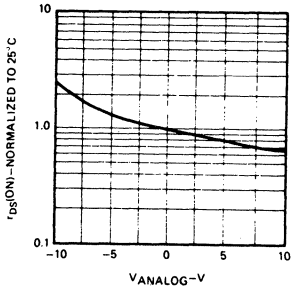
The ON-resistance of a good reed relay is substantially less than that of a typical analog switch. However, the widespread use of high input-impedance op-amp buffers has tended to decrease the importance of ON-resistance as a key parameter. It is almost always possible to design the circuitry interfacing with the switch so that an ON-resistance of 30Ω to 100Ω does not contribute a substantial error. Some of these techniques are illustrated in the applications given on pages 10 through 16.

In the case of the IH5009 series, the effective ON-resistance of the switches may be further reduced by use of the "compensating FET" as described earlier.

The linearity of ON-resistance as a function of the analog signal is dependent on the switch type. For junction FET switches, which are normally on, $R_{DS(on)}$ is independent of the analog signal (Figure 10). For PMOS switches, a negative gate bias is required to turn the device on. The analog signal thus modulates the bias voltage, giving rise to the characteristics seen in Figure 11. In the case of the CMOS switch, the $R_{DS(on)}$ of the "p" and the "n" channel in parallel tend to compensate, as shown in Figure 12.

The temperature characteristics of the different switch types are shown in Figure 13 through 15.

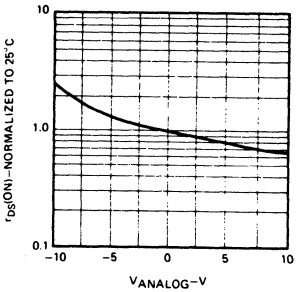
$r_{DS(ON)}$ AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE



OP01310I

Figure 10: JFET Switch

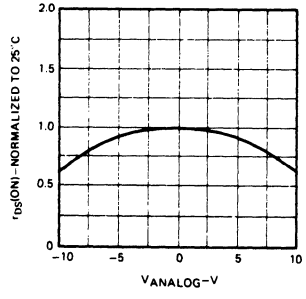
$r_{DS(ON)}$ AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE



OP01310I

Figure 11: PMOS Switch

$r_{DS(ON)}$ AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE



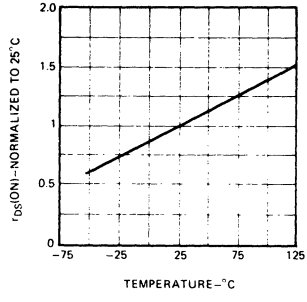
OP01320I

Figure 12: CMOS Switch

Speed

Table 1 shows the maximum switching times for various switch families. The waveform photos which follow illustrate the typical performance that can be expected under normal operating conditions. When the 5009 and the 5025 series are used in conjunction with an op-amp, the switching characteristics are usually limited by the slew rate and settling time of the op-amp. At the present time, for example, there are no monolithic op-amps capable of swinging 10 volts and settling to .01% in less than 500nS, even though the IH5009 is capable of such performance.

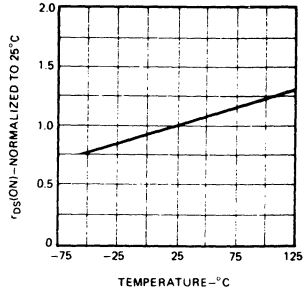
$r_{DS(ON)}$ AS A FUNCTION OF TEMPERATURE



OP01330I

Figure 13: JFET Switch

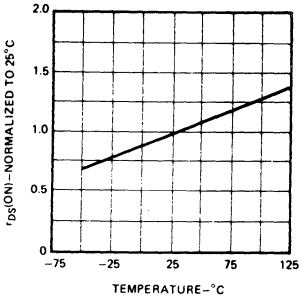
$r_{DS(ON)}$ AS A FUNCTION OF TEMPERATURE



OP01340I

Figure 14: PMOS Switch

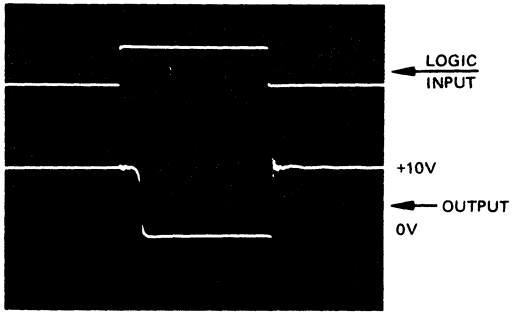
$r_{DS(ON)}$ AS A FUNCTION OF TEMPERATURE

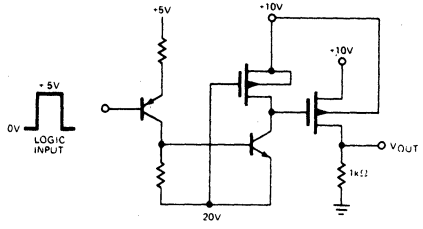


OP01350I

Figure 15: CMOS Switch

TYPICAL SWITCHING WAVEFORMS



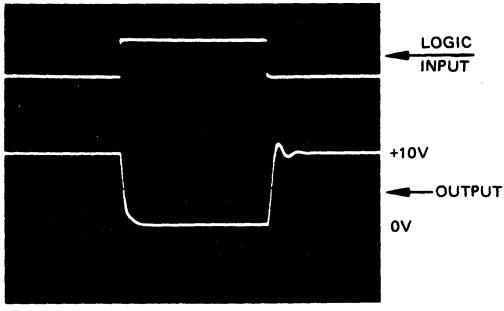


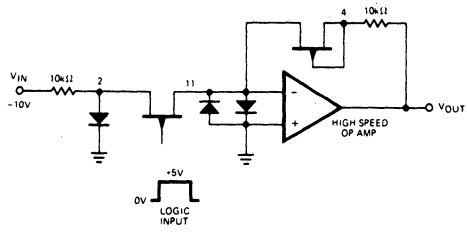
DS00730I

HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

WF00700I

Figure 16: DG118 (Note "Make-Before-Break" Action)



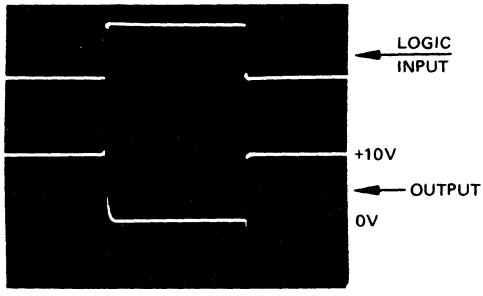


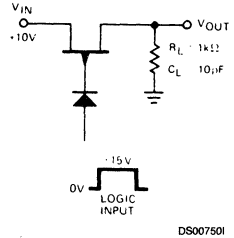
DS00740I

HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

WF00710I

Figure 17: IH5010



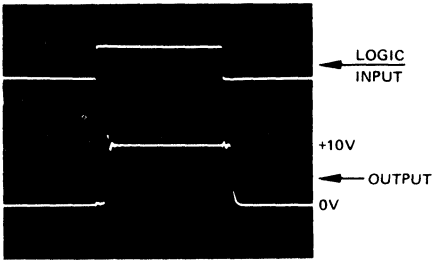


DS00750I

HORIZONTAL = 1 μs/div
VERTICAL (TOP) = 10V/div
VERTICAL (BOTTOM) = 5V/div

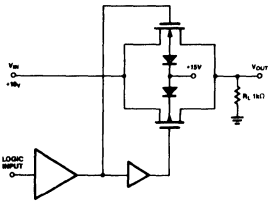
WF00720I

Figure 18: IH5025



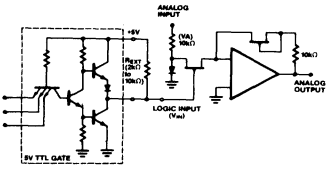
HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

WF00730I



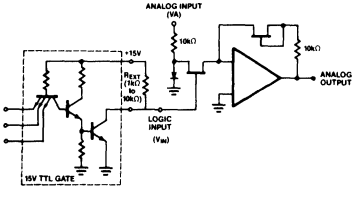
DS00760I

Figure 19: IH5041 (Note "Break-Before-Make" Action)



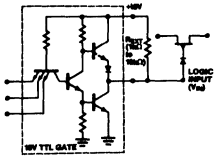
DS00790I

Figure 20: Interfacing IH5009 Family With 5V and 15V TTL



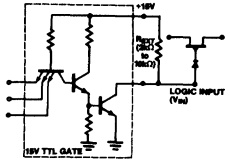
DS00770I

Figure 21: Interfacing IH5009 Family With 5V and 15V TTL



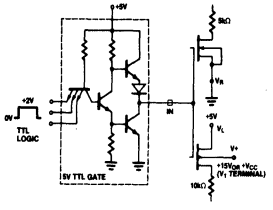
DS00800I

Figure 22: Interfacing IH5025 Family With 5V and 15V TTL



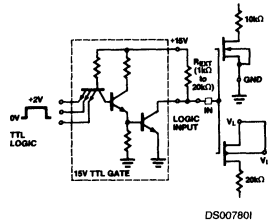
DS00820I

Figure 23: Interfacing IH5025 Family With 5V and 15V TTL



DS00810I

Figure 24: Interfacing IH5040 Family With 5V and 15V TTL



DS00780I

Figure 25: Interfacing IH5040 Family With 5V and 15V TTL

4

Logic Compatibility

All the popular solid state switches are compatible with TTL output swings; some require a pull-up resistor to guarantee correct operation however. Schematics showing how to interface with both standard (5V) TTL and high level open collector (15V) are given in Figure 20 through 25.

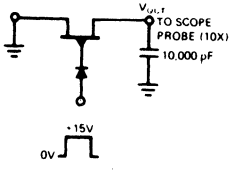
Power Supplies

The IH5009 and IH5025 require no external supplies; the only power used is gate leakage current drawn from the logic. The IH5040 CMOS circuits require ±15 volts and +5 volts, but again the only steady state power drain is a leakage current of 1μA typical. The hybrid switches utilizing bipolar drivers require ±15 volt supplies, and typically use 2mA in the ON condition. In the OFF state this current is much reduced and may only consist of a few microamps.

Charge Injection

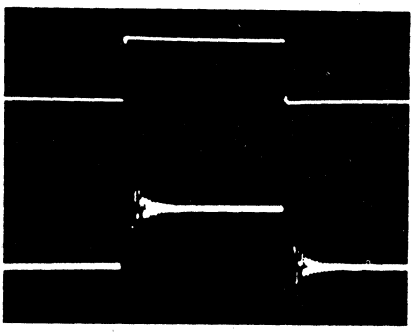
Most analog switches exhibit some degree of charge injection, due to capacitive coupling between the FET gate and the channel. This is a difficult parameter to define in quantitative terms since it depends on the rate of change of the gate drive signal.

However, it turns out that all the analog gates under discussion in this note exhibit similar charge injection characteristics. Using the IH5025, for example, in the test circuit of Figure 26, the waveform at the output is as shown in Figure 27. Note that the equivalent circuit of Figure 26 is simply a capacitance divider between the gate-channel capacitance and the load capacitance. For other operating conditions, the amplitude of the charge injection spike can be scaled proportionately. For example, doubling the size of the load capacitance will halve the spike amplitude.



DS00830I

Figure 26: Charge Injection Test Circuit Upper Waveform = Logic Input (10V/div) Lower Waveform = Output (5 mV/div) Horizontal = 1.0 μs/div



UPPER WAVEFORM = LOGIC INPUT (10V/div)
LOWER WAVEFORM = OUTPUT (5 mV/div)
HORIZONTAL = 1.0 μs/div

WF00740I

Figure 27: IH5025 Charge Injection

SUMMARY

As a guide to users trying to decide which of Intersil's family of analog gates is most appropriate for their system needs, the following summary may help to narrow the choice:

USE	INTERSIL FAMILY & KEY FEATURES
Any portable equipment	IH5040 CMOS family. Lowest power dissipation (25μW typ.). Compatible with CMOS logic levels.
Telephone switching	IH5009 or IH5025 family. Very fast switching to allow multiplexing many signals over the same line; lowest cost part.
Computer interfacing equipment (Disc readouts. Read and write circuits from memory drums, etc.)	IH5009 or IH5025 family for low cost.
Video or radar switching	IH5025 family for fastest speed.
Military Avionics	
a. Ground support material	DG116 thru DG164 family or IH5040 family when versatility is more important than cost.
b. Airborne equipment	IH5040 family for minimum waste of power and versatility to perform many different switching functions with the same part.
Any switching done in conjunction with operational amplifiers (i.e., switched integrators, switched gain, integrating sample and hold, etc.)	IH5009 family can be switched directly from logic in virtual ground applications.
Any system requiring switch to be off when power is off	DG116 thru DG125 family or IH5050 family. MOSFET and CMOS devices require power to be turned on.

APPLICATIONS — DG120 SERIES

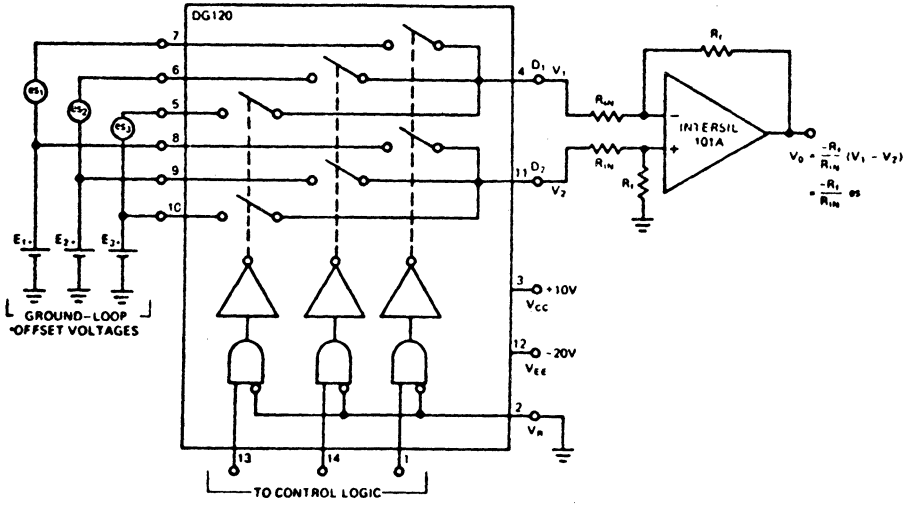


Figure 28: 3-Channel Differential Multiplexer

APPLICATIONS — DG120 SERIES (CONT.)

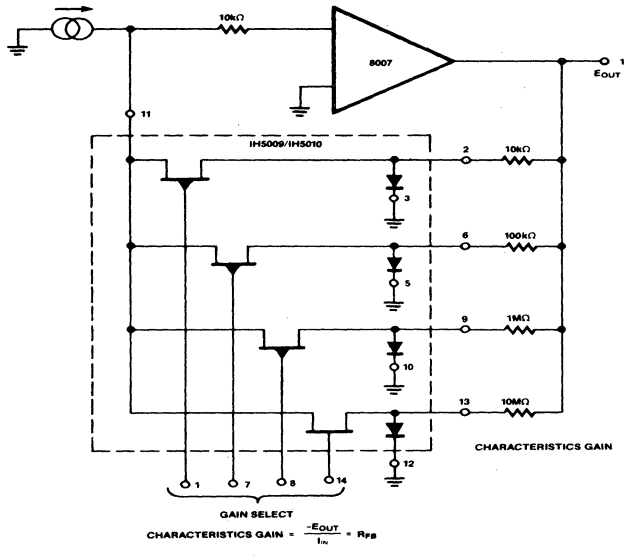


Figure 29: Gain Programmable Amplifier

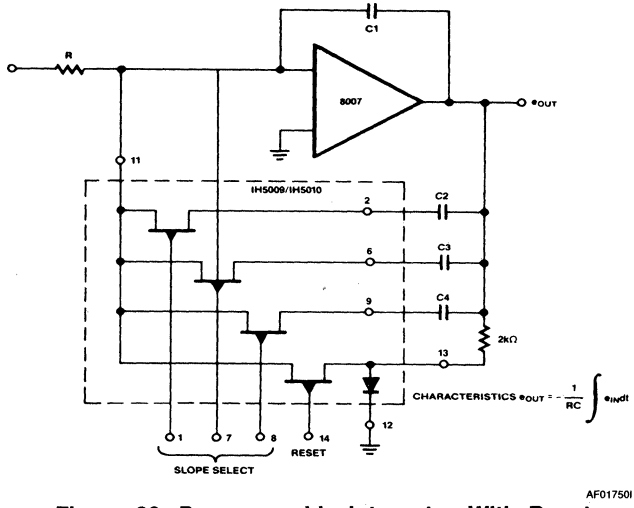


Figure 30: Programmable Integrator With Reset

APPLICATIONS — DG120 SERIES (CONT.)

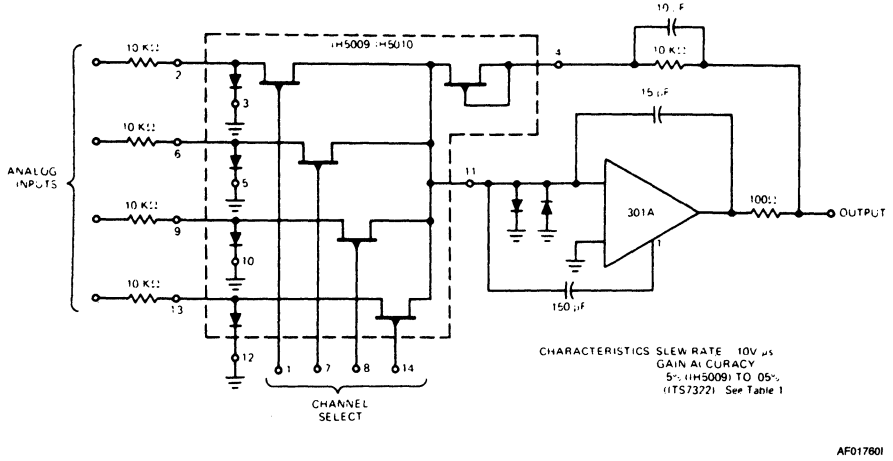


Figure 31: Low Cost 4 Channel Multiplexer

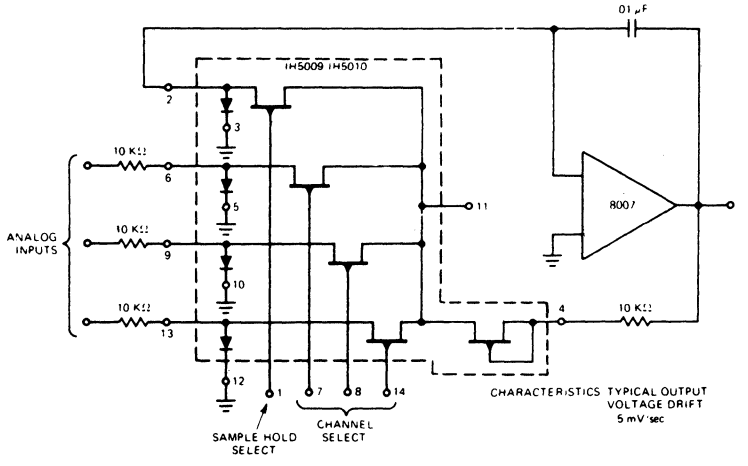


Figure 32: 3 Channel Multiplexer With Sample & Hold

APPLICATIONS — DG120 SERIES (CONT.)

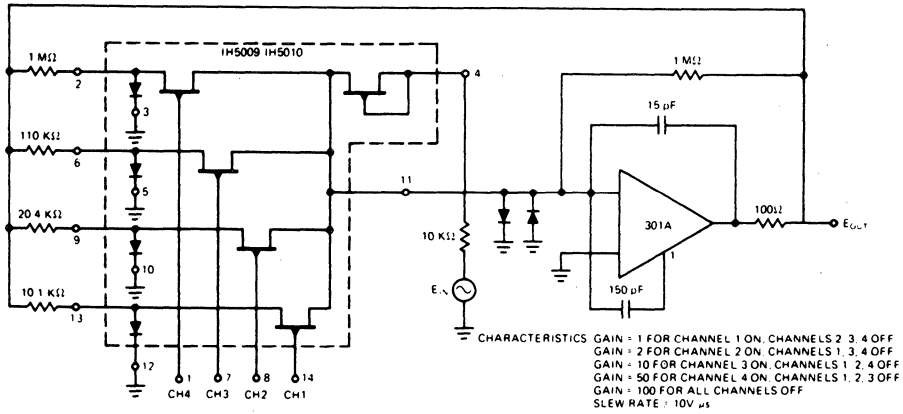


Figure 33: Gain Ranging Circuit

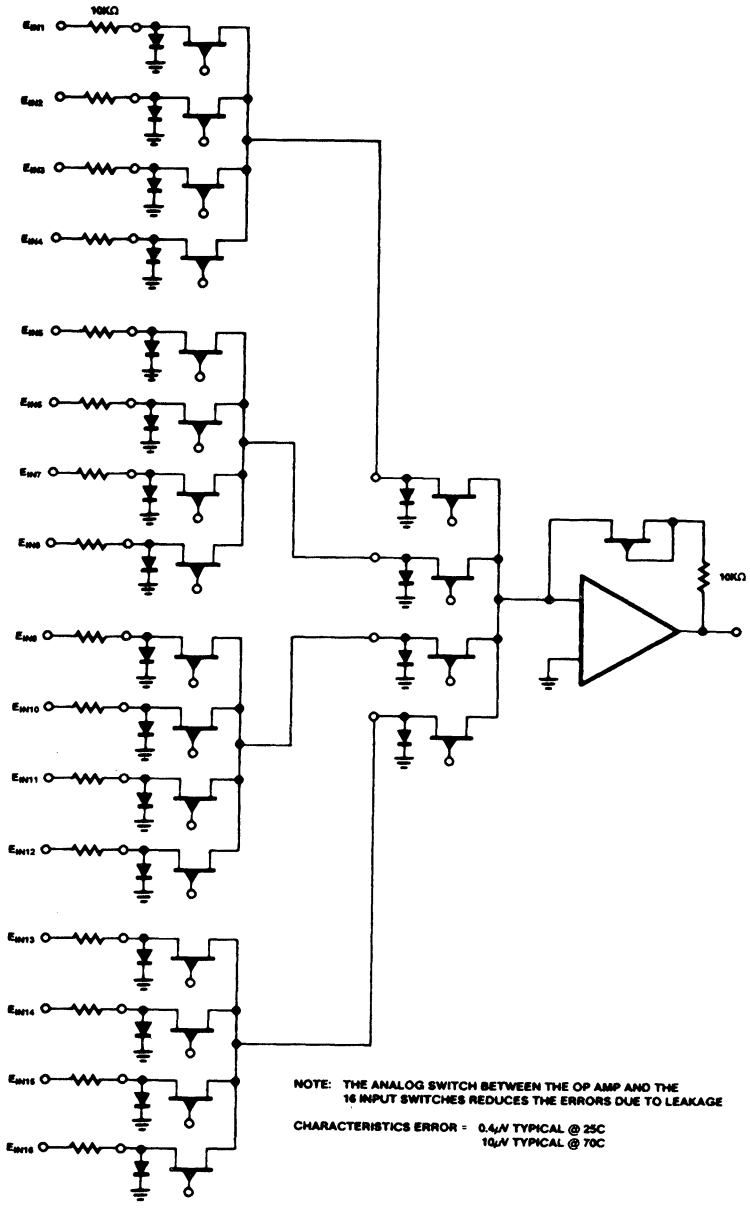
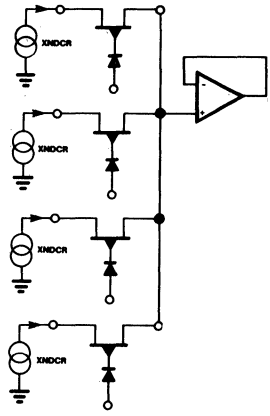


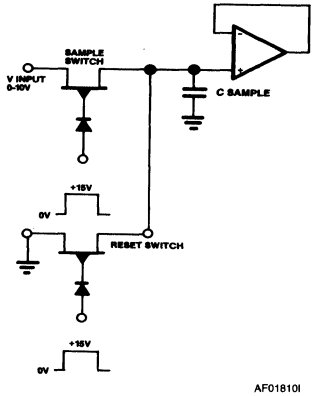
Figure 34: 16 Channel Multiplexer

APPLICATIONS — IH5025 SERIES



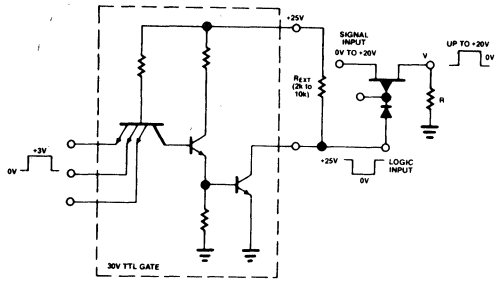
AF01800I

Figure 35: Multiplexer From Positive Output Transducers



AF01810I

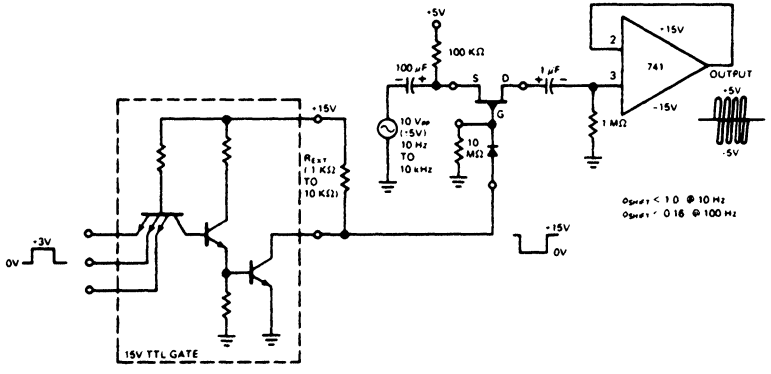
Figure 36: Sample and Hold Switch



AF01820I

Figure 37: Switching Up To +20V Signals With TTL Logic

APPLICATIONS — IH5025 SERIES (CONT.)



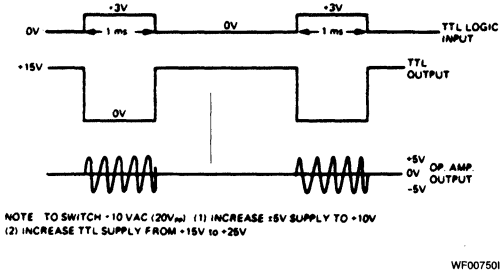
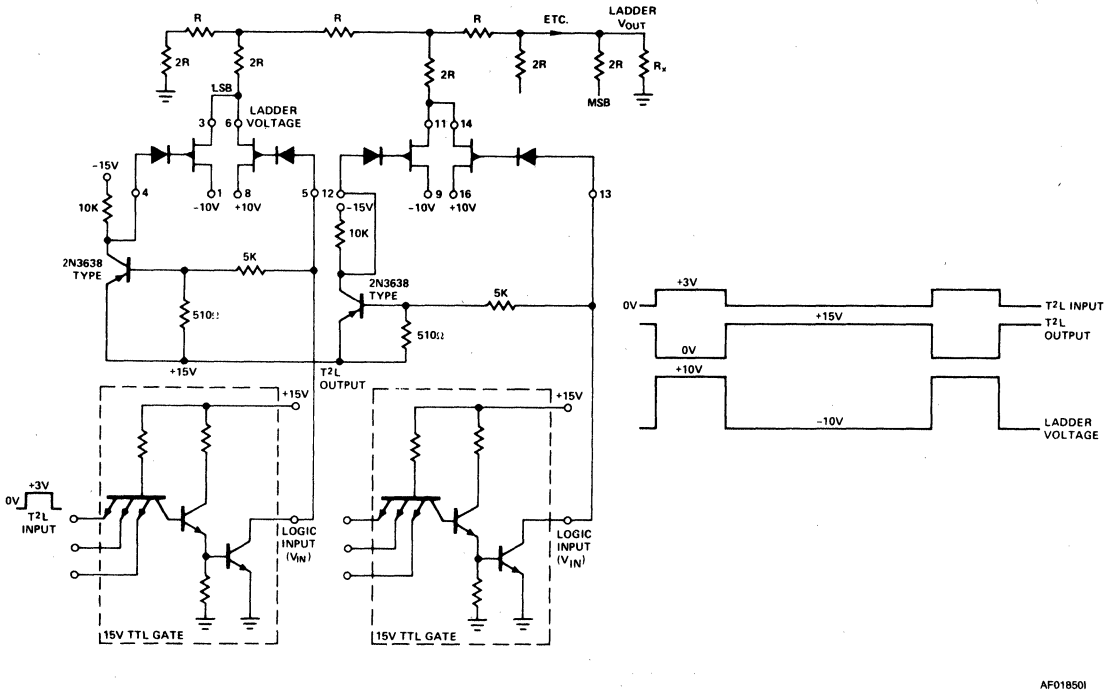


Figure 38: Switching Bipolar Signals With TTL Logic (Alternate Method)

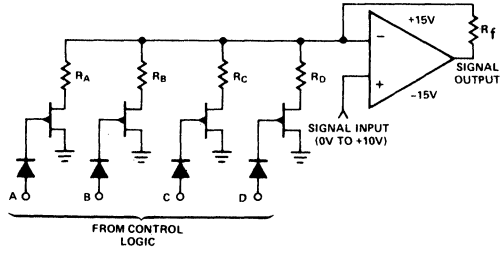
4

APPLICATIONS — IH5025 SERIES



AF01850I

Figure 39: Using The IH5028 As A Dual SPDT To Drive Ladder Networks For Bipolar Switching (Up To ±10V)



i.e. CHANNEL B, C, D, INPUTS = +15V;
CHANNEL A INPUT = 0V
SIGNAL OUTPUT = $\frac{R_f + R_A}{R_A}$ X SIGNAL INPUT

NOTE:
WHEN SWITCHING (+) OR (-) SIGNAL INPUTS, A SCHEME SIMILAR TO FIGURES 10 OR 11 SHOULD BE USED.

AF01840I

Figure 40: High Input Impedance Gain Control For Positive Input Signals Using IH5025

APPLICATIONS — IH5040 SERIES

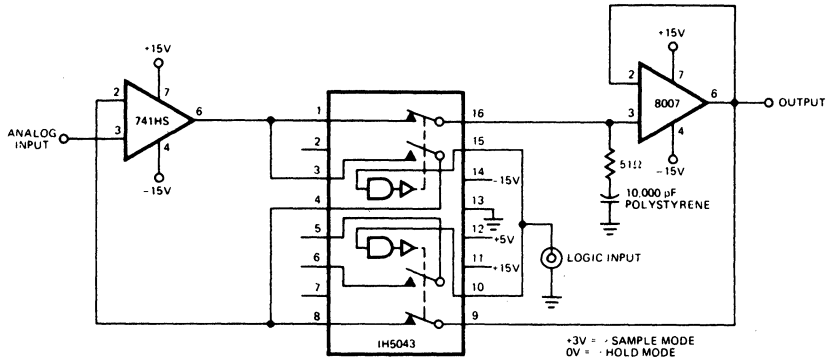


Figure 41: Improved Sample & Hold Using IH5043 (NOTE: This circuit is available as a hybrid from Intersil. Part number is IH5110/5111)

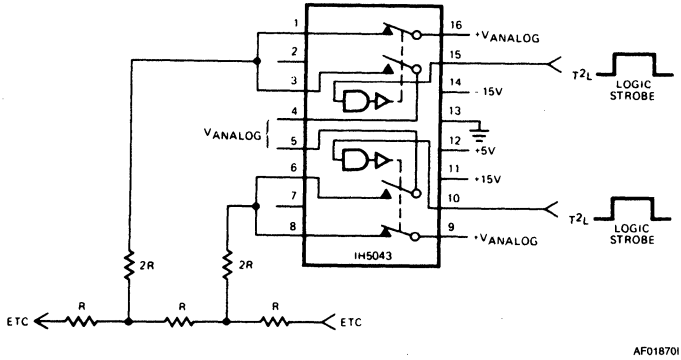
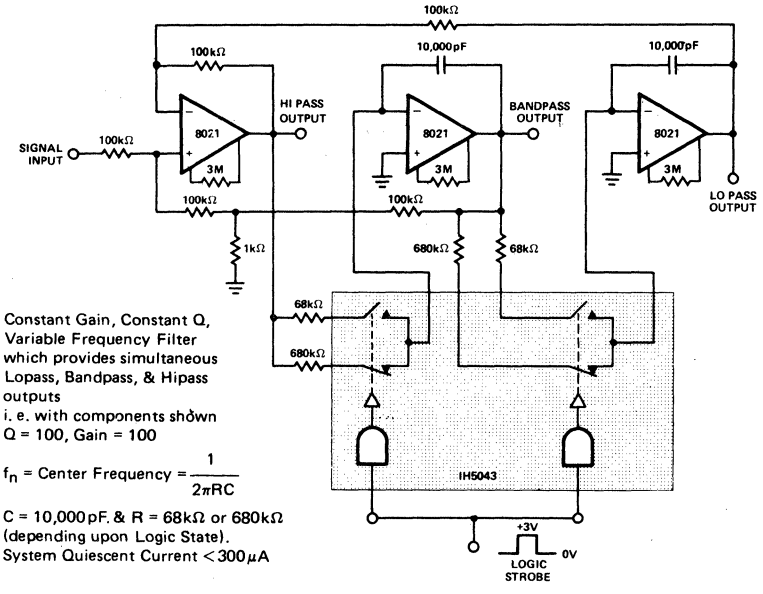


Figure 42: Using The CMOS Switch To Drive An R/2R Ladder Network (2 Legs)

APPLICATIONS — IH5040 SERIES (CONT.)



Constant Gain, Constant Q, Variable Frequency Filter which provides simultaneous Lopass, Bandpass, & Hipass outputs
i. e. with components shown
Q = 100, Gain = 100

f_n = Center Frequency = $\frac{1}{2\pi RC}$

C = 10,000pF. & R = 68kΩ or 680kΩ (depending upon Logic State).
System Quiescent Current $<300\mu A$

AF01880I

Figure 43: Digitally Tuned Low Power Active Filter

AO04
The IH5009 Analog Switch Series

INTRODUCTION

The IH5009 series of analog switches described in this note were designed by Intersil to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost was one of the primary design objectives (less than $1/switch in volume), performance and versatility have not been sacrificed. Up to four channels per package are available, no external power supplies are required, and switching speeds are guaranteed to be less than 500ns.

CIRCUIT OPERATION

Switching Virtual Ground Signals

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories: Those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed. In applications where the signal amplitude at the switch is greater than ±200mV, the simple design of the IH5009 is no longer appropriate and a more complex switch design is called for. See REF. 1 for a complete discussion of this type of switch.

It is important to realize that the ±200mV limitation applies ***only*** to the signal at the drain of the FET switch; signals of ±10V or greater can be commutated by the IH5009 in a circuit of the type shown in Figure 1. For a high gain inverting amplifier the signal level at the virtual ground point will only be a few microvolts for +10V input and output swings.

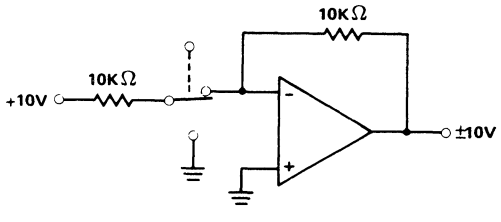


Figure 1: Switching At Virtual Ground Point

The Compensating FET

Those devices which feature common drains (IH5009, 5010, 5013, 5014, etc.) have another FET in addition to the channel switches (Figure 2). This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by:

$$\text{GAIN} = \frac{10k\Omega + T_{DS}\ \text{(compensator)}}{10k\Omega + R_{DS}\ \text{(switch)}}$$

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. The part numbers are shown in Table 1. Since the absolute value of $R_{DS(ON)}$ is only guaranteed to be less than 100Ω or 150Ω, it is clear that a substantial improvement in gain accuracy can be obtained by using the compensating FET. This is only true however when the input resistor and the feedback resistor are similar in value: for dissimilar values, the benefits of the compensating FET are less pronounced.

Logic Compatibility

The 5009 through 5024 series parts are primarily intended for constant-impedance multiplexing. The diode connected to the JFET source acts like a shunt switch, while the FET itself acts as a series switch. The advantage of this configuration is its high noise immunity when the series element is off. The diode then clamps the source to +0.7 TYP. with a low AC impedance to ground and prevents false triggering of the FET for positive inputs. Negative inputs present no problems since they further increase the OFF voltage beyond pinch-off.

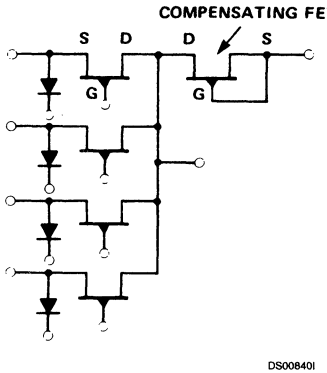


Figure 2: Schematic of IH5009 & IH5010

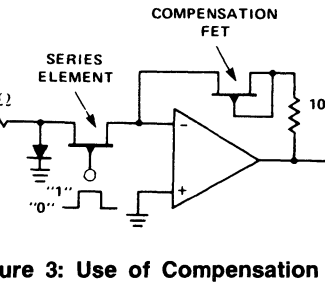


Figure 3: Use of Compensation FET

TABLE 1

PART NUMBER	INPUT LOGIC DRIVE	DESCRIPTION	EFFECTIVE $r_{DS(ON)}$ (OHMS) MAX	$r_{DS(ON)}$ (OHMS) MAX
IH5009	High Level	4-Channel, 15V Logic	50	100
IH5010	DTL, TTL, RTL	4-Channel, 5V Logic	50	150
ITS7318	High Level	4-Channel, 15V Logic	25	100
ITS7319	DTL, TTL, RTL	4-Channel, 5V Logic	25	150
ITS7320	High Level	4-Channel, 15V Logic	10	100
ITS7321	DTL, TTL, RTL	4-Channel, 5V Logic	10	150
ITS7322	High Level	4-Channel, 15V Logic	5	100
ITS7323	DTL, TTL, RTL	4-Channel, 5V Logic	5	150
IH5013	High Level	3-Channel, 15V Logic	50	100
IH5014	DTL, TTL, RTL	3-Channel, 5V Logic	50	150
ITS7324	High Level	3-Channel, 15V Logic	25	100
ITS7325	DTL, TTL, RTL	3-Channel, 5V Logic	25	150
ITS7326	High Level	3-Channel, 15V Logic	10	100
ITS7327	DTL, TTL, RTL	3-Channel, 5V Logic	10	150
ITS7328	High Level	3-Channel, 15V Logic	5	100
ITS7329	DTL, TTL, RTL	3-Channel, 5V Logic	5	150
IH5017	High Level	2-Channel, 15V Logic	50	100
IH5018	DTL, TTL, RTL	2-Channel, 5V Logic	50	150
ITS7330	High Level	2-Channel, 15V Logic	25	100
ITS7331	DTL, TTL, RTL	2-Channel, 5V Logic	25	150
ITS7332	High Level	2-Channel, 15V Logic	10	100
ITS7333	DTL, TTL, RTL	2-Channel, 5V Logic	10	150
ITS7334	High Level	2-Channel, 15V Logic	5	100
ITS7335	DTL, TTL, RTL	2-Channel, 5V Logic	5	150
IH5021	High Level	1-Channel, 15V Logic	50	100
IH5022	DTL, TTL, RTL	1-Channel, 5V Logic	50	150
ITS7336	High Level	1-Channel, 15V Logic	25	100
ITS7337	DTL, TTL, RTL	1-Channel, 5V Logic	25	150
ITS7338	High Level	1-Channel, 15V Logic	10	100
ITS7339	DTL, TTL, RTL	1-Channel, 5V Logic	10	150
ITS7340	High Level	1-Channel, 15V Logic	5	100
ITS7341	DTL, TTL, RTL	1-Channel, 5V Logic	5	150

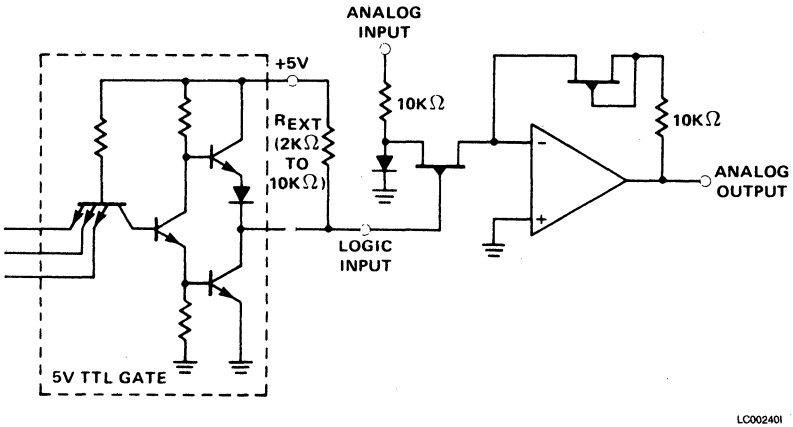


Figure 4: Interfacing With +5V Logic

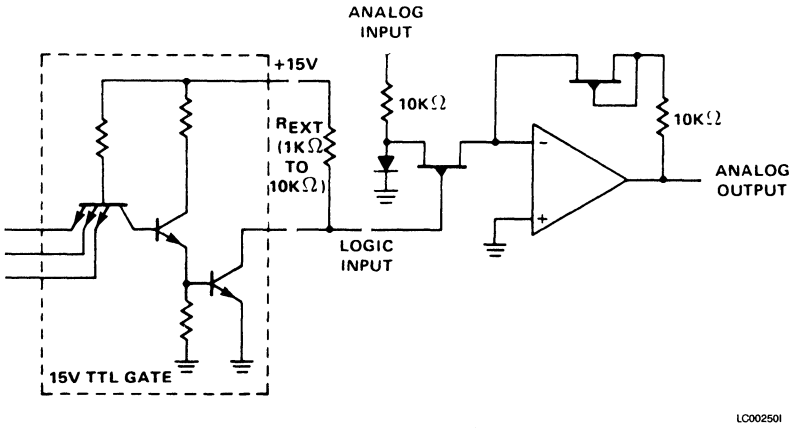


Figure 5: Interfacing With +15V Open Collector Logic

The even-numbered devices in the family (5010 through 5024) are designed for interfacing with 5V logic. The pinch-off of the FETs is selected to be less than 3.7V (Vp @ I_D = 1nA); therefore, a positive logic level +4.5V will supply adequate safety margin for proper gating action. To guarantee this +4.5V from series 54/74 TTL logic requires the use of a pull-up resistor: Values from 2kΩ to 10kΩ are suitable depending upon the speed requirements (Figure 4). Alternatively the TTL may be operated from +6V supplies. The "1" level will then be greater than +4.5V without the need for a pull-up resistor. The maximum on-resistance is guaranteed for +0.5V on the gate of the FET. Since the maximum low level output voltage from TTL is 0.4V, the ON-resistances specified are conservative. With 0V applied to the FET gate, typical ON-resistances of 90Ω will be obtained.

The odd-numbered devices in the family (5009 through 5023) are designed for interfacing with 15V logic. The pinch-off of these parts is selected to be less than 10V, so that a +11V positive logic level provides adequate safety margin. To obtain this level from open collector TTL logic also requires a pull-up resistor; 1kΩ to 10kΩ is suitable depending on the speed and fan-out requirements (Figure 5). The ON-resistance is measured with +1.5V applied to the gate and is guaranteed to be less than 100Ω at 25°C. For 0V on the gate, the typical R_{ON} is 60Ω.

In applications where low ON-resistance is critical, special selections can be made. Since high pinch-off FETs have lower ON-resistances than low pinch-off types (for a given geometry) it is advantageous to make such selections from the odd-numbered devices and use high level TTL for the control logic.

Maximum Switch Current

The maximum current through the switch is dictated primarily by leakage considerations rather than power dissipation problems. When the drain of the FET is held at virtual ground, current through the channel tends to bias the source positive. Eventually, the source-gate junction will forward bias, giving rise to large leakage currents. This is most likely to occur at high temperature when the junction turn-on potential is at its lowest. The data sheet guarantees maximum leakage for I_S = 1mA and 2mA, with V_{IN} = 0V. The substantial increase seen in the leakage in changing I_S from 1mA to 2mA (at 70°C) indicates that the turn-on potential is being approached rapidly under these conditions. Specifying the leakage for V_{IN} (the gate potential) = 0V is a worst case condition; under most circumstances V_{IN} = +200mV would be a more typical value. Thus 200mV additional signal would be required at the source to give the same leakage current.

Switching Speed and Crosstalk

The switching speed is guaranteed to be less than 500ns at 25°C. Typical turn-on and turn-off times are 150ns and 300ns, respectively.

When analog switches are used in conjunction with operational amplifiers, settling time is often an important parameter. In a typical fast amplifier, settling times of 1μs to 0.1% are seen. This time is primarily caused by non-linear modes of operation within the amplifier, and the inclusion of an analog switch at the virtual ground point will not cause significant degradation of the settling time.

Crosstalk can be measured using the circuit of Figure 6. At low frequencies, it is very difficult to obtain accurate values since the separation is better than 120dB. Typical crosstalk as a function of frequency is shown in Figure 7.

PRODUCT SUMMARY

Table 2 shows the different product numbers, their schematics, and their equivalent circuits. The even numbers are designed to be driven from 5V TTL, while odd numbers are designed to be driven from TTL open collector logic (15V).

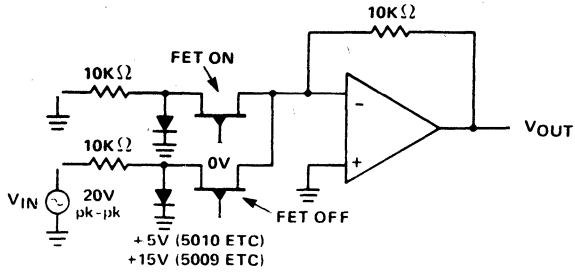


Figure 6: Crosstalk Measurement Circuit

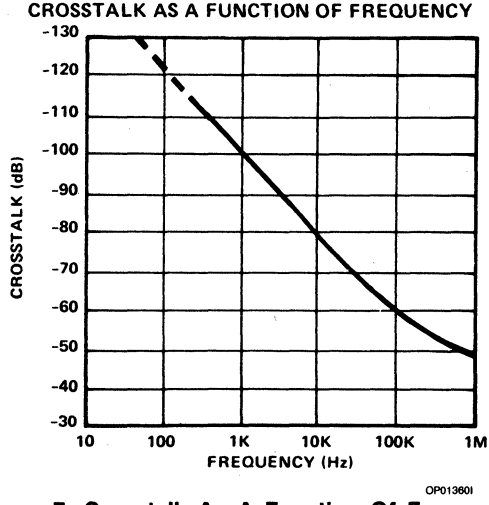
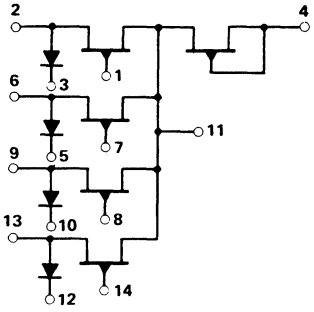


Figure 7: Crosstalk As A Function Of Frequency

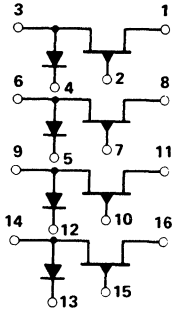
TABLE 2

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
(IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



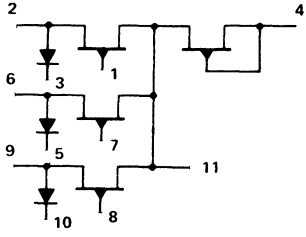
DS00870I

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
(IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



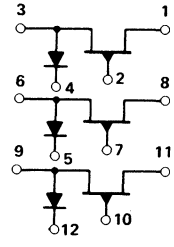
DS00910I

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



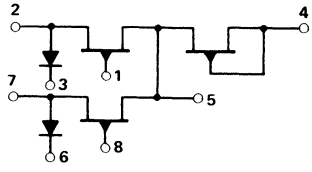
DS00880I

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



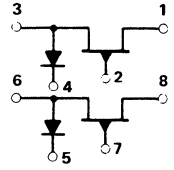
DS00920I

IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



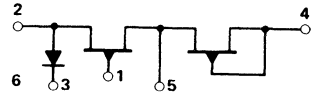
DS00890I

IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



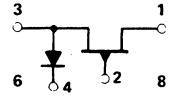
DS00930I

IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00900I

IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00940I

4

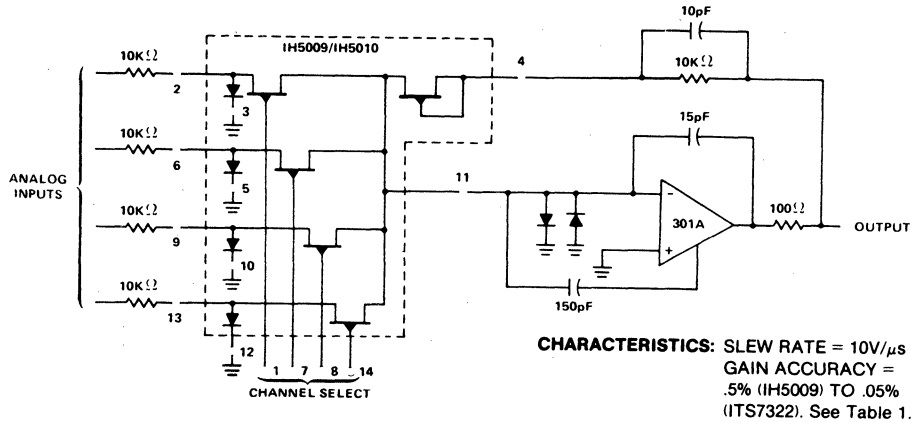


Figure 8: Low Cost 4 Channel Multiplexer

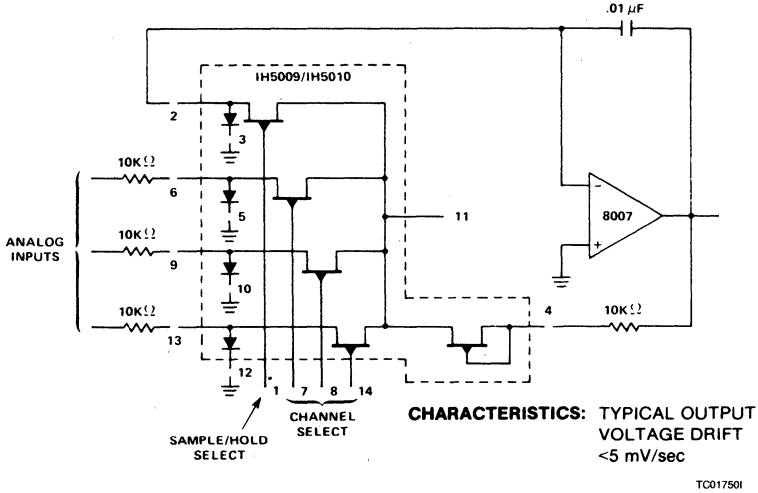
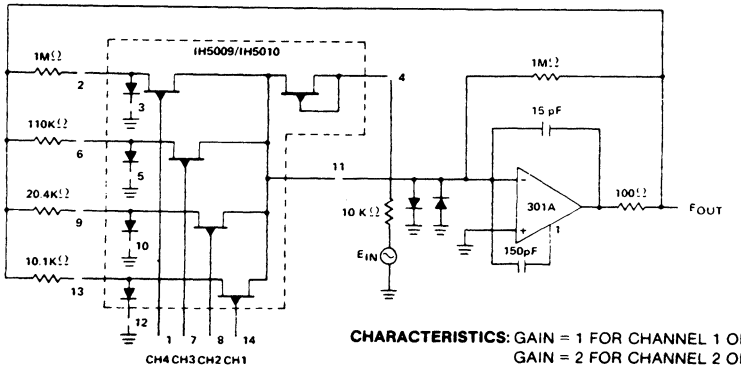


Figure 9: 3-Channel Multiplexer With Sample & Hold

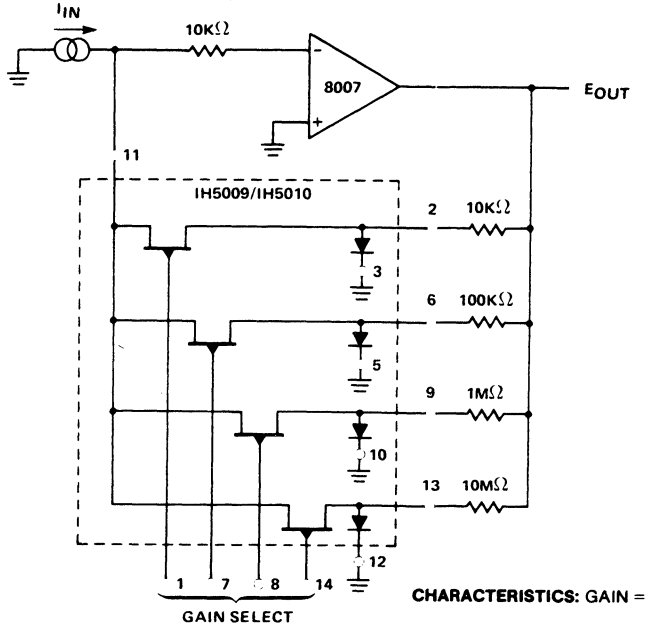


CHARACTERISTICS: GAIN = 1 FOR CHANNEL 1 ON; CHANNELS 2, 3, 4 OFF
GAIN = 2 FOR CHANNEL 2 ON; CHANNELS 1, 3, 4 OFF
GAIN = 10 FOR CHANNEL 3 ON; CHANNELS 1, 2, 4 OFF
GAIN = 50 FOR CHANNEL 4 ON; CHANNELS 1, 2, 3 OFF
GAIN = 100 FOR ALL CHANNELS OFF
SLEW RATE = 10V/μs

GAIN RANGING CIRCUIT

TC01760I

Figure 10: Gain Ranging Circuit



CHARACTERISTICS: GAIN = $\frac{-E_{OUT}}{I_{IN}} = R_{FB}$

TC01770I

Figure 11: Gain Programmable Amplifier

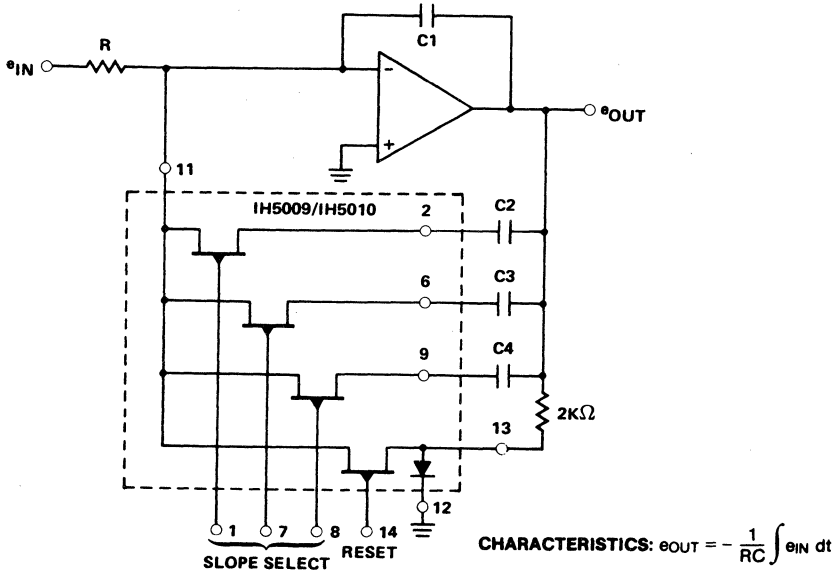


Figure 12: Programmable Slope Integrator

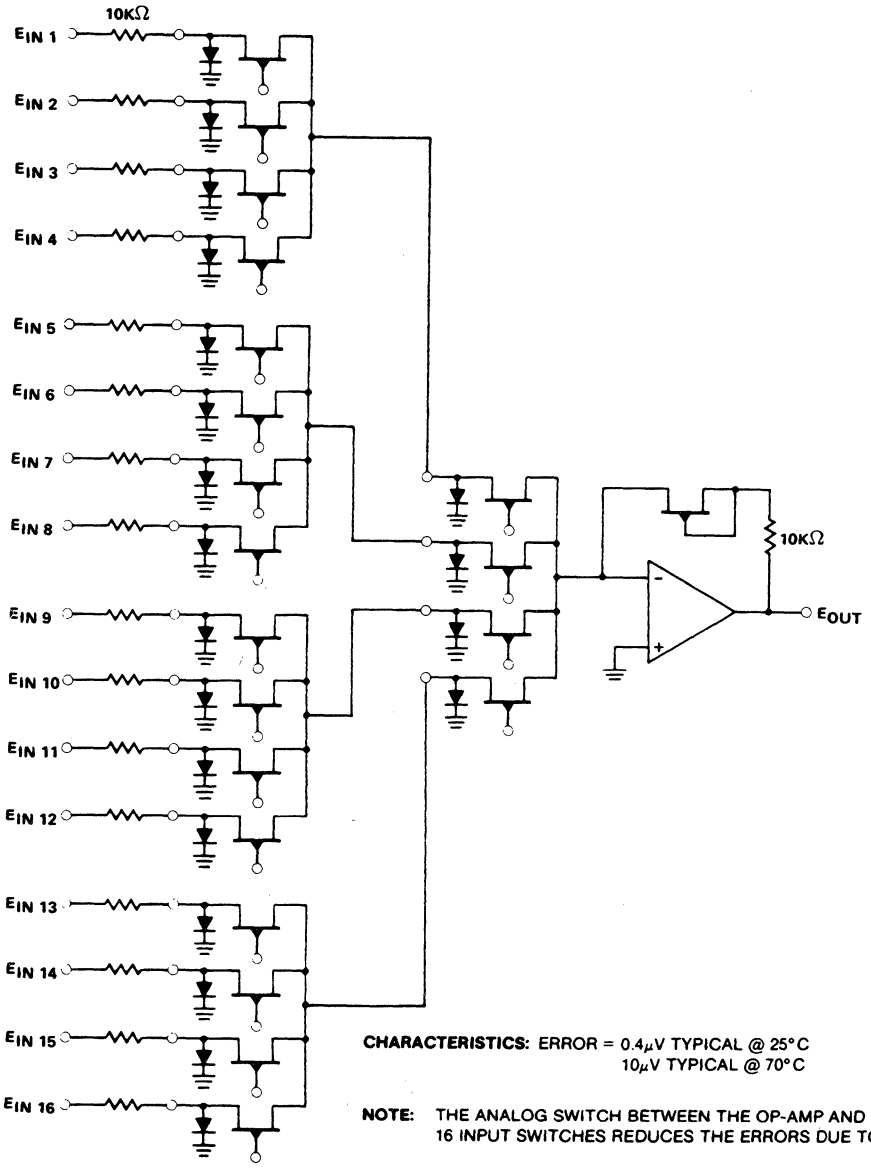


Figure 13: Sixteen Way Multiplexer

AO06
A New CMOS Analog Gate Technology

INTRODUCTION

A new CMOS process has been developed by Intersil which is destined to have a significant impact on the future of this technology in the fabrication of analog gates and multiplexers.

Up to the present time, all the analog gates and multiplexers manufactured with standard CMOS technology have suffered from a serious limitation: under certain conditions, these circuits "latchup", i.e., go into a non-operative state. They will only recover if both the power supplies and the input are removed and reapplied in a specific sequence. Under some circumstances the latchup is destructive and the only cure is replacement of the I.C.

This new process, developed and patented by Intersil, totally eliminates these problems. As well as preventing the latchup condition, this process provides effective overvoltage protection (to ±25V) without degradation of ON-resistance.

UNDERSTANDING THE LATCHUP PROBLEM

A simplified schematic of one channel of a typical CMOS analog switch (or multiplexer) is shown in Figure 1.

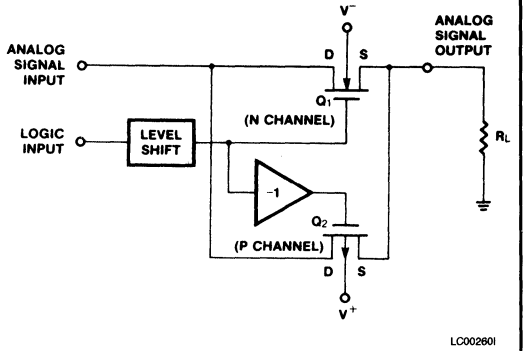


Figure 1: Typical CMOS Analog Switch or Multiplexer

The latchup condition occurs when a negative analog signal is applied to either the drain or source of the MOS transistors while V^- is at 0V. Since analog switches are frequently used to interface between different systems and sub-systems, these conditions occur surprisingly often, especially if the different parts of the system or sub-system have independent power supplies. It should also be noted that these conditions have only to occur briefly (as transients) for latchup to take place.

With V^- at 0V, and a negative potential on the analog input or output, a high current path exists through the forward biased body to drain junction of the N-channel device. Permanent damage or complete destruction of the I.C. can result from this current. This is shown in Figure 2.

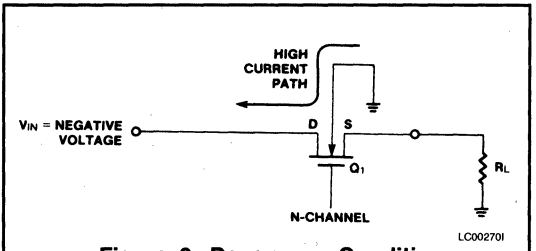


Figure 2: Dangerous Condition

However, the diode is not sufficient in itself to give rise to the latchup phenomena, but careful inspection of the cross section shown in Figure 3 will reveal that this diode forms part of an SCR. The drain and body of the N-channel FET form the emitter and base of the NPN transistor part of the SCR (Figure 4), the body of the P-channel FET (the substrate) acts as the collector; the source and body of the P-channel FET form the emitter and base of the PNP part of the SCR and the body of the N-channel device forms the collector for this PNP. If the beta product of these two transistors exceeds 1, an excellent SCR is formed. It is clear from Figure 4 that grounding the body of the N-channel FET (the gate of the SCR) and applying a negative potential to the analog input (the cathode of the SCR) will turn on the SCR and cause it to latch.

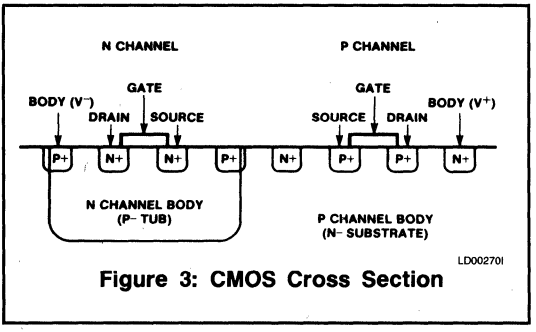


Figure 3: CMOS Cross Section

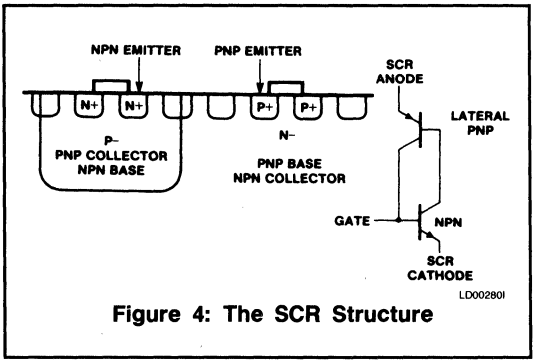


Figure 4: The SCR Structure

INTERSIL'S FLOATING BODY PROCESS

Intersil's improved CMOS process incorporates an additional diode in the connection to the body of the N-channel FET (Figure 5). The cathode of this diode is then tied to V^+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path described earlier, but also prevents the SCR from turning on. As an additional precaution, processing changes have been incorporated which reduce the beta product of the NPN-PNP combination to less than one. Thus in the unlikely event of excessive over-voltages being applied to the circuit (which could break down the blocking diode) the SCR action will still not occur.

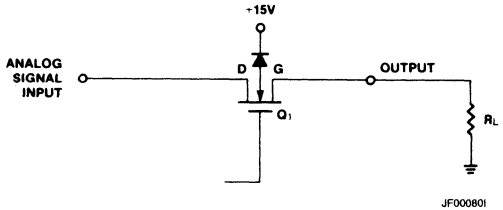


Figure 5: Protective Circuitry for N-Channel FET

CONCLUSION

Prior to "Floating Body" technology, solutions to the latchup problem have involved either using expensive and exotic manufacturing processes, such as dielectric isolation, or the addition of external components. Apart from being inconvenient, adding external components such as current limiting resistors always compromises the electrical performance.

The new "Floating Body" CMOS technology overcomes these problems and has resulted in a reliable, low cost monolithic analog gate function. For the first time it is possible to realize a monolithic gate capable of approaching $1.00 per channel without compromising performance or reliability.

R009
Reduce CMOS-Multiplexer Troubles Through Proper Device Selection

CMOS analog multiplexers exhibit problems with output leakage currents and overvoltage-protection circuitry. Here's how to deal with them.

Dick Wilenken, Intersil Inc

A CMOS analog multiplexer (MUX) is basically a channel-selector switch which can interface signal sensors and computers. It provides a number of input channels, which are time-shared onto a common output terminal. A central computer or microprocessor digitally sequences the MUX to "see" one channel at a time. The goal of designers is to pass the sensed signal through this multiplexer with virtually no error terms present. Providing adequate overvoltage protection also presents a challenge. Both objectives can tax designers' ingenuity unless they are familiar with multiplexer anatomy.

Many designers devise unnecessarily complex circuits in their efforts to avoid the substantial level of error terms that can be encountered during the multiplexing operation and to provide overvoltage protection for the CMOS circuitry. But you can save pc-board space, reduce component count and cost, and avoid the possibility of introducing new errors through proper identification of error sources. And adequate circuit self-protection is the result of the proper choice of multiplexing devices.

OUTPUT LEAKAGE — THE MAJOR ERROR SOURCE

A typical data-acquisition system, extending from sensors to computer, is shown in Figure 1. Here the sensors feed directly into the multiplexer input lines, but this is an idealized case, because most users insert operational amplifiers between the sensors and the MUX inputs. You can eliminate these op amps, however, if you utilize an IC MUX with very low output leakage currents.

Most popular CMOS analog multiplexers have finite ON resistance and leakage currents. Typical of these ICs are the DG506 to DG509 (Siliconix), HI506 to HI509 (Harris) and the IH6116/6208 Series (Intersil).

As noted, the design goal for the system in Figure 1 is to transfer the sensed signal into the sample-and-hold circuit with as little error as possible. Some potential error sources are labeled in Figure 2. One such error source arises from a voltage-divider action between $r_{DS(ON)}$ of a multiplexer ON channel (a consequence of finite channel resistance) and the input impedance of the follower op amp (R_{in}). The signal level at the positive input of the op amp is equal to the sensor voltage times $R_{in}/R_{in} + r_{DS(ON)}$. And the error produced is equal to the ratio of R_{in} to $R_{in} + r_{DS(ON)}$. Because R_{in} (at low frequencies to dc level) = 100MΩ and $r_{DS(ON)}$ = 1kΩ, the error equals $10^8/10^8 + 10^3 = 1/1 + 10^{-5}$. This set of conditions yields an accuracy of 0.001%; $r_{DS(ON)}$ can range as high as 10kΩ and still provide 0.01% accuracy. The obvious conclusion to be drawn is that the $r_{DS(ON)}$ of the ON channel is not a very significant factor so long as it is less than 10kΩ.

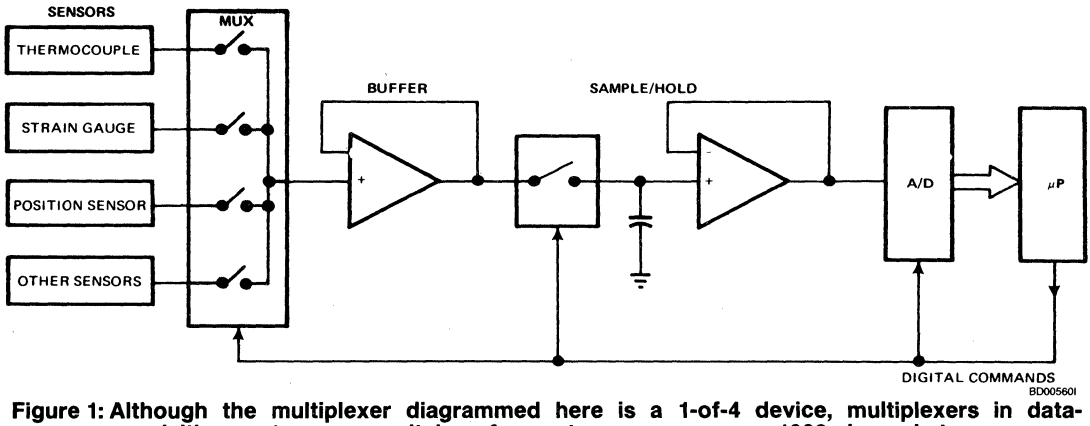


Figure 1: Although the multiplexer diagrammed here is a 1-of-4 device, multiplexers in data-acquisition systems can switch as few as two or as many as 1000 channels to a common output

A second and much more significant source of multiplexer error stems from I_{TOTAL} (basically total leakage plus input bias current) flowing across $r_{DS(ON)}$. (The total leakage is the sum of the OFF channel leakage plus the I_{ON} channel leakage.) For example, assume that $I_{OFF(1-4)}$ = 150nA, I_{ON} = 25nA and $r_{DS(ON)}$ = 2kΩ, all at 125°C. The voltage drop across $r_{DS(ON)}$ is then 175nA times 2kΩ, or 350μV. This 350-μV figure might be considered acceptable if the sensor output were 10V FS. However, thermocouple outputs of 16mV FS over a 160°C temperature range correspond to 100μV/°C. Thus, the 350-μV voltage drop across the switch is equivalent to a 3.5°C error — a deplorable level of accuracy. Of course, the same error would be reduced by a factor of approximately 1000 when the ambient temperature drops from 125°C to 25°C: 0.350μV at 25°C is virtually error-free.

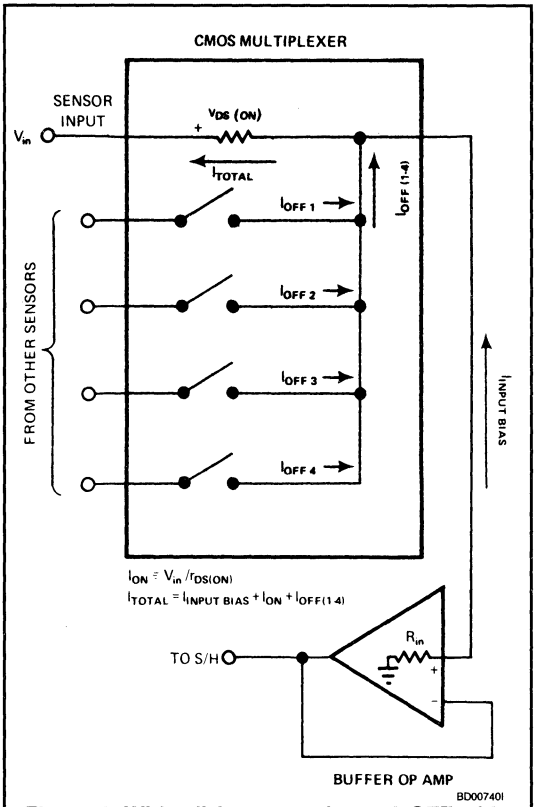


Figure 2: With all but one channel OFF, this equivalent circuit for the MUX/buffer portion of Figure 1 shows potential error terms

Specifically, the error factors cannot be reduced to $r_{DS(ON)}$ of the ON channel, but rather to ($I_{output\ leakage}$ + $I_{input\ leakage}$)$r_{DS(ON)}$. The currently available DG506 (1-of-16) multiplexers are specified at 500nA max at 125°C, and $r_{DS(ON)}$ is in the 500Ω range, producing an error term of 250μV for the multiplexer itself (exclusive of op-amp input bias currents). By comparison, IH6116 parts are rated at 100nA max at 125°C, with $r_{DS(ON)}$ of 1kΩ; the maximum error term therefore equals 100μV, or ±1°C for typical thermocouple sensors.

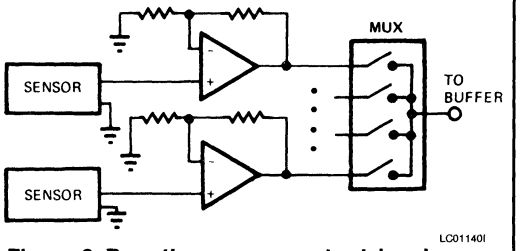


Figure 3: Boosting sensor output levels can overcome leakage and $r_{DS(ON)}$ errors, but you must pay for the added op amps and the resistors

DEALING WITH LEAKAGE

Figure .3 is a block diagram of a circuit providing a solution to the problem of leakage and $r_{DS(ON)}$ errors. In it, the signal levels are boosted so that the MUX error becomes a much smaller proportion of the multiplexer input signal. But this technique is expensive; the parts count is larger, more pc-board space is used, and new sources of error are introduced: op-amp offsets and temperature drifts.

You can zero the raw offset down to 100μV with a $0.50 potentiometer. But how do you reduce offset drift?

Because the thermocouple scale is 100μV/°C, the op-amp drift must be no greater than 100μV/°C to contribute less than 10% error. Therefore, the best solution is to avoid inserting op amps between the sensors and the multiplexer, and to choose instead a multiplexer with significantly lower output leakages.

You might have to spend a few dollars more to obtain a MUX specified at, say, a maximum $I_{D(OFF)} \leq$ 100nA at 125°C. But the alternative is the 16 op amps and all those gain resistors required for 16 channels of low-level sensing. And even if you use 741s, following this approach will cost you at least $4 (16 op amps at $0.25 each). However, if you choose a MUX with the lower leakage specifications, you'll save both money and pc-board space.

OVERVOLTAGE FAULT PROTECTION

As noted, CMOS multiplexers are designed to operate as sequential, time-shared multiple switches: When all supplies are correctly operating, only one channel is ON at a time. But when power supplies to a CMOS MUX are turned off, all sorts of damaging effects can occur.

Most of today's IC multiplexers operate from ±15V, GND and perhaps +5V. The sensor signals come from instruments powered by local supplies, which are usually independent of the MUX power supplies. When the multiplexer power is down while the signal inputs are active, the majority of today's CMOS multiplexers will not operate sequentially — instead, all channels will be turned ON simultaneously. In that case, one transducer is forced to drive the other transducers via the ON-channel resistances — operation that can be very tough on the sensors.

The origin of this problem lies in the design and fabrication techniques currently employed in manufacturing a CMOS multiplexer like the DG506 or IH6116.

A typical CMOS channel circuit is shown in Figure 4a. If the sensor input signals are lower than ±15V with MUX power on, no malfunctions occur. But if the sensor signals exceed the levels of the MUX power supplies, or if the multiplexer power is off, the channels are coupled.

Figure 4b depicts a condition where the MUX power is down with sensor signals present. Note that with the power off, the gates and bodies of the parallel n- and p-channel MOSFETs are at ground potential. Because most threshold voltages fall in the range of 1 to 5V, the devices are in the enhancement mode (turned ON) when the signal levels exceed these threshold voltages.

For example, assume that ±5V levels are being switched, with the n-channel $V_{threshold}$ at +2V and the p-channel $V_{threshold}$ at −3V. Thus, for −5V levels, the V_{GS} of the n-channel device equals +5V when the gate is at ground potential; this value is +3V more than the threshold voltage, and the FET turns ON. A similar condition occurs at +5V levels, when as a result, the p-channel device is turned ON. Either situation couples all channels with voltage levels higher than the MOSFET's threshold voltage.

While this coupling phenomenon occurs only with multiplexer power down, a similar situation occurs if the MUX power is at a normal ±15V level and the signal levels exceed ±15V, as happens with voltage spikes. Electrically, this condition is indistinguishable from the previous fault situation. Figure 4c shows that for levels in excess of −20V, the n-channel device's V_{GS} equals −15V minus the −20V value (resulting in a final figure of +5V), and the device is enhanced (ON). The opposite condition occurs at +20V, when the p-channel device is ON. In either case, all channels are coupled.

Another harmful condition can occur either when a multiplexer is powered-down or when excessive signal levels are present: Heavy current supplied by the sensors flows into the bodies of the n-channel or p-channel MOSFETs; this current could damage the sensors.

The origin of this problem lies in the junction-isolation technique inherent in the fabrication of CMOS devices. Figure 5 shows a cross-section of typical CMOS parts. Note that the body of the n-channel device contains the p− well (usually tied to −15V) and that the source-to-body junction is an n+/p− silicon junction that looks like a reverse-biased diode under no-fault operation. Specifically, the n+ source is ≤ +15V and ≥ −15V when the p− well is tied to −15V. When the −15V level is off, the p− well rides at ground potential, and the source might be forward-biased into the body. The only limits on current flow are the maximum current that the sensor can deliver and the bulk resistance of the substrate. A similar situation occurs in the p-channel device, at the source/body pn junction.

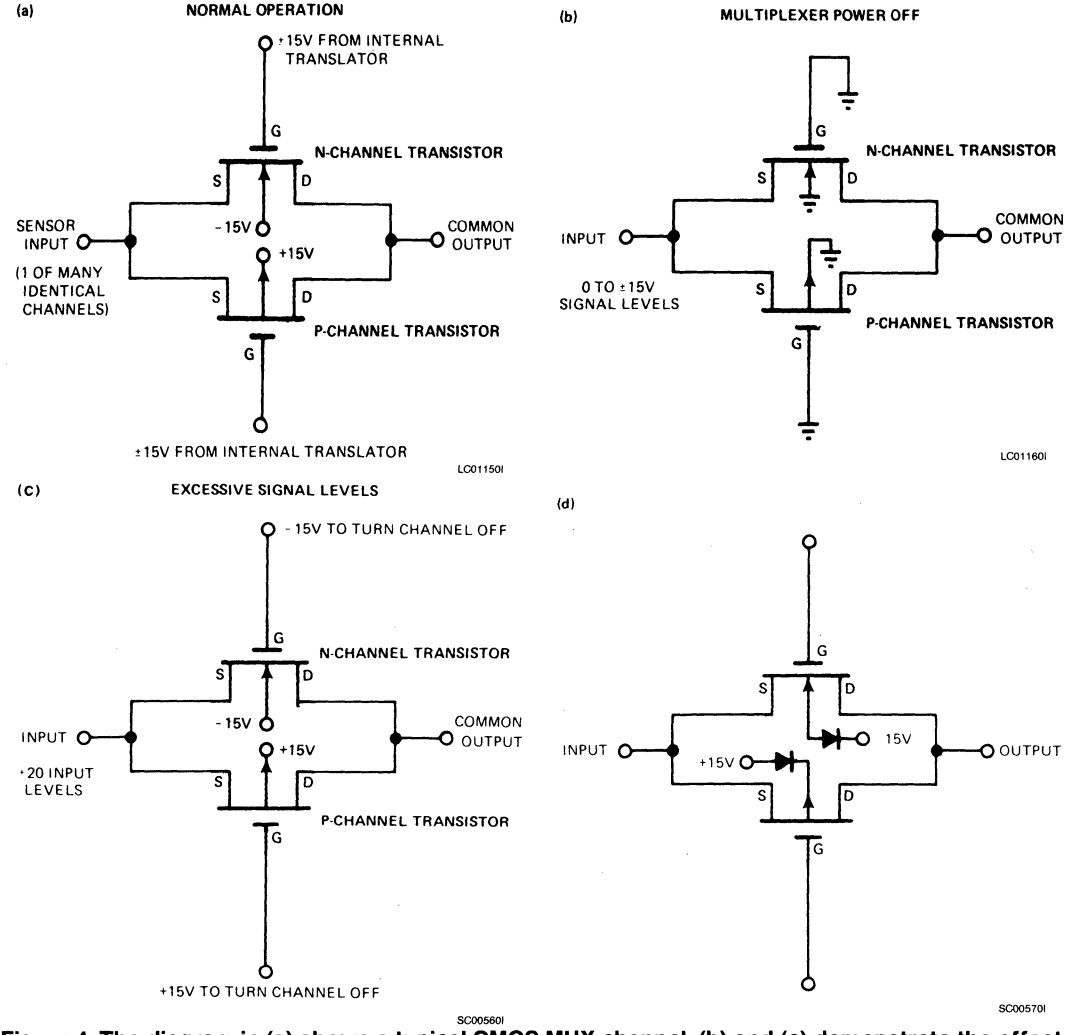


Figure 4: The diagram in (a) shows a typical CMOS MUX channel; (b) and (c) demonstrate the effects of power-down and overvoltage faults, respectively. Inserting diodes in the MUX supply lines affords protection from excessive currents (d).

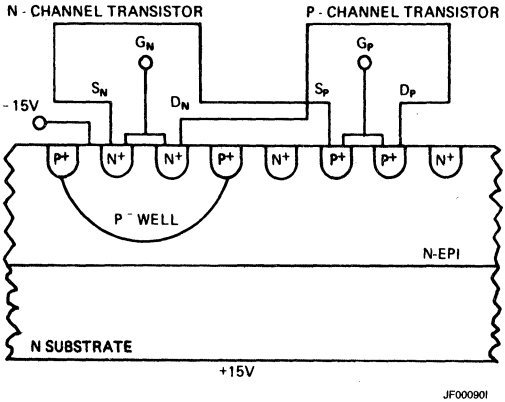
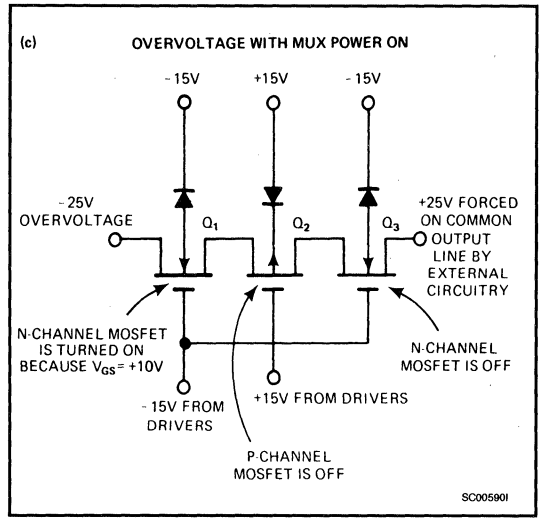
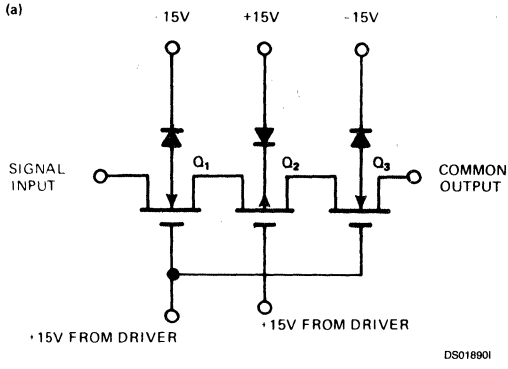


Figure 5: Power-down or overvoltage faults forward-bias the n-channel source/p-well junction and the p-channel source/n-epi junction





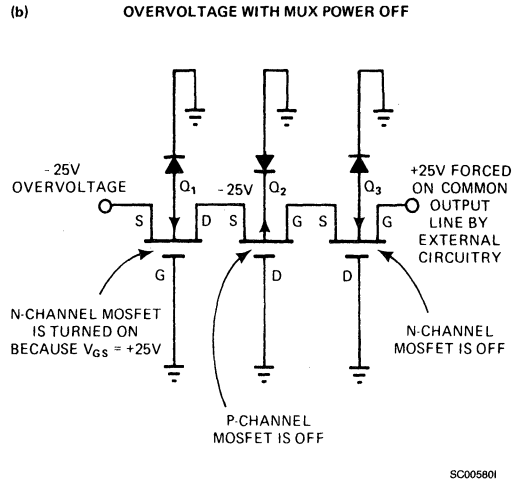


Figure 6: A series structure protects against power-down and overvoltage faults

A common technique to prevent this excessive current flow from the sensor into the MOSFETs' bodies is to add diodes to the multiplexer supply lines, as shown in Figure 4d. Addition of these diodes reduces the signal-handling level to +14V (with ±15V supplies). But this factor is somewhat academic because most operational amplifiers have maximum input levels below ±14V (see the follower op amp in Figures 1 or 2).

BETTER PROTECTION WITH A NEW STRUCTURE

Another family of CMOS multiplexers (Intersil's IH5108 and IH5208) features an improved fault-protection structure. These devices have a series combination of n- and p-channel MOSFETs instead of the parallel arrangement found in more conventional devices.

The new structures' output-channel configuration is shown in Figure 6a. The series-connected n-channel devices are located on either side of the p-channel MOSFET. The IH5108/5208 IC's series-oriented design produces the following electrical characteristics:

- When the ±15V multiplexer power is off, all channels are OFF, rather than being ON as occurs in the parallel output stage in Figure 4.
- No current is drawn from the sensors — only leakage current is present.
- All channels remain OFF and draw only leakage currents for ±25V overvoltage inputs, regardless of whether multiplexer power is on or off.

Figures 6b and 6c show two fault conditions and the performance of the series multiplexers' structure under these conditions. In Figure 6b, Q_1 is turned ON by the fault condition, but Q_2 and Q_3 remain OFF. Q_2 and Q_3 share a 50V breakdown, and the device with the lowest leakage has the highest voltage drop across it. The series structure is symmetrical, with an n-channel device on either side of the p-channel MOSFET. Reversing the 25V polarity has no effect, because only one n-channel device will be ON with either polarity in effect; the remaining two devices will always be OFF.

The same conditions exist in Figure 6c, with the ±15V MUX power turned on. In this case, the gates are driven to −15V for the n-channel devices and to +15V for the p-channel transistor — corresponding to the OFF-channel condition. The gate drive voltages derive from the on-chip TTL translator circuitry. Again, as in Figure 6b, Q_1 is turned ON by the overvoltage; Q_2 and Q_3 are OFF and serve to stand-off the 50V voltage drop.

A022
A New JFET Structure The VARAFET

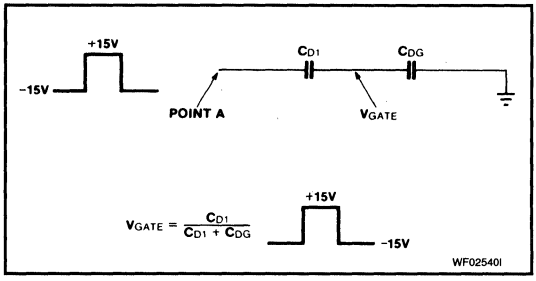
Intersil has introduced a new concept in junction field effect transistor technology — an integrated JFET circuit called the VARAFET. The VARAFET has been designed to take the place of the popular 2N4091–2N4093 and 2N4391–2N4393 families of n-channel switching FET's, and the big advantage of the new part over the present 2N4091 family is that the usual analog gate interfacing components are monolithically built-in, thus saving board space. The VARAFET can be used whenever solid state switching is required. The user will be pleasantly surprised to find that the VARAFET's cost is about the same as the 2N4091, even though it has the equivalent of three extra interfacing components.

Figure 1 shows a typical solid state switch or "analog gate" using the 2N4091 as the switching element. Compare this to Figure 2 which uses Intersil's new VARAFET for the same circuit function and the reason for the popularity of the VARAFET becomes apparent.

Notice that the solid state switch of Figure 1 requires a voltage translator circuit, three interfacing components — D1, C1 and Rf — and finally, the 2N4091 output switch. The same solid state switch in Figure 2 requires only the translator and the VARAFET, thus eliminating the need for interfacing components D1, C1, and Rf.

The translator converts the low level TTL voltages (typically 0.4V–2.4V) to the ±15V levels required by the output FET to handle up to ±10V analog signals. Point A of both Figures 1 and 2 corresponds to translator outputs, and this point swings from +15V (when TTL level is high) to −15V (when TTL level is low).

Interfacing components D1, C1 and R_f, are required for most switching applications when using any normal n-channel FET (Figure 1). D1 is needed to prevent forward biasing the drain to gate junction of the 2N4091. For example, when the switch is being turned "on," Point A goes to +15V; if analog signal input is at least a diode drop less than +15V, drain to gate forward biasing occurs and considerable signal current can be drawn. To prevent this, D1 is added in a back-to-back diode arrangement with the drain to gate (or source to gate) FET junction. However, the necessity for D1 creates a new problem — the back-to-back diode arrangement becomes a "charge area" switching device. This means that D1 in series with the drain to gate FET junction looks like two capacitors in series, and the voltage drop across either capacitor is a function of the ratio of the capacitors, i.e.,



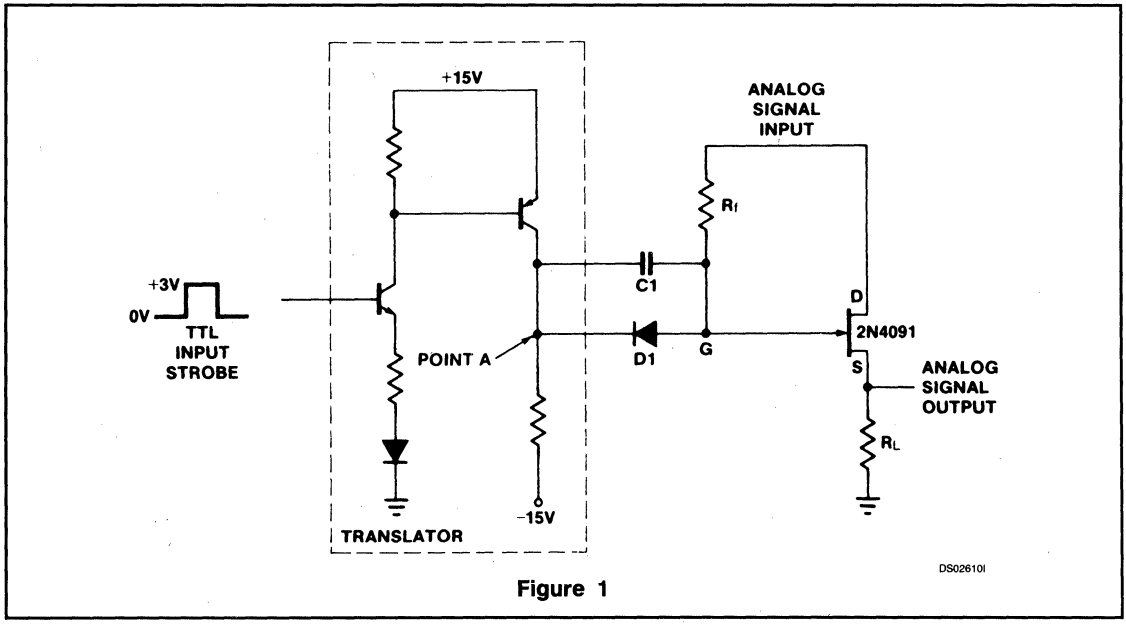


Figure 1

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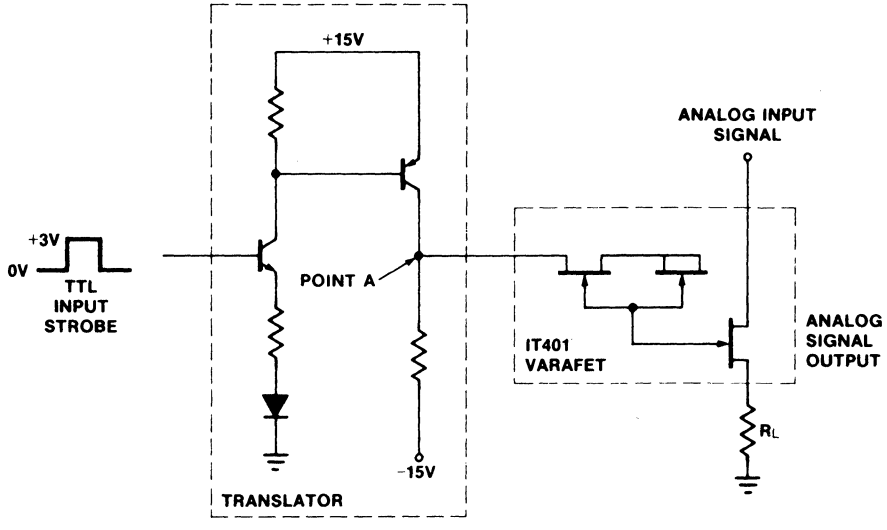
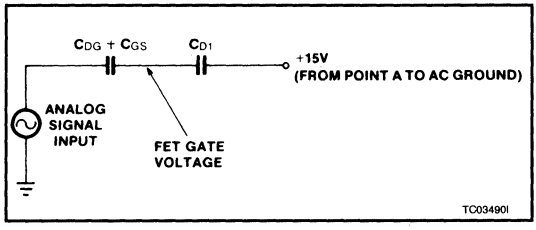


Figure 2

C_{D1} is the capacitance across diode D1, and C_{DG} is the capacitance between FET drain and gate junction. (Source to gate capacitance is the same magnitude but qualitatively the effect is the same.) The culprit then is diode capacitance C_{D1}, since little can be done about the FET capacitance. When the FET is turned on, C_{D1} should be as small as possible, since it limits AC peak-to-peak handling capability as shown in the schematic below.



In this case, since the FET is "on" when $V_{GS} = 0V$ (for minimum r_{DS} on), there should be no AC voltage drop across $C_{DG} + C_{GS}$. This only occurs when $C_{D1} = 0pF$, or more practically when $(C_{DG} + C_{GS}) \gg C_{D1}$. If, for example, the analog signal is $\pm 10V$ or $20V_{PP}$ and $C_{DG} = C_{GS} \cong 10pF$ and $C_{D1} = 2pF$, then $\Delta V_{GS} = \frac{2pF}{22pF} \times 20V_{PP} \cong 2V_{PP}$ or $\pm 1V$. The AC signal will be rectified in the gate to source/drain junctions and this means that $V_{GS} \neq 0$ (lowest $r_{DS(on)}$) but rather the "on" case corresponds to $V_{GS} = -1V \pm 1V$. For FET pinch-off voltages in excess of 5V, the effect is bad but not disastrous, but when V_P is 3V–4V, the 30Ω FET has an average "on" resistance of 200Ω or so.

While it is bad enough that the diode capacitance can limit the AC pp swing ($r_{DS(on)}$), even worse is the fact that it can prevent the switch from functioning at all. Figures 3 and 4 show, graphically, why this effect occurs.

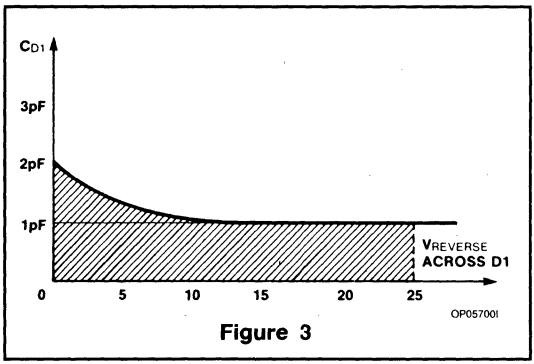


Figure 3

When the analog gate has to handle up to ±10V signals, the voltage drop across D1 varies from about 0V to 25V (of reverse bias). The total charge coupled through D1 is $\Delta Q_{D1} = \int_0^{25V} C_{D1} dV$, or the shaded area of Figure 3. Also, during the same switching interval, the voltage at the FET junctions (V_{GS} & V_{DG}) varies, V_{GS} from about 0V to 15V, and V_{DG} from approximately 0V to 25V. Algebraically adding these two functions results in the curve of Figure 4; a graphic representation of the total charge the 2N4091 requires to be able to handle ±10V analog signals, $\Delta Q_G = \int_0^{VDG} C_{DG}\ dV + \int_0^{VGS} C_{GS}\ dV$. The only place this charge can come from is D1, and a simple comparison of the two curves shows that for low voltages D1 has too little a charge area to allow proper switch operation.

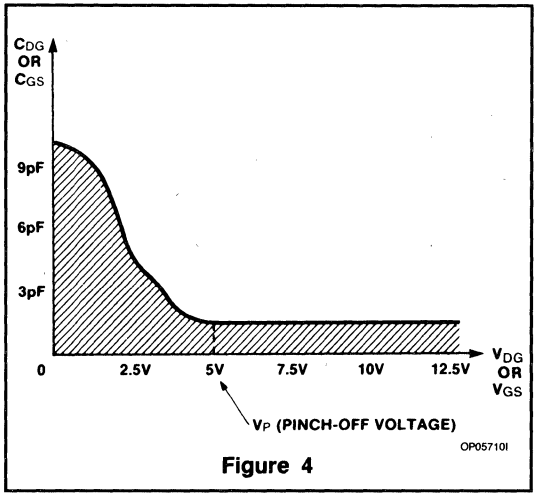


Figure 4

This can be remedied by using a special varactor diode, using a capacitor in parallel with D1, or adding a referral resistor (R_f) between analog input and the gate of the 2N4091. Each has its own disadvantages. The varactor is expensive, the added capacitor limits the analog peak-peak swing, and the referral resistor limits the negative excursions of the analog signals. Figure 5 shows the effective circuit of the last.

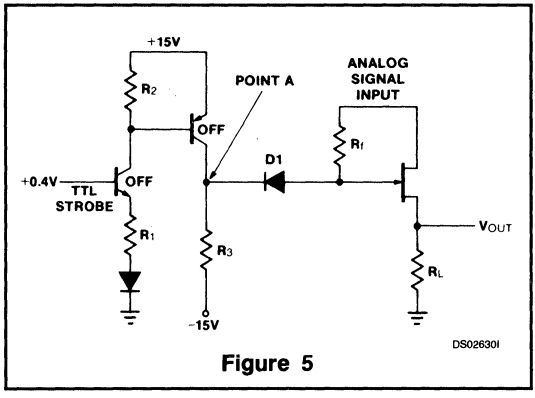


Figure 5

When the transistor is in the low state (TTL strobe input is 0.8V or less) the translator output PNP is off and the voltage at Point A is the result of a voltage divider between −15V and the analog signal input. For example, if $R_3 = 20k\Omega$ (typical value) and Rf = 100kΩ, and for an analog input of −10V, Point A will go to −14.28V instead of −15V, and a signal current of 36μA will be drawn.

The −14.28V will be seen on the cathode side of D1, and the anode side will be approximately −13.6V. Thus the gate of the 2N4091 is at −13.6V when the analog input is −10V. This means that V_P (pinch-off) of the 2N4091 must be less than 3.6V or the FET will be on when it's supposed to be off. In other words, this structure has lost 1.4V of pinch-off voltage and instead of $V_P < 5V$ (before Rf was added), we need $V_P < 3.6V$ to hold off−10V signals. With any safety margin, V_P must be less than 2.6V to work over the temperature range, and this translates as a useful pinch-off range of $1V < V_P < 2.6V$. This means a special selection from standard (1−5V) 2N4093s must be made, and this is expensive. Additionally, this range means that minimum $r_{DS(on)}$ is 80Ω instead of perhaps 30Ω.

Everything considered, the design of analog switching circuits is a nightmare of compromises at best, and may not work at all if the right interfacing components are not selected. The selection of D1, C1, R_f and V_P of the output FET requires a great deal of expertise (some say a lot of good luck). To put the design of solid state switches back into the system engineer's hands, Intersil developed the VARAFET.

The VARAFET is specified as a subsystem element to replace the D1, C1 and R_f and 2N4091 family elements; thus the user only need be concerned with system performance specifications such as $I_{D(off)}$, $I_{S(off)}$, $I_{D(on)}$ and $I_{S(on)}$, switching speeds, etc. To use the VARAFET, simply connect the output (Point A equivalent) of a translator to the FET's input. The output of the VARAFET is virtually identical to the source and drain of the 2N4092 type of discrete FET. The structure of the VARAFET is shown in Figure 6.

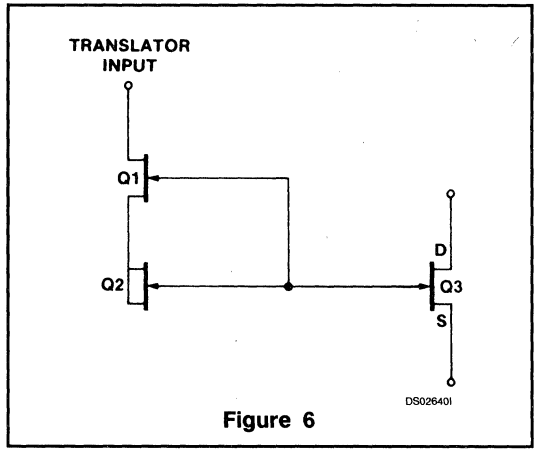


Figure 6

Q1 is a small FET which controls the charge area curve of Q2, a specially designed JFET which has a capacitance of approximately 60pF at 0V and 5pF at pinch-off and beyond. Q2 is designed so that its charge area curve is twice what Q3 needs to work properly, so 100% guardband exists. Since the 5pF off capacitance would drastically limit the peak-to-peak signal capability, Q1 has been added in series with Q2 and the series configuration produces an "off" capacitance of about 0.3pF. This allows the user to handle up to $26V_{PP}$ (if V− is chosen to be at least (V_P + 1V) over −13V negative excursion, i.e., −20V. Figure 7 shows the charge area effect of the combined Q1, Q2 system, compared to the required charge area for Q3.

Again, a visual inspection of the area under the curve (Q total) for the Q1, Q2 system will show that it is at least twice the area under the curve for (C_{GD} + C_{GS}) Q3 and thus proper operation is insured.

As previously stated, the Q1, Q2 and Q3 systems are monolithically integrated into about a 26 mil x 26 mil chip,

whose back side is the common gate. Figure 8 shows a cross section of the monolithic construction.

The VARAFET is being offered in two pinch-off ranges. IT401 has a V_P range of 4.0V to 7.5V, while IT401A has a 3V to 5V range. Of course, the IT401 has the lowest r_{DS} (on) resistance (30Ω maximum) while the IT401A is specified at 50Ω maximum. The $I_{D(off)}$, $I_{S(off)}$ and $I_{D(on)} + I_{S(on)}$ leakages are all typically in the range of 10pA to 20pA. The VARAFET's speed, $t_{on} + t_{off}$ is in the 10ns area, but this is limited practically by the translator speed. Intersil does offer a CMOS dual driver chip, the IH6201, which translates TTL levels into ±15V levels at speeds of 400ns for t_{on} and about 150ns for t_{off} (break-before-make). The combination of the CMOS driver and the VARAFET produces a solid state switch which will easily handle ±10V signals and yet draw no quiescent power supply current (< 10μA) from the ±15V supplies.

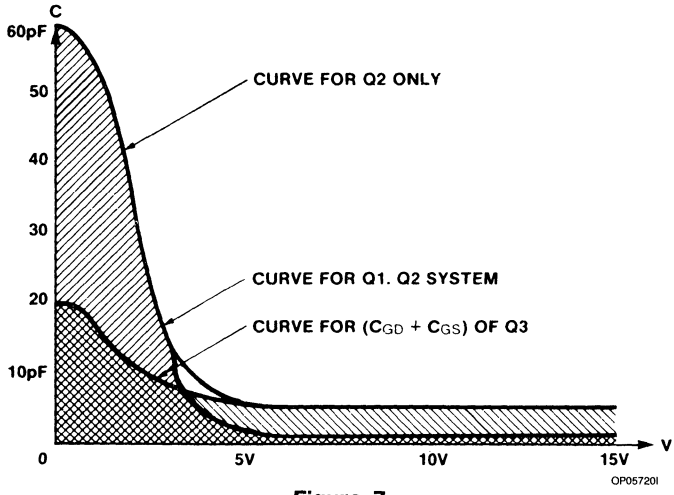


Figure 7

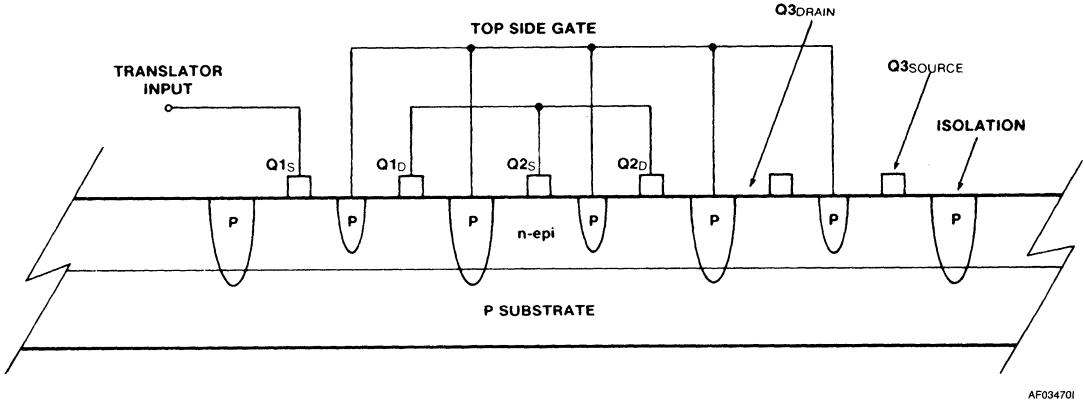


Figure 8

Chapter 5
Linear Circuits

AO24
High-speed Op Amps — They're in a Class by Themselves

The same special characteristics that make fast op amps useful in difficult applications can also create problems for unwary designers.

Fast operational amplifiers are not like other op amps. In addition to good dc characteristics such as high open-loop dc gain, low bias currents and low input offset drift, fast op amps have specially designed ac characteristics that come into play at high frequencies. Proper application of these amplifiers involves the selection of gain-bandwidth product, slew rate, settling time and output current. In addition, you must pay particular attention to many small circuit details like power-supply bypassing, proper routing of grounds, short lead lengths and minimization of stray capacitance. Poor design practice invariably produces an oscillator instead of a high-speed amplifier.

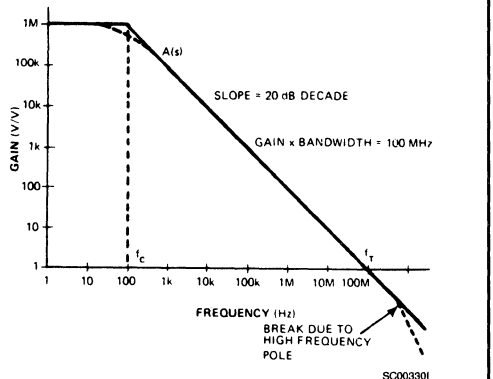


Figure 1: Well designed high-speed op amps have a smooth 20dB/decade roll-off. Additional amplifier pole should not occur until well beyond f_T.

YOU CAN'T IGNORE OP-AMP CHARACTERISTICS

Operational amplifiers offer designers one fundamental attraction: The characteristics of the closed-loop feedback circuit are determined almost exclusively by external circuit elements rather than by the op amp itself. Precise control of gain, offset, linearity, temperature stability, etc., in amplifier design itself thus reduces the user's task to the proper selection of the passive circuit components used around the op amp. Unfortunately, this simple relationship in general doesn't hold true for high-speed op amps: They're more difficult to handle than their low-frequency counterparts, and a detailed knowledge of their characteristics becomes essential:

Open-loop gain and bandwidth — Refer to Figure 1's gain-frequency (Bode) plot. The open-loop gain must be very high in a fast operational amplifier to reduce errors at the device's summing junction. Open-loop gain typically runs between 10^5 and 10^8 V/V in a good quality, high-speed op amp. As illustrated, the gain is flat from dc out to a corner frequency (100Hz in this case); then it decreases with increasing frequency. For well-designed amplifiers, gain decreases at a fixed rate of 20dB/decade of frequency, a roll-off rate that assures stable closed-loop operation and also produces the best settling-time performance.

The gain-frequency plot crosses the gain-of-one axis at unity gain frequency, f_T. This frequency should be as large as possible for a wide-band-width amplifier; 100MHz is common. Along the 20dB/decade slope of the gain roll-off, the product of gain and frequency remains constant and equal to f_T. Therefore, the value of f_T is frequently referred to as the gain-bandwidth product of the amplifier.

Smooth roll-off is generally maintained out beyond f_T for most fast amplifiers. Another op-amp pole usually occurs at a higher frequency as a result of a nonideal amplifier circuit, but if this frequency is considerably greater than the circuit's closed-loop bandwidth, the extraneous pole will have very little effect on high-frequency performance.

Slew rate — The ability of a high-speed op amp to reproduce fast, large signal outputs depends primarily on its specified slew rate, the maximum rate at which the output can change, expressed in V/μsec. When the output must respond to a step-input change, slew-rate limitation causes a longer large-signal settling time than you might expect from the bandwidth characteristics alone. Slew rates of modern high-speed op amps equal or exceed 1000 V/μsec.

Settling time — In servo theory this term specifies the maximum time required to achieve an accuracy of 5% or so after a step input is applied to the servo. With regard to op amps, it refers to the time required for much greater accuracies, typically 0.1% to 0.01% of F.S., and is best defined as follows:

"Settling time is the elapsed time from the application of a step input to an amplifier to the instant when the output has entered into and remained within a specified error band around its final value." Note that settling time must be specified with both the error band and the magnitude of the step change given. Almost all cases specify a F.S. output change of 10V.

TODAY'S FAST OP AMPS ARE FAST

Modular op amps introduced in the late 1960's featured settling times as low as 1 μsec to 0.01%, and they quickly became popular in 12-bit data-acquisition systems. Early in the 1970's, ultrafast modules became available, boasting even faster settling times, 100MHz gain-bandwidth products and 1000 V/μsec slew rates. More recently, hybrid units have achieved such performance levels, as shown below.

5

BASIC CHARACTERISTICS OF A TYPICAL HIGH SPEED OP AMP (AM-500)	
DC OPEN-LOOP GAIN	10^6 V/V
GAIN-BANDWIDTH PRODUCT	130 MHz
SLEW RATE	1000 V/μSEC
FULL POWER FREQUENCY (20V p-p)	16MHz
SETTLING TIME, 10V to 1%	70 nSEC
SETTLING TIME, 10V to 0.1%	100 nSEC
SETTLING TIME, 10V to 0.01%	200 nSEC
INPUT OFFSET DRIFT	1 μV/°C
OUTPUT VOLTAGE	±10V
OUTPUT CURRENT	±50mA

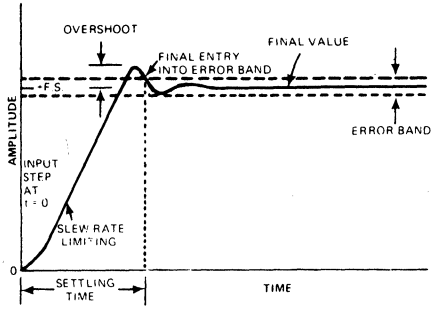


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Figure 2: Slewing time must be included in settling-time measurements.

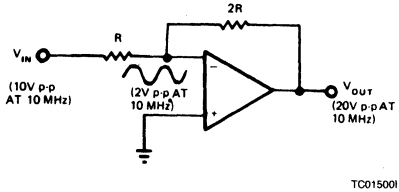
Figure 2 illustrates a typical settling response for a high-speed op amp. Usually the amplifier's output first goes into slew-rate limit, overshoots its final value, then enters the specified error band and remains there until it reaches the final steady-state level. (One word of caution: Measure settling time from t = 0, the instant that the input step was applied. Some manufacturers play "specmanship" games and fail to include the amplifier slewing time in their measurements.)

You can't predict amplifier settling time from bandwidth and slew-rate specifications alone: It's a measured, as well as designed-in, parameter. You can usually tell an op amp specifically designed for fast settling time from one that's not: The former's settling-time spec will be fairly predictable from bandwidth and slew-rate considerations; the latter's won't.

Low output impedance and high output current High-speed operational amplifiers almost always are designed to give low output impedance and relatively high output current. Low output impedance proves critical to stability for driving capacitive loads, while high output current (20 to 100mA) is required for both driving capacitive loads at high speed (I = Cdv/dt) and for driving relatively low-value feedback and load resistors. (Good high-frequency design practice keep all impedances as low as possible to cut phase shifts from parasitic capacitances.)

Why is input dynamic range important?

Figure 3 shows a simple, high speed op-amp circuit with an inverting gain of 2 to illustrate an important device characteristic. The signal input is a 10V p-p sine wave at 10MHz; the output, an inverted 20V p-p sinusoid. If we assume that the amplifier has the Bode plot shown in Figure 1, then its open-loop gain at 10MHz is 10. So for a 20V p-p output, the voltage at the op amp's summing junction must be 2V p-p. This is a rather large signal; in fact, most general-purpose op amps couldn't handle such a high level without distorting, limiting and/or clipping. Therefore, high-speed op amps must possess a large input dynamic range; i.e., significant peak-to-peak voltages applied directly across the device's input terminals must not cause the output to slew-rate limit or distort. Calculation of a high-speed op amp's input dynamic range is straightforward (see box at right).



TC01500I

Figure 3: The summing junction is NOT a virtual ground in high speed op-amp applications. Thus the amplifier must be designed with a large input dynamic range (IDR), or distortion, limiting or clipping will result.

Knowing the input dynamic range of an operational amplifier can help you determine how to best utilize the device while carefully avoiding slew-rate limitation problems. For instance, Figure 4 shows an op amp connected as a unity-gain inverter. If we assume that this device has an input dynamic range of ±1.23V (as calculated in the **box**), then the circuit can reproduce a 4.92V input step as a −4.92V output step without slew-rate limiting. (Observe that the 4.92V input step appears at the summing junction divided by a factor of two by the two equal-value resistors.)

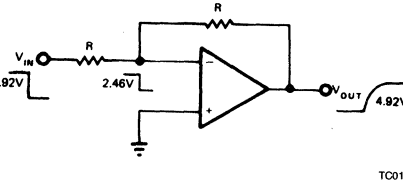


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Figure 4: Staying within an amplifier's IDR avoids slew-rate limitation problems and produces a smooth output response.

IDR is a function of SR and GB

The input dynamic range (IDR) of a high-speed op amp is related to the unit's slew rate (or full-power frequency) and its gain-bandwidth product. To compute IDR, assume that the output is at its full power frequency and amplitude (i.e., it's producing the largest and fastest output possible without distortion), then calculate the open-loop gain at this

frequency, and finally plug these values in the following formula:

$$IDR = (V_{pp} \times FPF)/GB$$

where V_{pp} = peak-to-peak full-power voltage, FPF = full-power frequency and

GB = gain-bandwidth product.

If the full-power frequency is not known, you can use an alternate equation:

$$IDR = V_{pp} \times SR/(20\pi GB)$$

where SR = slew rate.

EXAMPLE

What is the input dynamic range of the amplifier described in the previous **box** (the AM-500)?

$IDR = (20 \times 16MHz)/130MHz = 2.46V_{p-p}$ (or ±1.23V).

Thus, within an input range of ±1.23V, the op amp won't go into slew-rate limitation.

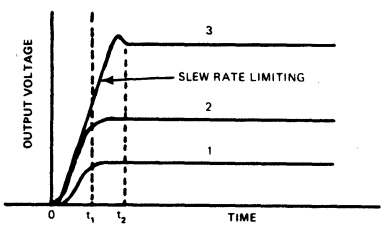

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Figure 5: Rise times for pulses of varying heights remain constant as long as you observe IDR limits.

To further appreciate the significance of input dynamic range, you must understand that within this input range the op amp's output rate of change is in direct proportion to the input voltage. Therefore, the output can make a large voltage transition in the time required to make a small voltage transition. Figure 5 illustrates three values of output steps for a fast op amp. Output steps 1 and 2 have identical rise times; since they lie within the IDR, they aren't slew-rate limited. Because Output 3 is generated outside the IDR, however, slew-rate limiting occurs, and the output takes considerably longer to reach its final value. Further, the waveform exhibits some overshoot, a common problem under slew-rate limit conditions.

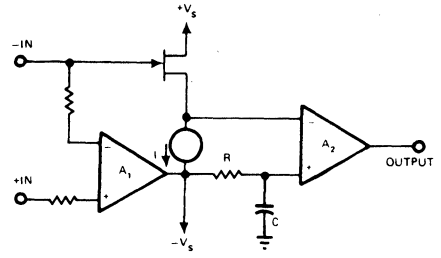

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Figure 6: Fast-feedforward amplifier design combines a low-drift bipolar IC op amp with an FET feedforward stage to produce excellent dc and ac characteristics.

It's no trivial task to design an op-amp input circuit that has good dc characteristics, plus good input dynamic range, plus the response needed to avoid slew-rate limiting. One approach combines the low-drift characteristics of a bipolar input op amp with the excellent IDR of an FET in a fast-feedforward design (Figure 6). This circuit produces very wide bandwidth, high slew rate and fast settling time. It also provides extremely high open-loop gain and very low input offset-voltage drift (typically 1μV/°C).

Your choice should start with bandwidth

When you select a high-speed operational amplifier, first determine your application's bandwidth requirement. The minimum closed-loop bandwidth is a function of both the op amp's gain-bandwidth product and its noise gain in the application. "Noise gain" is defined as the gain of the closed-loop amplifier to voltage noise or to any other signal inserted in series with one of the amplifier inputs (Figure 7).

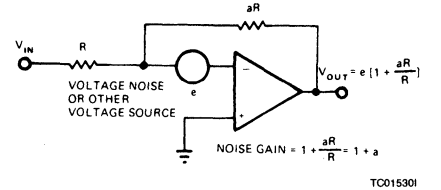

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Figure 7: Noise gain and signal gain differ. In an inverting circuit the noise gain equals the signal gain plus one.

The noise gain drawn on the Bode plot of an op amp determines the −3 dB closed-loop bandwidth. In Figure 8, for example, closed-loop gain equals 99, giving a noise gain of (1 + a) or 100. When plotted on the diagram, this noise gain gives a closed-loop 3dB bandwidth of 1MHz for the 100MHz gain-bandwidth amplifier illustrated.

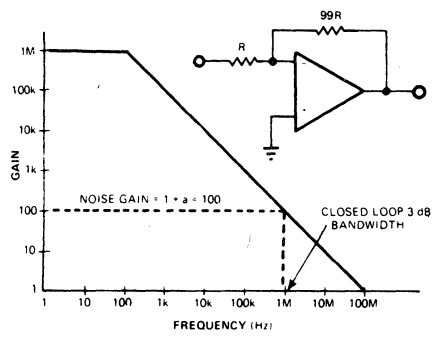

Figure 8: If the op amp exhibits a single-pole response, you can compute its settling time from frequency and noise-gain data. This approach works best at high noise gains.

(Note that for the common unity-gain inverting amplifier, the noise gain is 2; therefore the closed-loop bandwidth of such a circuit built with a 100MHz op amp would equal 50MHz, not 100MHz.)

A single pole simplifies response calculations . . .

If an op amp has a true single-pole response (as many do), you can calculate its step response for the closed-loop circuit by the expression:

$$E_{OUT} = aE_{IN}\ (1\text{-}e^{-2\pi f_T/(1+a)})$$

and the output error is then

$$\epsilon = e^{-\pi f_1/(1+a)}$$

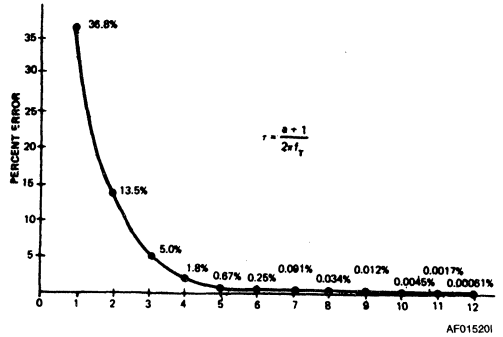

Figure 9: Output error decreases predictably as a function of the number of time constants when the op-amp circuit exhibits a single-pole response.

From the latter equation you can readily compute the settling time to various accuracies. For greatest convenience, perform this computation in terms of the time constant $\tau = (a + 1)/2\pi f_T$, where a is the closed-loop gain. The amplifier configuration of Figure 8, for instance, has a time constant (τ) of 159 nsec.

Figure 9 shows the number of time constants necessary to reach a given error, assuming a single-pole response. Thus, the amplifier configuration of Figure 8 would take nine time constants or 1.44μsec to settle to 0.01%. If the same amplifier (GB = 100MHz) were connected as a unity-gain inverter, its closed-loop bandwidth would equal 50MHz, giving τ = 3.2 nsec and a settling time to 0.01% of 28.8 nsec.

Using the ideal single-pole response with no slew-rate limiting to determine settling is a valid approach. At worst it gives a first approximation of the settling time, and this approximation gets closer at high noise gains. Given an op amp designed and specified for fast settling, you can obtain an even closer approximation by adding to the computed settling time that estimated extra time required to slew to the final voltage.

. . . but multiple poles often occur

In some cases the op-amp circuit is not really a single-pole system. Figure 10 shows three typical situations that add a second pole to the circuit. C_1 represents the input capacitance of the amplifier plus any stray capacitance from the summing junction to ground, as well as (where applicable) the output capacitance of the device driving the op amp. C_1 combines with resistances R and aR to produce a pole located at $-aRC_1/(a + 1)$ on the real axis of the s-plane. The finite output resistance of the amplifier, R_{11}, and load resistance R_1 combined with output capacitance C_L can add another pole located at $-R_OR_LC_L/(R_O + R_L)$. And the op amp itself can add a third extraneous pole if it has an extraneous high-frequency pole in its response as noted.

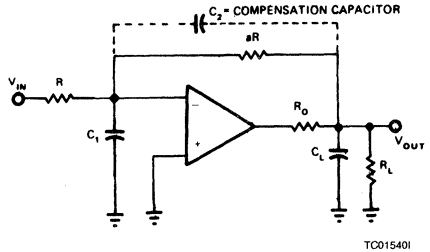

Figure 10: Three sources of extraneous poles appear in this diagram; input capacitance, load capacitance and the op amp itself. C_2 compensates for output ringing and is best chosen via experiments with the actual circuit components and layout.

In general, one of these "extra" poles will be dominant; i.e., closer in frequency to the amplifier's unity-gain frequency than the others. This dominant pole, of course, converts our first-order system into a second-order one and brings up the possibility of complex conjugate poles that produce ringing.

When ringing occurs, the amplifier must be compensated by a feedback capacitor (Figure 10). You can determine experimentally the optimum value for this compensation

capacitor by observing the step response and adjusting a trimmer to eliminate the ringing. Normally you want a damping ratio of one, but in some applications you may actually prefer a small amount of overshoot.

Calculations reveal that if the frequency of the second pole is at least 4 x the op amp's closed-loop bandwidth, the damping ratio will equal or exceed one, and overshoot won't occur. Since often you can quickly approximate the frequency of the extraneous pole, you can use this relationship to predict ringing in the circuit.

In the common situation where input capacitance C_1 causes the second pole, a good starting value for compensation capacitor C_2 is $C_2 = C_1/a$. Increase C_2 as necessary above this value to achieve a damping ratio of one. (The other two possible extraneous poles, even when they don't dominate, may still add some phase lag to the amplifier. This possibility explains the somewhat higher value of C_2 often needed to give the required compensation.)

Success is just a design tip away

We conclude our discussion by offering six brief, but important, hints on applying high-speed op amps:

- Keep all component leads as short as possible, particularly at the summing junction. Also, diligently strive to keep stray capacitance at the summing junction to an absolute minimum.
- Separate signal grounds from power grounds, connecting them only at one common physical point.
- If you must locate the source or load some distance from the op amp, use properly terminated coaxial cable for best response.
- If you mount the op amp on a pc board, incorporate a ground plane into the board's design for best performance.
- Make the input and feedback resistors as small as possible consistent with input-source drive capability and amplifier-output drive capability. A value in the range of 500 to 1000Ω is commonly used for the input resistor.
- Use good power-supply bypass capacitors and connect them right at the amplifier power-supply pins. We recommend tantalum capacitors in parallel with ceramics.

AO50
Using the IT500 Family to Improve the Input Bias Current of BIFET OPAMPS

INTRODUCTION

The LF156 family of BIFET OPAMPS is very popular because of the combination of high slew rate (typically 12V/μs @ unity gain) and moderate offset voltage (about 2mV). Input bias current, however, varies directly with input voltage, rising from 30pA @ $V_{IN} = -10V$, to 50pA @ $V_{IN} = 0V$, and finally to 80pA @ $V_{IN} = +10V$. This can be improved markedly by using one of the IT500 series to drive the inputs of the LF156.

The constant current source can be designed with any transistor pair having a high beta @ $I_C = 400\mu A$. See Figure 2.

An added bonus of the IT500 is its CMRR > 100dB, compared to the LF156 CMRR of 85dB.

This configuration is ideal for electrometer circuits, with good measurement accuracy down to 10pA of input current (< 10% error with 10pA of input current). A 10MΩ glass feedback resistor connected between the -INPUT and OPAMP OUTPUT does the trick. Other possible applications include sample and hold amplifiers, instrumentation amplifiers, etc.

Although this application note has dealt solely with the LF156, all present day BIFET OPAMPS exhibit the same I_{BIAS} vs. V_{IN} dependancy, and all will benefit from using the IT500 as a preamplifier.

The IT500, like the others in its family, is a dual cascoded n-channel JFET pair, featuring a typical input bias current of < 1pA with inputs ranging from -15V to +15V; actual I_G is guaranteed to be less than 5pA @ $V_{DG} = 50V$.

Figure 1 shows an IT500 being used to drive the inputs of an LF156. This greatly reduces the input bias current, and in no way affects the already superior slew rate; the offset voltage is not significantly degraded because of the excellent matching of the IT500.

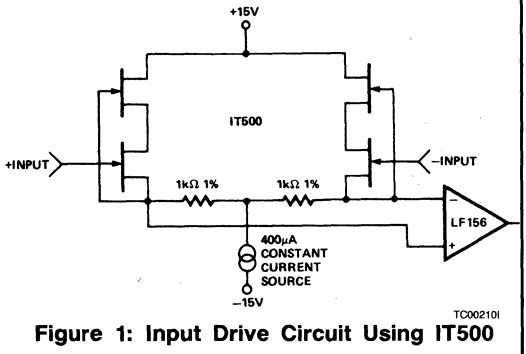

Figure 1: Input Drive Circuit Using IT500

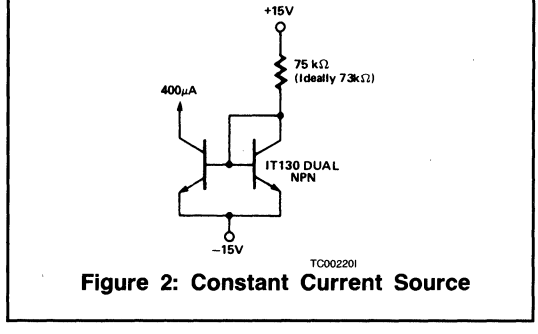

Figure 2: Constant Current Source

AO53
The ICL7650: A New Era in Glitch-Free Chopper Stabilized Amplifiers

by Peter Bradshaw

INTRODUCTION

Op Amps

Historically, the biggest single problem with the application of op amps has been the input offset voltage. This is indicated by the fact that almost all important op amps from the μA741 and LM101 on have offered offset null adjustment pins, special screening to low offset voltage values, and/or internal V_{OS} trimming (laser or Zener-zap). Also consider the extensive series of specifications devoted to its variability with temperature, time, common-mode voltage (CMRR), power supply (PSRR), output voltage (A_{VOL}), and sometimes even down to variation of temperature drift with offset null correction. Contrast this with the treatment afforded one other important (error-causing) input parameter, input bias current, which usually gets just a specified value under one set of conditions, a variation over temperature, and a term relating to its matching between the two inputs. If variation with common-mode voltage, power supply voltage, etc., is covered, it is generally only in a "typical curve" buried in the middle of the data sheet.

The answers to this concern have been many and varied. Several modules use chopper stabilization to provide very low offset voltages, although most of these do not provide differential inputs and they also have problems with input frequencies near the chopping rate (see Intermodulation Effects). The devices are typically bulky and expensive, and the two-path approach frequently used (Figure 1) tends to adversely affect settling times; the high-speed path and the low-speed path will settle to different points unless the pole-zero pairs are extremely well matched. The only monolithic chopper-stabilized devices previously available are probably best described as disappointing and expensive.

Therefore, considerable effort has been expended to improve the offset and drift characteristics of standard op amp devices, and some very good results have been achieved with several bipolar input devices, such as the OP-05 and OP-07. Careful die layout and circuit balance, in many cases combined with internal offset null trimming, bring initial offset voltages under 100μV, and temperature drifts below 0.5μV/°C. Although this is over an order of magnitude better than a good grade of μA741 or LM101A, there is still much room for, but little realistic hope of, substantial further improvement in this direction. In addition, the requisite screening of parts is expensive, even with currently available levels of automation.

Technology

In the last few years, a new technology, in the shape of CMOS, has entered the analog field, and has led to the introduction of a range of products previously only dreamed of. Most spectacular, perhaps, has been its rapid dominance of the A/D and D/A converter market (Figures 2 and 3). Today very few converter systems are being designed that don't use CMOS devices specifically intended for this purpose, and in most cases they provide virtually the whole function. More recently, CMOS technology has moved into the more traditional building blocks of analog circuits, so that now CMOS versions of the standard bipolar op amps, regulators, and timers are available, with comparable or better specifications, lower power dissipation, and close to competitive pricing (Figures 4-6). However, although these devices have solved many traditional op amp problems, input offset voltage and low frequency noise voltage were not among them. Using the op amp and analog switch capabilities of this CMOS technology, Intersil introduced in early 1979 a new approach to the low offset voltage requirement, the Commutating Auto-Zero or C_{AZ} amp, shown in Figure 7.

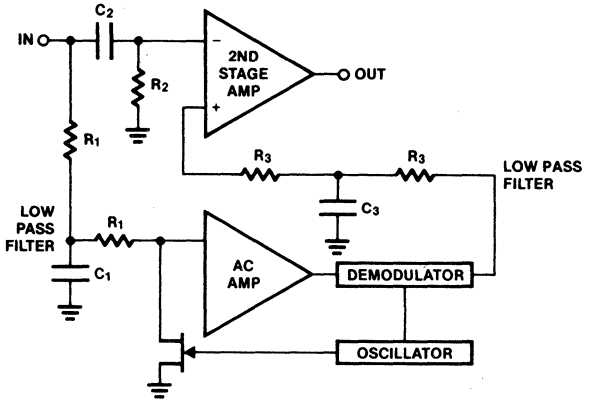

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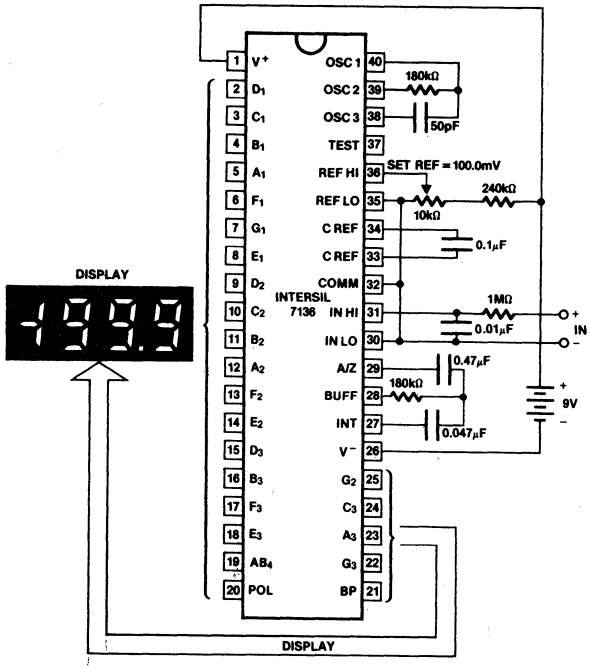
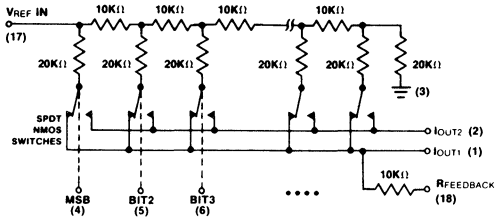
Figure 1: Typical Module Chopper-Stabilized Amplifier



CD00460I

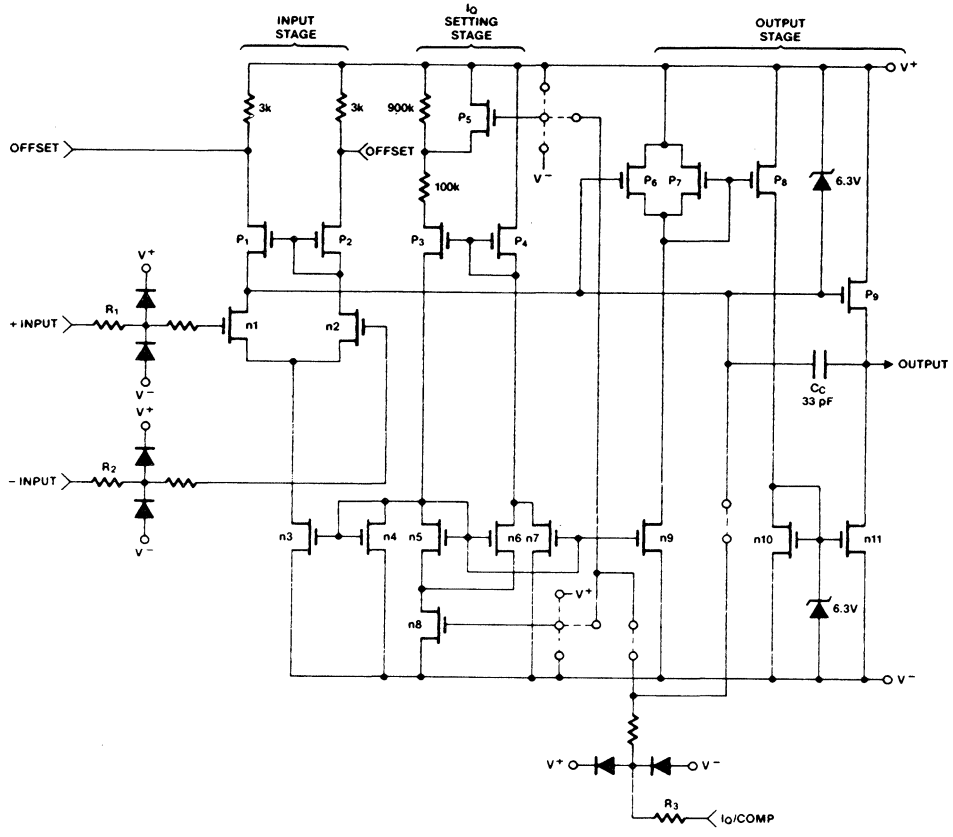
Figure 2: LCD Digital Panel Meter Using the ICL7136 CMOS A/D Converter



(Switches shown for Digital Inputs "High")

TC01790I

Figure 3: CMOS D/A Converter Functional Diagram (AD7541)



DS01030I

Figure 4: CMOS Op Amp Schematic (ICL7611 Family)

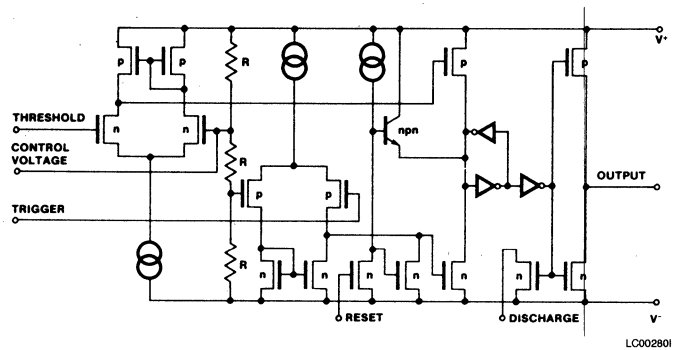


Figure 5: ICM7555/7558 CMOS Single and Dual Timers

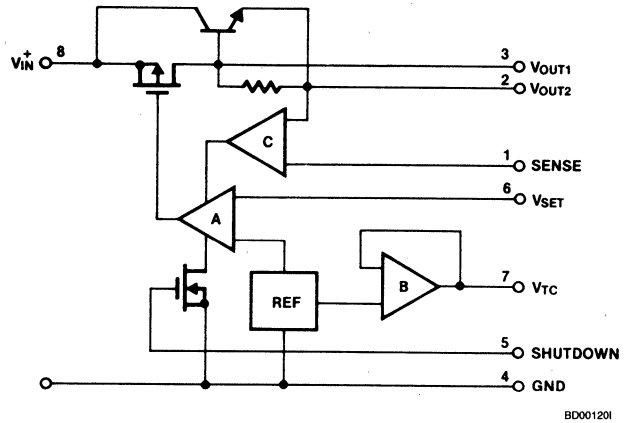


Figure 6: Functional Diagram of the ICL7663 CMOS Regulator

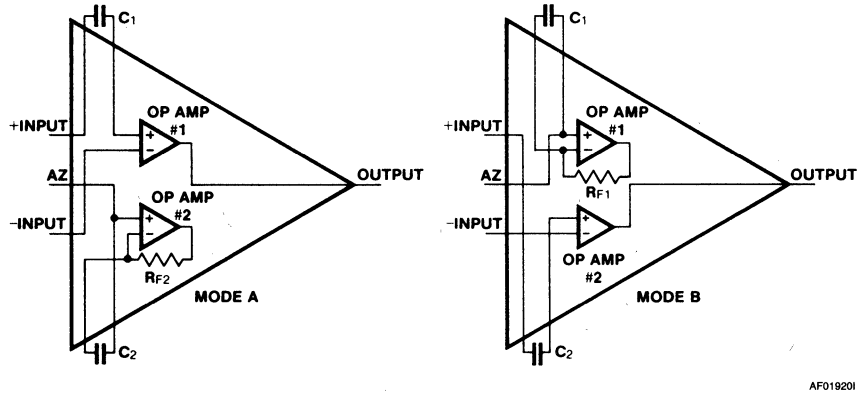


Figure 7: ICL7600/ICL7601 Commutating Auto-Zero (C_{AZ}) Operational Amplifier Showing Two-Cycle Operation

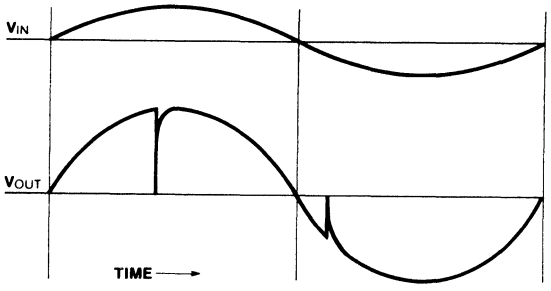


Figure 8: Output Spikes Due to Commutating Operation

These devices at once became the best monolithic amplifiers available in terms of offset voltage (at 5μV) and time and temperature drift. They utilize two internal op amps, one active while the other auto-zeroes itself into an external capacitor. Upon commutation, the roles change and the active op amp uses its capacitor to cancel its offset. Two capacitors are needed, but the values and characteristics are not critical. Although offering three orders of magnitude improvement over the input characteristics of the μA741/LM101A type, and nearly two orders of magnitude over the best bipolar devices in offset and drift, the C_{AZ} principle has some disadvantages. The input current does not exploit the CMOS capability fully, and there is appreciable spiking at both the input and output (Figure 8). This can be largely removed by filtering, but that limits the available bandwidth.

SYNTHESIS

Intersil therefore decided to try to overcome all these problems by applying the capabilities of CMOS technology to the principle of the chopper-stabilized amplifier. The result is the ICL7650, whose Functional Diagram is shown in Figure 9. The use of a single full-time main amplifier avoids any output glitches, and input switching glitches are minimized by careful area- and charge-balancing on the network of input switches. The chopping operation is performed by means of a nulling amplifier, which shares one input with the main amplifier. The other input is switched alternately between the two main amplifier inputs (Figure 10). When the inputs are shorted, its output drives a null point on itself, and when the inputs are across those of the main amplifier, it drives a null point on that amplifier. The two null points are the back-gates (often called "body connections") on the mirror transistors of the input stage, and by bypassing these to the equivalent point on the other leg with external capacitors, a simple low-leakage automatic offset null arrangement is achieved. Full differential input capability is retained, and the impedances on the two inputs are well balanced. The input stage legs are merged, as shown in Figure 11, to reduce the input noise and improve balance and high-frequency CMRR, etc.

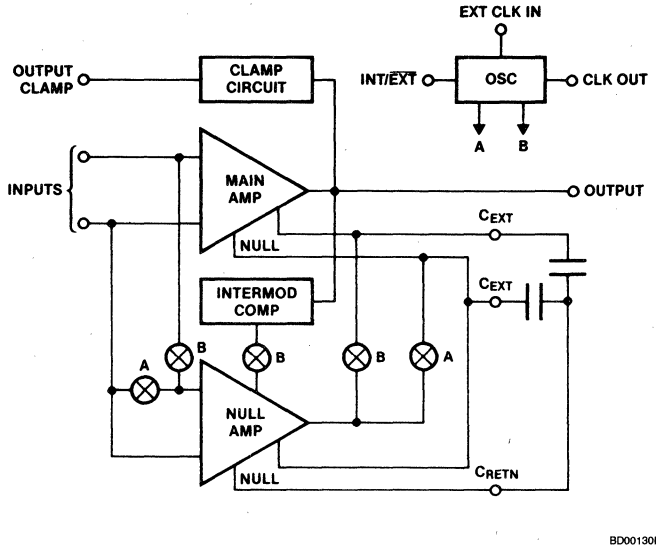


Figure 9: Functional Diagram of ICL7650

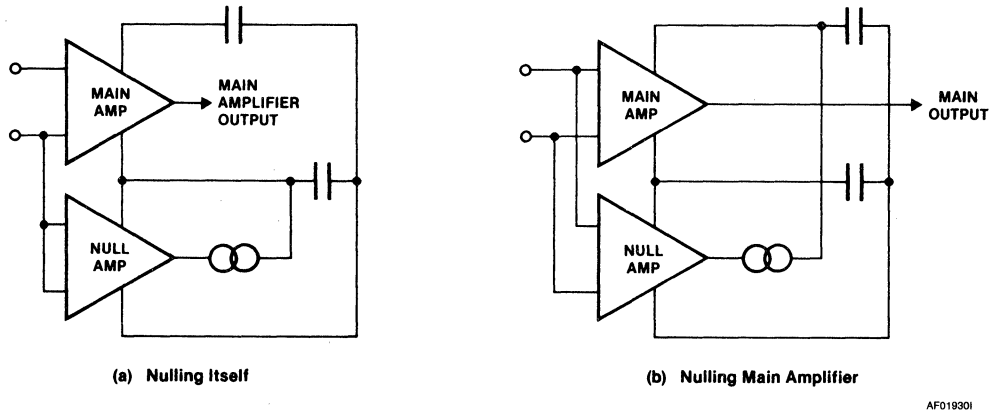


Figure 10: Two Phases of Nulling Operation

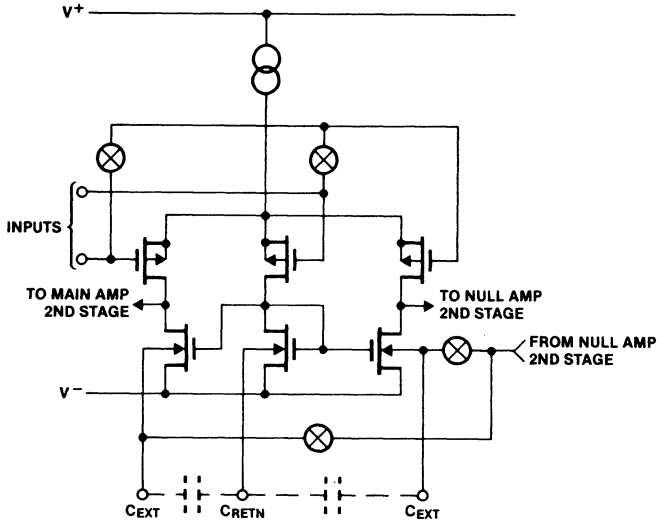
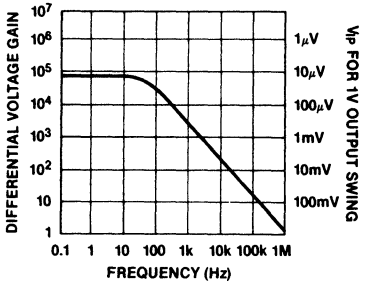


Figure 11: Three-Legged Input Stage (Simplified)



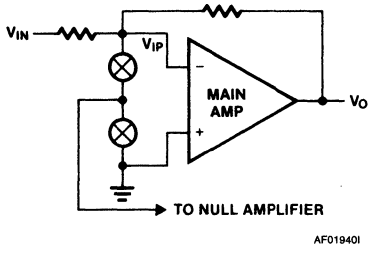


Figure 12: Gain Roll-Off and Input Voltage (Main Amplifier Alone without Null System) vs Frequency

The circuit automatically provides correction (at DC) for CMRR, PSRR, and A_{VOL}, to the same level as for V_{OS} (typically under 1μV), and the I_B remains in the low pA area, set by the leakage of the input switches (also acting as protection diodes) and the small net charge injection. The latter is doubly-balanced both by careful device matching and by the excellent recovery of any residual injection, due to the equipotential nature of the inputs. The open-loop gain-bandwidth product and the slew-rate are set purely by the main amplifier. The null system time constant is controlled by the effective g_m to the output of the nulling amplifier and the external capacitors, and is readily controlled to be much longer than the chopping period. In addition, the "injection" of the nulling signal into the first stage of the main amplifier ensures that the pole-zero match at this cross-over point is no problem.

INTERMODULATION EFFECTS

Two residual problems remain with the usual chopper-stabilized amplifier circuits. One of these is the intermodulation between applied signals and the chopping frequency, as mentioned earlier. This arises because the main amplifier has finite gain near this frequency, and so develops a small differential input signal to sustain the requisite output (distinct from any DC offset voltage). This signal is, of course, at the signal frequency, and has an amplitude determined by the gain roll-off characteristics (Figure 12) and the signal amplitude, and will be seen by the nulling circuit as an error signal equivalent to an input offset voltage. This circuit will then attempt to null out the input signal during the active null time. If the difference in frequency between the signal and the chopping rate is large compared to the null circuit time constant, this attempt will essentially fail, since the proposed direction of change will vary between (or during) each null time in such a way to

lead to little net resultant. On the other hand, if the signal and chopping frequencies are close together (in terms of the time constant), the null circuit will respond at the beat frequency, leading to two undesirable results. First, the gain and phase characteristics will be disturbed in the neighborhood of the chopping frequency, since the amplifier input signal will be partially reduced, with some delay. Second, the effective input will include a component at the beat frequency, not present in the true input.

The ICL7650 minimizes this problem by the simple expedient of introducing a compensating dynamic offset voltage in the nulling amplifier. This is possible since, at the frequency range of interest, the AC signal that causes the problem is a function only of the compensation capacitor, the input stage g_m, and the output signal amplitude. By adding another capacitor from the output signal of the main amplifier to the corresponding summing point in the nulling amplifier, with a value which is correctly scaled to allow for the ratio of the input stage g_ms, and connecting it only during the time when the main amplifier is being nulled, the nulling amplifier does not see the input-related signal at the main amplifier. Thus, no nulling signal is generated, and no beat frequency is generated. The required matching of the g_m and capacitor values is readily achieved, since they are all on a monolithic die, and the result is a device with virtually no interference between the normal operation of the main amplifier and the chopping action of the nulling amplifier.

OVERLOAD EFFECTS

The second traditional problem with chopper-stabilized amplifiers relates to their behavior under overload. Once again the problem arises through the presence of an input signal on the main amplifier which is not due to the input offset voltage. In this case, the presence of a large signal in the system leads to the output running up against the supply rails. Under these conditions the amplifier no longer has control, and the voltage at its input becomes only a function of the feedback network, the input signal, and the output swing limit of the amplifier, as shown in Figure 13. The nulling amplifier, however, has no means of knowing that this is the problem, and will attempt to "rectify" it by driving the null network to remove this input signal. This effort cannot succeed, and in fact will increase the depth of overload. If this condition is maintained long enough (compared to the nulling time constant), the null circuit itself will also be driven to its limit. Thus, when the input signal returns to an inrange value, the input offset voltage will be skewed heavily to one side. If the nulling range of the amplifier exceeds the input signal range, frequently the case in the high-gain applications common for such devices, the output will remain stuck at the supply rail until the null circuit has almost recovered. Since the null amplifier driving signal may be quite small, recovery may take a long time.

Several possible methods can be used to combat this effect. One is to detect the output limiting condition, and to stop the chopping operation during the time that this does (or can) occur. This has two disadvantages. It may not be possible to predict such overrange conditions, nor easy to detect their occurrence either. Further, even if this is done successfully, the nulling system will be unable to correct the inevitable loss of true null caused by leakage currents on the null points, etc. Thus, an extended overrange interval with the chopping stopped can leave the null badly disturbed, perhaps as much as when the chopping is active. Nevertheless, in situations where an overrange occurrence is predictable or readily detectable, and lasts only for a limited time, the technique is very useful. The ICL7650 facilitates this form of overload effect amelioration by providing an EXT CLK IN pin (in the 14-pin versions), which can be held "low", stopping the chopping action in a position where no capacitor charging can occur, and by allowing judicious use of the CLAMP pin (see below) as an overload detector.

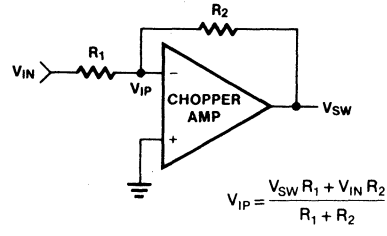


Figure 13: Voltages in Inverting Amplifier with Overload Input

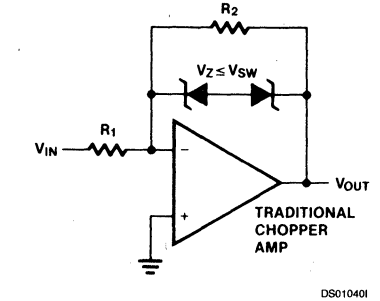
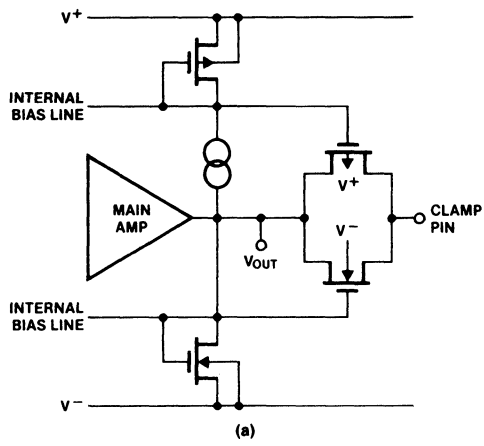


Figure 14: Avoiding Overload with Zener Clamps



(a)

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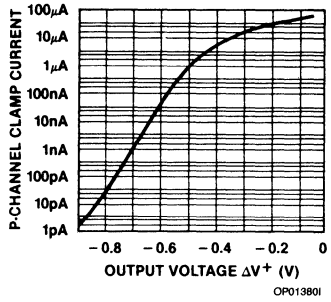

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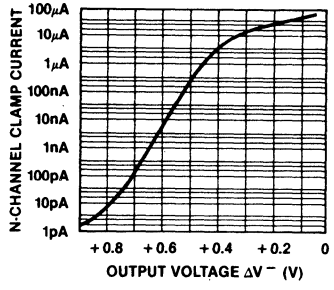


(b)

OP01390I

Figure 15: Output Clamp Circuit (a) and Conduction Characteristics (b)

The other technique for avoiding the overload problem involves adding a nonlinear element to the feedback network, so that overrange inputs do not cause the output to limit against the supply rail. One possible way of doing this is to parallel the feedback element with a pair of Zener diodes which conduct just before the limiting would occur, as shown in Figure 14 for the inverting configuration. The non-inverting arrangement is similar, but only reduces the gain to unity after the Zeners conduct. One disadvantage with this circuit is that the Zener voltage is quite critical, especially if the supply voltage variation is significant and the maximum allowable swing is desired. The ICL7650 avoids both of these problems by providing a CLAMP pin which will conduct current in the appropriate direction whenever the output voltage gets within a few hundred mV of either supply. The internal schematic is indicated in Figure 15a, and the output current characteristics as a function of the voltage margin to the supply rails in Figure 15b. The leakage currents due to the small N and P channel MOSFETs are negligible, and they can only be turned on if their common sources, tied to the output, get close to the relevant rail. If this pin is tied to the inverting input to the amplifier, and the impedance at this point is adequate, the desired limiting is readily achieved, with no disturbance to the null network, and usually negligible effect on the input bias current. The only penalties paid for this overload protection are a slight limitation on the output swing, and an increase in the input current on the inverting input when the output swings close to the rail. Also, the input circuit is not quite so easily guarded on a PC board if the CLAMP pin is used.

DEVICE CHARACTERISTICS

The net result, then, of all this technical wizardry is an op amp with quite remarkable characteristics. The input error-related parameters are unprecedented in a monolithic device, and rare indeed against all competitors, with a V_{OS} of under 5μV (typically under 1μV) and an input bias current of no more than 10pA. The V_{OS} value is maintained over the full range of the power supply, input common-mode, output swing, and temperature ranges. In other words the PSRR, CMRR, A_{VOL}, and dV_{OS}/dT or drift are all virtually unmeasurable, and well over 120dB, 120dB, 140dB, and under 10nV/°C, respectively. The long-term drift, which we can consider to be very very low frequency noise (as indeed it is from a device physics point of view), is also undetectable.

The other device characteristics also compare favorably with those of the μA741 and LM101 type. The Gain-Bandwidth product and slew rate are both about 3 times higher, at 2MHz and 2.5V/μs respectively, the supply current is about the same, at 2mA (3.5 max), the stability margin is similar, and the output swings between the supply rails. The only significant limitations on its use are the reduced supply voltage range (±8V max) and the 10kΩ load limitation. These are becoming less important with the growth of ±5V analog systems, and also can be readily side-stepped, as shown in the Applications section below.

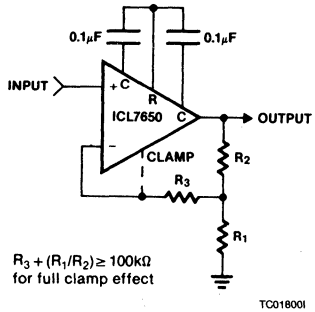
And to cap it all, this paragon of op amp virtue is a moderate-sized monolithic die made with a high-yielding mature low-cost process, so the device cost is quite low.

APPLICATIONS

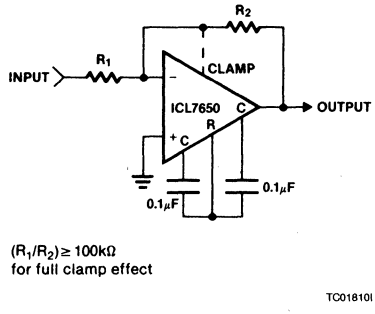
So much has been written about op amp applications over the last few decades that there is little point in trying to reproduce it all, even with revised specifications and capabilities. The most important point to be appreciated is that in any application where the performance of the circuit can be significantly enhanced by a reduction of input offset voltage and/or bias current, the ICL7650 can be put right to work. Further, any circuit using a null-trimming pot is an immediate candidate for replacement, since the cost of purchase, insertion, initial adjustment, and especially peri-

odic readjustment will generally be greater than the initial small premium for this device and two capacitors. Otherwise, the finite space available here will be used to present the particulars of this substitution as germane to the ICL7650, followed by the details of some circuits that utilize the specific capabilities of the part particularly well, and some combinations with other devices that concatenate their respective features.

The normal substitution requires nothing but the replacement of any null trim pot with two required capacitors. In the case of the 14-pin devices, the pinout corresponds to that of the LM108 type device, so substitution of the ICL7650 for a (rare) 14-pin LM101/A, LM107, μA741, OP-05/OP-07, or any similar part, can be done most readily with the 8-pin version. The alternative involves a minor PC board change. If good overload recovery is a requirement for the application, the connections to the CLAMP pin (see Overload Effects) should be made according to the basic configurations of Figure 16. The impedance at the point of attachment needs to be high enough, at least at DC, to permit the worst case input signal to be accommodated within the capability of the CLAMP pin output current, according to the curve of Figure 15b. Usually this is easily managed in the case of the inverting configuration, but in the non-inverting case, some additional input clamping may be necessary. Some alternatives for doing this are shown in Figure 17.

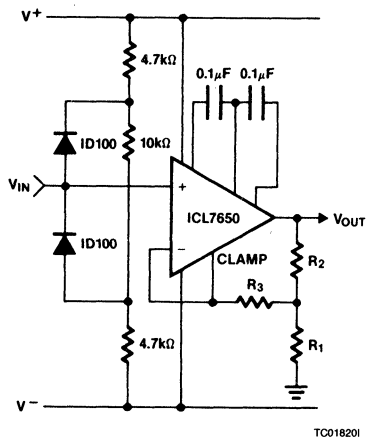


(a) Non-Inverting Amplifier



(b) Inverting Amplifier

Figure 16: Non-Inverting and Inverting Configurations with (Optional) Clamp Circuit Connection



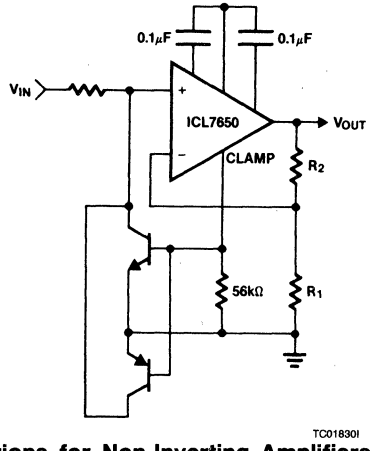


Figure 17: Some other Clamping Configurations for Non-Inverting Amplifiers

One frequent use of an op amp is as a comparator. This cannot be done with the usual chopper amplifiers because of their terrible behavior under overload conditions, the normal operating mode for an op amp so used (see Overload Effects). However, the optional overload avoidance feature built-in to the ICL7650 allows its use in many of these applications, as shown in Figure 18. The current from the CLAMP pin forces the inverting input to follow the signal input (within the output swing and input common-mode ranges), and the transfer characteristic is essentially a reflection of the characteristic of Figure 15b. The comparison voltage must be capable of absorbing the CLAMP pin current without distress to itself or other parts of the system. Only one polarity of comparison is possible with a high input impedance, but if a low impedance drive input is available, the roles can be reversed to achieve the other polarity. The speed of the circuit is limited to input ramp rates under 100V/sec for the most accurate performance, but above this rate the timing errors of most comparators exceed their input offset errors in any case.

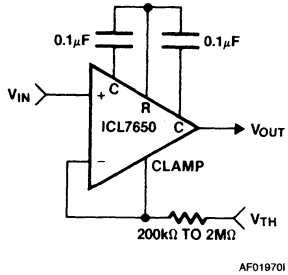


Figure 18: Low Offset Comparator

The usual instrumentation amplifier configurations work extremely well with the ICL7650. The standard three op amp configuration (Figure 19) has unbeatable CMRR, a function only of the resistors in practice. With a differential input A/D converter, such as the Intersil ICL71X6, 71X7, 7109 or 7135, just two ICL7650s will maintain high differential gain without any common-mode gain, ideal for pre-amplification of signals from such bridge-type transducers as strain gauges, etc. The arrangment is shown in Figure 20. This also works well with thermocouples whose shielding is grounded at the sensing end, especially in a noisy environment. Note that the offset and drift of the ICL7650 will contribute less than 1°C initial error and less than 0.2°C drift error to an absolute Platinum — Platinum/Rhodium Type S thermocouple between 0°C and 1750°C, or to a Type B thermocouple between 500°C and 1820°C (over the operating temperature range of the ICL7650). This is less than the errors associated with standard thermocouples themselves. Naturally, to realize this performance, all the other little thermocouples between the leads, the PC board, any IC socket, and the other components, etc., will have to be carefully handled. This topic is discussed in Achieving the Full Benefits.

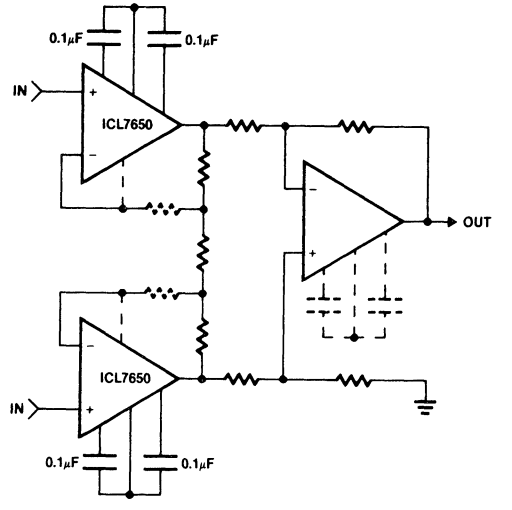


Figure 19: 3 Op Amp Instrumentation Amplifier

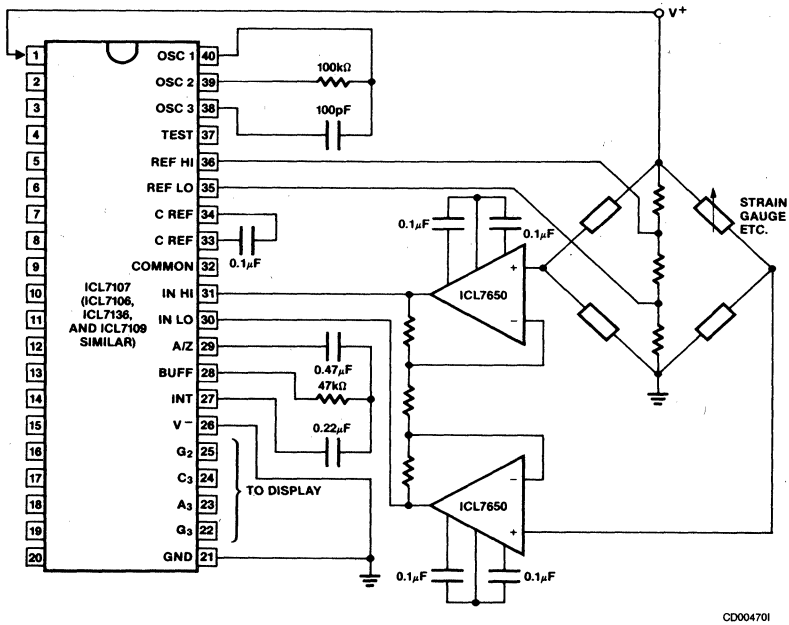


Figure 20: 2 Op Amp Differential Preamp for ICL7106/7/9 Families

Conventional logarithmic amplifiers have very high dynamic ranges in the current input mode, but in the voltage input mode they end up severely limited by errors associated with the input offset voltage of the input op amp. Two methods are available to combat this problem with the ICL7650. The device itself may be used as the main amplifier, as suggested in Figure 21. This will give a wide dynamic range of close to 6 decades. However, this arrangement lacks the built-in temperature compensation and scale factor adjustment of such monolithic log amps as the Intersil ICL8048. These can be combined with the same dynamic range enhancement by using the ICL7650 to offset null an ICL8048, as shown in Figure 22. The time constant of the nulling network needs to be high enough to avoid loop stability problems. The input current of the system will not be degraded by this configuration, so 6 decades of dynamic range will be available in both voltage and current input modes.

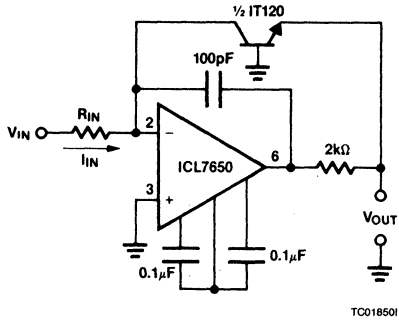


Figure 21: Basic Log Amplifier

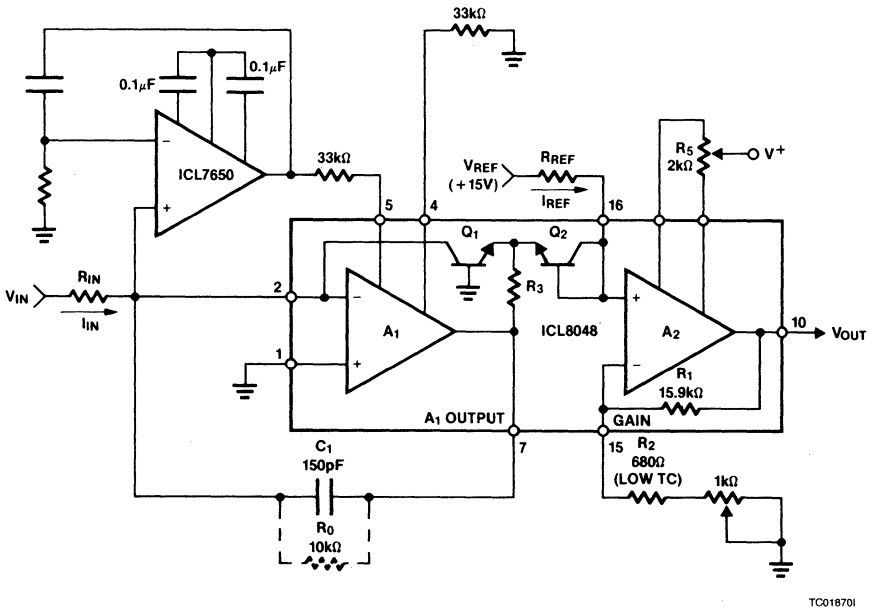


Figure 22: ICL8048 Offset Nulled by ICL7650

Although the overall performance of the ICL7650 is unprecedented, there are some parameters for which other devices remain better, and it does have some limitations. We have already mentioned the supply voltage limitation, for which the promised circumvention appears in Figure 23. The two JFETs have I_{DSS} values well above the supply current requirement of the ICL7650, and so operate close to "pinch-off". These "pinch-off" voltages constitute the supply voltages to the ICL7650, and must meet the specifications required, readily done with the parts listed. By boot-strapping the JFET gates to the output, a follower circuit whose input and output can span the full supply range can be constructed. High voltage JFETs would permit even higher supply voltages. A small amount of high-frequency roll-off is usually needed in the boot-strap to prevent RF instability.

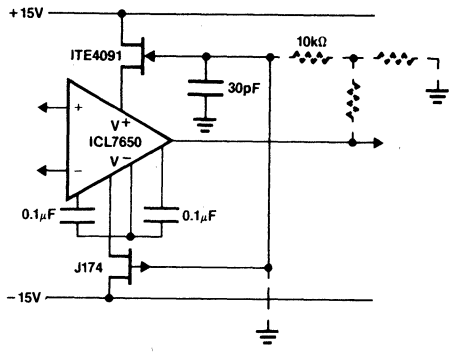


Figure 23: Operating with ±15V Supplies

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The output drive limitations may be readily overcome by buffering the ICL7650 with a device such as the μA741, after the fashion of Figure 24. This has the additional advantage of reducing the dissipation in the ICL7650 due to the load, and the thermal effects associated therewith (see Achieving the Full Benefits). These two circuits may be amalgamated in several ways to combine higher voltage operation with heavy load driving capability, such as those shown in Figure 25. One or more of these can be used to construct a configuration that will act correctly in any inverting or noninverting application, for any gain required. These circuits can be used to substitute for virtually any chopper-stabilized module, and most other standard op amps also, with a substantial improvement in input parameters and no loss in output characteristics.

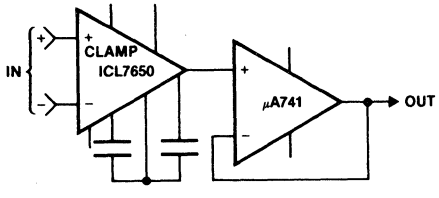


Figure 24: Using 741 to Boost Output Drive Capability

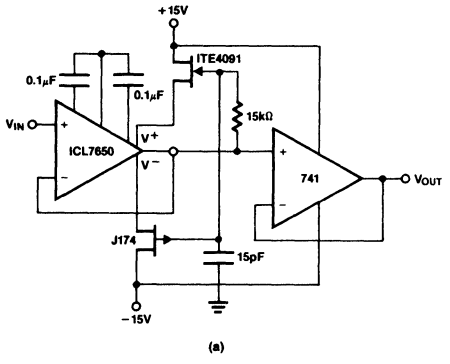
The high slew-rate and/or bandwidth of devices such as the HA2500/10/20 and the HA2600/20 families is not, of course, preserved by the arrangements of Figure 25. For these types of devices, the concept used in Figure 22 is preferable. Figure 26 shows two methods of doing this for several high speed devices, and Table 1 gives suitable component values. Note that although the input offset voltage is that of the ICL7650, the input current will generally be dominated by that of the other device. Also, no protection is provided against overload, and intermodulation is back (see Intermodulation Effects and Overload Effects). These three can be reduced or eliminated by extra complexity in the circuits, at the expense of further loss in generality. Figure 27 shows one method of balancing out the intermodulation terms, and a similar clamp circuit to that of the ICL7650 added externally.

A similar combination of the exceptional low noise performance of the OP-05 (and OP-07) with the ICL7650 is also possible, and incidentally gives the lowest available overall noise performance in any bandwidth from true DC to any other frequency of use with op amps. In this case, the roll-off in the external nulling network should be low enough in frequency to ensure that the cross-over between the two devices does not degrade the performance in the bandwidth of concern. The schematic, in Figure 28, is otherwise the same as that of Figure 26, and Table 1 includes the values for this circuit also. Many other combination circuits have been published in the literature, and the ICL7650 can be used to advantage in the majority of them.

Table 1

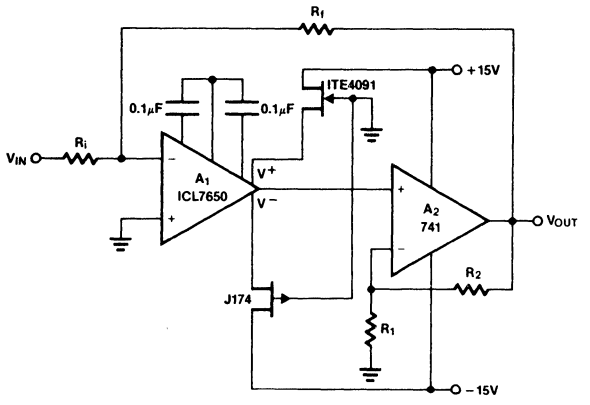
DEVICE FAMILY	WORST FAMILY V_{oe} (mV) OVER TEMP.	LOWEST SUPPLY VOLTAGE ±V	FIGURE 26(a) CIRCUIT				FIGURE 26(b) CIRCUIT		
			R_A (Ω)	R_S (Ω)	V_S	N_A PIN	R_A (Ω)	N_A PIN	N_G PIN
μA741	7.5	3.0	82K	2000	–	1	680k	1	5
LM101	10.0	3.0	2M	1M	–	5	1M	5	1
LM118	15.0	5.0	330k	180k	+	5	150k	5	1
LF155,6,7 (Note 1)	13.0	5.0	120k	5.1k	+	1	560k	1	5
HA2500 (Note 2)	14.0	10.0	6.8k	100	+	5	62k	5	1
HA2600	7.0	5.0	620k	18k	+	1	620k	1	5
CA3140	30.0 (Note 3)	4.5	1M	10k	–	5	240k	5	1
ICL8007	50.0 (Note 3)	5.0	100k	1.2k	–	5	150k	5	1
OP-05	1.6	3.0	1.6M	18k	+	8	2.4M	8	1
OP-07	0.25	3.0	10M	150k	+	8	10M	8	1

NOTES: 1. LF155, 156, 157 require 12k resistors from pin 1 and 5 to V^+, in addition to the resistors mentioned above.
2. ICL7650 supplies are ±8V max; HA2500 is not specified, but will work, with supplies under ±10V.
3. Unspecified; Value inferred from other data.



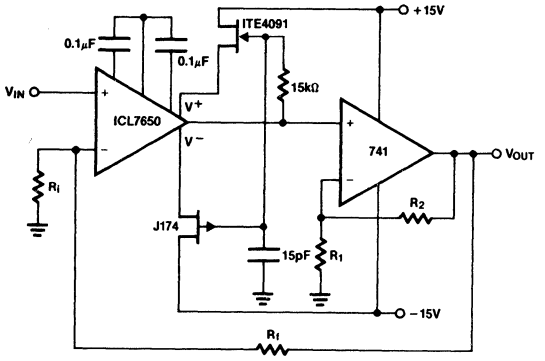
(a)

TC01880I



(b)

TC01970I



(c)

TC01890I

Figure 25: Several High Voltage-High Load Combination Circuits

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ACHIEVING THE FULL BENEFITS

The ICL7650 brings a new level of accuracy to the analog world, and in doing so exposes a new set of problems and difficulties in the environment of the typical op amp, previously masked by device errors. The standard care taken with ground loops is even more necessary here, and the prevention of PC board leakage is also more important. The pinout on the 14-pin device has been arranged so as to allow easy guarding of the input pins, and the same can be done on the TO-99 device by using a 10-pin outline mounting configuration, as shown in Figure 29. If the CLAMP pin is being used, the configurations of Figure 30 may be found more useful. Careful cleaning with TCE or alcohol, followed by a compressed air blow-dry, is advisable, and an epoxy or silicone rubber coating will prevent subsequent contamination. Careful use of Teflon® or similar standoffs may be helpful in stubborn cases of PC board troubles.

The impedances of the driving nodes for the offset null storage capacitors are quite high, as explained above, and care should be taken in the PC board layout to avoid coupling stray signals into these points. A pseudo guard ring tied to V^- could be applied in exceptionally difficult cases. The CAP RETN pin (14-pin parts only) is somewhat less sensitive, but should be treated with respect also.

Some consideration should be given to the capacitors themselves. On initial turn-on, and also if radical changes in common-mode or power supply voltages occur, the voltages on these capacitors must change to the (new) desired values. A capacitor with high dielectric absorption, such as a ceramic type, will absorb back part of the change in charge during the respective holding time during several clock cycles, or even for many seconds, leading to a significant initial (or recovery) settling time. If either of these is critical, a polypropylene capacitor should be used, although in many cases a mylar or similar film capacitor would be adequate. Another disadvantage of ceramic capacitors is that they frequently generate a significant amount of 1/f or "flicker" noise, which will be fed into the system through the null pins. For this reason, it is recommended that a film type capacitor be used, even though any low-leakage capacitor will "work".

The ultimate limitations to any high accuracy DC amplifier are the thermo-electric or Peltier effects in all the thermocouple junctions between dissimilar materials. The junctions of concern to us here are those between the silicon (n- or p-type) and the aluminum metallization on the die, the aluminum to bond-wire and bond-wire to header post or lead frame, and the post/lead to PC board junctions. If all these are at the same temperature, then no problems will arise, since an equal number of identical junctions are interposed on the return path. The power dissipation within the IC die is inherently low, and most applications will not add very much to that, so we can consider the die temperature to be fairly uniform. Thus, the thermocouples out to the bond-wires can be neglected unless a heavy load resistance is applied. The same is reasonably true for the bond-wire to post/lead junction. However, the post/lead to PC board junction can be a serious problem. The thermoelectric coefficient of the usual Kovar-copper junction present here is of the order of 30μV/°C, and the thermal contact between the individual junctions is not very good. A temperature gradient of as little as 0.1°C/inch will lead to an error as large as the typical offset voltage of the ICL7650! A point-source (power transistor, say) with a 10°C temperature rise must be kept 5 to 6 inches away, and a similar line-source would need to be many feet away. Even air currents from a standard forced-air heating system can cause gradients approaching this level. Similar effects can occur with other circuit elements, although generally their lead materials have lower thermo-electric coefficients.

The cure for these potential problems lies in exercising care in both the circuit design and the board layout. The power dissipation in the ICL7650 should be kept low (use the circuits of Figures 24–26 for load driving if needed), and power-dissipating components should be kept well away. A cooling fan or blower is undesirable unless an enclosure is used around the op amp and its associated components, and in any case the air flow should not pass over this area after a power-dissipating area. Low thermo-electric coefficient connections should be used wherever possible, and in all cases the PC board layout should emphasize thermal balance in loop paths.

An example of care in the electrical and thermal layout of a board, and appropriate choice of components to complement the performance of the ICL7650 may be found in the ICL7650EV/Kit, an evaluation kit that includes a test board which can be used to measure most of the critical parameters of the device, and to simulate various possible applications. The kit includes all the necessary passive and active components to build the circuits of Figures 23–25 also, so that they may be substituted for another device in an operating system for checkout.

SUMMARY

The ICL7650 represents a significant step-function in op amp performance (one that should not have occurred until 1990, according to one recent Wescon presentation). The design brings chopper-stabilized performance to a new level of availability, while making it virtually transparent to the user. Although it is too early to predict the demise of the trimming potentiometer industry, nevertheless this device and its successors can be expected to replace the need for many of them and their periodic re-adjustment, frequently without increasing the initial cost, and certainly with favorable lifetime cost benefits. The combination circuits suggested here allow an even closer approach to the "perfect op amp" than has ever been available before, and at remarkably low cost.

One side-effect of the remarkable performance potential of the ICL7650 is that several subtle error-causing effects that have previously been largely masked by the inherent errors of the available op amps, are now uncovered. Great care must be exercised to achieve the full performance benefits the device can offer. These caveats do not, of course, apply in cases where a simple replacement of a less accurate or less stable device is contemplated. The high degree of "user-transparency" achieved in the chopping operation promises a minimum of applications problems, borne out by the rapid acceptance of the device in a wide range of applications.

The author would like to acknowledge the design efforts of Lee Evans and Dane Snow in turning the concept of the device into such a magnificent reality, and Andy Wolff for refining, expanding, and testing many of the circuit applica-

tion ideas presented here. An additional acknowledgement should go to Bob Darling of Rutgers University for the basic concept of Figure 23. A list of relevant application notes and article reprints that may be found helpful in pursuing the ideas opened up in this one follows:

A007 "Using the ICL8048/8049 Monolithic Log-Antilog Amplifier", by Ray Hendry.

A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing", by Ed Sliger.

R017 "CMOS Chopper Op Amp Does Away with Glitches", by Peter Bradshaw, *Electronic Design,* August 2, 1980.

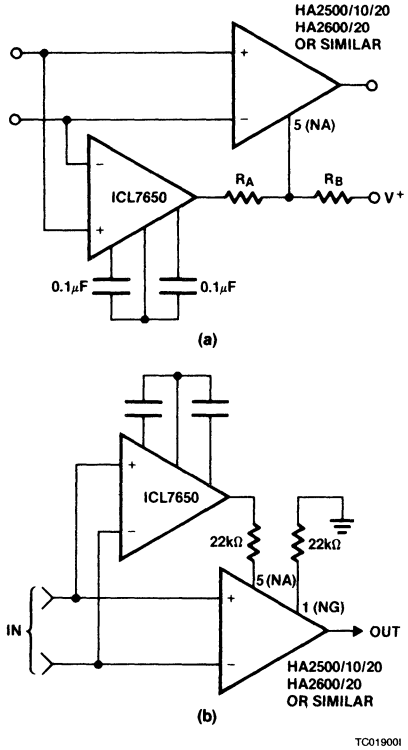

Figure 26: HA2500 or 2600 Offset Nulled by ICL7650

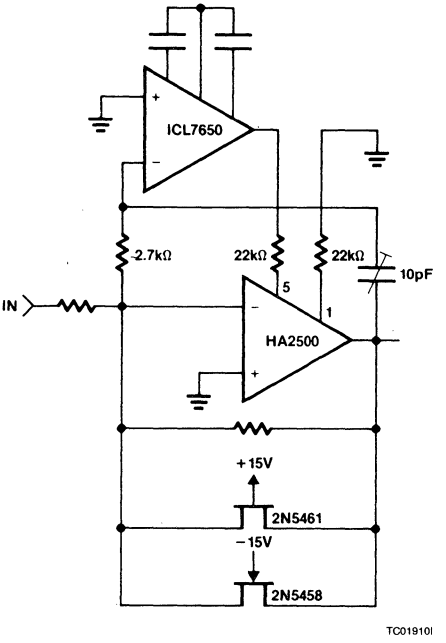

Figure 27: Nulled HA2500 with Dynamic Correction and Overload Clamp

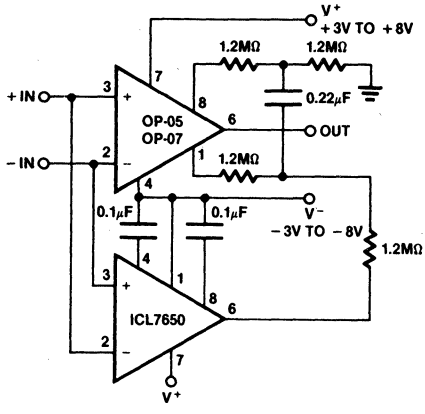

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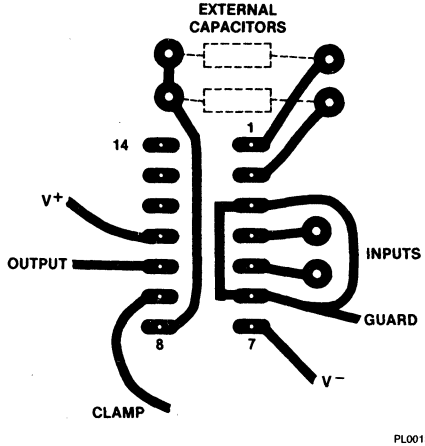
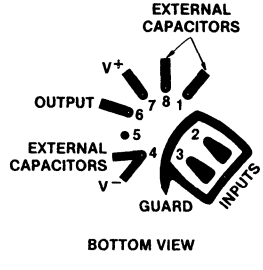
Figure 28: Auto-Nulling Circuit for OP-05/OP-07



PL00131I

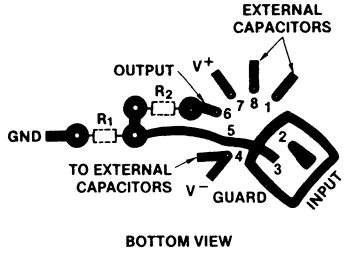


BOTTOM VIEW

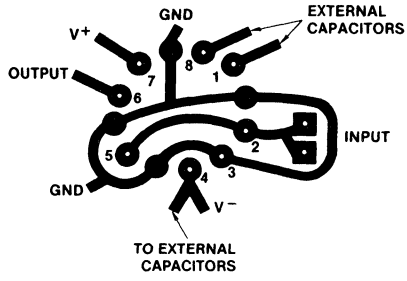
PL00140I

(a) 14-Pin Part **(b) TO-99 Package**

Figure 29: Board Layouts for Input Guarding



(a) Non-Inverting Amplifier with Clamp



(b) Inverting Amplifier with Clamp

Figure 30: Input Guarding with Clamp Pin

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R017
CMOS Chopper Op Amp Does Away With Glitches

Low-cost monolithic chopper-stabilized op amp with differential input compensates for intermodulation and holds input offset voltage errors to 1 μV over its full operating temperature range.

Most data-acquisition systems require operational amplifiers that provide enough inherent dc stability to eliminate tweaking with trimming potentiometers. Conventional op amps that have input offset voltages in the millivolt range approach this requirement, but they still need periodic adjustments. A new monolithic chopper-stabilized op amp, the ICL7650, achieves tweakless performance with a typical input offset voltage of 1μV or less over its full operating temperature range — and the device sells for only $2.75 in 100-unit quantities.

Fabricated with CMOS technology, the ICL7650 is virtually devoid of the glitches that plague older chopper-stabilized designs, which are derived from vacuum-tube equivalents (see "The Traditional Chopper — and Its Problems"). The ICL7650 depends on just two noncritical external capacitors, rather than on the two low-pass filters, one high-pass filter, and demodulator essential to popular choppers.

Designed for monolithic construction, the ICL7650 circuit (Figure 1a) consists of a main dc amplifier, a nulling dc amplifier, an output clamp, a compensation circuit that minimizes the intermodulation between applied signals and the chopping frequency, and switches controlled by a two-phase oscillator. These switches are actuated on alternate half-cycles of the chopping frequency.

HOW THE CHOPPER WORKS

A novel chopper-switching arrangement ensures virtually glitchless output. During one clock half-cycle of the oscillator, the A switches close and the B switches open, driving the nulling amplifier to a null (Figure 1b). A fraction of the voltage on capacitor C_1 is then added algebraically to the input of the nulling amplifier, so as to null the input-voltage offset error of this amplifier.

In the other clock half-cycle of the oscillator, the B switches close and the A switches open, driving the main amplifier to a null (Figure 1c). During this clock interval, capacitor C_1 holds the nulling amplifier in its nulled state, while the main amplifier is being nulled. Capacitor C_2 maintains the main amplifier in its nulled state. The null sequence continually repeats, to produce a very low offset voltage.

The ICL7650 minimizes intermodulation effect by generating a compensating dynamic offset in the nulling amplifier when the B switches are closed. Therefore, the nulling amplifier does not see the main-amplifier input signal as an offset error. Although the correction is not total, the intermodulation terms are reduced to such a low level that the ac and dynamic signals scarcely disturb the nulling system. The results are minimum phase error and a clean gain-frequency curve.

A very effective approach prevents input overloads — a clamp in the feedback network reduces the closed-loop gain of the main amplifier just before the circuit reaches its maximum output level. The clamp consists of a pair of low-leakage n and p-channel MOSFETs that turn on shortly before the output limits. The clamp network is brought out to an external pin. Tying this pin to the chip's inverting input implements the clamping automatically. The clamping action does not disturb the null network and has negligible effect on the device's input bias current in the active region.

Besides providing a virtually glitch-free output and very fast recovery from overloads, the ICL7650 offers differential inputs, a maximum phase error of 10 degrees, a gain-bandwidth product of 2MHz, and a low 100-piece price of $2.75. Furthermore, because the chip is CMOS, its power dissipation is low, with a typical no-load supply current of less than 2mA. Another advantage of CMOS is that the op amp operates from a single 5-V supply, so it is compatible with standard TTL systems. It can also operate with bipolar supplies up to ±8V. In either case, the input common-mode range includes the negative supply.

The ICL7650 comes in a choice of two packages and two temperature grades — a 14-pin plastic DIP for operation from 0 to 70°C, a 14-pin ceramic DIP for −25 to +85°C, and an 8-pin TO-99 metal can for operation over either temperature range. No matter the package, the device is internally compensated for unity-gain operation.

The 8-pin version is pin-compatible with standard op amps, except for the pull-system capacitors. The 14-pin version provides for an optional external oscillator. The duty cycle for the external oscillator is not critical, because an internal divide-by-two circuit ensures a 50% duty cycle.

Optimum values for the two external capacitors, C_1 and C_2 depend on the chopping frequency. For the preset 100Hz of the internal oscillator, the best value is 0.1μF. When an external oscillator is used, this value should change proportionately to maintain the relationship between the chopping frequency and the nulling time constant. A high-quality film capacitor (for example, mylar) is preferable, although a ceramic or other lower-grade type may be suitable in many applications.

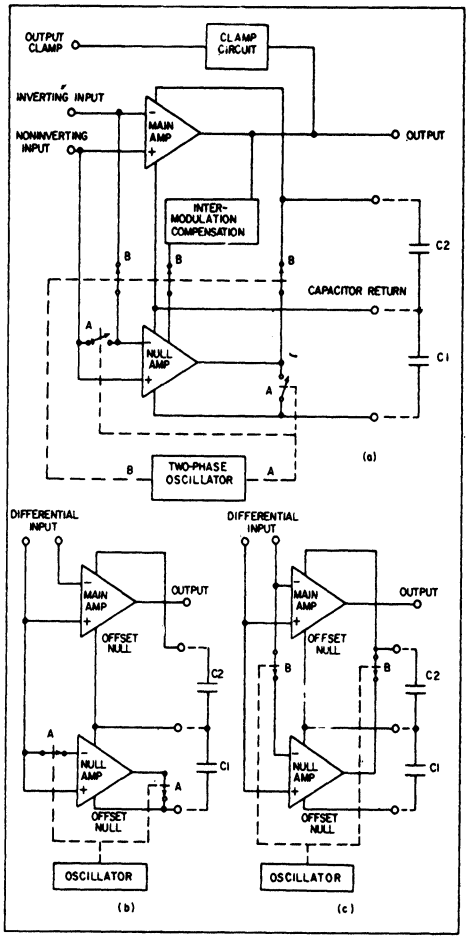

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Figure 1: The ICL7650 monolithic chopper op amp virtually eliminates output glitches. Besides a differential input, the CMOS chip (a) offers intermodulation compensation and an output clamp circuit. Priced at just $2.75, it holds input offset voltage to 1μV over temperature by nulling its nulling amplifier (b) and then the main amplifier (c).

PUTTING THE CHIP TO WORK

Any application where system performance can be significantly improved by a reduction in input offset voltage and bias current is right for the ICL7650.

Figure 2a shows the basic configuration for a noninverting amplifier with the clamp circuit connected; Figure 2b shows the inverting configuration, also with the clamp connected. For applications that require output swings greater than ±7.5V, the booster circuit of Figure 2c can be used.

In Figure 2d, the clamp circuit works to advantage in a zero-offset comparator. Here, the problems that usually prevent the selection of a chopper-stabilized amplifier are avoided, because the inverting input of the ICL7650 follows the input signal. The comparator's threshold input must tolerate the output-clamp current without disturbing other portions of the circuit.

The circuit of Figure 2e illustrates a logarithmic amplifier that has wide dynamic range. Because it avoids the limitations resulting from excessive input offset voltage, it can achieve about six decades of dynamic range in the voltage-input mode. Logarithmic amplifiers built with other devices usually have only a three-decade dynamic range.

The ICL7650 can also provide offset nulling for other amplifiers, such as the ICL8048. This monolithic temperature-compensated logarithmic amplifier can handle six decades of current input or three decades of voltage input. The nulling circuit (Figure 3a) adds three more decades of voltage range. The same concept may be applied to the HA2500 and HA2600 families of monolithic op amps to obtain very low offset and capitalize on the high slew rate and broad bandwidth of these devices (Figure 3b). Such circuits enchance performance factors like dc gain, common-mode rejection ratio, and power-supply rejection ratio.

THE TRADITIONAL CHOPPER — AND ITS PROBLEMS

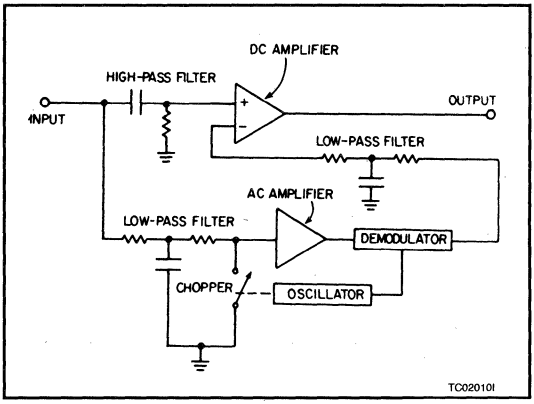
The most common configuration for a solid-state chopper-stabilized operational amplifier is actually based on a vacuum-tube circuit that employed electromechanical choppers. Although the solid-state version shows excellent drift characteristics, chopper-switching glitches often appear in the output.

The circuit has two amplifiers — a dc amplifier and an ac amplifier. High-pass and low-pass filters separate the input signal into its high and low-frequency components. The high-frequency component is applied to the main dc amplifier, and the low-frequency component is first chopped by an oscillator-controlled switch and then applied to the ac amplifier. After demodulation, the output of the ac amplifier passes through another low-pass filter before being applied to the noninverting input of the main dc amplifier.

A chopper configuration of this type reduces the offset and drift errors of the dc amplifier by a factor equal to the gain of the ac amplifier. However, the circuit does have several shortcomings. It can handle only single-ended inputs; it produces relatively high-phase error because of intermodulation at frequencies near the chopping frequency; it recovers slowly from overloads; its output has glitches associated with chopper switching; its gain-bandwidth product is below 1MHz; and its cost is relatively high.

The high phase error stems from the finite gain of the main amplifier near the chopping frequency. Even in the absence of an offset voltage, this amplifier develops a small differential input signal. The frequency of the differential input signal corresponds to the input frequency. Internal correction circuitry detects this signal and attempts to null it out. If the signal and chopping frequencies are well separated, successive nulling attempts will be weak, or will even cancel each other. However, if the two frequencies are close, the nulling circuit will generate significant beat-frequency terms. As a result, the intermodulation causes excessive phase error, as well as wrinkles in the circuit's gain-frequency curve.

Overload conditions present yet another problem. The feedback network has trouble coping with input signals when the amplifier output hits one power-supply rail or the other. Unless the offset null network recognizes the situation, the overload will be treated as an offset error, and the nulling amplifier will attempt to correct it. Since this attempt is bound to fail, the nulling network will be substantially offset. When the input signal returns to what should be the active region, the false null causes a maximum error, and recovery to a normal condition is very slow. This problem can be controlled if the nulling process is inhibited when the output approaches either supply rail, but leakages in the null network eventually compromise this solution.



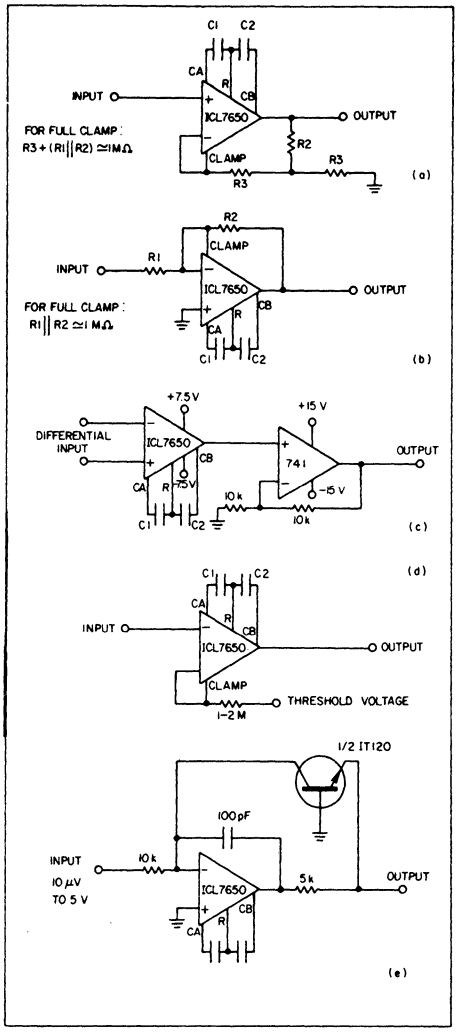


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Figure 2: The ICL7650 chopper op amp is a versatile circuit building block. It can function as either a noninverting (a) or an inverting (b) amplifier; its output can be boosted for swings of more than ±7.5V (c); and it can be employed as a zero-offset comparator (d) or even as a logarithmic amplifier (e) with a six-decade range.

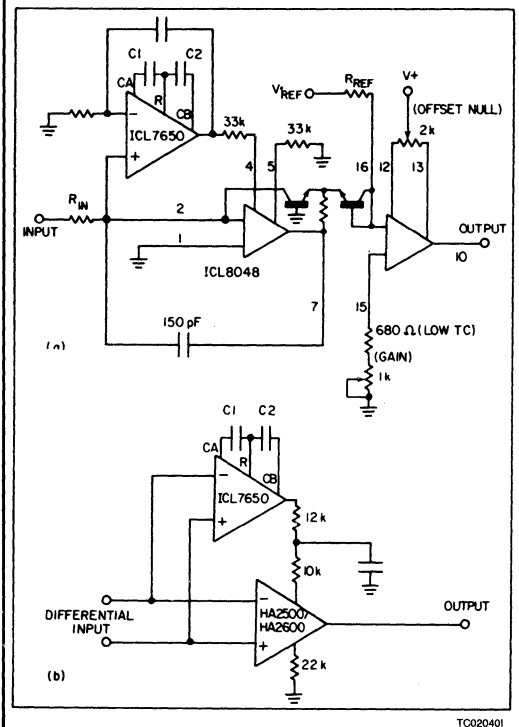

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Figure 3: The new chip enchances the performance of other amplifiers — for example, nulling the offset for an 8048 log amp (a) or for the 2500/2600 families of op amps (b).

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With the ICL7650, the standard three-op-amp configuration for an instrumentation amplifier (Figure 4a) yields excellent performance, because of the extremely good common-mode rejection ratio of the chip's front end. In the strain-gauge preamplifier of Figure 4b, two of the monolithic chopper op amps maintain high differential gain without any common-mode gain. This preamp mates with analog-to-digital converters that have differential-input front ends.

Thermocouples that are grounded on one side could use the single noninverting amplifier of Figure 2a. However, if a shielded thermocouple with a ground at the sensing end is used in a high-noise environment, the circuit of Figure 4b is preferable. With an absolute platinum-platinum-rhodium (type S) thermocouple, the very low offset and drift errors of the ICL7650 contribute less than 1°C initial error and less than 0.2°C drift error between temperatures of 0 and 1750°C.

The full benefit of the ICL7650's performance can only be realized when care is taken to minimize the introduction of spurious thermocouple voltages between the printed-circuit board, connectors, device sockets, and component leads. Moreover, heat sources must be well removed from critical portions of the circuit, and cooling air should not pass over this critical circuitry after the air has been used or

even beforehand, if possible. Even radiated heat can cause problems.□

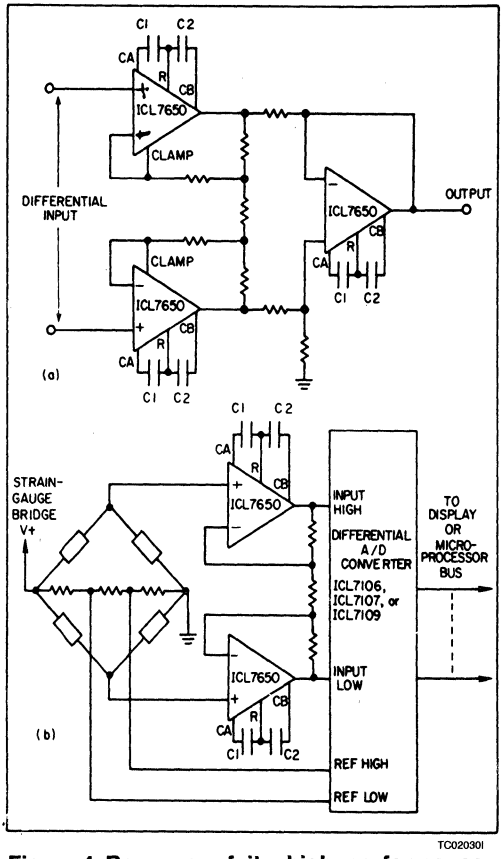

Figure 4: Because of its high performance, the ICL7650 has numerous applications — as an instrumentation amplifier (a) with a standard three-op-amp configuration and as a strain-gauge preamplifier (b) for an A/D converter.

AO26
D.C. Servo Motor Systems Using the ICH8510

By Ken McAllistar

INTRODUCTION

Intersil has developed a family of hybrid power operational amplifiers — the ICH8510 family — designed specifically for driving D.C. servo motors, D.C. linear and rotary actuators, electronic orifice valves and X-Y printer motors. There are three members of this family, the ICH8510, 8520 and 8530, capable of delivering 1 amp, 2 amps and 2.7 amps respectively, while operating at supply voltages up to ±35V.

The amplifiers operate in the linear mode and can be treated as high power (and higher voltage) versions of a μA 741 operational amplifier. The ICH8510 can typically swing ±26V across a 20Ω load and the 8520, 8530 versions can typically swing ±26V across a 10Ω load with supplies of ±30V. The typical quiescent current under no load conditions is ±20mA while input offset voltage, input bias current, slew rate, open loop voltage gain and input voltage range are the same as the basic 741 differential, operational amplifier. All the amplifiers are short circuit proof, being able to withstand indefinite shorts to ground at the output and also have unique safe area operating protection. This safe area protection allows the amplifier to handle the large inductive emf's caused by D.C. motors during reversal or load changes without damage, but does not hinder normal operation of the amplifier.

The open loop configuration of the ICH8510 family makes them very versatile for closed loop servo motor systems. Either positive or negative gains may be obtained using well known operational amplifier techniques. The ease with which the ICH8510 amplifier family can be implemented, relieves system designers of the headaches of excessive quiescent power supply currents, and inadequate amplifier stability. The power amplifiers are internally compensated and are available in an eight pin TO-3 package. They are unconditionally stable down to unity gain, non-inverting (the worst case).

SERVO SYSTEMS

BACKGROUND

Figure 1 shows the ICH8510 in an "open loop" control system, meaning that the motor is not within the closed loop of the amplifier and the associated feedback components. Figure 2 and 3 show the ICH8510 in typical open loop system applications.

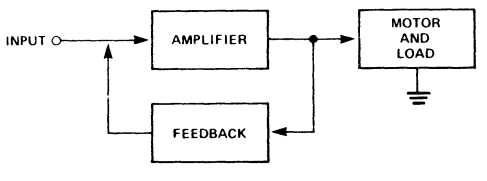

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Figure 1: Open Loop Control System

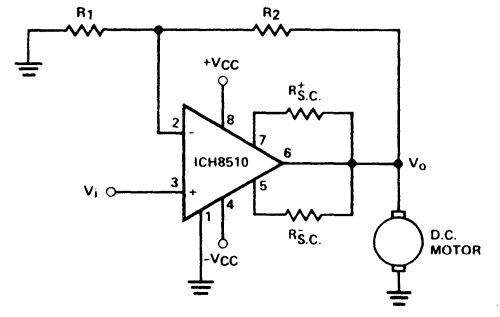

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Figure 2: Non-Inverting Gain Configuration

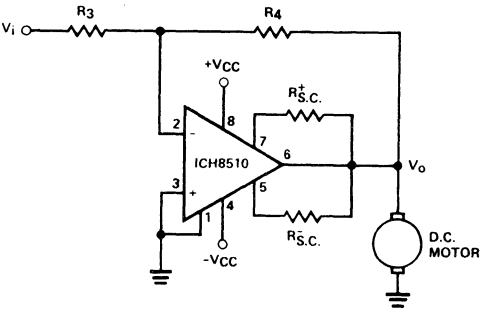

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Figure 3: Inverting Gain Configuration

Figure 2 shows the ICH8510 in the standard non-inverting operational amplifier configuration where the voltage gain

$$A_V = \frac{V_o}{V_i} = \frac{R_2 + R_1}{R_1} = 1 + \frac{R_2}{R_1}.$$

In Figure 3 the power amplifier is shown in the standard inverting gain configuration where the voltage gain

$$A_V = \frac{V_o}{V_i} = -\frac{R_4}{R_3}.$$

The resistors denoted $R^{+}_{S.C.}$ and $R^{-}_{S.C.}$ determine the current which will flow under output short circuit conditions from the output to ground. Such short circuits could come about as a result of a stalled motor where the only load resistance is the winding of the motor.

In an open-loop system any changes in the input, load or amplifier characteristics will cause corresponding changes in the output. In order to minimize those output deviations a

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closed loop system is normally used. With a closed loop system a portion of the system output is fed back to the input and summed with the input. Now the motor is actually part of the feedback network and variations which would occur in the open-loop system are divided by the feedback ratio.

Servo systems control basically three quantities or any combination of the following three quantities:

1. Motor velocity
2. Motor position (i.e., shaft rotational position)
3. Motor torque

A block diagram of a typical closed loop control system is shown in Figure 4.

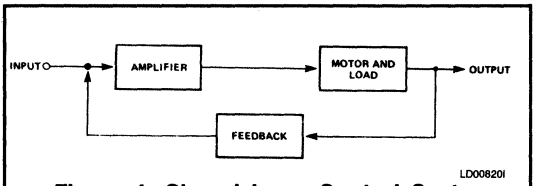

Figure 4: Closed Loop Control System

VELOCITY CONTROL

The purpose of a closed loop velocity control system is to maintain a constant velocity independent of load variations. Velocity control is accomplished by means of tachometer feedback as shown in Figure 5.

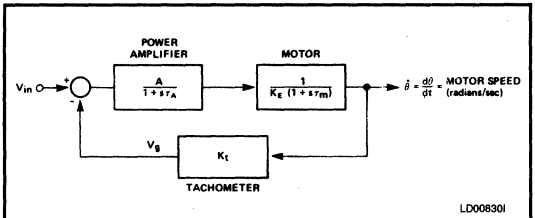

Figure 5: Velocity Control System

Where:

A = D.C. gain of amplifier

τ_A = dominant pole of amplifier

K_E = voltage constant of motor

τ_m = dominant pole of motor

K_t = tachometer constant

The model of the velocity control system shown in Figure 5, while not being an exact representation of the real system, allows the transfer function of the closed loop system to be determined. The transfer function is given by:

$$\frac{\theta}{V_{in}} = \frac{\frac{d\theta}{dt}\left(\frac{1}{1+S\tau_A}\right)\left(\frac{1}{K_E(1+S\tau_m)}\right)}{1+K_t\left(\frac{A}{1+S\tau_A}\right)\left(\frac{1}{K_E(1+S\tau_m)}\right)} \quad (1)$$

This form allows variations of the system parameters to be related back to the variable of most interest, which is the motor rotational speed or ω. A root locus of (1), may be drawn to determine overall stability with variations in the systems parameters.

The actual circuit implementation is presented in Figure 6 where the ICH8510 is used as both the driving amplifier and the summing amplifier.

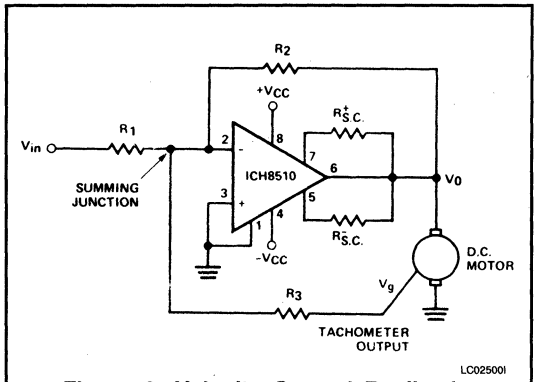

Figure 6: Velocity Control Realization

The output voltage of the amplifier is given by the following equation:

$$V_o = -\frac{R_2}{R_1}V_{in} + \left(-\frac{R_2}{R_3}\right)V_g. \quad (2)$$

The operation of the velocity control system can be understood from the following: if the speed of the motor tends to increase for whatever reason (i.e., less load friction), a larger voltage is induced in the windings of the tachometer. This voltage is fed back to the summing junction and opposes the input voltage which forces the output voltage down tending to keep the speed constant.

For some applications it may be desirable to monitor the rev/sec or rev/min of the motor shaft. This can be done very easily by using Intersil's ICL7106 or 7107, which are single chip 3-½ digit A/D Converters, and a simple scaling network connected to the tachometer output. By knowing the volts/r.p.m. rating of the tachometer, a simple resistor divider network can be constructed to scale the tachometer output voltage so the input of the A/D Converter will indicate motor speed directly. Here is an example:

$$\frac{\text{Tachometer Output}}{\text{Tachometer Constant}} = \frac{12V}{3V/1000\ \text{r.p.m.}} = 4000\ \text{r.p.m.}$$

The output of the A/D should indicate 4.00 Kr.p.m. The output voltage of the tachometer is scaled down as in Figure 7. Since the optimum full scale input voltage of the 7106 or 7107 is 200mV the reading of 4.00 Kr.p.m. should be scaled to correspond to 40mV at the input of the converter. The decimal point may be shifted so that the display, which the converter drives, will read 4.00.

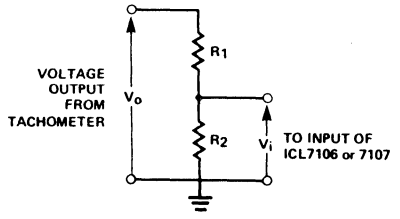

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Figure 7: Divider Network for A/D Converter Input

Now,

$$V_o = 12V \text{ and } V_i = 40mV$$

so R_1 and R_2 are determined by

$$V_i = \frac{R_2}{R_1 + R_2} V_o.$$

This equation cannot be solved by itself but by using the minimum load resistance of the tachometer as the second equation yields $R_1 + R_2 = Z_{Lmin}$. Using 10KΩ for $R_1 + R_2$, the value of R_2 is 34Ω and R_1 = 9.96KΩ.

POSITION CONTROL

The purpose of a closed loop position control system is fast and accurate control of the rotational position of the motor shaft. The position control may be random position changes or may occur at equal intervals of time with the position changes also being of equal distance. Rotational position is given the notation of θ, which signifies the angle deviation from a set reference angle. θ is equal to the integral of the angular velocity. The block diagram of a position control system is shown in Figure 8.

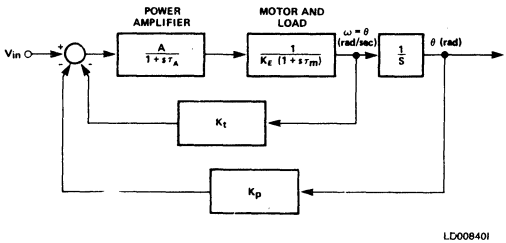

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Figure 8: Position Control System

The only parameters in Figure 8 that differ from the velocity control system in Figure 5 are:

K_p = integrator constant

$1/S$ = the integrator transfer function

From Figure 8 the transfer function of the position control system may be written and is equal to:

$$\frac{\theta}{V_{in}} = \frac{\frac{1}{S}\left(\frac{A}{1+S\tau_A}\right)\left[\frac{1}{K_E\,(1+S\tau_m)}\right]}{1 + \frac{K_t K_p}{S}\left(\frac{A}{1+S\tau_A}\right)\left[\frac{1}{K_E\,(1+S\tau_m)}\right]} \quad (3)$$

Here again the form of the transfer function given by (3) allows the effects of variations in system parameters to be determined.

While the block diagram at first glance seems a bit formidable, the functions of the integrator and integrator constant are both performed by a simple potentiometer coupled to the motor shaft. The equivalent circuit of the coupled pot is shown in Figure 9.

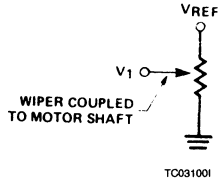

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Figure 9: Position Control Potentiometer

As the motor shaft turns, the wiper voltage varies from zero volts at the 0° reference point to V_{REF}. This output voltage then varies as $\frac{d\theta}{dta}$ which is the rotational speed of the motor; and this voltage is $\frac{dV_1}{d\theta}$. Referring to Figure 10 helps clarify this point.

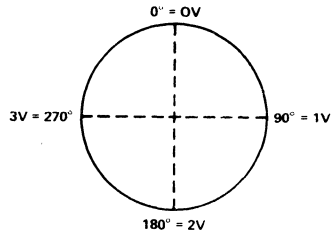

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Figure 10: Relationship Between Angular Position and Pot Wiper Voltage

For the conditions in Figure 10 a reference voltage, V_{REF} = 4V and a scaling factor of 1V/90° exists.

A complete position control system is shown in Figure 11.

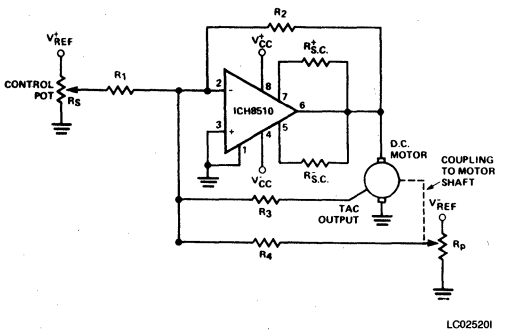

Figure 11: Practical Position Control System

The circuit of Figure 11 operates as follows: When the control pot is turned to a new position the motor begins turning until the voltage at the wiper of the motor pot produces a voltage which causes the output voltage to reach zero and the motor stops. At this point, the two voltages produced by the gains from the control pot and from the motor pot produce equal and opposite voltages at the output of the ICH8510 and this causes the motor to stop. If the load on the motor tries to turn the shaft to another position a voltage is produced which opposes the change in position and forces it to remain in the preset position. The control pot should be a 10 turn pot in order to obtain very accurate position control and may be calibrated to indicate angular position or linear position of the load.

TORQUE CONTROL

A torque control system is used whenever a motor is required to provide constant torque to a load. The torque of a D.C. motor is directly proportional to the motor current, the only difference being the torque constant of the motor. The relationship between the torque and motor current is given by the following relationship:

$$T = K_T I \qquad (4)$$

Where:

K_T = torque constant

T = motor torque

I = motor current

From (4) it can be seen that if constant current is delivered to the motor the motor will deliver constant torque.

The constant load current situation may be realized by placing the motor inside the feedback loop of the amplifier as shown in Figure 12.

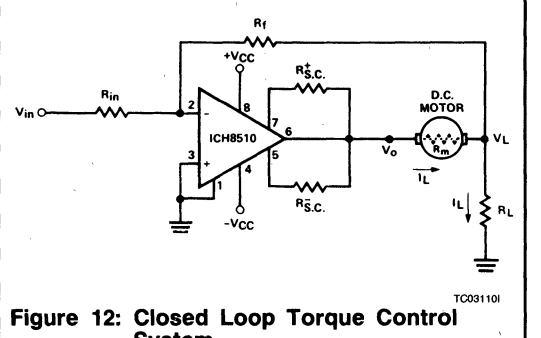

Figure 12: Closed Loop Torque Control System

The transfer function of the torque control system in Figure 12 is given by:

$$\frac{I_L}{V_{in}} = -\frac{R_f}{R_{in}} \cdot \frac{1}{R_L} \qquad (5)$$

assuming $R_f >> R_L$. By choosing appropriate values for R_f, R_{in} and R_L, a transconductance giving so many amps of load current for a given input voltage is realized. For example, if $R_{in} = R_f = 1K\Omega$ and $R_L = 10\Omega$,

$$\frac{I_L}{V_{in}} = -\frac{1 \times 10^3}{1 \times 10^3} \cdot \frac{1}{10} = -10^{-1} A/Volt.$$

The operation of the torque control system can be understood from basic operational amplifier theory. For a constant input voltage designated V_{in}, the current through R_{in} is $\frac{V_{in}}{R_{in}} = I_{in}$ and the current through the feedback resistor R_f is given by $\frac{V_L}{R_f} = I_f$; both of these under the assumption that the inverting input is a virtual ground. These two currents will be equal to one another assuming the input bias current is negligible, which results in a constant output voltage. With a constant load R_L the current through the load resistor and also the motor will be constant. This means under stall conditions, the amplifier delivers the same current as when in the unstalled mode. In effect, the stalled current of, say, Figures 2 or 3 will approach maximum output current of the amplifier. This difference is quite significant, i.e., a 1 amp at 24V motor during normal unstalled conditions becomes a 2–3 amp motor (this maximum limit is set by externally programmable R^+_{SC} and R^-_{SC} resistors) for stalled conditions. The Figure 12 circuit would keep the 1 amp drive current constant whether the motor was stalled or not.

REFERENCES

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2. Speed Controls, Servo-Systems, Electro-Craft Corporation, Hopkins, Minnesota, 1972
3. A021, *Power D/A Converters Using the ICH8510,* May, 1977
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A007
Using The 8048/8049 Log/Antilog Amplifier

GENERAL DESCRIPTION

A common problem in instrumentation and data transmission is the processing of signals over a wide dynamic range. The ICL8048 is designed to provide the solution.

The 8048 is a complete DC logarithmic amplifier, consisting of two FET input op amps and utilizing the fundamental logarithmic properties of a transistor junction. It will handle six decades of input current or three decades of voltage input, is temperature compensated from 0°C to 70°C, and features adjustable scale factor, reference current and offset voltage.

The 8049 is the anti-log counterpart of the 8048 and is designed to supply one full decade of output voltage for each 1 volt change at the input. And like the 8048, the reference current scale factor and offset voltage are externally adjustable.

THEORY OF OPERATION (Figure 1)

The logarithmic gain of the 8048 is derived from the inherent exponential characteristics of a transistor junction. Transistor Q_1 is used as the non-linear feedback element around op amp A_1 which has a FET-input stage to provide low input current noise and very low input bias current. Negative feedback is applied to the emitter of Q_1 through R_4. This forces the collector current of Q_1 to be exactly equal to the current through the input resistor R_1. The collector current for Q_2 is set by R_2 and the reference voltage, and since the collector current of Q_2 remains constant, the emitter base voltage also remains constant. Therefore, only the emitter base voltage of Q_1 varies with a change of input current. However, the output voltage is a function of the difference in emitter-base voltages of Q_1 and Q_2.

$$V_o = \frac{R_5 + R_3}{R_3} (V_{BE1} - V_{BE2}) \quad (1)$$

For matched transistors operating at different collector currents, the emitter base differential is given by

$$\Delta V_{BE} = \frac{kt}{q} \ln \frac{I_{C1}}{I_{C2}} \quad (2)$$

Combining Equation 1 and 2 and writing the expression for the output voltage gives

$$V_o = \frac{R_5 + R_3}{R_3} \left(\frac{kt}{q}\right) \ln \frac{I_{C1}}{I_{C2}} \quad (3)$$

This shows that the output is proportional to the logarithm of the input current, and hence voltage. The temperature dependence is minimized by control of the temperature coefficient of R_5.

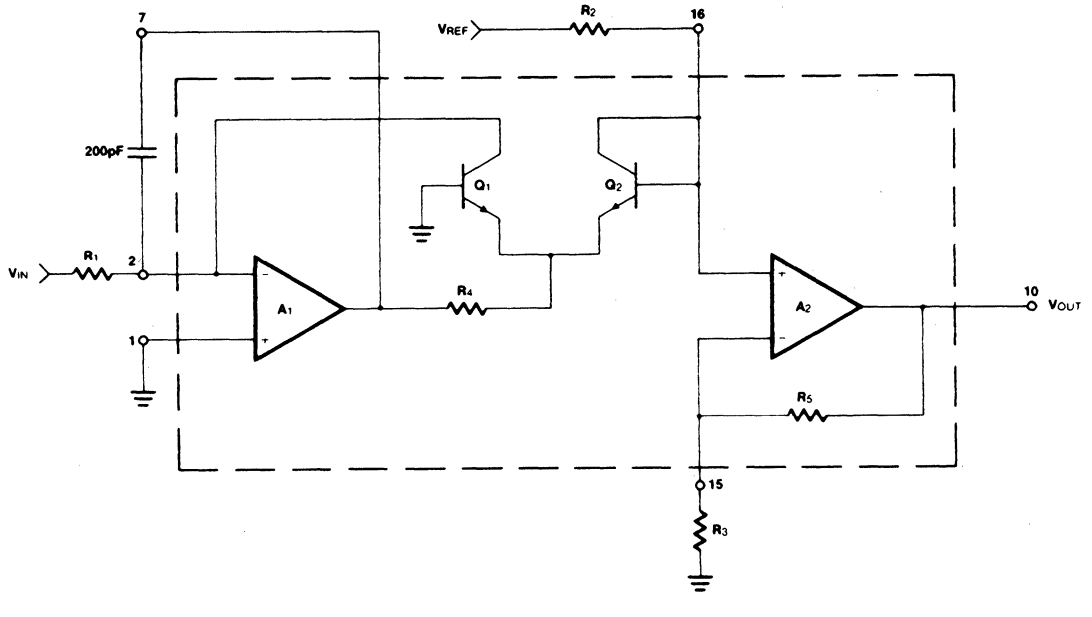

Figure 1: 8048 A Complete Monolithic Log Amp

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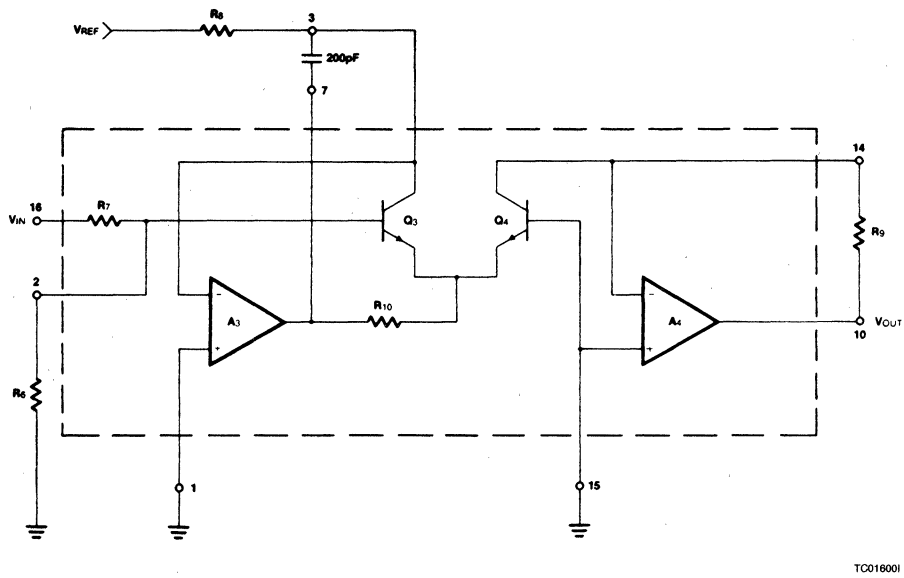

Figure 2: ICL8049 A Complete Monolithic Antilog Amp

The basic schematic of the 8049 is shown in Figure 2. A_3 forces Q_3 to operate at I_{REF}, shifting down the emitter voltage of Q_4 by the voltage applied to pin 2. The division ratio is controlled by R_6 and R_7, thus the V_{BE} of Q_4 will force a collector current given by:

$$I_{OUT} = I_{C(Q4)} = (I_{REF})^{a}\ V_{IN},\ \text{where}\ a = \frac{-qR_6}{kT(R_6 + R_7)},$$

therefore giving the desired antilog dependence.

A_4, together with R_9, acts as a current to voltage converter:

$$V_{OUT} = R_9(I_{REF})\ \text{antilog}\ (a\ V_{IN})$$

Again the temperature coefficient or R_7 corrects for the temperature dependence of a.

SOURCES OF ERROR

Log Conformity Error: Log conformity error is the difference between actual output voltage and the output voltage predicted by the log transfer equation. A plot of input versus output should be a straight line (when plotted on semilog paper), with a slope kT/q(60mV/decade). Any deviation from this straight line is log conformity error.

Offset Voltage (V_{OS}): The offset voltage of the internal FET amplifier. This voltage appears as a small DC voltage in series with the input terminals. For current logging applications, its error contribution is negligible, however for log voltage applications, best performance is obtained by nulling V_{OS}.

Reference Current (I_{REF}): I_{REF} is the current generated by R_2 and V_{REF} (Figure 1) to which all input currents are compared. I_{REF} tolerance errors appear as a DC offset at the output; a ±1% I_{REF} error, referred to the input, corresponds to a DC offset of ±4.3mV at the output. This offset is independent of input signal.

When a resistor is used to generate I_{REF}, as shown in Figure 1, pin 16 is not a true virtual ground. For the 8048, a fraction of the output voltage is seen on pin 16. This does not constitute an appreciable error, provided V_{REF} is much greater than this voltage; a 10V or 15V reference satisfies this condition. Alternatively, I_{REF} can be provided from a true current source. (See Figure 3)

Bandwidth: The gain bandwidth product of the logging element is relatively constant, and a change in gain will vary the bandwidth. Gain changes occur when input current to the logging elements varies with signal level. Consequently, slew rate and frequency response are specified as a function of input signal level and will vary accordingly.

It should be noted that zero collector current in the logging element for zero signal current is not the preferred condition, particularly if the input terminal is to be multiplexed and a rapid rise to the end value of output voltage is important. The rise time, in decades of collector current per second, is approximately proportional to collector current; accordingly, if the collector current had to start up from zero, the rise to the output voltage would take an undue length of time. This can be prevented by injecting a collector rest current equal to 1% of the lowest current to be measured.

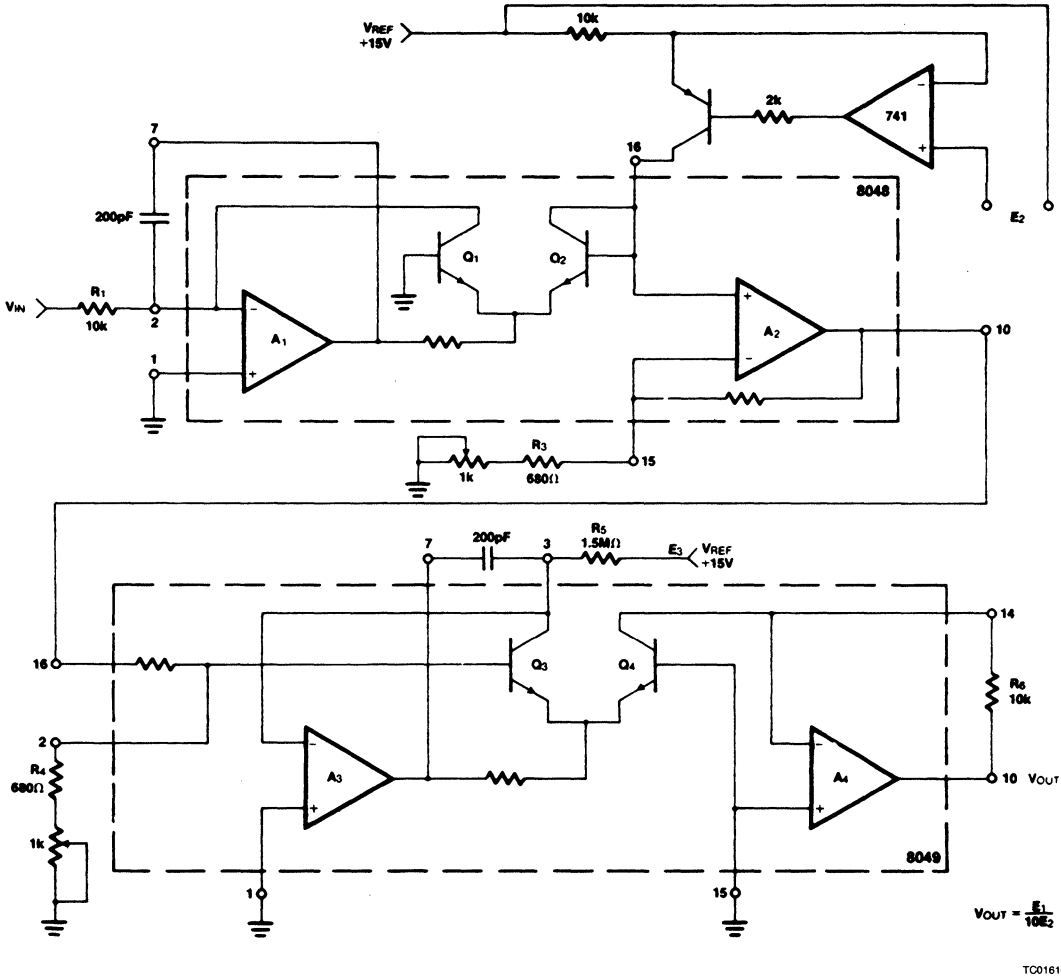

Figure 3: Complete One Quadrant Divider Using an 8048 Log Amp and an 8049 Antilog Amp

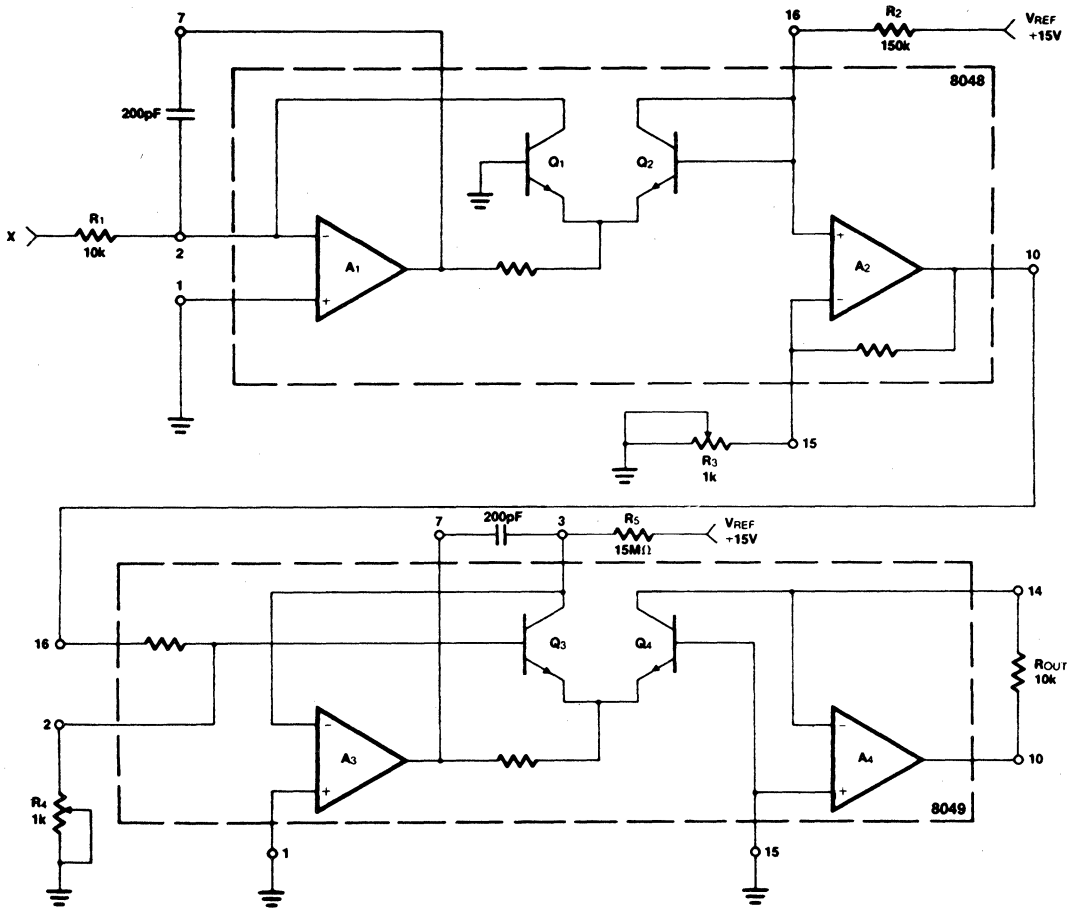

Figure 4: Circuit for Computing Exponential Functions

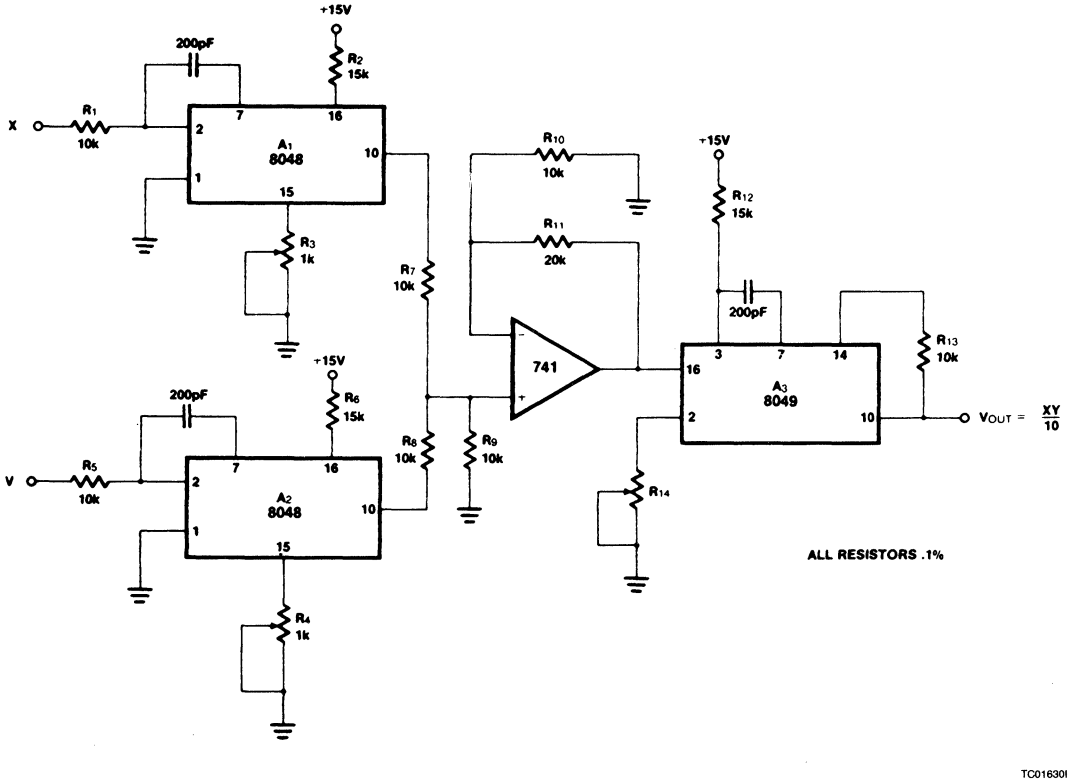

Figure 5: Multiplier

ONE QUADRANT DIVIDER

Computing the ratio of two analog voltages can be done with general-purpose analog multipliers, but the accuracy decreases if the denominator varies over a wide range. With log-amps, a one-quadrant divider with a better full-scale accuracy over a dynamic range of 100:1 can be designed, and with the flexibility of external adjustments, the scale factors are readily adjustable and the circuit can easily be optimized for other ranges.

The circuit in Figure 1 may be used as divider or reciprocal generator. The output of the 8048 is actually the ratio of the input current and the reference current through R_2, when used as a log generator, the reference current is held constant by connecting R_2 to a fixed voltage. If R_2 is driven by an input voltage, rather than the 15V reference, the output of the 8048 is the log ratio of the input current to the current through R_2. The antilog of this output voltage is the ratio of the inputs.

A complete one quadrant divider is shown in Figure 3. It is the log amplifier (8048) shown in Figure 1 driving the antilog amplifier (8049) shown in Figure 2. The log amplifier output drives the base of Q_3 with a voltage proportional to the log of E_1/E_2. Transistor Q_3 adds a voltage proportional to the log of E_3 and drives the anti-log transistor, Q_4. The collector current of Q_4 is converted to an output voltage by A_4 and R_6, with the scale factor set by R_6.

$$V_{OUT} = \frac{E_1}{10E_2} \quad (4)$$

Note that the current corresponding to E_2 is derived from a true current source to avoid the errors discussed above under "reference current".

ARBITRARY POWER LAW CIRCUIT

Log amplifiers are an excellent means of computing $Y = X^{\alpha}$ relationships. Powers or roots may be computed precisely by cascading a log amp (8048) and antilog amp (8049) with appropriate scale factors. General-purpose multipliers are good for squaring ($\alpha = 2$), but non-integer exponents, such as 1.3 or 1.5; are sometimes needed. The circuit for this is shown in Figure 4.

The output of the 8048 log amplifier with a DC voltage input X that ranges from 1V to 10V is:

$$V_{OUT} = -K_1 \log_{10}\left(\frac{X}{10K\ I_{REF}}\right) \quad (5)$$

where K_1 is the scale factor of the 8048 and I_{REF} is the reference current. Setting I_{REF} to 100μA will make:

$$V_{OUT} = -K_1 \log_{10} X \quad (6)$$

The output of the antilog circuit (8049) is:

$$V_{OUT} = R_{OUT}\ I_{REF2}\ \text{antilog}_{10}\left(\frac{K_1 \log_{10} X}{K_2}\right) \quad (7)$$

or in other words,

$$V_{OUT} = R_{OUT}\ I_{REF_2}\ (X)^{K_1/K_2} \quad (8)$$

where *R_{OUT} Output resistor connected between pins 10 and 14 of the 8049.

I_{REF_2} Reference current for the 8049.

X–Input ($+1V \leq X \leq +10V$).

K_1–Scale factor of 8048.

K_2–Scale factor of 8049.

The exponent is set by the ratio of the scale factors K_1 and K_2, and the coefficient is set by the product $R0I_{REF_2}$.

Referring to Figure 4, and considering that X varies between 1V and 10V, the output of the 8048 log amp will vary between K_1 and zero, with a reference current of 100μA, set by the +15V reference and R_2. Setting the scale factor K_1 at 10V/decade uses the full 10V range. Since the exponent is set by a ratio of K_1 and K_2, setting K_2 = 5V/decade means the exponent is 2. The coefficient for the 8049 is set by R_{OUT} and I_{REF2}, while the reference current is set by the +15V reference and R_5.

$$I_{REF_1} = 100\mu A$$

$$I_{REF_2} = 1\mu A$$

$$K_1/K_2 = 2$$

$$R_{OUT}I_{REF_2} = .01$$

Putting these values into equation 5:

$$V_{OUT} = .01X^2 \text{ where } +1V \leq X \leq +10V$$

MULTIPLIER

In a variety of circuit applications, it is necessary to obtain linear product of two input signals. With two log amplifiers in conjunction with an antilog amplifier and summing amplifier, it is possible to generate products such as

$$Z = KXY \quad (9)$$

where K is the gain constant of the multiplier. A one quadrant multiplier is shown in Figure 5.

A_1 and A_2 are 8048 log amplifiers with the reference currents set for 1mA and scale factors of 1 volt/decade. The output of A_1 and A_2 are summed together by the 741 operational amplifier and resistors R_7 through R_{11}.

The 741 output drives A_3, and 8049 antilog amplifier. The reference current for the 8049 is set for 1mA and the scale factor is adjusted so that a 1 volt change at the input generates a decade change at the output. The output voltage of the 8049 is proportional to the product of the two inputs, X and Y. To make the maximum use of a large signal range, the multiplier gain K is set such that

$$V_{OUT} = \frac{XY}{10} \quad (10)$$

where X and Y are DC analog voltages that range from +0.1V to +10V.

Accuracy is defined as the maximum deviation of the actual output level from the ideal one, given by Eq.(10), for any choice of X or Y values within the dynamic range of the multiplier. It is normally specified as a percentage of full-scale output. For example, 1 percent full-scale accuracy means that with +10V output the actual output would be within ±100mV of the ideal level.

LOG SWEEP

This circuit uses the output of the ICL8049 to control the frequency of the ICL8038 waveform generator, with the 741 op amp used to linearize the voltage-frequency response. The input voltage to the 8049 can be, for example, the horizontal sweep signal of an oscilloscope; the output of the 8038 will then sweep logarithmically across the audio range. By feeding this to the equipment being measured, and detecting the output, a standard frequency response can be obtained. If the output is fed through an ICL8048 before being displayed, a standard bode plot results.

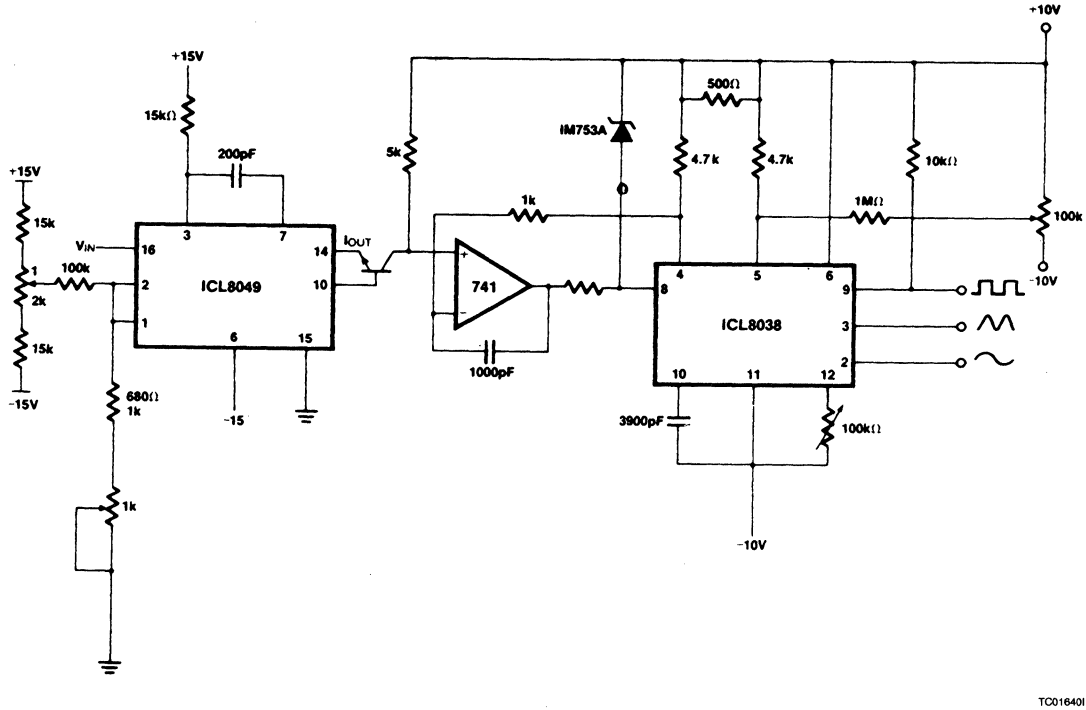

Figure 6: Logarithmic Sweep VCO for Audio Measurements

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A040
Using the ICL8013 Four Quadrant Analog Multiplier

CIRCUIT DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.

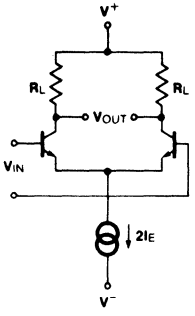

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Figure 1: Differential Amplifier

The small differential voltage gain on this circuit is given by

$$AV = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{I}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\frac{R_L}{r_e} = V_{IN}\cdot\frac{qI_ER_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \simeq \frac{V_Y}{R_Y} = 2I_E \text{ and } V_{OUT} = \frac{qR_L}{kTR_Y}(V_X\cdot V_Y)$$

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D

2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

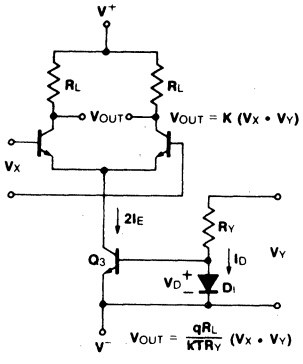

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Figure 2: Transconductance Multiplier

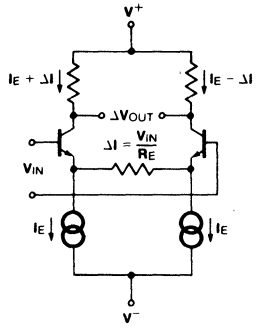

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Figure 3: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 4A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

$$\Delta V_{OUT} = 0V$$

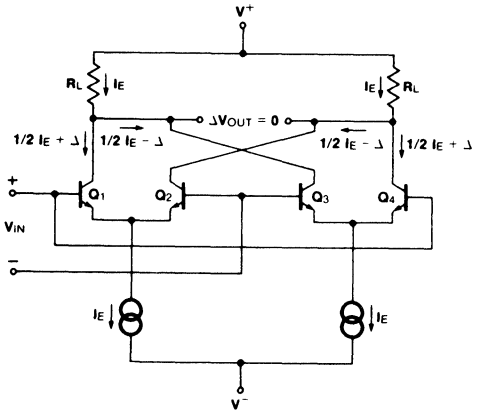

Figure 4A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

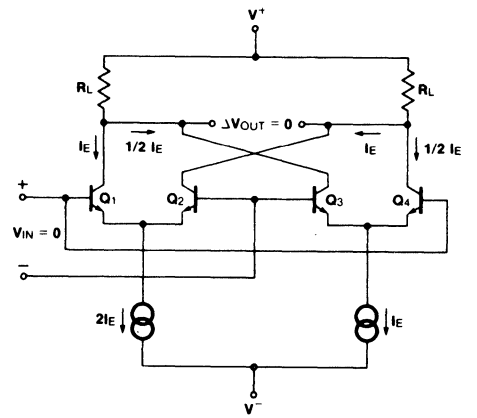

Figure 4B: No Input Signal with Unbalanced Current Sources

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).

This circuit of Figure 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

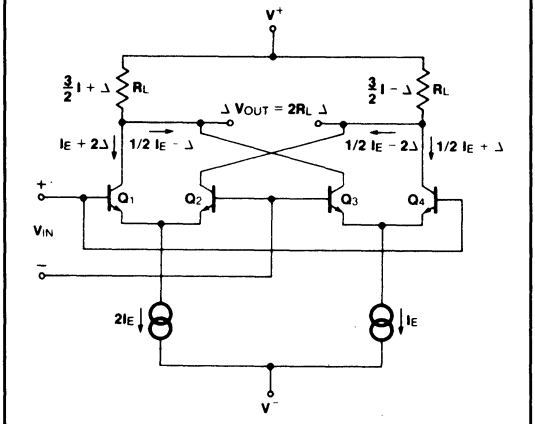

Figure 4C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

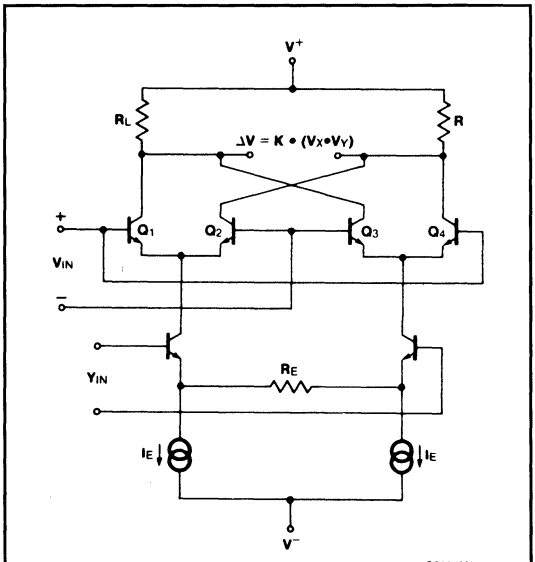

Figure 5: Typical Four Quadrant Multiplier-Modulator

Figure 3 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of

amplitude. If we combine this circuit with the voltage to current converter of Figure 3 we have Figure 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

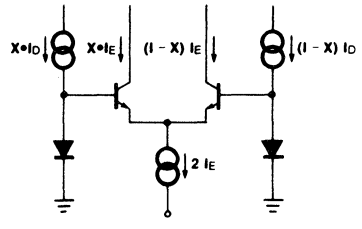

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Figure 6A: Current Gain Cell

The complete schematic is shown in Figure 7. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter.

The output amplifier comprises transistors Q_{16} through Q_{27}.

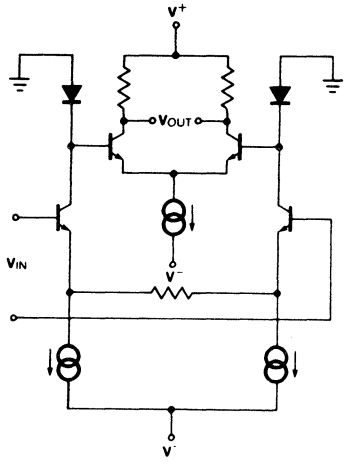

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Figure 6B: Voltage Gain with Signal Compression

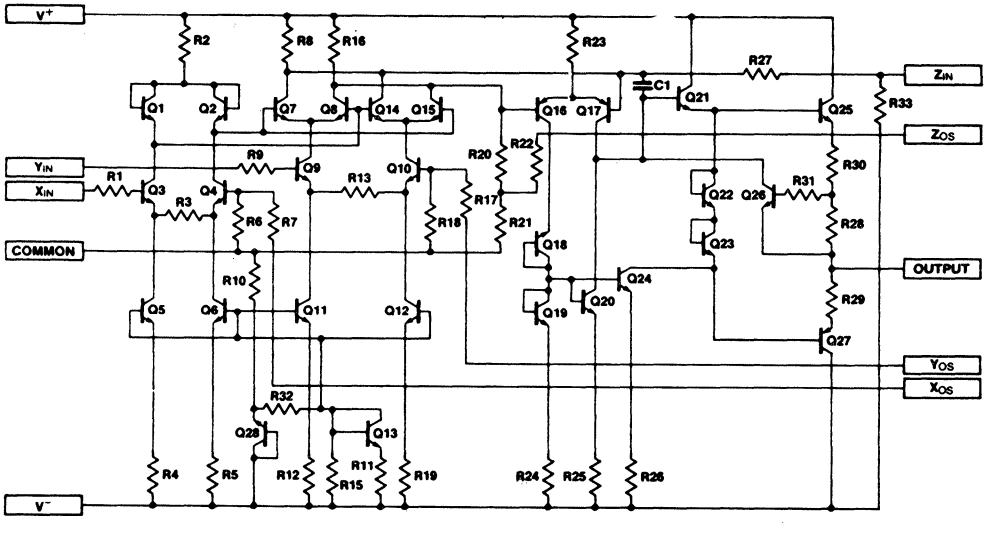

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Figure 7: ICL8013 Schematic

MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modular output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

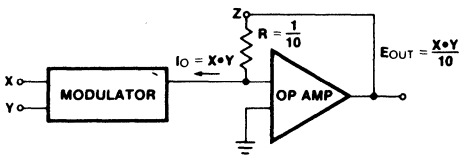


Figure 8A: Multiplier Block Diagram

MULTIPLIER Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤ 100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V$ DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output – Y_{IN}) = Zero.

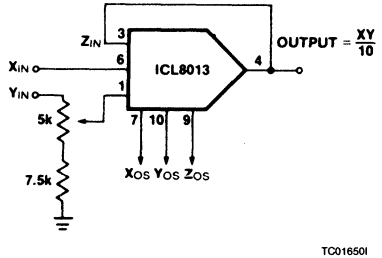


Figure 8B: Actual Circuit Connection

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X \cdot Y = \frac{Z}{R} = 10Z$$

$$\text{Since } Y = E_{OUT},\ E_{OUT} = \frac{10Z}{X}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

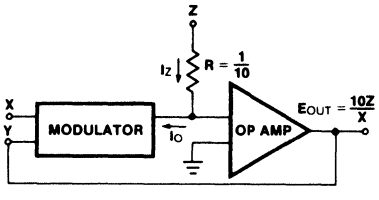


Figure 9A: Division Block Diagram

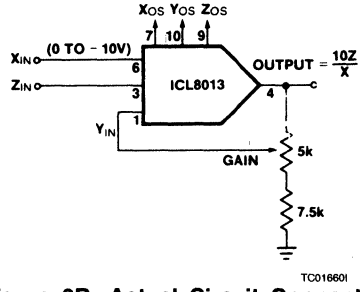


Figure 9B: Actual Circuit Connection

DIVIDER Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With $Z_{IN} = 0V$, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from –10V through –1V.
3. With $Z_{IN} = 0V$ and $X_{IN} = -10.0V$ adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from –10V to –1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (–10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from –10V to –3V.

SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2\omega = \frac{1}{2}(\cos 2\omega + 1)$.

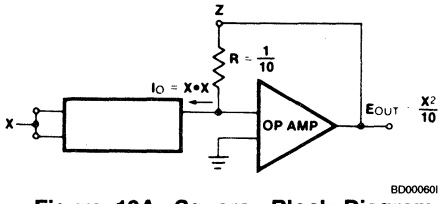


Figure 10A: Squarer Block Diagram

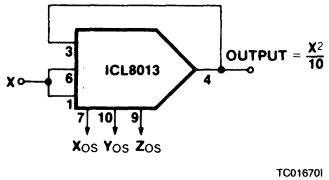


Figure 10B: Actual Circuit Connection

SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X \cdot Y = (-E_{OUT})^2 = 10Z$$

$$E_{OUT} = -\sqrt{10Z}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

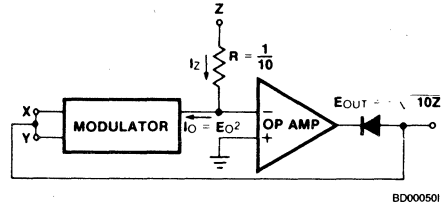


Figure 11A: Square Root Block Diagram

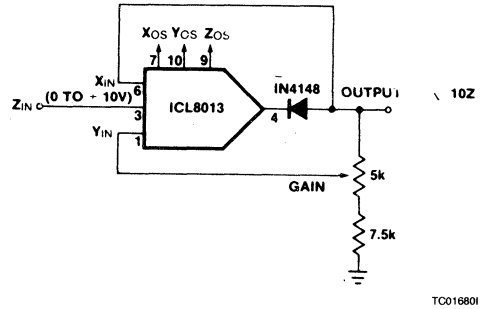


Figure 11B: Actual Circuit Connection

SQUARE ROOT Trimming Procedure

1. Connect the ICL8013 in the **Divider** configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

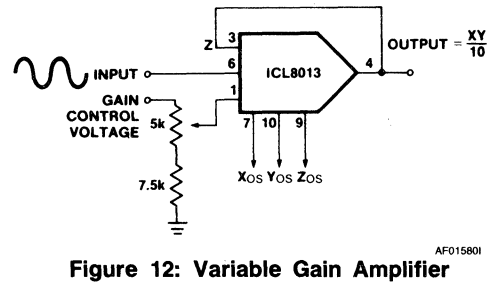
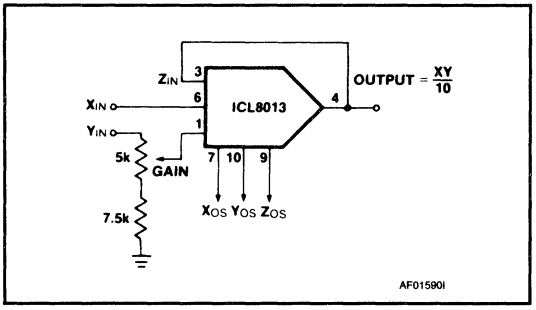


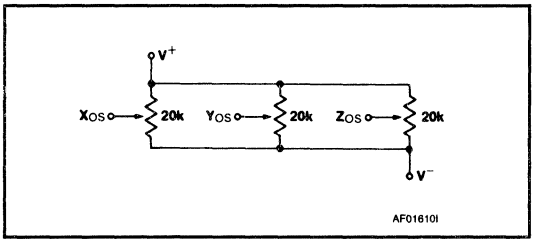
Figure 12: Variable Gain Amplifier

TYPICAL APPLICATIONS

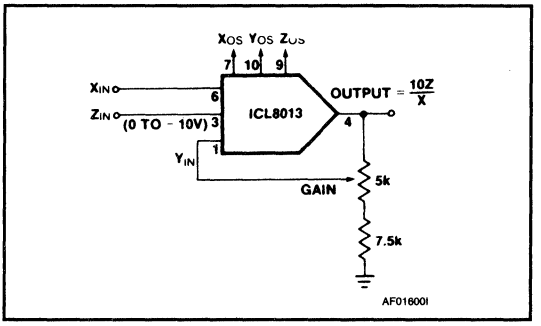
MULTIPLICATION



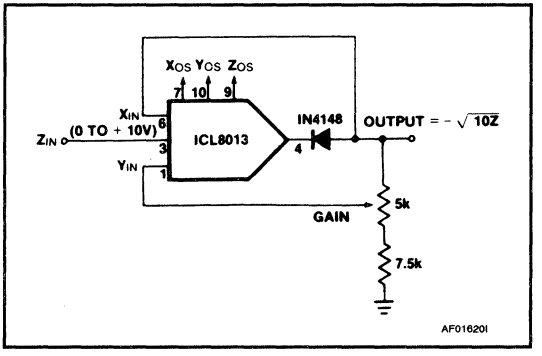
POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH



DIVISION

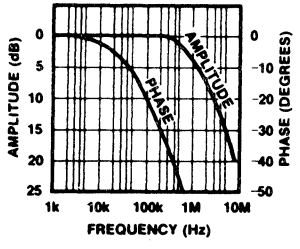


SQUARE ROOT

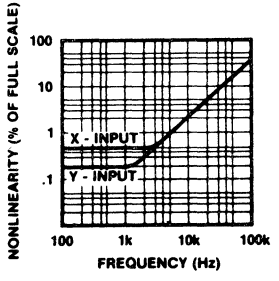


TYPICAL PERFORMANCE CHARACTERISTICS

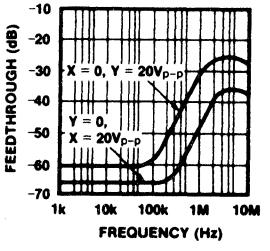
AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



NONLINEARITY AS A FUNCTION OF FREQUENCY



FEEDTHROUGH AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

AO13
Everything You Always Wanted To Know About The ICL8038

by Bill O'Neil

The 8038 is a function generator capable of producing sine, square, triangular, sawtooth and pulse waveforms (some at the same time). Since its introduction, marketing and application engineers have been manning the phones explaining the care and feeding of the 8038 to customers worldwide. This experience has enabled us to form articulate responses to the most frequently asked questions. So, with data sheet and breadboard in hand, read on and be enlightened.

Q1. I want to sweep the frequency externally but can only get a range of 100 to 1. (or 50 to 1)[or 10 to 1]. Your data sheet says 1000 to 1. How much sweep range can I expect?

A. Let's look at what determines the output frequency. Start by examining the circuit schematic at pin 8 in the upper left hand corner. From pin 8 to pin 5 we have the emitter-base of NPN Q_1 and the emitter-base of PNP Q_2. Since these two diode drops cancel each other (approximately) the potential at pins 8, 5 and 4 are the same. This means that the voltage from V+ to pin 8 is the same as the voltage across external resistors RA and RB. This is a textbook example of a voltage across two resistors which produce two currents to charge and discharge a capacitor between two fixed voltages. This is also a linear system. If the voltage across the resistors is dropped from 10V to 1V the frequency will drop by 10:1. Changing from 1 volt to 0.1V will also change the frequency by 10:1. Therefore, by causing the voltage across the external resistors to change from say 10V to 10mV, the frequency can be made to vary at least 1000:1. There are, however, several factors which make this large sweep range less than ideal.

Q2. You say I can vary the voltage on pin 8 (FM sweep input) to get this large range, yet when I short pin 8 to V+ (pin 6) the ratio is only around 100:1.

A. This is often true. With pin 8 shorted to V+, a check on the potentials across the external RA and RB will show 100mV or more. This is due to the VBE mismatch between Q_1 and Q_2 (also Q_1 and Q_3) because of the geometries and current levels involved. Therefore, to get smaller voltages across these R's, pin 8 must be raised above V+.

Q3. How can I raise pin 8 above V+ without a separate power supply?

A. First of all, the voltage difference need only be a few hundred millivolts so there is no danger of damaging the 8038. One way to get this higher potential is to lower the supply voltage on the 8038 and external resistors. The simplest way to do this is to include a diode in series with pin 6 and resistors RA and RB. See Figure 1. This technique should increase the sweep range to 1000 to 1.

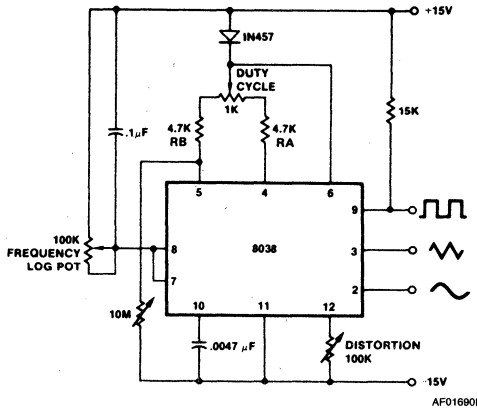


Figure 1: Variable Audio Oscillator, 20Hz to 20KHz

Q4. O.K., now I can get a large frequency range but I notice that the duty cycle and hence my distortion changes at the lowest frequencies.

A. This is caused partly by a slight difference in the VBE's of Q_2 and Q_3. In trying to manufacture two identical transistors, it is not uncommon to get VBE differences of several millivolts or more. In the standard 8038 connection with pins 7 and 8 connected together, there are several volts across RA and RB and this small mismatch is negligible. However, in a swept mode with the voltage at pin 8 near V+ and only tens of millivolts across RA and RB, the VBE mismatch causes a larger mismatch in charging currents, hence the duty cycle changes. For lowest distortion then, it is advisable to keep the minimum voltage across RA and RB around 100 millivolts. This would, of course, limit the frequency sweep range to around 100 to 1.

Q5. I have a similar duty cycle problem when I use high values of RA and RB. What causes this?

A. There is another error term which becomes important at very low charge and discharge currents. This error current is the emitter current of Q_7. The application note on the 8038 gives a complete circuit description but it is sufficient to know that the current charging the capacitor is the current in RA which flows down through diode Q_9 and into the external C. The discharge current is the current in RB which flows down through diode Q_8. Adding to the Q_8 current is the current of Q_7 which is only a few microamperes. Normally, this Q_7 current is negligible, but with a small current in RB, this current will cause a faster discharge than would be expected. This problem will also appear in sweep circuits when the voltage across the external resistors is small.

Q6. How can I get the lowest distortion over the largest frequency sweep range?

A. First of all, use the largest supply voltage available (±15V or +30V is convenient). This will minimize VBE mismatch problems and allow a wide variation of voltage on pin 8. The potential on pin 8 may be swept from V_{CC} (and slightly higher) to 2/3 V_{CC} +2V) where V_{CC} is the total voltage across the 8038. Specifically for ±15V supplies (+30V), the voltage across the external resistors can be varied from zero to nearly 8 volts before clipping of the triangle waveform occurs.

Second, keep the maximum currents relatively large (1 or 2mA) to minimize the error due to Q_7. Higher currents could be used, but the small geometry transistors used in the 8038 could give problems due to $V_{CE(sat)}$ and bulk resistance, etc.

Third, and this is important, use two separate resistors for RA and RB rather than one resistor with pins 4 and 5 connected together. This is because transistors Q_2 and Q_3 form a differential amplifier whose gain is determined by the impedance between pins 4 and 5 as well as the quiescent current. There are a number of implications in the differential amplifier connection (pin 4 and 5 shorted). The most obvious is that the gain determines the way the currents split between Q_2 and Q_3. Therefore, any small offset or differential voltage will cause a marked imbalance in the charge and discharge currents and hence the duty cycle. A more subtle result of this connection is the effective capacitance at pin 10. With pins 4 and 5 connected together, the "Miller effect" as well as the compound transistor connection of Q_3 and Q_5 can produce several hundred picofarads at pin 10 seriously limiting the highest frequency of oscillation. The effective capacitance would have to be considered important in determining what value of external C would result in a particular frequency of oscillation. The single resistor connection is fine for very simple circuits, but where performance is critical, the two separate resistors for RA and RB are recommended.

Finally, trimming the various pins for lowest distortion deserves some attention. With pins 7 and 8 connected together and the pot at pin 7 and 8 externally set at its maximum, adjust the ratio of RA and RB for 50% duty cycle. Then adjust a pot on pin 12 or both pins 1 and 12 depending on minimum distortion desired. After these trims have been made, set the voltage on pin 8 for the lowest frequency of interest. The principle error here is due to the excess current of Q7 causing a shift in the duty cycle. This can be partially compensated for by bleeding a small current away from pin 5. The simplest way to do this is to connect a high value of resistance (10 to 20mΩ) from pin 5 to V− to bring the duty cycle back to 50%. This should result in a reasonable compromise between low distortion and large sweep range.

Q7. This waveform generator is a piece of junk. The triangle wave is non-linear and has large glitches when it changes slope.

A. You're probably having trouble keeping the constant voltage across RA and RB really constant. The pulse output on pin 9 puts a moderate load on both supplies as it switches current on and off. Changes in the supply reflect as variations in charging current, hence non-linearity. Decoupling both power supply pins to ground right at the device pins is a good idea. Also, pins 7 and 8 are susceptible to picking up switching transients (this is especially true on printed circuit boards where pins 8 and 9 run side by side). Therefore, a capacitor (.1μF or more) from V+ to pin 8 is often advisable. In the case when the pulse output is not required, leave pin 9 open to be sure of minimizing transients.

Q8. What is the best supply voltage to use for lowest frequency drift with temperature?

A. The 8038AM, 8038AC, 8038BM and 8038BC are all temperature drift tested at V_{CC} = +20 V (or ±10V). A curve in the lower right hand corner of Page 4 of the data sheet indicates frequency versus temperature at other supply voltages. It is important to connect pin 7 and 8 together.

Q9. Why does connecting pin 7 to pin 8 give the best temperature performance?

A. There is a small temperature drift of the comparator thresholds in the 8038. To compensate for this, the voltage divider at pin 7 uses thin film resistors plus diffused resistors. The different temperature coefficients of these resistors causes the voltage at pins 7 and 8 to vary 0.5mV/°C to maintain overall low frequency drift at V_{CC} = 20V. At higher supply voltages e.g., ±15V (+30V), the threshold drifts are smaller compared with the total supply voltage. In this case, an externally applied constant voltage at pin 8 will give reasonably low frequency drift with temperature.

Q10. Your data sheet is very confusing about the phase relationship of the various waveforms.

A. Sorry about that! The thing to remember is that the triangle and sine wave must be in phase since one is derived from the other. A check on the way the circuit works shows that the pulse waveform on pin 9 will be high as the capacitor charges (positive slope on the triangle wave) and will be low during discharge (negative slope on the triangle wave). The latest data sheet corrects the photograph Figure 7 on Page 5 of the data sheet. The 20% duty cycle square wave was inverted, i.e., should be 80% duty cycle. Also, on that page under "Waveform Timing" the related sentences should read "RA controls the rising portion of the triangle and sine-wave and the 1 state of the square wave." Also, "the falling portion of the triangle and sine wave and the 0 state of the square wave is:"

Q11. Under Parameter Test Conditions on Page 3 of your 8038 data sheet, the suggested value for min. and max. duty cycle adjust don't seem to work.

A. The positive charging current is determined by RA alone since the current from RB is switched off. (See 8038 Application Note A012 for complete circuit description.) The negative discharge current is the ***difference*** between the RA current and twice the RB current. Therefore, changing RB will effect only the discharge time, while changing RA will effect

both charge and discharge times. For short negative going pulses (greater than 50% duty cycle) we can lower the value of RB (e.g., RA = 50KΩ and RB = 1.6KΩ). For short positive going pulses (duty cycles less than 50%) the limiting values are reached when the current in RA is twice that in RB (e.g., RB = 50KΩ and RA = 25KΩ). This has been corrected on the latest data sheet.

Q12. I need to switch the waveforms off and on. What's a good way to strobe the 8038?

A. With a dual supply voltage (e.g., ±15V) the external capacitor (pin 10) can be shorted to ground so that the sine wave and triangle wave always begin at a zero crossing point. Random switching has a 50/50 chance of starting on a positive or negative slope. A simple AND gate using pin 9 will allow the strobe to act only on one slope or the other, see Figure 2. Using only a single supply, the capacitor (pin 10) can be switched either to V+ or ground to force the comparator to set in either the charge or discharge mode. The disadvantage of this technique is that the beginning cycle of the next burst will be 30% longer than the normal cycle.

Q13. How can I buffer the sine wave output without loading it down?

A. The simplest circuit is a simple op amp follower as shown in Figure 3A. Another circuit shown in Figure 3B allows amplitude and offset controls without disturbing the 8038. Either circuit can be DC or AC coupled. For AC coupling the op amp non-inverting input must be returned to ground with a 100KΩ resistor.

Q14. Your 8038 data sheet implies all waveforms can operate up to 1 Megahertz. Is this true?

A. Unfortunately, only the square wave output is useful at that frequency as can be seen from the curves on page 4 of the data sheet, distortion on the sine wave and linearity of the triangle wave fall off rapidly above two hundred kilohertz.

Q15. Is it normal for this device to run hot to the touch?

A. Yes. The 8038 is essentially resistive. The power dissipation is then E^2/R and at ±15 volts the device does run hot. Extensive life testing under this operating condition and maximum ambient temperature has verified the reliability of this product. Copies of the reliability report are available from Intersil.

Q16. My data sheet shows a device with only 12 pins. The 8038 I received has 14 pins. How can I hook it up?

A. Our artist got lazy and decided to draw only the twelve pins that are used and omitted pins 13 and 14 which are not connected. The pin numbers and their functions are correct. This drawing has been corrected on the latest data sheet.

Q17. How stable are the output amplitudes versus temperature?

A. The amplitude of the triangle waveform decreases slightly with temperature. The typical amplitude coefficient is −.01%/°C giving a drop of about 1% at 125°C. The sine output is less sensitive and decreases only about 0.6% at 125°C. For the square wave output the $V_{CE(sat)}$ goes from 0.12V at room to 0.17 at 125°C. Leakage current in the "1" state is less than a few nanoamperes even at 125°C and is usually negligible.

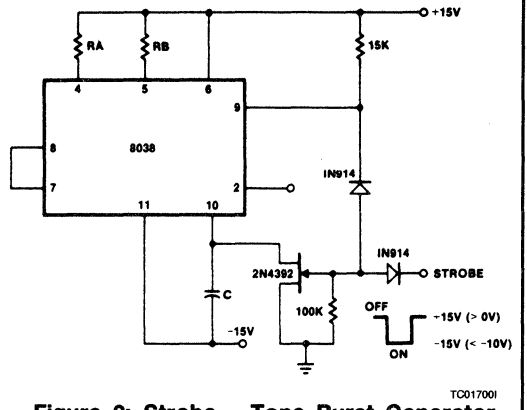


Figure 2: Strobe — Tone Burst Generator

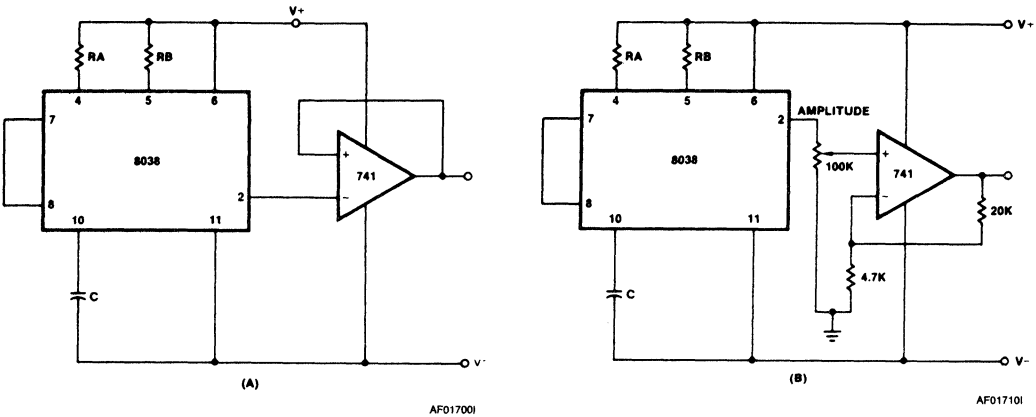
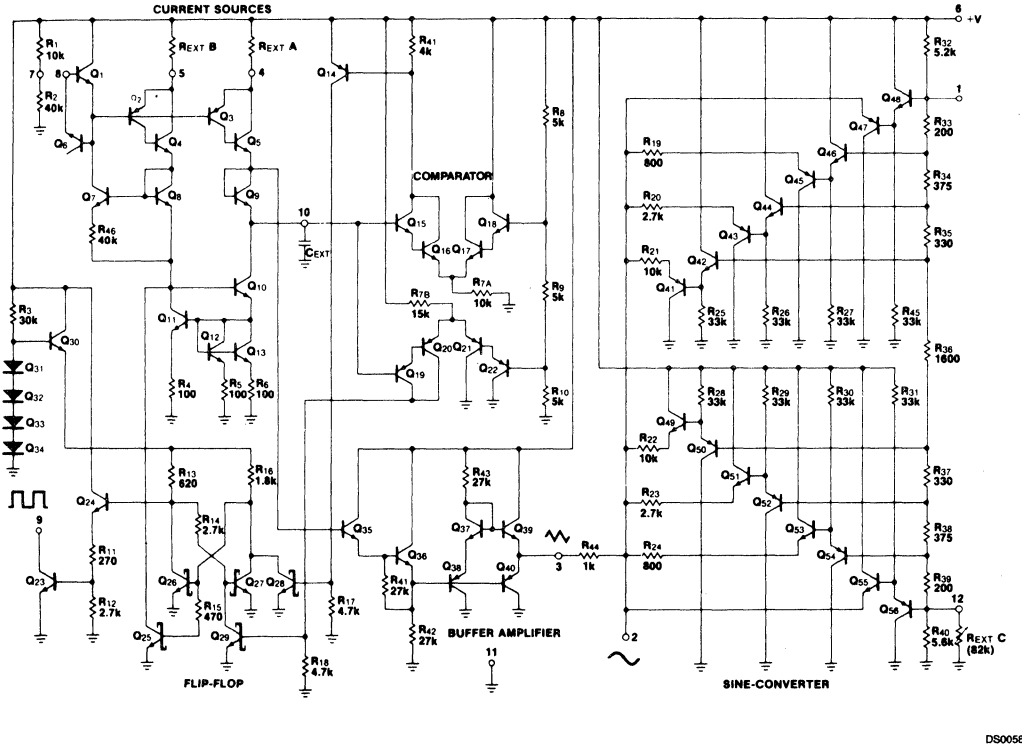


Figure 3: Sine Wave Output Buffer Amplifiers

DETAILED SCHEMATIC



A027
Power Supply Design Using The ICL8211 and 8212

INTRODUCTION

The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the THRESHOLD input is less than 1.15 volts. Figure 1 shows a simplified functional diagram of the ICL8211.

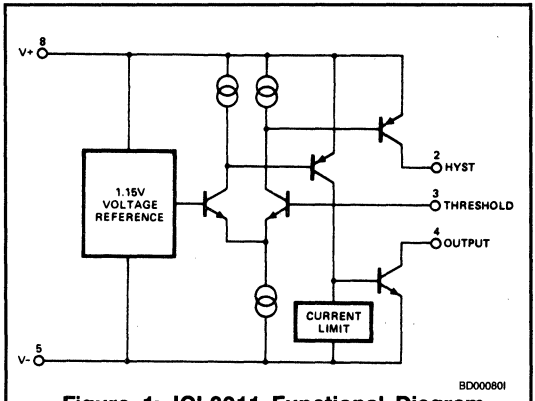


Figure 1: ICL8211 Functional Diagram

The ICL8212 provides a saturated transistor output (no current limit) whenever the input THRESHOLD voltage exceeds 1.15 volts. Both circuits have a low current HYSTERESIS output which is turned on when the THRESHOLD voltage exceeds 1.15 volts, enabling the user to add controlled hysteresis to his design. Figure 2 shows a simplified functional diagram of the ICL8212.

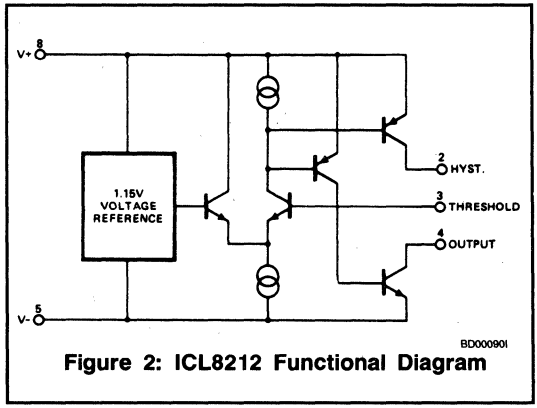


Figure 2: ICL8212 Functional Diagram

For a detailed circuit description of the ICL8211/12 refer to the data sheet. For large volume applications the ICL8211/12 may be customized by the use of metal mask options to include setting resistors or to vary the output options, or even to adapt the circuit as a temperature sensing element.

Applications for the ICL8211/12 include a variety of voltage detection circuits, power supply malfunction detectors, regulators, programmable zeners, and constant current sources. In this discussion we will explore the uses of the ICL8211/12 in power supply circuits of various types. Their attractiveness to the power supply designer lies largely in their ability to operate at low voltage and current levels where standard power supply regulator devices cannot be used. In addition, the unique features of the ICL8211/12 make them useful in many ancillary circuits such as current sources, overvoltage crowbars, programmable zeners and power failure protection.

POSITIVE VOLTAGE REGULATORS

Using the ICL8211/12 it is possible to design a series of power supply regulators having low minimum input voltage and small input/output differential. These are particularly useful for local regulation in electronic systems as their small input/output differential results in low power loss.

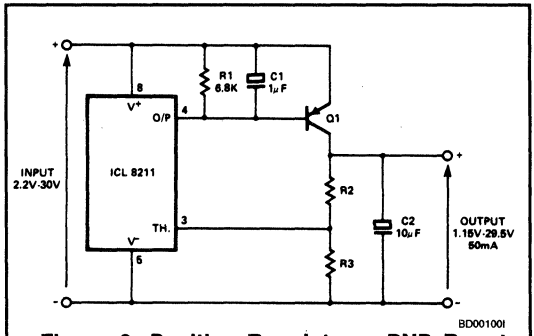


Figure 3: Positive Regulator — PNP Boost

The ICL8211 in Figure 3 provides the voltage reference and regulator amplifier while Q1 is the series pass transistor. R1 defines the output current of the ICL8211 while C1 and C2 provide loop stability and also act to suppress feedthrough of input transients to the output supply. R2 and R3 determine the output voltage as follows:

$$V_{OUT} = 1.15 \times \frac{R2 + R3}{R3}$$

In addition, the values of R2 and R3 are chosen to provide a small amount of standing current in Q1, which gives additional stability margin to the circuit. Where accurate setting of the output voltage is required, either R2 or R3 can be made adjustable. If R2 is made adjustable the output voltage will vary linearly with shaft angle; however, if the potentiometer wiper were to open circuit, the output voltage would rise. In general, therefore, it is better to make R3 adjustable as this gives failsafe operation.

The choice of Q1 depends upon the output requirements. The ICL8211 has a worst case maximum output current of 4mA, so with any reasonable device for Q1 the circuit should be capable of 50mA output current with an input to output drop of 0.5V. If larger output currents are required Q1 could be made into a complementary quasi-darlington, but the input/output differential will then increase.

Note also that Q1 provides an inversion within the loop so the non-inverting ICL8211 must be used to give overall negative feedback.

One limitation of the above circuit is that input voltages must be restricted to 30 volts due to the voltage rating of the ICL8211. The circuit of Figure 4 avoids this problem.

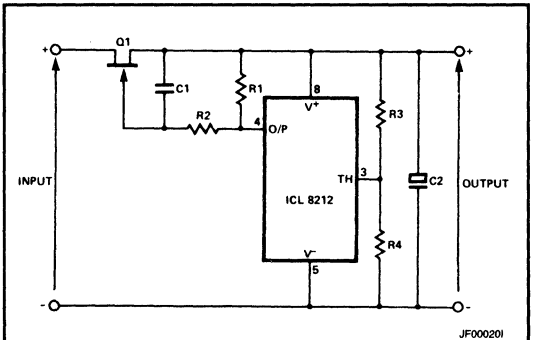


Figure 4: Positive Regulator — JFET Boost

In this circuit the input voltage is limited only by the voltage rating of Q1. The input/output differential is now dependent on the $R_{DS(ON)}$ of the JFET boost transistor. For instance, if Q1 were a 2N4391 the maximum output current would be equal to $I_{DSS(MIN)}$ which is 50mA and the input/output differential would be:

$$R_{DS(ON)} \times I_{LOAD} = 30\Omega \times 50mA = 1.5 \text{ Volts}$$

However, at lower load currents the input/output differential will be proportionately lower.

A further consideration when choosing the FET boost transistor is that its pinch-off voltage must be less than the output voltage in order for the ICL8212 to be able to pull the gate down far enough to turn the device off at no load.

The predominant loop time constant is provided by R2 and C1. This time constant should be chosen as small as possible commensurate with loop stability as it also affects load transient response. After an abrupt change in load current C1 must be charged to a new voltage level by R2 to regulate the current in Q1 to the new load level and therefore the smaller the R2 x C1 product the better the load transient response. The value of C2 should be chosen to maintain the output within desired limits during the recovery period of the main loop. Note, however, that because of the wide bandwidth of the ICL8212 and the absence of charge storage effects in the FET, these considerations are not particularly restrictive.

For higher current outputs the system could be further boosted using a bipolar transistor. One attraction of using a FET only output, however, is that the I_{DSS} of the FET gives a measure of output short circuit protection. Should both the low input/output differential of the circuit of Figure 3 plus the extended input voltage capability of Figure 4 be required, the circuit of Figure 5 may be used.

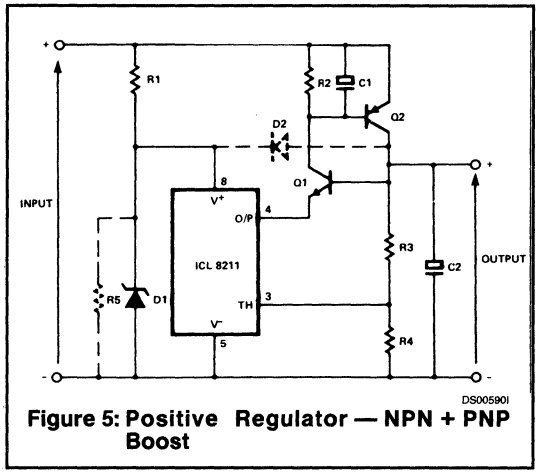


Figure 5: Positive Regulator — NPN + PNP Boost

This circuit is similar to that of Figure 3 except that Q1 has been added as a common base stage to buffer the output of the ICL8211 from the input supply and R1 and D1 to protect the input. Unfortunately, the ICL8211 cannot be supplied from the regulated output as this would result in the power supply being non self-starting. The choice of values for R2, R3, R4, C1 and C2 is identical to that of Figure 3, while D1 must be a voltage equal to or larger than the output voltage. R1 must be chosen to provide the relatively low supply current requirement of the ICL8211. An alternative arrangement for starting the circuit is to replace D1 with R5 and add D2. In this case the choice of R1 and R5 is such that once the output supply is established the ICL8211 is supplied through D2.

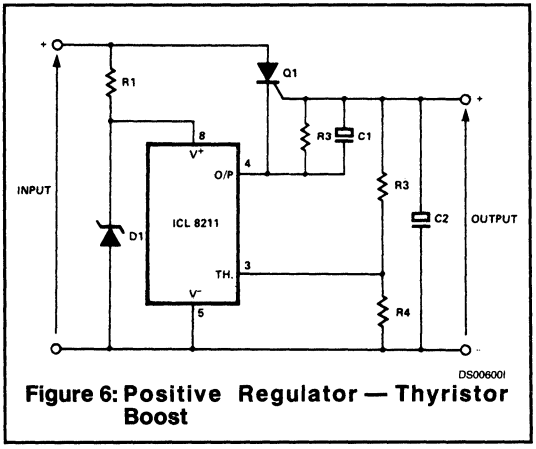


Figure 6: Positive Regulator — Thyristor Boost

In the circuit of Figure 5, Q1 and Q2 are connected in the classic S.C.R. or Thyristor configuration. Where higher input voltages or minimum component count are required the circuit of Figure 6 can be used. The thyristor is running in a linear mode with its cathode as the control terminal and its

gate as the output terminal. This is known as the remote base configuration.

A word of warning, however. Thyristor data sheets do not generally specify individually the gain of the PNP portion of the thyristor, on which the circuit relies. It must therefore either be very conservatively designed or some screening or guarantee of the PNP gain be provided.

Note that, with the exception of the I_{DSS} limit of Figure 4, none of the circuits so far described provide output current limiting. In general they are intended for applications in which the extra voltage drop of a current sensing resistor would be unacceptable. Where the circuits are used as local regulators and the output supplies are only connected to local circuitry the chance of output short circuits is relatively low and overcurrent protection is considered unnecessary. Where protection is required it can be added by any of the standard techniques. Figure 7 shows the simplest possible constant current protection added to the circuit of Figure 3.

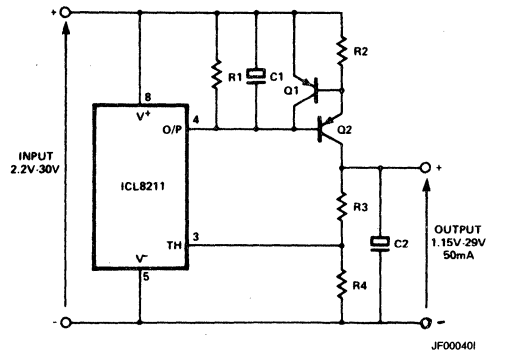


Figure 7: Positive Regulator — PNP Boost

In this circuit the current threshold is set by the base-emitter voltage of Q1 so that when the voltage drop in R2, due to load current, is sufficient to turn on Q1 base drive is removed from Q2 by Q1 collector. Note that this circuit works only because the output current of the ICL8211 is current limited so that there is no danger of Q1 and the ICL8211 blowing each other up with unlimited current.

NEGATIVE VOLTAGE REGULATORS

Because the reference voltage of the ICL8211/12 is connected to the negative supply rail, and their output consists of the open collector of an NPN transistor, it is not possible to construct a negative equivalent of the circuit of Figure 3. However, a negative equivalent of Figure 4 is easily constructed.

Of course the JFET must now be a P-channel device but otherwise the design considerations are identical to those for Figure 4. Should further boost of the output current level be required, an NPN boost transistor, Q2, (shown dotted) can be added. However, the charge storage effects of the NPN transistor will reduce the loop bandwidth so that R2 or C1 should be increased to maintain stability. Note also that in the circuit of Figure 8 an ICL8211 is used instead of an ICL8212 in order to maintain correct feedback polarity.

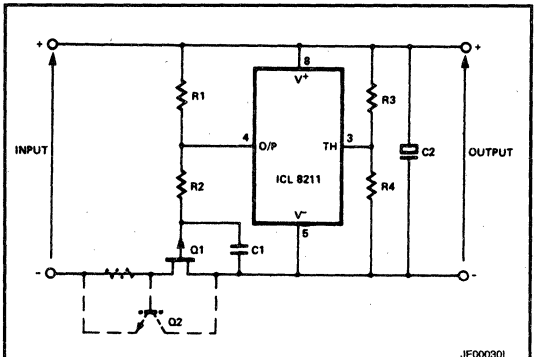


Figure 8: Negative Regulator — J-FET Boost

This is the closest negative equivalent to the circuits of Figures 5 and 6. In this case R1, R2 and D1 ensure that the circuit is self starting. The divider R1/R2 must be chosen to ensure that sufficient voltage (say −1 volt) is present at the base of Q1 to start the circuit under minimum output voltage conditions, but once the circuit is running D1 must remain forward biased even at maximum input voltage, otherwise the output of the ICL8212 will be unable to pull the emitter of Q1 low enough to turn it off under no load conditions. Thus for a 3 volt output supply which runs from a minimum 4 volt input the ratio of R1 to (R1 + R2) must be one quarter. In order that the base of Q1 is not taken below −3V once the circuit is running the maximum input voltage would therefore be −12V. An alternative arrangement which avoids this restriction is to replace R1 with a zener diode, reduce the value of R2 and delete D1.

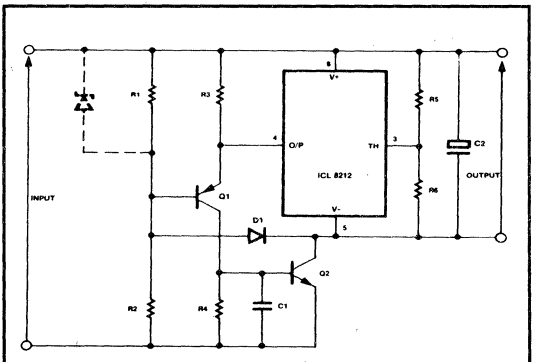


Figure 9: Negative Regulator — NPN + PNP Boost

In this case the only restriction is that the zener voltage shall be less than or equal to the output voltage of the regulator.

In the circuit of Figure 9, R3 must be chosen to provide sufficient base drive for Q2 via Q1 under maximum load conditions. The maximum value of the current in R3 which may be tolerated is 12mA, the worst case sink current of the ICL8212 output transistor.

Current limit can be applied to the circuits of Figure 9 in an analogous manner to Figure 7. In this case R3 is the

current source for the base of Q2, ensuring that the current limit transistor Q3 has a defined maximum collector current.

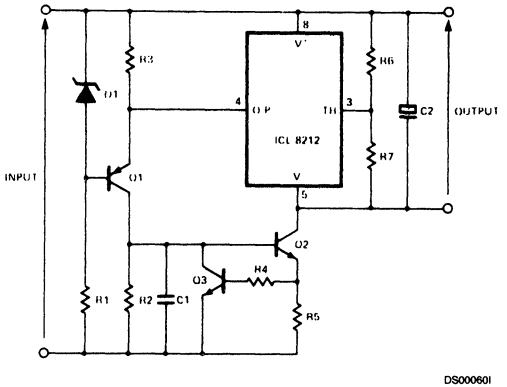


Figure 10: Current Limited Negative Regulator — NPN + PNP Boost

ANCILLARY POWER SUPPLY CIRCUITS

Figure 11 shows the ICL8212 connected as a programmable zener diode. Zener voltages from 2 volts up to 30 volts may be programmed by suitable selection of R2, the zener voltage being:

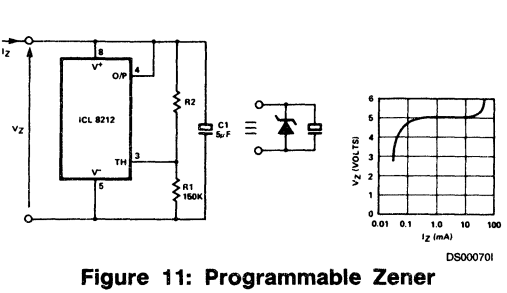


Figure 11: Programmable Zener

$$V_Z = 1.15 \times \frac{R_1 + R_2}{R_1}$$

Because of the absence of internal compensation in the ICL8212, C1 is necessary to ensure stability. Two points worthy of note are the extremely low knee current (less than 300μA) and the low dynamic impedance (typically 4 to 7 ohms) over the operating current range of 300μA to 12mA.

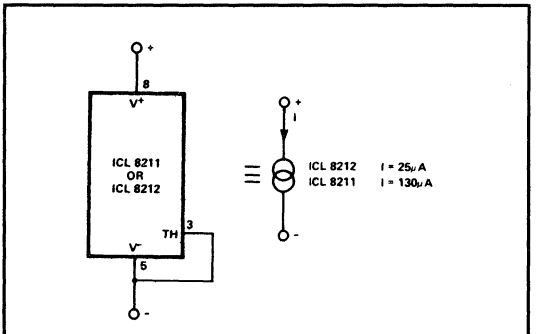


Figure 12: Constant Current Sources

The circuit of Figure 12 shows how the ICL8211/12 may be used as constant current circuits. At the current levels obtained with the ICL8211 or 12 on their own, the principal application will be in providing the "tail" currents of differential amplifiers which may be used in power supply design. A more useful application in power supplies is the programmable current source shown in Figure 13.

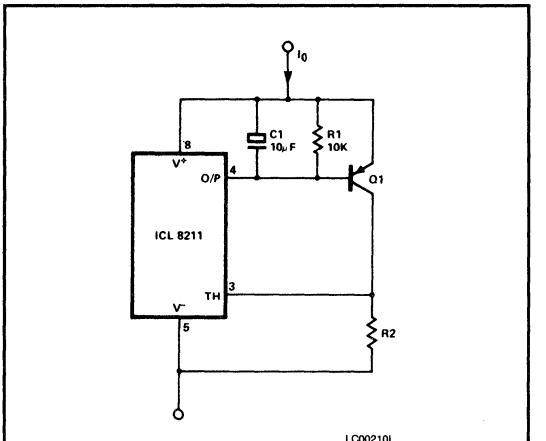


Figure 13: Programmable Current Source

In this case the output current is given by:

$$I_O = 25\mu A + \frac{V_{BE}}{R1} + \frac{1.15}{R2}(1 + \beta)$$

where β is the forward current gain of Q1 and V_{BE} is its emitter-base voltage. The principal cause of departure from a true current source for this circuit will be the variations in β with collector voltage of Q1. With the current settable anywhere in the range of about 300μA to 50mA and an operating voltage range from 2 to 30V, this circuit is particularly suitable as the current source driving the base of an output transistor in conventional series regulator power supplies. Another useful application is as the current source feeding a reference zener in highly stable reference supplies. Again, because of the absence of internal compensation in the ICL8212, C1 is provided to ensure loop

stability. It also helps to keep output current constant during voltage changes or transients.

The standard method of overcurrent protection in simple series regulated supplies is shown in Figure 14.

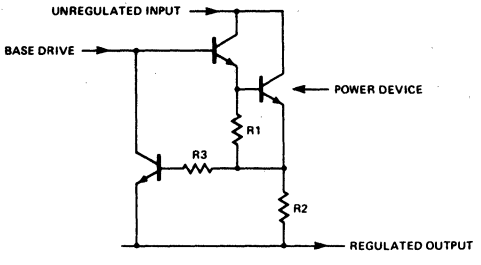


Figure 14: Standard Current Limit

The current limit value is simply:

$$I_{CL} = \frac{V_{BE(Q3)}}{R2}$$

The disadvantages of this circuits are the poor temperature coefficient of the emitter base voltage of Q3, the large variation of V_{BE} between different devices and the badly defined transition between constant voltage and constant current states due to the low gain of the current regulation loop.

In this case the current limit value is:

$$I_{CL} = \frac{1.15V}{R2}$$

One advantage of the circuit is the much improved temperature coefficient of the limit current. In Figure 14 the typical coefficient is 0.3%/°C, while in Figure 15 the typical coefficient is 0.02%/°C. In addition, the higher gain of the ICL8212 gives a much sharper transition between voltage limit and current limit conditions. The spread of threshold voltages will also be lower in this circuit, but if precise adjustment of the threshold is required R3 and R4 may be added as shown in Figure 15.

The major penalty of the system is the extra 500mV which must be dropped in R2 to effect current limiting. Note again that the low operating voltage and power supply current allow the ICL8212 to be powered directly from the base drive voltage of the power supply.

This circuit protects sensitive loads against high voltage transients on the power supply rail. Should the input voltage exceed the threshold set by R2 and R1, the ICL8211 will turn off Q1 and hence protect the load from the transient. R3 provides optional voltage hysteresis if so desired.

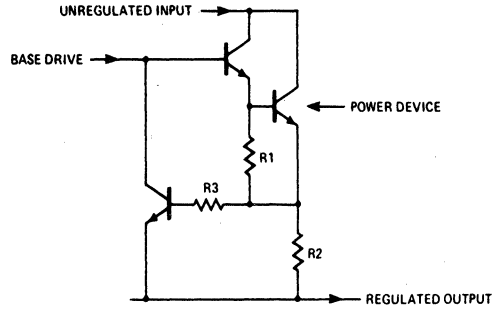


Figure 15: Improved Current Limit

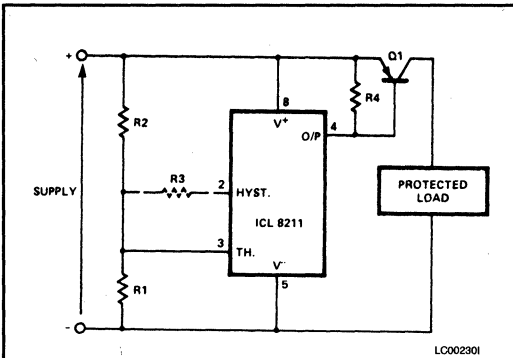


Figure 16: High Voltage Dump Circuit

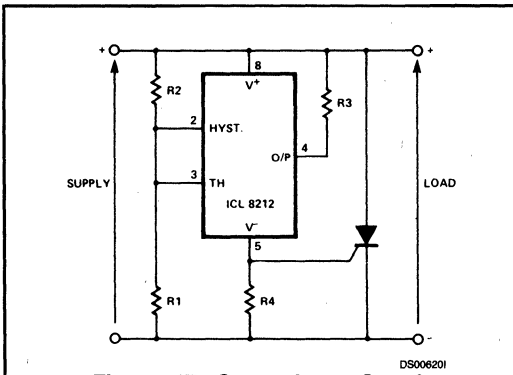


Figure 17: Overvoltage Crowbar

The most popular form of overvoltage protection is the Thyristor crowbar, which short circuits the supply in the event of an overvoltage condition. The circuit of Figure 17 triggers a thyristor when the supply voltage reaches a threshold defined by R1 and R2. The very low quiescent current of the ICL8212 means that there is negligible voltage drop in R4 during sensing so that accuracy is

unimpaired and there is no danger of triggering the thyristor. The connection from pin 2 provides hysteresis which is necessary in this case because the reference will rise on the top of R4 as soon as the threshold is reached and otherwise would provide negative feedback, which is overcome by the large positive feedback from pin 2. Resistor R3 limits the output current of the ICL8212 to a safe value of, say, 20mA. To operate properly the thyristor should have a gate trigger current not greater than about 10mA. Where higher gate currents are necessary the circuit of Figure 18 may be used.

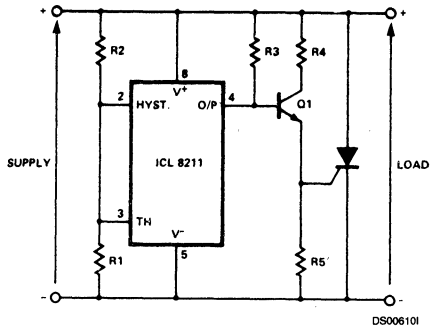


Figure 18: Overvoltage Crowbar

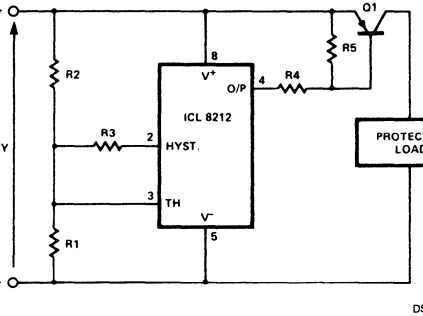


Figure 19: Low Voltage Disconnect

In this case the ICL8211 holds down the base of Q1 until the circuit is triggered. The current in R3 should not exceed 4mA as this is the worst case current the ICL8211 can sink at its output. With this circuit thyristors requiring gate drives in the 50 to 100mA region are easily tolerated.

Notice that in both the above circuits no extra supplies are needed to make the crowbars work down to voltages as low as 3V. In particular, this makes the circuits most suitable for use on 5V logic supplies where no other rails may be available to power a crowbar circuit or where, for reasons of safety, one does not wish to rely on auxiliary supplies.

In some systems it is undesirable to allow the supply rail to be partially established. For instance, in a logic system logical malfunctions may occur. Another example is the LM199/299/399 temperature stabilized reference. If the heater supply falls below about 9V the unit tends to "run away" and destroy itself.

Should the power supply voltage fall below the level determined by R1 and R2, Q1 is turned off, disconnecting the load entirely so that it cannot operate at partial voltage. Note that the removal of the load may cause the supply voltage to rise and the possibility of an oscillatory condition exists. Resistor R3 therefore provides a small hysteresis, which should be calculated to exceed the full load regulation drop of the supply.

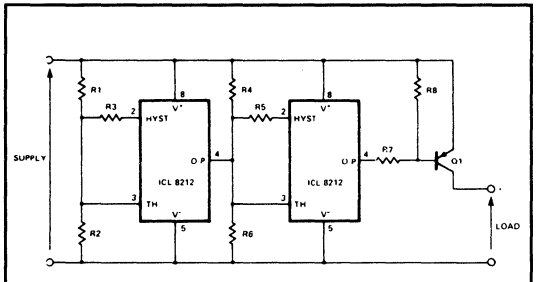


Figure 20: Power Supply Window Detector

The circuits of Figures 16 and 19 can be combined so that a load is only connected to the supply when the supply voltage is within a specified range. In this case IC1 senses the overvoltage condition while IC2 senses the undervoltage condition. Again, hysteresis may be added as necessary by the addition of R3 and R5.

In many systems, particularly those using microprocessors, it is necessary to provide a logic signal which gives advance warning of an impeding power failure so that the system can execute a shutdown routine before power is lost. A simple undervoltage detector on the regulated supply is generally insufficient as by the time an undervoltage signal is generated, the supply is already out of regulation and unless it falls very slowly there will not be sufficient time to shut the system down properly.

In the circuit of Figure 21, an incipient power failure is detected at the unregulated input of the regulator. Note that the value of main reservoir capacitor C1 must be large enough so that the shutdown routine can take place before the regulator drops out of regulation. Waveforms for a typical power failure are shown in Figure 22.

The threshold detector should be an ICL8212 if a logic '1' is required to initiate shutdown, or an ICL8211 if a logic '0' is required. Note that the ICL8212 will drive 7 TTL loads and the ICL8211 2 TTL loads.

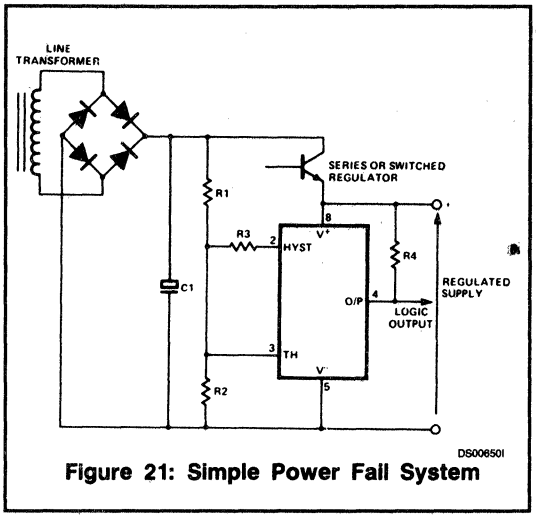


Figure 21: Simple Power Fail System

Notice that, because of the ripple always present on the unregulated supply, power failure was not actually detected until some time after the removal of input power. This waste of time means that larger voltage margins must be built into the system, reducing the regulator efficiency under normal operating conditions. In some instances, however, this circuit may be adequate.

In Figure 24, the power is monitored at a point isolated from the main capacitor C1 so that failure can be detected without having to wait for C1 to discharge below the minimum voltage of the normal ripple. Waveforms for this circuit are shown in Figure 24.

In this case R1 tops up C2 to the zener voltage each cycle, while C2 holds the input of the ICL8211 or ICL8212 (depending on the polarity of the required output signal) above its threshold during the zero crossings of the A.C. waveform. However, in the event of a power failure, C2 discharges through R2 to the threshold voltage of 1.15 volts, at which point the power fail signal is activated.

In this case, the worst point at which a power failure can occur is just before C1 begins to charge on the rising side of the input A.C. signal. However, because of the fast warning given by the system, it is still superior than that of Figure 21 in the time allowed for a shutdown routine.

CONCLUSIONS

Just a few of the many possible applications of the ICL8211 and ICL8212 in power supply systems have been described. Both in power supply systems and elsewhere, the features of the ICL8211 and ICL8212 make them very useful general purpose circuits. Once aware of the useful features of these low power, low voltage circuits the designer will rapidly discover a large number of applications for himself.

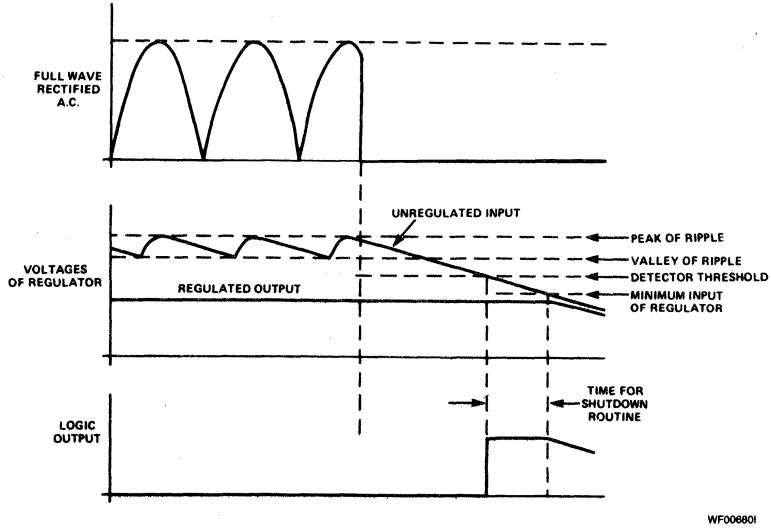


Figure 22: Simple Power Fail System Waveforms

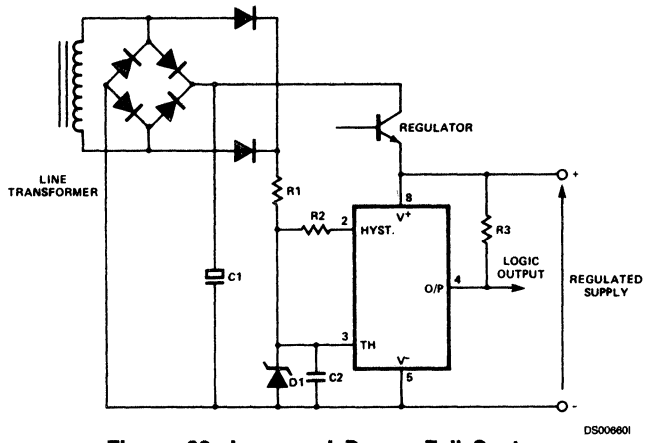


Figure 23: Improved Power Fail System

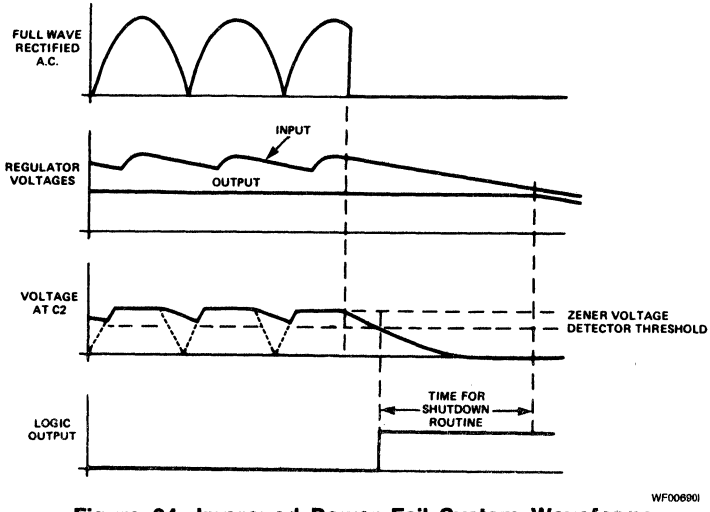


Figure 24: Improved Power Fail System Waveforms

5

R018
CMOS Regulators Improve Battery-Powered Equipment

Quiescent current of just 3.5μA and programmable outputs make two regulators (one positive and one negative) the answer to many common small power-supply problems.

A low-drain, voltage-programmable regulator would solve many of the problems associated with the design of power supplies for portable instruments, since system size, weight, operating temperature, cost, and accuracy are all dictated by the battery. Batteries with a flat discharge curve (i.e., "regulated voltage") are the most desirable but also the most expensive. For batteries that depend on a regulator, the choice is no longer between a monolithic regulator with a wastefully high quiescent drain (several milliamperes) and an expensive discrete design with many parts, some not suitable to the task.

Intersil's CMOS IC regulators, the ICL7663 and ICL7664, are programmable positive and negative-voltage regulators for battery-operated equipment. They draw just 3.5-μA quiescent current (with 9V input; 4μA with 15V), but they can regulate up to 40mA. The low quiescent current reflects the nanoampere operating currents of the reference, amplifier, comparator, and other devices within each regulator.

Although the regulators are complementary, they are not identical. The positive-voltage ICL7663 has a lower output impedance than the negative-voltage ICL7664 at currents above 1mA and has an additional output terminal (V_{TC}). The lower output impedance of the ICL7663 reflects the additional gain of an npn transistor connected as a voltage follower.

Among the parameters the regulators have in common (besides low I_Q) are a maximum input voltage of 16V and a reference voltage of 1.3V (produced by a micropower bandgap which is realized with CMOS, a significant achievement in itself), a line regulation of less than 0.01%/V, a reference temperature coefficient of ±200ppm/°C, and a dynamic output resistance of 1Ω at 1mA.

The output voltage of both regulators can be programmed with just two resistors, which may be high-value and, therefore, low-drain types. Each device has two output pins. The ICL7663 has high and low-current outputs; those of the ICL7664 are equal and are paralleled for higher currents.

For applications like remote data acquisition, which require equipment to turn on when interrogated, a useful feature is the shut-down terminal SHUTDOWN on the ICL7664). The low I_Q allows the system to idle at microamps and then respond to a turn-on logic signal. Unreliable switch contacts are thus eliminated. Both devices feature a comparator that senses output current and shuts down both outputs. A current-limiting resistor, chosen by the formula $R_{CL} = V_{TRIP}/I_{OUT}(max)$ connects to the desired output pin and (on its load side) to the sense pin. The comparator threshold or trip voltage is 0.7V in the ICL7663 and 0.35V in the ICL7664.

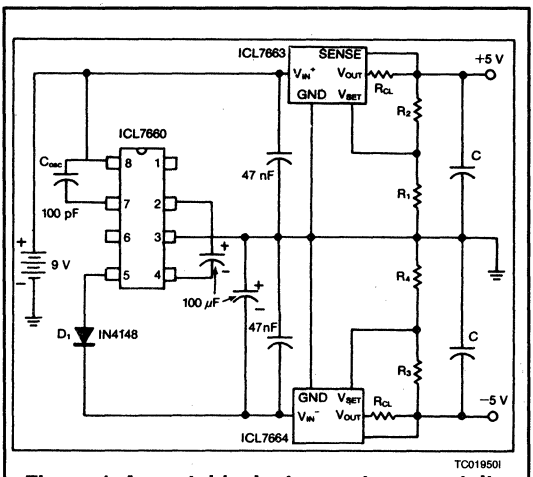


Figure 1: A portable instrument can get its positive/negative supply from a single battery with the ICL7663, ICL7664 and ICL7660 voltage converters. Because all three ICs are so efficient, a ±5-V instrument supply will operate even when the battery falls below 6V.

The ICL7663 and ICL7664 can join with an ICL7660 voltage converter in a dual power supply for portable instruments that depends on a single battery (Figure 1). The ICL7660 transforms the 9V into −9V (minus the drop across D_1): For greater efficiency, the ICL7660's internal oscillator is slowed from 10kHz to 1kHz by using C_{OSC} and changing the usual 10-μF capacitors to 100-μF. Regulated output voltages are determined by the ratios R_2/R_1 and R_4/R_3. That is, $V_{OUT} = V_{SET}(1 + R_2/R_1)$ for the ICL7663, $V_{SET}(1 + R_4/R_3)$ for the ICL7664. Asymmetric output voltages can be handled.

The 47-nF input capacitors prevent possible input instability and they should always be used. A small potential output-overshoot is eliminated by selecting C to reach 50% of the desired V_{OUT} in 10ms. From the formula $I = C\Delta V/\Delta T$,

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$$C = \frac{(10\ ms)\ (I_{OUT})}{0.5\ V_{OUT}},\ \text{or}\ 0.02\frac{I_{OUT}}{V_{OUT}}$$

Because all three ICs are highly efficient, operation at ±5 V_{OUT} can continue even when the battery voltage falls below 6V.

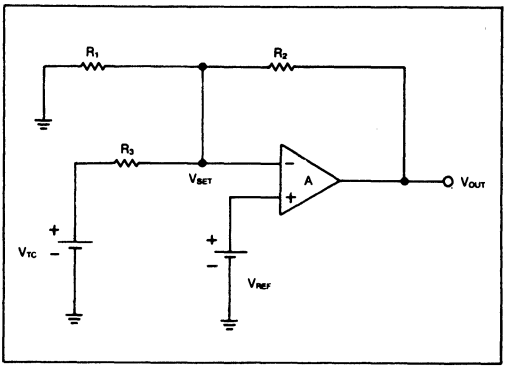

Figure 2: The negative temperature coefficient required by a multiplexed liquid-crystal display is scaled by adjusting the V_{TC} output terminal of an ICL7663 positive-voltage regulator relative to the V_{SET} input.

Multiplexed liquid-crystal displays (Figure 2) require an applied voltage with a negative temperature coefficient, so that the displays can operate over the widest possible range. The ICL7663's V_{TC} terminal enables the output to have a programmed temperature coefficient of up to −2000 ppm/°C. V_{TC} is 0.9V and is buffered.

The circuit in Figure 2 supplies a triplexed LCD display, which requires a peak voltage of 3V at 25°C. This voltage must have a temperature coefficient of −10mV/°C for operation from −10 to +60°C. The voltage is derived from the ICL7663 by using R_3 to inject V_{TC}, which has a temperature coefficient of +2.5mV/°C relative to GND or −2.5mV/°C relative to V_{SET}, R_3 works with R_2 to scale V_{TC} to the correct value:

$$V_{OUT} = V_{SET}\ (1 + \frac{R_2}{R_1}) + \frac{R_2}{R_3}\ (V_{SET} - V_{TC})$$

$$TC\ V_{OUT} = 0 + \frac{R_2}{R_3}(-TC\ V_{TC});\ [TC\ V_{SET} = 0]$$

$$-10mV/°C = \frac{R_2}{R_3}(-2.5mV/°C)$$

$$\frac{R_2}{R_3} = 4.$$

When these values are placed into the first equation,

$$3 = 1.3\ (1 + \frac{R_2}{R_1} + 4\ (0.4)$$

$$\frac{R_2}{R_1} = \frac{1}{13}$$

If R_2 is 1MΩ, R_1 is 13MΩ, and R_3 is 250kΩ.

In a two-terminal current source incorporating the ICL7663 (Figure 3, top), V_{prog} (V_{OUT}) is determined by R_1 and R_2. I_{source} is then V_{prog}/R_{prog} plus I_Q, which is the device quiescent current and the standing current through R_1 and R_2. R_{CL} may be omitted for small currents. A precision sink version (Figure 3, bottom), based on the ICL7664, may be set more accurately at low currents (less than 20μA), but the range is restricted for fixed R_L. The source circuit may be used as a sink (substituting an ICL7664) and the sink as a source (substituting an ICL7663), given the correct battery and capacitor polarities.

The two-terminal source replaces a whole boxful of current-limiting diodes, since it can be programmed over a much wider range of currents. In addition, a temperature coefficient of virtually zero is available at every current, instead of just one. The only other programmable monolithic current source available has a temperature coefficient so large that its main use is as a temperature sensor. Even that function can be performed at a lower cost when the ICL7663 serves as a current source (CS_1 and CS_2 in Figure 4).

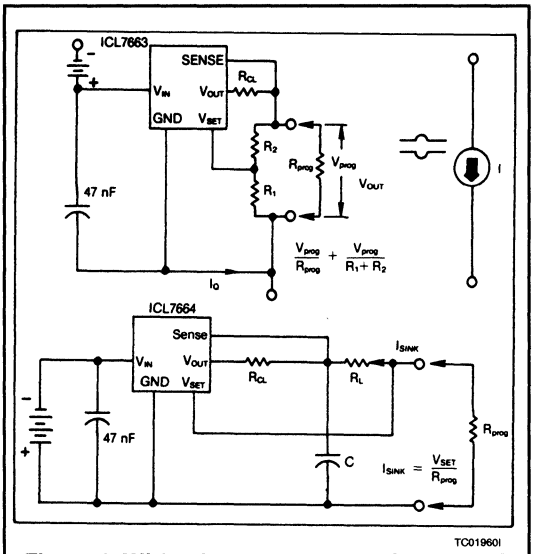

Figure 3: With the proper regulator and polarities, the two-terminal current source (top), and the precision current sink (bottom) can serve as either sink or source. In either capacity, however, the bottom circuit can be set more accurately for small currents.

5

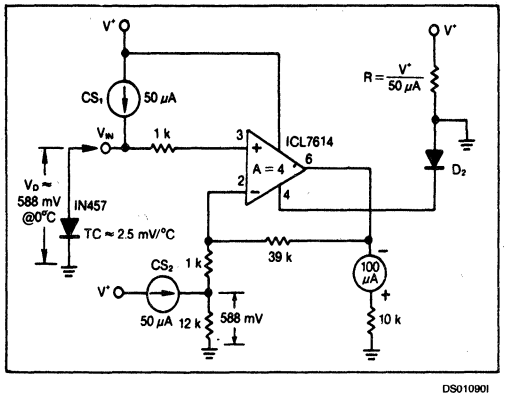

Figure 4: In this portable electronic thermometer, a current source (CS_1) based on the ICL7663 sets a constant current for the sensing diode at the given temperature (in this case, 588µA for 0°C).

The sensor is either a diode (least expensive) or diode-connected transistor (most predictable). One current source (CS_1) is then adjusted to make V_D, or V_{BE} in the case of a diode-connected transistor, equal to 588mV at a sensor temperature of 0°C. For any other sensor temperature (T), the formula V_{BE} (mV) = 588 – 2.5 T applies.

If a portable instrument requires constant current, it is usually derived via a resistor from the supply. This approach has two disadvantages. First, the constant current has a finite impedance, and the battery voltage limits the range of available current. Second, the difference between $V_{battery}$ and $V_{operating}$ is wasted across the regulator. In Figure 4, current sources 1 and 2, as well as the ICL7614 op-amp, can all work down to about 1.5V. Adding the drop across D_2 means a battery supply as low as 2V can be used. Therefore, a 9-V battery could theoretically drop to 2V before operation would cease. Since 5.4V is the actual end-of-life for such a battery, a better choice for the application is two 1.5-V cells. These cells give 3V for a much longer period yet occupy the same space. (Use of current sources to extend battery life has never been fully exploited.)

The diode D_2, along with R, divides the supply into positive and negative parts; the diode contributes –0.5V. This negative part ensures that the meter will deflect downscale for temperatures less than 0°C. The diode can be a Schottky (0.35V) or germanium (0.27V) type for less drop. If some zero fuzziness is acceptable, R and D_2 can be omitted.

The ICL7663 can also be designed into a voltage/current calibrator for field use (Figure 5). Decade ranges are used, but they can easily be changed to 1.999:1 ratios for digital readouts (use 1.900 — calibration is tricky at 1.999). Since this circuit has fixed currents and voltages, R_{CL} has been left out to make calibration simpler. If the battery cannot possibly be reversed, then the LED, 820-Ω resistor, and diode may also be omitted.

Because of their wide operating voltage range, the ICL7663 and ICL7664 can be considered programmable zeners, suitable as universal replacement devices. With their low drains, they are well suited to equipment that requires continuous self-calibration.□

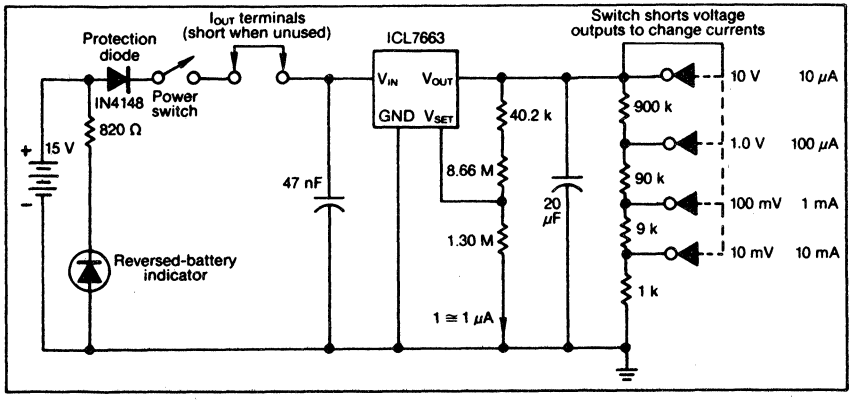

Figure 5: A portable voltage/current calibrator with fixed currents and voltages: The output sense resistor has been left out of the circuit to make calibration simpler.

AO51
Principles and Applications of the ICL7660 CMOS Voltage Converter

by Peter Bradshaw & Dave Bingham

INTRODUCTION

This application note describes a device originally designed to solve the specific problem of needing a negative supply when only a positive supply is available. This is very common, and occurs, for example, in systems using dynamic RAMs where the three-supply devices require a low current body bias supply of around −5V. Negative supply voltage is also desired in systems with a lot of digital logic (at +5V) but containing a small analog section using A/D converters, such as the ICL7107 or ICL7109 and/or op amps and comparators, operating on ground referenced signals. In all these cases, the current requirement and regulation are not very demanding, but nevertheless, generating such a −5-V supply is usually expensive and inefficient. Typically, a large number of discrete and integrated-circuit components are needed to convert the common +5-V line into a negative one, or to add an extra output to the main supply, the backplane wiring, etc.

This problem is solved by the ICL7660, a monolithic CMOS power supply circuit offering unique performance advantages over previously available devices. With the addition of only two non-critical capacitors (for charge pump and storage), it performs the complete supply voltage conversion from positive to negative for any input voltage between +1.5V and +10V, and provides the complementary output voltage of −1.5V to −10V. (An additional diode is needed for voltages above 6.5V.) The device operates by charging a pump capacitor to the input supply voltage and then applying the capacitor across the output supply, transferring the necessary charge to an open-circuit storage capacitor.

The ICL7660 delivers an open-circuit output equal to the negative of the input voltage to within 0.1%. Capable of producing 20mA, the device has a power-conversion efficiency of about 98% for load currents of 2 to 5mA. The use of two or more 7660s extends the device's capability, as will be shown later.

PRINCIPLES OF OPERATION

Since the 7660 multiplies either positive or negative voltages by a factor of two, it can be considered a simple voltage doubler. This basic voltage doubling operation is shown in Figure 1, where S1 and S3 are the switches used to charge C1, and S2 and S4 transfer the charge to C2. It differs from most voltage doublers in that the usual blocking diodes are replaced by on-chip active MOS transistor switches.

For a negligible load, clearly the voltage inversion will be nearly perfect, with only a tiny charge being lost to stray capacitance. With a significant load, the behavior is more complex.

The amount of charge transferred from C1 to C2 depends upon the amount lost from C2 to the load, and this charge must be made up by C1 from the basic power supply. The switches themselves also have series resistance, leading to further theoretical complications, but the net result is a typical overall output impedance of around 55Ω (100Ω max), provided that the capacitors are sufficiently large. For the natural oscillation frequency of the built-in oscillator (approx. 10kHz) values of 10μF are adequate.

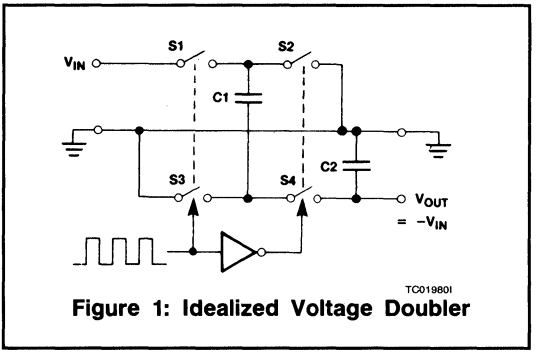

Figure 1: Idealized Voltage Doubler

The complete implementation of this function is achieved on a single CMOS chip, as shown in Figure 2.

The 7660 contains all the necessary conversion functions on-chip, except for the external pump and output reservoir capacitors and is made with a low-threshold CMOS technology using p- and n-channel transistors that turn on at 0.6V. The low power dissipation, simplicity, and small chip size of CMOS make it a near-ideal technology for this application.

The 7660 contains an RC oscillator, a series voltage regulator, a voltage-level translator, and a logic network (Figure 2). The logic network senses the voltage on the sources and drains of the two output n-channel transistors Q_3 and Q_4 and ensures that their substrates are always correctly biased.

POWER EFFICIENCY

In the case where a capacitor is charged and discharged between two voltages, V_1 and V_2, the energy lost is defined by

$$E = \frac{C(V_1 2 - V_2 2)}{2}$$

where C is value of the capacitor in farads and E is the lost energy. If $V_1 - V_2$ is very small compared with V_1, the percentage energy loss is also small, given as:

$$\frac{100(V_1 2 - V_2 2)}{2(V_1 2)}$$

At the limit, when $V_2 = V_1$, no energy is lost. If the values of C_1 and C_2 in Figure 1 are made very large and their impedances at the switching frequency are very low compared with the load resistance, energy-conversion efficiencies approaching 100% can be obtained. Energy is lost only

by a change of voltage during the transfer of charge into and out of a capacitor.

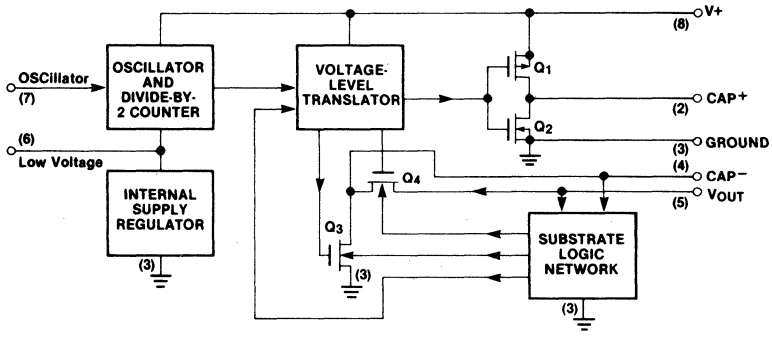

Figure 2: Functional Diagram of Complete Chip

DETAILED DESCRIPTION

Oscillator — Divider — Regulator

The 7660's oscillator (Figure 3) drives a conventional divide-by-2 counter whose principal function is to supply a 50% duty cycle output (at half the input frequency) to the voltage-level translator circuit. The conventional static counter requires a two-phase clock, and supplies an output signal and its complement.

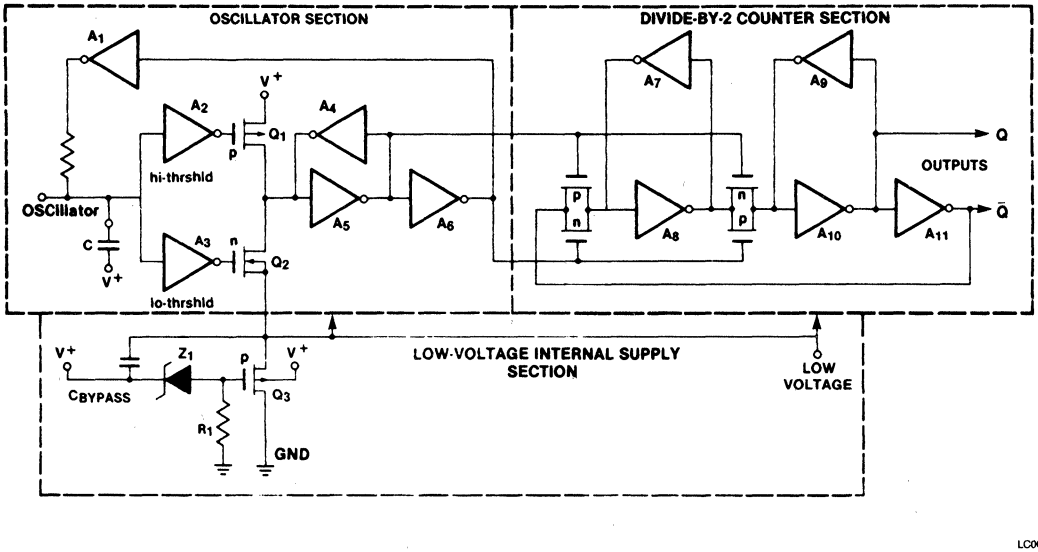

Figure 3: The 7660's Oscillator, Divider and Internal Regulator

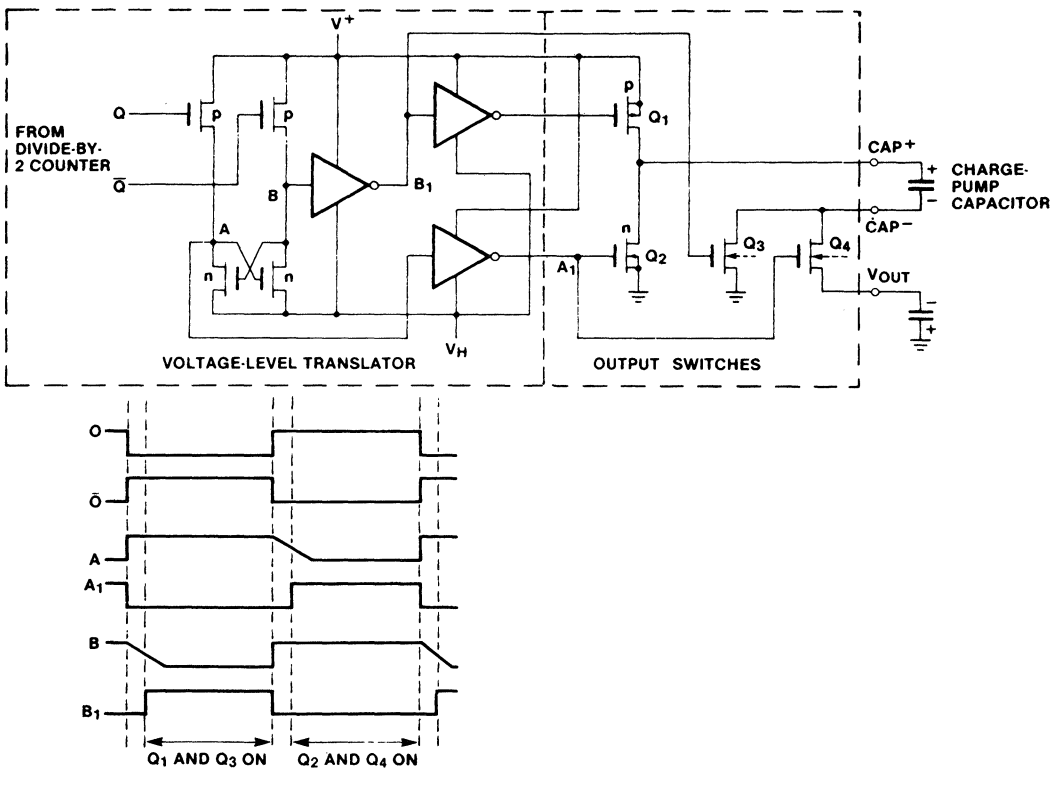

Figure 4: The 7660's Output Switches and Voltage-Level Translator Circuit

When the output of inverter A_1 is switched high, capacitor C charges positively until inverter A_2 (which has a high input-voltage trip point) switches its output low, to turn on transistor Q_1. Q_1 in turn forces the ratioed-inverter latch $A_4 - A_5$ to switch its output low. C then discharges negatively until inverter A_3 (which has a low input-voltage trip point) switches its output high, turning on transistor Q_2. The output of Q_2 resets $A_4 - A_5$ and restarts the cycle.

Since the oscillator has a high input impedance of about 1MΩ, it may be driven from an external source such as a TTL gate or equivalent, or its frequency may be lowered by the addition of an external capacitor. At room temperature with a +5-V supply and no external capacitor, the oscillator frequency will be 10kHz. The internal capacitance is about 10pF.

A series voltage regulator consisting of zener reference diode Z_1, resistor R_1, and source-follower p-channel transistor Q_3 provides a partially regulated supply for all the low-voltage circuitry on the chip. The regulator can supply up to −5V (with respect to the positive power supply) for input supply voltages of about 6V and higher. Because of the modest size of Q_3, the voltage regulator not only reduces power consumption at high supply voltages, but also limits the maximum current taken by the oscillator and the divide-by-2 counter.

The LV terminal can be used to short out the on-chip series regulator for better operation at low supply voltages. With the Low-Voltage terminal connected to ground, operation with an input supply voltage as low as 1V is possible. At higher voltages, however, it is mandatory that this terminal be open, in order to allow the internal voltage regulator to stop device latchup and avoid internal damage.

The Level-Translator and Output Switches

The level translators (Figure 4) provide switching signals to the gates of the four output transistors, Q_1 through Q_4, with amplitudes equal to the sum of the output and supply voltages. They also ensure that a break-before-make sequence takes place as switching alternates between charge and pump configurations.

The Substrate Logic Network

The substrate logic network (Figure 5) is the most critical part of the converter chip. Its two main functions are to make sure that the substrates of Q_2 and Q_4 (Figure 4) are never forward-biased with respect to their sources and drains, and to establish the most negative voltage of any

part of the circuit in either the charge or the pump cycles. This internal negative supply, V_H, is used to power the level translators. It drives the gate of either Q_3 or Q_4 to a voltage similar to that of the sources to ensure transistor turn off.

Transistors Q_3 and Q_4 require special drive considerations, since the sources and drains are inverted on each device during pump and charge phases. Consider Q_3's operation, for example. During the charge phase, the most positive source/drain terminal is connected to the external charge-pump capacitor. This terminal is then, by definition, the drain, whereas the source which is more negative is connected to ground. To minimize Q_3's resistance, it is also desirable to connect its substrate to ground and not to the output voltage or to V_H, since reverse-biasing the substrate of an MOS transistor with respect to its source increases its threshold voltage, and therefore the ON resistance.

During the pumping phase, the external capacitor's negative terminal is shifted negatively by a voltage approximately equal to the supply voltage. In this case, the most negative source/drain terminal is connected to the negative side of the external capacitor (and thus becomes the source of Q_3), and its drain is connected to ground.

Similar source-drain reversals occur for Q_4 except that here conditions are different for output short-circuit operation than during normal operation. Sensing circuitry monitors the voltages on the external capacitor's negative side and V_{OUT}, and compares them with ground. The substrate of Q_4 is then connected to the most negative of them. Figure 5 shows the substrate steering transistors for Q_3 and Q_4. The steering transistors (Q_{S1-5} are relatively small n-channel devices, and share Q_3 and Q_4's substrates.

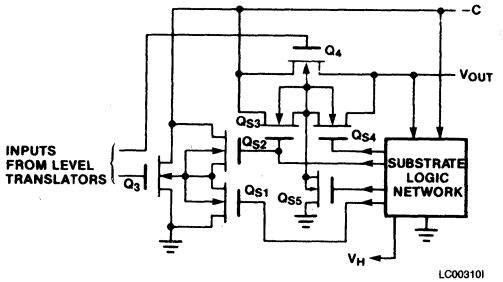

Figure 5: The Substrate Logic Network

SCR Latch Up

A CMOS device is inherently a four-layer, or silicon-controlled-rectifier (SCR), structure. This structure can be turned on through the forward biasing of the inherent pn junctions, and unless external current-limiting circuitry is used, latchup and resultant failure can occur.

The n-channel transistor source acts as the cathode of the SCR, and the p+ source of the p-channel transistor acts as the anode. Either n- or p-channel drains can act as the SCR gate. With about 2 V or more across the anode and cathode, the SCR can have either a low-impedance (ON) or high-impedance (OFF) state. For the ON state to occur, three things must happen: the product of the transistors' current gains, or betas, must be at least unity, a current greater than the holding current must be present, and a trigger pulse must be applied to either gate of the SCR. Trigger signals may be caused by static discharge on the gates or by connecting either gate to the power supplies before connecting power-supply lines to other terminals of the SCR. Even extremely high rates of voltage change across any two or more SCR pn junctions can produce latchup.

Triggering a CMOS SCR causes it to present an extremely low impedance (1 to 100ohms) across the power supply. Unless the power supply is current-limited, the device latches up and is often destroyed, usually by the vaporization of one of the bonding wires.

Although 7660 output-section switching transients are mainly capacitive, they inject currents into the substrate. At high input supply voltages, these transients can forward-bias junctions associated with the p- well or the Q_4 substrate. This in turn may trigger the inherent SCR in Q_4 and the adjacent on-chip circuitry. The result is to rapidly discharge the reservoir capacitor.

After the reservoir capacitor is almost totally discharged and the current in the SCR has fallen below the holding value, the device again operates correctly, until the output voltage (reservoir capacitance voltage) reaches the same critical value, and the latchup phenomenon starts again. Since this effect occurs only during the start of the charge cycle, and not during the pump cycle, isolating the reservoir capacitor with an external diode at the V_{OUT} terminal prevents capacitor discharge. This is recommended when using the device at higher voltage and temperatures. Otherwise the substrate logic network prevents SCR triggering, which is therefore not a problem for most operating conditions.

BASIC APPLICATION

The applications of the ICL7660 are remarkably varied, especially considering the rather narrow nature of the basic device function.

The basic circuit is shown in Figure 6, and the output characteristics for 5V inversion in Figure 7. For light loads, the output voltage follows the input very precisely, while for heavier loads, the output can be viewed as having perfect inversion, plus an output resistance of about 55Ω.

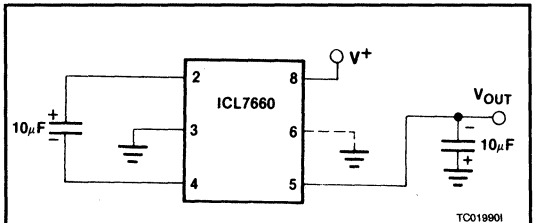

Figure 6: Simple Negative Converter

Thus at 18mA load, the output voltage drops about 1V below the input. Beyond around 40mA, the voltage drop becomes very non-linear, and the circuit self-limits, thereby protecting itself against excessive power dissipation. The output ripple is dependant primarily upon the output capacitor, since this must hold up the load during half the cycle time (or one oscillator period). In the steady-state case, this ripple is made up during the other half cycle time, and

enough pump capacitance should be used to ensure that this is done monotonically. The recommended values ensure this for the internal oscillator frequency.

For operation at low voltages, the output impedance begins to rise rather rapidly, as a result of reduced turn-on voltage on the MOSFET switches (Figure 8). This effect can be reduced by bypassing the internal regulator, tying LV to Ground, as shown in Figure 9. **This must not be done, however, if the incoming supply can exceed 6V under any circumstances, as the internal logic oscillator and divider stages will be damaged.** Note also the use of a series diode (Dx) at higher voltage and temperature, to protect the device against SCR action.

Figure 9 also shows an external oscillator capacitor. This can be used to reduce the oscillator frequency, giving a slight improvement in efficiency; see Figure 10.

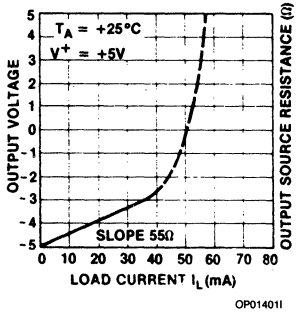

Figure 7: Output Characteristics

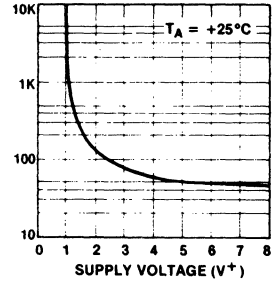

Figure 8: Output Resistance

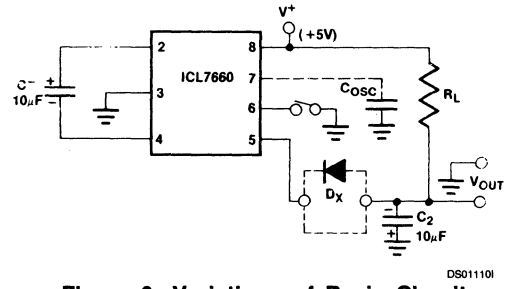

Figure 9: Variations of Basic Circuit

The dependence of the frequency on this external capacitance is shown in Figure 11. This can also be done to move the frequency away from a band of undue sensitivity to EMI in a system. However the output ripple will be increased, and the output impedance also unless the pump and storage capacitors are correspondingly increased.

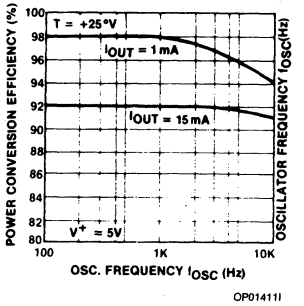

Figure 10: Efficiency Change with Oscillator Frequency

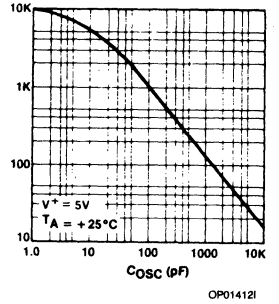

Figure 11: Frequency Variation with Oscillator Capacitance

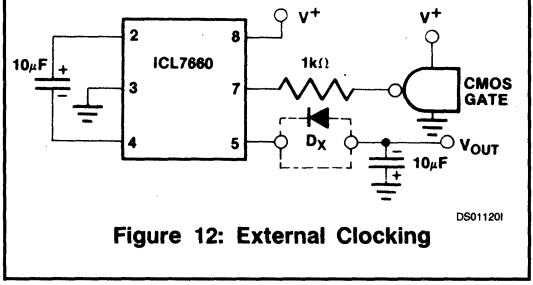

Figure 12: External Clocking

Synchronization to an external clock can be readily achieved, as shown in Figure 12. A TTL device can be used with the addition of a pull-up resistor (10kΩ to V^+ is suitable), as can any input swinging rail-to-rail on the positive supply. The series resistor prevents problems with overdrive on the internal logic. Output transitions occur on the positive edge of the external input.

WIDER (Parallel Connections)

For applications where the voltage drop due to load current is excessive, several ICL7660s can be paralleled. Normally this cannot be done efficiently with power supply circuits, since each one has a different idea of where the "ideal" output voltage would be and they usually end up fighting each other. However, here they see equal input voltages, and the virtually perfect inversion assures that each one does have the same idea of where the output should be so load-sharing is assured. Each device must have a separate pump capacitor, since the oscillators cannot be synchronized except with an external drive, and even then the −2 will be in a random condition. The connections are shown in Figure 13. Naturally the output capacitor is common to each device. Running independently, the ripple content will include components at the difference frequency as well as the individual pumping frequencies. If this is undesirable, a single exclusive NOR gate can be used to put two ICL7660s into antiphase by comparing the outputs on pin 2, and clocking one to maintain near synchronization with the basic oscillator of the other, as shown in Figure 14.

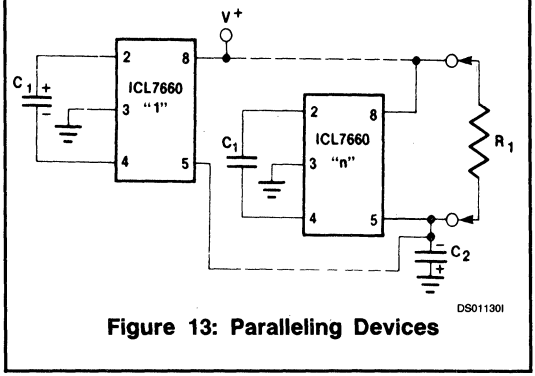

Figure 13: Paralleling Devices

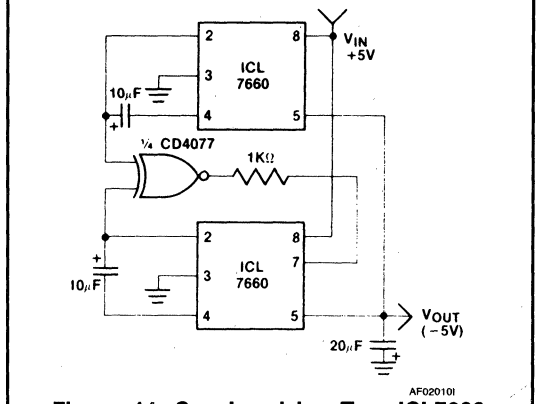

Figure 14: Synchronizing Two ICL7660s

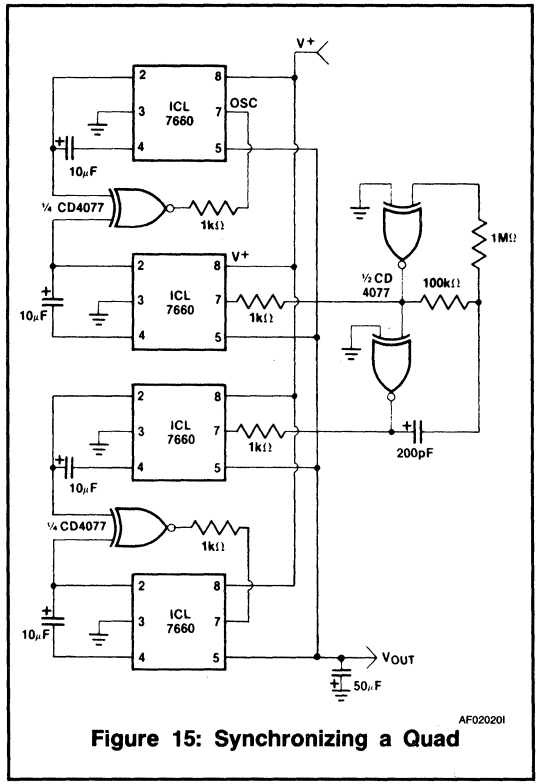

Figure 15: Synchronizing a Quad

The concept can be extended to drive four devices in four separate phases, using a single extra logic-gate package, as shown in Figure 15. The duty cycle of the oscillator is reasonably close to 50%, so driving two pairs, each in the configuration of Figure 14, from opposite phases of the oscillator gives four separately-timed pumps per cycle. This circuit will give about 75mA output before the voltage drops by 1V, or an output impedance of under 14Ω. The four-

phase operation minimizes the ripple, while ensuring very even load sharing. For even more parallel synchronous device, a Johnson counter using Q and Q outputs should be considered.

DEEPER (Series Connection)

It is also possible to connect ICL7660s in series, cascading them to generate higher negative voltages. The basic connections are shown in Figure 16.

This technique can be extended to several multiplication levels. However, the basic limitations of this technique must be recognized. In line with the Laws of Thermodynamics, the input current required for each stage is twice the load current on that stage, plus the quiescent current required to operate that stage.

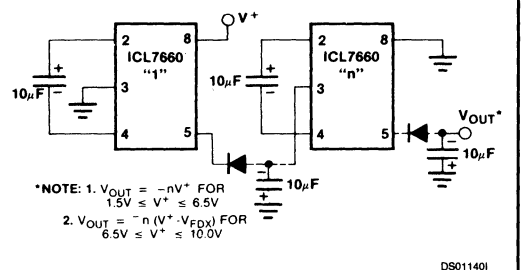

Figure 16: Cascading Devices for Increased Output Voltage

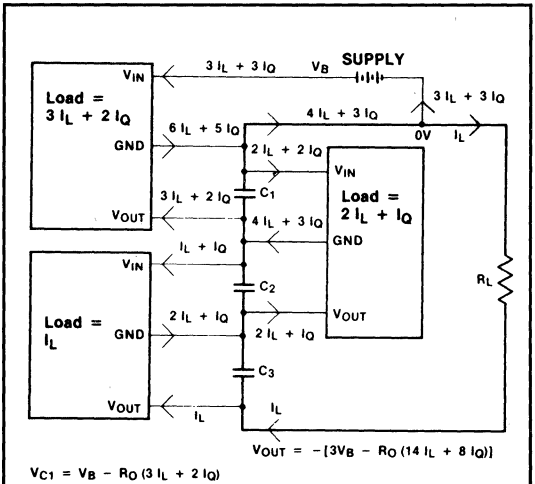

Figure 17: Current Flow for Cascaded Devices

Thus the load current is rapidly multiplied down the chain, as shown in Figure 17. Note also that the quiescent current increases the load current on each stage, though not as fast as the ultimate load itself.

Furthermore, the loss in voltage in early stages due to series resistance is multiplied through all subsequent stages. Thus the effective output impedance mounts rapidly with the number of stages. (See Table 1) This effect can be reduced by paralleling devices in the lowest stages (see above.) If the weighting corresponds to the square of the position, the effective resistance to load current goes up only linearly with the number of stages, but the cost quickly becomes prohibitive. Nevertheless, for light loads and moderate multiplication, useful performance can be achieved.

TABLE 1

#STAGES	RESISTANCE	MULTIPLIERS
n	$R_O(L)$	$R_O(Q)$
1	1	0
2	5	2
3	14	8
4	30	20
5	55	40

A variation of this circuit, another form of series circuit, is shown in Figure 18. This circuit can be used effectively to generate −15V from +5V in light load applications using only two devices. The output impedance corresponds roughly to n = 2 in Table 1, much better than if the previous circuit were used with n = 3. In general, geometric increases, as in Figure 18, are better until the voltage limit is reached, at which time arithmetic cascading as in Figure 16 must be utilized.

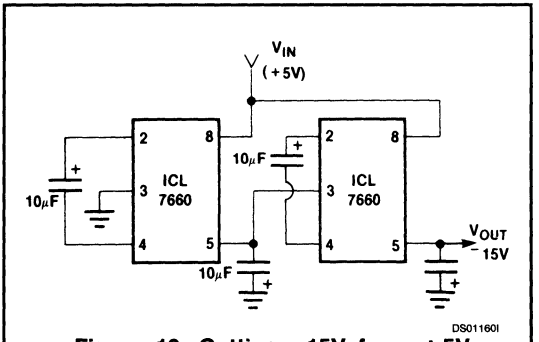

Figure 18: Getting −15V from +5V

UPSIDE DOWN (Positive Multiplication)

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1.) On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

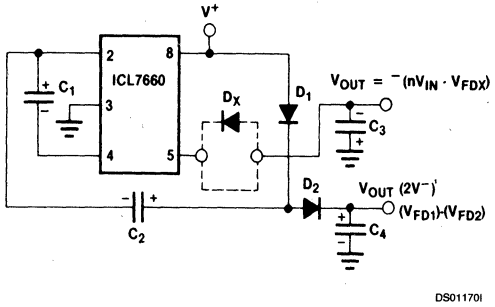

Figure 19: Combined Negative Converter and Positive Multiplier

DIVIDE AND CONQUER

The ICL7660 can be used to split a supply in half, as shown in Figure 20.

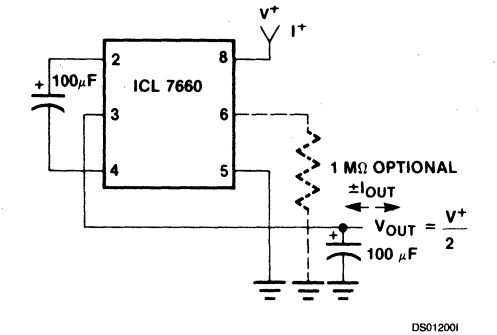

Figure 20: Efficient Supply Splitting

Here the "basic" output connection and the "basic" negative supply input are exchanged and the output voltage thus becomes the midpoint. Start-up can be a problem, and although careful capacitance and load balancing may frequently be adequate, a simple resistor to LV will always work. The circuit is useful for series-fed line systems, where a heavy local load at low voltage can be converted to a lighter current, at high voltage. Other useful applications are in driving low voltage (eg. ±7.5V) circuits from ±15V supplies, or low voltage logic from 9V or 12V batteries. The output impedance is extremely low; all parts of the circuit cooperate in sharing the current, and so act in parallel.

For other division ratios, the series configurations of Figure 16 can be driven backwards, to generate V_{IN}/n, or even $m/n(V_{IN})$, for small values of m and n. Again, care must be taken to ensure start up for each device.

One interesting combination of several preceding circuits is shown in Figure 21, where a +15V supply is converted, via +7.5V and −7.5V, to −15V using three ICL7660s. The output impedance of this circuit is about 250Ω.

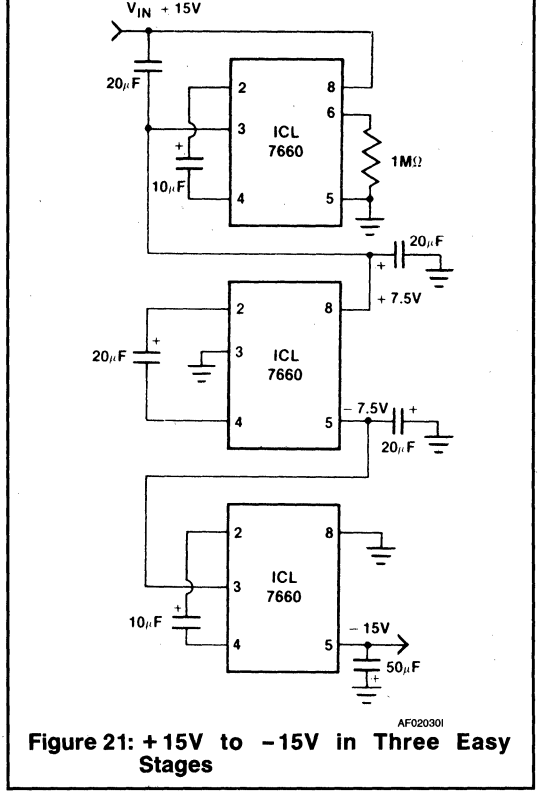

Figure 21: +15V to −15V in Three Easy Stages

For cases where the output impedance of an ICL7660 circuit is too high, obviously some form of output regulation can be used. However in most cases adequate regulation can be achieved at high efficiency by pre-regulating the input. A suitable circuit is shown in Figure 22, using the ICL7611 low power CMOS op amp. Because of the large source-current capability of this op amp, even on its lowest bias current setting, very efficient operation is possible. An ICL8069 band-gap device is used as the reference generator for the regulator. The output impedance can be reduced to 4Ω, while maintaining a current capability of well over 10mA. In designing circuits of this type, it is important to remember that there is a switching delay averaging one oscillator cycle between the output of the op amp and the actual output voltage. This can have substantial repercussions on the transient response if the time-constants in the circuit are not adequate. If multiple voltage converters are used, synchronization schemes such as those of Figures 14 and 15 are probably advisable.

MESSING ABOUT

The applications shown so far have corresponded to the use of the ICL7660 as a sort of equivalent of single turns on a power transformer, with paralleled turns to get more current, series turns for more voltage, etc. However, there are some other possibilities. By looking again at the block diagram (Figure 2), it is evident that the device could be used as a 50% duty cycle high power clock driver, using

either the internal oscillator or an external signal, as in Figure 23. An antiphase clock can also be derived from the circuit, as shown, but the pull-up on this output, being an N-channel switch only, does not have as good a voltage swing. It is adequate for TTL level operation, but for CMOS clocking may require an external pull-up resistor or transistor.

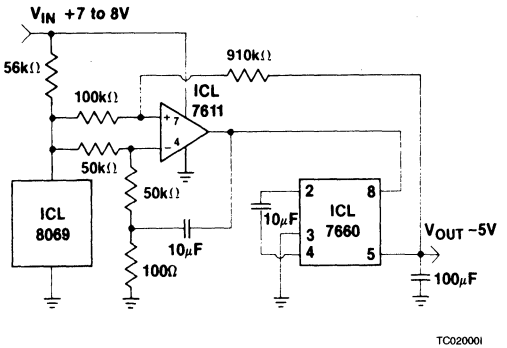

Figure 22: Regulated Output Inverter

Another interesting class of applications comes from the capability to synchronously detect the output of an AC driven transducer, as shown in Figure 24. (This could be viewed as a signal transformer application.) Although the circuit shown utilizes a linear transformer type of transducer, any similar device may be used. The output voltage, which is correctly phased and of either polarity, may be fed into an A/D converter such as an ICL106/7 or ICL7109, for display or microprocessor interface as desired.

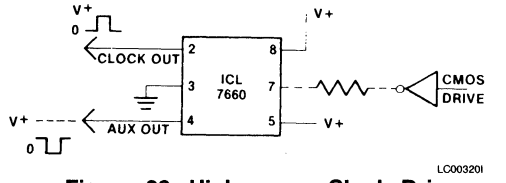

Figure 23: High power Clock Drive

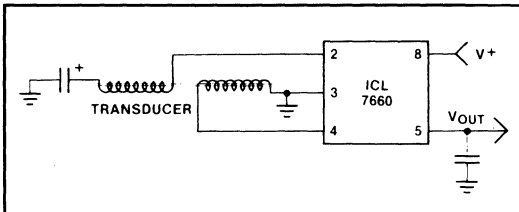

Figure 24: Transducer Driver and Detector

Chapter 6
Display Drivers

AO54
Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability

By Peter Bradshaw and Dan Watson

INTRODUCTION

For some time now Intersil has manufactured a line of display drivers oriented toward convenience of interface to the displays themselves and to the microprocessor bus or other digital system from which the displayed data comes. These devices have been mainly intended for numeric data (including hexadecimal and similar codes), and have been designed to drive Liquid Crystal (LCD), Light Emitting (LED) and Vacuum Fluorescent (VF) displays. Most have offered full-time drive, limiting the total number of segments that could be driven by each device to 28. The recent growth in popularity of alphanumeric displays, fueled by intelligent typewriters, language translators, Point of Sale Equipment, intelligent test equipment, and so on, has led to the development of a series of alphanumeric display drivers for LCDs and LEDs. The large number of segments involved means that any useful multi-character driver must use a multiplexing scheme, and fortunately LCD technology has reached a point where suitable multiplexable fluids are now becoming widely available. As for LEDs, the circuit and layout technology to handle the higher currents involved in a suitable LSI process has also been developed at the right time. A brief glance at the earlier products will lead us to a closer look at these new display drivers.

ADVANTAGES OF IC DRIVERS

Decoding and driving circuits for various types of numeric and alphanumeric displays have been greatly simplified by large scale integration. These new display drivers dramatically exhibit the following benefits and advantages over discrete designs:

- more circuit functions in less space
- simpler design effort for the user
- more flexible operation
- reduced circuit expense

Consider, for example, the design of an ASCII 8-character alphanumeric multiplexed LED display system. The block diagram for such a system constructed with discrete and MSI components is shown in Figure 1. Included as one of the blocks is an 8 word by 6-bit memory which stores the 6-bit ASCII word for each of the characters to be displayed. The addresses for the memory are selected either from the input circuitry, when writing to the display, or from the 3-bit counter, which generates the addresses for the 3 line to 8 line decoder. The NPN transistors drive the common cathode display for each character. The data from the memory is sent to a decoder which determines the correct segments to be turned on and must be a specially programmed ROM or PLA with an output for each of the 14- or 16-character segments. The PNP transistors serve as individual segment drivers, and the resistors in each of their collectors serve to set the current for that segment.

By contrast, Figure 2 shows an ASCII 8-character alphanumeric multiplexed LED display system in which all of the decoding, multiplexing, and driving is accomplished by a single integrated circuit, Intersil's ICM7243. The savings in board space, design time by the user, and cost are easy to see. Additionally, this single chip approach offers several additional features, such as built-in microprocessor compatibility, low power shutdown mode, and automatic interdigit blanking. These features would require extra circuitry in the discrete design and increase the cost of the system.

One advantage frequently not fully appreciated is the offloading of microprocessor software into the display driver. This can free up both memory and time for other tasks, as compared to designs using software-derived display decoding and timing.

The integrated circuits now available provide a wide selection of display driving capability and can be divided into several categories. Most numeric display drivers also provide a few alphabetic characters for displaying hexadecimal values. True alphanumeric display devices have numbers, letters, punctuation marks, and other symbols in their character sets. The interconnection to display driver ICs also varies from multiplexed BCD inputs to serial bit-stream arrangements or parallel microprocessor bus compatible input schemes.

NON-MULTIPLEXED DISPLAYS

One important category of driver circuit is the non-multiplexed, or direct drive type. In this case, direct drive means that there is one line for each segment of the display (e.g. 4 digits x 7 segments = 28 lines).

In many applications the use of a full-time or non-multiplexed configuration has a number of advantages. For relatively high current displays such as LEDs and VF, the absence of continuous and somewhat unpredictable display current changes can be a major advantage. Current spikes and level changes, reflected usually on supply lines to other circuitry, are minimized, and generally occur only when the display is changed, thus being under the control of the rest of the system. As for LCDs, multiplexable displays, though widely used in calculators, have not been available on the general market.

The ICM7211/12/35 series of full time display drivers come in a number of versions. The ICM7211 drives liquid crystal displays (LCD), the ICM7212 drives light emitting diode displays (LED) and the ICM7235 drives vacuum fluorescent display panels (VF). These three display drivers are identical except for the output driver structure. Multiplexed BCD or microprocessor bus compatible input configurations are available. As shown in the Functional Diagram of Figure 3, they all drive 4 digits of 7 segments each. The data input is fed through a decoder into the latch, from which the segment outputs are derived. This particular part is an LCD driver, and so includes a backplane oscillator and driver, which is also fed to the segment drivers. The oscillator is arranged so that the backplane driver can be disabled by tying the oscillator pin to the negative supply. Once this is done, the associated pin, together with the segment drivers keyed from it, can then be externally driven. Several display drivers can thus drive a multidigit

407059-001

display, with one backplane. The digit into which the incoming data is loaded is determined by individual select lines, for ready interface with the multiplexed BCD signals widely used in instrumentation, etc.

Another version is shown in Figure 4. This part, the ICM7212M, is oriented to microprocessor bus interface, with binary-coded digit select lines and active low $\overline{\text{CHIP SELECT}}$ lines. The device is an LED driver, and the backplane oscillator and control is replaced by a brightness control.

The output is set to drive common anode displays, with segment currents of typically 8mA. The Functional Diagram of the ICM7235M VF display driver is virtually identical, except for the polarity of the outputs. These outputs can withstand up to 30V when off, more than adequate for the standard VF displays available. The segment current is typically 2.5mA, which also allows the devices to be used for driving common cathode LEDs.

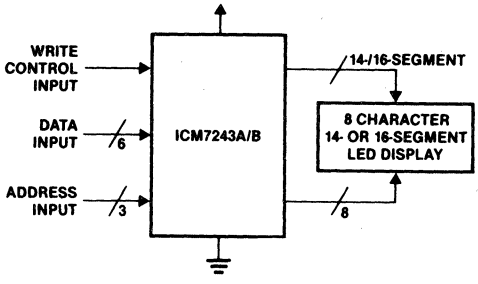

Figure 2: 8-Character Alphanumeric LED Display System (Single Chip Design)

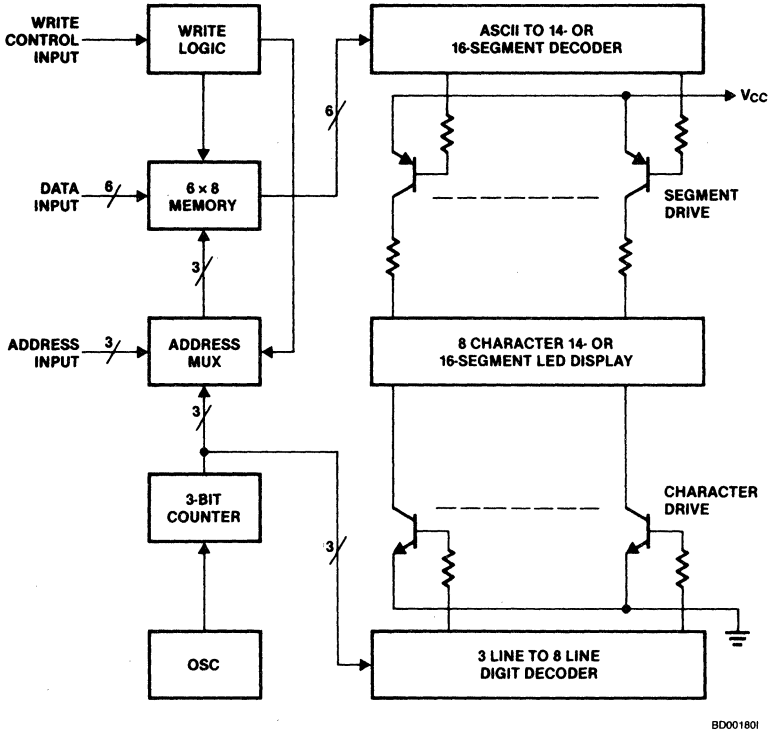

Figure 1: 8-Character Alphanumeric LED Display System (Discrete Design)

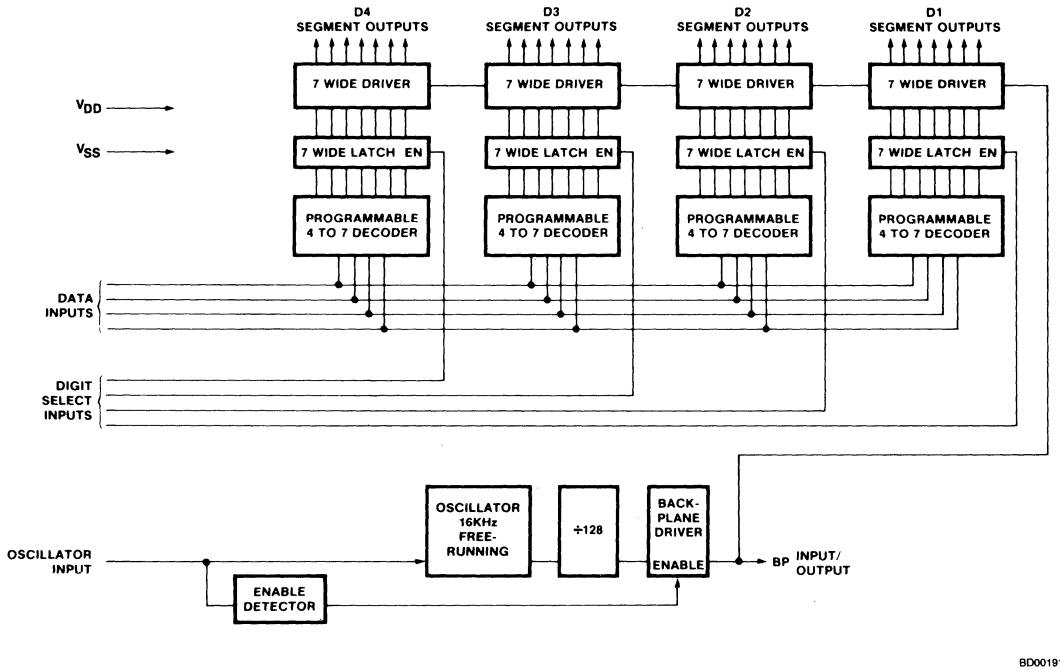

Figure 3: Functional Diagram of ICM7211

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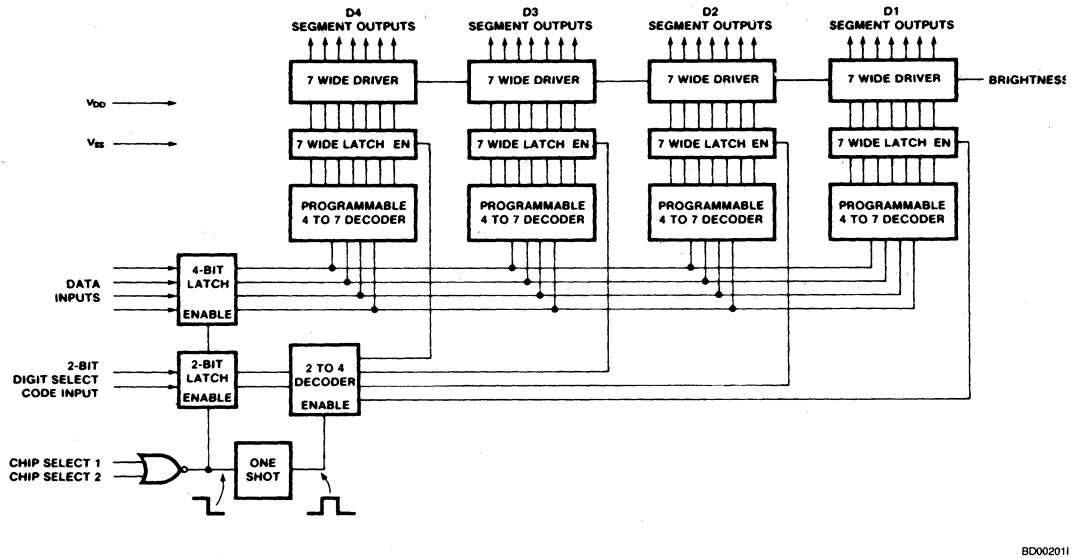


Figure 4: Functional Diagram of ICM7212M/ICM7235M

Another variation in this family of parts concerns the display font. The 4 line binary input data is decoded to 7-segment format in a mask programmable ROM, allowing any pattern to be constructed, and if desired separate decodes can be arranged for each digit. Two standard patterns are provided, as shown in Table 1. The hexadecimal code is widely used in microprocessor and other binary digital systems, while "Code B" is popular in instruments and equipment where certain test and warning messages can be provided readily. Both provide standard BCD decoding for numerals.

Some typical applications of these devices are shown in the next few figures. Figure 5 shows the ICM7211 interfaced to the ICL7135, a new single chip 4½-digit A/D converter. This device provides a multiplexed BCD output, together with polarity and overrange information. The circuit shown uses a CD4054 to drive the half digit, polarity, and overrange flags. A similar circuit for driving VF displays is shown in Figure 6, using the ICM7235. Brightness control is achieved by pulsed duty cycle using a CMOS 7555 timer on the ON/$\overline{\text{OFF}}$ input. The identical circuit (with a lower display voltage) can be used with common cathode LEDs, while substituting an ICM7212 will allow the use of common anode LEDs.

Table 1. Output Codes for 7-Segment Displays

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

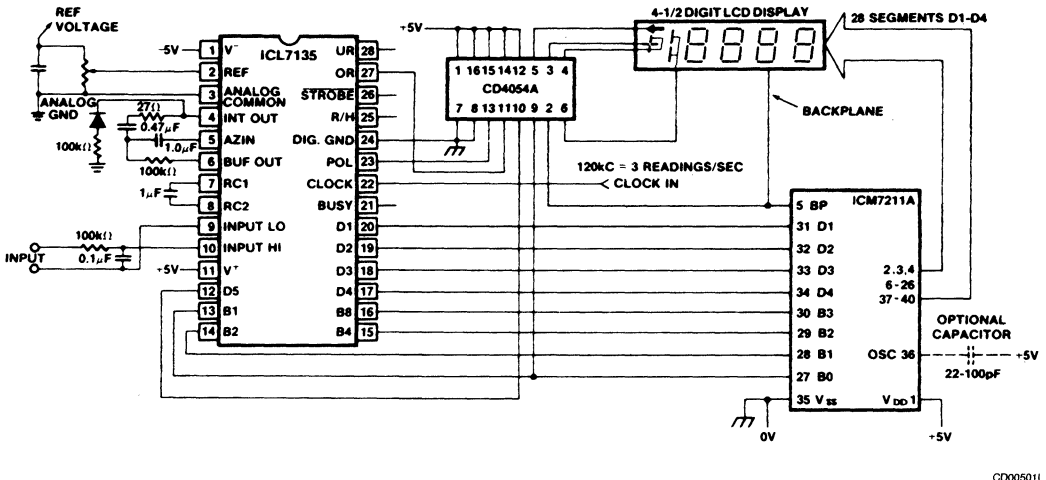


Figure 5: 4½-Digit A/D Converter with LCD Display

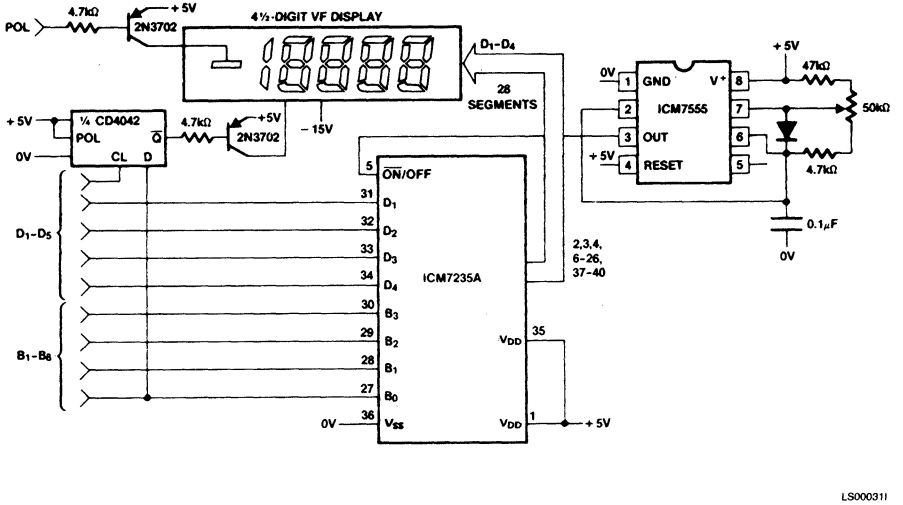


Figure 6: Vacuum Fluorescent Display Driver

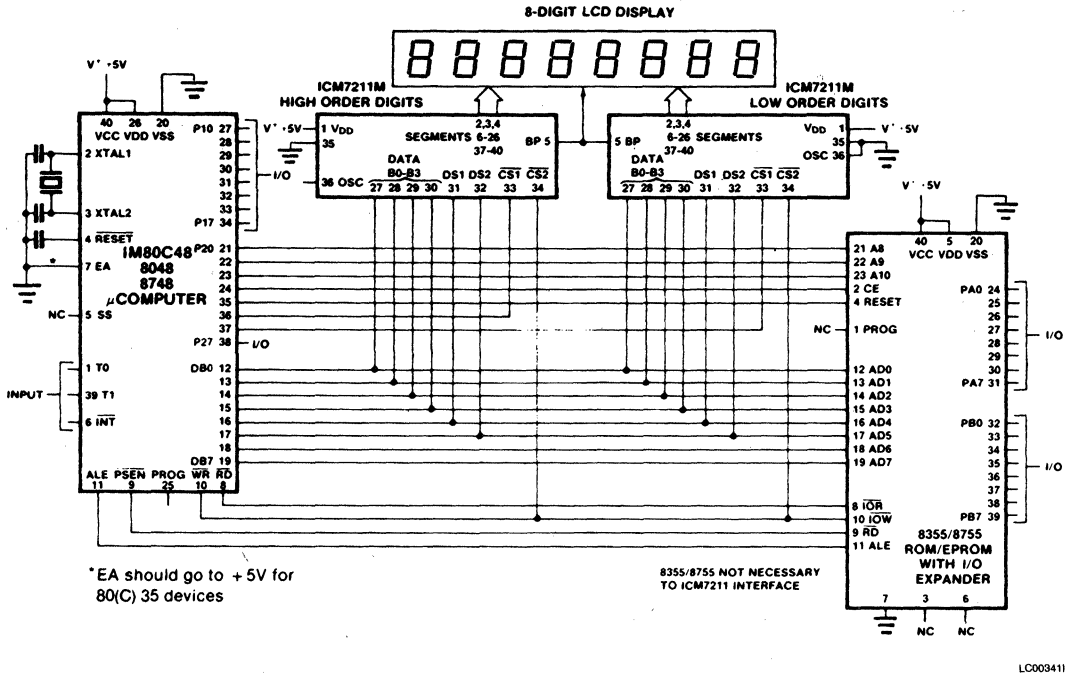


Figure 7: 8-Digit LCD Microcomputer Display

Figure 7 shows a pair of ICM7211M devices set up on an 8048 bus and accessed by port lines to form an 8-digit LCD display for a microcomputer based system. In this arrangement, any digit can be changed independently from the others and the display used for system values in decimal or hexadecimal notation. The lines B_0-B_3 are the data input lines of the display drivers; data on these lines is decoded from BCD to 7-segment format when the chip select ($\overline{CS}_1$ and $\overline{CS}_2$) conditions are met for that device. The digit to be written is determined by the digit select lines, DS_1 and DS_2. The 56 segment drive lines from the two ICM7211s are synchronized by use of the OSC INPUT (pin 36) on the righthand ICM7211. When this pin is tied low, the backplane output (pin 5) is transformed into an input and can be driven by the backplane output of the lefthand ICM7211. In this way a single 8-digit LCD display with one backplane connection can be driven by two LCD display drivers.

A similar interface can easily be designed for MCS-80/85/86 systems and the Motorola MC680X and MOS Technology/Rockwell MCS650X devices. Although the LCD devices are shown, the same arrangement can also be used with the ICM7212M and ICM7235M.

The ICM7211, 7212 and 7235 display drivers are directly related to a family of counter/display drivers, the ICM7224, 7225, and 7236. These devices are 4½-digit counters that directly drive LCD, LED or VF displays. They handle counting rates as high as 25MHz, display results up to 19999, and are easily cascadable to form higher resolution counters. Evaluation kits for these counters and display drivers, and the ICL7135 A/D converter, are available from Intersil.

MULTIPLEXED LED DISPLAYS

LEDs can be multiplexed quite easily, and the ICM7218 will run 8 digits of 7 segments plus decimal point. The advantage of multiplexing is immediately apparent, as most versions of this device require only 28 pins, compared to 40 for the devices just covered, and they drive twice as many digits. Versions are available to operate common cathode and common anode type displays. A further division is made between devices where the basic access mode is serial, i.e., each digit location must be loaded in sequence, and those where digit locations are individually addressable. The serial access devices have latches to control certain operating modes, whereas the random access parts select these via full-time control pins. These modes include a "shutdown" operation where the digit and segment drivers are turned off, and the multiplex scan oscillator is halted. Data can continue to be loaded, but the power drain is typically only 10μA. Other operating modes control the data decoding function. The 8 data input lines can be used to directly control the segment and decimal point outputs, without decoding at all (the decimal point input is inverted). Alternatively, the lowest 4 data bits can be decoded according to either of the hexadecimal and "Code B" fonts shown in Table 1. The device provides interdigit blanking for about 10μs between digit drive times to avoid ghosting. The peak drive current for the common anode device is about

40mA per segment, averaging to 5mA with a 12.2% duty cycle. The common cathode drivers offer about half the current, suitable for the smaller displays of this type.

A 16-digit microprocessor display application is shown in Figure 8 using two ICM7218C devices connected to the data and address lines of an 8048 microcomputer. Note that the individual 7-segment displays are interleaved to simplify the addressing of the two driver chips. The 3 digit address lines of each ICM7218 are tied to the same 3 address lines of the 8048. When data appears on the data output lines of the 8048 and the write command is given, the display drivers will be addressed simultaneously and the 2 digits addressed by DA_0, DA_1, and DA_2 will be written simultaneously. The decimal point inputs come from the 8048 address lines. The code selected by pin 9 of the ICM7218 is hexadecimal.

Independent addressing and the no-decode mode of the ICM7218A, B, and E allow them to be used in non-numeric applications. Since each LED segment is independently addressable by way of 8 data input lines and 8 segments per digit (7 + decimal point), it is possible to use them as LED system status panel drivers or as 64-segment bar graph drivers. Two LED system status panel examples are shown in Figure 9, one with 32 channels of red and green LEDs, and one with 21 channels of red, yellow, and green LEDs. Each of these status panels can be driven by one ICM7218 display driver with individual LEDs arranged in groups of 8 for each of the 8 digit drive outputs.

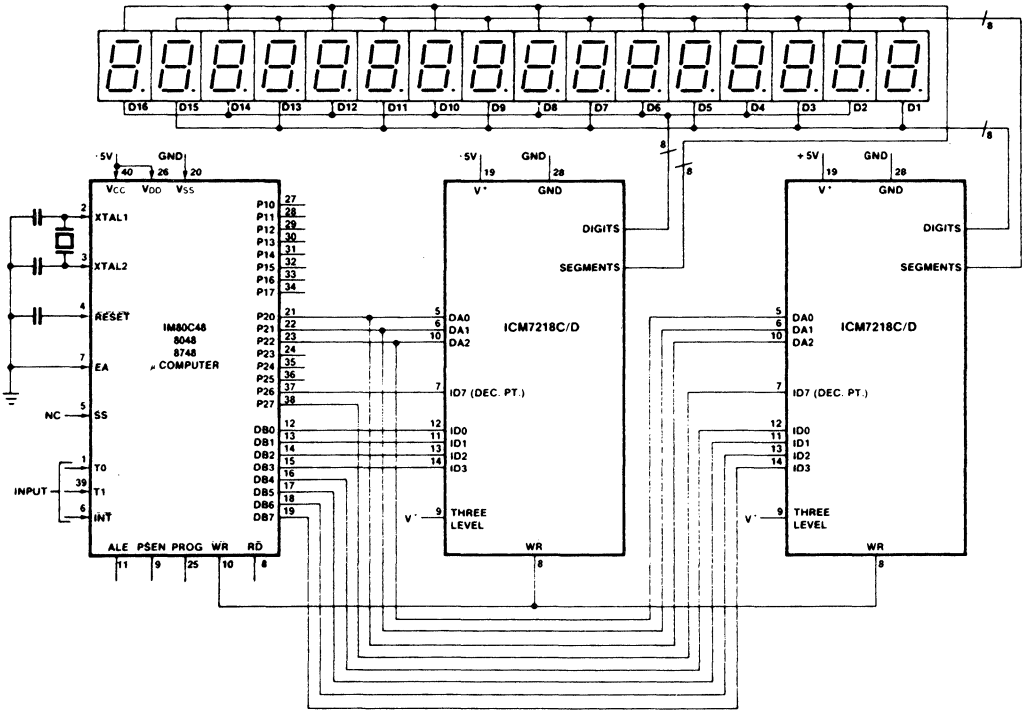


Figure 8: 16-Digit LED Microcomputer Display

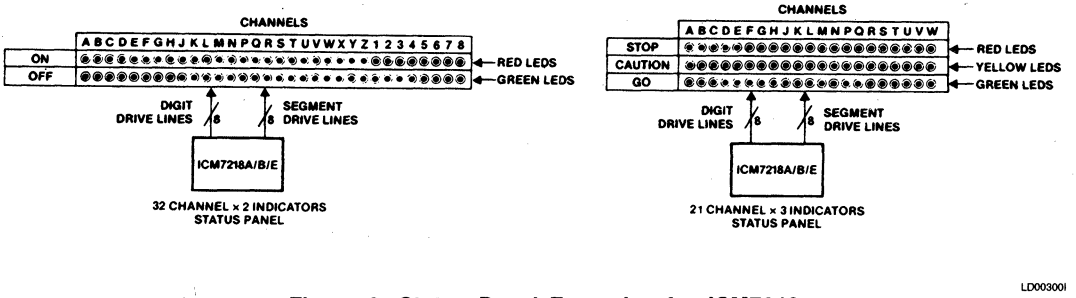


Figure 9: Status Panel Examples for ICM7218

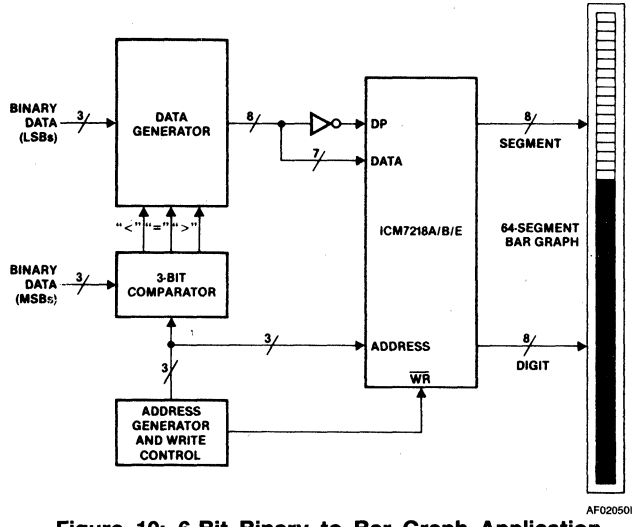


Figure 10: 6-Bit Binary to Bar Graph Application

Figure 10 shows a functional diagram of an ICM7218E used in a 6-bit binary to 64-segment bar graph application. The write control block generates the write command and address of the group of 8 segments to be written. The address is compared with the 3 MSBs of the input binary value. If the address to be written is less than the 3 MSBs, then the data is to be all "ones", turning on those 8 segments corresponding to the 3 MSBs. If the address is greater than the 3 MSBs, the data is to be all "zeros". When the address is equal to the 3 MSBs, the data generator uses the 3 LSBs of the input word to determine the point at which the bar graph changes from on to off. The data is found by:

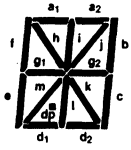
$$\text{data value} = (2n) - 1$$

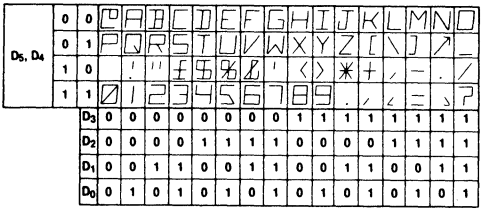
where n is the 3-bit LSB value (0 to 8).

Note that the data sent to the decimal point input (pin 8) needs to be inverted.

Alphanumeric LED display systems have recently been simplified in the same way that the numeric-only LED display system has been simplified by the ICM7218 family (Figures 1 and 2). A pair of integrated circuits dedicated to 14- and 16-segment alphanumeric LED displays have been developed — the ICM7243A and B. These devices accept a 6-bit parallel ASCII code, decode it, and drive the appropriate segments of an 8-character common cathode display. The mask programmable character sets and corresponding ASCII codes are shown in Table 2 for the 14- and 16-segment versions.

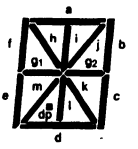
Table 2. Output Fonts for Alphanumeric LED Displays

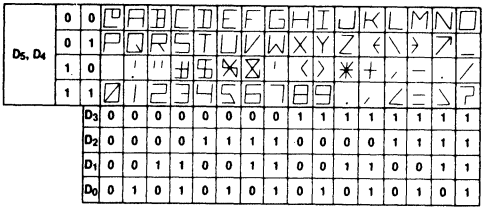




LC003601

ICM7243A — 16-Segment Character Font with Decimal Point

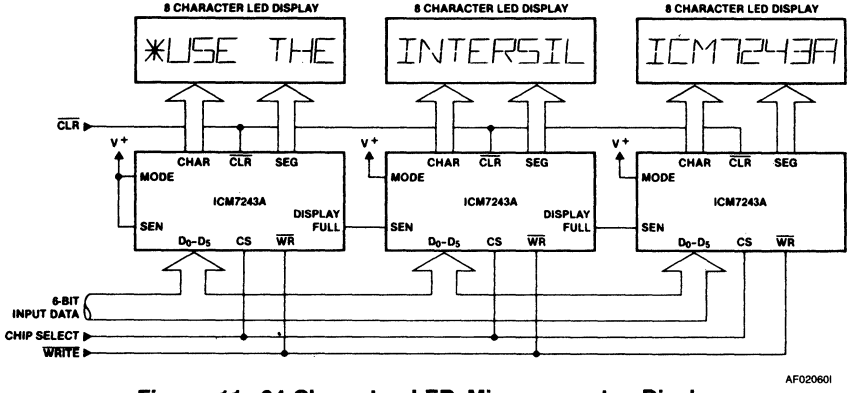




NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

LC003701

ICM7243B — 14-Segment Character Font with Decimal Point



AF020601

Figure 11: 24-Character LED Microcomputer Display

The ICM7243 has 2 input data modes. The Random Access (RA) mode allows independent addressing of characters by way of 3 digit address lines. The RA mode writes only the character addressed. The Serial Access (SA) mode writes characters from left to right on the display without having to externally address each character. Right to left writing can be done by wiring the digits in reverse order. The OSC/$\overline{OFF}$ pin on the ICM7243 provides a shutdown mode which, when grounded, will put the display driver in a low-power mode, blanking the displays while the memory section is kept active. The DISPLAY FULL and SERIAL ENABLE lines combine to make cascading display drivers easy. An example of a 24-character LED display is shown in Figure 11. The MODE lines are all tied high to set up serial input, and DISPLAY FULL is connected to SEN of the next device to enable cascading. When CHIP SELECT is high, the $\overline{WRITE}$ line is active-low. If, however, active-high is desired, $\overline{WRITE}$ can be tied low and CHIP SELECT used as an active-high write line. The characters will be written from left to right as new ASCII data is presented to the 6-bit input bus and the $\overline{WRITE}$ command is given.

Figure 12 shows the use of the OSC/$\overline{OFF}$ pin to get the shutdown mode. In this example two ICM7243s are dedicated to the same 8 characters of the LED display. The drivers are enabled alternately, performing a message select function. When the OSC/$\overline{OFF}$ pin is brought low by the open-collector inverter, all outputs of that driver are turned off freeing its group of 8 LED characters to be driven by the other ICM7243. The display driver is turned on by allowing the OSC/$\overline{OFF}$ pin to float.

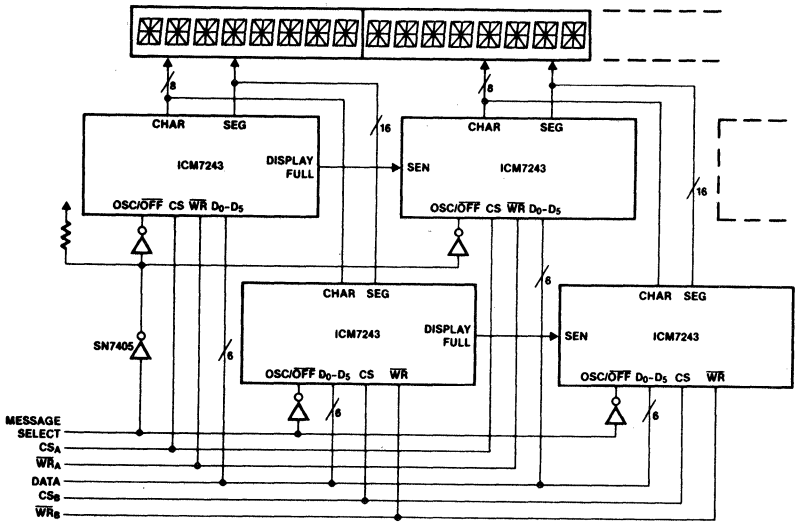
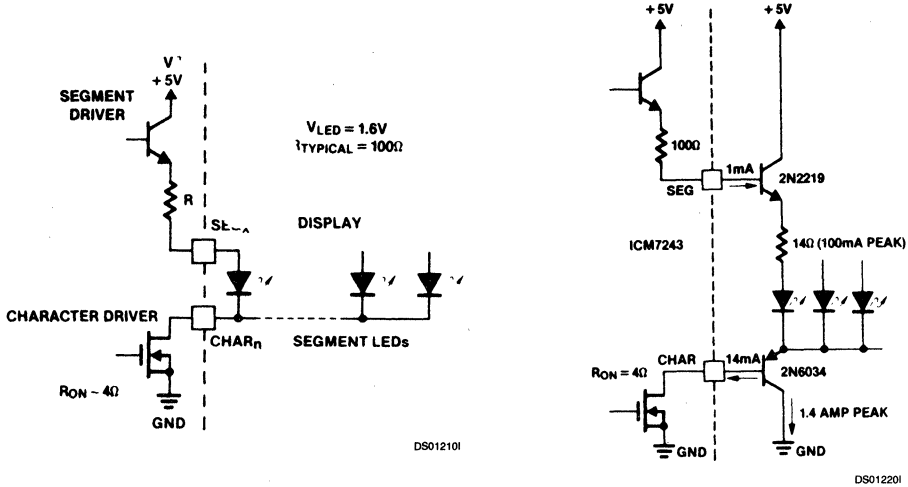


Figure 12: ICM7243 Message Select Application



Standard Display Connection

LED Current Boost Connection

Figure 13: Display Current Boost Circuit for ICM7243

The average segment current of the ICM7243 is 3mA maximum (24mA/8 digits). This is quite enough current to give good contrast to the 0.375 or 0.4 inch high displays. If larger displays are to be driven it is an easy task to add a simple transistor current boost circuit to each character and segment output. The current boost circuit shown in Figure 13 will provide an average segment current of about 12mA. This current should be sufficient to drive larger alphanumeric LED displays.

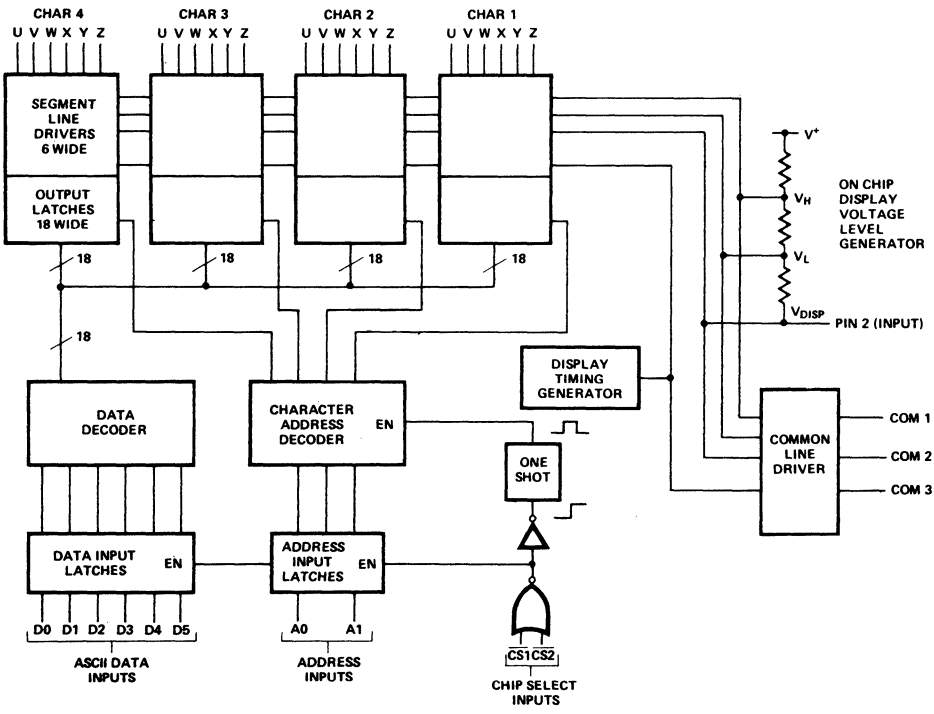


Figure 14: ICM7233 Functional Diagram

MULTIPLEXED LIQUID CRYSTAL DISPLAYS

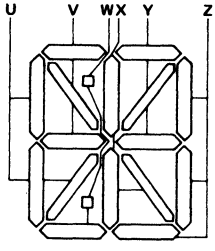
The benefits of multiplexing have been slow in coming to LCD systems, outside of a few consumer items. Much of the reason lies with the display. A reverse biased LED (or VF device) will not display anything, so part-time forward bias control is enough to control the overall result. But LCDs require an AC drive, and continuously look at the voltage between backplane and segment. Thus, multiplexing LCDs requires waveforms that rely on a threshold in the rms voltage-versus-contrast characteristics. The result is that until recently no multiplexed LCD displays were commercially available (off-the-shelf), and naturally it is hard to justify building display drivers for unavailable displays! Nevertheless, Intersil has introduced the ICM7231/32/33/34 family of Triplex Multiplexed LCD drivers, and several matching LCD displays have become available. Figure 14 shows a block diagram of the ICM7233 display driver for 4 characters of 18 segments.

The 6 data input lines are decoded into 18 segment lines according to the font shown in Table 3. These are then latched in the character location selected by the two address lines at the rising edge of one of the Chip Select inputs. The segments are arranged on 6 segment lines against 3 common (backplane) lines as shown in Figure 15. The resistive divider sets up a total of 4 voltage levels and the COMmon and SEGment lines are switched between these levels as shown in Figure 16. The resulting voltages between one segment in the display and its common backplane are shown in Figure 17. The ratio of rms voltages for ON and OFF conditions of the segment is 1.92:1 as shown. The relationship between contrast and applied voltage for a typical multiplexed LCD display is shown in Figure 18, and indicates that the viewing angle for adequate contrast at this level is satisfactory. Figure 19 shows the variation with temperature of the voltage margins (expressed as peak voltage) above and below which the display will begin to malfunction.

Table 3. 6-Bit ASCII 18-Segment Font (ICM7233/34)

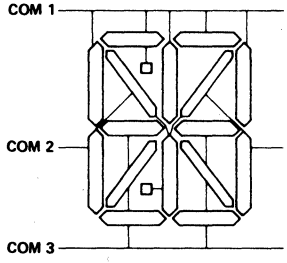
CODE INPUT				DISPLAY OUTPUT D5, D4			
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1
0	0	0	0	@	P		0
0	0	0	1	A	Q	!	1
0	0	1	0	B	R	"	2
0	0	1	1	C	S	#	3
0	1	0	0	D	T	$	4
0	1	0	1	E	U	%	5
0	1	1	0	F	V	&	6
0	1	1	1	G	W	'	7
1	0	0	0	H	X	(	8
1	0	0	1	I	Y	)	9
1	0	1	0	J	Z	*	:
1	0	1	1	K	[	+	;
1	1	0	0	L	\	,	<
1	1	0	1	M	]	-	=
1	1	1	0	N	↑	.	>
1	1	1	1	O	←	/	?

TB00010I



SEGMENT LINE CONNECTIONS

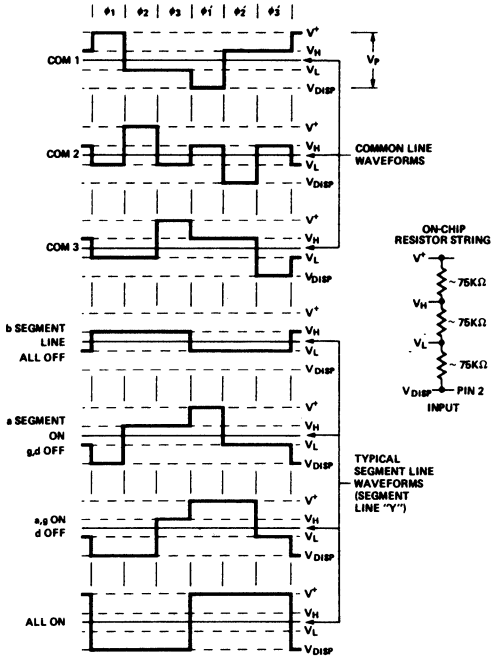
CD00510I



COMMON LINE CONNECTIONS

CD00520I

Figure 15: ICM7233 and ICM7234 Segment Pattern 18-Segment Alphanumeric



NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.

$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.

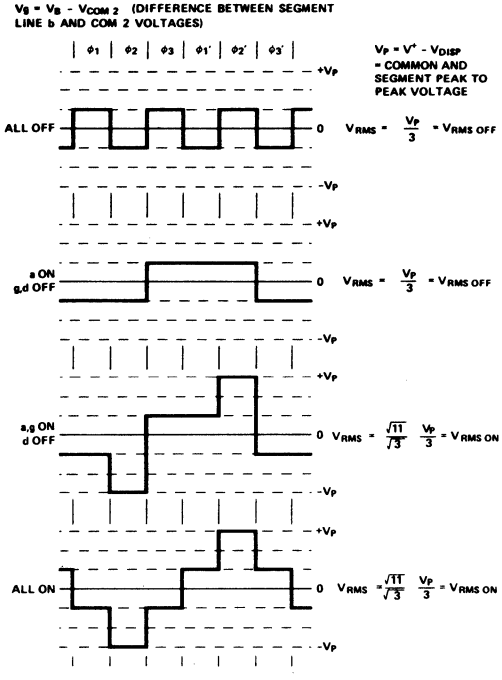
COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

WF00890I

Figure 16: Display Voltage Waveforms



NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.

$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

WF00900I

Figure 17: Voltage Waveforms on Segment

6

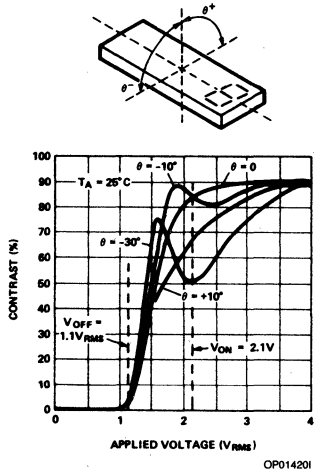


Figure 18: Contrast vs Applied rms Voltage

The ICM7231 uses 4 of the input data lines for binary display data, and 2 more for annunciator inputs. The segment latches are divided into 8 groups (digits) of 9 (7 segments plus 2 annunciators) with 1 extra address input provided for selection. Several different versions offer hexadecimal or Code B fonts (Table 1) and different annunciator connections (see Figure 20 for patterns).

The serial input versions, the ICM7232 and ICM7234, exchange the 6 data input lines for 6 more SEGment lines, allowing 2 digits or one character extra per driver. The Address and Chip Select Lines are replaced by 4 serial input control lines (Figure 21) which clock data and address information into a shift register before writing it into the display. A DATA ACCEPTED flag output indicates when enough data has been entered into the shift register, and enables the writing operation. $\overline{\text{WR}}$ite pulses also reset the shift register and DATA ACCEPTED flag. The two annunciator locations need not be filled, and clocking more data into the shift register than it can accept causes an automatic reset. This minimizes the chance of displaying incorrect information.

The serial input format on the ICM7234 is similar (Figure 22) except that all bits need to be loaded into the shift register to determine the character code and location. Data to be written into non-existent addresses is ignored.

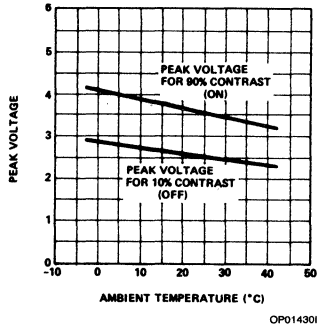


Figure 19: Temperature Dependence of LC Threshold

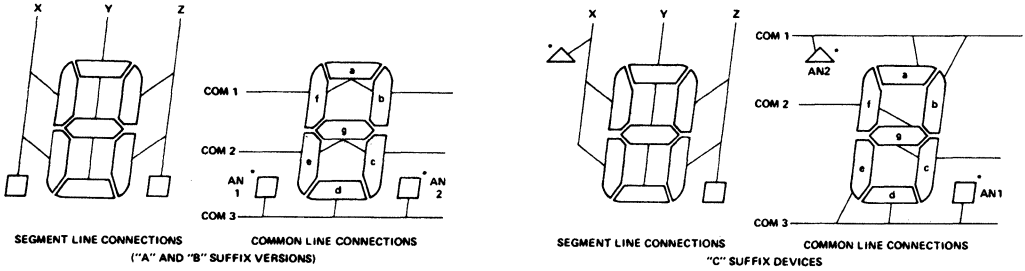
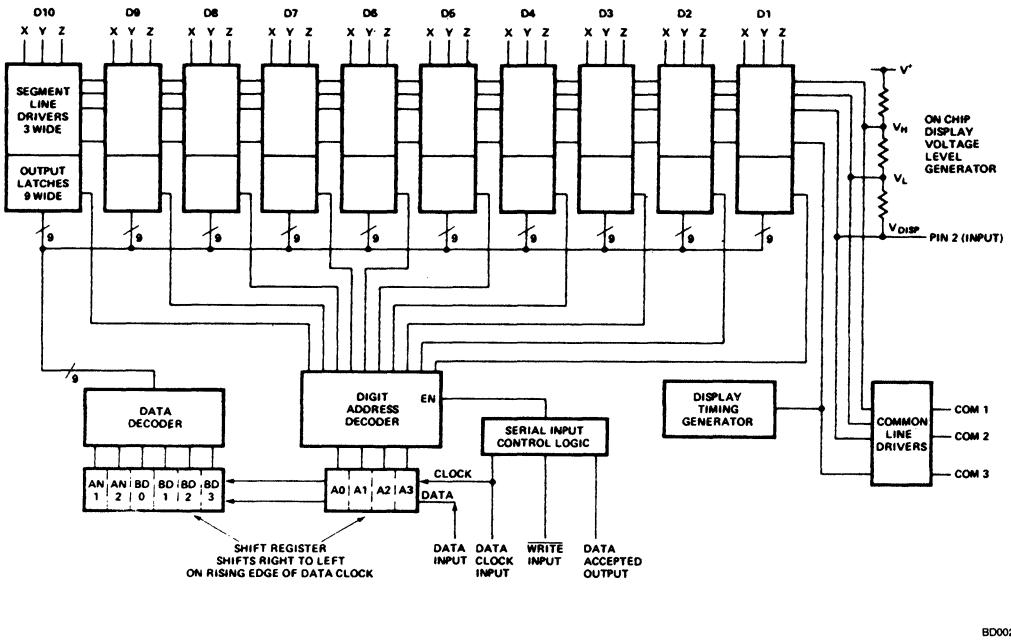
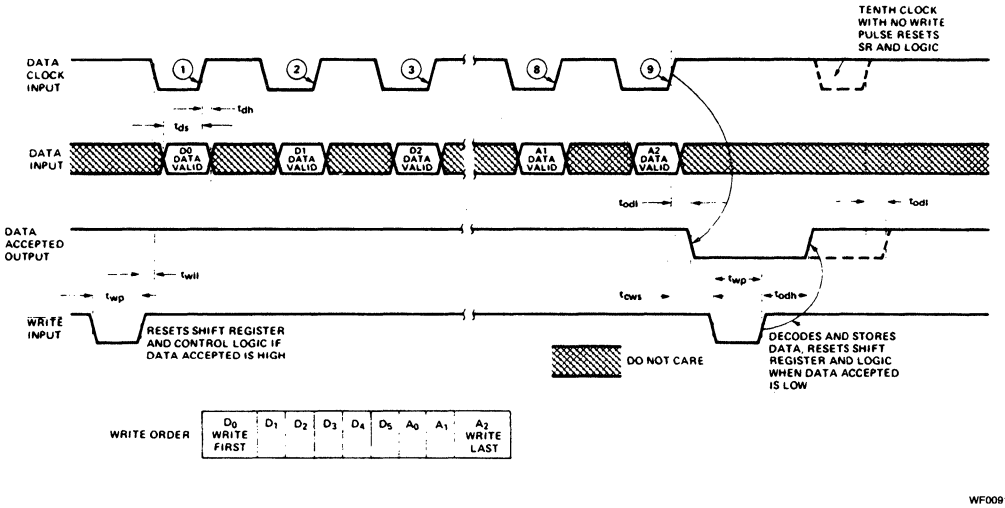


Figure 20: ICM7231 and ICM7232 Display Patterns



BD002201

Figure 21: ICM7232 Functional Diagram



WF009101

Figure 22: ICM7234 One Character Input Timing Diagram

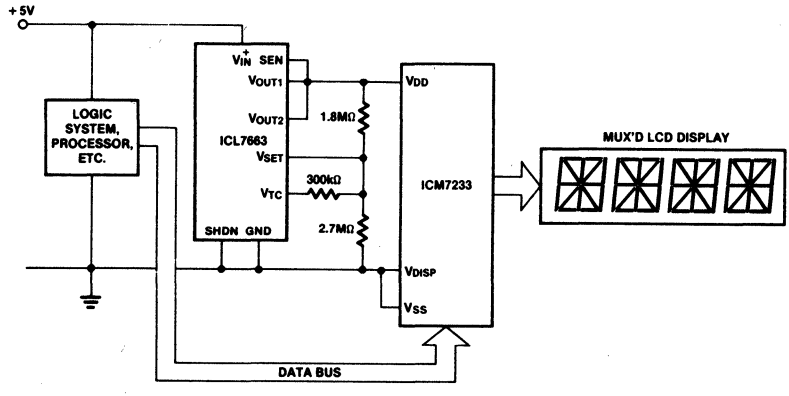


Figure 23: Driving a Multiplexed LCD Display

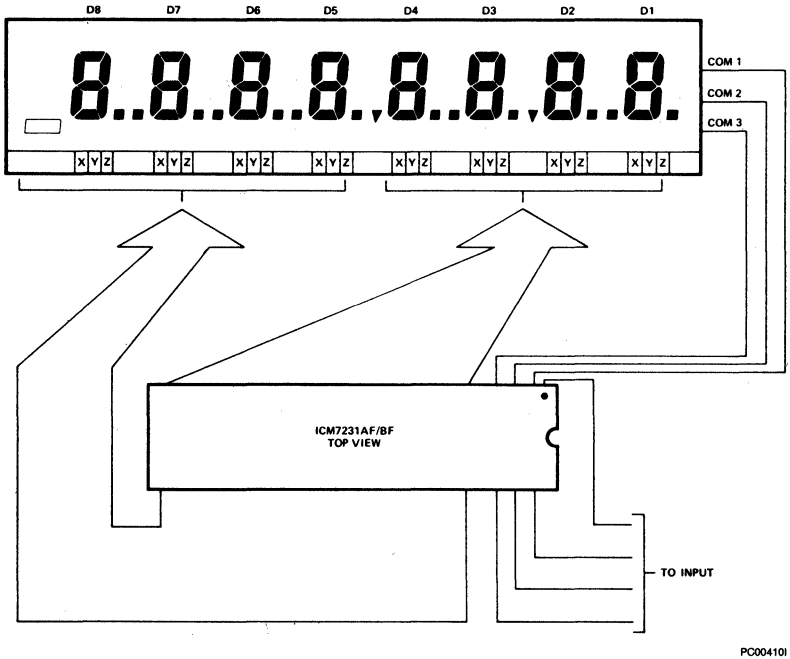


Figure 24: Pin Orientation and Display Connections

The initial set-up of the optimum display voltage, and its variation with temperature, shown in Figure 19, is accommodated in the ICM7231/32/33/34 devices by separating the display driving voltage from the logic voltage, and also allowing the input signals to exceed the logic supply in one direction. The display voltage can be controlled by the use of the ICL7663, as shown in Figure 23.

The device pinouts are arranged to simplify the board layout of display systems. The basic layout for the ICM7231 and a corresponding display, for example, is shown in Figure 24, and the others are similar.

The convenient interface with microprocessors is indicated in Figure 25. Here the 8-bit bus of an MCS-48 microcomputer is used to provide the 6 data bits and the 2 address

bits for writing to a series of 4-character drivers, the ICM7233. Port lines select specific drivers via one of the CHIP SELECT lines, while the other provides WR cycle timing. A similar arrangement can be used with any microprocessor that provides a WR line, such as the MCS-80/85. A slightly more complex interface to an MC680X processor is shown in Figure 26. Here, address lines are used for character and chip selection, enabled by a port line from another peripheral chip. Note that in both these circuits, and any other multiple chip systems of this kind, the 3 common lines must be separated for each group of digits or characters. Several displays organized in this manner are now available from some vendors (notably Epson), and more are expected soon.

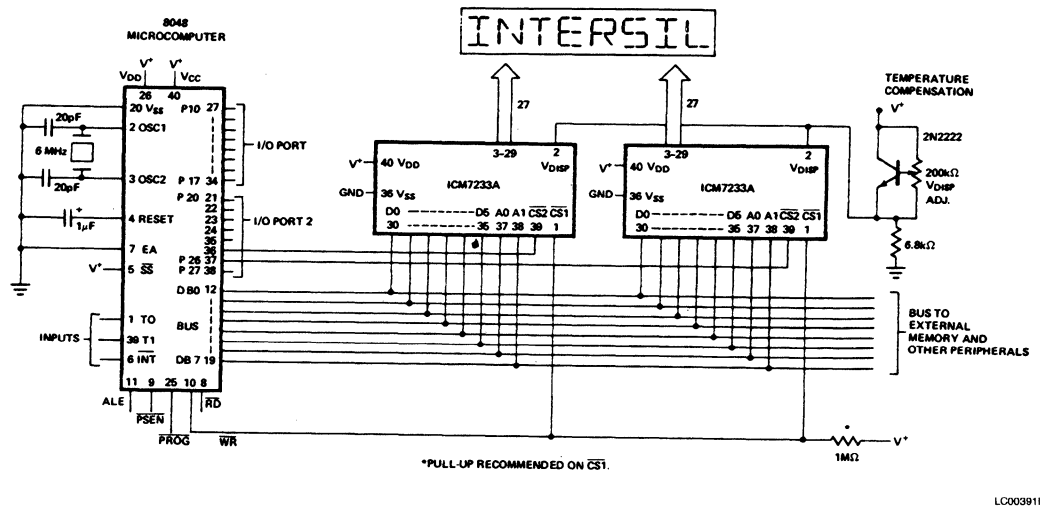


Figure 25: 8048/IM80C40 Microcomputer with 8-Character 16-Segment Full ASCII Triplex Liquid Crystal Display

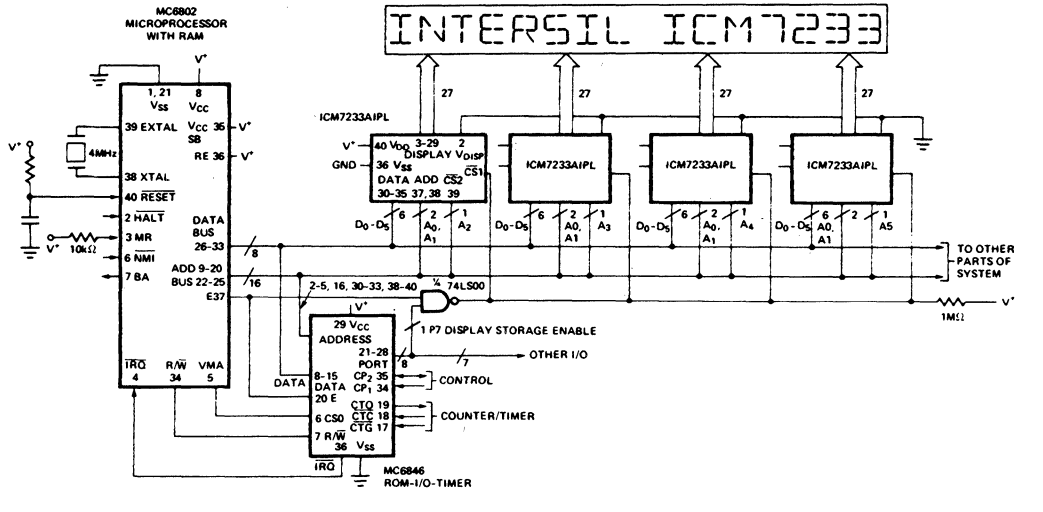


Figure 26: MC6502 Microprocessor with 16-Character 16-Segment Full ASCII Liquid Crystal Display

An example of the serial interface connection can be seen in Figure 27 where a COPS420C microcomputer has been fitted with a 10-character alphanumeric LCD display. The display and drivers can easily be located at some remote point in the system and communicate with the microcomputer via the 4 data lines, serial data, serial clock, WRITE 1, and WRITE 2.

The microcomputer controls which character is being written by sending the appropriate write pulse and by sending the digit address bits. The last 3 bits in the string of 9 sent to the ICM7234s are the digit address bits. Since the digit addressing is sent with each data word, the display may be written in random access mode.

SUMMARY

The display drivers mentioned here are examples of how CMOS technology is being used to simplify the design of numeric and alphanumeric display systems. The method of driving (direct, multiplex, triplex) is not usually as important to a system designer as the questions regarding the type of display (LCD, LED, Vacuum Fluorescent, Gas Discharge), the size of display, and the number of digits or characters. The actual construction of display systems is easier now that there is a wide selection of decoder/drivers from which to choose.

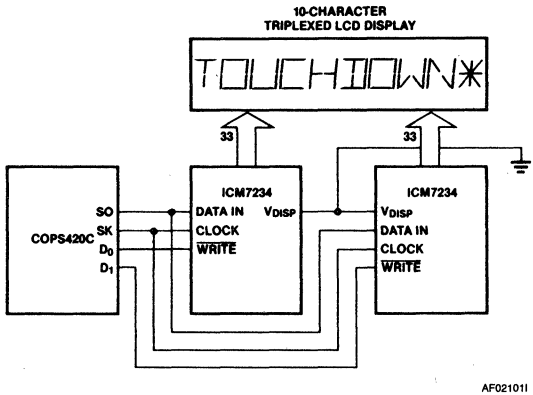
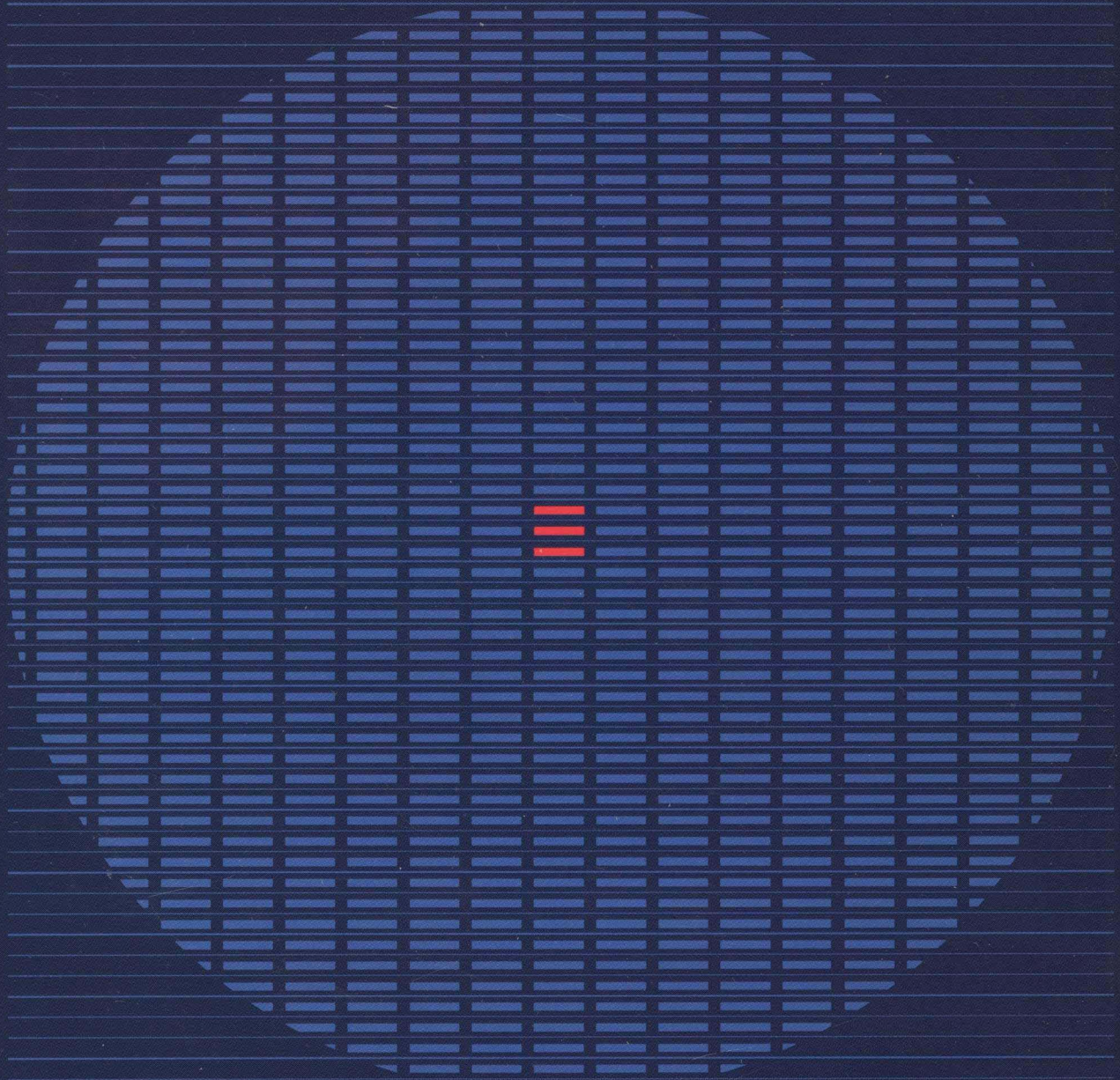


Figure 27: 10-Character Alphanumeric Triplexed LCD Display with Serial Microcomputer Interface

GE stands for Great Engineering

Intersil, Inc.
10600 Ridgeview Court
Cupertino, CA 95014



INTERSIL