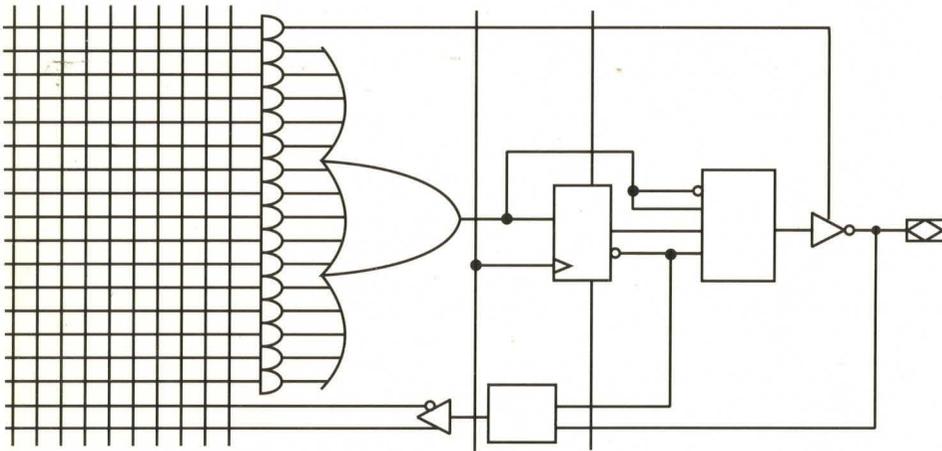


1992

GAL Data Book



GAL PRODUCT INDEX**Commercial Grade Devices**

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A/B	20	7.5, 10, 15, 25	55, 90, 115	E ² CMOS 20-Pin PAL Superset	2-1
GAL20V8A/B	24	7.5, 10, 15, 25	55, 90, 115	E ² CMOS 24-Pin PAL Superset	2-25
GAL18V10	20	15, 20	115	E ² CMOS Universal PLD	2-49
GAL22V10/B	24	7.5, 10, 15, 25	90, 130, 140	E ² CMOS Universal PLD	2-63
GAL26CV12/B	28	10, 15, 20	130	E ² CMOS Universal PLD	2-81
GAL20XV10B	24	10, 15, 20	90	E ² CMOS Exclusive-OR PLD	2-101
GAL20RA10	24	12, 15, 20, 30	100	E ² CMOS Asynchronous PLD	2-117
GAL6002B	24	15, 20	135	E ² CMOS FPLA	2-131
GAL6001	24	30, 35	150	E ² CMOS FPLA	2-147

Industrial Grade Devices

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
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GAL20V8A/B	24	10, 15, 20, 25	65, 130	E ² CMOS 24-Pin PAL Superset	2-25
GAL18V10	20	20	125	E ² CMOS Universal PLD	2-49
GAL22V10B	24	15, 20, 25	150	E ² CMOS Universal PLD	2-63
GAL26CV12/B	28	15, 20	150	E ² CMOS Universal PLD	2-81
GAL20XV10B	24	15, 20	110	E ² CMOS Exclusive-OR PLD	2-101
GAL20RA10	24	20	120	E ² CMOS Asynchronous PLD	2-117

MIL-STD-883 Grade Devices

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A/B	20	10, 15, 20, 25, 30	65, 130	E ² CMOS 20-Pin PAL Superset	3-5
GAL20V8A	24	15, 20, 25, 30	65, 130	E ² CMOS 24-Pin PAL Superset	3-13
GAL22V10/B	24	15, 20, 25, 30	150	E ² CMOS Universal PLD	3-19
GAL26CV12	28	20, 25	160	E ² CMOS Universal PLD	3-27
GAL20RA10	24	20, 25	120	E ² CMOS Asynchronous PLD	3-33

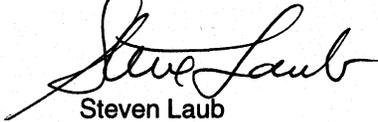
Lattice appreciates your interest in our industry leading GAL® product line.

Our 1992 GAL Data Book contains the world's highest performance CMOS programmable logic solutions, as well as innovative new device architectures. The GAL product line, offered in low power reprogrammable E²CMOS technology, obsoletes virtually all PAL® parts.

In addition, Lattice offers the new pLSI and ispLSI product families, the world's highest performance and most flexible high-density PLD solution. Please contact a Lattice representative to obtain our pLSI and ispLSI Data Book.

We look forward to satisfying all of your programmable logic requirements.

Sincerely,

A handwritten signature in black ink that reads "Steve Laub". The signature is written in a cursive style with a large, prominent "S" at the beginning.

Steven Laub
Vice President and General Manager

GAL Data Book

1992





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Products discussed in this literature are covered by U.S. Patents No. 4,761,768, 4,766,569, 4,833,646, 4,852,044, 4,855,954, 4,879,688, 4,887,239 and 4,896,296 issued to Lattice Semiconductor Corporation, and by U.S. and foreign patents pending.

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Introduction to Generic Array Logic

INTRODUCTION

Lattice Semiconductor, located in Hillsboro, Oregon, was founded in 1983 to design, develop and manufacture high-performance semiconductor components. At Lattice, we believe that technological evolution can be accelerated through the continued development of higher-speed and architecturally superior products.

GAL devices are ideal for four important reasons:

1. GAL devices have inherently superior quality and reliability.
2. GAL devices can directly replace PAL devices in nearly every application.
3. GAL devices have the low power consumption of CMOS, one-fourth to one-half that of bipolar devices.
4. GAL devices utilize Output Logic Macrocells (OLMCs), which allow the user to configure outputs as needed.

THE GAL CONCEPT

E²CMOS — THE IDEAL TECHNOLOGY

Of the three major technologies available for producing PLDs, the technology of choice is clearly E²CMOS. E²CMOS offers 100% testability, high quality, high speed, low power, and instant erasure.

TESTABILITY

The biggest advantage of E²CMOS over competing technologies is its inherent testability. Capitalizing on very fast (100ms) erase times, Lattice repeatedly patterns and erases all devices during the manufacturing process. Lattice tests each GAL device for AC, DC, and functional characteristics. The result is guaranteed 100% programming and functional yields.

LOW POWER

Another advantage of E²CMOS technology is the low power consumption of CMOS. CMOS provides users the immediate benefit of decreased system power requirements allowing for higher reliability and cooler running systems. Low power CMOS technology also permits circuit designs of much higher functional density, because of lower junction temperatures and power requirements on chip. The user benefits because higher functional density means further reduction of chip count and smaller boards in the system.

HIGH SPEED

Also advantageous is the very high speed attainable with Lattice's state-of-the-art E²CMOS process. Lattice GAL devices are as fast or faster than bipolar and UVCMS PLDs.

PROTOTYPING AND ERROR RECOVERY

Finally, E²CMOS gives the user instant erasability with no additional handling or special packages necessary. This provides ideal products for prototyping because designs can be revised instantly, with no waste and no waiting. On the manufacturing floor instant erasability can also be a big advantage for dealing with pattern changes or error recovery. If a GAL device is accidentally programmed to the wrong pattern, simply reprogram the device. No other technology offers this advantage.

Introduction to Generic Array Logic

A LOOK AT OTHER TECHNOLOGIES

Here, the technologies that compete with E²CMOS — bipolar and U²CMOS — are compared with the E²CMOS approach.

BIPOLAR

Bipolar fuse-link technology was the first available for programmable logic devices. Although it offers high speed, it is saddled with high power dissipation. High power dissipation increases your system power supply and cooling requirements, and limits the functional density of bipolar devices.

Another weakness of this technology is the one-time-programmable fuses. Complete testing of bipolar PLDs is impossible because the fuse array cannot be tested before programming. Bipolar PLD manufacturers must rely on complex schemes using test rows and columns to simulate and correlate their device's performance. The result is programming failures at the customer location. Any misprogrammed devices due to mistakes during prototyping or errors on the production floor must be discarded because bipolar PLDs cannot be reprogrammed.

U²CMOS

U²CMOS addresses many weaknesses of the bipolar approach but introduces many shortcomings of its own. This technology requires less power and is reprogrammable, but reprogrammability comes at the expense of slower speeds.

Testability is increased over bipolar since the "fuse" array can be programmed and tested by the manufacturer. The problem here is the long (20 minutes) erase times coupled with the requirement of exposing the devices to ultraviolet light for erasing. This becomes a very expensive step in the manufacturing process. Because of the time involved, patterning and erasing is performed only once — a compromised rather than complete functional test.

Additionally, the devices must be housed in expensive windowed packages to allow users to erase them. Again, programming these devices is time-consuming and cumbersome due to the 20-minute UV exposure required to erase them. As a cost-cutting measure, U²CMOS PLD manufacturers offer their devices in windowless packages. Although windowless packages are less expensive, they prevent the devices from being completely tested or reprogrammed. These factors significantly detract from the desirability of this technology.

THE GAL ADVANTAGE

GAL devices are ideal programmable logic devices because, as the name implies, they are architecturally generic. Lattice has employed the macrocell approach, which allows users to define the architecture and functionality of each output. The key benefit to the user is the freedom from being restricted to any specific architecture. This is advantageous at both the manufacturing level and the design level.

DESIGN ADVANTAGES

Early programmable logic devices gave the user the ability to specify a function, but limited them to specific, predetermined output architectures. Comparing the GAL device with fixed-architecture programmable logic devices is much like comparing these same fixed PLDs with SSI/MSI devices. The GAL family is the next generation in simplified system design. The user does not have to search for the architecture that best suits a particular design. Instead, the GAL family's generic architecture lets him configure as he goes.

MANUFACTURING ADVANTAGES

The one-device-does-all approach greatly simplifies the manufacturing flow. Carrying one generic architecture GAL device type in inventory versus having to monitor and maintain many different device types, saves money and minimizes paperwork. The manufacturing flow is much smoother because the handling process is greatly simplified. A generic architecture GAL device also reduces the risk of running out of inventory and halting production, which can be very expensive. Reduced chance of obsolete inventory and easier QA tracking are additional benefits of the generic architecture.

THE IDEAL PACKAGE

Programmable logic devices are ideal for designing today's systems. Lattice Semiconductor believes that the ideal design approach should be supported with the ideal products. It was on this premise that GAL devices were invented. The ideal device—with a generic architecture—fabricated with the ideal process technology, E²CMOS.

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Section 2: GAL Datasheets

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FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 7.5 ns Maximum Propagation Delay
 - F_{max} = 100 MHz
 - 5 ns Maximum from Clock Input to Data Output
 - TTL Compatible 24 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8B)**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 20-pin PAL[®] Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

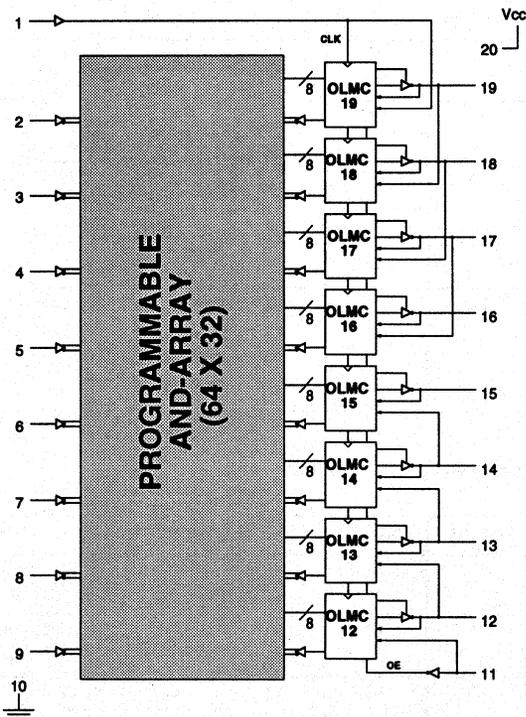
DESCRIPTION

The GAL16V8B, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

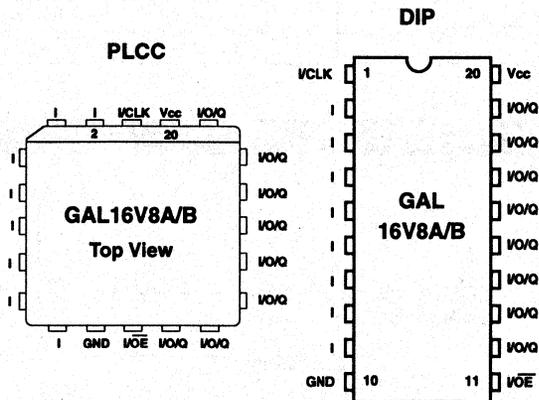
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8A/B are the PAL architectures listed in the table of the macrocell description section. GAL16V8A/B devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL[®] products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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Specifications **GAL16V8B** **GAL16V8A**

GAL16V8A/B ORDERING INFORMATION

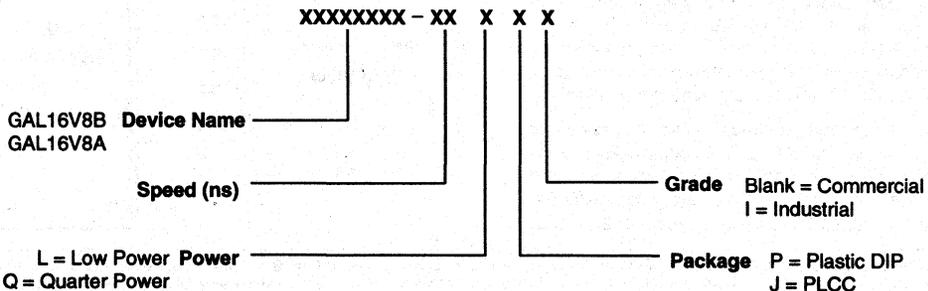
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	115	GAL16V8B-7LP	20-Pin Plastic DIP
			115	GAL16V8B-7LJ	20-Lead PLCC
10	10	7	115	GAL16V8B-10LP	20-Pin Plastic DIP
			115	GAL16V8B-10LJ	20-Lead PLCC
15	12	10	55	GAL16V8A-15QP	20-Pin Plastic DIP
			55	GAL16V8A-15QJ	20-Lead PLCC
			115	GAL16V8A-15LP	20-Pin Plastic DIP
			115	GAL16V8A-15LJ	20-Lead PLCC
25	15	12	55	GAL16V8A-25QP	20-Pin Plastic DIP
			55	GAL16V8A-25QJ	20-Lead PLCC
			90	GAL16V8A-25LP	20-Pin Plastic DIP
			90	GAL16V8A-25LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL16V8B-10LPI	20-Pin Plastic DIP
			130	GAL16V8B-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8B-15LPI	20-Pin Plastic DIP
			130	GAL16V8B-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8A-20QPI	20-Pin Plastic DIP
			65	GAL16V8A-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8A-25QPI	20-Pin Plastic DIP
			65	GAL16V8A-25QJI	20-Lead PLCC
			130	GAL16V8A-25LPI	20-Pin Plastic DIP
			130	GAL16V8A-25LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8A/B. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8A and GAL16V8B can emulate. It also shows the OLMC mode under which the GAL16V8A/B emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8A/B	GAL16V8A/B Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/IC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered" ¹	"Complex" ¹	"Simple" ¹	GAL16V8A
PLDesigner	P16V8R ²	P16V8C ²	P16V8C ²	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS ³	G16V8

1) Used with Configuration keyword.
 2) Prior to Version 2.0 support.
 3) Supported on Version 1.20 or later.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

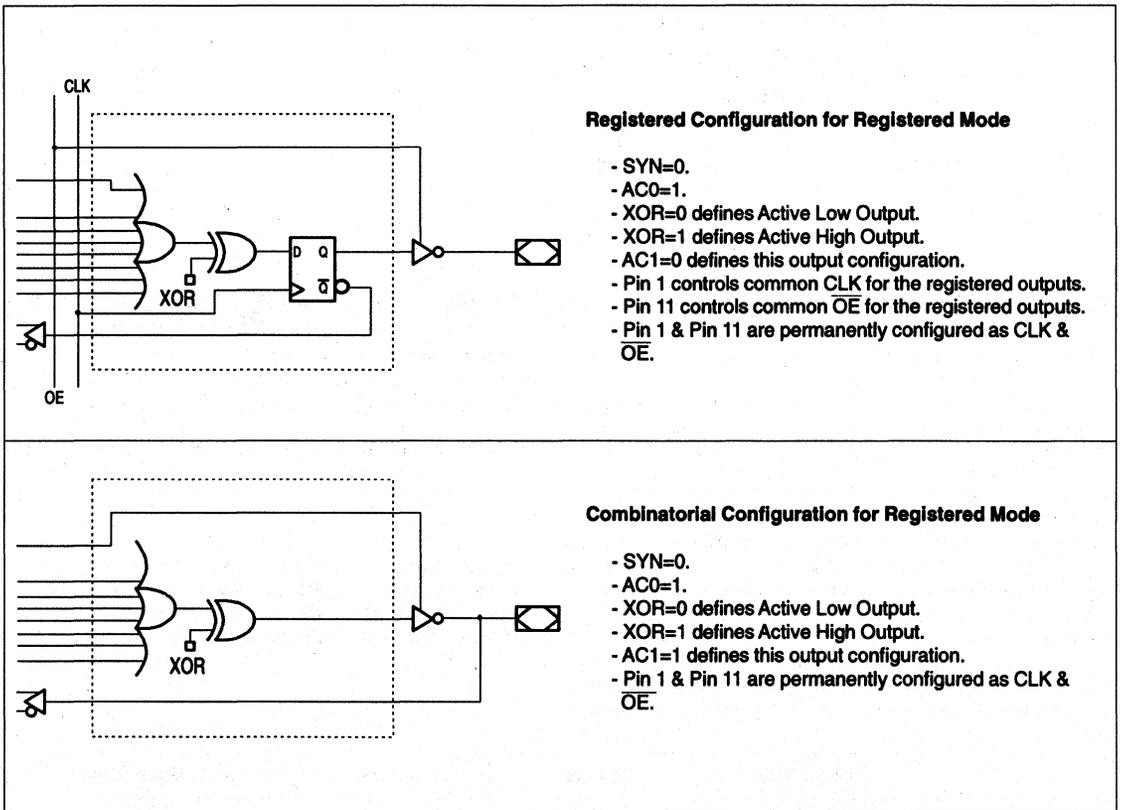
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this

mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

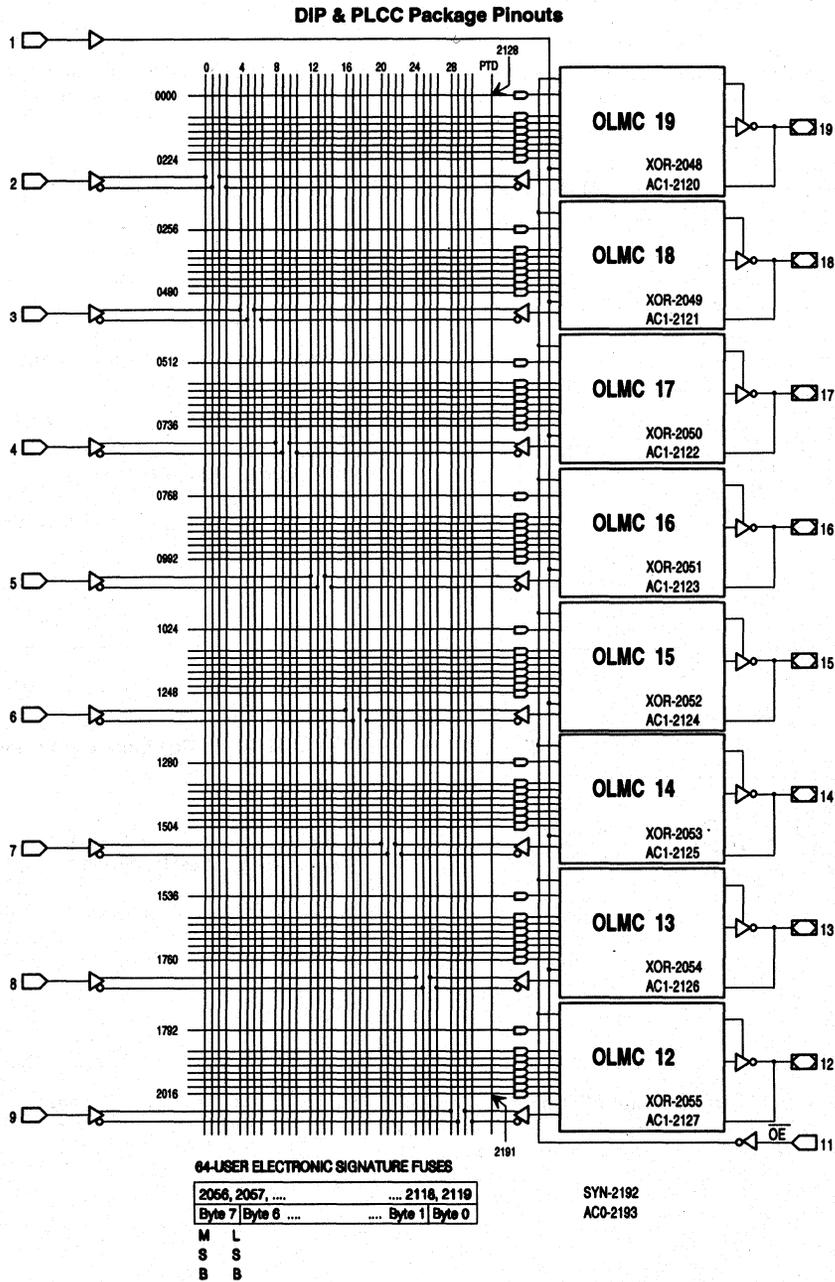
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM



COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

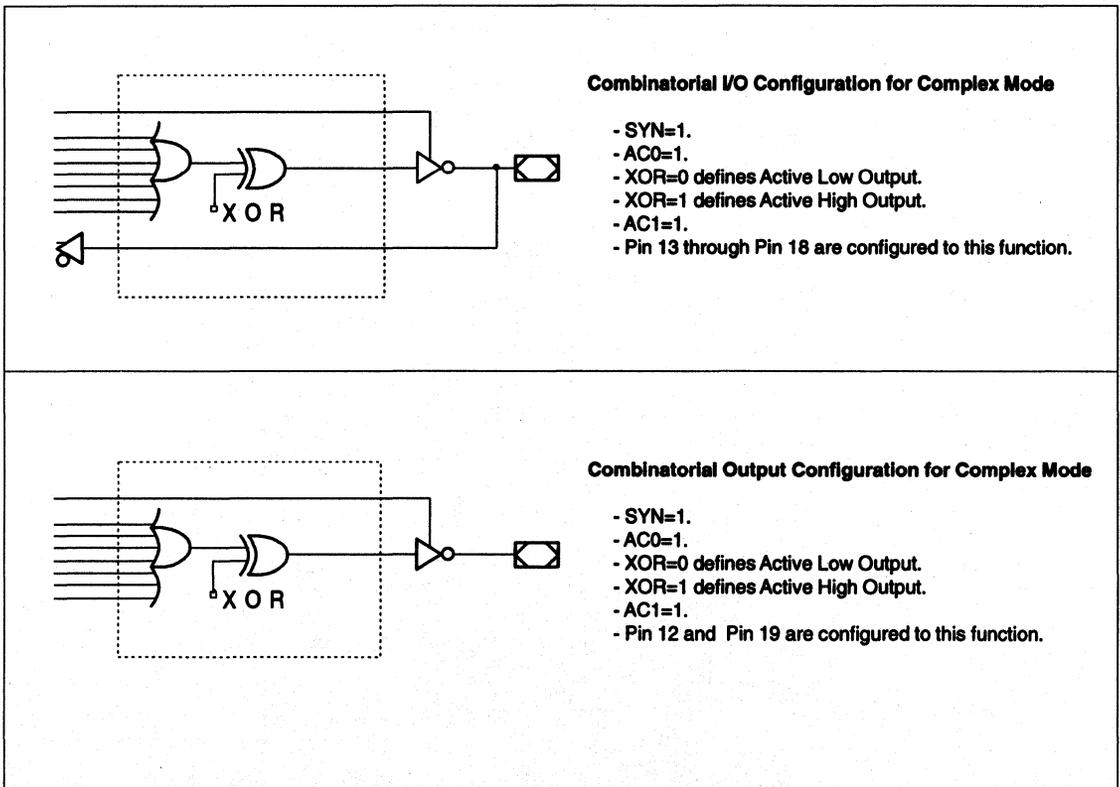
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input ca-

pability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

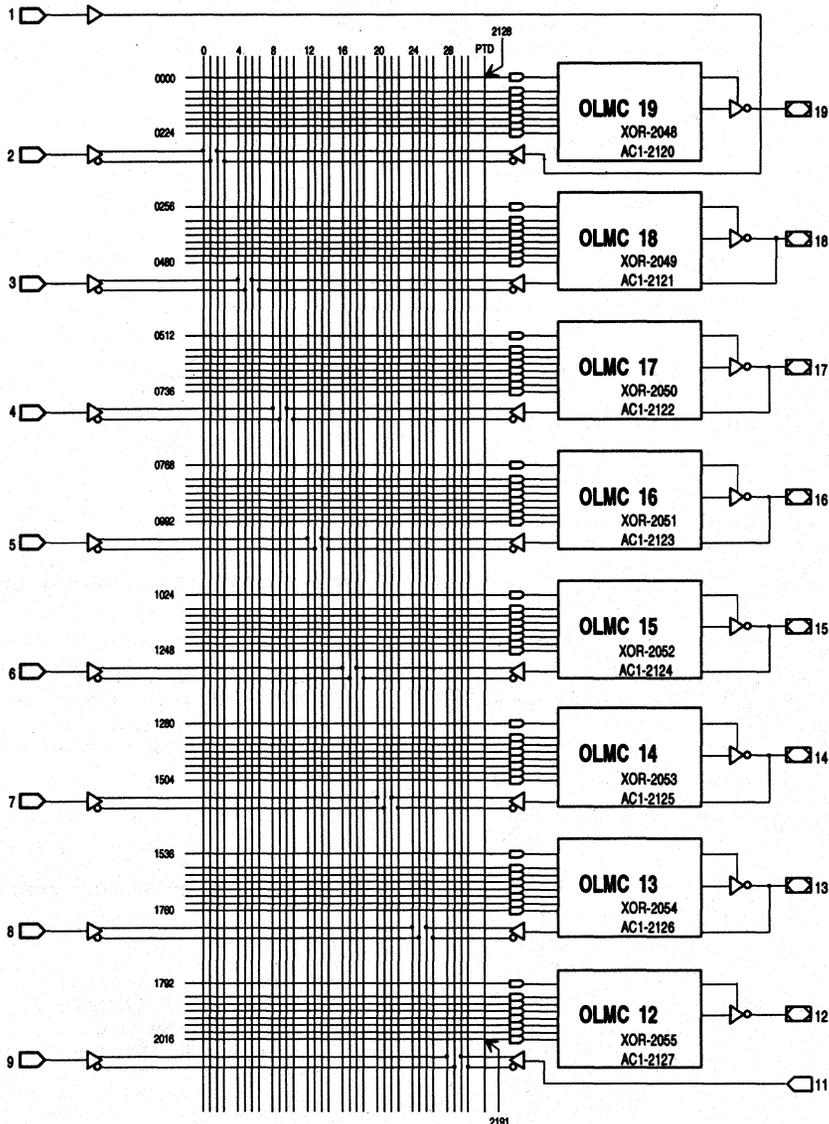
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, 2118, 2119
Byte 7 Byte 6 Byte 1 Byte 0

M L
S S
B B

SYN-2192
AC0-2193

SIMPLE MODE

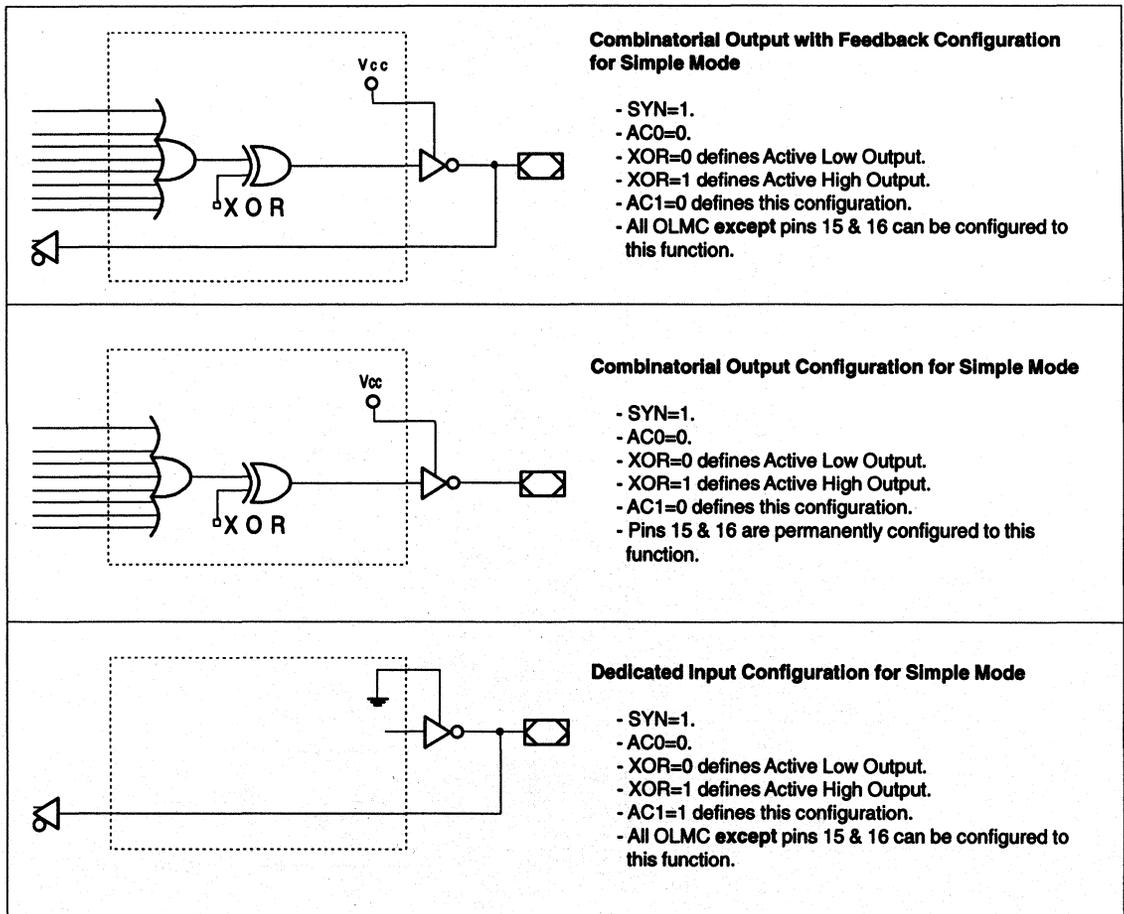
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

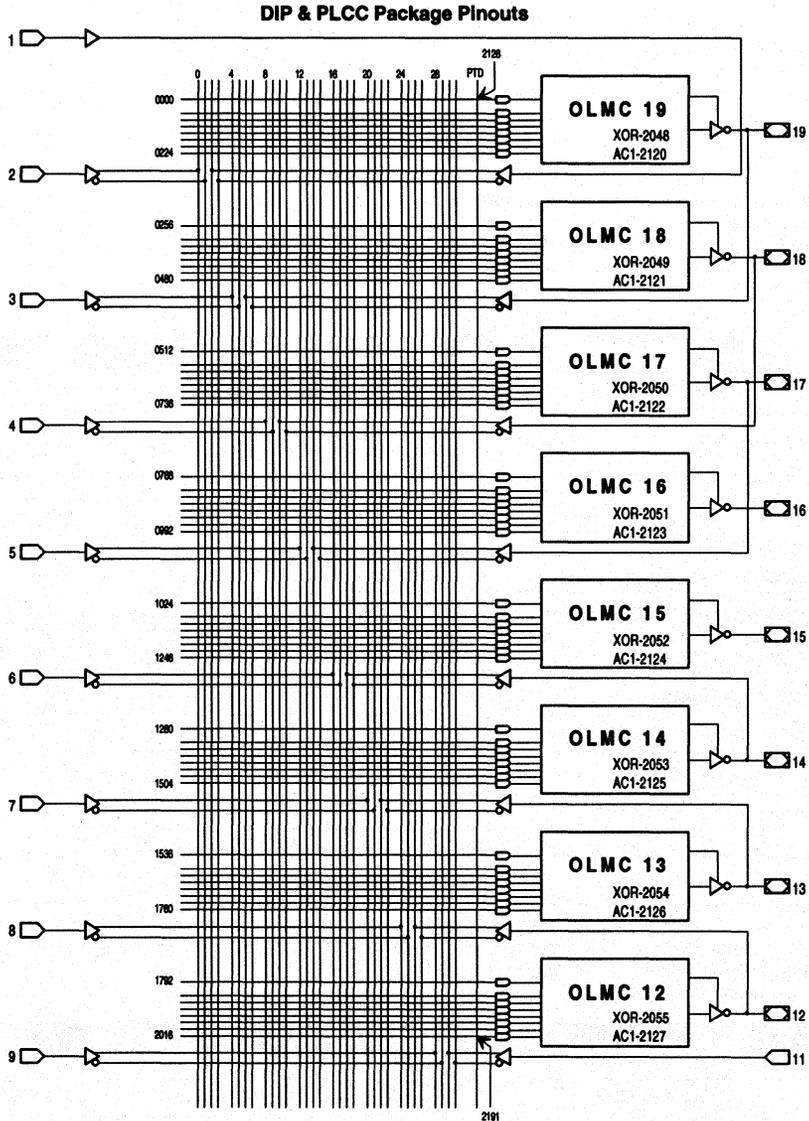
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, 2116, 2119
Byte 7 Byte 6 Byte 1 Byte 0

M L
S S
B B

SYN-2192
ACO-2193

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 25MHz$ Outputs Open (no load)	—	75	115	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{IO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-7		-10		UNITS	
			MIN.	MAX.	MIN.	MAX.		
t _{pd}	1	Input or I/O to Combinational Output	8 outputs switching	3	7.5	3	10	ns
			1 output switching	—	7	—	—	ns
t _{co}	1	Clock to Output Delay	2	5	2	7	ns	
t _{cf} ²	—	Clock to Feedback Delay	—	3	—	6	ns	
t _{su}	—	Setup Time, Input or Feedback before Clock	7	—	10	—	ns	
t _h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns	
f _{max} ³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	83.3	—	58.8	—	MHz	
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	100	—	62.5	—	MHz	
	1	Maximum Clock Frequency with No Feedback	100	—	62.5	—	MHz	
t _{wh}	—	Clock Pulse Duration, High	5	—	8	—	ns	
t _{wl}	—	Clock Pulse Duration, Low	5	—	8	—	ns	
t _{en}	2	Input or I/O to Output Enabled	3	9	3	10	ns	
	2	\overline{OE} to Output Enabled	2	6	2	10	ns	
t _{dis}	3	Input or I/O to Output Disabled	2	9	2	10	ns	
	3	\overline{OE} to Output Disabled	1.5	6	1.5	10	ns	

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

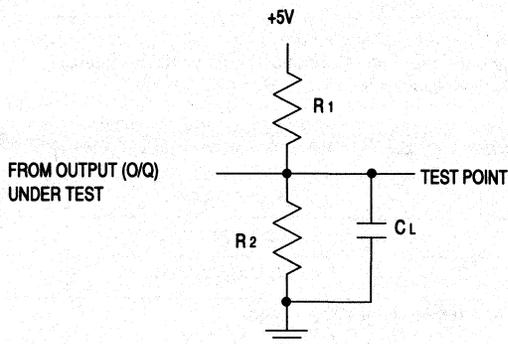
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	390Ω
	Active Low	200Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL16V8A** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Ambient Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A)0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS		
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V		
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V		
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA		
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA		
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V		
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V		
I_{OL}	Low Level Output Current		—	—	24	mA		
I_{OH}	High Level Output Current		—	—	-3.2	mA		
I_{OS}'	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA		
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ Outputs Open (no load)	$f_{toggle} = 25MHz$	L -15	—	75	115	mA
			$f_{toggle} = 15MHz$	L -25	—	75	90	mA
			$f_{toggle} = 15MHz$	Q -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{io}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{io} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	15	3	25	ns
t_{co}	1	Clock to Output Delay	2	10	2	12	ns
t_{cf}^2	—	Clock to Feedback Delay	—	8	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	45.5	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	50	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	41.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	12	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	25	ns
	2	\overline{OE} to Output Enabled	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	25	ns
	3	\overline{OE} to Output Disabled	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

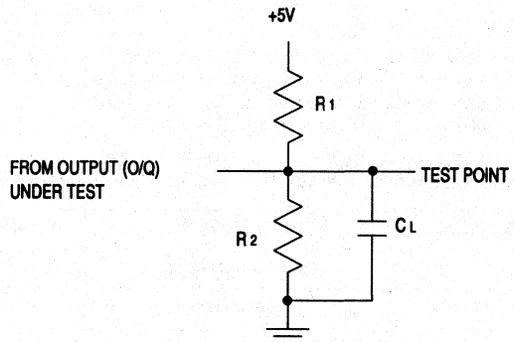
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	390Ω
	Active Low	200Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL16V8B** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 25MHz$ Outputs Open (no load)	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{io}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{io} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	10	3	15	ns
t_{co}	1	Clock to Output Delay	2	7	2	10	ns
t_{cf}^2	—	Clock to Feedback Delay	—	6	—	8	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	58.8	—	45.5	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	62.5	—	50	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	10	—	15	ns
	2	\overline{OE} to Output Enabled	2	10	—	15	ns
t_{dis}	3	Input or I/O to Output Disabled	2	10	—	15	ns
	3	\overline{OE} to Output Disabled	1.5	10	—	15	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.
- 3) Refer to **f_{max} Descriptions** section.

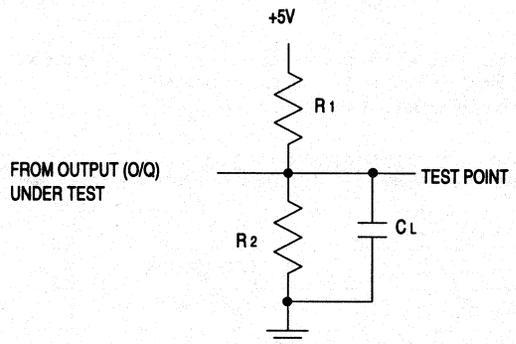
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	5pF
	Active Low	200Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL16V8A** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Ambient Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A)-40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}'	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	—	75	130	mA
	Supply Current	Outputs Open (no load)				
		$f_{toggle} = 25MHz$	L -25			
		$f_{toggle} = 15MHz$	Q -20/-25	—	45	65

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	20	3	25	ns
t_{co}	1	Clock to Output Delay	2	11	2	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	9	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	13	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	41.6	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	45.4	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	ns
t_{en}	2	Input or I/O to Output	—	20	—	25	ns
	2	\overline{OE} to Output	—	18	—	20	ns
t_{dis}	3	Input or I/O to Output	—	20	—	25	ns
	3	\overline{OE} to Output	—	18	—	20	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.
- 3) Refer to **f_{max} Descriptions** section.

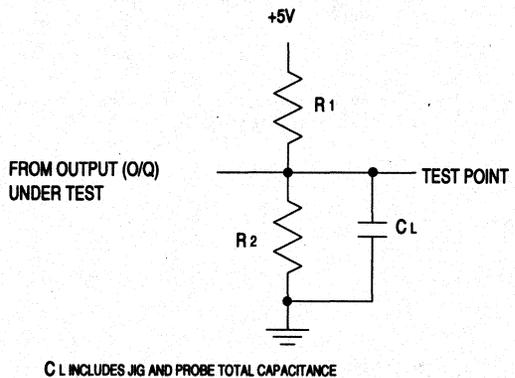
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

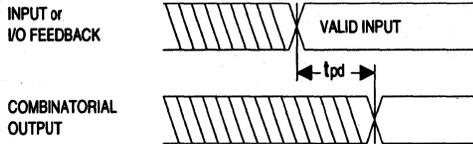
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

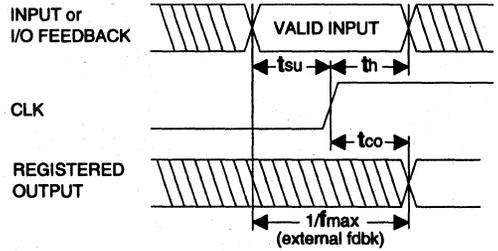
Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	390Ω
	Active Low	200Ω	390Ω



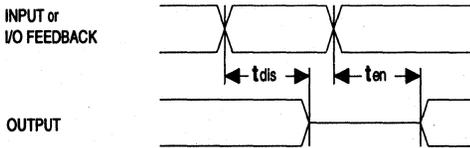
SWITCHING WAVEFORMS



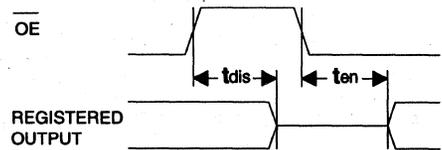
Combinatorial Output



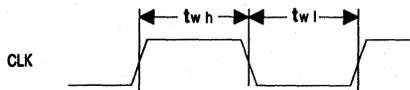
Registered Output



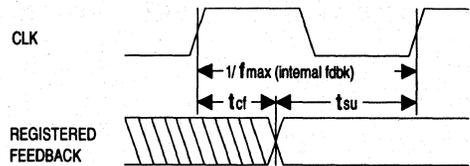
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

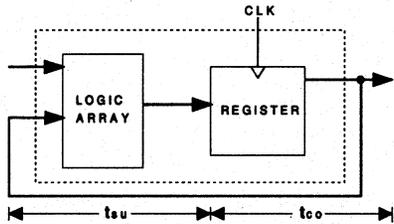


Clock Width



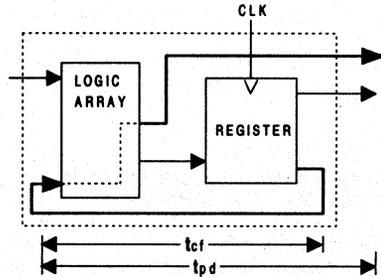
f_{max} with Feedback

f_{max} DESCRIPTIONS



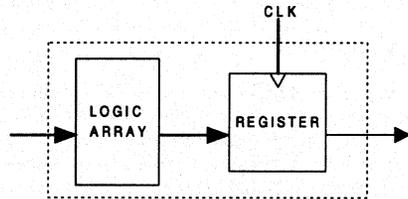
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL16V8A/B device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL16V8A/B devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL16V8A/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

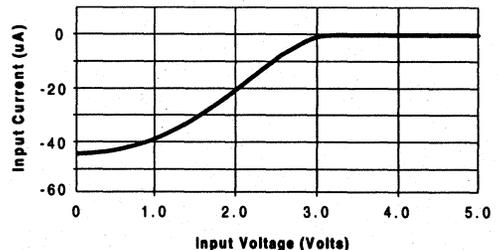
GAL16V8A/B devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

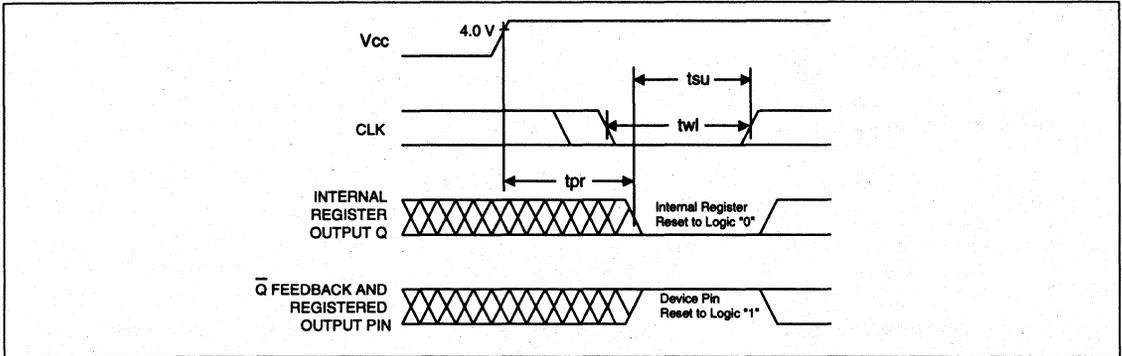
GAL16V8A/B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8B input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). In contrast, the GAL16V8A does not have active pull-ups within their input structures. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET

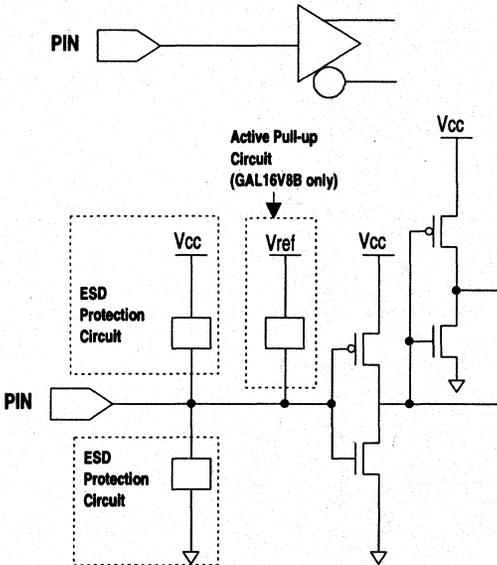


2

Circuitry within the GAL16V8A/B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

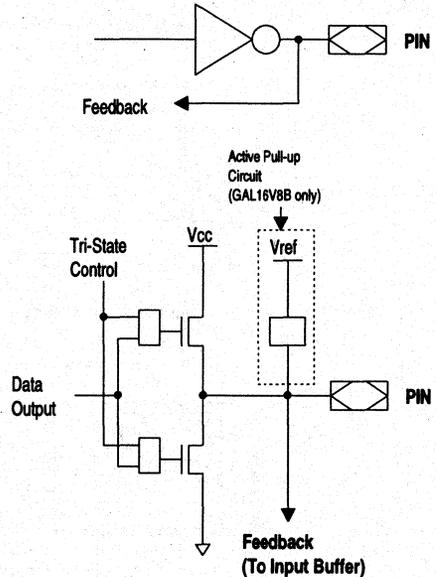
conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = 3.2V

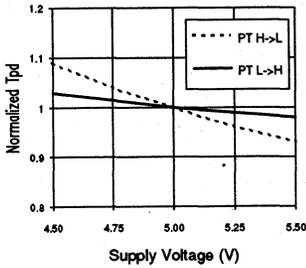
Typical Input



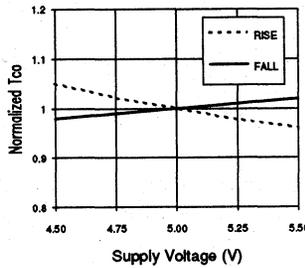
Typ. Vref = 3.2V

Typical Output

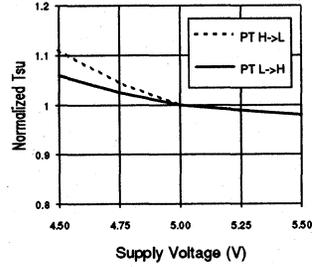
Normalized Tpd vs Vcc



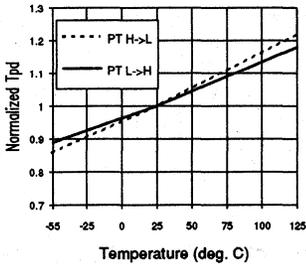
Normalized Tco vs Vcc



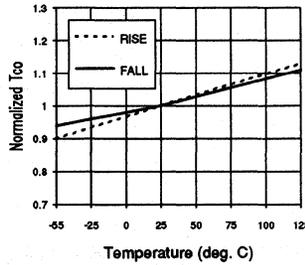
Normalized Tsu vs Vcc



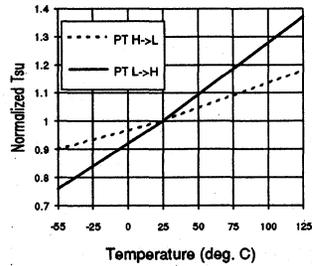
Normalized Tpd vs Temp



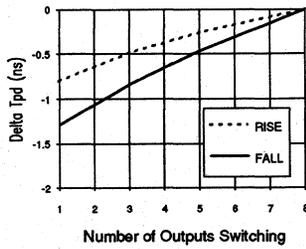
Normalized Tco vs Temp



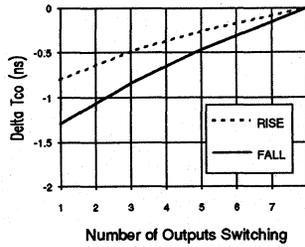
Normalized Tsu vs Temp



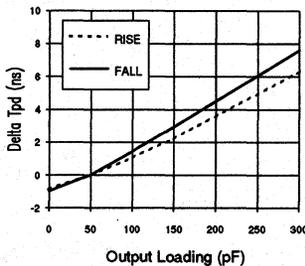
Delta Tpd vs # of Outputs Switching



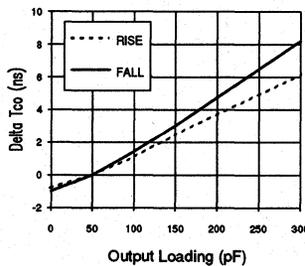
Delta Tco vs # of Outputs Switching



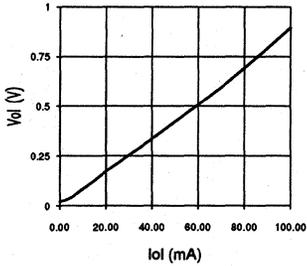
Delta Tpd vs Output Loading



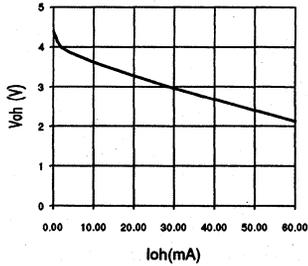
Delta Tco vs Output Loading



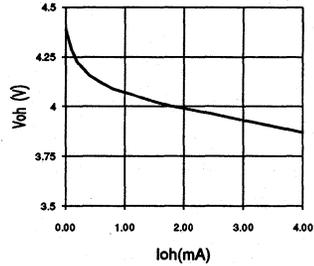
V_{ol} vs I_{ol}



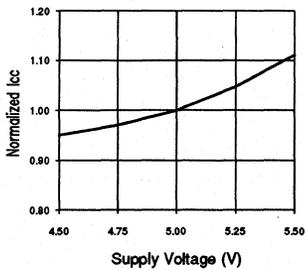
V_{oh} vs I_{oh}



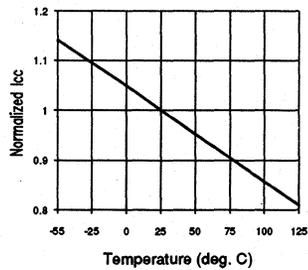
V_{oh} vs I_{oh}



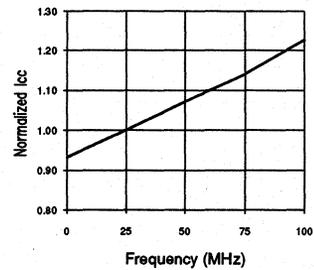
Normalized I_{cc} vs V_{cc}



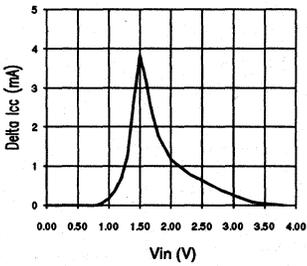
Normalized I_{cc} vs Temp



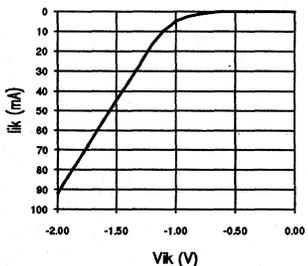
Normalized I_{cc} vs Freq.

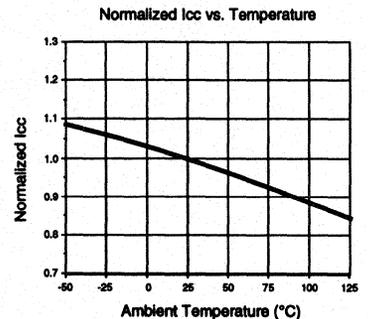
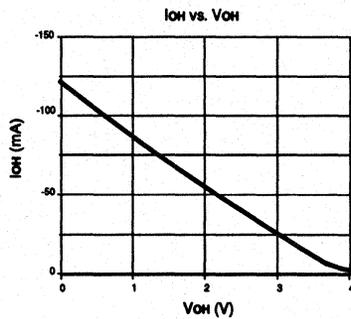
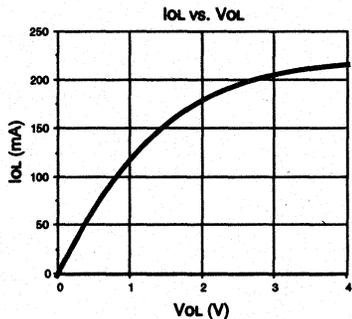
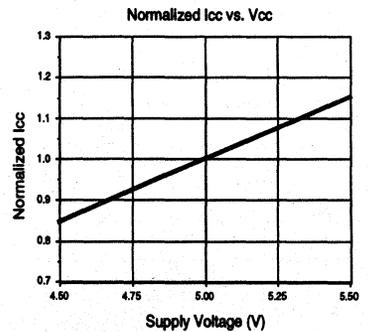
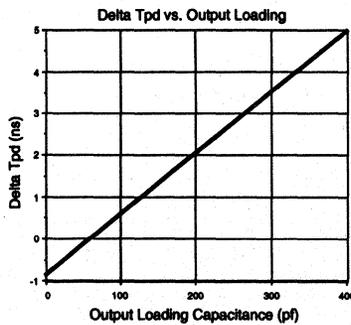
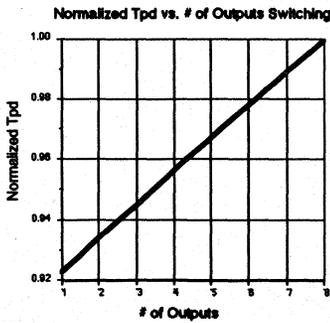
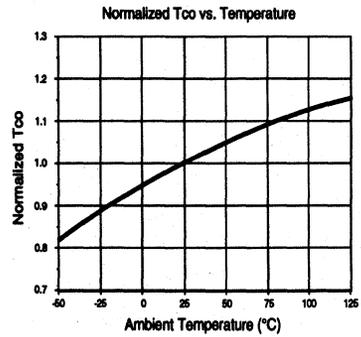
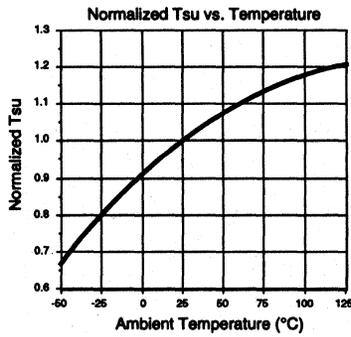
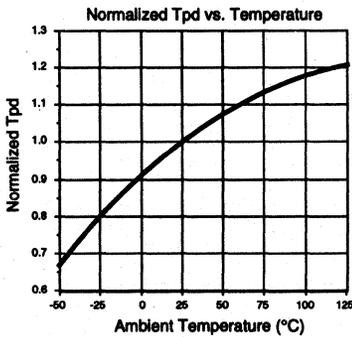
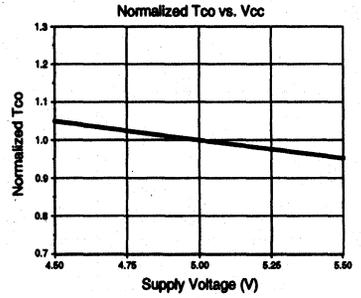
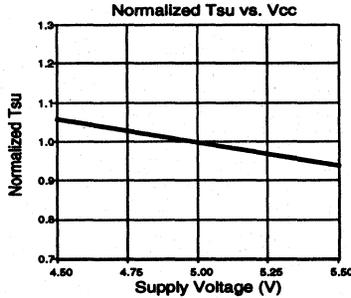
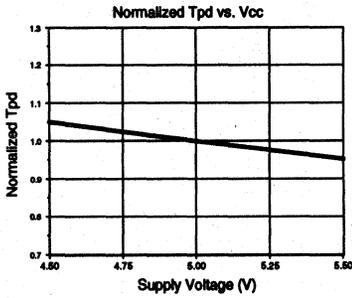


Delta I_{cc} vs V_{in} (1 Input)



Input Clamp (V_{ik})







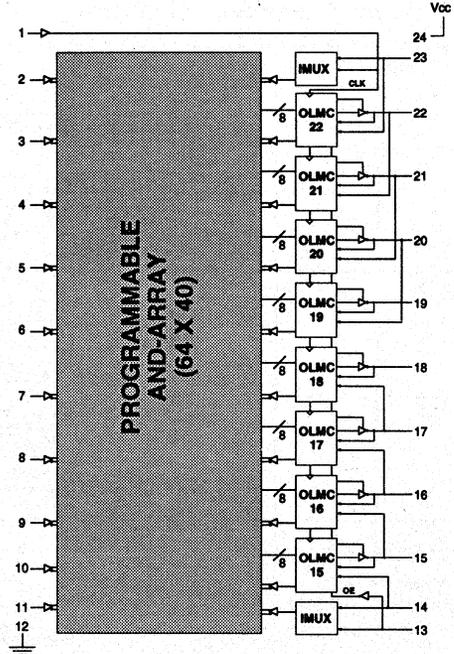
GAL20V8B GAL20V8A

High Performance E²CMOS PLD

FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 7.5 ns Maximum Propagation Delay
 - F_{max} = 100 MHz
 - 5 ns Maximum from Clock Input to Data Output
 - TTL Compatible 24 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS (GAL20V8B)**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 24-pin PAL[®] Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



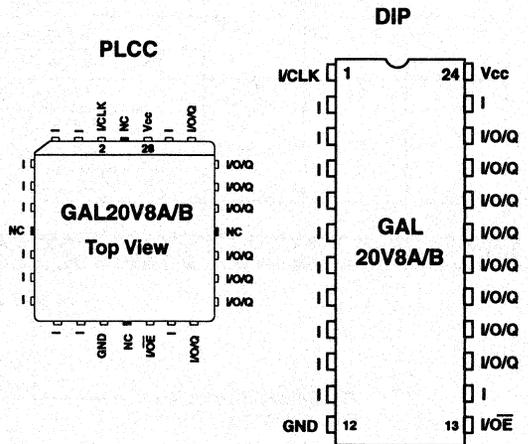
PIN CONFIGURATION

DESCRIPTION

The GAL20V8B, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8A/B are the PAL architectures listed in the table of the macrocell description section. GAL20V8A/B devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL[®] products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.



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GAL20V8A/B ORDERING INFORMATION

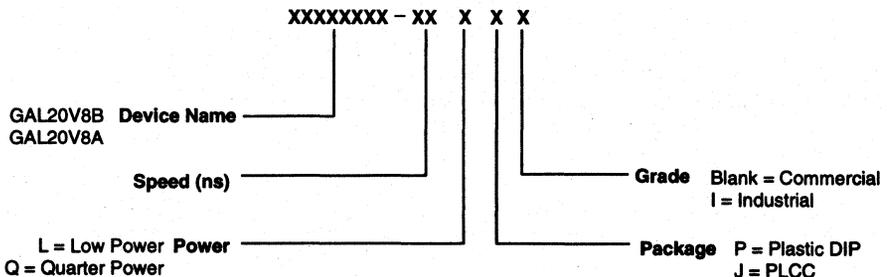
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	115	GAL20V8B-7LP	24-Pin Plastic DIP
			115	GAL20V8B-7LJ	28-Lead PLCC
10	10	7	115	GAL20V8B-10LP	24-Pin Plastic DIP
			115	GAL20V8B-10LJ	28-Lead PLCC
			115	GAL20V8A-10LP	24-Pin Plastic DIP
			115	GAL20V8A-10LJ	28-Lead PLCC
15	12	10	55	GAL20V8A-15QP	24-Pin Plastic DIP
			55	GAL20V8A-15QJ	28-Lead PLCC
			115	GAL20V8A-15LP	24-Pin Plastic DIP
			115	GAL20V8A-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8A-25QP	24-Pin Plastic DIP
			55	GAL20V8A-25QJ	28-Lead PLCC
			90	GAL20V8A-25LP	24-Pin Plastic DIP
			90	GAL20V8A-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8B-10LPI	24-Pin Plastic DIP
			130	GAL20V8B-10LJI	28-Lead PLCC
15	12	10	130	GAL20V8B-15LPI	24-Pin Plastic DIP
			130	GAL20V8B-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8A-20QPI	24-Pin Plastic DIP
			65	GAL20V8A-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8A-25QPI	24-Pin Plastic DIP
			65	GAL20V8A-25QJI	28-Lead PLCC
			130	GAL20V8A-25LPI	24-Pin Plastic DIP
			130	GAL20V8A-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8A/B. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8A and GAL20V8B can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8A/B	GAL20V8A/B Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 13 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOGIC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered" ¹	"Complex" ¹	"Simple" ¹	GAL20V8A
PLDesigner	P20V8R ²	P20V8C ²	P20V8C ²	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS ³	G20V8

- 1) Used with Configuration keyword.
- 2) Prior to Version 2.0 support.
- 3) Supported on Version 1.20 or later.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

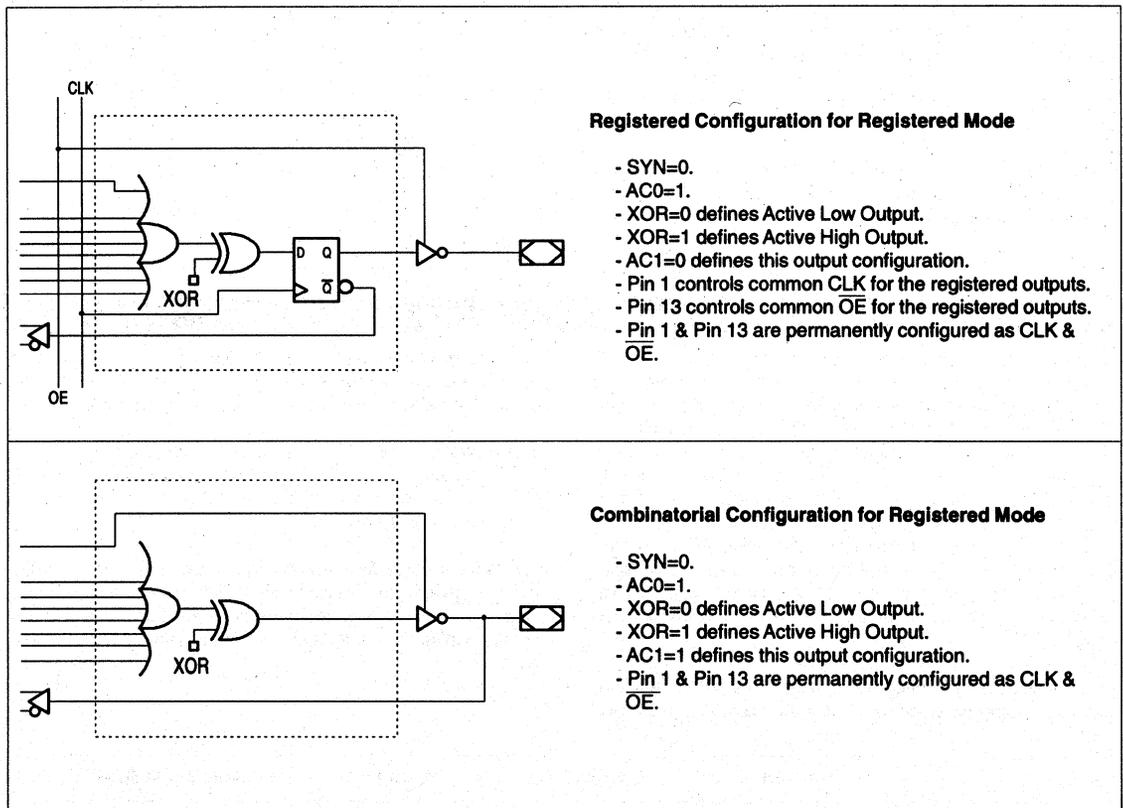
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this

mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

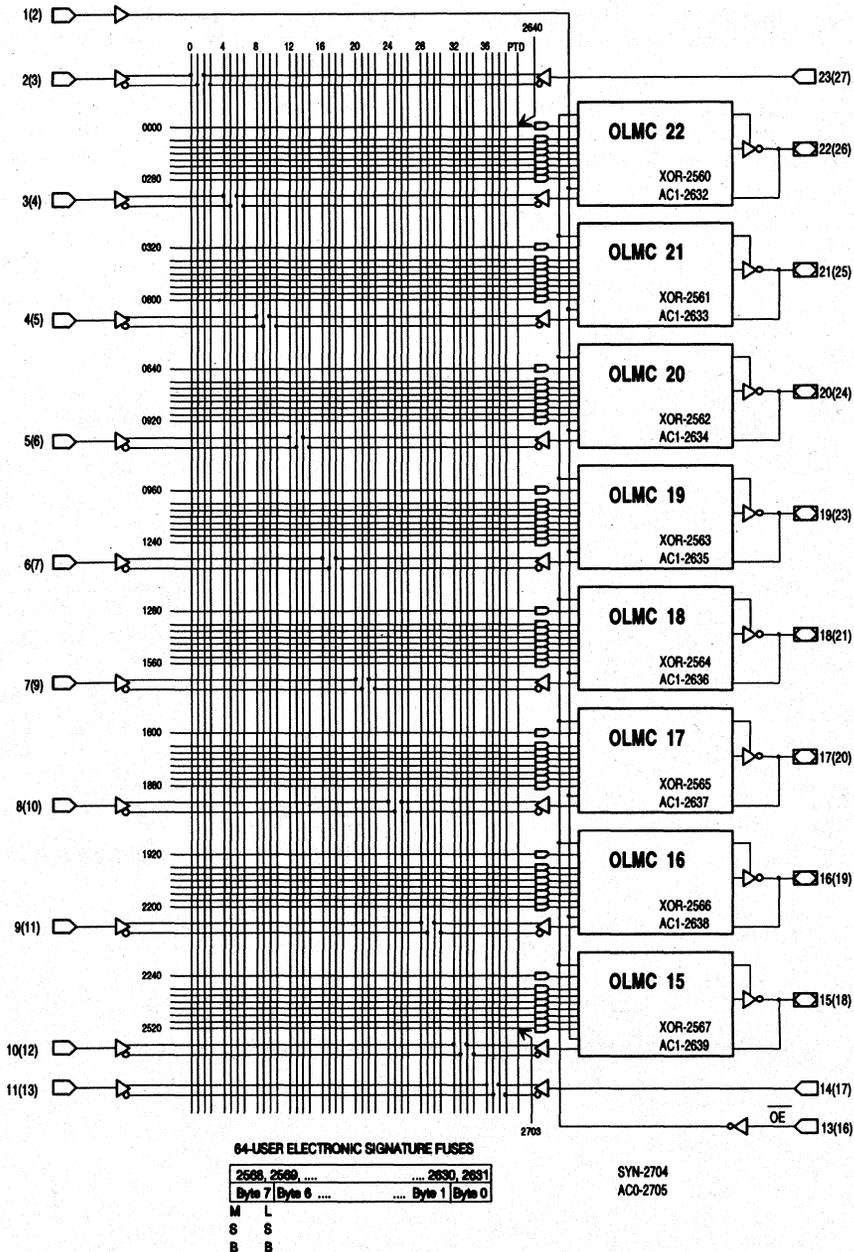
The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

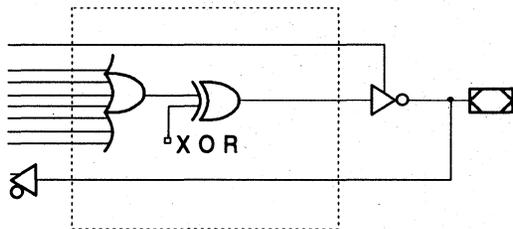
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input ca-

pability. Designs requiring eight I/O's can be implemented in the Registered mode.

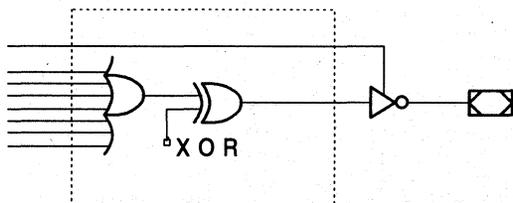
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



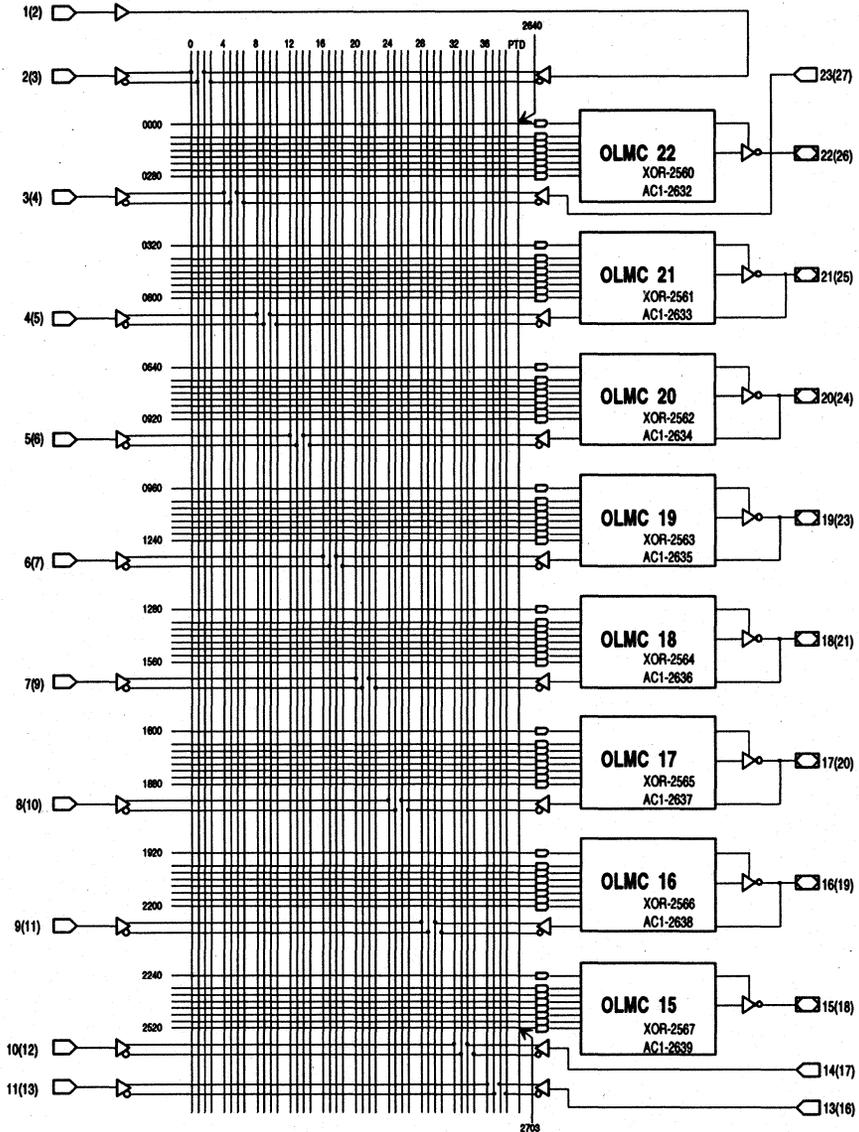
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-BITER ELECTRONIC SIGNATURE FUSES

2568, 2569, ..., 2630, 2631
Byte 7 | Byte 6 ... Byte 1 | Byte 0

M L
S S
B B

SYN-2704
ACO-2705

SIMPLE MODE

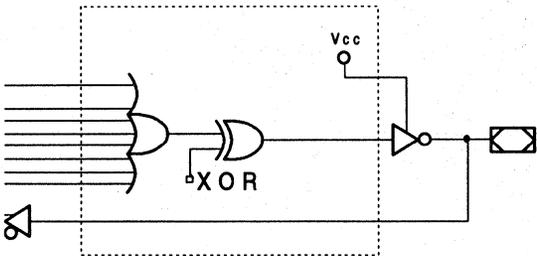
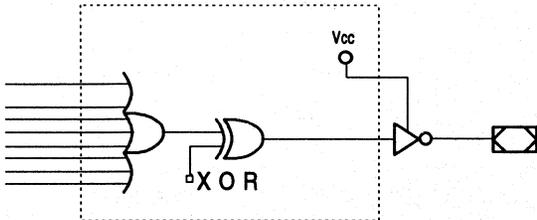
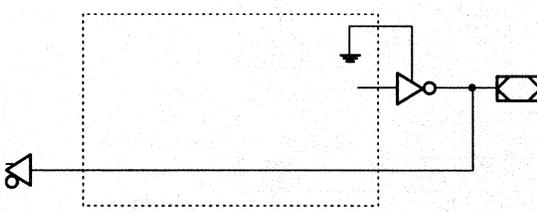
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 & 19) cannot be used in the input configuration.

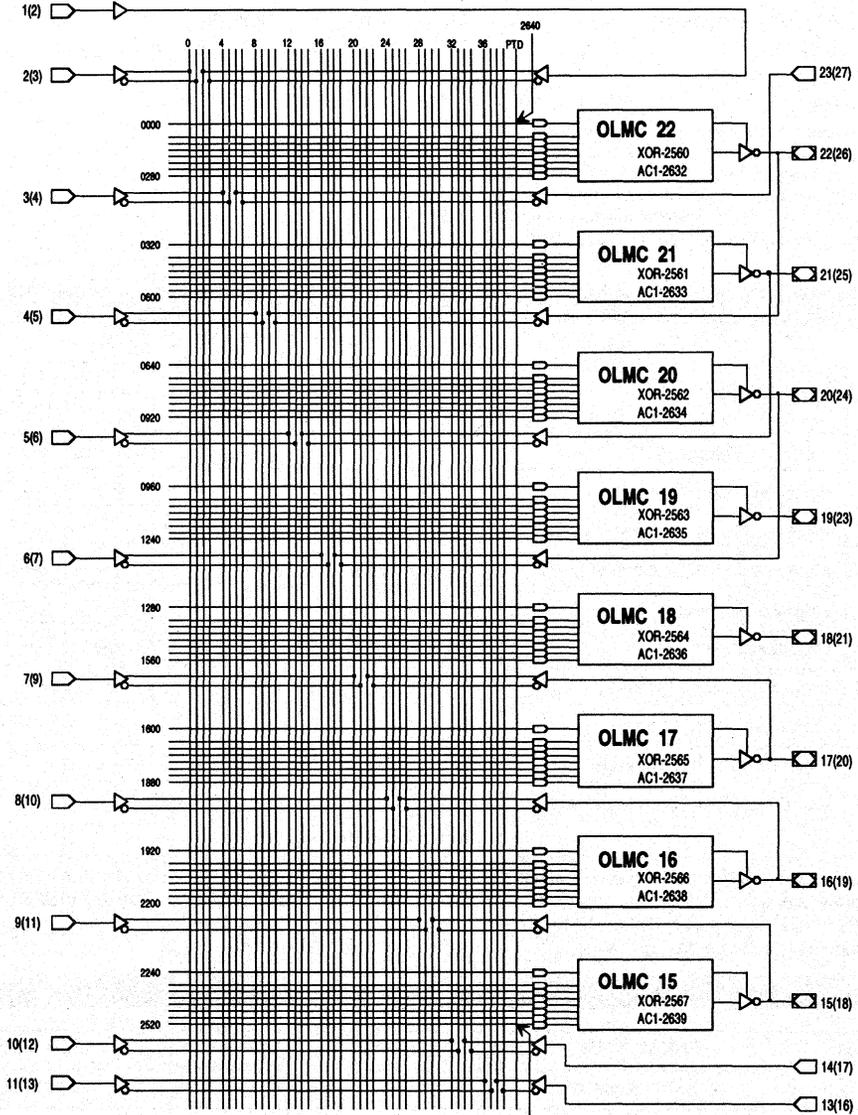
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 18 & 19 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 18 & 19 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	2630, 2631
Byte 7 Byte 6 ...	Byte 1 Byte 0

M L
S S
B B

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 25MHz$ Outputs Open (no load)	—	75	115	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-7		-10		UNITS	
			MIN.	MAX.	MIN.	MAX.		
t_{pd}	1	Input or I/O to Combinational Output	8 outputs switching	3	7.5	3	10	ns
			1 output switching	—	7	—	—	ns
t_{co}	1	Clock to Output Delay	2	5	2	7	ns	
t_{cf}	—	Clock to Feedback Delay	—	3	—	6	ns	
t_{su}	—	Setup Time, Input or Feedback before Clock	7	—	10	—	ns	
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns	
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	83.3	—	58.8	—	MHz	
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	100	—	62.5	—	MHz	
	1	Maximum Clock Frequency with No Feedback	100	—	62.5	—	MHz	
t_{wh}	—	Clock Pulse Duration, High	5	—	8	—	ns	
t_{wl}	—	Clock Pulse Duration, Low	5	—	8	—	ns	
t_{en}	2	Input or I/O to Output Enabled	3	9	3	10	ns	
	2	\overline{OE} to Output Enabled	2	6	2	10	ns	
t_{dis}	3	Input or I/O to Output Disabled	2	9	2	10	ns	
	3	\overline{OE} to Output Disabled	1.5	6	1.5	10	ns	

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

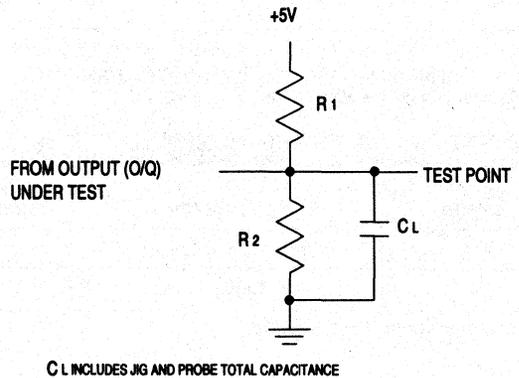
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	390Ω
	Active Low	200Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL20V8A** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with

Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS		
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V		
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V		
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA		
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA		
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V		
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V		
I_{OL}	Low Level Output Current		—	—	24	mA		
I_{OH}	High Level Output Current		—	—	-3.2	mA		
I_{OS}'	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA		
I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$						
	Supply Current	Outputs Open (no load)	$f_{toggle} = 25MHz$	L -10/-15	—	75	115	mA
			$f_{toggle} = 15MHz$	L -25	—	75	90	mA
			$f_{toggle} = 15MHz$	Q -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{io}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{io} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	10	3	15	3	25	ns
t_{co}	1	Clock to Output Delay	2	7	2	10	2	12	ns
t_{cf}^2	—	Clock to Feedback Delay	—	6	—	8	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	12	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	58.8	—	45.5	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	58.8	—	50	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	41.7	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	12	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	10	—	15	—	25	ns
	2	\overline{OE} to Output Enabled	—	10	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	10	—	15	—	25	ns
	3	\overline{OE} to Output Disabled	—	10	—	15	—	20	ns

USE GAL20V8B-10 FOR NEW DESIGNS

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.
- 3) Refer to **f_{max} Descriptions** section.

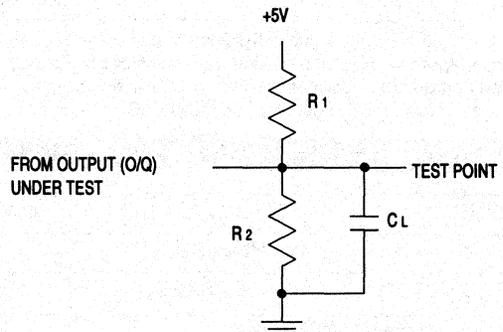
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	5pF
	Active Low	200Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$ Outputs Open (no load)	—	75	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	10	3	15	ns
t_{co}	1	Clock to Output Delay	2	7	2	10	ns
t_{cf}^2	—	Clock to Feedback Delay	—	6	—	8	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	58.8	—	45.5	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	62.5	—	50	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	10	—	15	ns
	2	\overline{OE} to Output Enabled	2	10	—	15	ns
t_{dis}	3	Input or I/O to Output Disabled	2	10	—	15	ns
	3	\overline{OE} to Output Disabled	1.5	10	—	15	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

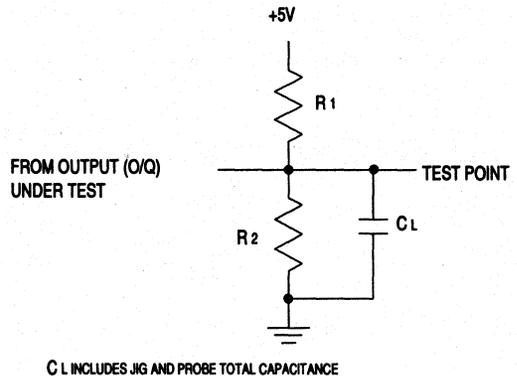
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R_1	R_2	C_L
1	200 Ω	390 Ω	50pF
2	Active High	∞	390 Ω
	Active Low	200 Ω	390 Ω
3	Active High	∞	5pF
	Active Low	200 Ω	390 Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications GAL20V8A Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ Outputs Open (no load)				
	Supply Current					
		$f_{toggle} = 25MHz \quad L - 25$	—	75	130	mA
		$f_{toggle} = 15MHz \quad Q - 20/-25$	—	45	65	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
 2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	20	3	25	ns
t_{co}	1	Clock to Output Delay	2	11	2	12	ns
t_{cf}²		Clock to Feedback Delay	—	9	—	10	ns
t_{su}		Setup Time, Input or Feedback before Clock	13	—	15	—	ns
t_h		Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	41.6	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	45.4	—	40	—	MHz
	1	Maximum Clock Frequency with External Feedback	50	—	41.6	—	MHz
t_{wh}		Clock Pulse Duration, High	10	—	12	—	ns
t_{wl}		Clock Pulse Duration, Low	10	—	12	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	ns
	2	\overline{OE} to Output Enabled	—	18	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	ns
	3	\overline{OE} to Output Disabled	—	18	—	20	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.
- 3) Refer to **f_{max} Descriptions** section.

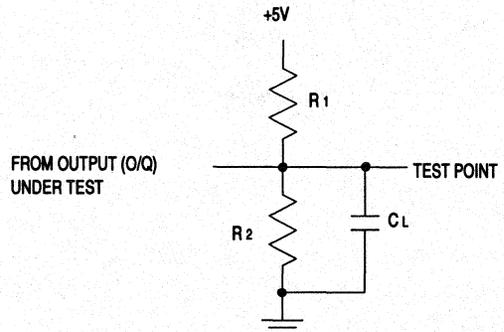
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

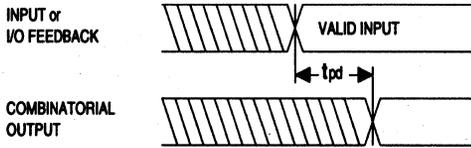
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

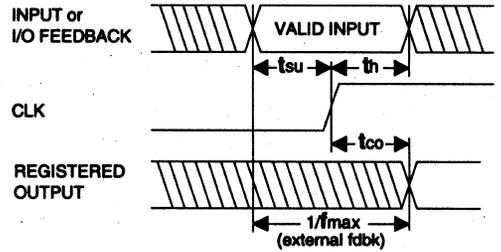
Test Condition	R ₁	R ₂	C _L
1	200Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	200Ω	390Ω
3	Active High	∞	5pF
	Active Low	200Ω	390Ω



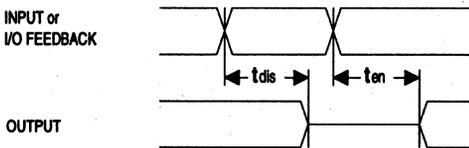
SWITCHING WAVEFORMS



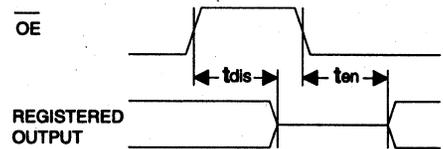
Combinatorial Output



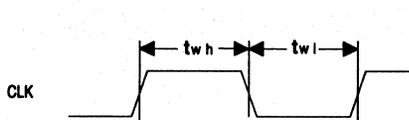
Registered Output



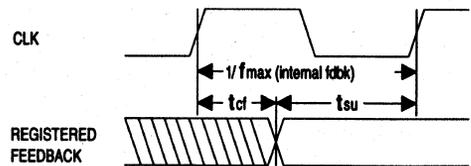
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

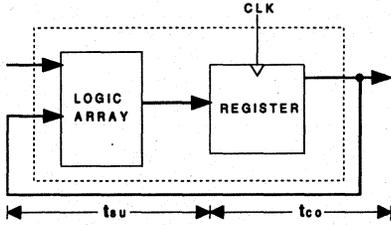


Clock Width



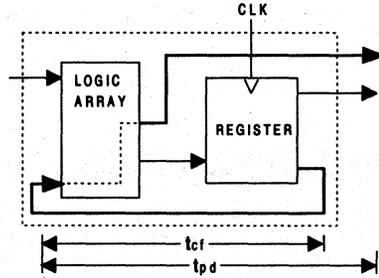
fmax with Feedback

f_{max} DESCRIPTIONS



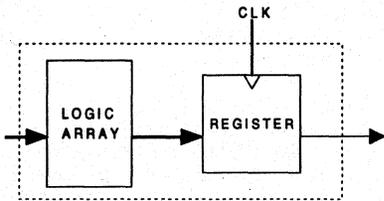
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.



f_{max} Without Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL20V8A/B device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

The security cell is provided on all GAL20V8A/B devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL20V8A/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

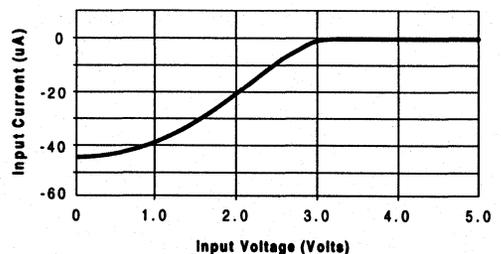
GAL20V8A/B devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

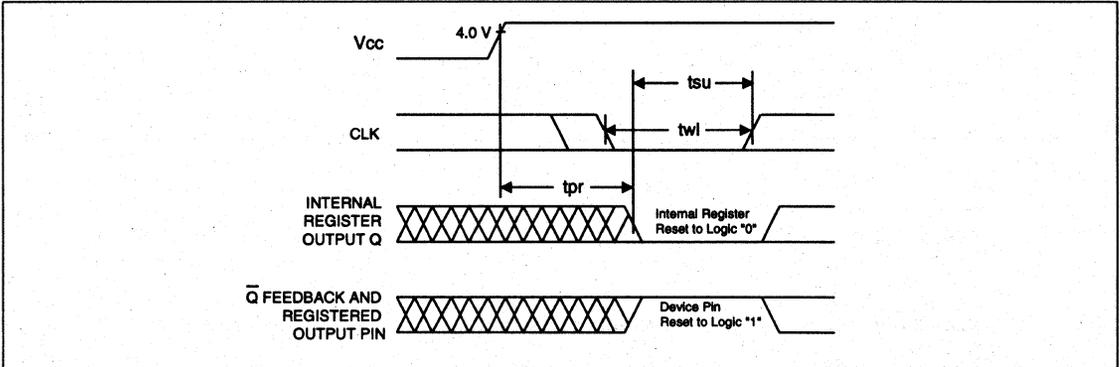
GAL20V8A/B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20V8B input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). In contrast, the GAL20V8A does not have active pull-ups within their input structures. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET

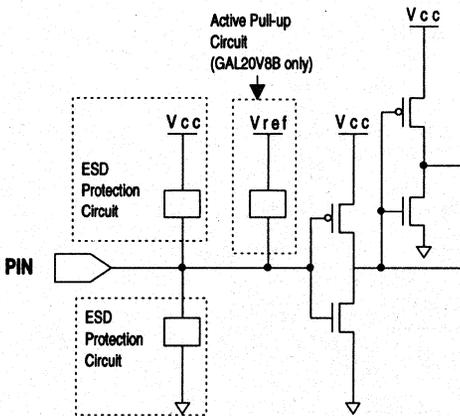
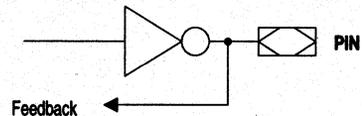
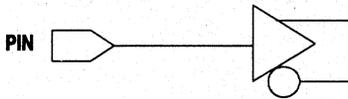


2

Circuitry within the GAL20V8A/B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

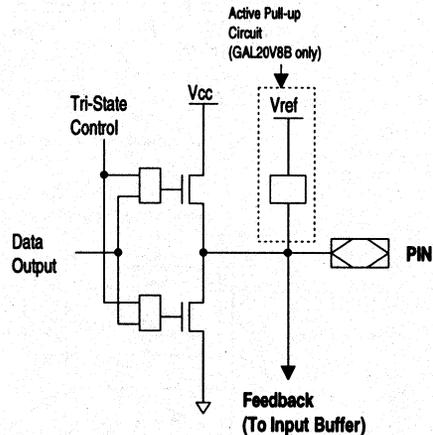
conditions must be met to guarantee a valid power-up reset of the device. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. $V_{ref} = 3.2V$

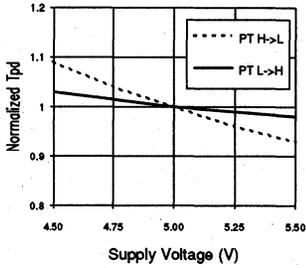
Typical Input



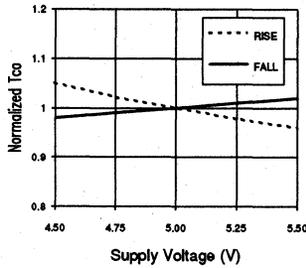
Typ. $V_{ref} = 3.2V$

Typical Output

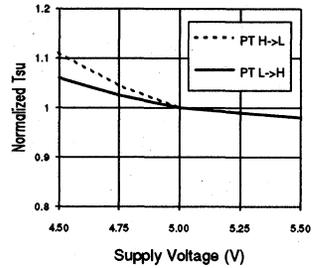
Normalized Tpd vs Vcc



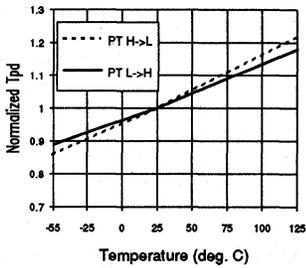
Normalized Tco vs Vcc



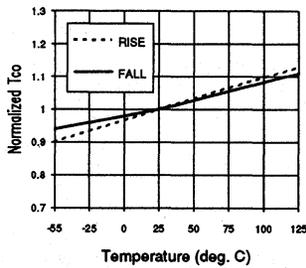
Normalized Tsu vs Vcc



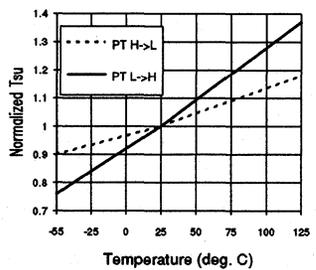
Normalized Tpd vs Temp



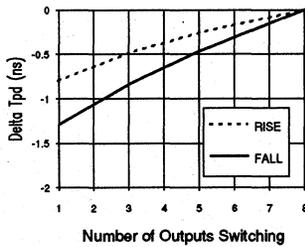
Normalized Tco vs Temp



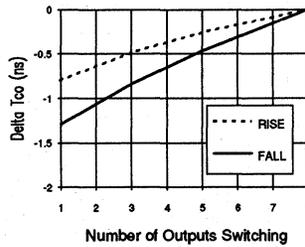
Normalized Tsu vs Temp



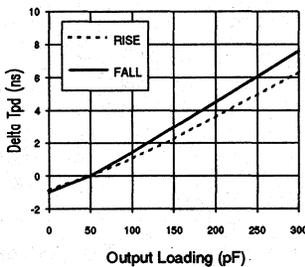
Delta Tpd vs # of Outputs Switching



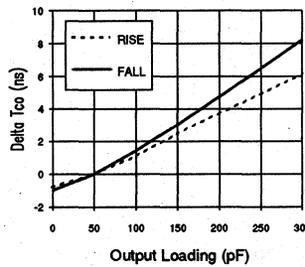
Delta Tco vs # of Outputs Switching



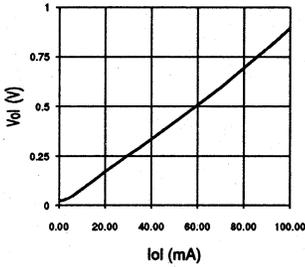
Delta Tpd vs Output Loading



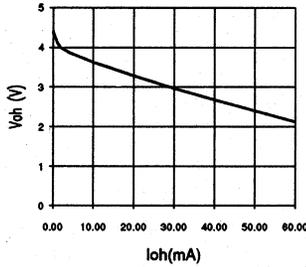
Delta Tco vs Output Loading



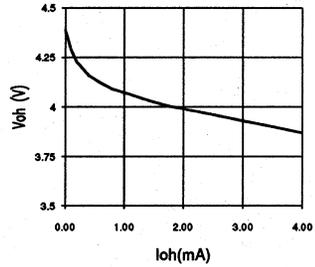
Vol vs Iol



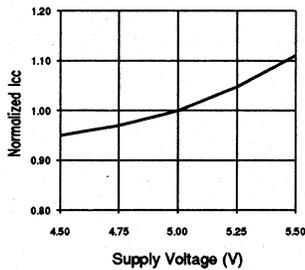
Voh vs Ioh



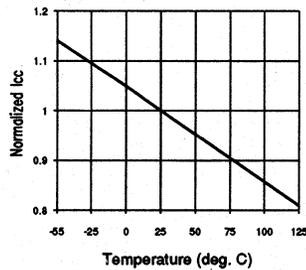
Voh vs Ioh



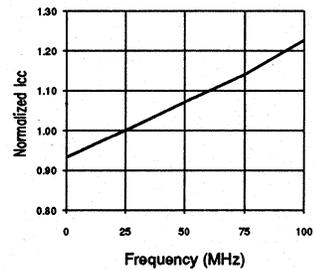
Normalized Icc vs Vcc



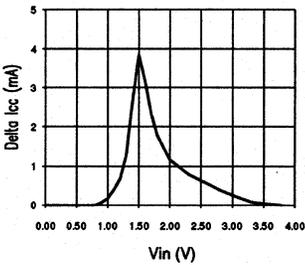
Normalized Icc vs Temp



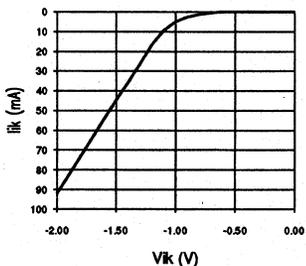
Normalized Icc vs Freq.

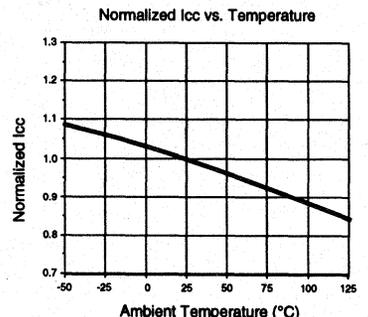
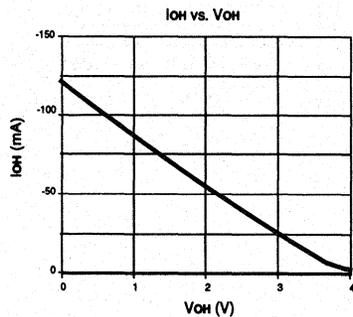
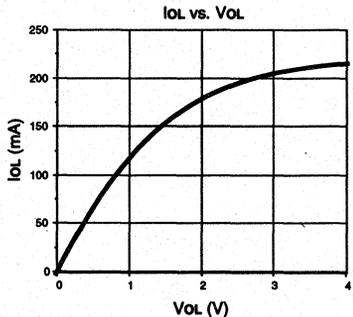
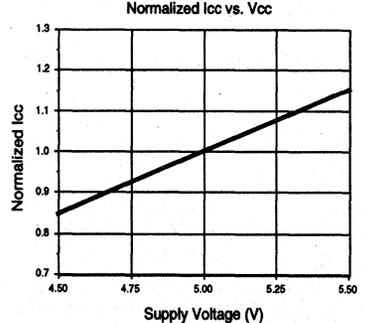
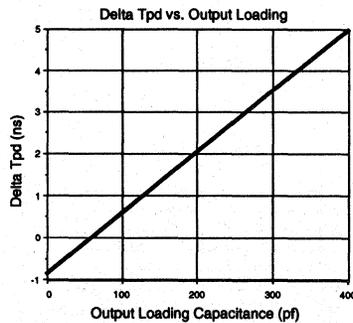
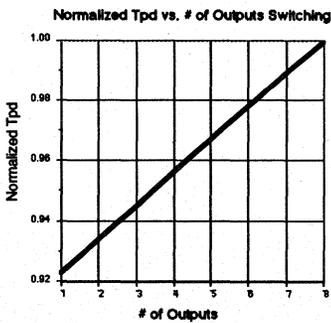
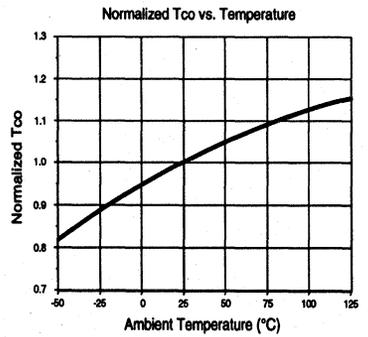
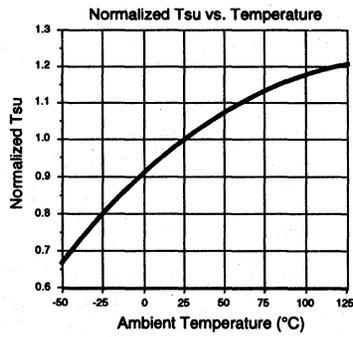
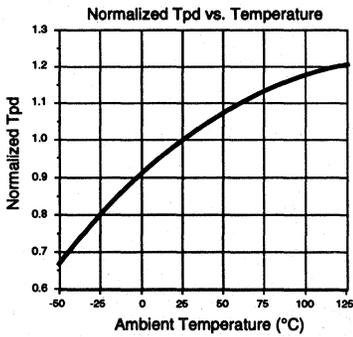
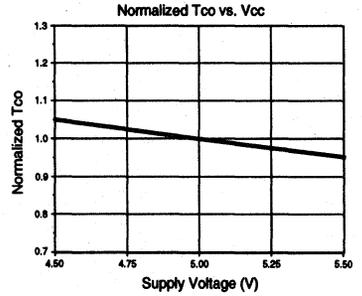
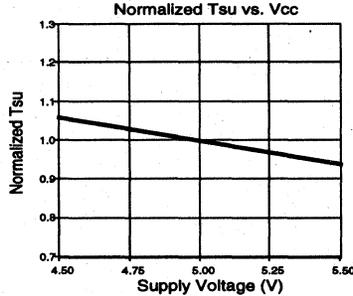
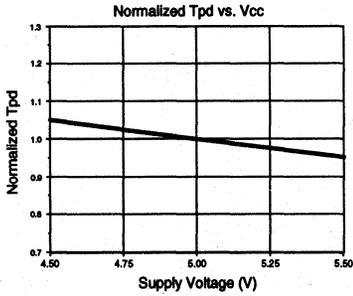


Delta Icc vs Vin (1 Input)



Input Clamp (Vik)





FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - F_{max} = 62.5 MHz
 - 10ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **LOW POWER CMOS**
 - 75 mA Typical I_{cc}
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Uses Standard 22V10 Macrocells
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

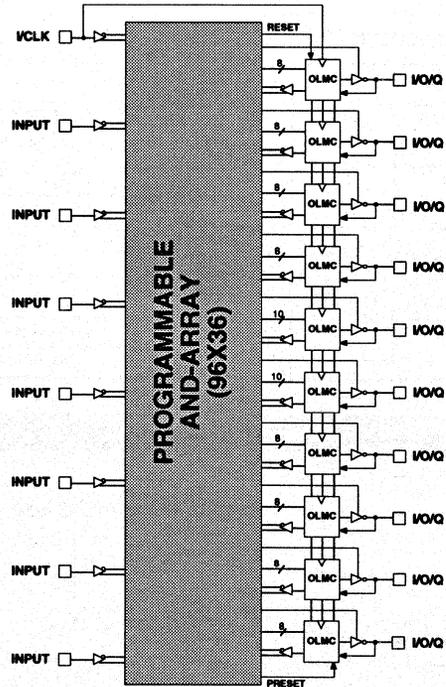
DESCRIPTION

The GAL18V10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide a very flexible 20-pin PLD. CMOS circuitry allows the GAL18V10 to consume much less power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

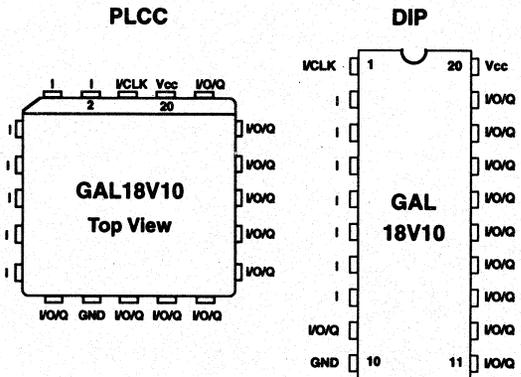
By building on the popular 22V10 architecture, the GAL18V10 eliminates the learning curve usually associated with a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL18V10 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



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GAL18V10 ORDERING INFORMATION

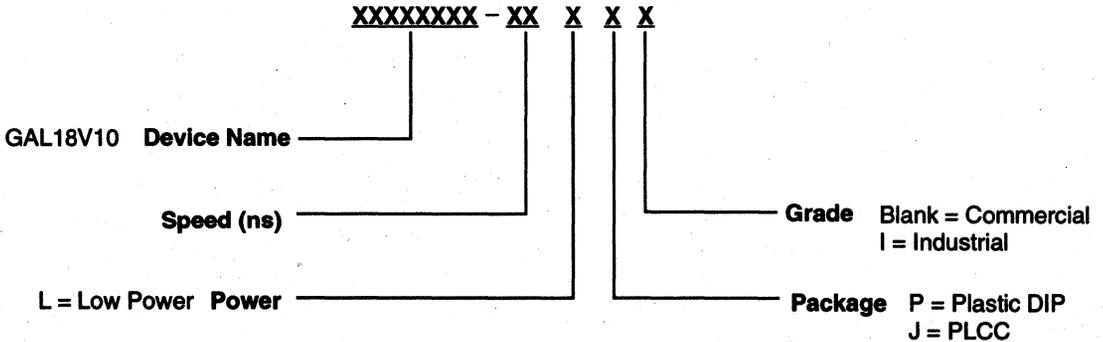
Commercial Grade Specifications

Tpd (ns)	Tau (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	115	GAL18V10-15LP	20-Pin Plastic DIP
			115	GAL18V10-15LJ	20-Lead PLCC
20	12	12	115	GAL18V10-20LP	20-Pin Plastic DIP
			115	GAL18V10-20LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	12	12	125	GAL18V10-20LPI	20-Pin Plastic DIP
			125	GAL18V10-20LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



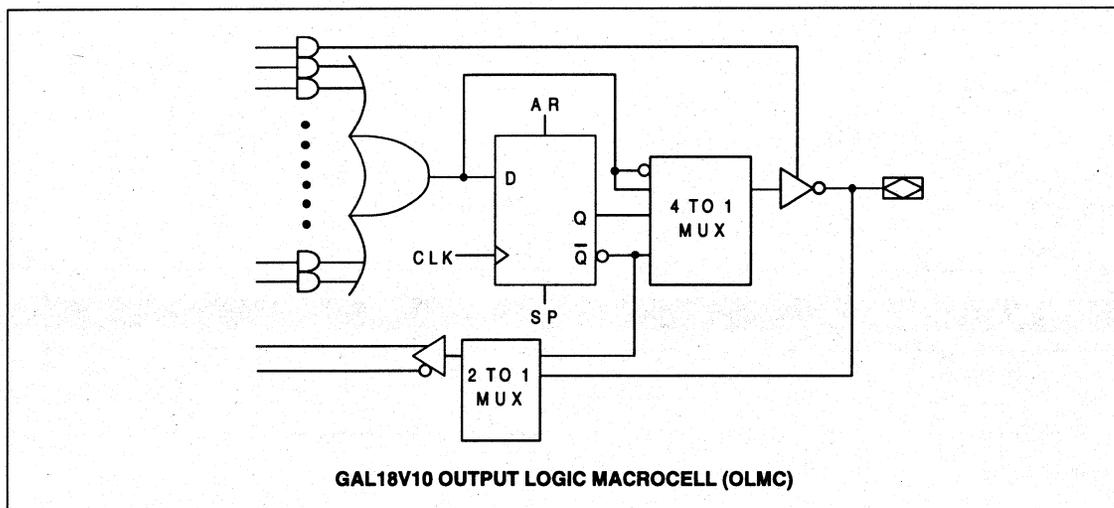
OUTPUT LOGIC MACROCELL (OLMC)

The GAL18V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to ten product terms (pins 14 and 15), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinational or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL18V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL18V10 has two primary functional modes: registered, and combinational I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

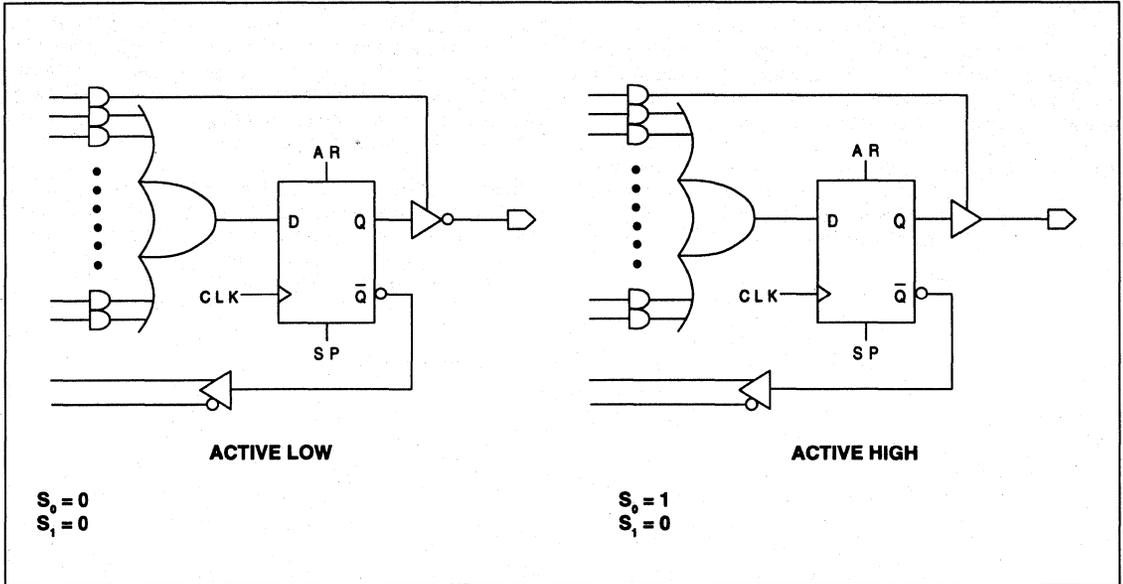
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinational pins.

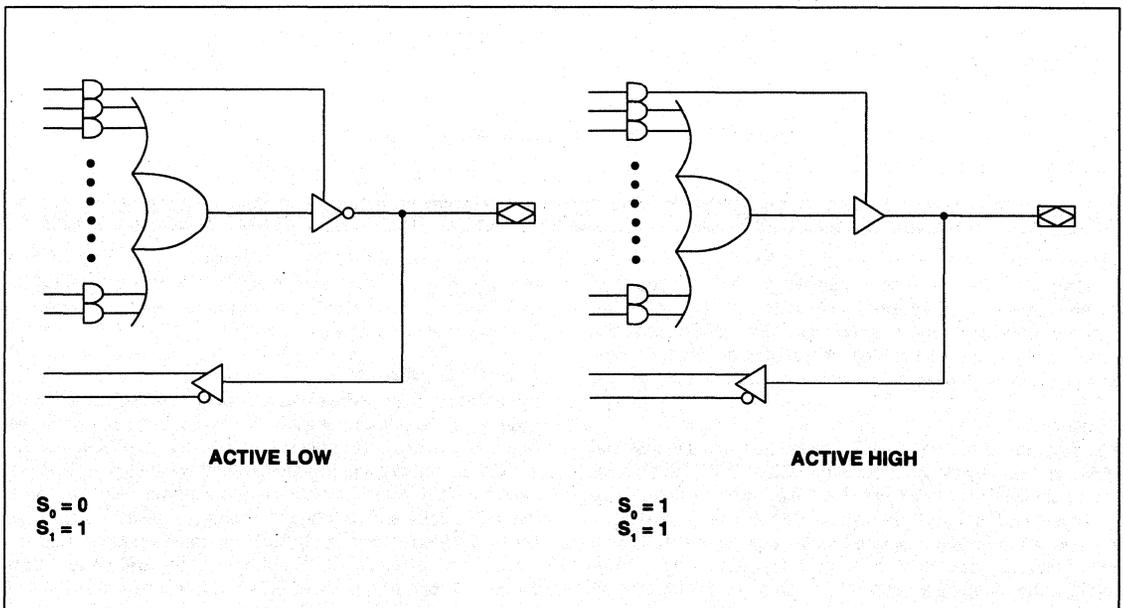
COMBINATORIAL I/O

In combinational mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

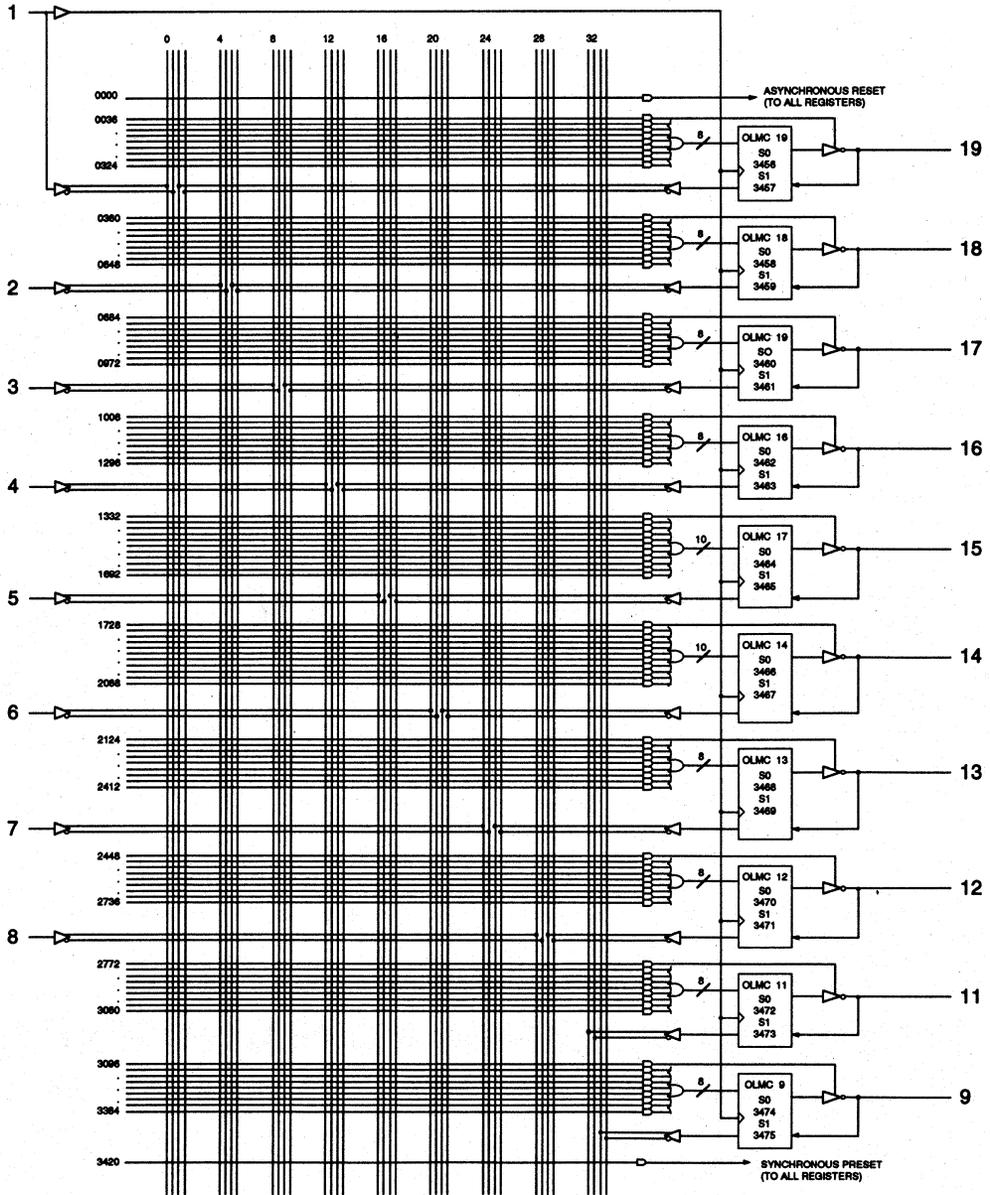
REGISTERED MODE



COMBINATORIAL MODE



GAL18V10 LOGIC DIAGRAM / JEDEC FUSE MAP



3476, 3477 ...	Electronic Signature	... 3638, 3639					
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
M	L						
S	S						

2



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	75	115	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	15	—	20	ns
t_{co}	1	Clock to Output Delay	—	10	—	12	ns
t_{cf}	—	Clock to Feedback Delay	—	7	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max} ³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	50	—	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	58.8	—	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
t_{rsw}	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
t_{rarr}	—	Asynchronous Reset to Clock Recovery Time	15	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

2



Specifications **GAL18V10** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with

Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C

Supply voltage (V_{CC})

with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \quad \text{Outputs Open}$	—	90	125	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

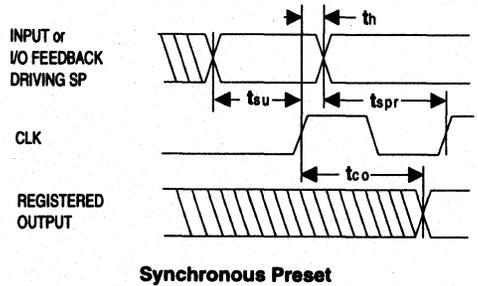
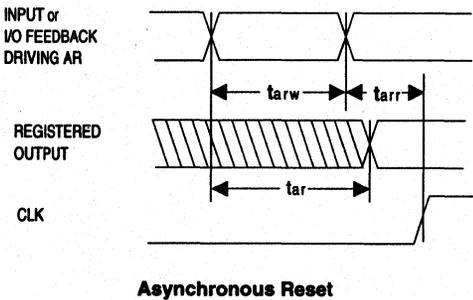
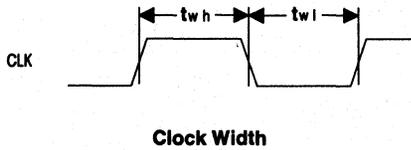
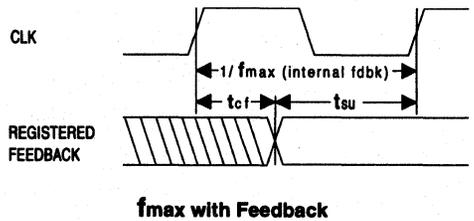
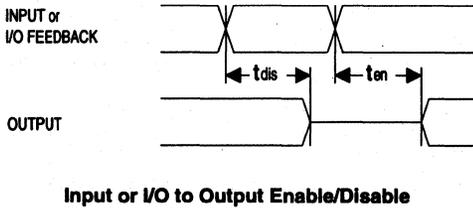
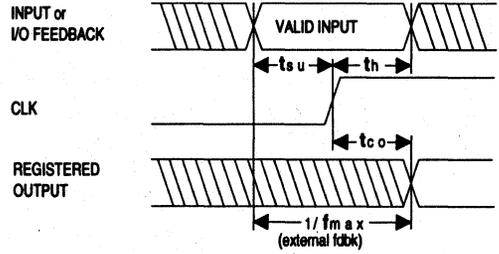
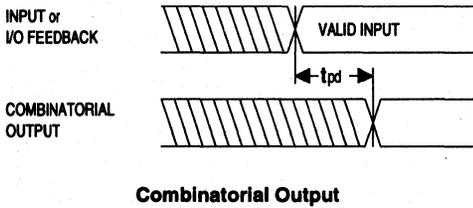
PARAMETER	TEST COND. ¹	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	ns
t_{co}	1	Clock to Output Delay	—	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.

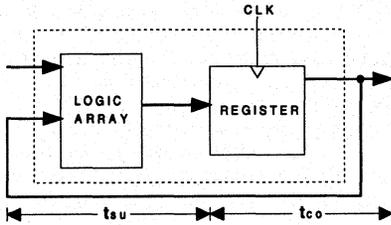
2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

SWITCHING WAVEFORMS

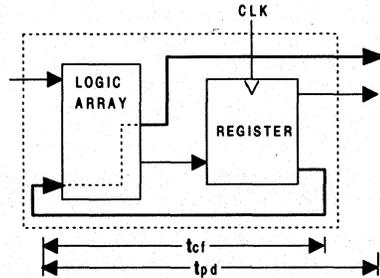


f_{max} DESCRIPTIONS



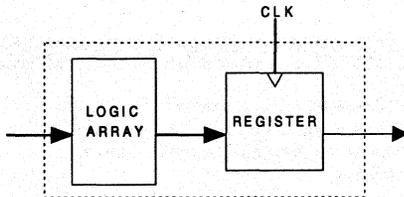
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

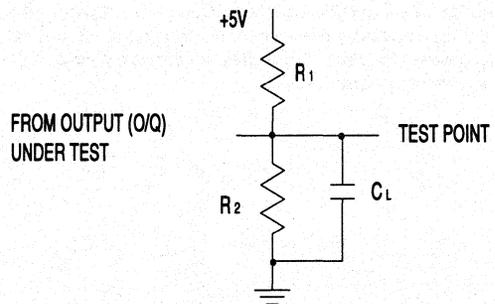
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L	
1	300Ω	390Ω	50pF	
2	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL18V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL18V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL18V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

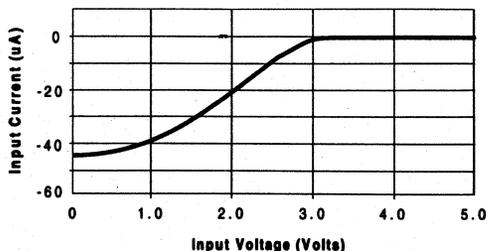
The GAL18V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

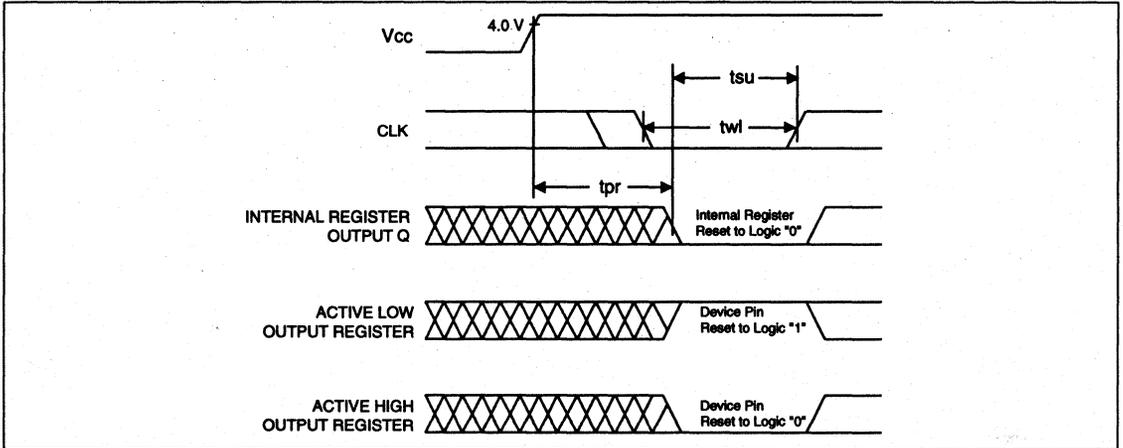
GAL18V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current



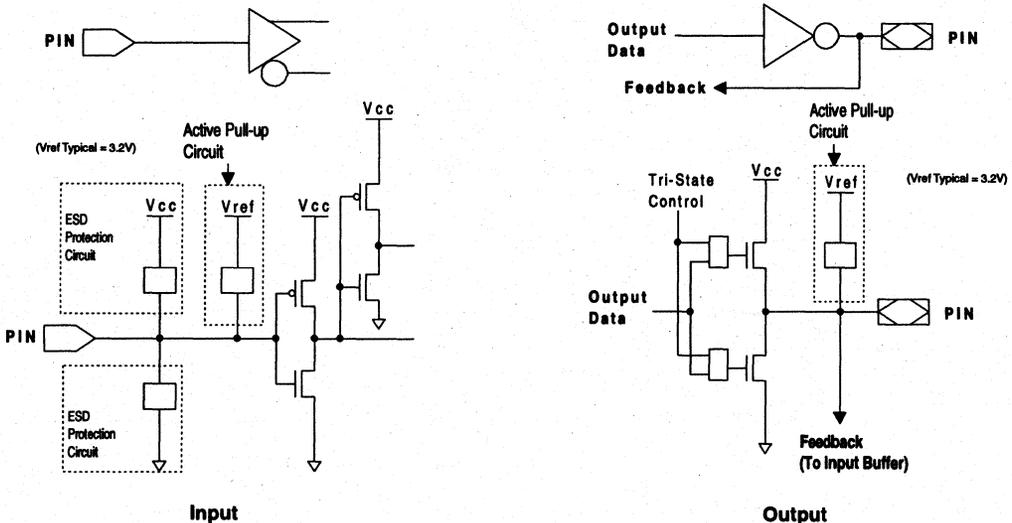
POWER-UP RESET

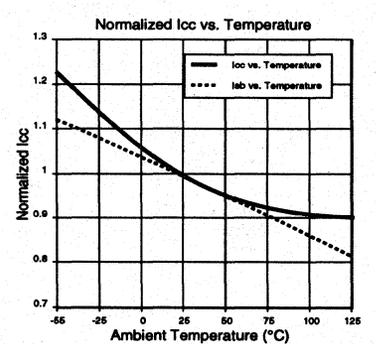
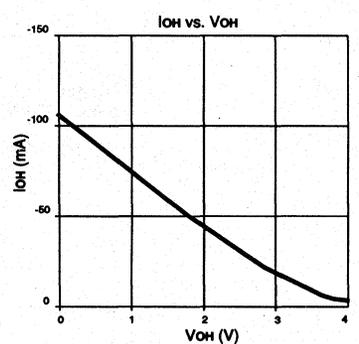
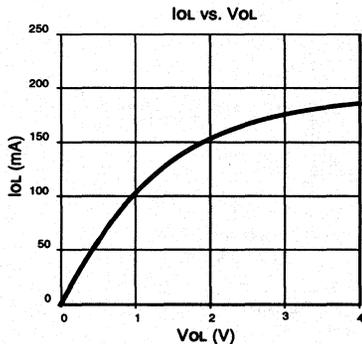
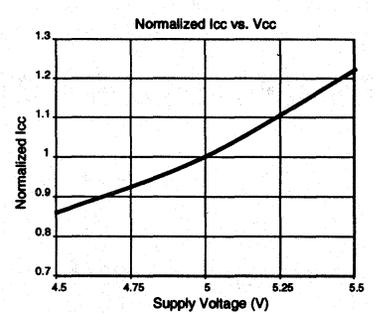
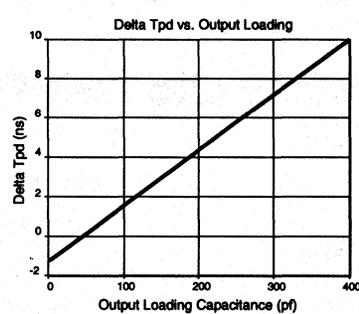
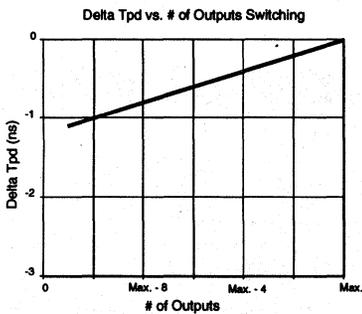
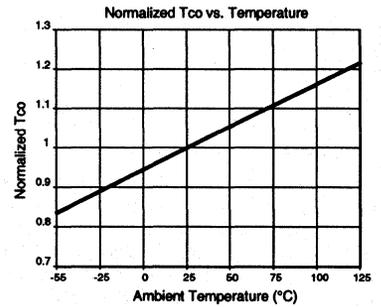
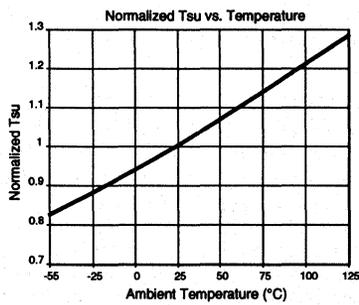
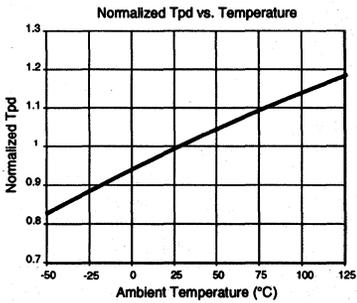
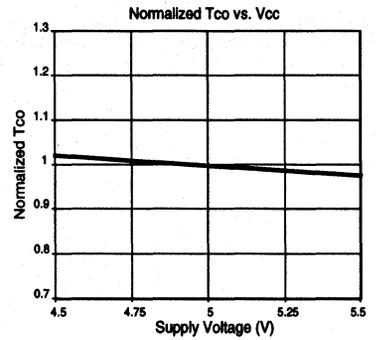
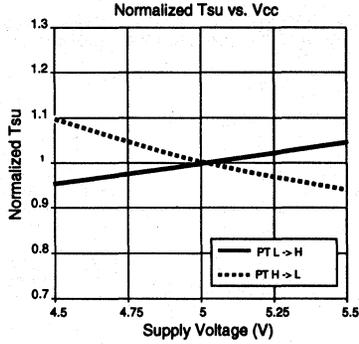
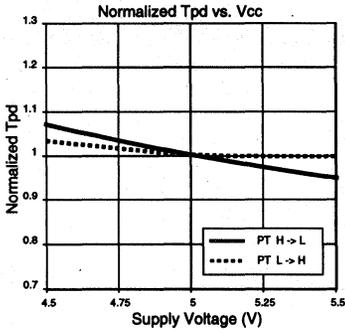


Circuitry within the GAL18V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS







GAL22V10B GAL22V10

High Performance E²CMOS PLD

FEATURES

- HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY
 - 7.5 ns Maximum Propagation Delay
 - F_{max} = 111 MHz
 - 5 ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- ACTIVE PULL-UPS ON ALL PINS
- COMPATIBLE WITH STANDARD 22V10 DEVICES
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMS 22V10 Devices
- 50% REDUCTION IN POWER VERSUS BIPOLAR
- E² CELL TECHNOLOGY
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
 - Maximum Flexibility for Complex Logic Designs
- PRELOAD AND POWER-ON RESET OF REGISTERS
 - 100% Functional Testability
- APPLICATIONS INCLUDE:
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

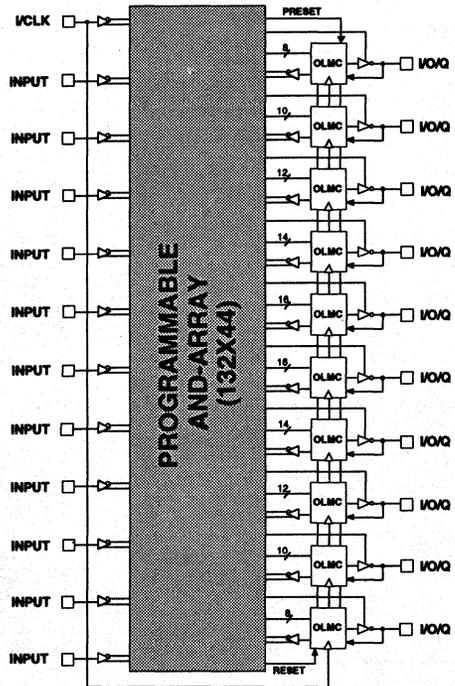
DESCRIPTION

The GAL22V10B, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10/B to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

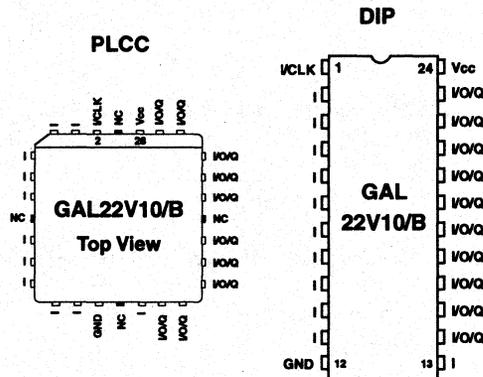
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10/B is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL[®] products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



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GAL22V10/B ORDERING INFORMATION

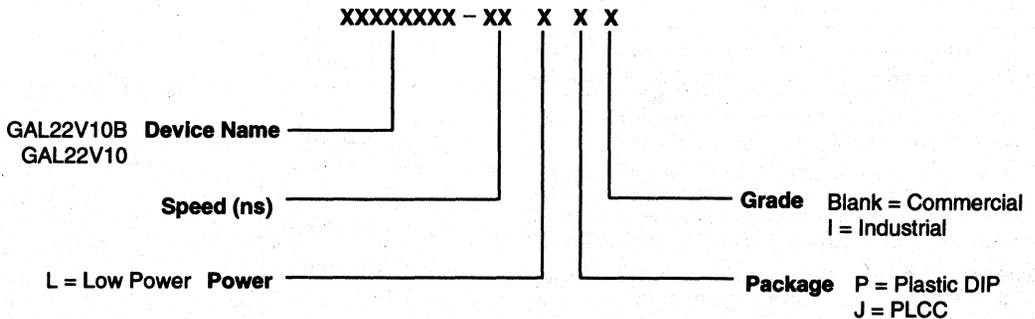
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6.5	5	140	GAL22V10B-7LP	24-Pin Plastic DIP
			140	GAL22V10B-7LJ	28-Lead PLCC
10	7	7	130	GAL22V10B-10LP	24-Pin Plastic DIP
			130	GAL22V10B-10LJ	28-Lead PLCC
15	10	8	130	GAL22V10B-15LP	24-Pin Plastic DIP
			130	GAL22V10B-15LJ	28-Lead PLCC
25	15	15	90	GAL22V10B-25LP	24-Pin Plastic DIP
			90	GAL22V10B-25LJ	28-Lead PLCC
			130	GAL22V10-25LP	24-Pin Plastic DIP
			130	GAL22V10-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	8	150	GAL22V10B-15LPI	24-Pin Plastic DIP
			150	GAL22V10B-15LJI	28-Lead PLCC
20	14	10	150	GAL22V10B-20LPI	24-Pin Plastic DIP
			150	GAL22V10B-20LJI	28-Lead PLCC
25	15	15	150	GAL22V10B-25LPI	24-Pin Plastic DIP
			150	GAL22V10B-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



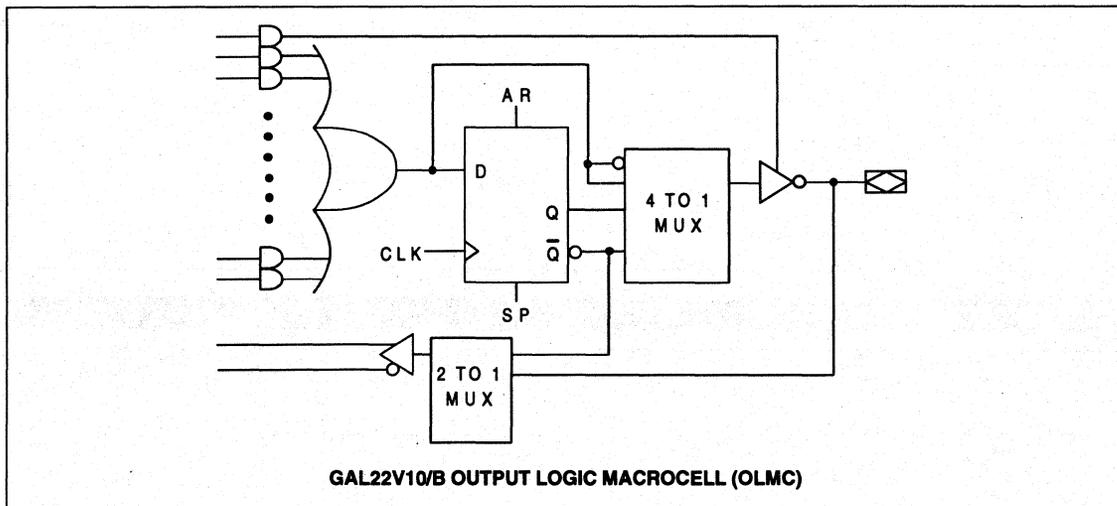
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22V10/B has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10/B has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22V10/B has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

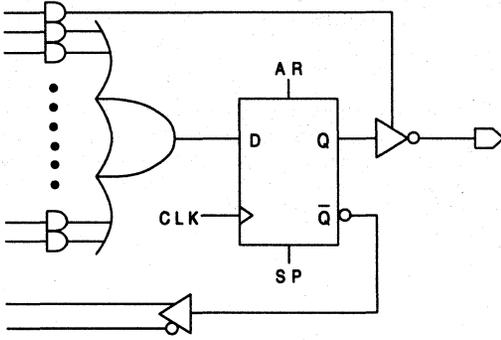
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

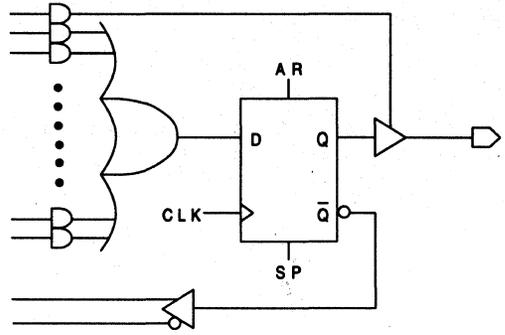
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

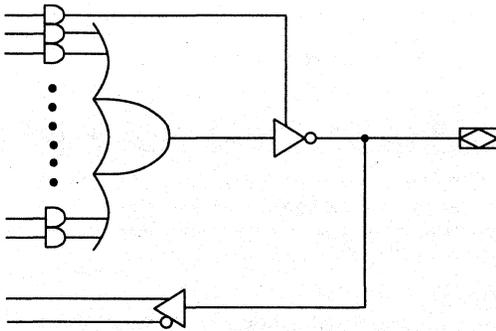
$S_0 = 0$
 $S_1 = 0$



ACTIVE HIGH

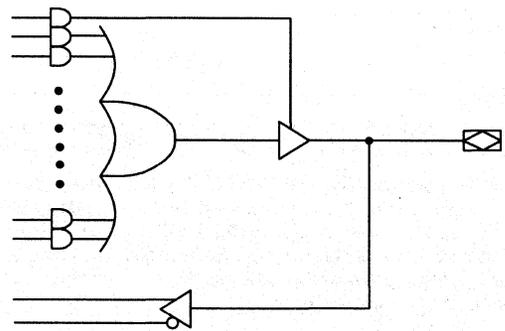
$S_0 = 1$
 $S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
 $S_1 = 1$

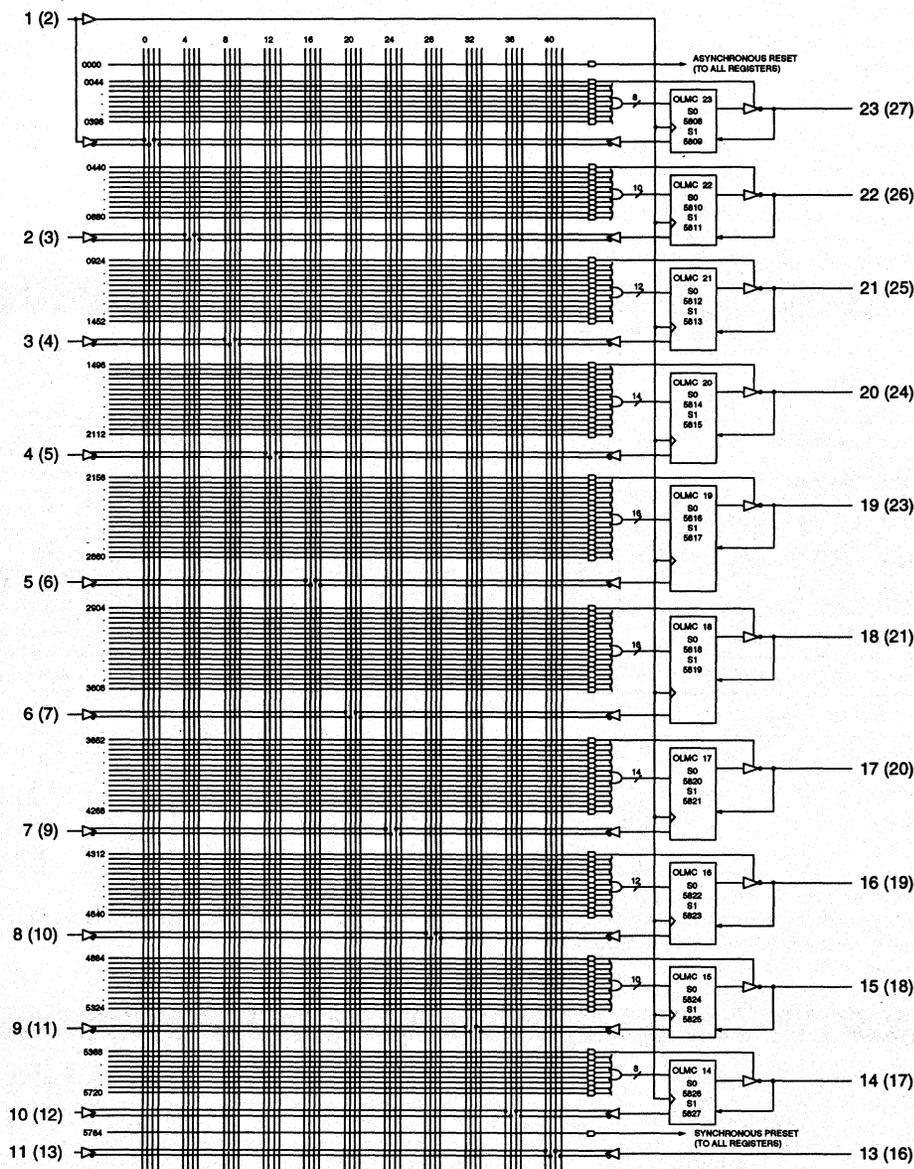


ACTIVE HIGH

$S_0 = 1$
 $S_1 = 1$

GAL22V10/B LOGIC DIAGRAM / JEDEC FUSE MAP

DIP (PLCC) Package Pinouts



5628 5629 Electronic Signature ...5600 5601
 Byte 7 Byte 6 Byte 5 Byte 4 Byte 3 Byte 2 Byte 1 Byte 0
 :
 :

2



Specifications **GAL22V10B** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Ambient Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS		
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V		
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V		
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA		
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA		
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V		
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V		
I_{OL}	Low Level Output Current		—	—	16	mA		
I_{OH}	High Level Output Current		—	—	-3.2	mA		
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA		
I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	$f_{toggle} = 25MHz$	-7	—	90	140	mA
	Supply Current	Outputs Open	$f_{toggle} = 25MHz$	-10/-15	—	90	130	mA
			$f_{toggle} = 15MHz$	-25	—	75	90	mA

- 1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{IO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-7		-10		-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	7.5	3	10	3	15	3	25	ns
t_{co}	1	Clock to Output Delay	2	5	2	7	2	8	2	15	ns
t_{cf}	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	—	13	ns
t_{su1}	—	Setup Time, Input or Feedback before Clock	6.5	—	7	—	10	—	15	—	ns
t_{su2}	—	Setup Time, SP before Clock	10	—	10	—	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	0	—	ns
f_{max} ³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	87	—	71.4	—	55.5	—	33.3	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	111	—	105	—	80	—	35.7	—	MHz
	1	Maximum Clock Frequency with No Feedback	111	—	105	—	83.3	—	38.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	4	—	6	—	13	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	4	—	6	—	13	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	8	3	10	3	15	3	25	ns
t_{dis}	3	Input or I/O to Output Disabled	3	8	3	9	3	15	3	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	13	3	13	3	20	3	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	8	—	15	—	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	8	—	8	—	10	—	25	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	10	—	10	—	15	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to f_{max} **Description** section.

3) Refer to f_{max} **Description** section.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-150	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \quad \text{Outputs Open}$	—	90	130	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
$C_{i/o}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{i/o} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-25		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	25	ns
t_{co}	1	Clock to Output Delay	2	15	ns
t_{cf}	—	Clock to Feedback Delay	—	13	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max} ²	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	33.3	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	35.7	—	MHz
	1	Maximum Clock Frequency with No Feedback	38.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	13	—	ns
t_{wl}	—	Clock Pulse Duration, Low	13	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	25	ns
t_{dis}	3	Input or I/O to Output Disabled	3	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	25	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	15	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL} ¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS} ²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA
I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	—	90	150	mA
	Supply Current	Outputs Open				

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

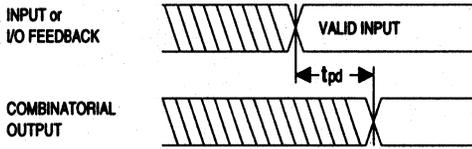
PARAMETER	TEST COND. ¹	DESCRIPTION	-15		-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	15	3	20	3	25	ns
t_{co}	1	Clock to Output Delay	2	8	2	10	2	25	ns
t_{cf}²	—	Clock to Feedback Delay	—	5	—	8	—	13	ns
t_{su1}	—	Setup Time, Input or Feedback before Clock	10	—	14	—	15	—	ns
t_{su2}	—	Setup Time, SP before Clock	12	—	14	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55.5	—	41.6	—	33	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	66.6	—	45.4	—	35.7	—	MHz
	1	Maximum Clock Frequency with No Feedback	66.6	—	50	—	38.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	10	—	13	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	10	—	13	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	15	3	20	3	25	ns
t_{dis}	3	Input or I/O to Output Disabled	3	15	3	20	3	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	20	3	25	3	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	20	—	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	10	—	20	—	25	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	14	—	15	—	ns

1) Refer to **Switching Test Conditions** section.

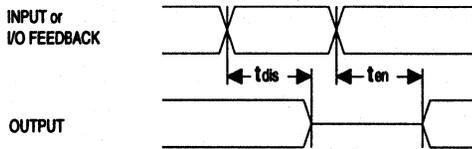
2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

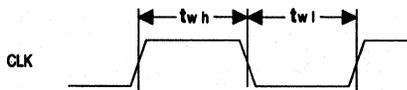
SWITCHING WAVEFORMS



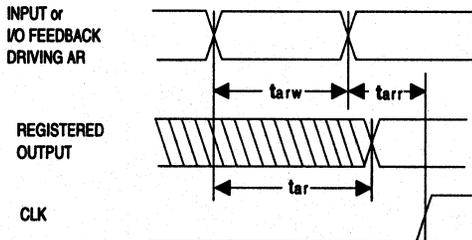
Combinatorial Output



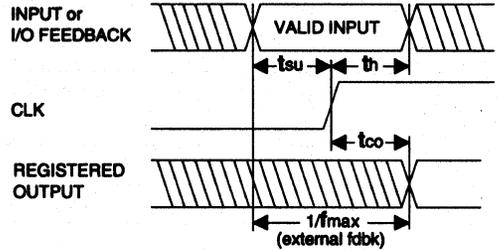
Input or I/O to Output Enable/Disable



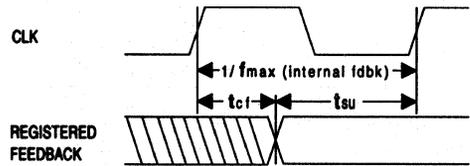
Clock Width



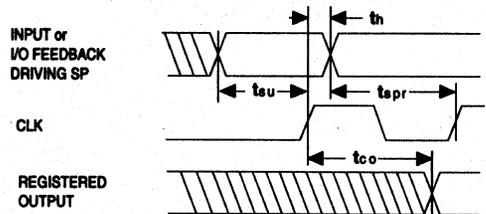
Asynchronous Reset



Registered Output

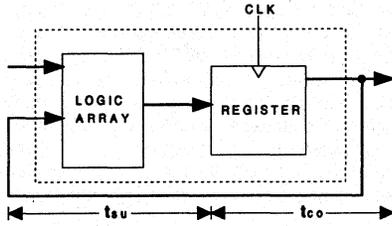


fmax with Feedback



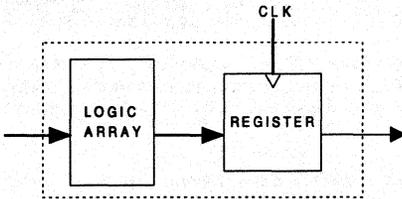
Synchronous Preset

f_{max} DESCRIPTIONS



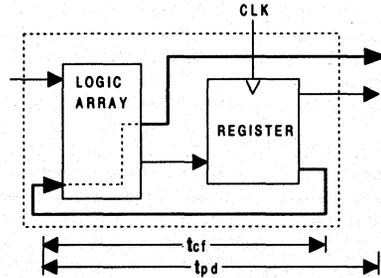
f_{max} with External Feedback $1/(t_{su} + t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su} + t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/ internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

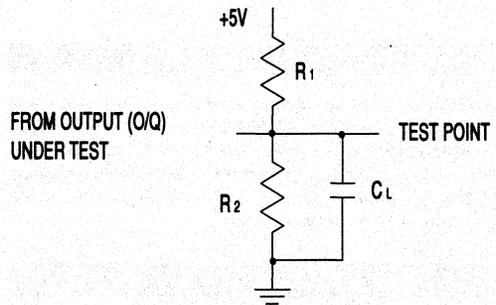
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2 – 3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	390Ω
	Active Low	300Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL22V10/B device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10/B contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10/B device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22V10/B device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL22V10/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

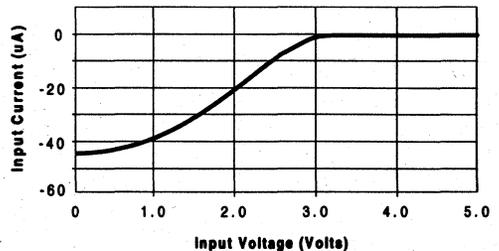
The GAL22V10/B device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

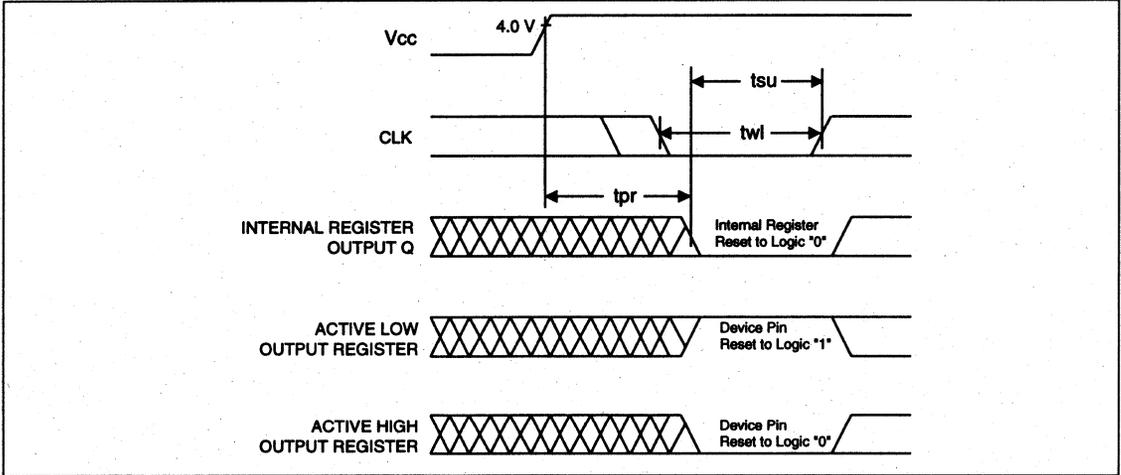
GAL22V10/B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current



POWER-UP RESET

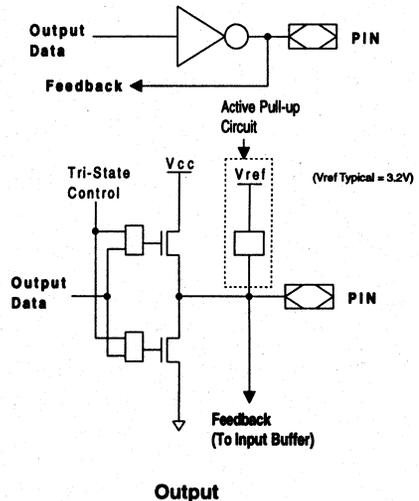
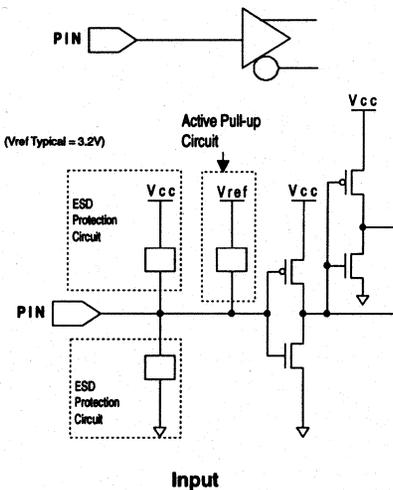


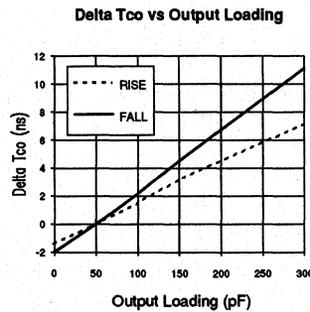
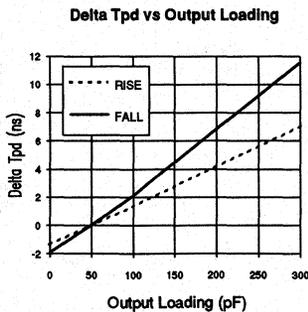
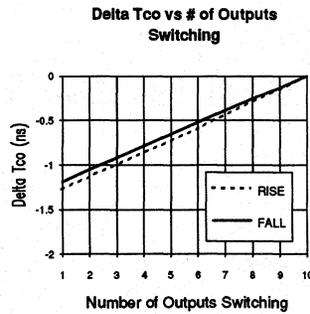
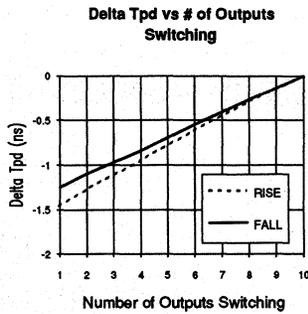
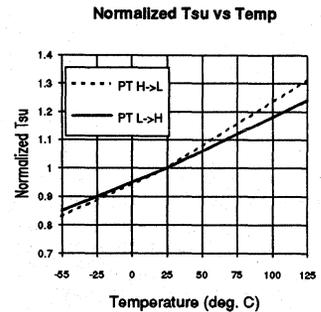
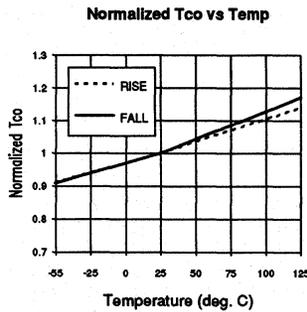
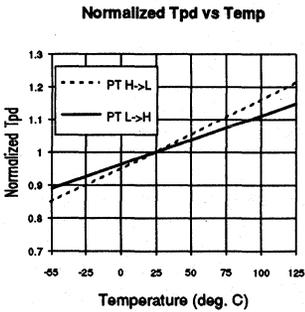
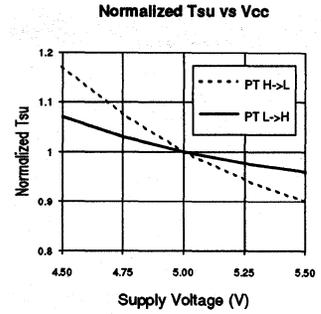
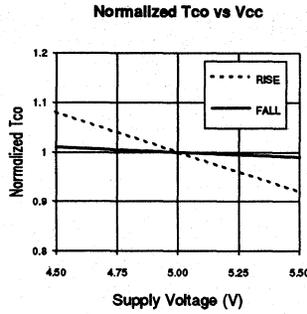
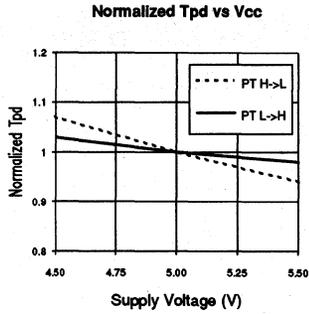
2

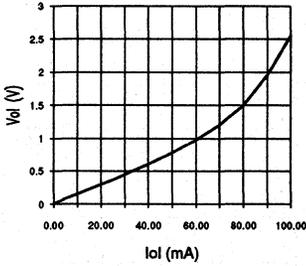
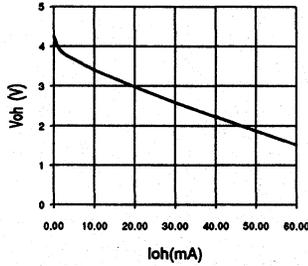
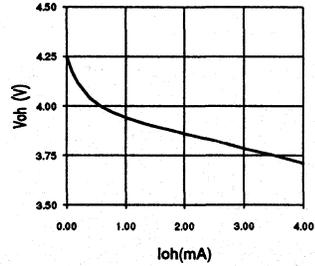
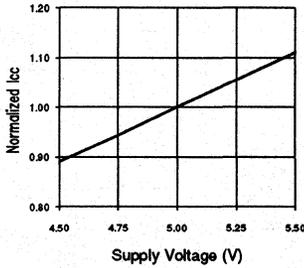
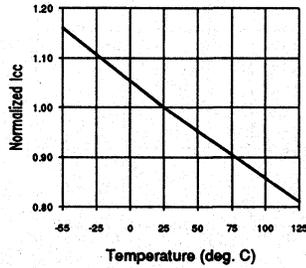
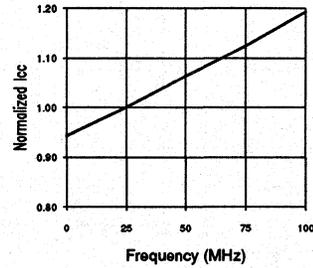
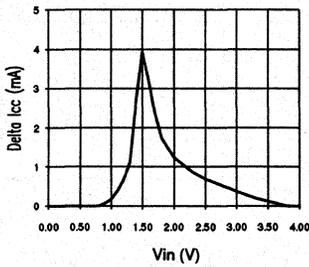
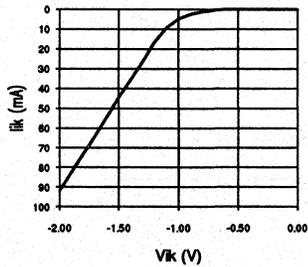
Circuitry within the GAL22V10/B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

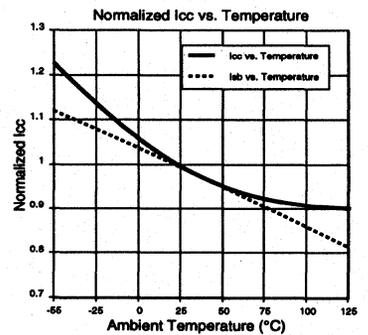
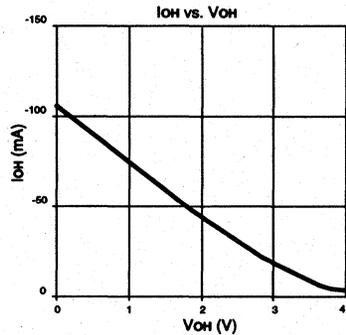
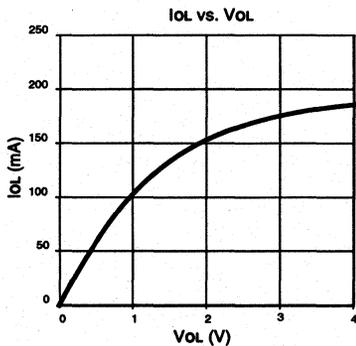
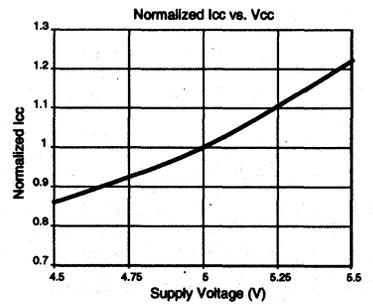
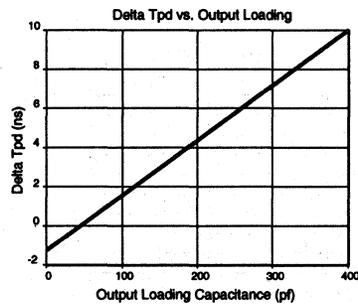
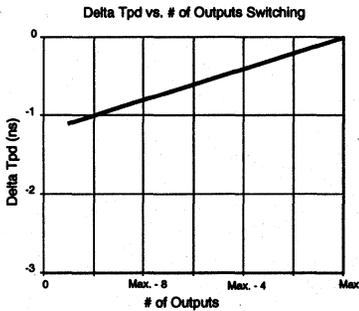
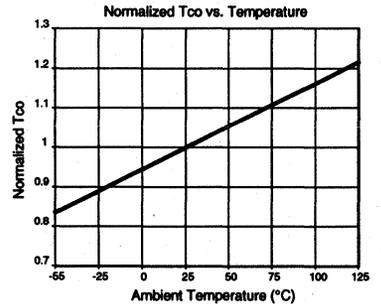
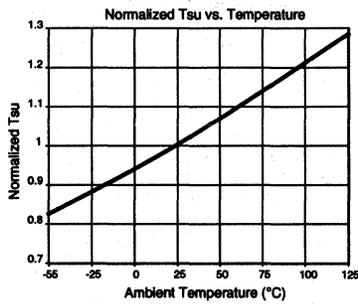
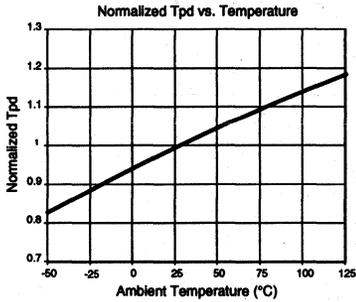
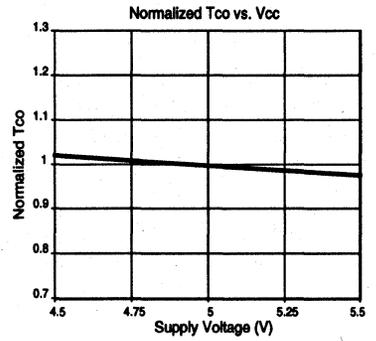
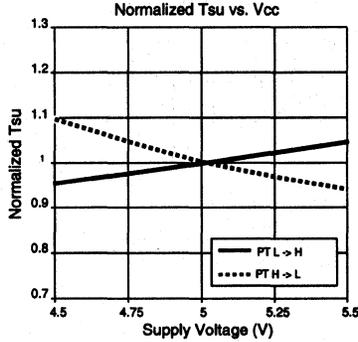
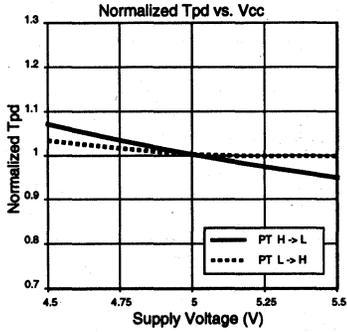
conditions must be met to guarantee a valid power-up reset of the device. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS





Vol vs Iol

Voh vs Ioh

Voh vs Ioh

Normalized Icc vs Vcc

Normalized Icc vs Temp

Normalized Icc vs Freq.

Delta Icc vs Vin (1 input)

Input Clamp (Vik)






GAL26CV12B GAL26CV12

High Performance E²CMOS PLD

FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - F_{max} = 105 MHz
 - 7ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
 - 90 mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TWELVE OUTPUT LOGIC MACROCELLS**
 - Uses Standard 22V10 Macrocells
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

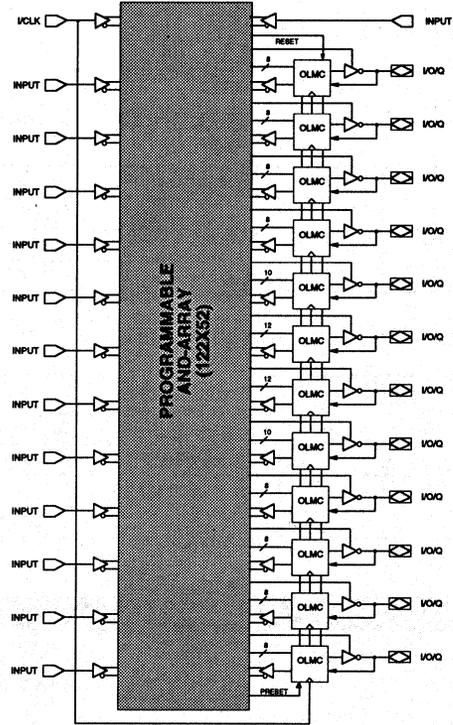
DESCRIPTION

The GAL26CV12B, at 10 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 28 pin PLD available on the market. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

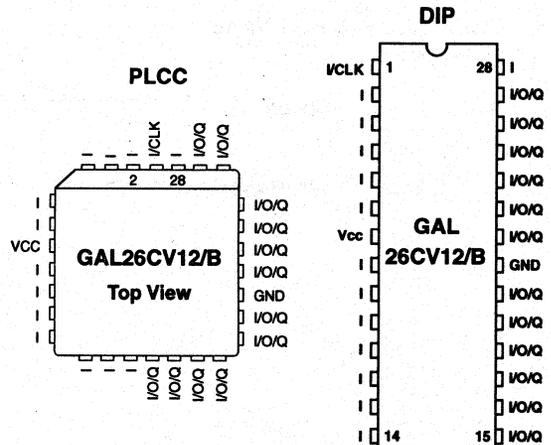
Expanding upon the industry standard 22V10 architecture, the GAL26CV12/B eliminates the learning curve typically associated with a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12/B OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL[®] products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



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GAL26CV12/B ORDERING INFORMATION

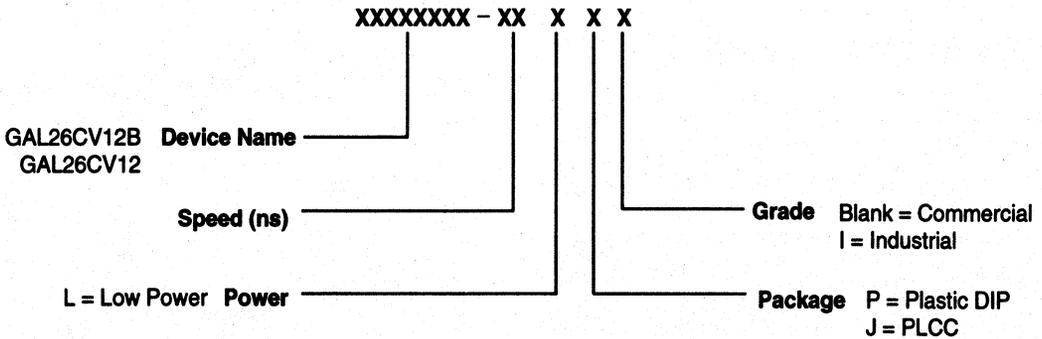
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	130	GAL26CV12B-10LP	28-Pin Plastic DIP
			130	GAL26CV12B-10LJ	28-Lead PLCC
15	10	10	130	GAL26CV12-15LP	28-Pin Plastic DIP
			130	GAL26CV12-15LJ	28-Lead PLCC
20	12	12	130	GAL26CV12-20LP	28-Pin Plastic DIP
			130	GAL26CV12-20LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	150	GAL26CV12B-15LPI	28-Pin Plastic DIP
			150	GAL26CV12B-15LJI	28-Lead PLCC
20	12	12	150	GAL26CV12-20LPI	28-Pin Plastic DIP
			150	GAL26CV12-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



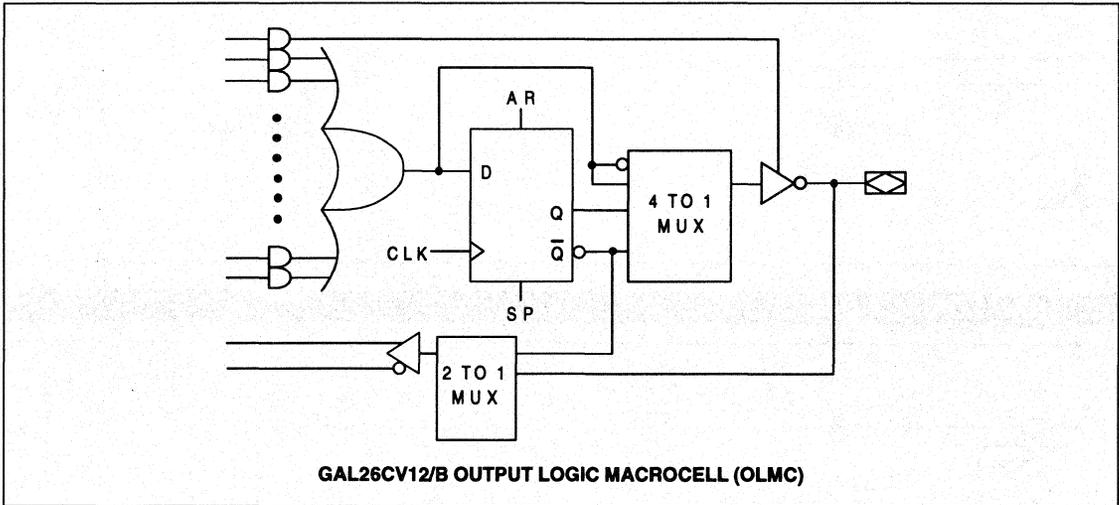
OUTPUT LOGIC MACROCELL (OLMC)

The GAL26CV12/B has a variable number of product terms per OLMC. Of the twelve available OLMCs, two OLMCs have access to twelve product terms (pins 20 and 22), two have access to ten product terms (pins 19 and 23), and the other six OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL26CV12/B has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL26CV12/B has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (S0 and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

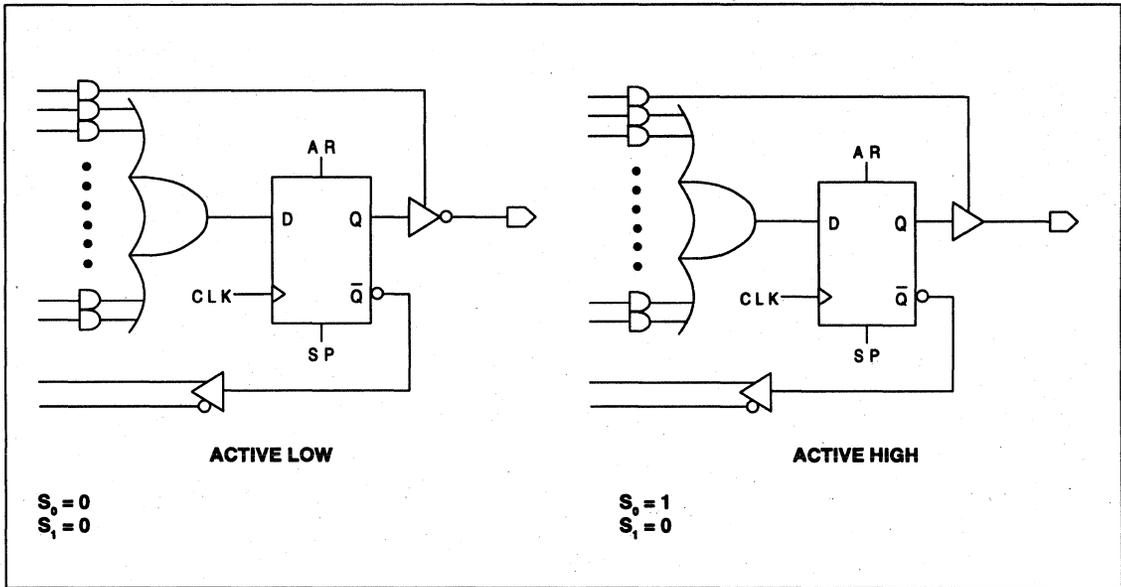
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

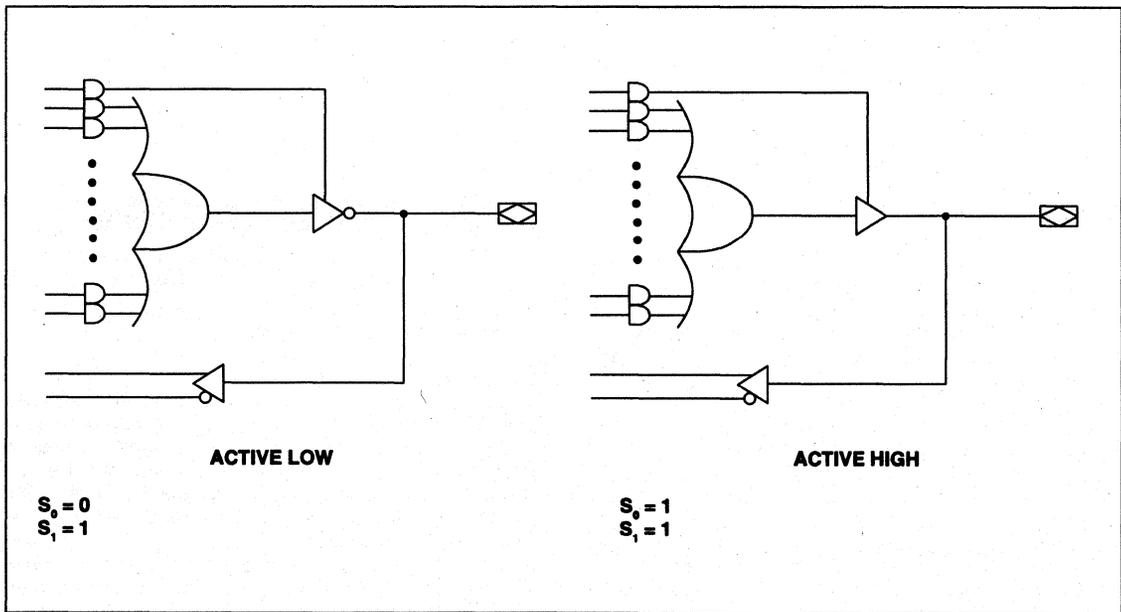
COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

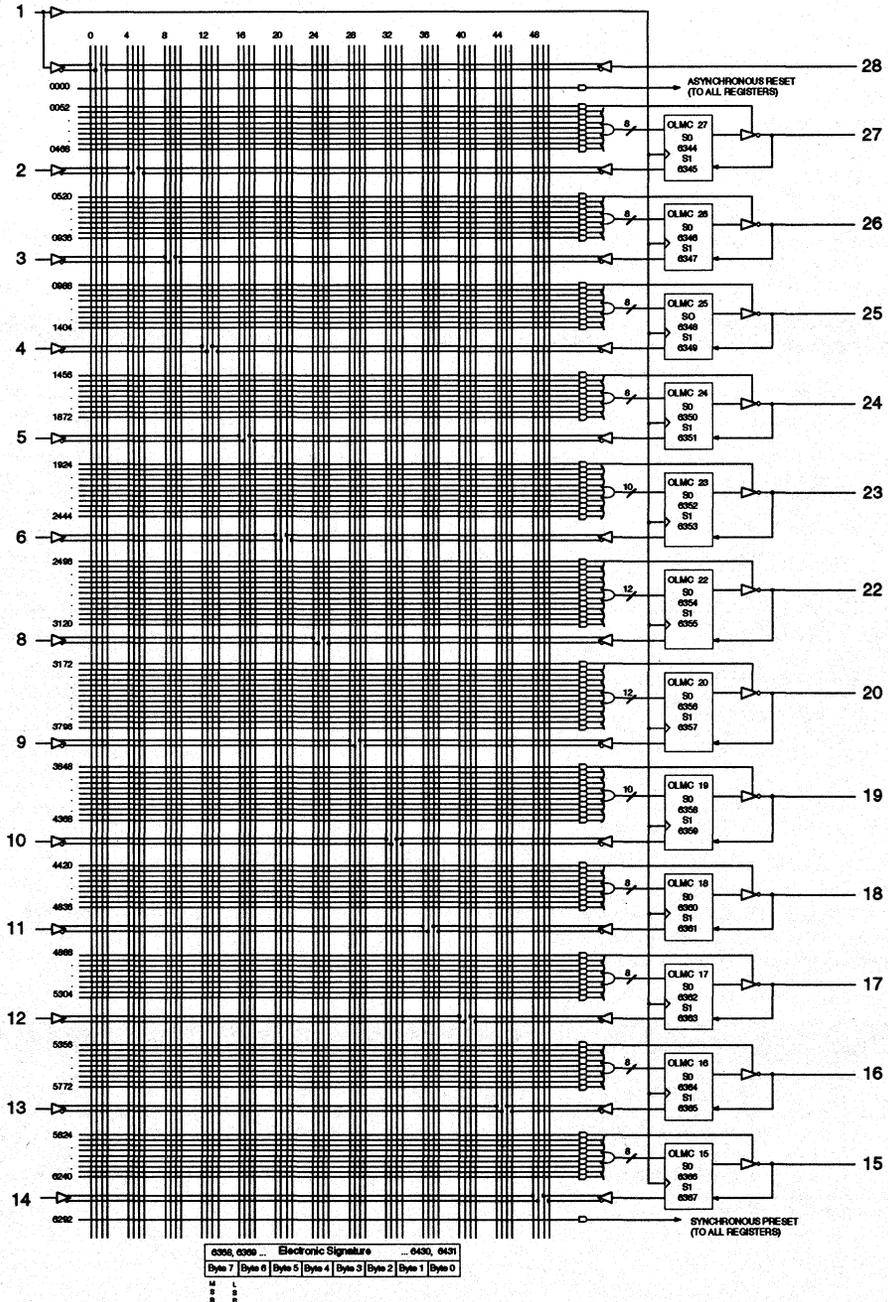
REGISTERED MODE



COMBINATORIAL MODE



GAL26CV12/B LOGIC DIAGRAM / JEDEC FUSE MAP



2



Specifications **GAL26CV12B** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	90	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{io}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-10		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	10	ns
t_{co}	1	Clock to Output Delay	2	7	ns
t_{cf}^2	—	Clock to Feedback Delay	—	2.5	ns
t_{su_1}	—	Setup Time, Input or Feedback before Clock	7	—	ns
t_{su_2}	—	Setup Time, SP before Clock	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	71.4	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	105	—	MHz
	1	Maximum Clock Frequency with No Feedback	105	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	10	ns
t_{dis}	3	Input or I/O to Output Disabled	3	10	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	13	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	8	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

3) Refer to **f_{max} Specification** section.



Specifications **GAL26CV12** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V V_{OUT} = 0.5V T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \text{ Outputs Open}$	—	90	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	15	—	20	ns
t_{co}	1	Clock to Output Delay	—	10	—	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	7	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	50	—	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	58.8	—	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.



Specifications **GAL26CV12B** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.5 to +5.5V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input buffer section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	15	ns
t_{co}	1	Clock to Output Delay	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	50	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	58.8	—	MHz
	1	Maximum Clock Frequency with No Feedback, 1/(t _{wh} + t _{wl})	62.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	15	ns
t_{dis}	3	Input or I/O to Output Disabled	3	15	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	10	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	ns

2

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

3) Refer to **f_{max} Specification** section.



Specifications **GAL26CV12** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
 Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	90	150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

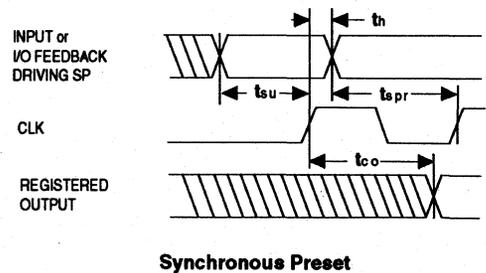
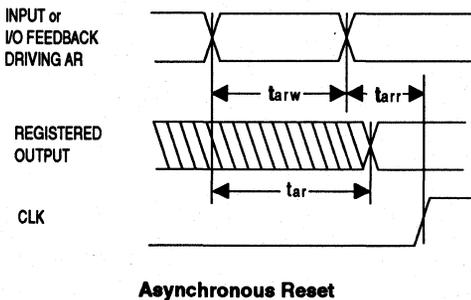
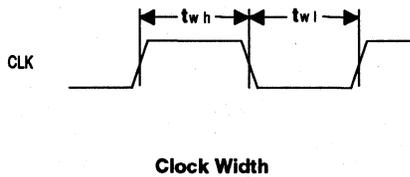
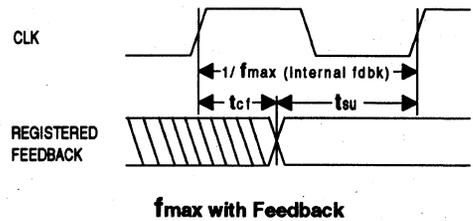
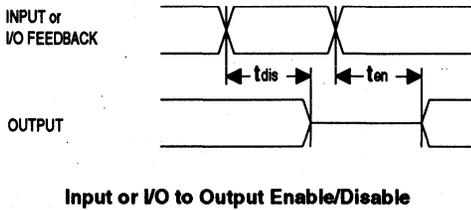
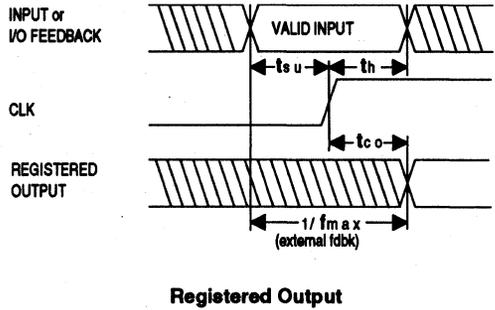
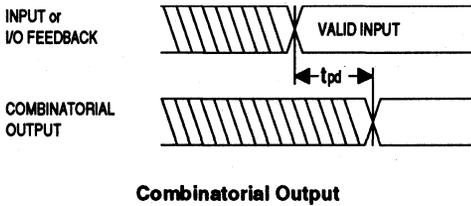
PARAMETER	TEST COND. ¹	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	ns
t_{co}	1	Clock to Output Delay	—	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.

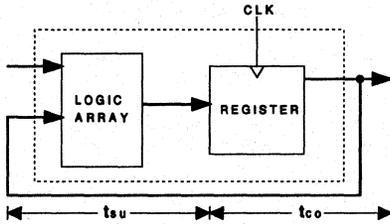
2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

SWITCHING WAVEFORMS

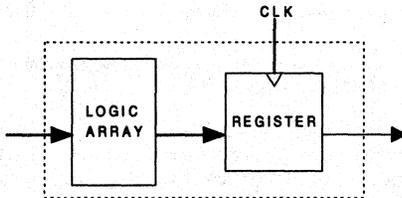


f_{max} SPECIFICATIONS



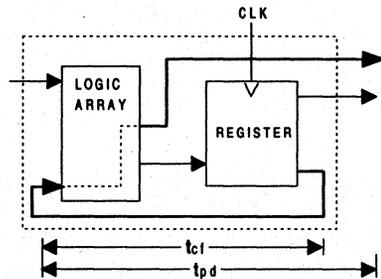
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



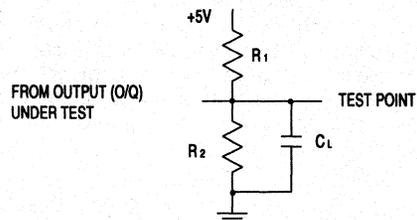
f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: tcf is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to tcf + tpd.

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

GAL26CV12 Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	470Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	470Ω	390Ω
3	Active High	∞	5pF
	Active Low	470Ω	390Ω

GAL26CV12B Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	5pF
	Active Low	300Ω	390Ω

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL26CV12/B device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL26CV12/B device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL26CV12/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

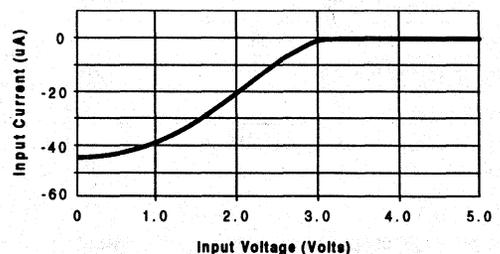
The GAL26CV12/B device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

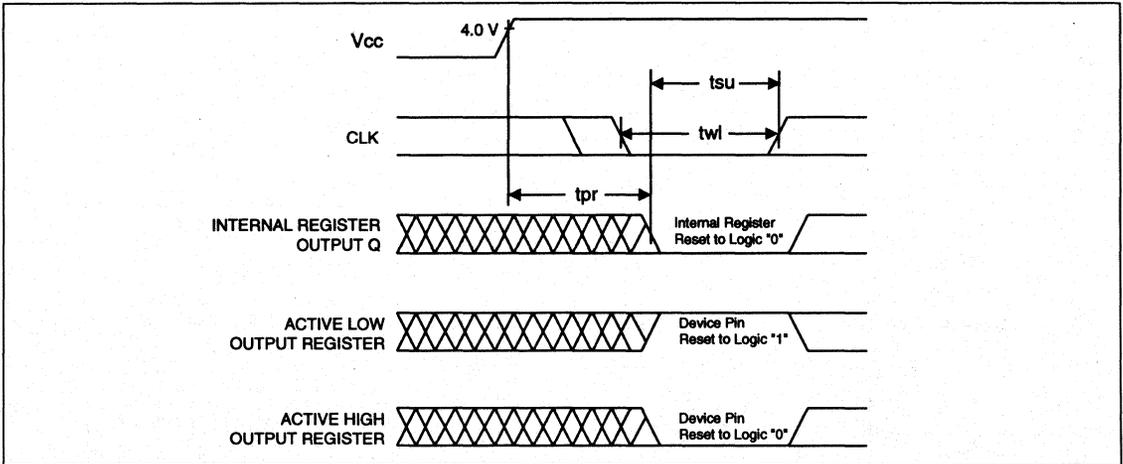
GAL26CV12/B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL logic.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce lcc for the device.

Typical Input Current



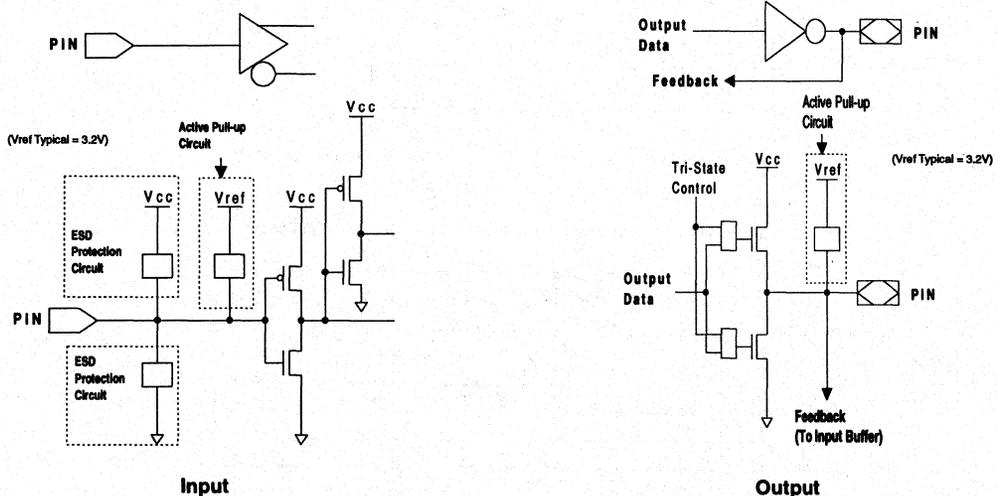
POWER-UP RESET



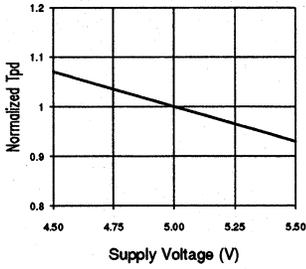
Circuitry within the GAL26CV12/B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

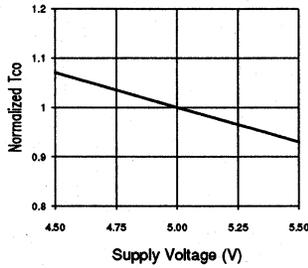
INPUT/OUTPUT EQUIVALENT SCHEMATICS



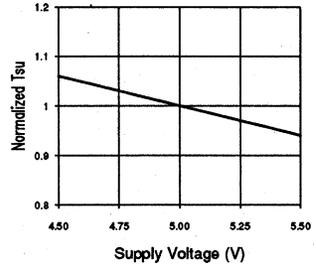
Normalized Tpd vs Vcc



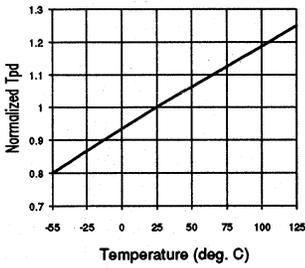
Normalized Tco vs Vcc



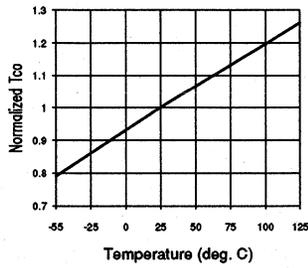
Normalized Tsu vs Vcc



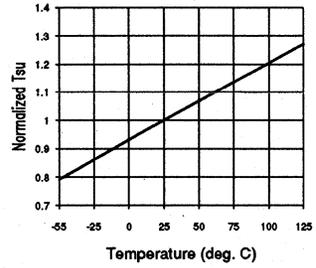
Normalized Tpd vs Temp



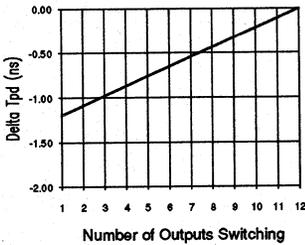
Normalized Tco vs Temp



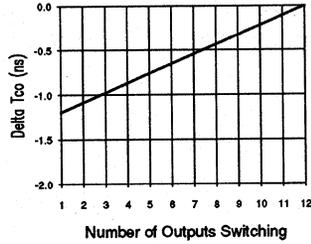
Normalized Tsu vs Temp



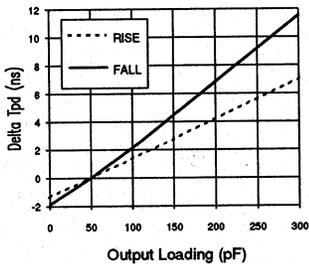
Delta Tpd vs # of Outputs Switching



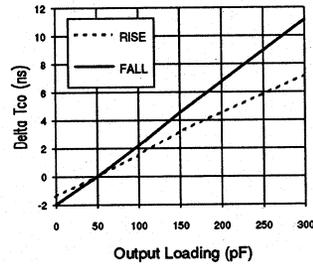
Delta Tco vs # of Outputs Switching



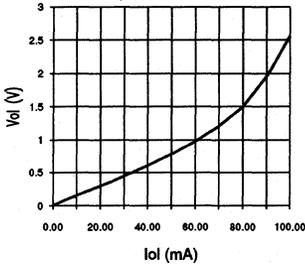
Delta Tpd vs Output Loading



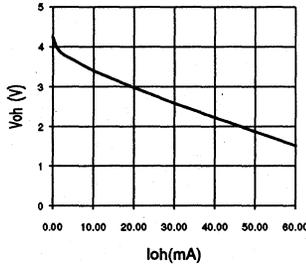
Delta Tco vs Output Loading



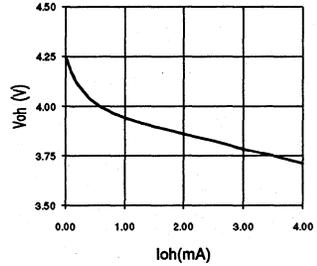
Vol vs Iol



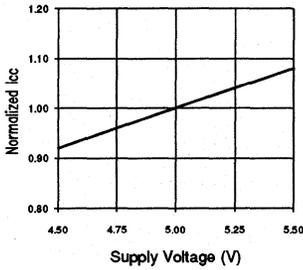
Voh vs Ioh



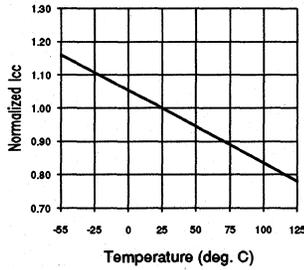
Voh vs Ioh



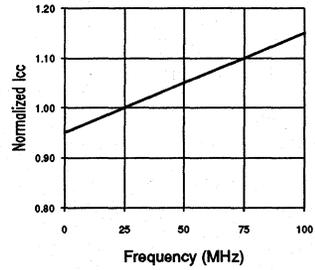
Normalized Icc vs Vcc



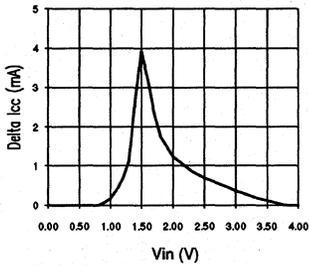
Normalized Icc vs Temp



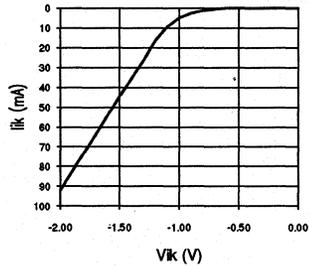
Normalized Icc vs Freq.



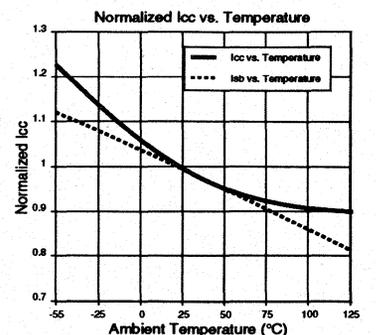
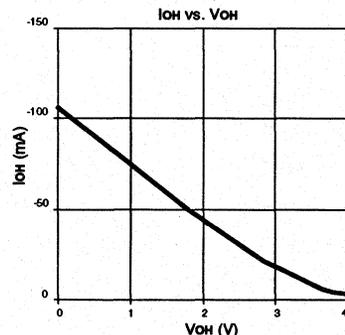
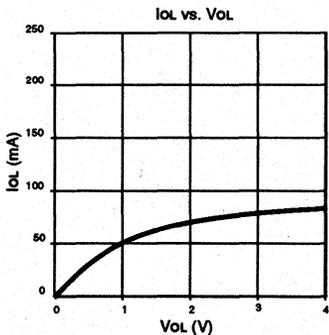
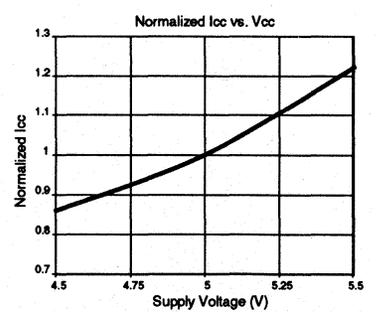
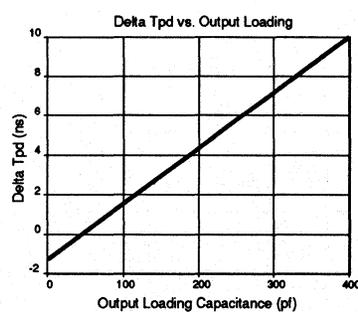
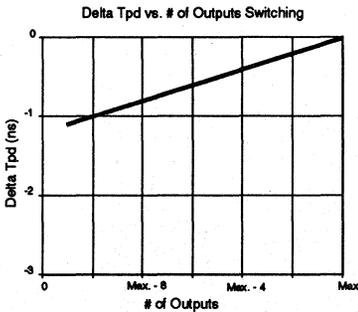
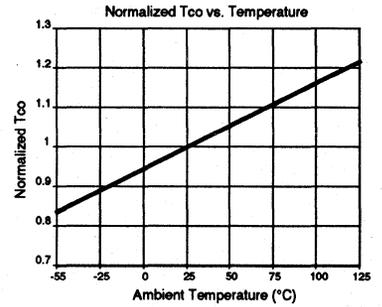
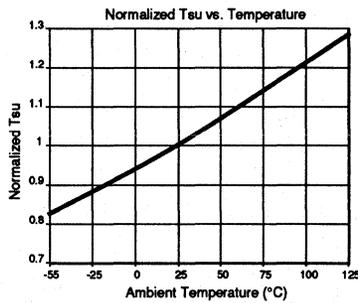
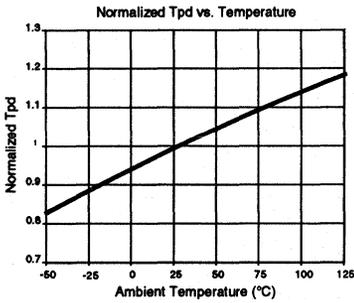
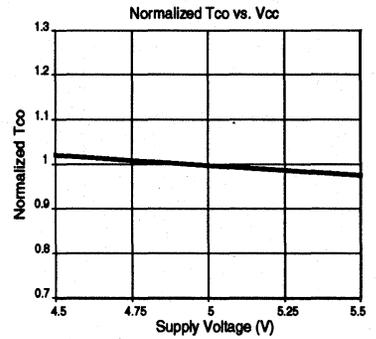
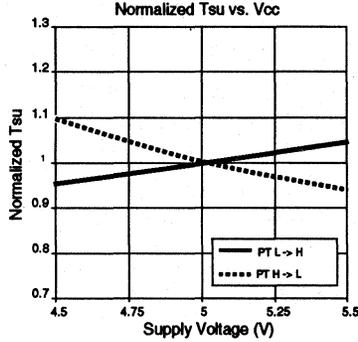
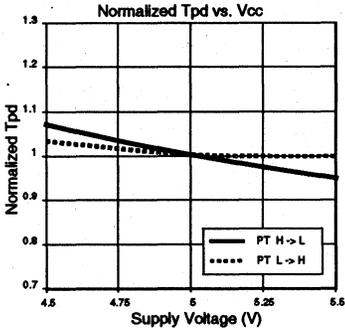
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



2



GAL20XV10B ORDERING INFORMATION

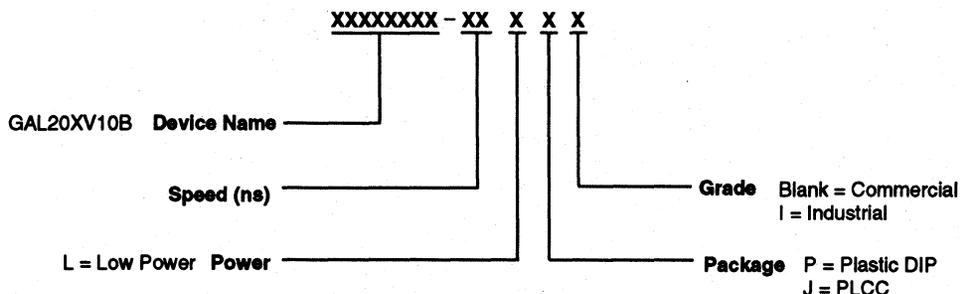
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	6	7	90	GAL20XV10B-10LP	24-Pin Plastic DIP
				GAL20XV10B-10LJ	28-Lead PLCC
15	8	8	90	GAL20XV10B-15LP	24-Pin Plastic DIP
				GAL20XV10B-15LJ	28-Lead PLCC
20	10	10	90	GAL20XV10B-20LP	24-Pin Plastic DIP
				GAL20XV10B-20LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	8	110	GAL20XV10B-15LPI	24-Pin Plastic DIP
				GAL20XV10B-15LJI	28-Lead PLCC
20	10	10	110	GAL20XV10B-20LPI	24-Pin Plastic DIP
				GAL20XV10B-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the Output Logic Macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The GAL20XV10B has two global architecture configurations that allow it to emulate PAL architectures. The Input mode emulates combinatorial PAL devices, with the I/CLK and I/OE pins used as inputs. The Feedback mode emulates registered PAL devices with the I/CLK pin used as the register clock and the I/OE pin as an output enable for all registers. The following is a list of PAL architectures that the GAL20XV10B can emulate. It also shows the global architecture mode used to emulate the PAL architecture.

PAL Architectures Emulated by GAL20XV10B	GAL20XV10B Global OLMC Mode
PAL12L10	Input Mode
PAL20L10	Input Mode
PAL20X10	Feedback Mode
PAL20X8	Feedback Mode
PAL20X4	Feedback Mode

INPUT MODE

The Input mode architecture is defined when the global architecture bit SYN = 1. In this mode, the I/CLK pin becomes an input to the AND array and also provides the clock source for all registers. The I/OE pin becomes an input into the AND array and provides the output enable control for any macrocell configured as an Exclusive-OR function. Feedback into the AND array is provided from macrocells 2 through 9 only. In this mode, macrocells 1 and 10 have no feedback into the AND array.

FEEDBACK MODE

The Feedback mode architecture is defined when the global architecture bit SYN = 0. In this mode the I/CLK pin becomes a dedicated clock source for all registers. The I/OE pin is a dedicated output enable control for any macrocell configured as an Exclusive-OR function. The I/CLK and I/OE pins are not available to the AND array in this mode. Feedback into the AND array is provided on all macrocells 1 through 10.

FEATURES

Each Output Logic Macrocell has four possible logic function configurations controlled by architecture control bits AC0 and AC1. Four product terms are fed into each macrocell.

XOR REGISTERED CONFIGURATION

The Macrocell is set to the Exclusive-OR Registered configuration when AC0 = 0 and AC1 = 0. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register. The register is clocked by the low-to-high transition of the I/CLK pin. The inverting output buffer is enabled by the I/

OE pin, which is an active low output enable common to all Exclusive-OR macrocells. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

REGISTERED CONFIGURATION

The Macrocell is set to Registered configuration when AC0 = 1 and AC1 = 0. Three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output. The register is clocked by the low-to-high transition of the I/CLK. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

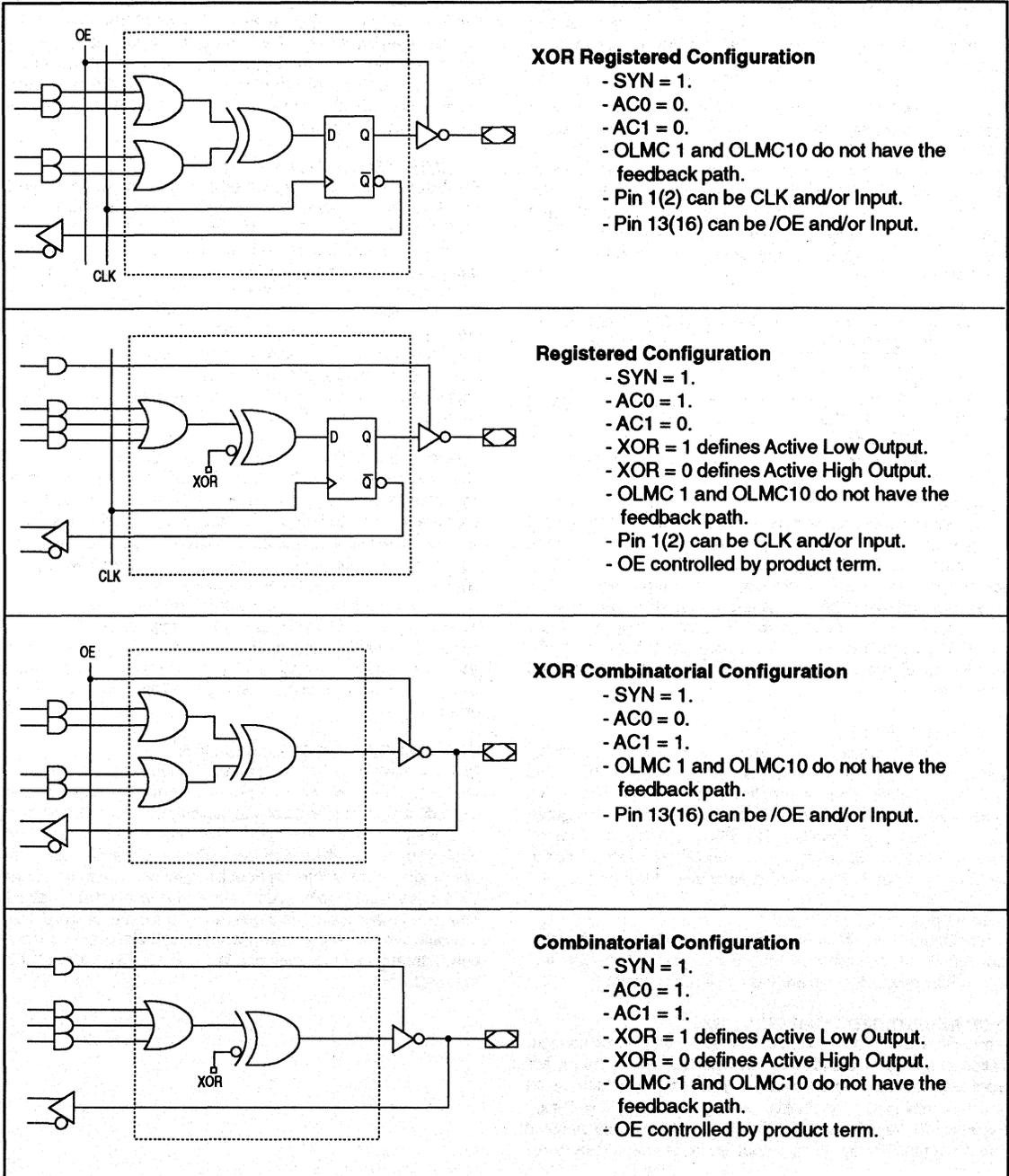
XOR COMBINATORIAL CONFIGURATION

The Macrocell is set to the Exclusive-OR Combinatorial configuration when AC0 = 0 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer. The inverting output buffer is enabled by the I/OE pin, which is an active low output enable that is common to all XOR macrocells. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

COMBINATORIAL CONFIGURATION

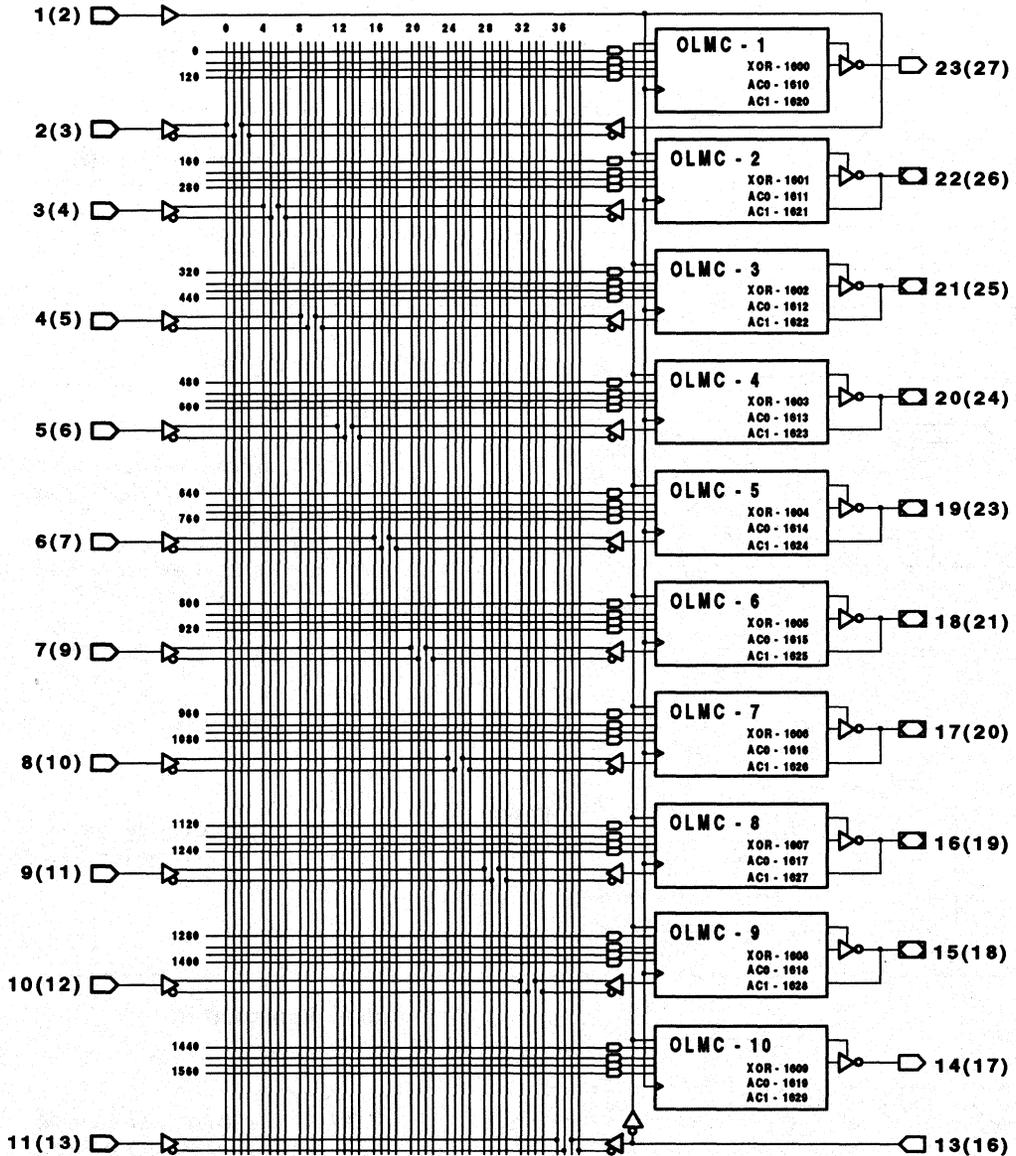
The Macrocell is set to Combinatorial mode when AC0 = 1 and AC1 = 1. Three of the four product terms are used as sum-of-product terms for the combinatorial output. The XOR bit controls the polarity of the output. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

INPUT MODE



INPUT MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinout

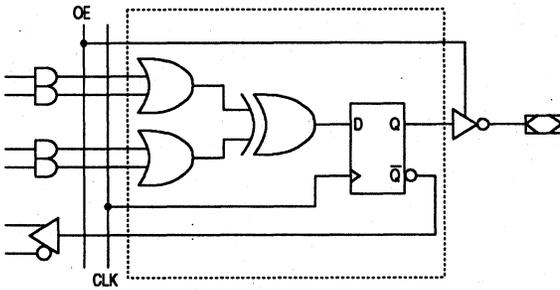


40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, 1669, 1670
Byte4 Byte3 Byte1 Byte0

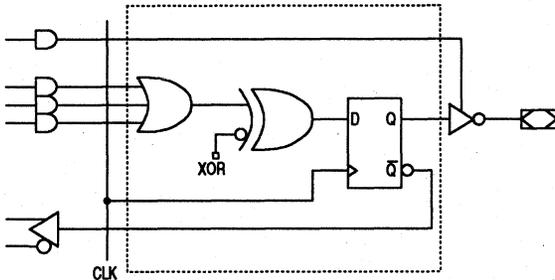
SYN - 1630

FEEDBACK MODE



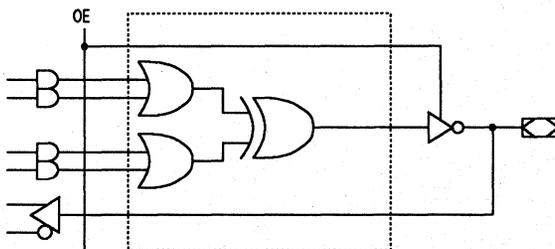
XOR Registered Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 0.
- Dedicated CLK input on Pin 1(2).
- Dedicated /OE input on Pin 13(16).



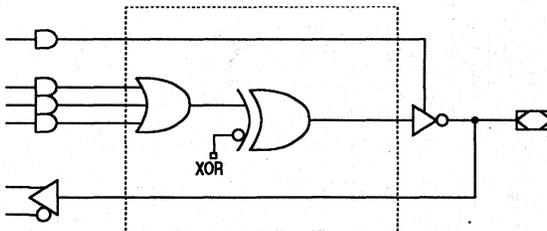
Registered Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- Dedicated CLK input on Pin 1(2).
- OE controlled by product term.
- Pin 13(16) is not connected to this configuration.



XOR Combinatorial Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 1.
- Dedicated /OE input on Pin 13(16).
- Pin 1(2) is not connected to this configuration.

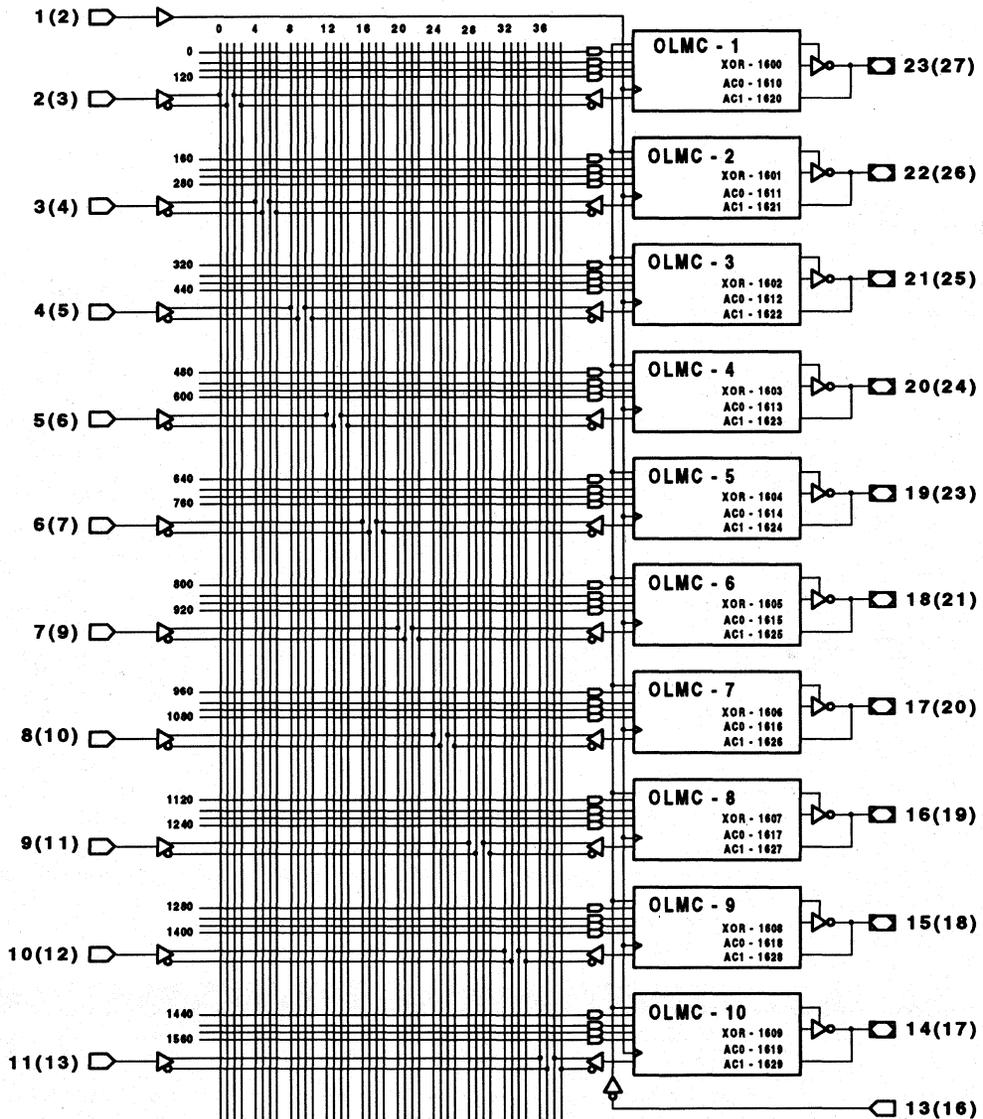


Combinatorial Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OE controlled by product term.
- Both pin1(2) and pin 13(16) are not connected to this configuration.

FEEDBACK MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinout



40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, 1669, 1670
Byte4 Byte3 Byte1 Byte0

SYN - 1630



Specifications **GAL20XV10B** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Ambient Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 25Mhz \quad \text{Outputs Open}$	—	75	90	mA

- 1) The leakage current is due to the internal pull-up on all input and I/O pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
$C_{i/o}$	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{i/o} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-10		-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
t_{co}	1	Clock to Output Delay	2	7	2	8	2	10	ns
t_{cf}^2	—	Clock to Feedback Delay	—	4	—	4	—	4	ns
t_{su}		Setup Time, Input or Feedback before Clock	6	—	8	—	10	—	ns
t_h		Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	76.9	—	62.5	—	50	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	100	—	83.3	—	71.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	100	—	83.3	—	71.4	—	MHz
t_{wh}		Clock Pulse Duration, High	4	—	6	—	7	—	ns
t_{wl}		Clock Pulse Duration, Low	4	—	6	—	7	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
	2	\overline{OE} to Output Enabled	2	9	2	10	2	15	ns
t_{dis}	3	Input or I/O to Output Disabled	3	9	3	15	3	20	ns
	3	\overline{OE} to Output Disabled	2	9	2	10	2	15	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to f_{max} Description section.

3) Refer to f_{max} Description section.

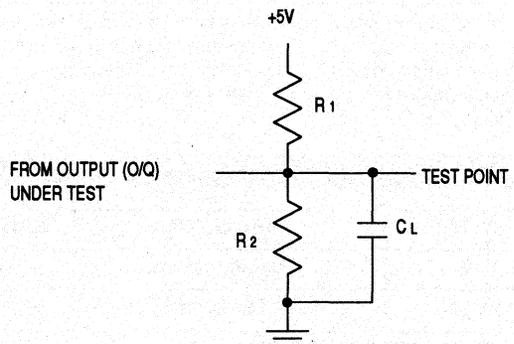
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	390Ω
	Active Low	300Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL20XV10B** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
 Ambient Temperature (T_A) -40 to +85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 25MHz \quad \text{Outputs Open}$	—	75	110	mA

- 1) The leakage current is due to the internal pull-up on all input and I/O pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
$C_{i/O}$	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	15	3	20	ns
t_{co}	1	Clock to Output Delay	2	8	2	10	ns
t_{cf}^2	—	Clock to Feedback Delay	—	4	—	4	ns
t_{su}		Setup Time, Input or Feedback before Clock	8	—	10	—	ns
t_h		Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	62.5	—	50	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	83.3	—	71.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	83.3	—	71.4	—	MHz
t_{wh}		Clock Pulse Duration, High	6	—	7	—	ns
t_{wl}		Clock Pulse Duration, Low	6	—	7	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	15	3	20	ns
	2	\overline{OE} to Output Enabled	2	10	2	15	ns
t_{dis}	3	Input or I/O to Output Disabled	3	15	3	20	ns
	3	\overline{OE} to Output Disabled	2	10	2	15	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to f_{max} **Description** section.

3) Refer to f_{max} **Description** section.

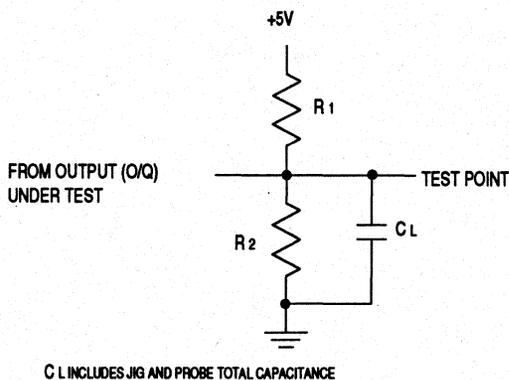
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

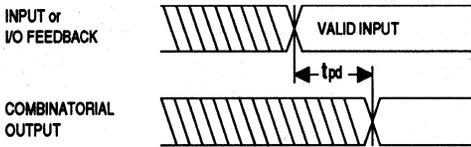
Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	5pF
	Active Low	300Ω	390Ω

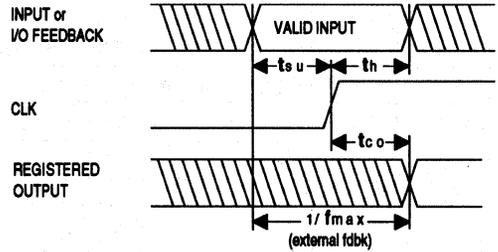


C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

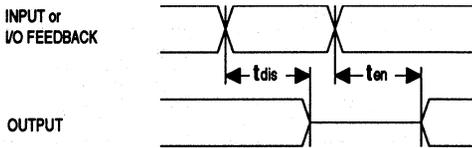
SWITCHING WAVEFORMS



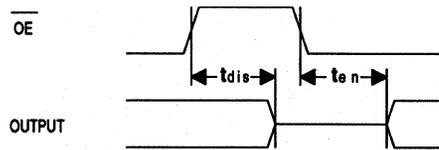
Combinatorial Output



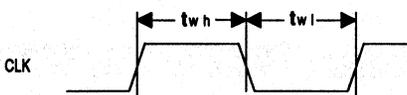
Registered Output



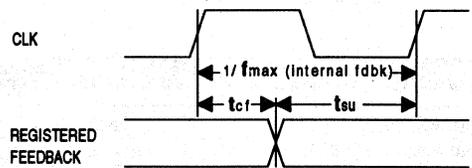
Input or I/O Feedback to Enable/Disable



OE to Output Enable/Disable

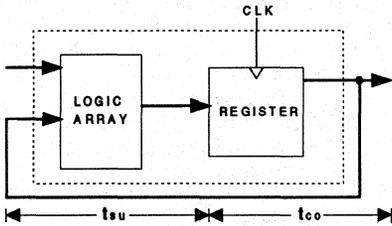


Clock Width



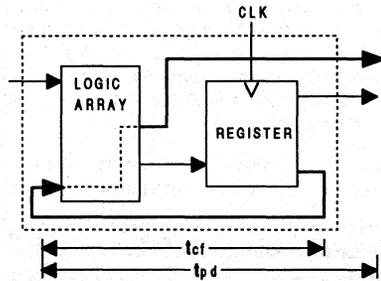
f_{max} with Feedback

fmax DESCRIPTIONS



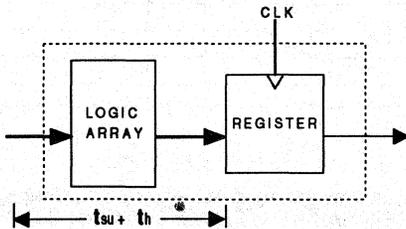
fmax with External Feedback $1/(t_{su} + t_{co})$

Note: fmax with external feedback is calculated from measured t_{su} and t_{co} .



fmax with Internal Feedback $1/(t_{su} + t_{cf})$

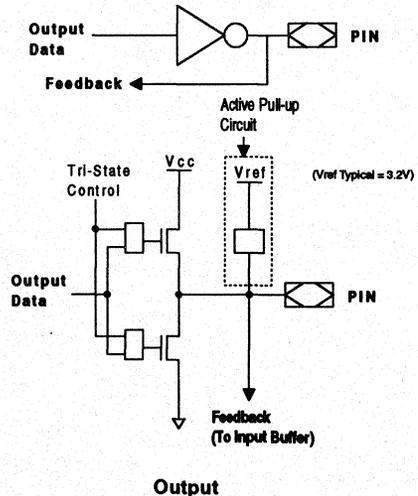
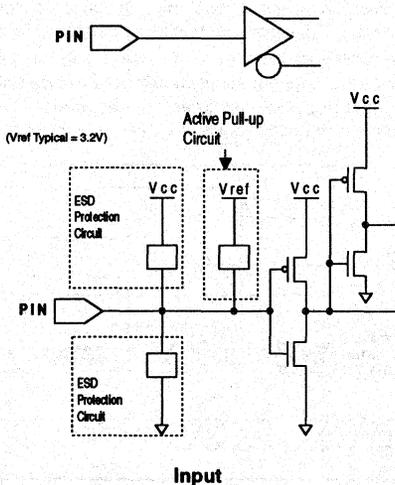
Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of fmax w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to $t_{cf} + t_{pd}$.



fmax Without Feedback

Note: fmax with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20XV10B device. It contains 40 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits, if programmed to any value other than zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20XV10B device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes less than a second. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

LATCH-UP PROTECTION

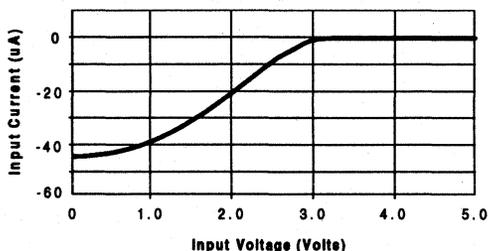
GAL20XV10B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL20XV10B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

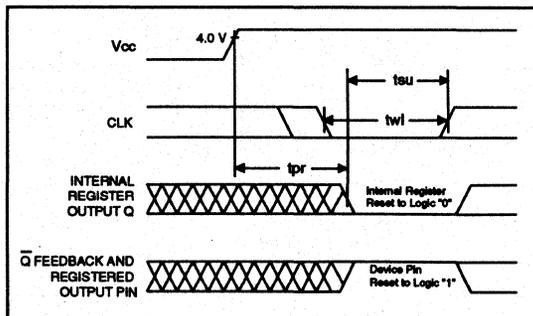
GAL20XV10B input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce lcc for the device.

Typical Input Pull-up Characteristic

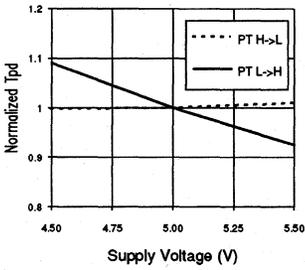


POWER-UP RESET

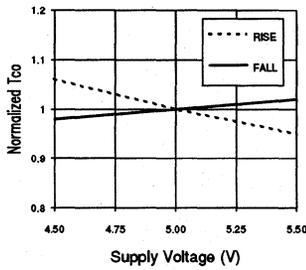
Circuitry within the GAL20XV10B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20XV10B. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.



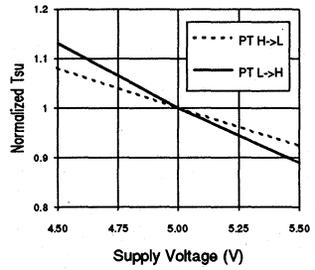
Normalized T_{pd} vs V_{cc}



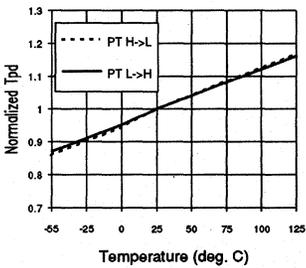
Normalized T_{co} vs V_{cc}



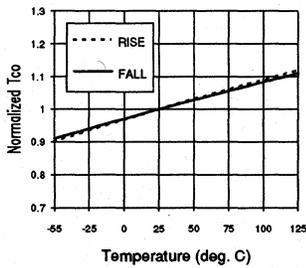
Normalized T_{su} vs V_{cc}



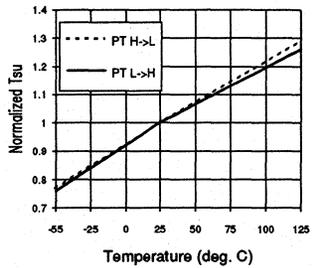
Normalized T_{pd} vs Temp



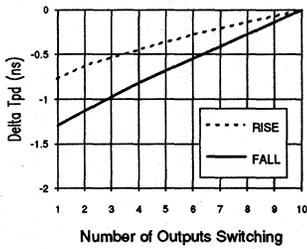
Normalized T_{co} vs Temp



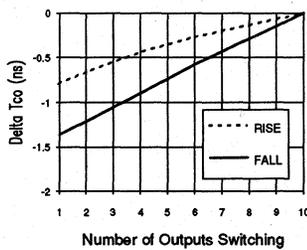
Normalized T_{su} vs Temp



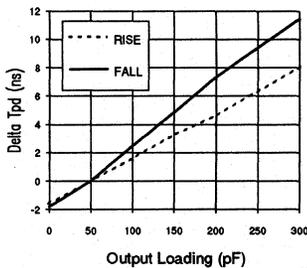
Delta T_{pd} vs # of Outputs Switching



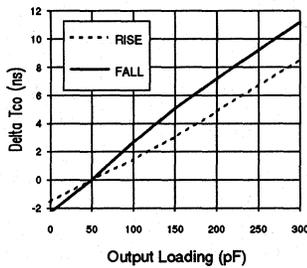
Delta T_{co} vs # of Outputs Switching



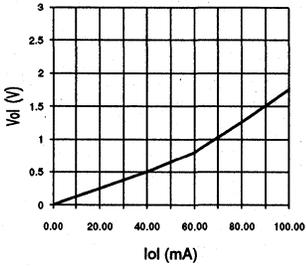
Delta T_{pd} vs Output Loading



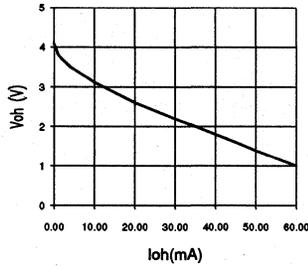
Delta T_{co} vs Output Loading



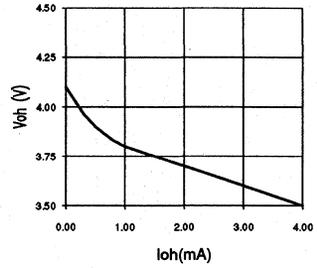
Vol vs Iol



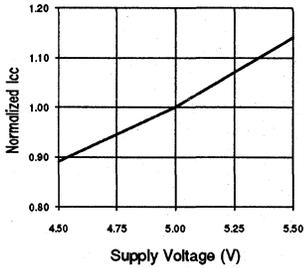
Voh vs Ioh



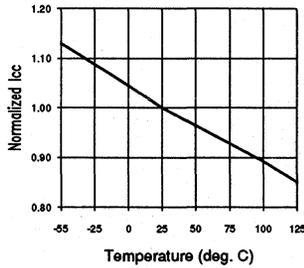
Voh vs Ioh



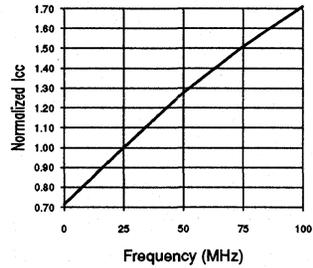
Normalized Icc vs Vcc



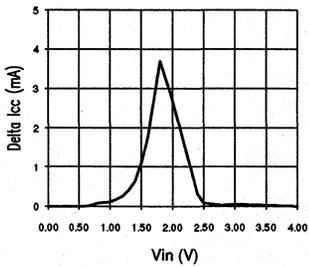
Normalized Icc vs Temp



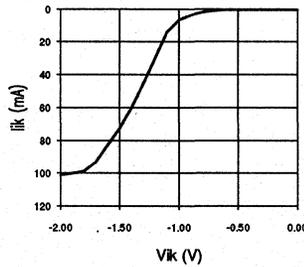
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)



Input Clamp (Vik)





GAL20RA10

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
 - 12 ns Maximum Propagation Delay
 - $f_{max} = 71.4$ MHz
 - 12 ns Maximum from Clock Input to Data Output
 - TTL Compatible 8 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc}
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100 ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Independent Programmable Clocks
 - Independent Asynchronous Reset and Preset
 - Registered or Combinatorial with Polarity
 - Full Function and Parametric Compatibility with PAL20RA10
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - State Machine Control
 - Standard Logic Consolidation
 - Multiple Clock Logic Designs
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

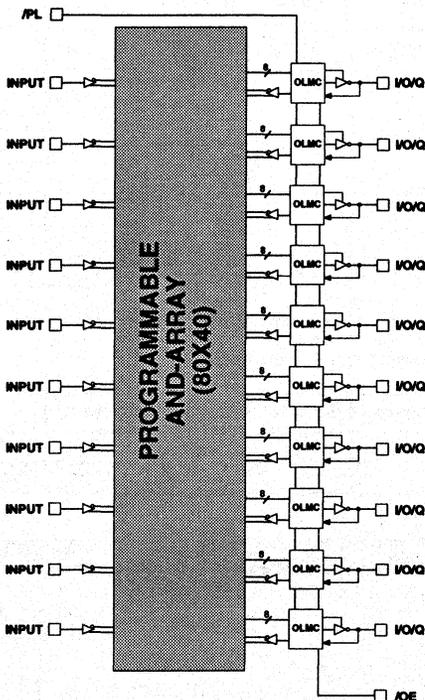
DESCRIPTION

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. Lattice's E²CMOS circuitry achieves power levels as low as 75mA typical I_{cc} , which represents a substantial savings in power when compared to bipolar counterparts. E² technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

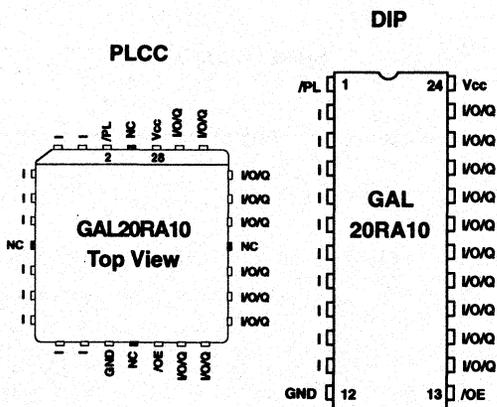
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC,DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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GAL20RA10 ORDERING INFORMATION

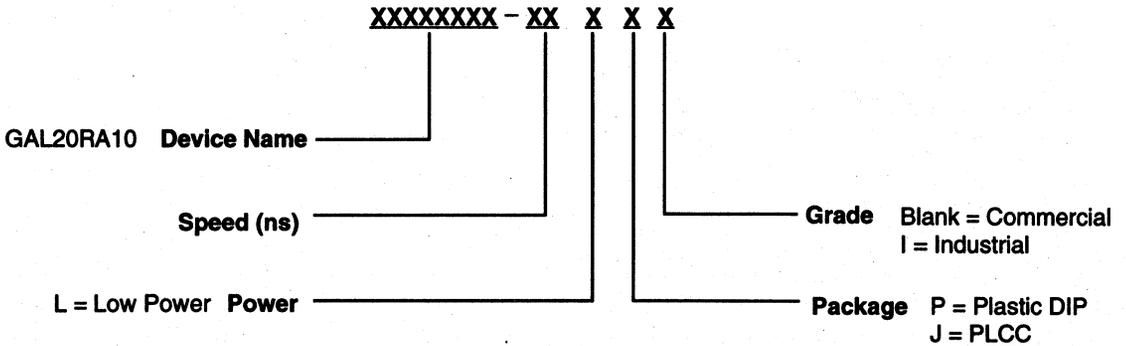
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
12	4	12	100	GAL20RA10-12LP	24-Pin Plastic DIP
			100	GAL20RA10-12LJ	28-Lead PLCC
15	7	15	100	GAL20RA10-15LP	24-Pin Plastic DIP
			100	GAL20RA10-15LJ	28-Lead PLCC
20	10	20	100	GAL20RA10-20LP	24-Pin Plastic DIP
			100	GAL20RA10-20LJ	28-Lead PLCC
30	20	30	100	GAL20RA10-30LP	24-Pin Plastic DIP
			100	GAL20RA10-30LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	10	20	120	GAL20RA10-20LPI	24-Pin Plastic DIP
			120	GAL20RA10-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The GAL20RA10 consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provide a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

INDEPENDENT PROGRAMMABLE CLOCKS

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allow up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

PROGRAMMABLE POLARITY

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. While any one of the four logic function product terms are active the D-input to the flip-flop will be low if the Exclusive-OR bit is set to zero(0) and high if the Exclusive-OR bit is set to one(1). It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independent of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

OUTPUT ENABLE

The output of each GAL20RA10 macrocell is controlled by the "AND'ing" of an independent output enable product term and a common active low output enable pin(13). The output is enabled while the output enable product term is active and the output enable pin(13) is low. This output control structure allows several output enable alternatives.

ASYNCHRONOUS RESET AND PRESET

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

RESET	PRESET	FUNCTION
0	0	Registered function of data product term
1	0	Reset register to "0" (device pin = "1")
0	1	Preset register to "1" (device pin = "0")
1	1	Register-bypass (combinatorial output)

COMBINATORIAL CONTROL

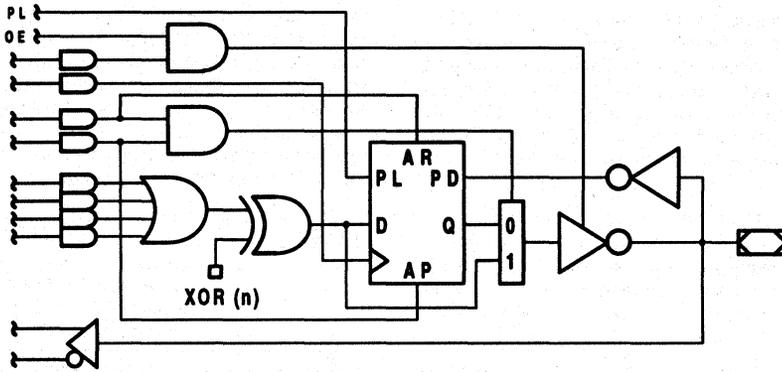
The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D- input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

PARALLEL FLIP-FLOP PRELOAD

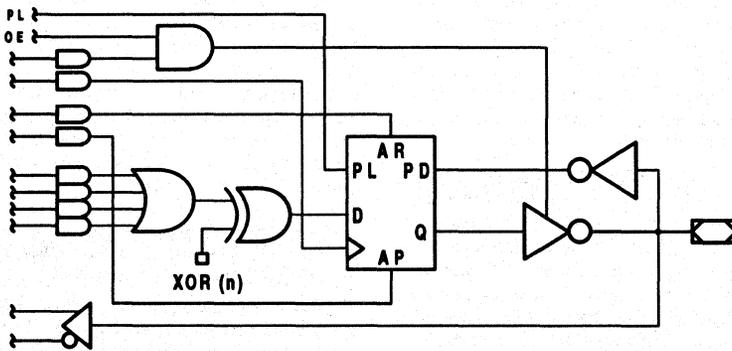
The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (1) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin (13) will disable all 10 outputs of the GAL20RA10 when held high.

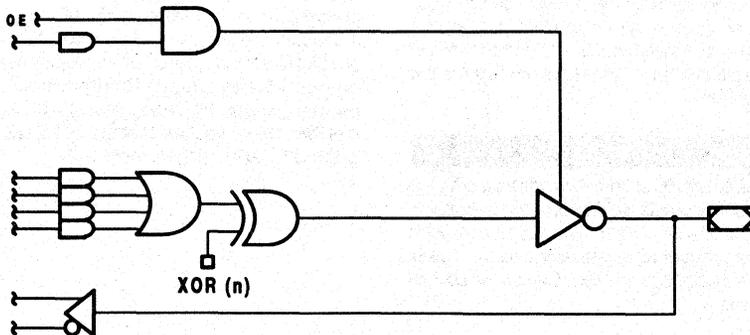
OUTPUT LOGIC MACROCELL DIAGRAM



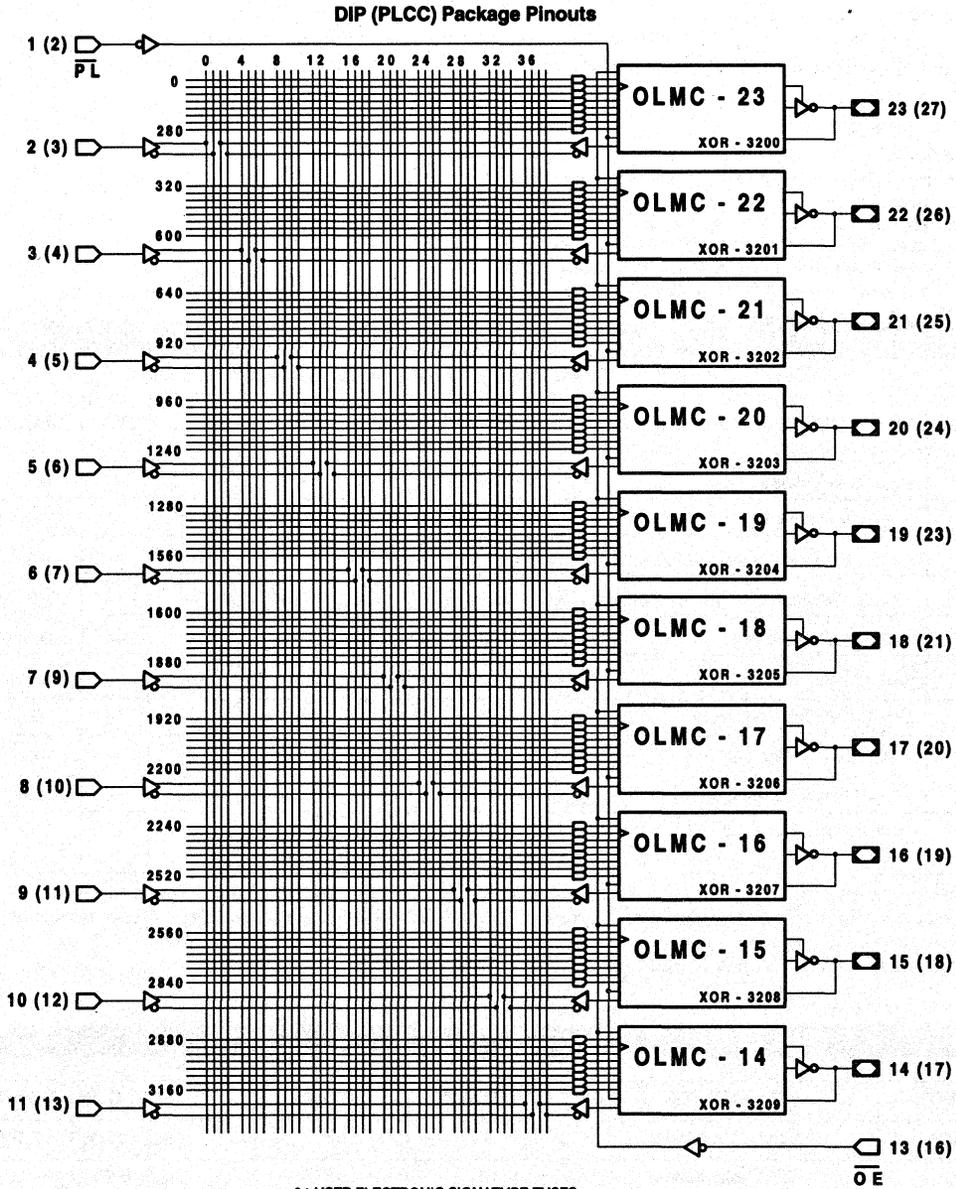
OUTPUT LOGIC MACROCELL CONFIGURATION (REGISTERED with POLARITY)



OUTPUT LOGIC MACROCELL CONFIGURATION (COMBINATORIAL with POLARITY)



GAL20RA10 LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

3210, 3211, 3272, 3273
Byte 7 Byte 6 Byte 1 Byte 0

M L
S S
B B



Specifications **GAL20RA10** Commercial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	75	100	mA

- 1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-12		-15		-20		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	12	—	15	—	20	—	30	ns
t_{co}	1	Clock to Output Delay	—	12	—	15	—	20	—	30	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	4	—	7	—	10	—	20	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	3	—	3	—	3	—	10	—	ns
f_{max}^2	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	62.5	—	45.0	—	33.3	—	20.0	—	MHz
	1	Maximum Clock Frequency without Feedback	71.4	—	50.0	—	41.7	—	25.0	—	MHz
t_{wh}	—	Clock Pulse Duration, High	7	—	10	—	12	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	7	—	10	—	12	—	20	—	ns
t_{en} / t_{dis}	2,3	Input or I/O to Output Enabled / Disabled	—	12	—	15	—	20	—	30	ns
t_{en} / t_{dis}	2,3	\overline{OE} to Output Enabled / Disabled	—	9	—	12	—	15	—	20	ns
t_{ar} / t_{ap}	1	Input or I/O to Asynchronous Reset / Preset	—	12	—	15	—	20	—	30	ns
t_{arw} / t_{apw}	—	Asynchronous Reset / Preset Pulse Duration	12	—	15	—	20	—	20	—	ns
t_{arr} / t_{apr}	—	Asynchronous Reset / Preset Recovery Time	7	—	10	—	12	—	20	—	ns
t_{wp}	—	Preload Pulse Duration	12	—	15	—	20	—	30	—	ns
t_{sp}	—	Preload Setup Time	7	—	10	—	15	—	25	—	ns
t_{hp}	—	Preload Hold Time	7	—	10	—	15	—	25	—	ns

1) Refer to **Switching Test Conditions** section.

2) Refer to **fmax Descriptions** section.

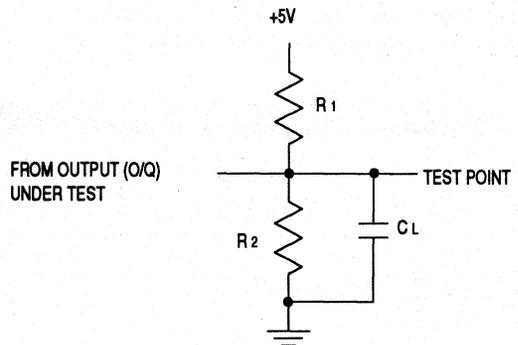
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	470Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	470Ω	390Ω
3	Active High	∞	5pF
	Active Low	470Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



Specifications **GAL20RA10** Industrial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Ambient Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:

Ambient Temperature (T_A)-40 to +85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	ns
t_{co}	1	Clock to Output Delay	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	3	—	ns
f_{max}^2	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	33.3	—	MHz
	1	Maximum Clock Frequency without Feedback	41.7	—	MHz
t_{wh}	—	Clock Pulse Duration, High	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	12	—	ns
t_{en} / t_{dis}	2,3	Input or I/O to Output Enabled / Disabled	—	20	ns
t_{en} / t_{dis}	2,3	\overline{OE} to Output Enabled / Disabled	—	15	ns
t_{ar} / t_{ap}	1	Input or I/O to Asynchronous Reset / Preset	—	20	ns
t_{arw} / t_{apw}	—	Asynchronous Reset / Preset Pulse Duration	20	—	ns
t_{arr} / t_{apr}	—	Asynchronous Reset / Preset Recovery Time	12	—	ns
t_{wp}	—	Preload Pulse Duration	20	—	ns
t_{sp}	—	Preload Setup Time	15	—	ns
t_{hp}	—	Preload Hold Time	15	—	ns

- 1) Refer to Switching Test Conditions section.
2) Refer to f_{max} Descriptions section.

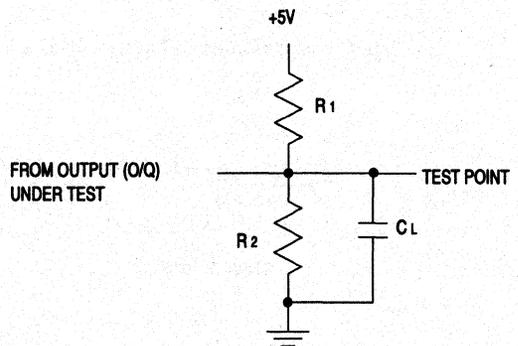
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

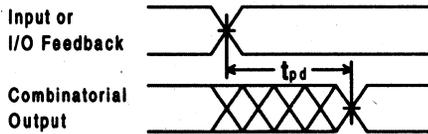
Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	470Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	470Ω	390Ω
3	Active High	∞	5pF
	Active Low	470Ω	390Ω

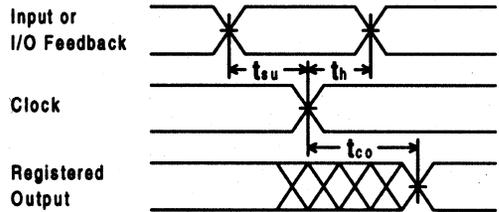


C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

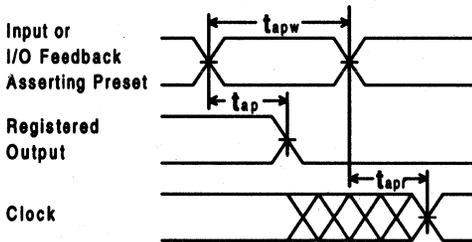
SWITCHING WAVEFORMS



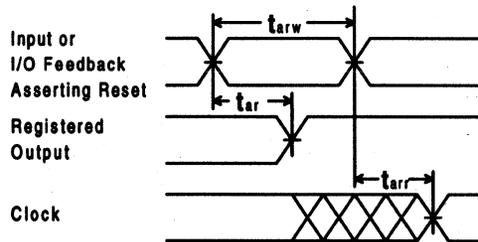
Combinatorial Output



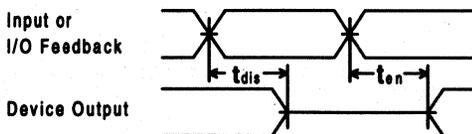
Registered Output



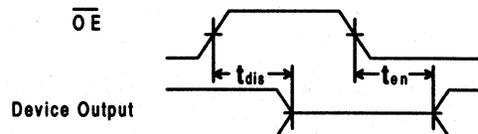
Asynchronous Preset



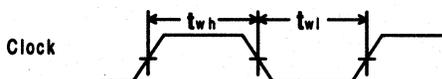
Asynchronous Reset



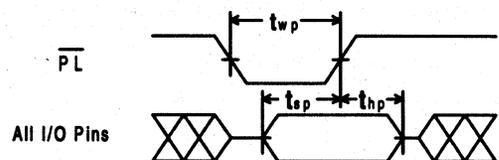
Input or I/O Feedback to Enable / Disable



OE to Enable / Disable

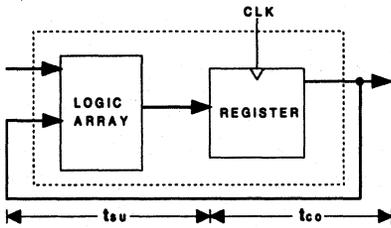


Clock Width



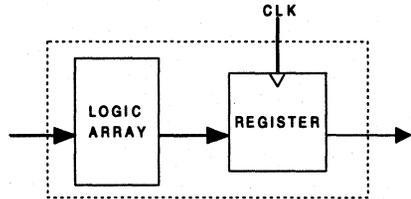
Parallel Preload

fmax DESCRIPTIONS



fmax with External Feedback $1/(t_{su}+t_{co})$

Note: fmax with external feedback is calculated from measured tsu and tco.

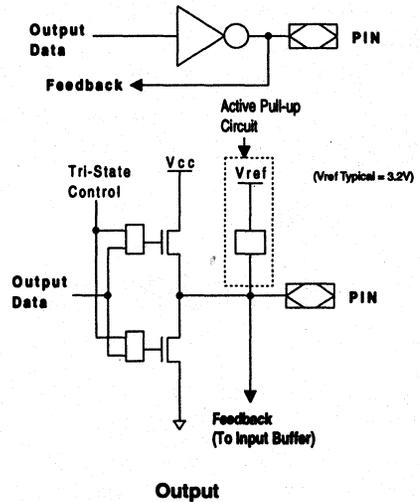
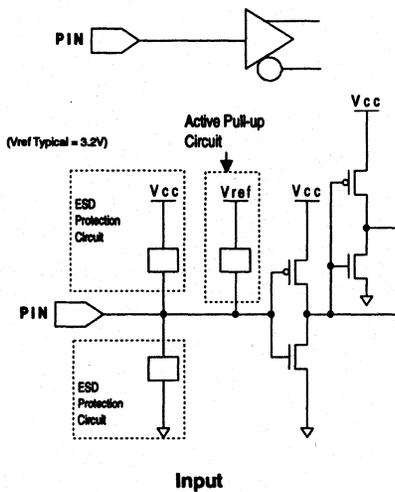


fmax With No Feedback

Note: fmax with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

2

INPUT/OUTPUT EQUIVALENT SCHEMATICS



ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits if programmed to any value other than zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20RA10 devices as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

LATCH-UP PROTECTION

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

POWER-UP RESET

Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be high on power-up, because of the inverting buffer on the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown to the right. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the V_{cc} rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of 1 μ s. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

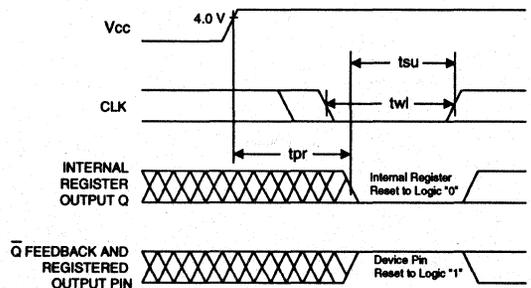
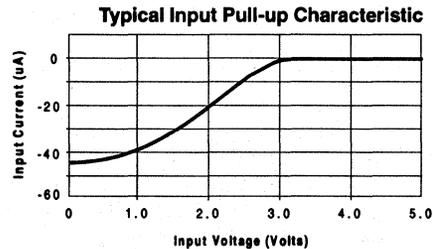
DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

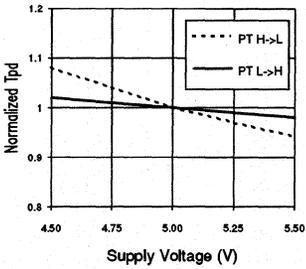
INPUT BUFFERS

GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

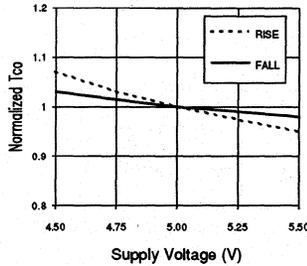
GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{cc} , or GND. Doing this will tend to improve noise immunity and reduce I_{cc} for the device.



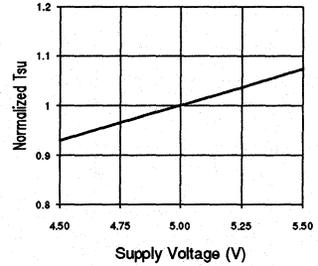
Normalized Tpd vs Vcc



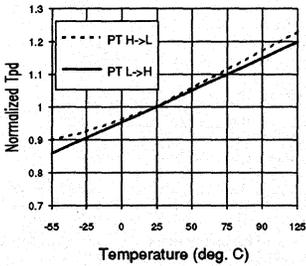
Normalized Tco vs Vcc



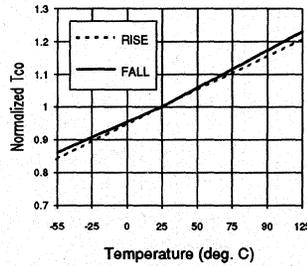
Normalized Tsu vs Vcc



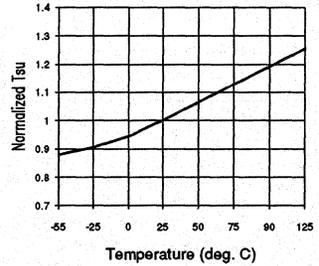
Normalized Tpd vs Temp



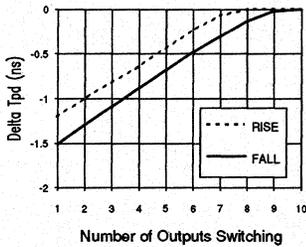
Normalized Tco vs Temp



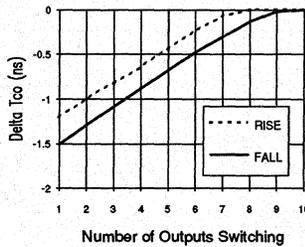
Normalized Tsu vs Temp



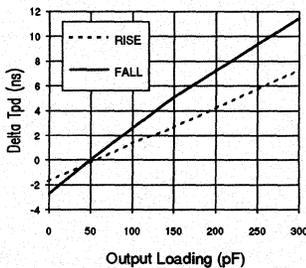
Delta Tpd vs # of Outputs Switching



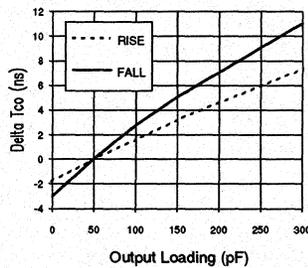
Delta Tco vs # of Outputs Switching



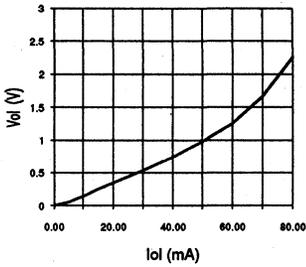
Delta Tpd vs Output Loading



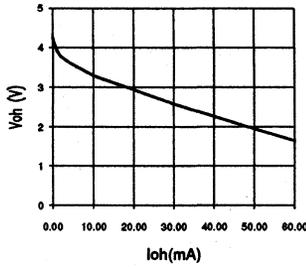
Delta Tco vs Output Loading



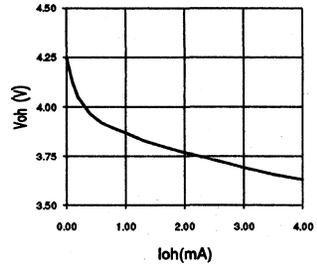
Vol vs Iol



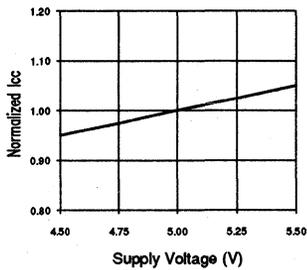
Voh vs Ioh



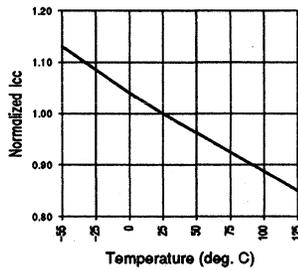
Voh vs Ioh



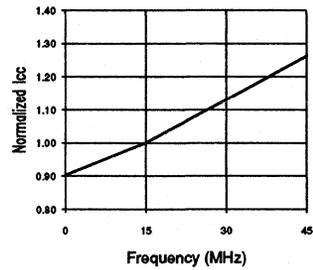
Normalized Icc vs Vcc



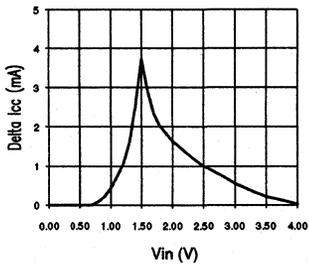
Normalized Icc vs Temp



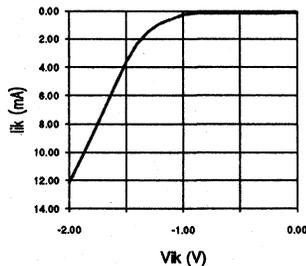
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 15ns Maximum Propagation Delay
 - 75MHz Maximum Frequency
 - 6.5ns Max. Clock to Output Delay
 - TTL Compatible 16mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
 - 90mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **UNPRECEDENTED FUNCTIONAL DENSITY**
 - 78 x 64 x 36 FPLA Architecture
 - 10 Output Logic Macrocells
 - 8 Buried Logic Macrocells
 - 20 Input and I/O Logic Macrocells
- **HIGH-LEVEL DESIGN FLEXIBILITY**
 - Asynchronous or Synchronous Clocking
 - Separate State Register and Input Clock Pins
 - Functional Superset of Existing 24-pin PAL[®] and FPLA Devices
- **APPLICATIONS INCLUDE:**
 - Sequencers
 - State Machine Control
 - Multiple PLD Device Integration

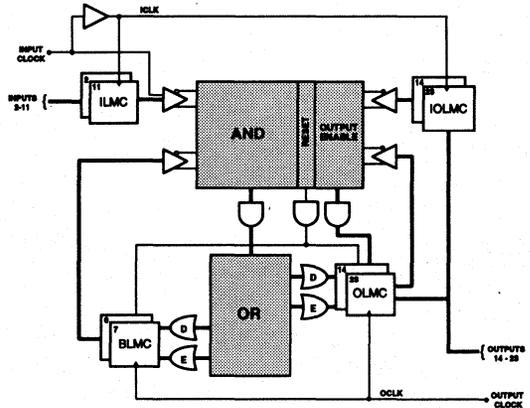
DESCRIPTION

Having an FPLA architecture, the GAL6002B provides superior flexibility in state-machine design. The GAL6002B offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package. E²CMOS technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The GAL6002B has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice is able to guarantee 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



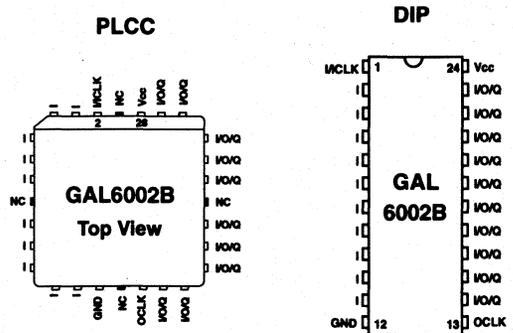
MACROCELL NAMES

ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

I ₀ - I ₁₀	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V _{CC}	POWER (+5V)
OCLK	OUTPUT CLOCK	GND	GROUND

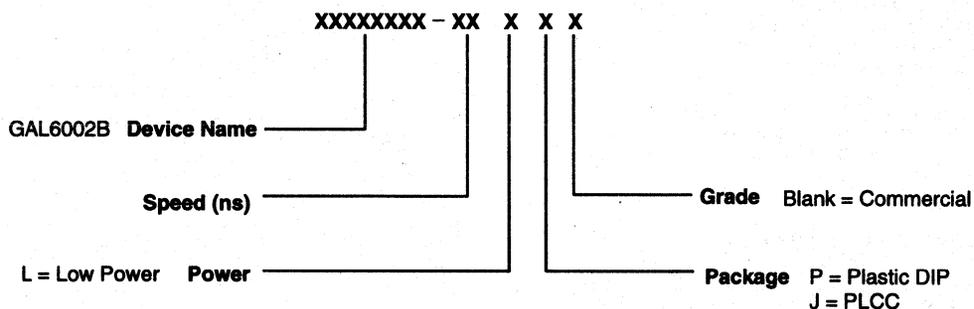
PIN CONFIGURATION



GAL6002B COMMERCIAL DEVICE ORDERING INFORMATION

Tpd (ns)	Fclk (MHz)	Icc (mA)	Ordering #	Package
15	75	135	GAL6002B-15LP	24-Pin Plastic DIP
		135	GAL6002B-15LJ	28-Lead PLCC
20	60	135	GAL6002B-20LP	24-Pin Plastic DIP
		135	GAL6002B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6002B features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is individually configurable as asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Individually configurable inputs provide system designers with unparalleled design flexibility. With the GAL6002B, external input registers and latches are not necessary.

Both the ILMC and the IOLMC are individually configurable and the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations and its associated fuse numbers are shown in the diagrams on the following pages. Note that these programmable cells are configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the programmable polarity control cell called XOR_D. Polarity selection for BLMCs is selected through the true and complement forms of their feedbacks to the AND array. Polarity of all E (Enable) sum terms is selected through the XORE programmable cells.

When the output or buried logic macrocell is configured as a D/E type register, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with count hold and state hold functions.

When the macrocell is configured as a D type register with a sum term clock, the register is always enabled and the associated "E"

sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

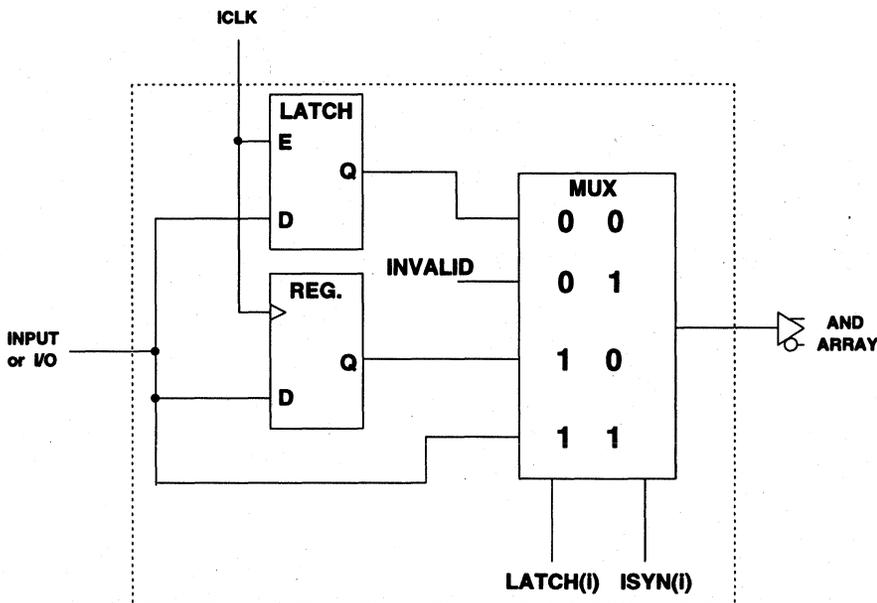
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. All registers reset to logic zero. With the inverting output buffers, the output pins will reset to logic one.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried without losing the use of the associated OLMC pin as an input, or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS, JK, and T registers with the same efficiency as a dedicated RS, JK, or T registers.

The three macrocell configurations are shown in the diagrams on the following pages. These programmable cells are also configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

ILMC AND IOLMC CONFIGURATIONS



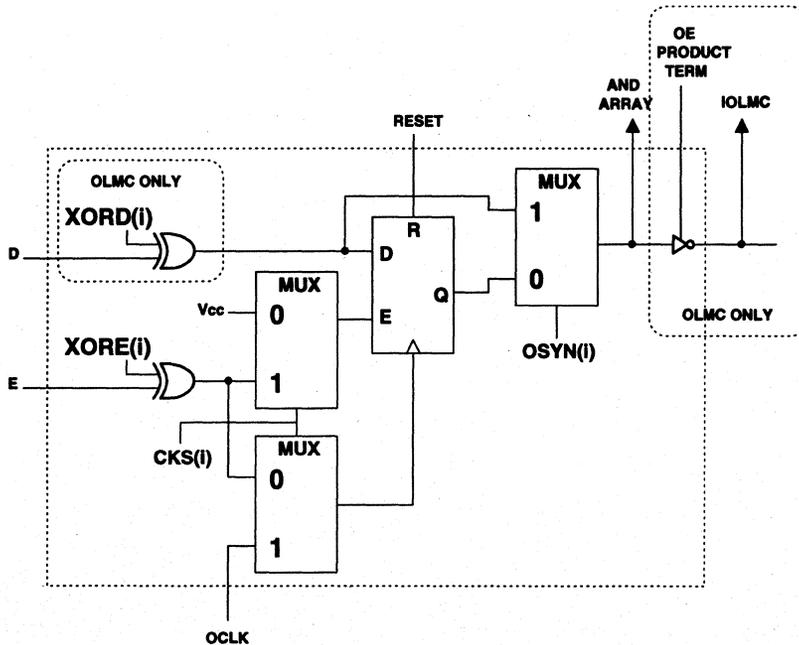
ILMC/IOLMC
Generic Logic Block Diagram

Input Macrocell JEDEC Fuse Numbers

INSYNC	INLATCH	ILMC
8218	8219	0
8220	8221	1
8222	8223	2
8224	8225	3
8226	8227	4
8228	8229	5
8230	8231	6
8232	8233	7
8234	8235	8
8236	8237	9

I/O Macrocell JEDEC Fuse Numbers

IOSYNC	IOLATCH	IOLMC
8238	8239	9
8240	8241	8
8242	8243	7
8244	8245	6
8246	8247	5
8248	8249	4
8250	8251	3
8252	8253	2
8254	8255	1
8256	8257	0

OLMC AND BLMC CONFIGURATIONS


OLMC/BLMC
Generic Logic Block Diagram

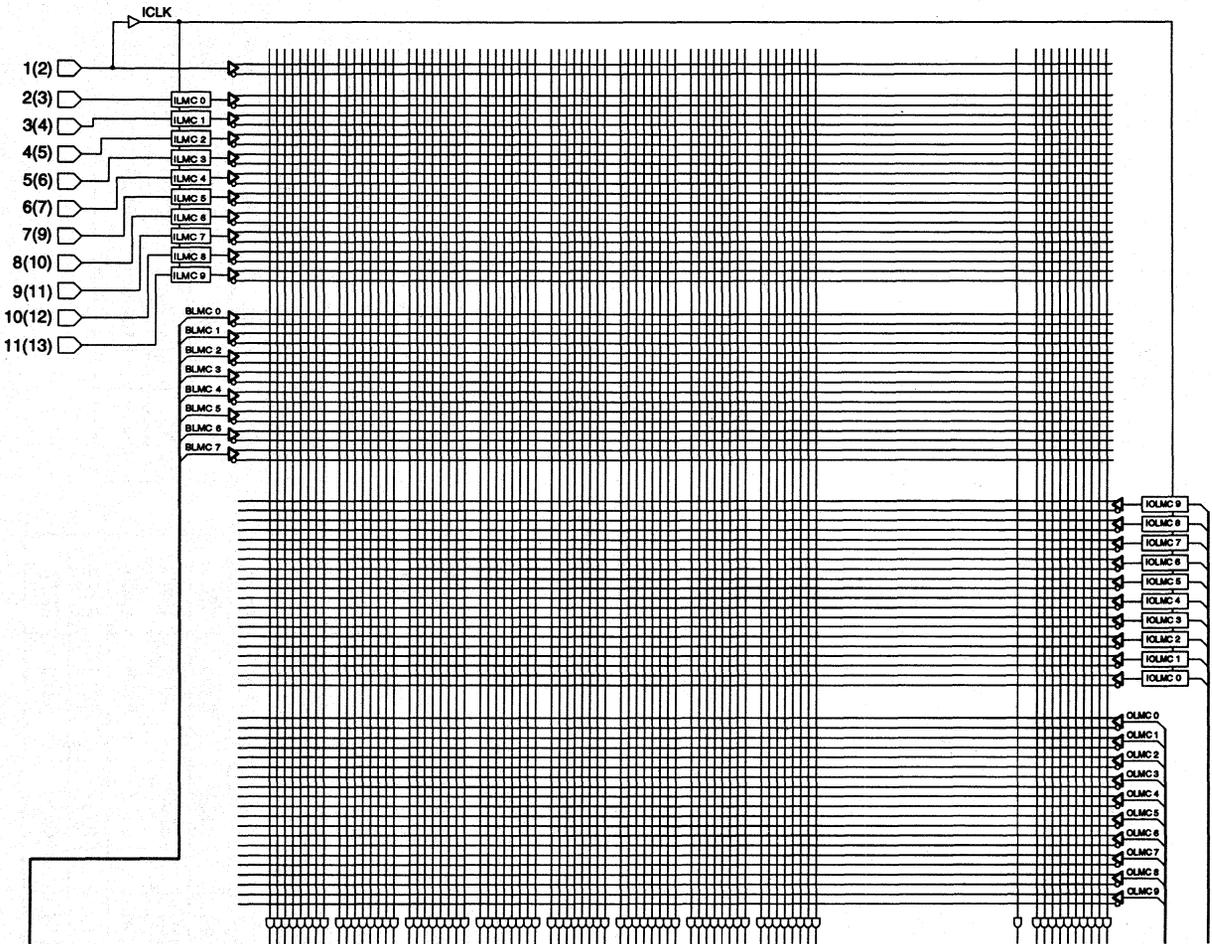
OLMC JEDEC Fuse Numbers

OLMC	CKS	OUTSYNC	XORD	XORE
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC JEDEC Fuse Numbers

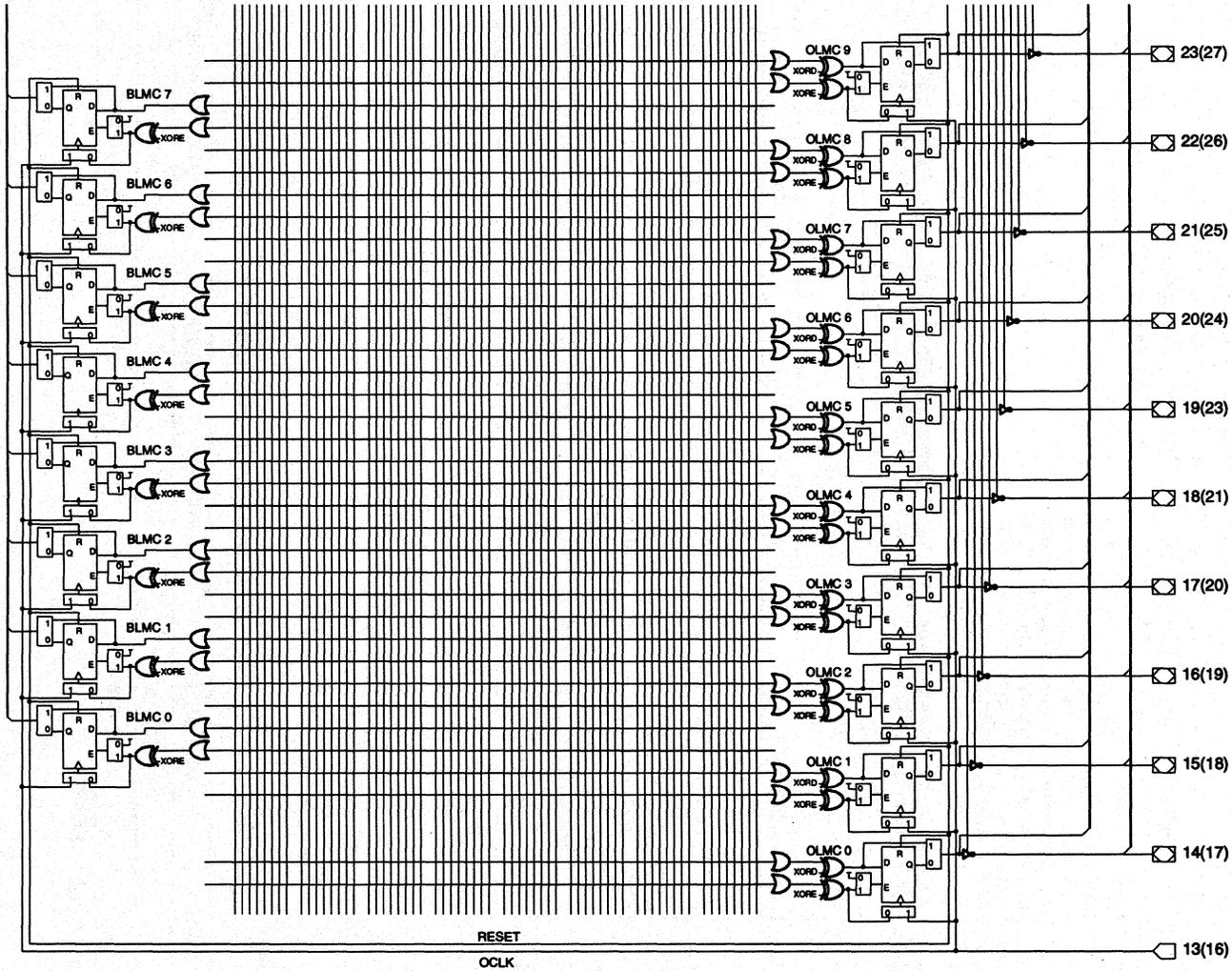
BLMC	CKS	OUTSYNC	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

LOGIC DIAGRAM





LOGIC DIAGRAM (CONT.)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$ Outputs Open (no load)	—	90	135	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t _{pd1}	1	Combinatorial Input to Combinatorial Output	—	15	—	20	ns
t _{pd2}	1	Feedback or I/O to Combinational Output	—	15	—	20	ns
t _{pd3}	1	Transparent Latch Input to Combinatorial Output	—	18	—	23	ns
t _{co1}	1	Input Latch ICLK to Combinatorial Output Delay	—	20	—	25	ns
t _{co2}	1	Input Reg. ICLK to Combinatorial Output Delay	—	20	—	25	ns
t _{co3}	1	Output D/E Reg. OCLK to Output Delay	—	6.5	—	8	ns
t _{co4}	1	Output D Reg. Sum Term CLK to Output Delay	—	18	—	20	ns
t _{cf1} ²	—	Output D/E Reg. OCLK to Buried Feedback Delay	—	3.6	—	7	ns
t _{cf2} ²	—	Output D Reg. STCLK to Buried Feedback Delay	—	10.1	—	13	ns
t _{su1}	—	Setup Time, Input before Input Latch ICLK	1.5	—	2	—	ns
t _{su2}	—	Setup Time, Input before Input Reg. ICLK	1.5	—	2	—	ns
t _{su3}	—	Setup Time, Input or Feedback before D/E Reg. OCLK	11.5	—	13	—	ns
t _{su4}	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK	5	—	7	—	ns
t _{su5}	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	15	—	20	—	ns
t _{su6}	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	7	—	9	—	ns
t _{h1}	—	Hold Time, Input after Input Latch ICLK	3	—	4	—	ns
t _{h2}	—	Hold Time, Input after Input Reg. ICLK	3	—	4	—	ns
t _{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	0	—	ns
t _{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	4	—	6	—	ns
f _{max1} ³	—	Max. Clock Frequency w/External Feedback, 1/(t _{su3} +t _{co3})	55.5	—	47.6	—	MHz
f _{max2} ³	—	Max. Clock Frequency w/External Feedback, 1/(t _{su4} +t _{co4})	43.4	—	37	—	MHz
f _{max3} ³	—	Max. Clock Frequency w/Internal Feedback, 1/(t _{su3} +t _{cf1})	66	—	50	—	MHz
f _{max4} ³	—	Max. Clock Frequency w/Internal Feedback, 1/(t _{su4} +t _{cf2})	66	—	50	—	MHz
f _{max5} ³	—	Max. Clock Frequency w/No Feedback, OCLK	75	—	60	—	MHz
f _{max6} ³	—	Max. Clock Frequency w/No Feedback, STCLK	70	—	60	—	MHz
t _{wh1}	—	ICLK Pulse Duration, High	6	—	7	—	ns
t _{wh2}	—	OCLK Pulse Duration, High	6	—	7	—	ns
t _{wh3}	—	STCLK Pulse Duration, High	7	—	8	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

3) Refer to **f_{max} Description** section.

AC SWITCHING CHARACTERISTICS (CONT.)

Over Recommended Operating Conditions

PARAMETER	TEST COND'.	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{w1}	—	ICLK Pulse Duration, Low	6	—	7	—	ns
t_{w2}	—	OCLK Pulse Duration, Low	6	—	7	—	ns
t_{w3}	—	STCLK Pulse Duration, Low	7	—	8	—	ns
t_{arw}	—	Reset Pulse Duration	12	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reg. Reset	—	16	—	20	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	11	—	14	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	4	—	6	—	ns

1) Refer to Switching Test Conditions section.

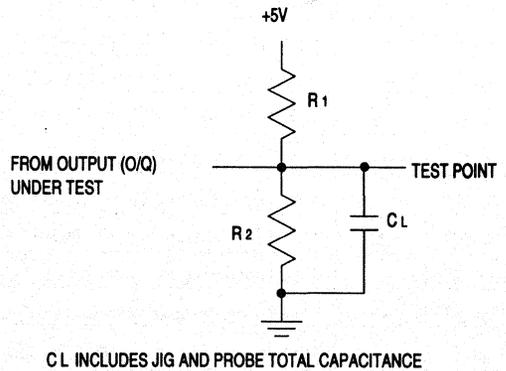
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

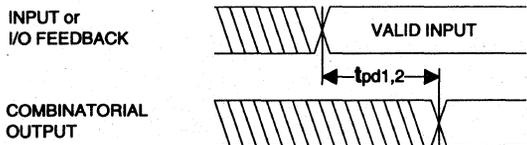
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

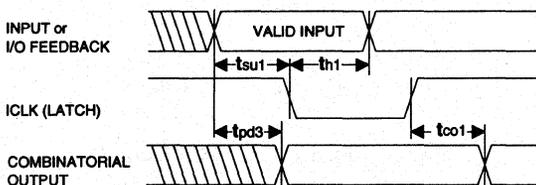
Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	5pF
	Active Low	300Ω	390Ω



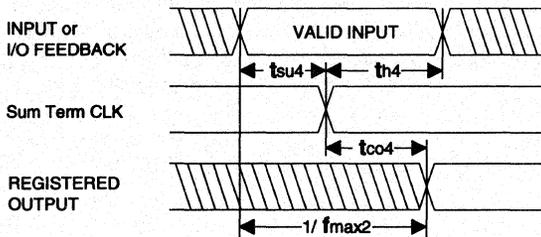
SWITCHING WAVEFORMS



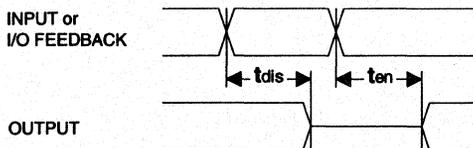
Combinatorial Output



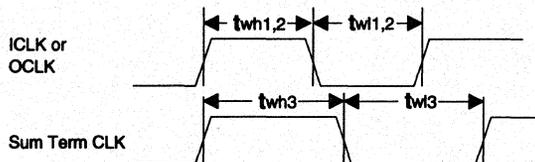
Latched Input



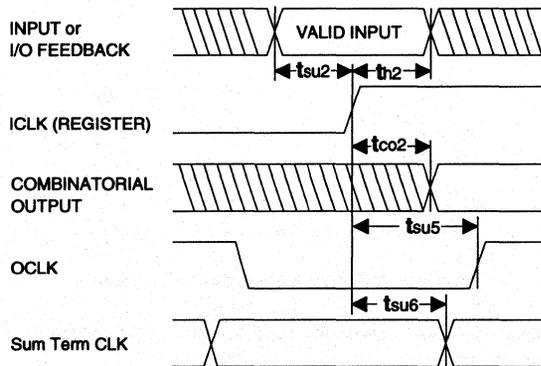
Registered Output (Sum Term CLK)



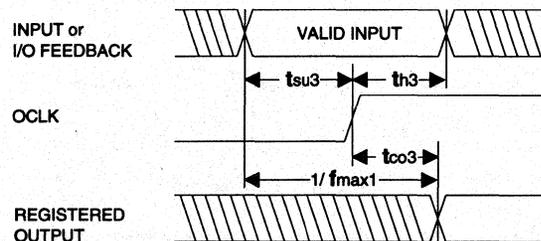
Input or I/O to Output Enable/Disable



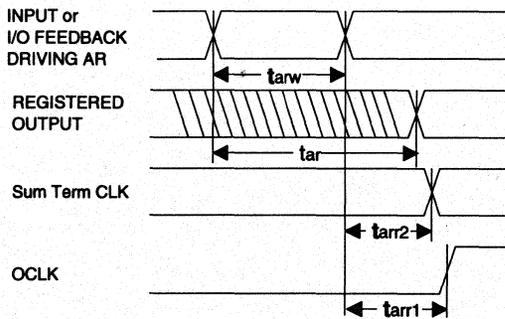
Clock Width



Registered Input



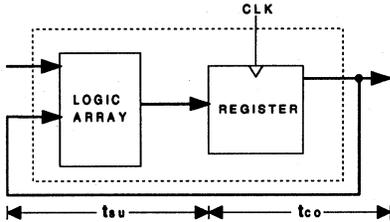
Registered Output (OCLK)



Asynchronous Reset

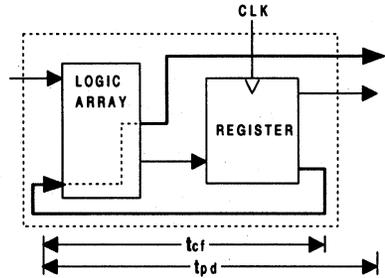
2

fmax DESCRIPTIONS



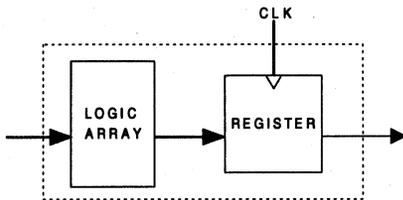
fmax with External Feedback $1/(t_{su}+t_{co})$

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback $1/(t_{su}+t_{cf})$

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to $t_{cf} + t_{pd}$.



fmax With No Feedback

Note: fmax with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

ARRAY DESCRIPTION

The GAL6002B contains two E² reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device I/O pins to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature is provided with every GAL6002B device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6002B device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because certain events may occur during system operation that cause the logic to be in an illegal state (power-up, line voltage glitches, brown-out, etc.). To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6002B can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

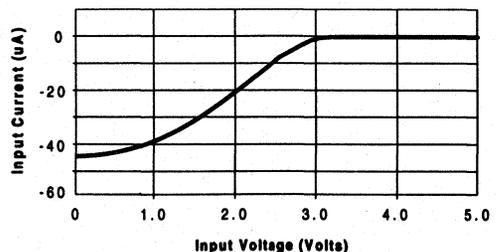
GAL6002B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

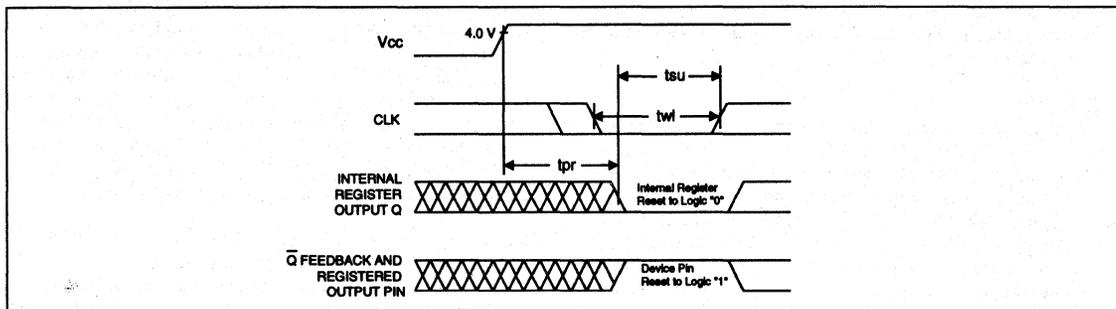
GAL6002B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL6002B input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET



Circuitry within the GAL6002B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6002B. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

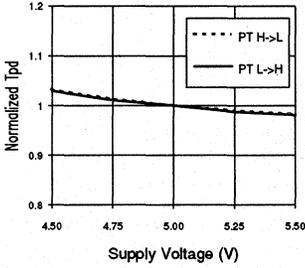
$$DPTS = \left| (P\text{-Terms})_{LH} - (P\text{-Terms})_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

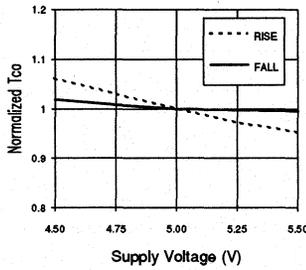
The majority of designs fall below 15 DPTS, with the upper limit being approximately 25 DPTS. Lattice guarantees and tests the GAL6002B for functionality at DPTS \leq 30.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6002B JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering Dept. (Tel: 503-681-0118 or 1-800-FASTGAL; FAX: 681-3037).

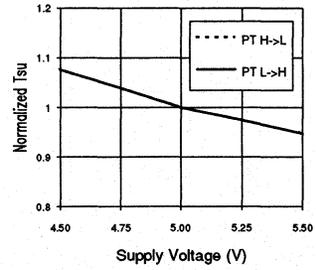
Normalized Tpd vs Vcc



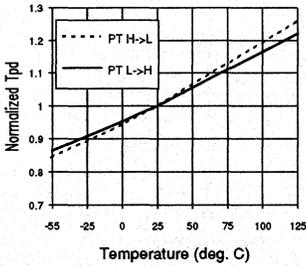
Normalized Tco vs Vcc



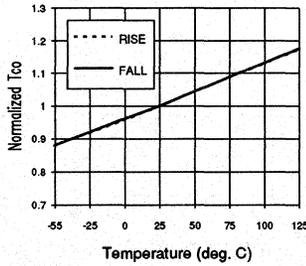
Normalized Tsu vs Vcc



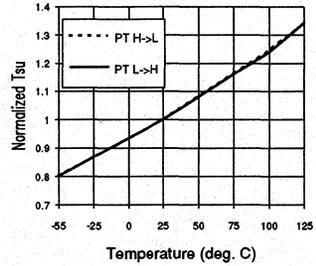
Normalized Tpd vs Temp



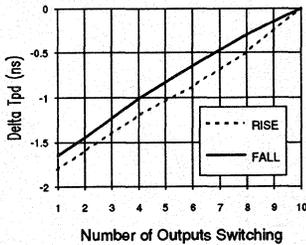
Normalized Tco vs Temp



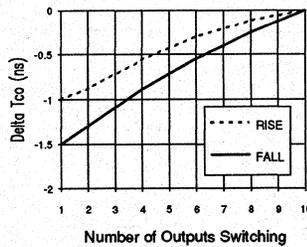
Normalized Tsu vs Temp



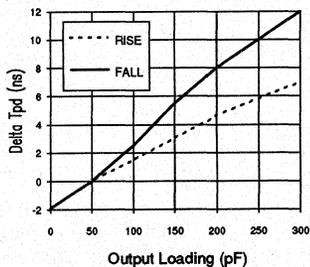
Delta Tpd vs # of Outputs Switching



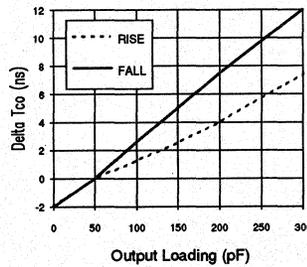
Delta Tco vs # of Outputs Switching



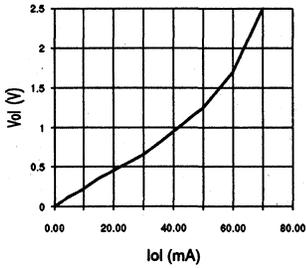
Delta Tpd vs Output Loading



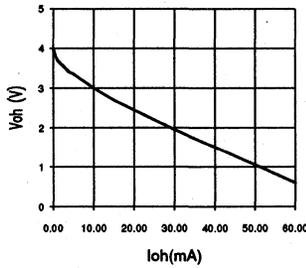
Delta Tco vs Output Loading



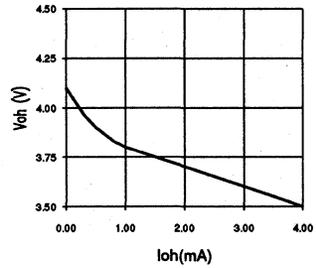
Vol vs Iol



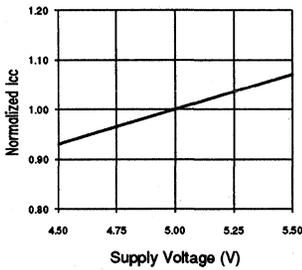
Voh vs Ioh



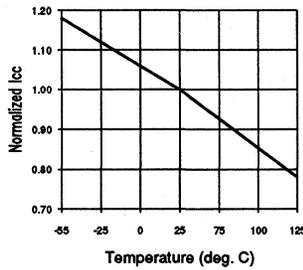
Voh vs Ioh



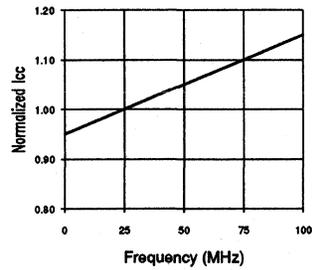
Normalized Icc vs Vcc



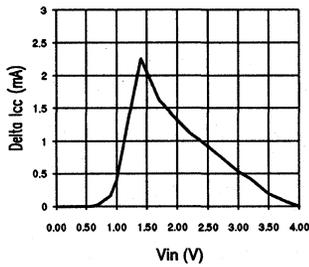
Normalized Icc vs Temp



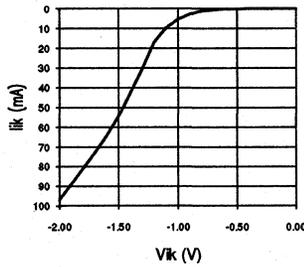
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 30ns Maximum Propagation Delay
 - 27MHz Maximum Frequency
 - 12ns Max. Clock to Output Delay
 - TTL Compatible 16mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **LOW POWER CMOS**
 - 90mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **UNPRECEDENTED FUNCTIONAL DENSITY**
 - 78 x 64 x 36 FPLA Architecture
 - 10 Output Logic Macrocells
 - 8 Buried Logic Macrocells
 - 20 Input and I/O Logic Macrocells
- **HIGH-LEVEL DESIGN FLEXIBILITY**
 - Asynchronous or Synchronous Clocking
 - Separate State Register and Input Clock Pins
 - Functional Superset of Existing 24-pin PAL® and FPLA Devices
- **APPLICATIONS INCLUDE:**
 - Sequencers
 - State Machine Control
 - Multiple PLD Device Integration

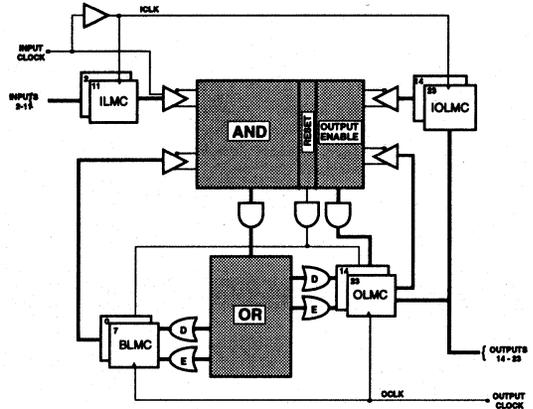
DESCRIPTION

Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers a high degree of functional integration and flexibility in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



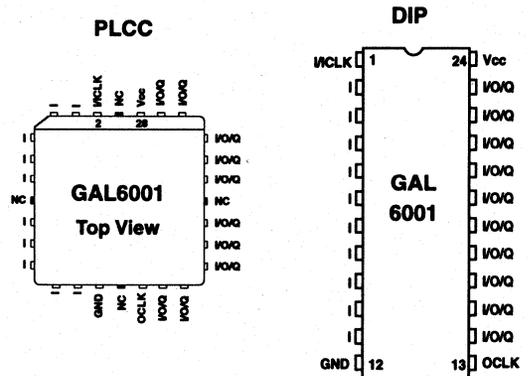
MACROCELL NAMES

ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

I ₀ - I ₁₀	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V _{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION



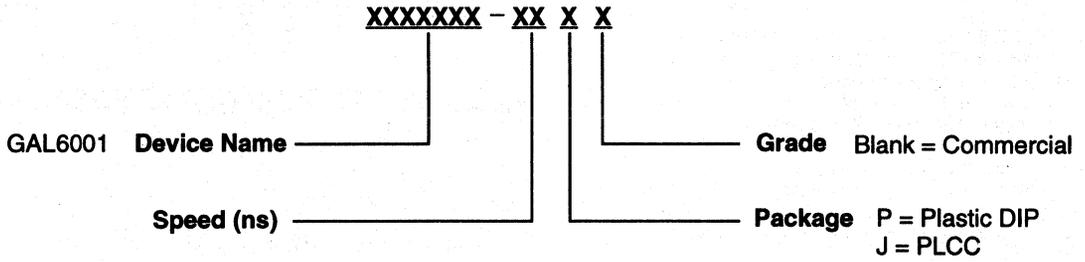
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GAL6001 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fclk (MHz)	Icc (mA)	Ordering #	Package
30	27	150	GAL6001-30P	24-Pin Plastic DIP
		150	GAL6001-30J	28-Lead PLCC
35	22.9	150	GAL6001-35P	24-Pin Plastic DIP
		150	GAL6001-35J	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide system designers with unparalleled design flexibility. With

the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

2**OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)**

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, "D-type register with sum term (asynchronous) clock", or "D/E-type register." Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a "D/E type registered", the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a "D type register with a sum term clock", the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

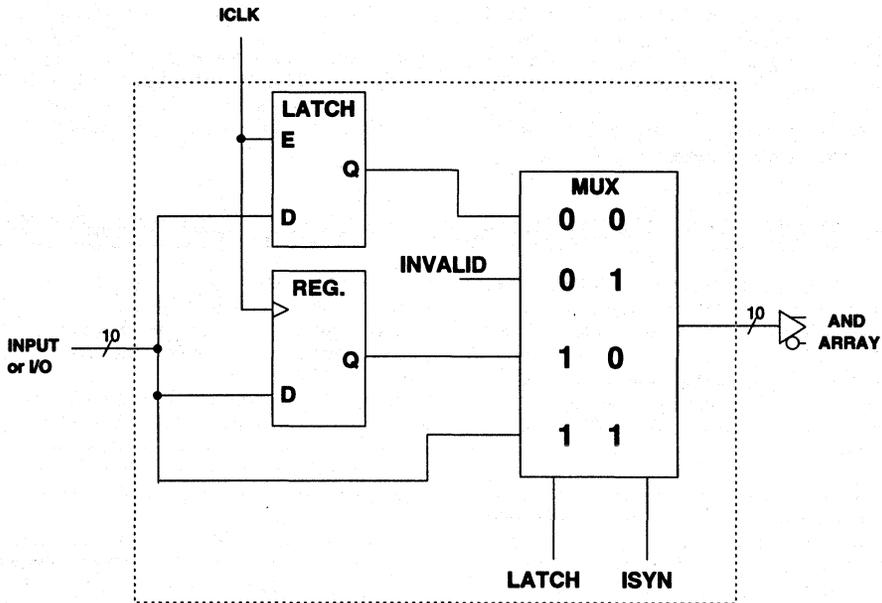
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

ILMC AND IOLMC CONFIGURATIONS



ILMC/IOLMC
Generic Logic Block Diagram

ILMC (Input Logic Macrocell)
JEDEC Fuse Numbers

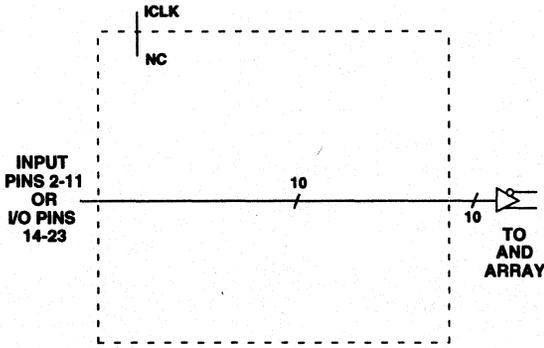
ISYN	LATCH
8218	8219

IOLMC (I/O Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8220	8221

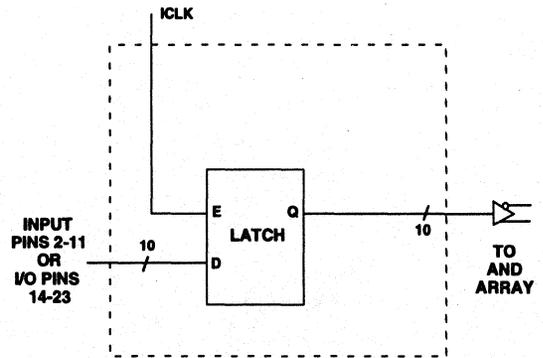
ILMC AND IOLMC CONFIGURATIONS

2



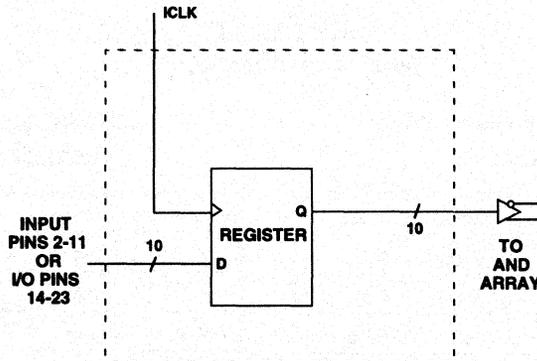
Asynchronous Input

ISYN	LATCH
1	1



Latched Input

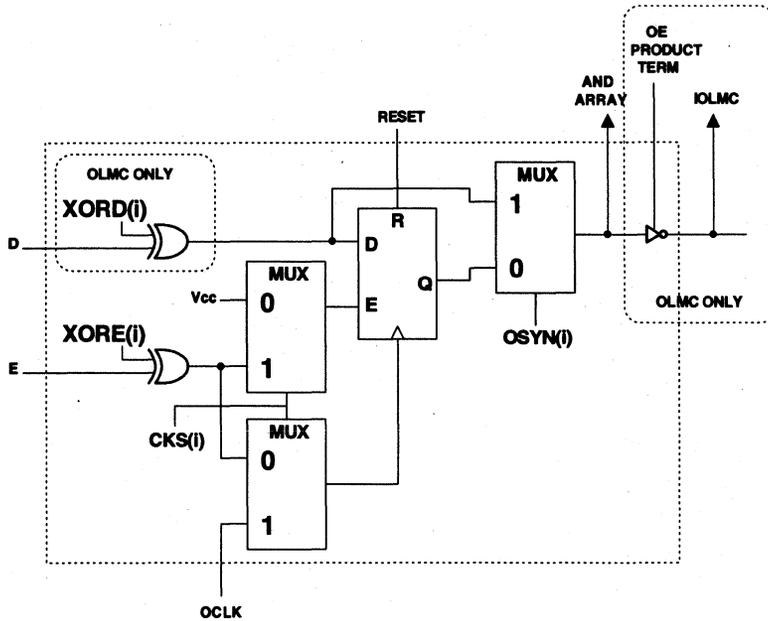
ISYN	LATCH
0	0



Registered Input

ISYN	LATCH
0	1

OLMC AND BLMC CONFIGURATIONS



OLMC/BLMC

Generic Logic Block Diagram

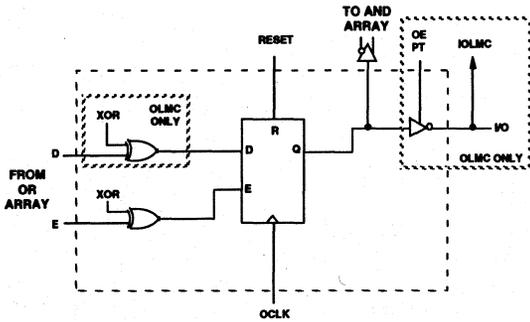
OLMC (Output Logic Macrocell) JEDEC Fuse Numbers

OLMC	OCLK	OSYN	XORD	XORE
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC (Buried Logic Macrocell) JEDEC Fuse Numbers

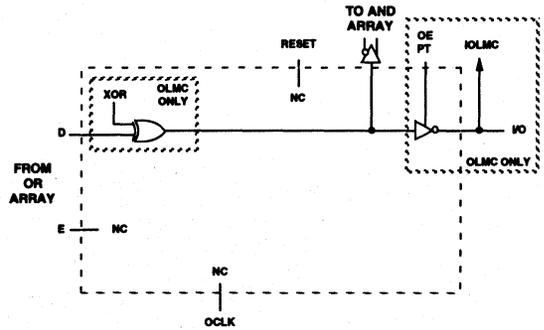
BLMC	OCLK	OSYN	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

OLMC AND BLMC CONFIGURATIONS



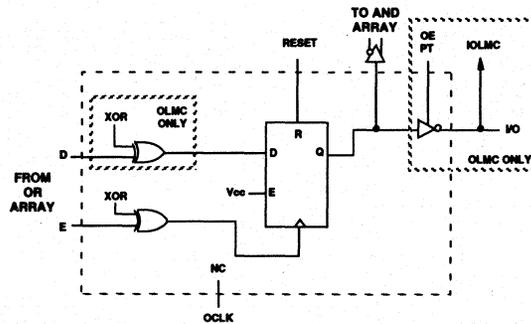
D/E Type Registered

OSYN(i)	OCKS(i)
0	1



Combinatorial

OSYN(i)	OCKS(i)
1	0

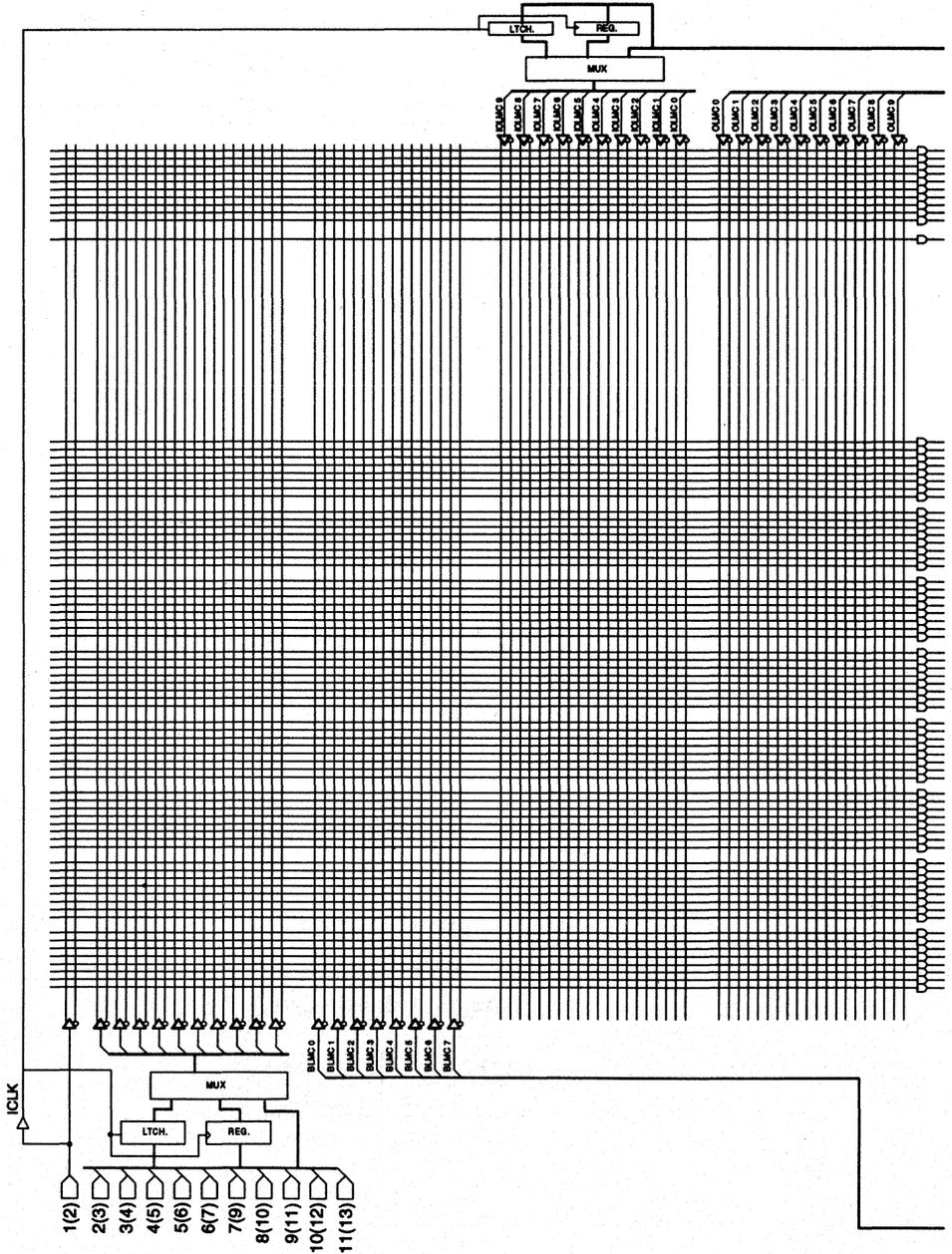


**D Type Register
with Sum Term
Asynchronous Clock**

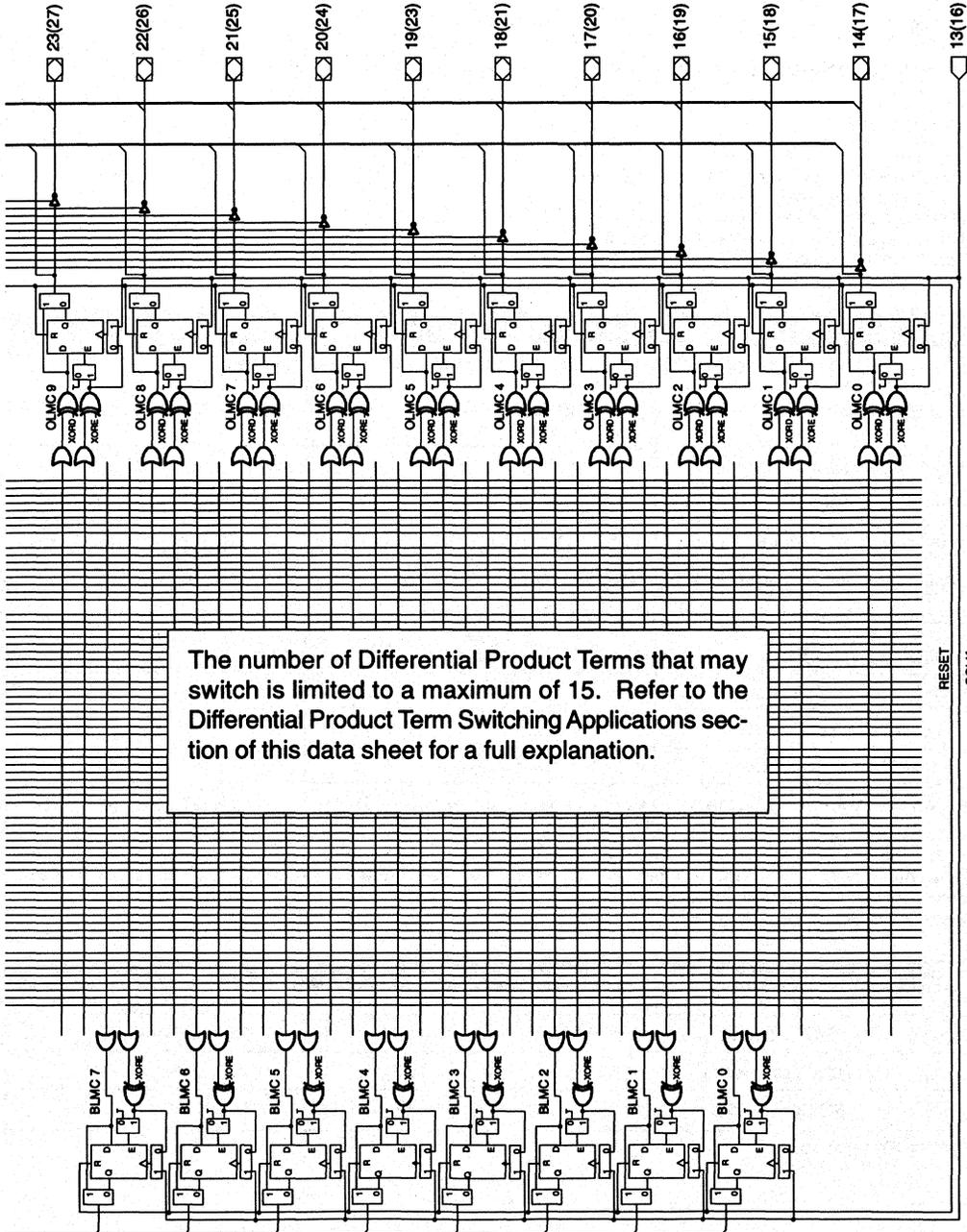
OSYN(i)	OCKS(i)
0	0

2

GAL6001 LOGIC DIAGRAM



GAL6001 LOGIC DIAGRAM (Cont.)



The number of Differential Product Terms that may switch is limited to a maximum of 15. Refer to the Differential Product Term Switching Applications section of this data sheet for a full explanation.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V$	-30	—	-130	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$ Outputs Open (no load)	—	90	150	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{IO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

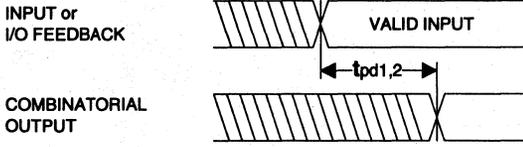
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

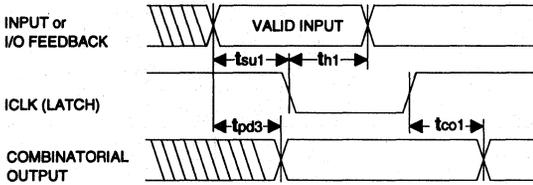
PARAMETER	TEST COND ¹ .	DESCRIPTION	-30		-35		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd1}	1	Combinatorial Input to Combinatorial Output	—	30	—	35	ns
t_{pd2}	1	Feedback or I/O to Combinatorial Output	—	30	—	35	ns
t_{pd3}	1	Transparent Latch Input to Combinatorial Output	—	35	—	40	ns
t_{co1}	1	Input Latch ICLK to Combinatorial Output Delay	—	35	—	40	ns
t_{co2}	1	Input Reg. ICLK to Combinatorial Output Delay	—	35	—	40	ns
t_{co3}	1	Output D/E Reg. OCLK to Output Delay	—	12	—	13.5	ns
t_{co4}	1	Output D Reg. Sum Term CLK to Output Delay	—	35	—	40	ns
t_{su1}	—	Setup Time, Input before Input Latch ICLK	2.5	—	3.5	—	ns
t_{su2}	—	Setup Time, Input before Input Reg. ICLK	2.5	—	3.5	—	ns
t_{su3}	—	Setup Time, Input or Feedback before D/E Reg. OCLK	25	—	30	—	ns
t_{su4}	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK	7.5	—	10	—	ns
t_{su5}	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	30	—	35	—	ns
t_{su6}	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	15	—	17	—	ns
t_{h1}	—	Hold Time, Input after Input Latch ICLK	5	—	5	—	ns
t_{h2}	—	Hold Time, Input after Input Reg. ICLK	5	—	5	—	ns
t_{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK	-5	—	-5	—	ns
t_{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	10	—	12.5	—	ns
f_{max}	—	Maximum Clock Frequency, OCLK	27	—	22.9	—	MHz
t_{wh1}	—	ICLK or OCLK Pulse Duration, High	10	—	10	—	ns
t_{wh2}	—	Sum Term CLK Pulse Duration, High	15	—	15	—	ns
t_{wl1}	—	ICLK or OCLK Pulse Duration, Low	10	—	10	—	ns
t_{wl2}	—	Sum Term CLK Pulse Duration, Low	15	—	15	—	ns
t_{arw}	—	Reset Pulse Duration	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	25	—	30	ns
t_{dis}	3	Input or I/O to Output Disabled	—	25	—	30	ns
t_{ar}	1	Input or I/O to Asynchronous Reg. Reset	—	35	—	35	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	20	—	20	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	10	—	10	—	ns

1) Refer to Switching Test Conditions section.

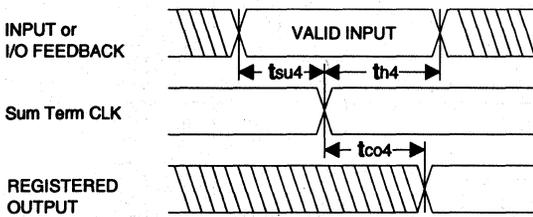
SWITCHING WAVEFORMS



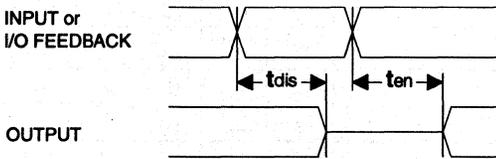
Combinatorial Output



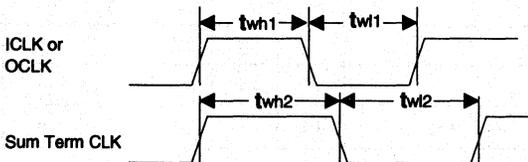
Latched Input



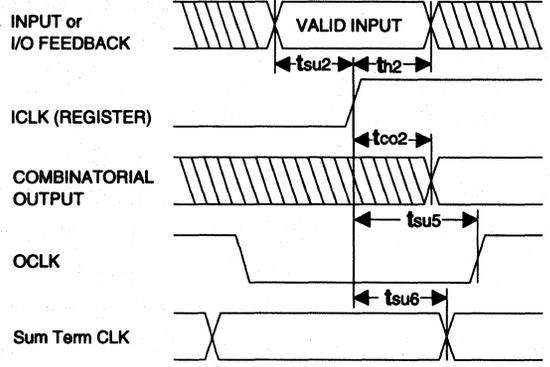
Registered Output (Sum Term CLK)



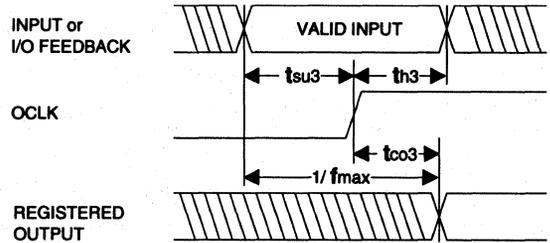
Input or I/O to Output Enable/Disable



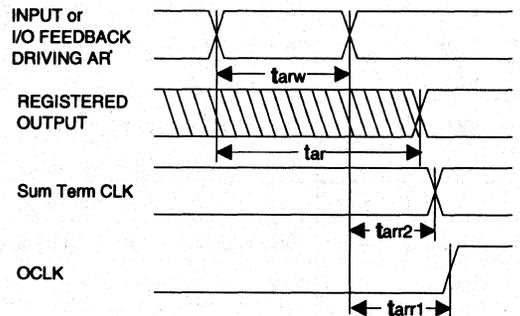
Clock Width



Registered Input



Registered Output (OCLK)



Asynchronous Reset

SWITCHING TEST CONDITIONS

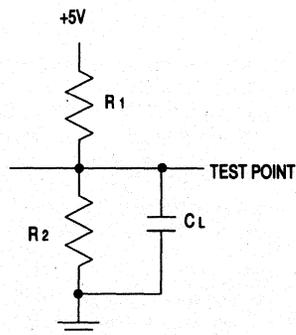
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	300Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	300Ω	390Ω
3	Active High	∞	5pF
	Active Low	300Ω	390Ω

FROM OUTPUT (O/Q)
UNDER TEST



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE WORD

An electronic signature (ES) is provided with every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

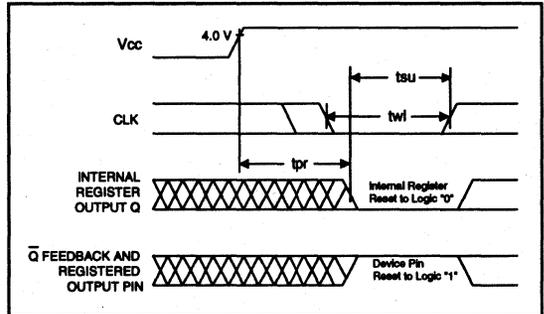
INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET

Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.



2

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (P\text{-Terms})_{LH} - (P\text{-Terms})_{HL} \right|$$

DPTS restricts the number of product terms that can be switched

simultaneously - there is no limit on the number of product terms that can be used.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering Dept. (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Military Program Overview	3-1
Military Ordering Information	3-3
GAL16V8A/B Military Datasheet	3-5
GAL20V8A Military Datasheet	3-13
GAL22V10/B Military Datasheet	3-19
GAL26CV12 Military Datasheet	3-27
GAL20RA10 Military Datasheet	3-33

Section 4: pLSI and ispLSI Products

Section 5: GAL Quality and Reliability

Section 6: GAL Technical Notes

Section 7: GAL Application Briefs

Section 8: Article Reprints

Section 9: General Information

Military Program Overview

CORPORATE PHILOSOPHY

Lattice Semiconductor is committed to leadership in performance and quality. Our family of military GAL devices is consistent with this philosophy. Lattice manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial through Military 883, are monitored under a quality program conformant to MIL-M-38510 Appendix A with inspections conformant to MIL-I-45208.

Complete reviews of Lattice's procedures, documentation and technical data are welcomed and can be arranged at the Company's facility near Portland, Oregon.

QUALITY AND TESTABILITY

Lattice Semiconductor processes its GAL devices to strict conformance with MIL-STD-883 Class B. In conjunction with the military flow, the inherent testability of E²CMOS technology allows Lattice to achieve a quality level superior to other PLD technologies.

All GAL devices are patterned and tested dozens of times throughout the manufacturing flow. Every GAL device is tested under worst case configurations to assure customers achieve 100% yields. Tests are performed using the same E² cell array that will be used for the final patterning of the devices. This 100% "actual test" philosophy does away with the correlated and simulated testing that is necessary with bipolar and UV (EPROM) based PLD devices.

RELIABILITY

Lattice Semiconductor performs extensive reliability testing prior to product release. This testing continues in the form of Reliability Monitors that are run on an ongoing basis to assure continued process integrity. A formal, written report of these test results is updated regularly and can be obtained from your local Lattice Sales Representative.

The reliability testing performed includes extensive analysis of fundamental design and process integrity. The reprogrammable nature of GAL devices allows for an inherently more thorough reliability evaluation than other programmable alternatives.

MIL-STD-883 COMPLIANCE

MIL-STD-883 provides a uniform and precise method for environmental, mechanical and electrical testing which ensures the suitability of microelectronic devices for use in military and aerospace systems. Table I summarizes the MIL-STD-883, Class B flow. Table II summarizes the conformance testing required by MIL-STD-883, Method 5005, for quality conformance testing of Lattice military microcircuits.

MIL-M-38510

MIL-M-38510, when used in conjunction with MIL-STD-883, defines design, packaging, material, marking, sampling, qualification and quality system requirements for military devices.

GROUP DATA

Group A and B data is taken on every inspection lot per MIL-STD-883, Class B requirements. This data, along with Generic Group C and D data can be supplied, upon written request, with your device shipment. Your Lattice sales representative can advise you of charges and leadtime necessary for providing this data.

STANDARD MILITARY DRAWINGS

Lattice actively supports the DESC Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883 product specifications to simplify military procurement.

Lattice recognizes the growing demand for SMD qualified devices, and in response, all new 883 product released by Lattice will be submitted to DESC for SMD qualification. Customers may facilitate this process by submitting a "Nonstandard Part Approval Request", DD Form 2052, to DESC. This form allows you to recommend to DESC the qualification of Lattice devices to SMD status.

A list of currently available SMD qualified devices is provided (see Military Ordering Information). Contact your local Lattice sales representative for the latest status of SMD qualifications in process with DESC.

Military Program Overview

**MILITARY SCREENING FLOW
(TABLE I)**

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E	100%
Hermeticity	1014	100%
Fine	Cond. A or B	
Gross	Cond. C	
Endurance Test	1033	100%
Retention Test	Unbiased Bake 24 HRS. T _A = 180°C	100%
Pre Burn-In Electrical	Applicable Device Specification T _c = 25°C	100%
Dynamic Burn-In	1015 Cond. D	100%
Post Burn-In Electrical	Applicable Device Specification T _c = 25°C PDA = 5%	100%
Final Electrical Test	Applicable Device Specification T _c = 125°C	100%
Final Electrical Test	Applicable Device Specification T _c = -55°C	100%
Final Electrical Test	Applicable Device Specification T _c = 25°C	100%
External Visual	2009	100%
QCI Sample Selection	MIL-M-38510 Sec. 4.5 and MIL-STD-883 Sec. 1.2	Sample

**MILITARY QUALITY CONFORMANCE
INSPECTIONS (TABLE II)**

Subgroup	Method	Sample
GROUP A: Electrical Tests		
<i>Subgroups 1, 7, 9</i> Electrical Test	Applicable Device Spec. 25°C	LTPD = 2
<i>Subgroups 2, 8A, 10</i> Electrical Test	Applicable Device Spec. Max. Operating Temp.	LTPD = 2
<i>Subgroups 3, 8B, 11</i> Electrical Test	Applicable Device Spec. Min. Operating Temp.	LTPD = 2
GROUP B: Mechanical Tests		
<i>Subgroup 2</i> Solvent Resistance	2015	4(0)
<i>Subgroup 3</i> Solderability	2003	LTPD = 10
<i>Subgroup 5</i> Bond Strength	2011	LTPD = 15
GROUP C: Chip Integrity Tests		
<i>Subgroup 1</i> Dynamic Life Test End Point Electrical	1005, 1,000 HRS. 125°C Applicable Device Spec.	LTPD = 5
<i>Subgroup 2</i> Unbiased Retention End Point Electrical	1,000 HRS. 150°C Applicable Device Spec.	LTPD = 5
GROUP D: Environmental Integrity		
<i>Subgroup 1</i> Physical Dimensions	2016	LTPD = 15
<i>Subgroup 2</i> Lead Integrity Hermeticity	2004, Cond. B 1014	LTPD = 5
<i>Subgroup 3</i> Thermal Shock Temp. Cycle Moisture Resistance Hermeticity Visual Examination Endpoint Electrical	1011, Cond. B, 15 Cycles 1010, Cond. C, 100 Cycles 1004 1014 1004, 1010 Applicable Device Spec.	LTPD = 15
<i>Subgroup 4</i> Mechanical Shock Vibration Constant Acceleration Hermeticity Visual Examination Endpoint Electrical	2002, Cond. B 2007, Cond. A 2001, Cond. E 1014 1010, 1011 Applicable Device Spec.	LTPD = 15
<i>Subgroup 5</i> Salt Atmosphere Hermeticity Visual Examination	1009, Cond. A 1014 1009	LTPD = 15
<i>Subgroup 6</i> Internal Water Vapor	1018 < 5,000 PPM, 100°C	3(0)
<i>Subgroup 7</i> Lead Finish Adhesion	2025	LTPD = 15
<i>Subgroup 8</i> Lid Torque	2024	5(0)

Military Ordering Information

Lattice offers the most comprehensive line of military E²CMOS Programmable Logic Devices. Lattice recognizes the trend in military device procurement towards using SMD compliant devices and encourages customers

to use the SMD number where it exists, when ordering parts. Listed below are Lattice's military qualified devices and their corresponding SMD numbers. Please contact your local Lattice representative for the latest product listing.

Military Products Selector Guide

DEVICE TYPE	Tpd (ns)	Icc (mA)	PACKAGE	LATTICE PART #	SMD #
GAL16V8	10	130	20-Pin Cerdip	GAL16V8B-10LD/883	5962-8983904RA
		130	20-Pin LCC	GAL16V8B-10LF/883	5962-89839042A
	15	130	20-Pin Cerdip	GAL16V8A-15LD/883	5962-8983903RA
		130	20-Pin LCC	GAL16V8A-15LF/883	5962-89839032A
	20	65	20-Pin Cerdip	GAL16V8A-20QD/883	5962-8983906RA
		65	20-Pin LCC	GAL16V8A-20QF/883	5962-89839062A
		130	20-Pin Cerdip	GAL16V8A-20LD/883	5962-8983902RA
		130	20-Pin LCC	GAL16V8A-20LF/883	5962-89839022A
	25	65	20-Pin Cerdip	GAL16V8A-25QD/883	5962-8983905RA
		65	20-Pin LCC	GAL16V8A-25QF/883	5962-89839052A
	30	130	20-Pin Cerdip	GAL16V8A-30LD/883	5962-8983901RA
		130	20-Pin LCC	GAL16V8A-30LF/883	5962-89839012A
GAL20V8	15	130	24-Pin Cerdip	GAL20V8A-15LD/883	5962-8984003LA
		130	28-Pin LCC	GAL20V8A-15LF/883	5962-89840033A
	20	65	24-Pin Cerdip	GAL20V8A-20QD/883	Contact Factory
		65	28-Pin LCC	GAL20V8A-20QF/883	Contact Factory
		130	24-Pin Cerdip	GAL20V8A-20LD/883	5962-8984002LA
		130	28-Pin LCC	GAL20V8A-20LF/883	5962-89840023A
	25	65	24-Pin Cerdip	GAL20V8A-25QD/883	Contact Factory
		65	28-Pin LCC	GAL20V8A-25QF/883	Contact Factory
	30	130	24-Pin Cerdip	GAL20V8A-30LD/883	5962-8984001LA
		130	28-Pin LCC	GAL20V8A-30LF/883	5962-89840013A
GAL22V10	15	150	24-Pin Cerdip	GAL22V10B-15LD/883	5962-8984103LA
		150	28-Pin LCC	GAL22V10B-15LF/883	5962-89841033A
	20	150	24-Pin Cerdip	GAL22V10-20LD/883	5962-8984102LA
		150	28-Pin LCC	GAL22V10-20LF/883	5962-89841023A
	25	150	24-Pin Cerdip	GAL22V10-25LD/883	5962-8984104LA
		150	28-Pin LCC	GAL22V10-25LF/883	5962-89841043A
	30	150	24-Pin Cerdip	GAL22V10-30LD/883	5962-8984101LA
		150	28-Pin LCC	GAL22V10-30LF/883	5962-89841013A
GAL26CV12	20	160	28-Pin Cerdip	GAL26CV12-20LD/883	Contact Factory
		160	28-Pin LCC	GAL26CV12-20LF/883	Contact Factory
	25	160	28-Pin Cerdip	GAL26CV12-25LD/883	Contact Factory
		160	28-Pin LCC	GAL26CV12-25LF/883	Contact Factory
GAL20RA10	20	120	24-Pin Cerdip	GAL20RA10-20LD/883	Contact Factory
		120	28-Pin LCC	GAL20RA10-20LF/883	Contact Factory
	25	120	24-Pin Cerdip	GAL20RA10-25LD/883	Contact Factory
		120	28-Pin LCC	GAL20RA10-25LF/883	Contact Factory

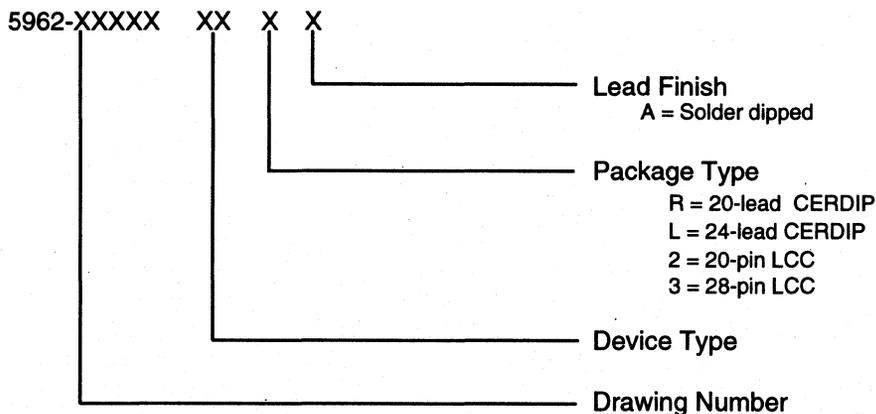
Military Ordering Information

DESC Standard Military Drawing Listing

SMD #	LATTICE PART #
5962-89839012A	GAL16V8A-30LR/883
5962-8983901RA	GAL16V8A-30LD/883
5962-89839022A	GAL16V8A-20LR/883
5962-8983902RA	GAL16V8A-20LD/883
5962-89839032A	GAL16V8A-15LR/883
5962-8983903RA	GAL16V8A-15LD/883
5962-89839042A	GAL16V8B-10LR/883
5962-8983904RA	GAL16V8B-10LD/883
5962-89839052A	GAL16V8A-25QR/883
5962-8983905RA	GAL16V8A-25QD/883
5962-89839062A	GAL16V8A-20QR/883
5962-8983906RA	GAL16V8A-20QD/883
5962-89840013A	GAL20V8A-30LR/883

SMD #	LATTICE PART #
5962-8984001LA	GAL20V8A-30LD/883
5962-89840023A	GAL20V8A-20LR/883
5962-8984002LA	GAL20V8A-20LD/883
5962-89840033A	GAL20V8A-15LR/883
5962-8984003LA	GAL20V8A-15LD/883
5962-89841013A	GAL22V10-30LR/883
5962-8984101LA	GAL22V10-30LD/883
5962-89841023A	GAL22V10-20LR/883
5962-8984102LA	GAL22V10-20LD/883
5962-89841033A	GAL22V10B-15LR/883
5962-8984103LA	GAL22V10B-15LD/883
5962-89841043A	GAL22V10-25LR/883
5962-8984104LA	GAL22V10-25LD/883

Standard Military Drawing Number Description





GAL16V8B/883 GAL16V8A/883

High Performance E²CMOS PLD

FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - F_{max} = 62.5 MHz
 - 7 ns Maximum from Clock Input to Data Output
 - TTL Compatible 24 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8B)**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 20-pin PAL[®] Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

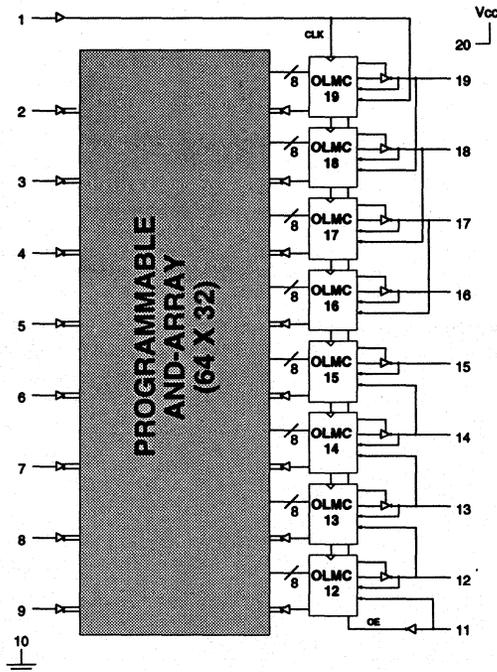
DESCRIPTION

The GAL16V8B/883 and GAL16V8A/883 are high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883. These military grade devices combine a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market. The GAL16V8B/883, at 10ns maximum propagation delay time, is the world's fastest military qualified CMOS PLD. CMOS circuitry allows the GAL16V8A quarter power devices to consume just 45mA typical I_{cc}, which represents a 75% savings in power when compared to bipolar counterparts.

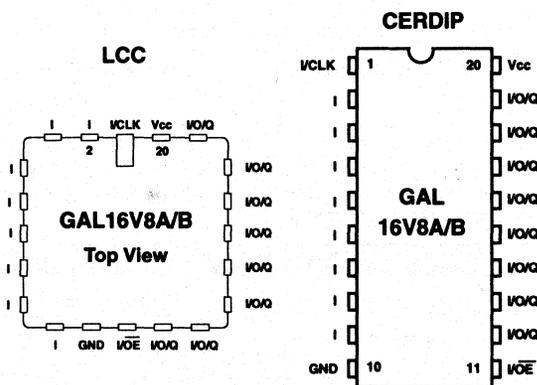
Generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8A/883 and GAL16V8B/883 are capable of emulating all standard 20-pin PAL[®] devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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Specifications **GAL16V8B/883**

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied-2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied-2.5 to $V_{CC} + 1.0V$
 Storage Temperature-65 to 150°C
 Case Temperature with
 Power Applied-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C)-55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 25 \text{ MHz}$ Outputs Open (no load)	—	75	130	mA

- 1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	2	10	ns
t_{co}	1	Clock to Output Delay	1	7	ns
t_{cf}	—	Clock to Feedback Delay	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	58.8	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	58.8	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	10	ns
	2	\overline{OE} to Output Enabled	—	10	ns
t_{dis}	3	Input or I/O to Output Disabled	—	10	ns
	3	\overline{OE} to Output Disabled	—	10	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.
- 3) Refer to **f_{max} Descriptions** section.

SWITCHING TEST CONDITIONS

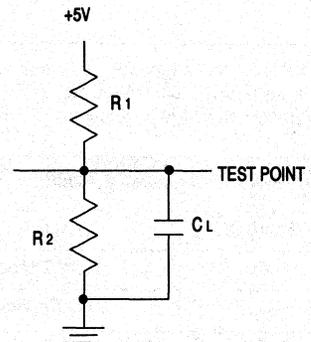
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	390Ω	750Ω	50pF
2	Active High	∞	750Ω
	Active Low	390Ω	750Ω
3	Active High	∞	750Ω
	Active Low	390Ω	750Ω

FROM OUTPUT (Q/Q)
UNDER TEST



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ L -15/-20/-30	—	75	130	mA
		Outputs Open (no load) f _{toggle} = 25MHz Q -20/-25	—	45	65	mA

- 1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- 2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{io}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{io} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	15	3	20	3	25	3	30	ns
t_{co}	1	Clock to Output Delay	2	12	2	15	2	15	2	20	ns
t_{cf}	—	Clock to Feedback Delay	—	12	—	15	—	15	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	15	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	0	—	ns
f_{max} ³	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	33.3	—	33.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	15	—	15	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	—	25	—	30	ns
	2	\overline{OE} to Output Enabled	—	15	—	18	—	20	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	—	25	—	30	ns
	3	\overline{OE} to Output Disabled	—	15	—	18	—	20	—	25	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

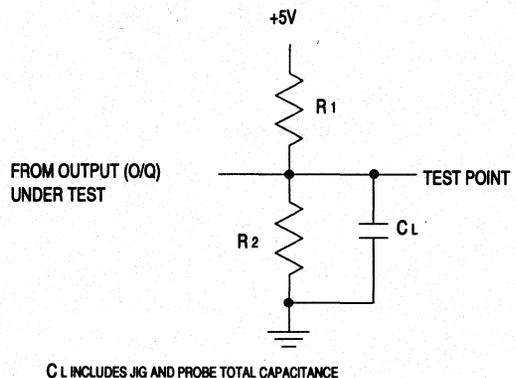
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

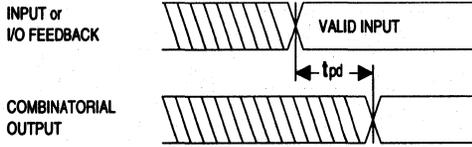
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

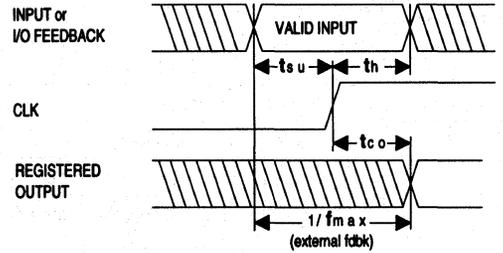
Test Condition	R ₁	R ₂	C _L
1	390Ω	750Ω	50pF
2	Active High	∞	750Ω
	Active Low	390Ω	750Ω
3	Active High	∞	750Ω
	Active Low	390Ω	750Ω



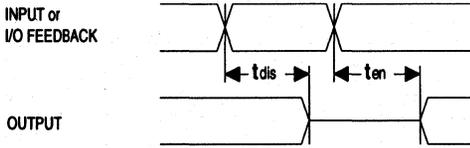
SWITCHING WAVEFORMS



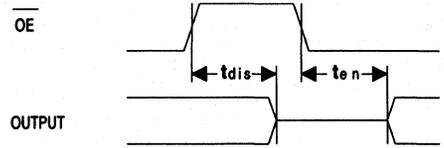
Combinatorial Output



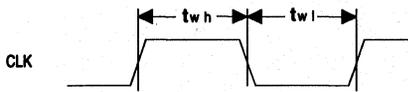
Registered Output



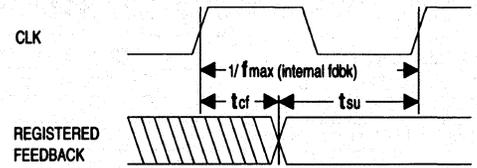
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

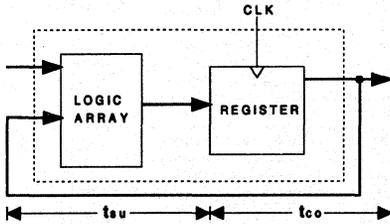


Clock Width



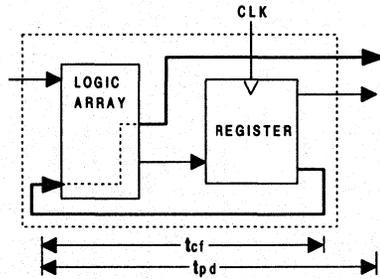
fmax with Feedback

fmax DESCRIPTIONS



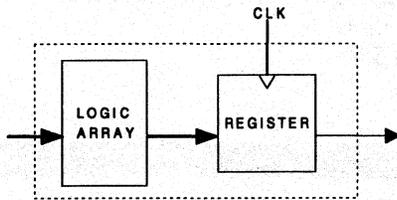
fmax with External Feedback $1/(t_{su}+t_{co})$

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback $1/(t_{su}+t_{cf})$

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/ internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to $t_{cf} + t_{pd}$.



fmax Without Feedback

Note: fmax with no feedback may be less than $1/(t_{wh} + t_{wl})$ this is to allow for a clock duty cycle of other than 50%.



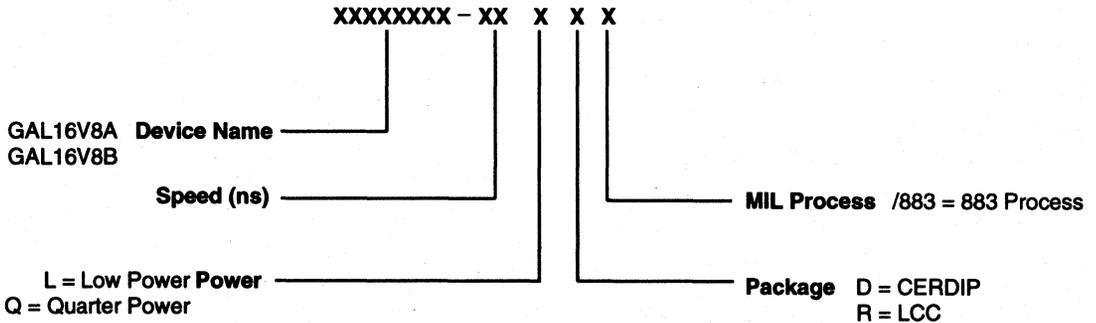
Specifications **GAL16V8B/883** **GAL16V8A/883**

GAL16V8A/B ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
10	10	7	130	20-Pin Cerdip	GAL16V8B-10LD/883	5962-8983904RA
			130	20-Pin LCC	GAL16V8B-10LR/883	5962-89839042A
15	12	12	130	20-Pin Cerdip	GAL16V8A-15LD/883	5962-8983903RA
			130	20-Pin LCC	GAL16V8A-15LR/883	5962-89839032A
20	15	15	65	20-Pin Cerdip	GAL16V8A-20QD/883	5962-8983906RA
			65	20-Pin LCC	GAL16V8A-20QR/883	5962-89839062A
			130	20-Pin Cerdip	GAL16V8A-20LD/883	5962-8983902RA
			130	20-Pin LCC	GAL16V8A-20LR/883	5962-89839022A
25	20	15	65	20-Pin Cerdip	GAL16V8A-25QD/883	5962-8983905RA
			65	20-Pin LCC	GAL16V8A-25QR/883	5962-89839052A
30	25	20	130	20-Pin Cerdip	GAL16V8A-30LD/883	5962-8983901RA
			130	20-Pin LCC	GAL16V8A-30LR/883	5962-89839012A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION





GAL20V8A/883

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - F_{max} = 50 MHz
 - 12 ns Maximum from Clock Input to Data Output
 - TTL Compatible 24 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

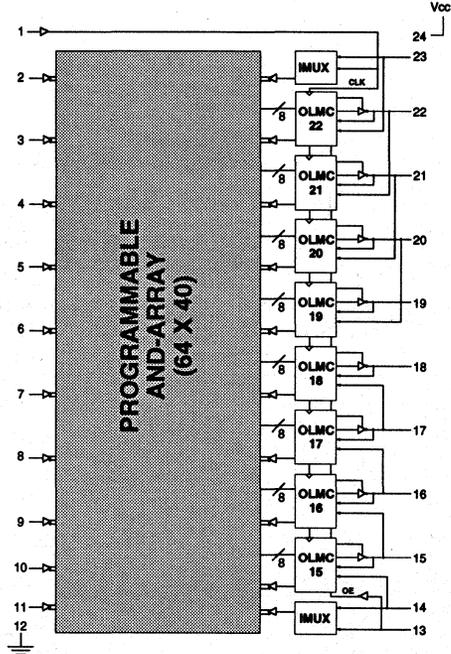
DESCRIPTION

The GAL20V8A/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. The GAL20V8A/883, at 15ns maximum propagation delay time, is the world's fastest military qualified 24-pin CMOS PLD. CMOS circuitry allows the GAL20V8A quarter power device to consume just 45mA typical I_{cc}, which represents a 75% savings in power when compared to bipolar counterparts.

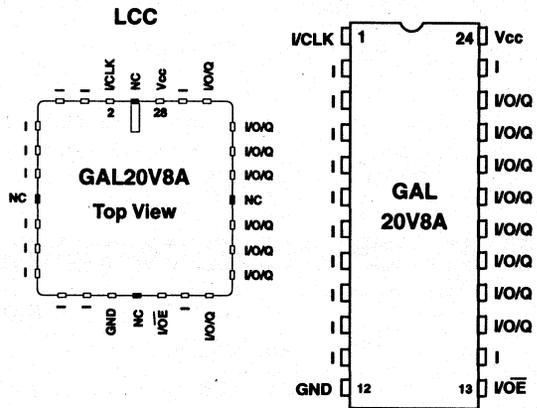
Generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8A/883 is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}¹	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	L -15/-20/-30	75	130	mA
		Outputs Open (no load) $f_{toggle} = 25MHz$				

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	15	3	20	3	25	3	30	ns
t_{co}	1	Clock to Output Delay	2	12	2	15	2	15	2	20	ns
t_{cf}^2	—	Clock to Feedback Delay	—	12	—	15	—	15	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	15	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	33.3	—	33.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	15	—	15	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	—	25	—	30	ns
	2	\overline{OE} to Output Enabled	—	15	—	18	—	20	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	—	25	—	30	ns
	3	\overline{OE} to Output Disabled	—	15	—	18	—	20	—	25	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

SWITCHING TEST CONDITIONS

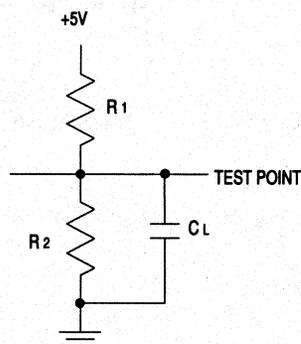
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

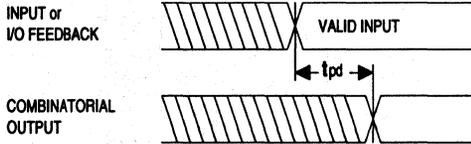
Test Condition	R ₁	R ₂	C _L
1	390Ω	750Ω	50pF
2	Active High	∞	750Ω
	Active Low	390Ω	750Ω
3	Active High	∞	750Ω
	Active Low	390Ω	750Ω

FROM OUTPUT (O/Q)
UNDER TEST

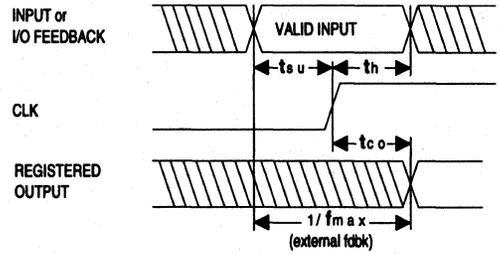


C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

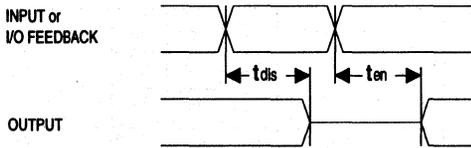
SWITCHING WAVEFORMS



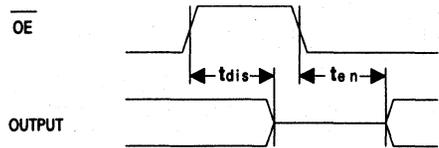
Combinatorial Output



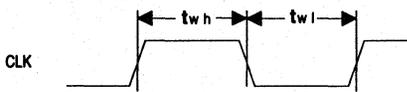
Registered Output



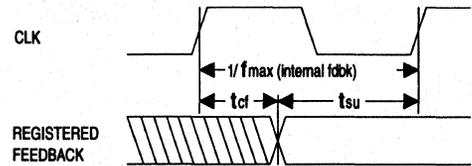
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

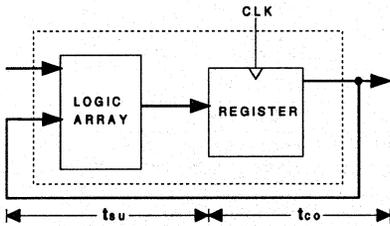


Clock Width



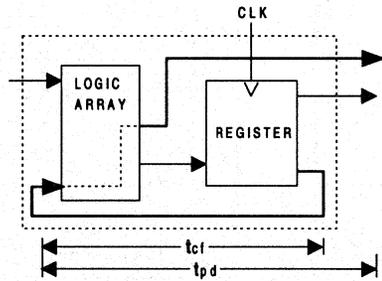
fmax with Feedback

f_{max} DESCRIPTIONS



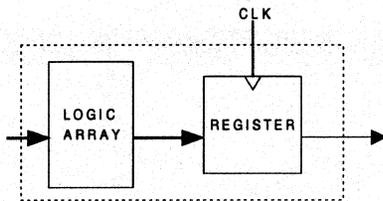
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.



f_{max} Without Feedback

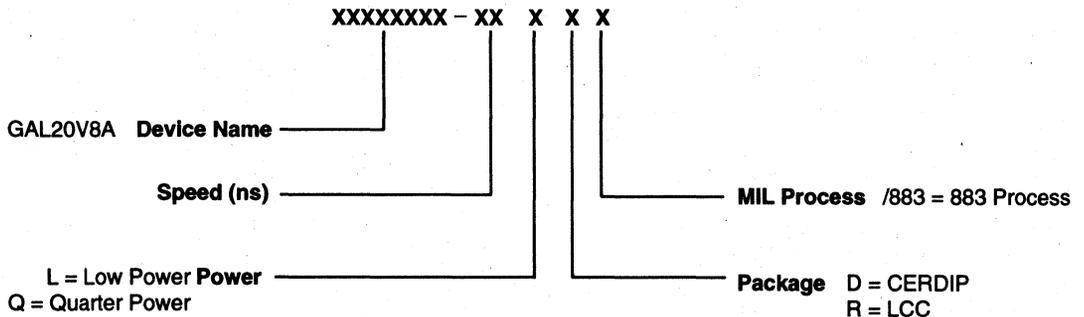
Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

GAL20V8A ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
15	12	12	130	24-Pin CERDIP	GAL20V8A-15LD/883	5962-8984003LA
			130	28-Pin LCC	GAL20V8A-15LR/883	5962-89840033A
20	15	15	65	24-Pin CERDIP	GAL20V8A-20QD/883	Contact Factory
			65	28-Pin LCC	GAL20V8A-20QR/883	Contact Factory
			130	24-Pin CERDIP	GAL20V8A-20LD/883	5962-8984002LA
			130	28-Pin LCC	GAL20V8A-20LR/883	5962-89840023A
25	20	15	65	24-Pin CERDIP	GAL20V8A-25QD/883	Contact Factory
			65	28-Pin LCC	GAL20V8A-25QR/883	Contact Factory
30	25	20	130	24-Pin CERDIP	GAL20V8A-30LD/883	5962-8984001LA
			130	28-Pin LCC	GAL20V8A-30LR/883	5962-89840013A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION





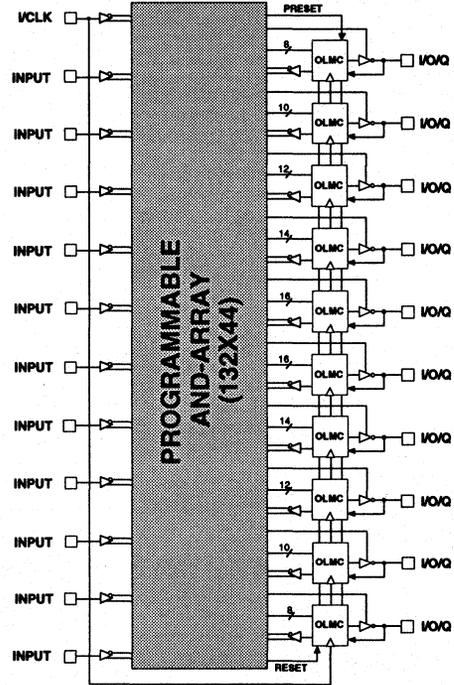
GAL22V10B/883 GAL22V10/883

High Performance E²CMOS PLD

FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - F_{max} = 62.5 MHz
 - 8ns Maximum from Clock Input to Data Output
 - TTL Compatible 12 mA Outputs
 - UltraMOS[®] Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMS 22V10 Devices
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



3

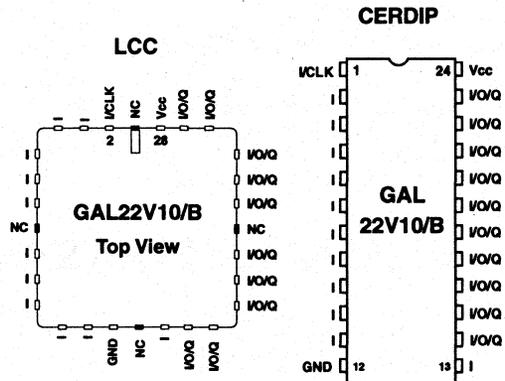
DESCRIPTION

The GAL22V10B/883 and GAL22V10/883 are high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883. These military grade devices combine a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10/B to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10B and GAL22V10 are fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL[®] products.

PACKAGE DIAGRAMS



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	—	90	150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	15	ns
t_{co}	1	Clock to Output Delay	—	8	ns
t_{cf}	—	Clock to Feedback Delay	—	8	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	50	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	50	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

 3) Refer to **f_{max} Description** section.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC}	-0.5 to +7V
Input voltage applied	-2.5 to $V_{CC} + 1.0V$
Off-state output voltage applied	-2.5 to $V_{CC} + 1.0V$
Storage Temperature	-65 to 150°C
Case Temperature with Power Applied	-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C)	-55 to 125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-150	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \quad \text{Outputs Open}$	—	90	150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{io}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{io} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

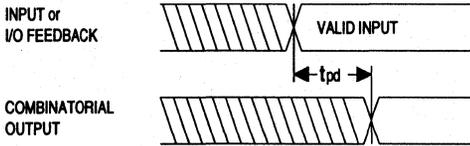
PARAMETER	TEST COND. ¹	DESCRIPTION	-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	—	25	—	30	ns
t_{co}	1	Clock to Output Delay	—	15	—	20	—	20	ns
t_{cf}²	—	Clock to Feedback Delay	—	15	—	20	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	17	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	ns
f_{max}³	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	31.2	—	25	—	22	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	31.2	—	25	—	22	—	MHz
	1	Maximum Clock Frequency with No Feedback	33	—	33	—	25	—	MHz
t_{wh}	—	Clock Pulse Duration, High	15	—	15	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	15	—	15	—	20	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	—	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	—	30	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	20	—	25	—	30	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	20	—	25	—	30	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	17	—	20	—	25	—	ns

 1) Refer to **Switching Test Conditions** section.

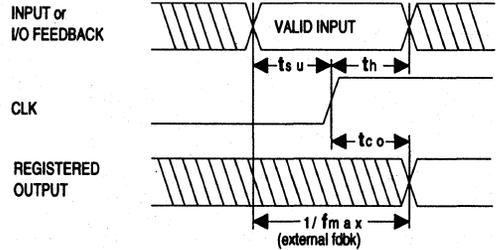
 2) Calculated from f_{max} with internal feedback. Refer to f_{max} **Description** section.

 3) Refer to f_{max} **Description** section.

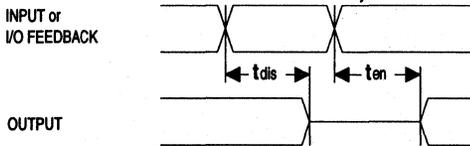
SWITCHING WAVEFORMS



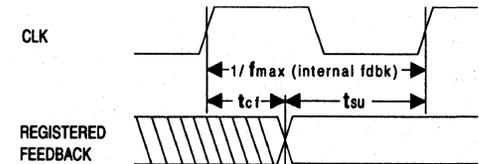
Combinatorial Output



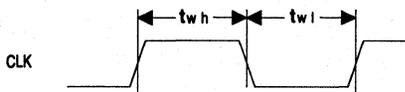
Registered Output



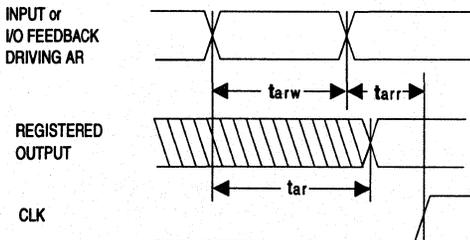
Input or I/O to Output Enable/Disable



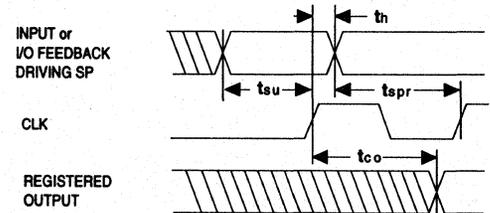
fmax with Feedback



Clock Width

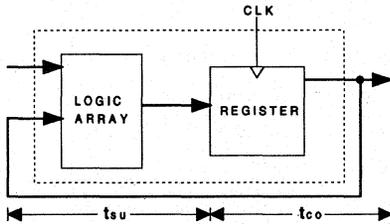


Asynchronous Reset



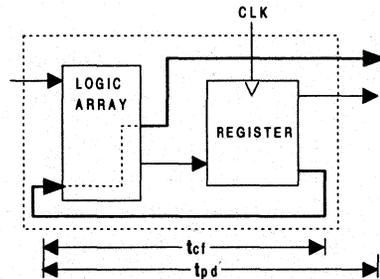
Synchronous Preset

f_{max} DESCRIPTIONS



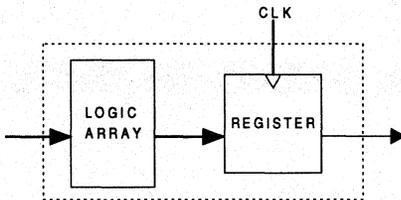
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/ internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

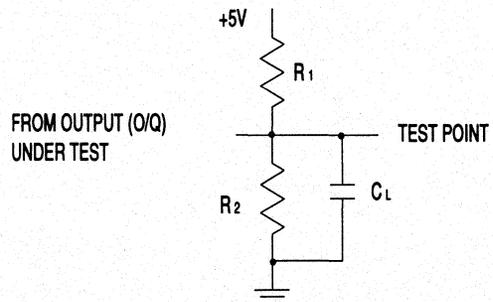
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	390Ω	750Ω	50pF
2	Active High	∞	750Ω
	Active Low	390Ω	750Ω
3	Active High	∞	5pF
	Active Low	390Ω	750Ω



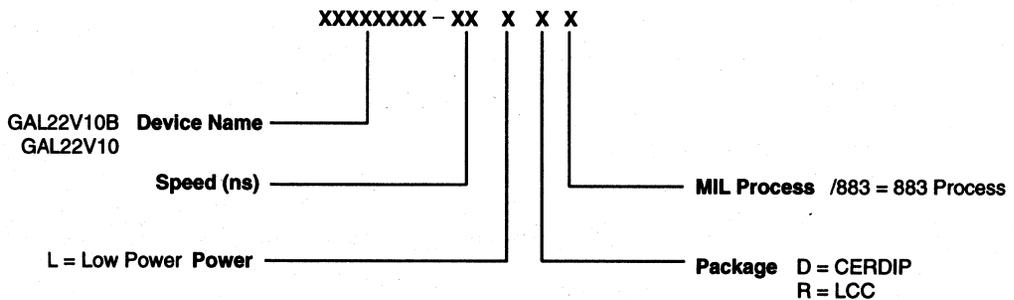
C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

GAL22V10/B ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
15	12	8	150	24-Pin Cerdip	GAL22V10B-15LD/883	5962-8984103LA
				28-Pin LCC	GAL22V10B-15LR/883	5962-89841033A
20	17	15	150	24-Pin Cerdip	GAL22V10-20LD/883	5962-8984102LA
				28-Pin LCC	GAL22V10-20LR/883	5962-89841023A
25	20	20	150	24-Pin Cerdip	GAL22V10-25LD/883	5962-8984104LA
				28-Pin LCC	GAL22V10-25LR/883	5962-89841043A
30	25	20	150	24-Pin Cerdip	GAL22V10-30LD/883	5962-8984101LA
				28-Pin LCC	GAL22V10-30LR/883	5962-89841013A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

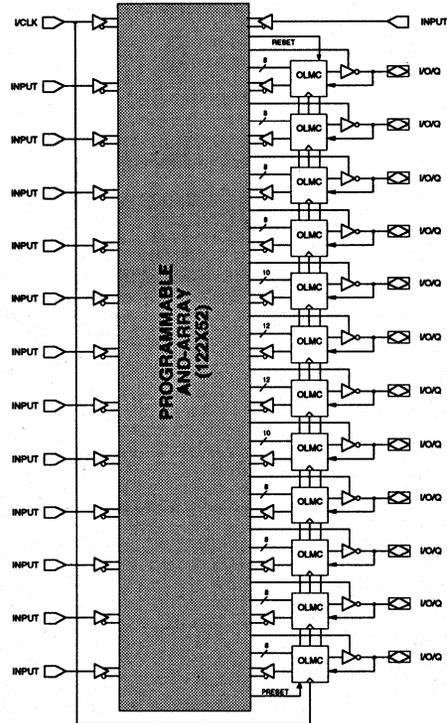
PART NUMBER DESCRIPTION



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 20 ns Maximum Propagation Delay
 - F_{max} = 33 MHz
 - 15 ns Maximum from Clock Input to Data Output
 - TTL Compatible 8 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL INPUTS AND I/Os**
- **LOW POWER CMOS**
 - 90 mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TWELVE OUTPUT LOGIC MACROCELLS**
 - Uses Standard 22V10 Macrocells
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



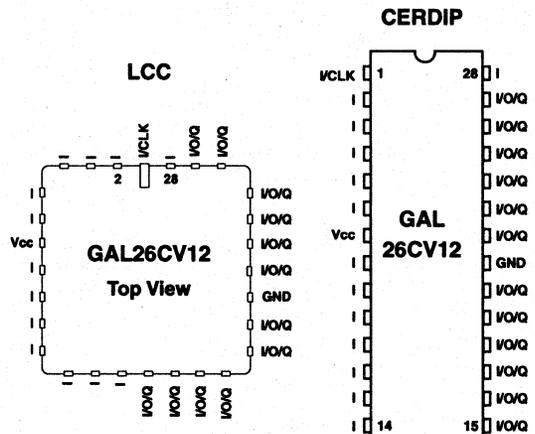
DESCRIPTION

The GAL26CV12/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. The GAL26CV12-20/883 combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the fastest 28-pin military PLD on the market. CMOS circuitry allows the GAL26CV12 to consume less power than comparable bipolar devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

By building on the popular 22V10 architecture, the military version of the GAL26CV12 allows designers to be immediately productive, eliminating the learning curve. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

PACKAGE DIAGRAMS



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to +125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \quad \text{Outputs Open}$	—	90	160	mA

- 1) The leakage current is due to the internal pull-up on all input and I/O pins. See Input Buffer section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_I = 2.0V$
C_{IO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

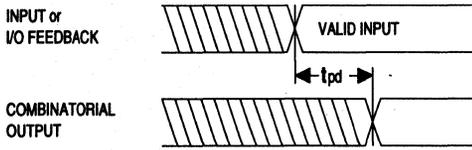
PARAMETER	TEST COND. ¹	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
t_{co}	1	Clock to Output Delay	—	15	—	20	ns
t_{cf}	—	Clock to Feedback Delay	—	15	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	17	—	20	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	31.2	—	25	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	31.2	—	25	—	MHz
	1	Maximum Clock Frequency with No Feedback	33.3	—	30	—	MHz
t_{wh}	—	Clock Pulse Duration, High	15	—	15	—	ns
t_{wl}	—	Clock Pulse Duration, Low	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	20	—	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	20	—	25	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	17	—	20	—	ns

 1) Refer to **Switching Test Conditions** section.

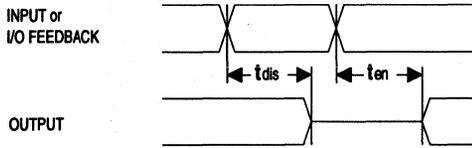
 2) Calculated from f_{max} with internal feedback. Refer to f_{max} **Description** section.

 3) Refer to f_{max} **Description** section.

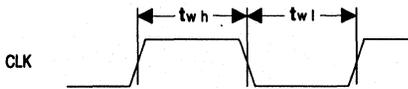
SWITCHING WAVEFORMS



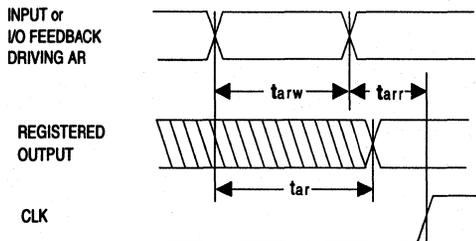
Combinatorial Output



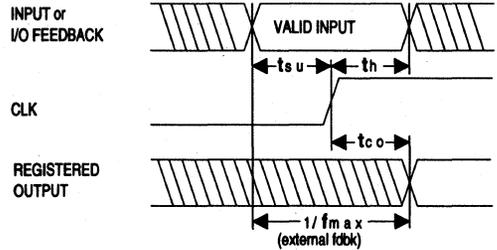
Input or I/O to Output Enable/Disable



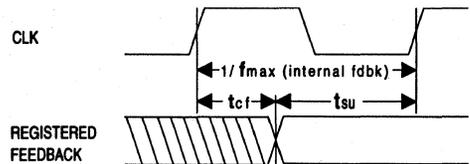
Clock Width



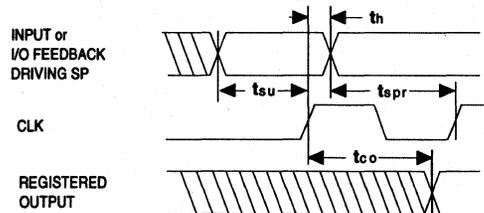
Asynchronous Reset



Registered Output

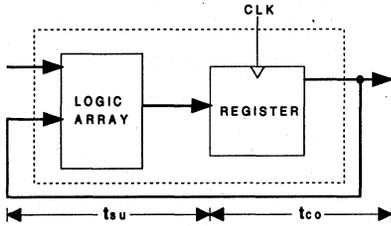


f_{max} with Feedback



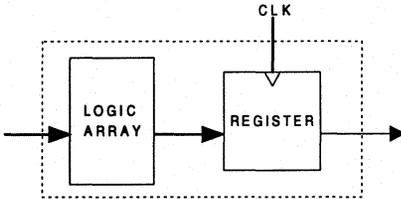
Synchronous Preset

f_{max} SPECIFICATIONS



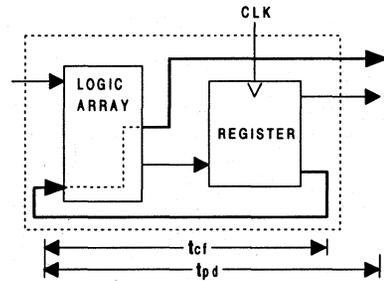
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: tcf is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to tcf + tpd.

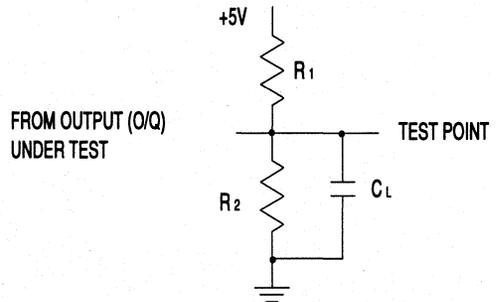
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	470Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	470Ω	390Ω
3	Active High	∞	5pF
	Active Low	470Ω	390Ω

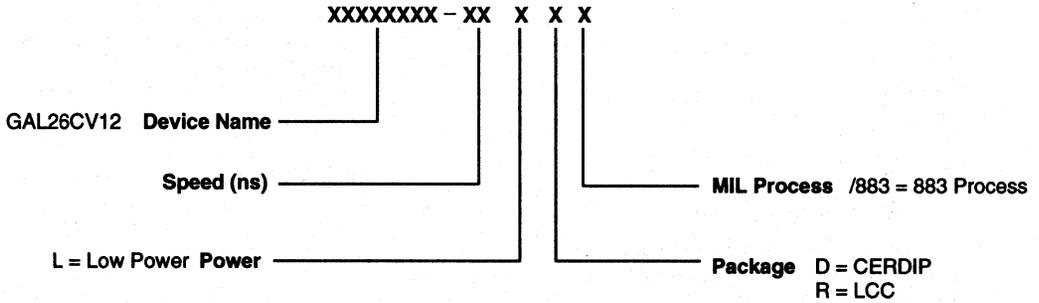


C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

GAL26CV12 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
20	17	15	160	28-Pin Cerdip	GAL26CV12-20LD/883	Contact Factory
			160	28-Pin LCC	GAL26CV12-20LR/883	Contact Factory
25	20	20	160	28-Pin Cerdip	GAL26CV12-25LD/883	Contact Factory
			160	28-Pin LCC	GAL26CV12-25LR/883	Contact Factory

PART NUMBER DESCRIPTION





GAL20RA10/883

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 20 ns Maximum Propagation Delay
 - F_{max} = 41.7 MHz
 - 20 ns Maximum from Clock Input to Data Output
 - TTL Compatible 8 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc}
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100 ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Independent Programmable Clocks
 - Independent Asynchronous Reset and Preset
 - Registered or Combinatorial with Polarity
 - Full Function and Parametric Compatibility with PAL20RA10
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - State Machine Control
 - Standard Logic Consolidation
 - Multiple Clock Logic Designs
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

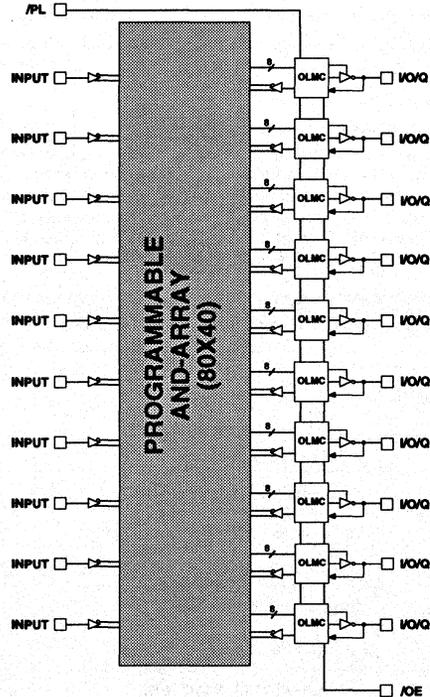
DESCRIPTION

The GAL20RA10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. With a 20ns maximum propagation delay time, it is the fastest military grade 20RA10 device on the market. In addition to speed performance, Lattice's Electrically Erasable (E²) floating gate technology provides low power performance. The GAL20RA10's typical I_{cc} of 75mA, represents a 50% savings in power when compared to bipolar counterparts. E² technology also offers high speed (<100ms) erase times providing the ability to reprogram or test the devices quickly and efficiently.

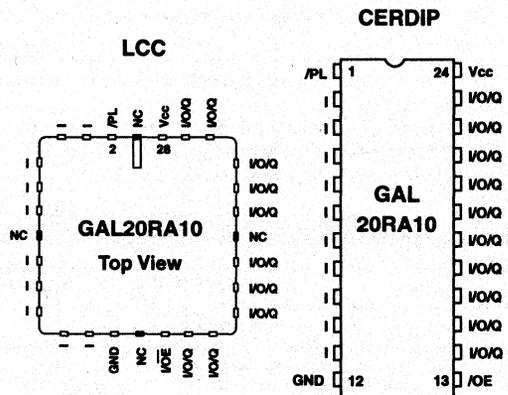
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE guarantees data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Military Devices:

Case Temperature (T_C) -55 to +125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15Mhz \quad \text{Outputs Open}$	—	75	120	mA

1) The leakage current is due to the internal pull-up on all pins. See the Input Buffer section in the commercial datasheet for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{IO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t _{pd}	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
t _{co}	1	Clock to Output Delay	—	20	—	25	ns
t _{su}	—	Setup Time, Input or Feedback before Clock	10	—	15	—	ns
t _h	—	Hold Time, Input or Feedback after Clock	3	—	5	—	ns
f _{max} ²	1	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	33.3	—	25.0	—	MHz
	1	Maximum Clock Frequency with No Feedback	41.7	—	33.3	—	MHz
t _{wh}	—	Clock Pulse Duration, High	12	—	15	—	ns
t _{wl}	—	Clock Pulse Duration, Low	12	—	15	—	ns
t _{en} / t _{dis}	2,3	Input or I/O to Output Enabled / Disabled	—	20	—	25	ns
t _{en} / t _{dis}	2,3	OE to Output Enabled / Disabled	—	15	—	15	ns
t _{ar} / t _{ap}	1	Input or I/O to Asynchronous Reset / Preset	—	20	—	25	ns
t _{arw} / t _{apw}	—	Asynchronous Reset / Preset Pulse Duration	20	—	25	—	ns
t _{arr} / t _{apr}	—	Asynchronous Reset / Preset Recovery Time	12	—	20	—	ns
t _{wp}	—	Preload Pulse Duration	20	—	25	—	ns
t _{sp}	—	Preload Setup Time	15	—	20	—	ns
t _{hp}	—	Preload Hold Time	15	—	20	—	ns

1) Refer to Switching Test Conditions section.

2) Refer to f_{max} Descriptions section.

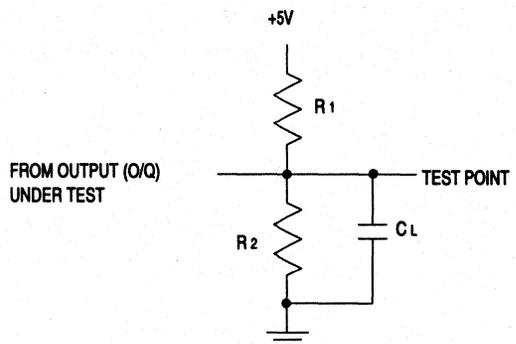
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

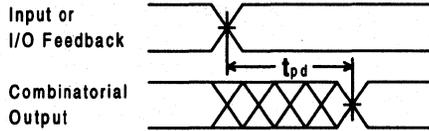
Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
1	470Ω	390Ω	50pF
2	Active High	∞	390Ω
	Active Low	470Ω	390Ω
3	Active High	∞	390Ω
	Active Low	470Ω	390Ω

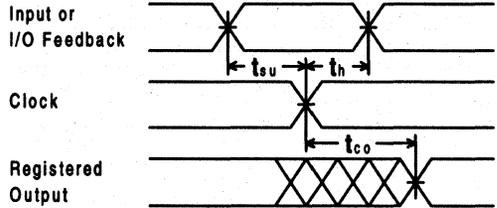


C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

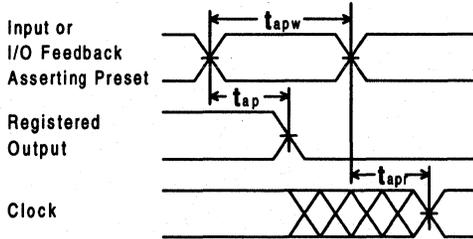
SWITCHING WAVEFORMS



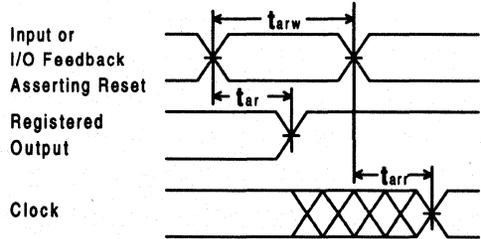
Combinatorial Output



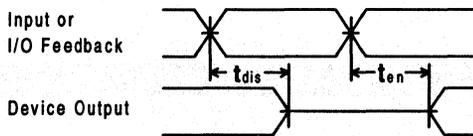
Registered Output



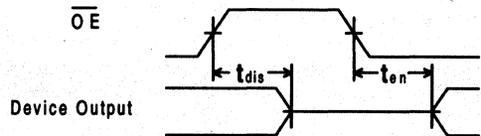
Asynchronous Preset



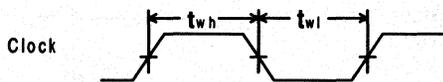
Asynchronous Reset



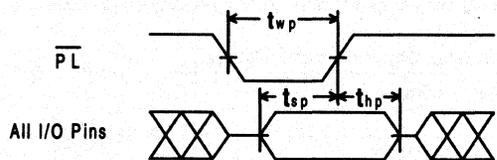
Input or I/O Feedback to Enable / Disable



OE to Enable / Disable

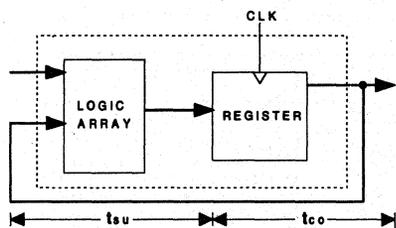


Clock Width



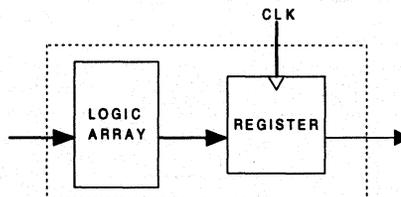
Parallel Preload

f_{max} DESCRIPTIONS



f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co} .



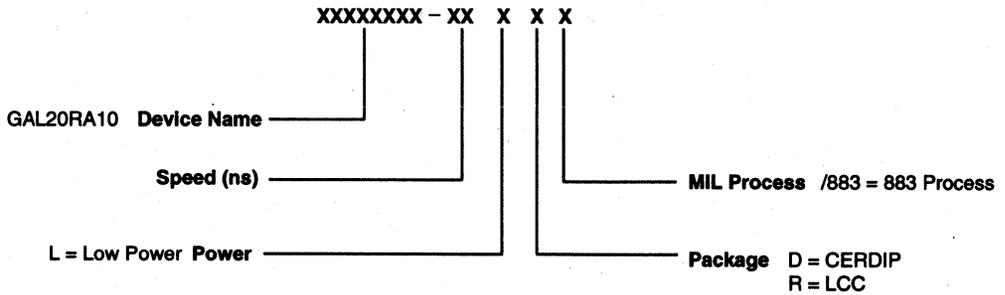
f_{max} With No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

GAL20RA10/883 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
20	10	20	120	24-Pin Cerdip	GAL20RA10-20LD/883	Contact Factory
				28-Pin LCC	GAL20RA10-20LR/883	Contact Factory
25	15	25	120	24-Pin Cerdip	GAL20RA10-25LD/883	Contact Factory
				28-Pin LCC	GAL20RA10-25LR/883	Contact Factory

PART NUMBER DESCRIPTION



Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: pLSI and ispLSI Products

Introduction to pLSI and ispLSI4-1

Section 5: GAL Quality and Reliability

Section 6: GAL Technical Notes

Section 7: GAL Application Briefs

Section 8: Article Reprints

Section 9: General Information

Introduction to pLSI™ and ispLSI™

Introduction to pLSI and ispLSI

Lattice Semiconductor's pLSI (programmable Large Scale Integration) and ispLSI (in-system programmable Large Scale integration) are two families of high density and high performance E²CMOS[®] programmable logic devices (see figure 1). They provide design engineers with a superior system solution for integrating high speed logic features on a single chip.

The Lattice pLSI and ispLSI families are the first programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI family also pioneers non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user reconfiguration.

Lattice's E²CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All the necessary development tools are available from Lattice and leading third-party companies. Utilizing a Windows-based graphical user interface, it is possible to complete a circuit design in hours, as opposed to days or weeks.

pLSI and ispLSI Product Families

- 80 MHz System Performance
- 15 ns tpd Pin-to-Pin
- Deterministic Performance
- High Density (2,000-8,000 PLD Gates)
- Flexible Architecture
- Easy to Use
- in-system programmable (ispLSI)
- Low Power Consumption

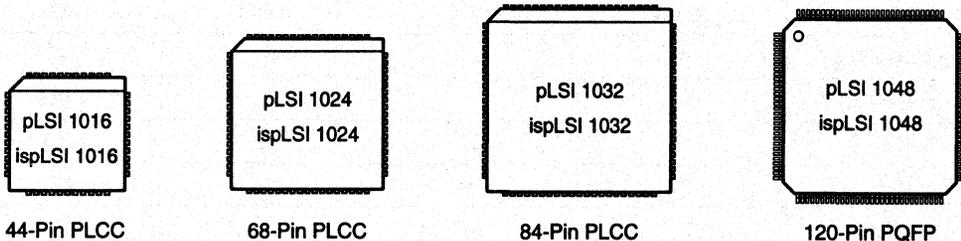
pLSI and ispLSI Technology

- E²CMOS — the PLD Technology of Choice
- Proven UltraMOS Technology
- Electrically Erasable/Programmable/Reprogrammable
- 100% Tested During Manufacture
- 100% Programming Yield
- High-Speed Programming

pLSI and ispLSI Development Tools

- Easy-to-Use Graphical Interface (Windows 3.0)
- Boolean Equations and Macro Input
- VHDL and Schematic Capture Entry
- Industry-Standard Third-Party Design Environment and Platforms
- Timing and Functional Simulation

Figure 1. pLSI and ispLSI Device Families



Introduction to pLSI and ispLSI

Family Overview

The pLSI and ispLSI families of high-density devices address high-performance system logic needs, ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD gate densities ranging from 2,000 to 8,000, the pLSI and ispLSI families provide a full range of programmable logic solutions to meet design requirements for today's and tomorrow's needs.

Each device contains multiple Generic Logic Blocks (GLBs), architected to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of more than 80% of available logic. Table 1 describes the family attributes.

The pLSI and ispLSI Architecture

The pLSI and ispLSI architecture was constructed with actual system design requirements in mind. This architecture provides the designer with the following advantages. Figure 2 shows the pLSI 1032 architecture.

- High Speed
- Predictable Performance
- Integration of Multiple Logic Functions
- Asynchronous Designs
- Flexible Logic Paths
- Advanced Global Clock Network

The Global Routing Pool (GRP)

Central to the pLSI and ispLSI architecture is the Global Routing Pool, which connects all of the internal logic and makes it available to the designer. The GRP provides complete interconnectivity with fixed and predictable delays. This unique connection scheme consistently provides high performance and allows effortless implementation of complex designs.

The Output Routing Pool (ORP)

Pin assignment flexibility is maximized via the Output Routing Pool (ORP), which provides the connections between the GLB outputs and the output pins.

Figure 2. pLSI 1032 Architecture

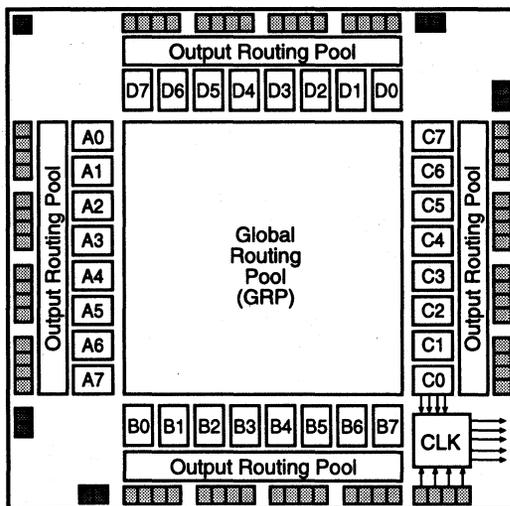


Table 1. pLSI and ispLSI Family Attributes

Family Member	1016	1024	1032	1048
Density (PLD Gates)	2,000	4,000	6,000	8,000
Speed: f_{max} (MHz)	80	80	80	70
Speed: t_{pd} (ns)	15	15	15	20
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs + I/O	36	54	72	106
Pin/Package	44-pin PLCC	68-pin PLCC	84-pin PLCC	120-pin PQFP

Introduction to pLSI and ispLSI

Generic Logic Block (GLB)

The basic logic element in the pLSI and ispLSI architecture is the Generic Logic Block. This powerful logic element provides an input-to-output ratio greater than 4:1. With 18 inputs driving an array of 20 product terms (PTs) — which in turn feed four outputs — the GLB efficiently handles both wide and narrow gating functions. Figure 3 describes the GLB functionality.

One element of architectural flexibility is the Product Term Sharing Array (PTSA). The PTSA allows the 20 Product Terms (PTs) from the AND array to be shared with any and all of the four GLB outputs as needed to implement logic designs. This ability to share PTs between all of the GLB outputs provides a highly efficient implementation of complex state machines by eliminating duplicate product term groups.

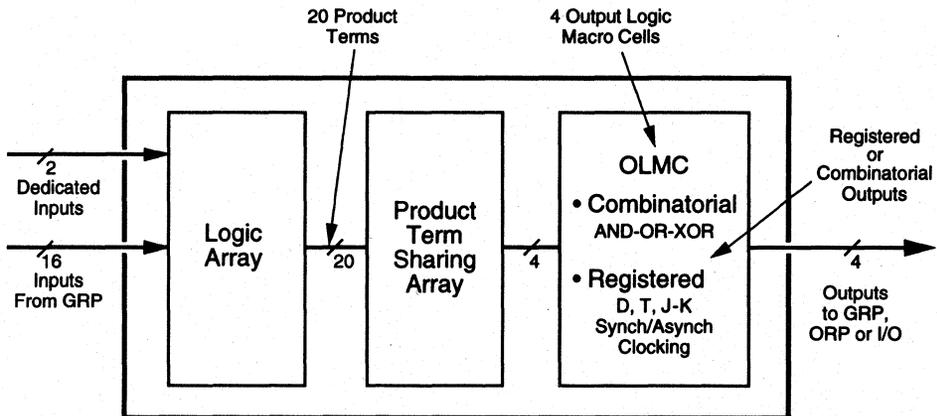
The architecture flexibility of the GLB, combined with its optimum input-to-output ratio, allows the GLB to implement virtually all 4-bit MSI functions.

Each of the four outputs from the PTSA feeds into a flexible Output Logic Macrocell (OLMC), consisting of a D-type flip-flop with an Exclusive-OR gate on the input. The OLMC allows each GLB output to be configured either combinatorial or registered. Combinatorial mode is available as AND-OR or Exclusive-OR; registered mode is available as D, T or J-K.

The GLB can be clocked synchronously or asynchronously. Global clocks from external pins or internally generated, provide all GLBs and I/O Cells with synchronous clock signals with selectable polarity. This provides multiple synchronous clock phases to all GLBs and I/Os.

4

Figure 3. Simplified Generic Logic Block Functionality



Introduction to pLSI and ispLSI

The GLB has several configuration options for each Output Logic Macrocell (OLMC). These can be mixed with each GLB. The configurations are described as standard, high-speed bypass, XOR and multi-mode configuration. Figure 4 demonstrates the multi-mode configuration.

Standard Configuration

- GLB Outputs Comprise of 4,4,5 or 7 Product Terms
- The PTSA Can Combine up to 20 PTs per GLB Output to Meet the Needs of Both Wide and Narrow Logic Functions.

High-Speed Bypass Configuration

- For Speed-Critical Timing Paths
- Enables Design of Fast Address Decoders

- Bypasses the PTSA and the Internal Exclusive-OR Gate of the OLMC
- Provides Four Product Terms Per Output

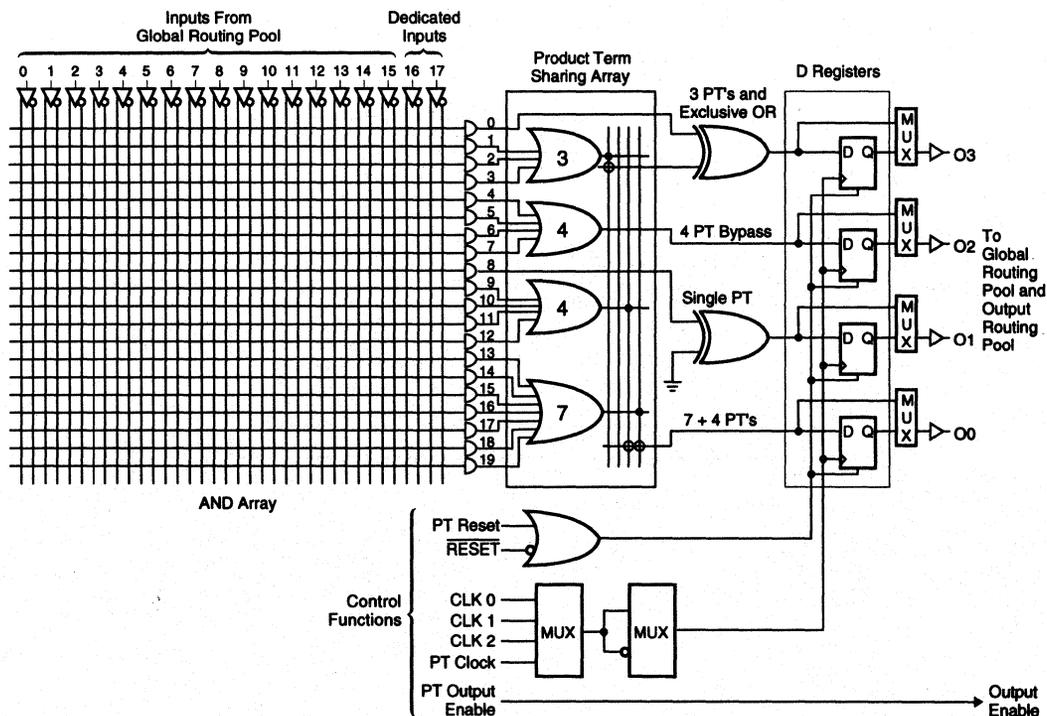
XOR Configuration

- Utilizes Powerful Exclusive-OR Architecture
- Powerful for Counters, Comparators and ALU Functions

Multi-Mode Configuration

- Individual Outputs are Independently Configurable
- PTSA Allows Flexibility on the Number and Selection of Product Terms Per Output

Figure 4. GLB: Multi-Mode Configuration



Introduction to pLSI and ispLSI

In-System Programmability

The in-system programmable Large Scale Integration (ispLSI) family is the industry's only high-density programmable logic family offering non-volatile in-system reconfigurability.

The ispLSI family is 100 percent functionally and parametrically compatible with the pLSI family, with the added ability of 5-volt in-system programmability and reprogrammability.

Complex logic functions can be implemented in multiple ispLSI devices, with complete on-board configurability. In-system programming of multiple ispLSI chip solutions is easily achieved through a proprietary in-system erase/program/verify technique.

In-system programmability can revolutionize the way boards are designed, manufactured and serviced (see figure 5).

Prototype board designs - in-system programming allows the programming and modification of logic designs "in-system" without removing the device(s) from the board.

This accelerates the system and board-level debug process and enables definition of board layout earlier in the design process.

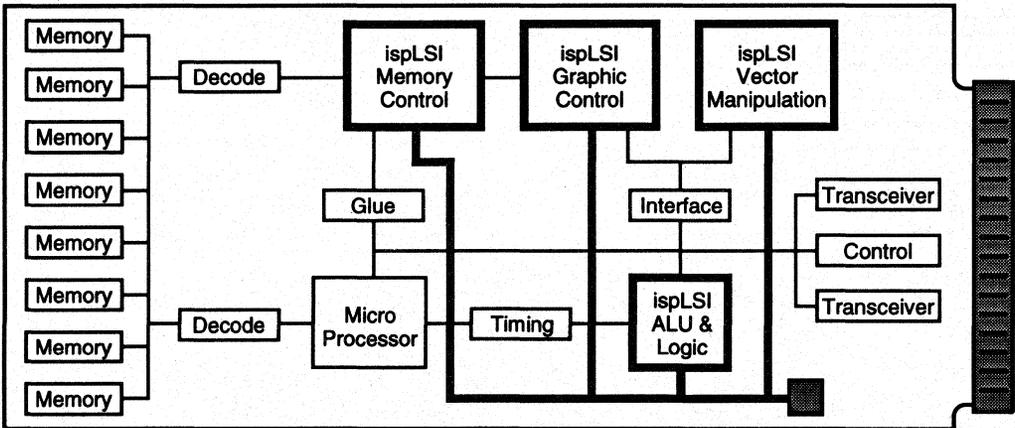
Reconfigurable systems - The options for accommodating changes are greatly increased when you have the ability to change the functionality of devices already soldered on a board. Multiple hardware configurations can be implemented with the same circuit board design. Multiple protocols or multiple system interfaces can be defined on a generic board as the last step in the manufacturing flow.

Diagnostic Capability - Using the ispLSI device, the diagnostic capability of the system can be enhanced. A test pattern can be programmed into the ispLSI device at board-test, enabling the logic to control and observe specific nodes of the entire board. After the diagnostic testing is complete, the functional pattern can be programmed into the device for normal system operation.

Easier field updates - With software reconfigurable systems, field updates are as easy as loading a new device configuration from a floppy, or downloading it through a modem.

4

Figure 5. in-system programmable "Generic" Board



Multiple ispLSI devices can be reconfigured through multiplexed signals interfaced via an edge connector, 5-post connector, microcontroller, or microprocessor.

□ ispLSI Devices
■ isp Interface

Introduction to pLSI and ispLSI

A powerful benefit of the ispLSI family is its potential to streamline the manufacturing process by eliminating the separate programming and labeling steps usually associated with PLDs. Quality is enhanced when product handling steps are reduced, in this case, those associated with programming, labeling and re-inventorying multiple device types. Eliminating socketing further improves quality and reduces board cost. Figure 6 shows the enhanced manufacturing with the ispLSI device.

All necessary programming is achieved via five TTL-level logic interface signals (see figure 7). These five signals control the on-chip programming circuitry, which is securely protected against inadvertent reprogramming via on-chip state machines. The ispLSI family can also be programmed using popular third-party logic programmers.

Figure 6. Manufacturing Flow Comparison

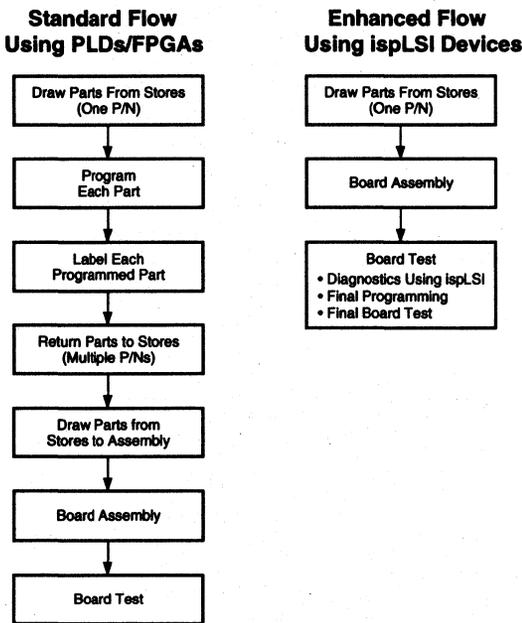
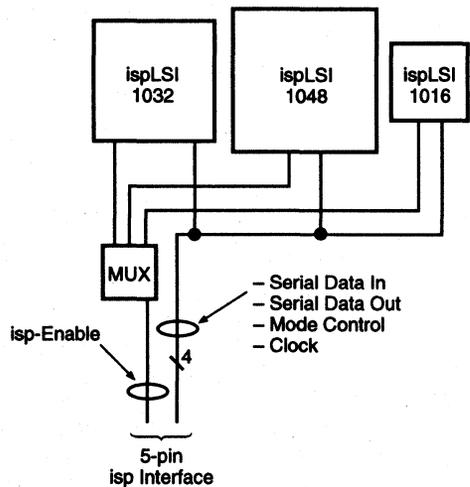


Figure 7. In-system programming Interface (Multi-Chip Solution)



Introduction to pLSI and ispLSI

pLSI/ispLSI Development System (pDS™)

The Lattice pLSI/ispLSI Development System (pDS) software is used to implement designs in pLSI and ispLSI devices. Quick and straightforward design alternatives can be implemented using the low cost Entry Level System or the Advanced Level System which features support from industry standard third party vendors. This section describes both the Entry Level and Advanced Level Development Systems. Programmer support is also discussed.

pDS—PC Entry Level

Features

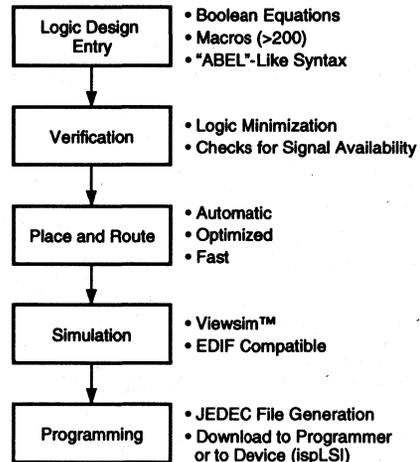
- High Performance, Low Cost Development Environment
- Supports pLSI and ispLSI Device Families
- Boolean Logic and Text File Design Entry
- Over 225 Macros Available
- Automatic Place and Route
- Logic Simulation with Viewlogic Viewsim
- JEDEC File Download Direct to Programmer or ispLSI Device

General Description

Both the pLSI and ispLSI families are supported by Lattice's low-cost pLSI/ispLSI Development System (pDS). It runs on IBM-compatible (386/486) PCs with Microsoft® Windows.

The easy-to-use graphical user interface with the familiar mouse driven pull-down menus, combined with Boolean logic data entry using ABEL-like syntax, makes design entry with the pLSI and ispLSI quick and straightforward (see figure 8).

Figure 8. pDS Design Flow



The pDS—PC Entry Level Software supports over 200 macros to help the design process. These macros cover most TTL functions, from gate primitives to 16-bit counters. pDS The software also supports user-definable macros which can be modifications of existing macros or custom creations.

The pDS—PC Entry Level Software automatically verifies the design, performs logic minimization and checks for signal availability.

Additionally, the Lattice Place and Route assigns pins and critical speed paths and ensures optimized 100% routability at 80% utilization.

Quick compilation speeds the design, debug and rework process dramatically. Incremental design techniques are also supported.

Timing and functional simulation are available from Lattice, using Viewsim simulation software.

The windows graphical user interface makes programming easy, using pull-down menus, intuitive point-and-click commands and self explanatory instructions. Without any up-front training, designs can be completed within hours instead of days or weeks.

Introduction to pLSI and ispLSI

pDS Advanced Level

Features

- Supports pLSI and ispLSI Device families
- Schematic capture, State Machine and VHDL Design Entry
- Expanded Macro Library
- Automatic Logic Minimization and Partitioning
- Automatic Place and Route
- Logic and Timing Simulation
- EDIF Compatible
- JEDEC File Download Direct to Programmer or ispLSI Device

General Description

For higher level design-entry environments, Lattice offers pLSI/ispLSI Advanced Development System software tools, which expand on the core capabilities of the pDS—PC Entry Level software. Schematic capture, state machine and VHDL entry are supported, along with an expanded macro library.

The Advanced Level software utilizes industry standard third-party design environments such as Viewlogic's Viewdraw and Data I/O's ABEL™.

Running on IBM compatible (386/486) PCs or workstation platforms, the Advanced Level Software supports automatic logic minimization and partitioning, as well as place and route, resulting in 100% routability at greater than 80% utilization.

For logic and timing simulation, support is available from Lattice through Viewlogic Viewsim simulation tools.

Third Party Programming Support

The pLSI and ispLSI families are supported by popular third-party logic programmers including Data I/O, Logical Devices, Stag, System General, SMS Microcomputer and Advin. Table 2 describes each vendor's specific programmer model that support the pLSI and ispLSI devices. No proprietary, expensive, high pin-count programmers are required. Additionally, the ispLSI family can be programmed on the board (in-system), which eliminates the need for a stand-alone programmer.

Table 2. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot GL/U40
	Pilot U84
BP Micro	PLD1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 32/40
	Allpro 88
SMS Microsystems	Sprint Expert
System General	Turpro 1

isp Engineering Kit

The ispLSI family may also be programmed with Lattice's isp Engineering Kit. This kit is designed for engineering purposes only and is not intended for production use. By connecting an 8 wire cable to the parallel printer port of a PC, JEDEC files can easily be downloaded into the ispLSI device. Additionally, this cable can be connected directly to the circuit board facilitating on board in-system programming.

Additional information on the pLSI and ispLSI Families may be obtained from a Lattice representative or by simply completing the reply card at the end of this data book.

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Quality Assurance Program

INTRODUCTION

Lattice views quality assurance as a corporate responsibility and an integral part of all planning activities. Lattice's Quality Assurance organization is independent from Manufacturing and has direct access to top management, assuring sufficient authority is afforded to quality issues.

Lattice's quality program is in full compliance to the quality assurance requirements of MIL-M-38510 Appendix A and all inspection system requirements of MIL-I-45208.

QUALIFICATION

All new products, processes and vendors must pass pre-defined evaluations before receiving initial qualification release. Major changes to products, processes or vendors require additional qualification before implementation. To assure continuing conformance to reliability requirements, an ongoing monitor program is maintained on all processes.

IN-PROCESS CONTROL

Qualified product must be manufactured under strict quality controls that start with regulated procurement and documented inspection plans for all incoming materials. Sample testing and in-line monitoring as well as statistical process control charts provide constant feedback at each critical step of the manufacturing process.

CALIBRATION

All critical equipment involved in the manufacture, testing, or inspection of Lattice product must meet the requirements of our established calibration system that is in compliance to MIL-STD-45662.

TRAINING

All Lattice manufacturing personnel complete a comprehensive training program and obtain formal certification for each production operation before they are allowed to manufacture products. Operators must be recertified on a periodic basis to assure ongoing compliance to all written procedures and specifications.

SUBCONTRACTOR CONTROL

All subcontracted operations must be performed by sources exhibiting a quality program commensurate to that of Lattice. These vendors are audited at least once every year to monitor their compliance to Lattice's Quality Assurance Program. Any major audit discrepancy requires corrective action and may result in disqualification.

DOCUMENT CONTROL

Lattice's document control system is under the direction of Quality Assurance and has the responsibility of assuring that every product has adequate written documentation released before production begins.

Drawings and specifications related to materials, processes, testing, products and subcontractors are maintained by the Document Control Department. A numbering system identifies each document by revision status, function and category.

Any change to existing documentation must be properly approved and released before implementation of the change. The change is implemented only if approved by the appropriate functional groups.

NONCONFORMING MATERIAL

Nonconforming material is identified, segregated, analyzed and dispositioned according to procedures that also require corrective action be specified to eliminate the cause of the defect.

Lattice has a Material Review Board (MRB) to investigate the cause of nonconformance and disposition the material. Lattice and customer specification requirements are thoroughly reviewed during MRB dispositions. The MRB consists of representatives from Manufacturing, Engineering, and Quality Assurance.

Product returned by customers (RMA) shall be analyzed and dispositioned with respect to Lattice and customer specifications.

FAILURE ANALYSIS

Failure modes discovered during qualification testing, inspections, customer returns or in-process screening are processed through Lattice's Failure Analysis group to determine the cause or relevancy of the failure and initiate corrective actions to eliminate the cause. All failure analysis reports are reviewed by Quality Assurance to convey awareness of any potential problems and assure that proper corrective action is taken.

Quality Assurance Program

Statistical Process Control Points for Commercial/Industrial Devices

<u>STEP</u>	<u>CHARACTERISTICS</u>
Oxidation	Thickness, CV Plot
Diffusion	Sheet Resistance
Photolithography	Resist Thickness, Pattern Size, Pattern Resolution
Ion Implant	Sheet Resistance
CVD	Thickness, Phosphorous Content
Metal Sputter	Thickness
Glassification	Thickness, Film Stress, Refractive Index
Etch	Etch Rates
Wafer Parametric Test	Test Structure Performance
Die Functional Test	Functional / DC Performance
Wafer Saw	Kerf Width, DI Water Resistivity
Die Attach	Visual, Epoxy Thickness, Die Shear, Cure Temperature
Wire Bond	Visual, Pull Strength, Ball Shear, Heater Block Temperature
Trim and Form	Visual, Coplanarity (PLCC only)
Mold	Visual, Plate Temperatures, Wire Sweep and Voids, Post Mold Cure Temperature
Lead Finish	Visual, Thickness, Lead (Pb) Ratio
Test	Functional / AC / DC Performance
Topside Mark	Visual
Lead Straighten	Splay, Lead Alignment (PDIP only)
Final QA Visual	Visual
Final QA Electrical	Functional / AC / DC Performance

Qualification Program

INTRODUCTION

Lattice has an intensive qualification program for examining and testing new products, processes, and vendors in order to insure the highest levels of quality. Lattice's Reliability Engineering Group is responsible for defining and implementing this qualification program.

The following table outlines the steps which must be performed before a new product, package or process is qualified. The requirements listed below are general guidelines. Detailed information on Lattice's qualification process is available to customers upon request.

Qualification Requirements

Test	# of Samples	Duration		
		New Product	New Wafer Process	New Package
125° C Operating Lifetest (5.25V)	300	1,000 Hours	2,000 Hours	2,000 Hours ¹
150° C Biased Retention Bake (5.25V)	450	1,000 Hours	2,000 Hours	2,000 Hours ¹
Endurance Cycling	75	10,000 Cycles	10,000 Cycles	N/A
ESD	48	End of Test	End of Test	N/A
Latch-Up Immunity	27	End of Test	End of Test	N/A
Temperature Cycling (-65 to 150° C)	150	1,000 Cycles	1,000 Cycles	1,000 Cycles
Biased 85/85 (5V)	225	N/A	1,000 Hours	1,000 Hours
Autoclave (121° C, 15psig)	150	N/A	336 Hours	336 Hours
Lead Integrity (DIP only)	9	N/A	N/A	End of Test
Solderability	9	N/A	N/A	End of Test
Centrifuge	75	N/A	N/A	End of Test
Bond Strength	12	N/A	N/A	End of Test

1. Required for new assembly technologies only.

5

Qualification Program

RELIABILITY MONITOR PROGRAM

The Reliability Monitor Program provides for a periodic reliability monitor of Lattice products. The program assures that all Lattice products comply on a continuing basis with established reliability and quality levels.

The Reliability Monitor Program is designed to monitor all fab and assembly facilities as well as each process technology in production. A summary of the program test and sampling plan is shown below.

Reliability Monitor Program

Test	# of Samples	Duration
125° C Operating Lifetest (7.00V)	70	160 Hours
200° C Biased Retention Bake (5.25V)	70	160 Hours
Autoclave (121° C, 15psig)	35	160 Hours

E²CMOS Testability Improves Quality

INTRODUCTION

The inherent testability of Lattice's E²CMOS PLDs significantly improves their quality and reliability. By using electrically erasable EEPROM technology to produce GAL devices, Lattice is able to perform 100% AC/DC, functional, and parametric testing of every single device. In order to achieve the highest quality levels, Lattice programs and tests each device repeatedly throughout the manufacturing process.

ACTUAL TEST VS. SIMULATED TEST

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM ALLOWS ACTUAL TEST

Each of the methods identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV EPROM devices can be erased, however the time required is 20-30 minutes (and an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 ms (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing. EEPROM technology has been used for PLD manufacturing by Lattice for more than half a decade. Lattice refers to their high performance EEPROM technology as E²CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

OTHER METHODS ARE IMPRECISE

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or require lengthy erase times severely constrain the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One need only look at the "normal" programming yield fallout of 0.5 → 3% or the "acceptable" post-programming test vector & board yield fallout of 0.5 → 2% to know that this correlation is weak. The quality systems of today are measuring defects in the parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

ACTUAL MATRIX PATTERNING

The unique capability of E²CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during Lattice's manufacturing test. Normal array cells in the programmable matrix are patterned, erased & tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E²CMOS devices. Programmability of every cell is checked dozens of times.

Historically, the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, black/white style check is not adequate to assure that the cell is programmed properly with sufficient margin to guarantee long-term reliable performance of the device. Lattice E²CMOS devices are processed through a proprietary cell verification step that consists of an analog measure (to millivolt accuracy) of the actual cell threshold. This capability is used for extensive reliability and quality measurements and testing.

WORST CASE AC/DC TESTING

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick

E²CMOS Testability Improves Quality

application of a series of worst case patterns that cover all of the permutations of input combinations, array load & switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration & test problem. Testing each additional worst case configuration takes fractions of a second, allowing multiple patterns to be checked to assure performance to rated speeds. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).■

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GAL Metastability Report

INTRODUCTION

The dictionary definition of metastability is "a situation that is characterized by a slight margin of stability." When applied to bi-stable (digital) logic, the term refers to an undesirable marginally stable output state between VIL max and VIH min.

Metastability can occur in bi-stable storage elements (registers, latches, memories, etc.) when setup and/or hold times are violated. Since setup and hold times vary with temperature and operating voltage, among other factors, the times referred to here are not the min/max numbers printed in data sheets, but rather the actual times for the given set of operating conditions. Typical applications where such times are likely to be violated include bus & memory arbiters, interfaces, synchronizers, and other state machines employing asynchronous inputs or asynchronous clocks.

Metastability manifests itself in a number of different ways. Common responses are (shown as they might be captured on a digital oscilloscope in Figure 1): runt pulse (1a), decreased output slew rate (1b), output oscillation (1c), and increased clock-to-output time (1d). By definition, the phenomenon of metastability is statistical in nature. Not only is entry into the state uncertain, but the time spent there is also variable.

Because PLDs are commonplace in today's designs, a thorough understanding of their metastable behavior is crucial. In some applications, output anomalies shorter than one clock cycle may be acceptable, but in applications where the register output is used as a control signal (clock, bus grant, chip select, etc.) for other circuitry, faults such as runt pulses and oscillation cannot be tolerated.

This report will not study the causes or characteristics of metastability in great detail; excellent material has already been prepared on this subject [1-5]. Rather, this report will introduce a mathematical model for the metastable phenomenon, discuss potential test methodologies, present and compare test results from various bipolar and CMOS PLDs, and discuss how to interpret the data. This report will close with suggestions on how to design metastable tolerant systems.

DERIVATION OF CONSTANTS

The basic premise of all metastability models is that a device's output is more likely to have settled to a valid state in time(t) than in time(t-n). In fact, the failure probability distribution follows an exponential curve. Figure 2 shows a typical failure frequency plot.

It is accepted [1] that metastable failures can be accurately modeled by the equation:

$$\log \text{Failure} = \log \text{MAX} - b(\Delta - \Delta_0) \quad (1)$$

In this equation, MAX represents the maximum failure rate for a particular environment, Δ is the time delayed before sampling the DUT (Device Under Test) output, and Δ_0 is the time at which the number of failures starts to decrease. On a failure frequency plot (such as the one in Figure 2), Δ_0 represents the knee of the curve. The constant b is rate at which the frequency of failures decreases after the knee is reached.

Recall that:

$$\log X = a \ln(X), \text{ where } a = \log(e)$$

Substituting this into (1):

$$a \cdot \ln \text{Failure} = a \cdot \ln \text{MAX} - b(\Delta - \Delta_0) \quad (2)$$

MAX is related to the clock frequency (fCLOCK) and data frequency (fDATA). That is,

$$\text{MAX} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) \quad (3)$$

Substituting (3) into (2) and applying some algebra:

$$a \cdot \ln \text{Failure} = a \cdot \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) - b(\Delta - \Delta_0)$$

$$\ln \text{Failure} - \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) = -b/a(\Delta - \Delta_0)$$

Setting $k2 = b/a$ and rearranging the equation yields:

$$\text{Failure} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA})e^{-k2(\Delta - \Delta_0)} \quad (4)$$

When used with equation (4), the constants $k1$, $k2$, and Δ_0 , completely describe a particular device's metastable characteristics; they indicate how quickly a device can resolve the metastable condition. Devices which transition out of the metastable region quickly are characterized by a small Δ_0 and a large $k2$.

The constant $k1$ is peculiar to the test apparatus (it can be thought of as a "scaling factor"). The maximum metastable failure rate (MAX) is limited by fCLOCK; a failure cannot occur if the device isn't clocked. Likewise, it is true that a metastable failure cannot occur unless data has changed. So, if $\text{fDATA} < \text{fCLOCK}$, then $\text{MAX} = \text{fDATA}$. This was the case in the test fixture Lattice used (fCLOCK=10MHZ, fDATA=2.5MHz). Substituting $\text{MAX} = \text{fDATA}$ back into equation (3) yields: $k1 = 1/\text{fCLOCK}$, so $k1 = 100\text{ns}$ for our tests.

GAL Metastability Report

TEST FIXTURE

The goal of testing a particular device's metastable characteristics is to generate real numbers for the constants k_2 and $\Delta\sigma$. To do this, the device must first be forced into the metastable state. This is done by intentionally violating setup and/or hold times. Once metastable, the output can be observed on an oscilloscope or used to increment an event counter.

Traditional Approach

One approach to characterizing a device's metastable behavior employs a test fixture similar to that shown in Figure 3a. In such a fixture, data to the device includes a "jitter band" so that the device sees changing data as it is clocked. The DUT output is fed to a window comparator to determine when

it is in the metastable region (between V_{IL} max and V_{IH} min). The comparator output can be sampled periodically and used to increment an event counter.

This method of testing, though it directly yields MTBF numbers, has some drawbacks. The first is that it does not distinguish between the different types of metastable behavior (runt pulse, oscillation, slow rise/fall time, delayed transition), and it may have difficulty detecting every type. Also, the registers used in the detector circuit itself may become metastable, which would adversely affect the results.

A New Approach

The test method used to gather data for this report used the circuit shown in Figure 3b. The tester employed an "infinite precision" variable delay circuit to control clock placement

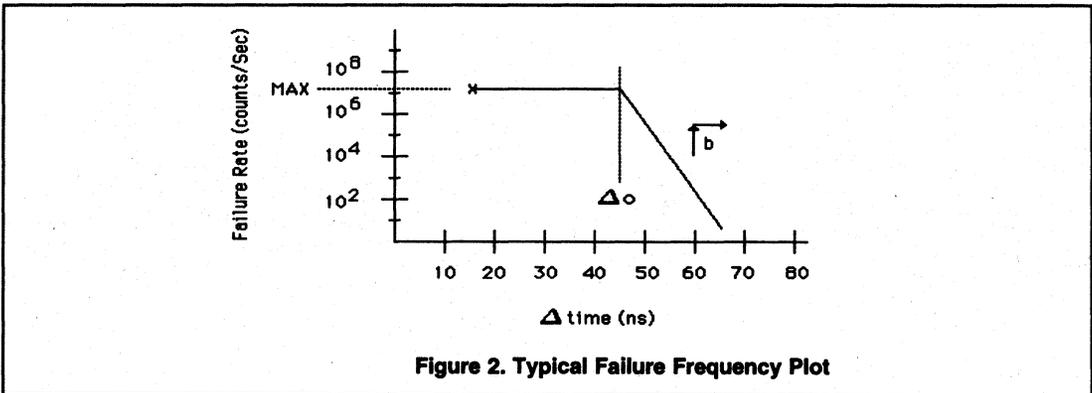
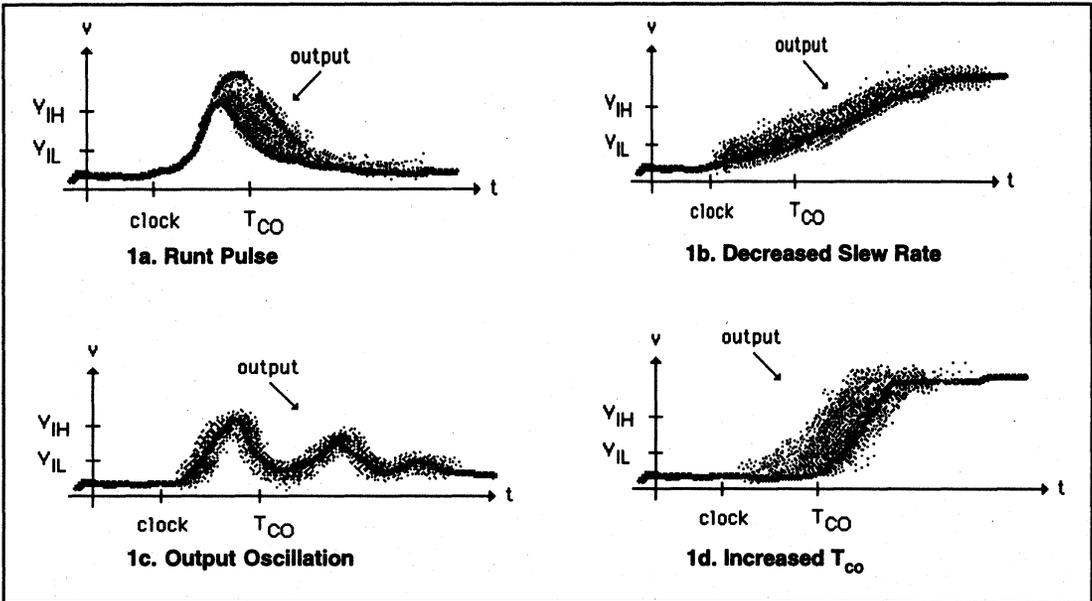


Figure 2. Typical Failure Frequency Plot

GAL Metastability Report

with respect to data. This arrangement allowed exact worst case placement of the clock, so as to induce metastability with nearly every clock pulse.

Using a digital oscilloscope (Tektronix 11403A) in point accumulate mode, metastable failures were recorded over a lengthy period of time. A hardcopy was then made and the constants empirically obtained (details below).

The oscilloscope approach, being visual in nature, enables the designer to make educated decisions regarding maximum clock and data rates, as well as the suitability of using the output to drive other circuitry. The five minute sample period used in our tests contained approximately 750 million failures. Much longer sample periods were evaluated, but they provided no perceptible gain in usable information.

A slight disadvantage of this approach is that extracting k_2 and Δ_0 values from the hardcopies is not straightforward. Because each point on the hardcopy can represent any number of actual samples (between one and 1.5 million), one cannot simply count the points at time(t) for the MTBF at that

time (although, in the case of the scattered points, the probability is low that a single isolated point represents more than one sample).

To generate values for k_2 and Δ_0 , it was necessary to refer to previous metastability studies [1]. By studying the output plots of devices with known constants, certain relationships were established. For example, it was determined that Δ_0 represents the time from the leading edge of the output until the "dot density" starts to decrease measurably. It should be noted that Δ_0 in previous studies included device propagation delays, whereas in our test it does not.

The time from Δ_0 until the dot density equals zero was defined to be the "time to metastable release" or simply time(r). The relationship between k_2 and time(r) is given below in (5), and shown graphically in Figure 4. Recall that $MAX=2.5 \times 10^6$ and $a=\log(e)$.

$$k_2 = \log(MAX) / (\text{time}(r) \cdot a) = 14.73/\text{time}(r) \quad (5)$$

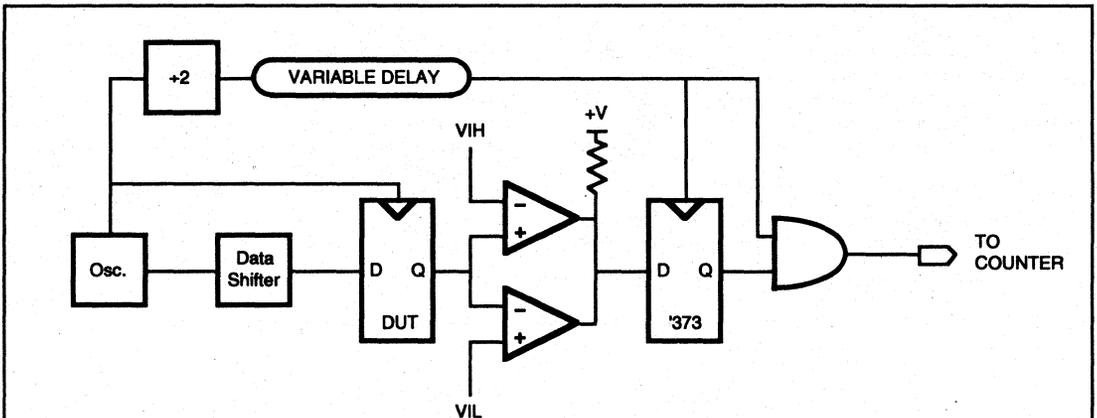


Figure 3a. Traditional Metastability Test Circuit

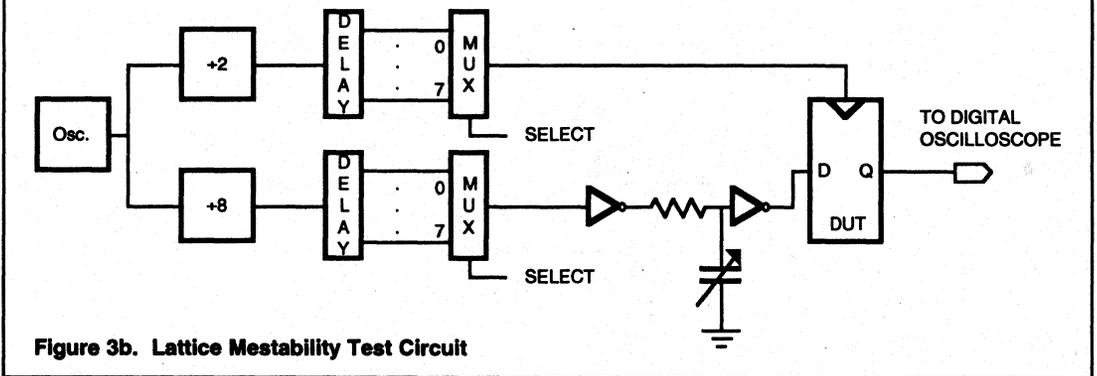


Figure 3b. Lattice Metastability Test Circuit

GAL Metastability Report

INTERPRETING THE RESULTS

In addition to examining E²CMOS GAL devices, this study also tested several bipolar PAL devices as well as other CMOS PLDs. To insure that the results of this study would be relevant, all necessary precautions were observed: the devices were of recent vintage and were acquired blindly through distributors; multiple samples of each device were tested and the results combined; all devices had either fixed 16R8 architectures or were configured to emulate the 16R8 architecture; the devices were programmed from the same JEDEC fuse map file (the source equations and the JEDEC fuse map file are presented in Listing 1).

Plots 1 through 6 on the following pages are some of the oscilloscope plots generated for this study. The top waveform in each plot is the clock signal, the middle trace is the metastable data output and the bottom trace is the histogram of the accumulated samples between 1V and 2V of the output signal. The horizontal scale is 2ns per division, so the exact clock to output time of the metastable output condition can be read directly. The vertical scale is 2V per division for the top trace, and 1V per division for the middle trace.

The middle waveform in each plot is the metastable device output which is the only signal captured in point accumulate mode. In every case, the output signal plot shows two stable levels after the transition. This is a direct result of the "indecision" caused by metastability; on some cycles the output settled to a high level, while on others it settled to a low level.

Plot 4 shows the response of a bipolar PAL 16R8-7. Notice the very well defined runt pulse (this correlates with previous data

gathered on similar devices by the manufacturer [1]). The absence of a secondary trace along ground indicates that the output always starts to transition to a high level, even when it finally settles to a low level. This characteristic makes the device unsuitable for use in control path applications (when metastability is possible). All of the bipolar parts examined showed similar results.

Plot 1, 2 and 3 are from GAL16V8B-7, GAL22V10B-10 and GAL6001-30, respectively. Aside from the fact that setup time violations may cause t_{∞} to increase by a small (but random) amount, the outputs are very clean and well behaved. The fact that there are no runt pulses or other anomalies is extremely significant, as the GAL6001 not only allows asynchronous clocking, but encourages that activity. Although GAL6001 is a much slower device as compared to GAL16V8 and GAL22V10, the similar metastable characteristics of the GAL6001 to the much faster GAL devices indicate that the inherent metastable characteristics of all the GAL devices have consistently desirable characteristics across all speed grades. Comparing Plot 1, 2 and 3 with Plot 4 and 5 shows that characteristics of the GAL devices are superior to those of bipolar PLDs. Plot 6 illustrates metastable characteristics of the TTL flip-flop (TISN74AS74).

For reference purposes, Plots 7 through 9 are included. Plot 7 shows a normal (ie. non-metastable) GAL16V8B-7 transition, and Plot 8 a normal PAL16R8-7 transition. Plot 9 is the normal transition of the TTL flip-flop (TI SN74AS74). For consistency, only rising edges have been shown. Our tests also covered falling edges which, in general, were interesting but did not provide any additional information.

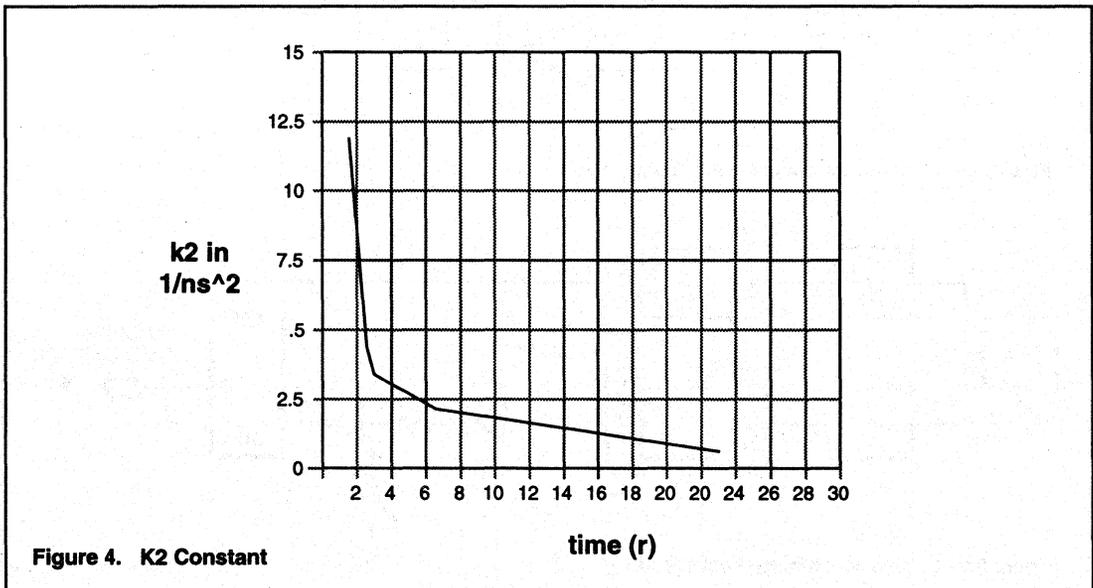


Figure 4. K2 Constant

For a more quantitative look at the phenomenon of metastability, refer to the table beneath each plot. These tables list the measured values of the constants Δ_0 and k_2 for the device whose plot is shown, and for similar devices. Recall that large k_2 and small Δ_0 values are desirable. The numbers in the tables correlate closely with the results of earlier tests [1,5], confirming the validity of our test method.

Since all current GAL devices possess very similar register and output buffer circuitry, and all are fabricated using the same basic process, the data shown in Table 1 for the GAL16V8 is considered applicable to all devices and speed grades in the GAL family.

USING THE RESULTS

If a register enters the metastable state in a system, then data was obviously unstable as the register was being clocked. The argument over which data should have been captured (old or new) is academic as the register will randomly pick one or the other. Signals in most asynchronous systems are active for more than one clock cycle, so if they are missed initially, they could be captured on a subsequent clock cycle.

It is the task of the state machine designer to take adequate precautions against metastability causing illegal states to be entered. One way to do this is by using "gray codes" when ordering states. Gray code state equations allow only one state bit to change during a state transition. Thus, the worst metastability could do would be to delay a state transition by one clock cycle. If more than one bit were allowed to change, the outcome would be purely random, and probably illegal. Figure 5 shows examples of both cases.

Other solutions are to externally (or internally) synchronize the asynchronous signals, or to increase cycle times to allow time for metastable outputs to settle. An example of the latter solution is given below.

It is worth noting at this point that state machines (synchronous or asynchronous) can fail for reasons other than metastability. A not insignificant component of a PLD's specified setup time is directly attributable to internal data skewing [2]. Data skewing is the inevitable result of differing signal path lengths, loading conditions, and gate delays. Stated another way, each input to output path has its own set of actual AC specifications. If insufficient setup time has passed, different "versions" of the same data may be present at the inputs of different registers as they are clocked. A good example of this is:

```
Output_Pin19 := Input_Pin2;  
Output_Pin15 := !Input_Pin2;
```

If clocked at precisely the right moment after an input transition, one register will capture old data while the other captures new data, resulting in a system failure. This condi-

tion, though also the result of a setup time violation, should not be confused with metastability (the "incorrect" data that is captured has normal output characteristics); it is, pure and simply, the result of a violation of specifications.

Example

To determine the maximum clock rate (given an acceptable error rate) that a particular device will allow in an asynchronous environment, equation (4) is used. For example, the system shown in Figure 6 utilizes a 9600 baud (bits/sec) asynchronous data stream. The system clock period is $t_{CO} + t_{PD} + t_{SU} + \Delta$. For one failure per year:

$$3.2 \times 10^{-8} = [(1 \times 10^{-7}) / (\Delta + 22)] (9600) e^{-4(\Delta - 44)}$$

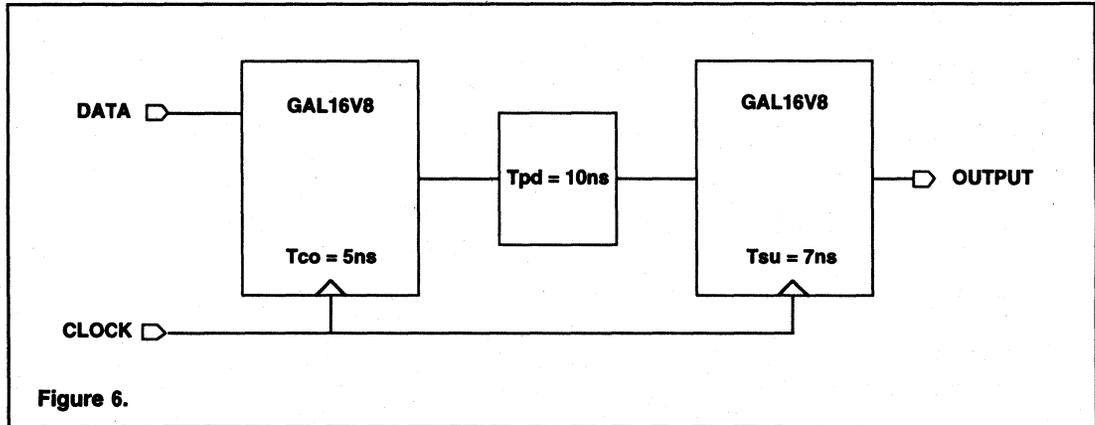
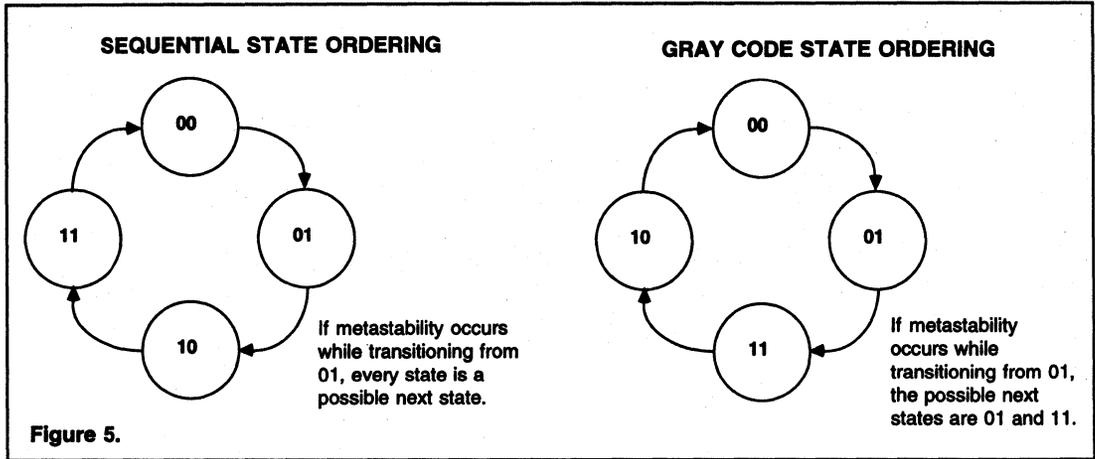
Solving for Δ yields $\Delta = 2.22$ ns, or about 2 ns, for a cycle time of 24 ns. Referring back to Plot 1, the additional delay of 2 ns intuitively makes sense. Remember, in terms of setup and hold time violations, the oscilloscope plots were made under worst case failure conditions; the scattered dots could represent MTBFs of days, years, or even millenniums in a typical asynchronous environment.

Due to the extremely quick metastable settling times of GAL devices, a relatively small increase in the cycle time will produce a dramatic improvement in reliability.

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3. K.Nootbaar (Applied Microcircuits Corp.), "Design, Testing, and Application of a Metastable Hardened Flip-Flop," *ibid.*, pp 16/2 1-9.
4. J.Birkner (MMI), "Understanding Metastability," *ibid.*, pp 16/3 1-3.
5. R.K.Breuninger, K.Frank, "Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families," application note SDAA004, Texas Instruments, 1985.

GAL Metastability Report



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MODULE metastable

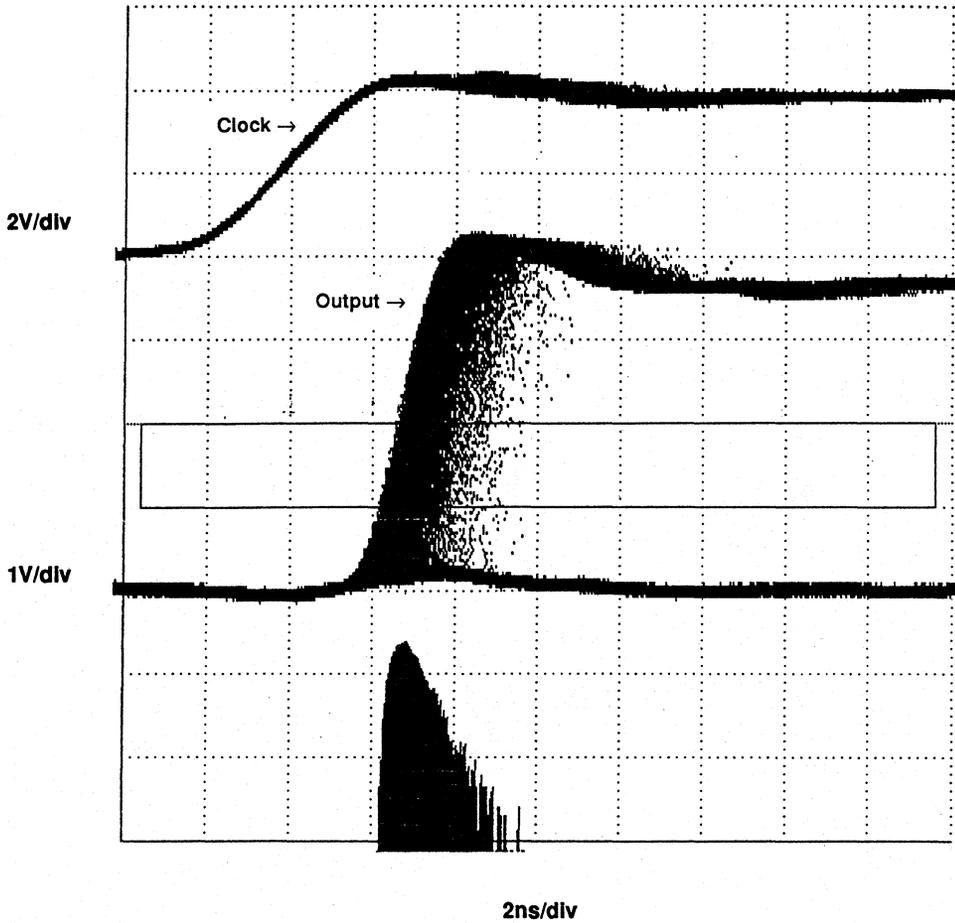
TITLE 'Metastable Test
Pattern'

uOO Device 'P16R8';

d    PIN 2;
q1,q2 PIN 12,19;
    EQUATIONS
q1 := d;
q2 := d;
    End metastable

JEDEC file for: P16R8
Metastability Test Pattern*
QP20* QF2048* F0*
L0000 10111111111111111111111111111111*
L1792 10111111111111111111111111111111*
C07F4*
    
```

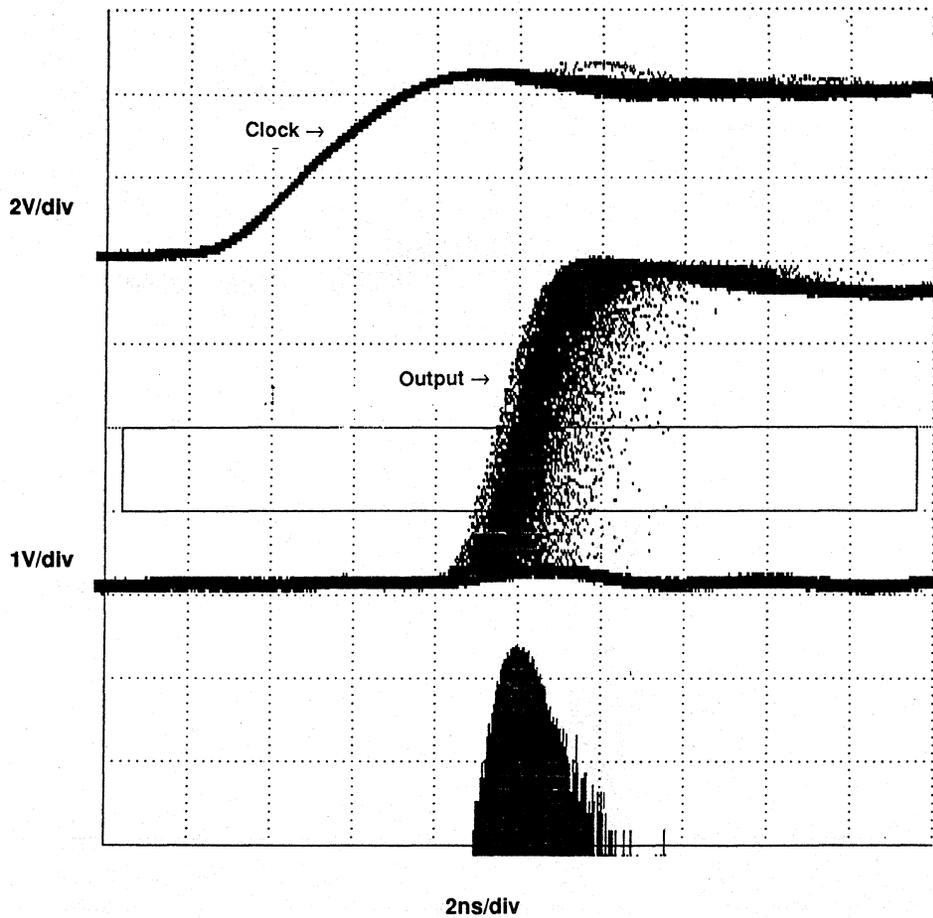
Listing 1a. Source equations **Listing 1b. JEDEC file**



Plot 1. GAL16V8B-7 Metastable Output

Part #	Manufacturer	Δo (ns)	$k2$ (1/ns ²)
GAL16V8B-7	Lattice	.44	5.0

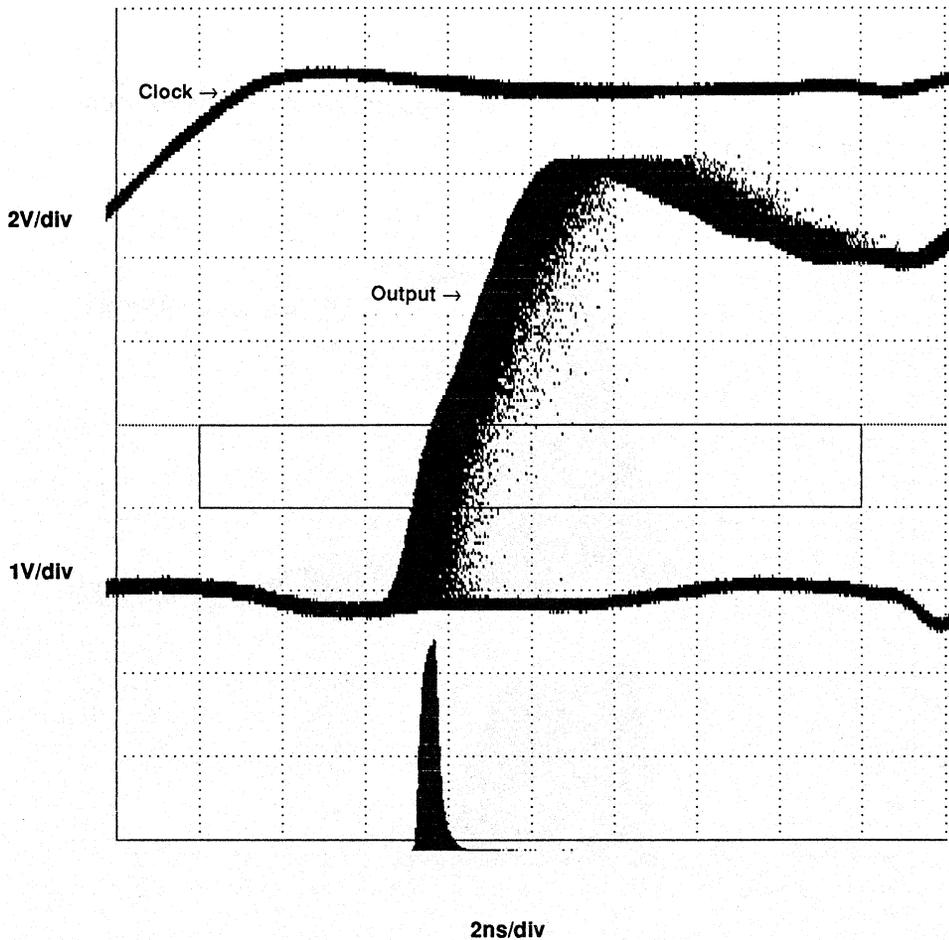
GAL Metastability Report



Plot 2. GAL22V10B-10 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 (1/ns ²)
GAL22V10B-10	Lattice	.51	5.2

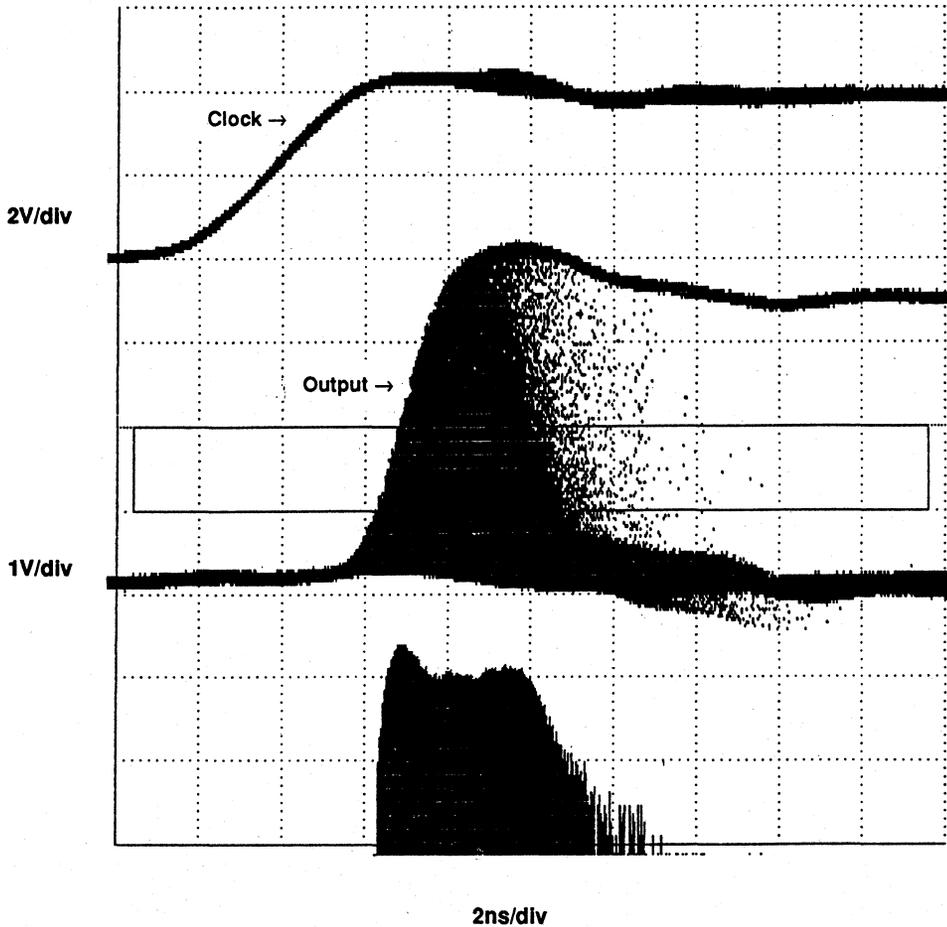
GAL Metastability Report



Plot 3. GAL6001-30 Metastable Output

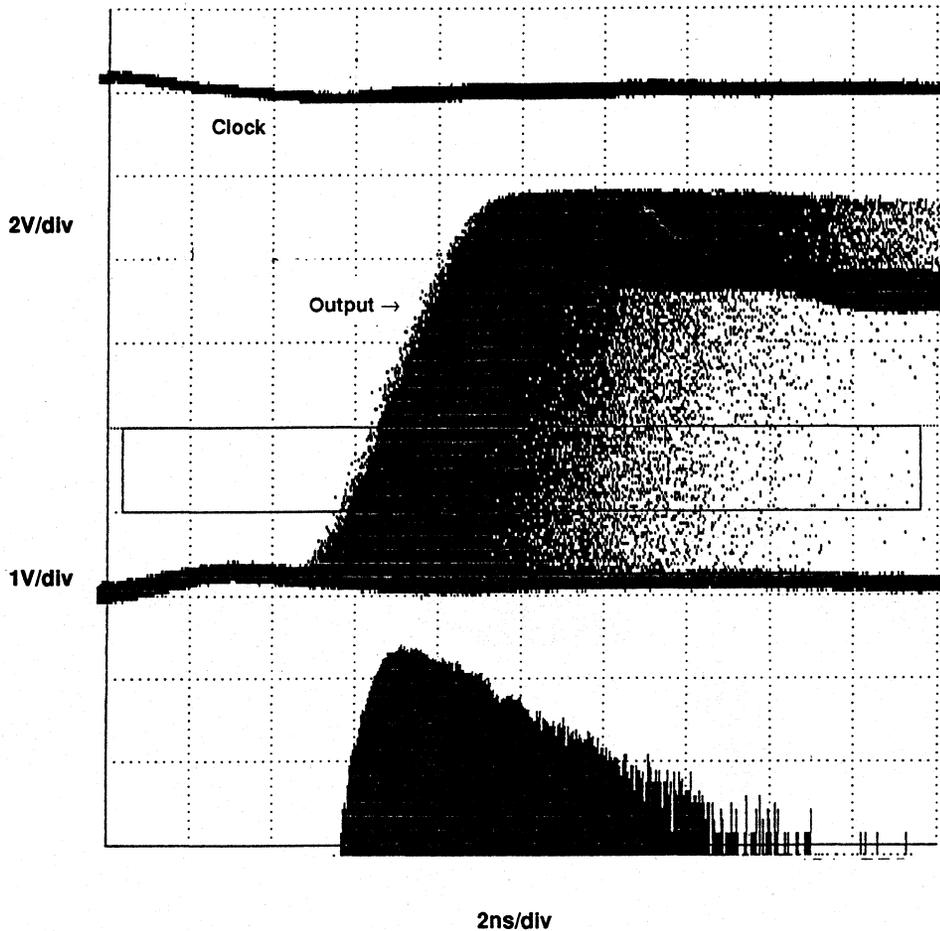
Part #	Manufacturer	Δo (ns)	$k2$ (1/ns ²)
GAL6001-30	Lattice	.22	7.3

GAL Metastability Report



Plot 4. PAL16R8-7 Metastable Output

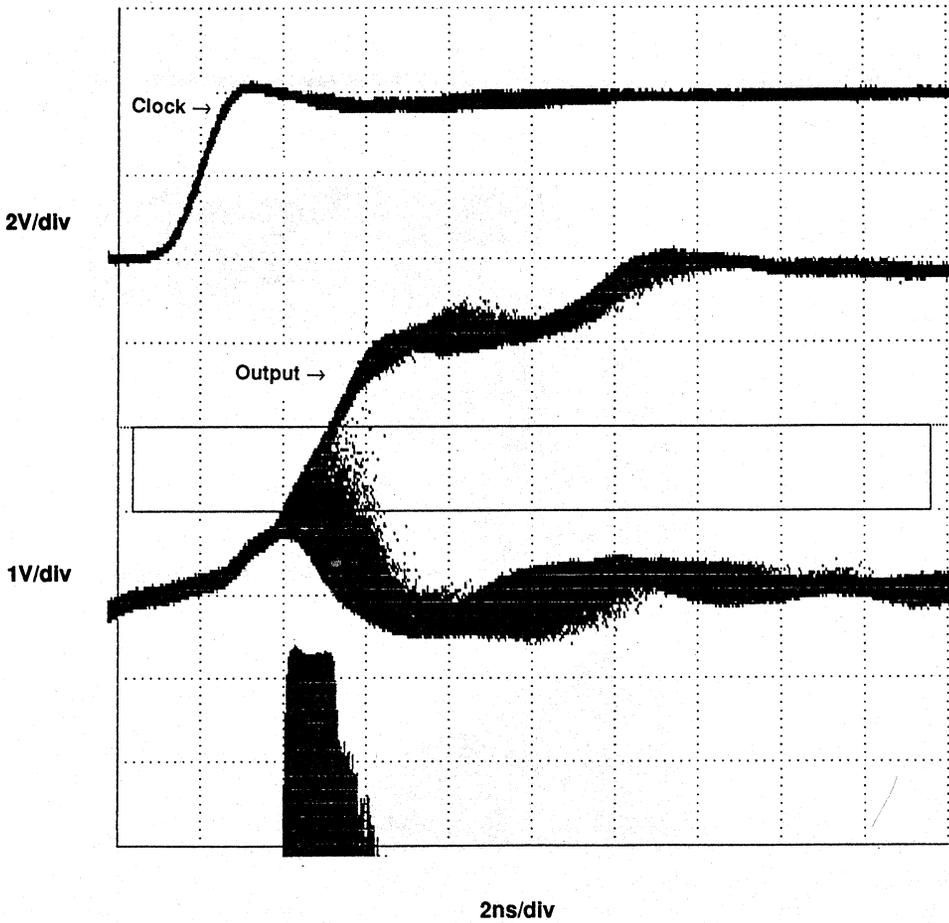
Part #	Manufacturer	Δo (ns)	$k2$ (1/ns ²)
PAL16R8-7	AMD	1.2	2.5



Plot 5. TIBPAL16R6-7 Metastable Output

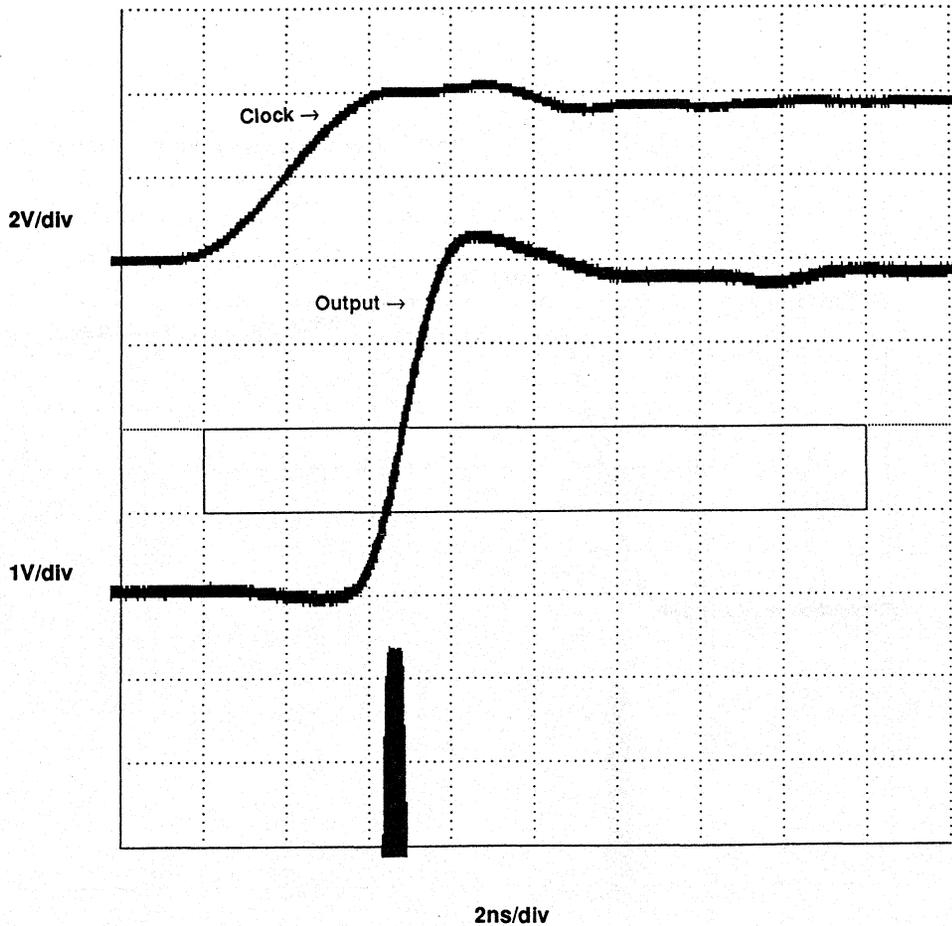
Part #	Manufacturer	Δo (ns)	$k2$ (1/ns ²)
TIBPAL16R6-7	TI	1.5	1.5

GAL Metastability Report



Plot 6. SN74AS74 Metastable Output

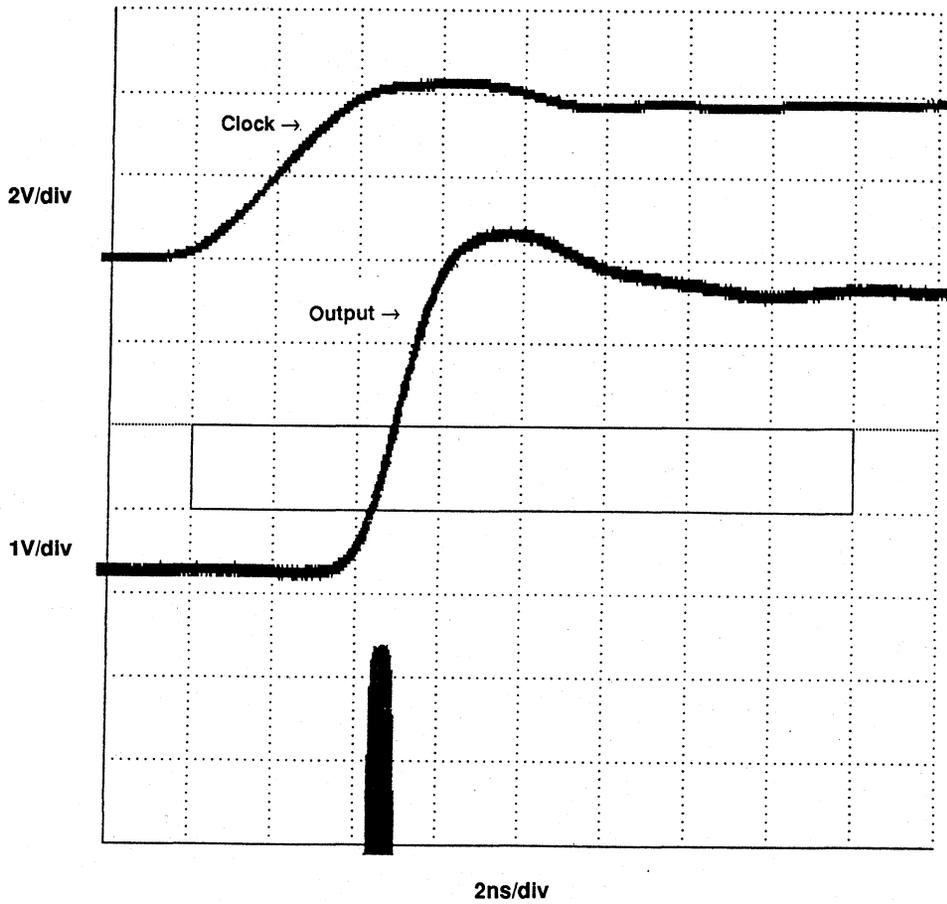
Part #	Manufacturer	Δo (ns)	$k2$ (1/ns ²)
SN74AS74	TI	.91	3.5



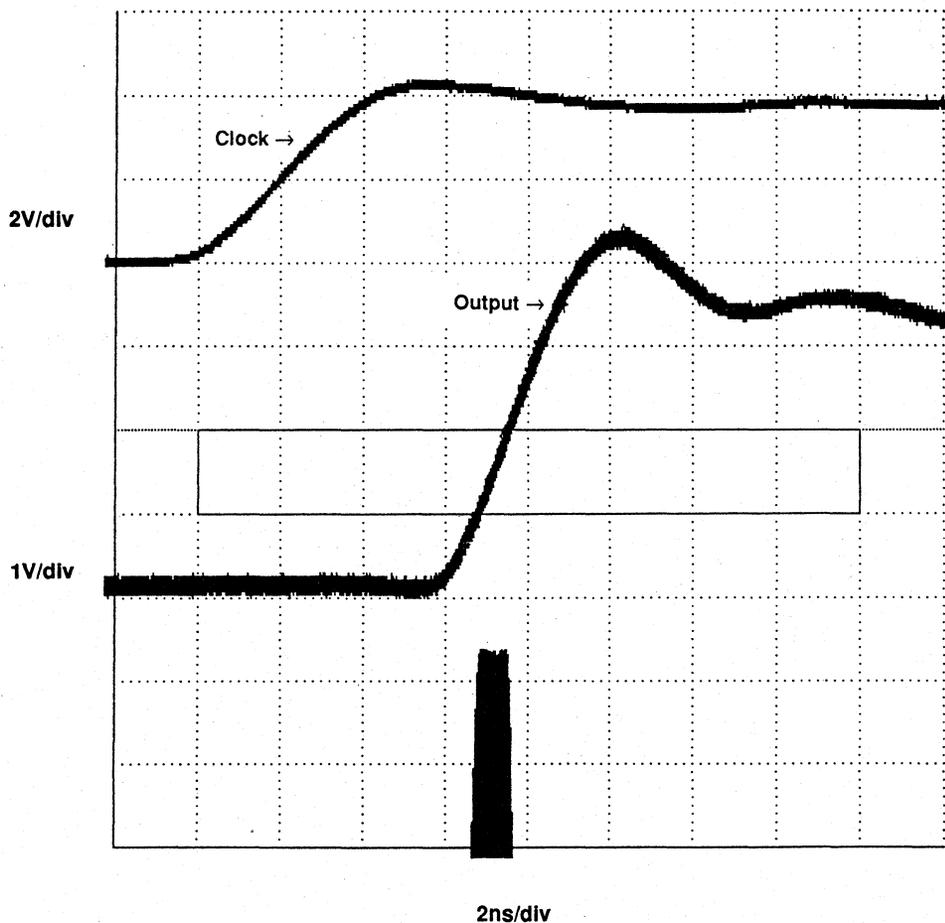
6

Plot 7. Normal GAL16V8B-7 Transition

GAL Metastability Report



Plot 8. Normal PAL16R8-7 Transition



6

Plot 9. Normal SN74AS74 Transition

END

Notes

Latch-up Protection

INTRODUCTION

The Lattice GAL family has been developed using a high-performance E²CMOS process. CMOS processing was chosen for the GAL family to provide maximum AC performance with minimal power consumption. A drawback common to all CMOS technologies is the destructive agent, latch-up.

This brief defines the phenomenon of latch-up, how it manifests itself, and what techniques have been used to control it. Also described are three device features employed in the GAL family to eliminate the occurrence of latch-up as well as the results of an intensive investigation conducted to reveal the GAL family's tolerance to latch-up.

Latch-up is destructive bipolar device action that can potentially occur in any CMOS processed device. It is characterized by extreme runaway supply current and consequential smoking plastic packages. Latch-up is peculiar to CMOS technology, which integrates both P and N channel transistors on one chip.

In the doping profile of a CMOS inverter, parasitic bipolar (PNPN) silicon-controlled-rectifier (SCR) structures are formed. Figure 1 shows the process cross section of a CMOS inverter, as well as the bipolar components to the parasitic SCR structure. In steady-state conditions, the SCR structure remains off. Destruction results when stray current injects in to the base of either Q₁ or Q₂ in Figure 1. The current is amplified with regenerative feedback

(assuming that the beta product of Q₁ and Q₂ is greater than unity), driving both Q₁ and Q₂ into saturation and effectively turning on the SCR structure between the device supply and ground. With the parasitic SCR on, the CMOS inverter quickly becomes a nonrecoverable short circuit; metal trace lines melt and the device becomes permanently damaged.

CAUSES OF LATCH-UP

It has been explained that parasitic bipolar SCR structures are inherent in CMOS processing. If triggered, the SCR forms a very low-impedance path from the device supply to the substrate, resulting in the destructive event. Two conditions are necessary for the SCR to turn on: The beta product of Q₁ and Q₂ must be greater than unity, which, although minimized, is usually the case; and a trigger current must be present. The cause of latch-up is best understood by examining the mechanisms that produce the initial injection current to trigger the SCR network. Figure 2 is a schematic of the parasitic bipolar network present in a CMOS inverter, where node "b" is the inverter output. It can be seen that two events might trigger latch-up: 1) the inverter output could overshoot the device supply, thereby turning on Q₃ and injecting current directly into the base of Q₂; and 2) the inverter output could undershoot the device ground, turning on Q₂ immediately. However, a third condition could also trigger latch-up; if the supply voltage to the P+ diffusion were to rise more quickly than the N-well bias, Q₁ could turn on. Within the device circuitry, overshoot and undershoot can be controlled by design. A problem area exists at the device

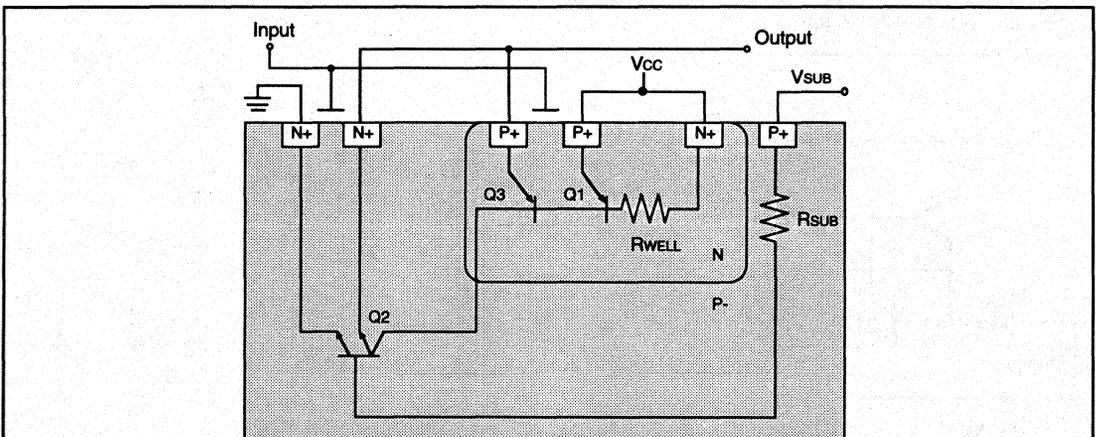


Figure 1. CMOS Inverter Cross-Section

Latch-up Protection

inputs, outputs and I/Os because external conditions are not always perfect. Powering up can also be a potential problem because of unknown bias conditions that may arise.

With CMOS processing the possibility of latch-up is always present. The major causes of latch-up are understood and it is clear that if CMOS is to be used, solutions to latch-up will have to be created. As the technology evolves, solutions to latch-up are becoming more creative. Two of the more straightforward solutions are presented here.

One direct way to reduce the threat of latch-up is to inhibit Q_2 (Figure 1) from turning on. This has been accomplished by grounding the substrate and reducing the magnitude of R_{sub} through the use of wafers with a highly conductive epitaxial layer. While the technique is successful, the wafers are more expensive to manufacture, due to the extra processing required to form the epitaxial layers.

The extensive use of "guard rings" helps to collect stray currents which may inadvertently trigger an SCR structure. A disadvantage to heavy use of guard rings is the constraints placed on circuit design and topological layout, and the resulting increase in die size and cost.

THE LATCH-LOCK APPROACH

The intent of the GAL family was to implement cost-effective solutions to each major cause of latch-up. The goal was met through three device features.

The most susceptible areas for latch-up are the device inputs, outputs and I/Os. Extreme externally applied voltages may cause a P+N junction to forward-bias, leading to latch-up. The inputs, by design, are safe; but outputs and I/Os present a danger.

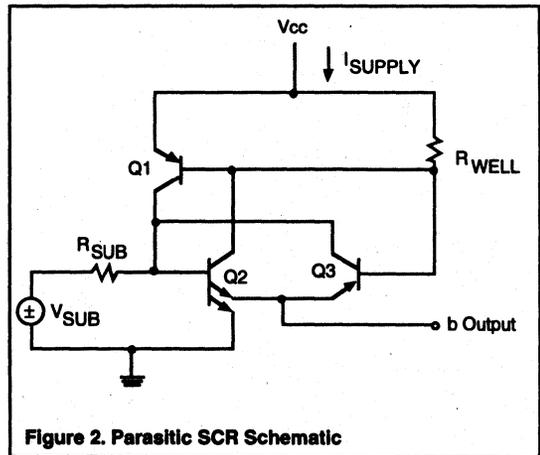


Figure 2. Parasitic SCR Schematic

To prevent latch-up by large positive swings on the device outputs or I/O pins, NMOS output drivers were used. This eliminates the possibility of turning on Q_2 (Figure 2) with an output bias in excess of the device supply voltage. Figure 3 contains the effective NMOS output driver and its switching characteristics. Note that the output does not fully reach the supply voltage, but still provides adequate V_{OH} margin for TTL compatibility.

To prevent negative swings on device output and I/O pins from forward-biasing the base-emitter junction of Q_2 , a substrate-bias generator was employed. By producing a V_{sub} of approximately -2.5v, undershoot margin is increased to about -3V.

To insure that no undesired bias conditions occur with P+ diffusions, Lattice Semiconductor has developed proprietary Latch-Lock power-up circuitry, illustrated in Figure 4. In short, the drain of all P channel devices normally connected to the device supply is now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

To determine the amount of latch-up immunity achieved with the three device features utilized in the GAL family, an intensive investigation was carried out. Each step was

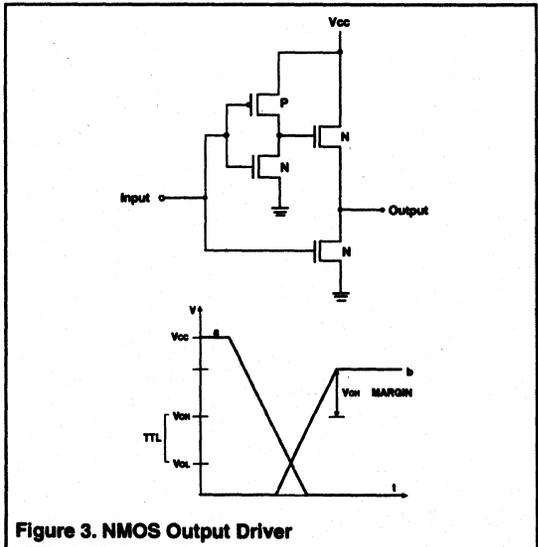


Figure 3. NMOS Output Driver

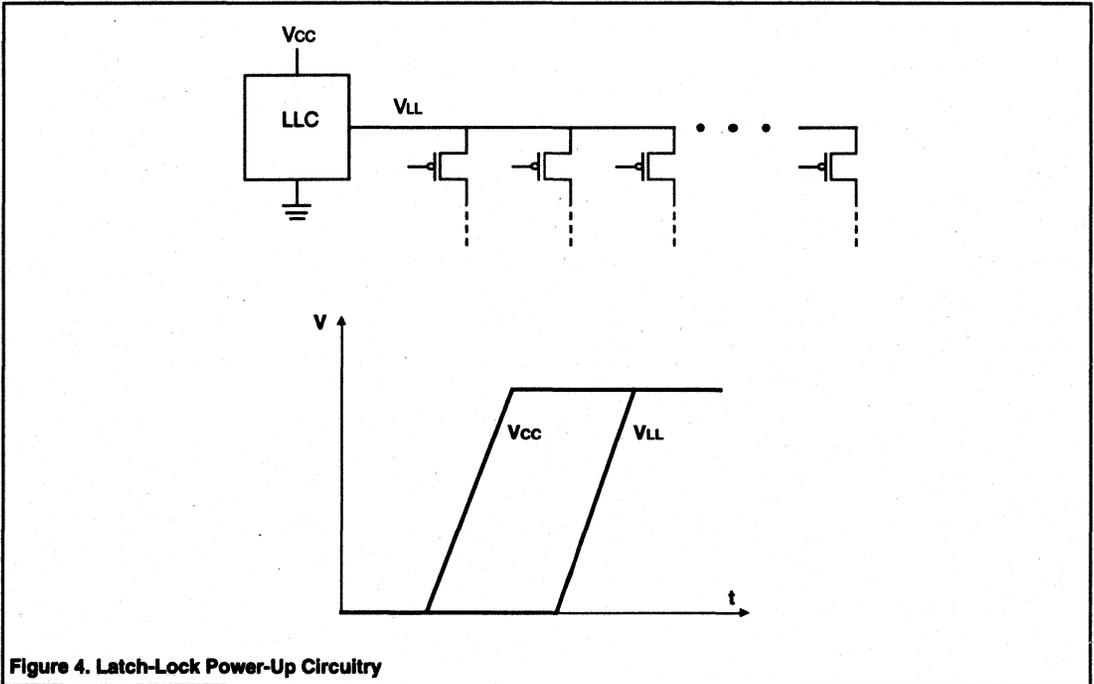
Latch-up Protection

conducted at 25° and 100°C; inputs, outputs, and I/Os were sequentially forced to -8V and +12V while the device underwent fast and slow power-ups; devices were repeatedly "hot socket" switched with up to 7.0V.

Even under the extreme conditions specified, no instance of latch-up occurred. In an attempt to provoke latch-up, $\pm 50\text{mA}$ was forced into each output and I/O pin. The device

output drivers were damaged in the battle, and still latch-up was not induced.

Based on the data, it is evident that the GAL family is completely immune to latch-up, even when subjected to a wide variety of extreme conditions, including current at inputs, outputs, and I/Os, power-supply rise time, hot-socket power-up and temperature. ■



6

Notes

Hidden Costs in PLD Usage

While the purchase price of a programmable logic device is an important consideration in identifying the most cost-effective solution for a system design, it is clearly not the only criterion. Hidden costs attributable to product testing, yield fallout, inventory management, and other factors can dramatically impact the final cost of using a PLD.

This brief investigates the overhead associated with PLD usage and the advantages of testable and reprogrammable E²C MOS GAL devices over one-time-programmable PLDs.

The GAL family of programmable logic devices is manufactured on a state-of-the-art E²C MOS process that not only provides a better speed-power product than the best bipolar devices, but offers an advantage unique among PLD manufacturers: guaranteed programming and post-programming yields of 100%.

The 100%-yield guarantee is the culmination of years of Lattice Semiconductor's circuit-design and manufacturing experience applied to the GAL device. The only way to be able to make this 100% yield statement—and to supply product that actually meets the 100% criterion—is to fully test all functions of the device, prior to shipment.

The electrically erasable (EE) matrix, unlike previous PLD matrix technologies (bipolar fuse-link and UV-erasable PROM), permits full testing of the programmability and reprogrammability of each and every matrix cell. The ability to pattern the actual matrix is extremely significant, since it also allows Lattice to test the functionality of each of the Macrocell logic blocks, under various worst-case configurations. This test approach is referred to at Lattice as 'Actual Test'. Unlike other PLD manufacturers' approaches, which include imprecise correlations, simulations, test rows, and phantom arrays, Actual Test conclusively verifies AC and DC performance of every cell in every GAL device.

ELIMINATES INCOMING QA

A consequence of Actual Test is that GAL devices do not require the typical incoming Quality Assurance testing that traditional fuse-link bipolar PLDs require. As such, the cost savings of using GAL devices begins the moment the parts arrive, since the average cost of an incoming QA operation—hardware, software development and maintenance, and handling—is approximately 7% of the raw device cost. Moreover, GAL devices become the optimal choice for implementation of Just-In-Time or Dock-To-Stock programs, since they eliminate the expense and time required by the incoming inspection process.

Still, a number of users require that all devices undergo incoming QA. In those cases, the use of GAL devices still simplifies the issue. A single generic test program can be used to test all configurations of the E²C MOS-based GAL device. The expense of generating and maintaining a test program for every architecture (16L8, 16R4, 10P8, and so on) is eliminated with Generic Array Logic.

Since the QA test for fuse-link PLDs, by its nature, requires the destructive patterning of the fuse array, QA testing of bipolar PAL devices can only be done through a sample plan. At best, a sample plan can provide a crude estimate of fuse-link yield loss; moreover, sampled devices cannot be erased and must be subsequently thrown away. GAL devices, utilizing the E²C MOS process can be patterned and erased at will, allowing 100% QA of all specifications and configurations. And, the devices can, of course, be erased to allow full reuse of the sample units in manufacturing.

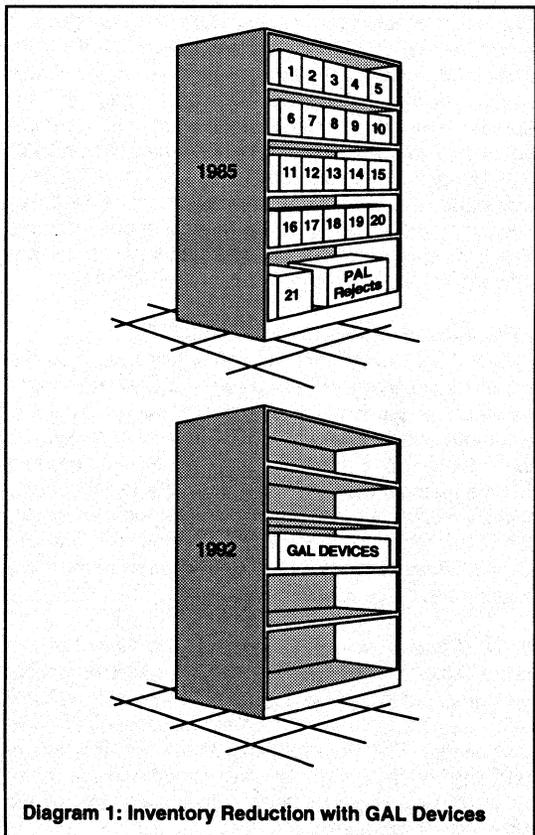


Diagram 1: Inventory Reduction with GAL Devices

Hidden Costs in PLD Usage

SIMPLIFIED INVENTORY MANAGEMENT

The generic architecture and high performance of the GAL devices allow two basic devices—the 20-pin GAL16V8 and 24-pin GAL20V8—to directly replace approximately 70% of PLD device types currently available, including 100% of the most popular types ('L8,' 'R8,' 'R6,' and 'R4') and a sizable portion of the FPLA and EPLD devices. The obvious benefit of using GAL devices is a substantial reduction in the number of part types that need be stocked (Figure 1).

Inventory management of dozens of speed-power options and device architectures is a painful process. The ideal cost of managing a device inventory adds some 2% of direct overhead; the real cost can be significantly greater, due to the risk that a shortage, 'outage,' or obsolete stock condition will exist. Improper planning could result in a shut-down of the assembly line. The generic architecture allows the GAL device to serve as insurance whenever needed to meet an immediate shortfall. The yields, at 100%, allow full planning confidence that the problem is solved.

Disposition of rejects is another inventory-management issue. The raw cost of the rejects themselves (at a 2% to 5% fallout rate) is compounded by the associated paperwork of obtaining a replacement or credit for the bad devices. Studies show that every time a buyer or purchasing agent picks up the phone or generates a debit memo, some \$30 to \$50 is spent. Follow-up activity—2 or 3 calls or letters—compounds the expense. Meanwhile, the manufacturing inventory is short of devices. What's more, carrying additional 'safety-stock' as insurance against a temporary shortage results in a higher inventory-carrying cost.

100% YIELDS REDUCE SYSTEM COST

Perfect yields, as provided through Actual Test, allow the manufacturing environment to run in a fully predictable manner. This allows purchasing and production control to accurately schedule all activities and product for system build. Just-In-Time material-requisition systems assume that the material will arrive on time, in the exact quantity necessary. With GAL devices, the source product inventory can be allocated for programming to various patterns with full confidence that the final patterned devices will be in the quantity and of the quality desired.

A rule of thumb, commonly known as the 'Factor of Ten Rule' (Table 1), details the cost of a failing unit throughout the manufacturing process. The point is that unit cost is not nearly as important as its contribution to subsequent costs (or savings). The Rule basically states that the cost of detecting and replacing a defective device increases by an order of magnitude for each subsequent step of the manufacturing process.

COST*	MULTIPLIER	OPERATION
\$ 5.00	X	Raw Cost of Device
\$ 50.00	10X	Cost of Detecting and Repairing a Board Failure
\$ 500.00	100X	Cost of Detecting and Repairing a System Failure
\$ 5,000.00+	1,000X	Cost of Repairing a Field Failure

Each successive operation results in 10 times the cost to detect the failing device. \$5.00 device cost assumed — use your actual cost and a 10x multiplier to obtain actual numbers.

Table 1: Factor of Ten Rule

It is extremely important to recognize that the additional difficulty and cost of using traditional PLDs has implications far beyond what the observed programming yield fallout portends. The hidden costs, time and expense aggravation of board failures (10x device cost to detect and repair), system failures (100x device cost), and the potential for field failures far outweigh the simple 2% to 5% yield losses observed on a programming fixture.

Figure 2 illustrates the differences between traditional PAL device yield loss and the 100% yields of the GAL devices. Notice that even operator errors and engineering pattern revisions are recoverable with GAL devices, which can be instantly erased and reprogrammed to the proper architecture and logic pattern.

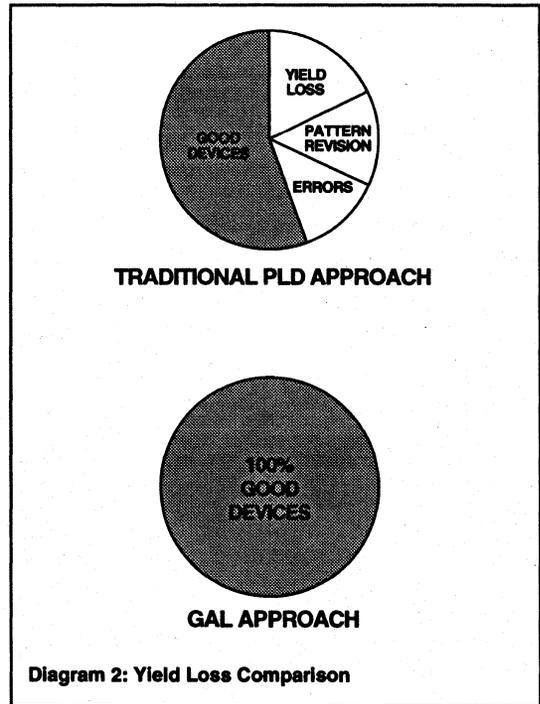


Diagram 2: Yield Loss Comparison

Hidden Costs in PLD Usage

In a typical manufacturing environment, device programming hardware patterns the array, and assuming the engineer has provided test vectors, the hardware performs a basic (slow) functional test of the device. Yield losses at these two operations average 2% to 5% and 1% to 2%, respectively.

What is not tested adequately at the PAL programming operation is the effect of partially programmed fuses that result in degraded AC performance or marginal reliability of the device. These failures are caught at board test and/or after board burn-in. Typical bipolar functional and AC parametric failure rates range between 0.5% and 2% for all manufacturers of fuse-link PAL devices. Even if one assumes the minimum failure rate of 0.5%, the system failure rates are still greatly magnified.

Two mechanisms are used to detect the failures of PAL devices: board test and system test. Using the 'Factor of Ten Rule' and assuming that board test fully screens bad devices (AC fallout), if a conservative device failure rate of 0.5% were observed, the actual parts cost would be:

$$\begin{aligned} \text{Acost} &= \text{Pcost} + (\text{Pcost} * 10 * 0.5\%) \\ &= \text{Pcost} + \text{Pcost} * 0.05 \\ &= 1.05 * \text{Pcost} \end{aligned}$$

Performing the screening at the system level, under the same scenario, makes a dramatic difference in the cost of the device:

$$\begin{aligned} \text{Acost} &= \text{Pcost} + (\text{Pcost} * 100 * 0.5\%) \\ &= \text{Pcost} + \text{Pcost} * 0.5 \\ &= 1.5 * \text{Pcost} \end{aligned}$$

These two different cost factors were determined using the

conservative failure rate of 0.5%. Using the GAL device, with its 0% failure rate, provides instead a cost factor of 1; i.e., no additional cost burden is generated.

The problem caused by PLD failures obviously grows in proportion to the number of devices in a system, since the probability of a failure among a group of PAL devices is higher than that for a single device. Figure 3 plots the probability of a board or system not working, as a function of the number of devices per system, for a variety of device failure rates.

For example, at a unit failure rate of 1.0%, a system incorporating 30 PAL devices will exhibit a 25% failure rate. That means that 1 out of every 4 systems will have to be reworked, at tremendous cost. The replacement of an average 0.5% of the units in a system results in an actual 8% added to the hidden device cost.

The difficulty in replacing board failures is compounded by the removal of soldered units. It is quite easy to destroy a board with the removal and replacement of a defective device.

Systems that fail in the field are not only the most costly in terms of dollars and cents, but in customer relations, as well. They require responding rapidly and performing repairs in a less-than-ideal environment, without the complete tools and supplies available at the factory. Field failures will always occur to some degree. However, the use of GAL devices can help reduce field repair costs when they do occur—even if the failing device is a traditional bipolar PLD—since the generic, erasable nature of GAL devices allows a minimum of field inventory to be carried, to debug system failure problems caused by other devices. The panel on the next page provides guidelines for calculating PLD usage costs.

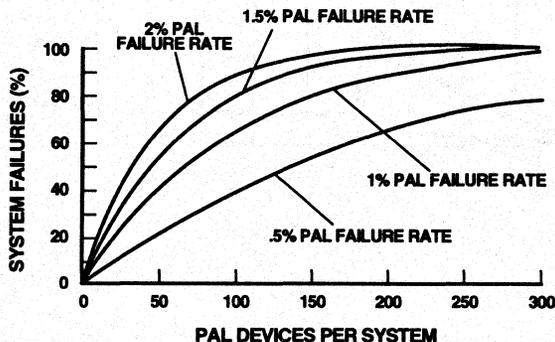


Diagram 3: Probability of System Failures Using Bipolar PLDs

Hidden Costs in PLD Usage

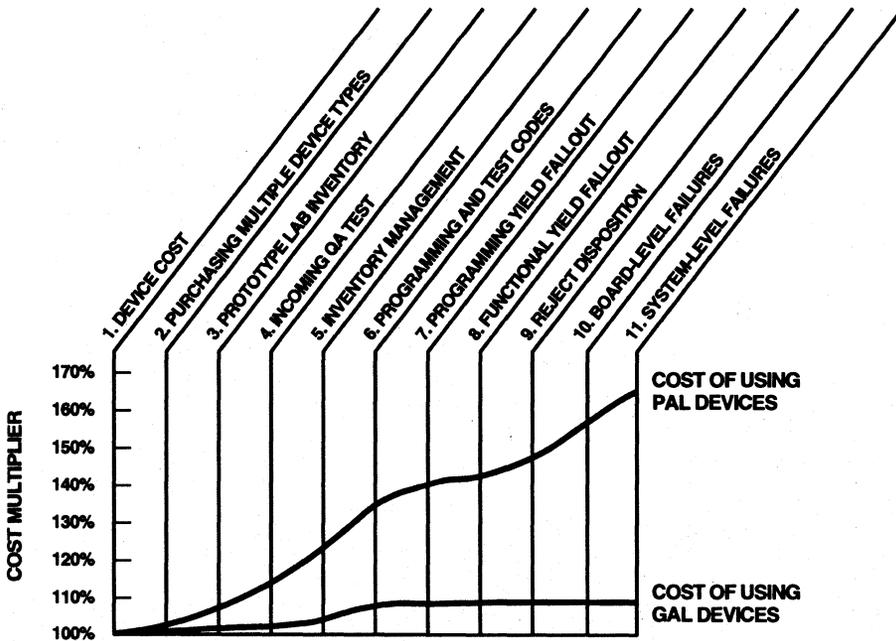
PLD Cost Analysis

The cost of using a PLD goes well beyond simply the raw device cost. Programming and vector-test yields are obvious contributors to higher unit cost. The less-obvious and hidden costs tend to be much more difficult to identify and quantify.

The purpose of the costing example is to provide the basis for your own cost analysis, using your own overhead and yield numbers. Estimates for reasonable ranges of the cost contributors are shown as a guide to using your own numbers.

The explanation for each of the contributors to the device cost multiplier follow the figure. These cost multipliers include the overhead for each operation, and as a result, are higher than the observed costs.

The example shown is based on actual data from a 100,000-piece-per-year user of traditional bipolar PLDs. The environment is a typical, high-volume, quality-controlled one. The GAL device checks in at 1.09 times the normalized cost, while the actual cost of using the bipolar PLD is 1.66 times—almost 40% higher.



Hidden Costs in PLD Usage

1 **Device Cost** is normalized to unity so that the raw purchase price has no bearing on the other cost factors.

2 **Purchasing Multiple Device Types** instead of the single GAL device adds to overhead in the purchasing and receiving departments. This contributes approximately 2% as the availability, quality, and quantity issues are resolved with each order. The GAL approach reduces this number to 1.25% with inventory simplification.

3 **Prototype Lab Inventory** and usage typically adds 5% to maintain experimentation stock of multiple device types for board debug. The GAL device multiplier is 1%, since the device can be reused over and over again.

4 **Incoming QA Test** and programs cost more than may be immediately apparent, with a 7% adder. The generation and maintenance of the software and hardware for the dozens of bipolar devices is considerably more expensive than the single GAL device software required. No sample-program waste is induced. Only the aspects of handling are required for GAL devices, resulting in a reduction to 1% (or 0%, if you eliminate the incoming QA operation entirely).

5 **Inventory Management** includes shelf space, safety stock, depreciation, obsolete stock write-off and personnel to maintain adequate control of the units. A typical overhead is 10%. The simplified GAL operation involves no safety or obsolete stock and a minimum of device types, adding a maximum 2% to 3% to overhead.

6 **Programming and Test** includes all handling and hardware expenses. Inventory issuance, counting and returns, handling during the program/test operation, labels, and paperwork contribute to a 12% multiplier. The 100% yielding, generic GAL approach reduces the problem to 4%.

7 **Programming Yield Fallout** is directly observed as bad units. A typical bipolar range is 1% to 4%. GAL devices have 0% yield fallout—guaranteed.

8 **Functional Yield Fallout** is detected by the device programmer immediately after programming, through the use of test vectors, and can average 1% to 3%. GAL devices guarantee 0% functional fallout. It should be noted that using test vectors does not screen out inadequate for AC performance, which will be manifested as a board failure.

9 **Reject Disposition** overhead runs 5% to obtain replacements and credits for fuse-link devices. Zero rejects with GAL devices eliminates costs associated with reject disposition. Notice that the cumulative multiplier for only the program/test/reject of fuse-link devices is 1.10, compared with GAL devices' 1.00 multiplier.

10 **Board-Level Failures** are typically where AC failures are detected. The 'Factor of Ten Rule' exacerbates the impact of the observed 1% to 4% fallout to an overall cost impact of 7% to 10%. GAL devices exhibit no board-level fallout (and therefore no cost impact). Board throughput is also a major cost contributor, with typical reworks of 20% to 30% a consequence of PAL quality levels.

11 **System-Level Failures** add 8% to 15% to the PLD cost, taking into consideration a 100x 'Factor of Ten Rule' multiple. GAL devices again provide 100% yields, and therefore exhibit no system-level-failure cost impact

Notes

Section 1: Introduction to Generic Array Logic

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Section 3: GAL Military Products

Section 4: pLSI and ispLSI Products

Section 5: GAL Quality and Reliability

Section 6: GAL Technical Notes

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Programmable Clocks Improve System Performance

Introduction

There is a growing need for innovative design techniques to increase the system throughput using the currently available Programmable Logic Devices (PLDs). One way of improving the system throughput is to make use of Lattice's new GAL20RA10-15. By taking advantage of the unique architecture featuring an individually controlled clock on each of the Output Logic Macro Cell (OLMC) registers, the resolution of the control signals generated by a GAL20RA10-based state machine can be doubled. The design example shown in this Application Brief takes advantage of this feature in a Dynamic RAM (DRAM) control logic design.

Design Example

The most common control signals generated by DRAM control logic are the Row Address Strobe (RAS) and the Column Address Strobe (CAS). The timing requirements of these control signals are strictly governed by the DRAM's timing requirements. Based on the DRAM's timing requirement, Figure 1a shows how the RAS and CAS control signals are generated from a standard PLD device which has only one dedicated active high clock signal driving all the output registers. The basic constraint of the high-to-low transition of RAS signal to the high-to-low transition of CAS signal for the 100ns DRAM is 15ns minimum (row address hold time after RAS). As illustrated in Figure 1b, the activation of CAS signal is unnecessarily delayed because of the

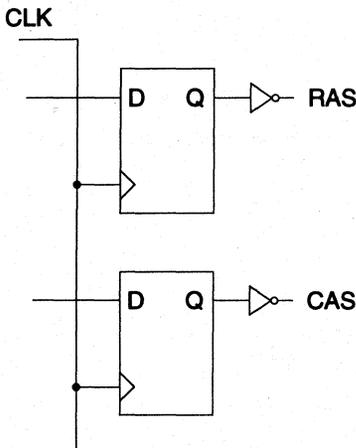


Figure 1a.
Standard PLD design with a
single active-high clock

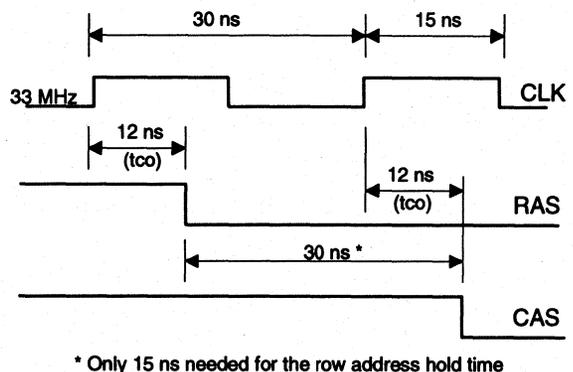


Figure 1b.
Control signal generation with a
single active-high clock

limitations of the standard PLD's single active-high clock driving all the output registers. This limitation is not a reflection of the DRAM's requirements but rather a limitation of the standard PLD.

Design engineers can improve this design method by using the GAL20RA10's independent OLMC clocks. Figure 2b shows the RAS and CAS signals being driven by both the rising and falling edges of the clock signal. This technique can be implemented in the GAL20RA10 by simply feeding the complement of the clock input from the RAS control register to the CAS control register, as shown in figure 2a.

Summary

The individual clock control on the OLMC is one of several different individual product-term controlled features which are available on the GAL20RA10. Other individual product-term controlled signals of the GAL20RA10 include the Asynchronous Preset (AP) and Asynchronous Reset (AR). These signals can also be used, similar to the clock signal, to enhance system performance. In addition to these features, the GAL20RA10 has an external preload (PL) capability to improve the control over the register contents — especially in state machine design. The full GAL20RA10 macrocell architecture is shown below, in figure 3.

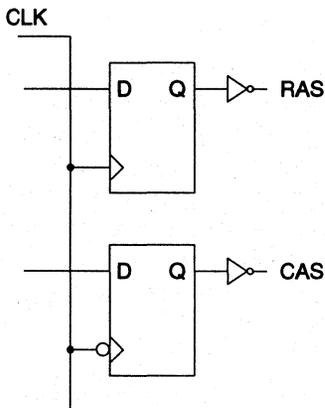


Figure 2a.

Standard PLD design with dual-polarity clocks

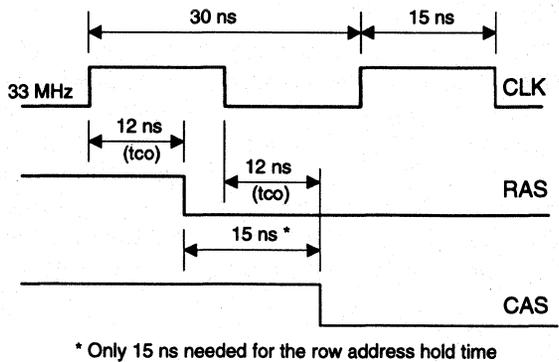


Figure 2b.

Control signal generation using a GAL20RA10

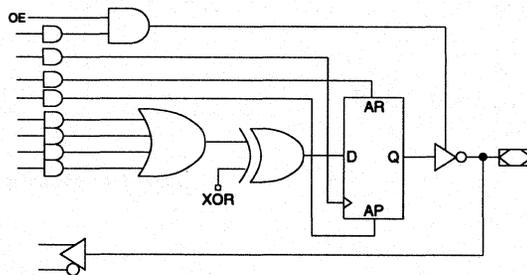


Figure 3.
GAL20RA10 Macrocell

Programmable Frequency Divider

Introduction

When designing with standard PLDs such as the GAL20V8 and GAL22V10, system design engineers are sometimes faced with the situation where a few extra product terms or extra macrocells are required to implement the design. These situations usually do not warrant adding a second standard PLD. The ideal solution is to find a way to add these extra product terms and/or outputs while still keeping the design to one device. The design example given in this application brief illustrates one example of how the extra outputs of the GAL26CV12 can solve the common problem of needing additional outputs. The design will show a programmable frequency divider that uses a 10-bit counter as a base and can therefore divide the incoming frequency by up to 1024.

Design Example

The design requirements for the programmable logic device are 10 macrocells for the internal counter, one macrocell for the programmable output frequency, 4 inputs for the frequency selection and one input clock. Figure 1 below shows the simple block diagram of the programmable frequency divider.

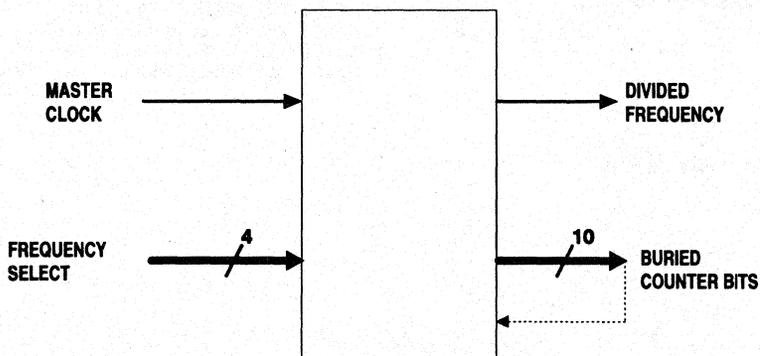


Figure 1. Block Diagram of Programmable Frequency Divider

This frequency divider implementation, using D type registers, requires more than 8 product terms for the two most significant counter bits on the 10-bit counter. The programmable frequency output also requires more than 8 products terms. Therefore, even two GAL20V8 devices (or other standard PAL devices) would not work for this design since they only have a maximum of 8 product terms per output. Since a total of 11 macrocells is required to

implement the counter and the programmable frequency output, even a 22V10 device would not work.

A single GAL26CV12 device satisfies both the product term requirements and the output macrocell requirements for the example design. The equations and the output pin assignments to implement the 10-bit programmable frequency divider are given below. Notice that the outputs that require more than 8 product terms are assigned to the inner-most pins of the device.

```

Q0.D = ( IQ0 );           *PIN 27
Q1.D = ( Q0 & IQ1
# IQ0 & Q1 );           *PIN 26
Q2.D = ( Q0 & Q1 & IQ2
# IQ1 & Q2
# IQ0 & Q2 );           *PIN 25
Q3.D = ( Q0 & Q1 & Q2 & IQ3
# IQ2 & Q3
# IQ1 & Q3
# IQ0 & Q3 );           *PIN 23
Q4.D = ( Q0 & Q1 & Q2 & Q3 & IQ4
# IQ3 & Q4
# IQ2 & Q4
# IQ1 & Q4
# IQ0 & Q4 );           *PIN 15
Q5.D = ( Q0 & Q1 & Q2 & Q3 & Q4 & IQ5
# IQ4 & Q5
# IQ3 & Q5
# IQ2 & Q5
# IQ1 & Q5
# IQ0 & Q5 );           *PIN 16
Q6.D = ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & IQ6
# IQ5 & Q6
# IQ4 & Q6
# IQ3 & Q6
# IQ2 & Q6
# IQ1 & Q6
# IQ0 & Q6 );           *PIN 17
Q7.D = ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & IQ7
# IQ6 & Q7
# IQ5 & Q7
# IQ4 & Q7
# IQ3 & Q7
# IQ2 & Q7
# IQ1 & Q7
# IQ0 & Q7 );           *PIN 18
Q8.D = ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & IQ8
# IQ7 & Q8
# IQ6 & Q8
# IQ5 & Q8
# IQ4 & Q8
# IQ3 & Q8
# IQ2 & Q8
# IQ1 & Q8
# IQ0 & Q8 );           *PIN 19
Q9.D = ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & Q8 & IQ9
# IQ8 & Q9
# IQ7 & Q9
# IQ6 & Q9
# IQ5 & Q9
# IQ4 & Q9
# IQ3 & Q9
# IQ2 & Q9
# IQ1 & Q9
# IQ0 & Q9 );           *PIN 20
FDIV = ( SEL0 & ISEL1 & ISEL2 & SEL3 & Q9
# ISEL0 & ISEL1 & ISEL2 & SEL3 & Q8
# SEL0 & SEL1 & SEL2 & ISEL3 & Q7
# ISEL0 & SEL1 & SEL2 & ISEL3 & Q6
# SEL0 & ISEL1 & SEL2 & ISEL3 & Q5
# ISEL0 & ISEL1 & SEL2 & ISEL3 & Q4
# SEL0 & SEL1 & ISEL2 & ISEL3 & Q3
# ISEL0 & SEL1 & ISEL2 & ISEL3 & Q2
# SEL0 & ISEL1 & ISEL2 & ISEL3 & Q1
# ISEL0 & ISEL1 & ISEL2 & ISEL3 & Q0 ); *PIN 22

```

Summary

The GAL26CV12 has a total of 12 output logic macrocells and a product term distribution of 8 terms on the outermost pins to 12 on the innermost pins. It comes in a 28-pin DIP and PLCC package, with center Vcc and Ground pins on the DIP package. When design engineers are frustrated by the limitations on the number of available product terms, output macrocells, or input pins on standard PLD devices, using the GAL26CV12 is a valuable design alternative. Since the GAL26CV12 can often save the cost of adding a second PLD, the design is simplified while also cutting cost and board space requirements.



The GAL18V10 Advantage

June 12, 1991

Application Brief #ABR1019

Introduction

Although the GAL16V8 is able to replace a number of different standard PLDs, such as the common PAL16L8 and PAL16R8, there are times when the designer needs more flexibility than the standard 20-pin PLDs offer. Moving the PLD design to the next package size means using a 24-pin DIP or 28-pin PLCC package. Often the increase in functionality is out of proportion to the increase in package size.

This application brief describes the most common limitations of a standard PLD and how the GAL18V10's unique architecture allows the designer much greater functionality while maintaining the same 20-pin package. In addition, the architecture of the 18V10 is exactly the same as the industry-standard 22V10 device, which means that learning a new device architecture is not necessary.

More Inputs

One of the benefits of Lattice's patterning of the GAL18V10 after the 22V10 device is that the macrocell structure allows for greater flexibility than the common 20-pin PAL-type devices. Whereas the GAL16V8, because of its exact emulation of many PAL devices, must limit the I/O pins that can have feedback or be configured as inputs, the 18V10 has no such limitations. Every one of the I/O pins on the GAL18V10 can be configured as registered or combinatorial, has feedback capability, and can be configured as a dedicated input or dynamic I/O pin.

<u>GAL16V8 emulation mode</u>	<u>No feedback or input</u>
Complex Mode (16L8)	pins 12, 19
Simple Mode (16H4, etc.)	pins 15, 16

More Outputs

As the name suggests, the GAL18V10 has a total of 10 possible outputs. In cases where more than eight outputs are needed on the standard PLD, a GAL18V10 makes an ideal replacement. One demonstration of the additional capability of the GAL18V10 is an eight-bit counter with a carry-out signal. A GAL16V8 or PAL16R8 device can be used to build an eight-bit counter. However to provide a carry-out and/or carry-in signal, more outputs are required. The GAL18V10 fits the bill nicely, since it is a functional superset of the already flexible GAL16V8. Adding a few extra lines of equations in the source file and re-compiling produces a JEDEC file for a totally pin-compatible replacement, but with extra functionality. Other uses for the additional output macrocells include implementing nine or ten bit counters and decoded outputs from eight or nine bit counters. All of these functions could be done in a 22V10 as well (at extra cost), but could not be done in any of the common 20-pin PAL devices, or even in newer devices such as the 85C220, 18CV8, or EP320. Below is an example of two implementations of an eight-bit counter with carry-in and carry-out. While this design fits in one GAL18V10, it requires two different 20-pin PAL devices.

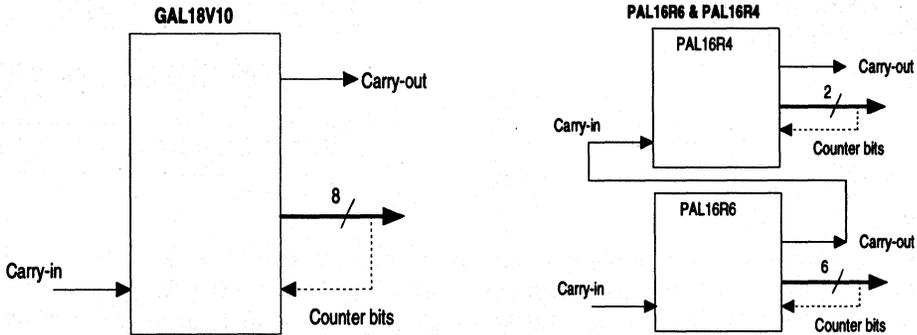


Figure 1. 8-bit Counter with Carry-In and Carry-Out

Reset and Preset

Another benefit of the 22V10 nature of the GAL18V10 is the inclusion of Asynchronous Reset and Synchronous Preset of the registers. These dedicated product terms can allow any pin or combination of inputs and/or feedbacks to trigger a global reset or preset to occur. In many other devices this can only be accomplished by using valuable product terms and extra design time to build this capability into the logic for each output. Since each output in these devices has only seven or eight product terms, the addition of the reset/preset logic may make it impossible to fit in the desired logic functions. For example, the eighth output of an eight-bit counter will look something like:

```

Q7 := ( Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & IQ7      "Product Term 1
      # !Q6 & Q7                                     "Product Term 2
      # !Q5 & Q7                                     "Product Term 3
      # !Q4 & Q7                                     "Product Term 4
      # !Q3 & Q7                                     "Product Term 5
      # !Q2 & Q7                                     "Product Term 6
      # !Q1 & Q7                                     "Product Term 7
      # !Q0 & Q7 );                                  "Product Term 8

      # !Synch_Preset                                " NO MORE PRODUCT TERMS AVAILABLE!

```

To add the capability for a synchronous preset would require the use of an additional product term, which may not be available. This same problem may come up in a complex state machine.

The Asynchronous Reset function cannot even be duplicated in the GAL16V8 or standard PAL devices. The GAL18V10 can be asynchronously reset, therefore simplifying the power-up routine by not requiring a clock cycle to put the device into a known state.

Flexible Output Enable

Again because of its exact emulation of the common 20-pin PAL devices, the GAL16V8 has limited options for placement of the Output Enable control pins. A GAL16V8 with any I/O macrocells configured in registered mode always has pin 11 dedicated to the output enable of

the register. Pin 11 is then no longer available as an input to the array. This means that any combinatorial outputs that need output enable control must use an additional pin, since the output enable control of combinatorial outputs is through a product term. A design with a mix of registered and combinatorial outputs using a GAL16V8 (or 20-pin PAL device) must always use two pins to get output enable control on all outputs. The GAL18V10 has no such restrictions. All output enable control is from a product term, regardless of whether the output is configured as registered or combinatorial.

Saving one pin on a 20-pin device can mean the difference between keeping the design in a 20-pin device and having to go to a larger (and more expensive) device. Figure 2 illustrates how the GAL18V10 can use one less pin than a GAL16V8 or 20-pin PAL device when both registered and combinatorial outputs must be tri-stated.

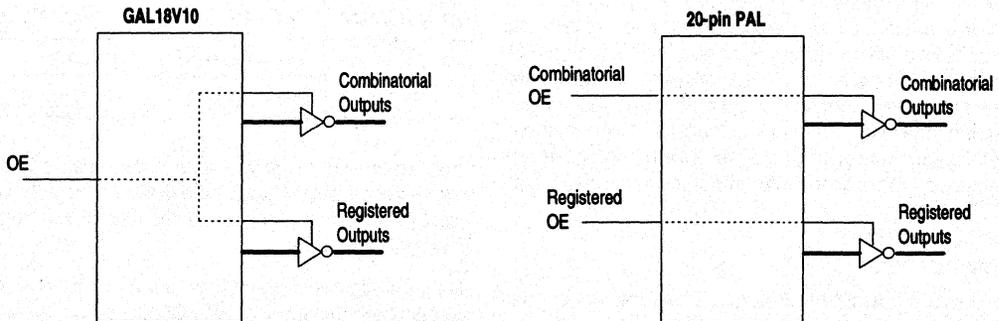


Figure 2. Output Enable Pin Consolidation

Conclusion

It is clear that standard PAL architectures have definite limitations. Lattice first addressed this issue with the GAL16V8 and GAL20V8 devices, which were able to replace all standard 20 and 24-pin PAL devices. For replacing those same PAL devices, and adding some additional flexibility, the GAL16V8 and GAL20V8 devices are a vast improvement and have become an industry standard in their own right.

However, as the previous examples have pointed out, there are many cases where the old standby programmable logic architectures, and even the first-generation GAL replacements, don't have the flexibility required. For 20-pin devices, the GAL18V10 provides complete design flexibility by using the familiar 22V10 architecture, while maintaining the ability to provide a pin-compatible superset of the GAL16V8.



Driving CMOS Inputs With GAL Devices

November 1991

Applications Brief #ABR1025

INTRODUCTION

While Lattice GAL[®] devices do not have a true CMOS output structure, in most cases they are able to reliably drive CMOS inputs. GAL devices are designed with TTL-level input and output specifications. There are two reasons for this. First, because Lattice GAL devices are as fast, or nearly as fast, as the fastest equivalent bipolar devices, they are often used as bipolar replacements. While a design may initially be done with bipolar devices, often the designer has the opportunity to replace the bipolar device with the lower-power and better tested GAL device. In these cases, the GAL device must drop into the same socket with identical functionality. Second, switching noise is greatly reduced by using TTL-level outputs. Switching an output from Vcc to Ground will generate considerably more noise than switching from a TTL high to a TTL low.

NMOS OUTPUTS

GAL devices use a NMOS output structure, which does not allow the output signal to go to the rail but still gives plenty of margin to TTL specs. The NMOS output structure also completely eliminates any possibility of latch-up.

Under typical conditions of room temperature and nominal Vcc, GAL devices will exhibit a VOH of about 4.2 volts. This value will change somewhat with temperature, Vcc, and normal process variations. Process and temperature are the most important factors, in that they affect the amount of voltage drop between Vcc and the output pin. Therefore the most valuable way to specify a VOH value is to specify the difference between Vcc and VOH. In this manner, a designer with greater control over Vcc can know exactly what the true worst-case VOH value will be. The following tables show the VOH values that can be expected under different conditions.

Commercial and Industrial Devices

Specification	Condition	Min. Value
VOH	IOH = 3.2 mA	2.4 V
	IOH = 100 μ A	Vcc -1.0 V

Military Devices

Specification	Condition	Min. Value
VOH	IOH = 2.0 mA	2.4 V
	IOH = 100 μ A	Vcc -1.2 V

One factor that helps to make it all work is that even though the output voltage or the GAL device will drop with Vcc, the input transition point of the CMOS devices being driven will also drop.

Using pull-up resistors on the outputs of the GAL device will also help to assure proper CMOS output levels. A 10 Kohm pull-up resistor will pull a GAL device's output to the rail. Of course the time required to do so depends on the total capacitance on the the output pin, which includes the I/O capacitance of the GAL device output, the input capacitance of the devices being driven, and the parasitic capacitances on the board.

For further assistance, contact Lattice Applications Engineering at Tel: 1-800-FASTGAL (327-8425) or FAX: (503) 681-3037.



GAL20XV10B

Design Example

November 1991

Applications Brief #ABR1027

Data Block Transfer Address Detector

Introduction

The Exclusive-OR (XOR) gate can efficiently implement arithmetic functions such as counters, adders and decoders. The XOR gate implements arithmetic functions using fewer product terms than the standard sum-of-product PLD's programmable AND, fixed OR array. This is demonstrated by the following logic equation example.

\$ - XOR function syntax
- OR function syntax

& - AND function syntax
! - INVERT function syntax

XOR Function

A \$ B /* 2 PT used
(A & B) \$ (C & D) /* 2 PT used

Equivalent AND/OR Function

(A & !B) # (!A & B) /* 2 PT used
(A & B & !C) # (A & B & !D) /* 4 PT used
(!A & C & D) # (!B & C & D)

To take full advantage of product term usage in a high speed system design, a high speed device with a built-in XOR function is needed. The Lattice GAL20XV10B fills the need for such a device. The GAL20XV10B achieves a 10ns Tpd while consuming only 90mA Icc (Max.). The closest competitor's device offers only a Tpd of 30ns at 180mA Icc. In addition, the generic architecture of the GAL20XV10B gives system designers the ability to configure outputs to any combination of registers, combinatorial, XOR and AND/OR structures.

Design Example

An address counter that uses a comparator to keep track of the block data transfer is a typical application which illustrates the advantages of the GAL20XV10B's XOR architecture. If the starting address and ending address are given, the address counter will take the starting address and counts to the transfer address when the transfer begins. The comparator then compares the counter bits with the ending address. When the counter value equals the ending address, the address comparator issues a transfer complete signal. The following CUPL example source file shows how this function can be implemented using CUPL compiler syntax. Notice that the syntax demonstrates the usage of .OE and .OEMUX to control the AND/OR product term configuration and XOR configuration, respectively.

Conclusion

This design example illustrates the efficient usage of XOR function by implementing the address counter with 11 product terms instead of the 14 product terms required with a standard programmable AND, fixed OR configuration. The bit-wise comparator, implemented with the XOR function, also makes the design clear and understandable, as can be seen from the logic equations. Furthermore, the design is implemented with a fast 10ns Tpd and a clock frequency which can run as fast as 100MHz.

GAL20XV10B Design Example

CUPL Example File

Name APPXV10;
Partno 00;
Date 3/3/92;
Revision 00;
Designer B. Leigh;
Company Lattice;
Assembly None;
Location None;
Device g20xv10;

```
/* *****  
/* This CUPL example use the GAL20XV10 to build the */  
/* 4-bit up counter with load function and a 4-bit */  
/* comparator. This counter implementation takes */  
/* advantage of the built-in XOR function of the */  
/* GAL20XV10. It also shows the XOR and AND/OR */  
/* configuration in CUPL syntax */  
/* *****
```

```
/** Input definition **/
```

```
PIN 1 = SYSCLK;  
PIN 2 = SA0; /* STARTING ADDRESS BITS */  
PIN 3 = SA1;  
PIN 4 = SA2;  
PIN 5 = SA3;  
PIN 6 = EA0; /* ENDING ADDRESS BITS */  
PIN 7 = EA1;  
PIN 8 = EA2;  
PIN 9 = EA3;  
PIN 10 = STARTLD; /* STARTING ADDRESS LOAD */  
PIN 11 = OE_COMP;  
PIN 13 = OUT_EN;
```

```
/** Output Definition **/
```

```
PIN 23 = !AC0; /* ADDRESS COUNTER BITS */  
PIN 22 = !AC1;  
PIN 21 = !AC2;  
PIN 20 = !AC3;  
PIN 19 = !CMP0; /* ADDRESS COMPARE BITS */  
PIN 18 = !CMP1;  
PIN 17 = !CMP2;  
PIN 16 = !CMP3;  
PIN 15 = EQUAL; /* EQUALITY COMPARE */
```

```
/** Equations **/
```

```
AC0.D = !STARTLD & AC0 /* AC0 TOGGLE WITH CLOCK **/  
$ STARTLD & SA0; /* LOAD SA0 **/  
AC0.OEMUX = OUT_EN;
```

GAL20XV10B Design Example

```
AC1.D = !STARTLD & AC0           /** AC1 CNT UP CONDITION **/  
      $ !STARTLD & AC1           /** TOGGLE AC1 **/  
      # STARTLD & SA1;           /** LOAD SA1 **/  
AC1.OEMUX = OUT_EN;  
  
AC2.D = !STARTLD & AC0 & AC1     /** AC2 CNT UP CONDITION **/  
      $ !STARTLD & AC2           /** TOGGLE AC2 **/  
      # STARTLD & SA2;           /** LOAD SA2 **/  
AC2.OEMUX = OUT_EN;  
  
AC3.D = !STARTLD & AC0 & AC1 & AC2 /** AC3 CNT UP CONDITION **/  
      $ !STARTLD & AC3           /** TOGGLE AC3 **/  
      # STARTLD & SA3;           /** LOAD SA3 **/  
AC3.OEMUX = OUT_EN;  
  
CMP0 = AC0 $ EA0;                /** COMPARE ADDR BIT0 **/  
CMP0.OEMUX = OUT_EN;  
  
CMP1 = AC1 $ EA1;                /** COMPARE ADDR BIT1 **/  
CMP1.OEMUX = OUT_EN;  
  
CMP2 = AC2 $ EA2;                /** COMPARE ADDR BIT2 **/  
CMP2.OEMUX = OUT_EN;  
  
CMP3 = AC3 $ EA3;                /** COMPARE ADDR BIT3 **/  
CMP3.OEMUX = OUT_EN;  
  
EQUAL = !CMP0 & !CMP1 & !CMP2 & !CMP3; /** MAGNITUDE COMPARE **/  
EQUAL.OE = OE_COMP;
```

Notes

GAL6002B Design Example

The condition of TxD and DSR after sending a byte of data is the same as before sending it. So, from an electrical perspective, there is no indication whether or not the computer is going to send another byte. If it is going to, it simply does so "when it feels like it."

3) Somewhere in the middle of the transfer, the printer runs out of paper, or its print buffer fills up, or for some other reason it must suspend communications. When this happens, the printer deasserts its DTR line, telling the computer to stop sending data. When the printer is again ready to accept data, it will reassert DTR.

As alluded to in #2 above, there is no absolute way to tell when the computer is finished sending data. In fact, the computer can be said to have "finished" its transmission after sending only the first byte of a multi-byte transmission. Each subsequent byte transfer can be viewed as an entirely new transaction. Extended periods of time may even elapse between byte transfers if the computer has to do disk access or is interrupted for some reason. Remember, RS232 is an asynchronous communications protocol.

FUNCTIONAL DESCRIPTION

The Port MUX has five ports, numbered 0 to 4. Port 0 is connected to the printer, while ports 1 through 4 are connected to the computers. The port MUX merely acts as an intelligent switch; data flows through it unhindered and unaltered. At any given time, there will always be one (and only one) computer connected to the printer.

Four signals per port are switched: TxD, RxD, DTR, and DSR. This arrangement is known to work for connecting IBM-PC compatible computers to an HP LaserJet. The RS-232 specification has no lack of ready/busy signals, so others could be substituted for DTR and DSR if necessary (CTS and RTS, for example). See Figure 2 for a block diagram of the port multiplexer.

Since RS-232 signal levels are not compatible with TTL levels, line driver/receiver circuits are needed to translate. For this project, Maxim MAX235 Driver/Receiver chips were used, though others devices will work as well. Each MAX235 IC has five drivers and five receivers; two MAX235 ICs are needed to build the Port MUX.

The multiplexer functions by sequentially scanning the four input ports until data appears at one of them.

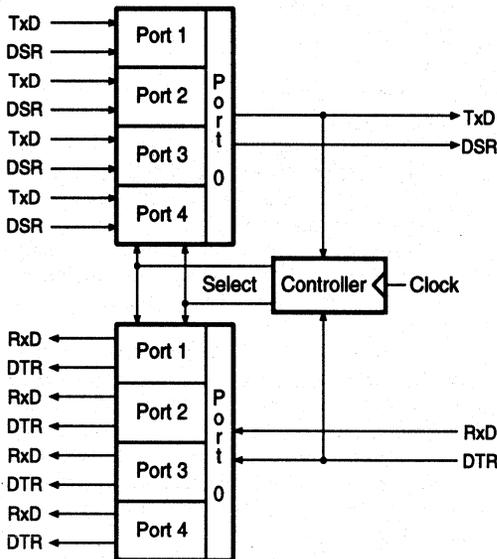


Figure 2. Block diagram of Port MUX

Scanning a port involves connecting that port to the printer and waiting for data to flow. If no data appears within a predetermined time period, the period of the system clock (- .25s), the process is repeated at the next port. When data does appear at a port, the port MUX "locks onto" that port and goes into the transmit mode. At the end of the transmission, the port MUX returns to the scan mode.

As mentioned in the discussion of RS-232 protocol, detecting the end of a transmission is non-trivial. To peripheral devices such as printers, the "end of transmission" concept is a fiction — to them, life is one big data transmission. The port MUX, on the other hand, must be able to determine when it is permissible to resume scanning. It should not return to the scan mode before the end of a transmission, and at the same time it must not lock onto a port for an inordinately long time. Both requirements are met by timing how long the computer's TxD line is idle, and returning to the scan mode if TxD is idle for longer than a predetermined time period (5 - 10 seconds is reasonable).

The data routing logic of the port multiplexer is controlled by two loosely coupled state machines and a status register. The state machines and the status register use the State Logic MacroCells (labeled as state bits S0 - S7). The status register determines the operating mode (scan or transmit), the first state machine determines the active port, and the second state machine is used as a timer.

GAL6002B Design Example

The basis for most state machines is the simple binary counter, with added logic to allowing branching, state skipping, etc. The most efficient way to build a binary counter in the GAL6002B is to configure the registers to emulate T-flip flops. This way, only the conditions that should cause the state bits to change state need to be specified. In the case of simple up counters, there is only one condition when all lower order bits are ones. The equations for a 4-bit up counter are as follows:

$$\begin{aligned}B0.D &= /BO.Q; \\B0.E &= 1; \\ \\B1.D &= /B1.Q; \\B1.E &= B0; \\ \\B2.D &= /B2.Q; \\B2.E &= B1*B0; \\ \\B3.D &= /B3.Q; \\B3.E &= B2*B1*B0;\end{aligned}$$

As you can see, counters of any size can be built using only two product terms per bit.

In the following discussions POTx and PODT are TxD and DTR respectively.

STATUS REGISTER

Recall that the beginning of a data transfer is signaled by POTx becoming active for one bit period. By using the start bit event to asynchronously set a status register, set = transmit, the operating mode of the port MUX is determined. Once set, the status bit will remain set until a time-out occurs.

The status register is implemented using state bit S0, configured to emulate a T-flip flop with a programmable clock. With such an arrangement, meeting the specified state transition conditions doesn't just allow a transition at the next clock, but actually causes the transition.

There are two situations that must cause the status register to toggle: if it is clear, clear = scan, and data is flowing, or if it is set and a timeout has occurred. The equations for the status register are:

$$\begin{aligned}S0.D &= /SO.Q; \\S0.CK &= /SO.Q*/POTx \\ &\quad +sO.Q*POTx*PODT*57.Q*56.Q*55.Q*54.Q*53.Q;\end{aligned}$$

The same function could have been implemented by "building" a latch from combinational equations, but the approach taken here is more efficient in terms of product term usage and is less prone to functional hazards.

PRIMARY STATE MACHINE

The primary state machine directly determines the active port. It is simply a 2-bit counter with a hold function. The conditions necessary for the counter to increment are that the status register be clear and that PODT be active.

The primary state machine uses state bits S1 and S2 in the D/E configuration to emulate T-flip flops. The equations for S1 and S2 are:

$$\begin{aligned}S1.D &= /S1.Q; \\S1.E &= PODT*/SO.Q; \\ \\S2.D &= /S2.Q; \\S2.E &= PODT*/SO.Q*S1.Q;\end{aligned}$$

TIMER

The second state machine, a 5-bit counter/timer, will only count while the status register is set and POTx is idle and PODT is active. The counter synchronously resets to zero if these conditions are not met. Thus, if PODT is active and POTx is idle on 31 consecutive OCLK edges, the timer will reach its maximum value, causing the status register to be cleared and the primary state machine to continue counting.

The 5-bit timer uses state bits S4 - S7 in the D/E configuration, again emulating T-flip flops. The equations for the timer are:

$$\begin{aligned}S3.D &= /S3.Q*SO.Q*POTx*PODT; \\S3.E &= 1; \\ \\S4.D &= /S4.Q*SO.Q*POTx*PODT; \\S4.E &= S3.Q \\ &\quad + /SO.Q; \\ \\S5.D &= /S5.Q*SO.Q*POTx*PODT; \\S5.E &= S3.Q*S4.Q \\ &\quad + /SO.Q; \\ \\S6.D &= /S6.Q*SO.Q*POTx*PODT; \\S6.E &= S3.Q*S4.Q*S5.Q \\ &\quad + /SO.Q; \\ \\S7.D &= /S7.Q*SO.Q*POTx*PODT; \\S7.E &= S3.Q*S4.Q*S5.Q*S6.Q \\ &\quad + /SO.Q;\end{aligned}$$

Time-out during a byte transfer, though statistically not impossible, is unlikely. If it should occur, however, it is not harmful. Because a time-out simply clears the status register and scanning does not resume until the next OCLK edge, the driving computer still has one OCLK period to finish the byte transfer (plenty of time!), during which time a logic zero on POTx returns the status register to the transmit mode. Thus, it is virtually impossible for a byte of data to be lost.

GAL6002B Design Example

If the port MUX should time-out and resume scanning between byte transfers, but before the end of a transmission, and another computer is waiting to use the printer, then that computer will be serviced before the first computer is again granted use of the printer. This would cause the second computer's data to be inserted into the middle of the first computer's transmission. This situation, though undesirable, is unavoidable. The good news is that the probability of it happening is very low.

CONCLUSION

The Port MUX provides a "real life" example of how the flexibility of the GAL6002B can simplify a complex design. Equally important, this example shows how various software tools are used to access the device's features. Unfortunately, the Port MUX is not a speed critical application. In fact, the GAL6002B's 15ns t_{pd} is overkill.

Though this example is complex, it still does not push the GAL6002B to its limits. The state machine and data routing equations use only 33 product terms, leaving over 48% of the AND array free for expansion. The GAL6002B's FPLA architecture allowed 5 product terms to be merged. If this design were implemented using a standard 24-pin PLD, it would take at least two devices to accomplish the task.

Section 1: Introduction to Generic Array Logic

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Section 3: GAL Military Products

Section 4: pLSI and ispLSI Products

Section 5: GAL Quality and Reliability

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Section 9: General Information

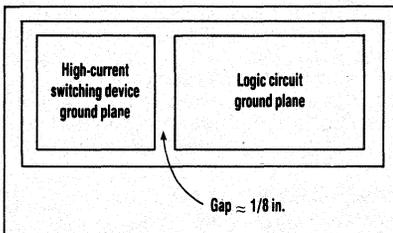
MAKE SURE THAT YOUR TURBO-CHARGED LOGIC SYSTEM WORKS BY PAYING AS MUCH ATTENTION TO PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES AS TO LOGIC DESIGN CONSIDERATIONS.

AVOID THE PITFALLS OF HIGH-SPEED LOGIC DESIGN

Modern high-speed systems demand modern high-speed logic families. Consequently, semiconductor houses have developed such product lines as ACT, FACT, and AS. But these systems also demand that the lay-out of their boards conform with the results of distributed-element theory, otherwise ringing, crosstalk, and other transmission-line phenomena render those systems inoperative. Meeting this second requirement necessitates something more than a new product introduction—it insists on a change in the way logic boards are engineered. The logic-systems designer and the board-layout designer must work hand-in-hand if a viable high-speed board or system is to be produced.

In the past, logic design and board layout were usually regarded as separate parts of the design process. First the system designer configured the logic, then the board engineer laid it out. That approach worked because slew rates were so low (0.3 to 0.5 V/ns) that crosstalk wasn't much of a problem; rise times were so long (4 to 6 ns) that ringing could settle down before a logic element could change state; and in general, the assumptions of lumped-element circuit theory usually worked out pretty well.

For systems designed with today's high-speed logic circuitry, those underlying assumptions no longer hold true. Today's slew rates are on the order of 2 to 3 V/ns, rise times are below 2 ns (frequently, below 1 ns), and transmission-line phenomena, such as ringing, can be a problem for trace



1. TO MINIMIZE NOISE, THE ground plane should be fragmented into separate areas for noisy high-current devices and for sensitive logic circuits. For best results, the number of signal lines that cross the gap between the fragments should be minimized.

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DESIGNING WITH HIGH-SPEED LOGIC

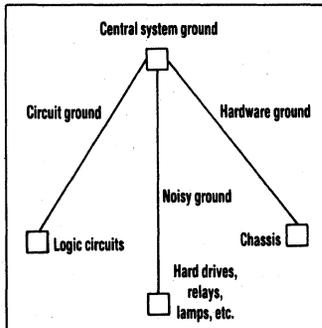
lengths as short as 7 in. As a result, logic designers must take certain steps:

- Use ground and power planes.
- Control conductor spacings to eliminate crosstalk.
- Make extensive use of decoupling capacitors.
- Pay attention to ac loading.
- Terminate lines properly to minimize reflections.

PLANE ADVICE

For high-speed logic, ground planes aren't simply suggested for reliable board performance—they are absolutely necessary. It's essential that one layer of the board be assigned for a ground plane and that it cover as large an area as possible. A solid ground plane lowers the ground-return-path impedance as well as the device-to-device ground pin impedance.

But a common ground plane for all of the circuitry in a system can cause problems by coupling noise from high-current switching devices into sensitive logic inputs. Therefore, the ground plane for such high-current



2. SEPARATE DEDICATED grounds should be supplied for the logic circuitry, noisy high-current devices, and the chassis. The three should come together at one point, the central system ground, which is usually located near the power supply.

devices as relays, lamps, motors, and hard drives should be separated from the logic ground. This can be accomplished by fragmenting the ground plane into discrete areas (Fig. 1).

But fragmentation causes problems of its own—it creates discontinuities in the characteristic imped-

ance of any transmission line that crosses the separation between fragments. Therefore, for best results, boards should be laid out so that only two fragments are needed. The gap between those fragments should be kept as narrow as possible (an eighth of an inch works well in most applications), and the number of signal lines that cross the gap should be minimized. Designers should also bear in mind that through-holes and vias subtract from the effective area of the plane, increasing its effective impedance.

As with grounding, an entire layer of the board should be designated as a power plane. Even though it is at a different potential, the power plane should be implemented in accordance with the same concepts as the ground plane. Therefore, it should be fragmented when necessary to isolate noisy components from delicate logic circuits.

A WELL-GROUNDED SYSTEM

In addition to properly designed power and ground planes, high-speed logic systems require the establishment of a good, clean (low-

SIGNAL LINES BECOME TRANSMISSION LINES

For the transmission line model illustrated in the diagram, the rise time (t_r) is less than the line propagation delay (T_D). In other words, a complete TTL level transition will occur before the pulse is received at the receiving end of the line and reflections (ringing) will result. The voltage change at point A on the line is expressed in Eq. 1:

$$\Delta V_A = \Delta V_{int} (Z_0 / (R_0 + Z_0))$$

Where: V_{int} = internal voltage on the output of the driver;

R_0 = output impedance of the driving gate;

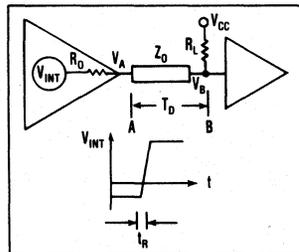
R_L = load impedance;

Z_0 = the characteristic line impedance;

and V_A = the source voltage at the sending end of the line.

Because R_0 is so small when compared to the line impedance, the change in voltage at point A (ΔV_A) will approximately equal the change in internal voltage (ΔV_{int}). This voltage transition propagates down the line and is seen at point B after the line propagation delay, T_D .

At point B, a portion of the wave will be reflected back towards point A in accordance with



the formula (Eq. 2):

Eq. 2

$$\rho_L = (R_L - Z_0) / (R_L + Z_0)$$

where ρ_L , called the voltage reflection coefficient (rho), is the ratio of the reflected voltage to the incident voltage.

After examining Eq. 2, it should be evident that $-1 \leq \rho \leq +1$. It should also be evident that there will be no reflected wave if $R_L = Z_0$ —if the line is terminated in its characteristic impedance. Note that the reflected wave can, in principle, be as large as the incident voltage and of either positive or negative polarity.

This analysis holds true for the sending end of the line, as well as the receiving end. That is,

Eq. 3

$$\rho_S = (R_0 - Z_0) / (R_0 + Z_0)$$

DESIGNING WITH HIGH-SPEED LOGIC

noise) system ground for reliable performance. A clean system ground ensures less noise within the system, and thus ensures good, strong transistor margins. At least 10% of the ground connections on the pc card should be connected to the system ground to reduce card-to-ground impedance.

Like the ground and power planes of the individual boards, the overall grounding scheme should be fragmented with separate conductors provided for the various sections of the system. For example, all relays, lamps, hard drives, and other noise-generating devices should have their own separate ground path. The system's mechanical package (chassis, panels, and cabinet doors) should have a dedicated ground. And, of course, the logic circuitry should have a ground of its own.

Those three grounds should then come together at the central system ground point, which will usually be located near the power supply (Fig. 2). This common-point grounding technique can also be very effective in reducing radiated interference (EMI and RFI).

TAMING CROSSTALK

Crosstalk—the undesirable coupling of a signal on one conductor to one on a nearby conductor—becomes an increasingly serious problem as slew rates go up. This signal coupling is made worse if the second trace has a high impedance or if the traces run parallel to one another for more than a few inches and are spaced less than 100 to 150 mils apart.

Crosstalk can be catastrophic to a logic board, sabotaging a conceptually flawless piece of logic design. For example, if a clock line and a data line run parallel to each other for more than several inches, and if the

data line cross-couples or superimposes its signal onto the clock line, the device that the clock is driving may detect an illegal level transition.

Methods to reduce crosstalk are straightforward, though not particularly elegant. The coupling can be attenuated by separating the adjacent traces as much as possible. The trouble with this approach is that available board real estate often lim-

creating a stub or a high-frequency antenna.

Another step that can be taken to reduce crosstalk is to lower the impedance of those traces into which crosstalk is especially to be avoided. The lower the impedance that a trace presents, the harder it will be to cross-couple a signal into it.

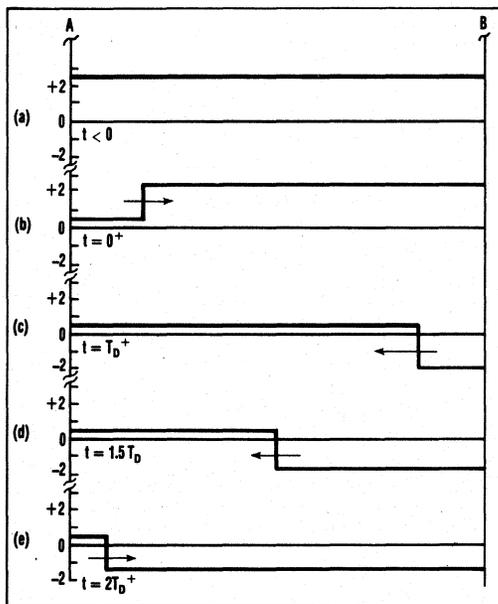
Even with the use of power and ground planes on a pc board, decoupling capacitors must be used on the V_{CC} pins of every high-speed device. Those devices demand a nearly instantaneous change in current whenever they switch states. Because the power plane can't meet that demand, a high-quality decoupling capacitor is required, otherwise the switching will cause noise on the V_{CC} plane.

A 0.1- μF multilayer ceramic (MLC) or other RF quality (low-inductance) capacitor should be placed on every fast-slew-rate device as close to the V_{CC} pin as possible. The commercially available DIP sockets with built-in decoupling capacitors also work well in this application.

Most designers, when they think of loading at all, think in terms of dc loading—traditionally referred to as fan-out and fan-in. But that type of loading rarely presents a problem with today's state-of-the-art logic devices. Much more significant when designing with high-speed logic are input and output ac loading.

INPUT CAPACITANCE

Because the input capacitance of a device impacts the overall performance of the logic circuit, it should be examined before a particular device is selected for a design. To ensure specified performance, the total load capacitance that a device drives—including the distributed ca-

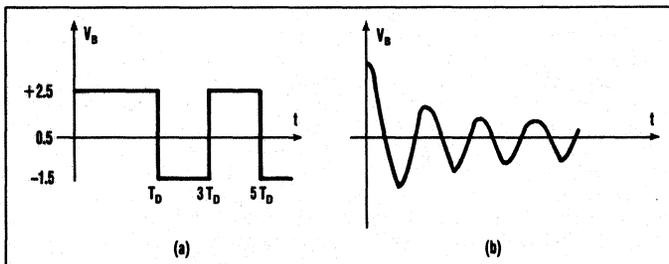


3. WAVE PROPAGATION along a transmission line occurs as follows: Prior to time zero, there is a steady-state voltage of 2.5 V dc on the line (a). At $t = 0$, the voltage at point A drops to 0.5 V, sending a negative pulse of -2 V toward point B (b). At $t = T_D$, that negative pulse is reflected from point B. It adds algebraically to the 0.5 V on the line and sends a -1.5-V pulse back toward point A (c). The reflections then continue as in (d) and (e).

its the possible separation to an inadequate amount.

Ground striping, or shielding, is an effective way to reduce crosstalk and it makes better use of available board area. With ground striping, a ground trace (the stripe) is run between the two parallel traces to act as a shield. If ground striping is used, through holes to the ground plane should be placed every 1 to 1.5 inches along the ground strip to eliminate the possibility of inadvertently

DESIGNING WITH HIGH-SPEED LOGIC



4. IDEALLY, THE VOLTAGE at point B oscillates forever between $+2.5$ V and -1.5 V (a). In reality, it will be a damped ringing (b).

capacitance of the trace—shouldn't exceed the device's specified capacitive load. Most high-speed logic devices have a maximum loading of 50 pF. As a rule of thumb, the maximum load on any logic element should be no more than four to six devices for best speed/load performance. However, there are some high-slew-rate devices on the market that have higher output drive capabilities.

BEWARE OF AUTOROUTER

The most common reason for not following the board-layout principles mentioned so far is having an autorouter do the layout. Autorouters do what they were designed to do very well: They place traces so as to make the most efficient use of the pc-board real estate. But most autorouters don't have the capability to determine which devices are high-speed and which are not. This is where the logic designer must step in

and lay out sections, or islands, of high-speed logic by hand in order to avoid the pitfalls of designing with high-speed logic.

TRANSMISSION LINES

In addition to the common-sense layout considerations discussed so far, designers of high-speed systems must have at least a basic understanding of transmission lines and proper termination techniques (see "Signal Lines Become Transmission Lines," p. 76). The reason: As frequencies go up, wavelengths come down to the point where they are of the same order as circuit-board dimensions. Once that happens, any connection between devices should be considered a transmission line. The lumped-element assumption is simply invalid above that point.

The most common consequence of failing to consider the distributed na-

ture of a high-speed logic board is ringing, which is caused by multiple reflections from the ends of unterminated transmission lines. An unterminated line has no load impedance ($R_L = \infty$) and is therefore an impedance-mismatched line. The behavior of this line when connected to a device with a fast slew rate can be understood from the following example: Prior to time zero, there's a steady-state voltage of 2.5 V dc at all points on the line (Fig. 3a). At $t = 0$, an initial TTL voltage transition from 2.5 V to 0.5 V occurs at point A (Fig. 3b). Time T_D later, the signal reaches point B and is reflected by the load reflection coefficient, ρ_L .

The input impedance of the device at point B is very high with respect to Z_0 ; R_L can be approximated by infinity. By plugging into Eq. 2 from the box (p. 76), the reflection coefficient approximately equals $+1$. In other words, the voltage reflected by the load is equal to the incident voltage (Fig. 3c). The reflected wave passes back along the signal path toward point A (Fig. 3d).

Repeating the calculations for the sending end of the line (point A), where $R_0 \approx 0$, you get a value for the source reflection coefficient, ρ_S , of -1 . In other words, there are reflections from the source as well as the load, but the source reflects the inversion of the wave that is incident upon it (Fig. 3e).

Looking just at the behavior of the signal at point B, the single-step volt-

RULES TO REMEMBER

The following ten rules summarize everything the logic designer needs to know when designing with high-speed CMOS.

- 1) Keep signal interconnections as short as possible.
- 2) Use a multilayer PCB.
- 3) Provide ground and power planes. Discontinuities in the planes should be avoided because reflections can occur from abrupt changes in the characteristic impedance.

4) Fragment the ground and power planes to supply separate sections for high-current switching devices.

5) Use decoupling capacitors on every high-speed logic device (0.1 μ F MLC type) located as close to the V_{CC} pin as possible.

6) Provide the maximum possible spacing among all high-speed parallel signal leads.

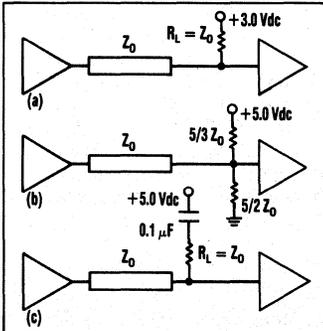
7) Terminate high-speed signal lines where $t_R < 2T_D$.

8) Beware of ac loading conditions within the design. Exceeding the manufacturer's recommended operating conditions, especially for capacitance, can cause problems.

9) When using parallel termination, put bends in all high-speed signal runs that go to more than one load. Use a termination load at the absolute end of the line.

10) Create islands of high-speed devices on the pc board. This simplifies board layout and ropes-off the high-speed areas.

DESIGNING WITH HIGH-SPEED LOGIC



5. THE BASIC PARALLEL

termination scheme works well but requires a separate 3-V supply (a). The Thevenin equivalent eliminates the need for a separate supply, but dissipates extra power from the regular 5-V supply (b). The use of a capacitor cuts dc dissipation altogether while supplying ac termination (c).

age transition at $t = 0$ leads to an endlessly oscillating signal with a total voltage swing of 4.0 V—twice the original level transition. The voltage doubling comes about because the voltage at point B is the sum of the incident and reflected waves at that point (Fig. 4a). Actually, because of the non-ideal nature of a real circuit board (finite input and output impedances, losses in the transmission lines, and so forth), ρ_L will be less than +1, and ρ_S will be greater than -1. As a result, the reflections will become successively smaller, causing the familiar damped ringing condition (Fig. 4b).

If the ringing amplitude is large enough, it can cause the receiving device to see an illegal level transition and possibly result in spurious logic states occupying the logic design. In some cases, the amplitude of the ringing can actually be large enough to damage the input of the receiving device.

TERMINATE YOUR TROUBLES

The way to eliminate ringing on a transmission line is to terminate the line in its characteristic impedance at either the sending or receiving end. The most common way to terminate a line is with a parallel termination at

the receiving end (Fig. 5).

In the configuration (Fig. 5a), $R_L = Z_0$ and R_L is pulled up to 3 V dc. In principle, R_L could be tied to ground, but TTL-compatible devices could not then supply the necessary drive.

Solving for ρ_L (Eq. 2), it can be seen that $\rho_L = 0$. Terminating a line in its characteristic impedance results in a reflection coefficient of zero, which means that there will be no reflections or distortions on the line. Other than the time delay, T_D , the line will act as if it were a dc circuit. It's important to note that even though devices or gates may be placed at any location on the line, the terminating resistor should be placed at the end of the line. In no case should the line be split like a Tee to feed several devices in parallel (Fig. 6a). Instead, it should be serpentine to feed them sequentially (Fig. 6b).

The 3-V power source shown (Fig. 5a) appears at first to be a major drawback, but R_L and the power supply can be expressed as a Thevenin equivalent running off the system power supply of 5 V dc (Fig. 5b). This variant works well, but the designer should bear in mind that it dissipates additional power.

REDUCING DISSIPATION

A solution that dissipates less power than either of the others uses a capacitor to cut the dc dissipation to zero (Fig. 5c). The recommended capacitor is a 0.1- μ F MLC type. Several manufacturers produce both capacitor-resistor and pull-up/pull-down termination packs. The pull-up/pull-down packs usually come in a single in-line package (SIP) with pins on 0.1-in. centers, while the capacitor-resistor combination comes in a standard 16-pin DIP. The most common SIP pull-up/pull-down resistor values are 220 Ω /330 Ω , 330 Ω /470 Ω combinations.

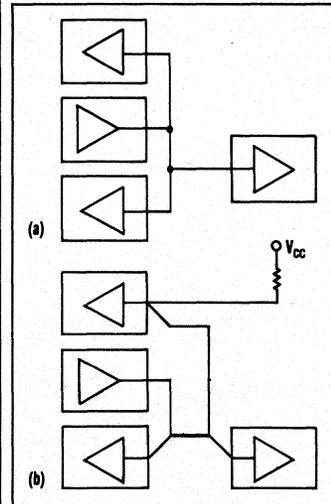
An alternative to a parallel termination at the receiving end is a series termination at the sending end (Fig. 7). The idea behind serial termination is to make $\rho_S = 0$ and $\rho_L = +1$. To do so, R_L is made equal to infinity (left unterminated) and a series resistor is added at the source to make the overall source impedance equal to the

characteristic impedance of the line—that is, $R_S + R_O = Z_{OL}$.

Making $R_S + R_O$ equal to Z_{OL} , of course, creates a voltage divider, which puts half of the signal amplitude across the line and half across the series combination of R_S and R_O . Therefore, with the series termination, the amplitude of the transmitted wave is half of what it would be without the termination.

Interestingly enough, the unterminated receiving end of the line precisely compensates for this halving of the amplitude. The reason is as follows: At the receiving end, the half-amplitude wave is received and a half-amplitude wave is reflected. But bear in mind that those are two separate waves whose amplitudes add at the point of reflection. As a result of this addition, the only thing seen at the receiving end of the line is a full-size pulse.

The main disadvantage of a series termination is that the receiving gate or gates must be at the end of the line—no distributed loading is possible. The obvious advantage of a series termination over a parallel one is that a series termination doesn't

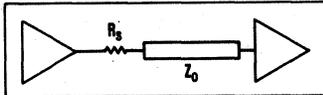


6. SERPENTINING IS essential when terminating a line. Never split the line to feed parallel devices (a). Rather, feed them sequentially with a serpentine line (b).

DESIGNING WITH HIGH-SPEED LOGIC

require any connection to a power supply.

Transmission-line effects must be taken into consideration whenever line propagation delays get up to the point where a signal transition can be completed before that signal can travel down a line, be reflected, and travel back to its starting point. In



7. THE SERIES termination needs no pull-up supply. Its main disadvantage is that it can't handle distributed loads.

other words, lines must be terminated when,

$$2T_D = T_R$$

CALCULATING DELAY

Taking 2 ns as a typical rise time for a state-of-the-art high-speed logic device, how long can a board trace get before its propagation delay gets to be 1-ns long? For a pc board with a continuous ground plane and a signal trace on the adjacent layer, the propagation delay depends on only one variable, the dielectric constant of the board material. That delay time is given by:

$$t_{PD} = 1.017 (0.475 e_R + 0.67)^{1/2} \text{ ns/ft}$$

For a typical board constructed of FR4 material, e_R (the dielectric constant) is 4.7 to 4.9. If an average e_R of 4.8 is used in the equation, then t_{PD} turns out to be 1.75 ns/ft, which works out to be 6.86 in./ns. As a rule of thumb, then, any line that is over 7 in. long should be considered a transmission line and approached accordingly. □

Jock Tomlinson, senior applications engineer at Lattice, holds a BSEE from Colorado State University.

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THE INDUSTRY NEWSPAPER FOR ENGINEERS AND TECHNICAL MANAGEMENT

Uses E²PROM PROGRAMMING Lattice fields FPGA

By STAN BAKER

Hillsboro, Ore. - Lattice Semiconductor Corp. is jumping into high-complexity PLDs with two families of devices that compete with FPGAs. The move significantly broadens the company's thrust in the logic market and puts it in the middle of the fastest-growing market segment. The new products also make Lattice the first company to move up from PAL devices to FPGAs with its own architecture.

Lattice's new pLSI and ispLSI devices will offer up to 8,000 equivalent gates. Both families will use E²PROM programming for the first time in

FPGAs, and the ispLSI family will be in-system programmable.

"I see the '90s as the decade of programmability," said Cyrus Tsui, president and CEO of Lattice. Market-research firms suggest he's right. They indicate the bipolar portion of the PLD business is dropping. Meanwhile, the CMOS portion is growing at a compound annual growth rate of more than 40 percent, and the high-complexity segment of the CMOS market is the most active.

"From a global standpoint, entering the high-density market will double

Lattice's total addressable market from 1 billion to 2 billion dollars in 1994," Tsui said. "In practical terms, these products will enable us to reach a class of customers in telecommunications, industrial control and the military that we currently cannot serve with our low-density GAL product offerings. This is both a unique product and company positioning."

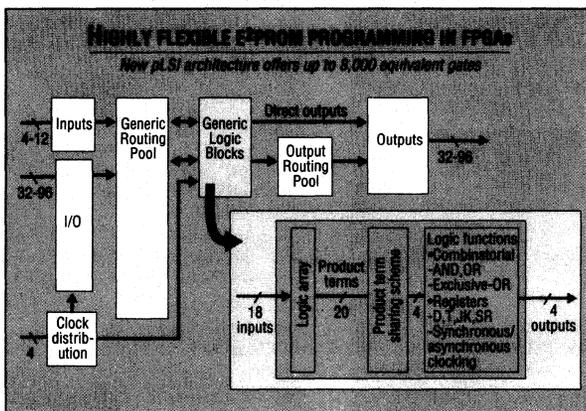
The new architecture features flexible granularity-the circuit blocks provide highly flexible programming of product terms, flexible choice of product-term sharing and steering, and choices of four outputs from the combinatorial and registered ports of the block.

Four functions

A single circuit block can implement up to four functions, since it has four outputs and the logic-array flexibility to separate them in the programmed cell routing. It can also implement functions from two to 18 lines wide in a single block, offering significant delay-time advantages over architectures that have to implement wide functions in a series of logic levels (see related story, on reverse side).

Unlike FPGAs, the design of the routing resources and the architecture of the circuit blocks makes the timing characteristics of these devices pre-

8



dictable-or "deterministic," to use the industry term-along with those of Altera and Plus Logic. Precise timing can be predicted from data sheets. This differs from the timing of the true FPGAs of Xilinx and Actel, for which the data sheet can give only statistical estimates of actual post-route timing.

Meets requirements

Lattice is coming to market with up to 8,000 equivalent gates soon after Xilinx forecasted 20,000 gates and Toshiba projected 40,000 gates for next year. But Lattice's complexity meets the current requirements of most customers for FPGAs and even gate arrays. As for the future path for the new architecture, "we plan to expand to include mask versions of these devices for high-volume designs," said Steve Donovan, director of marketing at Lattice. "And current product plans call for densities exceeding 20,000 gates. We will introduce these devices as market conditions warrant."

Lattice specifies its pLSI devices to

work at system clock rates up to at least 70 MHz. That's for a single circuit block operating through an input and output circuit. The delay time for such a function is 15 ns.

Lattice claims the circuit modules, called generic logic blocks, can implement 90 percent of all 4-bit MSI functions. The proprietary routing network provides global interconnectivity, 100 percent routability and over 80 percent device utilization.

The new Lattice products encompass eight devices, four of which offer in-system programming. The pinout count ranges from 44 to 120. The number of I/Os range from 32 to 104.

The ispLSI types are programmed, reprogrammed, and reconfigured for test without having to be removed from the circuit board. Real-time prototyping and debugging, and reconfiguring or upgrading the system in the field, are possible. With the E²PROM programming technology, the devices are guaranteed to deliver 100 percent

programming yields and 100 percent conformation to functional, ac and dc specifications.

Same process

The 0.8-micron process that is used to fabricate these devices is developed and maintained by Lattice engineers. The UltraMOSIV process is the same used in the 7.5-ns and 10-ns GAL devices now in production at Lattice.

The first pLSI devices will begin shipping in the third quarter of this year. The in-system programming ispLSI versions will come a quarter later. Software and programming support will accompany the first product shipments.

Beta testing of the new pLSI devices will begin next month. Engineering samples will be generally available by October. The general market release of software and silicon will come in November. The price of the 6,000-gate device with 192 registers in an 84-pin PLCC will be \$98.50 each in lots of 100.

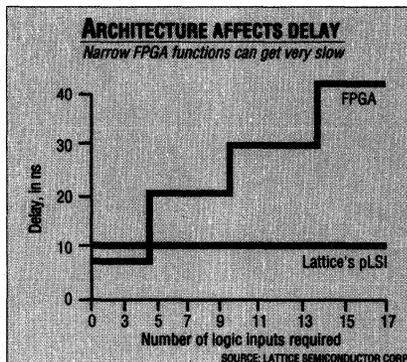
Lattice aims at best of architectural worlds

FPGA architectures generally implement gating functions up to four or five lines wide. Wider functions are then implemented using a series of such narrow functions. But every level of logic costs more delay time. Wider functions also can cost silicon area and waste circuitry where the width is not needed.

Lattice Semiconductor is trying to offer the best of both worlds with logic blocks that can handle widths up to 18 signals, but do so in logic arrays within the blocks that can be used for several narrow-width functions when the wide ones are not needed.

However, the company's research shows the most popular widths for gating functions are from eight to 12 lines. The current FPGA and other complex PLD devices offer less width than what is most needed, requiring two or three logic levels and,

consequently, two or three circuit delays. The accompanying figure, developed by Lattice engineers, shows the pLSI devices with a 10-ns delay per block not changing its delay from two through 18 inputs.



But a competing FPGA with five-input blocks starts at 8 ns, but adds another 8 ns each time the width expands by five inputs. For the most popular widths, from eight to 12, the competing FPGAs will have block delays of 20 ns to 30 ns. The delays are in 10-ns increments because of interconnect delays beyond the 8-ns delay in each block.

For wide gating applications, such as large counters, wide address decoding and multiplexing, the system speed slows considerably in current FPGAs because of the the need to cascade the logic block outputs.

—Stan Baker

BASIC TECHNIQUES LET DESIGNERS
BUILD A FINITE-IMPULSE-RESPONSE
FILTER IN DEDICATED HARWARE
USING PROGRAMMABLE LOGIC.

LEARN THE FUNDAMENTALS OF DIGITAL FILTER DESIGN

Historically, designers often have taken an analog approach to filtering. Filters were constructed using operational amplifiers, resistors, and capacitors. One op amp could implement a second-order filter, and higher-order filters could be implemented by cascading second-order filters. However, passive components with tolerances of 1% or better are necessary for the filter to have reproducible characteristics. And the filter is typically fine-tuned by trial-and-error substitution of available component values. In addition, operational amplifiers with a high gain-bandwidth product may be needed to keep undesirable phase shift to a minimum or keep a closed-loop system stable. These factors are among the many problems in real-world implementations of filters.

With the advances made in digital-signal processing, however, digital filters are becoming a more attractive design alternative to traditional analog techniques. Because digital-system information is in digital form, filtering can be accomplished relatively easily by passing the data through a filter algorithm. In addition, digital filters have the advantages of no filter-characteristic drift over time, temperature, or voltage. And they can easily be designed to filter low-frequency signals. Moreover, the filter response can be made to closely approximate the ideal response, and linear phase characteristics are possible.

There are many well established methods of determining the filtering algorithm. Basically, the designer establishes the desired filter characteristics, thereby yielding a filter transfer function. The continuous-time transfer function is then transformed to the equivalent linear discrete-time-difference function. This function in the Z domain has the general form of:

$$G(Z) = (A_0 + A_1Z^{-1} + A_2Z^{-2} + \dots + A_nZ^{-n}) / (1 + B_1Z^{-1} + B_2Z^{-2} + \dots + B_mZ^{-m}) = Y(Z)/X(Z)$$

The equation is referred to as the pulse transfer function. It's actually the Z transform of the continuous-time filter's unit impulse response. Conversely, the inverse Z transform of the pulse transfer function yields the impulse response of the filter.

The coefficients A_n and B_m determine the response of the digital filter. Changing

MIKE TRAPP

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DESIGN APPLICATIONS

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the coefficients changes the response of the filter. The terms Z^{-n} and Z^{-m} represent sampling delays or taps. The $G(Z)$ equation represents the algorithm of sampling the input, multiplying it by A_0 , and adding it to the previous sample that's been multiplied by A_1 , then adding that value to the next previous sample which has been multiplied by A_2 , and so on. An output value occurs when all N values have been multiplied and accumulated.

In parallel, each output value is stored, multiplied by B_1 , then added to the previous output value which has been multiplied B_2 , and so on. The equation can be rearranged so that the result of the output multiply accumulate is added to the result of the input multiply accumulate to produce an output. This procedure is referred to as convolution. An output sample is produced for every input sample (Fig. 1).

The key to digital-filter design is to determine the filter coefficients that will produce the desired frequency response. Recursive digital filters, or infinite-impulse-responsive (IIR) filters, are a type of digital filter in which the design methodology closely follows that of an analog filter. One method for determining the coefficients is to define a realizable

continuous-time domain Chebyshev, Butterworth, or equal-ripple filter then use Z transforms to transform the continuous-time-domain transfer function to the equivalent discrete-time transfer function that yields the filter coefficients.

A second popular method is the bilinear transform. In this method, engineers first design an analog filter so that after it's transformed to a digital filter, the resulting filter meets a set of desired digital-filter specifications. This analog filter is then transformed to a digital filter via the bilinear transform from the S variable of the Laplace transform to the Z variable of the Z transform.

In a non-recursive digital filter or finite-impulse-response (FIR) filter, the output is computed using the present input X_n and the previous inputs $X_{n-1}, X_{n-2} \dots X_{n-N}$. This implies that the coefficients, B_m , are all 0, and there's no feedback from the output. Designing non-recursive digital filters (FIR) involves defining an ideal desired frequency response from which the ideal impulse response is computed. The ideal impulse response is truncated to a finite number of non-zero samples using a windowing function, which is judiciously chosen. A common windowing function is the Kaiser window function.

An interesting property of FIR filters is that if an FIR system has linear phase, then its frequency response is constrained to be zero at $f = 1/2T$, where T equals the sampling frequency if:

$$h[M - n] = h[n] \text{ and } M \text{ is odd. (} M = \text{truncation length of the window).}$$

This implies the M should be even when designing high-pass and band-stop filters. Or,

$$h[M - n] = -h[n] \text{ and } M \text{ is even.}$$

A second method is the Parks-McClellan method. In this approach, the filter order and the edges of the passbands and stopbands are fixed, and the impulse-response coefficients are varied systematically so that an equal-ripple behavior is achieved in each approximation band. With this approach, the filter order can't be specified in advance. Therefore, a cut and try procedure must be used to find the minimum filter order. The cut and try can be reduced by using a formula that predicts the filter order required to meet a given set of specifications.

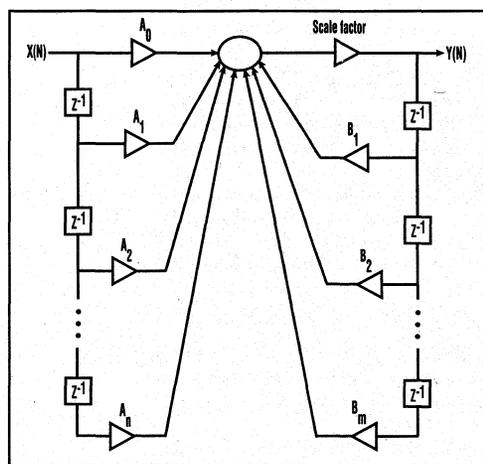
There are advantages and disadvantages to each type of digital filter (IIR and FIR). An FIR filter is always stable because there's no feedback from the output and the impulse response is finite. In addition, the amplitude and phase can be arbitrarily specified. On the other hand, an FIR filter will generally require more taps, and consequently more math, to compute the output value. The design methodology doesn't resemble the familiar analog design techniques.

An IIR will generally have fewer coefficients, but the required output feedback can make circuit implementation more complex. A stable IIR filter can become unstable if the coefficients aren't chosen properly to account for digital math errors.

There are four main types of errors that can arise in the design of digital filters. These are referred to as quantization errors. They are:

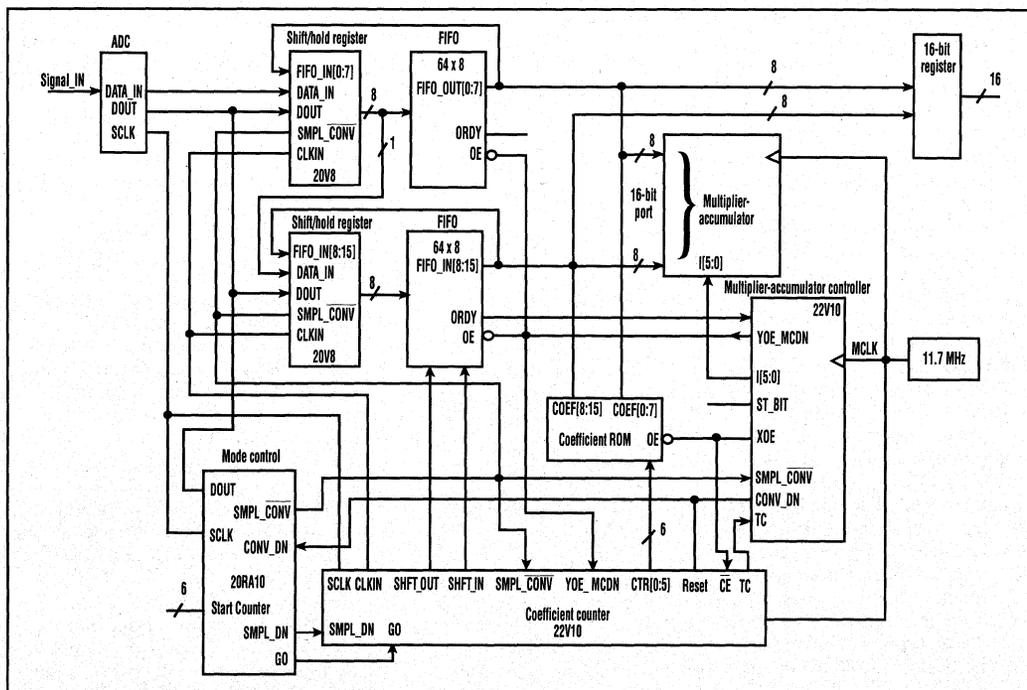
1. Quantization errors of the input analog-to-digital conversion
2. Quantization errors of the coefficients
3. Quantization errors due to arithmetic computations, including overflow
4. Limit cycles

In most cases, a 12-bit analog-to-digital converter (ADC) provides enough dynamic range and sufficiently small quantization noise. If floating-point numbers are used for the filter coefficients, the quantization error is usually small enough. However, floating-point arithmetic is more complex and more expensive



1. IN THE FUNCTIONAL structure of a digital filter, the A and B coefficients determine the response of the filter and the Z terms represent sampling delays called taps.

DESIGN APPLICATIONS
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2. AN FIR FILTER IS IMPLEMENTED in a circuit that uses a single-port 16-bit multiplier-accumulator capable of a 85-ns clock speed. Because it's based on microcode, the multiplier-accumulator can be controlled with a PLD.

to implement than integer or fixed-point arithmetic. If 12- or 16-bit coefficient are used, the quantization error is generally negligible.

In the digital domain, math is performed using finite precision binary arithmetic. All digital filters need to multiply a signal sample by a constant coefficient. Of course, multiplying 2 N-bit binary numbers results in a 2N-bit result, but digital systems are usually confined to a fixed number of bits with which to represent binary numbers. Therefore, it's necessary to round off the 2N-bit digital number back to N bits. If a 32-bit multiply accumulator is used and the final output is rounded to 16 bits, the arithmetic quantization errors can be minimized.

If overflow occurs during mathematical operations, the digital filter can behave in a nonlinear fashion and oscillations can occur. Twos-complement arithmetic can help eliminate overflow. In addition, a satu-

rating adder can be used. If the coefficients are less than one, then the resulting product will also be less than one. Scaling is used to force this condition. The coefficient can be scaled by a multiple of two so that the largest coefficient uses all available bits in the binary representation. The input is then scaled by the same amount.

The detail with which a digital filter can be described can seem endless. Fortunately, a wide variety of computer programs exist that help the engineer with the filter's design. One such product is the DFDP software from Atlanta Signal Processing Inc. (ASPI), Atlanta, Ga.

Before a signal can be digitally filtered it must be digitized by an ADC. If a delta-sigma converter is used, the need for antialiasing filters (which must be analog and can be many orders) is virtually eliminated. Delta-sigma converters may have sample rates as high as 100 kHz. The

filter algorithm can then be implemented in software or hardware.

A single-chip microprocessor can be used to implement a digital filter in software. However, "single chip" may be misleading, because a microprocessor system will generally require system RAM, ROM, I/O, and glue logic. The microprocessor can implement low- to medium-performance digital filters if the only function they're performing is the digital filtering. As the work load of the microprocessor increases, its capability to digitally filter a signal in real time decreases. Once the system is designed, changing the filter's characteristics is as easy as changing variables in software and downloading the code to the system.

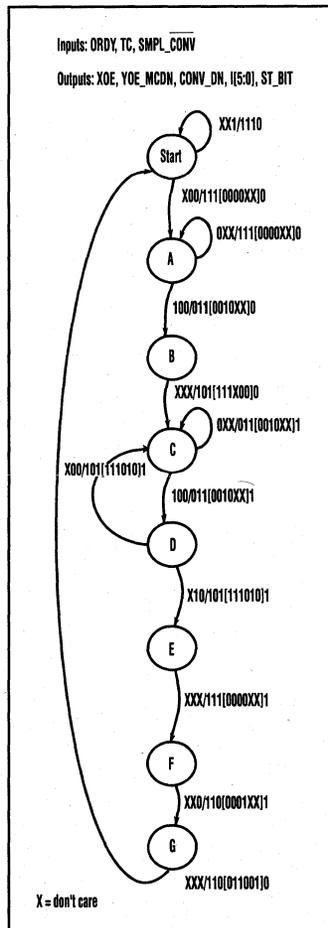
For higher performance and moderate flexibility, the filter can be implemented in dedicated hardware using programmable logic for design flexibility. The limiting parameter will be the time to do a multiply-accu-

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multimate function and the amount of physical space required for the hardware implementation of the taps. Consider a circuit that uses a single-port 16-bit multiplier-accumulator capable of an 85-ns clock speed (Fig. 2). The device can work in twos-compliment numbers and has output saturation capabilities. As stated before, these two features are desirable when implementing digital filters. In addition, the device can be easily controlled with a programmable logic device (PLD) because it's microcoded based.

First, the system must initially load the first N ($N = 64$) samples into the FIFO before any convolution takes place. Otherwise, the FIFO would never fill up. A counter implemented in a 20RA10 works well. The 6-bit counter is implemented with the four least-significant bits implemented as an asynchronous counter. $SMPL_DN$ (ADC sample done) acts as the clock. The two most-significant bits are implemented as a ripple counter. This type of counter design makes it possible for a long counter to be implemented with only four product terms per output. The $SMPL_DN$ signal is also generated in the 20RA10, and is triggered off signals from the ADC.

When the counter reaches the value 63, indicating that the FIFO is full minus the one sample that's held in the shift/hold register, GO becomes true and the system begins to execute the filtering algorithm. Because the system is linking two asynchronous subsystems (ADC and the multiplier-accumulator), there must be an asynchronous interface between the two. The 20RA10 is utilized by generating one interface signal $SMPL_CONV$ (sample or convolve mode). The system powers up with this line held in the sample mode ($SMPL_CONV = 1$). When GO goes true, synchronous with the falling edge of the clock from the ADC, $SMPL_CONV$ goes low asynchronously with $MCLK$ (synchronous with $SCLK$). Because $SMPL_CONV$ is an input to the state machine, the machine could be subject to a metastable input. The Lattice CMOS PLDs are very high



3. AN 8-STATE state machine implements the operations of loading a sample into the multiplier-accumulator, then loading the coefficients in and issuing the multiply-accumulate command until all N samples are done.

speed, so the metastable characteristics are excellent. That is, the state flip-flop has a very low probability of going metastable. Therefore, the state machine will have to wait, at most, one extra $MCLK$ cycle before starting the convolution.

Once the convolution is started, the operations of loading a sample into the multiplier-accumulator, then loading the coefficient into the

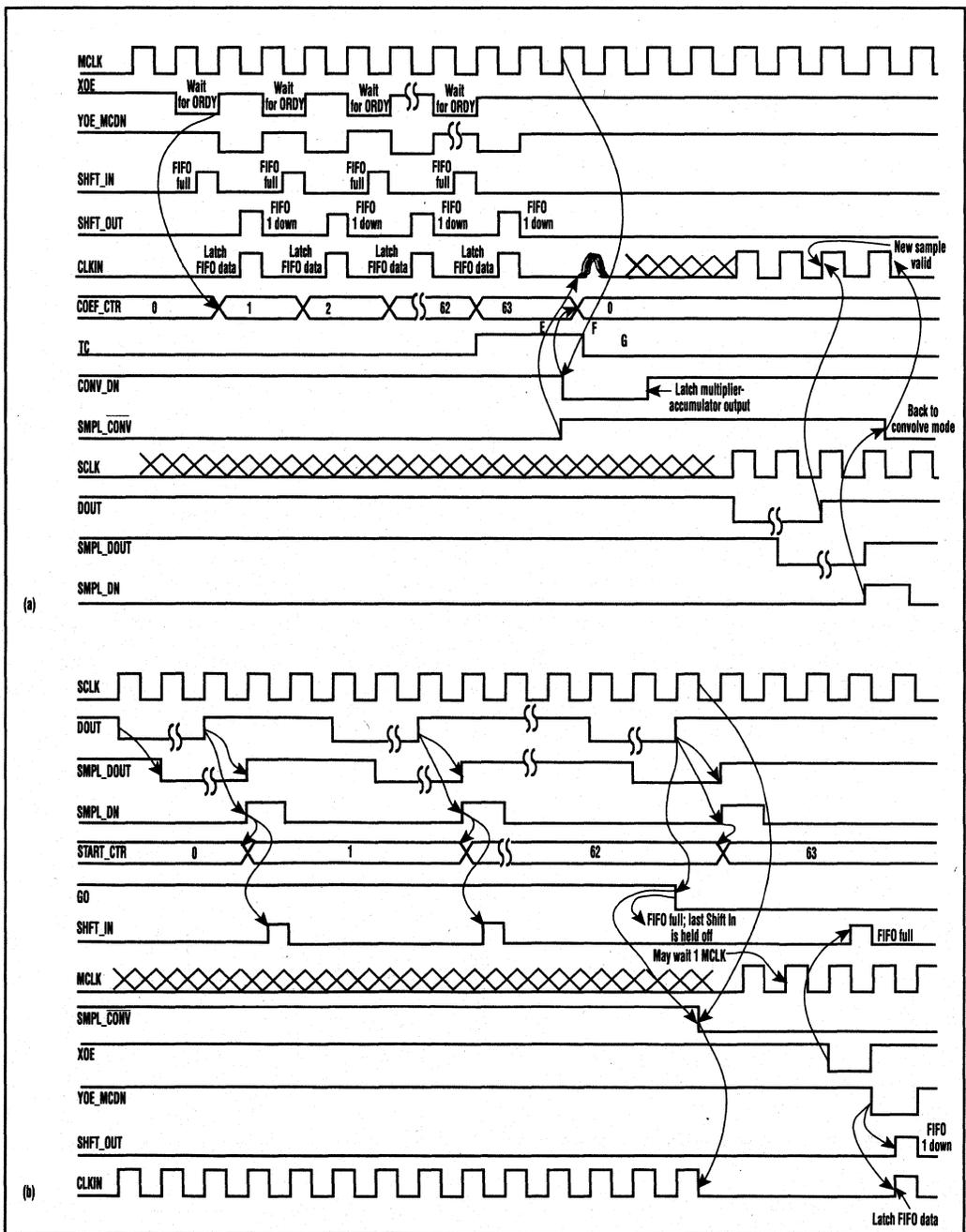
multiplier-accumulator and issuing the multiply-accumulate command, can be repeated until all N samples have been done. At this time, the filter output is valid and the cycle is restarted. These steps can be implemented with an 8-state state machine (multiplier-accumulator controller) (Fig. 3).

By coding the states properly, the state variables out of the state machine can be used to directly control the multiplier-accumulator. Two output enable signals, XOE and YOE_MCDN , control the data into the multiplier-accumulator. The signal $CONV_DN$ indicates that all N samples have been convolved. A dummy state variable (ST_BIT) is used so that the state bit (XOE , YOE_MCDN , $CONV_DN$) can be employed as outputs. If the dummy bit was unused, two states would be forced to have the same state assignments, which isn't allowed. The design takes advantage of the power-up reset of Lattice's programmable logic devices (PLD s). After power-up, the registers will be left in the 0 state, which by careful design is also the start state of the state machine.

Except for the last $SMPL_DN$ during initial load, every time $SMPL_DN$ (sample done by the ADC) takes place, $SHFT_IN$ occurs to load sampled data from the shift/hold registers into the FIFO. During convolution, XOE occurs every time a coefficient is loaded to the multiplier-accumulator. The first XOE of a convolution causes the last data sample left in the shift/hold registers during initial load or sample mode to be shifted into the FIFO. Following every XOE is a YOE_MCDN (Y-output enable, multiply-accumulate done). YOE_MCDN causes data from the FIFO's output to be parallel loaded into the shift/hold registers. A single data sample is then shifted out of the FIFO. The system is ready for the next XOE that shifts in the data held in the shift/hold registers and so on. This loop continues until $SMPL_CONV$ (sample or convolve mode) goes to sample mode, at which time a new sample is loaded into the shift register, restarting the cycle.

Inputs to the state machine,

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4. FIFO CONTROL SIGNALS are generated asynchronously. The system timing diagrams for the convolve (a) and initial load (b) operations show the appropriate Shift In and Shift Out signals, and clock signals sent to the shift/hold register.

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SMPL_CONV, tell the machine when it's time to begin the convolution cycle. This signal comes from the mode-control device. TC (Terminal Count) indicates when the convolution is to end. TC comes from a 6-bit coefficient counter, and is valid when the count equals 63, which indicates when all 64 samples have been convolved with the respective coefficients. ORDY comes from the FIFO and tells the state machine that the sample from the FIFO is valid. The state machine will continue to load in the coefficient to the multiplier-accumulator until ORDY goes true, at which time the state machine will advance to the next state. If the cycle time of the multiplier-accumulator never exceeds the access time of the FIFO, ORDY should always be true when it's an input the state machine depends on.

Microcoded instructions to the multiplier-accumulator are generated by decoding the state variables. The first instruction is a NOOP. When SMPL_CONV goes low, then state machine issues a XBUS instruction to the multiplier-accumulator. This causes the multiplier-accumulator to load data from the I/O port into an internal register. The state machine then issues a YBUS;

CLKMR TC. This command tells the multiplier-accumulator to perform a multiply operation in twos-complement without accumulation because it's the first multiply operation of the convolution.

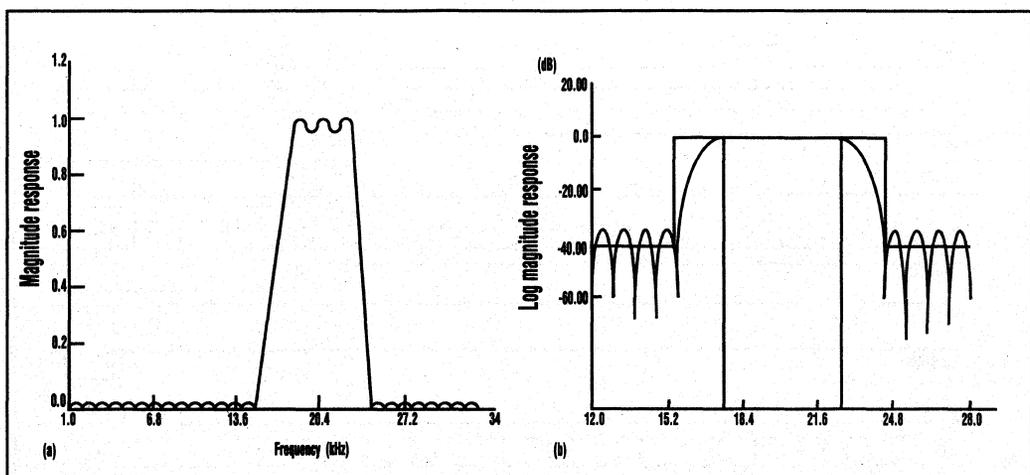
The machine then enters a loop and issues another XBUS command followed by a YBUS; CLMR; TC; MR+. This command is a multiply-accumulate function in twos-complement arithmetic. The machine remains in this loop until TC goes true, at which time the last multiplier-accumulator cycle is completed and the output command MS (SAT) is issued. MS causes the filter's outputs (multiplier-accumulator outputs) to become valid and latched into a final output register. This command will saturate the multiplier-accumulator output if the final value has an overflow, keeping the digital filter from oscillating. The multiplier-accumulator is statically configured to round off the final output to the most significant 16 bits.

The instructions to the multiplier-accumulator can be changed simply by decoding the state variables to different output values. If E²CMOS devices are used, the programmable device can simply be reprogrammed and put back into the circuit. An E²C-

MOS 22V10 from Lattice Semiconductor is one such device that can be used for this application.

Two 64-word-by-8-bit FIFOs can be used to implement the filter taps. The FIFO can be loaded up with the initial N samples. A sample is then shifted out of the FIFO and into the multiplier-accumulator for processing. This sample is also stored in a shift/hold register and is shifted back into the FIFO prior to the next sample being shifted into the multiplier-accumulator for processing. After all N samples have been processed, the oldest sample is shifted out and a new ADC sample shifted in. The multiplier-accumulator can then output a filter value. Programmable logic can be used to interface the digital filter to the ADC, act as temporary storage register, and implement FIFO control.

These shift/hold registers can be implemented with two 20V8 devices. In the sample mode (SMPL_CONV = 1), the devices act as shift registers. Data is serially loaded into them under control of the ADC. The registers are then placed in a hold mode so that the data sample isn't lost. When the system enters the convolve mode, (SMPL_CON = 0), data is immediately loaded into the



5.-A PLOT OF THE MAGNITUDE response shows that the bandpass filter's center frequency is 20 kHz with a passband of 5 kHz (a). The transition region occurred in 2 kHz. The log magnitude response plot reveals a 175-dB/decade slope at the edges of the filter (b). It would take a 9th-order analog filter to implement the same specifications.

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shift/hold registers in parallel.

Filter coefficients are stored in PLDs emulating ROM. A 6001 has a programmable AND and a programmable OR array so that it easily emulates a 64-by-8 high-speed PROM. Again, if E² devices are used, the filter coefficients can be changed simply by reprogramming the devices. An address counter is used to access the coefficients in the correct order. Because there are 64 required coefficients for the 64 taps, only 6 bits of address are required.

The coefficient-address counter is a simple 6-bit counter implemented in a 22V10. The counter is a synchronous type with a count enable. The clock is synchronous with the multiplier-accumulator clock. The count-enable input pin is connected to XOE from the multiplier-accumulator controller. Therefore, the counter is incremented only after the coefficient value has been loaded into the multiplier-accumulator. When the counter reaches 63, TC goes true to indicate that all 64 coefficients have been convolved. Again, the power-up reset is used to ensure that the counter starts in a known state.

The remaining four output-logic macro cells can be used to generate FIFO control signals. These signals are generated asynchronously. Depending on the state of the system—whether it be initially loading, sampling, or convolving—the appropriate Shift In, Shift Out, and clock signals for the shift/hold register will be generated (Fig. 4).

When the convolution is done, the state machine sets the CONV_DN signal true synchronous with MCLK. Hence, SMPL_CONV will also be set synchronous with MCLK. This will create glitches on the signal CLKIN, which is the clock to the shift/hold registers. This is a don't-care condition, as the registers will soon be loaded with a new valid data sample under the control of the ADC.

The system requires 133 MCLK cycles to complete the convolution. With a 11.7-MHz clock, this takes 11.4 μ s. This system used an ADC with a serial interface that requires 3.3 μ s to shift the data into the shift/

hold registers. Thus, the system can sample an input signal at $11.4 + 3.3 = 14.7 \mu$ s or 68 kHz. The Nyquist sampling theorem states that a signal must be sampled at twice the highest frequency component to accurately preserve the information in that signal. Therefore, this system can accurately filter a signal with the frequency component as high as 34 kHz.

Using the DFDP software from ASPI, a bandpass filter was designed using the Parks-McClellan method. The center frequency is at 20 kHz with a passband of 5 kHz. The transition region occurred in 2 kHz (Fig. 5). It's interesting to note that the edges of the filter have a slope of approximately 35 dB/0.2 decade, or 175 dB/decade. It would take a 9th-order analog filter to implement the same specifications.

The system presented in this example is a straightforward FIR filter. Because of the extensive use of programmable logic, the system can be easily adapted to implement an IIR filter. The final output value can be fed back into the FIFO prior to a new sample shifting into the FIFO. The coefficients can be staggered in the coefficient ROM so that the B_ms line up with the Y(n - M), and the A_ns line up with the X(n - N).

If enhancement of the system's performance is desired, a larger FIFO memory can be used with a faster multiplier-accumulator. Because 15-ns programmable-logic devices are used, they're not a limiting factor. If a parallel ADC, 64-by-8 FIFO, and a 45-ns multiplier-accumulator are employed, the system could be made to run at 167 kHz with little modification. □

The author would like to thank Atlanta Signal Processing for their help in developing this article.

Mike Trapp, an applications engineer for Lattice Semiconductor, holds a BSEE from the University of Colorado, Boulder.

Multiclock GAL doubles clock rate

Ted Marena

Lattice Semiconductor, Burlington, MA

Fig 1 shows a block diagram of a 386SX μ P system. The 386SX runs at 20 MHz. However, the memory circuitry needs to run at 40 MHz. The PLD program in Listing 1 sets up the multiple clocks in the GAL20RA10 to strobe on both the rising and falling edges of the μ P's clock, effectively synthesizing a 40-MHz clock for the memory circuitry.

The program also sets up the PLD to develop the DRAM's critical RAS and CAS signals according to the timing diagram in Fig 2. Note that CAS follows RAS by 25 nsec, meeting the 20-nsec minimum interval for 70-nsec DRAM. A 2-bit counter in the PLD satisfies RAS-precharge timing specs: RAS must be low for at least 70 nsec, high for at least 50 nsec, and go high only after CAS goes low. In this design, RAS goes low for 70 nsec and high for 60 nsec.

Note that because an EPROM's chip-select line does not have to be clocked, the program in the listing develops the EPROM-select signal using combinatorial logic. You can obtain the listing from the EDN BBS's DI Special Interest Group (617-558-4241, 300/1200/2400, 8, N, 1—from Main Menu, enter (s)ig, <s/di_sig>, rk1028).

EDN

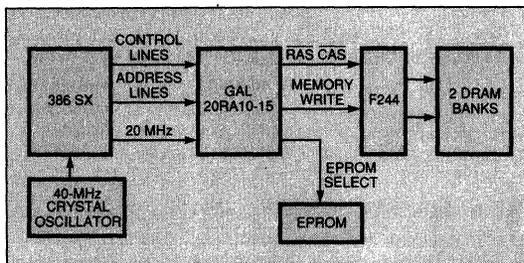


Fig 1—The PLD's internal circuitry can clock on both edges of the μ P's clock, thereby synthesizing a 40-MHz clock for the memory system.

Listing 1—Memory-control PLD program

```

Name GAL20ra10;
Partno meminterface;
Revision 02;
Date 3/7/91;
Designer Ted Marena;
Company Lattice Semiconductor;
Assembly PC Multi-Function;
Location U12;
Device g20ra10;

/******
/* This device controls the memory interface to a dram and eprom.
/* A 386sx cpu with 1 meg of dram and eprom placed above 1 meg
/* of address space.
/******
/* Allowable Target device Types:GAL20RA10
/******

/** Inputs **/

pin 2 = m_io; /* memory or I/O select */
pin 3 = !bhe; /*
pin 4 = !ble; /*
pin 5 = !refresh; /* control signals from the cpu
pin 6 = !ready; /*
pin 7 = a22; /*
pin 8 = a21; /* address bits to decode above
pin 9 = a20; /* and below 1 meg
pin 10 = wr_rd; /* write or read control from cpu
pin 11 = 20mclk; /* 20 mhz clock from the cpu

/** Outputs **/

pin 14 = !cas; /* cas for both banks of dram
pin 15 = !rasl; /* rasl to strobe low bank
pin 16 = !ras2; /* ras2 to strobe high bank
pin 17 = !apromsel; /* eprom select
pin 18 = !intras1; /* these 2 bits control the
pin 19 = !intras2; /* width of the ras pulse
pin 20 = !dramwr; /* write pulse for the dram

/** Declarations and Intermediate Variable Definitions **/

intras1.ck = 20mclk;
intras2.ck = !20mclk;
ras1.ck = 20mclk; /* both ras are clocked on one clk edge
ras2.ck = !20mclk; /* and cas is clocked on the other
cas.ck = !20mclk;

ras1.d = m_io & !ble & !refresh & !a20 & !a21 & !a22; /* start ras1 */
refresh & cas; /* cas before ras refresh
*/
ras2.d = m_io & !bhe & !refresh & !a20 & !a21 & !a22; /* start ras2 */
refresh & cas; /* cas before ras refresh
*/
cas.d = (ras1 & ras2) & !refresh; /* hold end cas
refresh & !a20 & !a21 & !a22 & !m_io; /* refresh cycle
*/
memwr = m_io & !refresh & wr_rd; /* write for memory */
epromsel = m_io & !refresh & a20 & a21 & a22 & ads & !wr_rd;
intras1.d = ras1 & ras2; /* cas before ras starts
*/
intras2.d = intras1; /* count 2 clocks to end ras
*/

ras1.ar = intras2; /* end ras1 by asynchronous reset
*/
ras2.ar = intras2; /* end ras2 by asynchronous reset
*/
intras2.op = !intras1; /* asynchronous preset to allow ras
*/
to begin next timing cycle

```

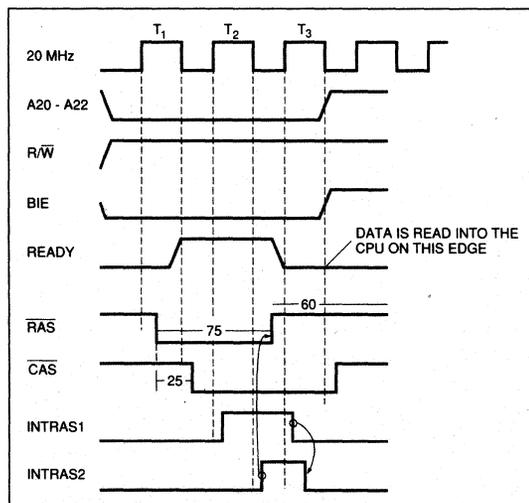


Fig 2—By generating internal clocks, intras1 and intras2, from both edges of the 20-MHz clock signal, the PLD effectively doubles the clock rate.

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: pLSI and ispLSI Products

Section 5: GAL Quality and Reliability

Section 6: GAL Technical Notes

Section 7: GAL Application Briefs

Section 8: Article Reprints

Section 9: General Information

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GAL Development Tools

Lattice Semiconductor recommends that customers use only Lattice qualified programming equipment. Lattice guarantees 100% programming yield to customers using qualified programming tools. Below is a matrix that provides the third-party programmers which are qualified to program Lattice GAL devices.

Lattice works closely with third-party programming equipment manufacturers to ensure that customers

achieve the highest programming yields and quality levels. Lattice's stringent qualification program includes an evaluation of algorithms, verification of timing and voltage levels, and a complete yield analysis.

For a current listing of Lattice qualified GAL programmers, please call Lattice's Literature Distribution Department (Tel: 503-693-0287; FAX: 503-681-3037).

LATTICE QUALIFIED PROGRAMMERS (as of May 1992)

Vendor	Programmer	Lattice GAL Device Type									
		16V8A/B	20V8A/B	18V10	22V10/B	26CV12B	26CV12	20XV10	20RA10	6002B	6001
Data I/O	Unisite	■	■	■	■	■	■	■	■	■	■
	3900	■	■	■	■	■	■	■	■	■	■
	2900	■	■	■	■	■	■	■	■	■	■
	29B	■	■	■	■	■	■	■	■	■	■
	60A/H	■	■	■	■	■	■	■	■	□	■
Logical Devices	Allpro 88	■	■	■	■	■	■	■	■	■	■
	Allpro 40	■	■	■	■	■	■	■	■	■	■
Stag	System 3000	■	■	■	■	□	■	□	■	□	■
	ZL30/A	■	■	■	■	■	■	■	■	■	■
System General	TURPRO-1	■	■	■	■	■	■	■	■	■	■
	SGUP-85A	■	■	■	■	■	■	■	■	□	■
	SGUP-85	■	■	■	■	□	■	□	■	□	■
SMS Microcomputer	Sprint Expert	■	■	■	■	■	■	■	■	■	■
	Sprint Plus	■	■	■	■	■	■	■	■	□	■
Digelec	Model 860	■	■	■	■	○	○	■	■	□	■
BP-Microsystems	CP-1128 PLD-1128	■	■	■	■	■	■	■	■	■	■
	PLD-1100	■	■	■	■	○	○	■	■	■	■
Prog. Logic Tech.	Logic Lab	■	■	■	■	□	■	■	■	□	■
Advin	Pilot-U84/U40	■	■	■	■	■	■	■	■	■	■
	Pilot-GL/GCE	■	■	■	■	■	■	■	■	■	■

■ = Programmer is qualified, refer to the GAL Development Tools document for additional information.

□ = Programmer was not qualified as of 5/92. Contact Lattice or programmer vendor for latest information.

○ = Programmer does not support 28-pin devices.

Development Tools

LOGIC COMPILER SUPPORT (as of May 1992)

Vendor	Logic Compiler	Lattice GAL Device Type								
		16V8A/B	20V8A/B	18V10	22V10/B	26CV12/B	20XV10B	20RA10	6002B	6001
Accel Tech.	Tango PLD	■	■	■	■	■	○	■	○	■
Data I/O	ABEL	■	■	■	■	■	■	■	■	■
ISDATA	LOG/IC	■	■	■	■	■	○	■	○	■
Logical Devices	CUPL	■	■	■	■	■	■	■	■	■
Minc	PLDesigner	■	■	■	■	■	○	■	○	■
OrCAD	OrCAD PLD	■	■	■	■	■	○	■	○	○
Omaton	Schema-PLD	■	■	■	■	■	○	■	○	■

■ = Compiler supports GAL device type. Contact vendor or Lattice for the current revision level.
 ○ = Contact vendor for support date.

PROGRAMMER/COMPILER VENDORS

Accel Technologies
 6825 Flanders Dr.
 San Diego, CA 92121
 Tel: (619) 554-1000
 FAX: (619) 554-1019

Advin Systems
 1050-L Duane Ave
 Sunnyvale, CA 94086
 Tel: (408) 243-7000
 FAX: (408) 736-2503

BP Microsystems
 10681 Haddington
 Suite #190
 Houston, TX 77043
 Tel: (713) 461-9430
 FAX: (713) 461-7431
 BBS: (713) 461-4958

Data I/O Corp.
 10525 Willows Road N.E.
 P.O. Box 97046
 Redmond, WA 98073-9746
 Tel: (206) 881-6444
 Tel: 1-800-247-5700
 FAX: (206) 882-1043
 In Europe contact:
 Data I/O Corp.
 Tel: +31 (0) 20-6622866
 In Japan contact:
 Data I/O Corp.
 Tel: (03) 432-6991

Digitronics Israel Ltd.
 25 Galgaley Haplada St.
 Herzliya B 46722
 Israel
 Tel: 052-559615
 FAX: 052-555240
 In the U.S. contact
 Digelec
 20144 Plummer St.
 Chatsworth, CA 91311
 Tel: (818) 701-9677
 FAX: (818) 701-5040

ISDATA GmbH
 Haid-und-Neu-Straße 7
 7500 Karlsruhe 1
 Germany
 Tel: 0721-693092
 FAX: 0721-174263
 In the U.S. contact
 ISDATA Inc.
 Tel: (408) 373-7359
 FAX: (408) 373-3622

Logical Devices
 1321 N.W. 65th Place.
 Fort Lauderdale, FL 33309
 Tel: (305) 974-0967
 FAX: (305) 974-8531

Minc Incorporated
 6755 Earl Dr.
 Colorado Springs, CO 80918
 Tel: (719) 590-1155
 FAX: (719) 590-7330

Omaton
 801 Presidential
 Richardson, TX 75081
 Tel: (214) 231-5167
 FAX: (214) 783-9072

OrCAD Systems Corp.
 3175 N.W. Aloclek Dr.
 Hillsboro, OR 97124
 Tel: (503) 690-9881
 FAX: (503) 690-9891

Programmable Logic Tech
 P.O. Box 1567
 Longmont, CO 80501
 Tel: (303) 772-9059
 FAX: (303) 772-5617

SMS Micro Systems
 IM Grund 15
 D-7988 Wangen
 Germany
 Tel: (49) 7522-5018
 FAX: (49) 7522-8929
 In the U.S. contact:
 SMS North America, Inc.
 16522 N.E. 135th Pl.
 Redmond, WA 98052
 Tel: (206) 883-8447
 FAX: (206) 883-8601

Stag Microsystems
 Martinfield
 Welwyn Garden City
 Herts AL7 1JT
 United Kingdom
 Tel: 011-44-707-332148
 FAX: 011-44-707-371503
 In the U.S. contact:
 Stag Microsystems
 1600 Wyatt Dr.
 Santa Clara, CA 95054
 Tel: (408) 988-1118
 FAX: (408) 988-1232

System General
 3Fl., No. 1, Alley 8, Lane 45
 Bao Shing Rd.
 Shin Dian
 Taipei, Taiwan R.O.C.
 Tel: 886-2-9173005
 FAX: 886-2-9111283
 In the U.S. contact:
 System General
 510 S. Park Victoria Dr.
 Milpitas, CA 95035
 Tel: (408) 263-6667
 FAX: (408) 262-9220

Copying PAL, EPLD & PEEL Patterns Into GAL Devices

INTRODUCTION

The generic/universal architectures of Lattice GAL devices are able to emulate a wide variety of PAL, EPLD and PEEL devices. GAL devices are direct functional and parametric replacements for most PLD device architectures. To use GAL devices in place of other PLD types, some conversion of the original device pattern may be needed. This conversion is not difficult, and can be accomplished at either the design or manufacturing level. The following sections describe several techniques available to convert PAL, EPLD and PEEL device patterns to Lattice GAL device patterns.

CROSS PROGRAMMING: GAL16V8 AND GAL20V8

The GAL16V8 and GAL20V8 devices replace most standard 20-pin and 24-pin PAL devices. To simplify the conversion process, Lattice has worked with programmer hardware manufacturers to provide the ability to program GAL devices directly from existing PAL JEDEC files, or master PAL devices. Lattice qualified programmers can automatically configure the architecture of a GAL device to emulate the source PAL device.

To provide a conceptual framework for the conversion from PAL devices to GAL devices, a mythical device known as a RAL device was created. A RAL device is simply a GAL device configured to emulate a PAL. There is a one-to-one correspondence between the name of a PAL device and that of a RAL device. For example, a RAL16L8 is simply a GAL16L8 configured as a PAL16L8. Some programmers list the RAL device types as choices for cross-programming, while others specifically state that a cross-programming operation is to be performed using a PAL device type as the architecture type. Other programmers list devices such as a Lattice 16L8. Even though Lattice does not make a 16L8 device, choosing this selection allows the programmer to accept a 16L8 JEDEC file, and will program a GAL16V8 device to emulate a PAL16L8.

To program a GAL16V8 or GAL20V8 device from an existing PAL JEDEC file, simply select the appropriate device code (either RAL type, or PAL type to cross-program from), then download the PAL JEDEC file to the programmer. Insert the appropriate GAL device that can directly emulate the PAL device (according to the chart in the GAL16V8 or GAL20V8 datasheets). The programmer will automatically configure the GAL device to emulate the PAL device during programming. The resulting GAL device is 100% compatible with the original PAL device.

A GAL device may also be programmed from a master PAL device by reading the pattern of the master PAL into the programmer memory, then selecting the appropriate RAL device or PAL type to cross-program from. The GAL device can then be programmed from the programmer memory.

CROSS PROGRAMMING: GAL22V10/GAL20RA10

The GAL22V10 and GAL20RA10 are direct replacements for bipolar PAL devices, and are JEDEC fuse map compatible with these industry standard devices. To program a GAL22V10 or GAL20RA10 device from an existing PAL JEDEC file, simply select the appropriate GAL device code, then download the PAL JEDEC file to the programmer. The resulting GAL device is 100% compatible with the original PAL.

GAL devices also may be programmed from Master PAL devices by reading the pattern of the Master PAL into the programmer memory, then selecting the appropriate GAL device code. The GAL device can then be programmed from the programmer memory.

The GAL22V10 and GAL20RA10 also can store a User Electronic Signature (see the datasheets on these devices for more information). To use this feature, the JEDEC file must contain this information. To add the signature data to the JEDEC map, use the PALtoGAL conversion utility (see next section) or recompile the source equations for a Lattice GAL device instead of a generic 22V10 type. Many programmers list two device types to differentiate between the two types of JEDEC files, and list both a GAL22V10 and a name such as GAL22V10-UES or GAL22V10-ES. Other programmers allow both types of JEDEC files to be accepted, and simply don't program the Signature fuses if they are not present in the file.

CROSS PROGRAMMING: GAL20XV10

The GAL20XV10 can be configured as a direct replacement for bipolar PAL20X10, 20X8, 20X4, and 20L10 devices. Many programmers provide cross-programming support similar to that provided for the GAL16V8/GAL20V8 devices. This allows the use of existing PAL device files to program the GAL20XV10 to emulate the PAL devices. The PALtoGAL conversion software (described below) also supports conversion of the PAL JEDEC files to a functionally equivalent GAL device file.

PALTOGAL CONVERSION UTILITY SOFTWARE

Lattice has created a software utility that will convert an existing PAL device JEDEC file to the appropriate GAL

Copying PAL Patterns Into GAL Devices

device JEDEC format. Called PALtoGAL, this software utility can be used to convert PAL device files to GAL device files, add/or change the User Electronic Signature without changing device functionality, and reformat existing GAL JEDEC files for readability.

Since a few programmable logic devices have features that a GAL device cannot exactly emulate, the PALtoGAL utility will clearly describe the incompatibility but will not create an output file. GAL devices programmed using files converted by PALtoGAL will be 100% compatible with the original logic device. PALtoGAL is just another method of cross-programming, and should produce the same results as using a programmer. The advantage is that a full GAL device JEDEC map is created, meaning that the appropriate GAL device may then be selected on the programmer, which may simplify the manufacturing flow. Also, the PALtoGAL conversion software provides conversions that programmers do not.

A copy of the PALtoGAL conversion utility software can be obtained through your local Lattice representative, or by

contacting the GAL Applications Hotline at 1-800-FASTGAL (327-8425) or (503) 693-0201. The software also may be downloaded from Lattice's Electronic Bulletin Board at (503) 693-0215; the file name is "PALTOGAL.EXE".

SOFTWARE COMPILER CONVERSION

If the equation source file is available for the PAL device, it can be converted by re-compiling using a suitable logic compiler that supports GAL devices. If there are any device incompatibilities (there shouldn't be in most cases), the compiler will describe the errors. The output of the compiler will be a GAL JEDEC file that can be used to program a GAL device directly. The resulting GAL device will be 100% functionally compatible with the original device.

Suitable logic compilers are listed in the Development Tools section. If additional questions arise, contact your compiler manufacturer or a Lattice Applications Engineer by calling the GAL Applications Hotline at 1-800-FASTGAL or (503) 693-0201.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #	MANUFACTURER	PART #	LATTICE PART #	
ALTERA	EP310 EP320 EP330	GAL16V8A/B' or... GAL18V10	AMD	AmPAL20RP10	GAL22V10/B	
AMD	PAL10H8 PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8A/B		PAL20S10 PAL20RS4 PAL20RS8 PAL20RS10	GAL22V10/B	
	PAL16L8 PAL16R4 PAL16R6 PAL16R8 PALC16L8 PALC16R4 PALC16R6 PALC16R8 AmPAL16L8 AmPAL16R4 AmPAL16R6 AmPAL16R8 PAL16P8 PAL16RP4 PAL16RP6 PAL16RP8	GAL16V8A/B		PAL12L10 AmPAL20L10 PAL20L10 PAL20X4 ² PAL20X8 ² PAL20X10 ²	GAL20XV10B	
	PALCE16V8	GAL16V8A/B		AmPAL22V10 PAL22V10 PALC22V10 PALCE22V10	GAL22V10/B	
	AmPAL18P8 PALC18U8	GAL16V8A/B' or... GAL18V10		PALCE24V10 PALCE26V12	GAL26CV12/B ¹	
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8A/B		ATMEL	AT22V10	GAL22V10/B
	PAL20L8 PAL20R4 PAL20R6 PAL20R8 AmPAL20RP4 AmPAL20RP6 AmPAL20RP8	GAL20V8A/B		CYPRESS	PALC16L8 PALC16R4 PALC16R6 PALC16R8	GAL16V8A/B
	PALCE20V8	GAL20V8A/B			PLDC18G8	GAL16V8A/B' or... GAL18V10
	PAL20RA10	GAL20RA10			PALC20CG10 PALC22V10 PAL22V10	GAL20V8A/B' or... GAL22V10/B
					PLD20RA10	GAL20RA10
		HARRIS	HPL16LC8 HPL16RC4 HPL16RC6 HPL16RC8	GAL16V8A/B		
		ICT	PEEL18CV8	GAL16V8A/B' or... GAL18V10		
			PEEL153 PEEL253	GAL16V8A/B' or... GAL18V10 ¹		
			PEEL20CG10 PEEL22CV10A	GAL20V8A/B' or... GAL22V10/B		

- 1) Possible conversion but not 100% compatible to this device.
2) DIP package compatible only.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #
INTEL	5C031 5C032 85C220	GAL16V8A/B' or... GAL18V10
	85C224	GAL20V8A/B' or... GAL22V10/B
NATIONAL	PAL10H8	GAL16V8A/B
	PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8A/B
	PAL16L8 PAL16R4 PAL16R6 PAL16R8	GAL16V8A/B
	GAL16V8 GAL16V8A	GAL16V8A/B
	GAL18V10	GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8A/B
	PAL20L8 PAL20P8 PAL20R4 PAL20RP4 PAL20R6 PAL20RP6 PAL20R8 PAL20RP8	GAL20V8A/B
	PAL20RA10	GAL20RA10
	PAL20L10 PAL20X4 PAL20X8 PAL20X10	GAL20XV10B
	GAL22V10	GAL22V10/B
	GAL26CV12	GAL26CV12/B
	GAL6001	GAL6001 or... GAL6002B

MANUFACTURER	PART #	LATTICE PART #
RICOH	EPL10P8 EPL12P6 EPL14P4 EPL16P2	GAL16V8A/B
	EPL16P8 EPL16RP4 EPL16RP6 EPL16RP8	GAL16V8A/B
SAMSUNG	CPL16L8 CPL16R4 CPL16R6 CPL16R8	GAL16V8A/B
	CPL20L8 CPL20R4 CPL20R6 CPL20R8	GAL20V8A/B
	CPL20L10	GAL20XV10B
	CPL22V10	GAL22V10/B
SGS-THOMSON	GAL16V8	GAL16V8A/B
	GAL20V8	GAL20V8A/B
	GAL39V18	GAL6001 or... GAL6002B
SIGNETICS	PLHS16L8 PLUS16L8 PLUS16R4 PLUS16R6 PLUS16R8	GAL16V8A/B
	PLHS18P8	GAL16V8A/B' or... GAL18V10
	PLS153 PHD16N8	GAL16V8A/B' or... GAL18V10'
	PLUS20L8 PLUS20R4 PLUS20R6 PLUS20R8	GAL20V8A/B
SPRAGUE	SPL14LC8 SPL16LC8 SPL16RC4 SPL16RC6 SPL16RC8	GAL16V8A/B

1) Possible conversion but not 100% compatible to this device.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #
SPRAGUE	SPL18LC4 SPL20LC2	GAL20V8A/B
	SPL20LC8 SPL20RC4 SPL20RC6 SPL20RC8	GAL20V8A/B
TI	TIBPAL16L8 TIBPAL16R4 TIBPAL16R6 TIBPAL16R8	GAL16V8A/B
	TICPAL16L8 TICPAL16R4 TICPAL16R6 TICPAL16R8	GAL16V8A/B GAL16V8A/B
	EP330 TIBPAD16N8	GAL16V8A/B ¹ or... GAL18V10 ¹
	TIBPAL20L8 TIBPAL20R4 TIBPAL20R6 TIBPAL20R8	GAL20V8A/B
	TIBPAL20L10 TIBPAL20X4 TIBPAL20X8 TIBPAL20X10	GAL20XV10B
	TIBPAL22V10 TICPAL22V10	GAL22V10/B

1) Possible conversion but not 100% compatible to this device.

Package Thermal Resistance

The following table provides information on the package thermal resistance of Lattice commercial and industrial grade devices. For information on the package thermal resistance of Lattice military grade devices, please refer to "MIL-M-38510, Appendix C".

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages" with devices

mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages".

Test Conditions

Power Dissipation = 0.5watts (IC chip reverse biased)
 Ambient Air Velocity = Zero (still air)
 Ambient Temperature = 65°C
 Measuring Current = 3mA

PACKAGE THERMAL RESISTANCE

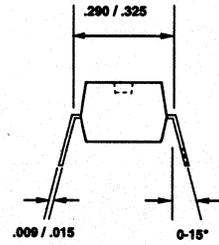
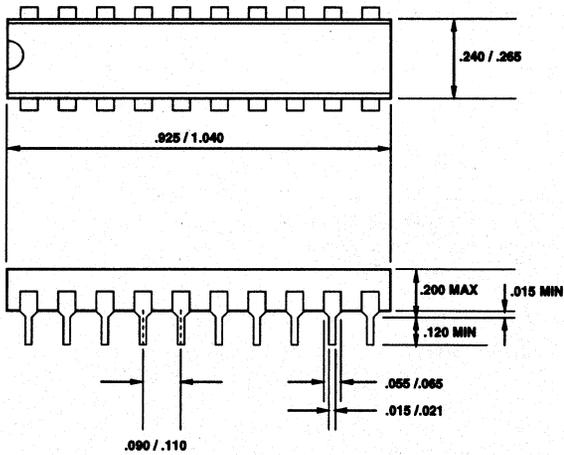
Commercial/Industrial Grade Devices

Package Type:	Device Type:	θ_{JA}	θ_{JC}
20-Pin Plastic DIP	GAL16V8A/B GAL18V10	67°C/W	39°C/W
24-Pin Plastic DIP	GAL20V8A/B GAL22V10/B GAL20XV10B GAL20RA10 GAL6001 GAL6002B	65°C/W	36°C/W
28-Pin Plastic DIP	GAL26CV12/B	52°C/W	33°C/W
20-Pin Plastic LCC	GAL16V8A/B GAL18V10	67°C/W	32°C/W
28-Pin Plastic LCC	GAL20V8A/B GAL22V10/B GAL20XV10B GAL20RA10 GAL26CV12/B GAL6001 GAL6002B	56°C/W	29°C/W

Package Diagrams

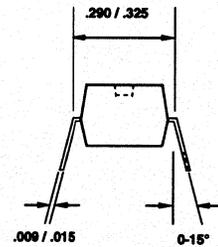
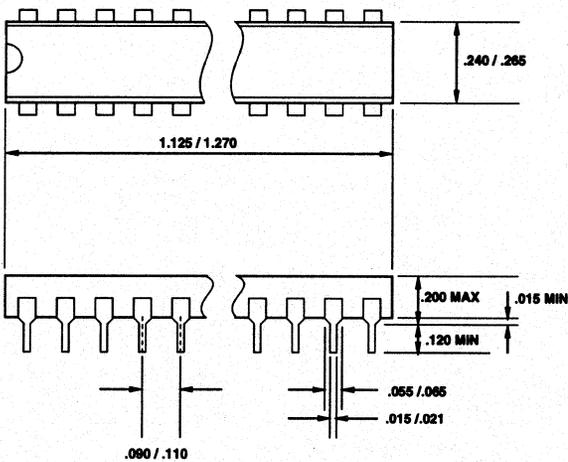
20-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



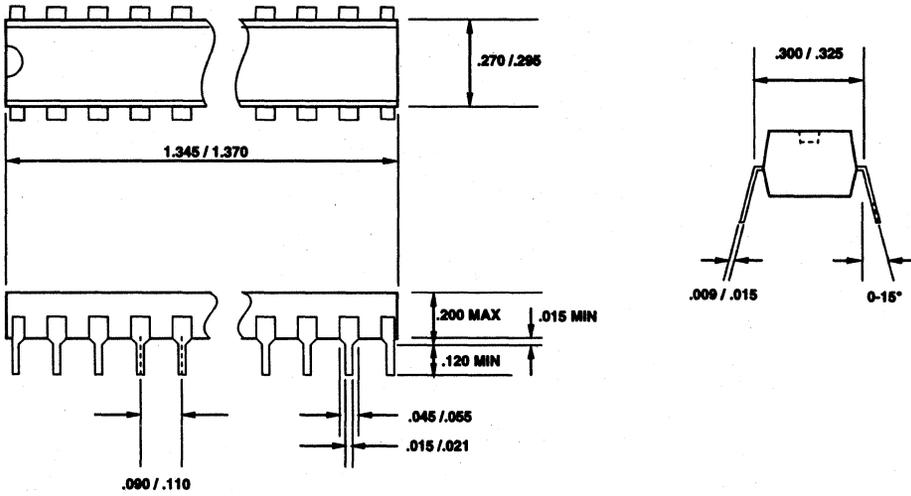
24-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



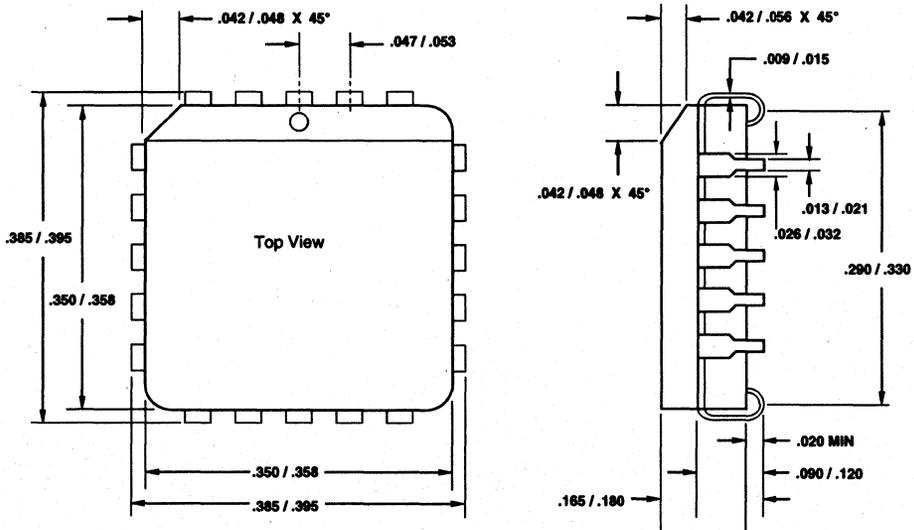
Package Diagrams

28-Pin Plastic DIP Dimensions in Inches MIN. / MAX.



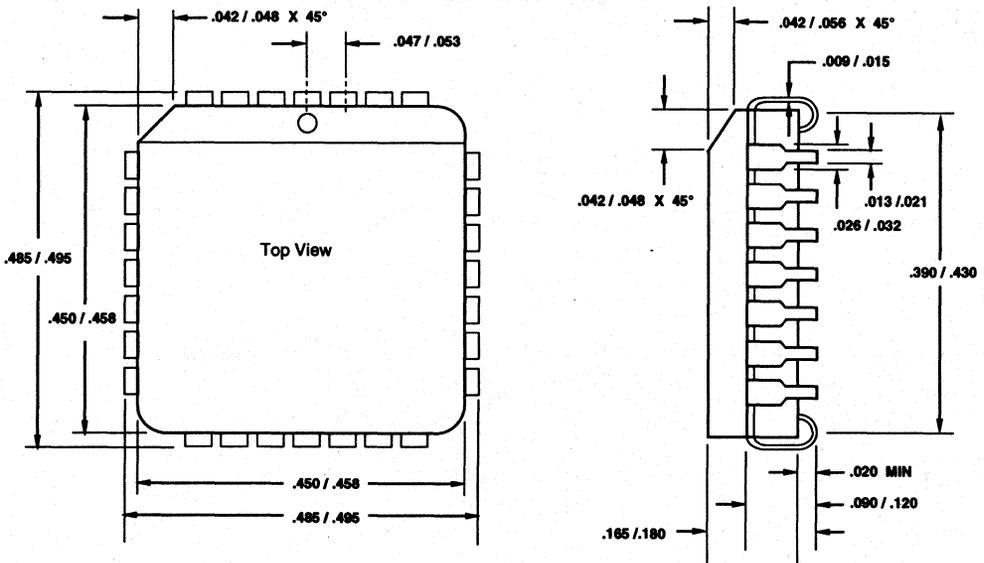
20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



28-Pin PLCC Package

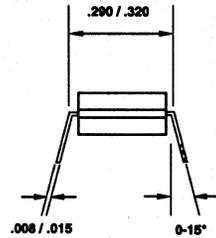
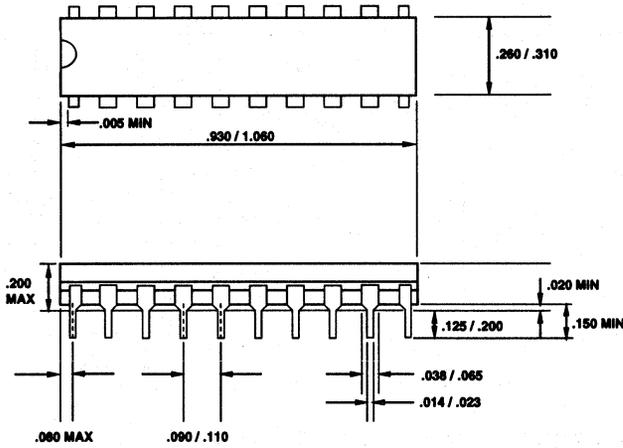
Dimensions in Inches MIN. / MAX.



Package Diagrams

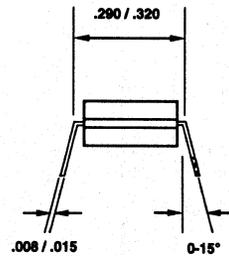
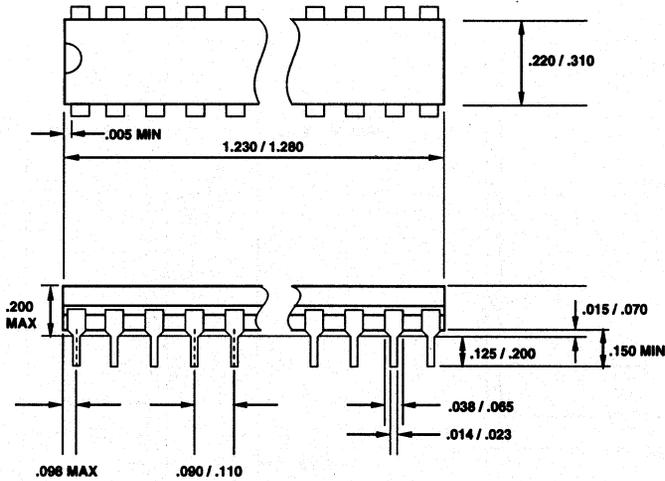
20-Pin (300 MIL) Cerdip

Dimensions in Inches MIN. / MAX.



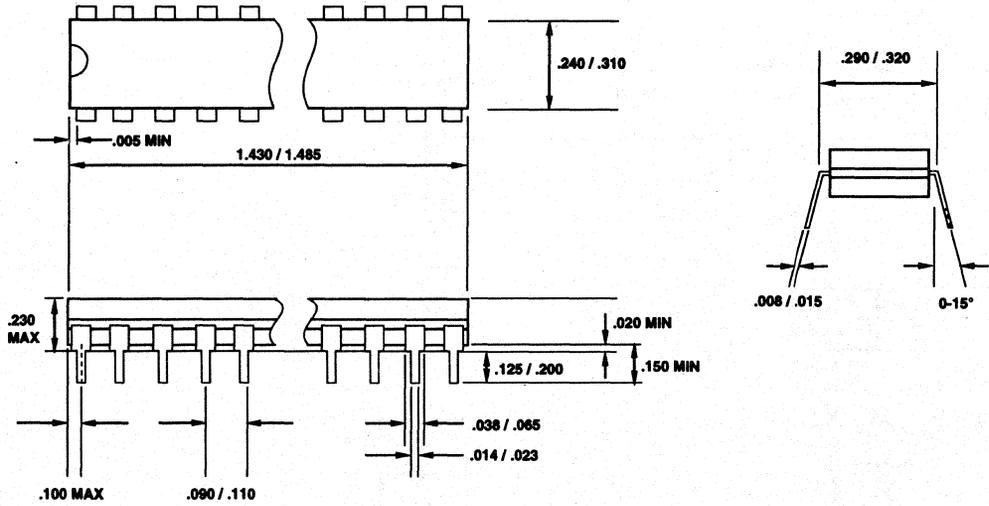
24-Pin (300 MIL) Cerdip

Dimensions in Inches MIN. / MAX.



28-Pin (300 MIL) Cerdip

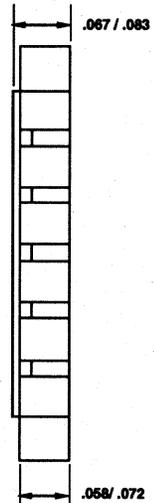
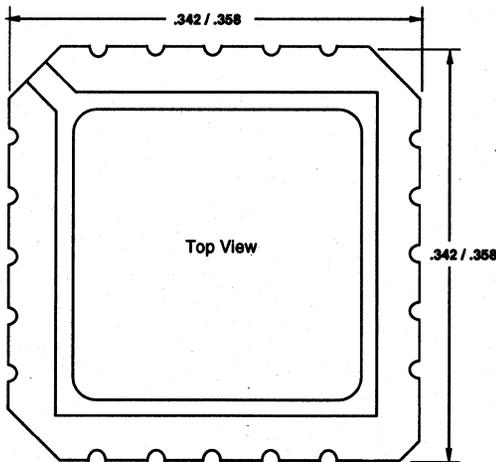
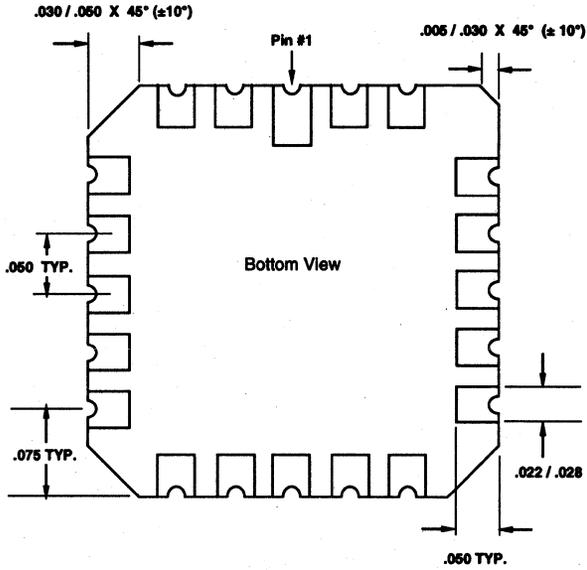
Dimensions in Inches MIN. / MAX.



Package Diagrams

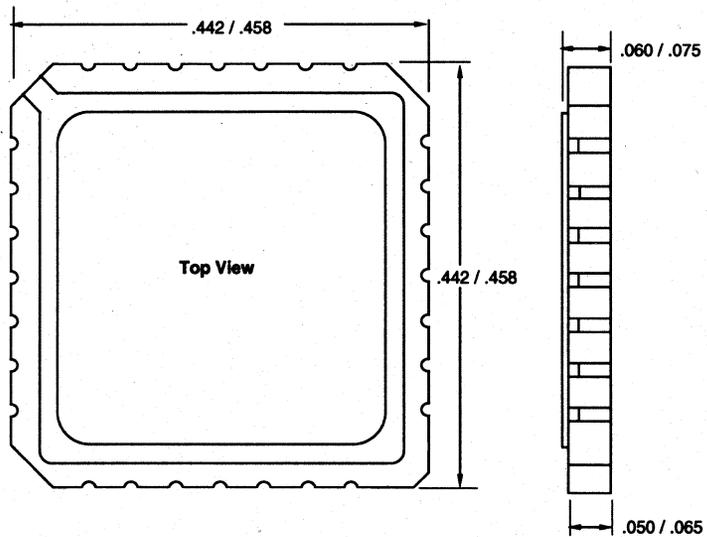
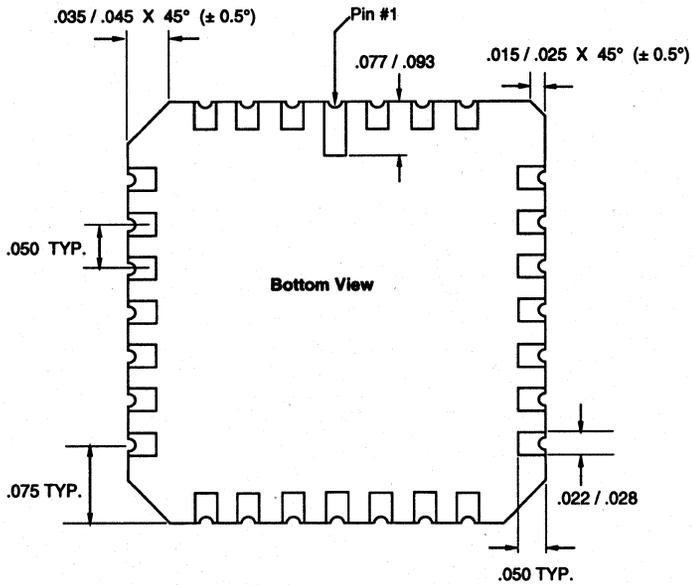
20-Pin LCC

Dimensions in Inches MIN. / MAX.



28-Pin LCC

Dimensions in Inches MIN. / MAX.



Tape and Reel Specifications

A tape-and-reel packing container is available for plastic leaded chip carriers to protect the product from mechanical/electrical damage and to provide an efficient method for handling. Lattice's tape-and-reel containers are shipped in full compliance to Electronics Industry Association Standard EIA-RS481.

The tape-and-reel packing system consists of a pocketed carrier tape loaded with one device per pocket. A protective cover tape seals the carrier tape and holds the devices in

the pockets. A full reel holds a maximum quantity of devices depending on the package size. Lattice requires ordering in full reel quantities. Once loaded, the tape is wound onto a plastic reel for labeling and packing.

Devices packaged in tape-and-reel containers must be factory programmed (pre-patterned). Custom marking of devices prior to mounting on tape-and-reel is available upon request. Contact your local Lattice sales office for more details on Lattice's tape-and reel packing system.

TAPE-AND-REEL QUANTITIES AND DIMENSIONS

Package	Pin Count	Carrier Tape Dimensions		Quantity Per 13 Inch Reel
		Width	Pitch	
PLCC	20-pin	16mm	12mm	1000
	28-pin	24mm	16mm	750

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