

**4, 6, 7, or 8-Channel Ferrite
Read/Write Circuits**

GENERAL DESCRIPTION

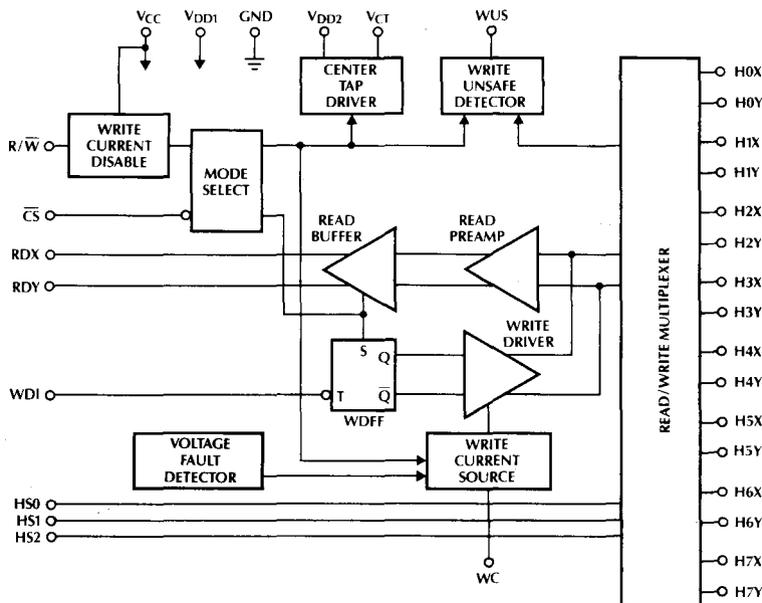
The ML511 is a bipolar monolithic read/write circuit designed for use with center-tapped ferrite recording heads. The ML511 and ML511R are performance upgrades from the ML501 and ML501R. The R designation in the part number indicates that this part has internal head damping resistors.

The ML511 provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The ML511 also provides a low noise read data path, and data protection circuitry for all of the channels.

FEATURES

- Enhanced write current stability
- ML511, ML511R is replacement for SSI 32R511/511R and is designed for center-tapped ferrite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Power supply fault protection
- 1.5 nV/√Hz maximum input noise voltage
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5V, +12V power supplies

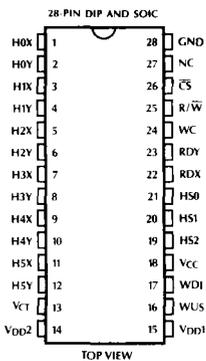
BLOCK DIAGRAM



PIN CONNECTIONS

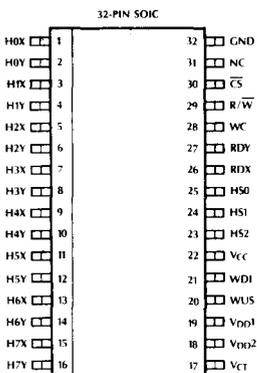
ML511-6 OR ML511R-6

6 Channels



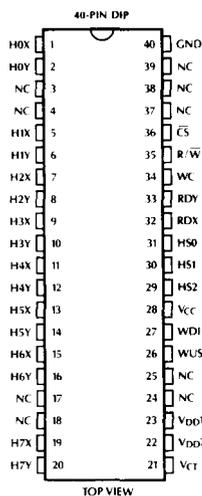
ML511-8 OR ML511R-8

8 Channels



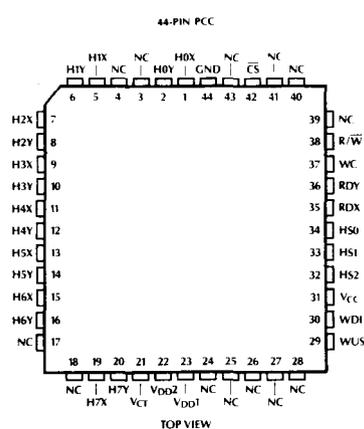
ML511-8 OR ML511R-8

8 Channels



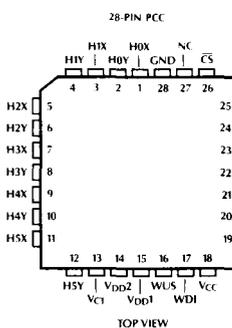
ML511-8 OR ML511R-8

8 Channels



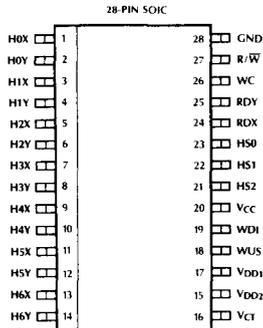
ML511-6 OR ML511R-6

6 Channels



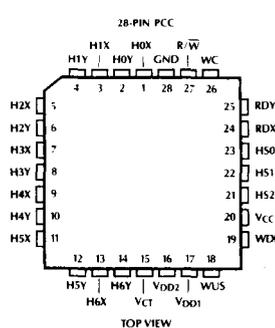
ML511R-7CS

28-Lead SOIC



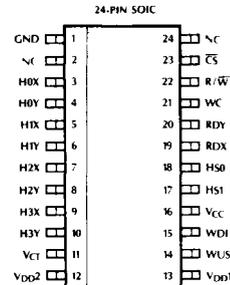
ML511R-7CQ

28-Lead PCC



ML511-4 OR ML511R-4

4 Channels



PIN DESCRIPTION

NAME	FUNCTION
HS0-HS2	Head Select (eight heads)
CS	Chip Select (low level enables chip)
R/W	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collector output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X-H7X	X head connections
H0Y-H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
VCT	Voltage Center Tap (center tap voltage source)
VCC	+5 volts
VDD1	+12 volts
VDD2	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range	
V _{DD1}	-0.3 to 14V _{DC}
V _{DD2}	-0.3 to 14V _{DC}
V _{CC}	-0.3 to 6V _{DC}
Input Voltage Range	
Digital Inputs (CS, R/W, HS, WDI)	-0.3 to V _{CC} +0.3V _{DC}
Head Ports (H0X-H7X, H0Y-H7Y)	-0.3 to V _{DD1} +0.3V _{DC}
Write Unsafe (WUS)	-0.3 to 14V _{DC}
Write Current (I _W)	60mA
Output Current	
Read Data (RDX, RDY)	-10mA
Center Tap Current (I _{CT})	-60mA
Write Unsafe (WUS)	12mA
Storage Temperature	-65°C to 150°C
Junction Temperature (T _J)	135°C
Lead Temperature (Soldering 10 sec.)	300°C

OPERATING CONDITIONS

Supply Voltage	
V _{DD1}	12V ± 10%
V _{CC}	5V ± 10%
Head Inductance	
L _H , ML511 or ML511R	5 to 15μH
Damping Resistor (R _D , ML511 only)	500 to 2000Ω
RCT Resistor (1/4 Watt)	120Ω ± 5%
Write Current (I _W)	10 to 40mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified V_{DD1} = V_{DD2} = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 40mA, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I _{CC}	V _{CC} Supply Current	Read or Idle Mode			35	mA
		Write Mode			30	mA
I _{DD}	V _{DD} Supply Current	Read Mode			35	mA
		Write Mode			20 + I _W	mA
		Idle Mode			20	mA
P _D	Power Dissipation	Read Mode			655	mW
		Write Mode I _W = 40mA, R _{CT} = 0Ω			960	mW
		Idle Mode			455	mW
DIGITAL INPUTS (CS, R/W, HS, WDI)						
V _{IH}	High Voltage		2			V _{DC}
V _{IL}	Low Voltage				0.8	V _{DC}
I _{IH}	High Current	V _{IH} = 2.0V			100	μA
I _{IL}	Low Current	V _{IL} = 0.8V	-0.4			mA
WUS OUTPUT						
V _{OL}	Output Low Voltage	I _{OL} = 8mA (Safe)			0.5	V _{DC}
I _{OH}	Output High Current	V _{OH} = 5V (Unsafe)			100	μA
CENTER TAP VOLTAGES						
V _{CT}	Read Mode	Read Mode		4		V _{DC}
V _{CT}	Write Mode	Write Mode		6		V _{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD1} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35\text{ mA}$, $L_H = 10\mu\text{H}$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5\text{ MHz}$, C_L (RDX, RDY) $\leq 20\text{ pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD1} \leq 8.7V$	-200		200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375		2.625	
V_{HD}	Differential Head Voltage Swing		7.0			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML511	10k			Ω
		$T_J = 25^\circ\text{C}$ ML511R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1\text{mV}_{P,P}$ @ 300kHz, R_L (RDX, RDY) = $1\text{k}\Omega$	85		115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5\text{mV}_{P,P}$ @ 300kHz	-3		+3	mV
BW	Bandwidth (-3 dB)	$ Z_S < 5\Omega$, $V_{IN} = 1\text{mV}_{P,P}$	30			MHz
e_{IN}	Input Noise Voltage	$BW = 15\text{ MHz}$, $L_H = 0$, $R_H = 0$			1.5	$\text{nV}/\sqrt{\text{Hz}}$
C_{IN}	Differential Input Capacitance	$f = 5\text{ MHz}$			20	pF
R_{IN}	Differential Input Resistance	$f = 5\text{ MHz}$, $T_J = 25^\circ\text{C}$ ML511	2k			Ω
		$V_{IN} = 6\text{mV}_{P,P}$ ML511R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD1} \leq 13.2V$	-200		200	μA
I_{IN}	Input Bias Current (1 side)				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100\text{mV}_{P,P}$ @ $f = 5\text{ MHz}$	50			dB
PSRR	Power Supply Rejection Ratio	$100\text{mV}_{P,P}$ @ 5 MHz on V_{DD1} , V_{DD2} , or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100\text{mV}_{P,P}$ @ 5 MHz and Selected Channel: $V_{IN} = 0\text{mV}_{P,P}$	45			dB
V_{OS}	Output Offset Voltage	Read Mode	-460		+460	mV
		Write or Idle Mode	-20		+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5		6.5	V
		Write or Idle Mode		5.3		V
R_{OUT}	Single-Ended Output Resistance	$f = 5\text{ MHz}$			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = $6V$ Write or Idle Mode	-100		100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	± 2.1			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD1} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35\text{ mA}$, $L_H = 10\mu\text{H}$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5\text{ MHz}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/ \bar{W} to Write Switching Delay	To 90% of Write Current Output			1	μs
t_{WR}	R/ \bar{W} to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	μs
t_{IW} or t_{IR}	\bar{CS} to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	μs
t_{WI} or t_{RI}	\bar{CS} to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	μs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	μs
t_{D1}	Safe to Unsafe Write Unsafe Delay	$I_W = 35\text{ mA}$	1.6		8	us
t_{D2}	Unsafe to Safe Write Unsafe Delay	$I_W = 35\text{ mA}$			1	us
t_{D3}	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points			25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

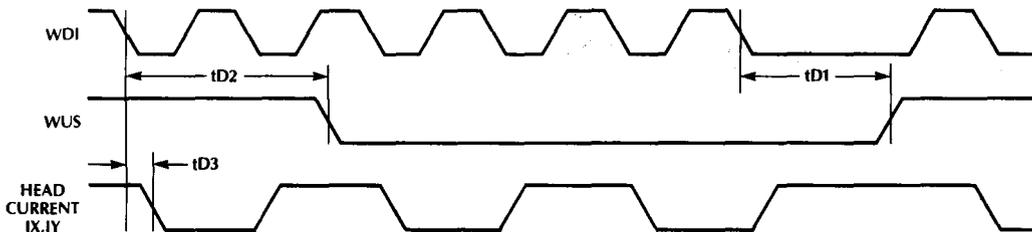
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_j) should not exceed 135°C.

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TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML511 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/W controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML511 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML511 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$$I_W = K/R_{WC}$$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML511 to write mode, the WDF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML511, ML511R exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML511 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select			
HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

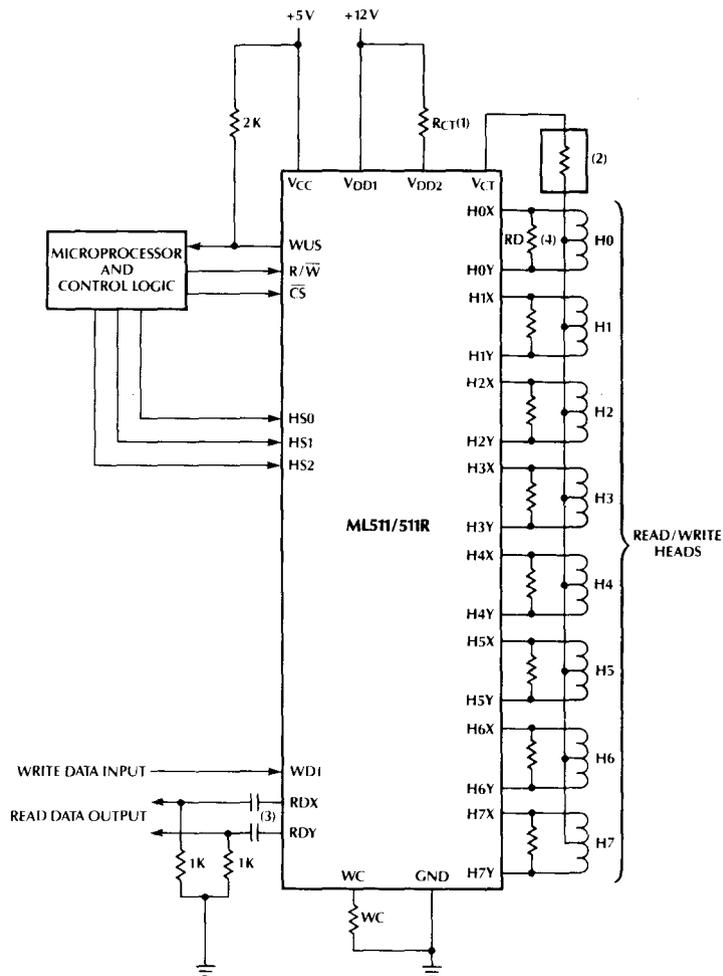
0 = Logic Level Low
 1 = Logic Level High
 X = Don't Care

Table 2.

Mode Select		
\overline{CS}	R/W	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
 1 = Logic Level High
 X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect V_{DD1} to V_{DD2}).
 $RCT (1/2 \text{ Watt}) = 120 (40 / I_w)$ ohms
 where I_w = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μ A.
4. Damping resistors not required on ML511R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML511-4CS	24-Lead SOIC (S24)	4
ML511R-4CS	24-Lead SOIC (S24)	4
ML511-6CP	28-Lead Molded DIP (P28)	6
ML511R-6CP	28-Lead Molded DIP (P28)	6
ML511-6CQ	28-Lead PCC (Q28)	6
ML511R-6CQ	28-Lead PCC (Q28)	6
ML511-6CS	28-Lead SOIC (S28)	6
ML511R-6CS	28-Lead SOIC (S28)	6
ML511R-7CS	28-Lead SOIC (S28)	7
ML511R-7CQ	28-Lead PCC (Q28)	7
ML511-8CP	40-Lead Molded DIP (P40)	8
ML511R-8CP	40-Lead Molded DIP (P40)	8
ML511-8CQ	44-Lead PCC (Q44)	8
ML511R-8CQ	44-Lead PCC (Q44)	8
ML511-8CS	32-Lead SOIC (S32)	8
ML511R-8CS	32-Lead SOIC (S32)	8

THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θ_{ja}
24-Lead	SOIC	75°C/W
28-Lead	PDIP	55°C/W
28-Lead	PCC	65°C/W
28-Lead	SOIC	70°C/W
32-Lead	SOIC	60°C/W
44-Lead	PCC	60°C/W
40-Lead	PDIP	45°C/W