MITSUBISHI SEMICONDUCTORS 1990

DIGITAL ASSP

DATA BOOK

MITSUBISHI ELECTRIC

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GUIDANCE 1

INTRODUCTION TO DIGITAL ASSP

What is ASSP?

Application Specific Standard Product (ASSP) is a semicoductor integrated circuit suitable for reducing development time and differentiating one's own office automation products from other manufacturers.

Fig. 1 shows the classification and design method of ASIC. Unlike ASCP (Application Specific Custom Product) ASSP is developed for multiple customers and is called an application specific standard product or dedicated standard product.

Typical examples are LSIs for image processing and for communication. The standard cell method is used for the basic design method and a variety of specific ASSP cells are developed and registered for small-scale systems as well as large-scale systems. This method reduces development time and realizes miniaturization of chips, which in turn lowers costs and smooths development for a variety of products.

What kind of effect does ASSP have for customers?

This section describes the positioning of ASSP as a customer system. Fig. 2 shows the position of each IC on the aspect of customer system. The horizontal axis shows the scale of system in which ICs are accommodated. The point of origin shows the point where system orientation is highest. The vertical axis defines the ratio of design by customers and by IC manufacturer, and the closer the position is to the point of origin, the greater the ratio of design by IC manufacturer. If an IC is to be considered as a customer system, the best point to be positioned is where the system orientation is highest and IC design is most dependent on IC manufacturers. The system orientation of ASSP is higher than that of gate array of ASCP and the ratio of design by manufacturers is greater than that of ASCP standard cell.

Fig. 2 does not show the development period, but no development period is required if a product is already prepared by manufacturers and a newly-developed product can be produced in the same period of time as that of the standard cell of ASCP. Compared to handmade ASCP, it can be developed in a very short period of time. The disigning of ASCP is appropriate if the technical know-how of the customer system is involved. By combining the merits of ASSP and ASCP, a unique system can be developed, having additional values different from those of other makers.

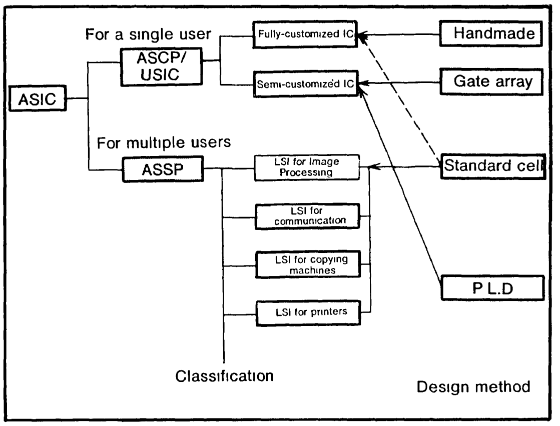


Fig. 1 Classification of ASIC and design method

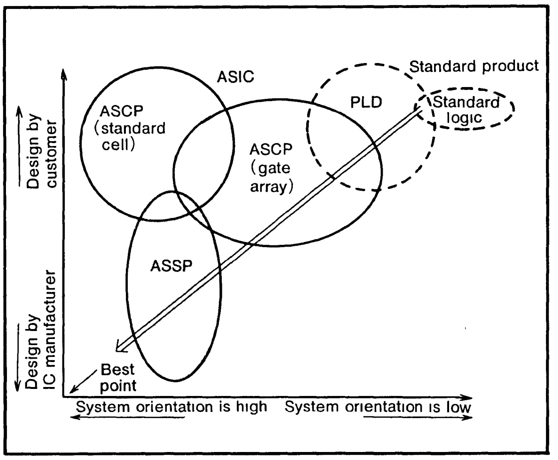


Fig. 2 Positioning of ASSP

INTRODUCTION TO DIGITAL ASSP

Development strategies of Mitsubishi digital ASSP

Mitsubishi digital ASSP has the following three developement strategies for industrial equipment as well as office automation equipment.

I. Peripheral LSI series for microcomputer and memory applicable to system evolution

High-speed access time and intelligent function (UART · for communication, programmable I/O, DRAM controller)

Peripheral LSI series for microcomputer and memory are the LSIs used for MPU (Micro Processor Unit), MCU (Micro Controller Unit) and for peripheral circuits such as memory. Compared to conventional LSIs, they are the new generation peripheral LSIs applicable to system evolution with additional values. Typical examples are given in the later section "System configuration examples by Mitsubishi digital ASSP". Interrupt controller and DMA controller are under development and these products can be used for a variety of systems.

II. Data buffer with the most suitable memory capacity for each function (Scan memory for LBP or FIFO for image data)

The capacity of optimum built-in memory of data buffer is becoming increasingly large and it is difficult to configure all systems only by large-capacity memory which is represented by recent general-purpose memory and it leads to waste of memory. The devices are intended to provide data buffers with optimum built-in memory required for image data or for communication at a reasonable price.

These data buffers have specific built-in control circuits required by customer systems. Compared to the system configured with general-purpose memory and control circuits (gate array, etc.), this device realizes higher performance, higher speed, space saving and reduced costs. The built-in memory mainly consists of SRAM and DRAM, but EPROM or EEPROM are under development.

Table 1 Classification of digital ASSP products

- I. Microcomputer/memory peripheral LSI series
  - (1)DRAM controller and peripheral IC
    - M66200AP/AFP (DRAM controller)
    - M66210P/FP M66211P/FP (10-bit data latch)
    - M66212P/FP M66213P/FP (5-bit data selector)
  - (2)MPU, MCU peripheral LSI
    - M66230P/FP (Asynchronous serial data communication control IC)
    - M66240P/FP (4-channel PWM generator)
    - M66500SP/FP (High-speed and high-voltage parallel I/O expander)
- II. Data buffer built-in memory
  - (1)Data buffer for communication
    - M66220SP/FP (Mail Box 256×8-bit)
    - M66221SP/FP (Mail Box 256×9-bit)
    - M66222SP/FP (Mail Box 128×8-bit×2)
  - (2)Line buffer
    - M66250P/FP (5KB FIFO/LIFO)
    - M66305P/FP (5120-bit ×2 Toggle line buffer)
    - M66307SP/FP (Parallel-input serial output 5120-bit scan line buffer)
- III. Application specific IC
  - (1)Dedicated controller
    - M66300P/FP (Eraser, panel display controller)
    - M66330SP/FP (Band compression and expansion controller for facsimiles)
  - (2)Driver
    - M66310/311/312/313/314P/FP (8-, 16- or 32-bit full CMOS LED driver)
    - M66510P/FP (Laser diode driver)
    - M66700P, M66705P/FP (Dual or Quad CCD clock driver)
    - M751270/71/72/73P/FP (FDD/HDD high-speed and high-drive driver)
    - M753114P (High-speed photo-coupler driver/receiver)
- IV. Others
  - (1)Original logic
    - M74HC-1 series (High-speed and high-drive CMOS logic)
    - CIC series (MAST, ALS complex BIPOLAR logic)
  - (2)Line interface
    - RS-232C, 422A, 485 compatible driver/receiver/transceiver
  - (3)Cross-point switch
    - M402100BP/BFP (4×4 cross-point switch)
    - M402101BP/BWP (4×8 cross-point switch)

III. Application-specific ICs to realize high performance and miniaturization in each system field. (Laser power driver, eraser controller)

Application-specific ICs are key products for configuring systems. These products have specific functions, such as, laser power drivers for LBP (laser beam printers) and eraser controllers. The Mitsubishi digital ASSP support the customer's hardware as a kit. Production of these application specific ICs requires cooperation both from customers and Mitsubishi Electric. In some cases, Mitsubishi offers ASCP as an alternative.

Wafer process methods employed for the production are the fine CMOS process, high-withstanding-voltage CMOS, BI-CMOS, high-speed bipolar and high-withstanding-voltage bipolar process. Table 1 shows the typical ASSP products classified by the above-mentioned criteria.

In section IV, (1) original logic, (2) line interface and (3) cross-point switch are described. The M74HC-1 series in (1) original logic incorporates basic technology of Mitsubishi's CMOS digital ASSP, and it guarantees the output current $I_O = \pm 24$mA as well as realizing the reduction of switching noise and E.M.I. (Electro-Magnetic Interference) by the employment of unique circuit technology. Most of the Mitsubishi's digital ASSP employs this technology and the output current of $I_O = \pm 24$mA is guaranteed and is effective for line or bus drivers, making the device easy to use in system configuration.

The M74HC-1 series consists of 32 products, including bus and line drivers.

CIC (Combination Integrated Circuit) in (1) original logic is a bipolar complex logic to realize high-speed and high-drive capability, which were not possible with the CMOS gate array, and is suitable for memory control as a peripheral circuit of high-speed MPU or bus line control. Any function can be selectively combined from the standard logic series of MAST (Mitsubishi Advanced Schottky TTL) and ALS (Advanced Lower Power Schottky).

Development procedure of Mitsubishi digital ASSP

Fig. 3 shows the development procedure of ASSP. Mitsubishi Electric is continuously researching the next generation system in each application field, mainly with the help of the Application System Development Department which prepares specifications for key parts in each field. The marketability of these parts is confirmed by listening to customer's opinions and ideas. This information is used to designate specifications that can become standardized in the industry. If feasible, the products are then developed at a risk to Mitsubishi Electric. If a customer's system need to be evaluated during development (Fig. 3.), a bread board can be submitted while the device is under development.

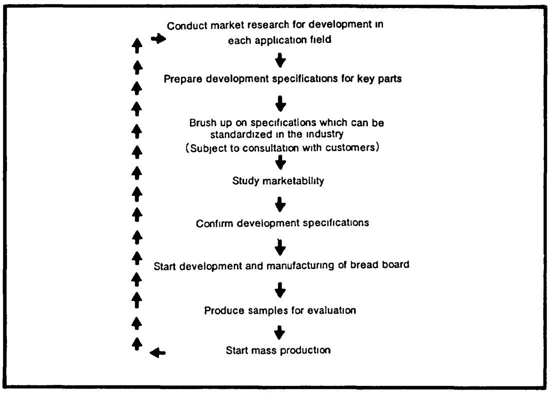


Fig. 3 Development procedure of ASSP

System configuration example by Mitsubishi digital ASSP

System configuration examples by Mitsubishi digital ASSP are given below, using office automation equipment.

Fig. 4 shows the basic configuration of office automation equipments. Office automation equipment always needs to have an image reading part and record output part for image data I/O and, therefore, mechanical control part to control paper feed, etc. is essential. Communication control part enables data I/O with external equipment such as personal computers. The input data is processed in data processing part for reduction, enlargement or trimming. System control part controls the whole process by the input from display / operation part and the status is displayed by LEDs. Examples of system configuration is given below using a page printer (LBP), digital copying machine and facsimile as office automation equipment.

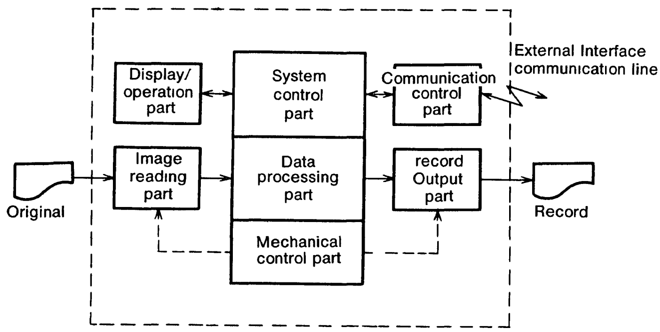


Fig. 4 Basic configuration of office automation equipment

● Page printer (LBP)

Page printers represented by a laser beam printer are now used in many offices due to their speed, print quality and low noise. Fig. 5 shows a system configuration example using digital ASSP. DRAM controller, async serial I/O controller and parallel I/O expander are used in the image creation part in which high-level data processing is executed with a 16-bit MPU.

Serial-output scan data buffer that stores one line of image data created in the image creation part simplifies data transfer to the engine part that requires synchronization.

On the other hand, a laser driver to realize high-speed switching of laser diode is available for the engine part for printer output. It can be combined with MCU to execute APC (auto-power control) of laser output.

● Digital copying machine

Fig. 6 shows a system configuration example of a copying machine using digital ASSP. CCD clock driver drives CCD image sensor for reading originals at a high speed in the image input part and this is one of the main features of a digital copying machine.

Mitsubishi Electric is now developing FIFO/LIFO memory which has a structure of 5120 words × 8-bit for high-speed line memory data storage after A-D conversion.

4-channel PWM generator and communication data buffer are suitable for realizing highly technological control mechanism and multi CPU systems. 256 bytes communication data buffer with dual access ports enables high speed data transfer of MPUs or MCUs.

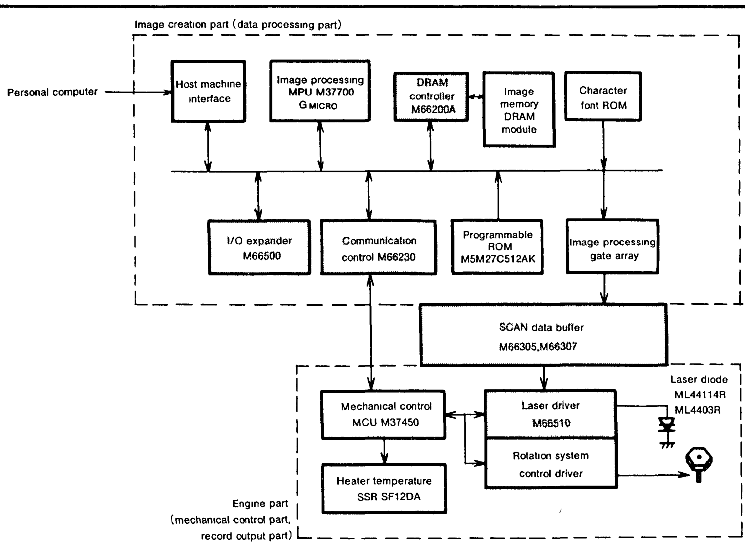


Fig. 5 System configuration example of a page printer (LBP)

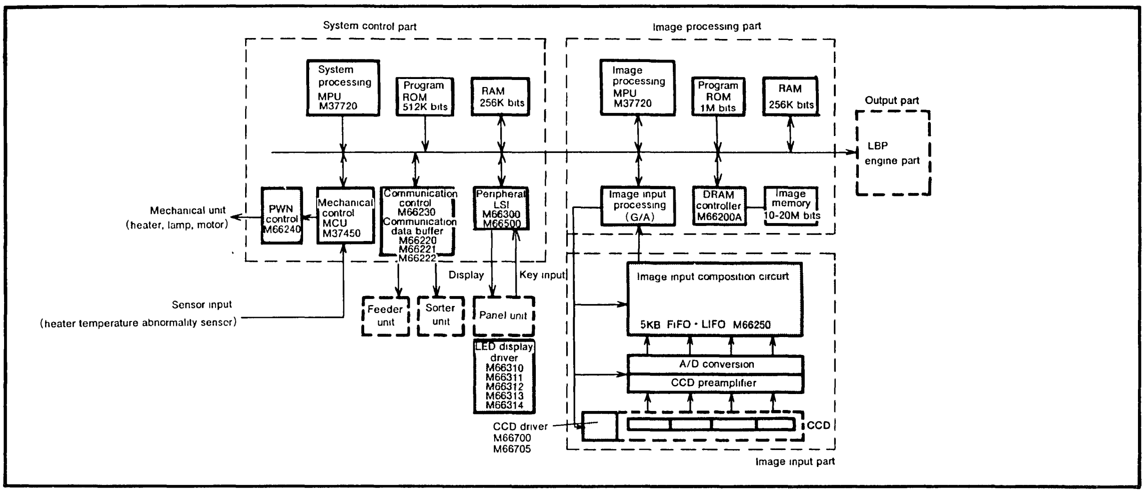


Fig. 6 System configuration example of a digital copying machine

● Facsimile

A facsimile consists of a system control part, original reading part by an image sensor, thermal printer part, image data processing part for image data coding/decoding and a communication control part using a modem. Fig. 7 shows a system configuration example using digital ASSP. DIP (Dual Inline Package) and SOP (Small Outline Package) are available for 4-channel CCD clock driver in the original reading part.

Mitsubishi is now developing a band compression and expansion controller which features built-in I/O line memory for image processing part which is the central core of facsimile with coding conversion (MH method ↔ MR method) and reduction functions.

System configuration examples using digital ASSP are given above. Table 2 summarizes the functions and features of each product.

Future development

The outline of digital ASSP and system configuration examples are described above using office automation equipments. The devices will be widely applied in the field of home-use equipment such as audio visual equipment or VCRs in which use of digital data processing is increasing. Mitsubishi Electric is planning to develop devices used in the fields other than office automation field.

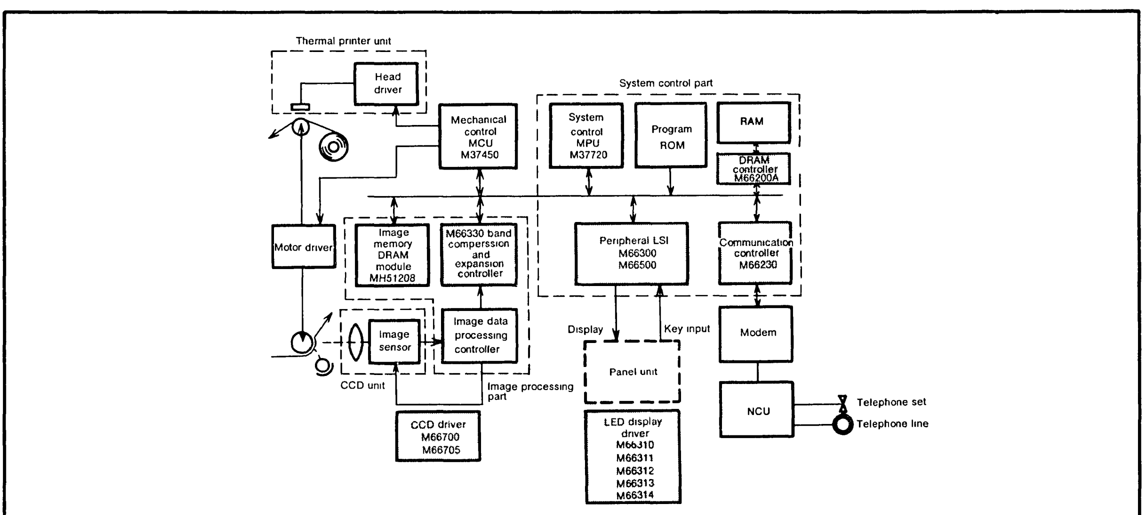


Fig. 7 System configuration example of a G-3 facsimile

Table 2 Functions and features of digital ASSP

Application	Function	Type name	Features
System control part Data processing part	DRAM controller	M66200AP/AFP M66210/211P/FP M66212/213P/FP	General-purpose MPU applicable 256K/1M DRAM controller 10-line data latch, high drive capacity ±24mA 2- to 1-line (×5) data selector, high drive capacity ±24mA
	Panel display controller	M66300P/FP	Built-in 63-byte FIFO, direct connection to microcomputer bus, serial output
	Scan data buffer	M66305P/FP M66307SP/FP	Two built-in circuits of 5120-bit serial buffer, toggle operation, 5120-bit parallel-input serial-output buffer
	Parallel I/O expander	M66500SP/FP	44-bit I/O expansion, 35V, 48mA output port (16 bits)
	Band compression and expansion controller	M66330SP/FP	MH/MR/MMR support, Built-in I/O line memory, coding method conversion and reduction function
Mechanical control part	4-channel PWM generator	M66240P/FP	High resolution of 16 bits, direct connection to microcomputer bus
Communication control part	Async serial I/O controller	M66230P/FP	Baud generator, built-in CRC circuit, built-in 4-byte FIFO for transmission/receiving
	Communication data buffer	M66220SP/FP M66221SP/FP M66222SP/FP	256×8-bit, high-speed dual port access (40ns) 256×9-bit, high-speed dual port access (40ns) 128×8-bit×2, high-speed dual port access (40ns)
	Line interface IC	M75 series M5A, M5M series	Supports RS-232C, 422A, 423A, 485
Image reading part	CCD clock driver	M66700P M66705P/FP	High-speed, high drive capacity, direct connection to gate array is possible
	High-speed line memory	M66250P/FP	5120×8-bit, FIFO/LIFO, start address specification
Record output part	Laser driver	M66510P/FP	Applicable to R-type laser diode, high-speed operation (20Mbps), Built-in laser power monitor circuit
Display panel part	CMOS LED driver	M66310P/FP M66311P/FP M66312P/FP M66313FP M66314FP	16-bit, high drive capacity −24mA (open drain) 16-bit, high drive capacity +24mA (open drain) 8-bit, high drive capacity ±16mA (3-state) 32-bit, high drive capacity +24mA (open-drain) 16-bit, high drive capacity −25mA, high withstanding voltage 20V

INDEX BY FUNCTION

■PERIPHRAL LSI SERIES FOR MICROCOMPUTER AND MEMORY

Type name	Function	Process	Supply voltage	Outline	Application/field	Page
M66200AP/AFP	DRAM controller: DRAM controller	CMOS	5±10%	P : 24P4D FP : 24P2	General digital equipment for industrial or home use (including all fields of personal computers or word processors)	2-3
M66210P/FP M66211P/FP	DRAM controller: Address driver: 10-line data latch	CMOS	5±10%	P : 24P4D FP : 24P2	General digital equipment for industrial or home use (including all fields of personal computers or word processors)	2-26
M66212P/FP M66213P/FP	DRAM controller: Address driver: 2- to 1- (×5) data selector	CMOS	5±10%	P : 20P4 FP : 20P2N	General digital equipment for industrial or home use (including all fields of personal computers or word processors)	2-31
M66230P/FP	A²RT Async serial data communication control	CMOS	5±10%	P : 24P4D FP : 24P2W	Data transfer for use in office automation equipment of PPC, printer, and personal computers	2-35
M66240P/FP	4-channel PWM generator	CMOS	5±10%	P : 24P4D FP : 24P2W	Control of DC motor, stepping motor and heater. Digital servo for office automation equipment and industrial equipment.	2-54
M66500SP/FP	High-drive and high-speed parallel I/O expander	Bi-CMOS	5±10%	SP : 64P4B FP : 64P6W	I/O expander for general digital equipment for industrial and home use, especially those equipment with many mechanical control such as LBP, PPC and FAX	2-70

■DATA BUFFER BUILT-IN MEMORY

Type name	Function	Process	Supply voltage	Outline	Application/field	Page
M66220SP/FP ★★	MAIL-BOX(Dual Port RAM)	CMOS	5±10%	P : 42P4B FP : 42P2R	Memory for data transfer between MPU and MCU	3-3
M66221SP/FP ★★	MAIL-BOX(Dual Port RAM)	CMOS	5±10%	P : 48P4B FP : 52P2G	Memory for data transfer between MPU and MCU	3-9
M66222SP/FP ★★	MAIL-BOX(Dual Port RAM)	CMOS	5±10%	P : 42P4B FP : 42P2R	Memory for data transfer between MPU and MCU	3-16
M66250P/FP	5KB FIFO/LIFO	CMOS	5±10%	P : 28P4Y FP : 28P2W	One-line delay, inverted output (mirror), time axis conversion for high-speed facsimile and digital copying machine	3-21
M66305P/FP	Toggle line buffer	CMOS	5±10%	P : 20P4 FP : 24P2W	Data buffer for image processing and peripheral circuits of LBP and FAX	3-34
M66307SP/FP ★★	Parallel-input serial-output scan line buffer	CMOS	5±10%	SP : 32P4B FP : 32P2W	Line buffer between image processing system and peripheral equipment such as high-speed FAX and printers	3-44

■APPLICATION SPECIFIC IC

Type name	Function	Process	Supply voltage	Outline	Application/field	Page
M66300P/FP	Parrallel-in serial-out data buffer with FIFO	CMOS	5±10%	P : 20P4 FP : 20P2	• PPC eraser controller • Panel display controller • LED module control	4-3
M66310P/FP	Shift register with latch: 16-bit, −24mA, P-ch open-drain output (cathode common LED drive)	CMOS	5±10%	P : 24P4D FP : 24P2	• PPC eraser LED drive • LED module drive such as LED display panel of button telephone set • General data parallel-serial conversion	4-13
M66311P/FP	Shift register with latch: 16-bit, +24mA, N-ch open drain output (anode common LED drive)	CMOS	5±10%	P : 24P4D FP : 24P2	• PPC eraser LED drive • LED module drive such as LED display panel of button telephone set • General data parallel-serial conversion	4-18
M66312P/FP	Shift register with latch: 8-bit, ±16mA, 3-state output (LED drive)	CMOS	5±10%	P : 16P4 FP : 16P2N	• PPC eraser LED drive • LED module drive such as LED display panel of button telephone set • General data parallel-serial conversion	4-23
M66313FP	Shift register with latch: 32-bit, +24mA, N-ch open drain output (anode common LED drive)	CMOS	5±10%	42P2R	• PPC eraser LED drive • LED module drive such as LED display panel of button telephone set • General data parallel-serial conversion	4-28
M66314FP	Shift register with latch: 16-bit, −25mA, 3-state output (cathode common LED drive, current variable)	CMOS	12~18	24P2	• PPC eraser LED drive • LED module drive such as LED display panel of button telephone set • General data parallel-serial conversion	4-34
M66320P/FP	Shift register with latch: 12-bit pre-head driver	CMOS	5±10%	P : 20P4 FP : 20P2N	• Pre-drive of printer head pin • General parallel-serial data conversion	4-40
M66330SP/FP ★★	Band compression and expansion controller for FAX	CMOS	5±10%	SP : 40P4B FP : 36P2R	• Facsimile	4-44
M66510P/FP ★★	Laser diode driver	High-speed Bipolar	5±5%	P : 20P4 FP : 20P2N	• Cathode stem type semiconductor laser driver (20Mbits/sec)	4-47
M66700P	Dual CCD clock driver	High-speed Bipolar	12±10%	8P4	• CCD image sensor drive for FAX, PPC or personal computers	4-51
M66705P/FP	Duad CCD clock driver	High-speed Bipolar	12±10%	P : 16P4 FP : 16P2N	• Capacitative load drive • High-speed drive of power MOSFET	4-55

★★ : Under Development

■LINE INTERFACE IC

Type name	Function	Process	Supply voltage	Outline	Application/field	Page
M5A26LS29P	Quad RS-423A driver	Bip	5±5%	16P4	Communication	5-3
M5A26LS31P/FP	Quad RS-422A driver	Bip	5±5%	P : 16P4 FP : 16P2N	LBP, HDD, PPC, POS	5-8
M5M3487P/FP						5-14
M5A26LS32AP/AFP	Quad RS-422A receiver	Bip	5±5%	P : 16P4 FP : 16P2N	LBP, HDD, PPC, POS	5-18
M5M3486P/FP						5-25
M5M34050P/FP **M5M34051P/FP**	Dual RS-422A transceiver	Bip	5±5%	P : 16P4 FP : 16P2N	LBP, HDD, PPC	5-29
M751270P/FP **M751271P/FP**	High-speed, high-drive open-collector driver	Bip	5±10%	P : 16P4 FP : 16P2N	FDD, HDD, LBP	5-34
M751272P/FP **M751273P/FP**						5-36
M75173P/FP	Quad RS-485 receiver	Bip	5±5%	P : 16P4 FP : 16P2N	POS, factory automation, personal computer	5-38
M75175P/FP						5-43
M75176P ★★ **M75177P** ★★ **M75178P** ★★ **M75179P** ★★	RS-485 transceiver	Bip	5±5%	8P4	POS, factory automation, personal computer	5-48
M75188P	Quad RS-232C driver	Bip	±9~±13.2	14P4	General office automation equipment	5-49
M75189P/FP	Quad RS-232C receiver	Bip	5±5%	P : 14P4 FP : 14P2N	General office automation equipment	5-53
M75189AP/AFP						5-58
M751701P	RS-232C transceiver	Bip	±4.5~±15	8P4	General office automation equipment	5-63
M753114P	High-speed photo-coupler driver/receiver	Bip	5±5%	8P4	PPC, FAX, factory automation	5-67

■CROSSPOINT SWITCH

Type name	Function	Process	Supply voltage	Outline	Application/field	Page
M402100BP/BFP	4×4 cross-point switch	CMOS	5~15	P : 16P4 FP : 16P2N	Line swiching for telephone set or communication equipment (PBX, button telephone set)	6-3
M402101BP/BWP	4×8 cross-point switch		5~15	P : 22P4H WP : 22P4		6-11

★★ : Under Development

INDEX BY FUNCTION

■M74HC-1 SERIES

ORDERING INFORMATION

The type codes and package outline of the Mitsubishi semiconductor integrated circuits are outlined below for your reference.

Example 1) Products

M 66 300 FP
M 5A26LS 31 P
M 74HC 534-1 P

- P — Package type
- 534-1 — Specification for each circuit
- 74HC — Application, series, or circuit type
- M — Mitsubishi's code

Example 2) Package

24 P 4 B

- B — Supplementary code
- 4 — Package outline
- P — Package structure
- 24 — Number of pins

SYMBOLOGY

Symbol	Description	
C_I	Input capacitance	The output capacitance at input terminals
C_L	Load capacitance	Externally connected output capacitance
C_O	Output disable capacitance	The output capacitance when the output is in the high-impedance state
C_{PD}	Power dissipation capacitance	The internal capacitance of the IC calculated from the power dissipation
f_I	Input frequency	The sine wave frequency applied to the input terminal
f_ϕ	Clock frequency	
f_{max}	Maximum repetition frequency	The maximum frequency of repetitive inputs at which the device operates normally
GND	Ground	
H	High level	Used as a suffix for current and voltage parameters to indicate the high logic level
I	Current or input	Currents flowing into the IC are positive, currents flowing out of the IC are negative
I_{CC}	Supply current	The current flowing into the IC at the V_{CC} pin
I_{DD}	Supply current	The current flowing into the IC at V_{DD} pin
I_I	Input current	The current that flows into the IC when an input voltage is applied
I_{IH}	High-level input current	The input current for a high-level input
I_{IL}	Low-level input current	The input current for a low-level input
I_O	Output current	Currents flowing into the IC are positive, currents flowing out of the IC are negative.
I_{OFF}	Input off-state leak current	The leakage between the input and output terminals of an analog switch in the off state
I_{OH}	High-level output current	Output load current in the high-level output state
I_{OL}	Low-level output current	Output load current in the low-level output state
I_{OS}	Output short circuit current	Output current for short circuit to GND in the high-level output state
I_{OZH}	Off-state high-level output current	Output current when logic high is applied to an output in the high-impedance state
I_{OZL}	Off-state low-level output current	Output current when logic low is applied to an output in the high-impedance state
L	Low level	Used as a suffix for current and voltage parameters to indicate the low logic level
O	Indicates output	
P_d	Power dissipation	The product of the supply voltage and supply current
PRR	Repetitive frequency	Pulse frequency supplied repetitively
R_I	Input resistance	External resistance connected at input
R_L	Load resistance	External load resistance
R_{OFF}	Analog switch off resistance	The resistance of an analog switch in the off state
R_{ON}	Analog switch on resistance	The resistance of an analog switch in the on state
T_a	Ambient temperature	The air temperature in the vicinity of the IC
t_f	Fall time	The period for an input pulse to change from logic high to low
t_h	Hold time	The period for another input must be held after a specified input is changed
T_{opr}	Operating (ambient) temperature	The ambient temperature range over which the IC will operate correctly
t_{pd}	Propagation delay time	The period from when the specified input is applied until the specified output changes
t_{PHL}	High-level to low-level output propagation time	The period required for the output to change from logic high to low after the specified input is applied
t_{PHZ}	Output disable time from high-level	The period required for the output to change from logic high to the high-impedance state after the specified input is applied
t_{PLH}	Low-level to high-level output propagation time	The period required for the output to change from logic low to high after the specified input is applied
t_{PLZ}	Output disable time from low level	The period required for the output to change from logic low to the high-impedance state after the specified input is applied
t_{PZH}	Output enable time from high-level	The period requied for the output to change from the high-impedance state to logic high after the specified input is applied
t_{PZL}	Output enable time to low-level	The period requied for the output to change from the high-impedance state to logic low after the specified input is applied
t_r	Rise time	The period for an input pulse to change from logic low to high
t_{rec}	Recovery time	The period required from when the input state is released until the next clock pulse can be applied
T_{stg}	Storage temperature	The temperature range over which the IC can be safely stored
t_{SU}	Setup time	The period that other specified inputs must be held before the specified input can be applied
t_{THL}	High-level to low-level output transition time	The time required for the output to fall after the specified input is applied
t_{TLH}	Low-level to high-level output transition time	The time required for the output to rise after the specified input is applied
t_W	Pulse width	The period over which a pulse remains within the reference voltage range

SYMBOLOGY

Symbol	Description	
V_{CC}	Supply voltage	The voltage applide to the V_{CC} pin
V_{DD}	Supply voltage	The voltage applied to the V_{DD} pin
V_{EE}	Supply voltage	The voltage applied to the V_{EE} pin
V_H	Hysteresis voltage	The difference between the positive-going and negative-going threshold voltage of a Schmitt trigger circuit
V_I	Input voltage	The voltage applied to an input
V_{IC}	Input clamp voltage	Forward voltage of input clamp diode
V_{IH}	High-level input voltage	The logic high voltage applied to an input
V_{IL}	Low-level input voltage	The logic low voltages applied to an input
V_O	Output voltage	The voltage applied to or appearing at an output.
V_{OH}	High-level output voltage	The voltage at the output in the high-level state
V_{OL}	Low-level output voltage	The voltage at the output in the low-level state
V_P	Pulse amplitude	Voltage between low-level and high-level of a pulse
V_{SS}	Supply voltage	The voltage applied at the V_{SS} pin
V_T	Threshold voltage	The input voltage level where the output state changes.
V_{T+}	Positive-going threshold voltage	The threshold voltage for the low-to-high state change
V_{T-}	Negative-going threshold voltage	The threshold voltage for the high-to-low state change
Z	High-impedance state	Indicates an output in the high-impedance state
Z_O	Output impedance	Load impedance to be connected to the output of a pulse generator

QUALITY ASSURANCE AND RELIABILITY

1. INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances, high integration, high speed, and sophisticated functionality. Now they have almost boundless applications in electronic systems and electrical appliances.
To meet the above trend of expanding utilization of IC & LSI, Mitsubishi finds it extremely important to supply good quality and highly reliable products to customers "Quality First" is the basic policy at Mitsubishi Electric and a great deal of emphasis is placed on it. Mitsubishi has established a "Quality Assurance System" that is applied to design, manufacturing, inventory and delivery for ICs & LSIs. This system has helped to supply reliable products to customers for many years.
The following describes the Quality Assurance System and how it applies to reliability control for Mitsubishi digital ASSP:

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in design and built-in quality in manufacturing. The System from development to delivry is summarized in Fig.1.

2.1 Quality Assurance in Design

The following steps are applied to design stages for new products.
(1) Establishing targets for performance, quality and reliability.
(2) Discussion of performance and quality for circuit design, device structure, process, material and packaging.
(3) Verification of design by CAD system to meet standardizations.
(4) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure mechanism.
(5) Reliability test (in-house qualification) for new product to confirm quality and reliability target.
(6) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery, etc..

2.2 Quality Assurance in Manufacturing

The following steps are applied to manufactuing:
(1) Environmental control such as temperature, humidity and dust as well as de-ionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipment, automatic testing equipments, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, masks and chemicals.
(4) In-process inspections for wafer-fabrication, assembly and testing.
(5) Electrical characteristics test and visual inspection.
(6) Lot by lot sampling and environmental and periodical endurance test.
(7) Inventory and shipping control, such as storage environment, data code identity handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product, tests are performed at three different stages, new product development, pre-production and mass-production.
With the development of new products the reliability tests are modeled to correspond to quality and reliability targets. The test plan includes in-house qualification test, and TEG evaluation. TEG chips are designed and prepared for new device structures, new processes and new materials. After the proto-type product has passed the in-house qualification test, the product advances to the next stage of pre-production. It is in this stage, that specific reliability tests are performed again to verify quality.
During mass production, the reliability tests are performed periodically to confirm the quality of the product according to the Quality Assurance System.
Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

2.4 Returned Product Control

When failure analysis is request by a customer, the failed devices are returned to Mitsubishi Electric via the sales office.

Table 1 TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test		Test condition
1	Solderability		230℃, 5sec, Rosin flux
2	Soldering heat		260℃, 10sec
	Thermal shock		125℃, −55℃, 5 min each, 15 cycles (liquid phase)
	Temperature cycle		−65℃, 150℃, 30 min each, 100 cycles (air phase)
3	Lead fatigue	Bending	250gr, 90 degrees 2 times
		Stretch	500gr, 30 sec
4	Mechanical shock		1500G, 0.5msec, three times
	Vibration		200G, 100~2000Hz, X, Y, Z directions 4min /cycle, four times each direction
	Constant acceleration		20000G, Y direction, 1min
5	Operating life		$T_a \geqq T_{opr}max$, $V_{CC}=V_{CC}max$ 1000hours
6	High temperature storage life		$T_a=T_{stg}max$, 1000hours
7	High temperature and high humidity		T_a=85℃, 85%R H 1000hours
	Pressure cooker		T_a=121℃, 100%R H 96hours

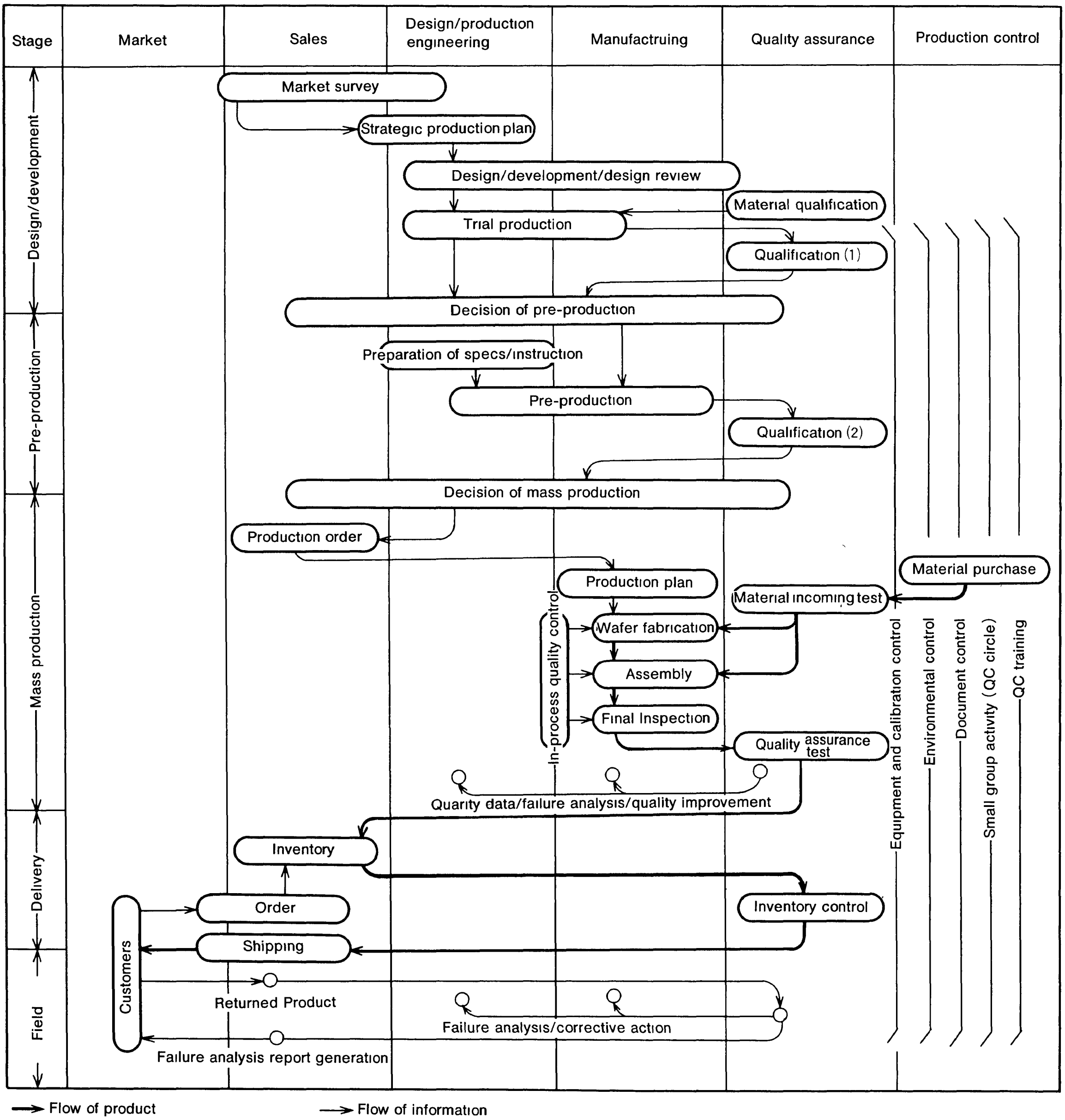


Fig. 1 Flow chart of quality assurance system

Mitsubishi provides various failure analysis equipments to analyze the returned product. A failure analysis report is given to the customer upon completion of the analysis. The analysis report is then used to apply corrective measures for design, fabrication, assembly or testing to ultimately improve reliability and realize a lower failure rate.

Fig. 2 shows the procedure of returned product control from customer.

3. RELIABRLITY TEST RESULTS

The reliability test results for Mitsubishi digital ASSP are shown in Table 2 to Table 6.

Table 2 QUALITY ASSURANCE TEST RESULTS (1)

Application	Type Number \ Parameter	High temperature Operating Life (T_a=125℃, V_{CC}=V_{CCmax}) Number of Samples	Device Hour	Number of Failures	High Temperature Storage (T_a=150℃, 1000 hours) Number of Samples	Number of Failures
Original High-speed CMOS Logic	M74HCXXX-1P	266	266000	0	132	0
	M74HCXXX-1FP	132	132000	0	88	0
Cross-point Switch	M402100BP	40	80000	0	22	0
	M402100BFP	22	22000	0	22	0
	M402101BP	32	32000	0	22	0
	M402101BWP	32	32000	0	22	0
DRAM Controller and Peripheral IC	M66200AP	38	76000	0	22	0
	M66200AFP	32	32000	0	22	0
	M66210P	38	38000	0	22	0
	M66210FP	22	22000	0	22	0
	M66212P	38	38000	0	22	0
High-drive High-speed Parallel I/O Expander	M66500SP	32	64000	0	22	0
	M66500FP	22	22000	0	22	0
Toggle Line Buffer	M66305P	32	32000	0	22	0
	M66305FP	32	32000	0	22	0
Parallel-in serial-out data buffer with FIFO	M66300P	38	38000	0	32	0
	M66300FP	22	22000	0	22	0
Line Interface	M75188P	38	38000	0	22	0
	M75189P	38	38000	0	22	0
	M75189AP	38	38000	0	—	—
	M75189AFP	22	22000	0	22	0
	M751701P	38	38000	0	22	0
	M5A26LS29P	38	38000	0	22	0
	M5A26LS31P	38	38000	0	22	0
	M5A26LS31FP	22	22000	0	22	0
	M5A26LS32AP	38	38000	0	—	—
	M5M34050P	38	38000	0	—	—
	M75173P	38	38000	0	22	0
Application Specific Driver	M66310P	32	32000	0	22	0
	M66310FP	22	22000	0	22	0
	M66311P	32	32000	0	22	0
	M66311FP	22	22000	0	22	0
	M66312P	32	32000	0	22	0
	M66312FP	22	22000	0	22	0
	M66700P	55	55000	0	22	0
	M66705P	22	22000	0	—	—
	M66705FP	22	22000	0	22	0
	M751270P	32	32000	0	22	0
	M751270FP	22	22000	0	22	0
	M751271P	32	32000	0	—	—
	M751272P	32	32000	0	22	0
	M751272FP	22	22000	0	32	0
	M751273P	32	32000	0	—	—
	M753114P	32	32000	0	32	0

Table 3 QUALITY ASSURANCE TEST RESULTS (2)

Application	Type Number	Soldering Heat 270℃, 10 seconds: Number of Samples	Soldering Heat 270℃, 10 seconds: Number of Failures	Thermal Shock −55～125℃, 15 Cycle: Number of Samples	Thermal Shock −55～125℃, 15 Cycle: Number of Failures	Temperature Cycle −65～150℃, 100 Cycle: Number of Samples	Temperature Cycle −65～150℃, 100 Cycle: Number of Failures
Original High-speed CMOS Logic	M74HCXXX-1P	228	0	228	0	228	0
	M74HCXXX-1FP	192	0	192	0	192	0
Cross-point Switch	M402100BP	22	0	22	0	22	0
	M402100BFP	22	0	22	0	22	0
	M402101BP	32	0	32	0	32	0
	M402101BWP	32	0	32	0	32	0
DRAM Controller and Peripheral IC	M66200AP	32	0	32	0	32	0
	M66200AFP	32	0	32	0	32	0
	M66210P	32	0	32	0	32	0
	M66211FP	32	0	32	0	32	0
	M66213P	32	0	32	0	32	0
High-drive High-speed Parallel I/O Expander	M66500SP	32	0	32	0	32	0
	M66500FP	22	0	22	0	22	0
Toggle Line Buffer	M66305P	32	0	32	0	32	0
	M66305FP	32	0	32	0	32	0
Parallel-in serial-out data buffer with FIFO	M66300P	45	0	45	0	45	0
	M66300FP	45	0	45	0	45	0
Line Interface	M75188P	38	0	38	0	38	0
	M75189P	38	0	38	0	38	0
	M75189AP	38	0	38	0	38	0
	M75189AFP	38	0	38	0	38	0
	M751701P	38	0	38	0	38	0
	M5A26LS29P	38	0	38	0	38	0
	M5A26LS31P	38	0	38	0	38	0
	M5A26LS31FP	38	0	38	0	38	0
	M5A26LS32AP	38	0	38	0	38	0
	M75173P	38	0	38	0	38	0
Application Specific Driver	M66310P	32	0	32	0	32	0
	M66310FP	32	0	32	0	32	0
	M66311P	32	0	32	0	32	0
	M66311FP	32	0	32	0	32	0
	M66312P	32	0	32	0	32	0
	M66312FP	32	0	32	0	32	0
	M66700P	32	0	32	0	32	0
	M66705P	32	0	32	0	32	0
	M66705FP	32	0	32	0	32	0
	M751270FP	32	0	32	0	32	0
	M751271P	32	0	32	0	32	0
	M751272P	32	0	32	0	32	0
	M751272FP	32	0	32	0	32	0
	M751273P	32	0	32	0	32	0
	M753114P	32	0	32	0	32	0

Table 4 QUALITY ASSURANCE TEST RESULTS (3)

Application	Type Number	High Temperature High Humidity Bias (85℃, 85%RH, $V_{CC}=V_{CCmax}$) Number of Samplse	Device Hour	Number of Failures	Pressure Cooker (121℃, Barometric height 2, 240 hours) Number of Samples	Number of Failures
Original High-speed CMOS Logic	M74HCXXX-1P	190	1000	0	190	0
Cross-point Switch	M402100BP	40	1000	0	40	0
	M402101BP	32	1000	0	32	0
	M402101BWP	32	1000	0	32	0
DRAM Controller and Peripheral IC	M66200AP	38	2000	0	38	0
	M66210P	—	—	—	38	0
	M66211P	38	1000	0	—	—
	M66212P	38	1000	0	38	0
High-drive High-speed Parallel I/O Expander	M66500SP	22	2000	0	32	0
Toggle Line Buffer	M66305P	22	2000	0	22	0
Parallel-in serial-out data buffer with FIFO	M66300P	32	2000	0	45	0
Line Interface	M75188P	38	1000	0	45	0
	M75189P	38	1000	0	45	0
	M75189AP	38	1000	0	—	—
	M751701P	38	1000	0	45	0
	M5A26LS29P	38	1000	0	45	0
	M5A26LS31P	38	1000	0	45	0
	M5A26LS32AP	38	1000	0	45	—
	M5M34050P	38	1000	0	—	—
	M75173P	—	—	—	45	0
Application Specific Driver	M66310P	32	2000	0	32	0
	M66311P	32	1000	0	32	0
	M66312P	32	2000	0	32	0
	M66700P	32	2000	0	32	0
	M66705P	22	1000	0	32	0
	M751270P	32	2000	0	—	—
	M751271P	32	1000	0	32	0
	M751272P	32	1000	0	32	0
	M751273P	—	—	—	32	0
	M753114P	32	1000	0	32	0

Table 5 QUALITY ASSURANCE TEST RESULTS (4)

Application	Type Number	High Temperature High Humidity Bias Note 1 (85℃, 85%RH, $V_{CC}=V_{CCmax}$) Number of Samples	Device Hour	Number of Failures	Pressure Cooker (121℃, Barometric height 2, 240 hours) Number of Samples	Number of Failures
Original High-speed CMOS Logic	M74HCXXX-1FP	88	1000	0	66	0
Cross-point Switch	M402100BFP	22	1000	0	22	0
DRAM Controller and Peripheral IC	M66200AFP	32	1000	0	32	0
	M66210FP	22	1000	0	—	—
	M66211FP	22	1000	0	32	0
	M66212FP	22	1000	0	—	—
High-drive High-speed Parallel I/O Expander	M66500FP	22	1000	0	22	0
Toggle Line Buffer	M66305FP	22	1000	0	22	0
Parallel-in serial-out data buffer with FIFO	M66300FP	22	1000	0	32	0
Line Interface	M75189AFP	22	1000	0	32	0
	M5A26LS31FP	22	1000	0	32	0
	M5A26LS32AFP	22	1000	0	—	—
	M5M34050FP	22	1000	0	—	—
	M75173FP	20	1000	0	—	—
Application Specific Driver	M66310FP	22	1000	0	32	0
	M66311FP	22	1000	0	32	0
	M66312FP	22	1000	0	32	0
	M66705FP	22	1000	0	32	0
	M751270FP	22	1000	0	22	0
	M751271FP	22	1000	0	—	—
	M751272FP	22	1000	0	22	0
	M751273FP	22	1000	0	—	—

Note 1 : Pre-processing is made as follows

○High temperature and high humidity storage·········85℃, 85% RH, 48 hours

↓

○Solder bath············260℃, 10 sec three times

High temperature and high humidity storage processing is not made for the M66500FP

Table 6 QUALITY ASSURANCE TEST RESULTS (5)

Application	Type Number	Solderability: Number of Samples	Solderability: Number of Failures	Terminal Strength: Number of Samples	Terminal Strength: Number of Failures	(Remarks) Package Number of Pins
Test Condition		230℃, 5 sec, flux		Bending, Three Times, 85g/250g		
Original High-speed CMOS Logic	M74HCXXX-1P	88	0	60	0	16,20P4, 24P4D
	M74HCXXX-1FP	45	0	45	0	16,20P2N, 24P2
Cross-point Switch	M402100BP	22	0	15	0	16P4
	M402100BFP	15	0	15	0	16P2N
	M402101BP	22	0	15	0	22P4H
	M402101BWP	22	0	15	0	22P4
DRAM Controller and Peripheral IC	M66200AP	15	0	15	0	24P4D
	M66210P	15	0	15	0	24P2
	M66210FP	—	—	15	0	24P2
	M66211FP	15	0	—	—	24P2
High-drive High-speed Parallel I/O Expander	M66500SP	15	0	15	0	64P4B
	M66500FP	15	0	15	0	64P6W
Toggle Line Buffer	M66305P	15	0	15	0	20P4
	M66305FP	15	0	15	0	20P2W
Parallel-in serial-out data buffer with FIFO	M66300P	15	0	15	0	24P4D
	M66300FP	15	0	15	0	24P2
Line Interface	M75188P	22	0	22	0	14P4
	M75189P	22	0	—	—	14P4
	M75189AFP	22	0	22	0	14P2N
	M751701P	22	0	22	0	8P4
	M5A26LS29P	22	0	—	—	16P4
	M5A26LS31P	22	0	22	0	16P4
	M5A26LS31FP	22	0	22	0	16P2N
	M5A26LS32AP	—	—	22	0	16P4
Application Specific Driver	M66310P	15	0	15	0	24P4D
	M66310FP	15	0	15	0	24P2
	M66311P	15	0	15	0	24P4D
	M66311FP	15	0	15	0	24P2
	M66312P	15	0	15	0	16P4
	M66312FP	15	0	15	0	16P2N
	M66700P	15	0	15	0	8P4
	M751271P	22	0	15	0	16P4
	M751271FP	22	0	15	0	16P2N
	M751272P	22	0	15	0	16P4
	M751272FP	22	0	15	0	16P2N
	M751273P	22	0	—	—	16P4
	M753114P	15	0	15	0	8P4

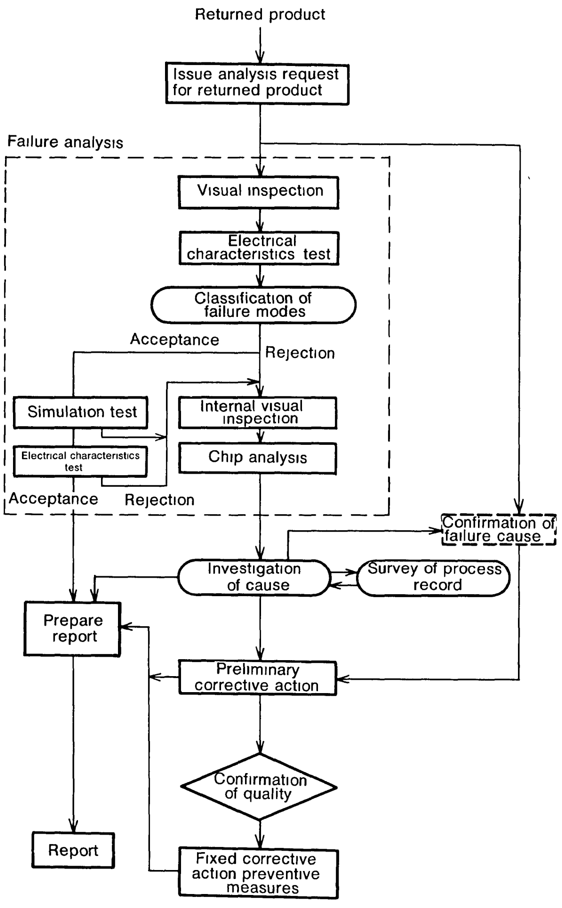


Fig. 2 Procedure of returned product control

4. SUMMARY

The Mitsubishi Quality Assurance System and example of reliability control have been presented. The customer's requirements for high reliability ICs & LSIs are increasing significantly. To satisfy the customer's demands Mitsubishi would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage. Reliability evaluations to expose latent failure modes and acceleration factors.

(2) Periodical endurance, environmental and mechanical testing to verify reliability targets and realize higher reliability.

(3) Focus on development for new failure analysis techniques. Detailed failure analysis, intensive corrective actions and quick response to customer's analysis request.

(4) Utilizing customer's quality data information regarding incoming inspection, production and field to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi kindly requests customers to provide quality/reliability data upon incoming inspection or field failure rate. These factors will be essential to help verify and improve the quality reliability of our ICs & LSIs.

PRECAUTION OF USE

Introduction
This section describes precautions for use of Mitsubishi digital ASSP. Mitsubishi recommends that you take care in logic design and system design by making use of the following application notes.

1. Unused Input Pins
Unused input pins, if left open, are considered to be high-level for BIPOLAR circuits and misoperation may occur due to enviromental noise.
Floating input voltage in CMOS circuit causes unstable operation and fluctuation in the output logical level. In any case, unused input pins should be connected to GND or V_{CC}. If unused blocks of circuits exist in a package, I_{CC} may increase when the input pins of the block are left open. Be sure to connect these input pins to GND or V_{CC}.

2. AND Tie of Output Pin
As active pull-up (current source) is used in the output circuit to enable high speed switching as well as to increase drive capacity of capacitative load, it is not possible to use an AND tie to connect each output pin to allow AND function. This is because the impedance of the active pull-up is low when the output is high-level. For example, when two outputs are connected and one output is high-level and the other output is low-level, excess current flows from high-level output pin to low-level output pin, increasing the low-level voltage. Increase of heat and current in the internal wiring may cause destruction and deterioration of reliability. This should be avoided by all means.

3. Shorting of Output Pin to GND or V_{CC}
The P-and N-channel transistors used in CMOS logic are not equipped with protection circuits to limit the output current. If output pins are accidentally shorted to V_{CC} or GND, excessive current will flow. These currents may cause overheating, damage to the IC's internal wiring, and deterioration of reliability. Therefore output pins should never be connected to GND or V_{CC} or any other fixed voltage level.

4. Output Load Capacitance
In many high-speed CMOS applications, capacitors are connected between I/O pins and either V_{CC} or GND to increase the propagation delay or to remove signal noises. Capacitors are charged by active pull-up from the power supply when the output changes from low-level to high-level and are discharged to GND via output transistors when the output changes from high-level to low-level. The larger the capacitors that are connected, the larger the charging/discharging energy via the IC's output circuit becomes, thus deteriorating the output circuit. A capacitor of less than 1000pF can be connected directly according to the output characteristics and charge/discharge cycle for an IC. If a larger capacitor is connected, resistors should be connected in series and the charge and discharge current should be limited.

5. Power Supply Lines
Fluctuation and ripples should be kept minimum within the recommended operating conditions.
To eliminate spikes generated by switching of ICs, the impedance of both the power supply and the supply line must be low. One method to lower this supply-line impedance is to connect a 0.01～0.22 μF plastic-film or ceramic capacitor with good high-frequency characteristics between the V_{CC} and GND lines. 10～100 μF electrolytic or tantalum capacitor should also be connected on each printed circuit board.
The power dissipation current varies widely with the operating frequency, supply voltage, capacitive load, supply voltage and input signal rise and fall times. The effect of these factors should be considered when designing the power supply. If digital circuits are used with high-current drivers, separate power supplies should be used for the logic and driver circuit, and common loads should be avoided.

6. Rise and Fall Time of the Input Signal
If a signal with long rise and fall times is applied to the input pin of the digital ASSP, the output may have a oscillation of several tens of MHz, abnormal waveform or misoperation. The rise and fall times of the input signal are specified in the timing requirement for some products. These products may cause misoperation if the input waveform is greater than the specified rise or fall time.
These products should be used within the upper or lower limits. The rise and fall times should be suppressed to the minimum even if the timing requirements of the products are not specified. However, products with Schmitt-trigger or hysteresis characteristics are exceptions.
Misoperation due to signals exceeding the rise or fall times can be prevented by revising the waveform with Schmitt trigger circuit.

7. Timing Requirement
The timing requirements specify the timing of input signals required to operate an IC normally. If the timing requirements are specified, these products should be used within these limits.

8. Parasitic Elements of Bipolar ICs

In the bipolar IC as shown in Fig. 1, transistors and diodes are surrounded by the p-channel area. The p-channel area is normally connected to GND. Between the GND pin and the n-channel area to form transistor collector, parasitic diodes are formed which are not described in the circuit diagram. Parasitic diodes are also connected between the GND pin and the supply voltage pin (V_{CC}) pin. Therefore, if the output level should be lower than the voltage of the GND pin, or if the IC is inserted backwards and the power is supplied, current flows through the parasitic diodes and the IC may be damaged. Care should be taken not to apply a voltage of -0.5V lower than to the GND pin. If -0.5V or less is applied to the input pin as shown in Fig. 1, most of the current flows from the GND pin to the input pin through Schottky barrier diode (SBD) , but part of the current flows from the base of the parasite transistors to the emitter and the collector current is amplified by the current amplification rate. The current flows from the collectors of the adjacent transistors to the input pin, and the collector current is drawn to the input pin, causing misoperation of the device. Care chould be taken not to apply a voltage lower than -0.5V to the I/O pins.

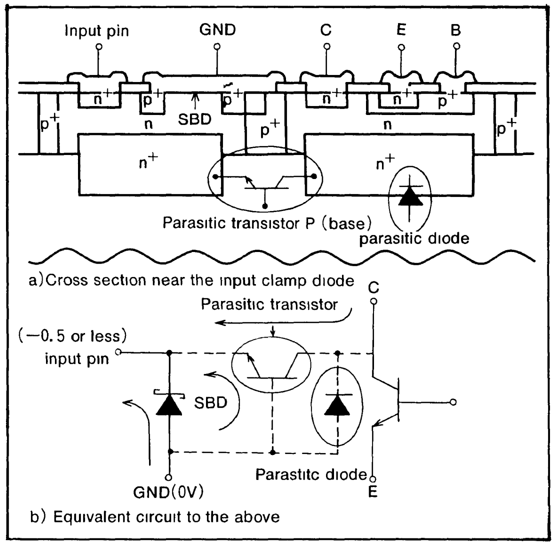


Fig. 1 Effect of parasitic transistor by the negative input voltage.

9. Latchup of CMOS IC

The CMOS circuit structure has built-in parasitic bipolar transistors. These transistor's function as thyristors (SCRs) : when they are triggered by an external surge, they turn on, causing a current to flow from V_{CC} to GND. Even after the trigger current ceases, this current continues to flow. The current is very large, and can easily damage or destroy the IC. For this reason, the phenomenon is called "latchup" . This section describes the mechanism and prevention method of latchup.

Fig. 2 shows the structure of a CMOS inverter and its parasitic bipolar transistors. T_{r1} and T_{r2} have pnpn thyristor structures. If any one of T_{r3}, T_{r4}, T_{r5} or T_{r6} turn on due to a current surge, a base current will flow to T_{r1} or T_{r2},initiating latchup. The following external factors can initiate latchup.

(1) Input voltage (V_I) exceeds supply voltage (V_{CC}).
$V_I > V_{CC}$
(2) Input voltage (V_I)falls below GND.
$V_I < GND$
(3) Output voltage(V_O)exceeds supply voltage (V_{CC}).
$V_O > V_{CC}$
(4) Output voltage (V_O) falls below GND.

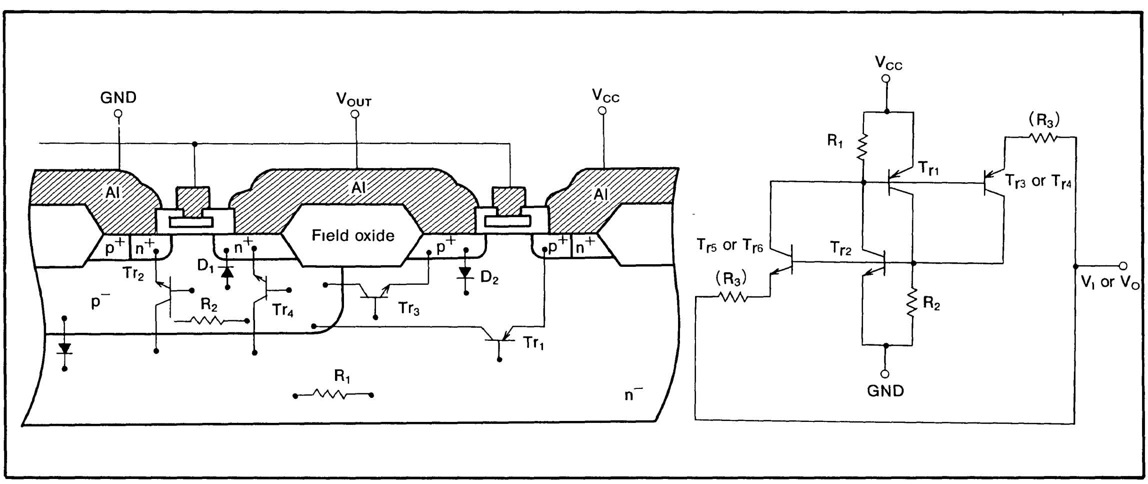


Fig. 2 COMS inverter mechanism and parasitic transistor.

V_O<GND

(5) Supply voltage (V_{CC}) becomes excessive. V_{CC} excessive.

Care should be taken not to allow an excessive surge to the I/O pin and the supply voltage pin.

10. Preventing Damage by Static Electricity

Static electricity is generated under low-humidity conditions by the friction of clothing, containers and other objects. Use of excellent protective circuits to all I/O pins, Mitsubishi digital ASSP devices can tolerate static voltages and this places them on equal footing with bipolar devices. However, the protection diodes that prevent static damage can tolerate only limited forward and reverse-bias currents. Large energy inputs should be avoided, as they will destroy these diodes and thin oxide layers at the transistor input gates. The following measures are recommended to prevent this type of damage.

(1) To prevent static damage during shipping, all ICs are shipped in conductive tubes. After receipt, the ICs should always be stored in conductive tubes or other conductive containers.

(2) Static charges on the body or clothing should be drained off by grounding through 100kΩ～1MΩ resistors.

(3) All assembly tubes, insertion machines, and measuring instruments, and other objects that will come in contact with the ICs should be grounded.

(4) Soldering irons and baths must have power-supply insulation resistances of over 10MΩ to prevent power-supply leakage to the IC_S. This equipment should also be grounded.

(5) Printed-circuit boards with IC_S installed should be protected from shock, vibration, and friction. To keep potential from building up, the boards should be stored in conductive envelopes, or the terminals should be shorted together.

(6) The humidity of the transport, storage and assembly environment should always be maintained at safe levels.

Mechanical and Thermal Stress

Cutting or deforming the external leads can result in lead breakage or humidity-induced corrosion. Mechanical stress should be avoided when mounting the IC_S. The component materials of IC_S have widely varying thermal-expansion coefficients, so rapid temperature changes, extended soldering and other thermal stresses should be avoided as far as possible because such stress can damage the semiconductors or break the internal wiring.

12. Caution for Surface-Mount Package

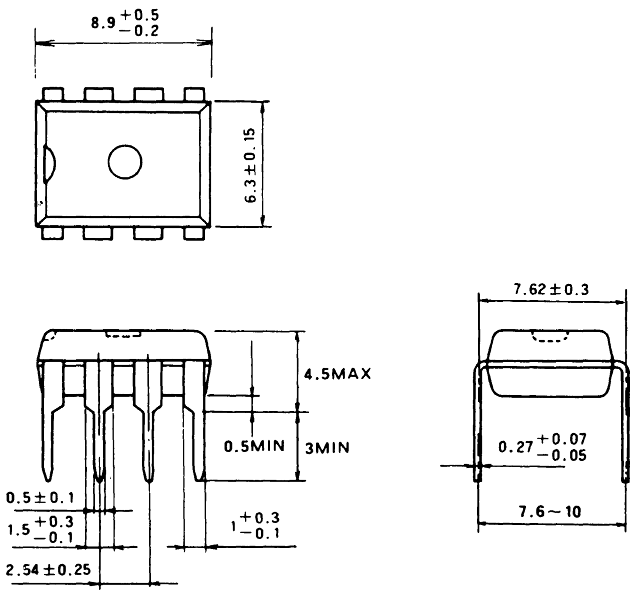
Surface-Mount packaging is available for most of Mitsubishi digital ASSP to miniaturize and make equipment lightweight. The allowable power dissipation of surface-mount packages is smaller than standard dual-in-line packages with the same number of pins. Please note some products have limitations on operating temperature and electrical characteristics.

Mounting method (soldering conditions), storage conditions, and cleaning conditions greatly influence the reliability of products but vary depending on the number of pins or the size of the package. Consult a Mitsubishi dealer for further information about the digital ASSP.

PACKAGE OUTLINE

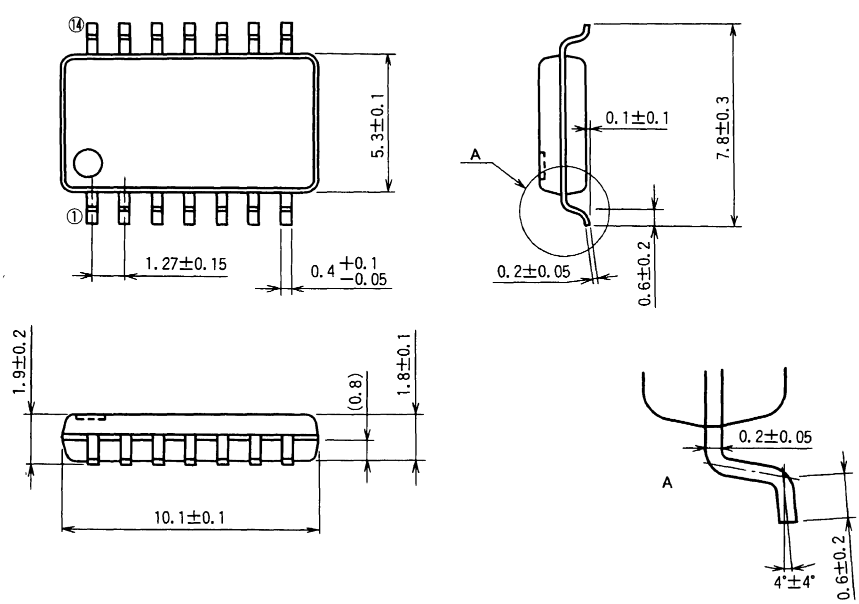
TYPE 8P4 8-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 14P2N 14-PIN MOLDED PLASTIC SOP

Dimension in mm

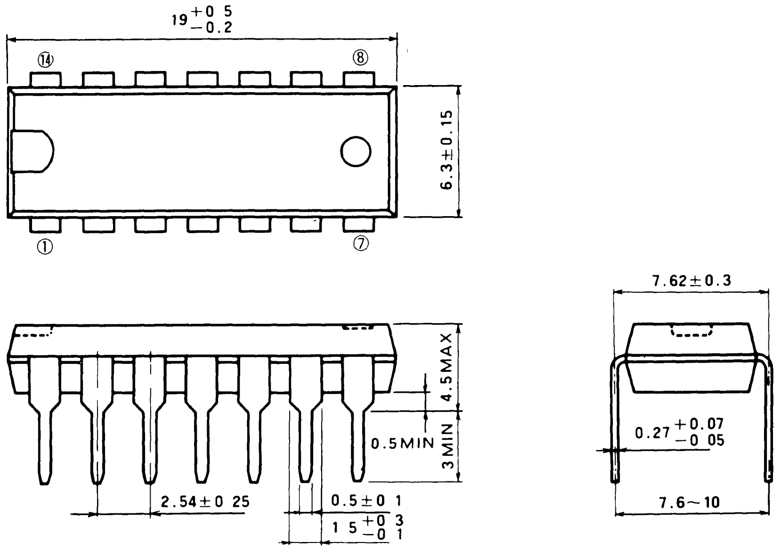


MITSUBISHI ELECTRIC

PACKAGE OUTLINE

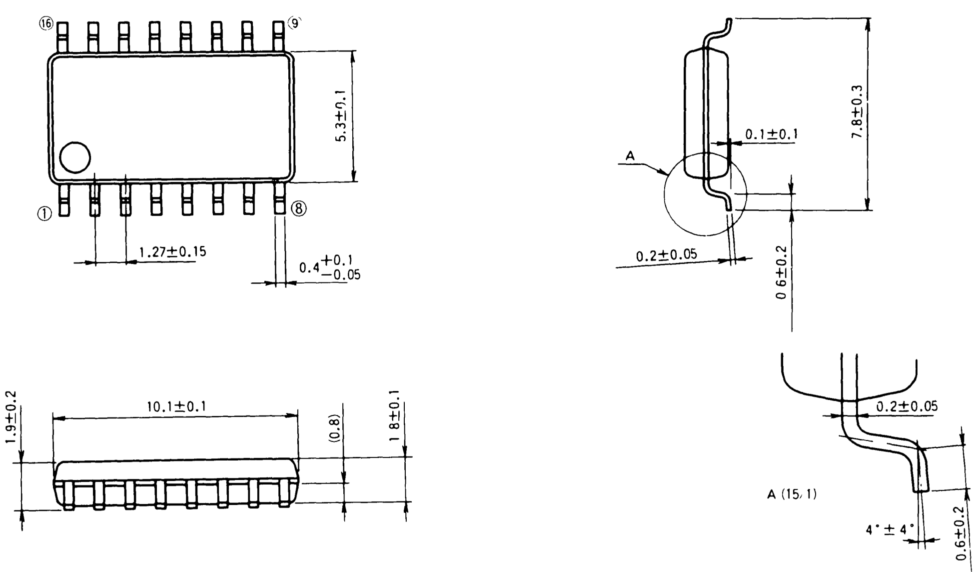
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



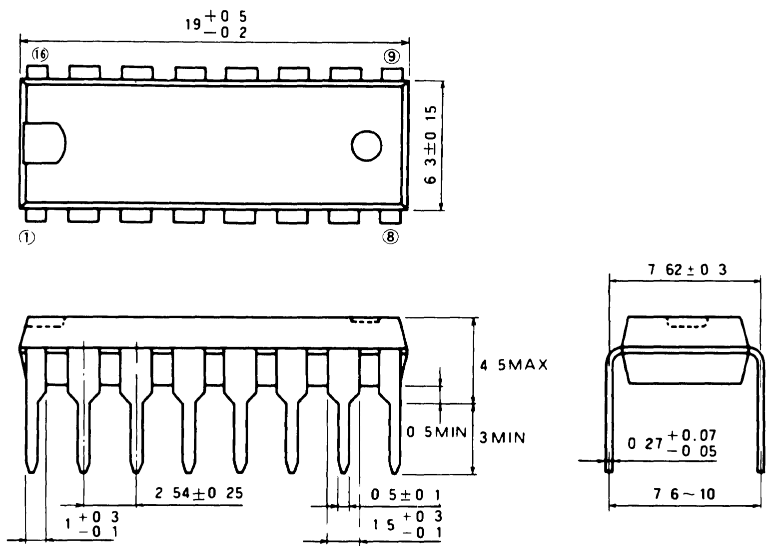
TYPE 16P2N 16-PIN MOLDED PLASTIC SOP

Dimension in mm



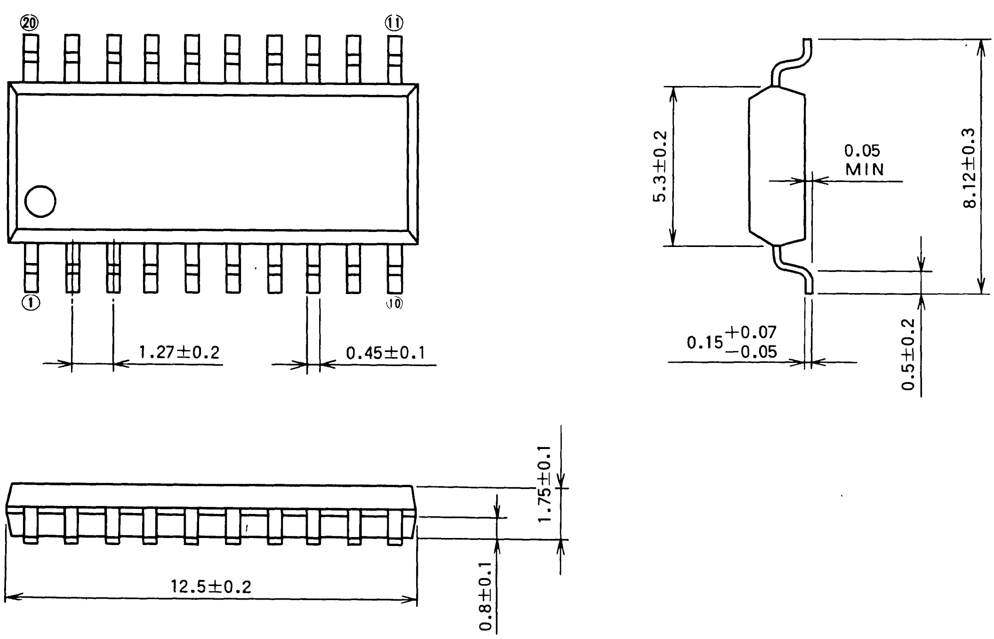
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 20P2 20-PIN MOLDED PLASTIC FLAT

Dimension in mm

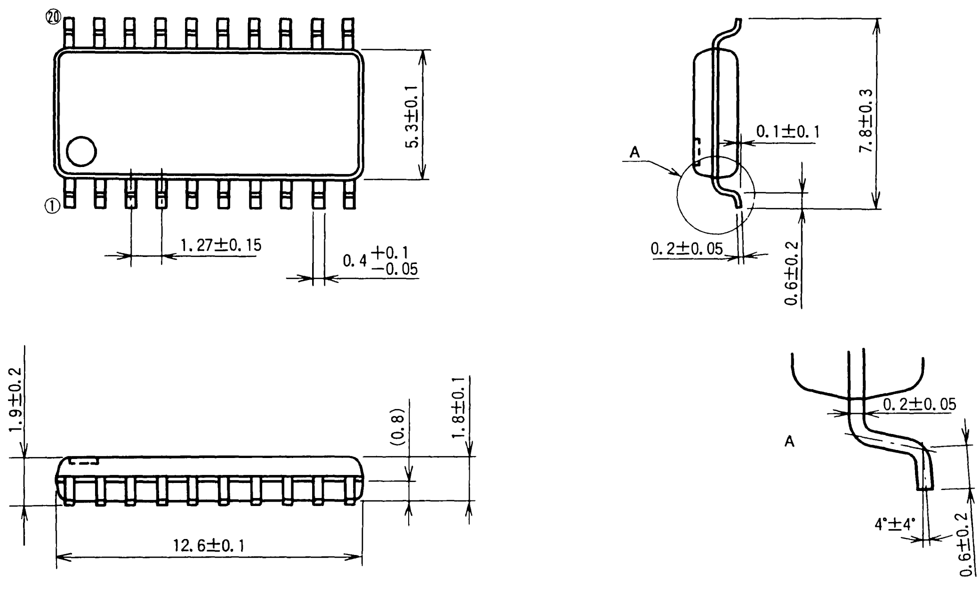


MITSUBISHI ELECTRIC

PACKAGE OUTLINE

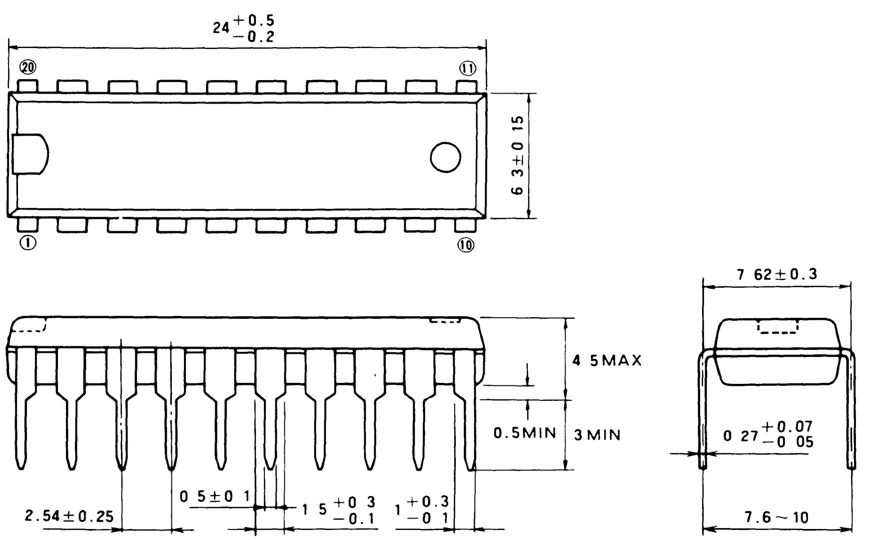
TYPE 20P2N 20-PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIP

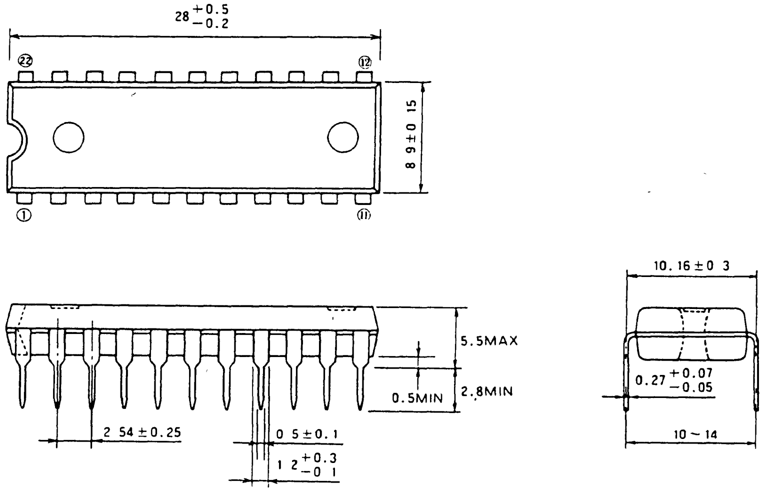
Dimension in mm



PACKAGE OUTLINE

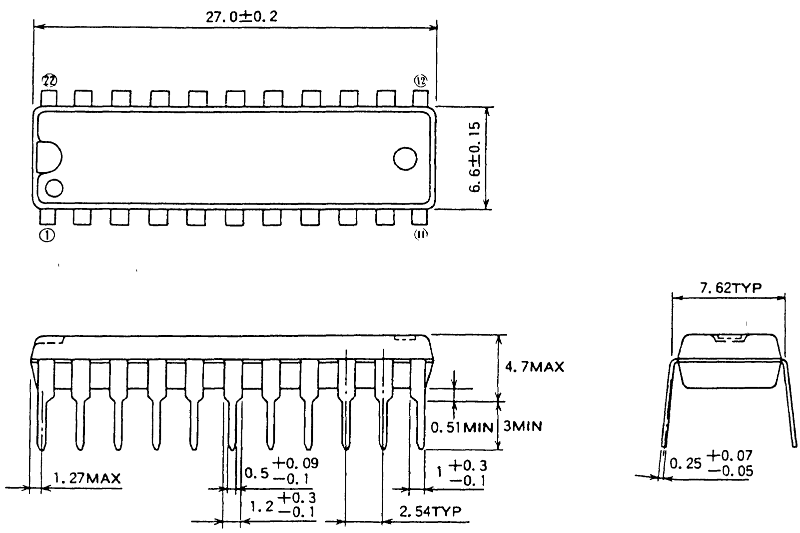
TYPE 22P4 22-PIN MOLDED PLASTIC DIP

Dimension in mm



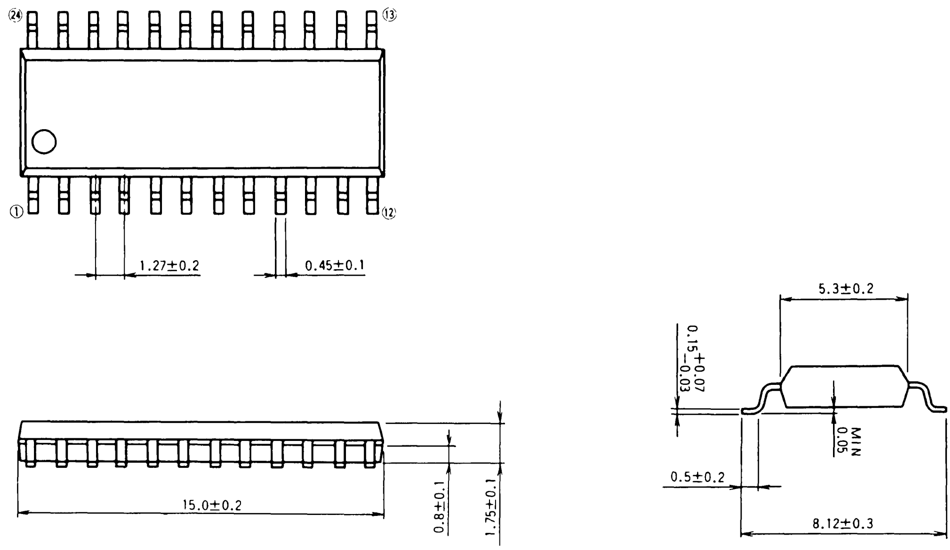
TYPE 22P4H 22-PIN MOLDED PLASTIC DIP

Dimension in mm



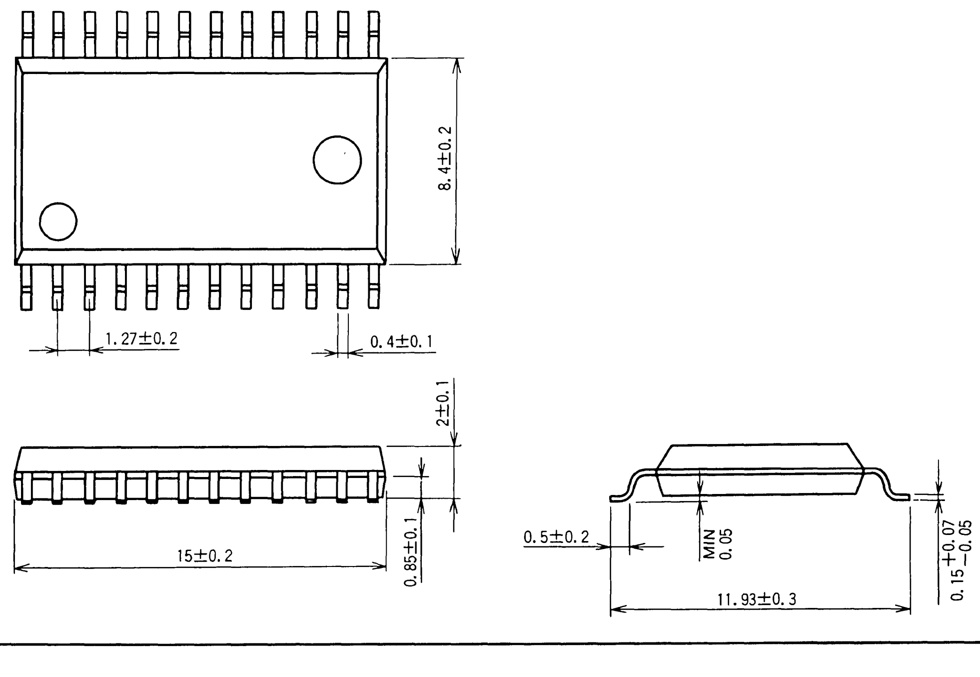
TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



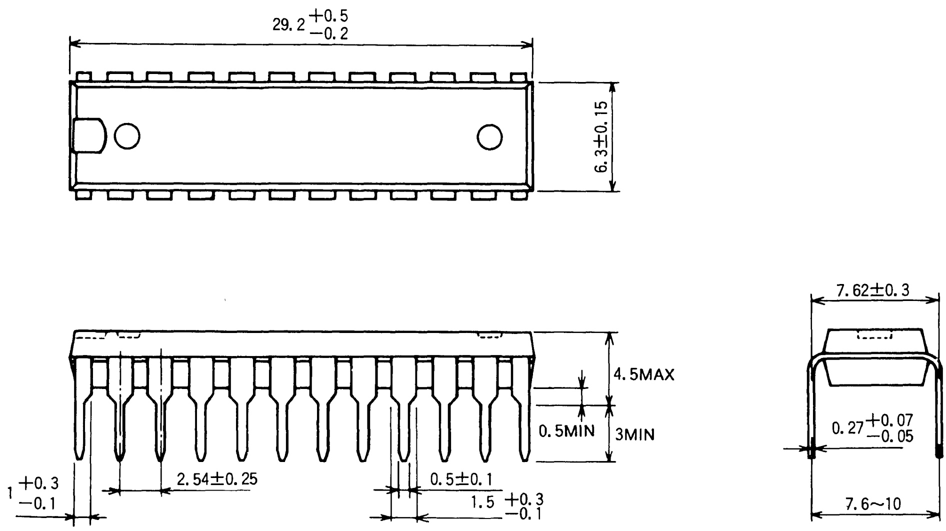
TYPE 24P2W 24-PIN MOLDED PLASTIC FLAT

Dimension in mm



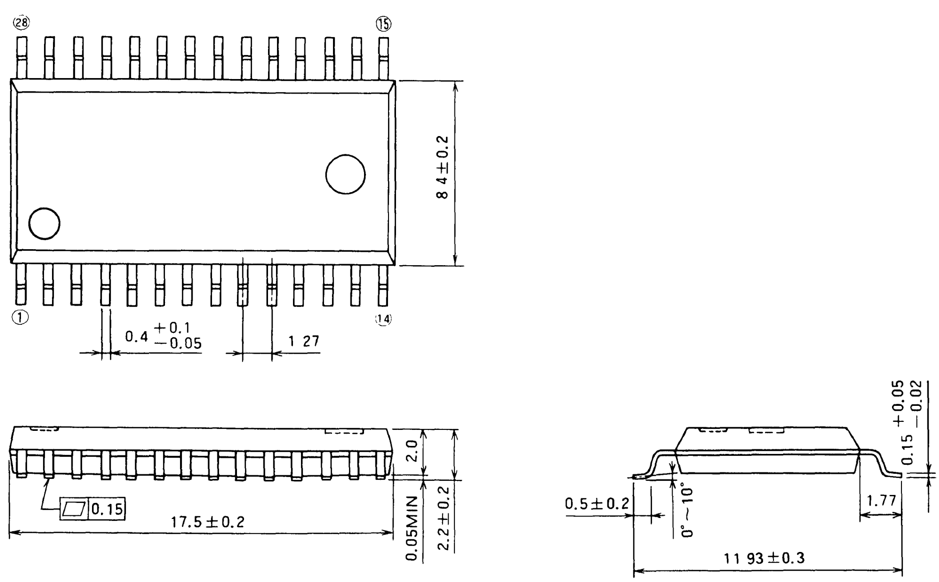
TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 28P2W 28-PIN MOLDED PLASTIC SOP

Dimension in mm



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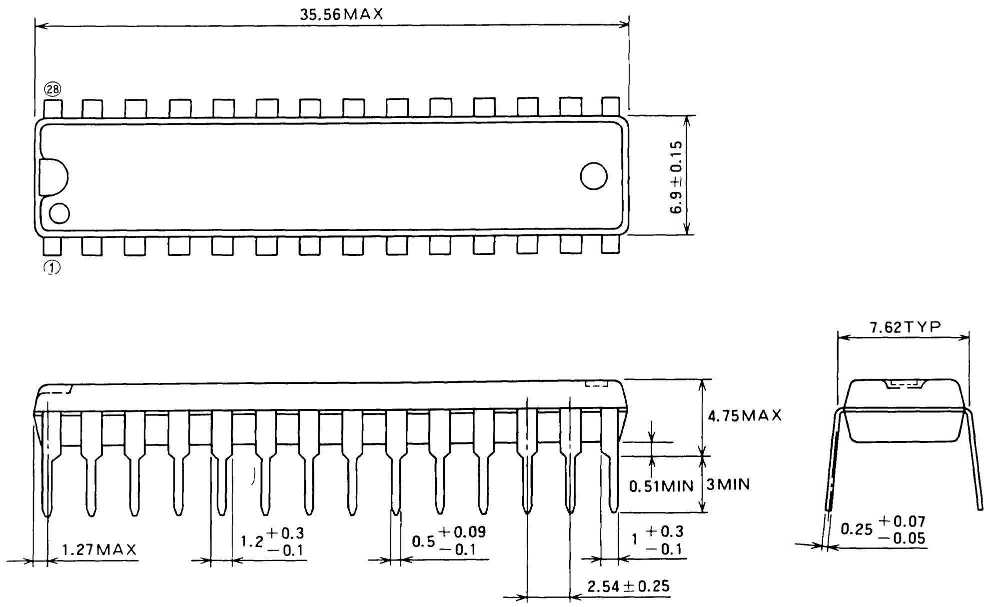
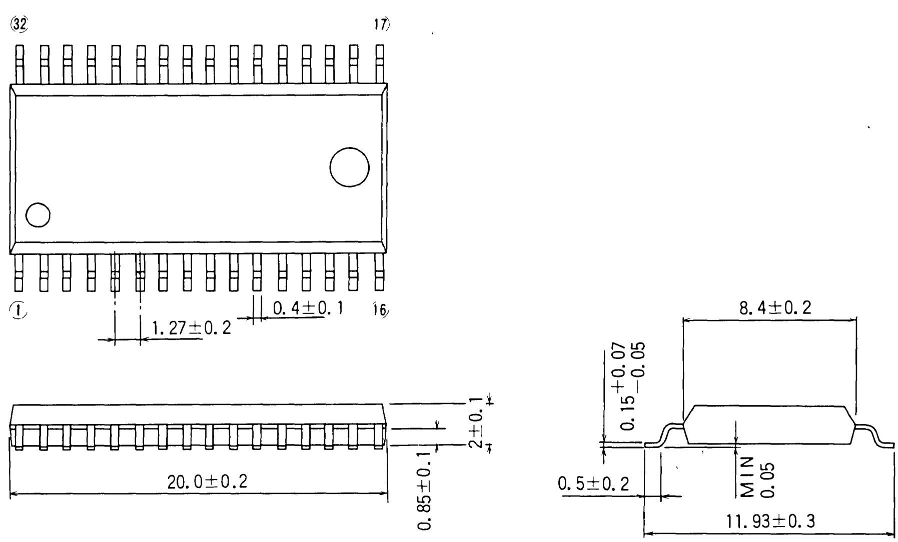
TYPE 28P4Y 28-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 32P2W 32-PIN MOLDED PLASTIC SOP

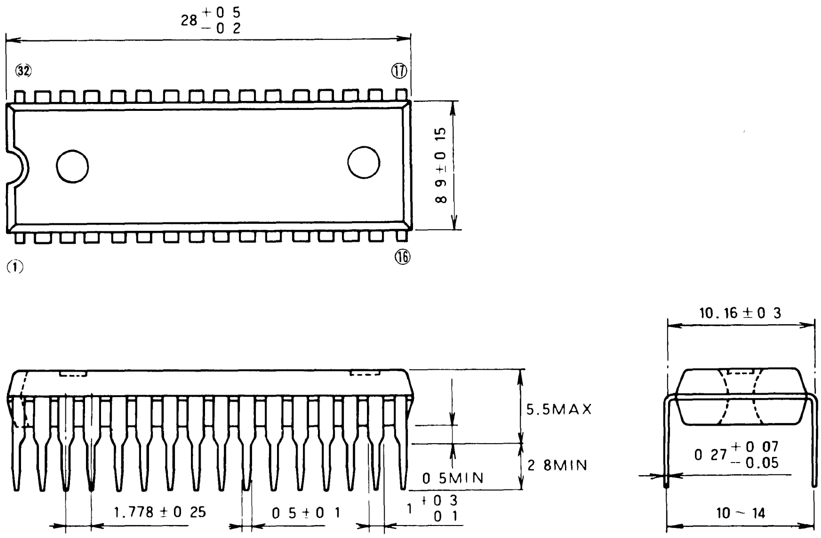
Dimension in mm



PACKAGE OUTLINE

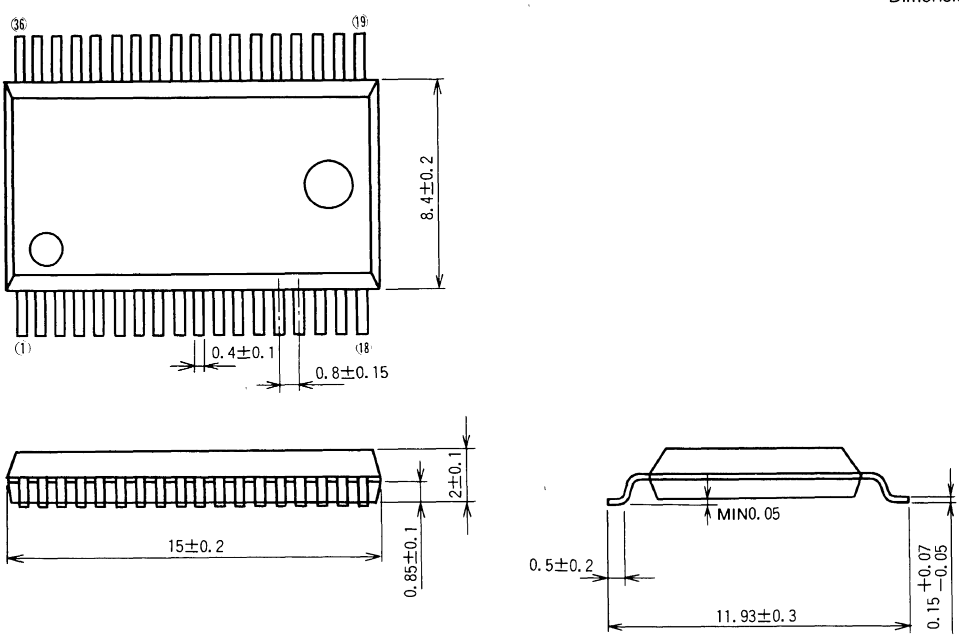
TYPE 32P4B 32-PIN MOLDED PLASTIC DIP (LEAD PITCH 1.778mm)

Dimension in mm



TYPE 36P2R 36-PIN MOLDED PLASTIC SOP

Dimension in mm

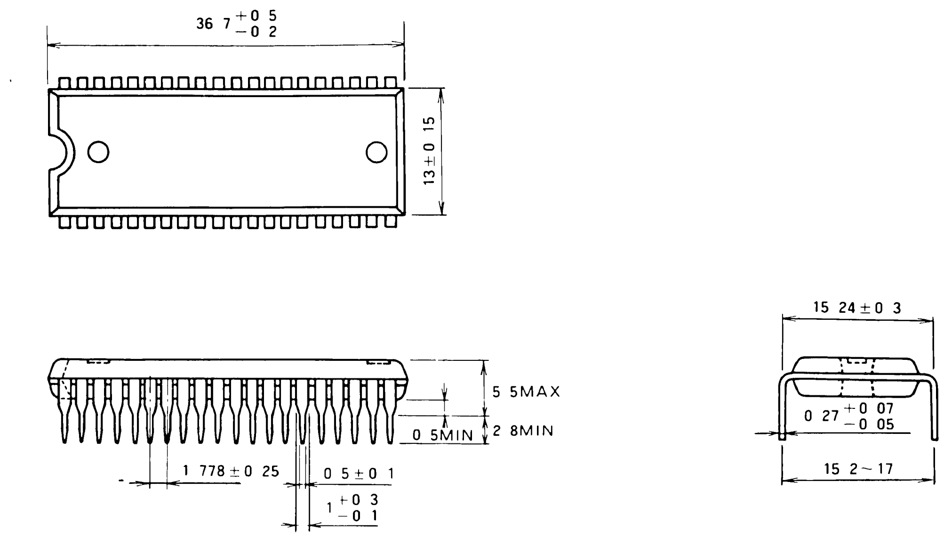


MITSUBISHI ELECTRIC

PACKAGE OUTLINE

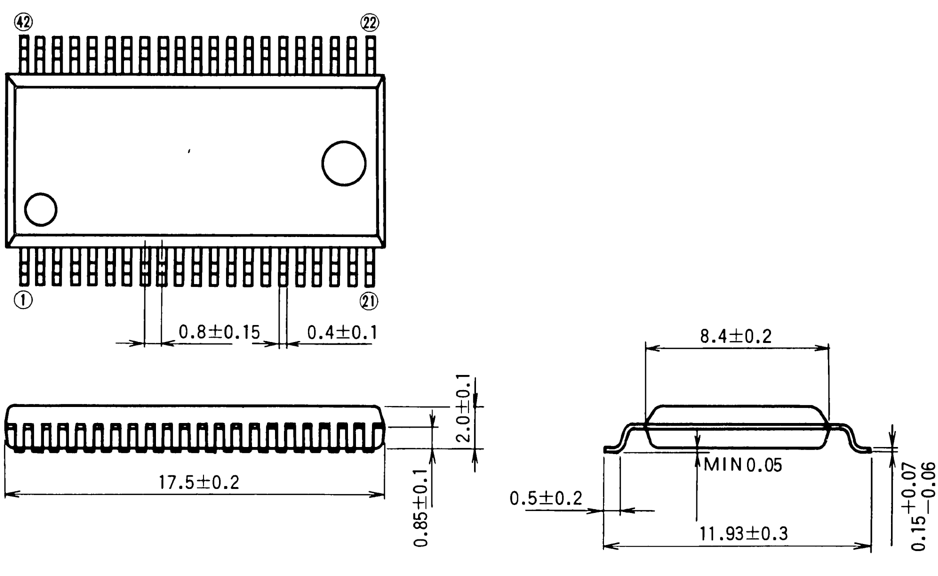
TYPE 40P4B 40-PIN MOLDED PLASTIC DIP(LEAD PITCH 1.778mm)

Dimension in mm



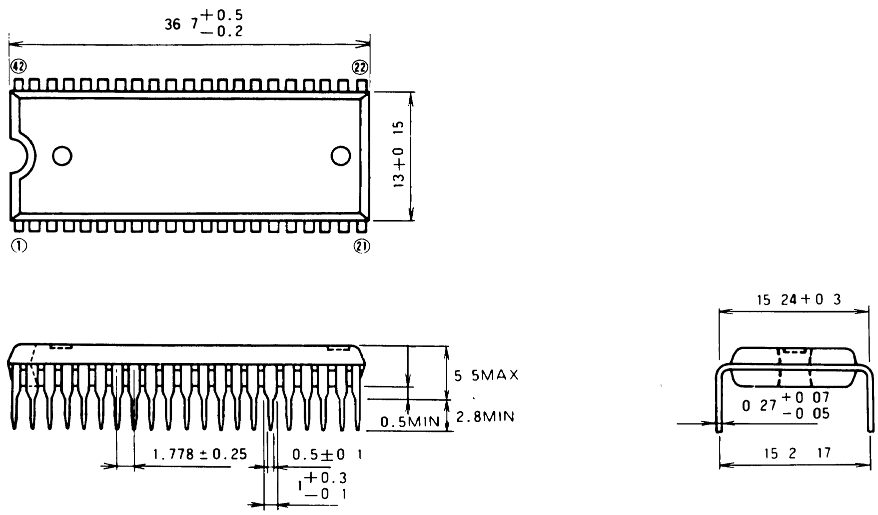
TYPE 42P2R 42-PIN MOLDED PLASTIC SOP

Dimension in mm



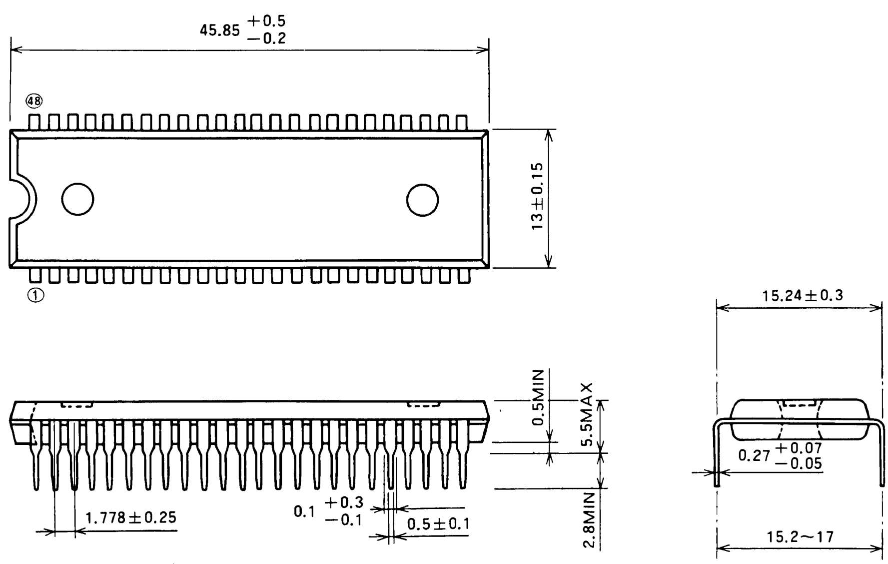
TYPE 42P4B 42-PIN MOLDED PLASTIC DIP(SHRINK)

Dimension in mm



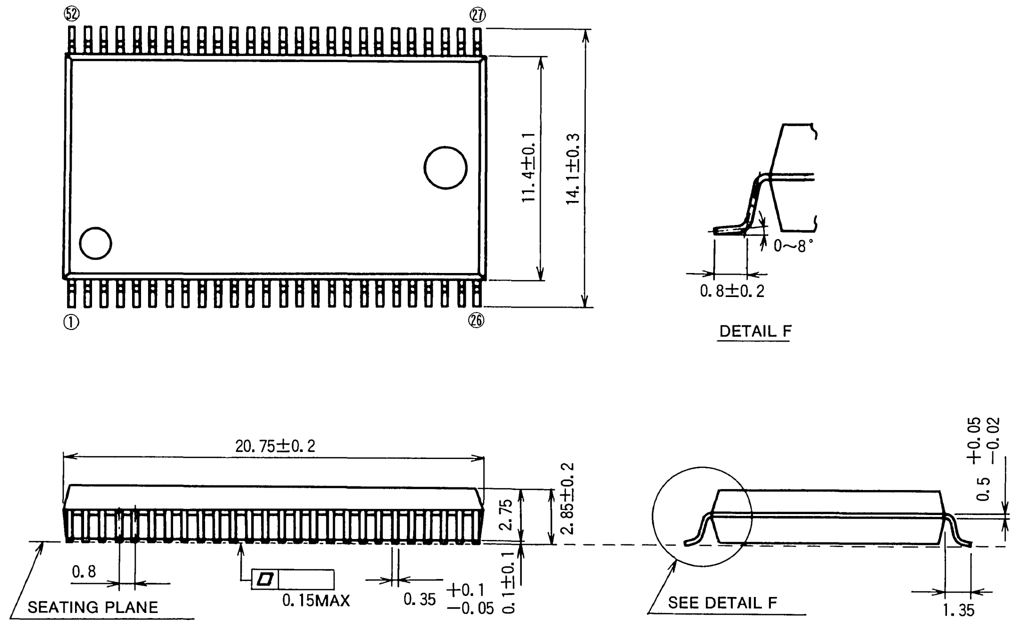
TYPE 48P4B 48-PIN MOLDED PLASTIC DIP (SHRINK)

Dimension in mm



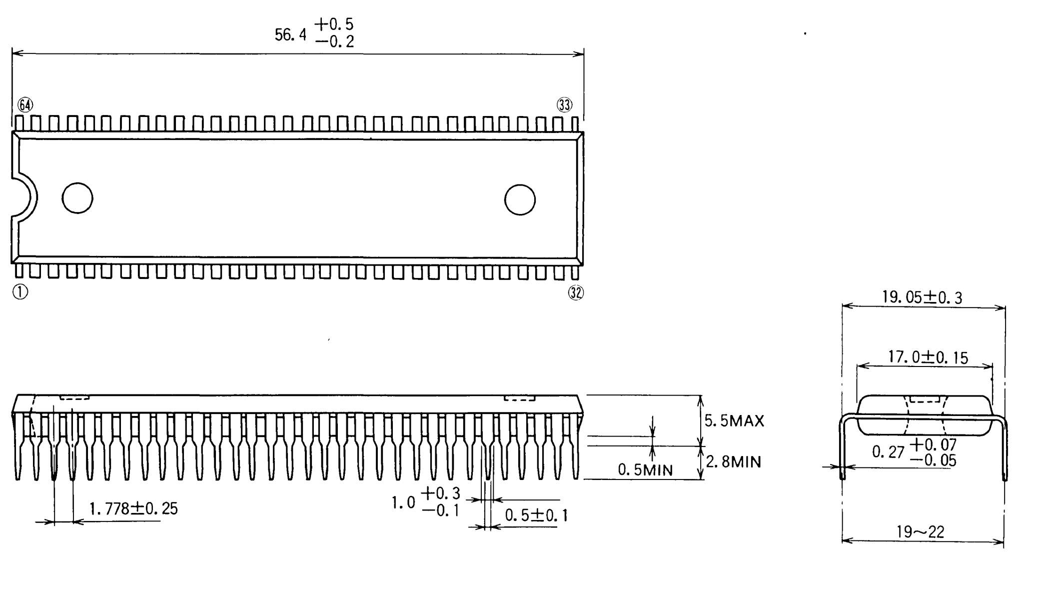
TYPE 52P2G 52-PIN MOLDED PLASTIC SOP(SHRINK)

Dimension in mm



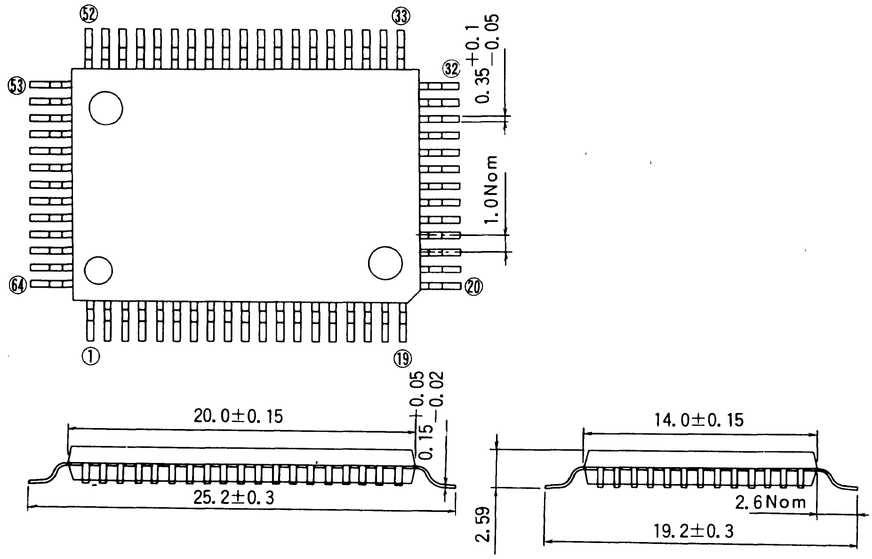
TYPE 64P4B 64-PIN MOLDED PLASTIC DIP(LEAD PITCH 1.778mm)

Dimension in mm



TYPE 64P6W 64-PIN MOLDED PLASTIC QFP

Dimension in mm



PERIPHERAL LSI SERIES FOR MICROCOMPUTER AND MEMORY

2

M66200AP/AFP

DRAM CONTROLLER

DESCRIPTION

The M66200AP/AFP is a semiconductor integrated circuit for 256K- and 1M-bit CMOS-process DRAM controllers. The device can control all necessary DRAM signals, including MPU, RAS and CAS memory control signals of signals and the signals to adjust the memory access and refresh.

The M66200AP/AFP can be used in combination with one of the address selectors of the M66210, M66211, M662112 and M66213.

The device supports almost all the 16-bit MPUs available in the market and supports 256K×1, 1M×1, 64K×1, 64K×4, 256K×4bit DRAMs.

FEATURES

- No-wait read/write access is possible if DRAM is less than 120ns when MPU is 8MHz or 10MHz.
- "Early write" feature
- Refresh
  - Automatic refresh: CAS before RAS method
  - External refresh: RAS only method
- Usable on either $\overline{RAS0}$ bank or $\overline{RAS1}$ bank
- Byte switching capability between $\overline{CAS0}$ and $\overline{CAS1}$
- Memory space:
  - When 1M-bit DRAMs are used: 4M bytes maximum
  - When 256K-bit DRAMs are used: 1M byte maximum
- Drive capability: $I_O = \pm 24$ mA
- TTL input level
- 5V single power supply
- The following types are available as an address selector IC
  - 10-line data latch (24-pin)
    - M66210P/FP (non-inverted output)
    - M66211P/FP (inverted output)
  - 2→1 line (×5) data selector (20 pins)
    - M66212P/FP (non-inverted output)
    - M66213P/FG (inverted output)

APPLICATION

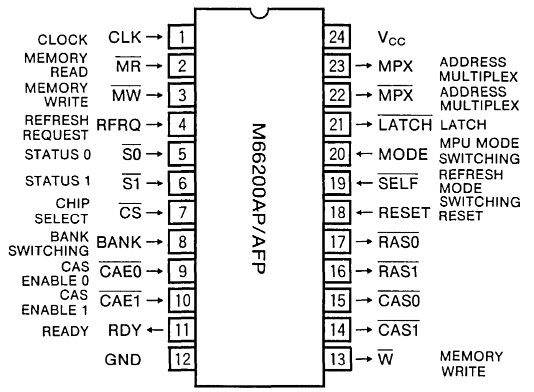
General-purpose 16-bit microprocessor and all systems using DRAM

FUNCTIONAL DESCRIPTION

The M66200A is an integrated circuit for a CMOS-process 256K- and 1M-bit DRAM controller which suppresses its noise caused by high output current switching by circuit configuration. The device supports general-purpose 16-bit microprocessors available in the market.

The chip select $\overline{CS}$, memory read ($\overline{MR}$), memory write ($\overline{MW}$), status ($\overline{SO}$ and $\overline{SI}$) as input as the MPU memory control signal, the system clock is input to CLK, and then $\overline{RAS}$, $\overline{CAS}$, memory write ($\overline{W}$), ready ($\overline{RDY}$), address multiplex (MPX, $\overline{MPX}$ and $\overline{LATCH}$) signals are output according to the memory access operation (memory read, memory write). Refresh operation is synchronized with the clock.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2

No-wait memory access is possible when a general-purpose 16-bit microprocessor is an 8MHz or 10MHz version and 256K- or 1M-bit DRAM is a high-speed version of 120ns or less.

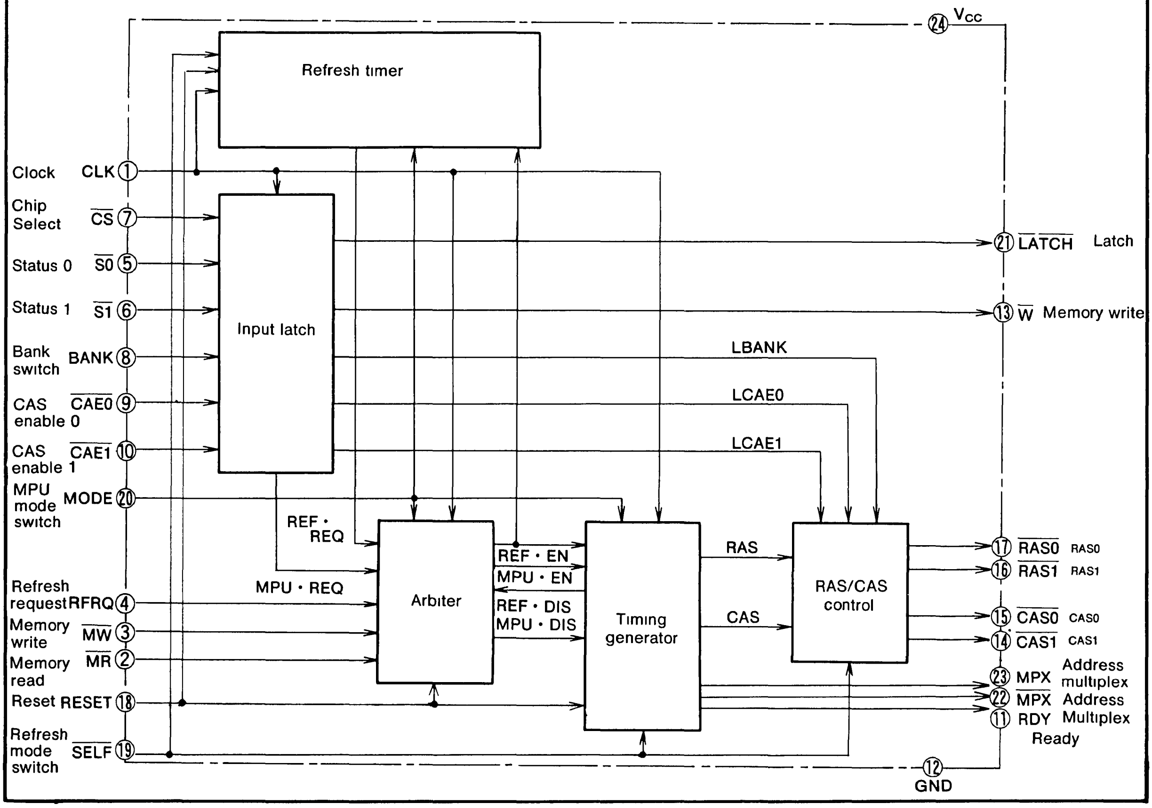
The built-in refresh timer controls refresh rate, (which is 14μs when the system clock is set to 8MHz).

The management of memory access and refresh requests are made by the built-in arbiter. The arbiter gives priority to the request that comes first. If a refresh request comes during a memory access, the refresh operation is started after the memory access is completed. On the other hand, if a memory access comes from the MPU during a refresh operation, the memory access request is not accepted until the refresh cycle is completed (RDY output is not made). And, a wait cycle is entered in the MPU (four-wait maximum).

Automatic refresh by the built-in refresh timer follows the "CAS before RAS" method. External refresh using the refresh request input RFRQ is also possible. In this case, the refresh is made by "RAS only" method.

The M66200A has a pair of RAS and CAS. Bank switching and byte switching is possible. This control mode uses bank switching input (BANK), and CAS enable inputs ($\overline{CAE0}$ and $\overline{CAE1}$).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION OF INTERNAL BLOCKS

Block name	Function
Refresh timer	When $\overline{SELF}$ is low, the refresh request signal is generated at a fixed interval. • When MODE is low, the refresh request signal is generated at an interval of 116 CLK pulses • When MODE is high, the refresh request signal is generated at an interval of 230 CLK pulses.
Input latch	$\overline{CS}$, $\overline{S0}$, $\overline{S1}$, BANK, $\overline{CAE0}$ and $\overline{CAE1}$ signals from MPU are latched
Arbiter	Determines and adjusts memory access cycle priority and refresh cycle priority. The arbiter gives priority to whichever comes first, memory access request or refresh request
Timing generator	RAS, CAS or W signals are generated according to the cycle that the arbiter determines The write cycle uses "early write method" and the refresh cycle use "CAS before RAS" (when $\overline{SELF}$ is low)
RAS, CAS control	Choice between RAS and CAS is determined by the combination of three inputs of BANK, $\overline{CAE0}$ and $\overline{CAE1}$.

FUNCTIONAL DESCRIPTION OF PINS

<table>
<tr><th>I/O</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="9">Input</td><td>RESET</td><td>Reset input
Reset input is set to "high" by built-in flip-flop reset input (Refresh operation is not executed as the refresh counter is reset during the reset period)</td></tr>
<tr><td>CLK</td><td>Clock input</td></tr>
<tr><td>$\overline{CS}$
$\overline{S0}$, $\overline{S1}$</td><td>MPU address decoder signal
Status signal from MPU
(Memory access cycle is started by the $\overline{CS}$, $\overline{S0}$ and $\overline{S1}$ signals
CLK falling edge-sampling)
<table>
<tr><th>$\overline{S0}$</th><th>$\overline{S1}$</th><th>A mode</th><th>B mode</th></tr>
<tr><td>L</td><td>L</td><td>Read</td><td>No access</td></tr>
<tr><td>L</td><td>H</td><td>Write</td><td>Write</td></tr>
<tr><td>H</td><td>L</td><td>Read</td><td>Read</td></tr>
<tr><td>H</td><td>H</td><td>No access</td><td>No access</td></tr>
</table></td></tr>
<tr><td>$\overline{MR}$</td><td>Read signal from MPU (Detects end of read cycle)</td></tr>
<tr><td>$\overline{MW}$</td><td>Write signal from MPU (Detects end of write cycle)</td></tr>
<tr><td>MODE</td><td>MPU select input
<table>
<tr><th>MODE</th><th>MPU mode</th><th>MPU</th></tr>
<tr><td>L</td><td>A mode</td><td>4-bus cycle MPU</td></tr>
<tr><td>H</td><td>B mode</td><td>2-bus cycle MPU</td></tr>
</table></td></tr>
<tr><td>$\overline{SELF}$</td><td>Refresh mode select input
<table>
<tr><th>$\overline{SELF}$</th><th>Refresh mode</th></tr>
<tr><td>L</td><td>Automatic refresh (CAS before RAS refresh)</td></tr>
<tr><td>H</td><td>External refresh (RAS only refresh)</td></tr>
</table></td></tr>
<tr><td>RFRQ</td><td>Refresh signal
Used when $\overline{SELF}$ is high (external refresh),
RFRQ becomes $\overline{RAS}$ Inputting the timing of $\overline{RAS}$ only refresh to this pin sets refresh to "$\overline{RAS}$ only refresh"
When $\overline{SELF}$ is low, this is set low (automatic refresh)</td></tr>
<tr><td>BANK
$\overline{CAE0}$
$\overline{CAE1}$</td><td>RAS and CAS which become valid by the combination of three inputs are determined
<table>
<tr><th>BANK</th><th>$\overline{CAE0}$</th><th>$\overline{CAE1}$</th><th>$\overline{RAS0}$</th><th>$\overline{RAS1}$</th><th>$\overline{CAS0}$</th><th>$\overline{CAS1}$</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Valid</td><td>H</td><td>Valid</td><td>Valid</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Valid</td><td>H</td><td>Valid</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Valid</td><td>H</td><td>H</td><td>Valid</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Valid</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>Valid</td><td>Valid</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>Valid</td><td>H</td><td>Valid</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>Valid</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td rowspan="6">Output</td><td>$\overline{RAS0}$
$\overline{RAS1}$</td><td>Row address strobe signal</td></tr>
<tr><td>$\overline{CAS0}$
$\overline{CAS1}$</td><td>Column address strobe signal</td></tr>
<tr><td>$\overline{W}$</td><td>Write signal to DRAM</td></tr>
<tr><td>MPX
$\overline{MPX}$</td><td>Multiplex signal to external data selector</td></tr>
<tr><td>LATCH</td><td>Latch signal to external data selector</td></tr>
<tr><td>RDY</td><td>Ready signal to MPU</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	+20	
I_{OK}	Input parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	+20	
I_O	Output current	$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{W}$		±50	mA
		MPX, $\overline{MPX}$, RDY, $\overline{LATCH}$		±20	
I_{CC}	Supply/GND current		V_{CC}, GND	±200	mA
P_d	Power dissipation			500	mW
Tstg	Storage temperature			−65~+150	℃
T_{opr}	Operating temperature			0~70	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits 25℃		Limits 0~70℃		Unit
					Min	Max	Min	Max	
V_{T+}	Positive threshold voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA			2.4		2.4	V
V_{T-}	Negative threshold voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA		0.6		0.6		V
V_H	Hysteresis voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA		0.2	1.8	0.2	1.8	V
V_{IH}	High-level input voltage	($\overline{SELF}$, MODE)	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.4		2.4		V
V_{IL}	Low-level input voltage	($\overline{SELF}$, MODE)	V_O=0.1, V_{CC}−0.1V, I_O=20μA			0.6		0.6	V
V_{IH}	High-level input voltage	(Other input)	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.0		2.0		V
V_{IL}	Low-level input voltage	(Other input)	V_O=0.1, V_{CC}−0.1V, I_O=20μA			0.8		0.8	V
V_{OH}	High-level output voltage	$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{W}$	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1		V_{CC}−0.1		V
				I_{OL} = −24mA, V_{CC}=4.5V	3.83		3.70		
V_{OL}	Low-level output voltage		V_I = V_{IH}, V_{IL}	I_{OH} = 20μA		0.1		0.1	V
				I_{OL} = 24mA, V_{CC}=4.5V		0.44		0.53	
V_{OH}	High-level output voltage	MPX, $\overline{MPX}$ RDY, $\overline{LATCH}$	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1		V_{CC}−0.1		V
				I_{OL} = −8mA, V_{CC}=4.5V	3.83		3.70		
V_{OL}	Low-level output voltage		V_I = V_{IH}, V_{IL}	I_{OL} = 20μA		0.1		0.1	V
				I_{OL} = 8mA, V_{CC}=4.5V		0.44		0.53	
I_{IH}	High-level input current		V_I = V_{CC}			0.1		1.0	μA
I_{IL}	Low-level input current		V_I = GND			−0.1		−1.0	μA
I_{CC}	Static power dissipation current		V_I = V_{CC}, GND, I_O = 0μA			10.0		100	μA
ΔI_{CC}	Maximum static power dissipation		V_I = 2.4V, 0.4V (Note)			2.7		2.9	mA
C_I	Input capacitance					10		10	pF

Note : This value is set to one input and all other inputs are fixed to V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~70℃)

This standard assumes the use of the address data selectors M66210P/FP~M66213P/FP

MEMORY ACCESS (A MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
—	f_{max}	Maximum repetitive frequency		20		MHz
1	t_{TLH}	Output transition time	C_L=50pF (RDY, $\overline{LATCH}$, MPX, $\overline{MPX}$)		15	ns
	t_{THL}				15	
2	t_{TLH}		C_L=50pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		10	ns
	t_{THL}				10	
	t_{TLH}		C_L=200pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		20	ns
	t_{THL}				20	
3	t_{PLH}	CLK—$\overline{RAS}$ propagation time	C_L=50pF		34	ns
	t_{PHL}				36	
4	t_{PLH}		C_L=150pF	10	36	ns
	t_{PHL}			13	40	
5	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{CAS}$ propagation time	C_L=50pF		41	ns
	t_{PHL}				36	
6	t_{PLH}	CLK—$\overline{CAS}$ propagation time	C_L=150pF	14	43	ns
	t_{PHL}			13	40	
7	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	21	62	ns
	t_{PHL}			21	62	
8	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	18	74	ns
	t_{PHL}			18	74	
9	t_{PLH}	$\overline{MW}$—$\overline{W}$ propagation time	C_L=50pF		48	ns
	t_{PHL}				25	
10	t_{PLH}	$\overline{S0}$—$\overline{W}$ propagation time (when $\overline{S0}$ and $\overline{S1}$ are used)	C_L=200pF		52	ns
	t_{PHL}				34	
11	t_{PLH}	$\overline{MW}$—$\overline{W}$ propagation time (when $\overline{S0}$ and $\overline{S1}$ are not used)	C_L=50pF		20	ns
	t_{PHL}				20	
12	t_{PLH}		C_L=200pF		24	ns
	t_{PHL}				28	
13	t_{PLH}	CLK—RDY propagation time	C_L=50pF		36	ns
14	t_{PHL}	$\overline{MR}$, $\overline{MW}$—RDY propagation time			36	
15	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{LATCH}$ propagation time	C_L=50pF		32	ns
16	t_{PHL}	CLK—$\overline{LATCH}$ propagation time			32	

MEMORY ACCESS (B MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
—	f_{max}	Maximum repetitive frequency		20		MHz
17	t_{TLH}	Output transition time	C_L=50pF (RDY, $\overline{\text{LATCH}}$, MPX, $\overline{\text{MPX}}$)		15	ns
	t_{THL}				15	
18	t_{TLH}		C_L=50pF ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$)		10	ns
	t_{THL}				10	
	t_{TLH}		C_L=200pF ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$)		20	ns
	t_{THL}				20	
19	t_{PLH}	CLK—$\overline{\text{RAS}}$ propagation time	C_L=50pF		34	ns
	t_{PHL}				36	
20	t_{PLH}		C_L=150pF	10	36	ns
	t_{PHL}			13	40	
21	t_{PLH}	$\overline{\text{MR}}$, $\overline{\text{MW}}$—$\overline{\text{CAS}}$ propagation time	C_L=50pF		41	ns
	t_{PHL}				36	
22	t_{PLH}	CLK—$\overline{\text{CAS}}$ propagation time	C_L=150pF	14	43	ns
	t_{PHL}			13	40	
23	t_{PLH}	CLK—MPX, $\overline{\text{MPX}}$ propagation time	C_L=50pF	21	62	ns
	t_{PHL}			21	62	
24	t_{PLH}	CLK—MPX, $\overline{\text{MPX}}$ propagation time	C_L=50pF	18	74	ns
	t_{PHL}			18	74	
25	t_{PLH}	$\overline{\text{MW}}$—$\overline{\text{W}}$ propagation time	C_L=50pF		48	ns
	t_{PHL}				25	
26	t_{PLH}	$\overline{\text{S0}}$—$\overline{\text{W}}$ propagation time	C_L=200pF		52	ns
	t_{PHL}				34	
27	t_{PLH}	CLK—RDY propagation time	C_L=50pF		36	ns
28	t_{PHL}	$\overline{\text{MR}}$, $\overline{\text{MW}}$—RDY propagation time			36	
29	t_{PLH}	$\overline{\text{MR}}$, $\overline{\text{MW}}$—$\overline{\text{LATCH}}$ propagation time	C_L=50pF		32	ns
30	t_{PHL}	CLK—$\overline{\text{LATCH}}$ propagation time			32	

INTERNAL REFRESH (CAS BEFORE RAS) (A MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
31	t_{PLH}	CLK—$\overline{\text{RAS}}$ propagation time	C_L=50pF		38	ns
	t_{PHL}				38	
32	t_{PLH}		C_L=150pF		41	ns
	t_{PHL}				41	
33	t_{PLH}	CLK—$\overline{\text{CAS}}$ propagation time	C_L=50pF		31	ns
	t_{PHL}				41	
34	t_{PLH}		C_L=150pF		33	ns
	t_{PHL}				45	

INTERNAL REFRESH (CAS BEFORE RAS) (B MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
35	t_{PLH}	CLK—$\overline{\text{RAS}}$ propagation time	C_L=50pF		38	ns
	t_{PHL}				38	
36	t_{PLH}		C_L=150pF		41	ns
	t_{PHL}				41	
37	t_{PLH}	CLK—$\overline{\text{CAS}}$ propagation time	C_L=50pF		31	ns
	t_{PHL}				33	
38	t_{PLH}		C_L=150pF		33	ns
	t_{PHL}				37	

EXTERNAL REFRESH (RAS ONLY)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
39	t_{PLH}	RFRQ—$\overline{RAS}$ propagation time	C_L=50pF		23	ns
	t_{PHL}				23	
40	t_{PLH}		C_L=150pF		27	ns
	t_{PHL}				27	

TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~70℃)
MEMORY ACCESS (A MODE)

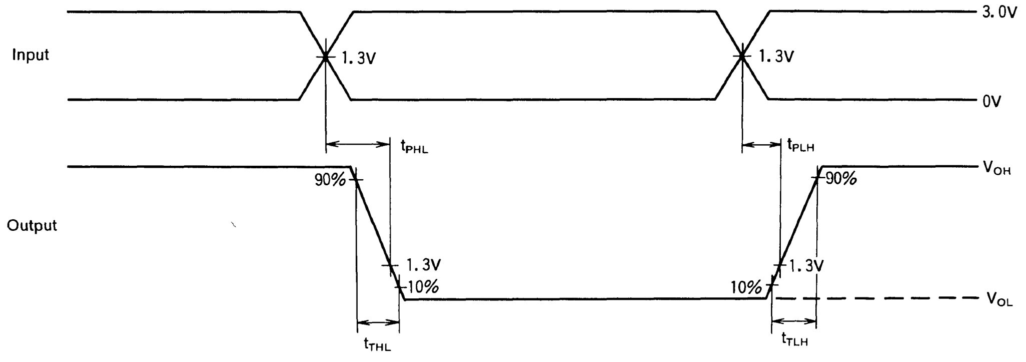
Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
41	t_{WH}	Clock pulse width (high level)		20		ns
42	t_{WL}	Clock pulse width (low level)		20		ns
43	t_{su}	CLK—$\overline{CS}$ setup time		20		ns
44	t_h	CLK—$\overline{CS}$ hold time		20		ns
45	t_{su}	CLK—$\overline{S0}$ setup time		20		ns
46	t_h	CLK—$\overline{S0}$ hold time		20		ns
47	t_{su}	CLK—$\overline{S1}$ setup time		20		ns
48	t_h	CLK—$\overline{S1}$ hold time		20		ns
49	t_{su}	CLK—$\overline{MR}$ setup time		20		ns
50	t_h	CLK—$\overline{MR}$ hold time		1.5CK+10	2.5CK−20	ns
51	t_{su}	CLK—$\overline{MW}$ setup time		20		ns
52	t_h	CLK—$\overline{MW}$ hold time		1.0CK+10	2.0CK−20	ns
53	t_{su}	CLK—BANK setup time		20		ns
54	t_h	CLK—BANK hold time		20		ns
55	t_{su}	CLK—$\overline{CAE0}$, $\overline{CAE1}$ setup time		20		ns
56	t_h	$\overline{MR}$, $\overline{MW}$—$\overline{CAE0}$, $\overline{CAE1}$ hold time		20		ns
57	t_{WH}	Reset pulse width (high level)		20		ns
58	t_{rec}	CLK—RESET recovery time		20		ns

MEMORY ACCESS (B MODE)

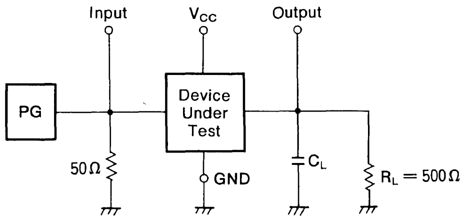
Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
59	t_{WH}	Clock pulse width (high level)		20		ns
60	t_{WL}	Clock pulse width (low level)		20		ns
61	t_{su}	CLK—$\overline{CS}$ setup time		20		ns
62	t_h	CLK—$\overline{CS}$ hold time		20		ns
63	t_{su}	CLK—$\overline{S0}$ setup time		20		ns
64	t_h	CLK—$\overline{S0}$ hold time		20		ns
65	t_{su}	CLK—$\overline{S1}$ setup time		20		ns
66	t_h	CLK—$\overline{S1}$ hold time		20		ns
67	t_{su}	CLK—$\overline{MR}$ setup time		20		ns
68	t_h	CLK—$\overline{MR}$ hold time		2.0CK	2.5CK	ns
69	t_{su}	CLK—$\overline{MW}$ setup time		20		ns
70	t_h	CLK—$\overline{MW}$ hold time		1.5CK	2.0CK	ns
71	t_{su}	CLK—BANK setup time		20		ns
72	t_h	CLK—BANK hold time		20		ns
73	t_{su}	CLK—$\overline{CAE0}$, $\overline{CAE1}$ setup time		20		ns
74	t_h	CLK—$\overline{CAE0}$, $\overline{CAE1}$ hold time		20		ns
75	t_{WH}	Reset pulse width (high level)		20		ns
76	t_{rec}	CLK—RESET recovery time		20		ns

Note : The limits of 50, 52, 68 and 70 (max) assume the continuous access from MPU and do not show the limits of operation

SWITCHING WAVEFORM



TEST CIRCUIT

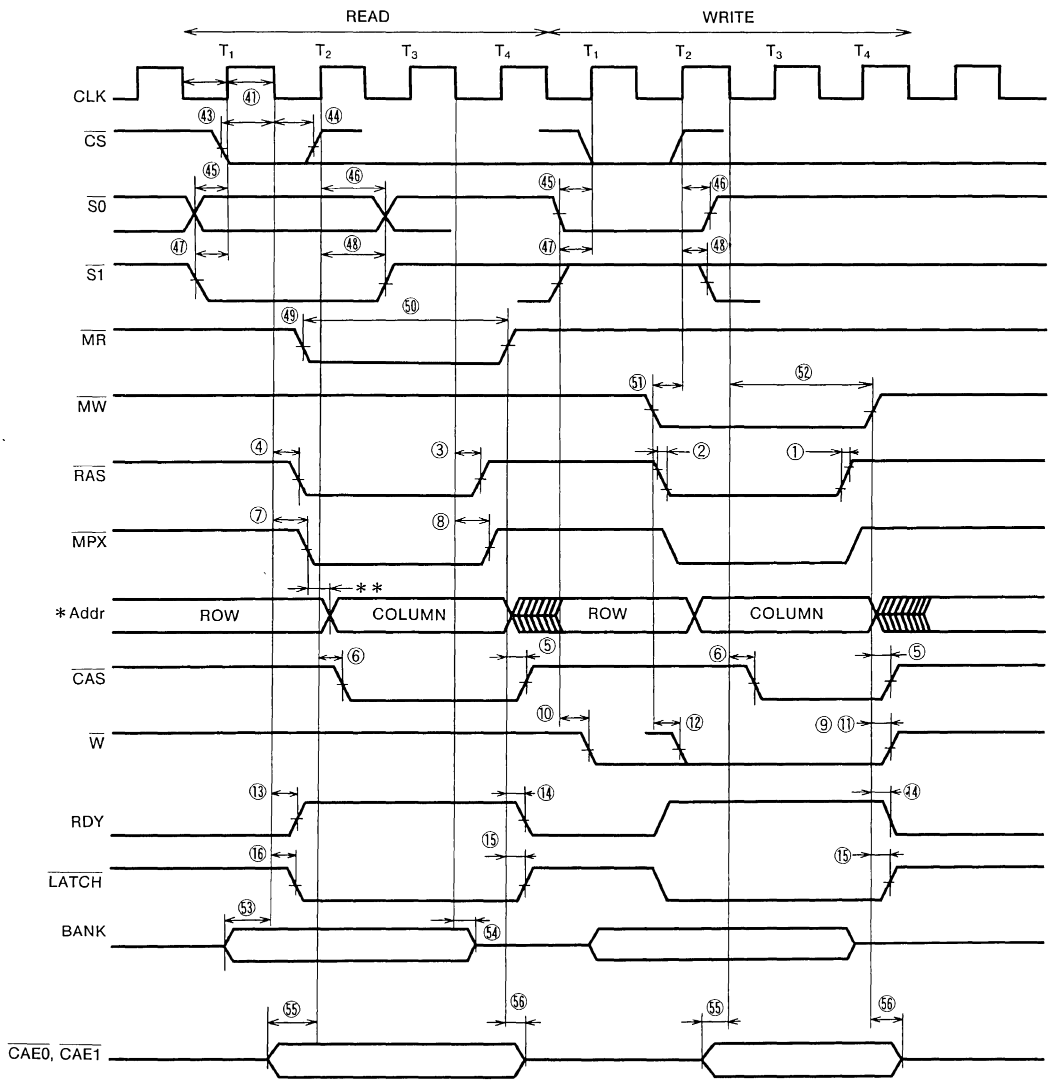


(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

MITSUBISHI ELECTRIC

TIMING DIAGRAM

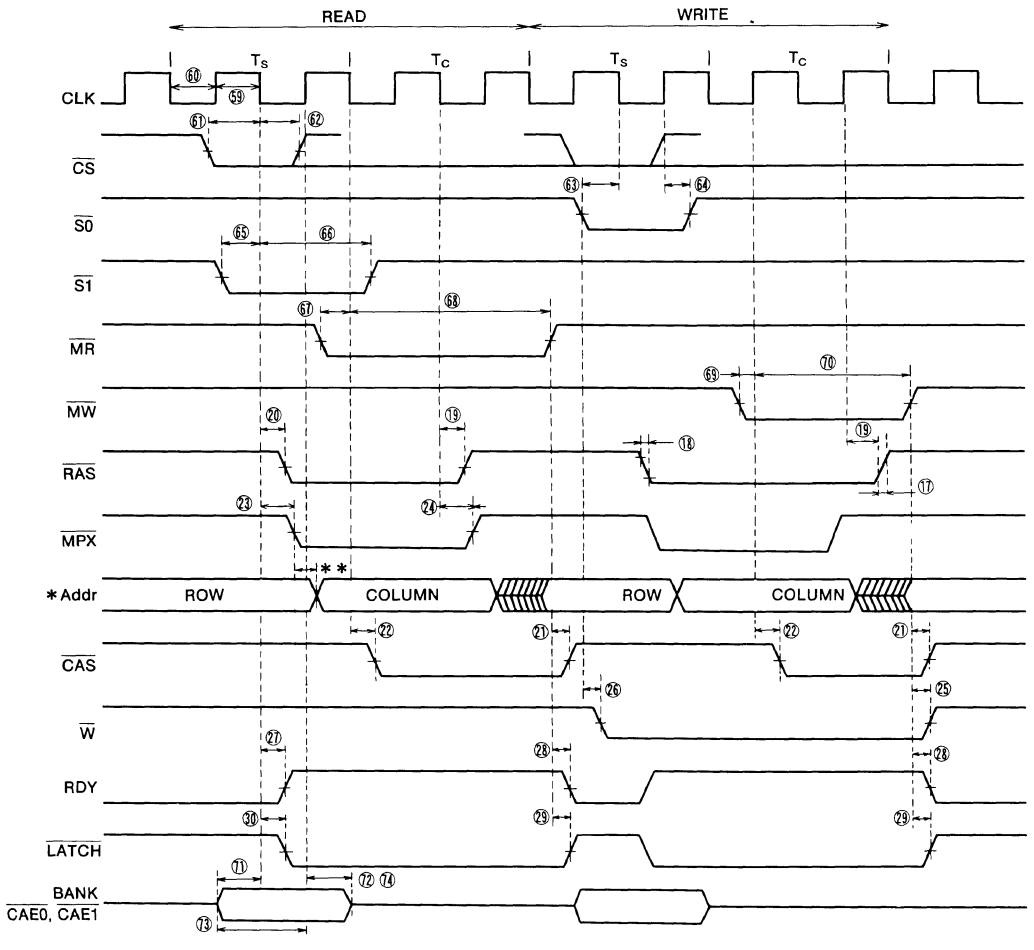
Memory access A mode



*Addr is the output of M66210P/FP~M66213P/FP

* * : See the standards of M66210P/FP~M66213P/FP

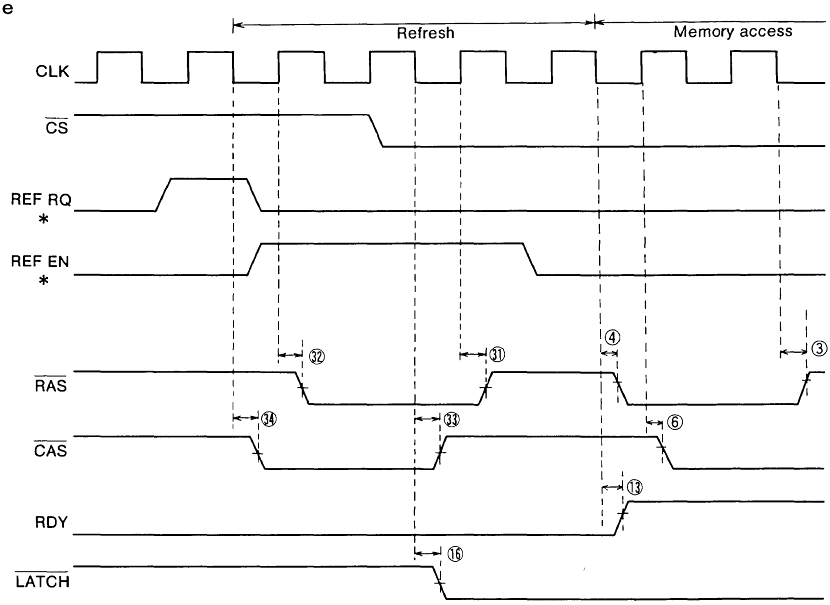
Memory access B mode



*Addr is the output of M66210P/FP~M66213P/FP

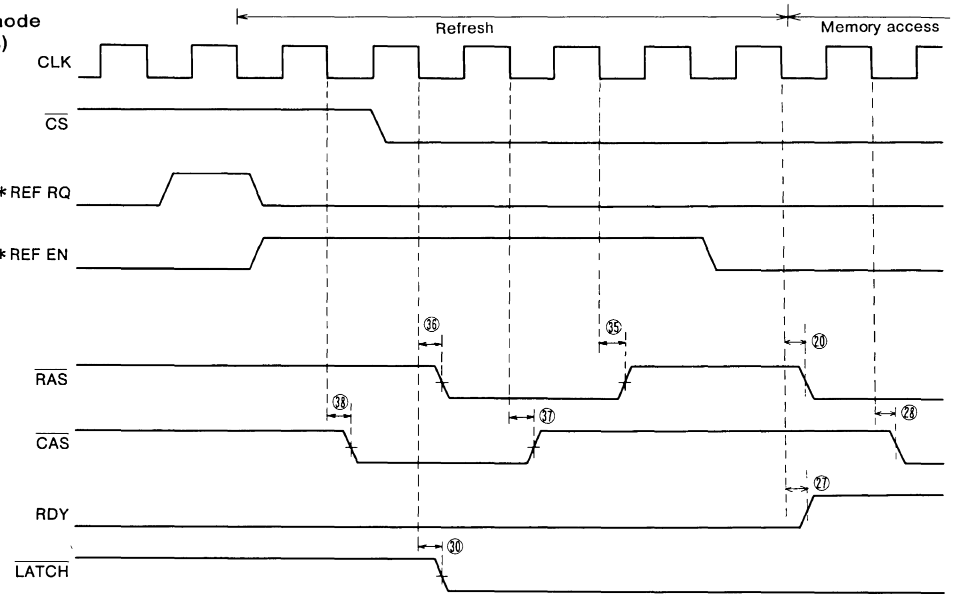
** : See the standards of M66210P/FP~M66213P/FP

Internal refresh A mode
(CAS before RAS)



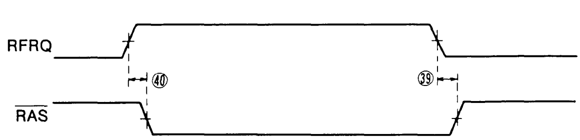
* Indicates the internal signal of the M66200AP/AFP

Internal refresh B mode
(CAS before RAS)

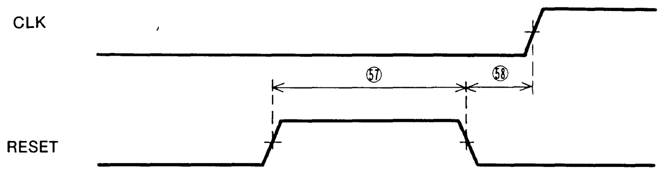


* Indicates the internal signal of the M66200AP/AFP

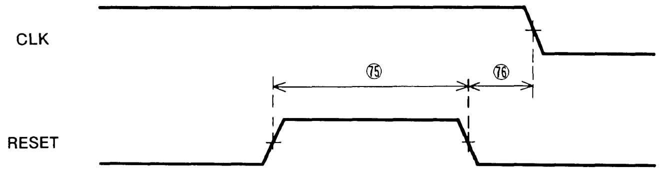
External refresh
(RAS only)



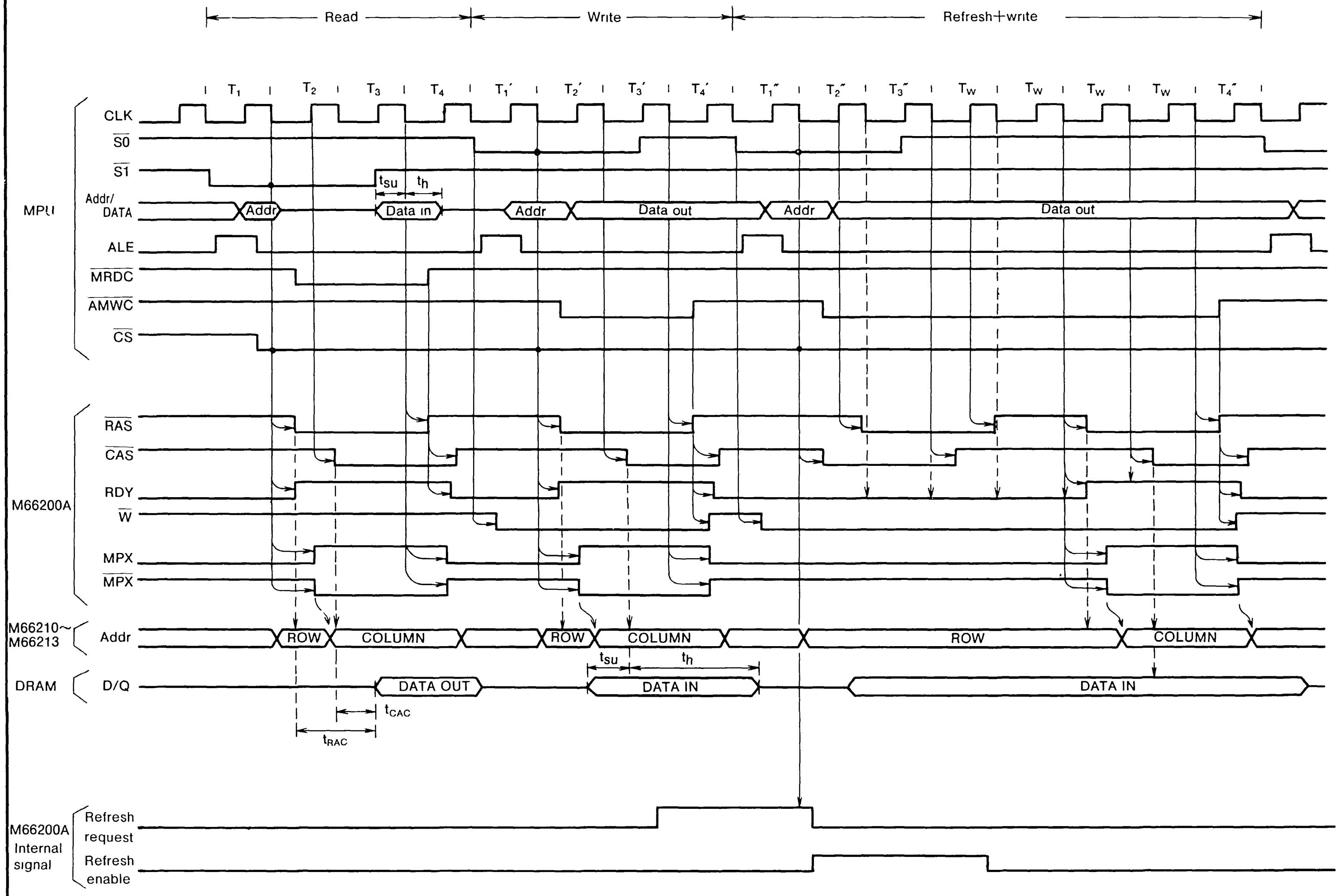
Reset timing A mode



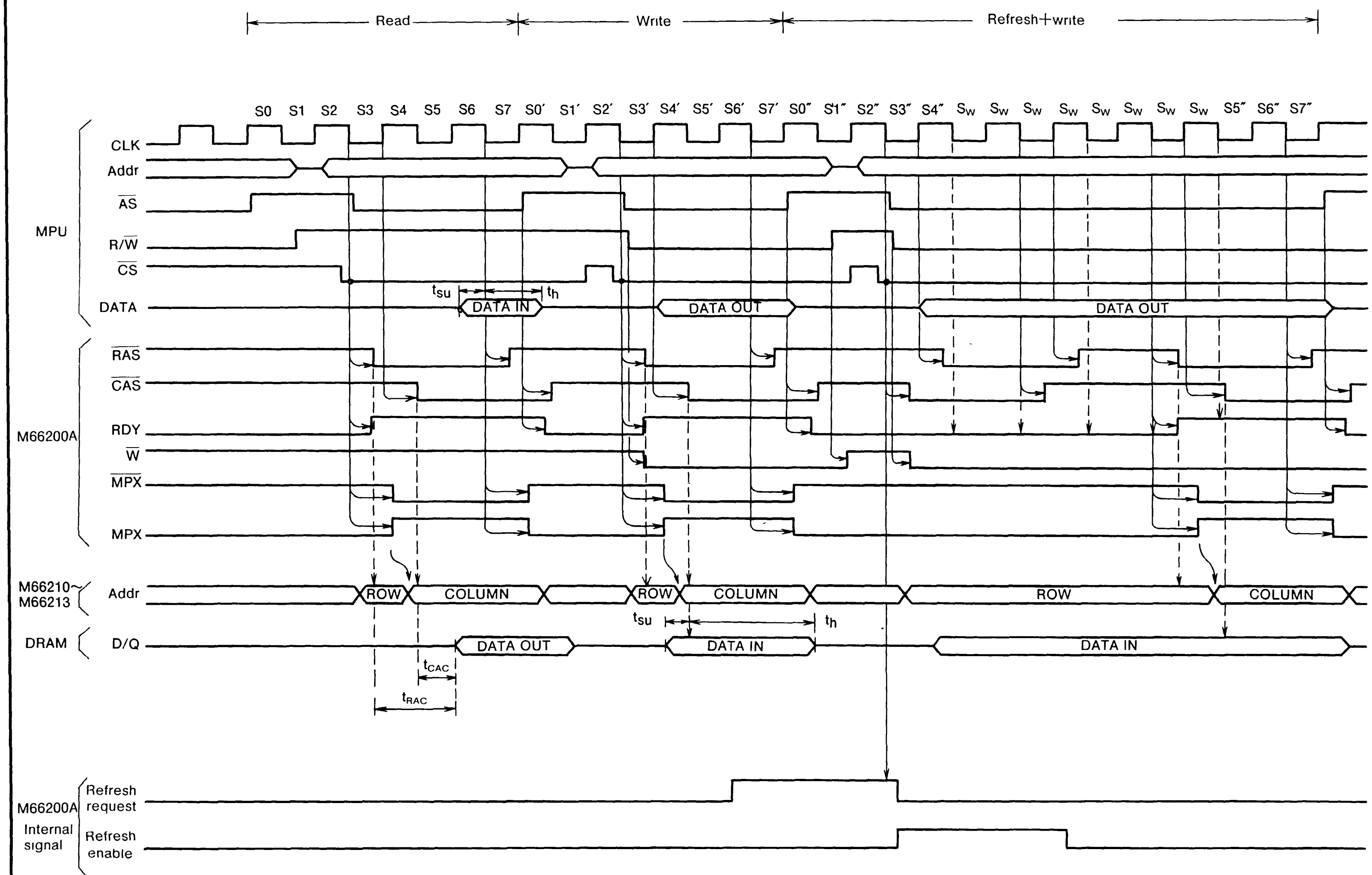
Reset timing B mode



System timing diagram A mode



System timing diagram A mode



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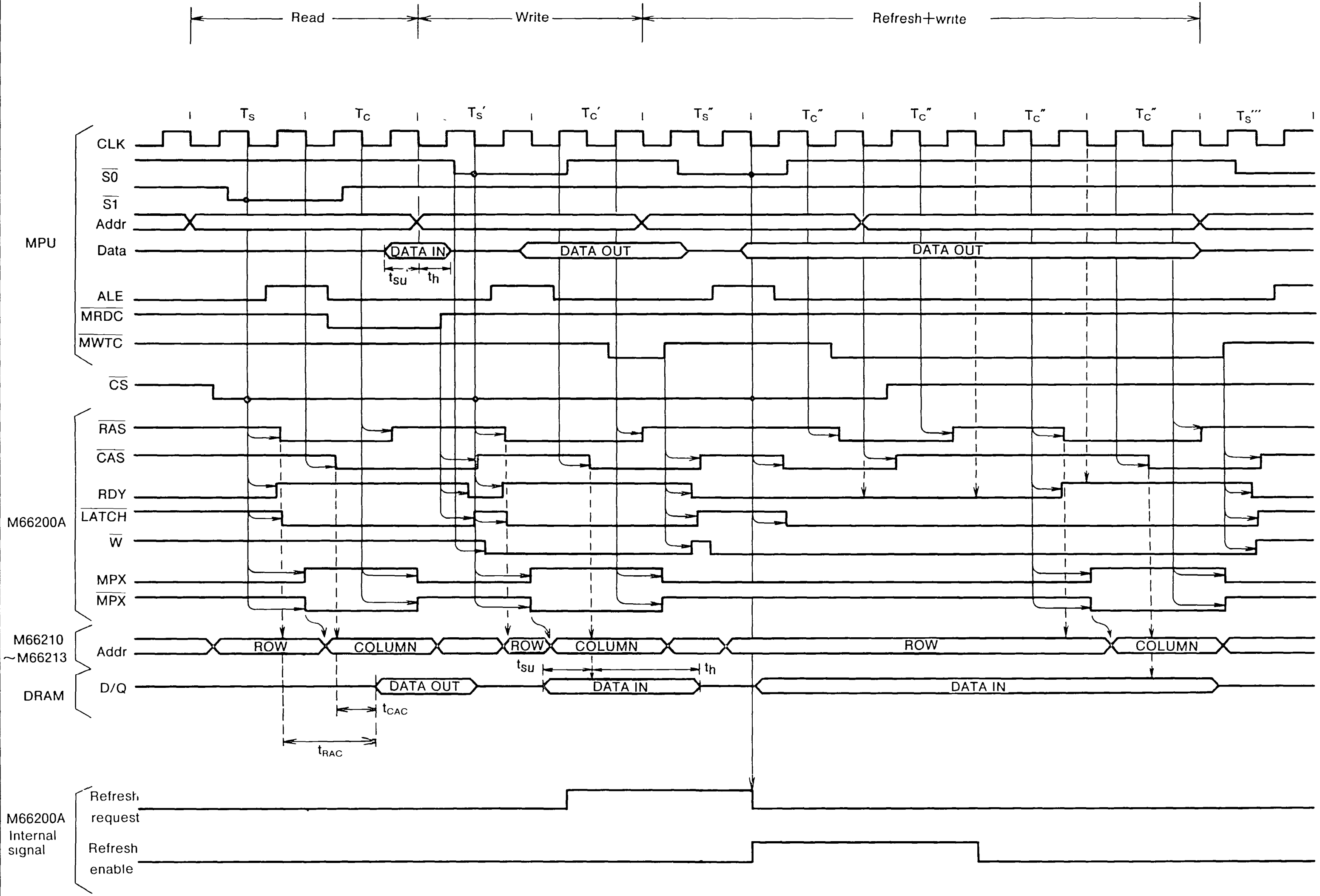
System timing diagram B mode



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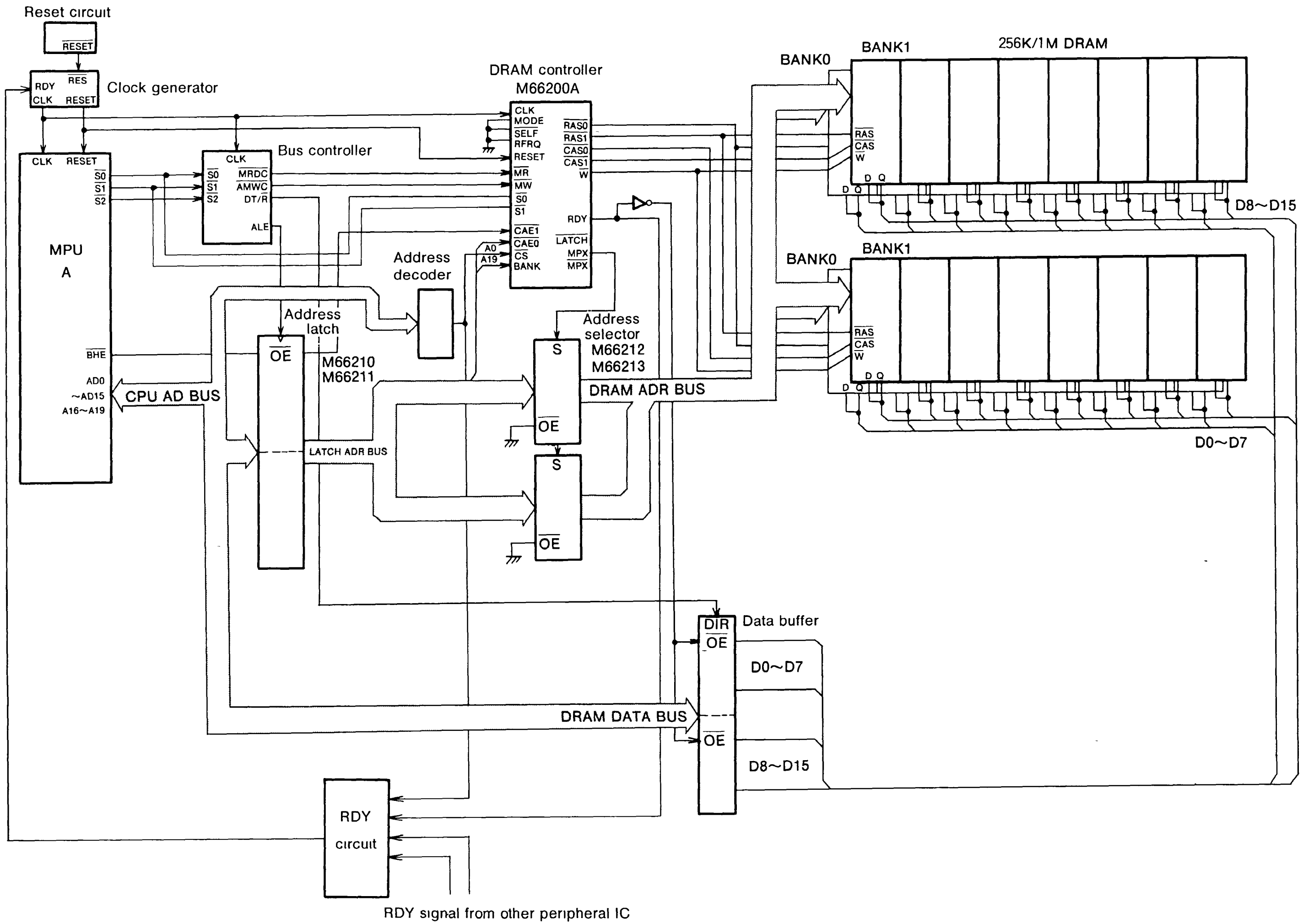
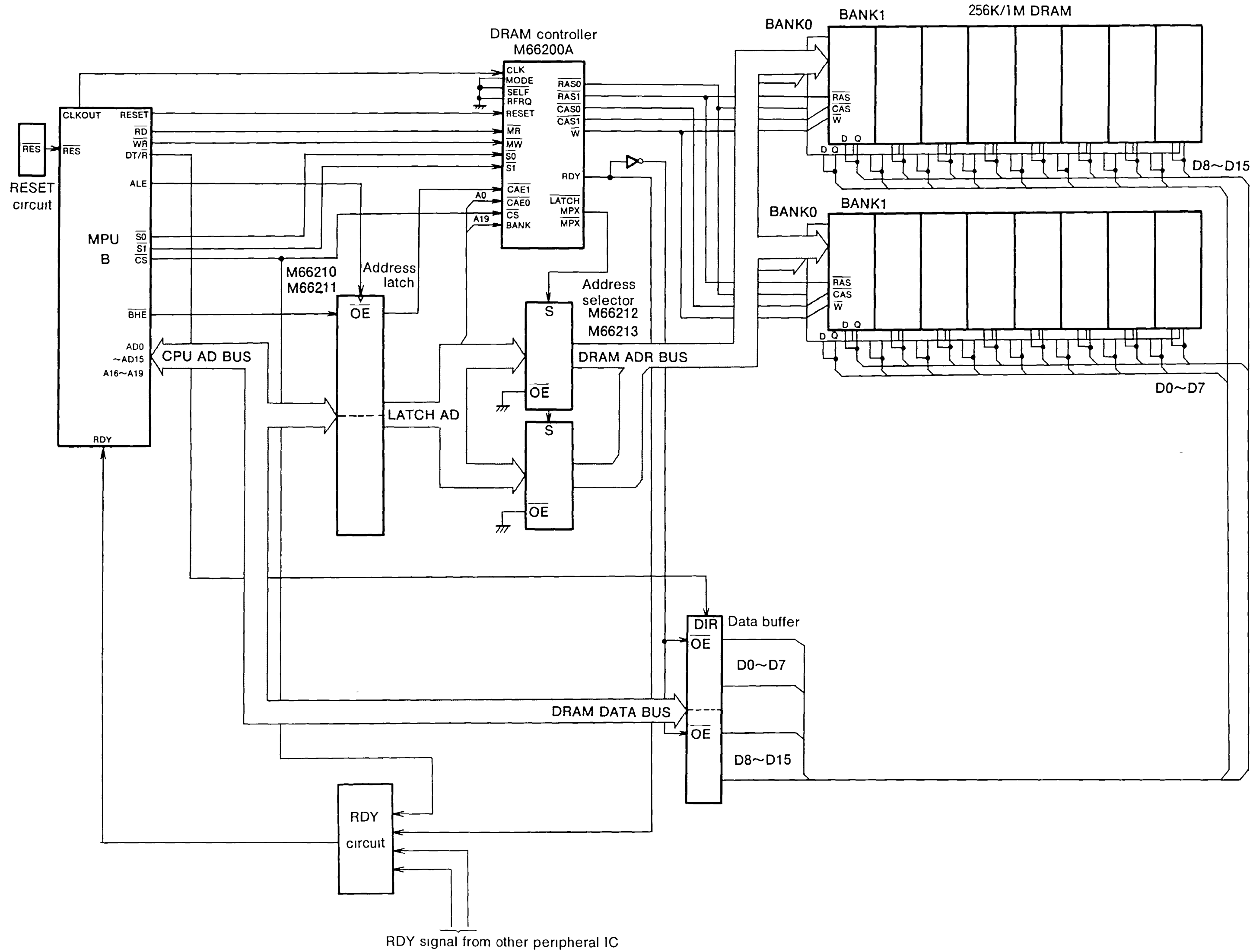
System wiring diagram

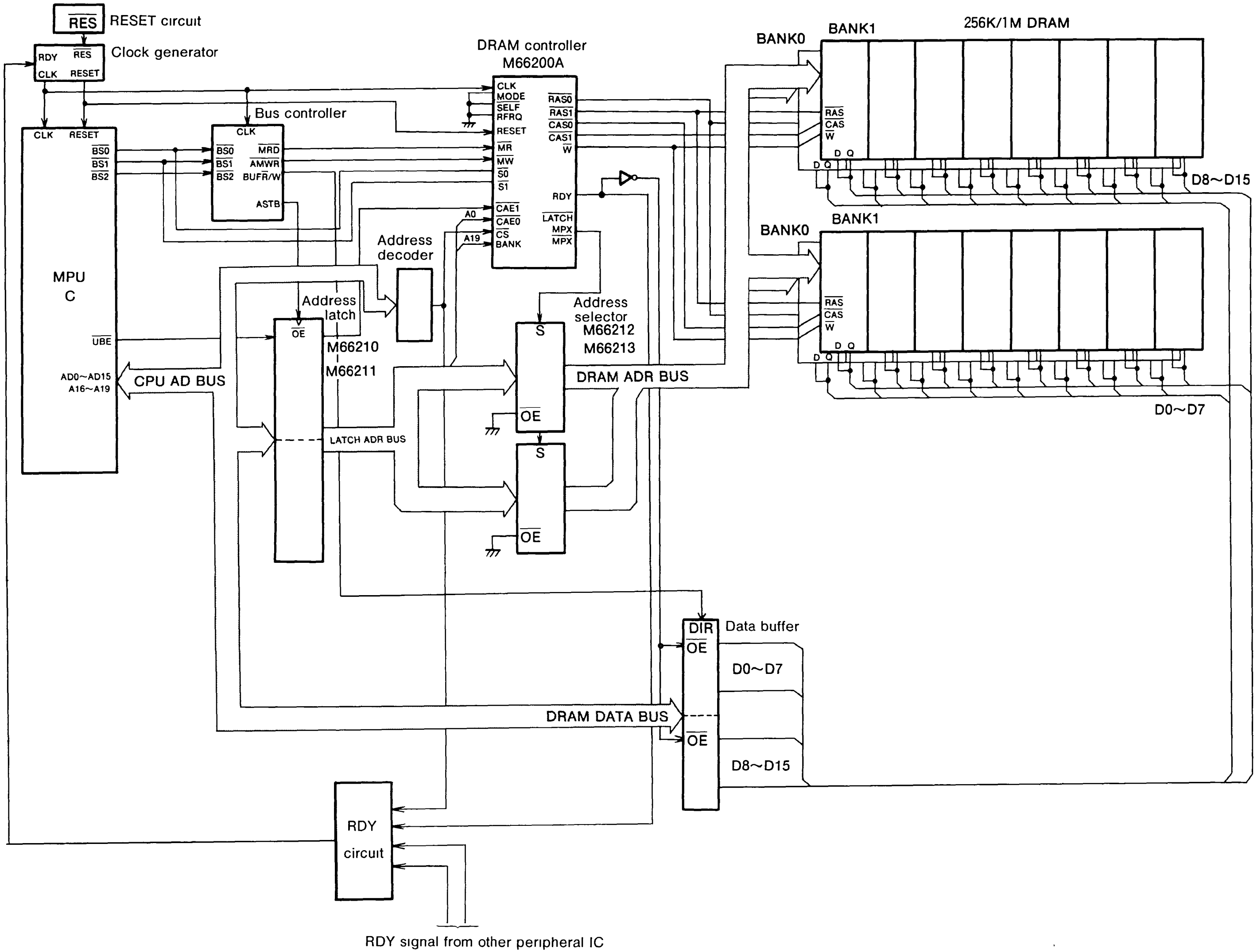
System application example 1



System application example 2



System application example 3



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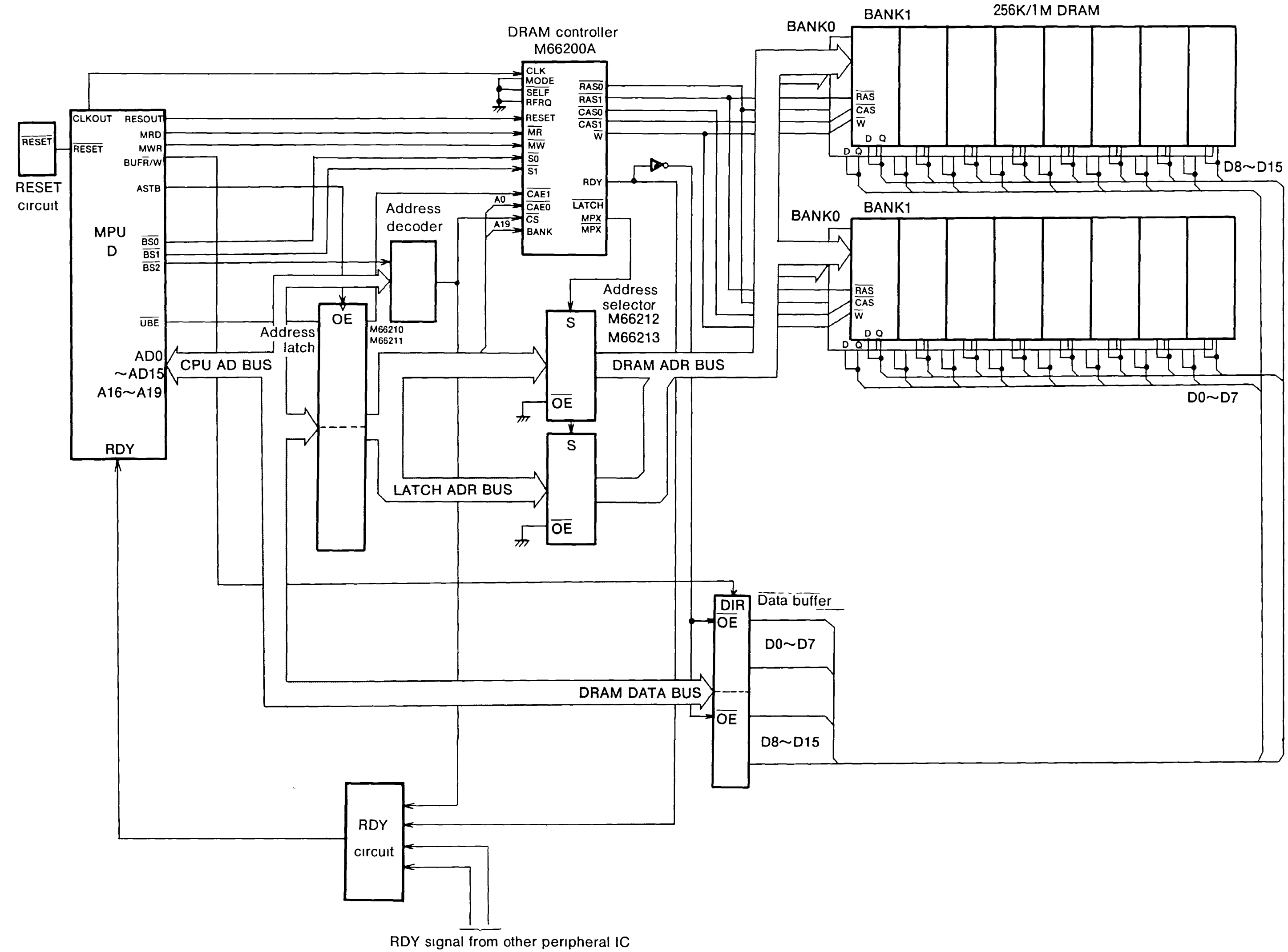
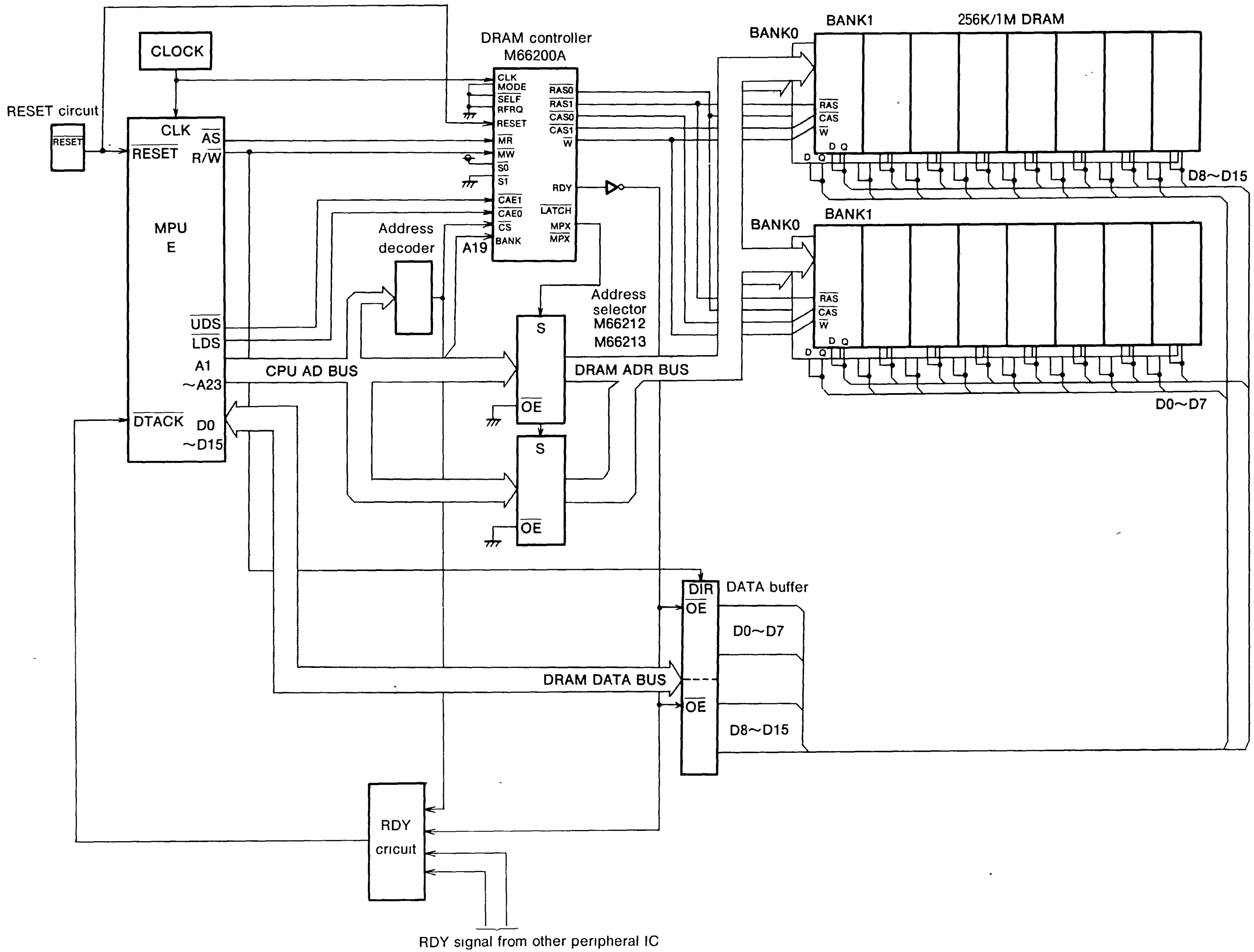
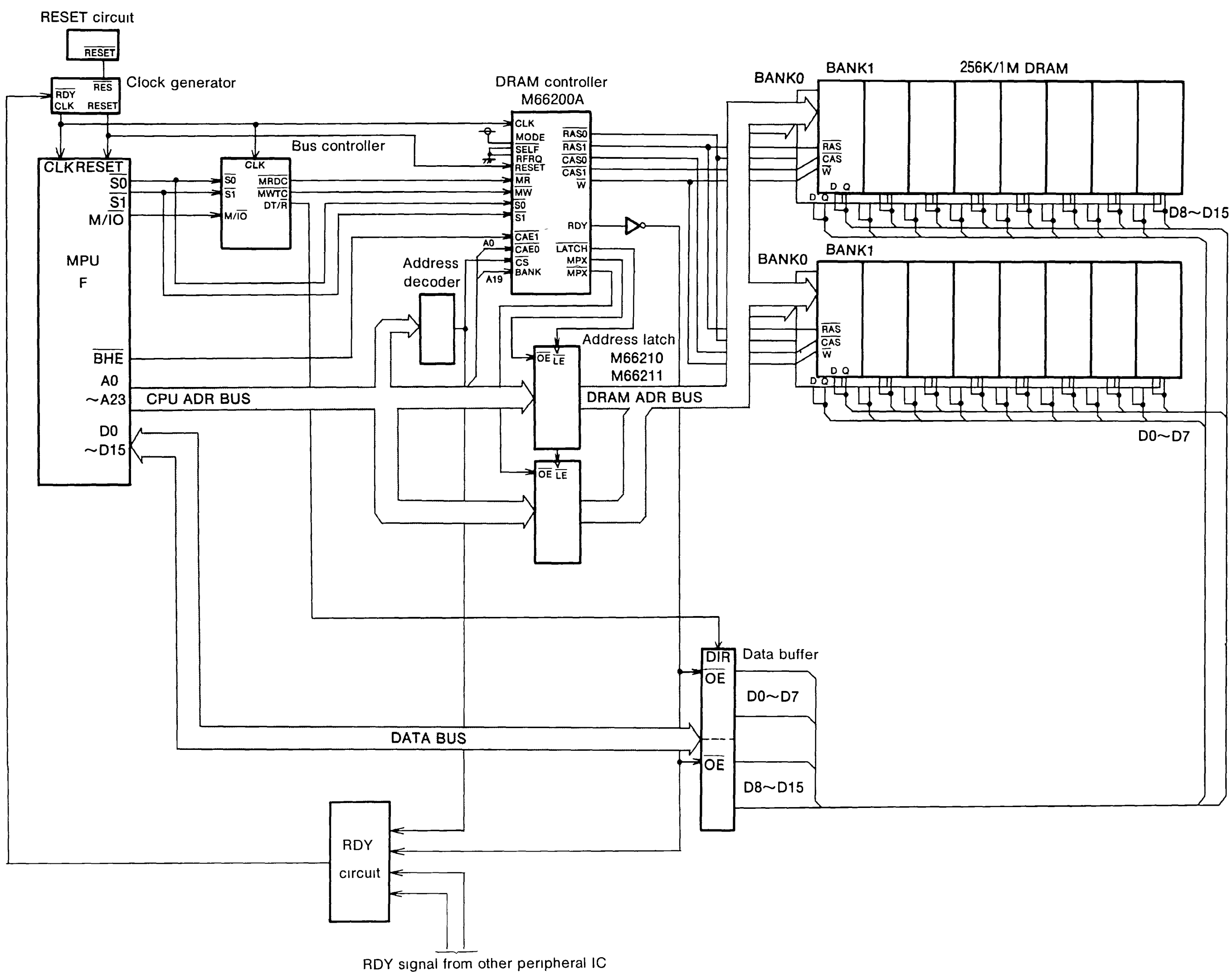
System application example 4



Application example 5



System application example 6



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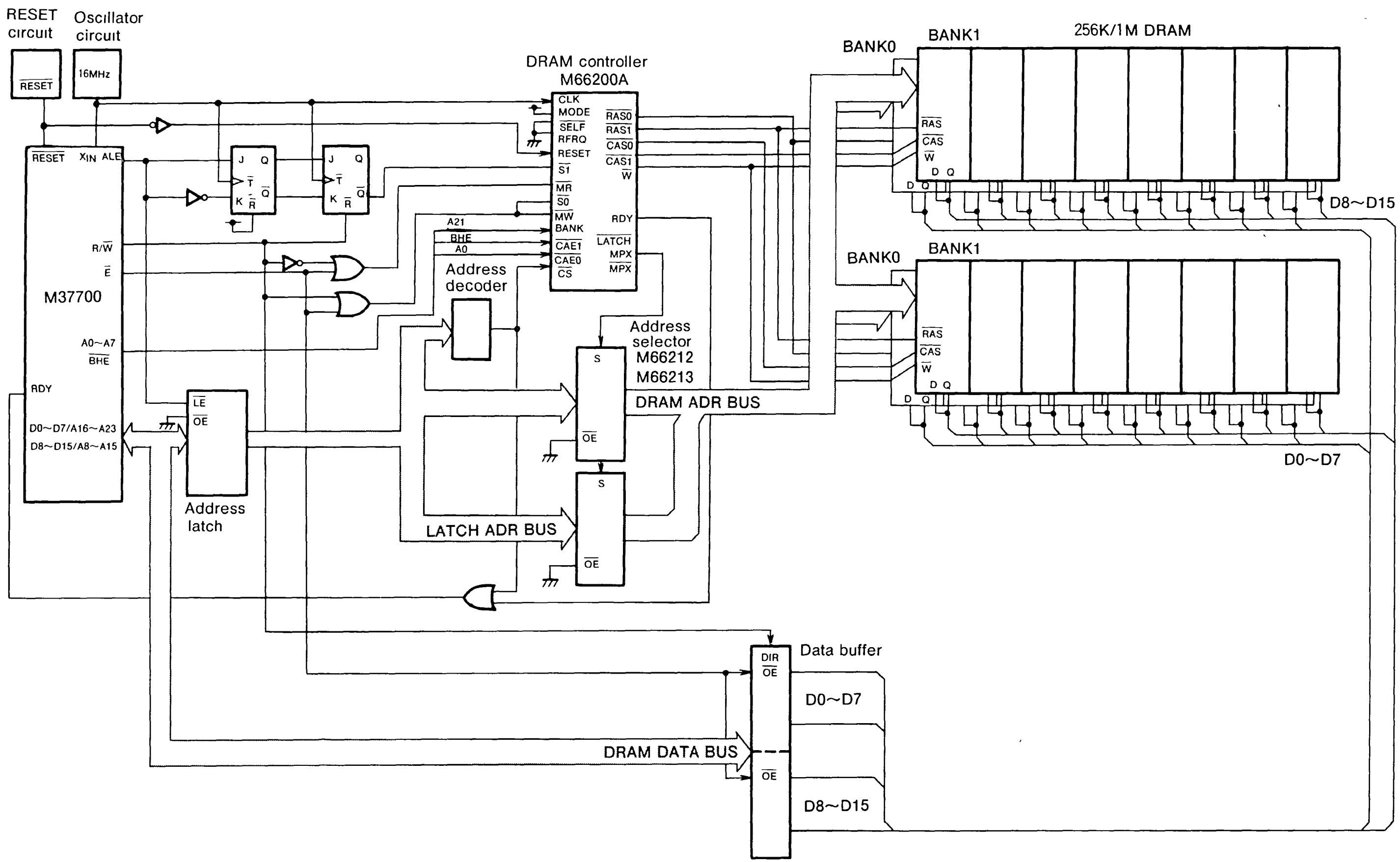
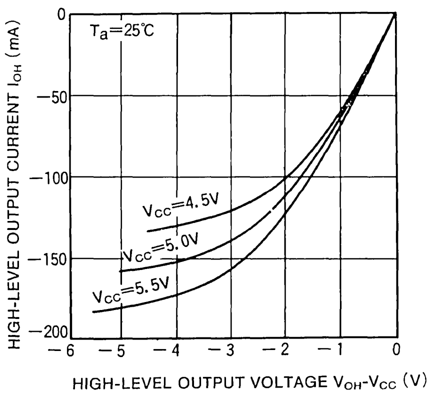
System application example 7 (M37700)



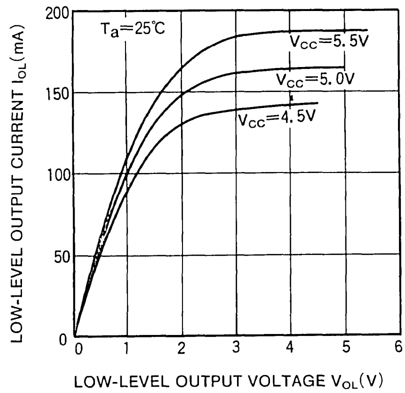
Note 1 : Provides an external oscillator circuit (less than 16MHz) and connects it to X_{IN} pin of the M37700 and CLK pin of the M66200 The X_{OUT} pin of the M37700 is open
Operated by setting the processor mode register of wait bit (bit 2 of address $005E_H$) of the M37700 to "ϕ"

TYPICAL CHARACTERISTICS

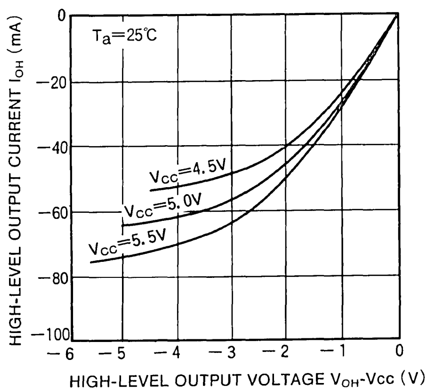
HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)



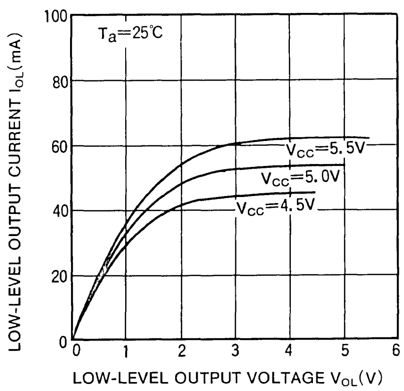
LOW-LEVEL OUTPUT CURRENT VS LOW-LEVEL OUTPUT VOLTAGE ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)



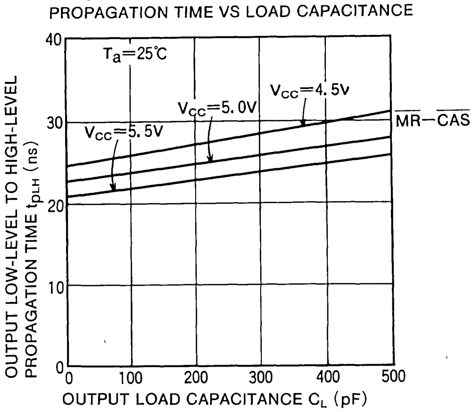
HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE (MPX, $\overline{MPX}$, $\overline{LATCH}$, RDY)



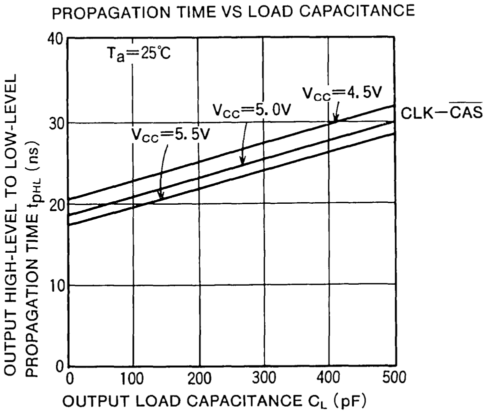
LOW-LEVEL OUTPUT CURRENT VS LOW-LEVEL OUTPUT VOLTAGE (MPX, $\overline{MPX}$, $\overline{LATCH}$, RDY)



OUTPUT LOW-LEVEL TO HIGH-LEVEL PROPAGATION TIME VS LOAD CAPACITANCE



OUTPUT HIGH-LEVEL TO LOW-LEVEL PROPAGATION TIME VS LOAD CAPACITANCE



M66210P/FP
M66211P/FP
10-LINE DATA LATCH

DESCRIPTION
The M66210P/FP and M66211P/FP are semiconductor integrated circuits consisting of ten D-type latches with 3-state outputs, common latch-enable input and output-enable input.

FEATURES
- TTL level input V_{IL}=0.8V max, V_{IH}=2.0V min.
- High fan-out 3-state output (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed 9 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation 50μW/package maximum (V_{CC}=5V, Ta=25℃, quiescent state)
- Suitable for 256K-or 1M-bit DRAM address drivers

APPLICATION
Data latch for microcomputer systems

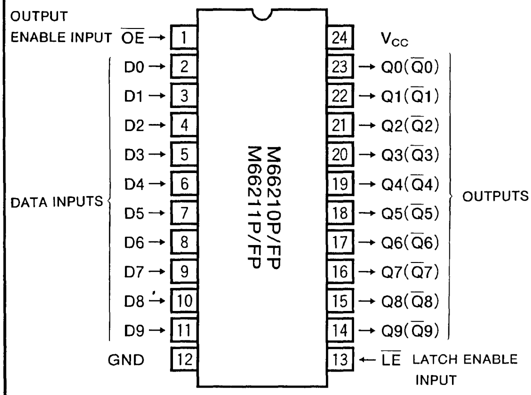
FUNCTION
Use of the silicon gate process allows for high speed processing while maintaining low power dissipation and a high noise margin on the M66210/M66211. A circuit configuration is designed to suppress the switching noise due to increases in output current.

The M66210 is a data latch for non-inverted output while the M66211 is used for inverted output.

The M66210/M66211 has ten built-in D-type latches, making the device suitable for an address driver for 256K- or 1M-bit dynamic RAMs.

When latch-enable input $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to Q. When the state of D changes, the state of Q will also change.

PIN CONFIGURATION (TOP VIEW)

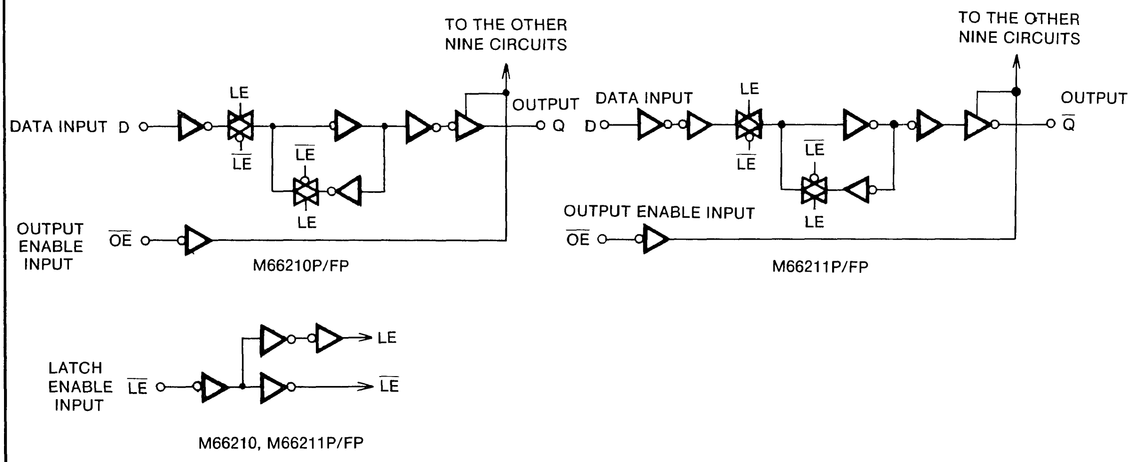


Outline 24P4D 24P2

When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch. Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected.

When output-enable input $\overline{OE}$ is high, all outputs Q will become high-impedance state.

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$Q(\overline{Q})$
L	H	H	H(L)
L	H	L	L(H)
L	L	X	Q^0
H	X	X	Z

Note 1. Q^0 : The state of Q before $\overline{LE}$ changes.
Z : High-impedance
X : Don't care
( ) : M66211P/FP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	+20	
I_{OK}	Output parastic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	+20	
I_O	Output current		±50	mA
I_{CC}	Power supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Storage temperature	0		70	℃

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	0～70℃ Min	0～70℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC}=4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC}=4.5V			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				0.1		1.0	μA
I_{OZ}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				5.0		50.0	μA
I_{OZ}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, V_O = GND				5.0		50.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, I_O = 0μA				10.0		100	μA
ΔI_{CC}	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 2)				2.7		2.9	mA

Note 2 : Only one input is set to this value and other inputs are tied to V_{CC} or GND

SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_a=0\sim70℃$)

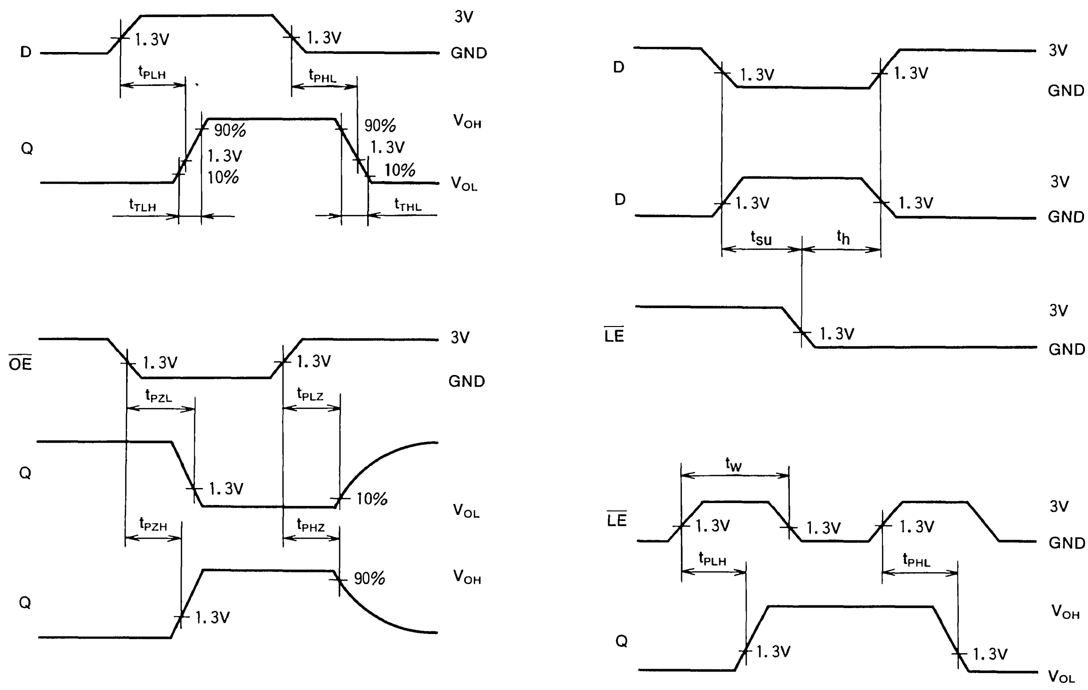
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Output transition time	$C_L=50pF$		4	10	ns
t_{THL}				4	10	
t_{TLH}		$C_L=200pF$		9	20	ns
t_{THL}				10	20	
t_{PLH}	D−Q($\overline{Q}$) propagation time	$C_L=50pF$		9	21	ns
t_{PHL}				12	21	
t_{PLH}		$C_L=200pF$		11	27	ns
t_{PHL}				16	27	
t_{PLH}	$\overline{LE}$−Q($\overline{Q}$) propagation time	$C_L=50pF$		11	26	ns
t_{PHL}				14	26	
t_{PLH}		$C_L=200pF$		12	31	ns
t_{PHL}				18	31	
t_{PLZ}	$\overline{OE}$−Q($\overline{Q}$) disable time	$C_L=50pF$		9	23	ns
t_{PHZ}				11	23	
t_{PLZ}		$C_L=200pF$	7	12	28	ns
t_{PHZ}			7	18	28	
t_{PZL}	$\overline{OE}$−Q($\overline{Q}$) enable time	$C_L=50pF$		11	23	ns
t_{PZH}				9	23	
t_{PZL}		$C_L=200pF$	7	15	28	ns
t_{PZH}			7	10	28	
C_I	Input capacitance				10	pF
C_O	Off state output capacitance	$\overline{OE}=V_{CC}$			15	pF
C_{PD}	Power dissipation capacitance (Note 3)			46		pF

Note 3 : C_{PD} is internal equivalent capacitance calculated according to the operating dissipation current with no load (per latch). The dynamic dissipation current can be obtained from the following equation under a no load condition.
$P_D=C_{PD}\cdot V_{CC}^2\cdot f_1+I_{CC}\cdot V_{CC}$

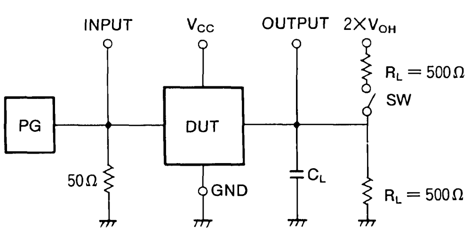
TIMING REQUIREMENT ($V_{CC}=5V\pm10\%$, $T_a=0\sim70℃$)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_W	Latch enable pulse width		15	4		ns
t_{SU}	D setup time with respect to $\overline{LE}$		13	0		ns
t_h	D hold-time with respect to $\overline{LE}$		10	0		ns

TIMING DIAGRAM



TEST CIRCUIT

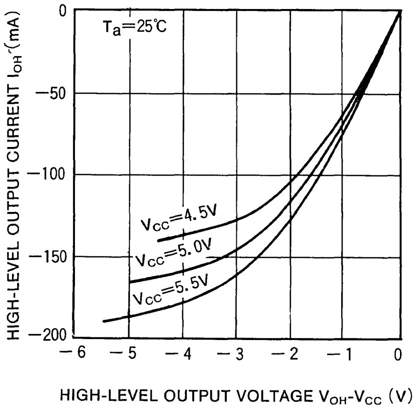


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

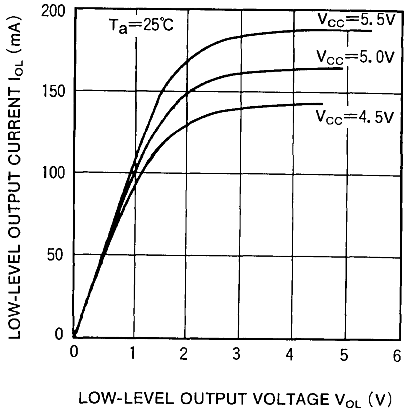
(1)Characteristics of pulse generator(PG)(10%~90%)
$t_r = 3ns$、$t_f = 3ns$
(2)C_L includes stray probe and wiring capacitance

TYPICAL CHARACTERISTICS

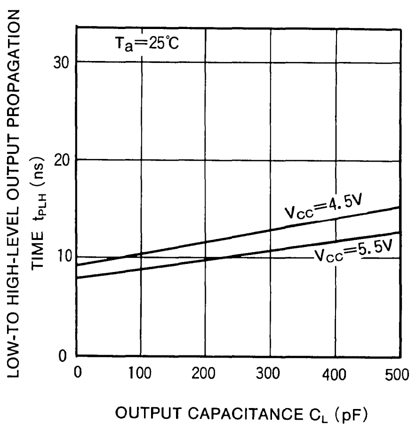
HIGH-LEVEL OUTPUT CURRENT VS
HIGH-LEVEL OUTPUT VOLTAGE



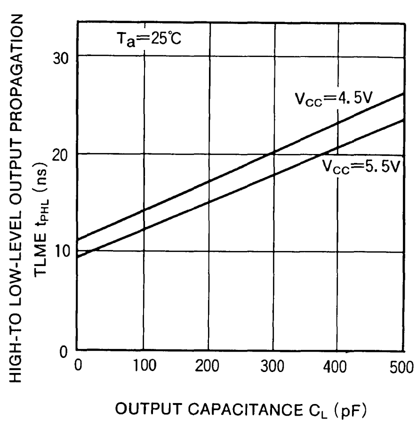
LOW-LEVEL OUTPUT CURRENT VS
LOW-LEVEL OUTPUT VOLTAGE



LOW-TO HIGH-LEVEL OUTPUT PROPAGATION
TIME VS LOAD CAPACITANCE



HIGH-TO LOW-LEVEL OUTPUT PROPAGATION
TIME VS LOAD CAPACITANCE



M66212P/FP
M66213P/FP

2→1-LINE(×5)DATA SELECTOR

DESCRIPTION

The M66212P/FP and M66213P/FP are semiconductor integrated circuits consisting of five 2-line to 1-line data selectors/multiplexers.

FEATURES

- TTL level input V_{IL}=0.8V max., V_{IH}=2.0V min.
- High fan-out output (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed 9 ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation 50μW/package maximum (V_{CC}=5V, Ta=25℃, quiescent state)
- Suitable for 256K-or 1M-bit DRAM address drivers

APPLICATION

Data selector for microcomputer systems

FUNCTION

Use of the silicon gate process allows for high speed processing while maintaining low power dissipation and a high noise margin on the M66212/M66213. The circuit configuration is designed to suppress the switching noise due to increases in output current.

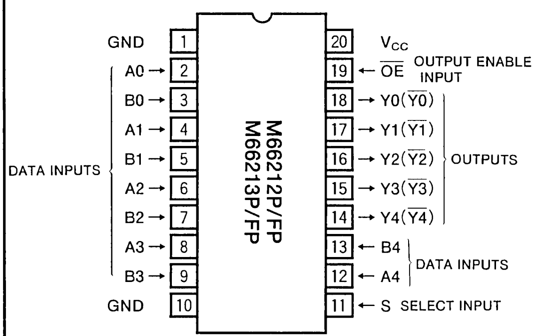
The M66212 is a data selector for non-inverted output while the M66213 is for inverted output.

The M66212/M66213 has five built-in data selector circuits, making the device suitable for an address driver for 256K- or 1M-bit dynamic RAMs.

The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y.

By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B data will be output at Y synchronous with the clock pulse in the order A-B. Both S and output-enable input $\overline{OE}$ are common to all five circuits. When $\overline{OE}$ is high, all outputs of the M66212 become low and those of the M66213 become high, irrespective of the data on the inputs.

PIN CONFIGURATION (TOP VIEW)



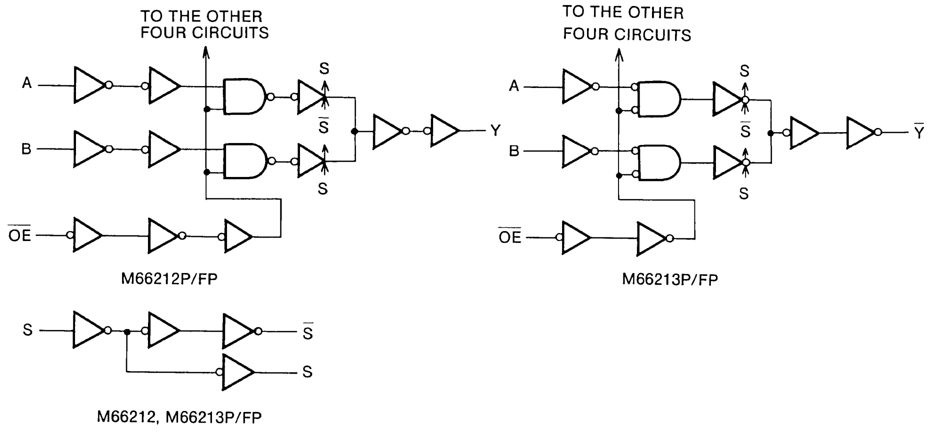
Outline 20P4 20P2N

FUNCTION TABLE

Inputs				Output
$\overline{OE}$	S	A	B	Y($\overline{Y}$)
H	X	X	X	L(H)
L	L	L	X	L(H)
L	L	H	X	H(L)
L	H	X	L	L(H)
L	H	X	H	H(L)

Note 1 : X : Don't care
( ) : M66213P/FP

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	+20	
I_{OK}	Output parastic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	+20	
I_O	Output current		±50	mA
I_{CC}	Power supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation		500	mW
Tstg	Storage temperature		−65~+150	℃

RECOMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Storage temperature	0		70	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits 0~70℃ Min	Limits 0~70℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC}=4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC}=4.5V			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				0.1		1.0	μA
I_{CC}	Quiescent supply corrent	$V_I = V_{CC}$, GND, I_O = 0μA				10.0		100	μA
ΔI_{CC}	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 2)				2.7		2.9	mA

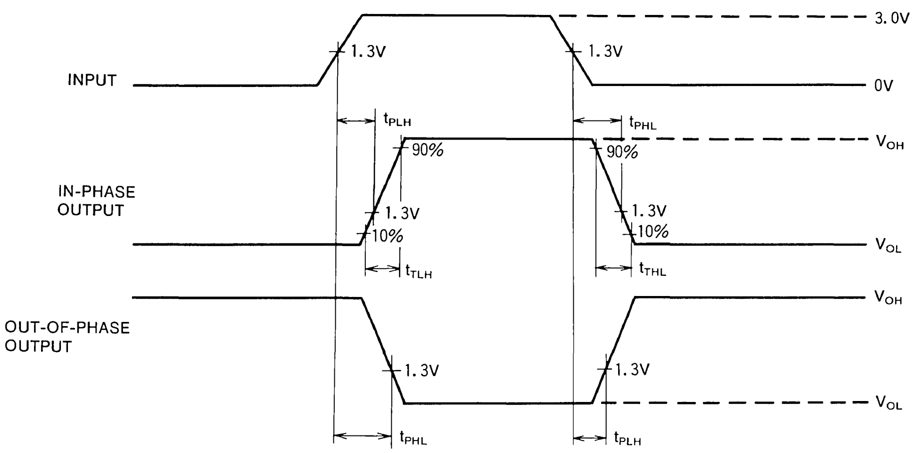
Note 2 : Only one input is set to this value and other inputs are tied to V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0~70℃)

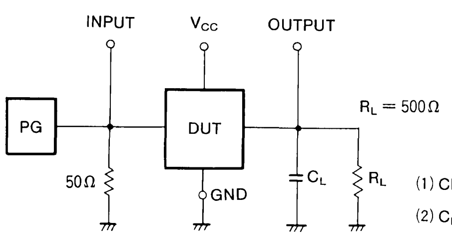
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Output transition time	C_L=50pF		5	10	ns
t_{THL}				3	10	
t_{TLH}		C_L=200pF		11	20	ns
t_{THL}				8	20	
t_{PLH}	A, B—Y, $\overline{Y}$ propagation time	C_L=50pF		9	21	ns
t_{PHL}				11	21	
t_{PLH}		C_L=200pF		11	27	ns
t_{PHL}				15	27	
t_{PLH}	S—Y, $\overline{Y}$ propagation time	C_L=50pF		12	23	ns
t_{PHL}			•	14	23	
t_{PLH}		C_L=200pF	7	13	28	ns
t_{PHL}			7	17	28	
t_{PLH}	$\overline{OE}$—Y, $\overline{Y}$ propagation time	C_L=50pF		12	21	ns
t_{PHL}				12	21	
t_{PLH}		C_L=200pF		13	26	ns
t_{PHL}				15	26	
C_I	Input capacitance				10	pF
C_{PD}	Power dissipation capacitance (Note 3)			40		pF

Note 3 : C_{PD} is an internal equivalent capacitance calculated according to the operating dissipation current with no load (per selector) The dynamic dissipation current can be calculated from the following equation under a no load condition
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING DIAGRAM



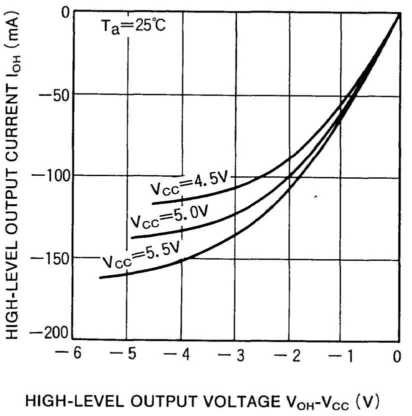
TEST CIRCUIT



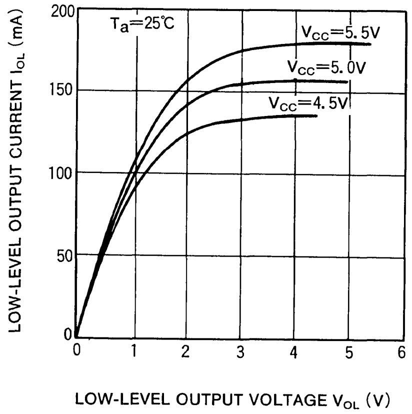
(1) Characteristics of pulse generator (PG) (10% —90%) t_r = 3ns, t_f = 3ns
(2) C_L includes stray probe and wiring capacitance

TYPICAL CHARACTERISTICS

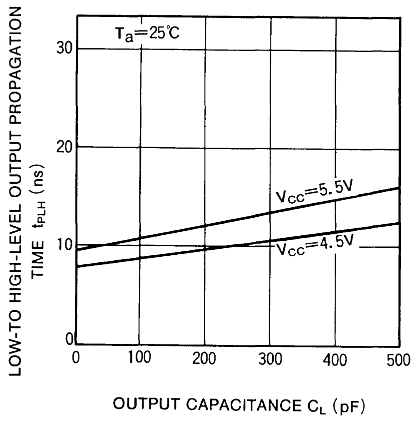
HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE



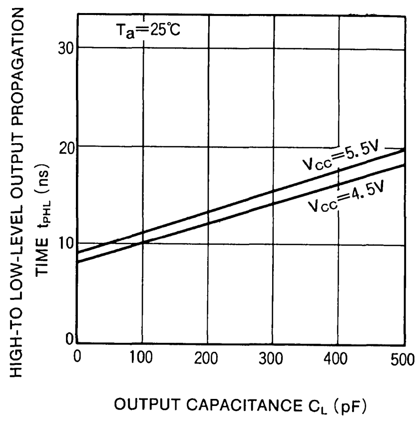
LOW-LEVEL OUTPUT CURRENT VS LOW-LEVEL OUTPUT VOLTAGE



LOW-TO HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE



HIGH-TO LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE



M66230P/FP

A²RT(ADVANCED ASYNCHRONOUS RECEIVER & TRANSMITTER)

DESCRIPTION

The M66230P/FP is an integrated circuit for asynchronous serial data communications.It is used in combination with an 8-bit micro-processor and is produced using the silicon-gate CMOS technology.

FEATURES

- Baud rate generator 500kbps (max)
- 4-byte FIFO data buffer for transmission and reception
- Error detection : CRC-CCITT, parity, overrun, and framing
- Wakeup function
- Transmisson / reception data format (number of bits)
  - Start bit 1
  - Data bit 8
  - Wakeup bit 1 or nil
  - Parity bit 1 or nil
  - Stop bit 1 or 2
- Access time t_a (RD-D) : 100ns (max)
- High output current
  $I_{OH}=-24mA$, $I_{OL}=24mA$ T_XD, $\overline{RTS}$, P0, P1 pins
- Schmitt triggered input R_XD,$\overline{CTS}$,$\overline{RESET}$ pins

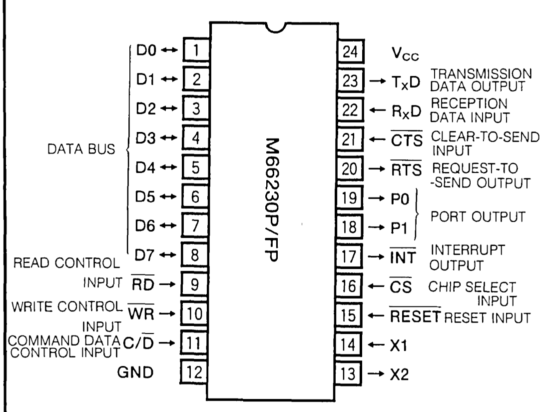
APPLICATION

Data communication control

FUNCTION

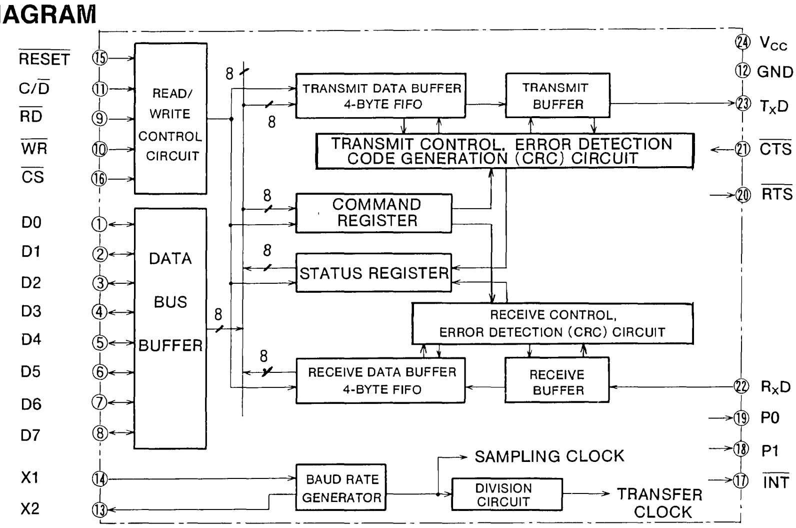
The M66230P/FP is a UART (Universal Asynchronovs Receiver/Transmitter) and is used in the peripheral circuit of a MPU. The M66230 receives parallel data, converts into serial format, and then transmits the serial data via the T_XD pin. The device also receives data via the R_XD pin from external circuits and converts it into parallel format, and sends the parallel data via the data bus.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2W

BLOCK DIAGRAM



OPERATION

The M66230 is interfaced to a system bus and provides all functions needed for data communication.

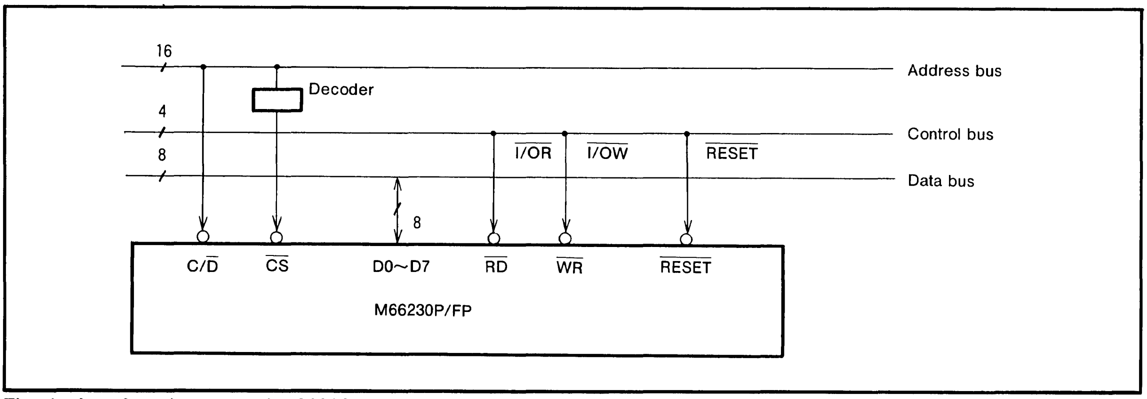


Fig. 1 Interface between the M66230 and MPU system bus.

When using the M66230, it is necessary to program the initial setting, baud rate, character length, CRC, parity, in accordance with the communication system. Once programmed, the communcation system functions are executed continuously.

When initial setting of M66230 is completed, data communication becomes possible. When the transmitter is transmit-enabled (TxEN) by a command instruction and $\overline{CTS}$ is low-level, data transfer starts up. If these conditions are not satisfied, data transmission is not executed. Reception is possible when the receiver is receive -enabled (RxEN) by a command instruction.

The MPU is able to read data when the interrupt output, $\overline{INT}$, goes low by packet end (PE) or buffer full (BF).

While receiving data, the M66230 checks for errors and provides status information. It checks for four types of errors : CRC, parity, overrun and framing errors. When an error occurs, M66230 continues operation. The error status is maintained until the error reset, ER, is modified by a command instruction.

The access method of the M66230 is shown Table 1.

TABLE 1 Access method of the M66230.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	M66230 operation	MPU operation
L	L	H	L	Data bus←Receiving data buffer (FIFO)	Read receive data
L	H	L	L	Data bus→transmit data buffer (FIFO)	Write transmit data
H	L	H	L	Data bus←Status register	Read the status
H	H	L	L	Data bus→Command register	Write the command
×	H	H	L	Data bus : high impedance	×
×	×	×	H	Data bus : high impedance	×

Note : ×=Don't care

PIN DESCRIPTIONS

Pin	Name	I/O	Function
X1, X2	Clock input/ output	Input/ output	A crystal is externally connected to these pins for generating an internal clock An external clock signal can be input to X1 instead of a crystal
$\overline{\text{RESET}}$	Reset input	Input	This reset is a master reset, therefore commands should be loaded after the reset
$\overline{\text{CS}}$	Chip select input	Input	A low level signal on the chip select input enables the M66230 The device can not be accessed when the signal is high-level
C/$\overline{\text{D}}$	Command/ data control input	Input	This signal distinguishes whether the information on the M66230 data bus is data, command or status information When the signal is high-level, the data bus has command or status information When the signal is low-level, the data bus has data
$\overline{\text{RD}}$	Read control input	Input	The receiving data or status information is output to the data bus from the M66230 by a low-level signal
$\overline{\text{WR}}$	Write control input	Input	The data or command output from the MPU is written to the M66230 by a low-level signal
D0～D7	Data bus	Input/output	This is an 8-bit bi-directional bus buffer Command, status information, and transfer data are transferred to/from the MPU via this data bus buffer
$\overline{\text{INT}}$	Interrupt output	Output	This is used as an interrupt request to MPU The interrupt request is generated when the receive FIFO is full, the transmit FIFO is empty, or the block reception is complete D2 bit of command 6 controls the switching of low-level and high-level interrupt
RxD	Serial data input	Input	The serial data is sent to this pin
TxD	Serial data output	Output	The serial data is transmitted from this pin
P0	Port output	Output	This is an ordinary port pin This pin is controlled by the D0 bit of command 6.
P1	Port output	Output	This pin has the same function as that of P0 pin and provides information of packet transmission's completion The switching of this function is controlled by command 6, D1 bit
$\overline{\text{CTS}}$	Clear-to-send input	Input	When the TxEN bit (D0) of command 4 is set to 1 and the $\overline{\text{CTS}}$ input is low-level, serial data is sent from the TxD pin This is used as the clear-to-send signal
$\overline{\text{RTS}}$	Request-to-send output	Output	This is used as the request-to-send signal This pin is controlled by the D3 bit of command 4

● Baud rate generator

The 8-bit programmable divider (baud rate generator) generates the baud rate for transmit or receive. The division rate is (n+1) with a range of n=0～255. The baud rate is calculated by the following formula :

baud rate=
f/(prescaler division rate (2 or 32) • baud rate generator division rate (n+1) • 16).

The prescaler division rate is set by the D0 bit of command 1. The baud rate generator division rate is set by command 2. Example as follows :

9600bps=(9.8304MHz)/(2 • (31+1) • 16)

where prescaler division rate is 2 and baud rate division rate is 31.

● Block length counter

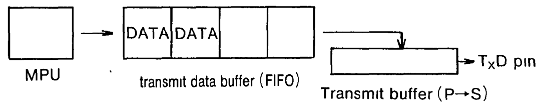
The M66230 can handle multiple-bytes of data as one block (packet).
Therefore, CRC of bytes is possible. The block length counter is a 6-bit programmable counter. The block length is (m+1) bytes with the allowed values of m=0～63.

● Transmit data buffer FIFO

The transmit data buffer (FIFO) consists of 4-bytes.
The transmit data buffer (FIFO) functions according to the block length.

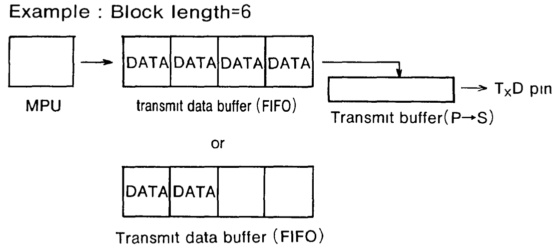
Block length=1～3
When the transmit data buffer (FIFO) becomes empty (buffer empty) and $\overline{INT}$ is set to low-active, the interrupt output $\overline{INT}$ is set to a low-level. The MPU verifies the buffer is empty when the D2 bit of the status 1 information is read. The MPU should write the block length data to the transmit data buffer (FIFO) at this moment.
When a block of data is written to the transmit data buffer (FIFO), $\overline{CTS}$ is high-level and TxEN is high-level, the data in the transmit data buffer (FIFO) is sent to the transmit buffer. If $\overline{CTS}$ is high-level while data is transmitted, all data is transmitted (including the data in the transmit data buffer (FIFO). When the buffer becomes empty, the data in the transmit data buffer (FIFO) is not be sent to the transmit buffer until MPU writes a new block of data to the transmit data buffer (FIFO). The MPU can not write new data to the transmit data buffer (FIFO) until the buffer becomes empty.

Example : Block length=2



comes empty. When the transmit data buffer (FIFO) becomes empty and $\overline{INT}$ is set low-active, the interrupt output $\overline{INT}$ becomes low. The MPU verfies the buffer is empty by reading the D2 bit of the status information.
Block length=4 or more
When this happens, the MPU should write the 4-bytes of data to the transmit data buffer (FIFO). The data in the transmit data buffer (FIFO) is sent to the transmit buffer, when $\overline{CTS}$ is low-level and TxEN is high-level. When $\overline{CTS}$ is high-level while data is transmitted, all transmitted data (including the data in the transmit data buffer (FIFO)) is transmitted. When the number of bytes from the MPU becomes less than 4 at the last stage of the block transmission, the same operation should be made as the block length=1～3.
When the buffer becomes empty, the data in the transmit data buffer (FIFO) is not be sent to the transmit buffer until MPU writes data of the fixed block length to the transmit data buffer (FIFO). The MPU cannot write data to the transmit data buffer (FIFO) until the buffer becomes empty. When the transmit data buffer (FIFO) becomes empty and $\overline{INT}$ is set low-active, the interrupt output $\overline{INT}$ becomes low. The MPU verifies the buffer is empty by receiving the D2 bit of the status information.

Example : Block length=6



MITSUBISHI ELECTRIC

● Receive data buffer FIFO

The receive data buffer (FIFO) consists of 4-bytes. The receive data buffer (FIFO) functions according to the block length.

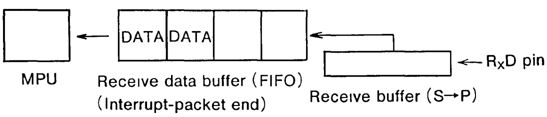
Block length=1~3

When the data of the block length is received and $\overline{INT}$ is set to low-level, the interrupt output $\overline{INT}$ becomes low-level. The MPU acknowledges the packet end by setting the D0 bit of the status 1 information.

In this case, the MPU should read all data from the receive data buffer (FIFO).

At the packet end, the data from the receive buffer cannot be transmitted to the receive data buffer (FIFO) until the MPU reads all data in the receive data buffer (FIFO). The MPU cannot read data in the receive data buffer until the packet end.

Example · Block length=2



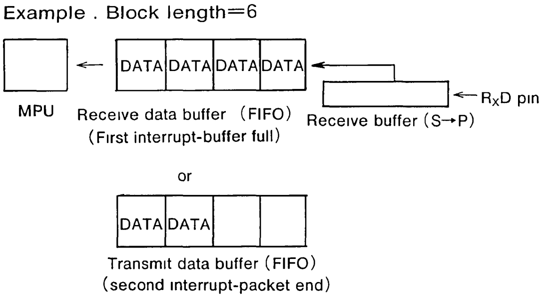
Block length=4 or more

When 4-byte data enters the receive data buffer (FIFO) (buffer full) and $\overline{INT}$ is set to low-active, the interrupt output $\overline{INT}$ becomes low-level. The MPU acknowledges the buffer full status by setting the D1 bit of the status information.

In this case, the MPU should read all data in the receive data buffer (FIFO).

When the last data enters the receive data buffer (FIFO), the packet end becomes the same operation as for 1~3 byte block length. If the block length is a multiple of four, the D1 and D2 bits of the status 1 information are set when the last data enters the receive data buffer (FIFO). At packet end or buffer full, the new data cannot be transferred from the receive buffer to the receive data buffer (FIFO). The MPU cannot read data in the receive data buffer (FIFO) until block end or buffer full occurs.

Example . Block length=6



SUPPLEMENTARY DESCRIPTION

FIFO

The major purpose is not to interrupt the MPU by each character. The MPU is interrupted when :

Transmit data buffer (FIFO) empty

Receive data buffer (FIFO) full or packet end

The MPU interruption interval is as follows :

Approximately 90μs (min) until the FIFO becomes full at 500kbps.

Approximately 36.7ms (min) until the FIFO becomes full at 1.2kbps.

Read/write operation by the MPU should be made for all data in FIFO at once.

● Wakeup

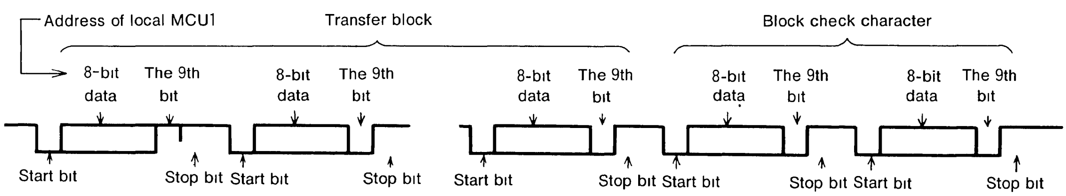
The wakeup mode of the M66230 can be set by setting the D2 bit of command 4 to "1". In wakeup mode, a 9th bit is automatically added (the wakeup bit).
Only the 9th bit of the first byte is "1", and the remainer blocks 9th bits are set to "0".
The wakeup is used when one master MPU and multiple local MPU are connected by serial I/O.
Examples of wakeup are shown below.

① Initial setting
The initial setting should be made by the input of each command.

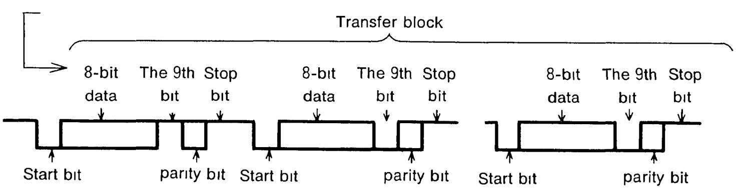
② Wakeup mode
The wakeup mode of the M66230 is activated by setting D2 bit of the command 4 to "1". Command 5 can be input as the second byte of command 4 by setting D2 bit of the command 4 to "1" and each address is input. In the wakeup mode, the 9th bit is automatically added. Others remain the same.

③ Wakeup and data transfer (between master MPU and local MPU1)
Data is transmitted from the master MPU to each local MPU.
The first byte should hold the address of the local MPU. (in this case local MPU1.)
Each local M66230 checks the data (address) against command 5 (each address) when the first byte (address) is received. the M66230 which matches the address starts to accept the following data (wakeup). the M66230 which does not match the address, only accepts data, where the 9th bit is "1".

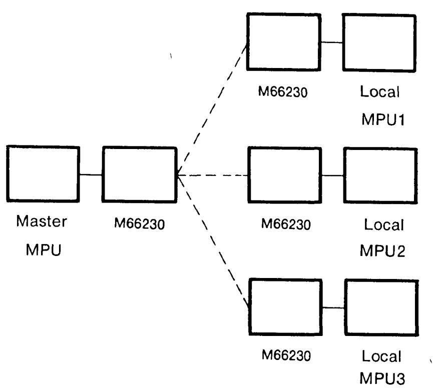
When CRC is enabled

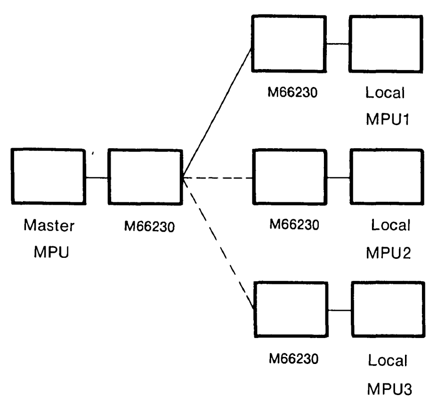


When parity is enabled



Note . The wakeup function is automatically canceled when the transfer block data has been read by the MPU
(The wakeup mode continues.)





● Error detection

Parity error

When a parity error occurs, D5 bit of status 1 information is set. The data is send to the receive data buffer (FIFO).

Framing error

When a framing error occurs, D3 bit of the status 1 information is set. The data is sent to the receive data buffer (FIFO).

Overrun error

When data is received before all data in the receive data buffer (FIFO) has been read by MPU, D4 bit of the status 1 information is set as an overrun error.

In this case, the new data in the receive buffer are lost.

CRC error

When an error occurs after receiving block check character, D6 bit of the status 1 information is set.

The above error information is maintained until D4 bit of command 4 is set.

SUPPLEMENTARY DESCRIPTION

Comparison between parity check and CRC

Parity check

Parity check needs only one additional bit and is highly efficient. The formula is straightforward, and includes even parity and odd parity checks. In both cases, one bit is added.

CRC

The CRC polynominal expression is CRC-CCITT $X^{16}+X^{12}+X^5+1$.

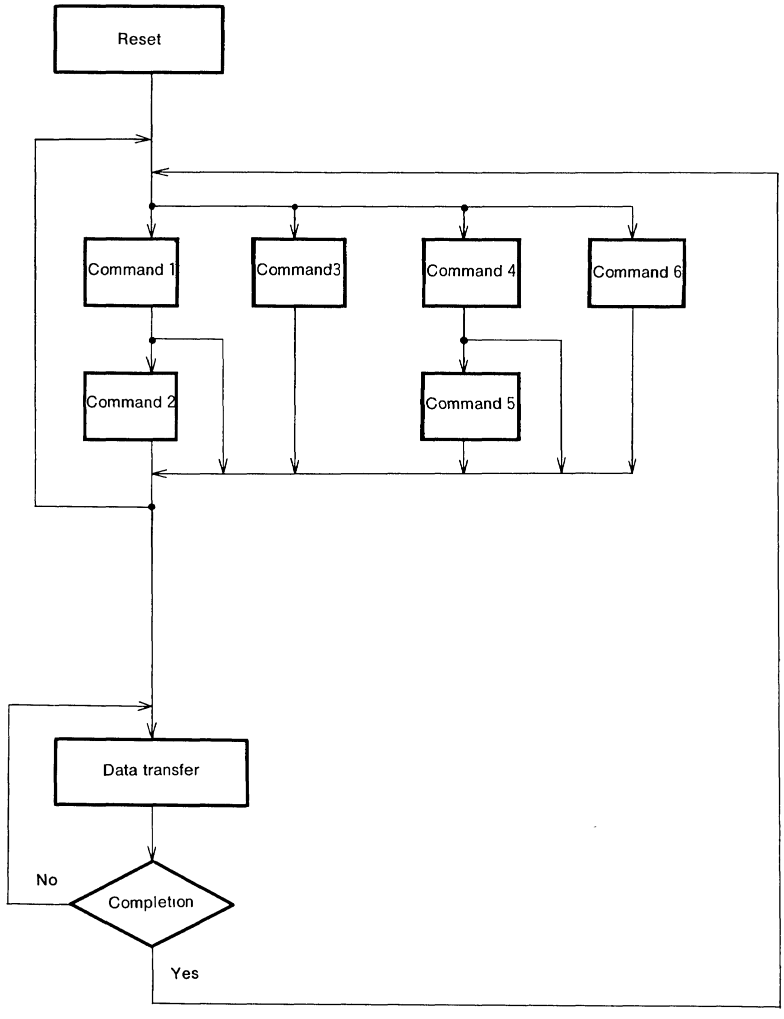
CRC deals with data characters in transmitted or received blocks. (Start, stop and wakeup bits are excluded.)

When the CRC is enabled, the transmit and receive data consists of block length (1～64 bytes) +2 bytes (block check characters). The following table shows the comparision between parity check and CRC.

Parity check	Burst error is not detected. (50% of which can be detected.)
CRC	Burst error can be detected (Burst error detection rate is more than 99.9%.)

PROGRAMMING

The command must be loaded first to the M66230 by the MPU before data communication. M66230 has 6 command registers.
Data transfer is possible when commands have been loaded to these command registers after reset.
The flowchart of the initial setting is shown in the following diagram.



Flowchart of the M66230 initial setting.

COMMAND-INSTRUCTION FORMAT

The commands are decoded by D7 and D6.

Command1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ST	EP	PEN	CRCEN	BAUD	PS

Bit	Function	Setting
D5 (ST)	Stop bit	1 : 2 bits 0 : 1 bit
D4 (EP)	Parity check	1 : Even parity 0 : Odd parity
D3 (PEN)	Parity enable	1 : Enable 0 : Disable
D2 (CRCEN)	CRC enable	1 : Enable 0 : Disable
D1 (BAUD)	Baud rate setting	1 : To command 2 (Baud rate setting)
D0 (PS)	Prescaler	1 : 1/32 division 0 : 1/2 division

Note 1 : Priority is given to parity enable, if parity enable and CRC enable are both "1" (D3, D2=1)

Command 2 (Baud rate setting The second byte when D1 bit of the command 1 is set to "1")

D7	D6	D5	D4	D3	D2	D1	D0
0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1

n : 0 ~ 255

Command 3 (Block length setting)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	D5	D4	D3	D2	D1	D0
		0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1	0 ~ 1

m : 0 ~ 63

Command 4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	IR	ER	RTS	WUMODE	RXEN	TXEN

Bit	Function	Setting
D5 (IR)	Internal reset	1 : reset
D4 (ER)	Error reset	1 : Error flag clear
D3 (RTS)	Transmission carrier control	1 : $\overline{RTS}$="L" 0 : $\overline{RTS}$="H"
D2 (WUMODE)	Wakeup mode	1 : Enable 0 : Disable
D1 (RXEN)	Receive enable	1 : Enable 0 : Disable
D0 (TXEN)	Transmit Enable	1 : Enable 0 : Disable

Command 5 (Address setting The second byte when D2 bit of the commnd 4 bit is set to "1".)

D7	D6	D5	D4	D3	D2	D1	D0

Command 6

1	1	D5	D4	D3	D2	D1	D0
D7	D6						

- D3: 1 : FIFO disable / 0 : FIFO enable
- D2: 1 : INT / 0 : $\overline{INT}$
- D1: 1 : P1=Packet transmission is complete / 0 : P1=P0
- D0: 1 : P0="H" / 0 : P0="L"

STATUS INFORMATION

Status 1

0	CRCE	PE	OE	FE	TxBEMP	RxFULL	RxBPE
D7	D6	D5	D4	D3	D2	D1	D0

- D6 (CRCE): 1 indicates that a CRC error is found in the received data
- D5 (PE): 1 indicates that a parity error is found in the received data
- D4 (OE): 1 indicates that an overrun error is found in the received data
- D3 (FE): 1 indicates that a framing error is found in the received data
- D2 (TxBEMP): 1 indicates that the transmission data buffer (FIFO) is empty
- D1 (RxFULL): 1 indicates that the received data buffer (FIFO) is full
- D0 (RxBPE): 1 indicates that the received data buffer (FIFO) is block end

Status 2

1	L	L	L	TxEMP	TxPE	WUEN	WUMODE
D7	D6	D5	D4	D3	D2	D1	D0

- D3 (TxEMP): 1 indicates that the transmission characters are not found in the transmit data buffer and transmit buffer
- D2 (TxPE): 1 indicates that packet transmission is complete from the transmit buffer
- D1 (WUEN): 1 indicates that wakeup is maintained
- D0 (WUMODE): 1 indicates the wakeup mode

TRANSMISSION FORMAT

Transmit

Parity enabled

MPU→M66230

Data character (8 bits)

Assembled data format

Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Parity bit (nil or 1 bit)	Stop bit (1~2 bits)

Transmitter output

T_XD mark condition	Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Parity bit (nil or 1 bit)	Stop bit (1~2 bits)

CRC enabled

MPU→M66230

Data character (8 bits)

After assembly

Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)

Transmitter output

		Start bit	Character	Wakeup bit	Stop bit
Block length m+1	T_XD mark condition	Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
		⋮	⋮	⋮	⋮
		Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
	+	Start bit (1 bit)	Block check character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
	+	Start bit (1 bit)	Block check character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)

TRANSMISSION FORMAT

Receive

Parity enabled

Receiver input

RxD mark condition	Start bit (1 bit)	Data character(8 bits)	Wakeup bit (nil or 1 bit)	Parity bit (nil or 1 bit)	Stop bit (1-2 bits)

Receive format

Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Parity bit (nil or 1 bit)	Stop bit (1~2 bits)

M66230→MCU

Data character (8 bits)

CRC enabled

Receiver input

		Start bit	Character	Wakeup bit	Stop bit
Block length m+1	RxD mark condition	Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
		⋮	⋮	⋮	⋮
		Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
	+	Start bit (1 bit)	Block check character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)
	+	Start bit (1 bit)	Block check character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)

Receive format

Start bit (1 bit)	Data character (8 bits)	Wakeup bit (nil or 1 bit)	Stop bit (1~2 bits)

M66230→MCU

Data character (8 bits)

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Value using the GND pin as reference	−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
P_d	Power dissipation	Actually mounted	500	mW
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
Topr	Operating temperature	−40		+85	℃

ELECTRICAL CHARACTERISTICS (T_a=−40~+85℃, V_{CC}=5V±10%, GND=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage	$\overline{RD}$, $\overline{WR}$, C/$\overline{D}$, $\overline{CS}$, D0~D7	2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage	X1	V_{CC}×0.8			V
V_{IL}	Low-level input voltage				V_{CC}×0.2	V
V_{T+}	Positive threshold voltage	R_XD, $\overline{CTS}$, $\overline{RESET}$			2.4	V
V_{T-}	Negative threshold voltage		0.6			V
V_H	Hysteresis width		0.2			V
V_{OH}	High-level output voltage	I_{OH}=−8mA $\overline{INT}$,D0~D7	V_{CC}−0.8			V
		I_{OH}=−24mA T_XD, $\overline{RTS}$, P0, P1				
V_{OL}	Low-level output voltage	I_{OL}=8mA $\overline{INT}$,D0~D7			0.55	V
		I_{OL}=24mA T_XD, $\overline{RTS}$, P0, P1			0.55	
I_{IH}	Low-level input current	V_I=V_{CC}			1.0	μA
I_{IL}	Low-level input current	V_I=GND			−1.0	μA
I_{OZH}	Off-state high-level output current	V_O=GND			5.0	μA
I_{OZL}	Off-state low-level output current	V_O=GND			−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND			40	mA
C_I	Input capacitance				10	pF
$C_{I/O}$	I/O capacitance				20	pF

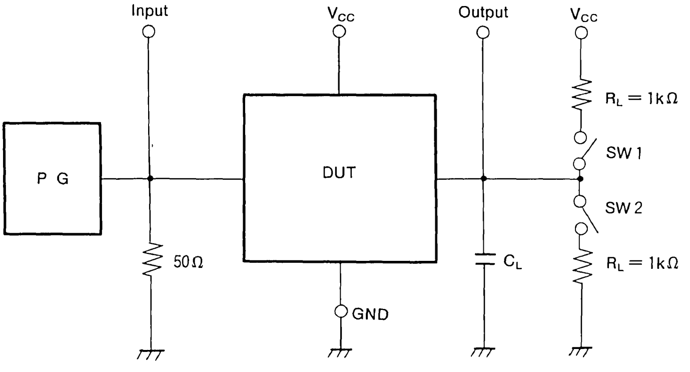
TIMING REQUIREMENTS ($T_a = -40 \sim +85$℃, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(X1)}$	Clock frequency		62.5	18		ns
$t_{w(X1)}$	Clock high-level pulse width		30	5		ns
$t_{w(X1)}$	Clock low-level pulse width		30	8		ns
$t_{r(X1)}$	Clock rise time				20	ns
$t_{f(X1)}$	Clock fall time				20	ns
$t_{su(A-\overline{R})}$	Address setup time before read ($\overline{CS}$, C/$\overline{D}$)		0	−8		ns
$t_{h(\overline{R}-A)}$	Address hold time after read ($\overline{CS}$, C/$\overline{D}$)		0	−10		ns
$t_{w(\overline{R})}$	Read pulse width		100	35		ns
$t_{su(A-\overline{W})}$	Address setup time before write ($\overline{CS}$, C/$\overline{D}$)		0	−8		ns
$t_{h(\overline{W}-A)}$	Address hold time after write ($\overline{CS}$, C/$\overline{D}$)		0	−9		ns
$t_{w(\overline{W})}$	Write pulse width		100	23		ns
$t_{su(DQ-\overline{W})}$	Data setup time before write		50	9		ns
$t_{h(\overline{W}-DQ)}$	Data hold time after write		5	−7		ns
$t_{rec(\overline{RESET})}$	Recoverry time between write		100			ns
$t_{w(\overline{RESET})}$	Reset pulse width		100	10		ns

SWITCHING CHARACTERISTICS ($T_a = -40 \sim +85$℃, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZH(\overline{R}-DQ)}$	Data output enable time after read			43	100	ns
$t_{PZL(\overline{R}-DQ)}$	Data output enable time after read			52	100	ns
$t_{PHZ(\overline{R}-DQ)}$	Data output disable time after read			33	85	ns
$t_{PLZ(\overline{R}-DQ)}$	Data output disable time after read			32	85	ns
$t_{PLH(\overline{R}-\overline{INT})}$	$\overline{INT}$ output propagation time after read data			62	170	ns
$t_{PHL(\overline{R}-\overline{INT})}$	$\overline{INT}$ output propagation time after read data			63	170	ns
$t_{PLH(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write data			54	150	ns
$t_{PHL(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write data			54	150	ns
$t_{PLH(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write command (command 4)			33	100	ns
$t_{PHL(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write command (command 4)			35	100	ns
$t_{PLH(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write command (command 6)			28	100	ns
$t_{PHL(\overline{W}-\overline{INT})}$	$\overline{INT}$ output propagation time after write command (command 6)			30	100	ns
$t_{PLH(\overline{W}-P0)}$	P0 output propagation time after write command			25	70	ns
$t_{PHL(\overline{W}-P0)}$	P0 output propagation time after write command			28	70	ns
$t_{PLH(\overline{W}-P1)}$	P1 output propagation time after write command			26	70	ns
$t_{PHL(\overline{W}-P1)}$	P1 output propagation time after write command			28	70	ns
$t_{PLH(\overline{W}-\overline{RTS})}$	$\overline{RTS}$ output propagation time after write command			25	70	ns
$t_{PHL(\overline{W}-\overline{RTS})}$	$\overline{RTS}$ output propagation time after write command			27	70	ns

TEST CIRCUIT

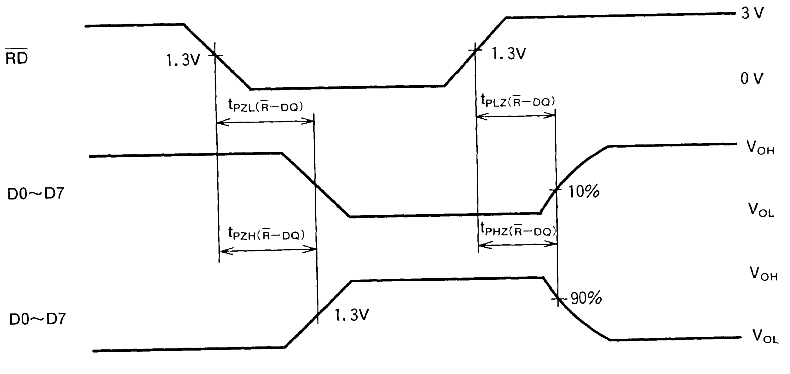


Parameter	SW1	SW2
t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

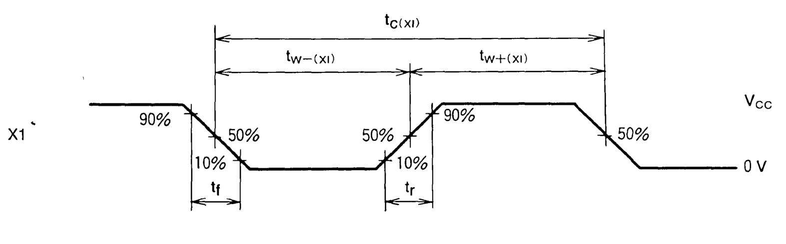
(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r=3ns, t_f=3ns
(2) The capacitance C_L = 150pF includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

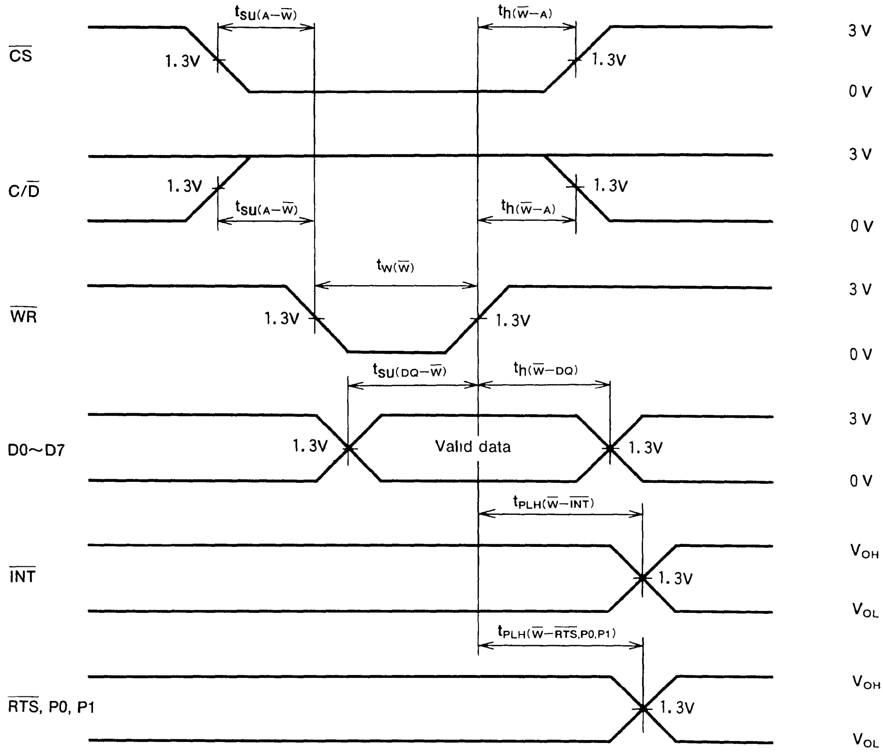
Input/output waveform at read data and read status



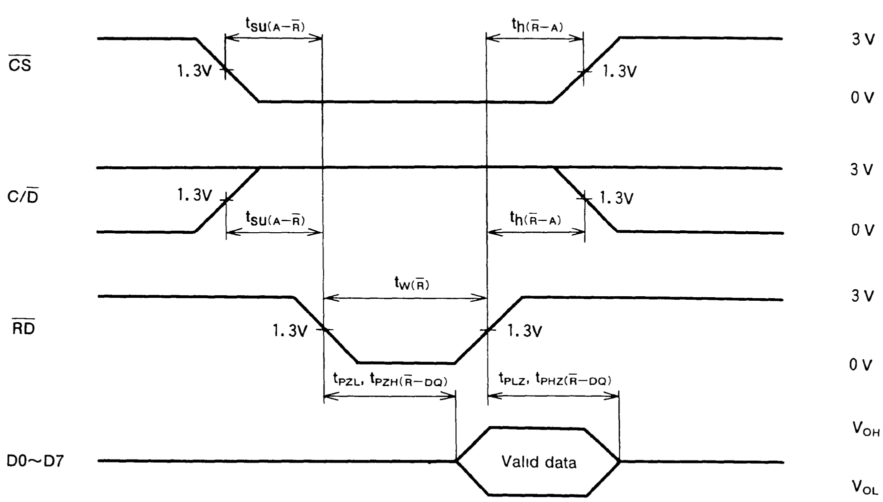
Clock Timing



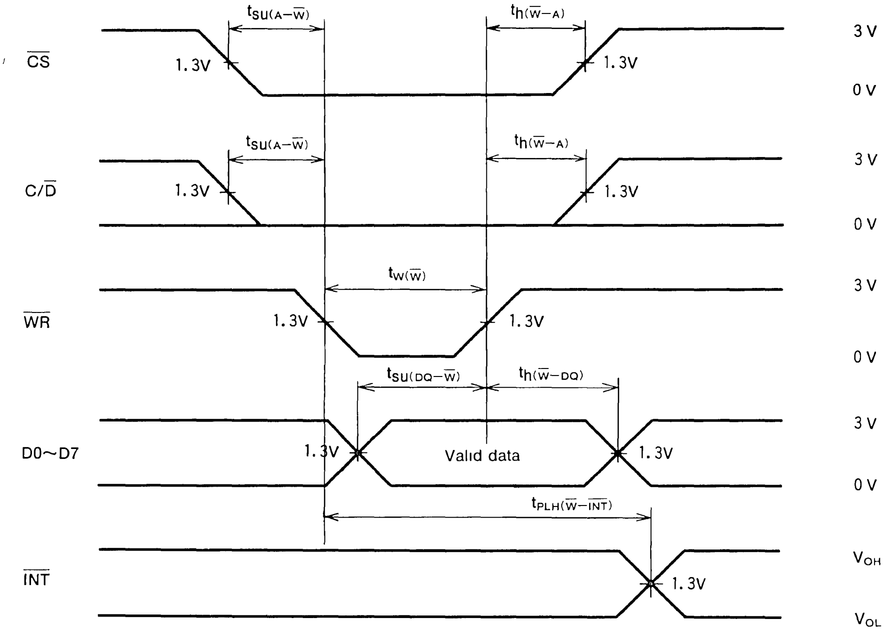
Write control cycle (MPU→M66230)



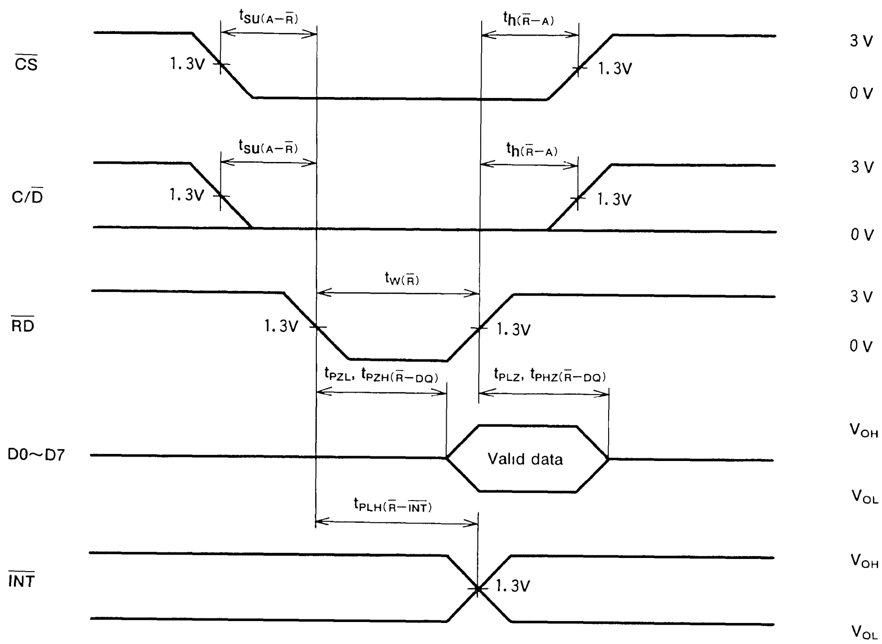
Read control cycle (M66230→MPU)



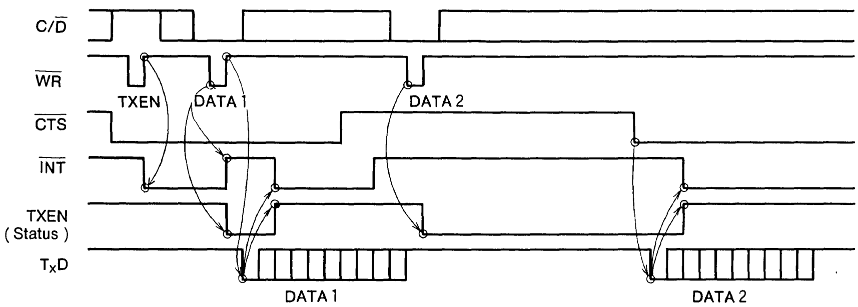
Write data cycle (MPU→M66230)



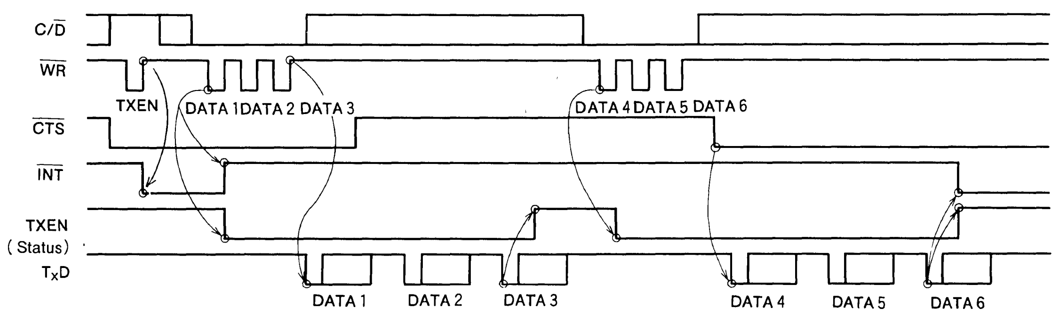
Read data cycle (M66230→MPU)



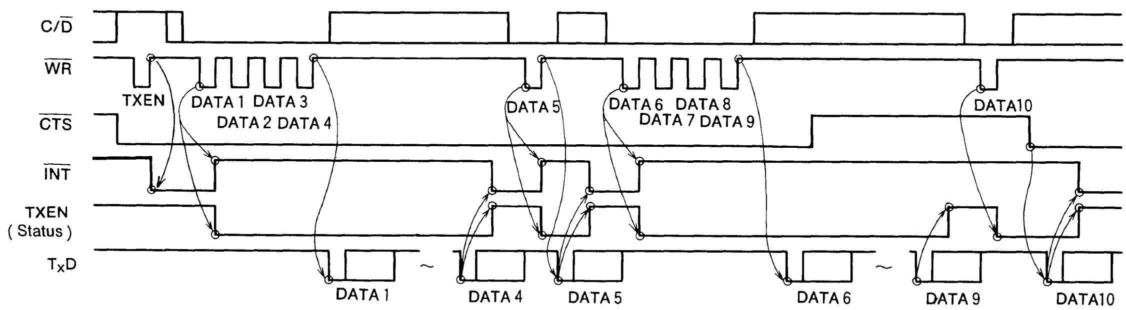
Transmitter control and flag timing (block length=1)



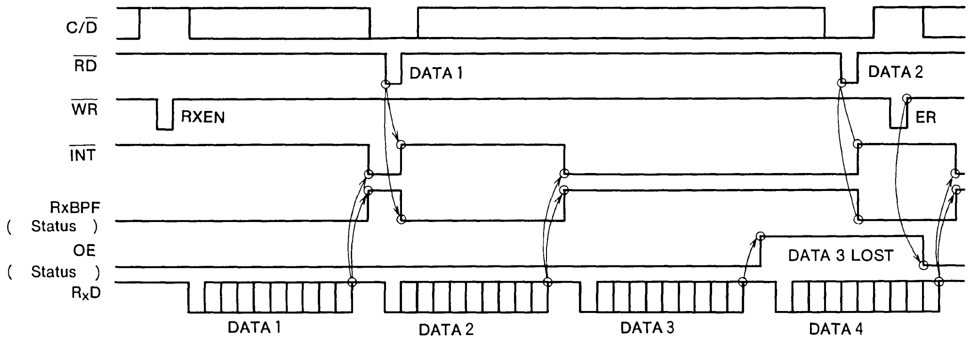
Transmitter control and flag timing (block length=3)



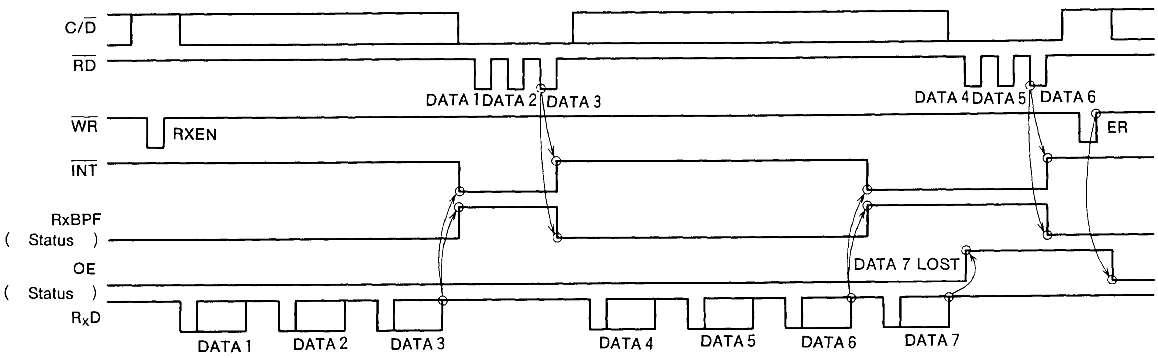
Transmitter control and flag timing (block length=5)



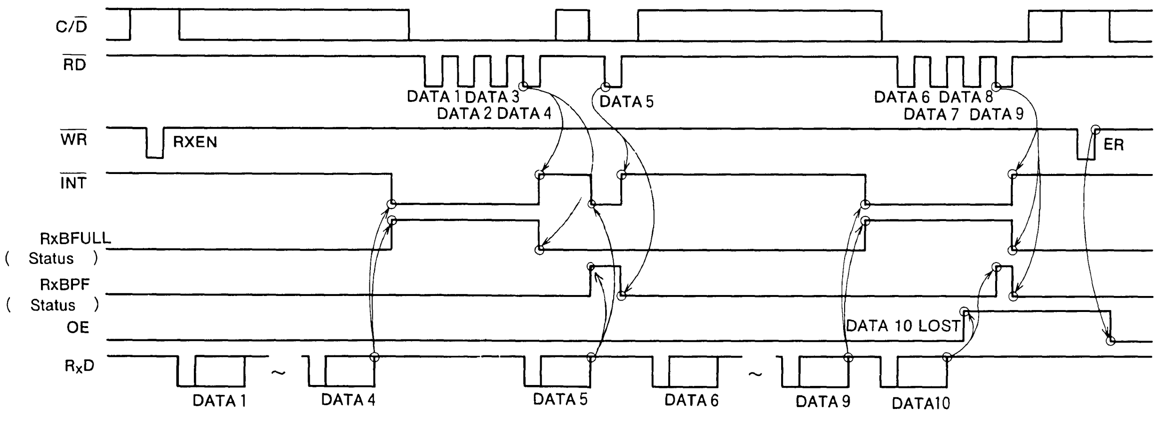
Receiver control and flag timing (block length=1)



Receiver control and flag timing (block length=3)



Receiver control and flag timing (block length=5)



DESCRIPTION

The M66240P/FP is an integrated circuit for a 4-channel PWM generator made using the CMOS process.

The M66240P/FP can connect directly to the MPU data bus and consists of a 16-bit prescaler and a PWM counter. The pulse output includes PWM mode, one-shot mode and high-level and low-level independent setting mode, and independent channel control is possible. A software servo system is implemented by combining A-D function and timer function of on a MCU (Micro controller unit).

FEATURES

- 4-channel independent control possible
- 3 operation modes : PWM mode (Mode 0), one-shot mode (Mode 1), high-level and low-level independent setting mode (Mode 2)
- PWM repetitive frequency : 50kHz (max) (Mode 0, 8-bit resolution, prescaler setting=0 : $f(X_{IN})/255$)
- Output polarity selection possible
- External triggering possible
- Output after reset and disable is placed in the high-impedance state.
- Change of mode setting becomes effective after the current cycle.
- Output buffer drive capability : $I_O = \pm 24mA$

APPLICATION

Control of DC motors and stepping motors, heater phase controllers, software servos for office automation equipment, and industrial equipment.

FUNCTION

Input to D0~D7 is loaded as command when C/$\overline{D}$=1, and as data when C/$\overline{D}$=0. There are three kinds of commands. (See Fig. 2.)

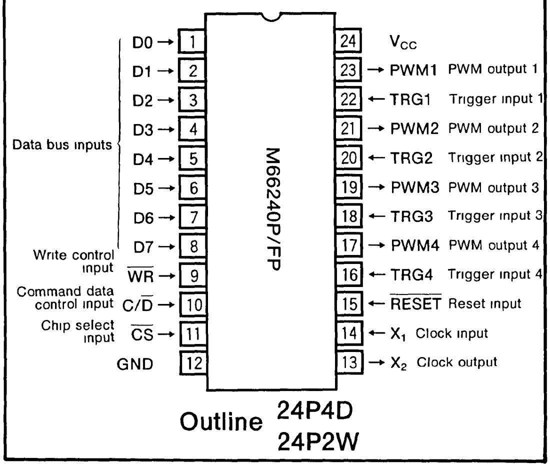
Command 1 sets each channel's mode.

Command 2 specifies to which register data is written, either the prescaler of each channel, or the 16-bit data register for PWM counter. The data after the second byte specified by command 2 is written in the order shown by Fig. 3.

The PWM values are written to the H register in Mode 0 and Mode 1. (In mode 0 at 8-bit resolution, only the lower byte of the H register is used.) In Mode 2, the PWM values are written to both H and L registers.

Command 3 is used to start or stop the prescaler and PWM counter operation. The output enters the high-impedance state if a disable is specified during PWM output.

PIN CONFIGURATION (TOP VIEW)



To change the values of all 16 bits in the prescaler or the PWM counter during operation, values should be written to the upper byte first and then to the lower byte. To change the values of the lower byte only, the values of only the lower byte should be written.

To change the values of the upper byte, the values of all 16 bits should be written. To change the values of H register in Mode 2, the H register value should be written followed by the L register value.

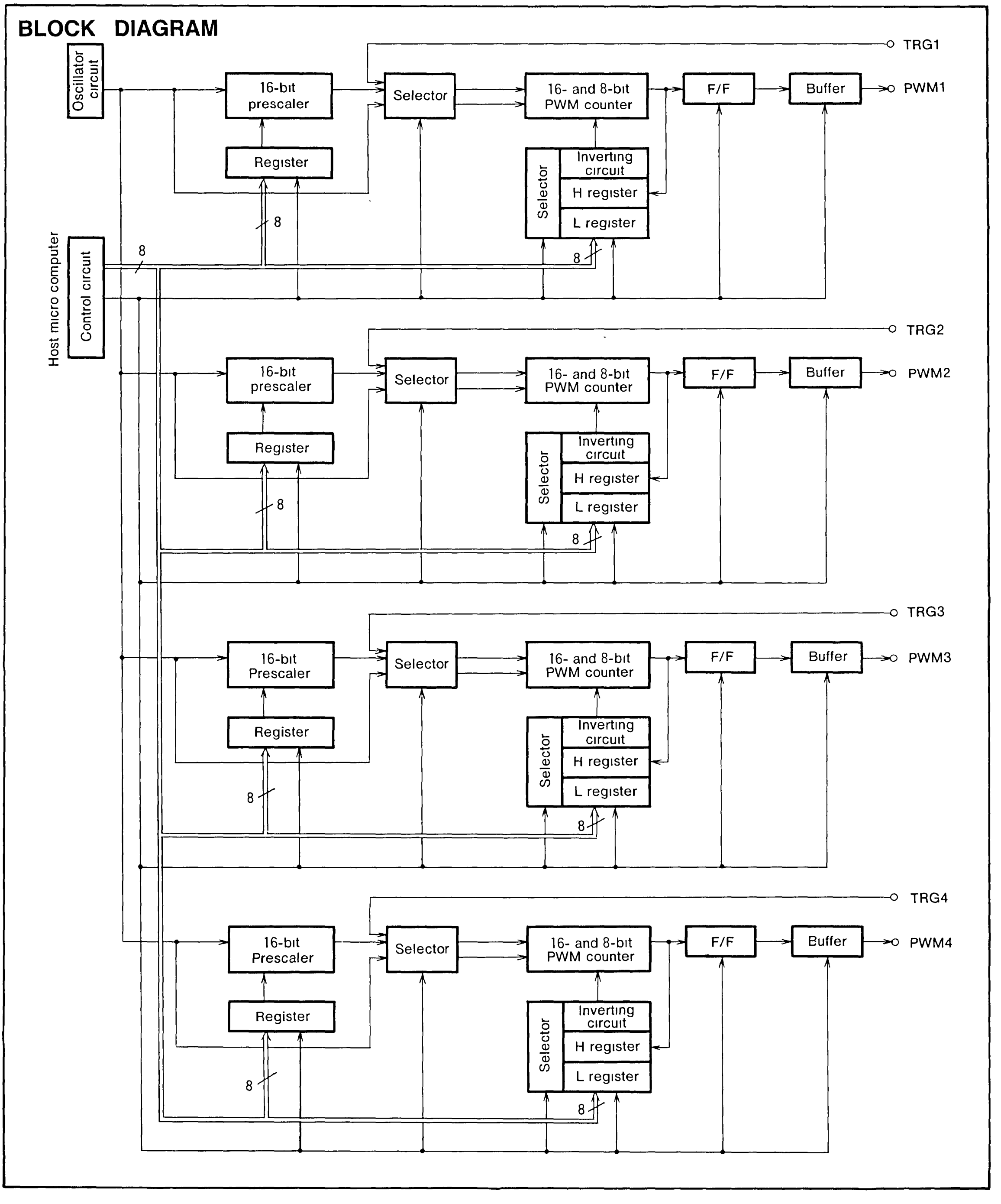
When values are written to the lower byte (lower byte of L register in Mode 2), the write cycle of data register is completed.

If data register value is changed during PWM output (cycle A), (i. e. when write to the lower byte of the prescaler register or the PWM register is completed), PWM output is changed from the next cycle (B) to the output PWM cycle (A). (See Fig. 1)

To change the mode (i.e., to execute command 1), disable the output first (i.e., execute command 3).

Fig. 4 shows the flow chart of the basic operation. (The order of the prescaler's and PWM counter's data setting is not fixed.)

BLOCK DIAGRAM



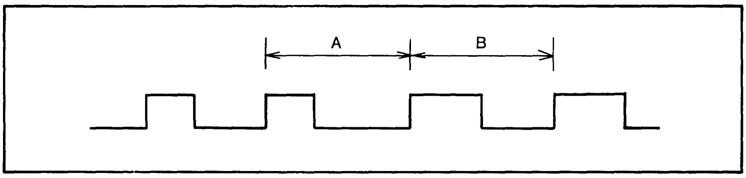


Fig. 1 Change of PWM output

Command 1

D7	D6	D5	D4	D3	D2	D1	D0
"1" Mode selection	Channel selection 00 : PWM1 01 : PWM2 10 : PWM3 11 : PWM4		Mode 00 : Mode 0 (PWM mode) 01 : Mode 1 (One-shot mode) 10 : Mode 2 (H, L specific mode) 11 : Prohibition		PWM resolution 0 : 8 bits 1 : 16 bits (Effective only in Mode 0)	External trigger 0 : OFF 1 : ON	"H" width polarity 0 : L 1 : H

Command 2

D7	D6	D5	D4	D3	D2	D1	D0
"0" Numeric value control	Channel selection 00 : PWM1 01 : PWM2 10 : PWM3 11 : PWM4		0 : Numeric value control	0 : For prescaler	×	0 : For lower byte 1 : For upper byte	×
				1 : For PWM counter	0 : For L width 1 : For H width	1 : For upper byte 0 : For lower byte	×

"1" is specified for Mode 0 and 1

Prescaler value and PWM counter value are set by the unit of byte after the second byte

(See Fig 3)

Command 3

D7	D6	D5	D4	D3	D2	D1	D0
"0" Enable/disable control	×	×	1 : Enable control	PWM4	PWM3	PWM2	PWM1

D3–D0: 0 : Disable, 1 : Enable

× : Don't care

Fig. 2 Commands

First byte (command 2)			Second byte	Third byte	Fourth byte	Fifth byte	Remark
D3	D2	D1					
1	1	1	Upper byte for PWM H register	Lower byte for PWM H register	—	—	When Mode0 or 1
1	1	0	Lower byte for PWM H register	—	—	—	
1	1	1	Upper byte for PWM H register	Lower byte for PWM H register	Upper byte for PWM L register	Lower byte for PWM L register	When Mode 2
1	1	0	Lower byte for PWM H register	Upper byte for PWM L register	Lower byte for PWM L register		
1	0	1	Upper byte for PWM L register	Lower byte for PWM L register	—	—	
1	0	0	Lower byte for PWM L register	—	—	—	
0	×	1	Upper byte for prescaler register	Lower byte for prescaler register	—	—	
0	×	0	Lower byte for prescaler register	—	—	—	

× : Don't care

Fig. 3 Data-setting sequence for registers

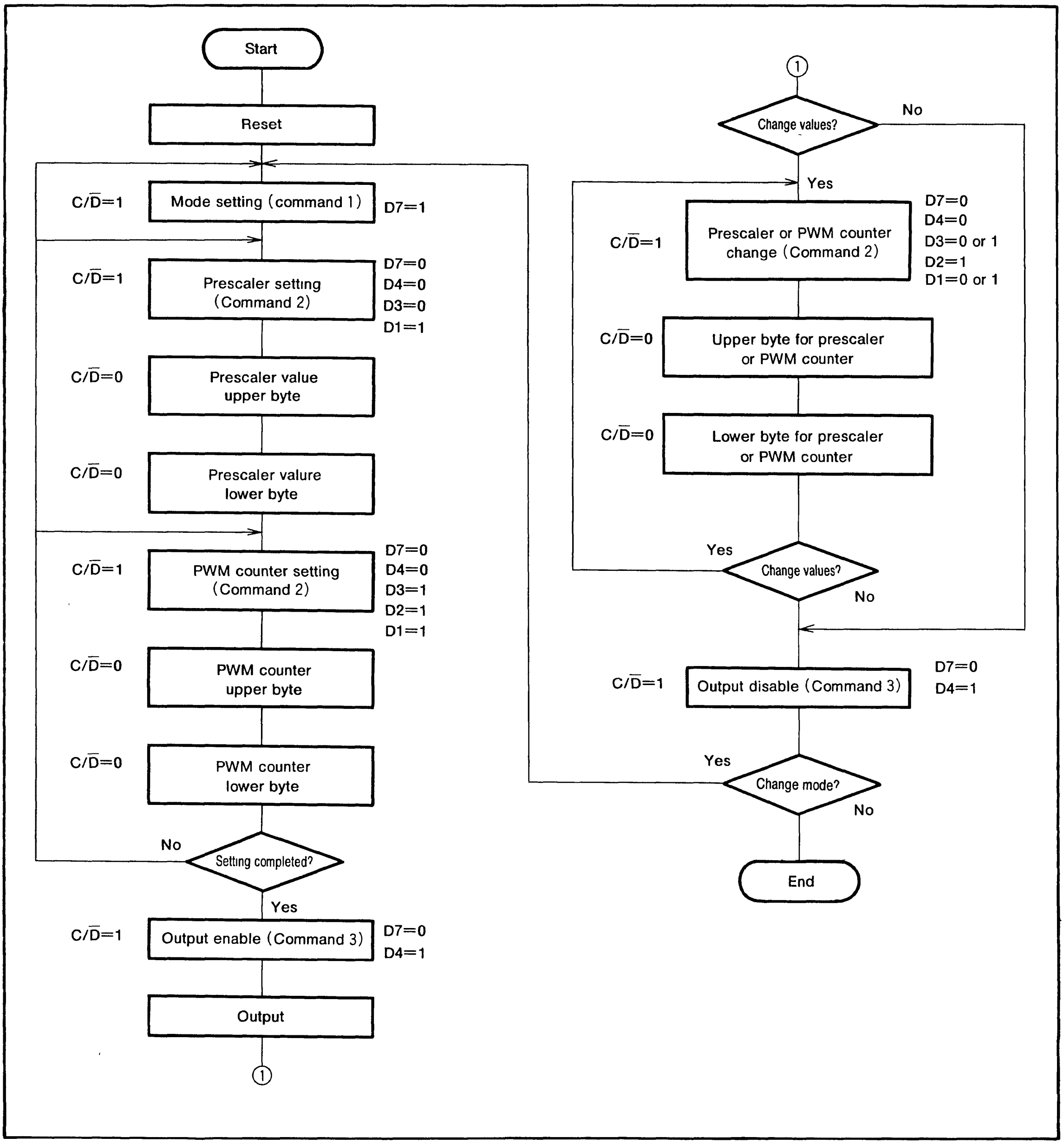


Fig. 4 Flow chart in Mode 0 or 1 (for one channel)

PIN DESCRIPTION

Pin name	Description	I/O	Function
$\overline{RESET}$	Reset input	Input	Clears command register at low level
D0～D7	Data bus input	Input	8-bit data bus to input data or commands from MCU
$\overline{WR}$	Write control input	Input	Write data on the data bus to command register or data register at the leading edge from low-to high-level
C/$\overline{D}$	Command/data control input	Input	Data at the data bus is regarded as a command at high level and as data at low level.
$\overline{CS}$	Chip select input	Input	Communication with MPU is enabled at low-level Any control from MCU is ignored at high level.
X_1	Clock input	Input	I/O to the built-in clock generator circuit A crystal oscillator is connected between X_1 and X_2 To use the external clock, connect the clock oscillator source to the pin X_1 and leave pin X_2 open
X_2	Clock output	Output	
TRG1～TRG4	Trigger input	Input	This is used when external trigger is selected in mode setting Set to low level when not in use
PWM1～PWM4	PWM output	Output	PWM output pins Outputs become the high-impedance state after reset or after disable is specified by command 3

MODE DESCRIPTION

The M66240P/FP has a built-in 16-bit prescaler and a PWM counter. The duty cycle of output pulse can be freely specified by changing the values of the prescaler and the PWM counter. The output modes include PWM mode (Mode 0), one-shot mode (Mode 1) and high-level and low-level independent setting mode (Mode 2). The description of these modes is given below.

(1) PWM mode (Mode 0)

This mode is selected by writing "0" to D4 and D3 in command 1.

Fig. 10-A shows the block diagram of this mode (for one channel).

The 16-bit PWM counter can be used as an 8-bit PWM counter only in this mode (command 1 : D2=0). Write the PWM value to the lower byte of H register when PWM resolution is set at 8-bit. In this mode, the H output pulse width is determined by the prescaler register value L and PWM register valure M. The PWM output cycle time is determined by the prescaler register valure L, irrespective of the PWM register value. (See Fig. 5)

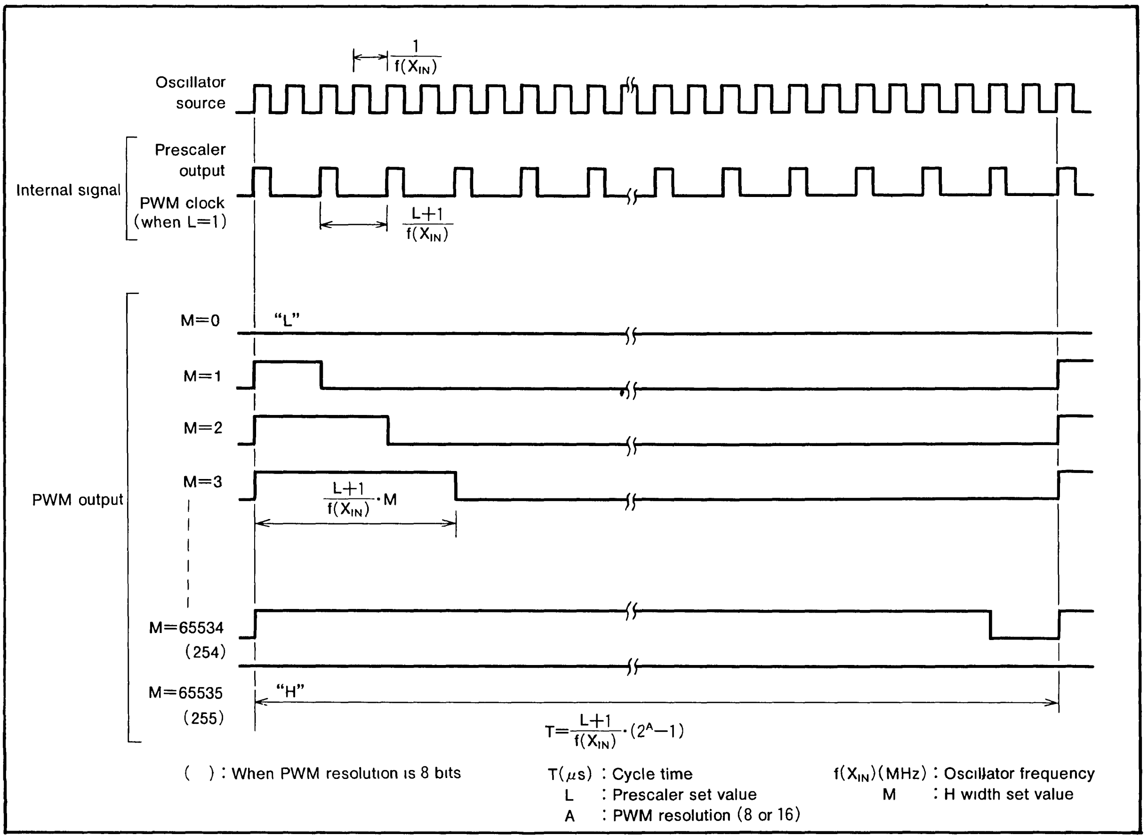


Fig. 5 PWM mode (Mode 0)

If the external trigger ON is selected by D1 in command 1, no pulse is output to the PWM output even if enable in command 3 is specified

In this case, pulse is output to PWM output by setting the trigger input TRG to high level.

If TRG is set to low level during PWM output, the PWM output maintains the state at that time. It is started from that point if the TRG is set to high level. (See Fig. 6)

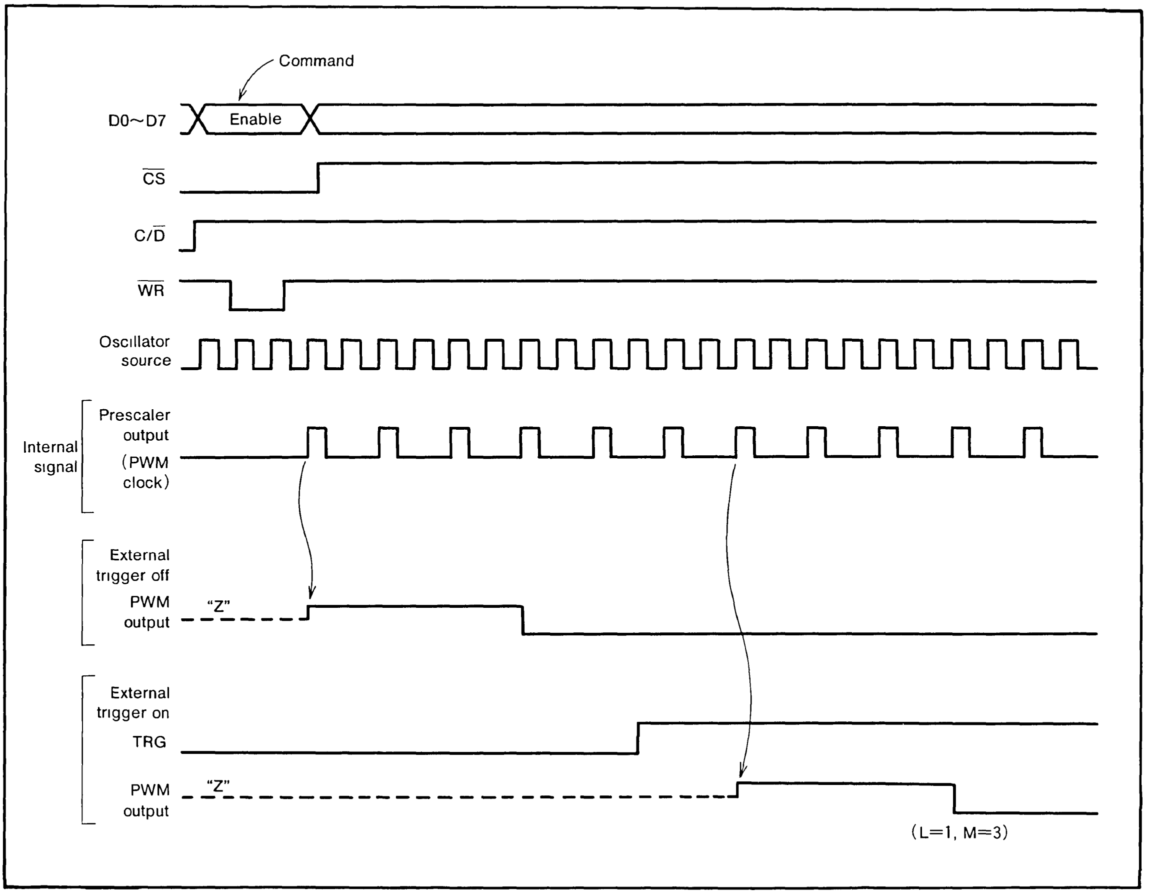


Fig. 6 PMW mode (Mode 0) with external trigger

(2) One-shot mode (Mode 1)
This mode is selected by setting D4=0 and D3=1 in command 1.
Fig. 11-B shows the block diagram in this mode (for one channel).
In this mode, one-shot output, determined by the PWM register value M, is output by the trigger signal. Operation varies according to the choice of external and internal trigger signals.
① External trigger selected (D1 = 1 in command 1): In this mode, one-shot output is output on the input of trigger pulse to the trigger input TRG. Therefore, the cycle of the output pulse is the same as the cycle of the trigger input TRG pulse f_{IN}.
The output pulse duty cycle is determined by the prescaler register value L and PWM register valure M. (See Fig. 7)

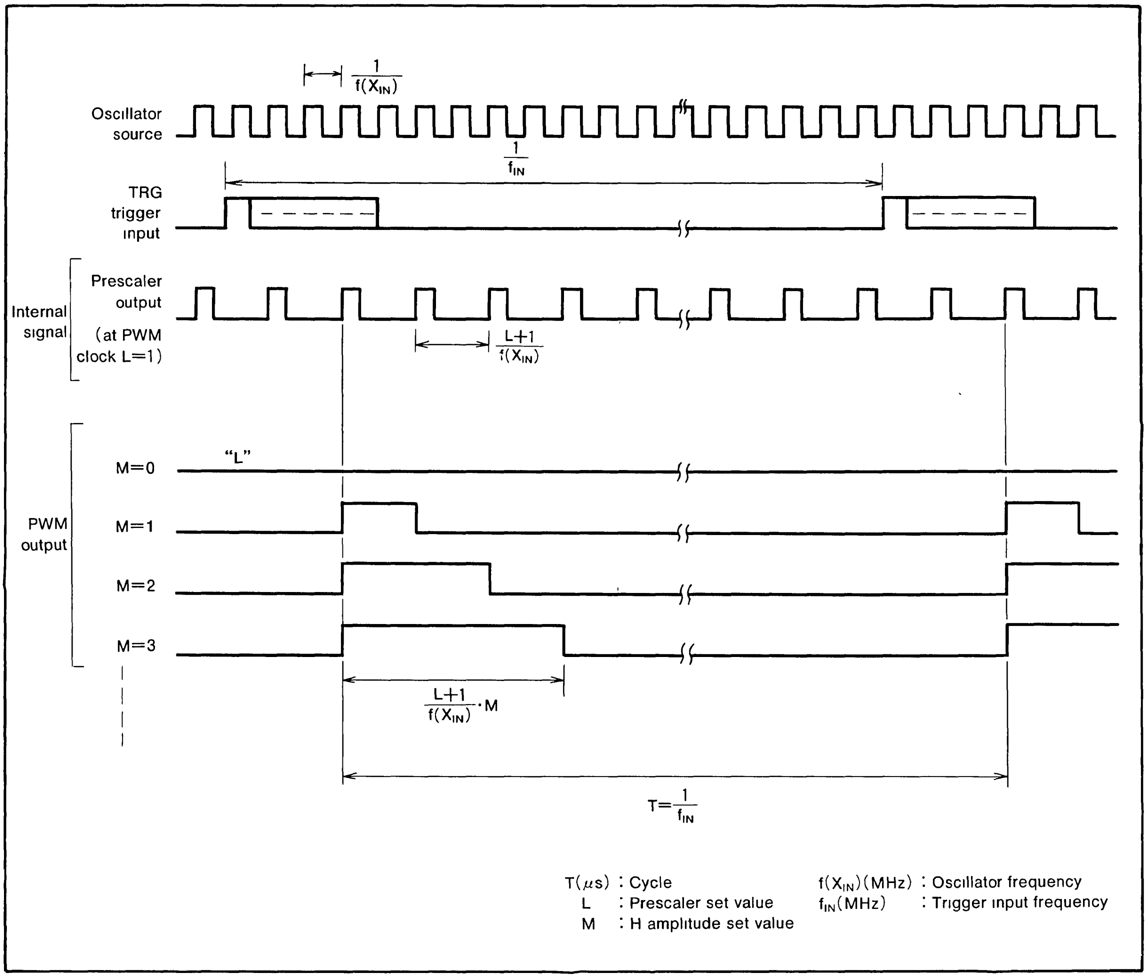


Fig. 7 One-shot mode (Mode 1) with external trigger

② When the internal trigger is selected (D1 = 0 in command 1)
In this mode, the trigger signal is generated by the prescaler. Therefore, the cycle time T of output pulse is determined by the prescaler register value L. In this case, the oscillator source becomes the PWM counter clock and the output pulse duty cycle is determined by the PWM register value M. (See Fig. 8)

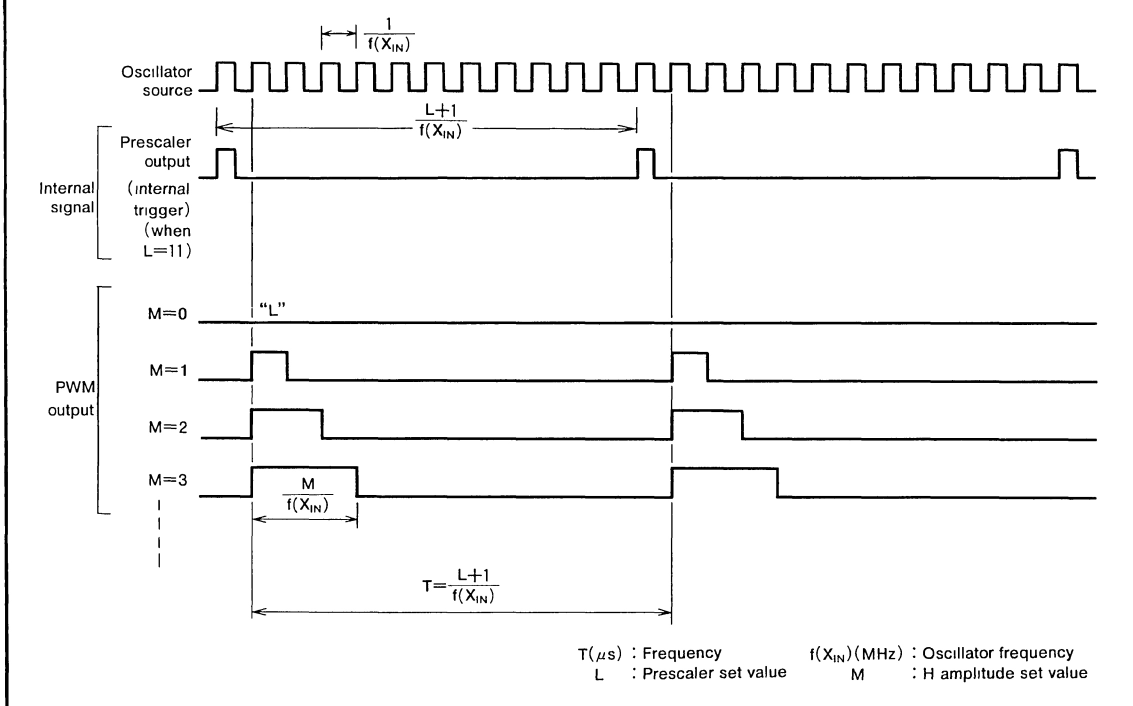


Fig. 8 One-shot mode (Mode 1) with internal trigger

In the one-shot mode, if the cycle of the trigger pulse becomes smaller than the PWM register value, the trigger state is started.

(3) H, L independent setting mode (Mode 2)
This mode is selected by writing D4=1 and D3=0 in command 1. Fig. 10-C shows the block diagram of this mode (for one channel).
The high-level pulse value M is set to the H register of PWM in Modes 0 and 1, but, in this mode, the high-level pulse value M is set to the H register of PWM and the low-level pulse value N is set to the L register of PWM. Therefore, the duty cycle of PWM output and the cycle time T are determined by the prescaler register value L and H and L register values M and N. (See Fig. 9)
If external trigger ON is set by D1 in this mode, pulse is output by setting the trigger input TRG at high level in the same manner as in Mode 0.

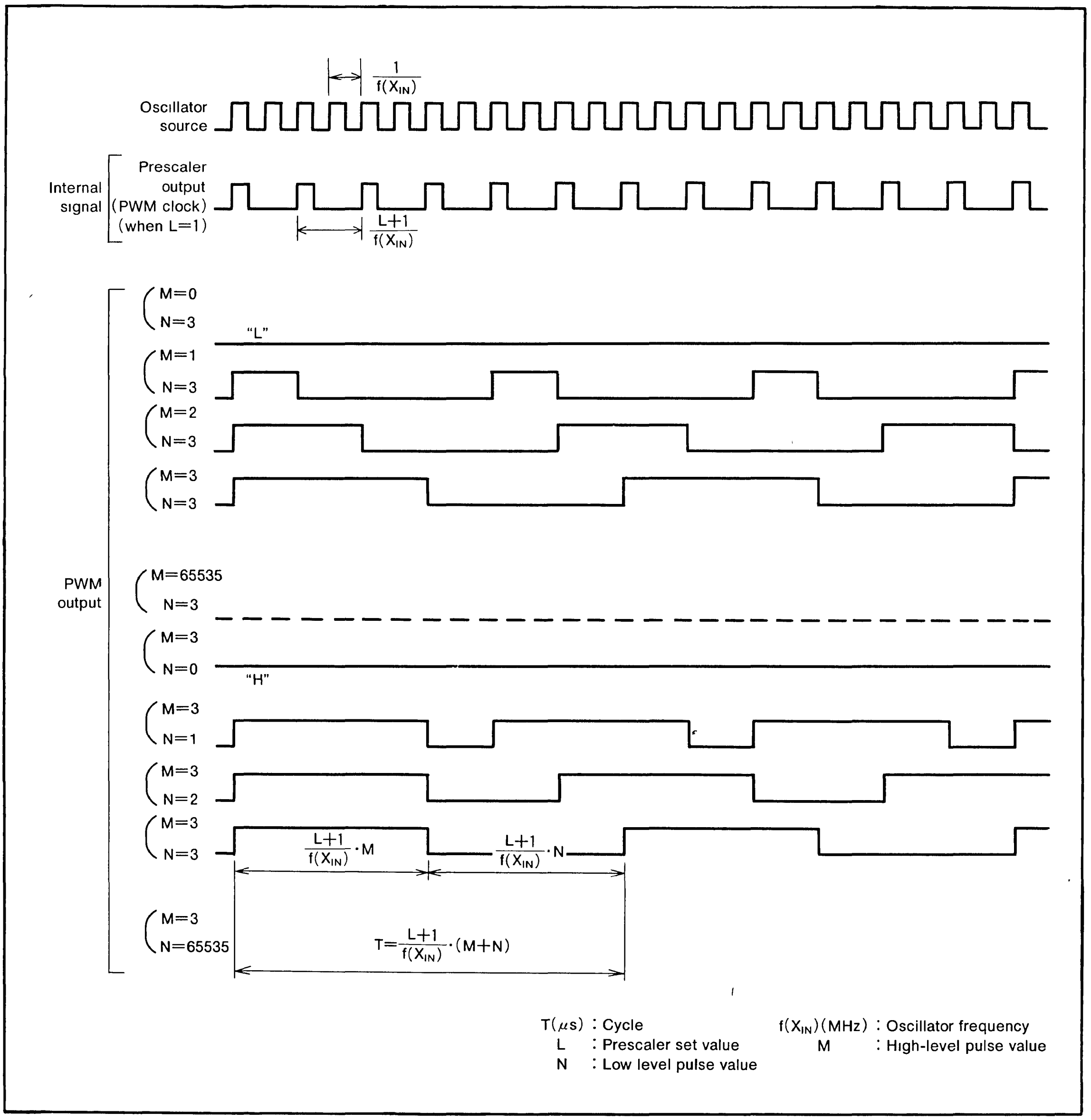


Fig. 9 H, L independent setting mode (Mode 2)

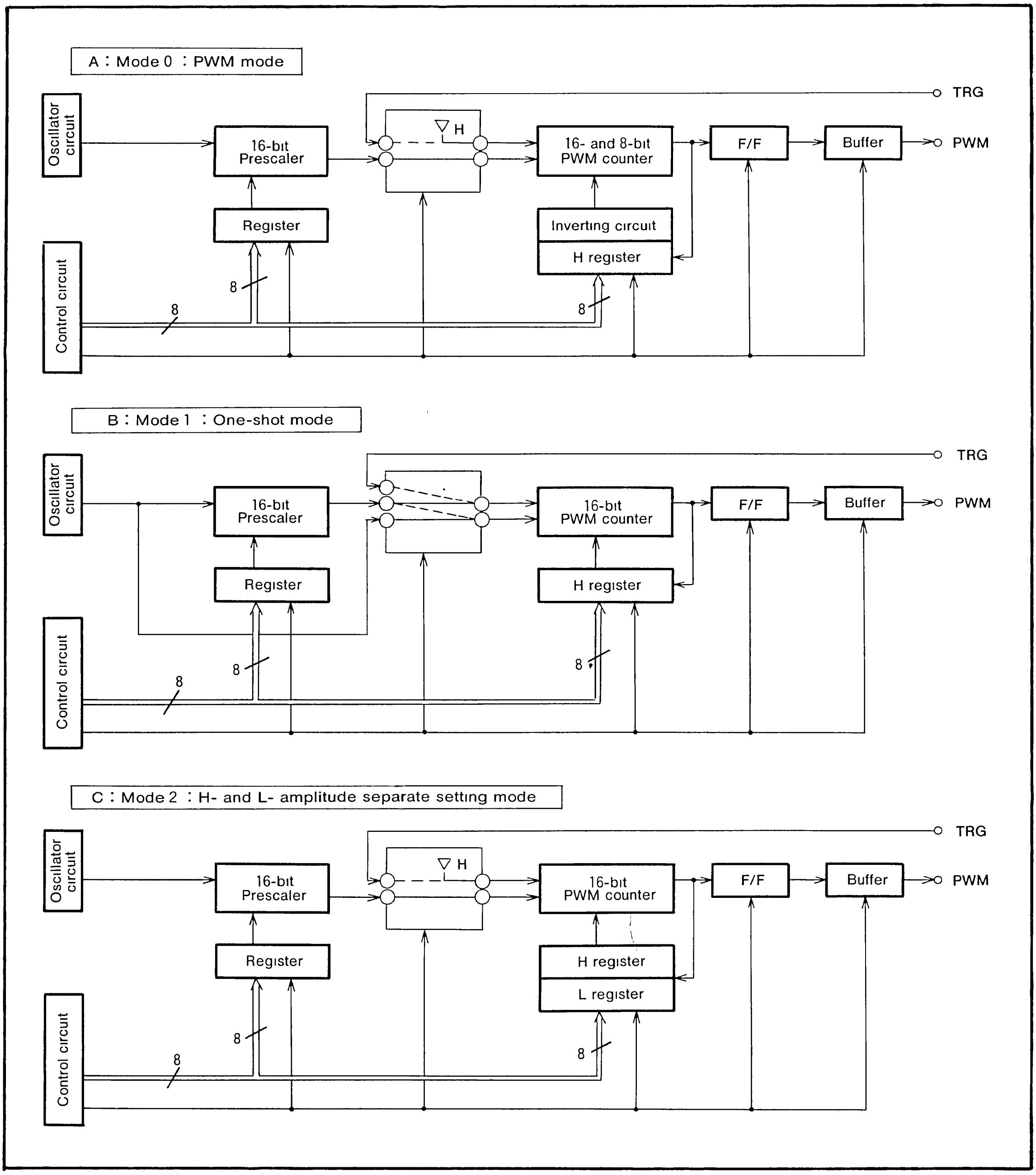
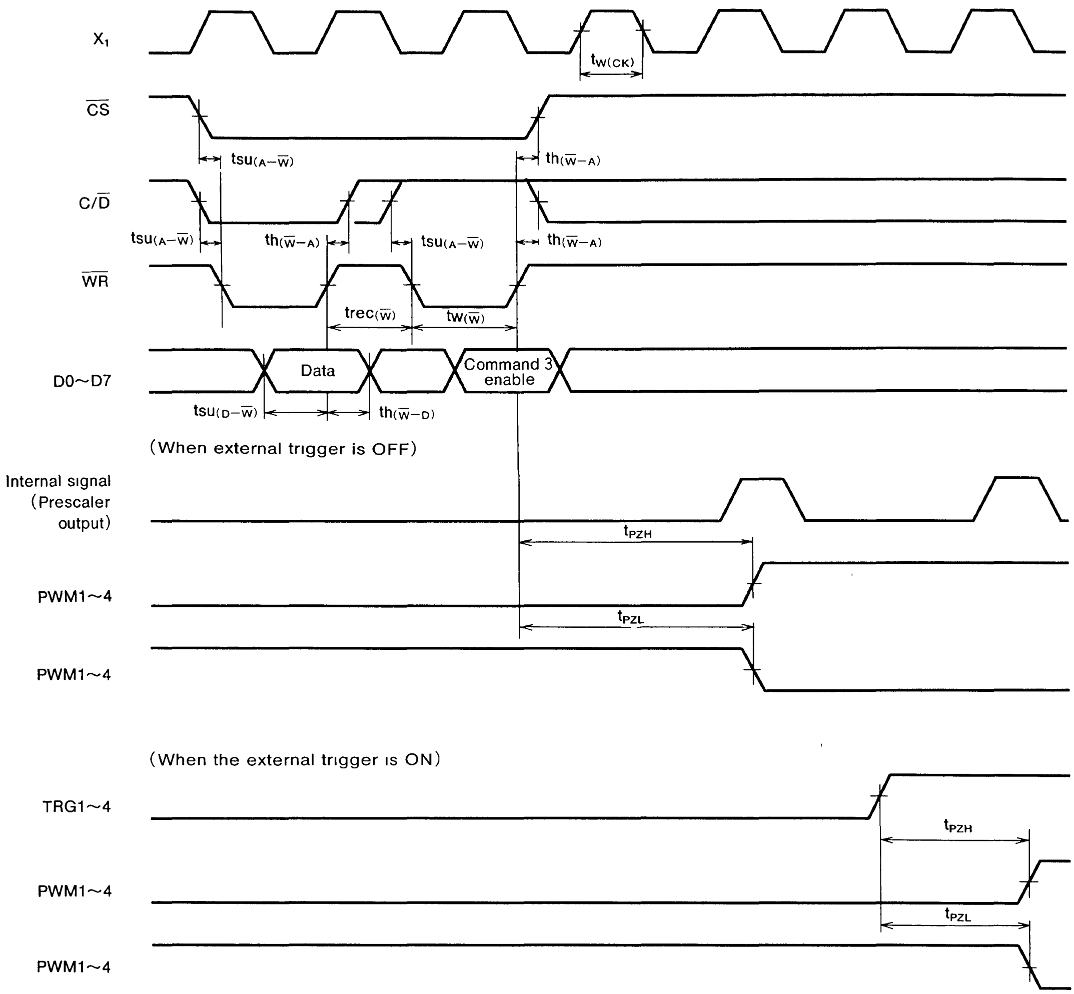


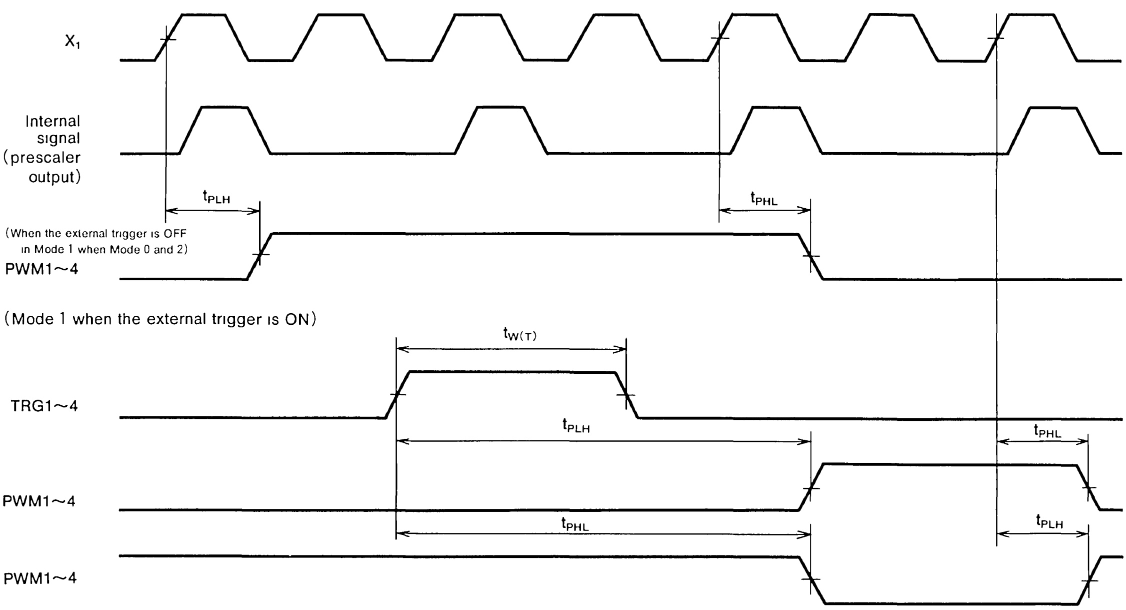
Fig. 10 Block diagram (each mode)

TIMING DIAGRAM

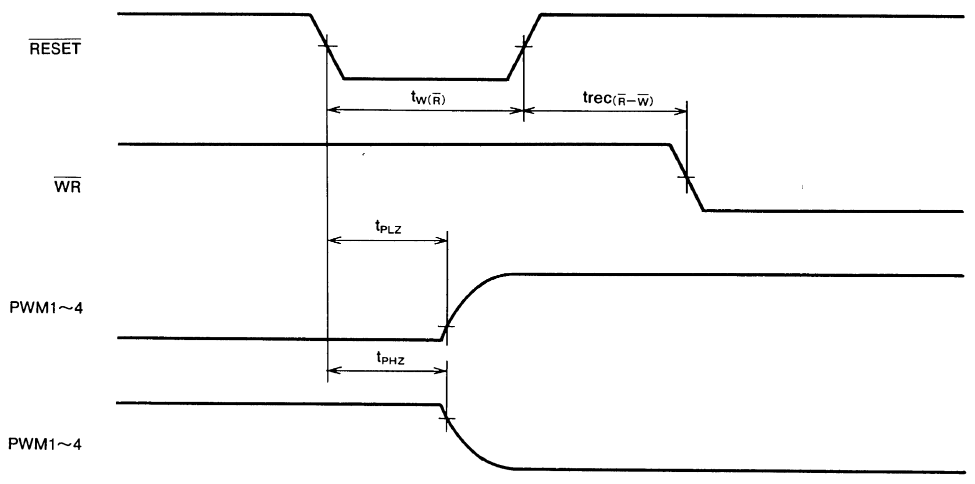
(1) MCU Interface



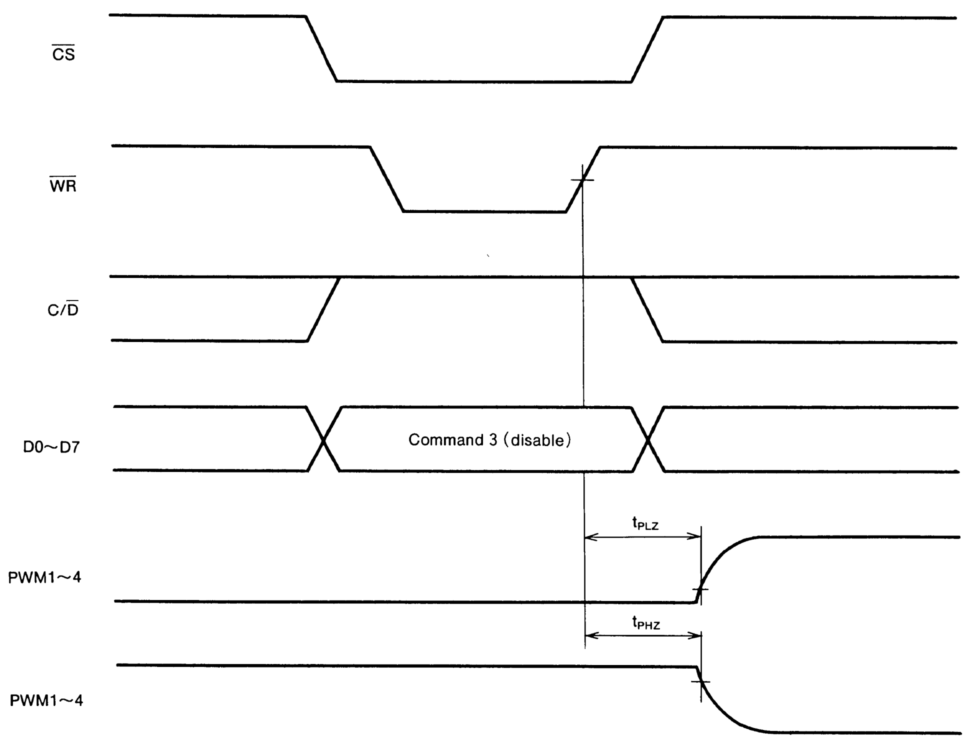
(2) Operation


X1
Internal signal (prescaler output)
tPLH
tPHL
(When the external trigger is OFF in Mode 1 when Mode 0 and 2)
PWM1~4
(Mode 1 when the external trigger is ON)
tW(T)
TRG1~4
tPLH
tPHL
PWM1~4
tPHL
tPLH
PWM1~4

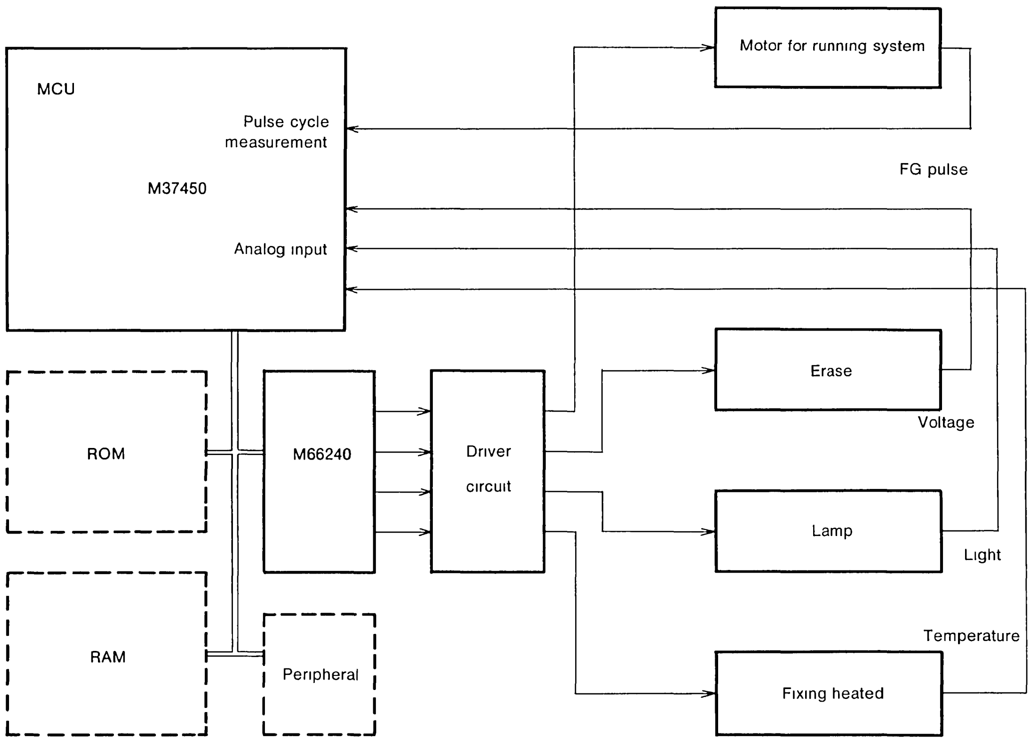
(3) When reset



(4) When disabled



APPLICATION EXAMPLE



Note : M37450 :	ROM	4KB～16KB
	RAM	128B～384B
	Timer	Multi-function 16-bit type with pulse cycle measurement mode 3 pieces
	A-D	8 bits 8 channels
	PWM	20kHz cycle 1 channel
	UART	Clock sync and async one channel

M66500SP/FP

PROGRAMMABLE BUFFERED I/O EXPANDER

DESCRIPTION
The M66500SP/FP is a large-scale integrated circuit chip for programmable high-speed I/O interface, manufactured using a Bi-CMOS process and is suitable for 8-and 16-bit high-speed CPU I/O ports The device is operated by a single 5V power supply and consists of three sets of 8-bit I/O ports, two sets of 8-bit high-withstand voltage output-only ports, and one 4-bit input-only port.

FEATURES
- I/O expandable up to 44 bits
- No-wait direct connection with 12MHz CPU
- Output pattern write in the input mode
- Output pin state read from CPU
- Transistor array drive
- 16-bit high-withstand voltage output-only port, 35V and 48mA*
- TTL input level at CPU-side pin
- CMOS-level Schmitt trigger input for I/O pin

APPLICATION
I/O port expander for microprocessors M37450, M37700 and M5L8085.

FUNCTIONAL DESCRIPTION
The M66500P/FP is a high-speed general-purpose programmable I/O expander that can be directly connected to high-speed CPUs with 0 wait states. The device consists of three sets of 8-bit I/O ports (ports A, B and C), two sets of 8-bit high-withstand voltage output-only ports (ports E and F), and a 4 bit input-only port G. These I/O ports can be programmed as input or output ports.

Ports A, B and C consist of CMOS circuits and are capable of driving transistor arrays with $I_{OH} = -2.5mA$ and $I_{OL} = 2.5mA$.

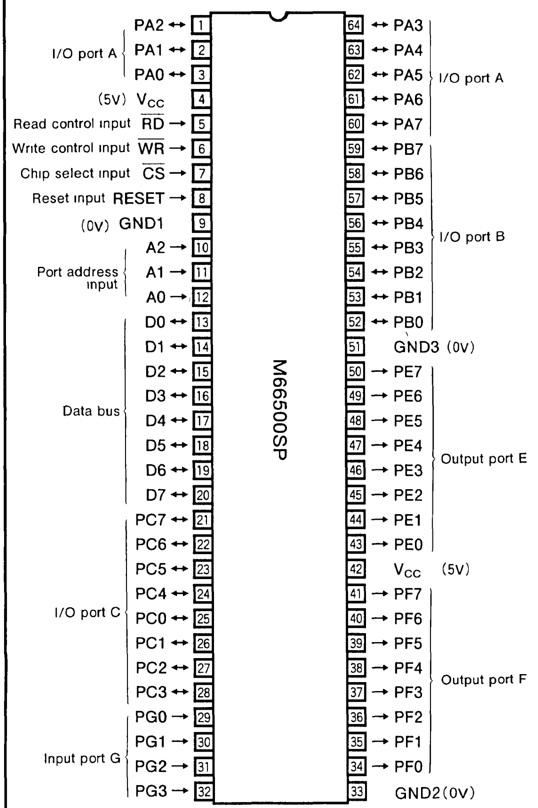
Ports E and F are high-withstand voltage, high-current-drive, bipolar open collector outputs. Ports G is an input-only port with hysteresis input.

Port C can be divided into a pair of 4-bit I/O ports. Any bit can be set or reset if the port is originally set for output.

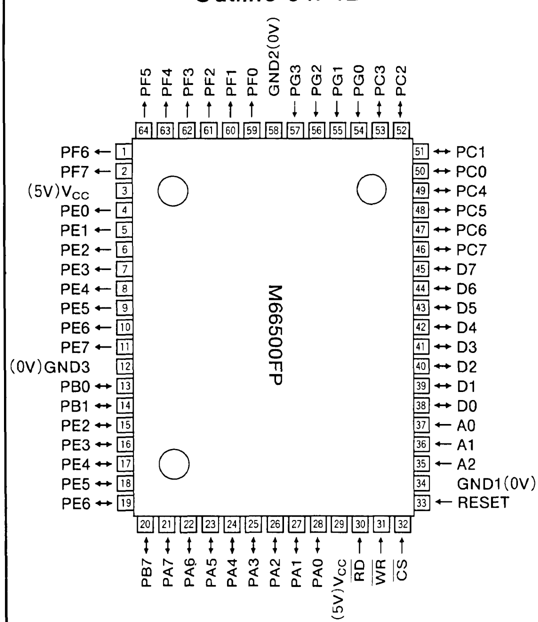
If the reset input (RESET) becomes high-level, output-only ports E and F enters a high-level output disable status, I/O ports are set to input mode, and all other ports enter the high-impedance state.

 * : I_{OL} of the M66500FP is 24mA.

PIN CONFIGURATION (TOP VIEW)

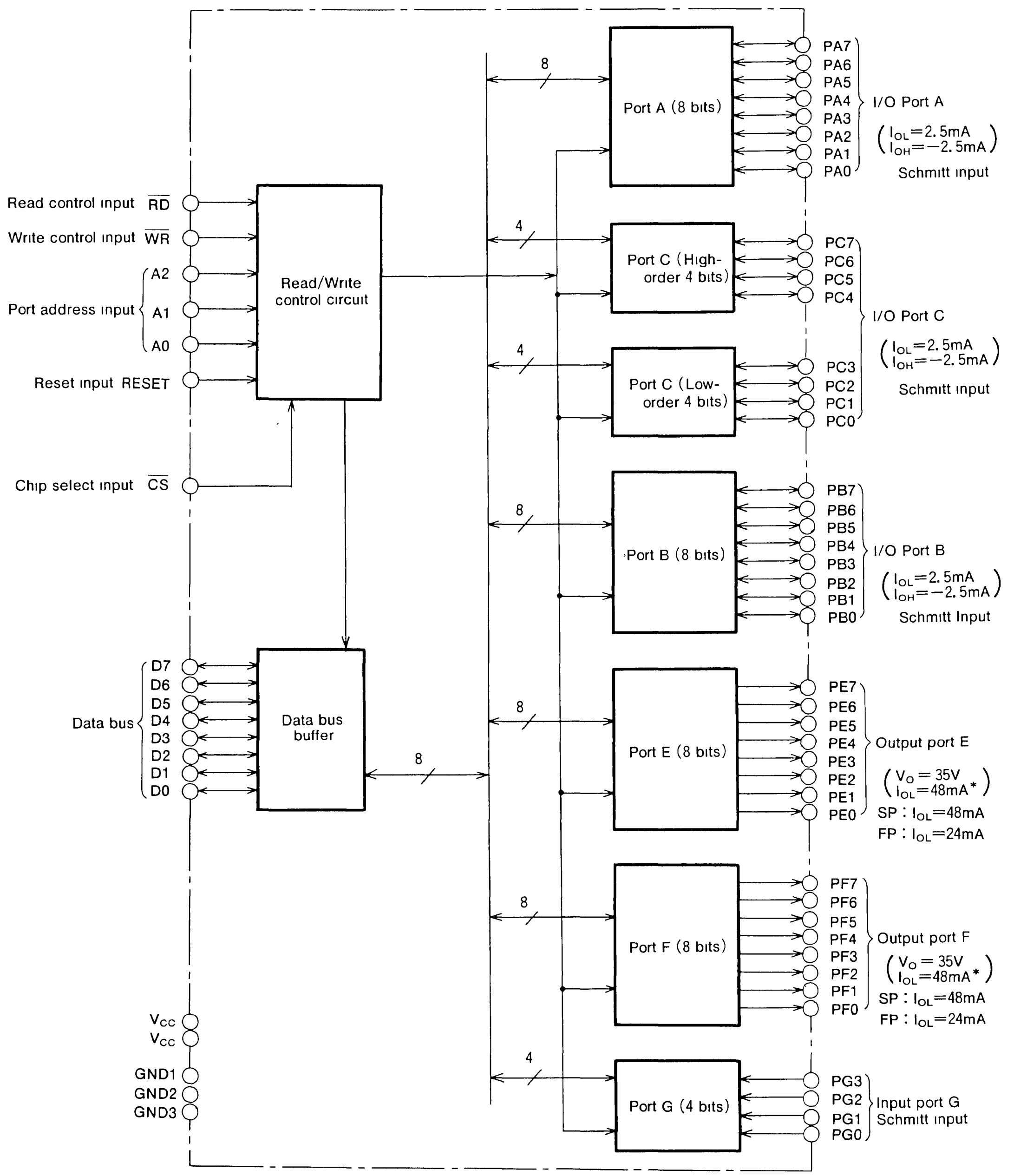


Outline 64P4B



Outline 64P6W

BLOCK DIAGRAM



* : The I_{OL} of the M66500FP is 24mA

GND1 (SP 9-pin, FP 34-pin) : For data bus, port C, port G and internal logic unit
GND2 (SP 33-pin, FP 58-pin) : For output unit of port F
GND3 (SP 51-pin, FP 12-pin) : For I/O buffer of port A and port B, and port E output

FUNCTION (Reference Bloon Diagram)

RD (read) Input
If the input is low-level, the port input data or port latch contents appear at the data bus.

WR (write) Input
The data on the data bus is written to the control register or to the port latch on the leading edge transition from low-level to high-level.

A0, A1, A2 (Port Selection) Input
The low-order three bits of the address bus are used for selection of each port and control register. See Table 1 for the basic functions.

RESET Input
Clears the control register with high level input. In this case, I/O ports A, B and C enter the input mode (high-impedance state) and output-only ports E and F enter the disable state (high-level output status). The data in the port latch is maintained.

CS (Chip Select) Input
Communication with CPU becomes possible with low-level input. If the input is high-level, the data bus maintains the high-impedance state and control from MPU is ignored.
The status of each port and the content of the port latch are not affected.

Read/Write Control Circuit
Control signals from the MPU sets the status of each port and enables data transfer between the data bus and ports.

Data bus buffer
8-bit bi-directional bus buffer to transfer data of a data bus.

Port A and Port B
Ports A and B are 8-bit I/O ports with an input buffer and an output latch buffer and are set to input or output ports by the control command from the MPU. The output circuit consists of a CMOS 3-state totem pole circuit. The output sink current I_{OL} is 2.5mA, the output source current I_{OH} is −2.5mA and transistor array drive is possible. The device has CMOS-level Schmitt trigger inputs.
If the port is set for output, the data on the data bus is written to the port latch on WR rise and the data is output to the port. If the port is set for output and RD is low-level, the port output data appears on the data bus.
If the port is set for input and RD is low-level, the data input to the port appears on the data bus. If the port is set for input and WR is low-level, the data in the data bus is written to the port latch on WR rise. Therefore port output data is available after the port is set for output.
The content of port latch is not fixed at power on.

Port C
Port C can be divided into a pair of 4-bit I/O ports in addition to the functions provided by ports A and B. If the port is set for output, each bit can be set/reset individually.

Port E and Port F
Port E and F are 8-bit output-only ports with output withstand voltage $V_0 = 35V$, output sink current I_{OL} is 48mA *. The output circuit is an open-collector using bipolar transistors.
If the port is selected, the data in the data bus is written to the port latch at WR rise and if the port is set to enable status, the latch data is output at the port. If the port is set to disable status, the port output is high-level, irrespective of latch data.
If RD = low-level, the content of port latch appears at the data bus.
* : The I_{OL} of the M66500FP is 24mA.

Port G
Port G is a 4-bit input-only port with a Schmitt triger circuit. If RD is low-level, the data of the port appears in the low-order 4 bits of the data bus.

NOTE : Data from the data bus is available only to the selected port including the control register, or both the port output data and port status will not change unless the port is selected and WR rises.

Table 1 Basic functions.

A2	A1	A0	CS	RD	WR	Function		
0	0	0	0	0	1	Data bus	←	Port A
0	0	1	0	0	1	Data bus	←	Port B
0	1	0	0	0	1	Data bus	←	Port C
0	1	1	0	0	1	Data bus	←	Port G
1	0	0	0	0	1	Data bus	←	Port E latch data
1	0	1	0	0	1	Data bus	←	Port F latch data
0	0	0	0	1	↑	Port A	←	Data bus
0	0	1	0	1	↑	Port B	←	Data bus
0	1	0	0	1	↑	Port C	←	Data bus
1	0	0	0	1	↑	Port E	←	Data bus
1	0	1	0	1	↑	Port F	←	Data bus
1	1	1	0	1	↑	Control register	←	Data bus
X	X	X	1	X	X	Data bus is in the high-impedance state.		

0 indicates low-level and 1 indicates high-level

Control Word

When (A0, A1, A2, $\overline{WR}$, D7) = (1, 1, 1, ↑, 1), the data in the data bus is regarded as the control word and the port status is set, or when (1, 1, 1, ↑, 0), a Port C bit is set/reset. See Figure 1 and 2.

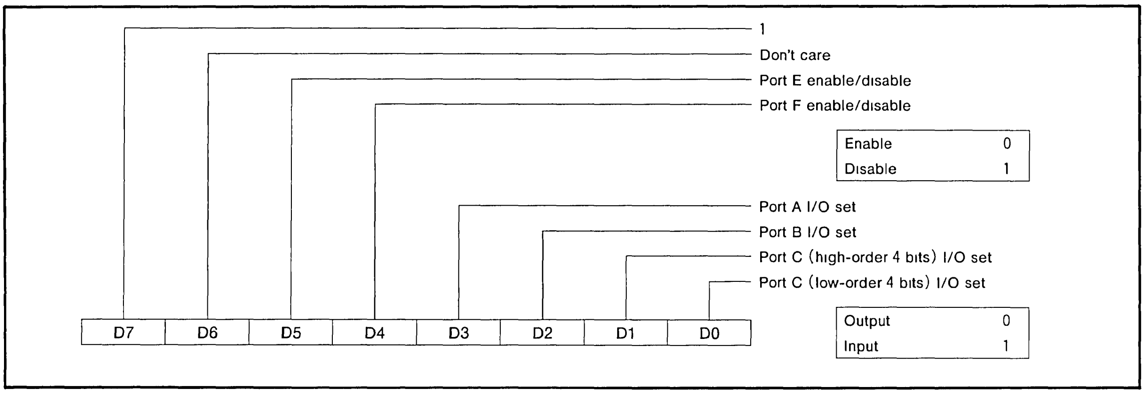
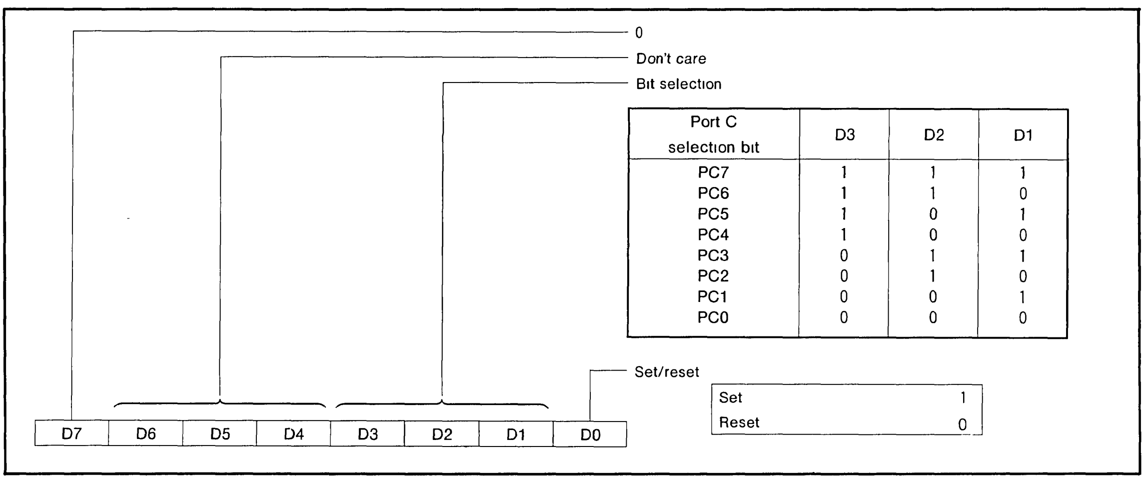


Fig. 1 Port status set control word



Port C selection bit	D3	D2	D1
PC7	1	1	1
PC6	1	1	0
PC5	1	0	1
PC4	1	0	0
PC3	0	1	1
PC2	0	1	0
PC1	0	0	1
PC0	0	0	0

Fig. 2 Port C bit set/reset control word

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.3~+7	V
V_I	Input voltage			−0.3~V_{CC}+0.3	V
V_O	Output voltage			−0.3~V_{CC}+0.3	V
P_d	Power dissipation	M66500SP	T_a=25℃ when a single IC is used (Note 1)	1.9	W
		M66500FP	T_a=25℃ when a single IC is used (Note 2)	1.4	
Tstg	Storage temperature			−65~+150	℃

Note 1 : T_a≧25℃ is derated at 15.4mW/℃
2 : T_a≧25℃ is derated at 11mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage			4.5	5	5.5	V
V_O	High-level output voltage	Ports E, F	I_{OH}≦250μA	0		35	V
I_{OL}	Low-level output current		V_{OL}≦0.6V (M66500SP)	0		48	mA
			V_{OL}≦0.5V (M66500FP)	0		24	
Topr	Operating temperature			−20		+75	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Typ *	Max	Unit
V_{IH}	High-level input voltage	Control pin			2			V
V_{IL}	Low-level input voltage	Data bus (Note 3)					0.8	V
V_{T+}	Upper threshold voltage	Ports A, B, C				2.0	2.8	V
		Port G				2.7	3.5	
V_{T-}	Lower threshold voltage	Ports A, B ,C			0.8	1.3		V
		Port G			1.1	1.9		
V_{OH}	High-level output voltage	Data bus	I_{OH}=−2.5mA		3.0			V
V_{OL}	Low-level output voltage	Ports A, B, C	I_{OL}=2.5mA				0.45	V
V_{OL}	Low-level output voltage	Port E, F	I_{OL}=48mA (M66500SP)				0.6	V
			I_{OL}=24mA (M66500FP)				0.5	
I_{OH}	High-level output current	Port E, F	V_O=35V				250	μA
I_I	Input leakage current		V_I= 0 ~V_{CC}				±10	μA
I_{OZ}	Off-state output current		V_O= 0 ~V_{CC}				±10	μA
I_{CC}	Supply current		All ports high-level output				5	mA
			All ports low-level output	M66500SP		80	110	
				M66500FP		40	60	
C_I	Input pin capacitance		f= 1 MHz				10	pF
$C_{I/O}$	I/O pin capacitance		0 V except measuring pins				20	pF

Note 3 : The control pins are $\overline{RD}$, $\overline{WR}$, RESET, $\overline{CS}$, A2, A1 and A0 pins
* : Typical values are at T_a=25℃, V_{CC}= 5 V

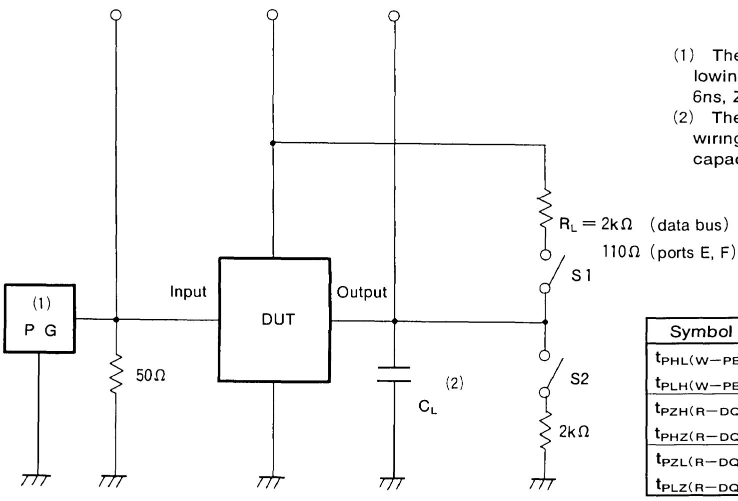
TIMING REQUIREMENTS (T_a=−20~+75℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min	Max	Unit
$t_{w(R)}$	Read pulse width	$t_{su(A-R)}$= 0 ns		160		ns
		$t_{su(A-R)}$≧40ns		120		
$t_{su(PE-R)}$	Peripheral setup time before read			0		ns
$t_{h(R-PE)}$	Peripheral hold time after read			0		ns
$t_{su(A-R)}$	Address setup time before read			0		ns
$t_{h(R-A)}$	Address hold time after read			0		ns
$t_{w(W)}$	Write pulse width			120		ns
$t_{su(DQ-W)}$	Data setup time before write			40		ns
$t_{h(W-DQ)}$	Data hold time after write			0		ns
$t_{su(A-W)}$	Address setup time before write			0		ns
$t_{h(W-A)}$	Address hold time after write			0		ns

SWITCHING CHARACTERISTICS (T_a=−20~+75℃, V_{CC}=5V±10%, unless otherwise noted)

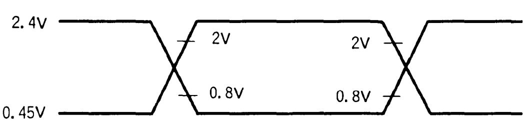
Symbol	Parameter		Test conditions	Limits		Unit
				Min	Max	
$t_{PZH(R-DQ)}$	Propagation time from read to data output	$t_{su(A-R)}$= 0 ns	C_L=150pF (Note 4)		120	ns
$t_{PZL(R-DQ)}$		$t_{su(A-R)}$≧40ns			85	
$t_{PHZ(R-DQ)}$ $t_{PLZ(R-DQ)}$	Propagation time from read to data floating		C_L=150pF(Note 4)	10	85	ns
$t_{PHL(W-PE)}$ $t_{PLH(W-PE)}$	Propagation time from write to output	Ports A, B, C	C_L=150pF(Note 4)		200	ns
		Ports E, F	C_L=150pF, R_L=110Ω(Note 4)		250	

Note 4 : Test Circuit



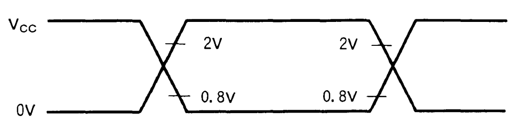
(1) The pulse generator (PG) has the following characteristics t_r=6ns, t_f=6ns, Z_0=50Ω
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

Symbol	Output pin	S 1	S 2
$t_{PHL(W-PE)}$	Ports A,B,C	Open	Open
$t_{PLH(W-PE)}$	Ports E,F	Closed	Open
$t_{PZH(R-DQ)}$ $t_{PHZ(R-DQ)}$	Data bus	Open	Closed
$t_{PZL(R-DQ)}$ $t_{PLZ(R-DQ)}$	Data bus	Closed	Open



Control pin input

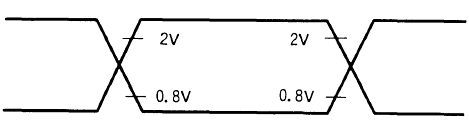
Data bus input



Port input

V_{IH}=2V, V_{IL}=0 8V

Input pulse levels and input reference levels

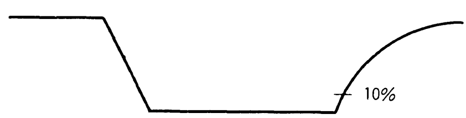


V_{OH}=2V, V_{OL}=0 8V (Data bus, ports A, B, C)

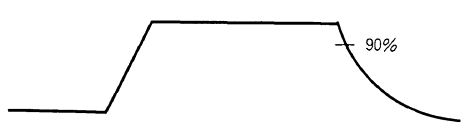
V_{OH}=V_{OL}=1. 5V (Ports E, F)

$t_{PHL(W-PE)}$ $t_{PZH(R-DQ)}$

$t_{PLH(W-PE)}$ $t_{PZL(R-DQ)}$



$t_{PLZ(R-DQ)}$

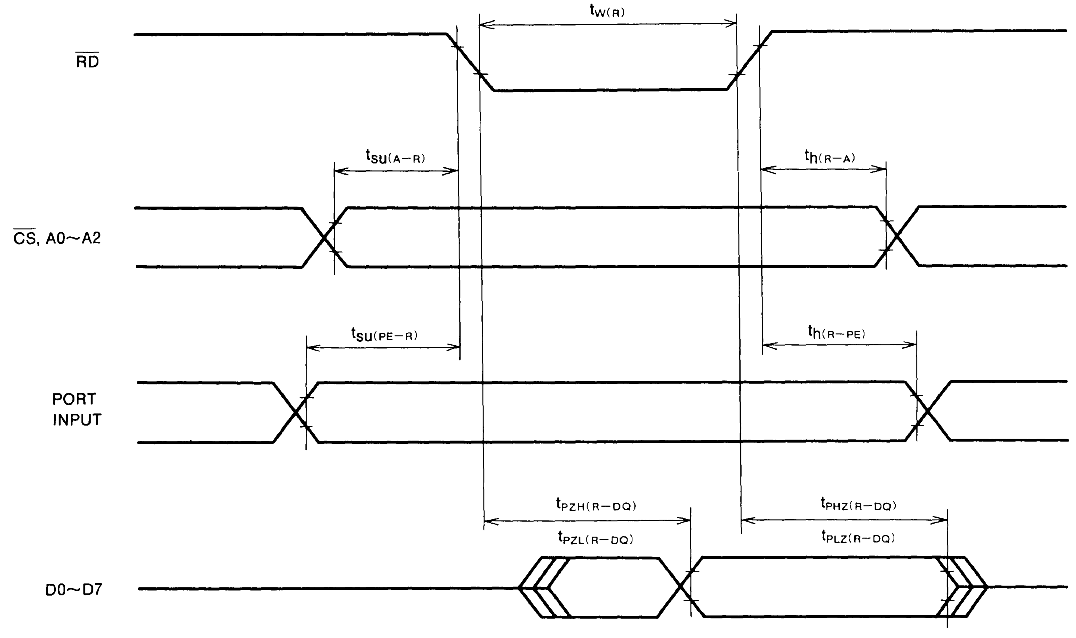


$t_{PHZ(R-DQ)}$

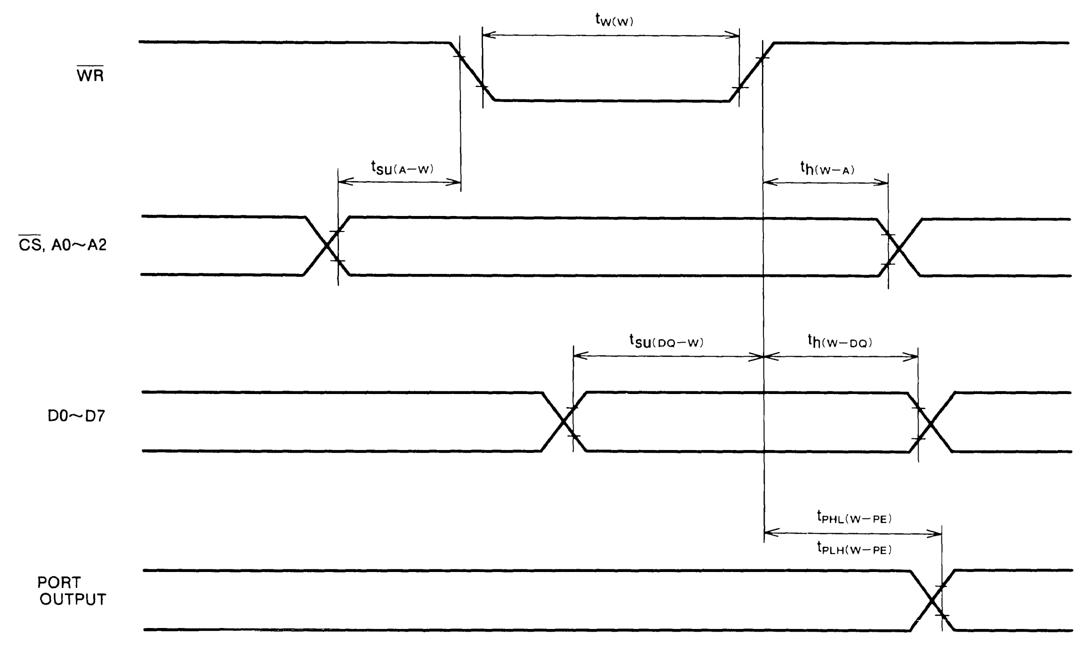
Output reference levels

TIMING DIAGRAM

Read operation timing

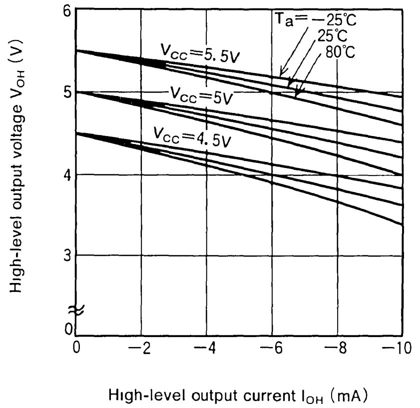


Write operation timing (includes control register write)

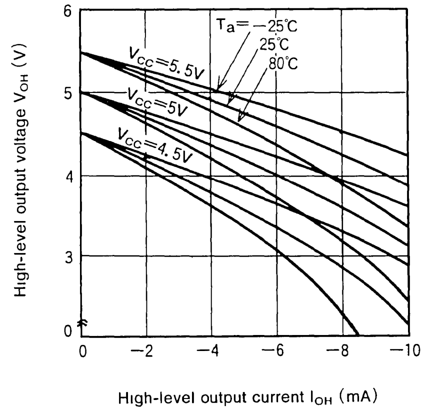


TYPICAL CHARACTERISTICS

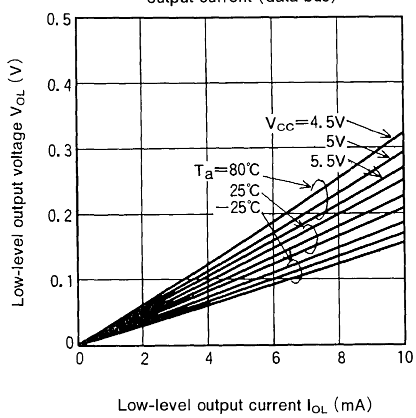
High-level output voltage vs high-level output current (data bus)



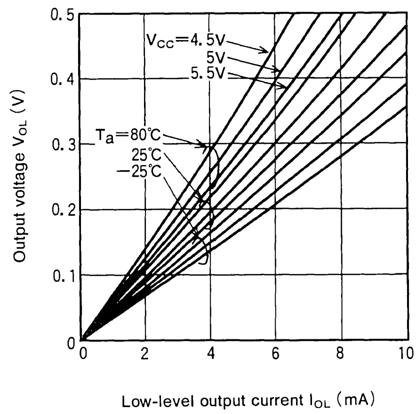
High-level output voltage vs high-level output current (ports A, B, C)



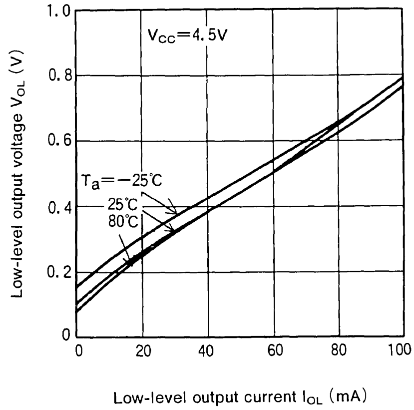
Low-Level output voltage vs low-level output current (data bus)



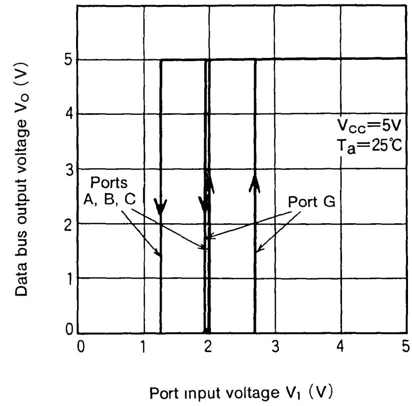
Low-level output voltage vs low-level output current (ports A, B, C)



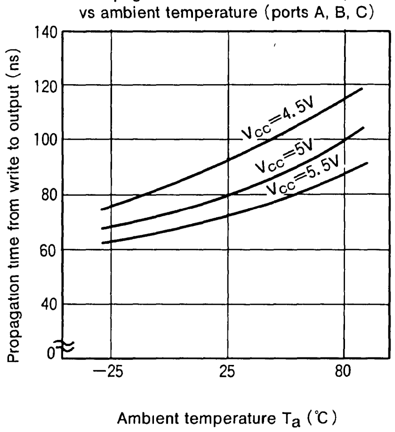
Low-level output voltage vs low-level output current (ports E, F)



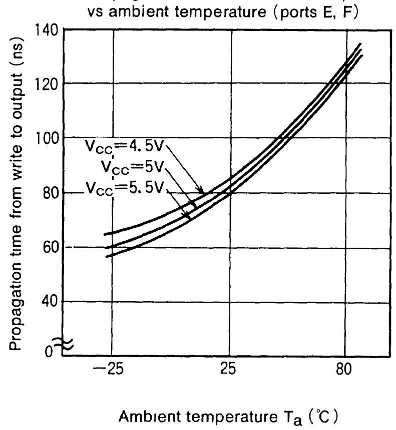
I/O transfer characteristics (port→data bus)



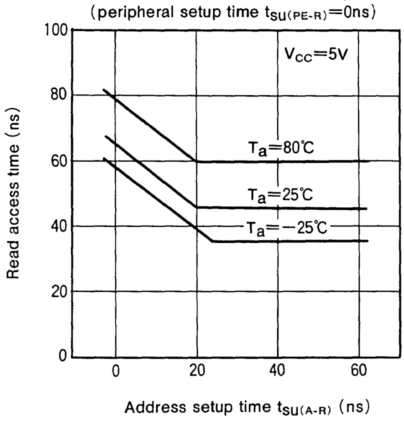
Propagation time from write to output vs ambient temperature (ports A, B, C)



Propagation time from write to output vs ambient temperature (ports E, F)



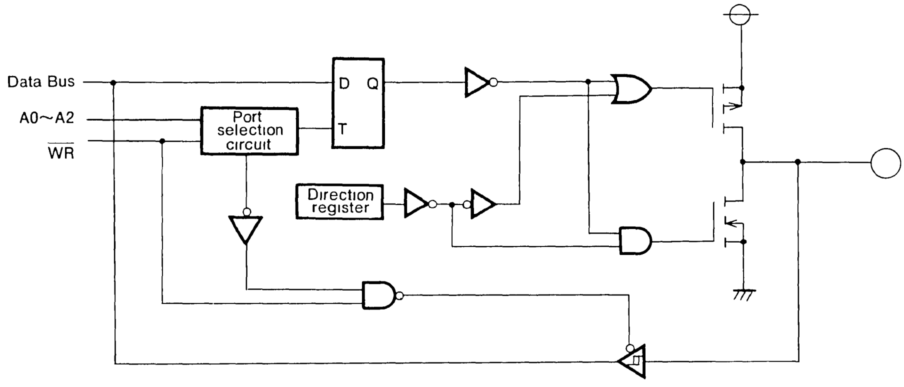
Read access time vs address setup time (peripheral setup time $t_{su(PE-R)}$=0ns)



MITSUBISHI ELECTRIC

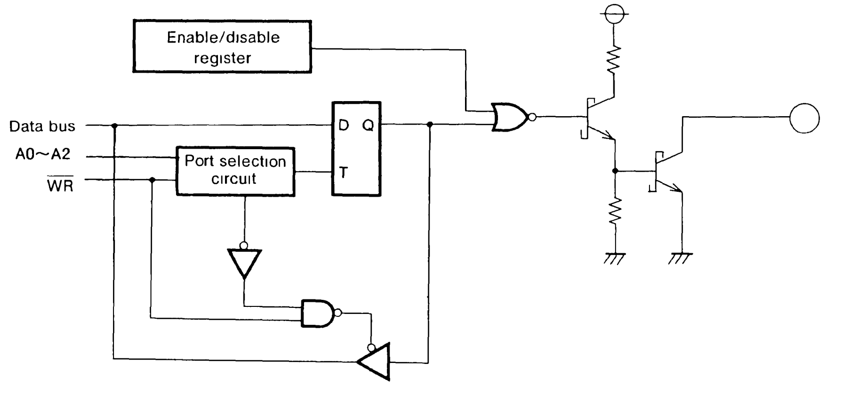
PORT BLOCK DIAGRAM

(Ports A, B, C*)

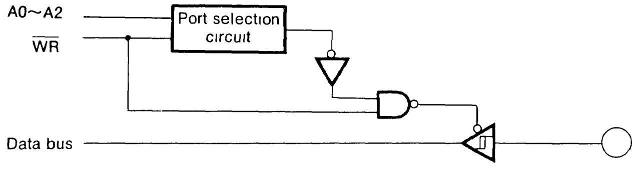


*: The bit set/reset circuit is added to port C

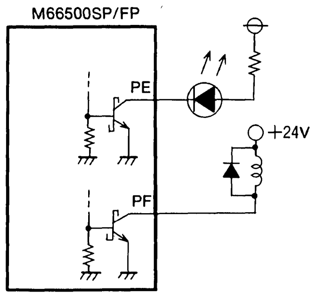
(Ports E, F)



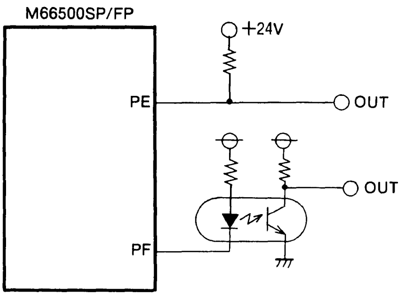
(Port G)



APPLICATION EXAMPLE



1. LED, relay drive



2. Level shift, photo-coupler drive

DATA BUFFER BUILT-IN MEMORY

3

The specifications are subject to change without notice

DESCRIPTION

The M66220SP/FP is an integrated circuit for a mailbox with a built-in 256×8-bit, complete CMOS-type, common memory cell, with two access ports A and B, made with the high-performance silicon-gate CMOS process technolgy.
To be able to read from and write in a common memory independently and asynchronously from both access ports, the M66220SP/FP has independent address, $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ control pins, and I/O pins . The device also has a built-in arbitration function to decide a port in case that address collisions from both ports occur.

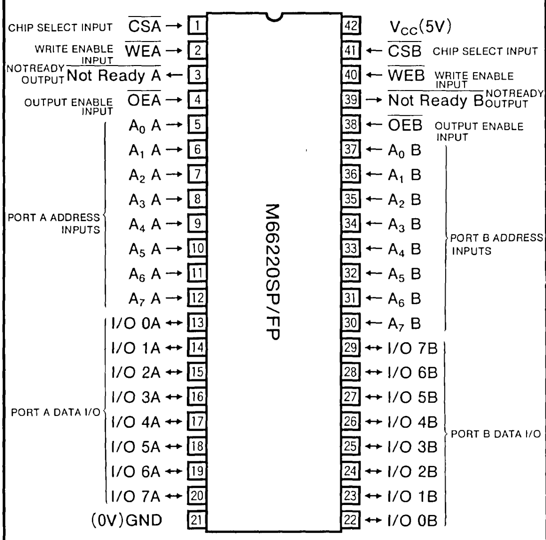
FEATURES

- Memory configuration 256×8-bit
- High-speed access : address access time 40ns(typ)
- Complete asynchronous access from both ports of A and B is posible.
- Completely static operation
- Built-in port arbitration function
- Low power dissipation for CMOS design
- Single 5V power supply
- Not Ready output pin is provided(open drain output)
- Direct connetion of I/O to TTL is possible
- 3-state output for I/O pins

APPLICATION

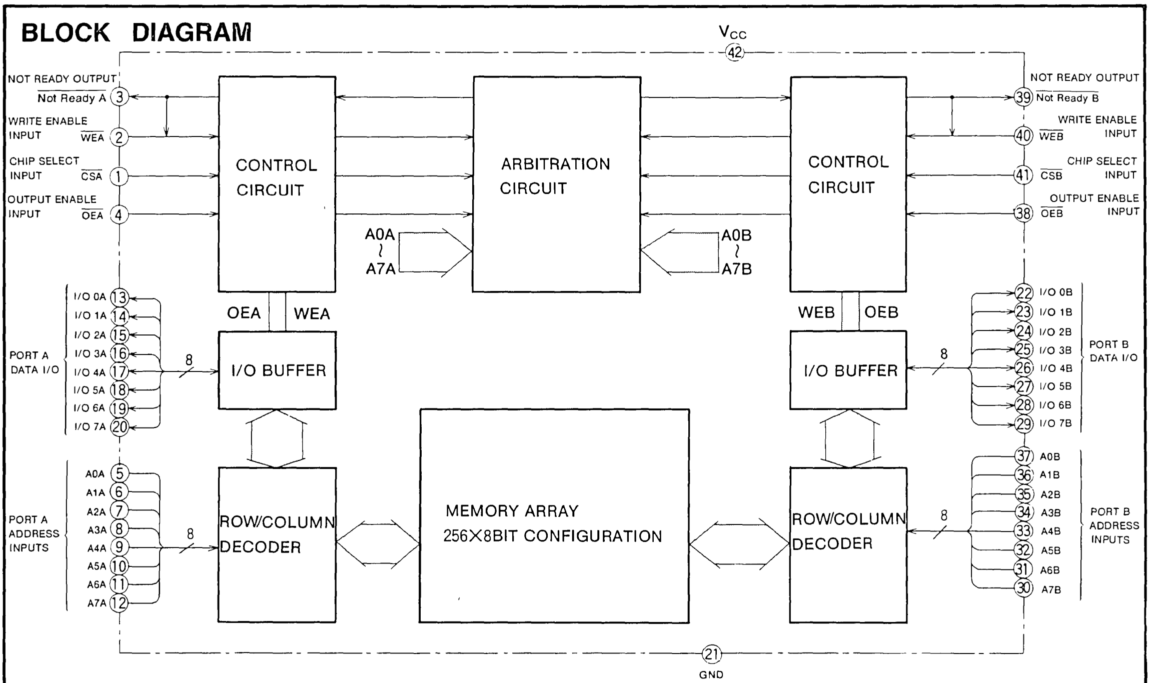
Data transfer memory between MPUs, buffer memory for image processing system.

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B
42P2R

BLOCK DIAGRAM



FUNCTION

The M66220 is a mailbox suitable for data transfer between MPUs using a multi-port method. The 256×8-bit common memory cell with two sets of address lines and data lines enables to read/write independently and asynchronously from both access ports A and B. Therefore the common memory can be accessed as simple RAM from one side of MPU. Because access to common memory is possible irrespective of access by other MPUs, the performance of multi-port processor systems is considerably improved.
If collision on the same memory address occurs from both ports A and B, the built-in arbitration function determines the first-come port and gives priority of access.
The M66220 outputs the low-level $\overline{\text{Not Ready}}$ signal for the late-come port and makes access from the MPU invalid.

If the address $A_0 \sim A_7$ is specified and the $\overline{CS}$ signal is set to low-level, the I/O pins are in the input mode, and if the $\overline{WE}$ signal is set to low-level, the data of the I/O pins is written. If the $\overline{WE}$ signal is set to high-level and the $\overline{CS}$ and the $\overline{OE}$ signals are set to low-level, the I/O pins are in output mode, and if the address $A_0 \sim A_7$ is specified, data of spcified address are output to the I/O pins. If $\overline{CS}$ is set to high-level, the M66220 is in no-selection state, being unable to write or read. and The output is in floating state (high-impedance state), enabling OR ties with other chips. If the $\overline{OE}$ signal is set to high-level, the output is set to the floating state. If the I/O bus method is used, collision of input data and output data on the bus is avoided by setting $\overline{OE}$ to high-level during write operation. If the $\overline{CS}$ is set to high-level, the device is set to the standby state and the supply current is lowered. (See Tables 1 and 2.)

FUNCTION TABLE 1 (A0A~A7A≠ A0B~A7B)

Port A inputs			Port B inputs			Flag		Function
$\overline{CSA}$	$\overline{WEA}$	$\overline{OEA}$	$\overline{CSB}$	$\overline{WEB}$	$\overline{OEB}$	$\overline{\text{Not Ready A}}$	$\overline{\text{Not Ready B}}$	
H	X	X	X	X	X	H	H	Port A is set to no-selection mode
X	X	X	H	X	X	H	H	Port B is set to no-selection mode.
L	L	X	X	X	X	H	H	Port A is set to write mode for memory
L	H	L	X	X	X	H	H	Port A is set to read mode for memory
X	X	X	L	L	X	H	H	Port B is set to write mode for memory.
X	X	X	L	H	L	H	H	Port B is set to read mode for memory

X=Irrelevant "H" = High level "L" = Low level

FUNCTION TABLE 2 BASIC FUNCTION OF EACH PORT

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	I_{CC}
H	X	X	No-selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Operation
L	H	L	Read	D_{OUT}	Operation
L	H	H		High-impedance	Operation

FUNCTIONAL DESCRIPTION

Arbitration Function

The M66220 allows asynchronous access to the common memory from two independent ports, improving the total efficiency of the processor system by using the multi-port method. However, independent and asynchronous access from the two ports may cause collision on the same address of the common memory, selected by both ports. If the same address is selected from both ports, four basic operations may take place according to the access mode setting.

(1) Port A—Read Port B—Read
(2) Port A—Read Port B—Write
(3) Port A—Write Port B—Read
(4) Port A—Write Port B—Write

In case (1) in which both ports are in the read mode, data is read correctly for both ports and the memory content would not be destroyed. But, in case (2) or (3), in which one port is in write mode and the other in the read mode, the write would be performed correctly, but the data of the opposite port read operation may change in the same cycle. In case (4), in which both ports write, both ports write opposing data, making the memory content unstable, and therefore, the operation cannot be secured.

To solve these problems, the M66220 has a built-in arbitration function to arbitrate the address collision from both ports. The arbitration function determines which port was confirmed first and gives priority to the first-come port without condition. (The $\overline{\text{Not Ready}}$ signal is kept high-level.) While the same address are selected by both ports, the $\overline{\text{Not Ready}}$ output pin of late-come port is set to low-level irrespetive of read/write operation, and the write operation to late-come port from MPU is prohibited. If the first-come port changes address and the addresses of both ports do not match, the $\overline{\text{Not Ready}}$ output is canceled to high-level and the late-come ports is allowed to access again. If the same address is selected at a time by both ports, the arbitration function allows access of only one port, and set the $\overline{\text{Not Ready}}$ output of another port to low-level and make the access from the MPU invalid. Table 3 shows the port arbitration function and port access.

- Collision No. 1 (address control)

Table 3 shows the port access status and the $\overline{\text{Not Ready}}$ output condition when the same address in the common memory is selected by both port A and B.

TABLE 3

$\overline{CSA}=\overline{CSB}=$"L"

Address setting when the same address is selected	Port A			Port B		
	Mode setting	Access	$\overline{\text{Not Ready A}}$	Mode setting	Access	$\overline{\text{Not Ready B}}$
Port A comes first	Read	○	H	Read	○	L
Port B comes first	Read	○	L	Read	○	H
Port A comes first	Read	○	H	Write	×	L
Port B comes first	Read	○	L	Write	○	H
Port A comes first	Write	○	H	Read	○	L
Port B comes first	Write	×	L	Read	○	H
Port A comes first	Write	○	H	Write	×	L
Port B comes first	Write	×	L	Write	○	H
Port A and B at the same time	Arbitration Resolved			Arbitration Resolved		

"H"=High-level, "L"=Low-level

- Collision No. 2 ($\overline{CS}$ control)

If the $\overline{CS}$ input settings of both ports results in a situation where A0A～A7A=A0B～A7B, the port access status and the $\overline{\text{Not Readv}}$ output status are the same as the address input setting in collision No. 1.

ABSOLUTE MAXIMUM RATINGS (T_a=0～70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3～+7.0	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	T_a=25℃	T. B. D	W
Tstg	Storage temperature range		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
V_I	Input voltage	0		V_{CC}	V
Topr	Operating temperature range	0		70	℃

ELECTRICAL CHARACTERISTICS (T_a=0～70℃, V_{CC}=5V±10%, unless otherwise noted)

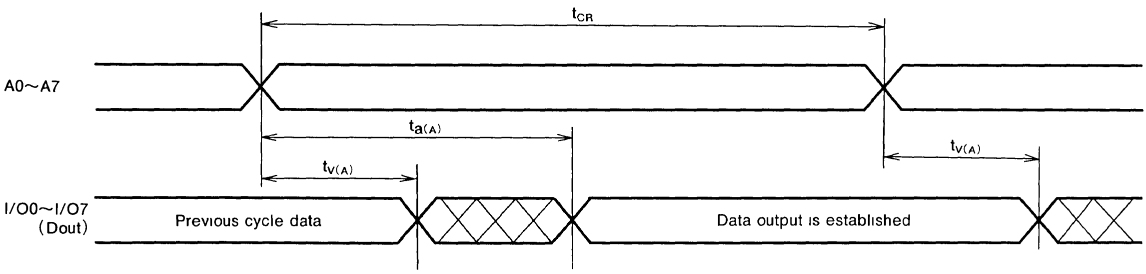
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.8	V
V_{OH}	High-level output voltage(I/O)		I_{OH}=−2mA	2.4			V
V_{OL}	Low-level output voltage(I/O)		I_{OL}=4mA			0.5	V
V_{OL}	Open drain low-level output voltage($\overline{\text{Not Ready}}$)		I_{OL}=8mA			0.5	V
I_I	Input leakage current		V_I=0～V_{CC}			±10	μA
I_O	Output leakage current		$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=0～V_{CC}			±10	μA
I_{CC}	Average operating supply current (Both ports active)		$\overline{CS}=V_{IL}$ Output pin open		T. B. D		mA
I_{SB1}	Standby current	Both ports standby	$\overline{CS_A}$, $\overline{CS_B}=V_{IH}$		T. B. D		mA
I_{SB2}	Standby current	One port standby	$\overline{CS_A}$ or $\overline{CS_B}=V_{IH}$ I_{OUT}=0mA (Active port output pin open)		T. B. D		mA
I_{SB3}	Standby current	Both ports full standby	$\overline{CS_A}$, $\overline{CS_B}\geqq V_{CC}-0.2V$ Other input $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$		T. B. D		mA
I_{SB4}	Standby current	One port full standby	$\overline{CS_A}$ or $\overline{CS_B}\geqq V_{CC}-0.2V$ Other input $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$ I_{OUT}=0mA (Active port output pin open)		T. B. D		mA

Note 1 The current flowing into the IC is positive.
2 Typical values are at V_{CC}=5V, T_a=25℃.

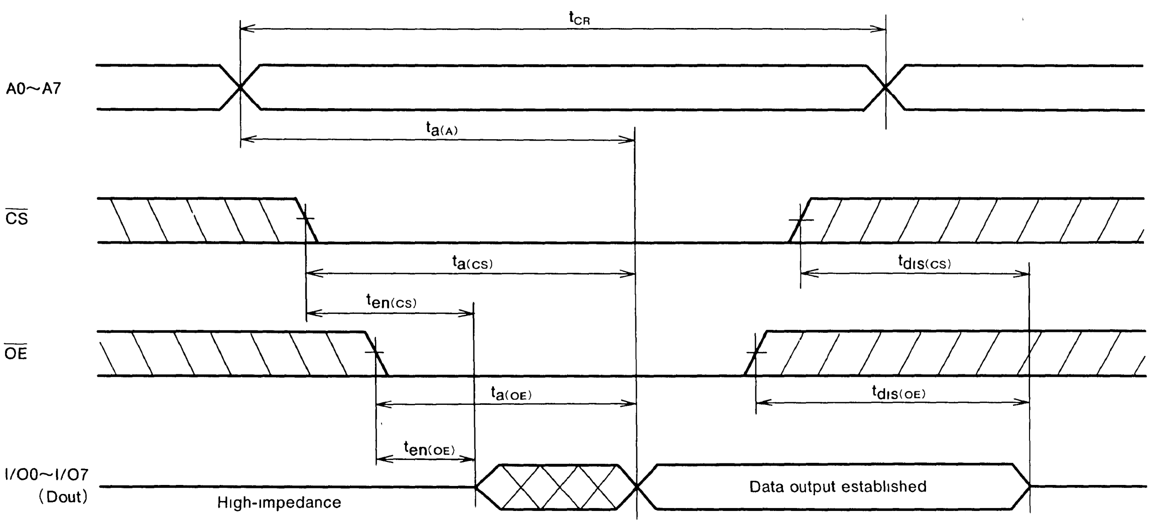
TIMING DIAGRAM

Read Cycle ($\overline{WE}=V_{IH}$)

● Read Cycle No. 1 (Address Control) ($\overline{CS}=\overline{OE}=V_{IL}$)

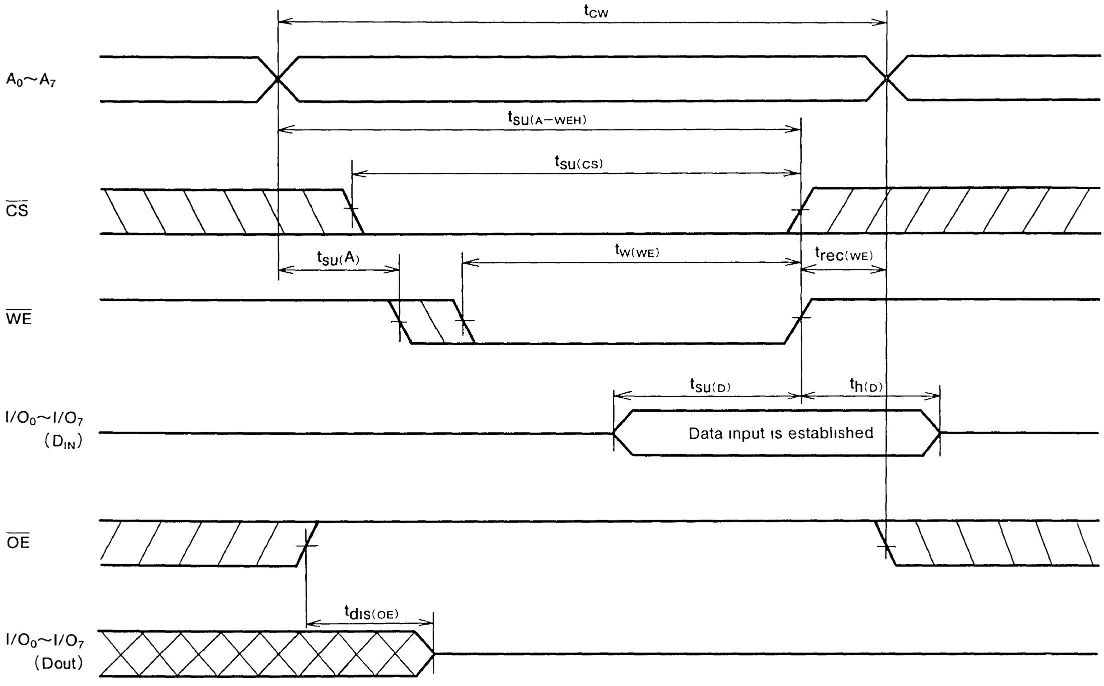


● Read Cycle No. 2 ($\overline{CS}$ Control)

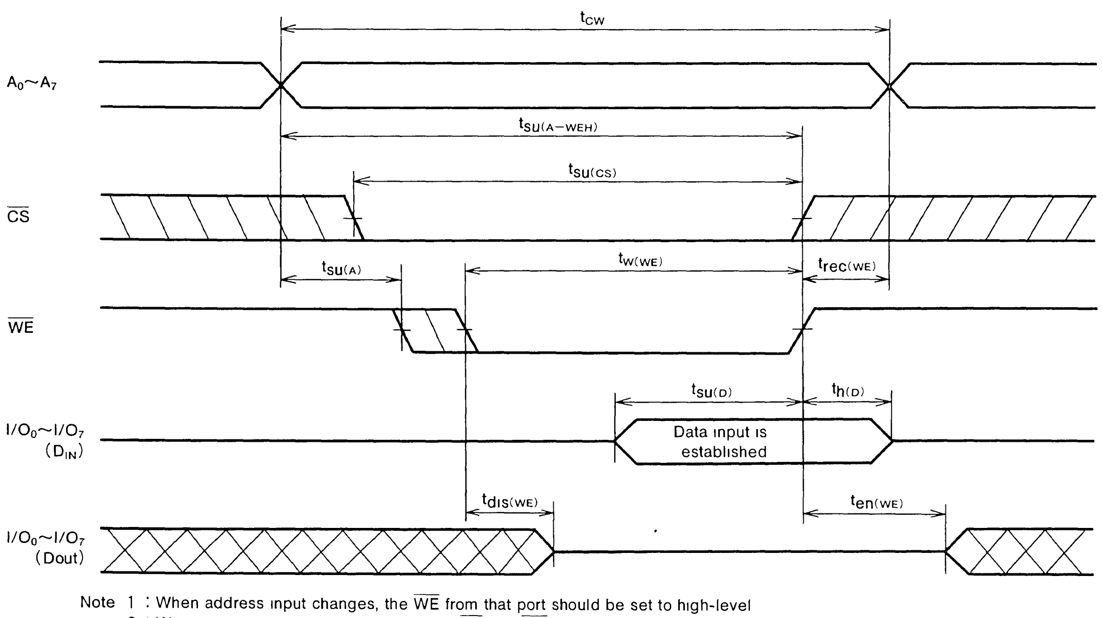


Write Cycle

● Write Cycle No. 1 ($\overline{WE}$ Control) See Note 1, 2 and 3



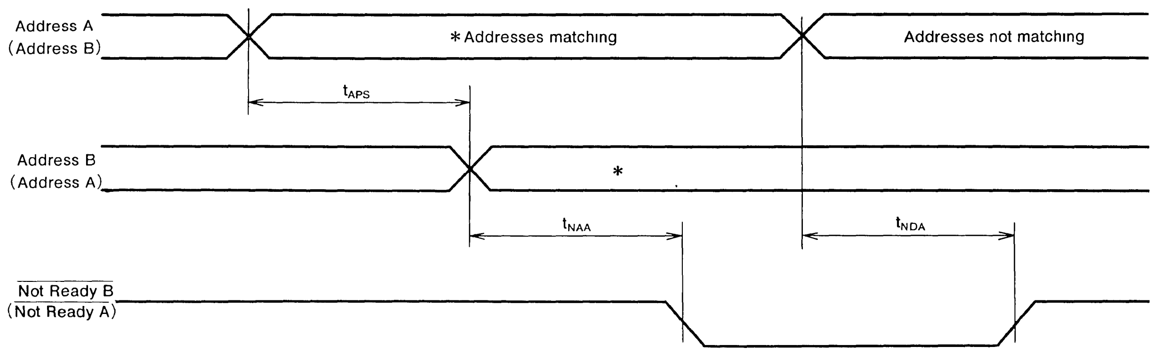
● Write Cycle No. 2 ($\overline{WE}$ Control) See Note 1, 2, 3 and 4



Note 1 : When address input changes, the $\overline{WE}$ from that port should be set to high-level
2 : Write operation is performed while both $\overline{CS}$ and $\overline{WE}$ are low-level
3 : Do not apply reverse-phase signal when I/O pin is in the output state
4 : Output is kept in the high-impedance state if the trailing edge of $\overline{WE}$ happens before or at the same time of the trailing edge of $\overline{CS}$, or if the leading edge of $\overline{WE}$ happens at the same time or after the leading edge of $\overline{CS}$
5 : Shaded area=don't care

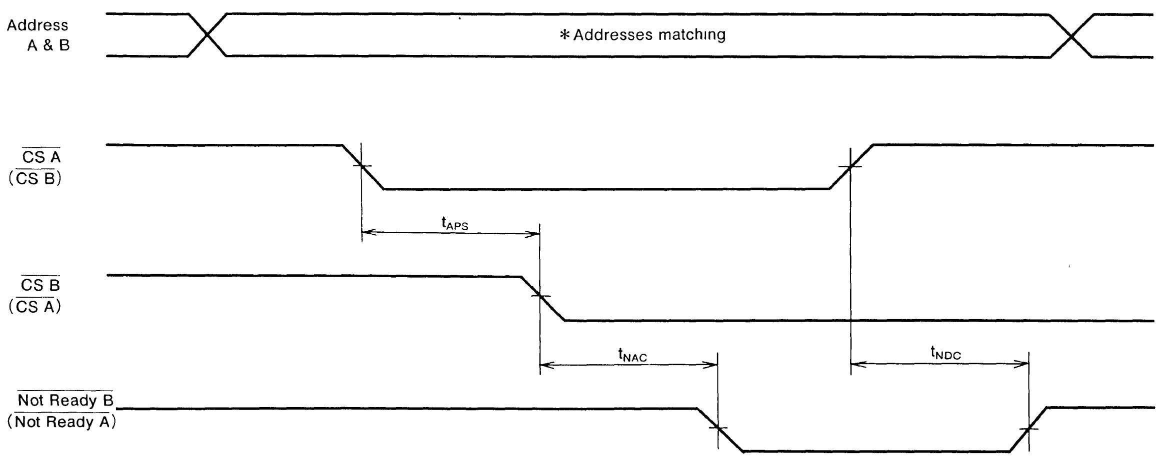
Collision Cycle

● Collision Cycle No. 1 (Address Control) Note 6, 7



*Address A=Address B

● Collision Cycle No. 2 ($\overline{CS}$ Control) Note 6, 8



*Address A=Address B

Note 6 : The $\overline{\text{Not Ready}}$ output of the first-come port is kept at high-level
7 : The $\overline{CS}$ is set low-level before the address input is established
8 : The address input is established before the low-level transition of $\overline{CS}$

M66221SP/FP

256×9-BIT MAILBOX

The specifications are subject to change without notice.

DESCRIPTION

The M66221SP/FP is an integrated circuit for a mailbox with a built-in 256×9-bit, complete CMOS-type common memory cell with two access ports A and B, made with a high-performance silicon-gate CMOS process technology.

To be able to read from and write in a common memory independently and asynchronously from both access ports, the M66221SP/FP has independent address, $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ control pins, and I/O pins. The device also has a built-in arbitration function to decide a port in case that address collisions from both ports occur.

FEATURES

- Memory configuration 256×9-bit
- High-speed access : address access time 40ns(typ)
- Complete asynchronous access from both port A and B is posible.
- Complete static operation
- Built-in port arbitration function
- Low power dissipation for CMOS design
- Single 5V power supply
- $\overline{\text{Not Ready}}$ output pin provided(open drain output)
- Direct connection of I/O to TTL is possible
- 3-state output for I/O pins

APPLICATION

Data transfer memory between MPUs, buffer memory for image processing system.

FUNCTION

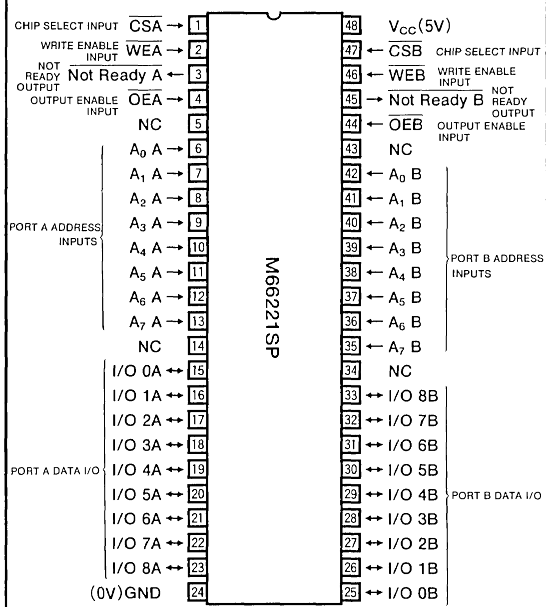
The M66221 is a mailbox suitable for data transfer between MPUs, using a multi-port method. The 256×9-bit common memory cell with two sets of address lines and data lines enables to read/write independently and asynchronously from both access ports A and B. Therefore the common memory can be accessed as simple RAM from one side of MPU. Because access to common memory is possible irrespective of access by other MPUs, the performance of multi-port processor systems is considerably improved.

If the same address in memory is selected from both ports A and B(collision), the built-in arbitration function decides the first-come port and gives priority of access.

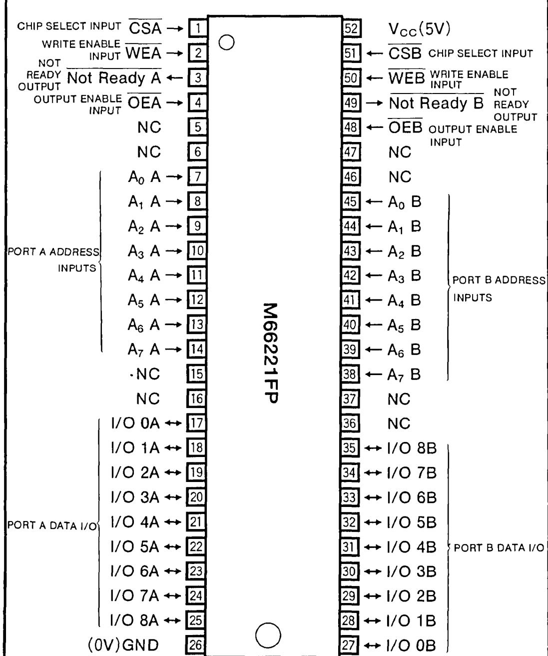
The device outputs the low-level $\overline{\text{Not Ready}}$ signal for the late-come port and makes access from the MPU invalid.

If the address $A_0 \sim A_7$ is specified and the $\overline{CS}$ signal is set to low-level, the I/O pins are in the input mode, and if the $\overline{WE}$ signal is set to low-level, the data of the I/O pins is written. If the $\overline{WE}$ signal is set to high-level and the $\overline{CS}$ and the $\overline{OE}$ signals are set to low-level, the I/O pins are in output mode, and if the address $A_0 \sim A_7$ is specified, datas of specified address are output to the I/O pins. If $\overline{CS}$ is set to high-level, the M66221 is in no-selection states, being unable to write or read. The output is in a floating state(high-impedance state), enabling OR ties with other chips.

PIN CONFIGURATION (TOP VIEW)

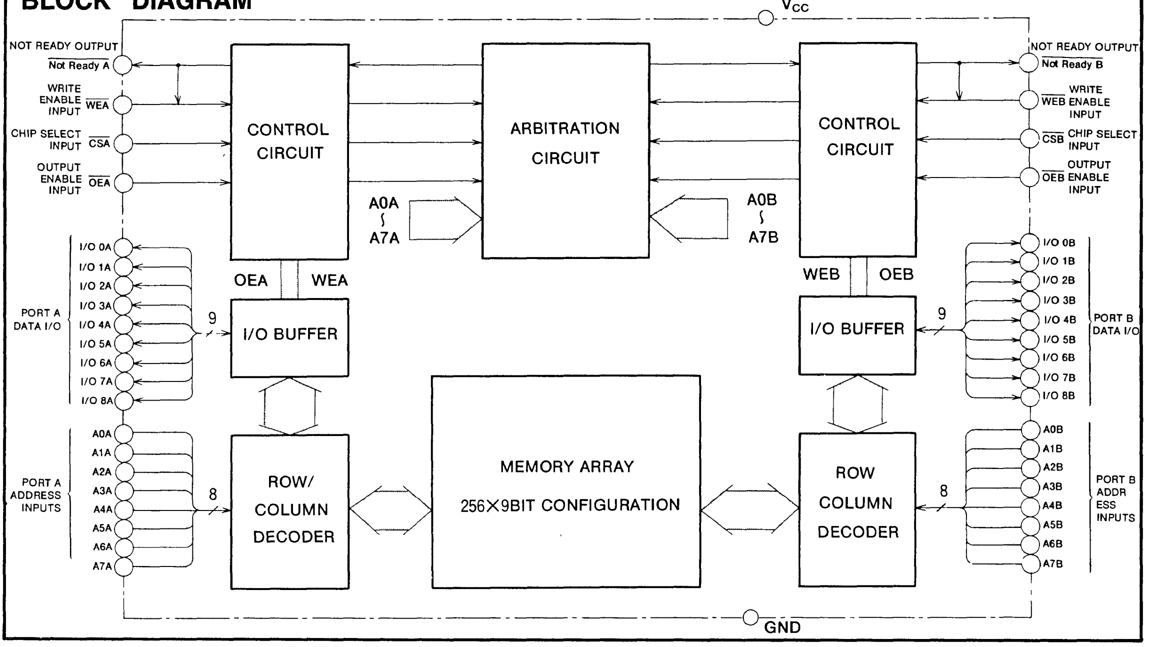


Outline 48P4B



Outline 52P2G NC : No connection

BLOCK DIAGRAM



If the $\overline{OE}$ signal is set to high-level, the output is set to the floating state. If the I/O bus method is used, collision of input data and output data on the bus is avoided by setting $\overline{OE}$ to high-level during the write operation. If the $\overline{CS}$ is set to high-level, the device is set to the standby state and the supply current is lowered. (See Tables 1 and 2)

FUNCTION TABLE 1 (A0A~A7A≠A0B~A7B)

Port A inputs			Port B inputs			Flag		Function
$\overline{CSA}$	$\overline{WEA}$	$\overline{OEA}$	$\overline{CSB}$	$\overline{WEB}$	$\overline{OEB}$	$\overline{Not\ Ready\ A}$	$\overline{Not\ Ready\ B}$	
H	X	X	X	X	X	H	H	Port A is set to no-selection mode
X	X	X	H	X	X	H	H	Port B is set to no-selection mode
L	L	X	X	X	X	H	H	Port A is set to write mode for memory
L	H	L	X	X	X	H	H	Port A is set to read mode for memory
X	X	X	L	L	X	H	H	Port B is set to write mode for memory.
X	X	X	L	H	L	H	H	Port B is set to read mode for memory

X =Irrelevant, "H" =High-level, "L" =Low-level

FUNCTION TABLE 2 BASIC FUNCTION OF EACH PORT

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	I_{CC}
H	X	X	No-selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Operation
L	H	L	Read	D_{OUT}	Operation
L	H	H		High-impedance	Operation

MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

Arbitration Function

The M66221 allows asynchronous access to the common memory from two independent ports, improving the total efficiency of the processor system by using the multi-port method. However, independent and asynchronous access from the two ports may cause collision on the same address in the common memory selected by both ports. If the same address is selected from both ports, four basic operations may take place according to the access mode setting.

(1) Port A—Read Port B—Read
(2) Port A—Read Port B—Write
(3) Port A—Write Port B—Read
(4) Port A—Write Port B—Write

In case (1) in which both ports are in the read mode, data is read correctly for both ports and the memory content would not be destroyed. But, in case (2) or (3), in which one port is in write mode and the other in read mode, the write would be performed correctly. But the data of the opposite port in read operation may change in the same cycle.in case (4) in which both ports in write opration, both ports write opposing data, making the memory content unstable, and, therefore, the operation cannot be secured.

To solve these problems, the M66221 has a built-in arbitration function to arbitrate the address collisions of both ports. The arbitration function determines which port was confirmed first and gives priority to the first-come port without condition. (The $\overline{\text{Not Ready}}$ signal is kept high-level.) While the same address are selected by both ports, the $\overline{\text{Not Ready}}$ output pin of late-come port is in set to low-level irrespective of read/write operation, and the write operation to late-come port from MPU is prohibitited.If the first-come port address changes and the addressese of both ports do not match, the $\overline{\text{Not Ready}}$ output is canceled to high-level, and the late-come port is allowed to access again. If the same address is selected at a time by both ports, the arbitration function allows access of only one port, and sets the $\overline{\text{Not Ready}}$ output of another port to low-level and makes the access from the MPU invalid. Table 3 shows the port arbitration function and port access.

● Collision No. 1 (address control)

Table 3 shows the port access status and the $\overline{\text{Not Ready}}$ output conditions when the same address in the common memory is selected by the address input setting from both ports A and B.

● Collision No. 2 ($\overline{CS}$ control)

If the $\overline{CS}$ input setting of both ports results in a situation where A0A～A7A＝A0B～A7B, the port access status and the $\overline{\text{Not Ready}}$ output status are the same as the address input setting collision No. 1.

TABLE 3

$\overline{CSA}=\overline{CSB}=$"L"

Address setting when the same address is selected	Port A			Port B		
	Mode setting	Access	$\overline{\text{Not Ready A}}$	Mode setting	Access	$\overline{\text{Not Ready B}}$
Port A comes first	Read	○	H	Read	○	L
Port B comes first	Read	○	L	Read	○	H
Port A comes first	Read	○	H	Write	×	L
Port B comes first	Read	○	L	Write	○	H
Port A comes first	Write	○	H	Read	○	L
Port B comes first	Write	×	L	Read	○	H
Port A comes first	Write	○	H	Write	×	L
Port B comes first	Write	×	L	Write	○	H
Port A and B at the same time	Arbitration Resolved			Arbitration Resolved		

"H"=High-level "L"=Low-level

ABSOLUTE MAXIMUM RATINGS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3~+7.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	T_a=25℃	T. B. D	W
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
V_I	Input voltage	0		V_{CC}	V
Topr	Operating temperature range	0		70	℃

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±10%, unless otherwise noted)

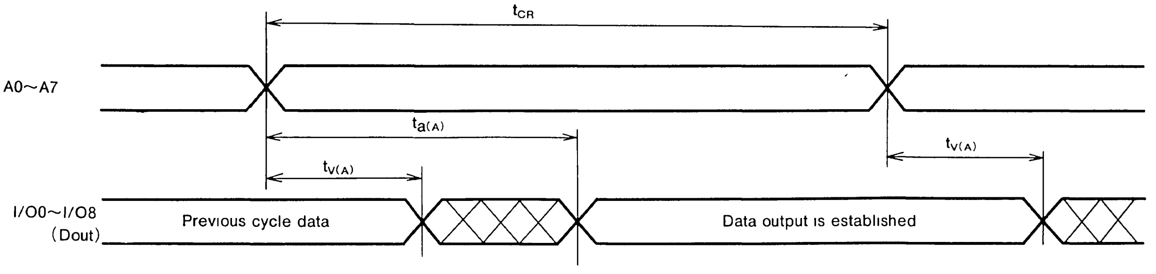
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.8	V
V_{OH}	High-level output voltage(I/O)		I_{OH}=−2mA	2.4			V
V_{OL}	Low-level output voltage(I/O)		I_{OL}=4mA			0.5	V
V_{OL}	Open drain low-level output voltage($\overline{\text{Not Ready}}$)		I_{OL}=8mA			0.5	V
I_I	Input leakage current		V_I=0~V_{CC}			±10	μA
I_O	Output leakage current		$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=0~V_{CC}			±10	μA
I_{CC}	Average operating supply current (Both ports active)		$\overline{CS}$=V_{IL} Output pin open		T. B. D		mA
I_{SB1}	Standby current	Both ports standby	$\overline{CS_A}$, $\overline{CS_B}$=V_{IH}		T. B. D		mA
I_{SB2}	Standby current	One port standby	$\overline{CS_A}$ or $\overline{CS_B}$=V_{IH} I_{OUT}=0mA (Active port output pin open)		T. B. D		mA
I_{SB3}	Standby current	Both ports full standby	$\overline{CS_A}$, $\overline{CS_B}$≧ V_{CC}−0.2V Other input V_{IN}≧ V_{CC}−0.2V or V_{IN}≦0.2V		T. B. D		mA
I_{SB4}	Standby current	One port full standby	$\overline{CS_A}$ or $\overline{CS_B}$≧ V_{CC}−0.2V Other input V_{IN}≧ V_{CC}−0.2V or V_{IN}≦0.2V I_{OUT}=0mA (Active port output pin open)		T. B. D		mA

Note 1 The current flowing into the IC is positive
2 Typical values are at V_{CC}=5V, T_a=25℃.

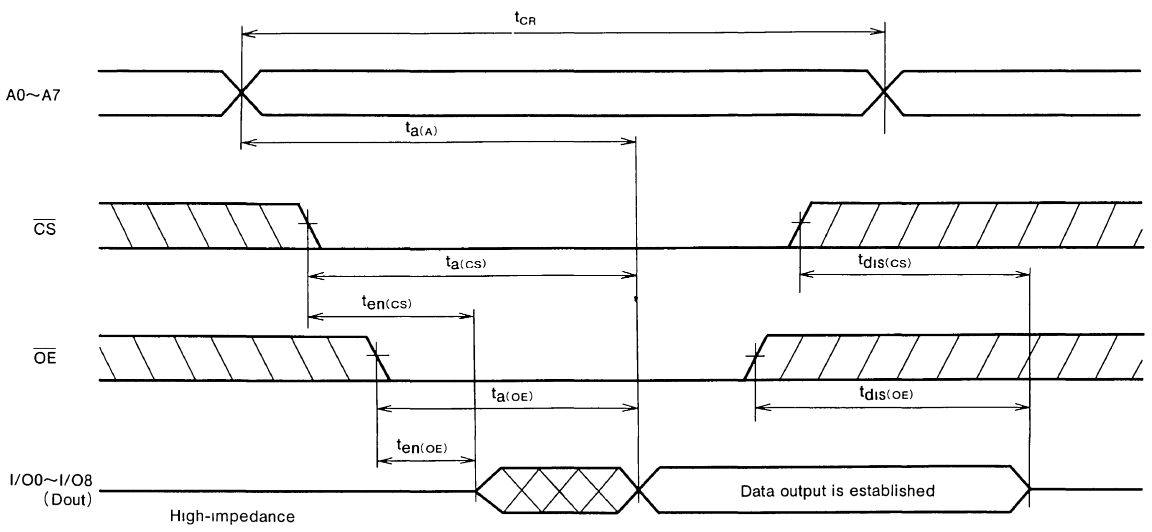
TIMING DIAGRAM

Read Cycle ($\overline{WE}=V_{IH}$)

● Read Cycle No. 1 (Address Control) ($\overline{CS}=\overline{OE}=V_{IL}$)

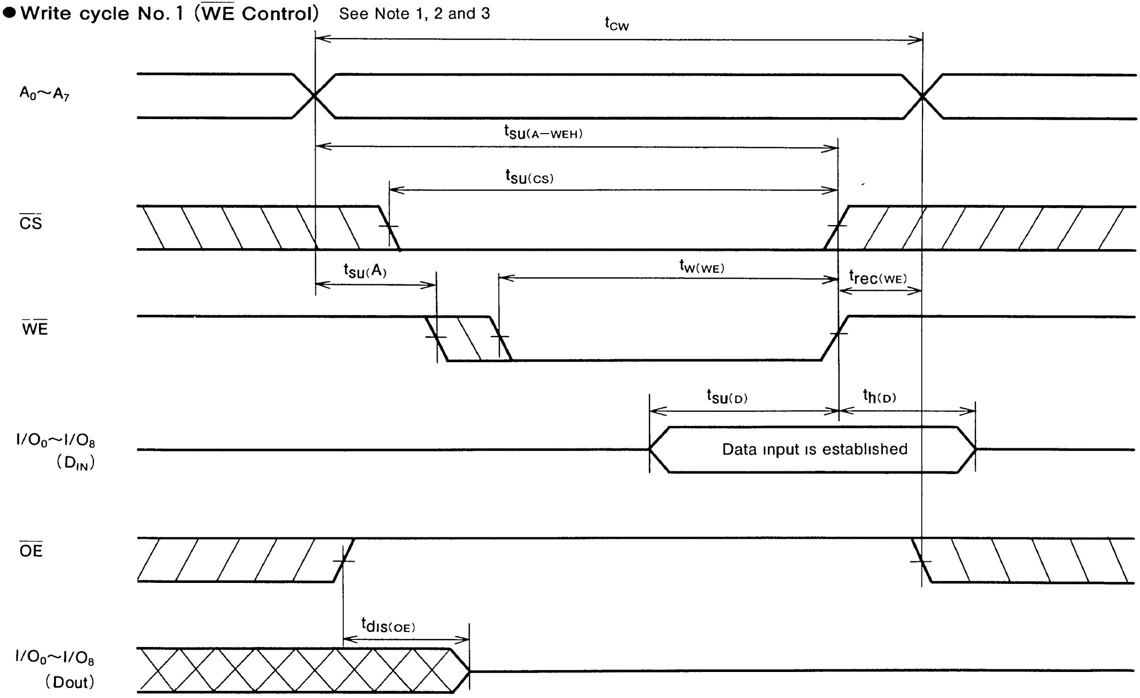


● Read Cycle No. 2 ($\overline{CS}$ Control)

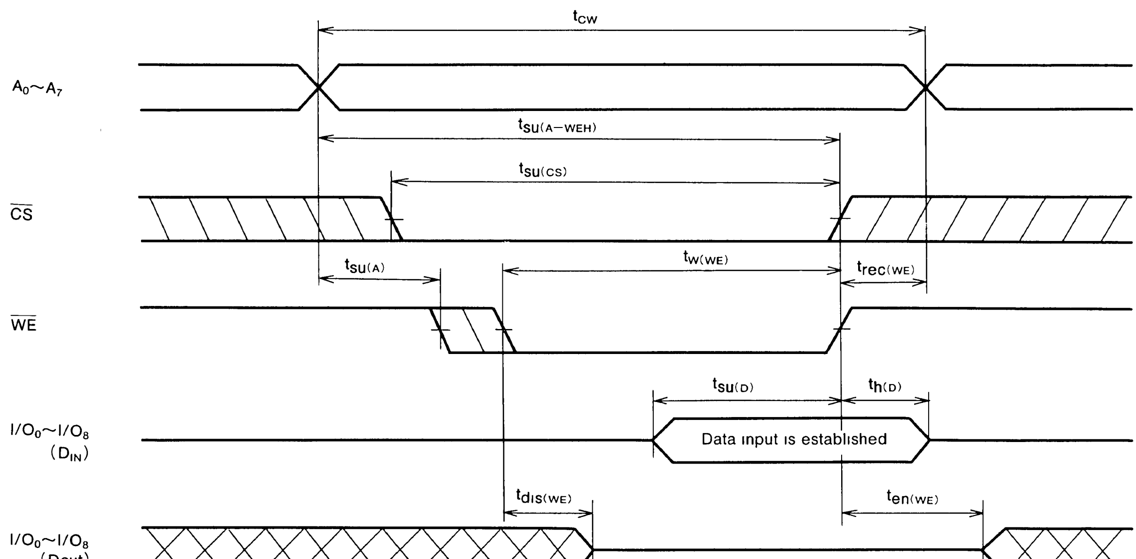


Write Cycle

● Write cycle No. 1 ($\overline{WE}$ Control) See Note 1, 2 and 3



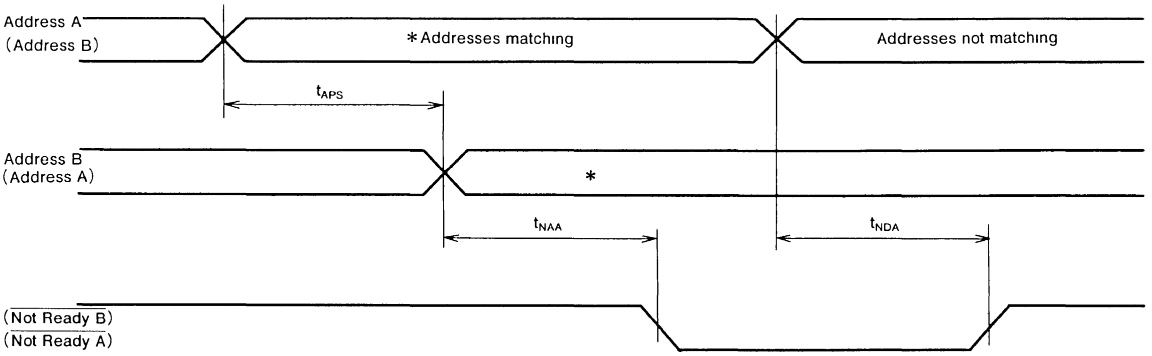
● Write Cycle No. 2 ($\overline{WE}$ Control) See Note 1, 2, 3 and 4



Note 1 : When address input changes, the $\overline{WE}$ from that port should be set to high-level
2 : Write operation is performed while both $\overline{CS}$ and $\overline{WE}$ are low-level
3 : Do not apply reverse-phase signal when I/O pin is in the output state
4 : The output is kept in the high-impedance state if the trailing edge of $\overline{WE}$ happens before or at the same time of the trailing edge of $\overline{CS}$, or if the leading edge of $\overline{WE}$ happens at the same time or after the leading edge of $\overline{CS}$
5 : Shaded area=don't care

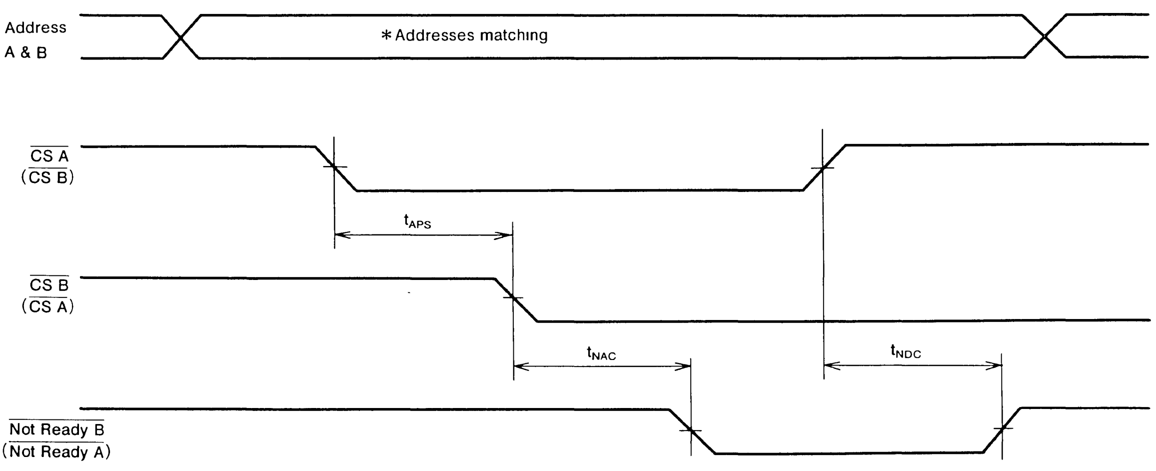
Collision Cycle

● Collision Cycle No. 1 (Address Control) Note 6, 7



*Address A=Address B

● Collision Cycle No. 2 ($\overline{CS}$ Control) Note 6, 8



*Address A=Address B

Note 6 : The $\overline{\text{Not Ready}}$ output of the first-come port is maintained at high-level
7 : The $\overline{CS}$ is set low-level before the address input is established
8 : The address input is established before the low-level transition of $\overline{CS}$

M66222SP/FP

128×8-BIT×2 MAIL BOX

DESCRIPTION

The M66222SP/FP is an integrated circuit for a mailbox with a pair of built-in 128 × 8-bit, complete CMOS-type, common memory cells with two access ports, A and B, made with high-performance silicon-gate CMOS process technology.

To be able to read from and write in a common memory independently and asynchronously by both access ports, the M66222SP/FP has independent addressing control pins, $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$, and I/O pins One memory area is read from port A and written from port B, while another memory area is written from port A and is read from port B.

FEATURES

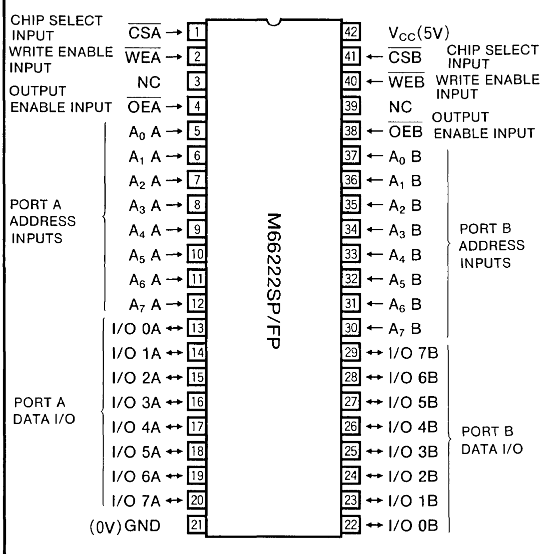
- Memory configuration 128×8bits×2 memory areas
- High-speed access : address access time 40ns(typ)
- Complete asynchronous access from both ports of A and B is possible.
- Access port for read/write is fixed for each memory area
- Completely static operation
- Low power dissipation for CMOS design
- Single 5V power supply
- Direct connection of I/O to TTL is possible
- 3-state output for I/O

APPLICATION

Buffer memory for communication, data transfer memory between MCUs (Micro Controller Unit)

The specifications are subject to change without notice

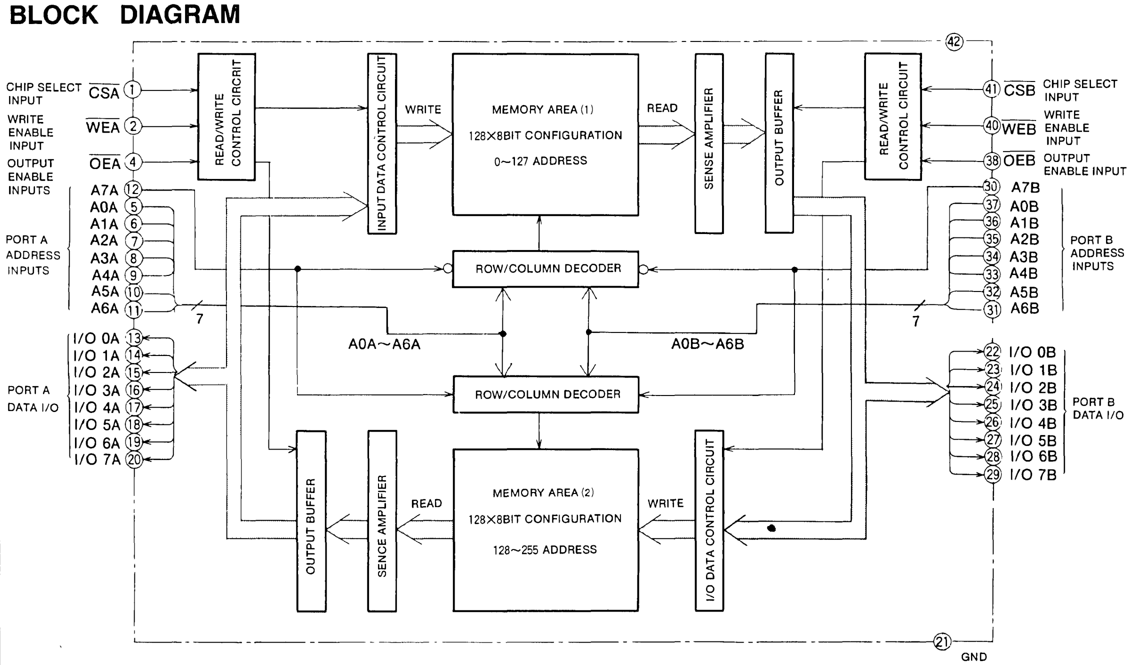
PIN CONFIGURATION (TOP VIEW)



Outline 42P4B 42P2R

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION

The M66222 is a mailbox suitable for data transfer between MCUs. Each 128×8-bit common memory cell with two sets of address lines and data line enables independent and asynchronous read and write operation from port A and B. The M66222 has a pair of 128 × 8-bit memory area : the memory area 1 is written from port A and read from port B while memory area 2 is read from port A and is written from port B.

If the address $A_0 \sim A_7$ is specified and $\overline{CS}$ is set to low-level, I/O pins are in input mode, and then $\overline{WE}$ is set to low-level, data at the I/O pins are written. If $\overline{WE}$ is set to high-level and $\overline{CS}$ and $\overline{OE}$ are set to low-level, I/O pins are in output mode, and then address $A_0 \sim A_7$ are specified, data of specified address are output to I/O pins. If $\overline{CS}$ is set to high-level, the M66222 is in no-selection state, being unable to read or write. The outputs are in a floating state (high-impedance state), enabling OR ties with other outputs. When I/O bus method is used, collisions of input and output data can be avoided by setting $\overline{OE}$ to high-level during write operations. When $\overline{CS}$ is set to high-level, the M66222 is in the standby state where the supply current is lowered.

FUNCTIONAL DESCRIPTION

As independent and asynchronous access to the M66222 from two ports is possible, four basic operations may take place according to mode setting of both ports.

(1) Port A—Write Port B—Write
(2) Port A—Write Port B—Read
(3) Port A—Read Port B—Write
(4) Port A—Read Port B—Read

When both ports are in the same mode, read or write, as in the case (1) or (4), the same address of memory will not be selected. Then there is no problem about data unstable. If, however, one port is in read mode and the other is in write mode, the same address may be selected in the case (2) or (3).

In this case, the data at the port in read mode may be changed from the already written data to the newly written data during the same cycle by writing the data in the same address from other port. See Fig. 1.

EXAMPLE : PORT A——ADDRESS SETTING FIRST-COME READ OPERATION
PORT B——ADDRESS SETTING LAST-COME WRITE OPERATION

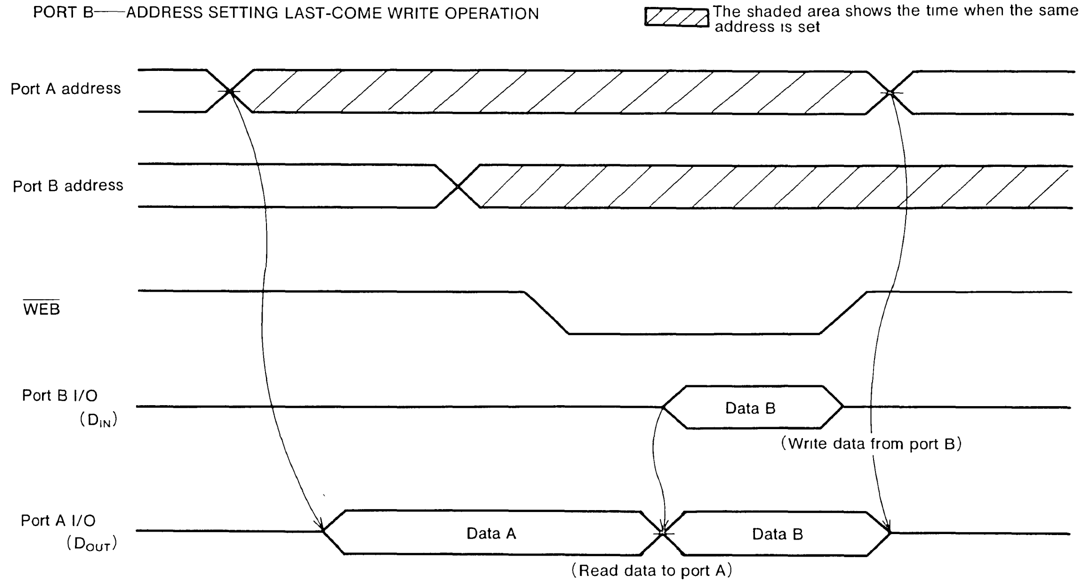


Fig. 1 Example of read data transition when the same address is selected.

ABSOLUTE MAXIMUM RATINGS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3~+7.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	T_a=25℃	T. B. D	W
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
V_I	Input voltage	0		V_{CC}	V
Topr	Operating temperature range	0		70	℃

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±10%, unless otherwise noted)

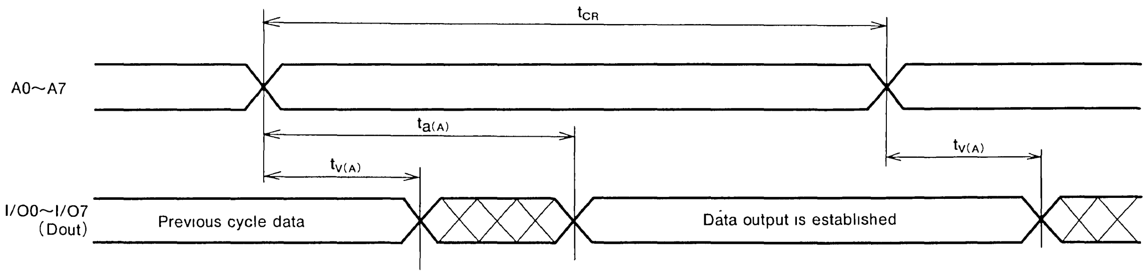
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.8	V
V_{OH}	High-level output voltage(I/O)		I_{OH}=−2mA	2.4			V
V_{OL}	Low-level output voltage(I/O)		I_{OL}=4mA			0.5	V
I_I	Input leakage current		V_I=0~V_{CC}			±10	μA
I_O	Output leakage current		$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=0~V_{CC}			±10	μA
I_{CC}	Average operating supply current (Both ports active)		$\overline{CS}$=V_{IL} Output pin open		T B. D		mA
I_{SB1}	Standby current	Both ports standby	$\overline{CS_A}$, $\overline{CS_B}$=V_{IH}		T B. D		mA
I_{SB2}	Standby current	One port standby	$\overline{CS_A}$ or $\overline{CS_B}$=V_{IH} I_{OUT}=0mA (Active port output pin open)		T. B. D		mA
I_{SB3}	Standby current	Both ports full standby	$\overline{CS_A}$, $\overline{CS_B}$≧ V_{CC}−0.2V Other input V_{IN}≧ V_{CC}−0.2V or V_{IN}≦0.2V		T. B. D		mA
I_{SB4}	Standby current	One port full standby	$\overline{CS_A}$ or $\overline{CS_B}$≧ V_{CC}−0.2V Other input V_{IN}≧ V_{CC}−0.2V or V_{IN}≦0.2V I_{OUT}=0mA (Active port output pin open)		T. B. D		mA

Note 1. The current flowing into the IC is positive
2 Typical values are at V_{CC}=5V, T_a=25℃

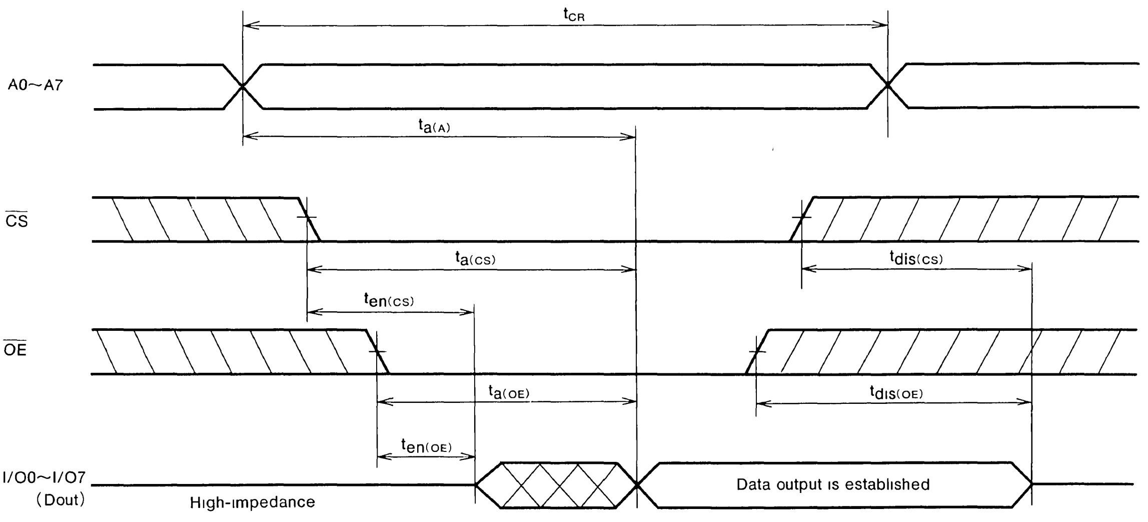
TIMING DIAGRAM

Read Cycle ($\overline{WE}=V_{IH}$)

● Read Cycle No. 1 (Address Control) ($\overline{CS}=\overline{OE}=V_{IL}$)

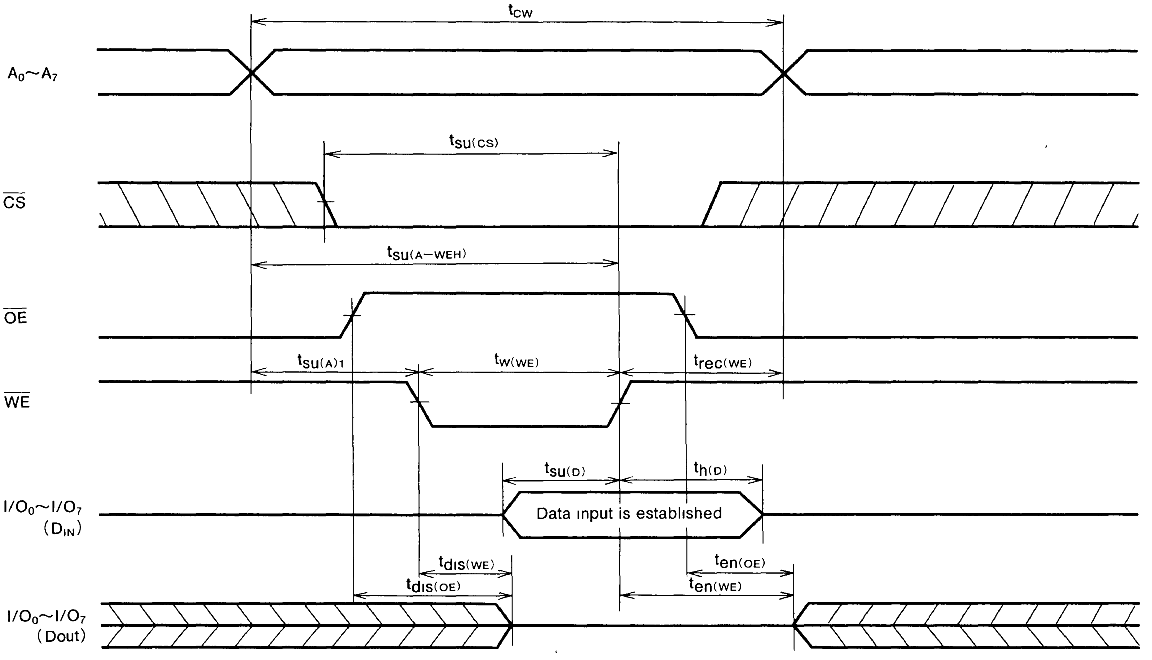


● Read Cycle No. 2 ($\overline{CS}$ Control)

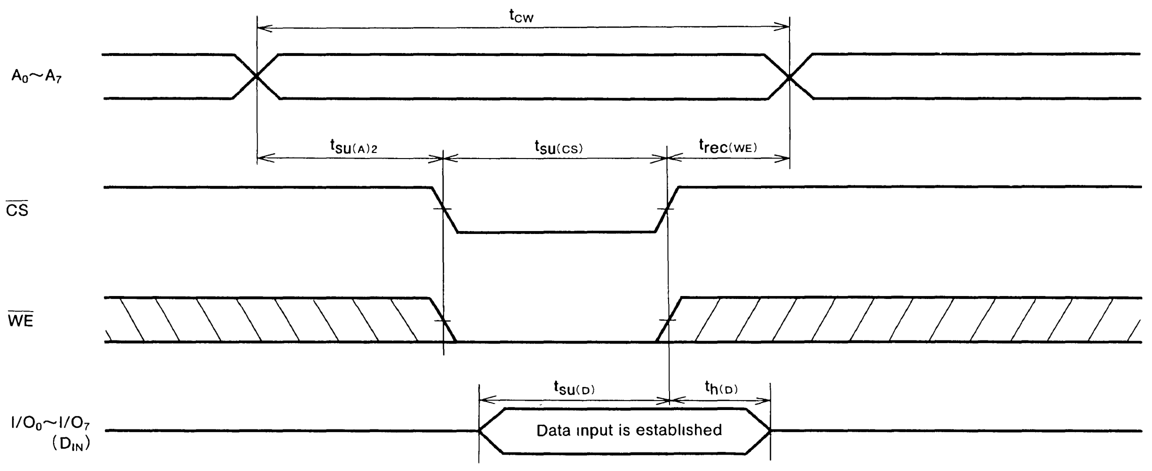


Write Cycle

● Write Cycle No. 1 ($\overline{WE}$ Control) Note 1, 2 and 3



● Write Cycle No. 2 ($\overline{CS}$ Control) Note 1, 2



Note 1 : Write operation is performed while both $\overline{CS}$ and $\overline{WE}$ are low-level
2 : Do not apply the reverse-phase signal when I/O pin is in the output state
3 : The output is maintained in the high-impedance state if the trailing edge of $\overline{WE}$ is performed before or at the same time of the trailing edge of $\overline{CS}$, or if the rising edge of $\overline{WE}$ is performed at the same time or after the leading edge of $\overline{CS}$.
4 : Shaded area=don't care

DESCRIPTION

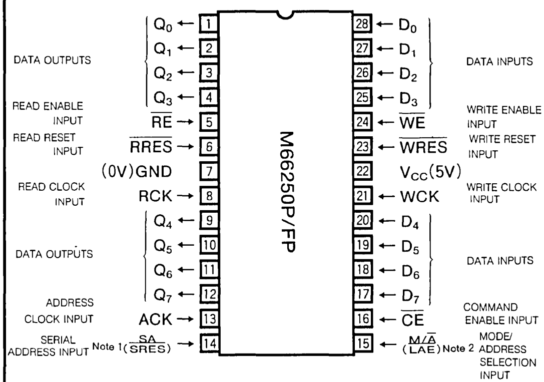
The M66250P/FP is an integrated circuit consisting of a high-speed line memory with a FIFO (First In First Out) structure in a 5120×8-bit configuration, using high-performance silicon-gate CMOS technology.

The M66250 can also be used for LIFO (Last In First Out). The start address of reading can be specified. As writes and reads can be done independently and asynchronously during each cycle, the device is suitable for buffer memory between equipment with different data processing speeds.

FEATURES

- 5120×8 bit organization
- High-speed access: access time 40ns
- FIFO/LIFO switching function
- Start address specification function (at reading)
- LIFO operation on a single chip
- Built-in pullup/pulldown resistor for the mode control pin.
- Completely independent and asynchronous read and write operation
- Variable-length delay bit
- I/O can be directly connected to TTL
- 3-state output

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y
28P2W

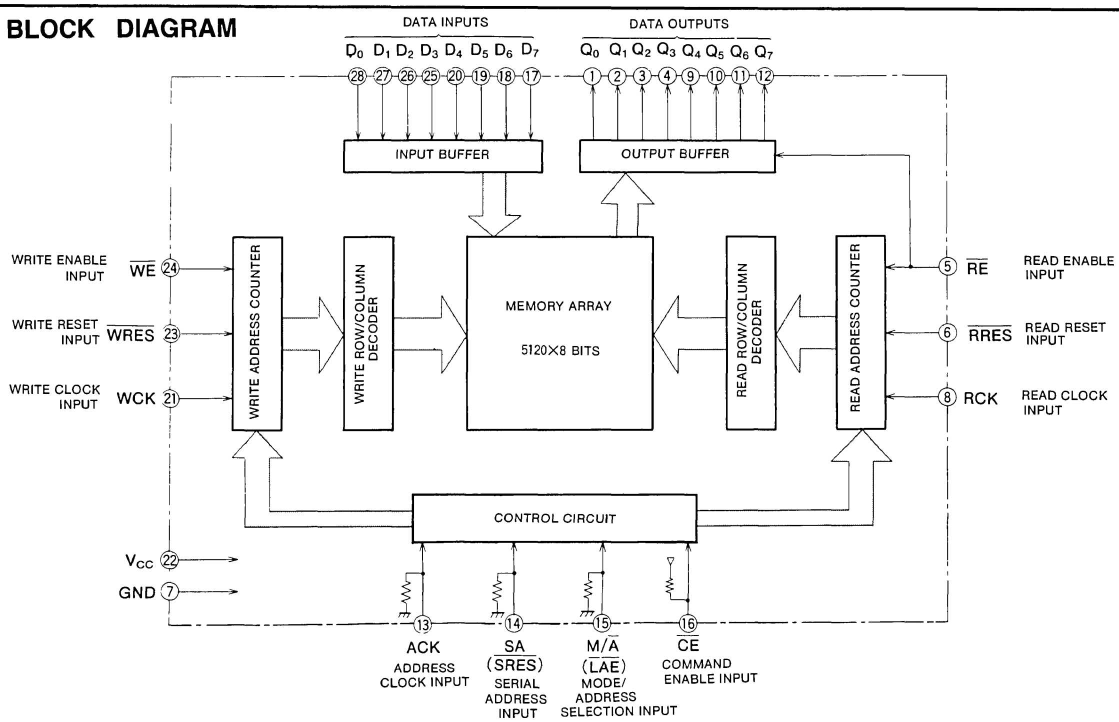
Note 1 : $\overline{\text{SRES}}$ sets the system reset mode

Note 2 : $\overline{\text{LAE}}$ can switch to a validness or invalidness of start address except during instruction cycles.

APPLICATION

High-speed facsimiles, digital copying machines, laser beam printers.

BLOCK DIAGRAM



FUNCTION

Write is performed by taking in the content of data inputs $D_0 \sim D_7$, in synchronous with the rise of the write clock input WCK, when write enable input $\overline{WE}$ is low-level, the write address counter incrementing or decrementing simultaneously. When $\overline{WE}$ is high-level, write is prohibited and the write address counter stops. When the write reset input $\overline{WRES}$ is set to low-level, the write address counter is initialized. When the read enable input $\overline{RE}$ is low-level, read is performed by outputting the memory content to data output $Q_0 \sim Q_7$ in synchronous with the rise of the read clock input RCK, and the read address counter is incremented or decremented at same time.

When $\overline{RE}$ is high-level, read is prohibited, and the read address counter stops. The output enters the floating state (high-impedance state).

When the read reset input $\overline{RRES}$ is set to low-level, the read address counter is initialized.

When command enable input $\overline{CE}$ is low-level, the instruction cycle is enabled. The FIFO/LIFO mode is set by the serial address input SA in synchronous with the rise of the address clock input ACK during the instruction cycle when the mode/address selection input $M/\overline{A}$ is high-level. The start address is set by the serial address input SA in synchronous with the rise of the address clock input ACK during the instruction cycle when $M/\overline{A}$ is low-level.

FUNCTIONAL DESCRIPTION

1. Function Setting

(1) Function setting table

① **System reset setting**

$\overline{CE}$	(SA) $\overline{SRES}$	$\overline{RRES}$	RCK	Function
H	L	L	↑	FIFO mode, no start address setting, read counter reset

$\overline{CE}$	(SA) $\overline{SRES}$	$\overline{WRES}$	WCK	Fuction
H	L	L	↑	FIFO mode, no start address setting, write counter reset

② **Mode setting**

$\overline{CE}$	$M/\overline{A}$ ($\overline{LAE}$)	ACK	SA ($\overline{SRES}$)	Function
L	H	↑	H	FIFO mode setting
L	H	↑	L	LIFO mode setting
L	L	↑	×	Start address setting (13 bits)

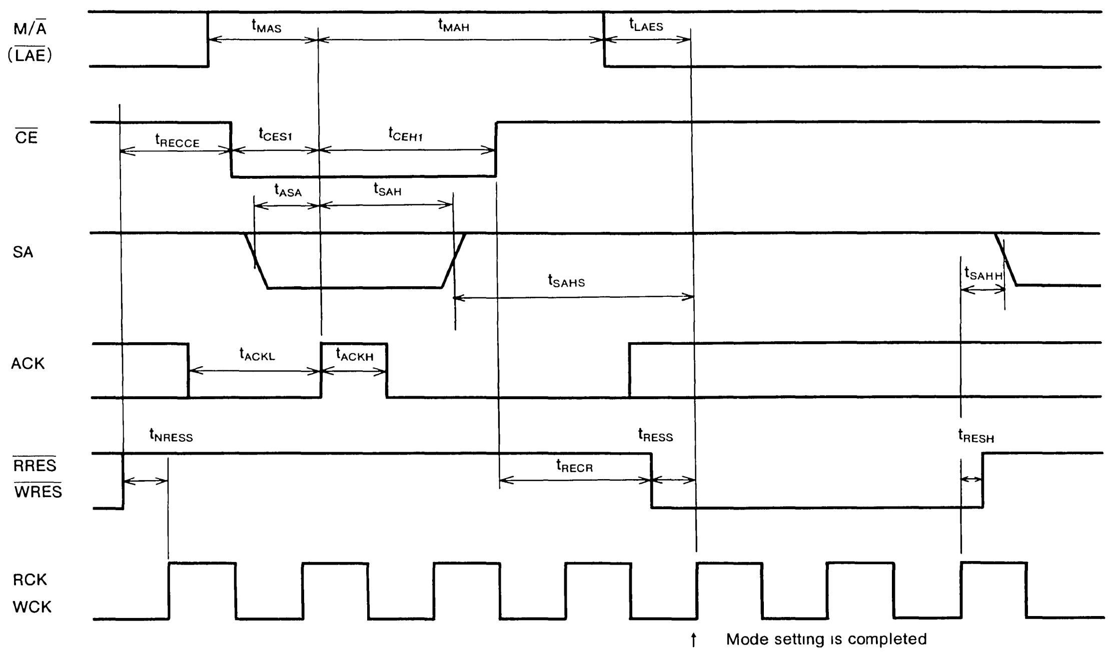
× : L or H

Note : The above mode becomes effective after the first reset.

③ **Effect of start address setting**

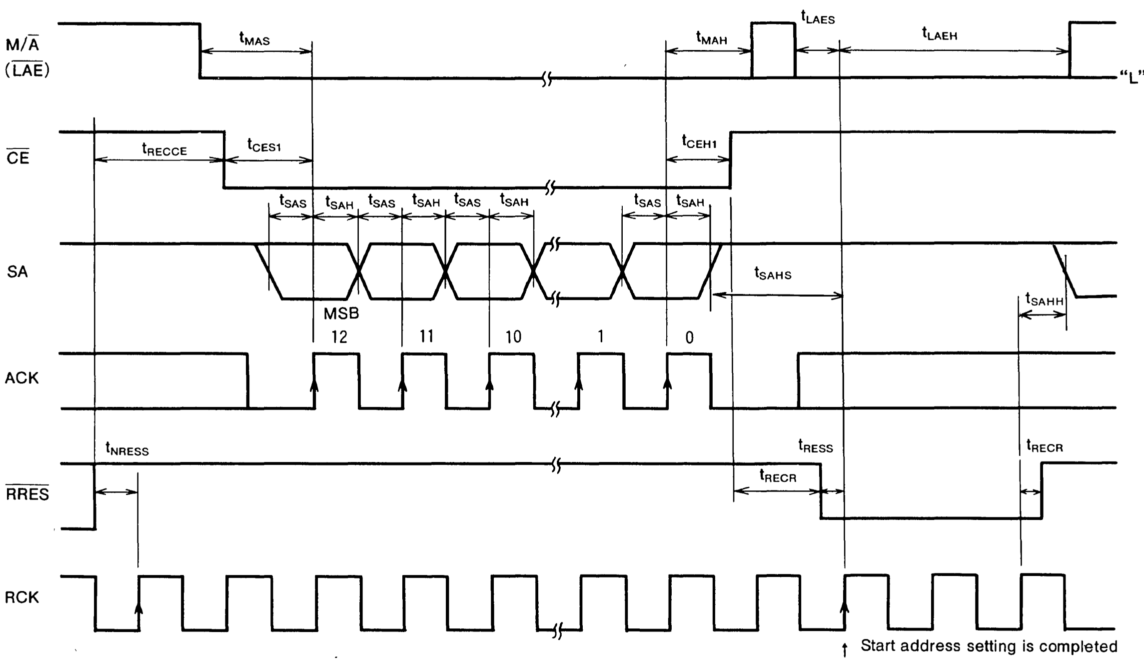
$\overline{CE}$	SA ($\overline{SRES}$)	($M/\overline{A}$) $\overline{LAE}$	$\overline{RRES}$	RCK	Function
H	H	L	L	↑	Start address setting is effective
H	H	H	L	↑	Start address setting is not effective

(2) FIFO/LIFO mode setting
When the mode/address selection input $M/\overline{A}$ is high-level and the command enable input $\overline{CE}$ is low-level, the FIFO/-LIFO mode is selected by the serial address input SA, in synchronous with the address clock input ACK. When the command enable input $\overline{CE}$ is high-level and the write reset input $\overline{WRES}$ is low-level, mode setting is completed in synchronous with the rise of the write clock input WCK, also provided that the write reset input $\overline{WRES}$ is low-level, in synchronous with the rise of the read clock input RCK and the read reset input $\overline{RRES}$ is low-level. The address counter is initialized at the same time.

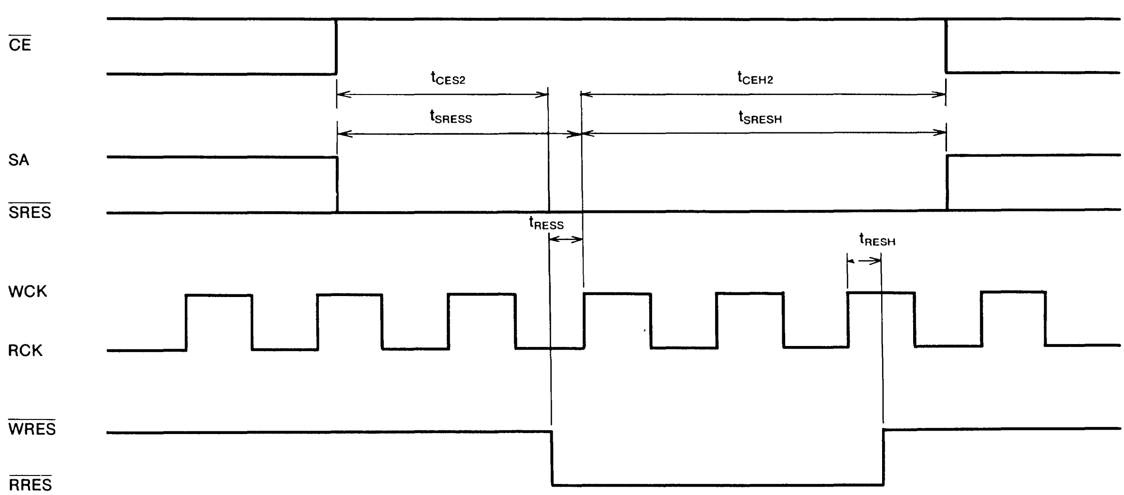


In the FIFO mode, the write address counter moves to address 0 in synchronous with the rise of the write clock input WCK when the write reset input $\overline{WRES}$ is set to low-level. The address of the write address counter increases in synchronous with the rise of the write clock input WCK.
When the read reset input $\overline{RRES}$ is low-level, the read address counter moves to address 0 if the start address is not specified, and moves to the start address if the start address is specified, in synchronous with the rise of the read clock input RCK. The cycles of the read address counter increases in synchronous with the read clock input RCK.
In LIFO mode the write address counter moves to address 0 or 5119 in synchronous with the rise of write clock input WCK, when the write reset input $\overline{WRES}$ is low-level, and, the read address counter moves to address 0 or 5119 if the start address is not specified or to the start address m or 5119-m if the start address is specified, in synchronous with the rise of the read clock input RCK. When the read reset input $\overline{RRES}$ is low-level. The cycle of the write address counter goes up or down in synchronous with the rise of the write clock input WCK.

(3) Start address setting
When the mode/address selection input $M/\overline{A}$ is low-level and the command enable input $\overline{CE}$ is low-level, the address that reading starts from is set by serial address input SA in synchronous with the rise of the address clock input ACK. When the command enable input $\overline{CE}$ is high-level and the read reset input $\overline{RRES}$ is low-level, the read address counter moves to the specified address in synchronous with the rise of the read clock invut RCK.

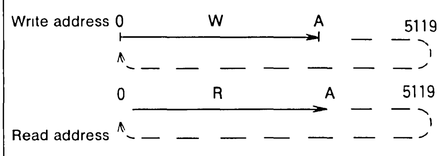
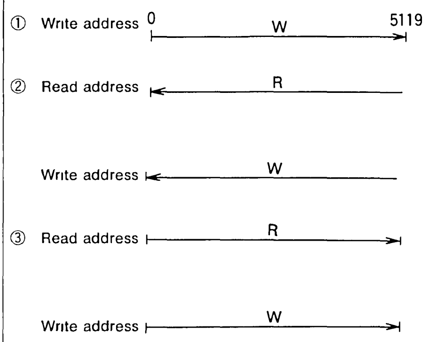
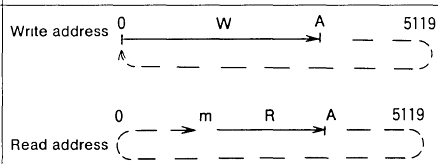
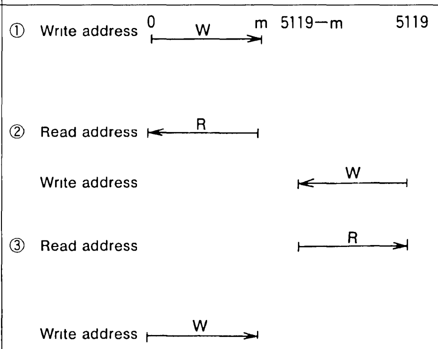


(4) System reset setting
(FIFO and address counter reset setting)
When the command enable input $\overline{CE}$ is high-level and $\overline{SRES}$ is low-level, and if the write reset input $\overline{WRES}$ and read reset input $\overline{RRES}$ are set to low-level, then the FIFO mode setting and the address counter are reset in synchronous with the rise of WCK and RCK.

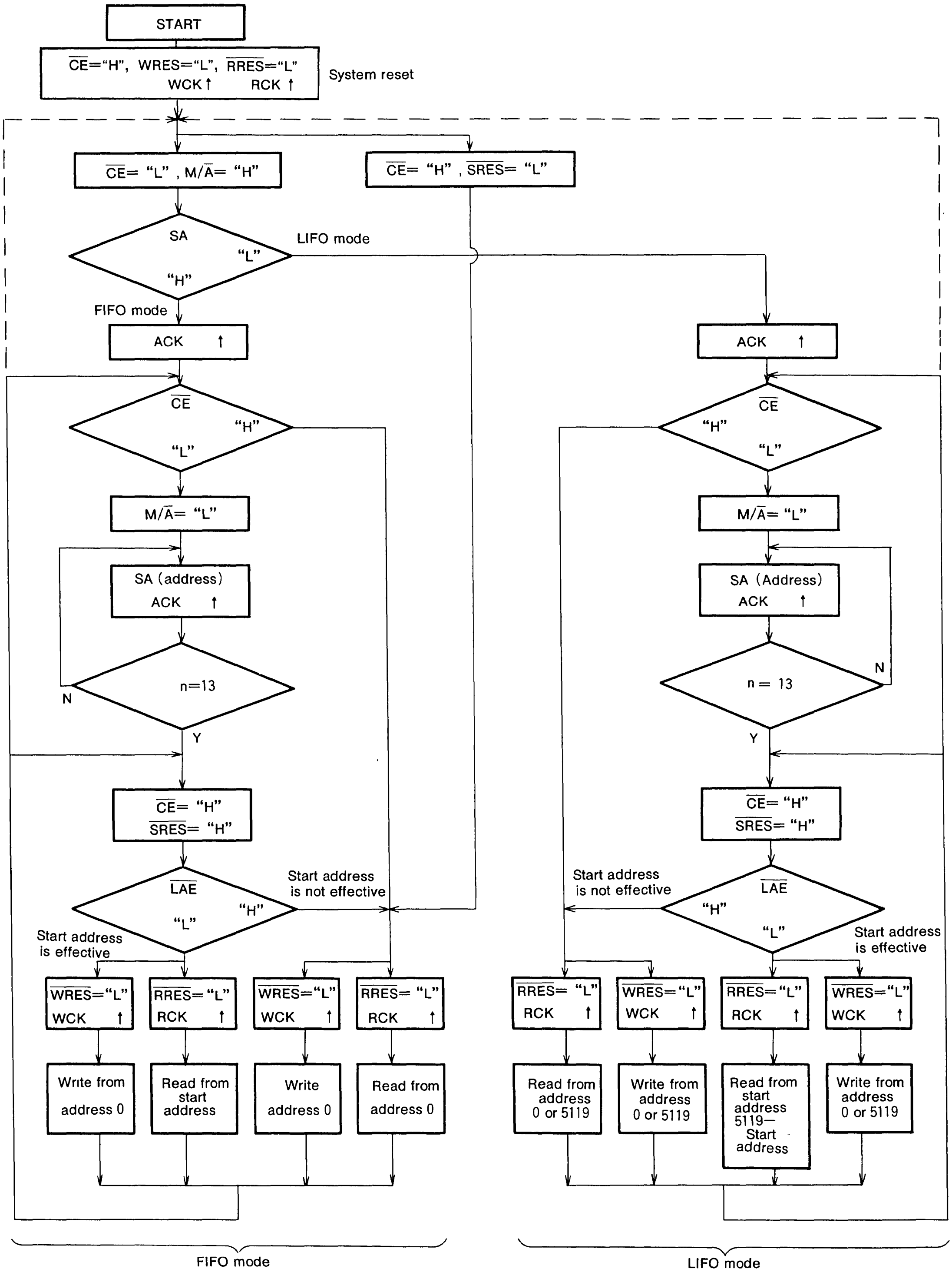


MITSUBISHI ELECTRIC

2. Write address and read address operation in FIFO and LIFO mode

FIFO and LIFO mode setting	Start address setting	Write address and read address operation	Write address/read address in read reset/write reset operation
FIFO	No		Write address : Move to address 0 Read address : Move to address 0
LIFO	No		Write address : Move to address 0 or 5119 Read address : Move to address 0 or 5119
FIFO	Yes		Write address : Move to address 0 Read address : Move to address m specified by the start address
LIFO	Yes		Write address : Move to address 0 or 5119 Read address : Move to the address that specified as the start address

OPERATION FLOW CHART



Note : Perform write reset and read reset before setting function after power-on.

MITSUBISHI
ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20+70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
Pd	Maximum power dissipation	Ta=25℃	500	mW
Tstg	Storage temperature range		−65 ~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+70℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Ground		0		V
T_{opr}	Operating ambient temperature range	−20		70	℃

ELECTRICAL CHARACTERISTICS (T_a=−20~+70℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max.	
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		V_{CC}−0.8			V
V_{OL}	Low-level output voltage	I_{OL}=4mA				0.55	V
I_{IH}	High-level input current	V_I=V_{CC}	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, $\overline{CE}$, D0~D7			1.0	μA
		V_I=V_{CC}	ACK, SA($\overline{SRES}$), M/$\overline{A}$($\overline{LAE}$)			0.27	mA
I_{IL}	Low-level input current	V_I=GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, ACK, SA($\overline{SRES}$), M/$\overline{A}$($\overline{LAE}$), D0~D7			−1.0	μA
		V_I=GND	$\overline{CE}$			−0.27	mA
I_{OZH}	Off state high-level output current	V_0=V_{CC}				5 0	μA
I_{OZL}	Off state low-level output current	V_0=GND				−5.0	μA
I_{CC}	Average operating supply current	V_I=V_{IH}, V_{IL} Output open t_{WCK}, t_{RCK}=100ns				100	mA
CI	Input capacitance	f=1MHz				10	pF
CO	Output capacitance when off	f=1MHz				15	pF

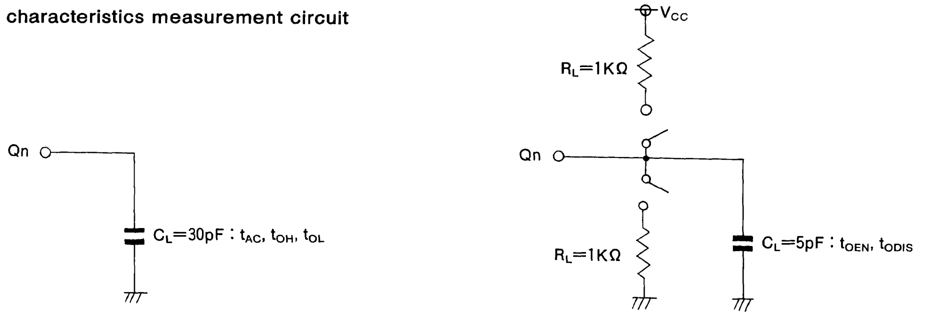
SWITCHING CHARACTERISTICS (T_a=−20~+70℃, V_{CC}= 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
t_{AC}	Access time				40	ns
t_{OH}	Output hold time		5			ns
t_{OL}	Output “L” period when reset		5		40	ns
t_{OEN}	Output enable time		5		40	ns
t_{ODIS}	Output disable time		5		40	ns

TIMING REQUIREMENTS (T_a=−20∼+70℃, V_{CC}= 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{WCK}	Write clock (WCK) cycle		50			ns
t_{WCKH}	Write clock (WCK) "H" pulse width		25			ns
t_{WCKL}	Write clock (WCK) "L" pulse width		25			ns
t_{RCK}	Read clock (RCK) cycle		50			ns
t_{RCKH}	Read clock (RCK) "H" pulse width		25			ns
t_{RCKL}	Read clock (RCK) "L" pulse width		25			ns
t_{DS}	Data set up time before WCK		15			ns
t_{DH}	Data hold time after WCK		5			ns
t_{RESS}	Reset set up time before WCK, RCK		15			ns
t_{RESH}	Reset hold time after WCK, RCK		5			ns
t_{NRESS}	Non-reset set up time before WCK, RCK		25			ns
t_{NRESH}	Non-reset hold time after WCK, RCK		5			ns
t_{WES}	$\overline{WE}$ set up time before WCK		15			ns
t_{WEH}	$\overline{WE}$ hold time after WCK		5			ns
t_{NWES}	$\overline{WE}$ non-select set up time before WCK		15			ns
t_{NWEH}	$\overline{WE}$ non-select hold time after WCK		5			ns
t_{RES}	$\overline{RE}$ set up time before RCK		15			ns
t_{REH}	$\overline{RE}$ hold time after RCK		5			ns
t_{NRES}	$\overline{RE}$ non-select set up time before RCK		15			ns
t_{NREH}	$\overline{RE}$ non-select hold time after RCK		5			ns
t_H	Data hold time				20	ms
t_{MAS}	M/$\overline{A}$ set up time before ACK		25			ns
t_{MAH}	M/$\overline{A}$ hold time after ACK		5			ns
t_{CES1}	$\overline{CE}$ set up time before ACK		25			ns
t_{CEH1}	$\overline{CE}$ hold time after ACK		5			ns
t_{SAS}	SA set up time before ACK		25			ns
t_{SAH}	SA hold time after ACK		5			ns
t_{LAES}	$\overline{LAE}$ set up time before WCK, RCK		25			ns
t_{LAEH}	$\overline{LAE}$ hold time after WCK, RCK		5			ns
t_{SAHS}	SA "H" set up time before WCK, RCK when reset		25			ns
t_{SAHH}	SA "H" hold time after WCK, RCK when reset		5			ns
t_{CES2}	$\overline{CE}$ set up time before WCK, RCK when system reset		25			ns
t_{CEH2}	$\overline{CE}$ hold time after WCK, RCK when system reset		5			ns
t_{SRESS}	$\overline{SRES}$ set up time before WCK, RCK when system reset		25			ns
t_{SRESH}	$\overline{SRES}$ hold time after WCK, RCK when system reset		5			ns
t_{ACKH}	"H" pulse width for ACK		50			ns
t_{ACKL}	"L" pulse width for ACK		50			ns
t_{RECR}	WCK, RCK recovery time after mode set		100			ns
t_{RECCE}	$\overline{CE}$ recovery time after reset		100			ns
t_r, t_f	Input pulse rise and fall time				20	ns

Switching characteristics measurement circuit

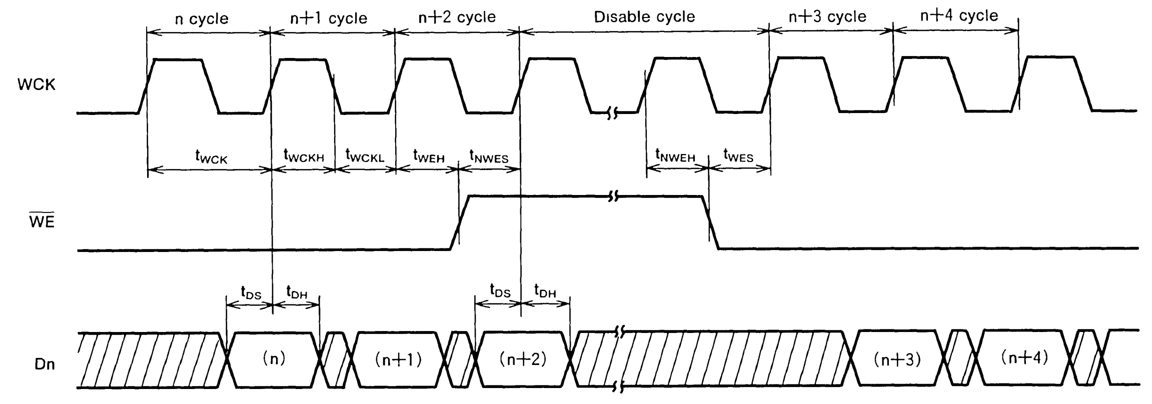


Input pulse amplitude		: 0∼3V
Input pulse rise and fall time		: 3ns
Reference voltage	Input	: 1.3V
	Output	: 1.3V

OPERATION TIMING

1. FIFO mode

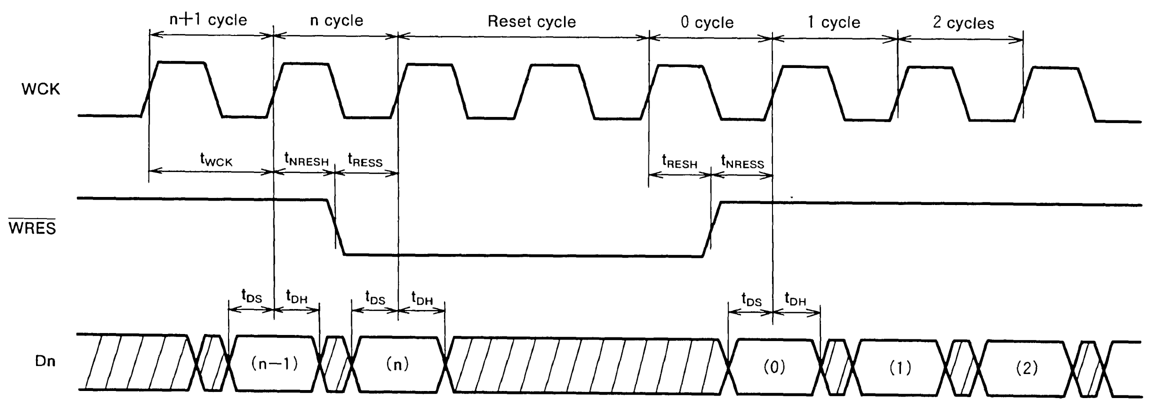
- Write cycle (Irrelevant to start address setting)



WRES= "H" , LAE= "L" or "H"
SRES= "H"

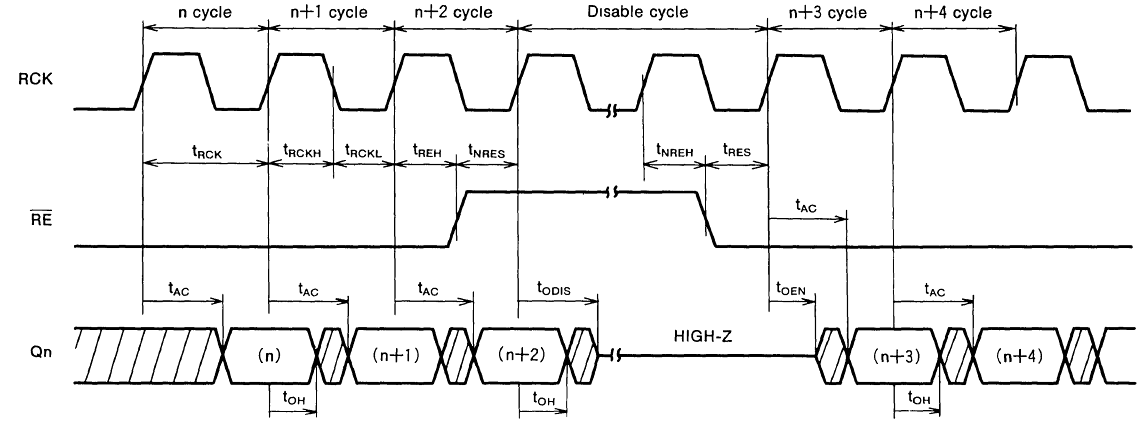
- Write reset cycle (Irrelevant to start address setting)

(The reset cycle requires a minimum of two cycles Before the first reset cycle and after the power is turned on WRES should be set to high-level for 1 cycle or more)



WE= "L" , LAE= "L" or "H"
SRES "H"

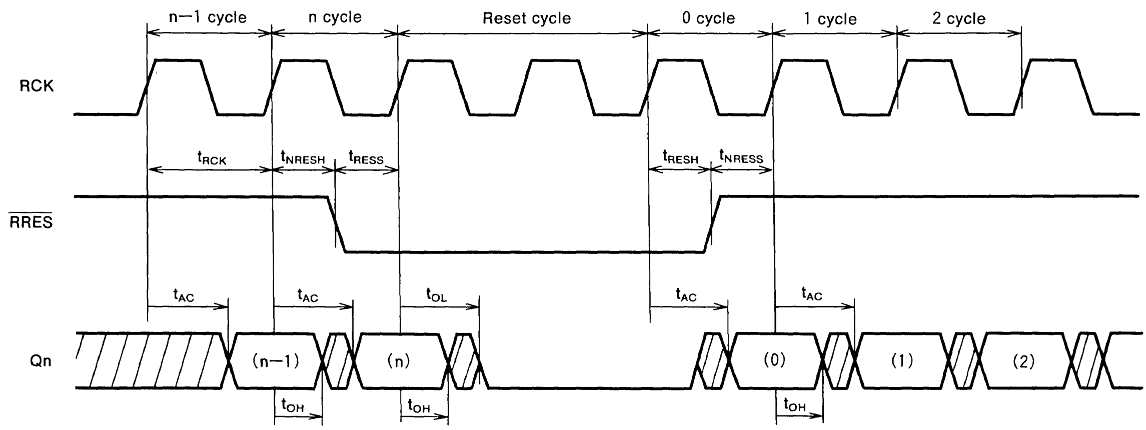
- **Read cycle**



$\overline{RRES}$= "H" , $\overline{LAE}$= "L" or "H"
$\overline{SRES}$= "H"

- **Read reset cycle**

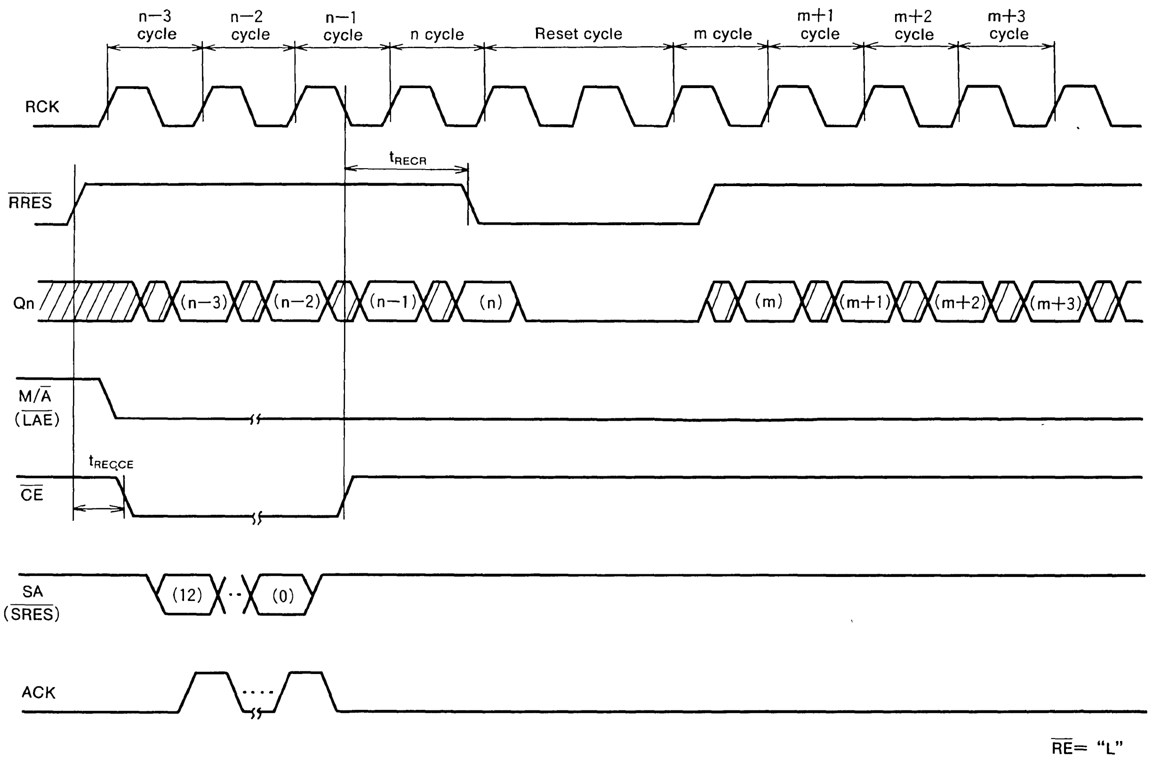
(The reset cycle requires two cycles at minimum During the first two cycles Qn is low-level For one cycle or more, $\overline{RRES}$ should be set to high-level befor the first reset cycle, and after power is turned on)



$\overline{RE}$= "L" , $\overline{LAE}$= "H"
$\overline{SRES}$= "H"

- Read reset cycle (start address is set)

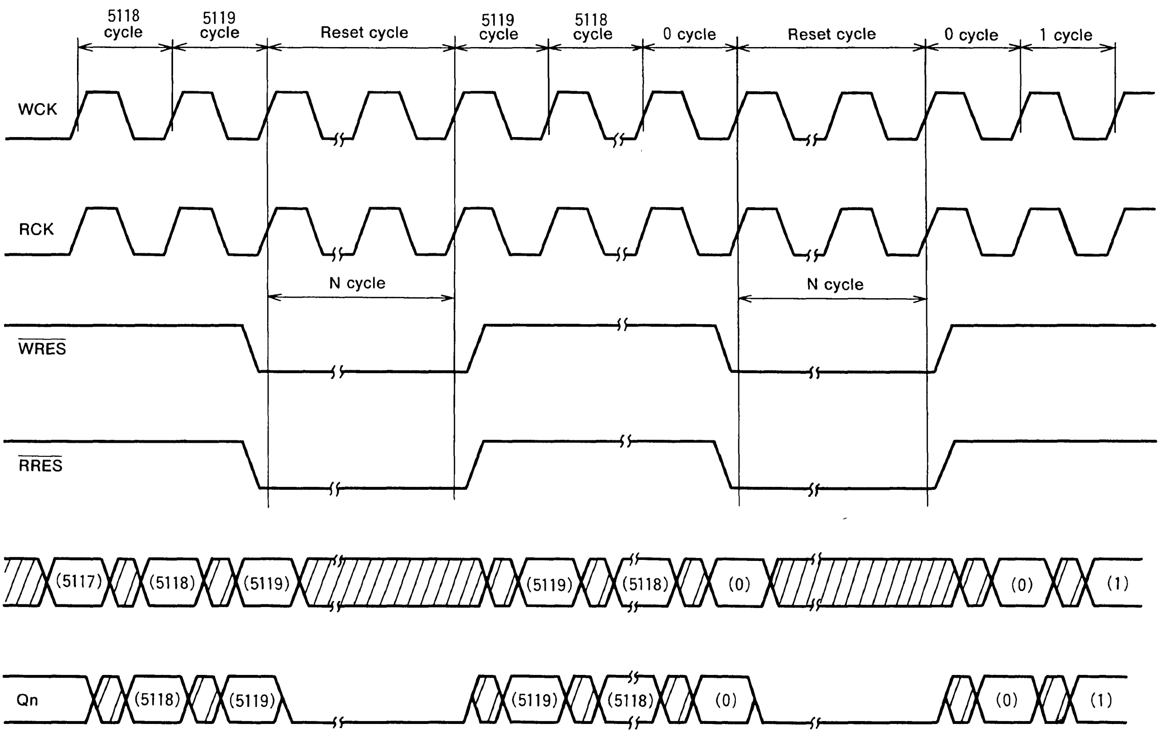
(The reset cycle requires two cycles at minimum During the first two cycles, Qn is low-level For at least one cycle $\overline{RRES}$ should be set to high-level before the first reset cycle, and after power is turned on.)



2. LIFO MODE

● **Start address is not set**

(The reset cycle requires two cycles at minimum. During the first two cycles, Qn is low-level For at least one cycle, $\overline{RRES}$ should be set to high-level and $\overline{WRES}$ should be set to high-level before the first reset cycle and after power is turned on.)



N≧2 $\overline{RE}$, $\overline{WE}$ = "L"

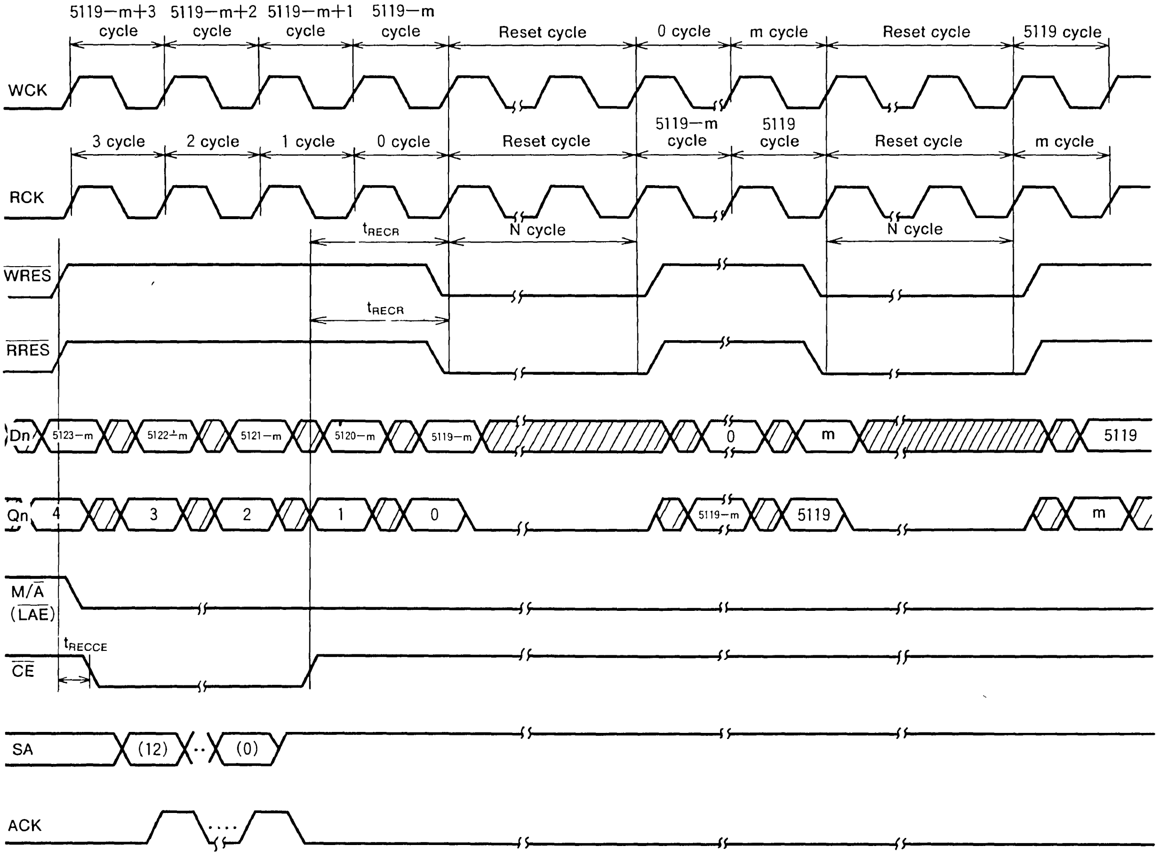
$\overline{LAE}$ = "H"

$\overline{CE}$ = "H"

$\overline{SRES}$ = "H"

● Start address is set

(The reset cycle requires two cycles at minimum, and the first two cycles Qn is low-level More than one cycle should be set when RRES is high-level before the first reset cycle after power on)



N≧2 RE, WE= "L"

M66305P/FP

TOGGLE LINE BUFFER

DESCRIPTION

The M66305P/FP is an integrated circuit consisting of a pair of 5,120-bit line memories. The clocked serial input data is output as a serial data synchronized with external clock at a speed up to 10Mbit/sec.

The device employs a double buffer configuration in which while data is being written to one memory, data can be read out of another one, realizing completely simultaneou operation of reading and writing.

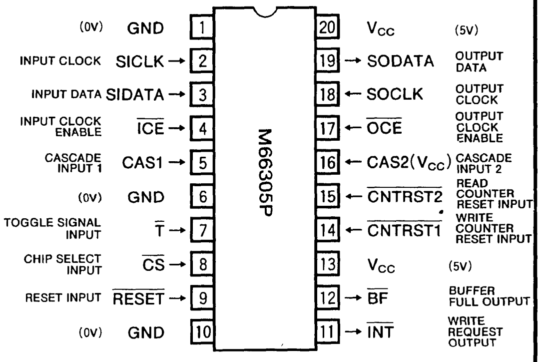
FEATURES

- 5,120X1-bit serial input and serial output line buffer memory.
- Transfer speed up to 10M bit/sec.
- Two line buffer can be selected by the external toggle signal.
- Cascade connection enables doubled memory capacity.
- The output level after output is completed can be set either high or low by the cascade input terminal (CAS1).
- Low-noise and high-output current output.
  $I_O = \pm 24mA$
- Schmitt triger circuit for all input terminals.
- Negative noise reduction circuit for $\overline{RESET}$, $\overline{T}$, $\overline{CNTRST1}$, and $\overline{CNTRST2}$.

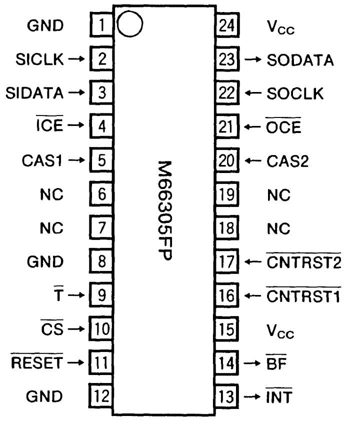
APPLICATION

Data buffer between image processing systems and peripheral equipments.

PIN CONFIGURATION (TOP VIEW)



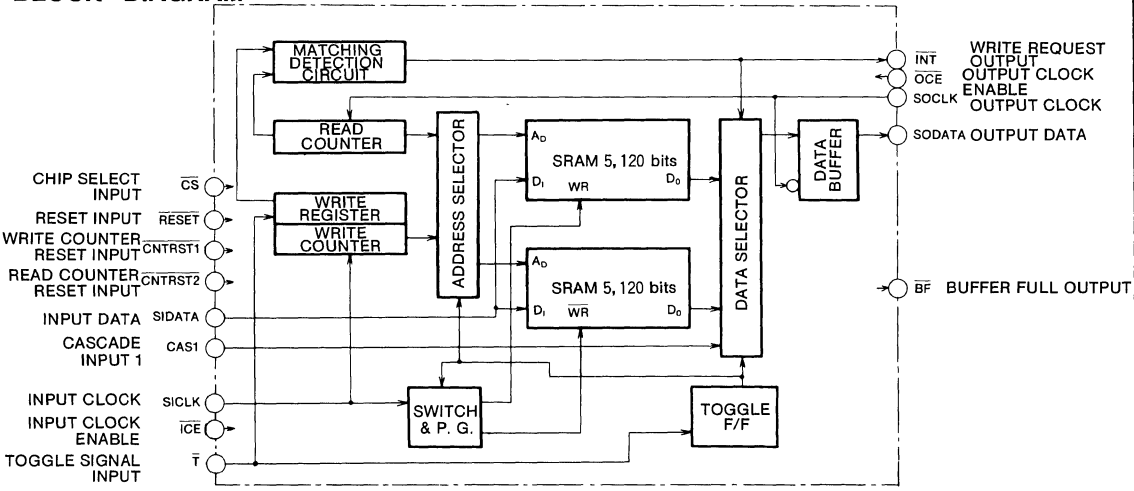
Outline 20P4



Outline 24P2W

NC : No connection

BLOCK DIAGRAM



FUNCTION

Input data (SIDATA) is written to the internal line memory synchronized with the rising edge of the input clock (SICLK) with input clock enable ($\overline{ICE}$) being low-level. Output data (SODATA) is output synchronized with the falling edge of output clock (SOCLK) with output clock enable ($\overline{OCE}$) being low-level. Double buffer configuration makes independent read and write operation possible.

Toggle signal ($\overline{T}$) is to be turned to low-level after completion of both read and write operation, and changes operation mode of each line memory where line memory being used in write mode turns to read mode and vice versa. Write counter reset input ($\overline{CNTRST1}$) enables re-writing and read counter reset input ($\overline{CNTRST2}$) enables repeated output.

FUNCTION TABLE

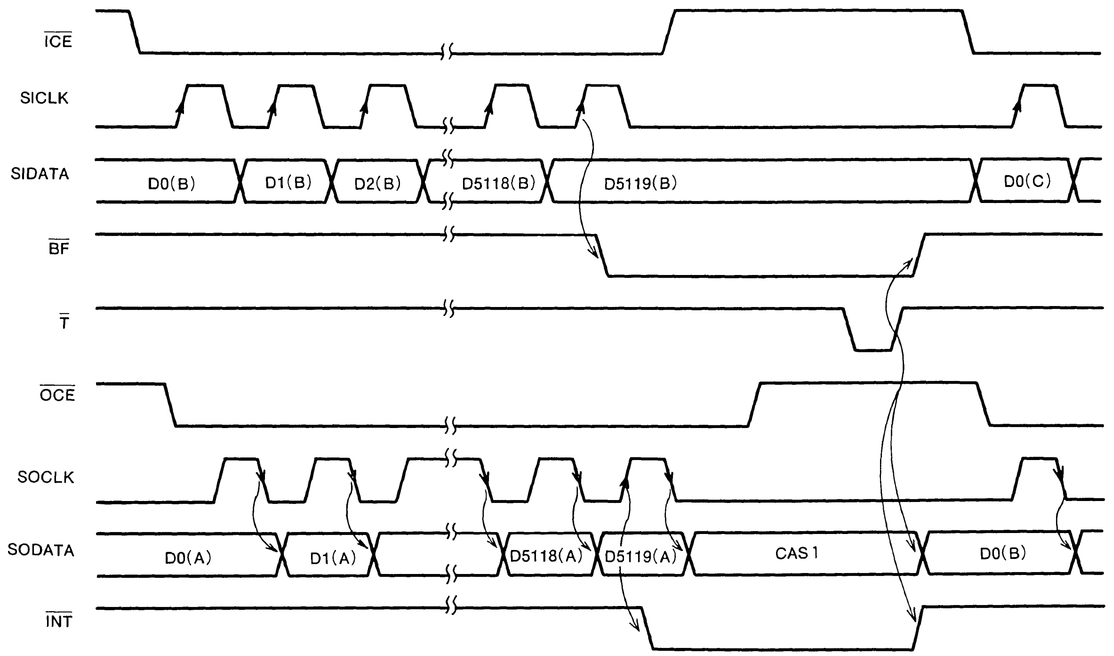
Inputs									Outputs			Remark
$\overline{RES}$	$\overline{CS}$	$\overline{ICE}$	SIC	$\overline{OCE}$	SOC	$\overline{T}$	$\overline{CR1}$	$\overline{CR2}$	SOD	$\overline{INT}$	$\overline{BF}$	
L	×	×	×	×	×	×	×	×	L	H	H	Initialization
H	H	×	×	×	×	×	×	×	Q^0	Q^0	Q^0	The internal and output conditions are not changed.
H	L	H	×	H	×	H	H	H	Q^0	Q^0	Q^0	The internal and output conditions and not changed
H	L	L	⎍	H	×	H	H	H	Q^0	Q^0	*1	Writes the data to the line buffer memory at the rise of SICLK
H	L	H	×	L	⎍	H	H	H	*2	*3	Q^0	Output the data at the fall of SOCLK
H	L	L	⎍	L	⎍	H	H	H	*2	*3	*1	Write and read operation
H	L	L	L	L	L	⊔	H	H	*4	H	H	At the rise of $\overline{T}$, 1) Sets the line buffer memory in read mode to write mode and in write mode to read mode 2) Disables $\overline{BF}$ and $\overline{INT}$.
H	L	H	×	L	L	⊔	H	H				
H	L	L	L	H	×	⊔	H	H				
H	L	H	×	H	×	⊔	H	H				
H	L	L	L	×	×	H	⊔	H	*5	*5	H	The internal write counter is reset by $\overline{CNTRST1}$ and re-writing operation is enabled
H	L	H	×	×	×	H	⊔	H				
H	L	×	×	L	L	H	H	⊔	*6	H	*6	The internal read counter is reset by $\overline{CNTRST2}$ and repetition of output is possible
H	L	×	×	H	×	H	H	⊔				

Q^0 : No change
× : Don't Care
* 1 : $\overline{BF}$ changes from high-to low-level on the rise of SICLK to write the 5, 120th bit.
* 2 : Written data is output in sequence synchronized with the falling edge of SOCLK.
* 3 : $\overline{INT}$ changes from high-to low-level on the rise of SOCLK reading the last data written.
* 4 : Output the first data written (D_0).
* 5 : Output operation can be made, irrespective of $\overline{CNTRST1}$.
* 6 : SODATA changes to the data written first (D_0). Write operation is not affected by $\overline{CNTRST2}$.

PIN DESCRIPTION

Pin name	Description	Function
$\overline{\text{RESET}}$	Reset input	Initialize M66305 (SODATA="L", $\overline{\text{BF}}$=$\overline{\text{INT}}$="H")
$\overline{\text{CS}}$	Chip select input	At low-level,M66305 is enabled while at high-level, any input data except for $\overline{\text{RESET}}$ are ignored
$\overline{\text{ICE}}$	Input clock enable	At low-level, input clock (SICLK) is enabled, and disabled at high-level.
SICLK SIDATA	Input clock Input data	Input data (SIDATA) is written to the line buffer memory at the rising edge of input clock (SICLK).
$\overline{\text{OCE}}$	Output clock enable	At low-level, the output clock (SOCLK) is enabled, and disabled at high-level.
SOCLK SODATA	Output clock Output data	Output date (SODATA) is read out on the falling edge of output clock (SOCLK).
$\overline{\text{T}}$	Toggle signal input	Sets a line buffer memory in write mode to read mode, and vice versa
$\overline{\text{BF}}$	Buffer full output	$\overline{\text{BF}}$ is output on the rise of the 5,120th bit and shows that no more writing is possible, and write operation is disabled. The rising edge of the toggle signal ($\overline{\text{T}}$) disables $\overline{\text{BF}}$
$\overline{\text{INT}}$	Write request output	$\overline{\text{INT}}$ is output on the rising edge of SOCLK after the last written data is output, and output operation is disabled The rising edge of the toggle signal ($\overline{\text{T}}$) disables $\overline{\text{INT}}$
$\overline{\text{CNTRST1}}$	Write counter reset input	Enable this input when re-write operation is required during writing
$\overline{\text{CNTRST2}}$	Read counter reset input	Enable this input to repeat the same output data
CAS1	Cascade input1	CAS1 input data is output on the fall of SOCLK after the last written data is output Make sure to connect to V_{CC} or GND when cascade connection is not used
CAS2	Cascade input2	Up to two cascade can be available Connect the CAS2 terminal of the master to V_{CC} and the CAS2 terminal of the slave to GND See APPLICATIION EXAMPLE for details
NC	No Connection	Applicable only to the M66305FP and this is no-connection terminal .

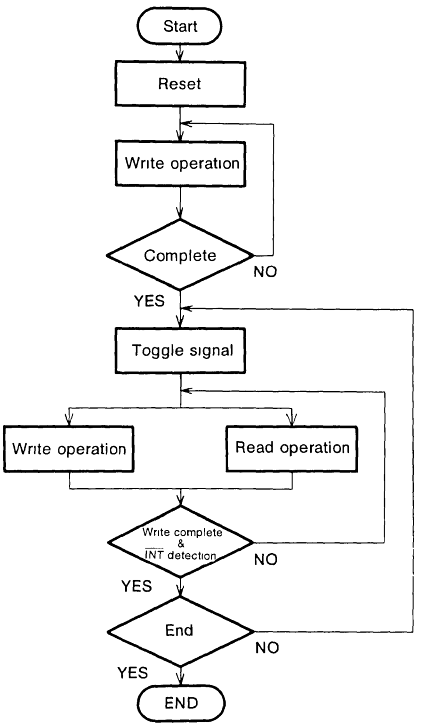
TIMING DIAGRAM



* This timing is for one line length of 5,120 bits If the length is shorter than this, $\overline{BF}$ stays high-level

OPERATION FLOW CHART

The first operation after reset is write operation only. Input the toggle signal ($\overline{T}$) after one line is written.
After the above operation, the previously written data can be output or new data can be written in parallel. After one line is completed, and after the output is completed ($\overline{INT}$ output), input the toggle signal ($\overline{T}$).



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5\sim+7.0$	V
V_I	Input voltage		$-0.5\sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5\sim V_{CC}+0.5$	V
Pd	Power dissipation	Mounted	700	mW
Tstg	Storage temperature		$-65\sim+150$	℃

RECOMMENDED OPERATING CONDITIONS ($T_a=-10\sim+70$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
GND	Supply voltage			0.0		V
V_I	Input voltage		0.0		V_{CC}	V
V_O	Output voltage		0.0		V_{CC}	V
Topr	Storage temperature		−10		+70	℃

ELECTRICAL CHARACTERISTICS ($T_a=-10\sim+70$℃, $V_{CC}=5V\pm10\%$, GND=0V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
V_{T+}	Positive threshold voltage	All input			2.4	V
V_{T-}	Nagative threshold voltage	All input	0.6			V
$V_{T+}-V_{T-}$	Hysteresis width	All input		0.4		V
V_{OH}	High-level output voltage	$I_{OH}=-24mA$	$V_{CC}-0.8$	$V_{CC}-0.35$* $V_{CC}-0.4$**		V
V_{OL}	Low-level output voltage	$I_{OL}=+24mA$		0.25* 0.30**	0.53	V
I_{CC}	Static power dissipation	$V_I=V_{CC}$ or GND		55* 45**	110	mA
I_{IH}	High-level input current	$V_I=5.5V$			+1.0	μA
I_{IL}	Low-level input current	$V_I=0V$			−1.0	μA
C_I	Input capacitance				10	pF

Note 1: The current flowing into the IC is positive current *$T_a=25$℃ **$T_a=70$℃

TIMING REQUIREMENTS (T_a=−10~+70℃, V_{CC}=5V±10%, GND=0V unless otherwise noted)

Symbol	Parameter	Test condition	Limits Min	Limits Typ	Limits Max	Unit
$t_{w\pm(SIC)}$	Input clock pulse width (Note 2)		30			ns
$t_{w\pm(SOC)}$	Output clock pulse width (Note 2)	Ta=25℃	43			ns
		Ta=−10~+70℃	50			
$t_{w(\overline{T})}$	Toggle signal input pulse width		150			ns
$t_{w(\overline{RES})}$	Reset input pulse width		100			ns
$t_{w(\overline{CR1})}$	Write counter reset input pulse width		100			ns
$t_{w(\overline{CR2})}$	Read counter reset input pulse width		100			ns
$t_{su(SID-SIC)}$	Input data setup time before input clock		25			ns
$t_{h(SIC-SID)}$	Input data hold time after input clock		0			ns
$t_{su(\overline{ICE}-SIC)}$	Input clock enable setup time before input clock		25			ns
$t_{h(SIC-\overline{ICE})}$	Input clock enable hold time after input clock		0			ns
$t_{su(\overline{CS}-SIC)}$	Chip select setup time before input clock		150			ns
$t_{h(SIC-\overline{CS})}$	Chip select hold time after input clock		100			ns
$t_{su(\overline{OCE}-SOC)}$	Output clock enable setup time before output clock		25			ns
$t_{h(SOC-\overline{OCE})}$	Output clock enable hold time after output clock		0			ns
$t_{su(\overline{CS}-SOC)}$	Chip select setup time before output clock		150			ns
$t_{h(SOC-\overline{CS})}$	Chip select hold time after output clock		100			ns
$t_{su(\overline{CS}-\overline{T})}$	Chip select setup time before toggle signal		100			ns
$t_{h(\overline{T}-\overline{CS})}$	Chip select hold time after toggle signal		100			ns
$t_{h(SIC-\overline{T})}$	Toggle signal hold time after input clock		100			ns
$t_{rec(\overline{T}-SIC)}$	Input clock recovery time after toggle signal		150			ns
$t_{h(SOC-\overline{T})}$	Toggle signal hold time after output clock		100			ns
$t_{rec(\overline{T}-SOC)}$	Output clock recovery time after toggle signal		150			ns
$t_{su(\overline{CS}-\overline{CR1})}$	Chip select setup time before write counter reset		100			ns
$t_{h(\overline{CR1}-\overline{CS})}$	Chip select hold time after write counter reset		100			ns
$t_{su(\overline{CS}-\overline{CR2})}$	Chip select setup time before read counter reset		100			ns
$t_{h(\overline{CR2}-\overline{CS})}$	Chip select hold time after read counter reset		100			ns
$t_{rec(\overline{R}-SIC/SOC)}$	Input and output clock recovery time after reset		100			ns
$t_{rec(\overline{CR1}-SIC)}$	Input clock recovery time after write counter reset		150			ns
$t_{rec(\overline{CR2}-SOC)}$	Output clock recovery time after read counter reset		150			ns

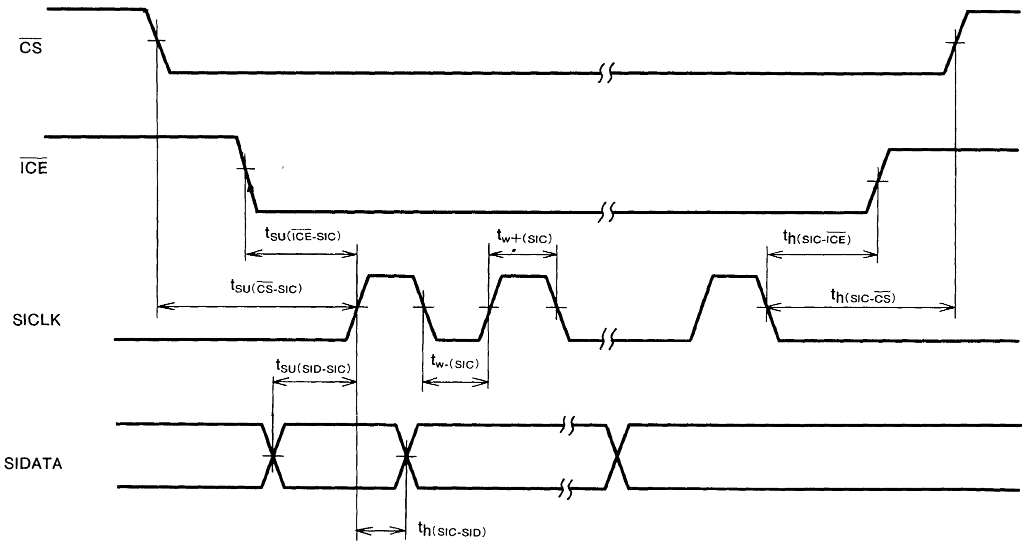
Note 2 : Conditions to satisfy the switching characteristics f_{max}=10MHz (cycle 100ns) :
$100ns \leqq (t_{w+})+(t_{w-})$

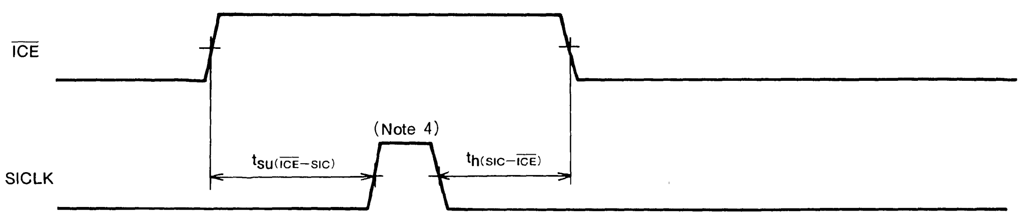
SWITCHING CHARACTERISTICS (T_a=−10~+70℃, V_{CC}=5V±10%, GND=0V)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$f_{max(SICLK)}$	Input clock maximum repetitive frequency		10			MHz
$f_{max(SOCLK)}$	Output clock maximum repetitive frequency		10			MHz
$t_{PLH(SOC-SOD)}$	Propagation time between input clock and output data	C_L=50pF			36	ns
		C_L=150pF			40	
$t_{PHL(SOC-SOD)}$		C_L=50pF			36	ns
		C_L=150pF			40	
$t_{PHL(SIC-\overline{BF})}$	Propagation time between input clock and $\overline{BF}$	C_L=50pF			75	ns
		C_L=150pF			85	
$t_{PHL(SOC-\overline{INT})}$	Propagation time between output clock and $\overline{INT}$	C_L=50pF			75	ns
		C_L=150pF			85	
$t_{PLH(\overline{T}-\overline{BF})}$	Propagation time between toggle signal and $\overline{BF}$	C_L=150pF			100	ns
$t_{PLH(\overline{T}-\overline{INT})}$	Propagation time between toggle signal and $\overline{INT}$				100	ns
$t_{PLH(\overline{R}-\overline{BF})}$	Propagation time between reset input and $\overline{BF}$				100	ns
$t_{PLH(\overline{R}-\overline{INT})}$	Propagation time between reset input and $\overline{INT}$				100	ns
$t_{PLH(\overline{CR1}-\overline{BF})}$	Propagation time between write counter reset and $\overline{BF}$				100	ns
$t_{PLH(\overline{CR2}-\overline{INT})}$	Propagation time between read counter reset and $\overline{INT}$				100	ns

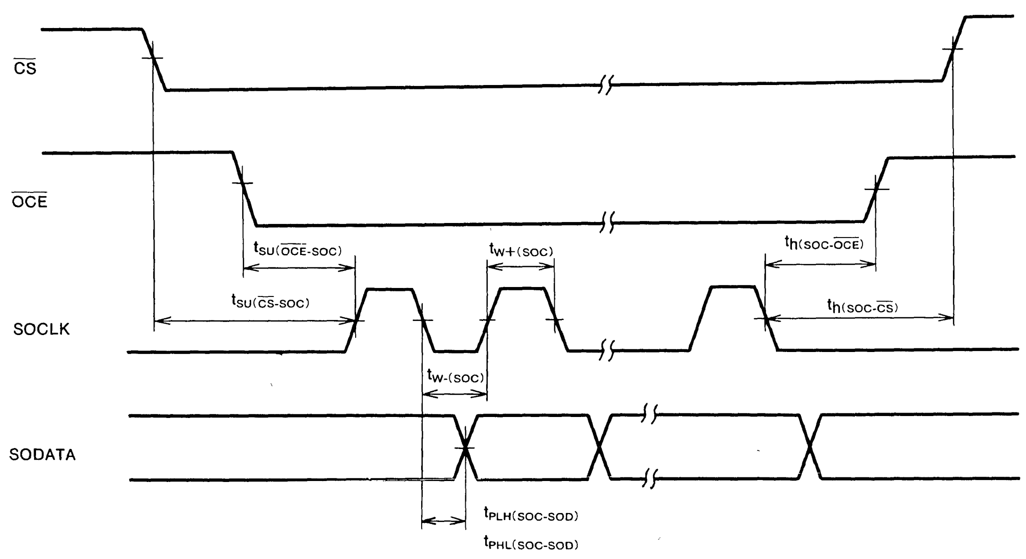
Note 3 : AC test waveform
Input pulse level 0~3V
Input pulse rise time 6ns
Input pulse fall time 6ns
Compare voltage Input voltage 1.3V
Output voltage 1.3V

TIMING DIAGRAM

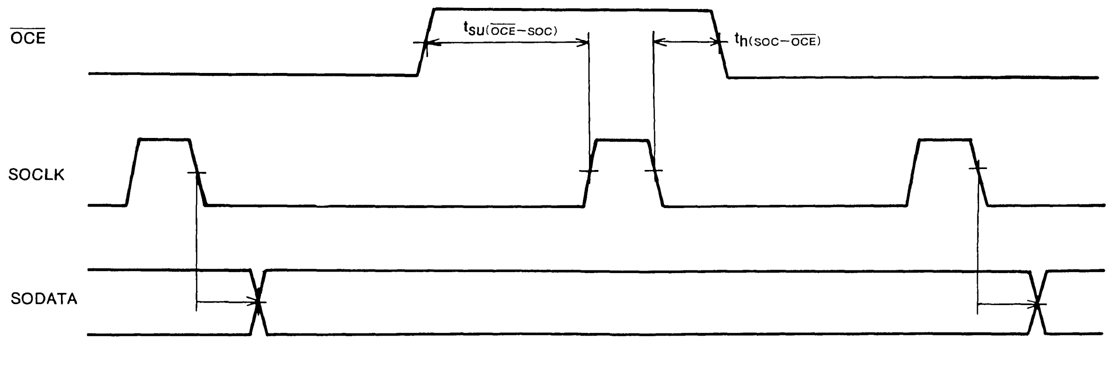


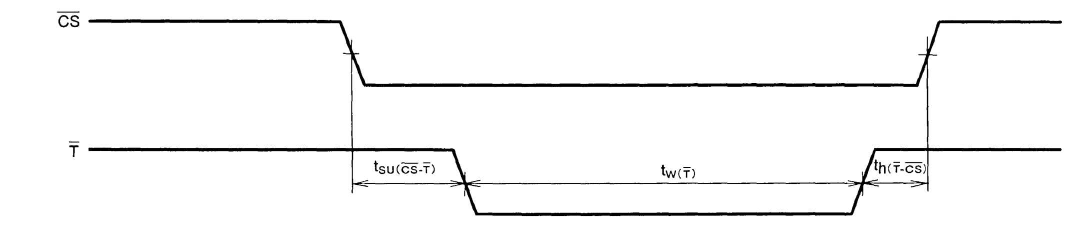


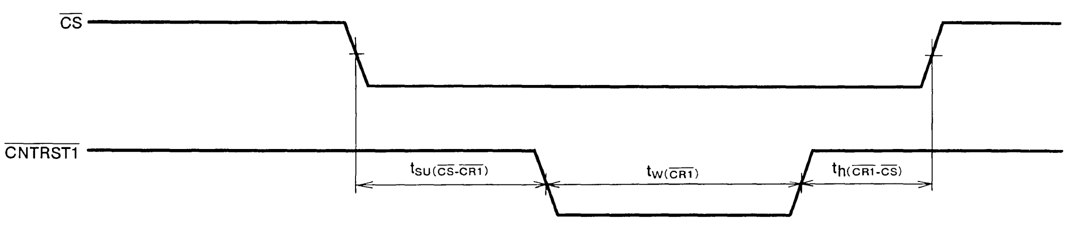
Note 4 : Timing that invalidates this clock

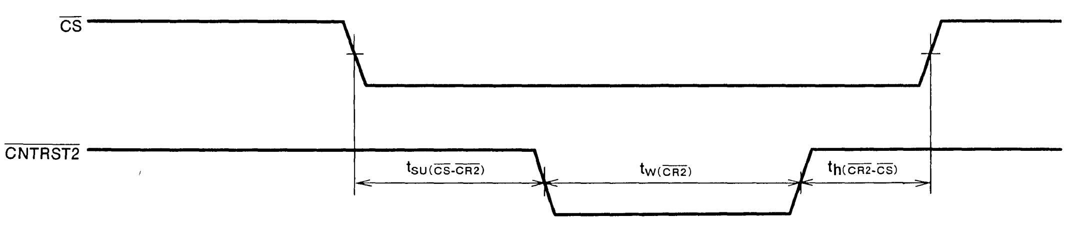


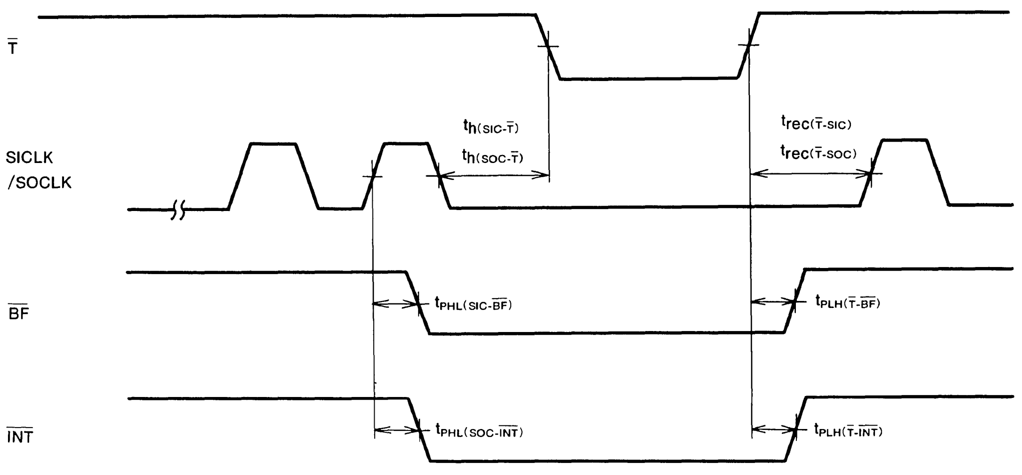
MITSUBISHI ELECTRIC

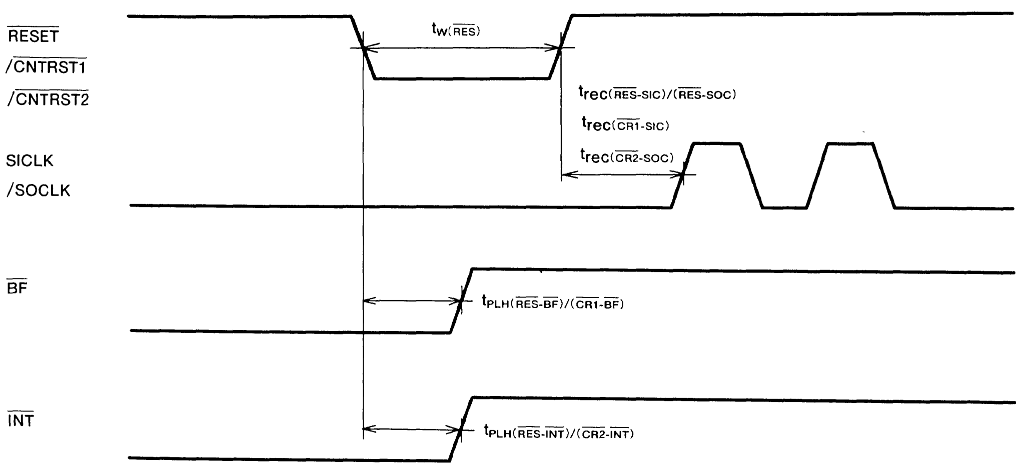

$\overline{OCE}$
$t_{su(\overline{OCE}-SOC)}$
$t_{h(SOC-\overline{OCE})}$
SOCLK
SODATA


$\overline{CS}$
$\overline{T}$
$t_{su(\overline{CS}-\overline{T})}$
$t_{w(\overline{T})}$
$t_{h(\overline{T}-\overline{CS})}$


$\overline{CS}$
$\overline{CNTRST1}$
$t_{su(\overline{CS}-\overline{CR1})}$
$t_{w(\overline{CR1})}$
$t_{h(\overline{CR1}-\overline{CS})}$

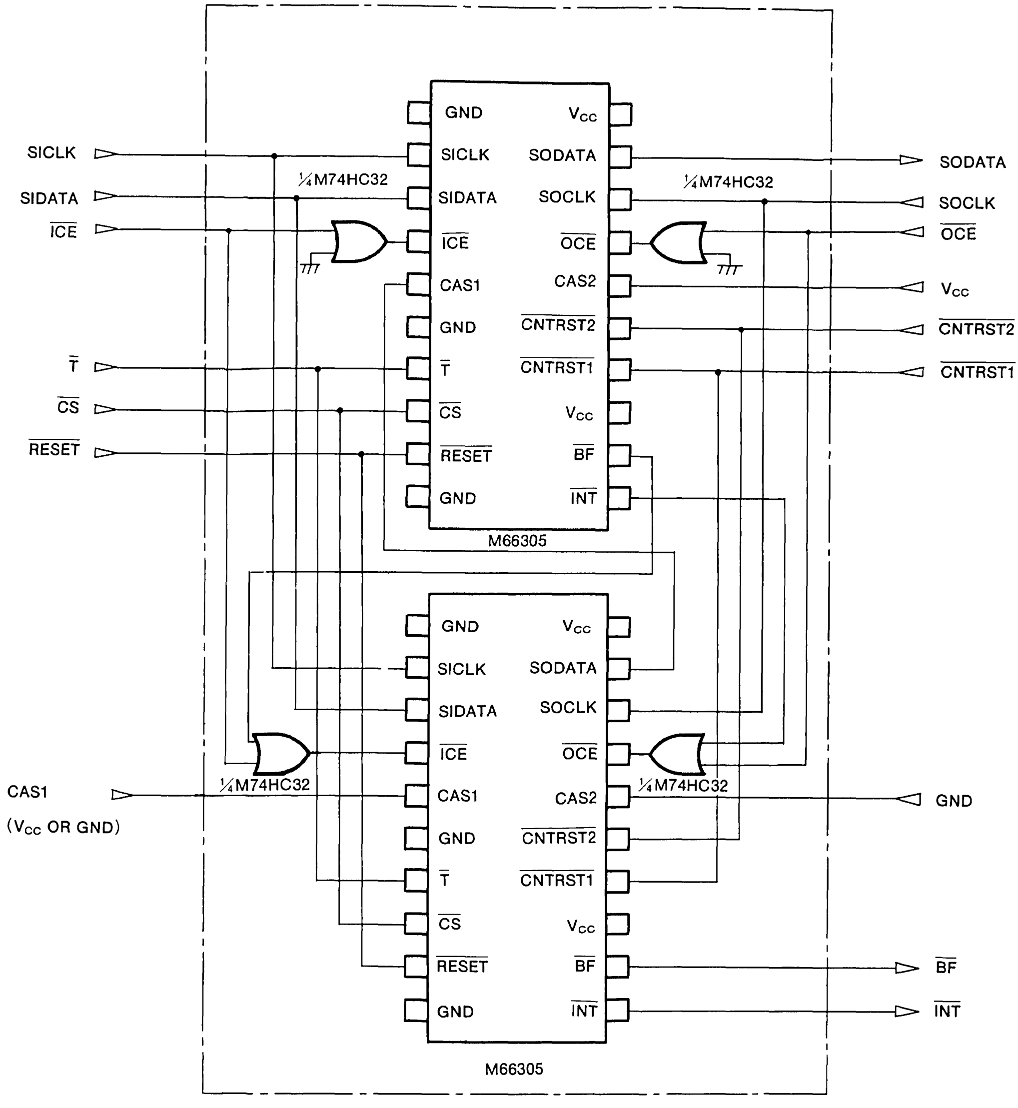

$\overline{CS}$
$\overline{CNTRST2}$
$t_{su(\overline{CS}-\overline{CR2})}$
$t_{w(\overline{CR2})}$
$t_{h(\overline{CR2}-\overline{CS})}$


T̄
SICLK
/SOCLK
B̄F̄
ĪN̄T̄
th(SIC-T̄)
th(SOC-T̄)
trec(T̄-SIC)
trec(T̄-SOC)
tPHL(SIC-B̄F̄)
tPLH(T̄-B̄F̄)
tPHL(SOC-ĪN̄T̄)
tPLH(T̄-ĪN̄T̄)


R̄ĒS̄ĒT̄
/C̄N̄T̄R̄S̄T̄1̄
/C̄N̄T̄R̄S̄T̄2̄
SICLK
/SOCLK
B̄F̄
ĪN̄T̄
tw(R̄ĒS̄)
trec(R̄ĒS̄-SIC)/(R̄ĒS̄-SOC)
trec(C̄R̄1̄-SIC)
trec(C̄R̄2̄-SOC)
tPLH(R̄ĒS̄-B̄F̄)/(C̄R̄1̄-B̄F̄)
tPLH(R̄ĒS̄-ĪN̄T̄)/(C̄R̄2̄-ĪN̄T̄)

APPLICATION EXAMPLE

2-stage Cascade connection (memory capacity (5, 120×2)×1 bit)



Note 5 : Output clock recovery time t_{rec} ($\overline{T}$-SOC) after toggle signal is required to have the following characteristics, if cascade connection is used and if one line length is 5, 125 bits (5, 120+5) or less : t_{rec} ($\overline{T}$−SOC)≧500ns
if cascade connection is used and if one line length is 5, 126 bits (5, 120+6) or more :
t_{rec} ($\overline{T}$−SOC)≧150ns

M66307SP/FP

SERIAL-OUTPUT LINE SCAN BUFFER WITH 16-BIT MPU BUS

DESCRIPTION

The M66307SP is an integrated circuit consisting of a line buffer with built-in static memory capable of storing an A3-size page at 400DPI, produced using a silicon gate CMOS process. The device performs serial conversion of data stored from 16-bit MPU bus, and outputs data at a transfer speed of 10Mbps maximum, or according to an external request clock, or in sync with any serial clock.

FEATURES

- 16-bit MPU bus compatible
- Data writing by MPU or DMAC.
- 320-word (5,120 bit) static RAM
- Maximum data output speed 10Mbps
- A fixed data of specified length can be added at the head of output data. (A fixed data, "H" or "L" level data)
- Selection of output types, FIFO or LIFO
- Choice of two output methods
  (1) In sync with an any continuous clock on the system side (ϕIN). In this case, the clock output (CLK OUT) can be selected in 5 divisions (1, 2, 4, 8, 16).
  (2) In sync with a data request clock on the peripheral equipment side
- Cascade connections
  (1) Toggle configuration
  (2) Applicable to 32-bit bus
- Low-noise and high-output circuit
  (CLK/ϕ IN OUT, DATA OUT) $I_O = \pm 24mA$
- Schmitt trigger for clock input (CLK/ϕ IN)
- Negative noise reduction circuit for ($\overline{RESET}$), ($\overline{WR}$) and ($\overline{TOG}$).

APPLICATION

General office automation equipments dealing with image processing

FUNCTION

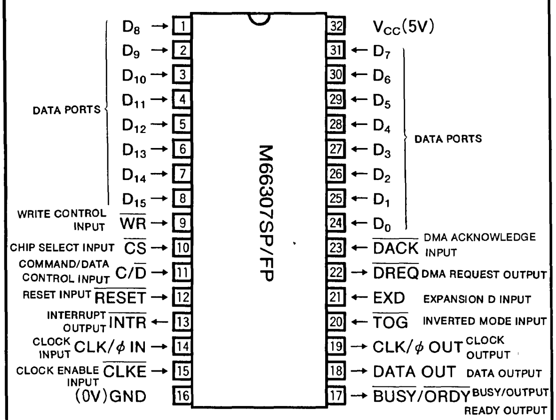
The M66307 outputs serial data from a system bus to peripheral equipment. The M66307 has an internal buffer of 320 words (5,120 bits); any number of words stored from the data bus can be sent out as serial data. The data is sent out in sync with any continuous clock (ϕ IN) on the system side or in sync with the data request clock (CLK IN).

The sending method can be programmed to output the MSB, LSB, FIFO (First-in First-out) or LIFO (Last-in First-out). The default settings are CLK IN, MSB and FIFO.

In addition to the basic function, M66307 can output the fixed data of a specified length before data output, store one-line "blank" data on a single command, and repeat the output of data stored in the line buffer.

The specifications are subject to change without notice.

PIN CONFIGURATION (TOP VIEW)

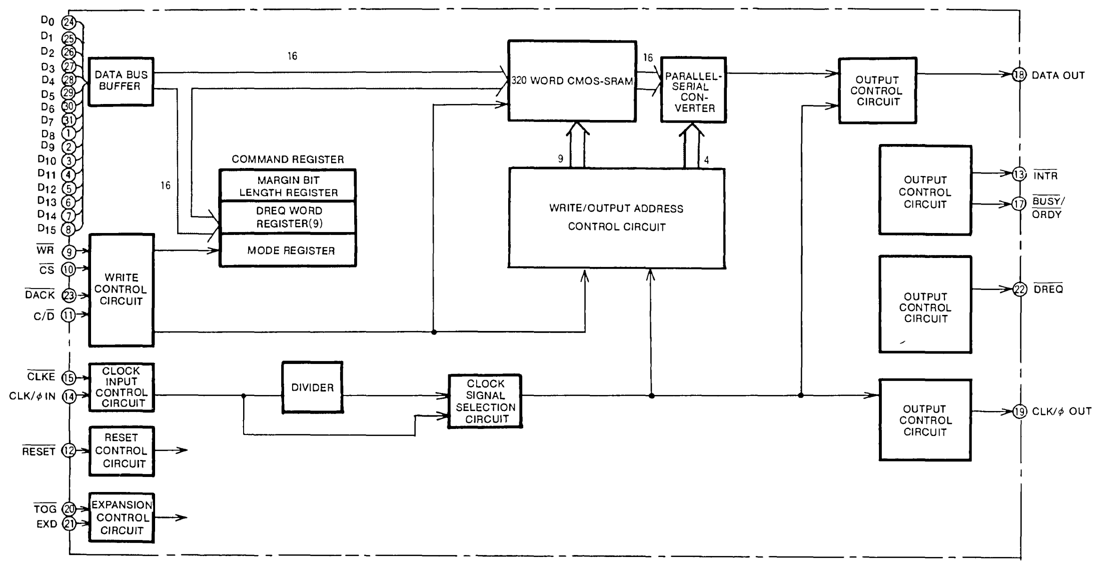


Outline 32P4B
32P2W

MITSUBISHI ELECTRIC

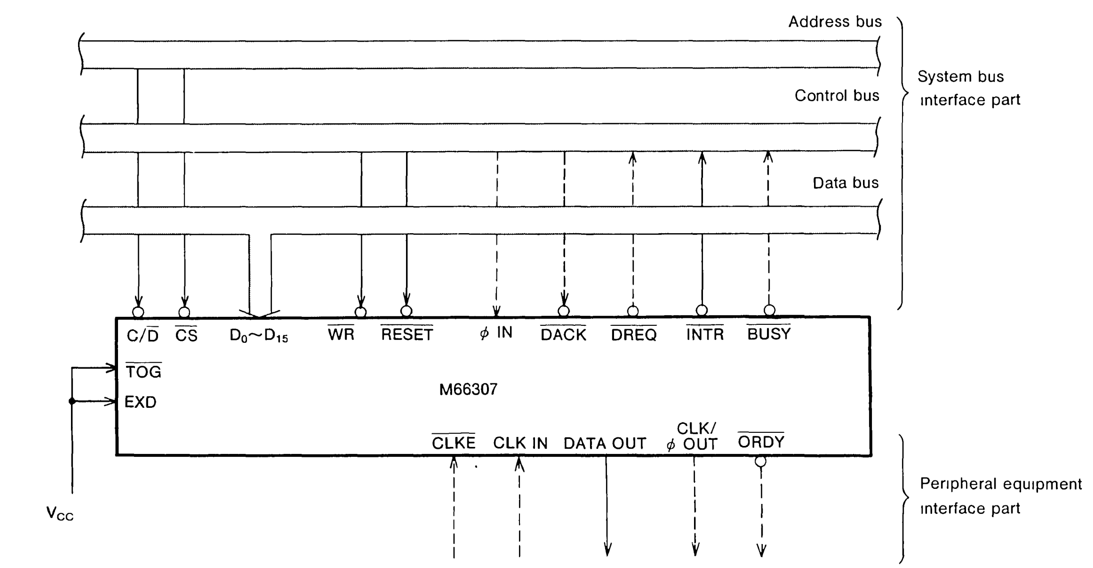
SERIAL-OUTPUT LINE SCAN BUFFER WITH 16-BIT MPU BUS

BLOCK DIAGRAM



Interface of the M66307

The M66307 has two interfaces, one on the system bus side and one on the peripheral equipment side. It outputs data up to 320 words long, read from the system bus side, to peripheral equipment in serial format.



Note : ● Make sure to pull-up low-level active input not used to V_{CC}.

Fig.1 M66307 interface to MPU system bus

APPLICATION SPECIFIC IC

4

M66300P/FP

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

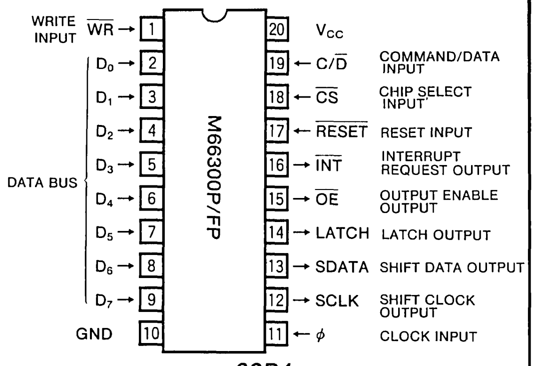
DESCRIPTION

The M66300P/FP is a CMOS-type large-scale integrated circuit with 63-byte FIFO (First-In First-Out Memory). Commands or data up to 63 bytes can be stored in directly from the 8-bit bus. The data stored in the FIFO can be output as serial data on command and, when output ends, an interrupt request signal is output. Having 2-bit output ($\overline{OE}$, LATCH) which can be set/reset by the command, M66300 can be connected to peripheral circuits that have a serial latch structure.

FEATURES

- General-purpose 8-bit CPU bus compatible
- Built-in 63-byte FIFO
- High-speed output (10Mbps)
- Direct connection to LED array driver such as M66310 or M66311
- Low-noise, high-output circuit
  I_{OL}=24mA, I_{OH}=−24mA
  (I_{OL}=4mA, I_{OH}=−4mA for $\overline{INT}$)
- TTL compatible inputs
  V_{IL}=0.8V max, V_{IH}=2.0V min
- Schmitt input ($\overline{RESET}$)
  Hysteresis 0.8V typ

PIN CONFIGURATION (TOP VIEW)

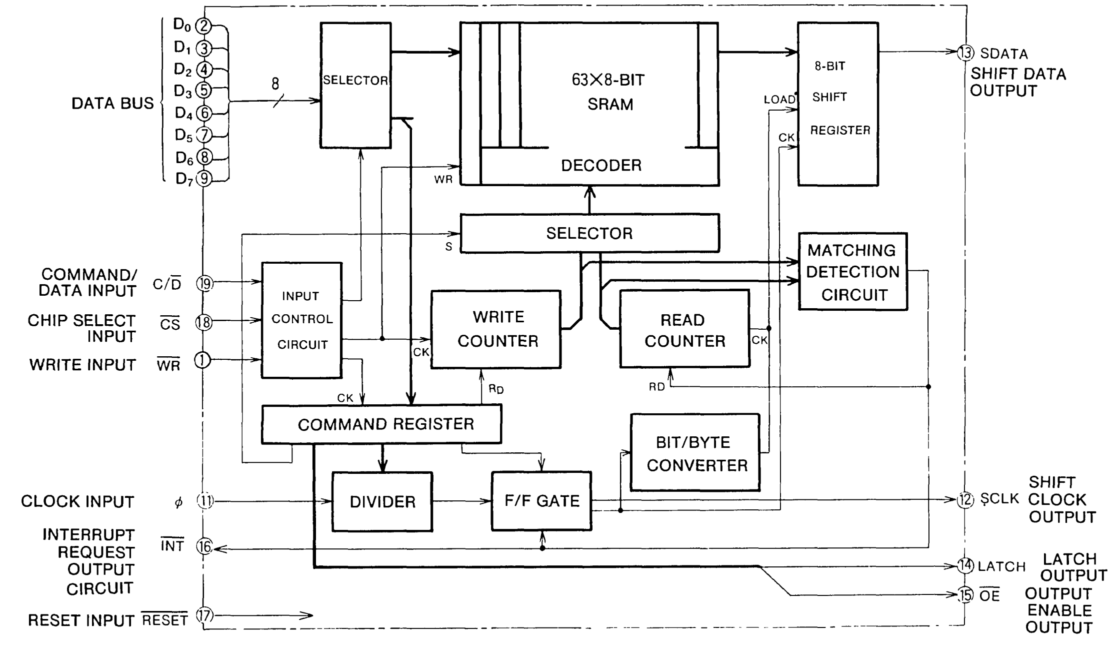


Outline 20P4
20P2

APPLICATION

General digital equipment for industrial and home use, panel display controllers, and eraser unit controller for copying machine.

BLOCK DIAGRAM



FUNCTION

The information on data bus $D_0 \sim D_7$ is considered as commands when $C/\overline{D}=1$, and as data when $C/\overline{D}=0$. There are four kinds of commands.

Command 1 sets division ratio for clock input ϕ and outputs as shift clock SCLK.

Command 2 sets the M66300 to write mode. The CPU is capable of writing 8-bit parallel data ($C/\overline{D}=0$) of up to 63 bytes into the internal memory (FIFO) of the M66300.

Command 3 sets the M66300 to serial output mode. All data written in the internal memory (FIFO) is output as serial data starting with the LSB, in sync with the clock, which is set by command 1.

When output ends, the interrupt request $\overline{INT}$ is output to the CPU.

Command 4 cancels the $\overline{INT}$ and sets/resets the two control ports (LATCH, $\overline{OE}$).

If command 3 is executed immediately after command 4, the same data is output again.

Table 1 Function table

Command	Inputs												Outputs					Remark	
	Control inputs				Data inputs														
	$\overline{R}$	$\overline{CS}$	$C/\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	SCLK	SDATA	$\overline{INT}$	$\overline{OE}$	LATCH		
—	0	×	×	×	×	×	×	×	×	×	×	×	0	0	1	1	0	Initialize	
—	1	1	×	×	×	×	×	×	×	×	×	×	*1	*1	*1	*2	*2	Memory contents not changed	
1	1	0	1	↑	1	0	0	0	×	×	×	×	0	0	1	1	0	ϕ	Valid when D_7 is high-level
					1	0	0	1					0	0	1	1	0	1/2 division of ϕ	
					1	0	1	0					0	0	1	1	0	1/4 division of ϕ	
					1	0	1	1					0	0	1	1	0	1/8 division of ϕ	
			↓	↓	1	1	0	0	↓	↓	↓	↓	0	0	1	1	0	1/16 division of ϕ	
2			1	↑	0	×	×	×	0	×	×	0	0	0	1	1	0	WRITE MODE setting	WRITE MODE
			0	↑	×	×	×	×	×	×	×	×	0	0	1	1	0	WRITE operation	
3		↓	1	↑	0	×	×	×	0	×	×	1	*3	*4	1	1	0	SERIAL OUT MODE setting	SERI. OUT MODE
		*5	×	×	×	×	×	×	×	×	×	×	*3	*4	1	1	0	SERIAL OUT	
		*5	×	×	×	×	×	×	×	×	×	×	0	0	0	1	0	SERIAL OUT end	
4	↓	0	1	↑	0	×	×	×	1	D2	D1	×	0	0	1	D2	D1	set/reset the $\overline{OE}$ and LATCH, cancel $\overline{INT}$	

Note 1 : *1 : The same operation as *3 and *4 in the SERIAL OUT mode. The output is not changed in other modes
*2 : The output is not chaged
*3 : The ϕ division pulse, which is set by command 1 is output on $\overline{WR}$ rise
*4 : SDATA (n) is output on SCLK fall (n−1).
*5 : Indicates 1 when WR is 0 Don't care when WR is 1.
× : Don't care

BASIC OPERATION

Fig. 1 shows the basic operation flowchart. On the C/$\overline{D}$ signal, data inputs $D_0 \sim D_7$ are switched among four commands and 8-bit parallel data. When C/$\overline{D}$ is 1, the command is stored on the rise of $\overline{WR}$.

First, command 1 is stored. Command 1 sets the division ratio for clock input ϕ as 5 divisions of 1, 1/2, 1/4, 1/8 and 1/16. (The default division is 1.)

Then command 2 is stored. When command 2 is stored, 8-bit parallel data is written into the internal memory (FIFO), up to 63 bytes on the write cycle of the CPU.

When the write operation ends, command 3 is stored, and all data written in the internal memory is output as serial data (SDATA), starting with the LSB, in sync with the shift clock (SCLK output), which is set by command 1.

The SDATA changes on the fall of SCLK. If data output ends, an interrupt request is output to the CPU.

$\overline{INT}$ is canceled by command 4 or by command 2 and 3. The command 4 sets/resets two control ports (LATCH, $\overline{OE}$) as well as canceling $\overline{INT}$.

If command 3 is executed without executing command 2 after Command 4, the same data is output again. If the repeat output is not required, return to command 2.

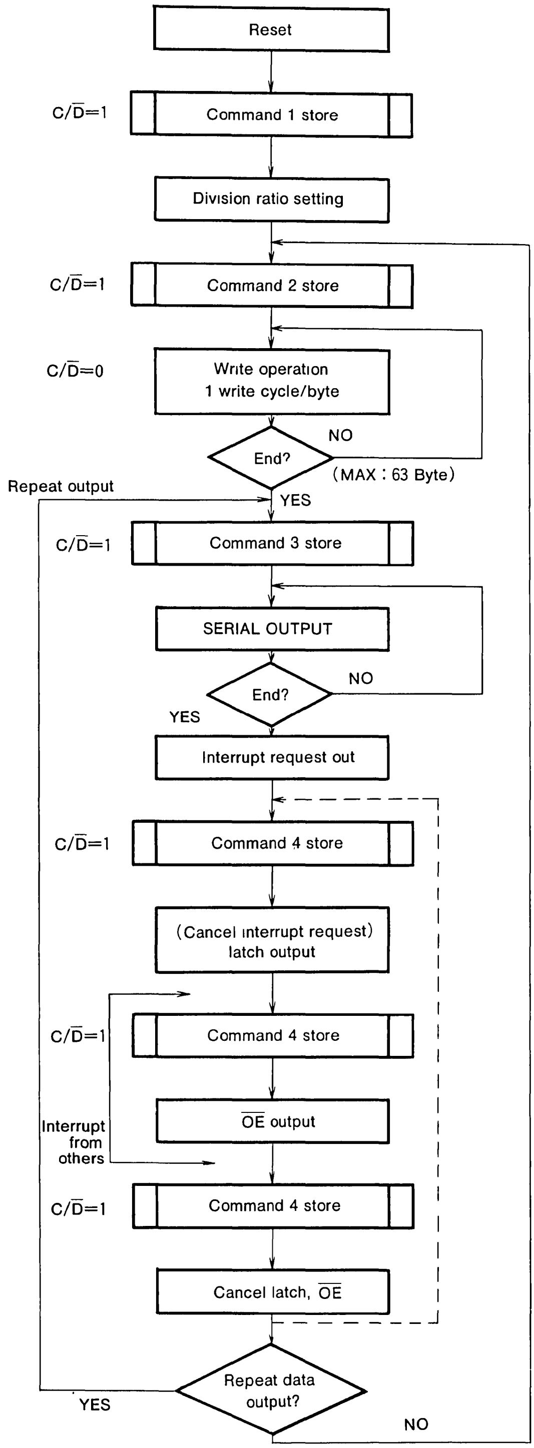


Fig. 1 Flowchart (Basic operation)

PIN DESCRIPTION

● $\overline{\text{RESET}}$ (Reset input)

When this is low-level, it clears the command and shift register and initializes the address of the internal memory (FIFO).

● ϕ (Clock input)

When the frequency of clock input ϕ is f_O, the frequency f of shift clock output SCLK is given by the following equation.

$$f=(1/n) \cdot f_O \quad (n=1, 2, 4, 8, 16)$$

● $\overline{\text{CS}}$ (chip select input)

When this is low-level, communication between the M66300 and the CPU becomes possible. When this is high-level, data from the CPU is ignored. However, data in the internal memory is maintained. In the serial output mode, data output operation continues and, as soon as it ends, an interrupt request instruction $\overline{\text{INT}}$ is output. ($\overline{\text{INT}}$ can be canceled only when $\overline{\text{CS}}$ is low-level.) In other modes, output is maintained as it is.

● C/$\overline{\text{D}}$ (Command/data input)

The information on $D_0 \sim D_7$ is regarded as commands when this is high-level and is regarded as data when this is low-level.

● $\overline{\text{WR}}$ (Write input)

On $\overline{\text{WR}}$ rise, a command from the CPU is written into the command register and data is written into the internal memory. This input generates the serial data start signal, cancels $\overline{\text{INT}}$, and sets the 2-bit control ports (LATCH, $\overline{\text{OE}}$).

● SCLK (Shift clock output)

The clock frequency is determined by $D_6 \sim D_4$ when D_7 is 1, as shown in Table 2 and Fig. 2. Clock output starts on $\overline{\text{WR}}$ rise of command 3.

● SDATA (Shift data output)

All data written in the internal memory are output as serial data in sync with the SCLK.

● $\overline{\text{INT}}$ (Interrupt request output)

When output of all data in the internal memory ends, a low-level signal is output.

● LATCH (Latch output)

● $\overline{\text{OE}}$ (Output enable output)

These two outputs are set/reset by command 4 on $\overline{\text{WR}}$ rise. The signal was named after the IC (ex. M66310 or M66311) connected in the next stage, but it can be used freely for other applications.

INSTRUCTION SET

Four commands can be set by the 8-bit command words from the CPU.

1) Command 1 — $80_{16} \sim C0_{16}$ (Note 2)
   Division ratio setting
2) Command 2 — 00_{16} (Note 3)
   Write mode from the CPU to the internal memory is set.
3) Command 3 — 01_{16} (Note 3)
   Data output mode from the internal memory (FIFO) is set.
4) Command 4 — $08_{16} \sim 0F_{16}$ (Note 3)
   Cancels the $\overline{\text{INT}}$ and sets the two control ports (LATCH, $\overline{\text{OE}}$). (Note 4)

Note 2 : Lower byte can be 0~F.
3 : Upper byte can be 1~7.
4 : $\overline{\text{INT}}$ can also be canceled by command 2 or 3.

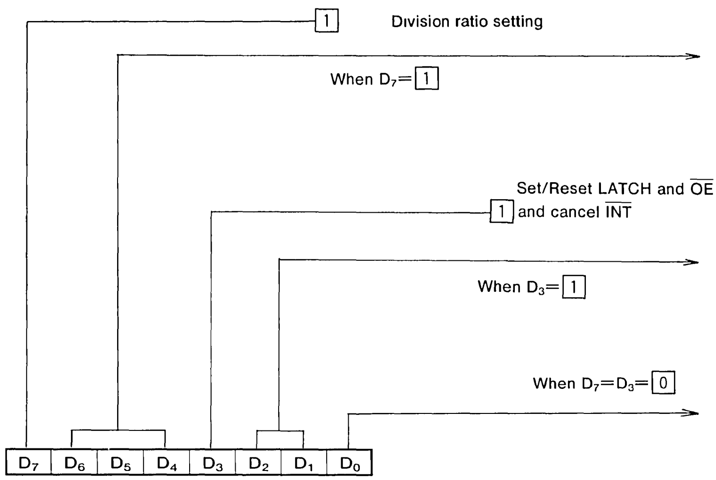
Fig. 2 shows the method for determining the command word for the instruction set. When D_7 is 1, $D_3 \sim D_0$ are masked and when D_3 is 1, D_0 is masked.

Table 2 Division ratio setting

$D_7 \sim D_4$	Division
8_{16}	ϕ
9_{16}	1/2 of ϕ
A_{16}	1/4 of ϕ
B_{16}	1/8 of ϕ
C_{16}	1/16 of ϕ

Table 3 $\overline{\text{OE}}$, LATCH setting

$D_3 \sim D_0$	$\overline{\text{OE}}$	LATCH	$\overline{\text{INT}}$ cancellation
8_{16}, 9_{16}	0	0	canceled
A_{16}, B_{16}	0	1	↓
C_{16}, D_{16}	1	0	↓
E_{16}, F_{16}	1	1	↓



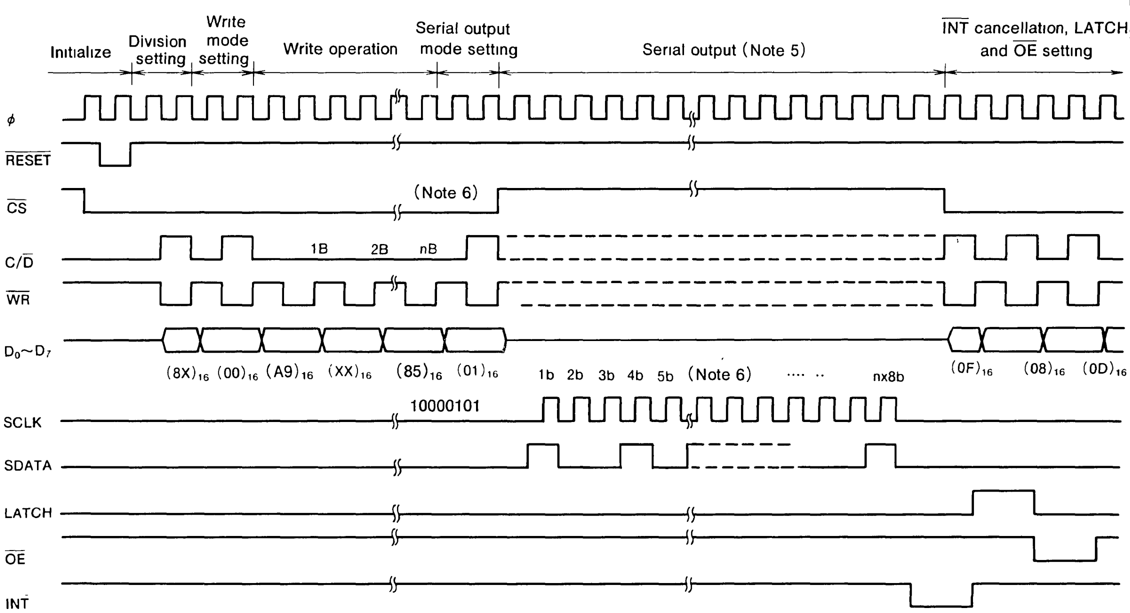
D_6	D_5	D_4	Division ratio
0	0	0	ϕ
0	0	1	1/2 of ϕ
0	1	0	1/4 of ϕ
0	1	1	1/8 of ϕ
1	0	0	1/16 of ϕ

D_2	D_1	$\overline{OE}$	LATCH
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

D_0	Mode setting
0	WRITE
1	SERIAL OUT

Fig. 2 Instruction set

EXAMPLE OF TIME CHART



Note 5 : Always maintain $\overline{WR}$ at high-level when $\overline{CS}$ is low-level
6 : B.=Byte, b =bit
7 : ϕ need not be the CPU signal (ϕ and $\overline{WR}$ need not be synchronous.)
8 : ϕ indicates the value when division ratio is set 1 If the division ratio is other than 1, a similar time chart is obtained if ϕ is regarded as the waveform divided

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+V_{CC}+0.5	V
V_O	Output voltage		−0.5∼+V_{CC}+0.5	V
P_d	Power dissipation		500	mW
Tstg	Storage temperature		−65 ∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
GND	Supply voltage			0		V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−10		75	℃

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, V_{CC}=5 V±10%, GND=0 V)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage		Inputs other than $\overline{RESET}$		2	1.4		V
V_{IL}	Low-level input voltage		Inputs other than $\overline{RESET}$			1.4	0.8	V
V_{T+}	Positive input threshold voltage		$\overline{RESET}$			1.8	2.4	V
V_{T-}	Negative input threshold voltage		$\overline{RESET}$		0.6	1.0		V
$V_{T+}-V_{T-}$	Hysteresis width		$\overline{RESET}$		0.2	0.8		V
V_{OH}	High-level output voltage	$\overline{INT}$		I_{OH}=−4 mA	V_{CC}−0.80	V_{CC}−0.30		V
		Output pin other than $\overline{INT}$		I_{OH}=−24mA		V_{CC}−0.40		
V_{OL}	Low-level output voltage	$\overline{INT}$		I_{OL}=4 mA		0.10	0.53	V
		Output pin other than $\overline{INT}$		I_{OL}=24mA		0.25		
I_{CC}	Supply current		V_I=V_{CC} or GND			20	50	mA
I_{IH}	High-level input current		V_I=V_{CC}			0.0	+1	μA
I_{IL}	Low-level input current		V_I=0 V			0.0	−1	μA
C_I	Input capacitance					5	10	pF

Note 9 : The current flowing into the IC is positive (no sign)

TIMING REQUIREMENTS (T_a=−10～+75℃, V_{CC}= 5 V±10%, GND= 0 V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi)}$	Clock pulse width		50	20		ns
$t_{w(\overline{W})}$	Write pulse width		100	30		ns
$t_{w(\overline{R})}$	Reset pulse width		100	5		ns
$t_{su(D-\overline{W})}$	Data setup time before write		50	15		ns
$t_{h(\overline{W}-D)}$	Data hold time after write		0	−15		ns
$t_{su(A-\overline{W})}$	Address setup time before write		0	$30-t_w(\overline{W})$		ns
$t_{h(\overline{W}-A)}$	Address hold time after write		0	−25		ns
$t_{rec(\overline{W})}$	Write recovery time		100	$35-t_w(\overline{W})$		ns
$t_{rec(\overline{INT}-\overline{W})}$	Write recovery time after $\overline{INT}$		100	0 or less		ns
$t_{rec(\overline{R}-\overline{W})}$	Write recovery time after reset		100	—		ns

Note 10 : Increase of the input rise time (t_r) and fall time (t_f) of clock input ϕ may cause misoperation
t_r, t_f : These are recommended to be 20ns or less

SWITCHING CHARACTERISTICS (T_a=−10～+75℃, V_{CC}= 5 V±10%)

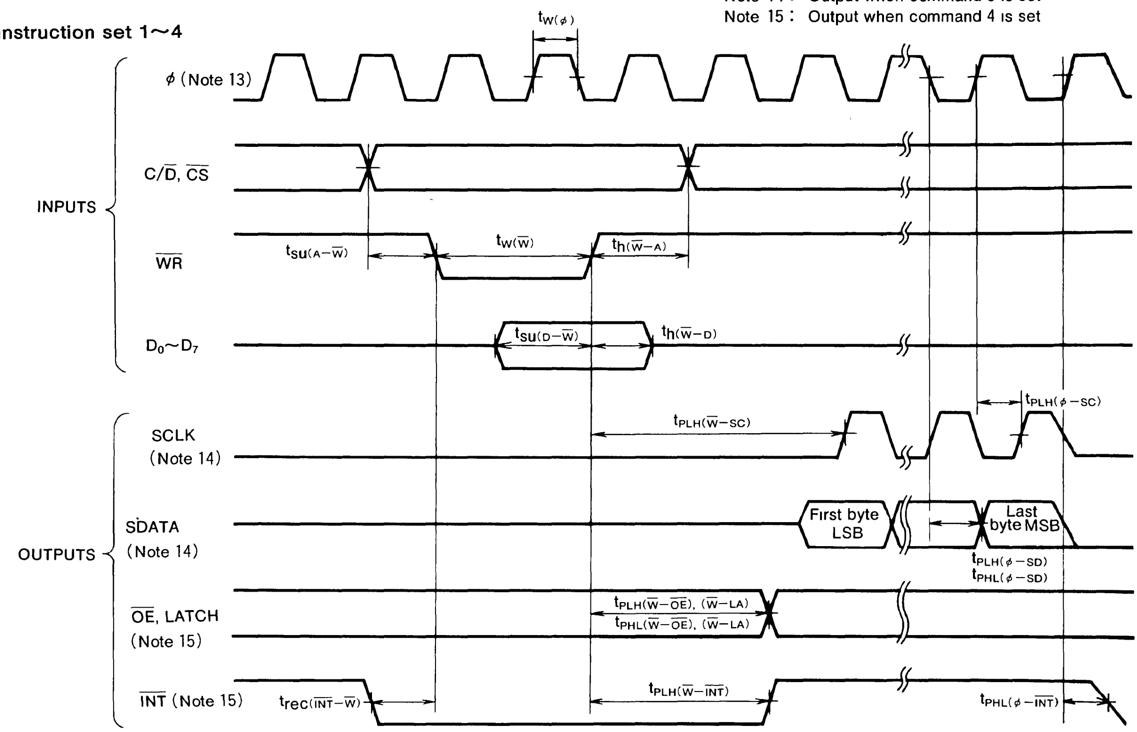
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{max(\phi)}$	Maximum repetitive frequency		10	30		MHz
$t_{PLH(\overline{W}-\overline{INT})}$	Propagation time between write and $\overline{INT}$	C_L= 50pF		30	100	ns
$t_{PHL(\overline{R}-\overline{INT})}$	Propagation time between $\overline{RESET}$ and $\overline{INT}$	C_L= 50pF		20	100	ns
$t_{PLH(\overline{W}-\overline{OE})}$	Propagation time between write and $\overline{OE}$	C_L=150pF		20	100	ns
$t_{PHL(\overline{W}-\overline{OE})}$	Propagation time between write and $\overline{OE}$	C_L=150pF		25	100	ns
$t_{PLH(\overline{W}-LA)}$	Propagation time between write and LATCH	C_L=150pF		20	100	ns
$t_{PHL(\overline{W}-LA)}$	Propagation time between write and LATCH	C_L=150pF		25	100	ns
$t_{PLH(\overline{W}-SC)}$	Propagation time between write and SCLK	C_L=150pF	1 XT	—	2 XT+100	ns
$t_{PLH(\phi-SC)}$	Propagation time between ϕ and SCLK	C_L=150pF		35	100	ns
$t_{PLH(\phi-SD)}$	Propagation time between ϕ and SDATA	C_L=150pF		30	100	ns
$t_{PHL(\phi-SD)}$	Propagation time between ϕ and SDATA	C_L=150pF		30	100	ns
$t_{PHL(\phi-\overline{INT})}$	Propagation time between ϕ and $\overline{INT}$	C_L=150pF		30	100	ns
$t_{PLH(\overline{R}-\overline{OE})}$	Propagation time between $\overline{RESET}$ and $\overline{OE}$	C_L=150pF		20	100	ns
$t_{PHL(\overline{R}-LA)}$	Propagation time between $\overline{RESET}$ and LATCH	C_L=150pF		25	100	ns
t_{TLH}	Low-to high-level output transition time ($\overline{INT}$)	C_L= 50pF		10	25	ns
t_{THL}	High-to low-level output transition time ($\overline{INT}$)	C_L= 50pF		6	25	ns
t_{TLH}	Low-to high-level output transition time (SCLK, SDATA, $\overline{OE}$, LATCH)	C_L=150pF		10	25	ns
t_{THL}	High-to low-level output transition time (SCLK, SDATA, $\overline{OE}$, LATCH)	C_L=150pF		7	25	ns

Note 11 : $T=(1/\phi(f_O))\times(1/\text{division ratio})$ns
12 : AC test waveform
Input pulse level 0～3V
Input pulse rise time 6ns
Input pulse fall time 6ns
Reference voltage
Input voltage 1.3V
Output voltage 1.3V

TIMING DIAGRAM

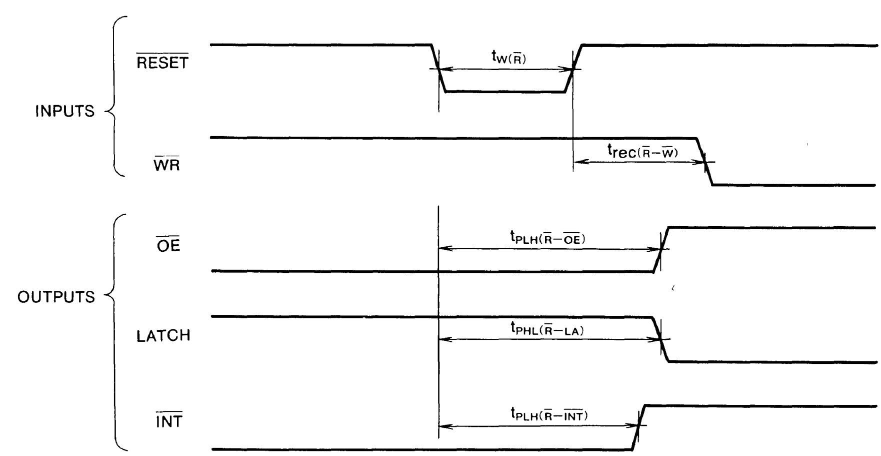
Note 14 : Output when command 3 is set
Note 15 : Output when command 4 is set

Instruction set 1~4

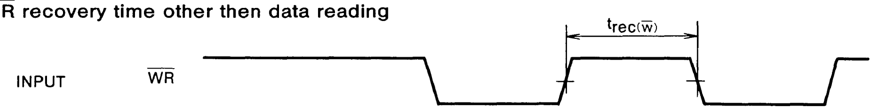


Note 13 : The timing diagram when division ratio is set (1/2, 1/4, 1/8, 1/16) is regarded as the waveform as divided by φ There are specific φ inputs for switching from each φ state.

Timing diagram when RESET



WR recovery time other then data reading



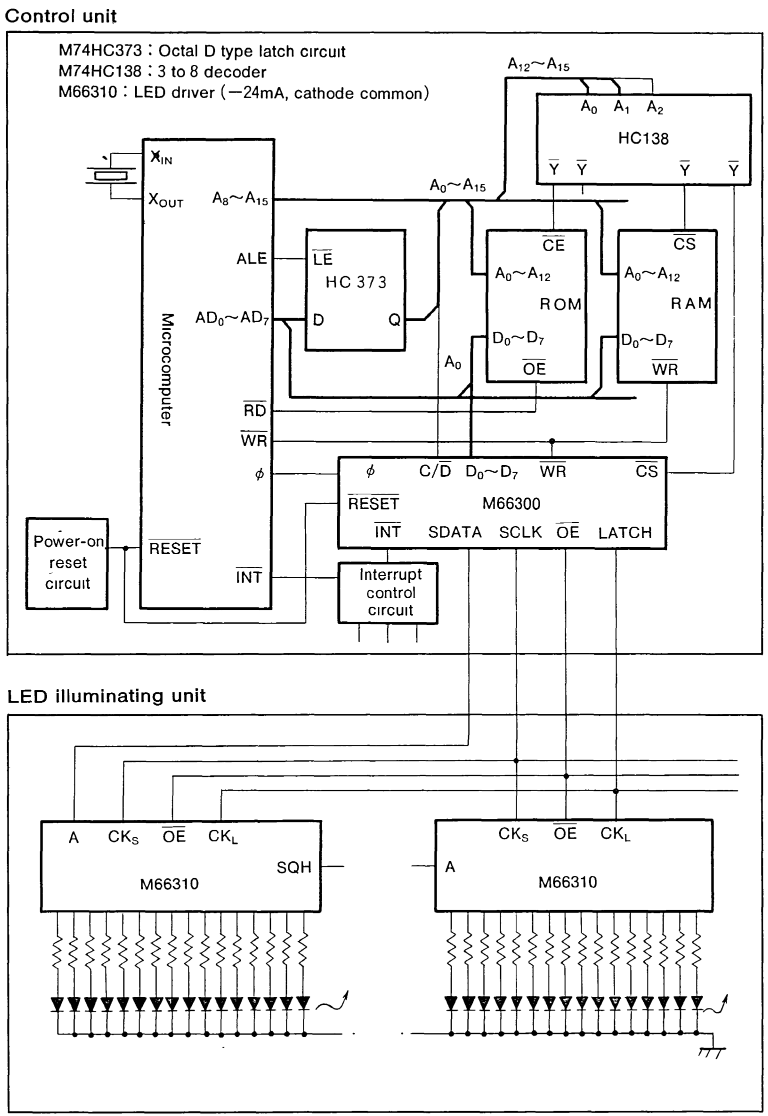


Fig. 3 Application example 1 (PPC copying machine eraser circuit)

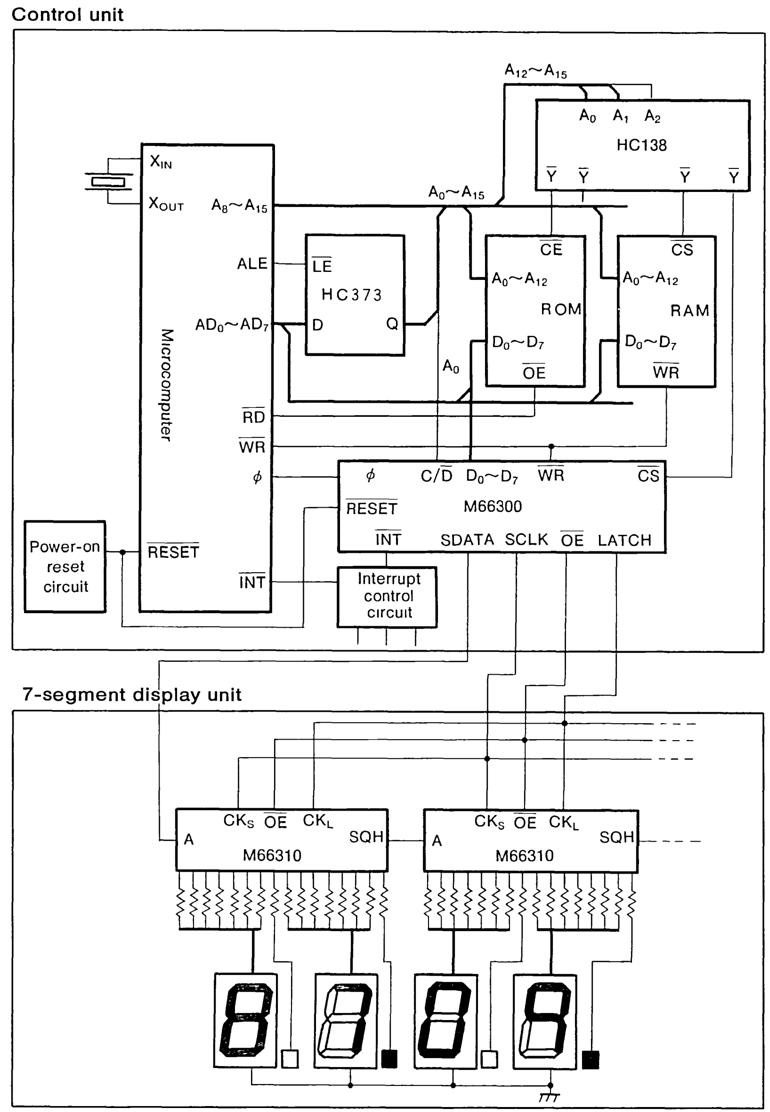
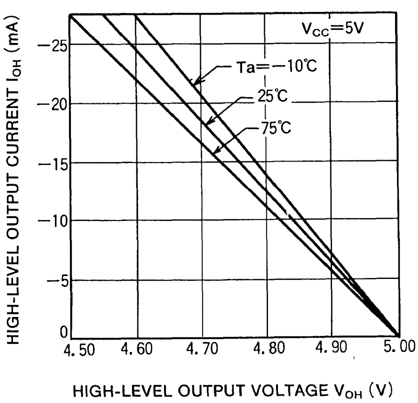


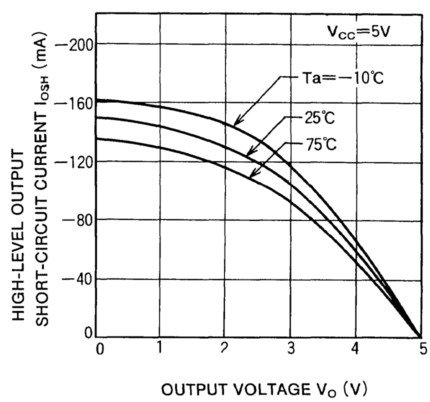
Fig. 4 Application example 2 (Panel display circuit)

TYPICAL CHARACTERISTICS (24mA OUTPUT PIN)

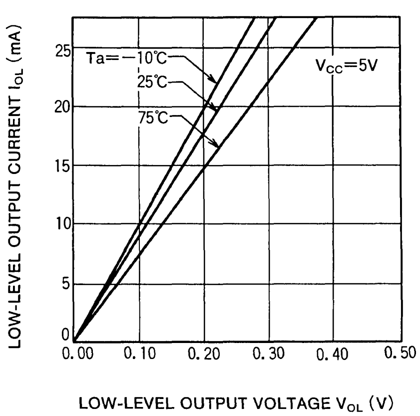
I_{OH} VS V_{OH}



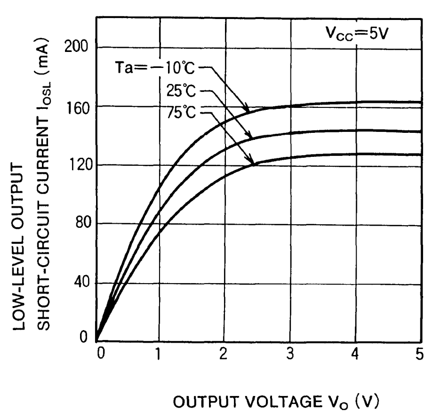
I_{OSH} VS V_O



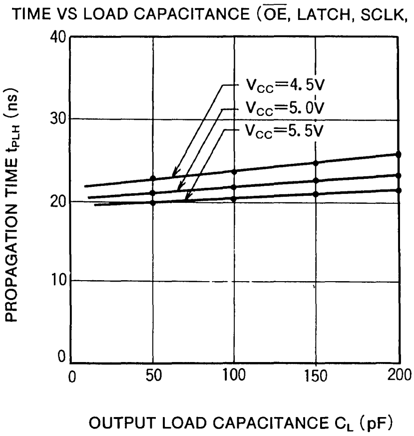
I_{OL} VS V_{OL}



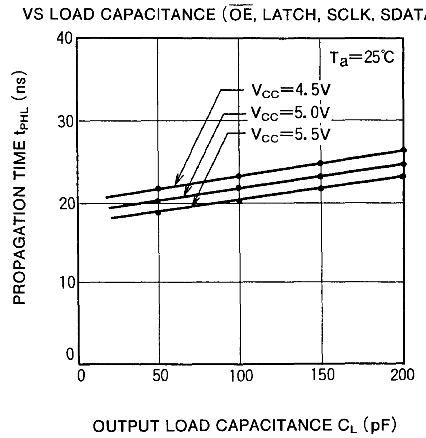
I_{OSL} VS V_O



LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE ($\overline{OE}$, LATCH, SCLK, SDATA)



HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION TIME VS LOAD CAPACITANCE ($\overline{OE}$, LATCH, SCLK, SDATA)



M66310P/FP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

M66310P/FP is a LED array driver having a 16bit serial-input and parallel output shiftregister function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24mA which is sufficient for cathode common LED drive, capable of flowing 16bits continuously at the same time.

Parallel output is open drain output.

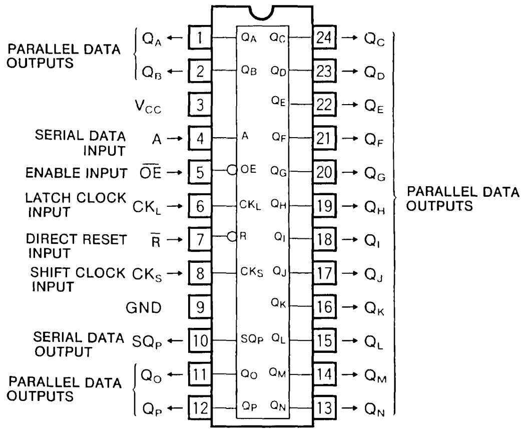
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin lay-out ensures the realization of an easy printed circuit.

FEATURES

- Cathode common LED drive
- High output current
  all parallel output $I_{OH}=-24mA$
  simultaneous lighting available
- Low power dissipation : 100μW/package (max)
  (V_{CC}=5V, Ta=25℃, quiescent state)
- High noise margin
  schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output
  (except serial data output)
- Wide operating temperature range
  : Ta=−40~+85℃
- Pin lay-out facilitates printed circuit wiring. (This lay-out facilitates cascade connection and LED connection.)

PIN CONFIGURATION (TOP VIEW)

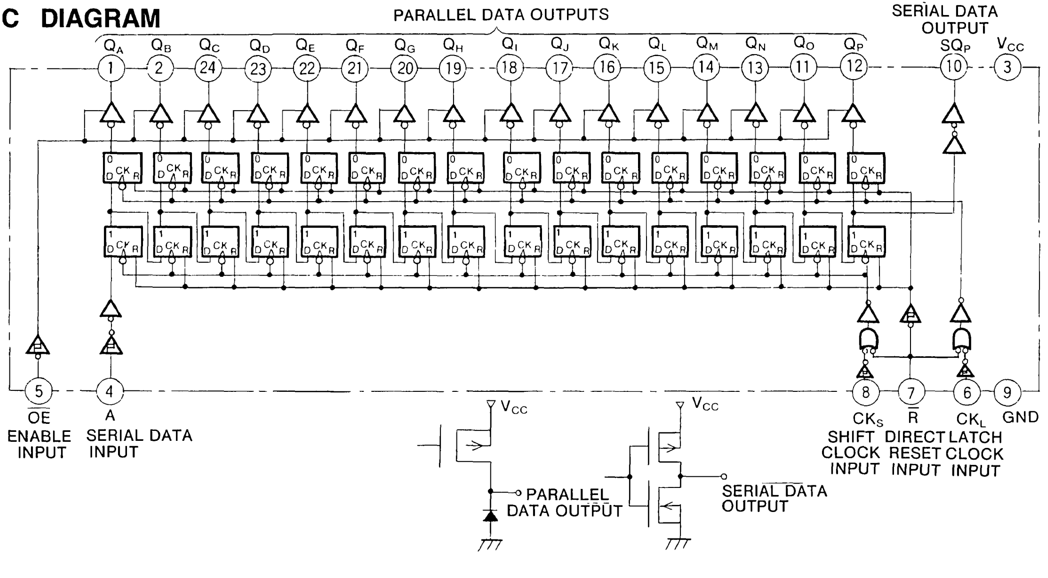


Outline 24P4D
24P2

APPLICATION

LED array drive of BUTTON TELEPHONE
LED array drive of ERASER of a PPC copier
Other various LED modules

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

As M66310P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CKs and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S. When A is "L", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from $Q_A \sim Q_P$.

Outputs from $Q_A \sim Q_P$ are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to $Q_A \sim Q_P$.

When reset input $\overline{R}$ is changed to "L", $Q_A \sim Q_P$ and SQ_P are reset. In this case, shifting and latching registers are reset.

If "H" is impressed to output enable input $\overline{OE}$, $Q_A \sim Q_P$ reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

FUNCTION TABLE (Note : 1)

Operation mode		Input					PARALLEL DATA Output																Serial data output SQP	Remarks
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	Q_I	Q_J	Q_K	Q_L	Q_M	Q_N	Q_O	Q_P		
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	—
Shift latch operation	Shift t1	H	$\uparrow$	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	Q_P^0	q_O^0	Output lighting "H"
	Latch t2	H	X	$\uparrow$	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
	Shift t1	H	$\uparrow$	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	Q_P^0	q_O^0	Output lights-out "L"
	Latch t2	H	X	$\uparrow$	X	L	Z	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_P	—

Note 1 : $\uparrow$: Change from low-level to high-level
Q^0 : Output state Q before CK_L changed
X : Irrelevant
q^0 : Contents of shift register before CK_S changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (Ta=−40～+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7.0	V
V_I	Input voltage			−0.5～V_{CC}+0.5	V
V_O	Output voltage			−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current per output pin	Q_A～Q_P		−50	mA
		SQ_P		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	−410, +20	mA
Pd	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65～+150	℃

Note 2 : M66310FP, T_a=−40～+70℃, T_a=70～85℃ are derated at −6mW/℃

RECOMMENDED OPERATING CONDITIONS (Ta=−40～+85℃)

Symbol	Parameter	Limits Min	Typ*	Max	Unit
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5～5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Ta=25℃ Min	Ta=25℃ Typ	Ta=25℃ Max	Ta=−40～+85℃ Min	Ta=−40～+85℃ Max	Unit
V_{T+}	Positive-going threshold voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		0.35×V_{CC}		0.7×V_{CC}	0.35×V_{CC}	0.7×V_{CC}	V
V_{T-}	Negative-going threshold voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		0.2×V_{CC}		0.55×V_{CC}	0.2×V_{CC}	0.55×V_{CC}	V
V_{OH}	High-level output voltage Q_A～Q_P	V_I=V_{T+}, V_{T-}, V_{CC}=4.5V	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−24mA	3.83			3.66		
		Note3	I_{OH}=−40mA	3.50			3.25		
V_{OH}	High-level output voltage SQ_P	V_I=V_{T+}, V_{T-}, V_{CC}=4.5V	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−4mA	3.83			3.66		
V_{OL}	Low-level output voltage SQ_P	V_I=V_{T+}, V_{T-}, V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=4mA			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}, V_{CC}=5.5V				0.5		5.0	μA
I_{IL}	Low-level input current	V_I=GND, V_{CC}=5.5V				−0.5		−5.0	μA
I_O	Maximum output leakage current Q_A～Q_P	V_I=V_{T+}, V_{T-}, V_{CC}=5.5V	V_O=V_{CC}			1.0		10.0	μA
			V_O=GND			−1.0		−10.0	
I_{CC}	Quiescent supply current	V_I=V_{CC}, GND, V_{CC}=5.5V				20.0		200.0	μA

Note 3 : M66310 is used under the condition of an output current I_{OH}=−40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle—I_{OH} of Standard characteristics

SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency		5			4		MHz
t_{PLH}	Low-level to high-level and high-level to low-level				100		130	ns
t_{PHL}	output propagation time (CK_S-SQ_P)				100		130	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$-SQ_P)	C_L=50pF			100		130	ns
t_{PHZ}	High-level to low-level output propagation time ($\overline{R}$-Q_A~Q_P)	R_L= 1 kΩ			150		200	ns
t_{PZH}	Low-level to high-level and high-level to low-level	(Note 5)			100		130	ns
t_{PHZ}	output propagation time (CK_L−Q_A~Q_P)				150		200	ns
t_{PZH}	Output enable time to low-level and high-level				100		130	ns
t_{PHZ}	($\overline{OE}$−Q_A~Q_P)				150		200	ns
C_I	Input Capacitance				10		10	pF
C_O	Output Capacitance	$\overline{OE}$=V_{CC}			15		15	pF
C_{PD}	Power dissipation Capacitance (Note 4)			11				pF

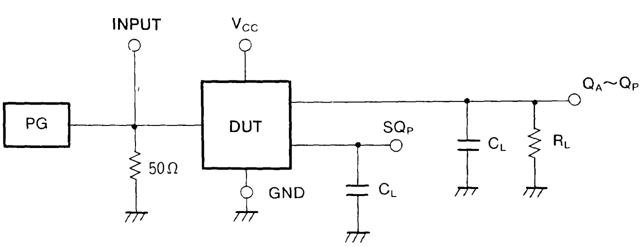
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
t_W	CK_S, CK_L, $\overline{R}$ pulse width		100			130		ns
t_{su}	A setup time with respect to CK_S		100			130		ns
t_{su}	CK_S setup time with respect to CK_L	(Note 5)	100			130		ns
t_h	A hold time with respect to CK_S		10			15		ns
t_{rec}	$\overline{R}$, recovery time with respect to CK_S, CK_L		50			70		ns

Note 5 : Test Circuit

Note 5 : Test Circuit

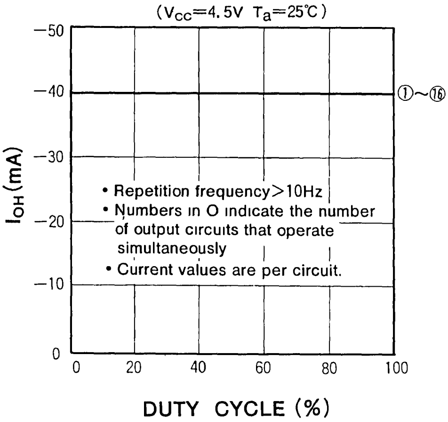


(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr =6ns, tf=6ns

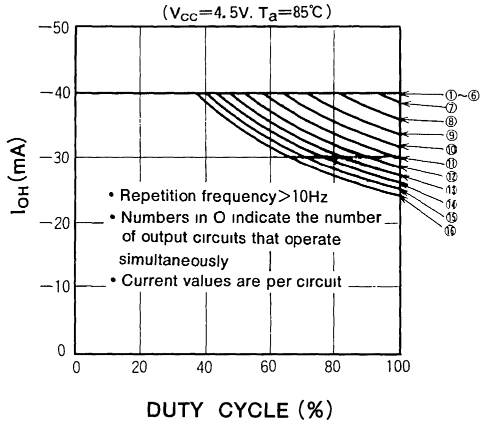
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

STANDARD CHARACTERISTICS

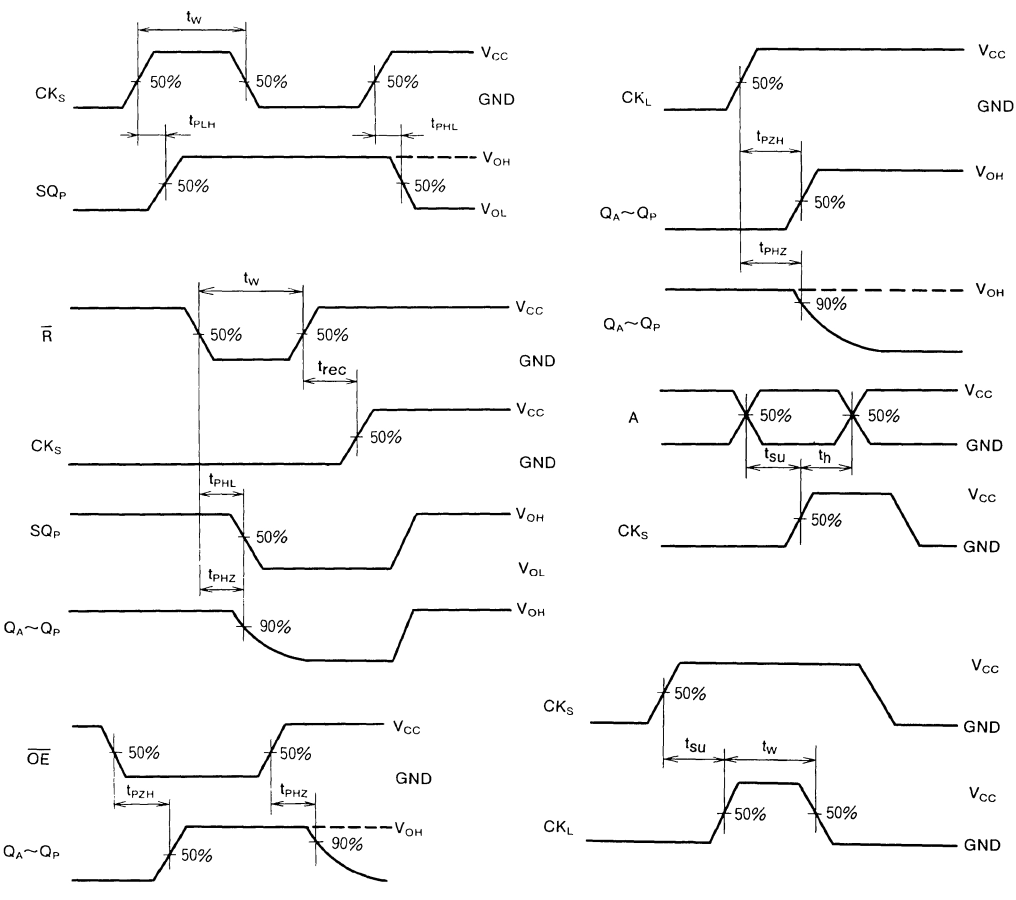
DUTY CYCLE—I_{OH} CHARACTERISTICS
(V_{CC}=4.5V T_a=25℃)



DUTY CYCLE—I_{OH} CHARACTERISTICS
(V_{CC}=4.5V. T_a=85℃)



TIMING DIAGRAM



M66311P/FP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

M66311P/FP is a LED array driver having a 16bit serial-input and parallel output shiftregister function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24mA which is sufficient for anode common LED drive, capable of flowing 16bits continuously at the same time.

Parallel output is open drain output.

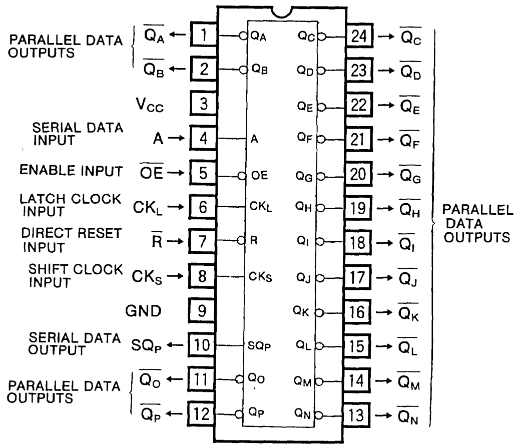
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin lay-out ensures the realization of an easy printed circuit.

FEATURES

- Anode common LED drive
- High output current
  all parallel output $I_{OL}=24mA$
  simultaneous lighting available
- Low power dissipation : 100μW/package (max)
  ($V_{CC}=5V$, $Ta=25°C$, quiescent state)
- High noise margin
  schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output
  (except serial data output)
- Wide operating temperature range
  : $Ta=-40\sim+85°C$
- Pin lay-out facilitates printed circuit wiring. (This lay-out facilitates cascade connection and LED connection.)

PIN CONFIGURATION (TOP VIEW)

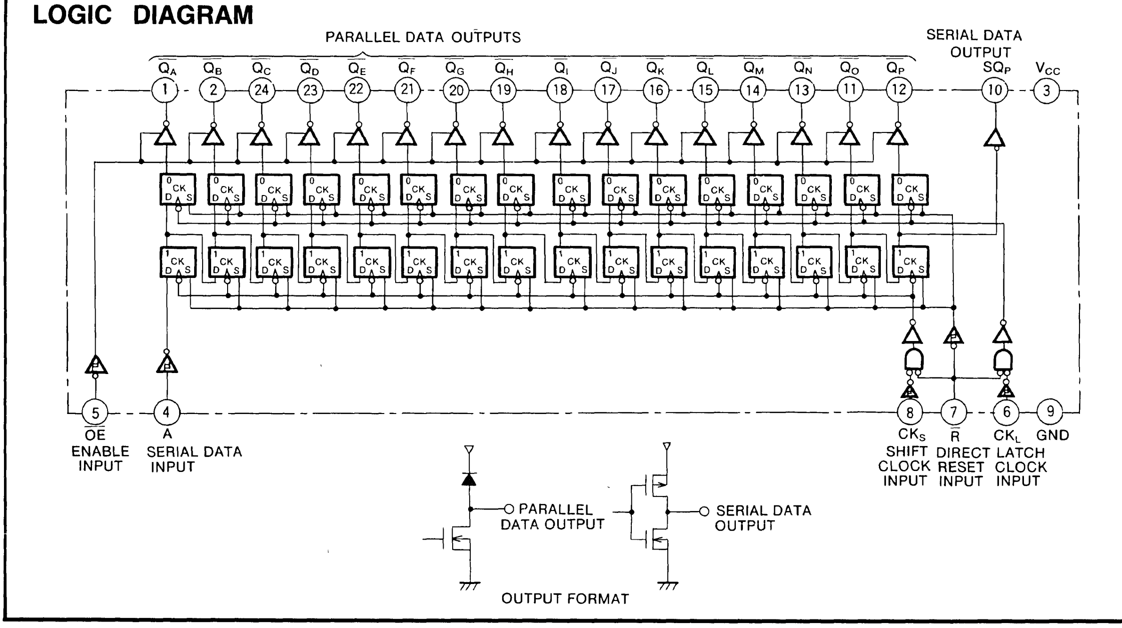


Outline 24P4D
24P2

APPLICATION

LED array drive of BUTTON TELEPHONE
LED array drive of ERASER of a PPC copier
Other various LED modules

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONAL DESCRIPTION

As M66311P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CKs and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S. When A is "H", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from $\overline{Q_A}$~$\overline{Q_P}$.

Outputs from $\overline{Q_A}$~$\overline{Q_P}$ are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to $\overline{Q_A}$~$\overline{Q_P}$.

When reset input $\overline{R}$ is changed to "L", $\overline{Q_A}$~$\overline{Q_P}$ and SQ_P are reset. In this case, shifting and latching registers are set.

If "H" is impressed to output enable input $\overline{OE}$, $\overline{Q_A}$ ~ $\overline{Q_P}$ reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

FUNCTION TABLE (Note : 1)

Operation mode		Input					PARALLEL DATA Output																Serial data output SQP	Remarks
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	$\overline{Q_A}$	$\overline{Q_B}$	$\overline{Q_C}$	$\overline{Q_D}$	$\overline{Q_E}$	$\overline{Q_F}$	$\overline{Q_G}$	$\overline{Q_H}$	$\overline{Q_I}$	$\overline{Q_J}$	$\overline{Q_K}$	$\overline{Q_L}$	$\overline{Q_M}$	$\overline{Q_N}$	$\overline{Q_O}$	$\overline{Q_P}$	SQ_P	
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	—
Shift latch operation	Shift t1	H	↑	X	H	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	$\overline{Q_C}^0$	$\overline{Q_D}^0$	$\overline{Q_E}^0$	$\overline{Q_F}^0$	$\overline{Q_G}^0$	$\overline{Q_H}^0$	$\overline{Q_I}^0$	$\overline{Q_J}^0$	$\overline{Q_K}^0$	$\overline{Q_L}^0$	$\overline{Q_M}^0$	$\overline{Q_N}^0$	$\overline{Q_O}^0$	$\overline{Q_P}^0$	q_O^0	Output lighting "H"
	Latch t2	H	X	↑	X	L	L	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
	Shift t1	H	↑	X	L	L	$\overline{Q_A}^0$	$\overline{Q_B}^0$	$\overline{Q_C}^0$	$\overline{Q_D}^0$	$\overline{Q_E}^0$	$\overline{Q_F}^0$	$\overline{Q_G}^0$	$\overline{Q_H}^0$	$\overline{Q_I}^0$	$\overline{Q_J}^0$	$\overline{Q_K}^0$	$\overline{Q_L}^0$	$\overline{Q_M}^0$	$\overline{Q_N}^0$	$\overline{Q_O}^0$	$\overline{Q_P}^0$	q_O^0	Output lights-out "L"
	Latch t2	H	X	↑	X	L	Z	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_P	—

Note 1 : ↑ : Change from low-level to high-level
$\overline{Q}^0$: Output state $\overline{Q}$ before CK_L changed
X : Irrelevant
q^0 : Contents of shift register before CK_S changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current per output pin	$\overline{Q_A}$~$\overline{Q_P}$		50	mA
		SQ_P		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	−20, +410	mA
Pd	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65~+150	℃

Note 2 : M66311FP ; T_a=−40~+70℃, T_a=70~85℃ are derated at −6mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits T_a=25℃ Min	Typ	Max	T_a=−40~+85℃ Min	Max	Unit
V_{T+}	Positive-going threshold voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		0.35×V_{CC}		0.7×V_{CC}	0.35×V_{CC}	0.7×V_{CC}	V
V_{T-}	Negative-going threshold voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		0.2×V_{CC}		0.55×V_{CC}	0.2×V_{CC}	0.55×V_{CC}	V
V_{OL}	Low-level output voltage $\overline{Q_A}$~$\overline{Q_P}$	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=24mA			0.44		0.53	
		Note3	I_{OL}=40mA			0.73		0.94	
V_{OH}	High-level output voltage SQ_P	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−4mA	3.83			3.66		
V_{OL}	Low-level output voltage SQ_P	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=4mA			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}, V_{CC}=5.5V				0.5		5.0	μA
I_{IL}	Low-level input current	V_I=GND, V_{CC}=5.5V				−0.5		−5.0	μA
I_O	Maximum output leakage current $\overline{Q_A}$~$\overline{Q_P}$	V_I=V_{T+}, V_{T-} V_{CC}=5.5V	V_O=V_{CC}			1.0		10.0	μA
			V_O=GND			−1.0		−10.0	
I_{CC}	Quiescent supply current	V_I=V_{CC}, GND, V_{CC}=5.5V				20.0		200.0	μA

Note 3 : M66311 is used under the condition of an output current I_{OL}=40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle−I_{OL} of Standard characteristics.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

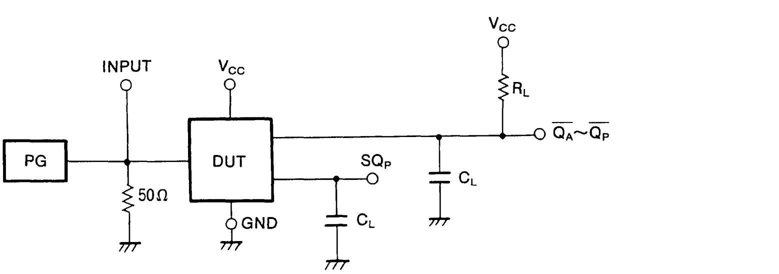
Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L=50pF, R_L= 1 kΩ (Note 5)	5			4		MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_S-SQ_P)				100		130	ns
t_{PHL}					100		130	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$-SQ_P)				100		130	ns
t_{PLZ}	Low-level to high-level output propagation time ($\overline{R}$-$\overline{Q_A}$~$\overline{Q_P}$)				150		200	ns
t_{PZL}	Low-level to high-level and high-level to low-level output propagation time (CK_L−$\overline{Q_A}$~$\overline{Q_P}$)				100		130	ns
t_{PLZ}					150		200	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$−$\overline{Q_A}$~$\overline{Q_P}$)				100		130	ns
t_{PLZ}					150		200	ns
C_I	Input Capacitance				10		10	pF
C_O	Output Capacitance	$\overline{OE}$=V_{CC}			15		15	pF
C_{PD}	Power dissipation Capacitance (Note 4)			5				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
t_w	CK_S, CK_L, $\overline{R}$ pulse width	(Note 5)	100			130		ns
t_{su}	A setup time with respect to CK_S		100			130		ns
t_{su}	CK_S setup time with respect to CK_L		100			130		ns
t_h	A hold time with respect to CK_S		10			15		ns
t_{rec}	$\overline{R}$, recovery time with respect to CK_S, CK_L		50			70		ns

Note 5 : Test Circuit

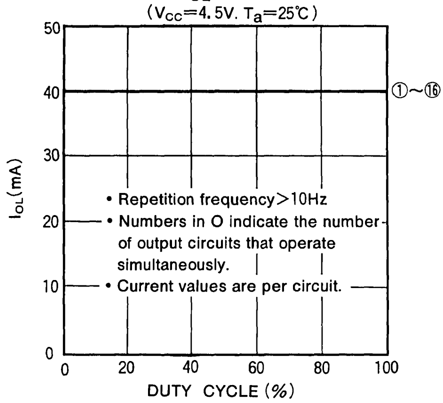


(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr =6ns, tf=6ns

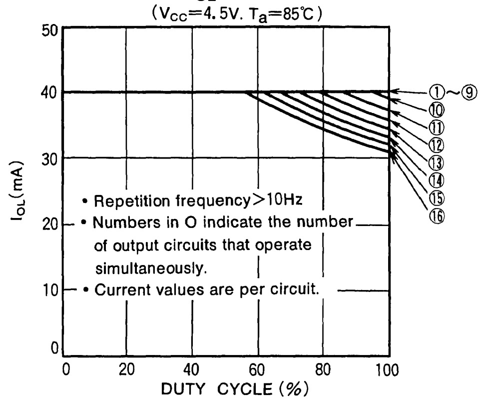
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

STANDARD CHARACTERISTICS

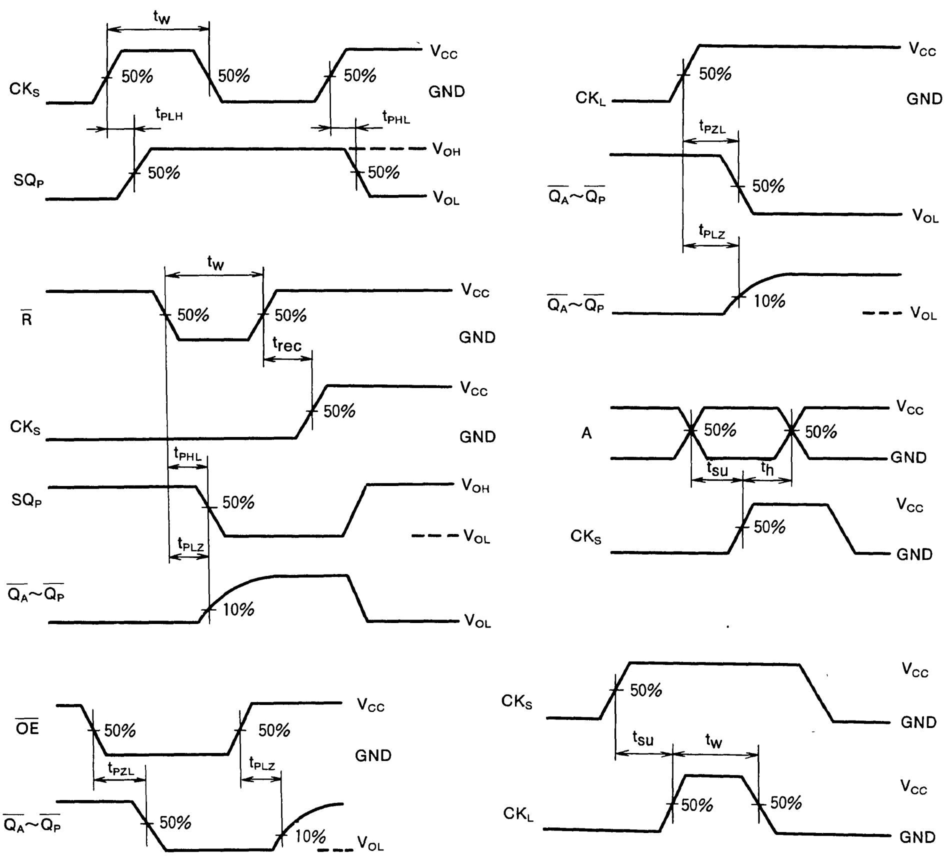
DUTY CYCLE—I_{OL} CHARACTERISTICS
(V_{CC}=4.5V. T_a=25℃)



DUTY CYCLE—I_{OL} CHARACTERISTICS
(V_{CC}=4.5V. T_a=85℃)



TIMING DIAGRAM



All values shown in this catalogue are subject to change for product improvement.
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8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

DESCRIPTION

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

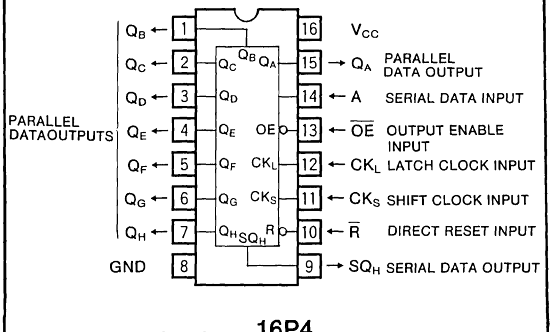
This product guarantees the output electric current of 16mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

FEATURES

- High output current I_{OL}=16mA, I_{OH}=−16mA
- High speed (clock freguency) : 30MHz (typ) (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 20μW/package (max) (V_{CC}=5V, Ta=25℃, quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range : Ta=−40～+85℃

PIN CONFIGURATION (TOP VIEW)

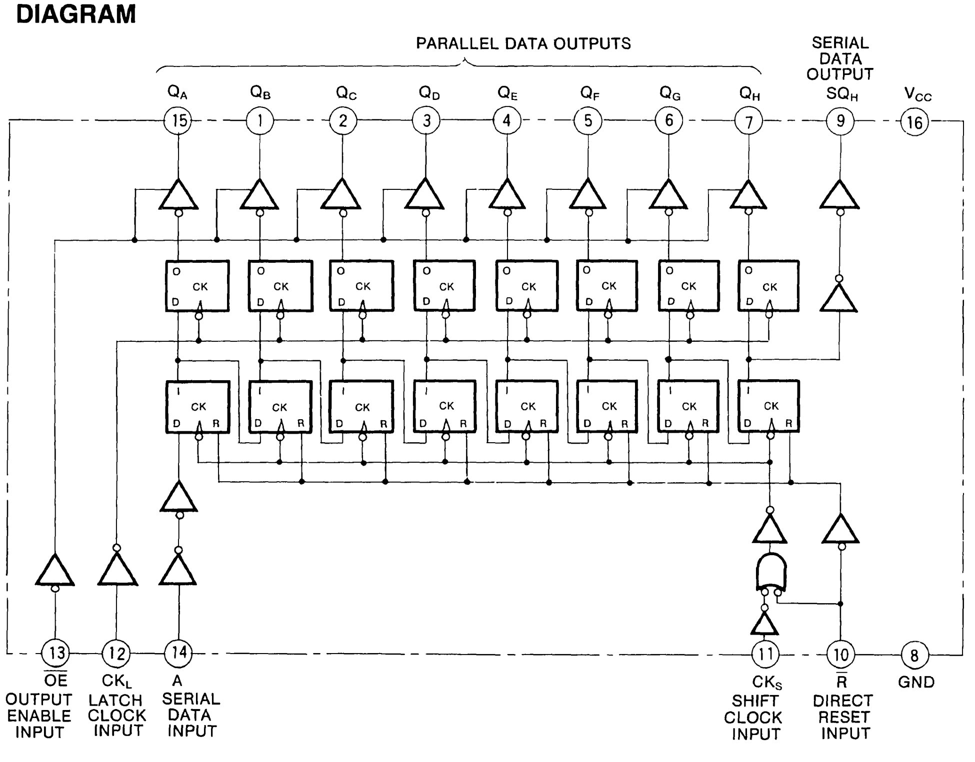


Outline 16P4
16P2N

APPLICATION

LED array drive of PRINTER
LED array drive of BUTTON TELEPHONE

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shiting registers one by one when a pulse is impressed to CK_S. When A is "H", the signal of "H" shifts. When A is "L", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the output from Q_A through Q_H are 3-state outputs.

To extend the number of bits, serial data output SQ_H is used to output the 8-bit of the shift register.

By connecting CKs and CK_L, the shift register state delayed by 1 clock cycle is output at Q_A through Q_H.

When reset input $\overline{R}$ is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by $\overline{R}$.

When output-enable input $\overline{OE}$ is high, Q_A through Q_H will become high impedance state, but SQ_H is not changed. Even if $\overline{OE}$ is changed, shift operation is not affected.

FUNCTION TABLE (Note : 1)

Operation mode		Input					Parallel data output								Serial data output SQ_H
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	
Reset	Shift t_1	L	X	X	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L
	Latch t_2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift t_1	H	↑	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t_2	H	X	↑	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
	Shift t_1	H	↑	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t_2	H	X	↑	X	L	L	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
3 state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q_H

Note 1 : ↑ : Change from low-level to high-level
Q^0 : Output state Q before CK_L changed
X : Irrelevant
q^0 : Contents of shift register before CK_S changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7.0	V
V_I	Input voltage			−0.5∼V_{CC}+0.5	V
V_O	Output voltage			−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current per output pin	Q_A∼Q_H		±35	mA
		SQ_H		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	±132	mA
P_d	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65∼+150	℃

Note 2 : M66312FP , T_a=−40∼+70℃, T_a=70∼85℃ are derated at −6mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40∼+85℃)

Symbol	Parameter		Limits Min	Limits Nom	Limits Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
tr, tf	Input rising and falling time	V_{CC}=4.5V	0		500	ns
		V_{CC}=5.5V	0		400	

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5∼5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits T_a=25℃ Min	Limits T_a=25℃ Typ	Limits T_a=25℃ Max	Limits T_a=−40∼+85℃ Min	Limits T_a=−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V |I_O| = 20μA		0.70×V_{CC}			0.70×V_{CC}		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V |I_O| = 20μA				0.30×V_{CC}		0.30×V_{CC}	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
	Q_A∼Q_H	V_{CC}=4.5V	I_{OH}=−16mA	3.70*			3.55*		
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
	SQ_H	V_{CC}=4.5V	I_{OH}=−4mA	4.0			3.9		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL}=20μA			0.1		0.1	V
	Q_A∼Q_H	V_{CC}=4.5V	I_{OL}=16mA			0.7*		0.85*	
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL}=20μA			0.1		0.1	V
	SQ_H	V_{CC}=4.5V	I_{OL}= 4 mA			0.4		0.5	
I_{IH}	High-level input current	V_I=V_{CC}, V_{CC}=5.5V				0.1		1.0	μA
I_{IL}	Low-level input current	V_I=GND, V_{CC}=5.5V				−0.1		−1.0	μA
I_{OZH}	Off state high-level output current Q_A∼Q_H	V_I=V_{IH}, V_{IL}	V_O=V_{CC}			1.0		10.0	μA
I_{OZL}	Off state low-level output current Q_A∼Q_H	V_{CC}=5.5V	V_O=GND			−1.0		−10.0	μA
I_{CC}	Quiescent supply current	V_I=V_{CC}, GND, V_{CC}=5.5V				4.0		40.0	μA

* : Limits of single PIN operating state

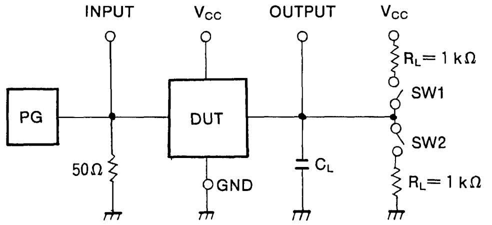
SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L=50pF	15			12		MHz
t_{PLH}	Low-level to high-level and high-level to low-level				70		88	ns
t_{PHL}	output propagation time CKs-SQ_H	C_L=15pF			70		88	ns
t_{PHL}	High-level to low-level output propagation time $\overline{R}$-SQ_H	(Note 3)			60		76	ns
t_{PLH}	Low-level to high-level and high-level to low-level	C_L=50pF			60		76	ns
t_{PHL}	output propagation time CK_L-Q_A~Q_H	(Note 3)			60		76	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L=5pF			50		64	ns
t_{PHZ}	$\overline{OE}$-Q_A~Q_H	(Note 3)			50		64	ns
t_{PZL}	Output enable time to low-level and high-level	C_L=50pF			56		70	ns
t_{PZH}	$\overline{OE}$-Q_A~Q_H	(Note 3)			56		70	ns

TIMING REQUIREMENTS (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
t_W	CK_S, CK_L, $\overline{R}$ pulse width		32			40		ns
t_{su}	A setup time with respect to CK_S		40			50		ns
t_{su}	CK_S setup time with respect to CK_L		40			50		ns
t_h	A hold time with respect to CK_S		10			10		ns
t_{rec}	$\overline{R}$ recovery time with respect to CK_S		20			26		ns

Note 3 : Test Circuit



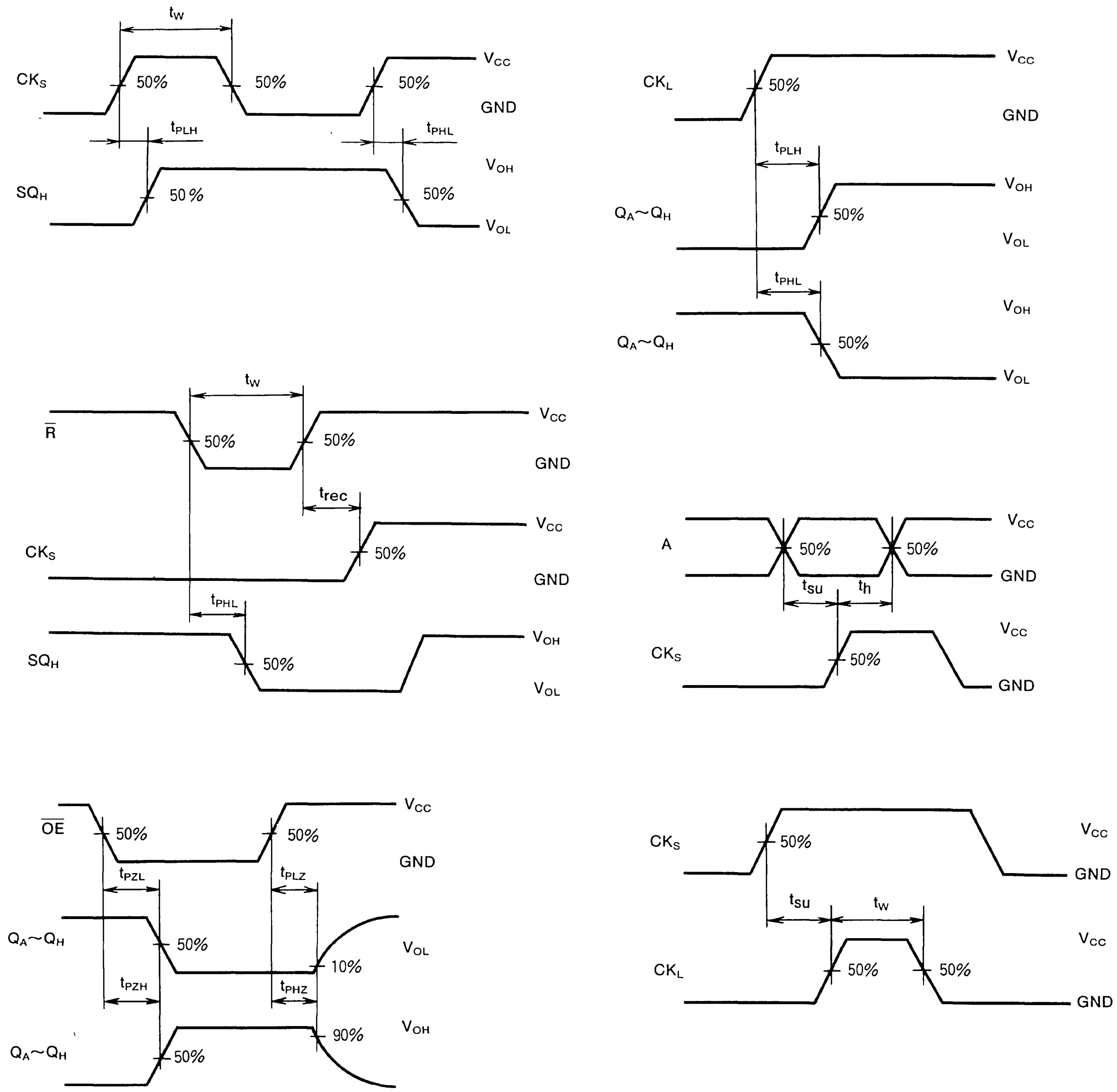
Item	SW1	SW2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PLZ}	CLOSE	OPEN
t_{PHZ}	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN
t_{PZH}	OPEN	CLOSE

(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr =6ns, tf=6ns

(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

TIMING DIAGRAM



M66313FP

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

FEATURES

- High output current
  All parallel output $I_{OL}=+24mA$, LEDs can be turned on simultaneously.
- Low power dissipation : 200μW/package (max)
  ($V_{CC}=5V$, $T_a=25$℃, quiescent state)
- High noise margin
  Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{S_D}$)
- Open-drain output ($\overline{Q_1}\sim\overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range ($T_a=-40\sim+85$℃)
- Pin configuration for easy layout on PCB.
  (Pin configuration allows easy cascade connection or LED connection)

APPLICATION

LED array drive for eraser unit of a copying machine
LED array drive of a button telephone set
Various LED modules

FUNCTION

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs $\overline{Q_1}\sim\overline{Q_{32}}$ are open-drain outputs.

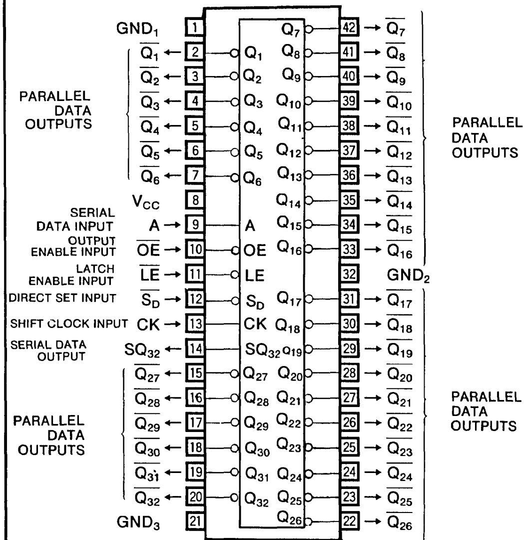
If the latch-enable input $\overline{LE}$ is turned high-level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.

If the direct set input $\overline{S_D}$ is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input $\overline{OE}$, $\overline{Q_1}\sim\overline{Q_{32}}$ are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift opration is not affected when $\overline{OE}$ is changed.

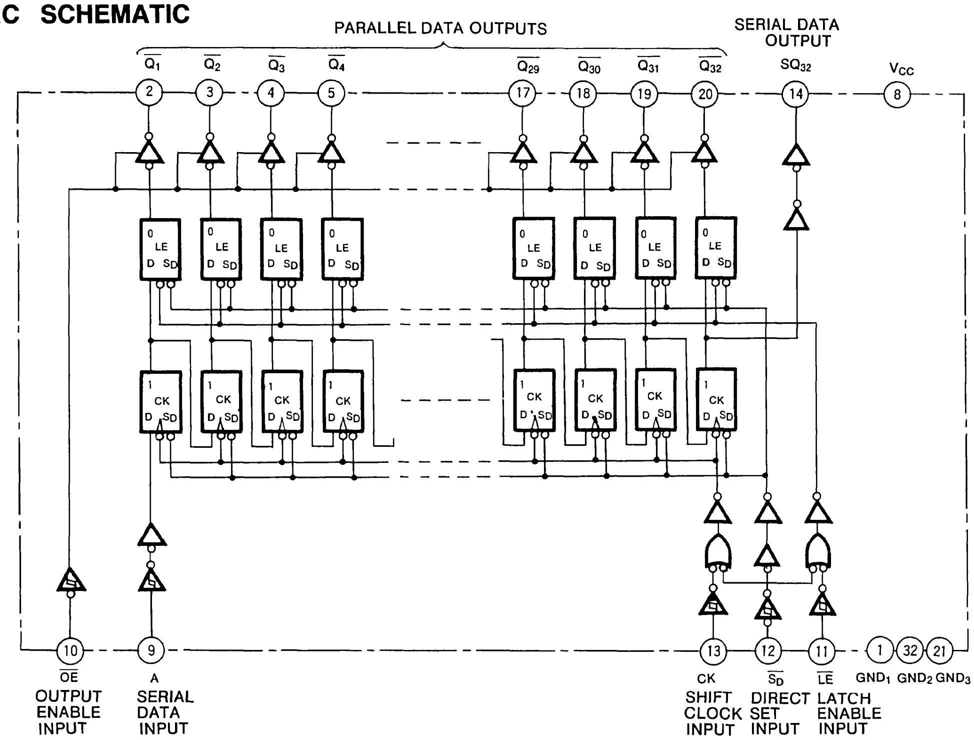
PIN CONFIGURATION (TOP VIEW)

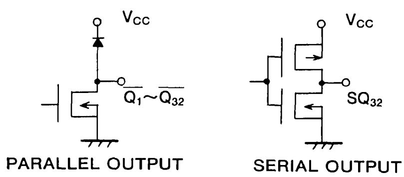


Outline 42P2R

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

LOGIC SCHEMATIC





OUTPUT TYPE

FUNCTIONAL TABLE (Note 1)

OPERATION MODE	INPUT					PARALLEL OUTPUTS																															SERIAL OUTPUT
	$\overline{S_D}$	CK	$\overline{LE}$	A	$\overline{OE}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$	$\overline{Q_8}$	$\overline{Q_9}$	$\overline{Q_{11}}$	$\overline{Q_{12}}$	$\overline{Q_{13}}$	$\overline{Q_{14}}$	$\overline{Q_{15}}$	$\overline{Q_{16}}$	$\overline{Q_{17}}$	$\overline{Q_{18}}$	$\overline{Q_{19}}$	$\overline{Q_{20}}$	$\overline{Q_{21}}$	$\overline{Q_{22}}$	$\overline{Q_{22}}$	$\overline{Q_{23}}$	$\overline{Q_{24}}$	$\overline{Q_{25}}$	$\overline{Q_{26}}$	$\overline{Q_{27}}$	$\overline{Q_{28}}$	$\overline{Q_{29}}$	$\overline{Q_{30}}$	$\overline{Q_{31}}$	$\overline{Q_{32}}$	SQ_{32}
SET	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
SHIFT	H	↑	L	H	L	L	$\overline{Q^0_{1}}$	$\overline{Q^0_{2}}$	$\overline{Q^0_{3}}$	$\overline{Q^0_{4}}$	$\overline{Q^0_{5}}$	$\overline{Q^0_{6}}$	$\overline{Q^0_{7}}$	$\overline{Q^0_{8}}$	$\overline{Q^0_{9}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
	H	↑	L	L	L	Z	$\overline{Q^0_{1}}$	$\overline{Q^0_{2}}$	$\overline{Q^0_{3}}$	$\overline{Q^0_{4}}$	$\overline{Q^0_{5}}$	$\overline{Q^0_{6}}$	$\overline{Q^0_{7}}$	$\overline{Q^0_{8}}$	$\overline{Q^0_{9}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
LATCH	H	X	H	X	L	$\overline{Q^0_{1}}$	$\overline{Q^0_{2}}$	$\overline{Q^0_{3}}$	$\overline{Q^0_{4}}$	$\overline{Q^0_{5}}$	$\overline{Q^0_{6}}$	$\overline{Q^0_{7}}$	$\overline{Q^0_{8}}$	$\overline{Q^0_{9}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	$\overline{Q^0_{32}}$	q_{32}
OUTPUT DIS-ABLE	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_{32}

Note 1 ↑ : Transition from low-to-high-level.
$\overline{Q^0}$: Shows the status of output $\overline{Q}$ before CK input changes.
X : Irrelevant
q^0 : The content of shift register before CK changes
q : The content of the shift register.
Z : High-impedance state

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current	$\overline{Q_1}$~$\overline{Q_{32}}$		50	mA
		SQ_{32}		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	−920, +20	mA
Pd	Power dissipation			650	mW
Tstg	Storage temperature range			−65~+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating free-air ambient temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits					Unit
					T_a=25℃			T_a=−40~+85℃		
					Min	Typ*	Max	Min	Max	
V_{T+}	Positive-going threshold voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20µA		0.35XV_{CC}	2.8	0.7XV_{CC}	0.35XV_{CC}	0.7XV_{CC}	V
V_{T-}	Negative-going threshold voltage		V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20µA		0.2XV_{CC}	2	0.55XV_{CC}	0.2XV_{CC}	0.55XV_{CC}	V
V_{OH}	High-level output voltage	SQ_{32}	V_I = V_{T+}, V_{T-} V_{CC}=4.5V	I_{OH}=−20µA	V_{CC}−0.1			V_{CC}−0.1		V
				I_{OH}=−4mA	3.83			3.66		
V_{OL}	Low-level output voltage	$\overline{Q_1}$~$\overline{Q_{32}}$	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20µA			0.1		0.1	V
				I_{OL}=24mA		0.20	0.41		0.50	
				I_{OL}=28mA		0.25	0.48		0.55(Note 2)	
		SQ_{32}		I_{OL}=20µA			0.1		0.1	
				I_{OL}=4mA			0.44		0.53	
I_{IH}	High-level input current		V_I=V_{CC}, V_{CC}=5.5V				0.5		5.0	µA
I_{IL}	Low-level input current		V_I=GND, V_{CC}=5.5V				−0.5		−5.0	µA
I_O	Maximum output leak current	$\overline{Q_1}$~$\overline{Q_{32}}$	V_I=V_{T+}, V_{T-} V_{CC}=5.5V	V_O=V_{CC}			1.0		10.0	µA
				V_O=GND			−1.0		−10.0	
I_{CC}	Quiescent state dissipation current		V_I=V_{CC}, GND V_{CC}=5.5V				40.0		400.0	µA

* : All typical values are at V_{CC}=5V, T_a=25℃
Note 2 : T_a=−40~+70℃

SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

Symbol	Parameter		Test conditions	Limits					Unit
				T_a=25℃			T_a=−40~+85℃		
				Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency		C_L=50pF R_L=1kΩ (Note 3)	5	30		4		MHz
t_{PZL}	Output enable time to low-level	CK-$\overline{Q_1}$~$\overline{Q_{32}}$(Turned on)			35	150		200	ns
t_{PLZ}	Output disable time from low-level	CK-$\overline{Q_1}$~$\overline{Q_{32}}$(Turned off)			35	200		250	ns
t_{PLH}	Low-to-high, high-to-low output propagation time	CK-SQ_{32}			35	100		130	ns
t_{PHL}					40	100		130	ns
t_{PZL}	Output enable time to low-level	$\overline{S_D}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			35	150		200	ns
t_{PLH}	Low-to-high output propagation time	$\overline{S_D}$-SQ_{32}			40	100		130	ns
t_{PZL}	Output enable time to low-level	$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			30	100		130	ns
t_{PLZ}	Output disable time from low-level	$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)			35	150		200	ns
t_{PZL}	Output enable time to low-level	$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			30	100		130	ns
t_{PLZ}	Output disable time from low-level	$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)			35	150		200	ns
C_I	Input capacitance				3	10		10	pF
C_O	Output capacitance		$\overline{OE}$=V_{CC}		6	15		15	pF
C_{PD}	Power dissipation capacitance(Note 4)				160				pF

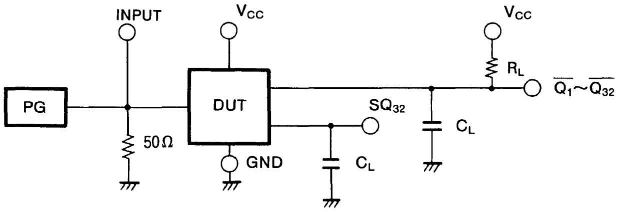
Note 4 : C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load The operating power dissipation without load is given as follows·

$$P_D=C_{PD} \cdot V_{CC}^2 \cdot f_I+I_{CC} \cdot V_{CC}$$

TIMING REQUIREMENT (V_{CC}= 5 V)

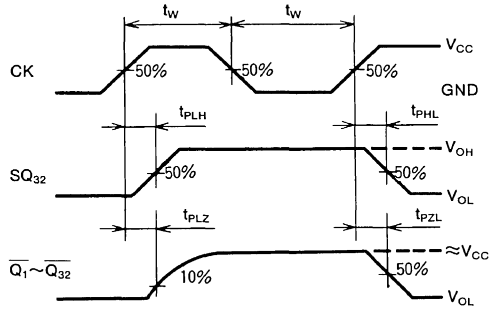
Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40～+85℃		
			Min	Typ	Max	Min	Max	
t_w	CK, $\overline{LE}$, $\overline{S_D}$ pulse width	(Note 3)	100	16		130		ns
t_{su}	Setup time A to CK		100	27		130		ns
t_h	Hold time A to CK		10	5		15		ns
	Hold time $\overline{LE}$ to CK		50	15		70		
t_{rec}	Recovery time CK to $\overline{S_D}$		50	20		70		ns

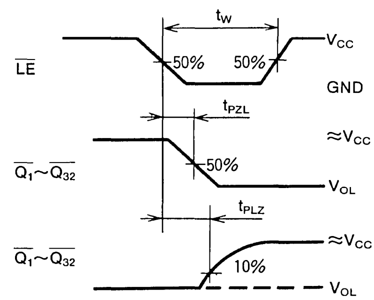
Note 3 : Test circuit

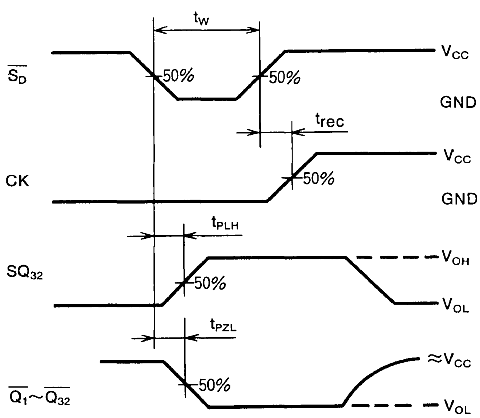


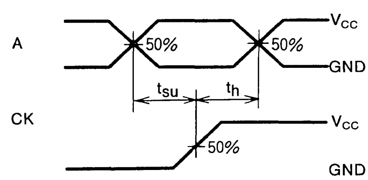
(1) Characteristics of pulse generator(PG): t_r= 6 ns, t_f= 6 ns
(2) C_L includes probe and jig capacitance.

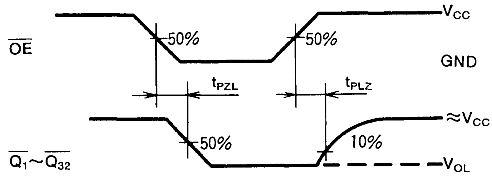
TIMING DIAGRAM

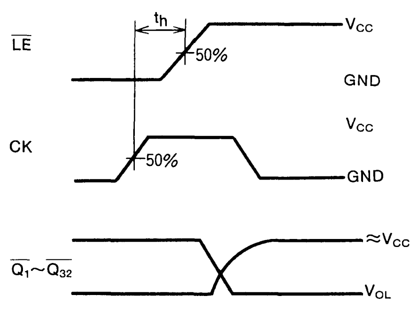












M66314FP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

The M66314FP is an integrated circuit consisting of an LED array driver with 16-bit serial-in parallel-out shift register and output latch. Use of the CMOS process allows the M66314FP to integrate a bipolar output driver and a CMOS logic circuit on a signgle chip. Serial data is output by converting it into parallel data using a shift register. The previous data can be output during shift register data transfer using the latch. Output current of -25mA is sufficient to drive an LED. The pin configuration is designed for easy layout on a printed-circuit board.

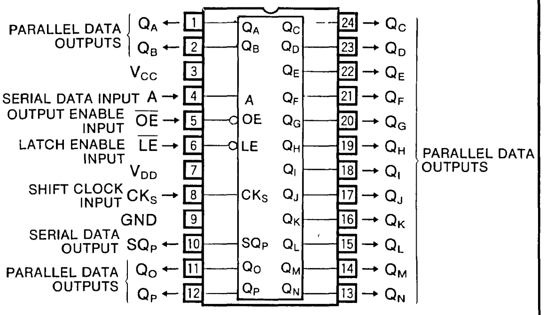
FEATURES

- High output current. All parallel output $I_{OH} = -25$mA (V_{DD}=18V). Simultaneous drive possible
- NPN bipolar transistor output (except serial data output)
- Built-in level shifter, allowing control with 5V system
- High noise margin, Schmitt input circuit
- Low power dissipation. 720μW/package max (V_{DD} = 12V, T_a=25°C, no load)
- Pin configuration disigned for easy layout on a printed circuit board

APPLICATION

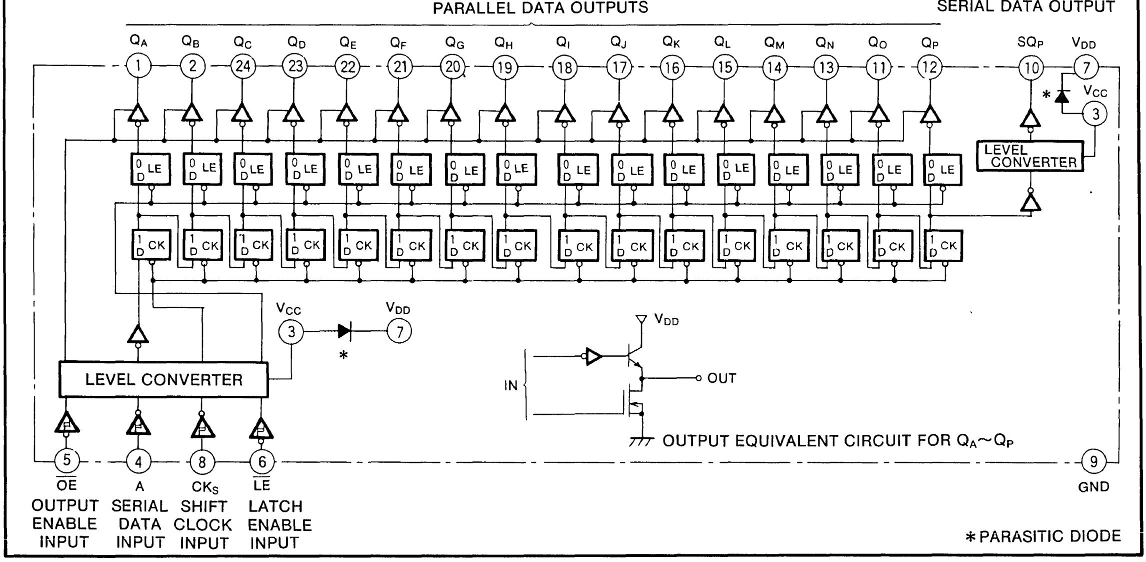
LED array drive for printers, LED array drive for push-button telephones, or LED array drive for PPC copying machine eraser units.

PIN CONFIGURATION (TOP VIEW)



Outline 24P2

LOGIC DIAGRAM



16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

FUNCTION

Use of a high voltage CMOS process allows the M66314FP to maintain low power dissipation and high noise margin characteristics.

Each bit of the shift register consists of a shift flip-flop and a latch connected to the output. Shift operation takes place when the clock input changes from low-to high-level.

The serial data input A is input to the first-stage shift register, and the data A shifts the shift register when pulses are applied to CKs. When A is high-level, the high-level data shifts and when A is low-level, the low-level data shifts. If the latch enable input $\overline{LE}$ is set low-level, the content of the shift register is latched. To expand the number of bits, serial data output SQ_P is available, to which 16th-bit shift register is output.

If the output enable input $\overline{OE}$ is set to high-level, $Q_A \sim Q_P$ become high-impedance states. In this case, the content of 16th-bit shift register is output to SQ_P. The shift operation is not affected even if the $\overline{OE}$ changes.

FUNCTION TABLE (Note 1)

Inputs				Parallel outputs																Serial output
CK_S	$\overline{LE}$	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	Q_I	Q_J	Q_K	Q_L	Q_M	Q_N	Q_O	Q_P	SQ_P
↑	H	H	L	H	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	q_O^0
↑	H	L	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	q_O^0
X	L	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	Q_P^0	q_P
X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_P

Note 1 : ↑ : Change from low-to high-level
Q^0 : Output state Q before clock input changed
X : Irrevant
q^0 : The content of shift register before CK_S changed
q : The content of shift register

ABSOLUTE MAXIMUM RATINGS (T_a=0～+40℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{DD}	Supply voltage (1)			−0.5～+20	V
V_{CC}	Supply voltage (2)			−0.5～+20	V
$V_{DD}-V_{CC}$	Supply voltage (1)−supply voltage (2)			−0.5～+20	V
V_I	Input voltage			−0.5～V_{DD}+0.5	V
V_O	Output voltage			−0.5～V_{DD}+0.5	V
I_O	Output current	$Q_A \sim Q_P$		−50, +5	mA
		SQ_P		±10	
I_{CC}	Supply/GND current		V_{CC}, GND	+420, −10	mA
Pd	Power dissipation		(Note 2)	570 [750]	mW
Tstg	Storage temperature range			−65～+150	℃

Note 2 : [ ] shows the value when mounted on the printed circuit board

RECOMMENDED OPERATING CONDITIONS (T_a=0～+40℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage (1) (Note 3)	12		18	V
V_{CC}	Supply voltage (2)	4.75	5	5.25	V
V_I	Input voltage	0		V_{CC}	V
Topr	Operating temperature range	0		+40	℃

Note 3 : As the parasitic diode is formed as shown in the logic diagram, turn on the V_{DD} first at power-on and turn off the V_{CC} first at power-off

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				T_a=25℃			T_a=0~+40℃		
			V_{DD}(V)	Min	Typ	Max	Min	Max	
V_{OH}	High-level output voltage Q_A~Q_P	$\|I_O\|$ < 1 μA, V_I=GND, V_{CC}	12	11.0			11.0		V
			18	17.0			17.0		
V_{OH}	High-level output voltage SQ_P		12	V_{CC}−0.05			V_{CC}−0.05		V
			18	V_{CC}−0.05			V_{CC}−0.05		
V_{OL}	Low-level output voltage Q_A~Q_P	$\|I_O\|$ < 1 μA, V_I=GND, V_{CC}	12			0.05		0.05	V
			18			0.05		0.05	
V_{OL}	Low-level output voltage SQ_P		12			0.05		0.05	V
			18			0.05		0.05	
I_{OH}	High-level output current Q_A~Q_P	V_{OH}=10.5V	12	−15			−15		mA
		V_{OH}=16.5V	18	−25			−25		
		V_I=GND, V_{CC}							
I_{OH}	High-level output current SQ_P	V_{OH}=V_{CC}−1.0V	12	−0.16			−0.12		mA
		V_{OH}=V_{CC}−1.0V	18	−0.16			−0.12		
		V_I=GND, V_{CC}							
I_{OL}	Low-level output current Q_A~Q_P	V_{OL}=0.4V	12	0.22			0.18		mA
		V_{OL}=0.4V	18	0.22			0.18		
		V_I=GND, V_{CC}							
I_{OL}	Low-level output current SQ_P	V_{OL}=0.4V	12	0.44			0.36		mA
		V_{OL}=0.4V	18	0.44			0.36		
		V_I=GND, V_{CC}							
V_{IH}	High-level input voltage	V_O=1.2V, 10.8V	12	0.80×V_{CC}			0.80×V_{CC}		V
		V_O=1.8V, 16.2V	18	0.80×V_{CC}			0.80×V_{CC}		
		$\|I_O\|$ < 1 μA							
V_{IL}	Low-level input voltage	V_O=1.2V, 10.8V	12			0.20×V_{CC}		0.20×V_{CC}	V
		V_O=1.8V, 16.2V	18			0.20×V_{CC}		0.20×V_{CC}	
		$\|I_O\|$ < 1 μA							
I_{IH}	High-level input current	V_{IH}=18V	18			0.3		1.0	μA
I_{IL}	Low-level input current	V_{IL}=0V	18			−0.3		−1.0	μA
I_{OZH}	Off-state high-level output current	V_O=18V	18			0.5		30	μA
I_{OZL}	Off-state low-level output current	V_O=0V	18			−0.5		−30	μA
I_{DD}	Static supply current	V_I=GND, V_{CC}	12			60		100	μA
			18			130		200	

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

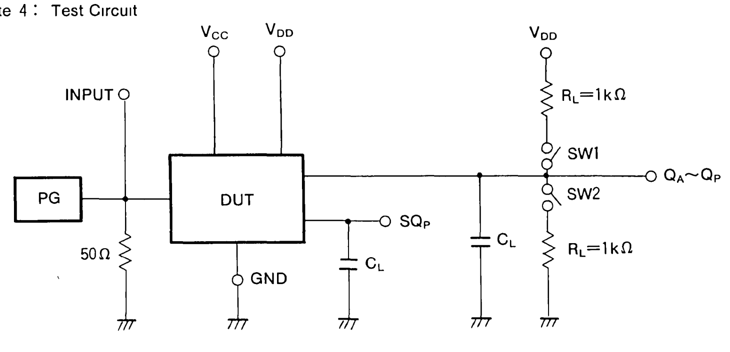
SWITCHING CHARACTERISTICS (T_a=25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions		Limits			Unit
			V_{DD}(V)	Min	Typ	Max	
f_{max}	Maximum repetitive frequency		12～18	1			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	12			100	ns
			18			100	
t_{THL}			12			150	ns
			18			150	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK_S–Q_A～Q_P)		12			600	ns
			18			600	
t_{PHL}			12			600	ns
			18			600	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK_S—SQ_P)		12			600	ns
			18			600	
t_{PHL}			12			600	ns
			18			600	
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$—Q_A～Q_P)		12			500	ns
			18			500	
t_{PHL}			12			500	ns
			18			500	
t_{PHZ}	High-level and low-level output disable time ($\overline{OE}$—Q_A～Q_P)		12			500	ns
			18			500	
t_{PLZ}			12			500	ns
			18			500	
t_{PZH}	High-level and low-level output enable time ($\overline{OE}$—Q_A～Q_P)		12			300	ns
			18			300	
t_{PZL}			12			300	ns
			18			300	
C_I	Input capacitance					7.5	pF

TIMING REQUIREMENTS (T_a=25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions		Limits			Unit
			V_{DD}(V)	Min	Typ	Max	
t_r, t_f	CK_S rise time and fall time		12～18			1.0	μs
t_W	CK_S, $\overline{LE}$ pulse width		12～18	200			ns
t_{SU}	A setup time with respect to CK_S		12～18	200			ns
t_h	A hold time with respect to CK_S		12～18	200			ns

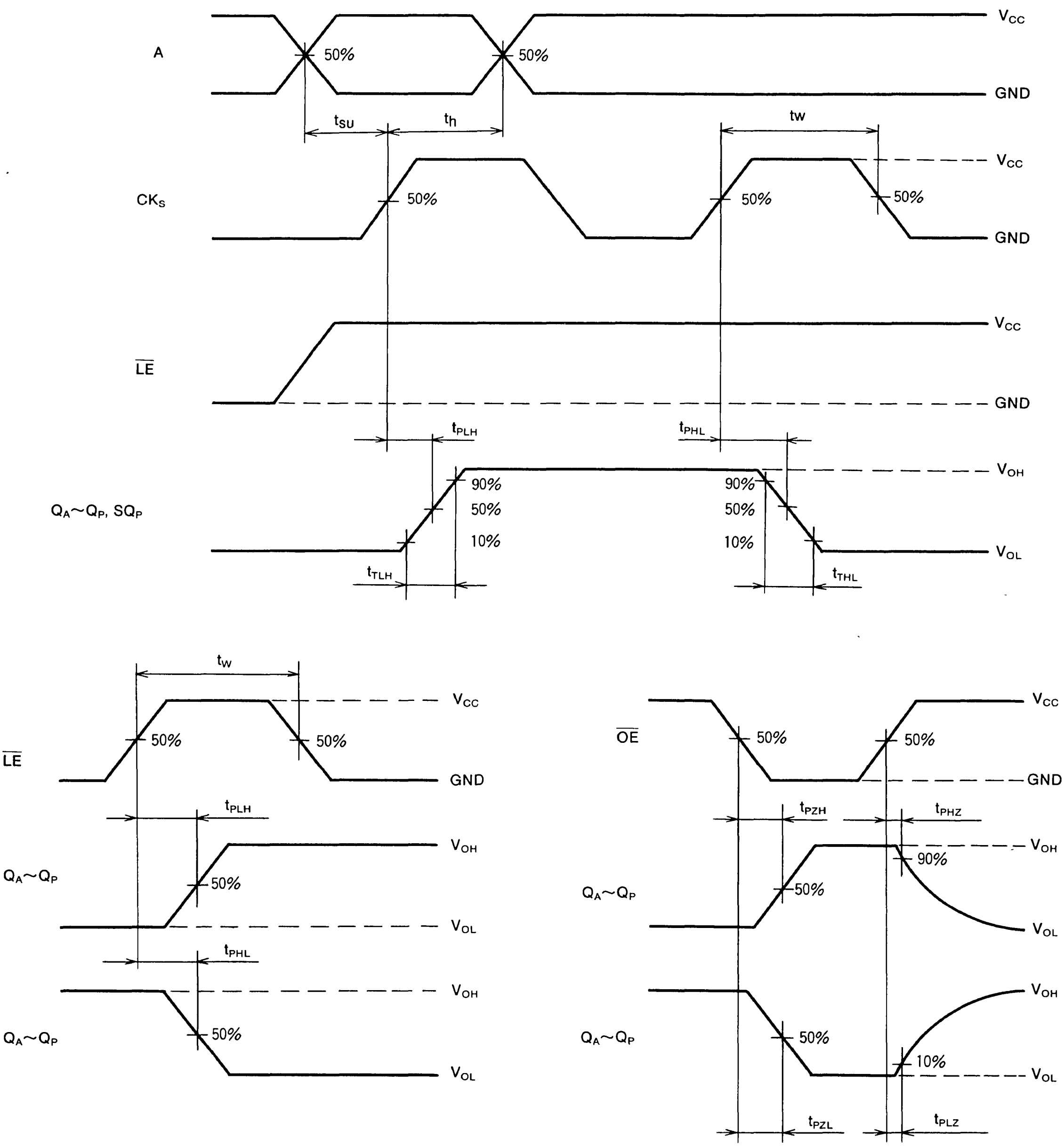
Note 4 : Test Circuit



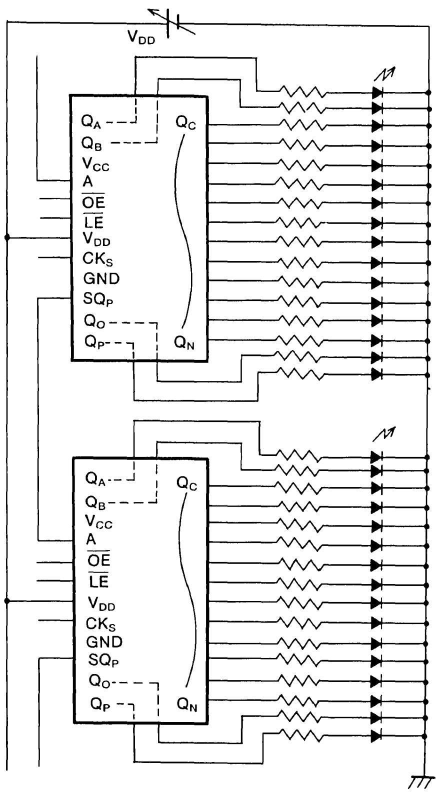
Parameter	SW 1	SW 2
t_{PHZ}	Open	Closed
t_{PLZ}	Closed	Open
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open

(1) The pulse generator (PG) has the following characteristics (10%～90%) : t_r=20ns, t_f=20ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

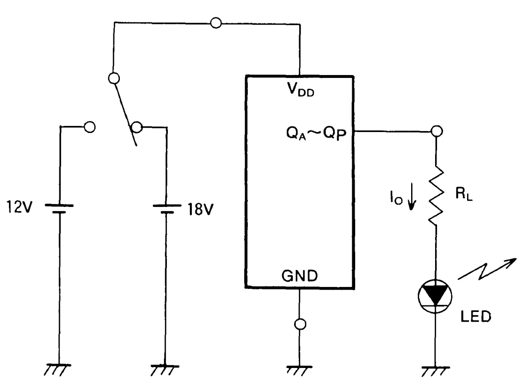
TIMING DIAGRAM



APPLICATION EXAMPLE 1



APPLICATION EXAMPLE 2



When V_{DD}=12V I_O=15mA
When V_{DD}=18V I_O=25mA
(R_L=592Ω)

$$I_O=\frac{V_{OH}-V_F}{R_L}$$

Where M66314

V_{DD}	V_{OH}(TYP)
12V	11.0V
18V	17.0V

LED(GL-9PR10)

I_F	V_F
15mA	2.13V
25mA	2.20V

M66320P/FP

12-BIT SHIFT REGISTER WITH OUTPUT LATCH

DESCRIPTION
The M66320P/FP is an integrated circuit for a 12-bit serial-in parallel-out shift register with an output latch. The device can be used as a pre-driver to drive a printer head. Each output pin is capable of driving two LSTTLs.

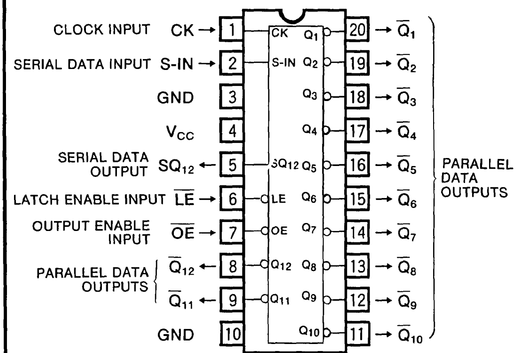
Use of CMOS design allows the M66320P/FP to reduced power dissipation considerably compared to bipolar or Bi-CMOS products.

The M66320 can also be used as a serial-to-parallel data converter or for microcomputer peripheral equipment.

FEATURES
- Low power dissipation 100μW/package maximum (V_{CC}=5V, Ta=25℃, when input is open)
- Schmitt input (CK, $\overline{LE}$)
- Wide operating temperature range Ta=−40~85℃

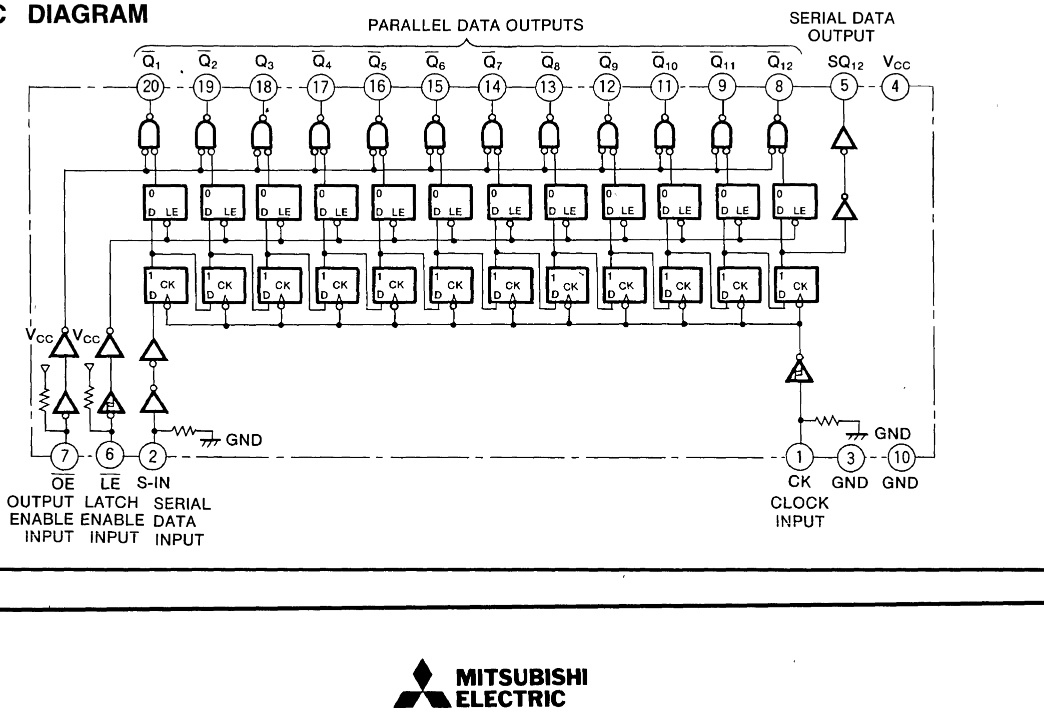
APPLICATION
Pre-driver for printer head pins.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

LOGIC DIAGRAM



12-BIT SHIFT REGISTER WITH OUTPUT LATCH

FUNCTION

Use of a silicon-gate CMOS process allows the M66320 to maintain low power dissipation and high noise margin characteristics.

Each bit of the shift register consists of a shift flip-flop and a latch connected to the output. Shift operation takes place when the clock input changes from low-to high-level. The serial data input S-IN is the data input of the first-stage shift register, and the data S-IN shifts the shift register when CK is applied. When the S-IN is high-level, the high-level data shifts and, when the S-IN is low-level, the low-level data shifts.

The inverted data of the shift register is output to $\overline{Q_1}$~$\overline{Q_{12}}$. If the latch enable input $\overline{LE}$ is set to low-level, the contents of the shift register are latched. To expand the number of bits, use the serial data output SQ_{12} to which the content of the 12th-bit shift register is output. If the output enable input $\overline{OE}$ is set to high-level, $\overline{Q_1}$~$\overline{Q_{12}}$ becomes high-level. In this case, the content of the 12th-bit shift register is output to SQ_{12}. The shift operation is not affected even if the $\overline{OE}$ changes.

FUNCTION TABLE (Note 1)

Inputs				Parallel outputs												Serial output
CK	$\overline{LE}$	S-IN	$\overline{OE}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$	$\overline{Q_8}$	$\overline{Q_9}$	$\overline{Q_{10}}$	$\overline{Q_{11}}$	$\overline{Q_{12}}$	SQ_{12}
↑	H	H	L	L	$\overline{Q_1}^0$	$\overline{Q_2}^0$	$\overline{Q_3}^0$	$\overline{Q_4}^0$	$\overline{Q_5}^0$	$\overline{Q_6}^0$	$\overline{Q_7}^0$	$\overline{Q_8}^0$	$\overline{Q_9}^0$	$\overline{Q_{10}}^0$	$\overline{Q_{11}}^0$	q_{11}^0
↑	H	L	L	H	$\overline{Q_1}^0$	$\overline{Q_2}^0$	$\overline{Q_3}^0$	$\overline{Q_4}^0$	$\overline{Q_5}^0$	$\overline{Q_6}^0$	$\overline{Q_7}^0$	$\overline{Q_8}^0$	$\overline{Q_9}^0$	$\overline{Q_{10}}^0$	$\overline{Q_{11}}^0$	q_{11}^0
X	L	X	L	$\overline{Q_1}^0$	$\overline{Q_2}^0$	$\overline{Q_3}^0$	$\overline{Q_4}^0$	$\overline{Q_5}^0$	$\overline{Q_6}^0$	$\overline{Q_7}^0$	$\overline{Q_8}^0$	$\overline{Q_9}^0$	$\overline{Q_{10}}^0$	$\overline{Q_{11}}^0$	$\overline{Q_{12}}^0$	q_{12}
X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	q_{12}

Note 1 : ↑ : Change from low-to high-level
$\overline{Q}^0$: Output state $\overline{Q}$ before clock input changed
X : Irrevant
q^0 : The content of shift register before clock changed
q : The content of shift register

ABSOLUTE MAXIMUM RATINGS (Ta=−40~+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7.0	V
V_I	Input voltage			−0.5~V_{CC}+0.5	V
V_O	Output voltage			−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I<0V	−20	mA
			V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O<0V	−20	mA
			V_O>V_{CC}	20	
I_O	Output current	$\overline{Q_1}$~$\overline{Q_{12}}$, SQ_{12}		±3	mA
I_{CC}	Supply/GND current		V_{CC}, GND	±20	mA
Pd	Power dissipation		(Note 2)	500	mW
Tstg	Storage temperature range			−65~+150	℃

Note 2 : For M66320FP, a derating of 7mW/℃ should be made when Ta≧75℃

RECOMMENDED OPERATING CONDITIONS (Ta=−40~+85℃)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating temprature range	−40		+85	℃
t_r, t_f	Input rise time, fall time S-IN, $\overline{OE}$	0		500	ns

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5V~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				T_a=25℃			T_a=−40~+85℃		
				Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage S-IN, $\overline{OE}$	V_O=0.1V, V_{CC}−0.1V $\lvert I_O \rvert$ = 20μA		0.70×V_{CC}			0.70×V_{CC}		V
V_{IL}	Low-level input voltage S-IN, $\overline{OE}$	V_O=0.1V, V_{CC}−0.1V $\lvert I_O \rvert$ =20μA				0.30×V_{CC}		0.30×V_{CC}	V
V_{T+}	Positive threshold voltage CK, $\overline{LE}$	V_O=0.1V, V_{CC}−0.1V $\lvert I_O \rvert$ = 20μA		0.35×V_{CC}		0.8×V_{CC}	0.35×V_{CC}	0.8×V_{CC}	V
V_{T-}	Negative threshold voltage CK, $\overline{LE}$	V_O=0.1V, V_{CC}−0.1V $\lvert I_O \rvert$ = 20μA		0.2×V_{CC}		0.65×V_{CC}	0.2×V_{CC}	0.65×V_{CC}	V
V_{OH}	High-level output voltage $\overline{Q_1}\sim\overline{Q_{12}}$, SQ_{12}	V_I=V_{T+}, V_{T-}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
		V_{CC}=4.5V	I_{OH}=−1.0mA	4.1			4.0		
V_{OL}	Low-level output voltage $\overline{Q_1}\sim\overline{Q_{12}}$, SQ_{12}	V_I=V_{T+}, V_{T-}	I_{OL}=20μA			0.1		0.1	V
		V_{CC}=4.5V	I_{OL}=1.0mA			0.4		0.5	
I_{CC}	Static supply current	When input is open, V_{CC}=5.5V				20.0		200.0	μA
		V_I=V_{CC}, GND, V_{CC}=5.5V				1.5		2.2	mA

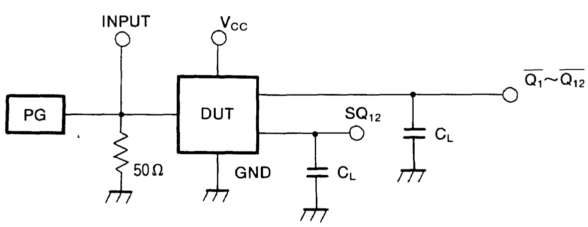
SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum repetitive frequency	C_L=15pF (Note 3)	3			2.5		MHz
t_{PLH}	Low-to high-level and high-to low-level				300		400	ns
t_{PHL}	output propagation time from CK to SQ_{12}				300		400	ns
t_{PLH}	Low-to high-level and high-to low-level				300		400	ns
t_{PHL}	output propagation time from CK to $\overline{Q_1}\sim\overline{Q_{12}}$				300		400	ns
t_{PLH}	Low-to high-level and high-to low-level				300		400	ns
t_{PHL}	output propagation time from $\overline{OE}$ to $\overline{Q_1}\sim\overline{Q_{12}}$				300		400	ns
t_{PLH}	Low-to high-level and high-to low-level				300		400	ns
t_{PHL}	output propagation time from $\overline{LE}$ to $\overline{Q_1}\sim\overline{Q_{12}}$				300		400	ns

TIMING REQUIREMENTS (V_{CC}= 5 V)

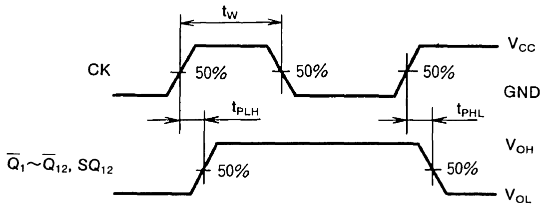
Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40~+85℃		
			Min	Typ	Max	Min	Max	
t_W	CK pulse width		160			200		ns
t_{SU}	S-IN setup time with respect to CK		80			100		ns
t_h	S-IN hold time with respect to CK		80			100		ns

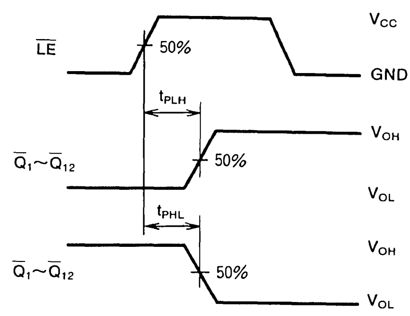
Note 3 : Test circuit

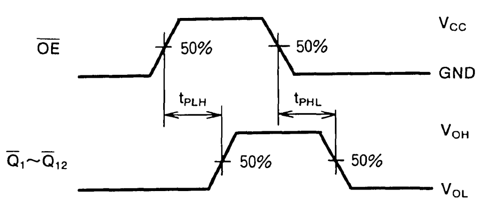


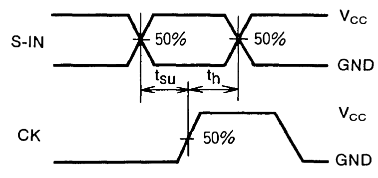
(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=6ns, t_f=6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM









BAND COMPRESSION AND EXPANSION CONTROLLER

DESCRIPTION

M66330SP/FP is a high speed CODEC (Coder and Decoder) LSI that encodes image data to MH or MR data and decodes MH or MR data to image data under control of system MPU (Micro Processor Unit).

Operating modes, coding and decoding method (MH, MR or MMR), pixels per each line and image data processing can be set by commands from system MPU.

For high speed operation, M66330 includes 3 line memories of 2048-bit and MR mode detection circuit as well as serial bus for image data input and output.

FEATURES

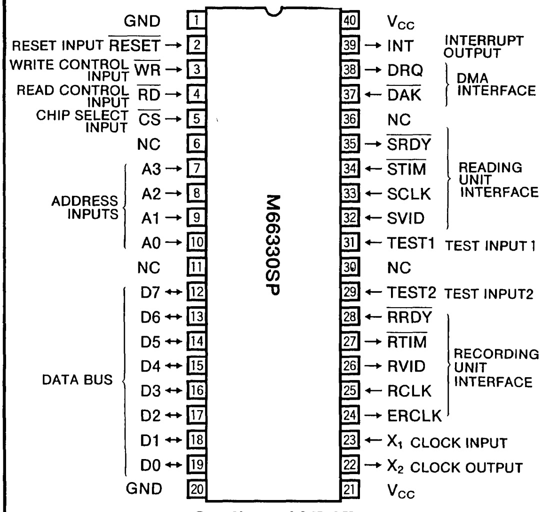
- Various operating mode
  - G2 data transmission/receive mode
  - G3 data transmission/receive mode (MH/MR/MMR)
  - G2 data to G3 data conversion mode
  - G3 data to G2 data conversion mode
  - Copying mode
- Image data processing function
  - Selectable pixels per line : 2048 bit (max)
  - Image data reduction (B4 size to A4 size)
  - Journal output
  - Header line output indicating transmitter
  - Received stamp output
- High-speed operation
  - Serial bus for image data input/output
  - 3 line memories of 2048-bit included
  - Run length detection circuit for MH coding
  - MR mode detection circuit for MR coding
  - Control terminals for external DMA controller

APPLICATION

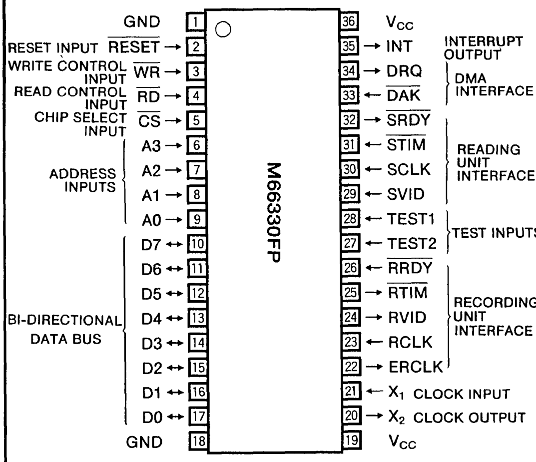
Facsimile

The specifications are subject to change without notice

PIN CONFIGURATION (TOP VIEW)



Outline 40P4B



Outline 36P2R

NC : NO CONNECTION

BAND COMPRESSION AND EXPANSION CONTROLLER UNDER DEVELOPMENT

FUNCTION

(1) Pixels per line and reduction of image data can be selected.
Pixel 2048-bit max. (Equivalent to 8 pel/mm on B4 paper)
Reduction B4→A4

(2) The following operating modes can be set by MPU command.

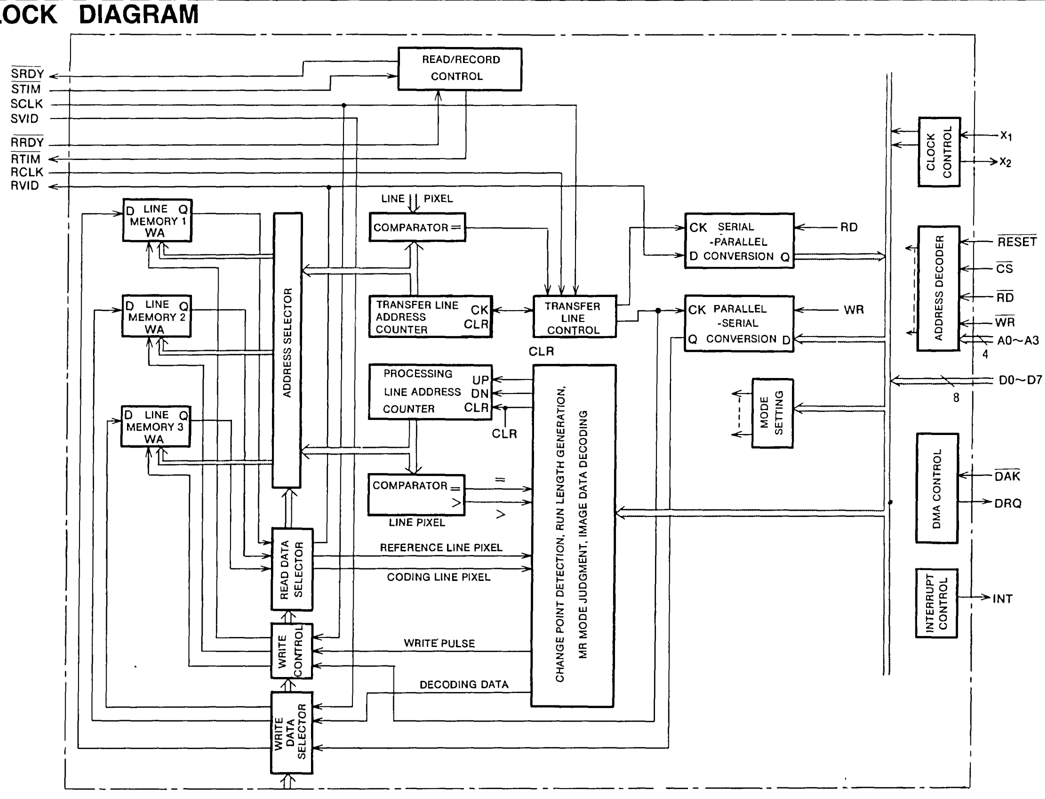
- Copy mode
- G3→G2 conversion mode
- G2→G3 conversion mode
- G3 receiving mode
- G2 receiving mode
- G3 transmission mode
- G3 transmission mode

Continuous conversions of G3→G2 and G2→G3 will result in G3 to G3 conversion. (Code method, paper size)

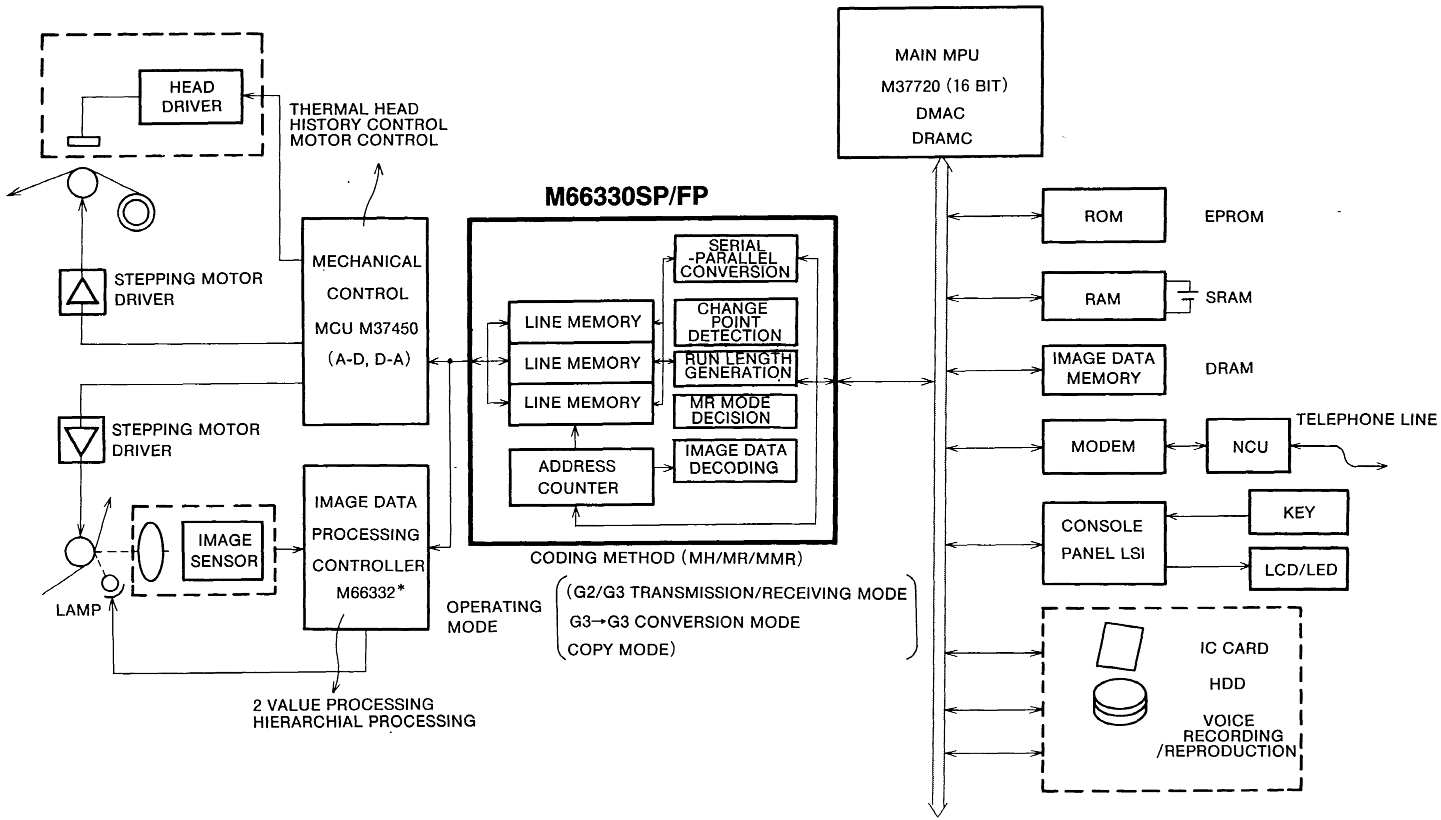
(3) The operation of this controller and the MPU in G3 code/decode processing (MH and MR methods) is shown in the following table.

Method	Process	Controller	MPU
MH	Coding	Generates black and white run length data from the image data from the read sensor and sends it to the MPU	Encodes black and white run length data from the controller to MH code and sends it to the modem
	Decoding	Generates image data from the black and while run length data from the MPU and outputs it to the recording unit	Converts the MH codes from the modem into black and while run length data and sends it to the controller
MR	Coding	Finds the MR mode of the image data from the read sensor and sends it to the MPU. Also sends run length data in the horizontal mode	Encodes MR mode from the controller to MR code and sends it to the modem.
	Decoding	Generates the image data from the MR mode from the MPU and outputs it to the recording unit	Converts MR codes from the modem into MR mode and sends it to the controller

BLOCK DIAGRAM



APPLICATION EXAMPLE



* : Under development

M66510P/FP

R-TYPE LASER DIODE DRIVER

The specifications are subject to change without notice

DESCRIPTION

The M66510P/FP is an integrated circuit to drive a semiconductor laser diode (Mitsubishi R-type laser), whose cathode is connected to the stem. The laser drive current is set by applying the externally rated voltage. The laser can be driven by a maximum 120mA current. The device operates with a single 5V power supply. The laser drive current can be switched at 20Mbit/s.

FEATURES

- Cathode-stem type semiconductor laser diode drive.
- Laser current cut-off pin.
- Comparator output for a laser power monitoring. (TTL level)
- Analog output for a laser power monitoring.
- High-speed switching. (20Mbit/s)
- High drive current. (120mA max)
- Single 5V power supply.

APPLICATION

Laser beam printer.

FUNCTION

The M66510P/FP is a semiconductor laser diode driver to drive a cathode-stem type semiconductor laser (Mitsubishi R-type laser). Use of R-type laser makes fixing the laser directly to the equipment easy and improves the heat radiation effect.

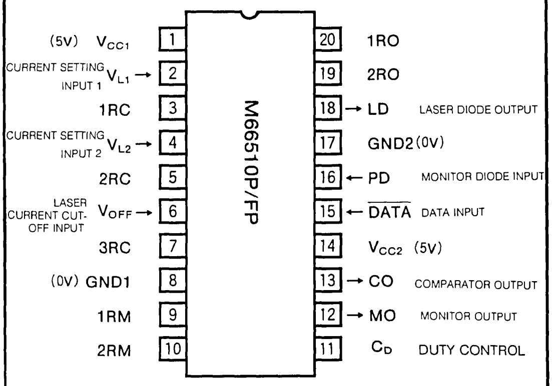
The M66510P/FP drives a laser with the rated current according to the external voltage. Two independent current setting inputs enable accurate drive current setting.

To detect the operating laser output power, the monitor diode's current is converted to the differential voltage by an externally connected resistor and is output as an analog voltage value. The compared result with the internal reference voltage is output as TTL-level.

The M66510P/FP is optimal for APC (Auto Power Control) systems in semiconductor lasers that use microcomputers. (See Application Example.)

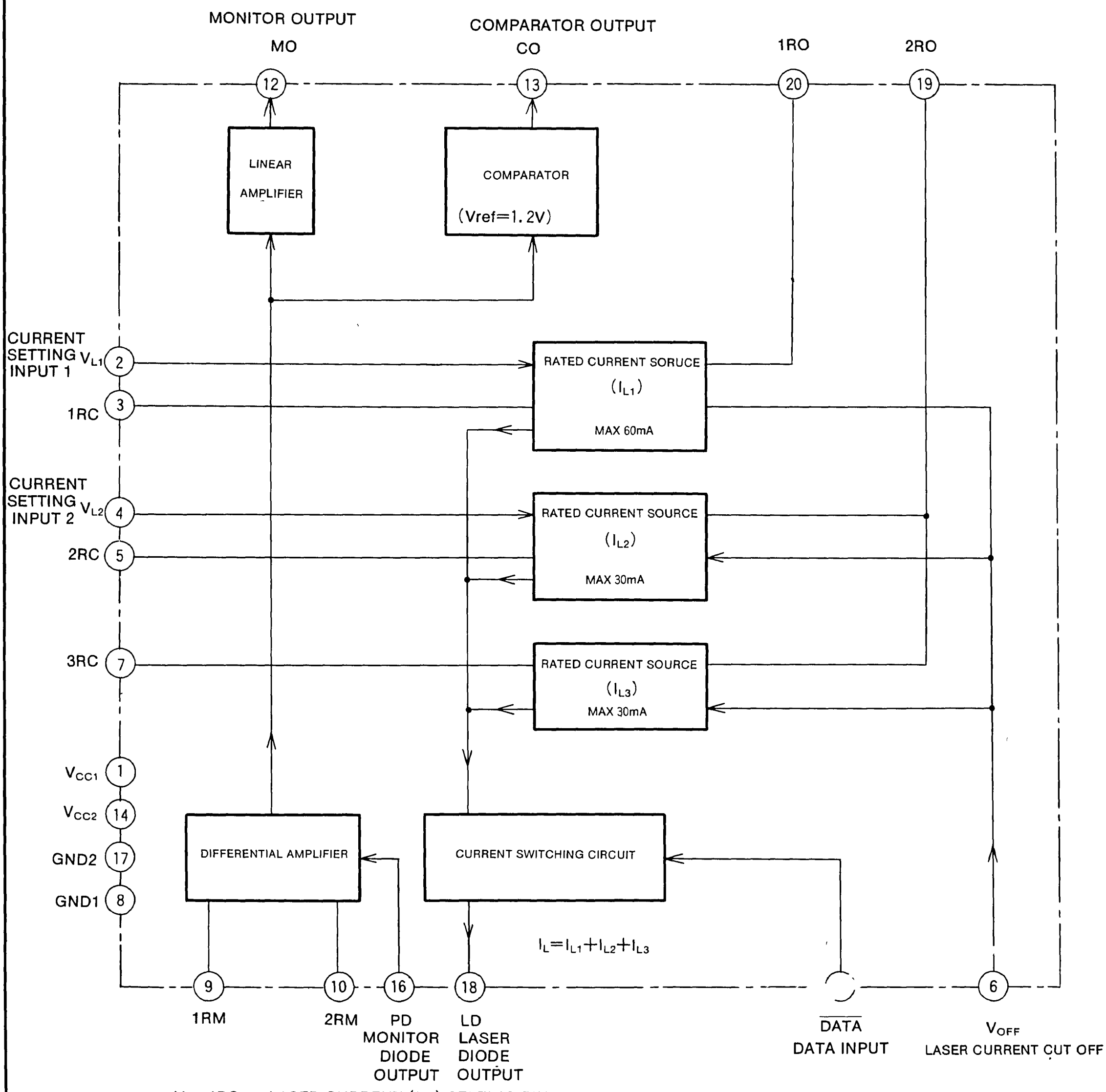
The laser current cut-off pin prevents excess current applied to the laser at power-on.

PIN CONFIGURATION (TOP VIEW)



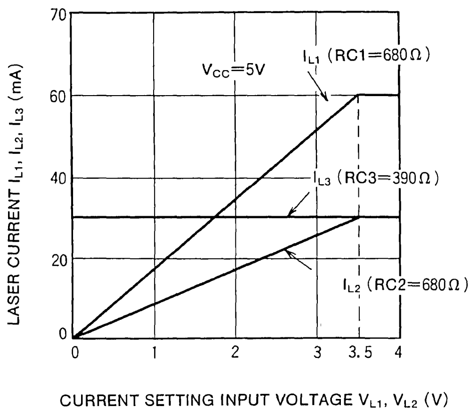
Outline 20P4
20P2N

BLOCK DIAGRAM

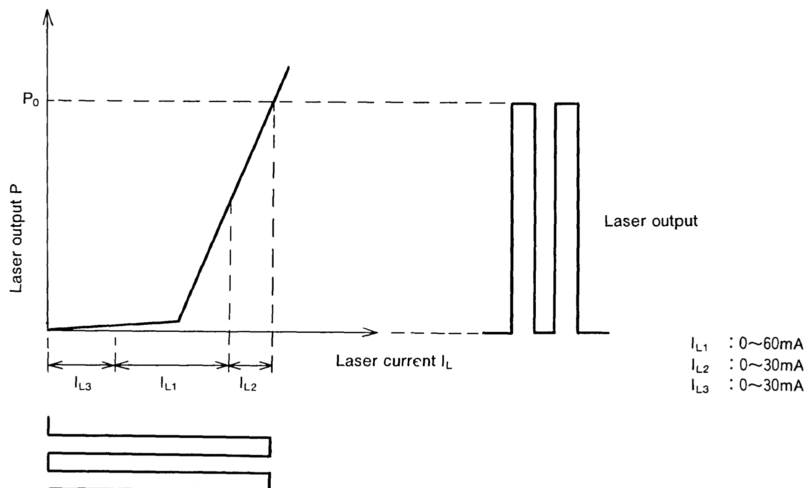


V_{L1}, 1RC : LASER CURRENT (I_{L1}) SETTING PIN
V_{L2}, 2RC : LASER CURRENT (I_{L2}) SETTING PIN
3RC : LASER CURRENT (I_{L3}) SETTING PIN
V_{CC1}, GND1 : INTERNAL ANALOG POWER SUPPLY PIN
V_{CC2}, GND2 : INTERNAL DIGITAL POWER SUPPLY PIN

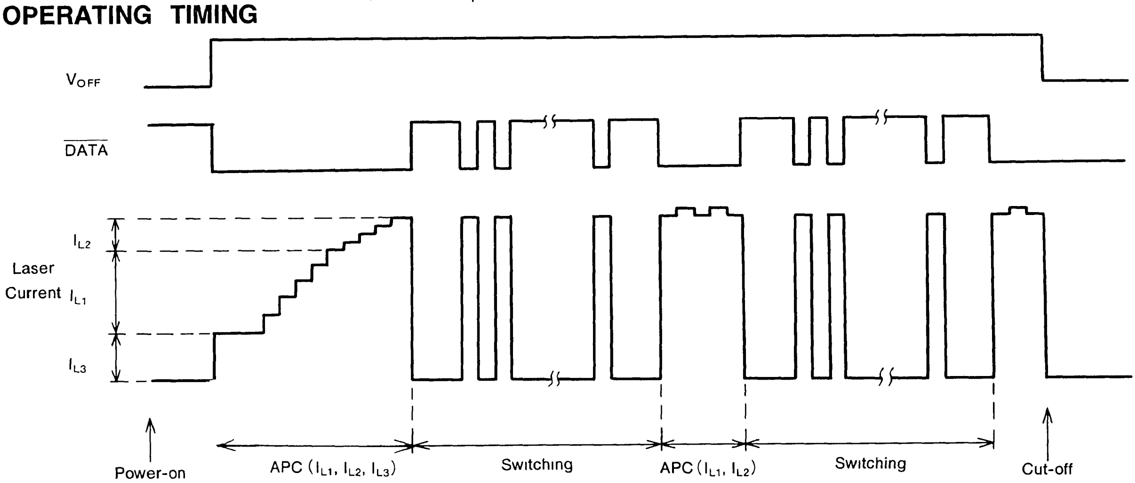
CURRENT SETTING INPUT VOLTAGE VS LASER CURRENT



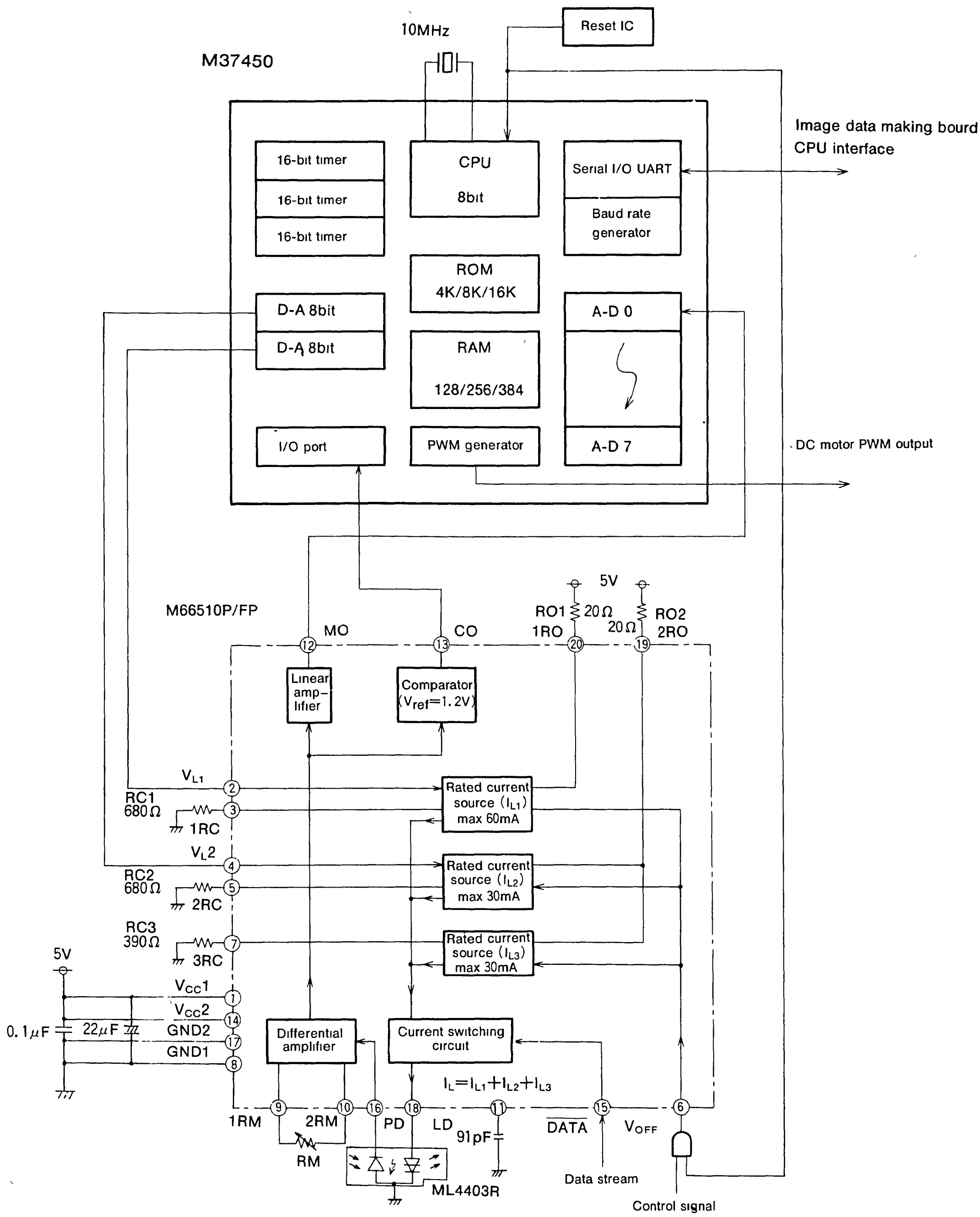
OPERATING WAVEFORM



OPERATING TIMING



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

MITSUBISHI 〈DIGITAL ASSP〉

M66700P

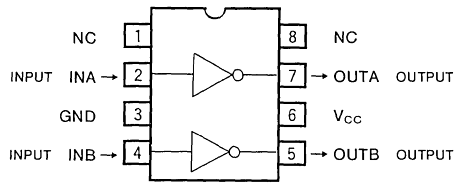
DUAL HIGH-SPEED CCD CLOCK DRIVER

DESCRIPTION
The M66700P is a semiconductor integrated circuit for high-speed driving of transfer clock of a CCD linear image sensor used for facsimiles or copying machines. TTL-level input enables direct drive in the IC of TTL system.

FEATURES
- Output amplitude ································12V
- High-speed rise/fall waveform
  $t_r=t_f=33ns$ (typ.) $C_L=1000pF$
- High output high-level voltage ·········· ($V_{CC}-1$)V (min.)
- Low output low-level voltage ····················0.5V (max.)
- Direct drive is possible by TTL-level input.

APPLICATION
CCD image sensor driver for facsimiles, image scanners and copying machines

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

NC : NO CONNECTION

ABSOLUTE MAXIMUM RATINGS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+15	V
V_I	Input voltage		−0.5~+15	V
V_O	Output voltage	When the output is high-level	V_{CC}	V
P_d	Power dissipation (Note 1)	T_a=25℃	950	mW
Tstg	Storage temperature range		−65~+150	℃

Note 1. Derating of 7.7mW/℃ should be made at $T_a \geqq 25$℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Limits Min	Limits Nom	Limits Max	Unit
V_{CC}	Supply voltage	10.8	12.0	13.2	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
T_{opr}	Operating temperature range	0		70	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=12V±10%, T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ (*)	Limits Max	Unit
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IC}=-18mA$		−0.82	−1.5	V
V_{OH}	High-level output voltage	$V_I=0.4V$, $I_{OH}=-1mA$	$V_{CC}-1$	11.3		V
V_{OL}	Low-level output voltage	$V_I=2.0V$, $I_{OL}=+1mA$		0.23	0.5	V
I_{IH}	High-level input current	$V_I=5.5V$		<1	100	μA
I_{IL}	Low-level input current	$V_{CC}=12V$, $V_I=0.4V$		−0.13	−0.4	mA
I_{CCH}	High-level supply current	$V_{CC}=12V$, $V_I=0.0V$		2.2	5	mA
I_{CCL}	Low-level supply current	$V_{CC}=12V$, $V_I=4.5V$		29.2	38	mA

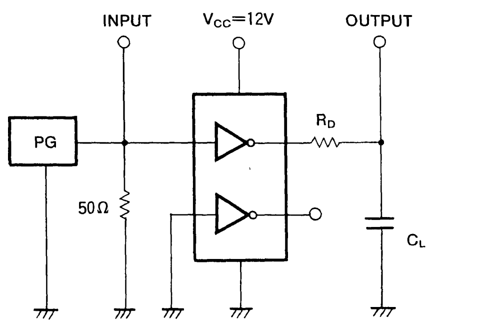
(*) All typical values are at V_{CC}=12V, T_a=25℃

SWITCHING CHARACTERISTICS (V_{CC}=12V, T_a=25℃, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ (*)	Limits Max	Unit
t_{on}	Turn-on time	V_{CC}=12V		7	30	ns
t_{off}	Turn-off time	R_D=10Ω (Note 2)		10	30	ns
t_r	Rise time	C_L=1000pF		34	50	ns
t_f	Fall time	See test diagram		32	50	ns

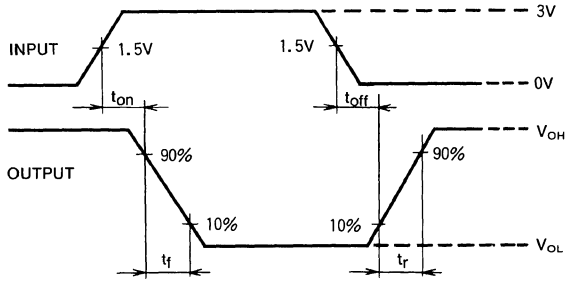
Note 2. If the M66700P is operated at high speed, overshooting or undershooting may occur. To reduce them, connect a dumping resistor of R_D=10~30Ω to the output.
(*) All typical values are at V_{CC}=12V, T_a=25℃

TEST CIRCUIT



The output conditions of PG (pulse generator) are as follows:

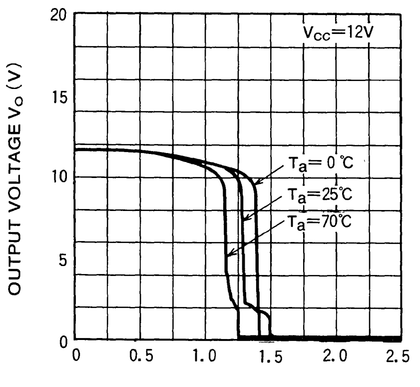
Rise time	t_r≦6ns
Fall time	t_f≦6ns
Repetitive frequency	PRR=1MHz
Pulse width	t_w=500ns
Pulse amplitude	V_P=3V_{P-P}



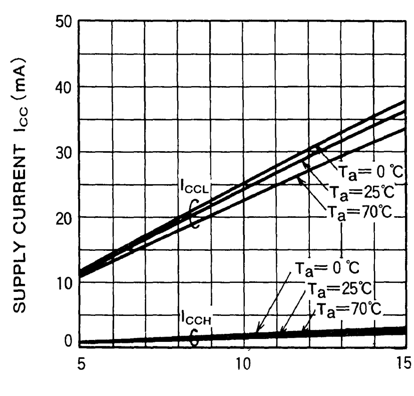
Voltage waveform

TYPICAL CHARACTERISTICS

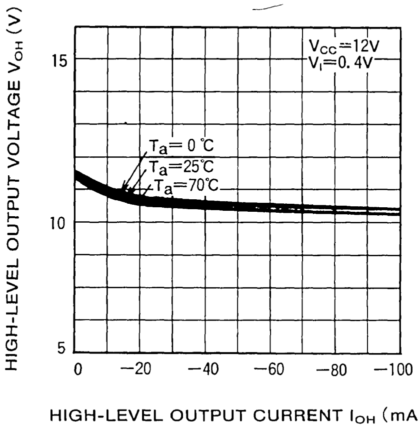
I/O TRANSMISSION CHARACTERISTICS



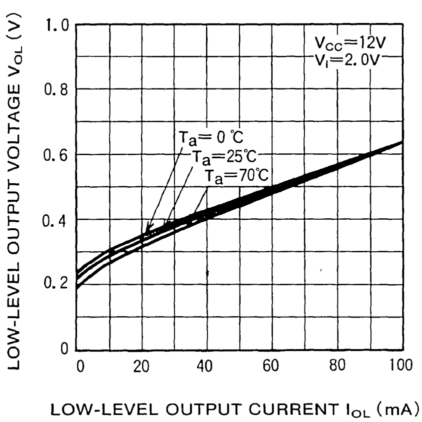
SUPPLY CURRENT VS SUPPLY VOLTAGE



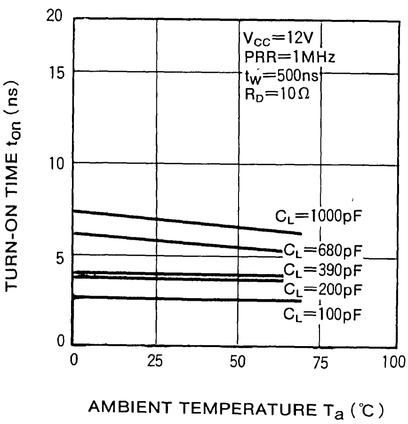
HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



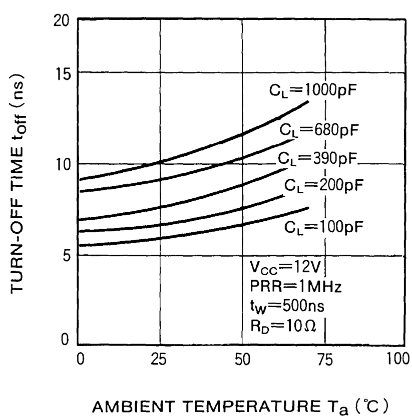
LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



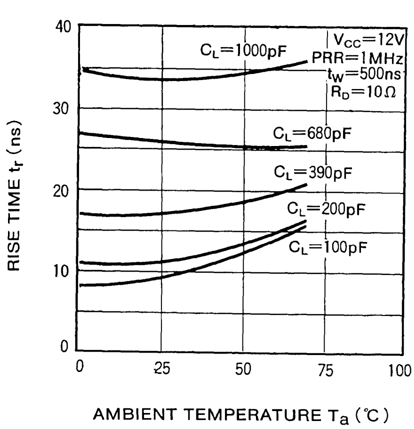
TURN-ON TIME VS AMBIENT TEMPERATURE



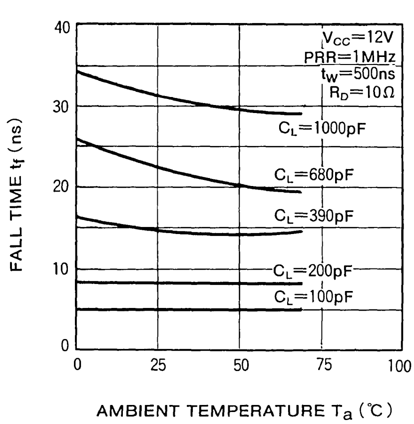
TURN-OFF TIME VS AMBIENT TEMPERATURE



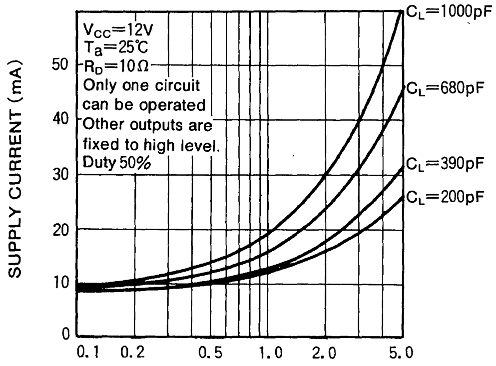
RISE TIME VS AMBIENT TEMPERATURE



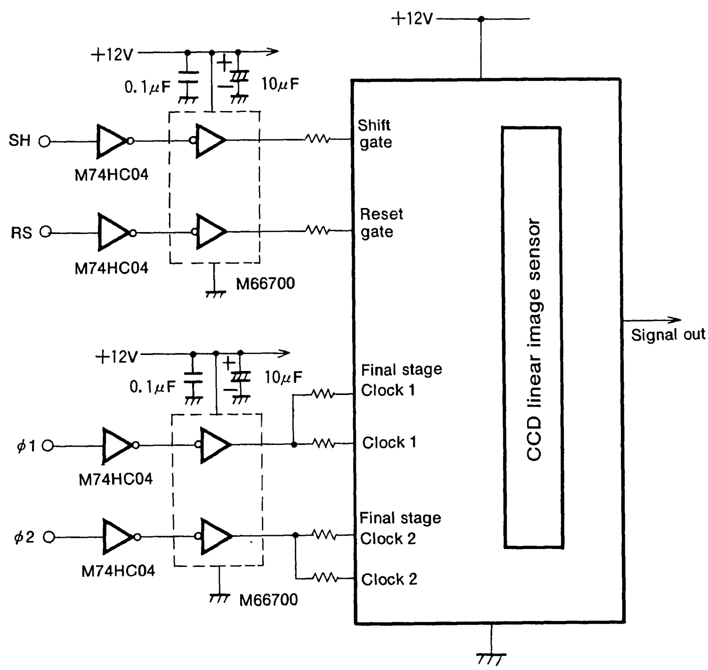
FALL TIME VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS OPERATING FREQUENCY



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M66705P/FP

QUADRUPLE HIGH-SPEED CCD CLOCK DRIVER

DESCRIPTION

The M66705P/FP is a semiconductor integrated circuit for high-speed driving of transfer clock of a CCD linear image sensor used for facsimiles or copying machines. TTL-level input enables direct drive in the IC of TTL system.

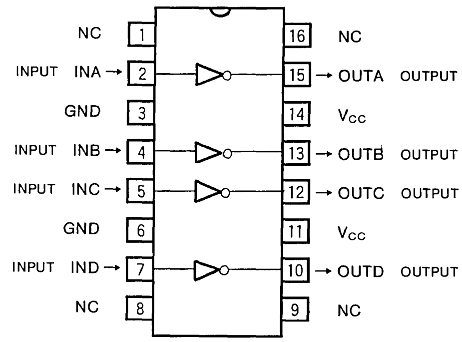
FEATURES

- Output amplitude ······ 12V
- High-speed rise/fall waveform ······ $t_r = t_f = 33ns$ (typ.) $C_L = 1000pF$
- High output high-level voltage ······ $(V_{CC} - 1)V$ (min.)
- Low output low-level voltage ······ 0.5V (max.)
- Direct drive is possible by TTL-level input.

APPLICATION

CCD image sensor driving for facsimiles, image scanners and copying machines

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N

NC : NO CONNECTION

ABSOLUTE MAXIMUM RATINGS ($T_a = 0 \sim 70°C$, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			−0.5 ~ +15	V
V_I	Input voltage			−0.5 ~ +15	V
V_O	Output voltage	When the output is high-level		V_{CC}	V
P_d	Power dissipation (Note 1)	DIP	$T_a = 25°C$	1100	mW
		SOP	$T_a = 25°C$	640	
T_{stg}	Storage temperature range			−65 ~ +150	°C

Note 1. Derating should be made according to the attached thermal derating characteristics at $T_a \geqq 25°C$

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70°C$, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	10.8	12.0	13.2	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
T_{opr}	Operating temperature range	0		70	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12V \pm 10\%$, $T_a = 0 \sim 70°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ (*)	Max	
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IC} = -18mA$		−0.82	−1.5	V
V_{OH}	High-level output voltage	$V_I = 0.4V$, $I_{OH} = -1mA$	$V_{CC} - 1$	11.3		V
V_{OL}	Low-level output voltage	$V_I = 2.0V$, $I_{OL} = +1mA$		0.23	0.5	V
I_{IH}	High-level input current	$V_I = 5.5V$		<1	100	μA
I_{IL}	Low-level input current	$V_{CC} = 12V$, $V_I = 0.4V$		−0.13	−0.4	mA
I_{CCH}	High-level supply current	$V_{CC} = 12V$, $V_I = 0.0V$		4.4	6	mA
I_{CCL}	Low-level supply current	$V_{CC} = 12V$, $V_I = 4.5V$		58.5	75	mA

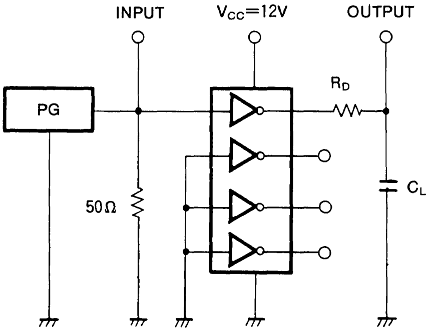
(*) All typical values are at $V_{CC} = 12V$, $T_a = 25°C$

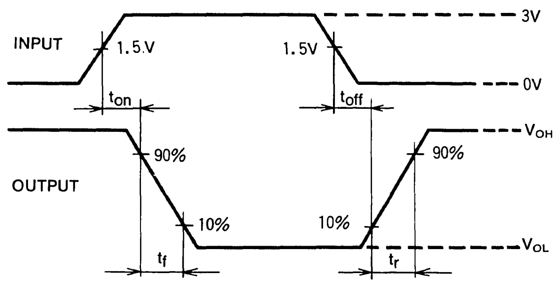
SWITCHING CHARACTERISTICS (V_{CC}=12V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.(＊)	Max	
t_{on}	Turn-on time	V_{CC}=12V		7	30	ns
t_{off}	Turn-off time	R_D=10Ω (Note 2)		10	30	ns
t_r	Rise time	C_L=1000pF		34	50	ns
t_f	Fall time	See test diagram		32	50	ns

Note 2. If the M66705 is operated at high speed, overshooting or undershooting may occur. To reduce them, connect a dumping resistor of R_D=10～30 Ω to the output.
(＊)All typical values are at V_{CC}=12V, T_a=25℃.

TEST CIRCUIT





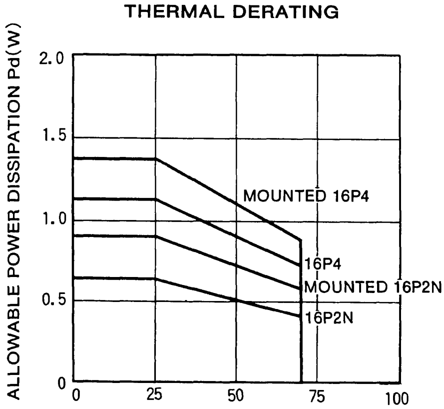
Voltage waveform

The output conditions of PG (pulse generator) are as follows·

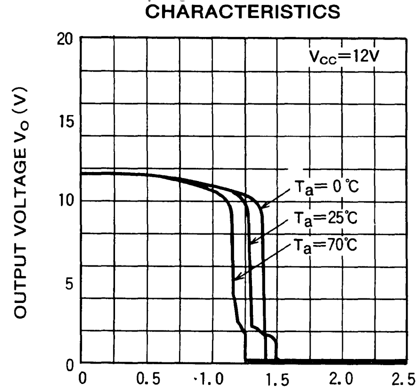
Rise time	$t_r \leq 6ns$
Fall time	$t_f \leq 6ns$
Repetitive frequency	PRR=1MHz
Pulse width	t_W=500ns
Pulse amplitude	$V_P=3V_{P-P}$

TYPICAL CHARACTERISTICS

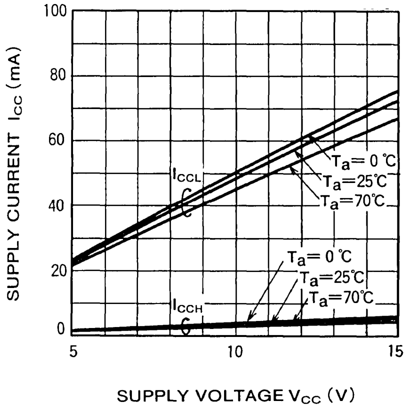
THERMAL DERATING



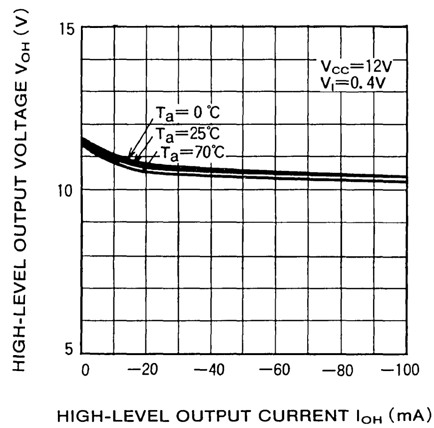
I/O TRANSMISSION CHARACTERISTICS



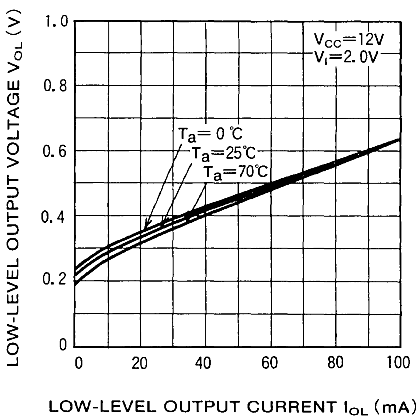
SUPPLY CURRENT VS SUPPLY VOLTAGE



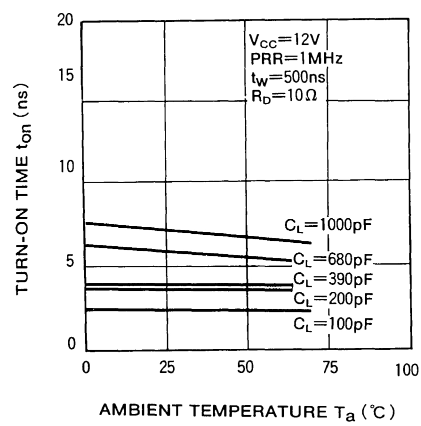
HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



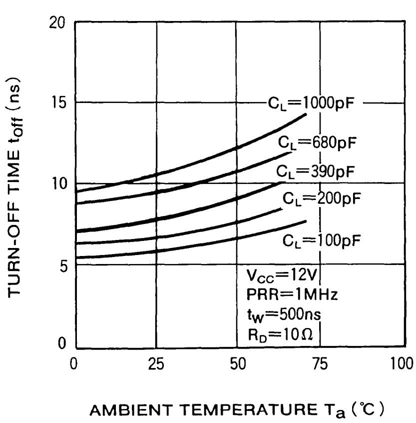
LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



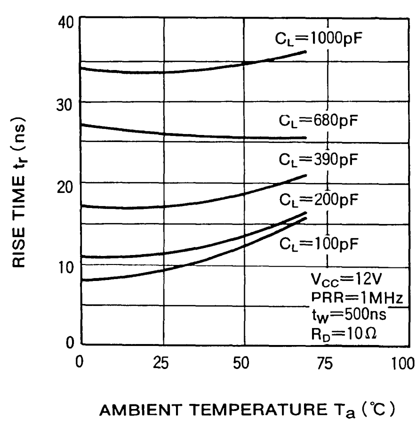
TURN-ON TIME VS AMBIENT TEMPERATURE



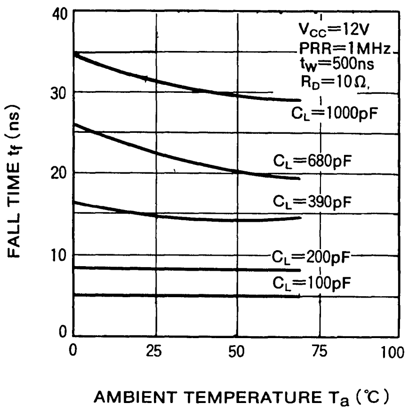
TURN-OFF TIME VS AMBIENT TEMPERATURE



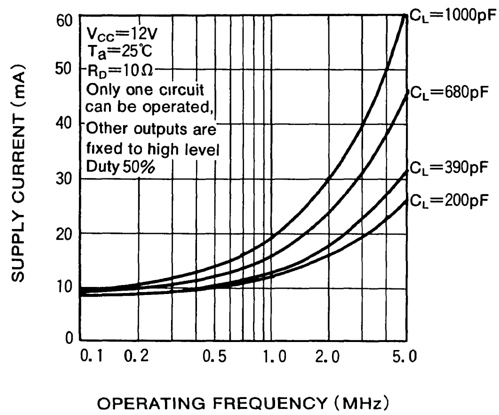
RISE TIME VS AMBIENT TEMPERATURE



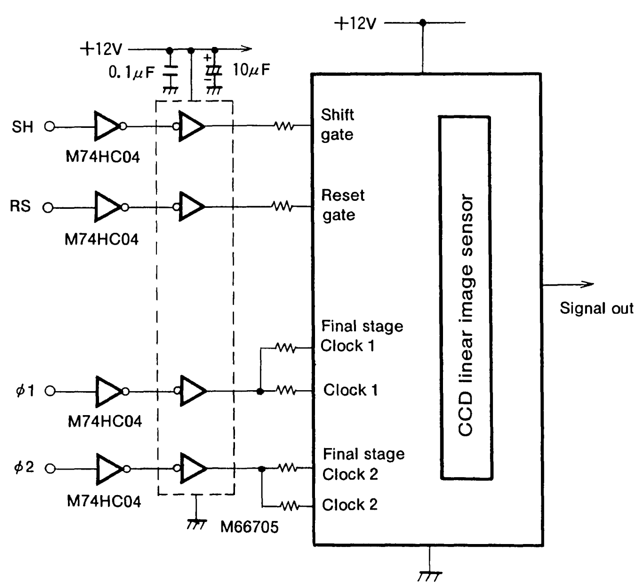
FALL TIME VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS OPERATING FREQUENCY



APPLICATION EXAMPLE



LINE INTERFACE IC

M5A26LS29P

QUADRUPLE 3-STATE SINGLE ENDED LINE DRIVER

DESCRIPTION

The M5A26LS29P is a semiconductor integrated circuit containing 4 line drivers for use with unbalanced digital data transmission, which meets EIA Standards RS-423-A.

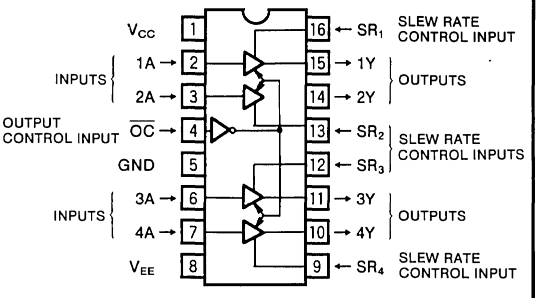
FEATURES

- Output characteristics meet EIA Standards RS-423-A
- Each driver has slew rate control input
- Capable of driving large output capacitive load
- Limitting circuit for short-circuit output current is provided
- 3-state outputs
- Input characteristics are compatible with TTL circuits

APPLICATION

For use as a data transmission interface in digital equipment

PIN CONFIGURATION (TOP VIEW)



OUTLINE 16P4

FUNCTIONAL DESCRIPTION

Input A has the equivalent electrical characteristics, capable of direct drive with integrated circuits of TTL system.
Output control input $\overline{OC}$ is common to all 4 drivers.
Slew rate control input SR is provided for each output and slew rate can be controlled by varying external capacitance connected between SR and output Y. Refer to the specifications. The slew rate is controlled based on transmisson line length and transmisson speed. Controling slew rate reduces crosstalk to other receivers connected to the line.
Y has source current of −60mA (typ) and sink current of 60mA (typ), capable of driving transmission line and large capacitive load. Positive power supply V_{CC} and negative power supply V_{EE} are used and Y changes symmetrically to the ground potential. When $\overline{OC}$="H" or power is off, Y is in a high-impedance state in the range of −10V to +10V and results in less loading of the bus line.

This integrated circuit is suitable for data transmission interface in digital equipment and the output characteristics meet EIA Standards RS-423-A. Refer to Table 1. The M5A26LS32AP is availabe as a receiver which meets this standard. The transmission form is unbalanced type. Refer to TYPICAL APPLICATION.

FUNCTION TABLE (Note 1)

A	$\overline{OC}$	Y
L	L	L
H	L	H
X	H	Z

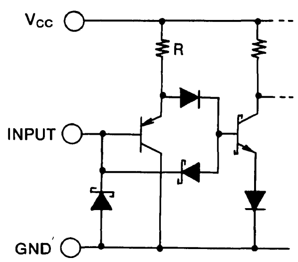
Note 1 : X : irrelevant
Z : high-impedance

Table 1 Eia standards RS-423-A

	Parameter	RS-423-A	M5A26LS29P Corresponding parameters (symbol)
Common	Transmission form	Unbalanced	Output Y
	Maximum transmission distance	1200m	
	Maximum transmission speed	100Kbit/s	S_{rc}
Driver	Maximum output voltage (no load)	±6V	V_O, $\overline{V_O}$
	Minimum output voltage (loaded)	±3.6V	V_T, $\overline{V_T}$
	Minimum output resistance (power off)	100μA(−6V<V_O<+6V)	I_{x+}, I_{x-}
	Maximum short-circuit output current	±150mA	I_{S+}, I_{S-}
	Slew rate	Controllable	S_{rc}
Receiver	Input resistance	≧4kΩ	
	Maximum input threshold	−0.2～+0.2V	
	Maximum input voltage	−12～+12V	

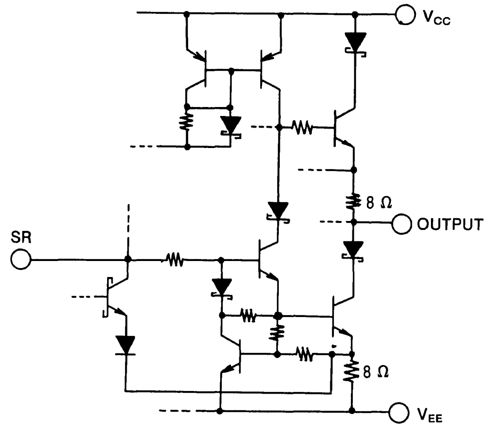
QUADRUPLE 3-STATE SINGLE ENDED LINE DRIVER

INPUT EQUIVALENT CURCUIT



INPUT	R
A	12kΩ
$\overline{OC}$	6.5kΩ

OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Positive supply voltage		0~+7	V
V_{EE}	Negative supply voltage		0~−7	V
V_I	Input voltage		−0.5~+15	V
V_O	Output voltage	When power supply is off	−15~+15	V
P_d	Power dissipation	T_a=25℃ (Note 2)	600	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2: Derate as 9mW/℃ when T_a≧40℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Positive power supply	4.75	5	5.25	V
V_{EE}	Negative power supply	−4.75	−5	−5.25	V
V_I	Input voltage	0		5.5	V
V_O	Output voltage (power off)	−10		+10	V
Topr	Operating free-air ambient temperature range	−20		+75	℃

QUADRUPLE 3-STATE SINGLE ENDED LINE DRIVER

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, V_{EE}=−5V±5%, T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Typ*	Max	Unit
V_O	Output voltage	$R_L=\infty$	V_I=2.4V	3.9(Note 3)	4.4	6.0	V
$\overline{V_O}$			V_I=0.4V	−3.9(Note 4)	−4.4	−6.0	V
V_T	Output voltage	R_L=450Ω	V_I=2.4V	3.6	4.1		V
$\overline{V_T}$			V_I=0.4V	−3.6	−4.1		V
$\|V_T\|-\|\overline{V_T}\|$	Output unbalance	$\|V_{CC}\|=\|V_{EE}\|$, R_L=450Ω			0.02	0.4	V
I_{X+}	Output leak current (power off)	$V_{CC}=V_{EE}$= 0 V	V_O=10V		2.0	100	μA
I_{X-}			V_O=−10V		−2.0	−100	μA
I_{S+}	Short-circuit output current	V_O= 0 V	V_I=2.4V		−60	−150	mA
I_{S-}			V_I=0.4V		60	150	mA
I_{slew}	Slew-control current	$V_{SLEW}=V_{EE}$+0.9V			±110		μA
I_{CC}	Positive supply current	V_I=0.4V, $R_L=\infty$			18	30	mA
I_{EE}	Negative supply current	V_I=0.4V, $R_L=\infty$			−10	−22	mA
I_O	Off-state output current	V_{CC}=5.25V	V_O=10V		2.0	100	μA
		V_{EE}=−5.25V	V_O=−10V		−2.0	−100	
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High-level input current	V_I=2.4V			1.0	40	μA
		V_I≤15V			10	100	
I_{IL}	Low-level input current	V_I=0.4V			−30	−200	μA
V_{IK}	Input clamp voltage	I_{IK}=−12mA				−1.5	V

* : All typical values are at V_{CC}=5V, V_{EE}=−5V, T_a=25℃, with maximum load

Note 3 : 4.0V minimum for T_a=0~75℃

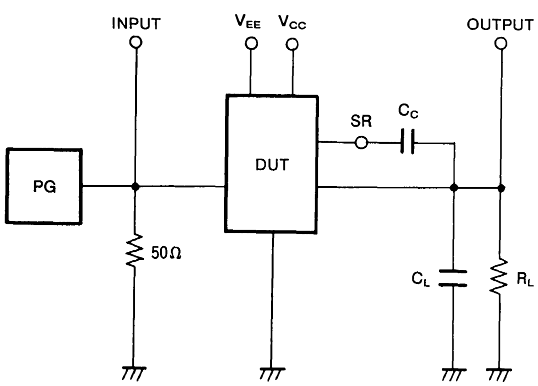
4 : −4.0V minimum for T_a=0~75℃

SWITCHING CHARACTERISTICS (V_{CC}=5V, V_{EE}=−5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Typ	Max	Unit
t_{TLH}	Low-to-high level, high-to-low level output transition time from input A to output Y	R_L=450Ω, C_L=500pF (Note 5)	C_C=50pF		3.0		μs
			C_C= 0 pF		150	300	ns
t_{THL}		R_L=450Ω, C_L=500pF (Note 5)	C_C=50pF		3.0		μs
			C_C= 0 pF		130	300	ns
S_{RC}	Slew rate coefficient	R_L=450Ω, C_L=500pF (Note 5)(Note 6)			0.06		μs/pF
t_{PLZ}	Output disable time from low level	R_L=450Ω, C_L=500pF, C_C= 0 pF (Note 5)			60	300	ns
t_{PHZ}	Output disable time from high level				80	350	ns
t_{PZL}	Output enable time to low level				180	350	ns
t_{PZH}	Output enable time to high level				120	300	ns

Note 6 : Slew rate coefficient=transition time (t_{TLH}, t_{THL})/external capacitance (C_C)

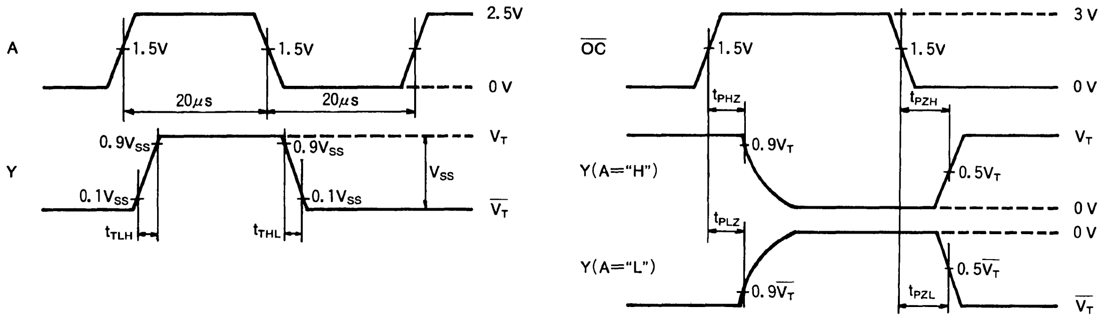
Note 5 : Test circuit



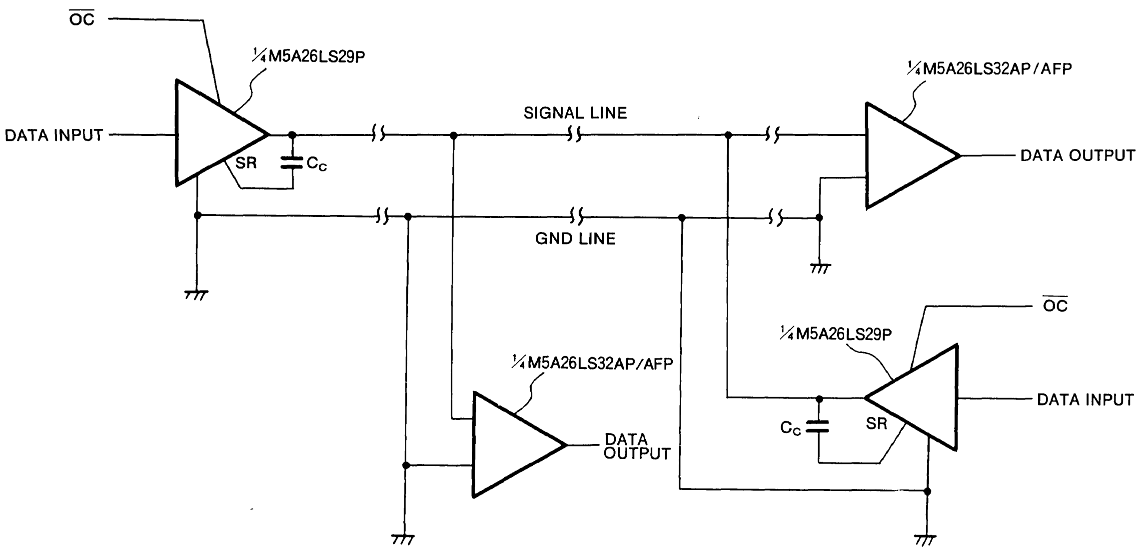
(1) The pulse generator (PG) has the following characteristics : PRR=25KHz, t_r≤10ns, t_f≤10ns, Z_O=50Ω

(2) C_L includes probe and jig capacitance

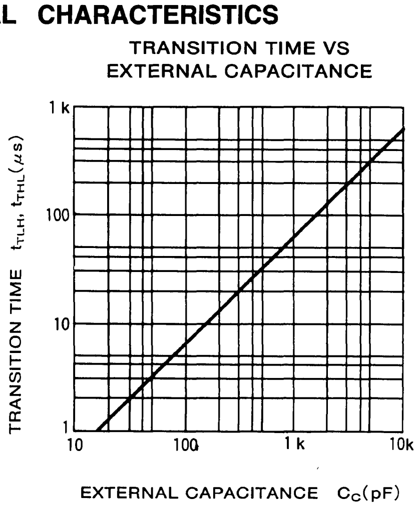
TIMING DIAGRAM



TYPICAL APPLICATION

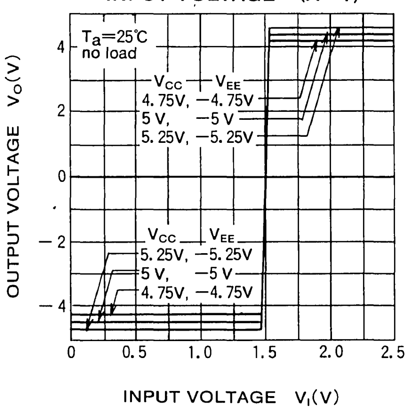


TYPICAL CHARACTERISTICS

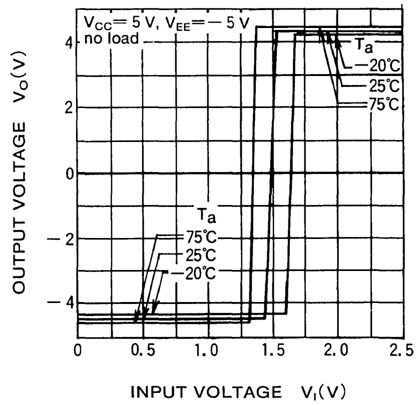


TYPICAL CHARACTERISTICS

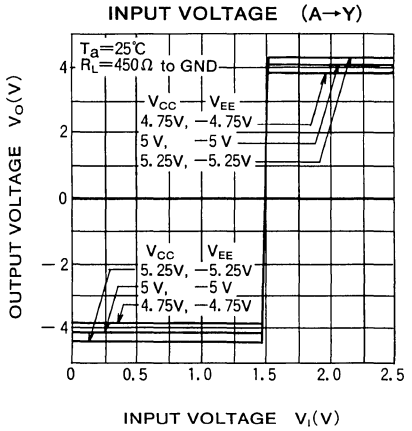
OUTPUT VOLTAGE VS
INPUT VOLTAGE (A→Y)



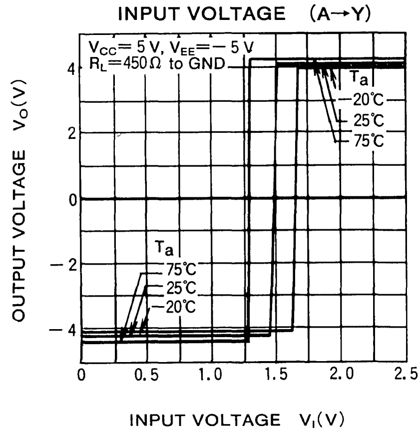
OUTPUT VOLTAGE VS
INPUT VOLTAGE (A→Y)



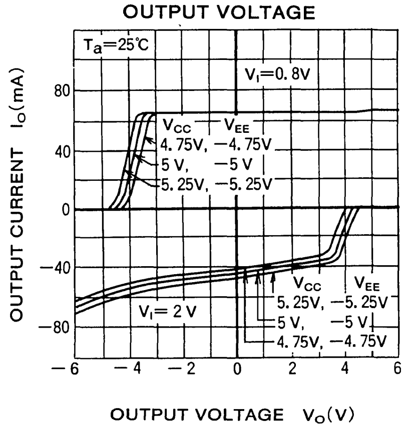
OUTPUT VOLTAGE VS
INPUT VOLTAGE (A→Y)



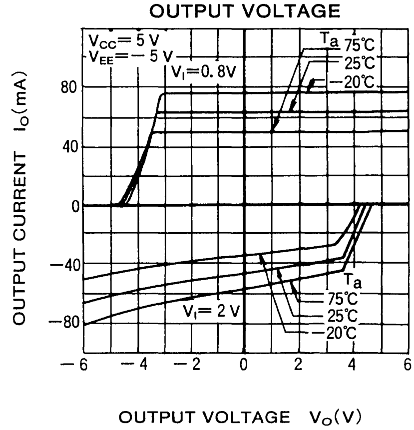
OUTPUT VOLTAGE VS
INPUT VOLTAGE (A→Y)



OUTPUT CURRENT VS
OUTPUT VOLTAGE



OUTPUT CURRENT VS
OUTPUT VOLTAGE



M5A26LS31P/FP

QUADRUPLE DIFFERENTIAL LINE DRIVER

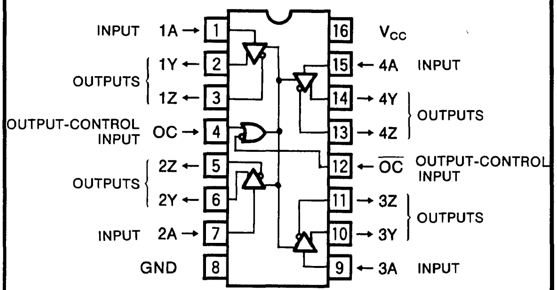
DESCRIPTION
The M5A26LS31P/FP is a semiconductor integrated circuit containing 4 line drivers for use with balanced digital data transmission, which meet EIA Standards RS-422-A.

FEATURES
- Output characteristics meet EIA Standards RS-422-A
- Connection of a termination resistor of 100Ω between complementary outputs is possible
- High output impedance in power-off conditions
- Limitting circuit for short-circuit output current is provided
- Input characteristics are compatible with TTL circuits
- Output control input is provided (OC, $\overline{OC}$)
- Operates from single 5V power supply

APPLICATION
For use as a data transmission interface in digital equipment

FUNCTIONAL DESCRIPTION
Input A can be driven directly with TTL circuits.
Output control inputs OC, $\overline{OC}$, are common to all 4 drivers.
Outputs Y and Z are complementary, where Y is non-inverted output, and Z inverted output. The sink current is 20mA, the source current is −20mA. Impedance matching can be made by connecting termination resistors to the transmission line whose characteristic impedance is 100Ω. When OC=low-level, and $\overline{OC}$=high-level, Y and Z are set to be in high-impedance state resulting in less loading of the bus line.
This integrated circuit is suitable for data transmission interface in digital equipment and the output characteristics meet EIA Standards RS-422-A. Refer to Table 1. The M5A26LS32AP/AFP is available as a receiver which meets this Standard. The transmission mode is of balanced. Refer to TYPICAL APPLICATION.

PIN CONFIGURATION (TOP VIEW)



OUTLINE 16P4 16P2N

FUNCTION TABLE (Note1)

A	OC	$\overline{OC}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Note 1 : Z : high-impedance
X : irrelevant

Table 1 Eia standards RS-422-A

	Parameter	RS-422-A	M5A26LS31P Corresponding parameters (Symbol)
Common	Transmission form	Balanced	Output Y, Z
	Maximum transmission distance	1200m	—
	Maximum transmission speed	10Mbit/s	I_{OH}, I_{OL}
Driver	Maximum output voltage (no load)	6V (Between outputs)	With V_{CC}=5V±5%, the voltage between outputs never becomes greater than 6V.
	Minimum output voltage (loaded)	2V (Between outputs)	V_{OH}, V_{OL}
	Minimum output resistance (power off)	100μA(−0.25V<V_O<+6V)	I_{X+}, I_{X-}
	Maximum short-circuit output current	±150mA	I_{OS}
	Slew rate	No need to control	
Receiver	Input resistance	≧4kΩ	
	Maximum input threshold	−0.2∼+0.2V	
	Maximum input voltage	−12∼+12V	

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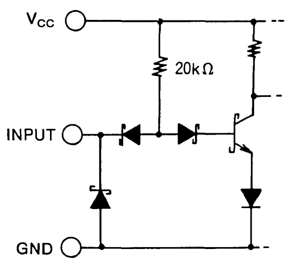
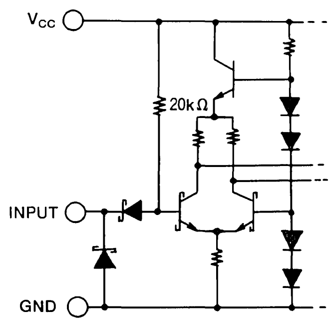
QUADRUPLE DIFFERENTIAL LINE DRIVER

INPUT EQUIVALENT CIRCUIT

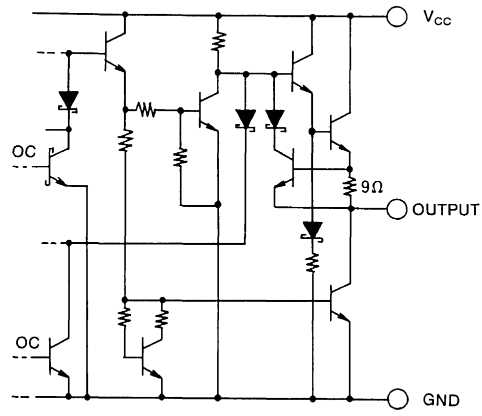


a) INPUT OC, $\overline{OC}$



b) INPUT A

OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7	V
V_I	Input voltage			−0.5～+7	V
V_O	Output voltage		When output is in high-impedance state	−0.5～+5.5	V
P_d	Power dissipation	DIP	T_a=25℃ (Note 2)	1000	mW
		SOP	T_a=25℃ (Note 3)	900	
Tstg	Storage temperature range			−65～+150	℃

Note 2 : For operation above 40℃ free-air temperature, derating of 9 mW/℃ is necessary.
3 : For operation above 25℃ free-air temperature, derating of 7.2mW/℃ is necessary

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Power supply			4.75	5	5.25	V
I_{OH}	High-level output current		V_{OH}≧2.5V	0		−20	mA
I_{OL}	Low-level output current		V_{OL}≦0.5V	0		20	mA
Topr	Operating free-air ambient temperature range	DIP	Dismounted	−20		+75	℃
		SOP	Mounted	−20		+70	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		DIP			0.8	V
			SOP			0.7	
V_{IK}	Input clamp voltage	V_{CC}=4.75V, I_{IK}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, I_{OH}=−20mA		2.5	2.9		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, I_{OL}=20mA			0.34	0.5	V
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_O=0.5V				−20	μA
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_O=2.5V				20	μA
I_{X+}	Output leak current when power off	V_{CC}= 0 V	V_O= 6 V			50	μA
I_{X-}			V_O=−0.25V			−50	μA
I_I	Maximum input current	V_{CC}=5.25V, V_I= 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.36	mA
I_{OS}	Short-circuit output current	V_{CC}=5.25V (Note 4)		−30	−75	−150	mA
I_{CC}	Supply current	V_{CC}=5.25V, All outputs disabled			43	85	mA

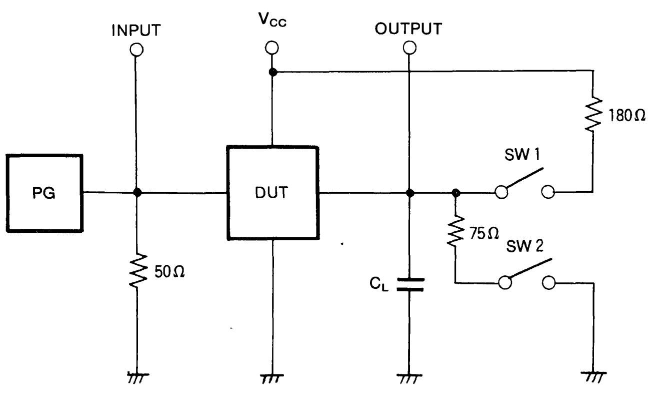
* : All typical values are at V_{CC}=5V, T_a=25℃

Note 4 : All measurements should be done quickly and not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test condtions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation	C_L=30pF (Note 5)		9	20	ns
t_{PHL}	time from input A to output Y			9	20	ns
Skew	Skew (Between outputs Y, Z)			1	6	ns
t_{PZH}	Output enable time to high level	C_L=30pF, R_L=75Ω (Note 5)		12	40	ns
t_{PZL}	Output enable time to low level	C_L=30pF, R_L=180Ω (Note 5)		21	45	ns
t_{PHZ}	Output disable time from high level	C_L=10pF (Note 5)		10	30	ns
t_{PLZ}	Output disable time from low level			10	35	ns

Note 5 : Test circuit



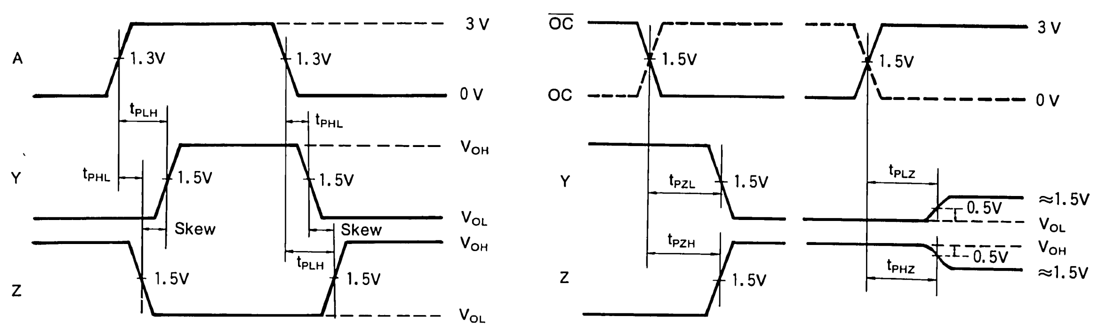
Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics :
PRR=1MHz, t_r≦15ns, t_f≦ 6 ns, V_P=3V_{P-P}, Z_O=50Ω

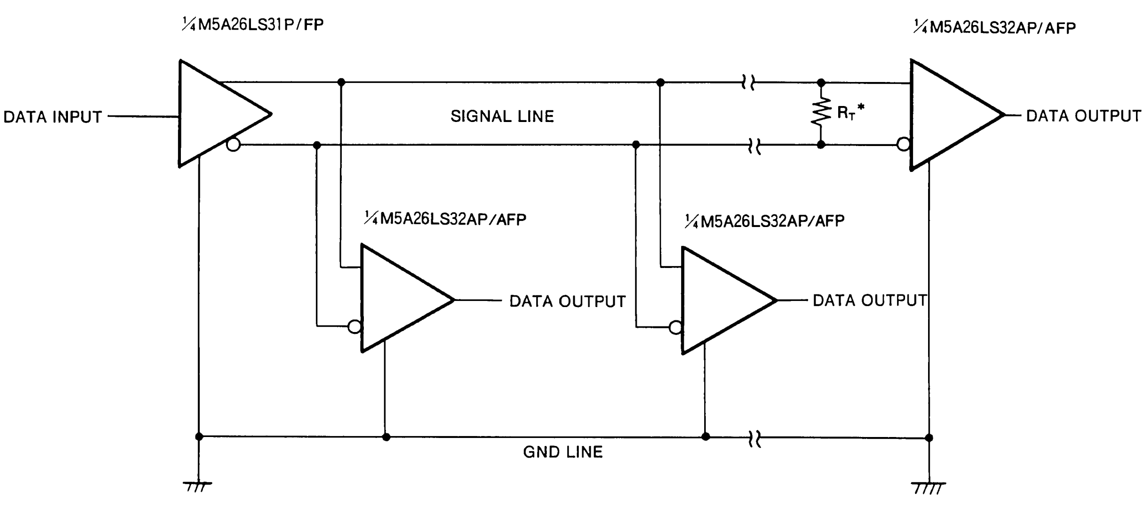
(2) When measuring propagation time and skew, switches SW1 and SW2 are open

(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM



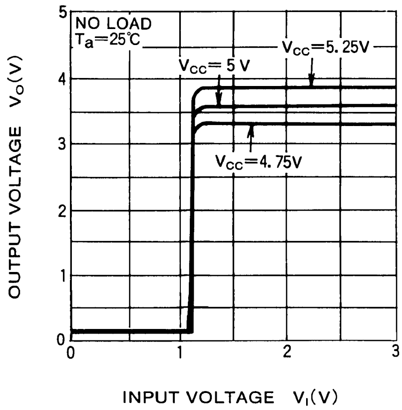
TYPICAL APPLICATION



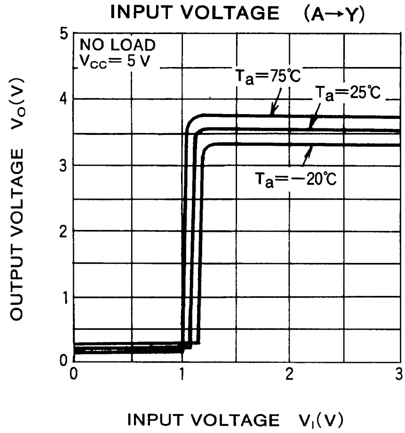
R_T* = Characteristic impedance of transmission line

TYPICAL CHARACTERISTICS

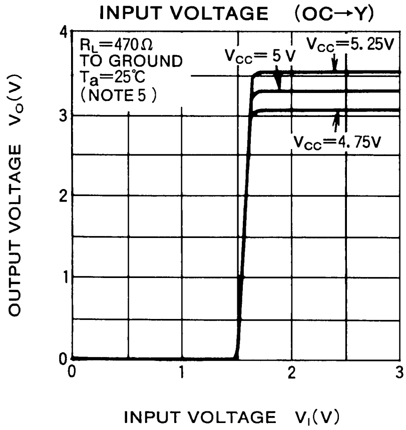
OUTPUT VOLTAGE VS INPUT VOLTAGE (A→Y)



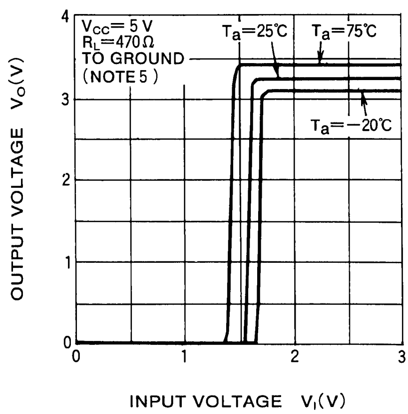
OUTPUT VOLTAGE VS INPUT VOLTAGE (A→Y)



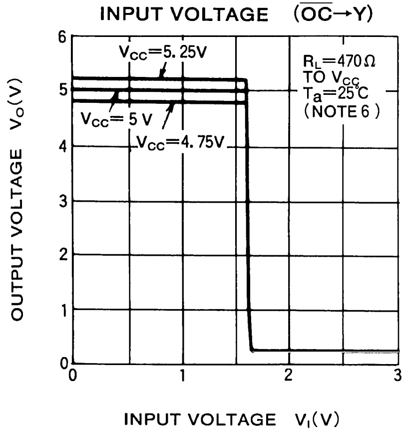
OUTPUT VOLTAGE VS INPUT VOLTAGE (OC→Y)



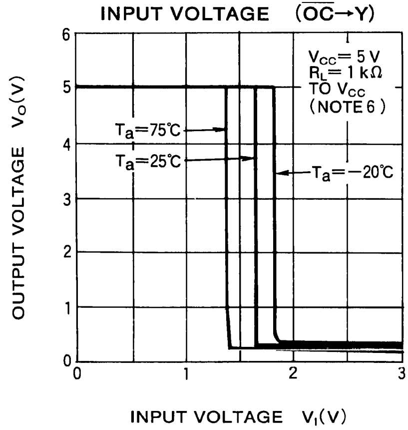
OUTPUT VOLTAGE VS INPUT VOLTAGE (OC→Y)



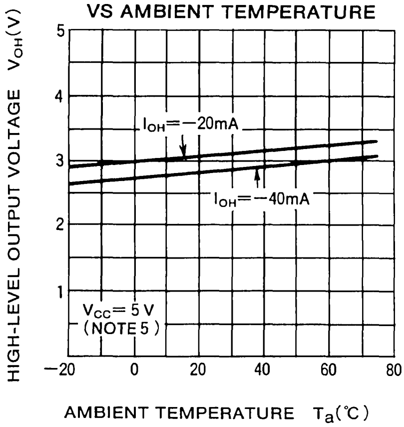
OUTPUT VOLTAGE VS INPUT VOLTAGE ($\overline{OC}$→Y)



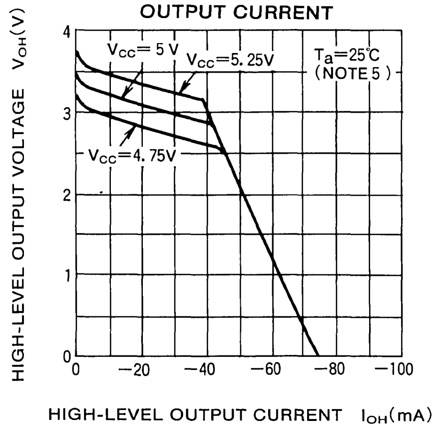
OUTPUT VOLTAGE VS INPUT VOLTAGE ($\overline{OC}$→Y)



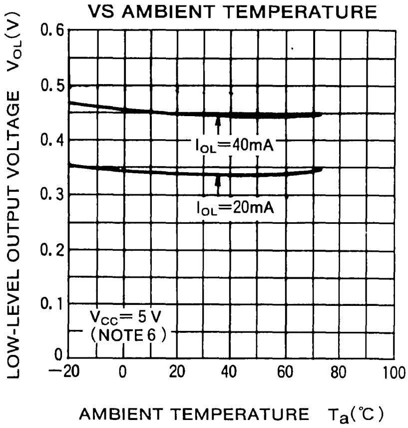
HIGH-LEVEL OUTPUT VOLTAGE VS AMBIENT TEMPERATURE



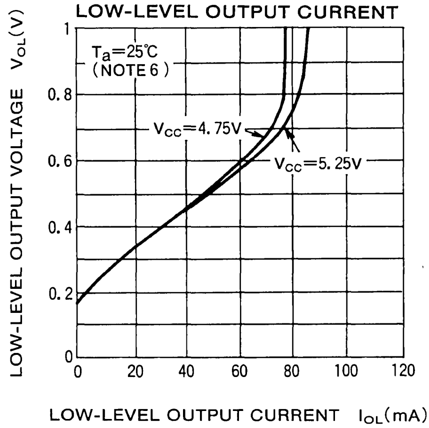
OUTPUT VOLTAGE VS OUTPUT CURRENT



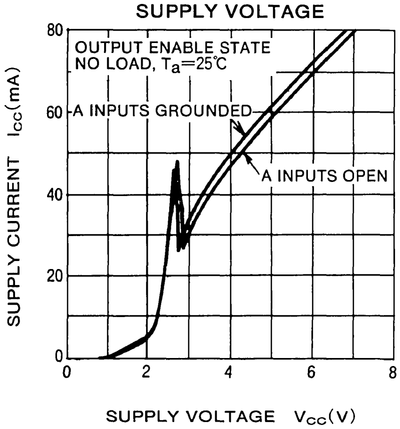
LOW-LEVEL OUTPUT VOLTAGE VS AMBIENT TEMPERATURE



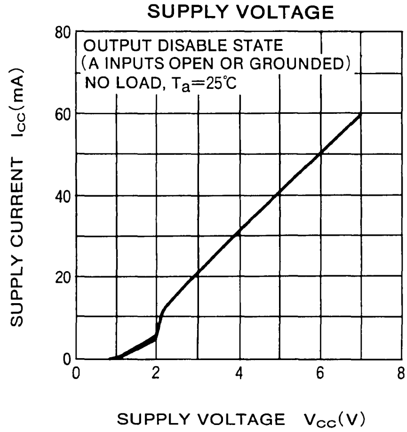
LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



SUPPLY CURRENT VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE



Note 5 : Input A is connected to V_{CC} when output Y is measured.
Input A is connected to GND when output Z is measured.

Note 6 : Input A is connected to GND when output Y is measured.
Input A is connected to V_{CC} when output Z is measured

M5M3487P/FP

QUADRUPLE DIFFERENTIAL LINE DRIVER

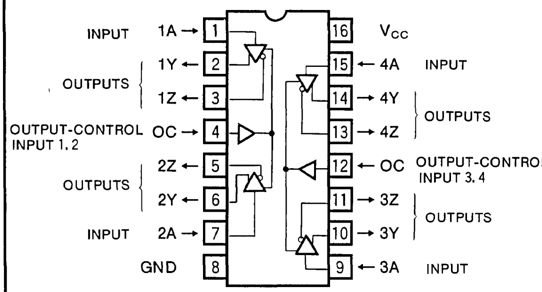
DESCRIPTION

The M5M3487P/FP is a semiconductor integrated circuit containing 4 line drivers for use with balanced digital data transmission, which meet EIA Standards RS-422-A.

FEATURES

- Output characteristics meet EIA Standards RS-422-A
- Connection of a termination resistor of 100 Ω between complementary outputs is possible
- High output impedance in power-off conditions
- Limitting circuit for short-circuit output current is provided
- Input characteristics are compatible with TTL circuits
- Output control inputs are provided
- Operates from single 5V power supply

PIN CONFIGURATION (TOP VIEW)



OUTLINE 16P4
16P2N

APPLICATION

For use as a data transmission interface in digital equipment

FUNCTIONAL DESCRIPTION

Input A can be driven directly with TTL circuits.
Output control inputs OCs are common to all 2 drivers.
Outputs Y and Z are complementary, where Y is non-inverted output, and Z inverted output. The sink current is 20mA, the source current is −20mA. Impedance matching can be made by connecting termination resistors to the transmission line whose characteristic impedance is 100 Ω. When OC = low-level, Y and Z are set to be in high-impedance state in the range of −0.2V to +6V and resulting in less loading of the bus line.

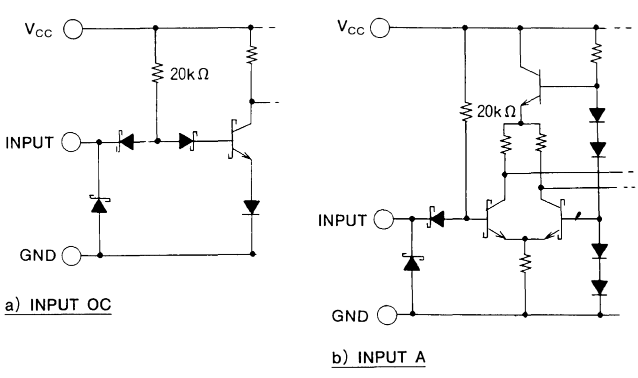
This integrated circuit is suitable for data transmission interface in digital equipment and the output characteristics meet EIA Standards RS-422-A. The M5M3486P/FP and M5A26LS32AP/AFP is available as a receiver which meets this Standard. The transmission mode is of balanced. Refer to TYPICAL APPLICATION.

FUNCTION TABLE (Note 1)

A	OC	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

Note 1 : Z : high-impedance
X : irrelevant

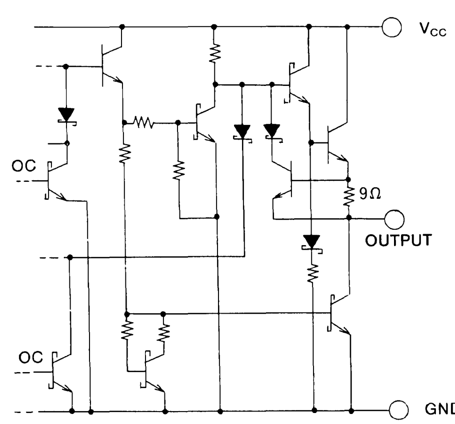
INPUT EQUIVALENT CIRCUIT



a) INPUT OC

b) INPUT A

OUTPUT EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7	V
V_I	Input voltage			−0.5～+7	V
V_O	Output voltage		When output is in high-impedance state	−0.5～+5.5	V
P_d	Power dissipation	DIP	T_a=25℃ (Note 2)	1000	mW
		SOP	T_a=25℃ (Note 3)	900	
Tstg	Storage temperature range			−65～+150	℃

Note 2 : For operation above 40℃ free-air temperature, derating of 9mW/℃ is necessary
3 : For operation above 25℃ free-air temperature, derating of 7.2mW/℃ is necessary.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Power supply			4.75	5	5.25	V
I_{OH}	High-level output current		V_{OH}≧2.5V	0		−20	mA
I_{OL}	Low-level output current		V_{OL}≦0.5V	0		20	mA
Topr	Operating free-air ambient temperature range	DIP	Dismounted	−20		+75	℃
		SOP	Mounted	−20		+70	

ELECTRICAL CHARACTERISTICS

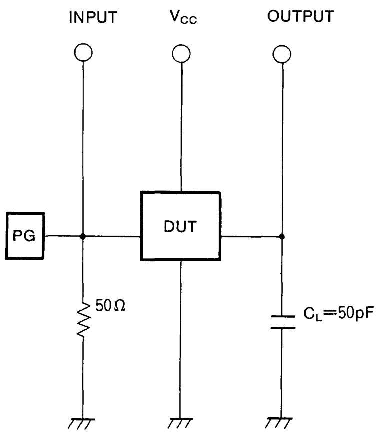
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		DIP			0.8	V
			SOP			0.7	
V_{IK}	Input clamp voltage	V_{CC}=4.75V, I_{IK}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, I_{OH}=−20mA		2.5	2.9		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, I_{OL}=20mA			0.34	0.5	V
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_O=0.5V				−20	μA
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_O=2.5V				20	μA
I_{X+}	Output leak current when power off	V_{CC}= 0 V	V_O= 6 V			50	μA
I_{X-}			V_O=−0.25V			−50	μA
I_I	Maximum input current	V_{CC}=5.25V, V_I= 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.36	mA
I_{OS}	Short-circuit output current	V_{CC}=5.25V (Note 4)		−30	−75	−150	mA
I_{CC}	Supply current	V_{CC}=5.25V, All outputs disabled			63	85	mA

* : All typical values are at V_{CC}=5V, T_a=25℃
Note 4 : All measurements should be done quickly and not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

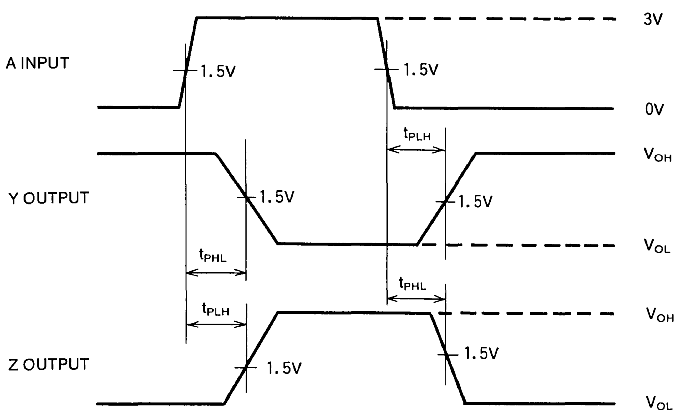
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation	C_L=50pF (Note 5)		9	20	ns
t_{PHL}	time from input A to output Y, Z			10	20	ns
Skew	Skew (Between outputs Y, Z)			1	6	ns
t_{PZH}	Output enable time to high level	C_L=50pF (Note 6)		10	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level			20	25	ns
t_{PLZ}	Output disable time from low level			15	25	ns

Note 5 : Test circuit

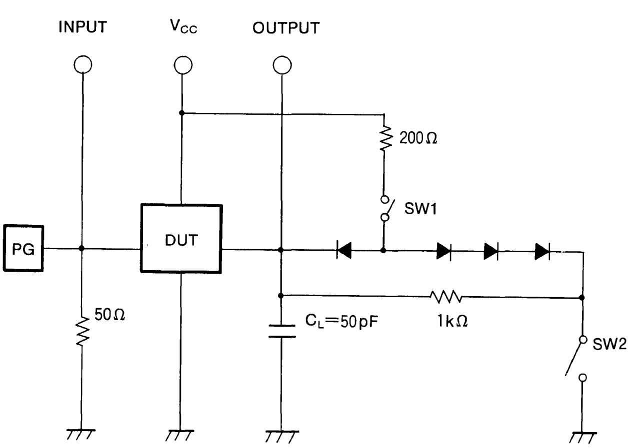


(1) The pulse generator (PG) has the following characteristics : PRR=1MHz, t_W=500ns, $t_r \leqq$ 5 ns, $t_f \leqq$ 5 ns, Z_O=50Ω
(2) All diode are switching diode ($t_{rr} \leqq$ 4 ns)
(3) C_L includes probe and jig capacitance.

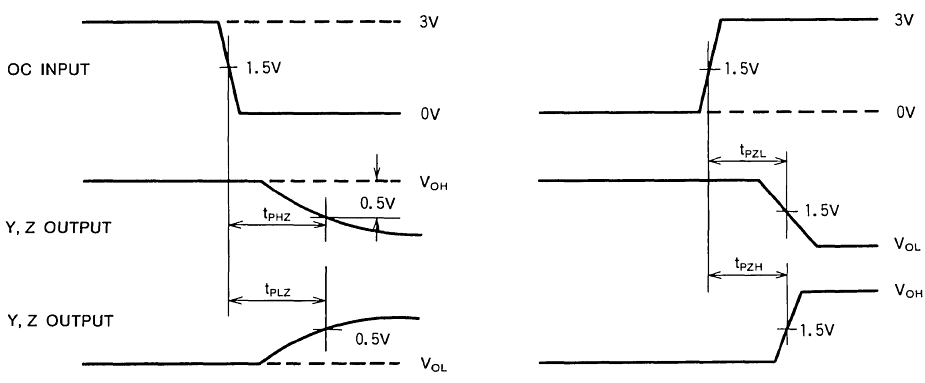
TIMING DIAGRAM



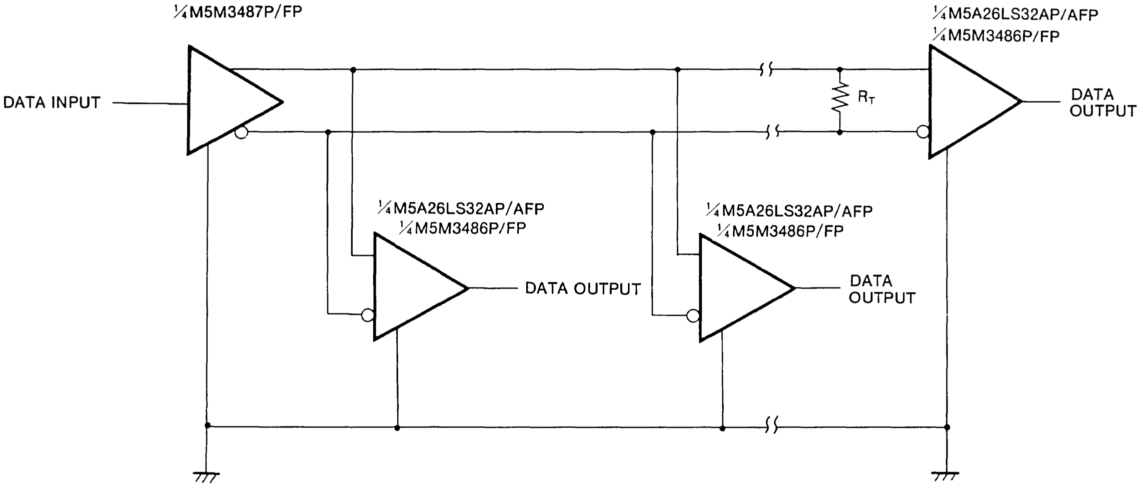
Note 6 : Test circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



TYPICAL APPLICATION



R_T=Characteristic impedance of transmission line

M5A26LS32AP/AFP

QUADRUPLE DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The M5A26LS32AP/AFP is a semiconductor integrated circuit containing 4 line receivers for use with balanced and unbalanced digital data transmission, which meets EIA Standards RS-422-A and RS-423-A.

FEATURES

- Input characteristics meet EIA Standards RS-422-A and RS-423-A
- Differential input voltage range from −7 to +7V
- Input with hysteresis (A, $\overline{A}$ 50mV typ)
- Common mode input voltage range from −7 to +7V
- Input sensitivity of ±200mV
- High input impedance of 12kΩ (min)
- Output control input (OC, $\overline{OC}$: Input characteristics are compatible with TTL circuits)
- Output characteristics are compatible with TTL circuits
- Three-state output
- Fail safe operation. Output always high when inputs are open
- Operated by single 5V power supply

APPLICATION

For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

Within the common mode voltage range of −7 to +7V, the threshold voltage of A and $\overline{A}$ is ±200mV. The hysteresis of A and $\overline{A}$ is 50mV typ. and eliminates differential noise for a signal of long transition time. As the input impedance of A and $\overline{A}$ is 12kΩ (min), the device will be easy to use.

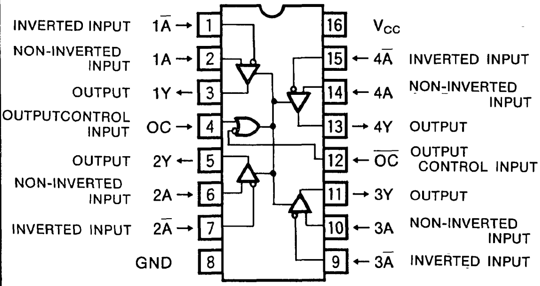
Output control inputs OC and $\overline{OC}$ are common to all four cirucits of the receiver. The input characteristics of OC and $\overline{OC}$ are compatible with TTL circuits.

Output Y has three states and there will be a high impedance condition when OC is low and $\overline{OC}$ is high. The Y output characteristics are compatible with TTL circuits.

The M5A26LS32AP can be used as a receiver for balanced and unbalanced data transmission.

This integrated circuits is suitable for data transmission interface in digital equipment and the input characteristics meet EIA Standards RS-422-A and RS-423-A. Refer to Table 1, which shows these standards. Balanced transmission driver M5A26LS31P/FP meets RS-422-A, while unbalanced transmission driver M5A26LS29P meets RS-423-A. Refer to the TYPICAL APPLICATION for further information.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N

FUNCTION TABLE (Note1)

A	$\overline{A}$	OC	$\overline{OC}$	Y
$V_{ID} > V_{TH}$		H	X	H
		X	L	H
$V_{TL} < V_{ID} < V_{TH}$		H	X	*
		X	L	*
$V_{ID} < V_{TL}$		H	X	L
		X	L	L
X		L	H	Z

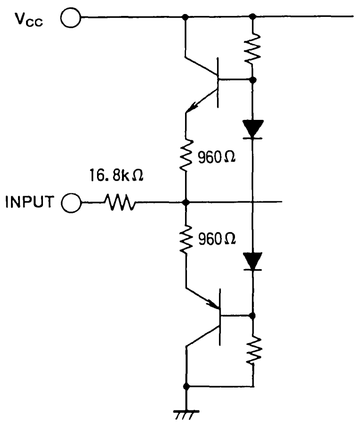
Note 1 : V_{ID} : (applied voltage A)−(applied voltage $\overline{A}$)
V_{TH} : 0.2V
V_{TL} : −0.2V
X : irrelevant
* : indeterminate
Z : high-impedance

Table 1 Eia standards RS-422-A, RS-423-A

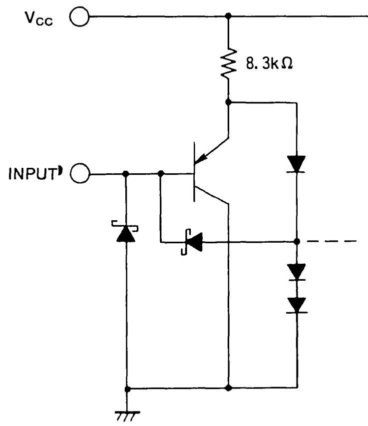
	Parameter	RS-422-A	RS-423-A	M5A26LS32AP Corresponding parameters (symbol)
Common	Transmission form	Balanced	Unbaranced	Input A, $\overline{A}$
	Maximum transmission distance	1200m	1200m	
	Maximum transmission speed	10Mbit/s	100Kbit/s	
Driver	Maximum output voltage (no load)	6 V (between outputs)	±6 V	
	Minimum output voltage (loaded)	2 V (between outputs)	±3.6V	
	Minimum output resistance (power off)	100μA(−0.25V<V_O<+6 V)	100μA(−6 V<V_O<+6 V)	
	Maximum short-circuit output current	±150mA	±150mA	
	Slew rate	Control not required	Controllable	
Receiver	Input resistance	≧4 kΩ	≧4 kΩ	r_I
	Maximum input threshold	−0.2~+0.2V	−0.2~+0.2V	V_{TH}, V_{TL}
	Maximum input voltage	−12~+12V	−12~+12V	I_I

QUADRUPLE DIFFERENTIAL LINE RECEIVER

INPUT EQUIVALENT CIRCUIT

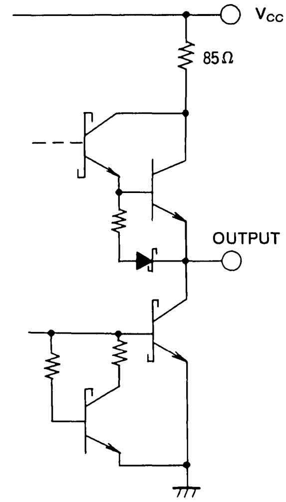


a) INPUT A, $\overline{A}$



b) OUTPUT CONTROL INPUT OC, $\overline{OC}$

OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7	V
V_I	Input voltage	A, $\overline{A}$		−25~+25	V
		OC, $\overline{OC}$		−0.5~+7	V
V_{ID}	Voltage between inputs	A, $\overline{A}$		−25~+25	V
I_{OL}	Low-level output current			0~50	mA
P_d	Power dissipation	DIP	T_a=25℃ (Note 2)	1000	mW
		SOP	T_a=25℃ (Note 3)	640	
Tstg	Storage temperature range		−65~+150	℃	℃

Note 2 : A derating of 9 mW/℃ should be made when T_a≧40℃
3 : A derating of 5.1mW/℃ should be made when T_a≧25℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IC}	Common mode input voltage (Note 4)	A, $\overline{A}$	−7		+7	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−440	μA
I_{OL}	Low-level output current	V_{OL}≦0.45V	0		8	mA
Topr	Operating free-air ambient temperature range		−20		+75	℃

Note 4 : Common mode input voltages A, $\overline{A}$ is the average value of the voltages applied on A, $\overline{A}$

QUADRUPLE DIFFERENTIAL LINE RECEIVER

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, V_{IC}=−7∼+7V, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Typ*	Max	Unit
V_{TH}	High threshold voltage	A, $\overline{A}$	V_{OH}=2.7V, I_{OH}=−440μA, V_{ID}=V_{TH}				0.2	V
V_{TL}	Low threshold voltage	A, $\overline{A}$	V_{OL}=0.45V, I_{OL}=8mA, V_{ID}=V_{TL}		−0.2			V
$V_{T+}-V_{T-}$	Hysteresis (Note 5)	A, $\overline{A}$				50		mV
V_{IH}	High-level input voltage	OC, $\overline{OC}$			2			V
V_{IL}	Low-level input voltage	OC, $\overline{OC}$					0.8	V
V_{IK}	Input clamp voltage	OC, $\overline{OC}$	V_{CC}=4.75V, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_{ID}=1V, $V_{I(\overline{OC})}$=0.8V, I_{OH}=−440μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_{ID}=−1V	I_{OL}=4mA			0.4	V
			$V_{I(\overline{OC})}$=0.8V	I_{OL}=8mA			0.45	
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_O=0.4V				−20	μA
I_I	Input current	A, $\overline{A}$	V_I=15V, other input at −10∼+15V				1.2	mA
			V_I=−15V, other input at −15∼+10V				−1.7	
I_{IH}	High-level input current	OC, $\overline{OC}$	V_I=5.5V				100	μA
			V_I=2.7V				20	
I_{IL}	Low-level input current	OC, $\overline{OC}$	V_I=0.4V				−0.36	mA
r_i	Input resistance	A, $\overline{A}$	V_{IC}=−15∼+15V, other inputs are AC GND		11 (Note 6)	15		kΩ
I_{OS}	Short-circuit output current		V_{CC}=5.25V (Note 7)		−15		−85	mA
I_{CC}	Supply current		V_{CC}=5.25V, A=$\overline{A}$=0V, All outputs disabled			52	70	mA

* : Typical values are at V_{CC}=5V, T_a=25℃, and V_{IC}=0V.

Note 5 : Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

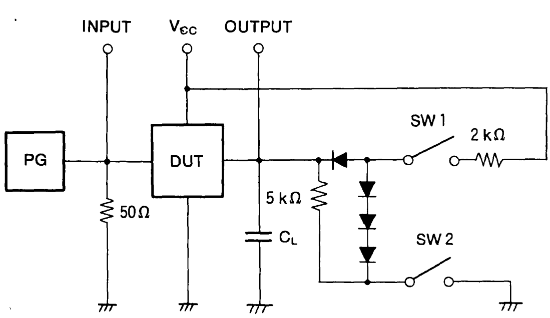
6 : The minimum value is 12k Ω within the range of T_a=0 to 75℃.

7 : All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{PLH}	Low-to-high-level, high-to-low-level output	C_L=15pF (Note 8)		14	35	ns
t_{PHL}	propagation time, from input A, $\overline{A}$ to output Y			22	35	ns
t_{PZH}	Output enable time to high level	C_L=15pF (Note 8)		18	22	ns
t_{PZL}	Output enable time to low level			20	25	ns
t_{PHZ}	Output disable time from high level	C_L=5pF (Note 8)		20	30	ns
t_{PLZ}	Output disable time from low level			24	40	ns

Note 8 : Test circuit



(1) The pulse generator (PG) has the following characteristics :
PRR=1MHz, t_w=500ns, t_r≦5ns, t_f≦5ns, Z_O=50Ω

(2) All diodes are switching diodes (t_{rr}≦4ns)

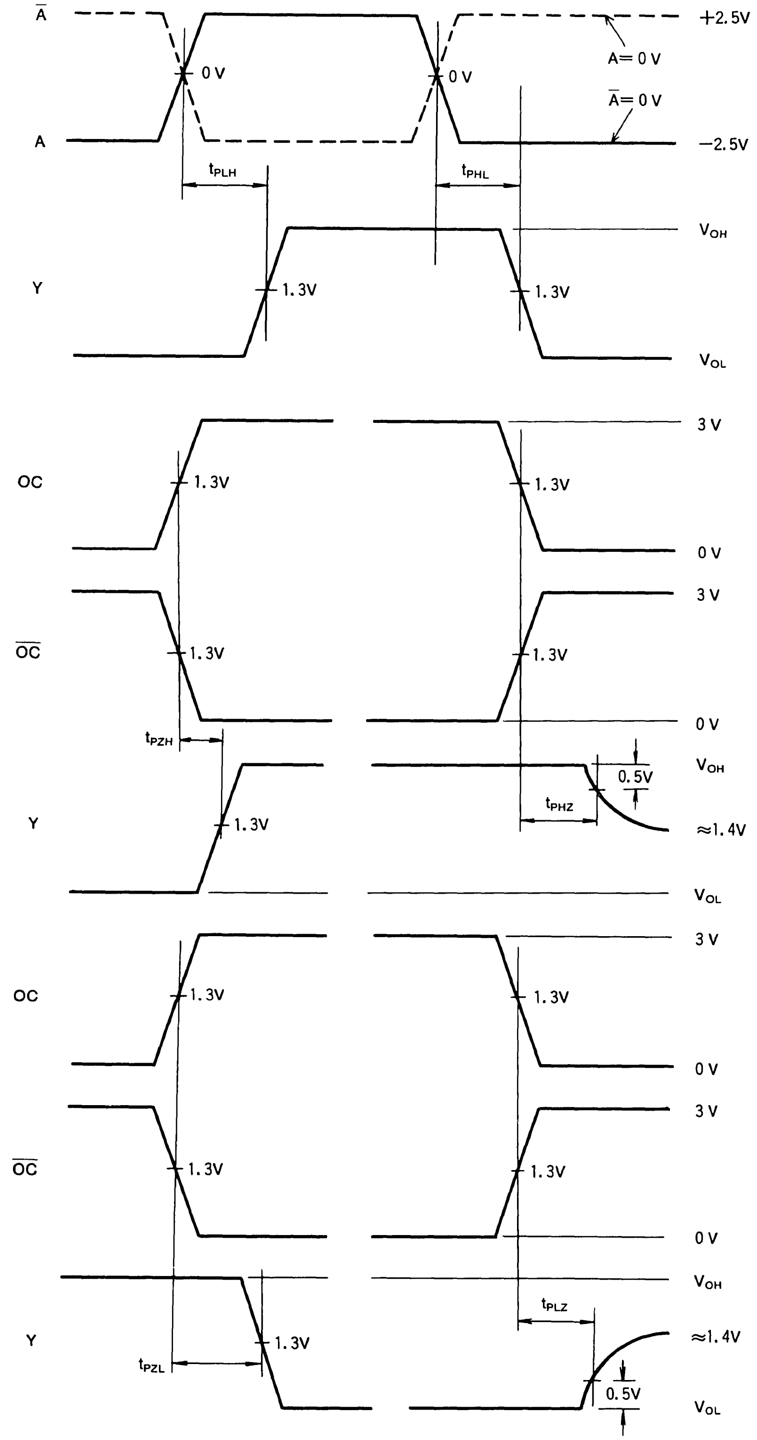
(3) C_L includes probe and jig capacitance.

(4) Output control OC is tested with $\overline{OC}$ high, $\overline{OC}$ is tested with OC low

Parameter	SW1	SW2
t_{PLH}, t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

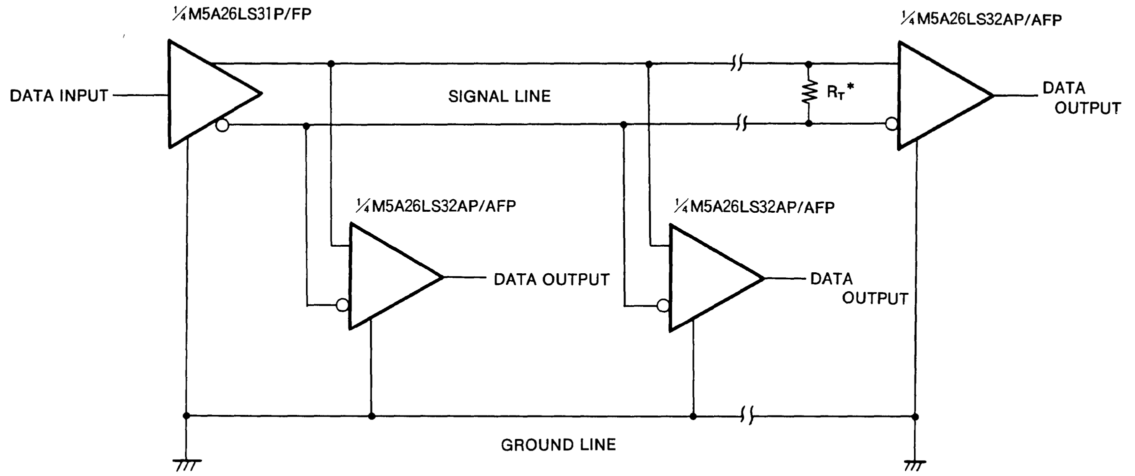
MITSUBISHI ELECTRIC

TIMING DIAGRAM



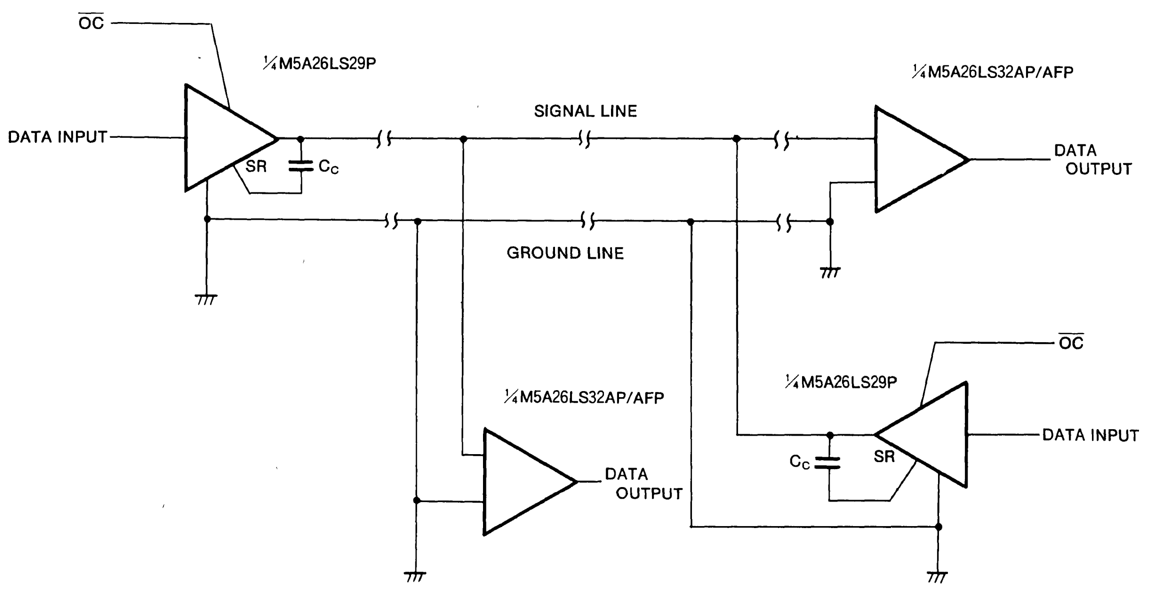
TYPICAL APPLICATION

a) BALANCED



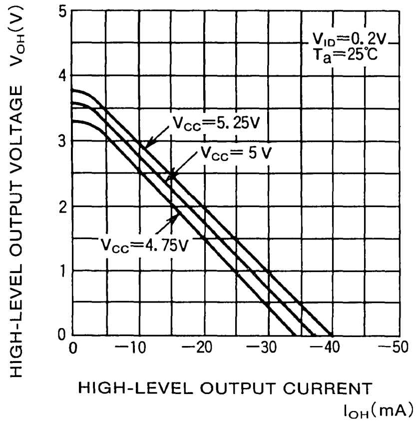
R_T* = Characteristic impedance of transmission line.

b) UNBALANCED

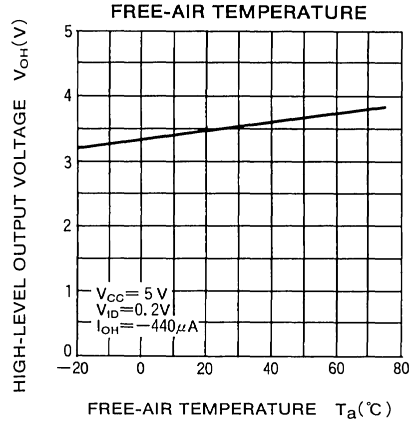


TYPICAL CHARACTERISTICS

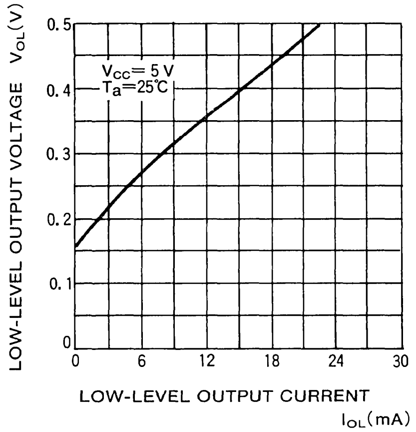
HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



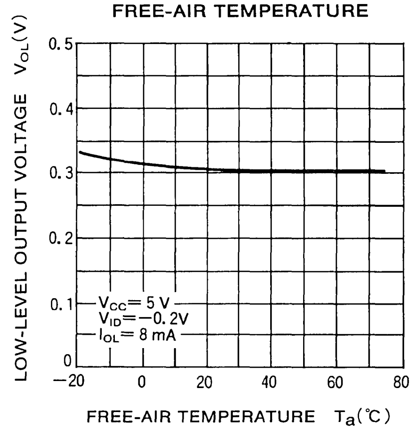
HIGH-LEVEL OUTPUT VOLTAGE VS FREE-AIR TEMPERATURE



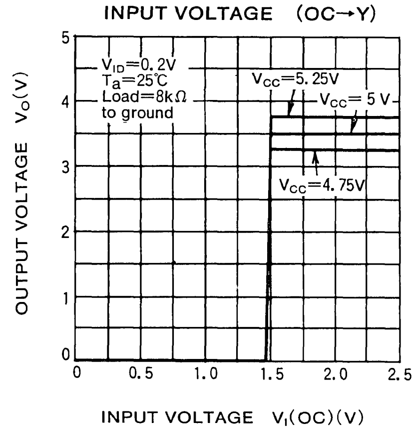
LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



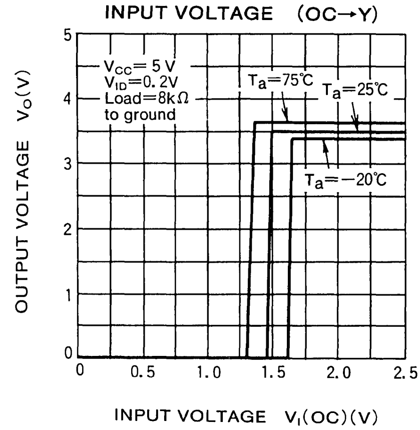
LOW-LEVEL OUTPUT VOLTAGE VS FREE-AIR TEMPERATURE

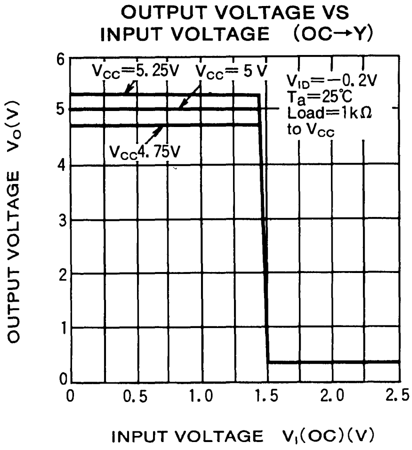


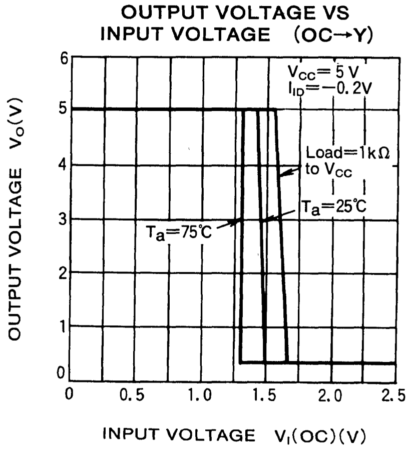
OUTPUT VOLTAGE VS INPUT VOLTAGE (OC→Y)

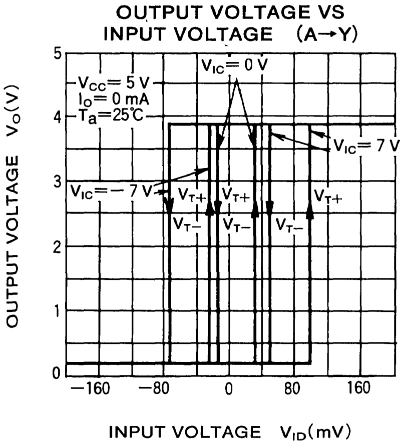


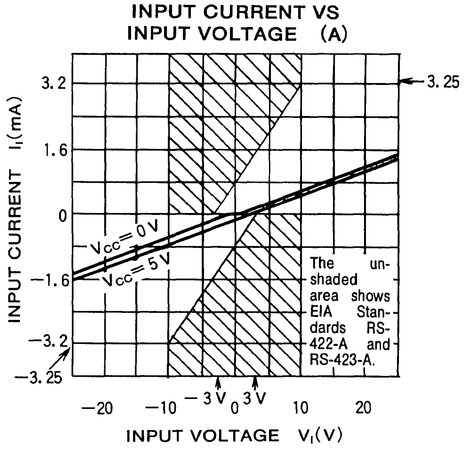
OUTPUT VOLTAGE VS INPUT VOLTAGE (OC→Y)











MITSUBISHI ELECTRIC

M5M3486P/FP

QUADRUPLE DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The M5M3486P/FP is an integrated circuit, consisting of 4 line receivers for use with balanced and unbalanced digital data transmission, which meets EIA standards RS-422A and RS-423A.

FEATURES

- Input characteristics meet EIA Standards RS-422A and RS-423A.
- Input with hysteresis (A, $\bar{A}$ 50mV typ)
- Common mode input voltage range from −7 to +7V
- Input sensitivity of ±200mV (max)
- Fail-safe operation. Output always set high when inputs A and $\bar{A}$ are open
- Three-state output
- Operated by single 5V power supply

APPLICATION

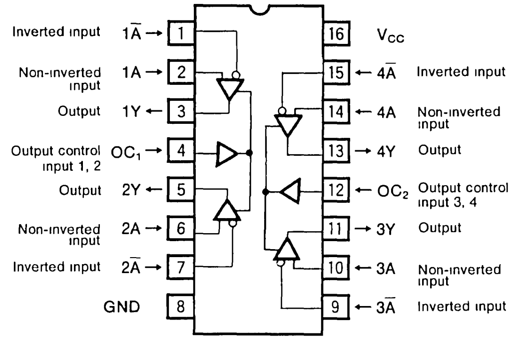
For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

Within the common mode voltage range of −7V to +7V, the threshold voltage of A and $\bar{A}$ is ±200mV. The characteristic hysteresis of A and $\bar{A}$ is 50mV typ.

Output control inputs OC_1 and OC_2 are common to two circuits of the receiver. Output Y has three states and has a high impedance condition when OC is low. The Y output characteristics are compatible with TTL circuits. The M5M3486P/FP can be used as a receiver for balanced data transmissions and the input characteristics meet EIA Standards RS-422A and RS-423A. Balanced transmission driver M5A26LS31P/FP meets RS-422A while unbalanced transmission driver M5A26LS29P meets RS-423A. Refer to the APPLICATION EXAMPLE for further information.

PIN CONFIGURATION (TOP VIEW)



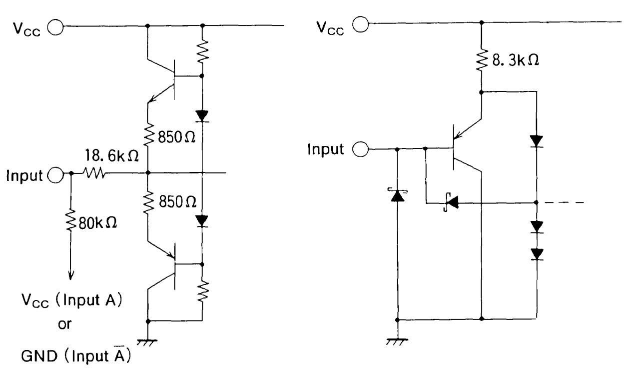
Outline 16P4
16P2N

FUNCTION TABLE (Note 1)

A	$\bar{A}$	OC	Y
$V_{ID} > V_{TH}$		H	H
$V_{TL} < V_{ID} < V_{TH}$		H	*
$V_{ID} < V_{TL}$		H	L
X		L	Z

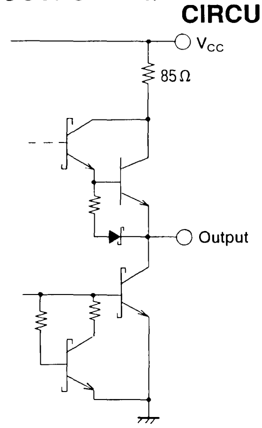
Note 1 : V_{ID} : (applied voltage A)−(applied voltage $\bar{A}$)
V_{TH} : 0.2V
V_{TL} : −0.2V
X : irrelevant
* : indeterminate
Z : high-impedance

INPUT EQUIVALENT CIRCUIT



a) Input A, $\bar{A}$ b) Output control input OC

OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7	V
V_I	Input voltage	A, $\overline{A}$		−25~+25	V
		OC		−0.5~+8	
V_{ID}	Voltage difference between inputs	A, $\overline{A}$		−25~+25	V
I_{OL}	Low-level output current			0~50	mA
Pd	Power dissipation	DIP	When T_a=25℃ (Note 2)	1000	mW
		SOP	When T_a=25℃ (Note 3)	640	
Tstg	Storage temperature			−65~+150	℃

Note 2 : A derating of 9mW/℃ should be made when $T_a \geqq 40$℃
3 : A derating of 5.1mW/℃ should be made when $T_a \geqq 25$℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IC}	Common mode input voltage (Note 4)	A, $\overline{A}$	−7		+7	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.5V$	0		8	mA
Topr	Ambient temperature		−20		+75	℃

Note 4 : Common mode input voltage A, $\overline{A}$ is the average value of the voltage applied on A, $\overline{A}$

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, V_{IC}=−7~+7V, T_a=−20~+75℃)

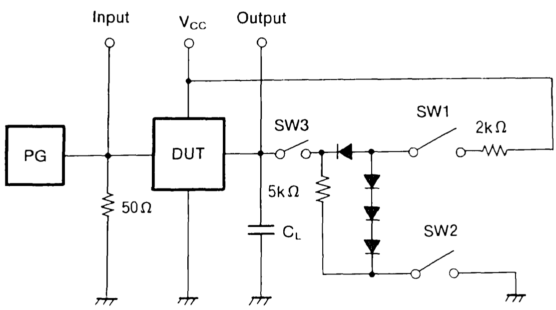
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{TH}	High threshold voltage	A, $\overline{A}$	V_{OH}=2.7V, I_{OH}=−400μA				0.2	V
V_{TL}	Low threshold voltage	A, $\overline{A}$	V_{OL}=0.5V, I_{OL}=8mA		−0.2			V
$V_{T+}-V_{T-}$	Hysteresis (Note 5)	A, $\overline{A}$				50		mV
V_{IH}	High-level input voltage	OC			2			V
V_{IL}	Low-level input voltage	OC					0.8	V
V_{IK}	Input clamp voltage	OC	I_I=−10mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID}=0.4V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{ID}=−0.4V, I_{OL}=8mA			0.31	0.5	V
I_{OZH}	Off-state high-level output current		V_I=0.8V, V_{ID}=−3V, V_O=2.4V				40	μA
I_{OZL}	Off-state low-level output current		V_I=0.8V, V_{ID}=3V, V_O=0.5V				−40	μA
I_I	Input current	A, $\overline{A}$	V_{CC}=0V or 5.25V Other inputs 0V	V_I=−10V			−3.25	mA
				V_I=−3V			−1.5	
				V_I=3V			1.5	
				V_I=10V			3.25	
I_{IH}	High-level input current	OC	V_I=5.25V				100	μA
			V_I=2.7V				20	
I_{IL}	Low-level input current	OC	V_I=0.5V				−100	μA
I_{OS}	Output short circuit current (Note 6)		V_O=0V		−15		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V, V_{OC}=0V			55	75	mA

* : Typical values are at V_{CC}=5V, T_a=25℃ and V_{IC}=0V.
Note 5 : Hysteresis is the difference between the positive-going input threshold voltage V_{T+} and negative-going input threshold voltage V_{T-}.
6 : All measurement should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to high-level, high-to-low-level output propagation time, from input A, $\overline{A}$ to output Y	C_L=15pF(Note 7)		14	30	ns
t_{PHL}				22	35	ns
t_{PZH}	High-level output enable time	C_L=15pF(Note 7)		18	30	ns
t_{PZL}	Low-level output enable time			20	30	ns
t_{PHZ}	High-level output disable time	C_L=5pF(Note 7)		20	35	ns
t_{PLZ}	Low-level output disable time			24	35	ns

Note 7 : Test circuit



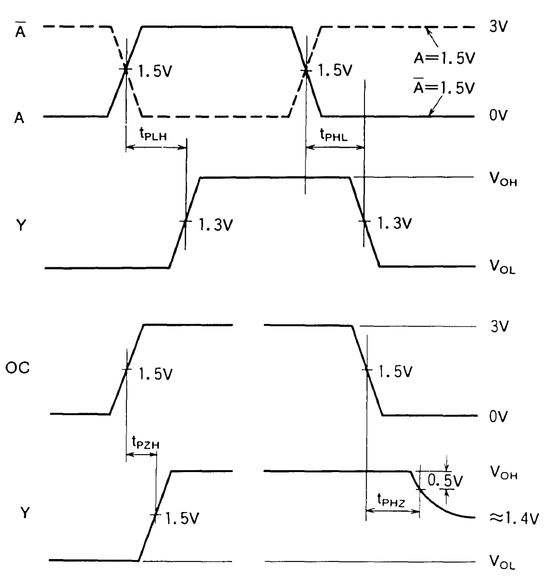
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_W=500ns, $t_r \leq$ 5ns, $t_f \leq$ 5ns, Z_O=50Ω

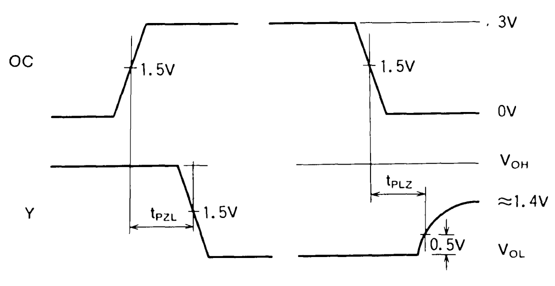
(2) All diodes are high-speed switching diodes ($t_{rr} \leq$ 4ns)

(3) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Parameter	SW 1	SW 2	SW3
t_{PLH}, t_{PHL}	—	—	Open
t_{PZH}	Open	Closed	Closed
t_{PZL}	Closed	Open	Closed
t_{PHZ}	Closed	Closed	Closed
t_{PLZ}	Closed	Closed	Closed

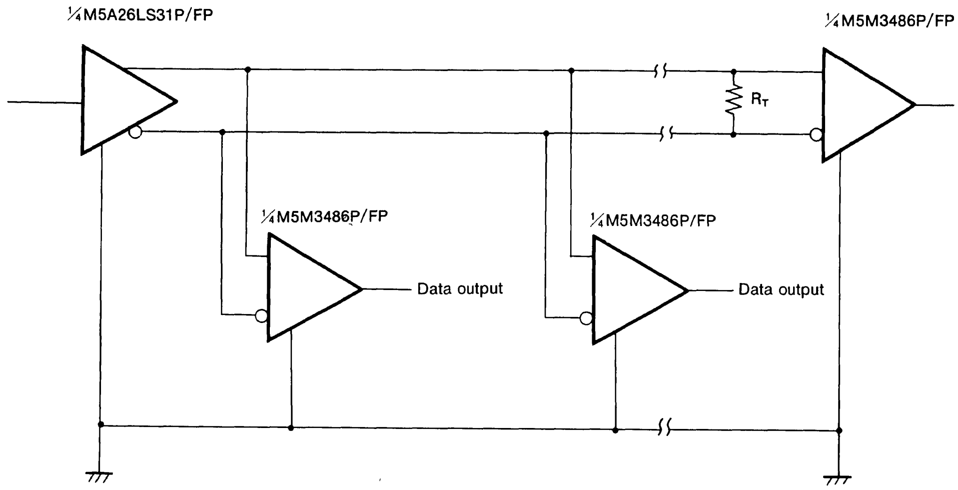
TIMING DIAGRAM





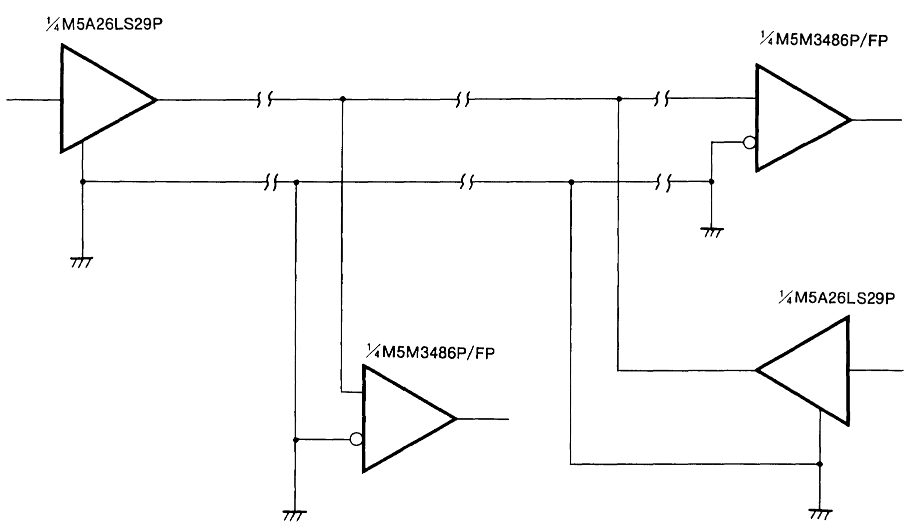
APPLICATION EXAMPLE

a) Balanced Type



R_T is characteristic impedance of transmission line

b) Unbalanced type



M5M34050P/FP
M5M34051P/FP
DUAL RS-422A TRANSCEIVER

DESCRIPTION
The M5M34050P/FP and M5M34051P/FP are semiconductor integrated circuits each with two differential drivers and differential receivers fulfilling the RS-422A EIA Standards.

FEATURES
【Common】
- Single 5V power supply
- Wide operating temperature range
  (T_a=−20 ～ +75℃)
- Both DIP and SOP packages are available.

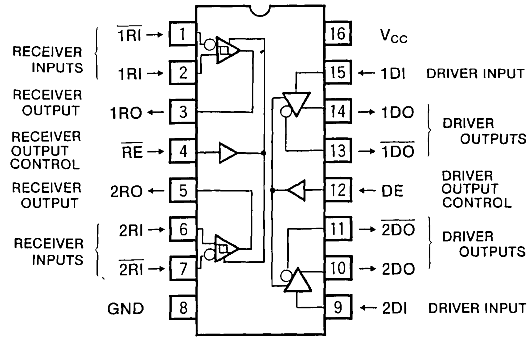
【Driver】
- Termination resistance of 100 Ω can be connected between outputs.
- High output impedance when power is off.
- Includes output control input

【Receiver】
- High input sensitivity (±200mV max.)
- Hysterisis input (50mV typ.)
- High input impedance (12kΩ min.)
- When input is open, output is "H" (failsafe function).
- Includes output control input (M5M34050P/FP)

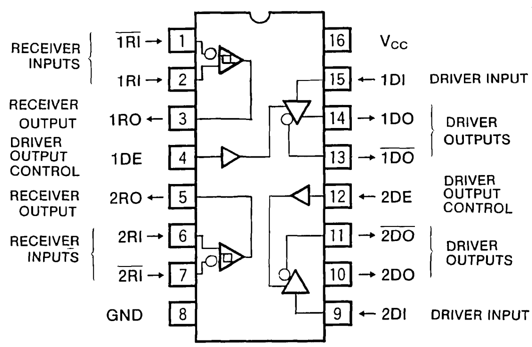
APPLICATION
HDD, LBP, printers, POS and other digital equipment high-speed data transmission interfaces.

FUNCTIONAL DESCRIPTION
The drivers and the receivers have the same characteristics as the M5A26LS31P and the M5A26LS32AP, respectively.
The driver input, receiver output, and the two output control inputs have electrical characteristics equivalent to LSTTL, enabling direct drive of TTL ICs. The M5M34050P/FP has independent output control inputs DE and $\overline{RE}$ for the driver and receiver, respectively, and the same control signal can be applied to these to alternately enable and disable the driver and receiver.
The M5M34051P/FP has separate output control inputs 1DE and 2DE for the drivers, enabling individual enable and disable settings for each driver.

PIN CONFIGULATION (TOP VIEW)



OUTLINE M5M34050P 16P4
M5M34050FP 16P2N



OUTLINE M5M34051P 16P4
M5M34051FP 16P2N

FUNCTION TABLE
(1) Driver

DI	DE	DO	$\overline{DO}$
L	H	L	H
H	H	H	L
X	L	Z	Z

(2) Receiver

RI	$\overline{RI}$	$\overline{RE}$	RO
V_{ID}>+0.2V		L	H
−0.2V<V_{ID}<0.2V		L	*
V_{ID}<−0.2V		L	L
X		H	Z

Note 1 : X : Irrelevant
Z : high impedance
* : Output status unspecified
V_{ID} : (RI applied voltage)−($\overline{RI}$ applied voltage)

ABSOLUTE MAXIMUM RATINGS (T_a=−20 ~ +75℃ unless otherwise noted)

Symbol	Parameter		Conditions	Ratings Min.	Ratings Max	Unit
V_{CC}	Supply voltage			−0.5	+7	V
V_I	Input voltage	RI, $\overline{RI}$		−20	+20	V
		Other than above		−0.5	+7	
V_{ID}	Voltage between inputs	RI, $\overline{RI}$		−20	+20	V
V_O	Output voltage		When output is in high impedance condition	−0.5	+5.5	V
Pd	Power dissipation	DIP	T_a=25℃ (Note 2)	1000		mW
		SOP	When mounted on PCB, T_a=25℃ (Note 3)	900		
T_{stg}	Storage temperature range			−65	+150	℃

Note 2 : When T_a≧40℃, derate as 9mW/℃.
3 : When T_a≧25℃, derate as 7.2mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20 ~ +75℃ unless otherwise noted)

Symbol	Parameter		Conditions	Limits Min	Limits Nom	Limits Max	Unit
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	"H" output current	DO, $\overline{DO}$	V_{OH}≧2.5V	0		−20	mA
		RO	V_{OH}≧2.7V	0		−400	μA
I_{OL}	"L" output current	DO, $\overline{DO}$	V_{OL}≦0.5V	0		20	mA
		RO	V_{OL}≧0.45V	0		8	
V_{IC}	Common mode input voltage (Note 4)			−7		+7	V
T_{opr}	Operating temperature range	DIP		−20		+75	℃
		SOP	When IC is mounted on PCB	−20		+75	

Note 4 : The common mode input voltage is the average value of the voltage applied to RI and $\overline{RI}$.

ELECTRICAL CHARACTERISTICS (T_a=−20 ~ +75℃ unless otherwise noted)

<Driver Section>

Symbol	Parameter	Test conditions		Limits Min	Limits Typ *	Limits Max.	Unit
V_{IH}	"H" input voltage			2			V
V_{IL}	"L" input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC}=4.75V, I_{IK}=−18mA				−1.5	V
V_{OH}	"H" output voltage	V_{CC}=4.75V, I_{OH}=−20mA		2.5	3.1		V
V_{OL}	"L" output voltage	V_{CC}=4.75V, I_{OL}=20mA			0.32	0.5	V
I_{OZL}	"L" output current when off	V_{CC}=5.25V, V_O=0.5V				−20	μA
I_{OZH}	"H" output current when off	V_{CC}=5.25V, V_O=2.5V				20	μA
I_{X+}	Output leak current when power off	V_{CC}=0V	V_O=6V			50	μA
I_{X-}			V_O=−0.25V			−50	μA
I_{IH}	"H" input current	V_{CC}=5.25V	V_I=7.0V			0.1	mA
			V_I=2.7V			20	μA
I_{IL}	"L" input current	V_{CC}=5.25V, V_I=0.4V			−0.05	−0.36	mA
I_{OS}	Output short current (Note 5)	V_{CC}=5.25V		−30		−150	mA

Note 5 : Measurement is conducted over a short period of time, and more than 2 outputs should not be shorted at a time

〈Receiver Section〉

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{TH}	High threshold voltage	RI, $\overline{RI}$	V_{OH}=2.7V, I_{OH}=−400μA V_{IO}=V_{TH}				0.2	V
V_{TL}	Low threshold voltage	RI, $\overline{RI}$	V_{OL}=0.45V, I_{OH}= 8 mA V_{IO}=V_{TL}		−0.2			V
V_{T+} V_{T-}	Hysteresis width (Note 6)	RI, $\overline{RI}$				50		mV
V_{IH}	"H" input voltage	$\overline{RE}$			2			V
V_{IL}	"L" input voltage	$\overline{RE}$					0.8	V
V_{IK}	Input clamp voltage	$\overline{RE}$	V_{CC}=4.75V, I_{IK}=−18mA				−1.5	V
V_{OH}	"H" output voltage		V_{CC}=4.75V, $V_{I(\overline{RE})}$=V_{IL} V_{IO}=0.4V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	"L" output voltage		V_{CC}=4.75V V_{IO}=−0.4V $V_{I(\overline{RE})}$=V_{IL}	I_L= 4 mA			0.4	V
				I_{OL}= 8 mA		0.31	0.45	
I_{OZL}	"L" output current when off		V_{CC}=5.25V, V_O=0.4V V_{IO}= 3 V				20	μA
I_{OZH}	"H" output current when off		V_{CC}=5.25V, V_O=2.4V V_{IO}= 3 V				−20	μA
I_I	Input current	RI, $\overline{RI}$	0 ≦V_{CC}≦5.25V, V_I=12V				1.0	mA
			0 ≦V_{CC}≦5.25V, V_I=−7V				−0.8	
I_{IH}	"H" input current	$\overline{RE}$	V_I=7.0V				100	μA
			V_I=2.7V				20	
I_{IL}	"L" input current	$\overline{RE}$	V_I=0.4V				−0.36	mA
I_{OS}	Output short current (Note 5)		V_{CC}=5.25V		−15		−85	mA

Note 6 : The hysteresis width is the difference between the threshold voltage V_{T+} and V_{T-} in the positive and negative directions, respectively.

〈Power Supply Section〉

Symbol	Parameter	Test conditions	Limits Min	Limits Typ *	Limits Max	Unit
I_{CC}	Supply current	V_{CC}=5.25V, output enable condition		58	80	mA

* : All typical values are at V_{CC}=5V and T_a=25℃

SWITCHING CHARACTERISTICS (V_{CC}=5V and T_a=25℃)

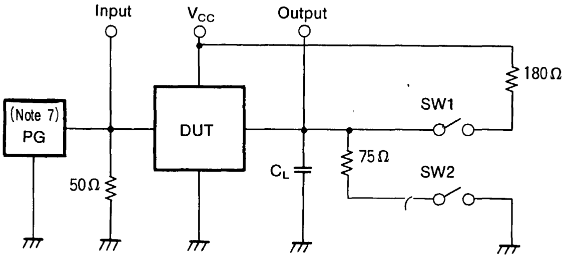
〈Driver Section〉

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{PLH}	Outputs "L—H", "H—L" propagation time, from input DI to output DO, $\overline{DO}$	C_L=30pF		11	20	ns
t_{PHL}				11	20	ns
Skew	Skew (between outputs DO and $\overline{DO}$)				6	ns
t_{PZH}	"H" output enable time	C_L=30pF R_L=75Ω to GND		8	40	ns
t_{PZL}	"L" output enable time	C_L=30pF R_L=180Ω to V_{CC}		18	45	ns
t_{PHZ}	"H" output disable time	C_L=10pF R_L=75Ω to GND		10	30	ns
t_{PLZ}	"L" output disable time	C_L=10pF R_L=180Ω to V_{CC}		11	35	ns

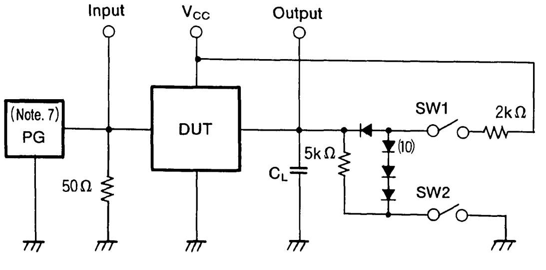
〈Receiver Section〉

Symbol	Parameter	Test conditions	Limits Min	Limits Typ.	Limits Max.	Unit
t_{PLH}	Outputs "L—H", "H—L" propagation time, from inputs RI and $\overline{RI}$ to output RO	C_L=15pF		19	40	ns
t_{PHL}				29	40	ns
t_{PZH}	"H" output enable time	C_L=15pF		10	30	ns
t_{PZL}	"L" output enable time			16	30	ns
t_{PHZ}	"H" output disable time	C_L=15pF		18	35	ns
t_{PLZ}	"L" output disable time			16	35	ns

TEST CIRCUIT



For driver section



For receiver section

Parameter	SW1	SW2	C_L
t_{PLH}	Open	Open	30pF
t_{PHL}	Open	Open	30pF
t_{PZH}	Open	Closed	30pF
t_{PZL}	Closed	Open	30pF
t_{PHZ}	Open	Closed	10pF
t_{PLZ}	Closed	Open	10pF

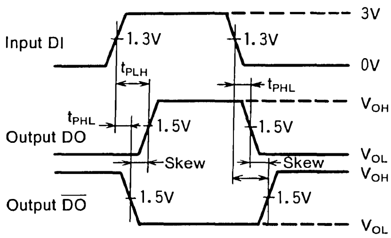
Parameter	SW1	SW2	C_L
t_{PLH}	Open	Open	15pF
t_{PHL}	Open	Open	
t_{PZH}	Open	Closed	
t_{PZL}	Closed	Open	
t_{PHZ}	Closed	Closed	
t_{PLZ}	Closed	Closed	

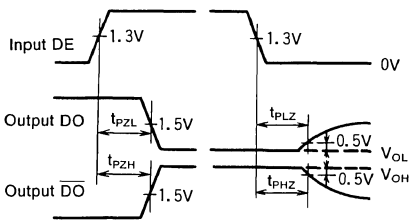
Note 7 : PG (pulse generator) output conditions are as follows.
Rising time : t_r≦15ns
Falling time : t_f≦ 6 ns
Repeat frequency : PRR= 1 MHz
Pulse amp. : V_P= 3 V_{P-P}
Output impedance : Z_O=50Ω

MITSUBISHI ELECTRIC

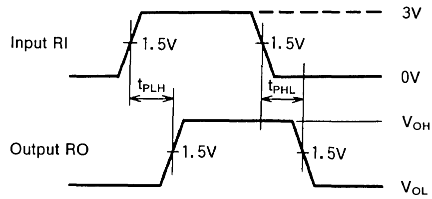
TIMING DIAGRAM

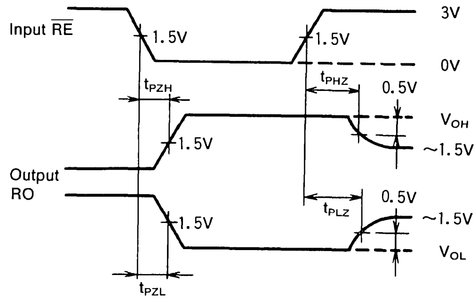
Driver Section





Receiver Section





M751270P/FP
M751271P/FP

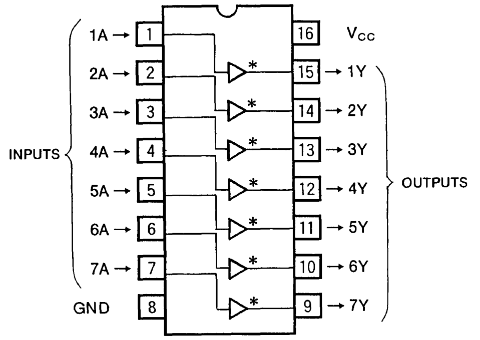
SEPTUPLE INVERTER/BUFFER DRIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION
The M751270P/FP and M751271P/FP are semiconductor integrated circuits with seven high output voltage, high drive open collector output buffers each. They have the same characteristics as the TTL 7406/7407, and adopt data flow-through pin arrangement ideal for mounting.

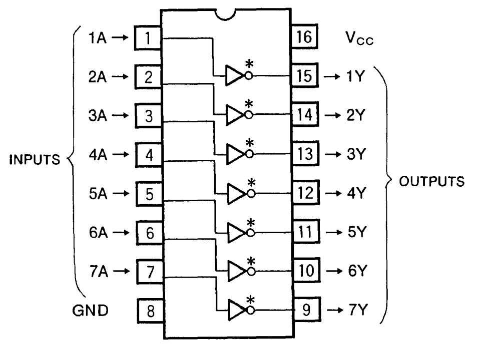
FEATURES
- Open collector output
- High output voltage (V_O=30V)
- High drive capacity (I_{OL}=48mA)
- High-speed operation (t_{pd}=10ns typ.)
- Wide operating voltage range (V_{CC}=5V±10%)
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION
FDD/HDD interface driver, LBP interface buffer, LED driver

PIN CONFIGURATION (TOP VIEW)



M751270P/FP



M751271P/FP

OUTLINE 16P4/16P2N

* : Open collector

FUNCTION TABLE

M751270

Input	Output
A	Y
H	H
L	L

M751271

Input	Output
A	Y
H	L
L	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~+15	V
V_O	Output voltage	When output is "H"	−0.5~+30	V
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage		4.5	5.0	5.5	V
I_{OH}	"H" output current	V_O=15V			100	μA
		V_O=30V			250	
I_{OL}	"L" output current	V_{OL}≦0.5V			40	mA
		V_{OL}≦0.7V			48	
Topr	Operating temperature range		−20		+75	℃

SEPTUPLE INVERTER/BUFFER DRIVER WITH OPEN COLLECTOR OUTPUT

ELECTRICAL CHARACTERISTICS (T_a=−20~+75℃, unless otherwise noted)

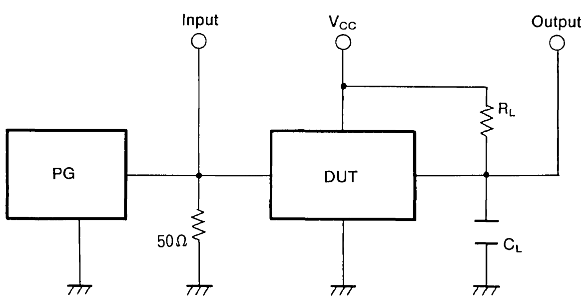
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.*	Max.	
V_{IH}	"H" input voltage			2.0			V
V_{IL}	"L" input voltage					0.8	V
V_{OL}	"L" output voltage	V_{CC}=4.5V	I_{OL}=40mA		0.40	0.5	V
		V_I=V_{IH}/V_{IL}	I_{OL}=48mA		0.45	0.7	
I_{OH}	"H" output current	V_{CC}=4.5V	V_O=15V			100	μA
		V_I=V_{IH}/V_{IL}	V_O=30V			250	
I_{IH}	"H" input current	V_{CC}=5.5V	V_I=2.7V			20	μA
			V_I=10V			100	
I_{IL}	"L" input current	V_{CC}=5.5V, V_I=0.4V				−0.2	mA
I_{CCH}	"H" power supply current	V_{CC}=5.5V			8	15	mA
I_{CCL}	"L" power supply current	V_{CC}=5.5V	M751270		28	50	mA
			M751271		32	55	

* : All typical values are at V_{CC}=5.0V and T_a=25℃.

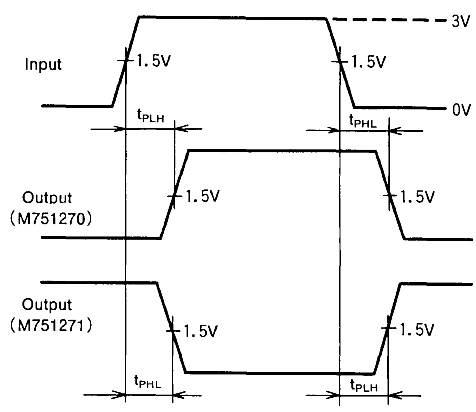
SWITHING CHARACTERISTICS (V_{CC}=5.0V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max.	
t_{PHL}	Output "H-L" propagation time	R_L=110Ω		12	30	ns
t_{PLH}	Output "L-H" propagation time	C_L=15pF		6	15	ns

TEST CIRCUIT



Rising time : t_r≦15ns
Falling time : t_f≦ 6 ns
Repeat frequency : PRR= 1 MHz
Pulse amp. : V_P= 3 V_{P-P}
Output impedance : Z_O=50Ω



Input/output voltage waveforms

M751272P/FP
M751273P/FP
PERIPHERAL DRIVER ARRAYS

DESCRIPTION
The M751272P/FP and M751273P/FP are semiconductor integrated circuit with six high drive capacity open collector drivers each.

FEATURES
- Open collector output
- High drive capacity (I_{OL}=48mA)
- High-speed operation (t_{pd}=10ns)
- Single 5V power supply
- Wide operating temperature range (T_a=−20∼+75℃)

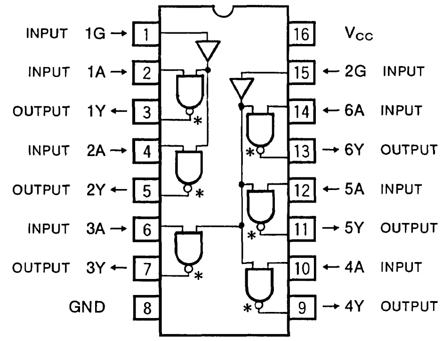
APPLICATION
Ideal for use as interface (daisy-chain) driver for floppy disks and hard disks.

FUNCTION TABLE

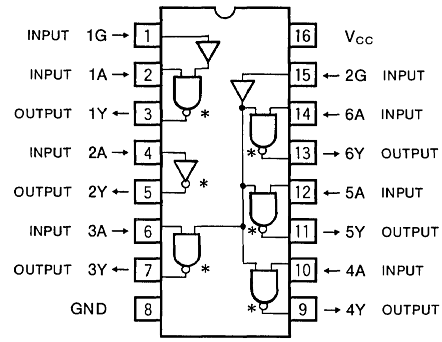
Input		Output
G	A	Y
L	X	H
H	L	H
H	H	L

X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



M751272P/FP



M751273P/FP

Outline 16P4/16P2N

* : Open collector output

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼+15	V
V_O	Output voltage	When output is "H"	−0.5∼+7	V
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Nom.	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
I_{OH}	"H" output current	V_O=5.5V			250	μA
I_{OL}	"L" output current	V_{OL}≦0.5V			48	mA
Topr	Operation temperature range		−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a = −20～+75℃, unless otherwise noted)

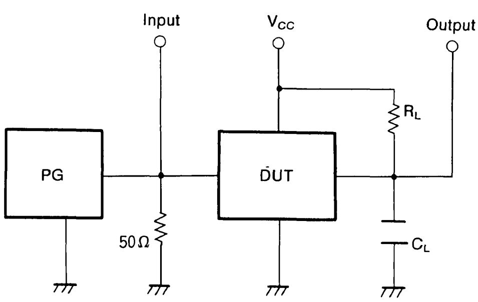
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ.*	Max	
V_{IH}	"H" input voltage			2.0			V
V_{IL}	"L" input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.5	V
I_{OH}	"H" output current	V_{CC}=4.5V, V_O=5.5V				250	μA
V_{OL}	"L" output voltage	V_{CC}=4.5V, I_{OL}=48mA			0.4	0.5	V
I_{IH}	"H" input current	V_{CC}=5.5V	V_I=2.7V			20	μA
			V_I=10V			100	
I_{IL}	"L" input current	V_{CC}=5.5V, V_I=0.4V				−0.2	mA
I_{CCH}	"H" power supply current	V_{CC}=5.5V			1.5	6	mA
I_{CCL}	"L" power supply current	V_{CC}=5.5V			38	60	mA

* : All typical values are at V_{CC}=5V and T_a=25℃.

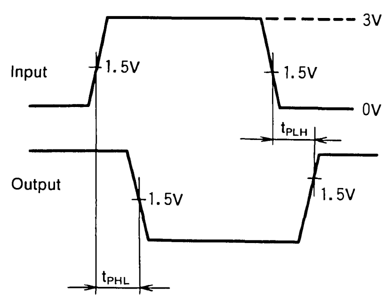
SWITCHING CHARACTERISTICS (V_{CC}=5.0V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PHL}	Output "H-L" propagation time	R_L=110Ω		10	50	ns
t_{PLH}	Output "L-H" propagation time	C_L=50pF		10	50	ns

TEST CIRCUIT



Rising time : t_r≦15ns
Falling time : t_f≦ 6 ns
Repeat frequency : PRR= 1 MHz
Pulse amp. : V_P= 3 V_{P-P}
Output impedance : Z_O=50Ω



Voltage waveforms

M75173P/FP

QUADRUPLE DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The M75173P/FP is an integrated circuit consisting of 4 line receiver for use with balanced and unbalanced digital data transmission meets EIA Standards RS-485, RS-422A and RS-423A.

FEATURES

- Input characteristics meet EIA Standards RS-485, RS-422A and RS-423A.
- Input with hysteresis (A, $\overline{A}$ 50mV typ)
- Common mode input voltage range −12∼+12V
- Input sensitivity of ±200mV (max)
- High input impedance 12kΩ (min)
- Fail safe operation. Output always high when inputs A and $\overline{A}$ are open
- Three-state output
- Operated by single 5V power supply

APPLICATION

For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

Within the common mode voltage range of −12V to +12V, the threshold voltage of A and $\overline{A}$ is ±200mV. The hysteresis of A and $\overline{A}$ is 50mV typ. As the input impedance of A and $\overline{A}$ is 12kΩ (min), the device will be easy to use.

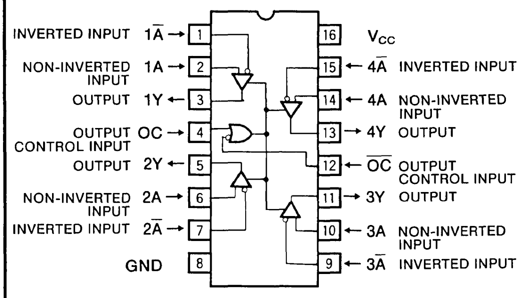
Output control inputs OC and $\overline{OC}$ are common to all circuits of the receiver. Output Y has three-state and will be high impedance when OC is low and $\overline{OC}$ is high.

Y output characteristics are compatible with TTL circuits.

The M75173P/FP can be used as a receiver for balanced and unbalanced receiver. The device is suitable for data transmission and multi-point transmission circuit can be made in combination with drivers compatible with RS-485 Standards. Up to 32 driver/receiver pairs can be connected to the bus..

Refer to the APPLICATION EXAMPLE for further information.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N

FUNCTION TABLE (Note 1)

A	$\overline{A}$	OC	$\overline{OC}$	Y
$V_{ID} > V_{TH}$		H	X	H
		X	L	H
$V_{TL} < V_{ID} < V_{TH}$		H	X	*
		X	L	*
$V_{ID} < V_{TL}$		H	X	L
		X	L	L
X		L	H	Z

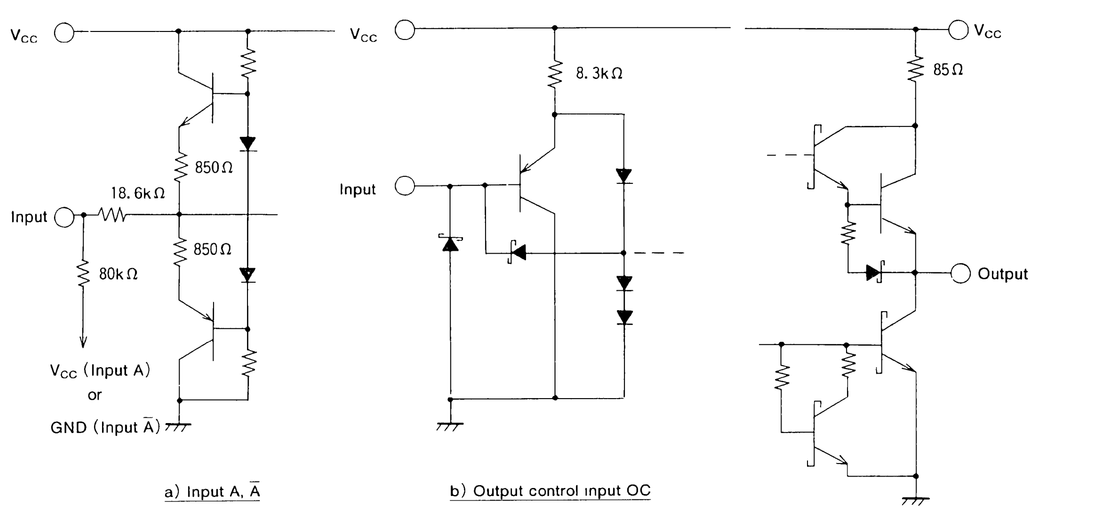
Note 1 : V_{ID} : (applied voltage A)−(applied voltage $\overline{A}$)
V_{TH} : 0.2V
V_{TL} : −0.2V
X : irrelevant
* : indeterminate
Z : high-impedance

MITSUBISHI ELECTRIC

QUADRUPLE DIFFERENTIAL LINE RECEIVER

INPUT EQUIVALENT CIRCUIT

OUTPUT EQUIVALENT CIRCUIT



a) Input A, $\overline{A}$

b) Output control input OC

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7	V
V_I	Input voltage	A, $\overline{A}$		−25~+25	V
		OC,		−0.5~+7	
V_{ID}	Voltage between inputs	A, $\overline{A}$		−25~+25	V
I_{OL}	Low-level output current			0~50	mA
P_d	Power dissipation	DIP	T_a=25℃ (Note 2)	1000	mW
		SOP	T_a=25℃ (Note 3)	640	
Tstg	Storage temperature range			−65~+150	℃

Note 2 : A derating of 9mW/℃ should be made when $T_a \geq 40$℃
3 : A derating of 5.1mW/℃ should be made when $T_a \geq 25$℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IC}	Common mode input voltage (Note 4)	A, $\overline{A}$	−12		+12	V
I_{OH}	High-level output current	$V_{OH} \geq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.5V$	0		16	mA
Topr	Ambient temperature range		−20		+75	℃

Note 4 : Common mode input voltage A, $\overline{A}$ is the average value of the voltages applied on A, $\overline{A}$

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, V_{IC}=−12∼+12V, T_a=−20∼+75℃)

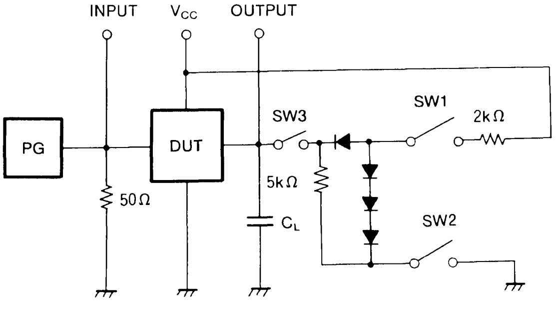
Symbol	Parameter		Test conditions		Limits Min	Typ*	Max	Unit
V_{TH}	High threshold voltage	A, $\overline{A}$	V_{OH}=2.7V, I_{OH}=−400μA				0.2	V
V_{TL}	Low threshold voltage	A, $\overline{A}$	V_{OL}=0.5V, I_{OL}=16mA		−0.2			V
$V_{T+}-V_{T-}$	Hysteresis(Note 5)	A, $\overline{A}$				50		mV
V_{IH}	High-level input voltage	OC, $\overline{OC}$			2			V
V_{IL}	Low-level input voltage	OC, $\overline{OC}$					0.8	V
V_{IK}	Input clamp voltage	OC, $\overline{OC}$	I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID}=0.2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{ID}=−0.2V	I_{OL}=8mA		0.31	0.45	V
				I_{OL}=16mA		0.40	0.5	
I_{OZH}	Off-state high-level output current		V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_O=0.4V				−20	μA
I_I	Input current	A, $\overline{A}$	Oter inputs 0V	V_I=12V			1	mA
				V_I=−7V			−0.8	
I_{IH}	High-level input current	OC, $\overline{OC}$	V_I=2.7V				20	μA
I_{IL}	Low-level input current	OC, $\overline{OC}$	V_I=0.4V				−100	μA
r_I	Input resistance	A, $\overline{A}$			11(Note 6)	15		kΩ
I_{OS}	Output short circuit current (Note 6)				−15		−85	mA
I_{CC}	Supply current		All outputs in disable state			52	70	mA

* : Typical values are at V_{CC}=5V, T_a=25℃, V_{IC}=0V
Note 5 : Hysteresis is the difference between the positive-going input threshold voltage V_{T+} and negative-going input threshold voltage V_{T-}.
6 : Minimum value is 12kΩ with T_a=0∼75℃.
7 : All measurement should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{PLH}	Low-to high-level, high-to low-level output	C_L=15pF (Note 8)		18	35	ns
t_{PHL}	propagation time, from input A, $\overline{A}$ to output Y			29	35	ns
t_{PZH}	High-level output enable time	C_L=15pF (Note 8)		20	30	ns
t_{PZL}	Low-level output enable time			21	30	ns
t_{PHZ}	High-level output disable time	C_L=5pF (Note 8)		18	35	ns
t_{PLZ}	Low-level output disable time			27	35	ns

Note 8 : Test circuits

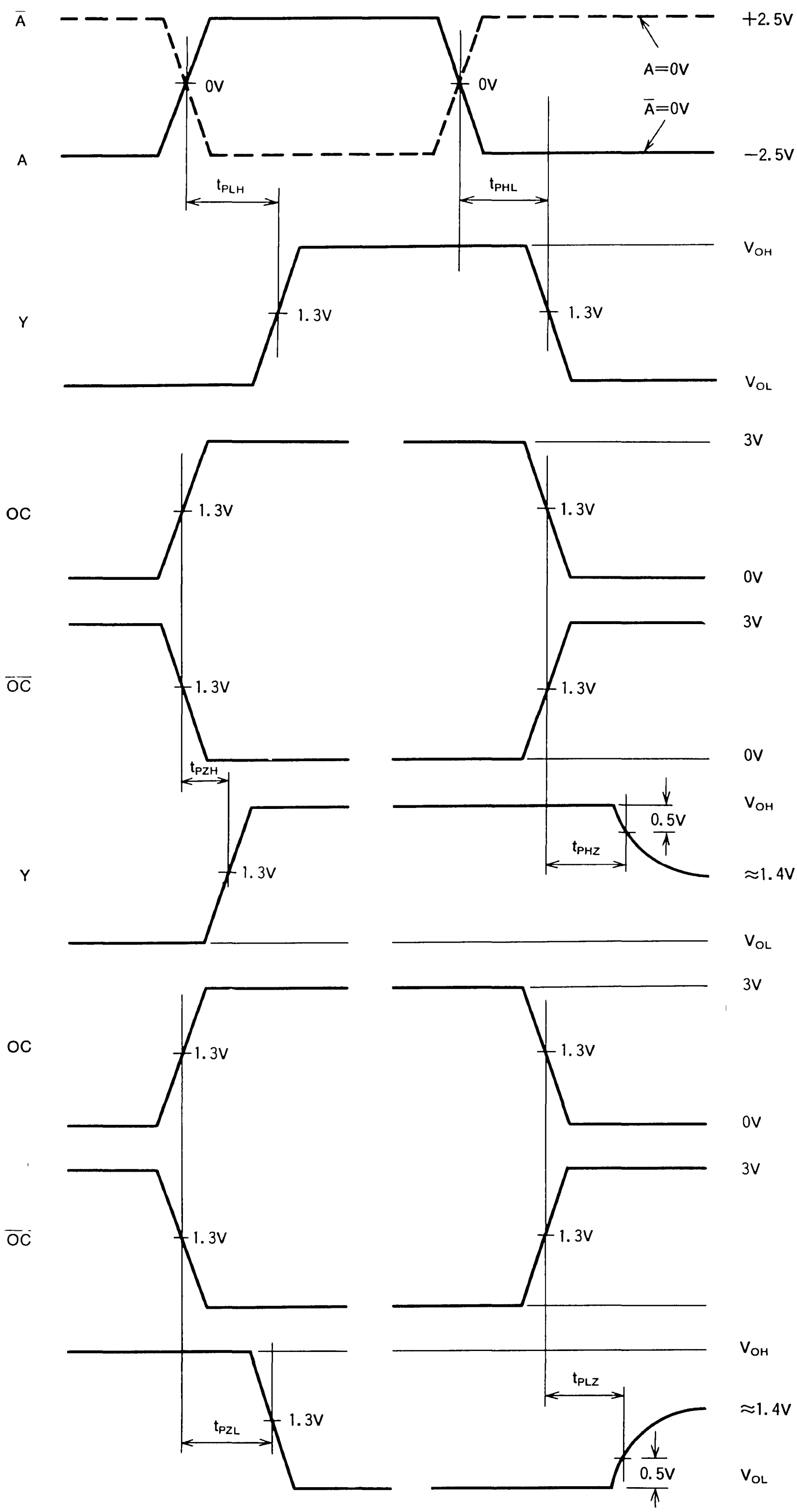


(1) The pulse generator (PG) has the following characteristics :
PRR=1MHz, t_W=500ns, t_r≦5ns, t_f≦5ns, Z_O=50Ω
(2) All diodes are high-speed switching diodes (t_{rr}≦4ns)
(3) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.
(4) When output control input OC is tested, output control input $\overline{OC}$ is high. When $\overline{OC}$ is tested, OC is low.

Parameter	SW 1	SW 2	SW3
t_{PLH}, t_{PHL}	−	−	Open
t_{PZH}	Open	Closed	Closed
t_{PZL}	Closed	Open	Closed
t_{PHZ}	Closed	Closed	Closed
t_{PLZ}	Closed	Closed	Closed

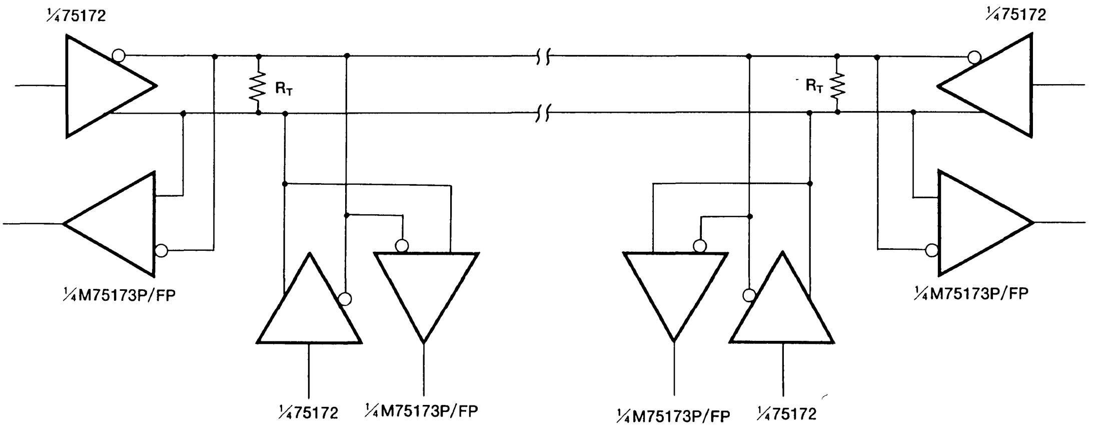
MITSUBISHI ELECTRIC

TIMING DIAGRAM



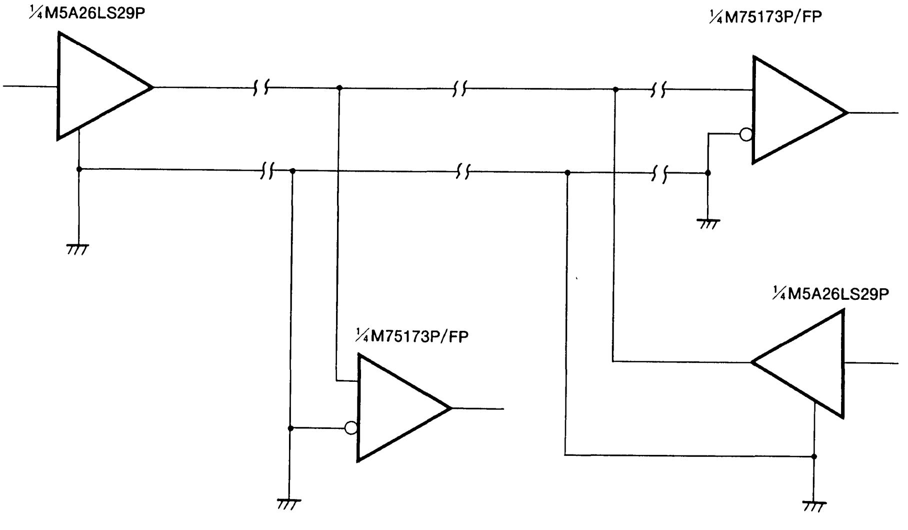
APPLICATION EXAMPLE

a) Balanced type



R_T is characteristics impedance of transmission line

b) Unbalanced type



M75175P/FP

QUADRUPLE DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The M75175P/FP is an integrated circuit consisting of 4 line receivers for use with balanced and unbalanced digital data transmissions meeting EIA standards RS-485, RS-422A and RS-423A.

FEATURES

- Input characteristics meet EIA standards RS-485, RS-422A and RS-423A.
- Input with hysteresis (A, $\overline{A}$ 50 mV typ)
- Common mode input voltage range −12∼+12V
- Input sensitivity of ±200 mV (max)
- High input impedance 12kΩ (min)
- Fail safe operation. Output always high when inputs A and $\overline{A}$ are open
- Three-state output
- Operated by single 5V power supply

APPLICATION

For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

Within the common mode voltage range of −12V to +12V, the threshold voltage of A and $\overline{A}$ is ±200mV. The hysteresis of A and $\overline{A}$ is 50mV typ. As the input impedance of A and $\overline{A}$ is 12kΩ (min), the device will be easy to use.

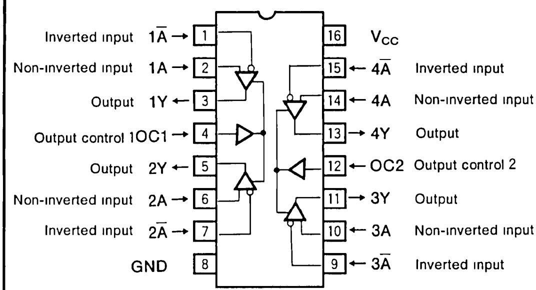
Output control inputs OCs common to each two circuits of the receiver. Output Y has three-state and will be high impedance when OC is low.

Y output characteristics are compatible with TTL circuits.

The M75175P/FP can be used as a receiver for balanced and unbalanced receiver. The device is suitable for data transmission and multi-point transmission circuit can be made in combination with drivers compatible with RS-485 standards. Up to 32 driver/receiver pairs can be connected to the bus.

Refer to the APPLICATION EXAMPLE for further information.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N

FUNCTION TABLE (Note 1)

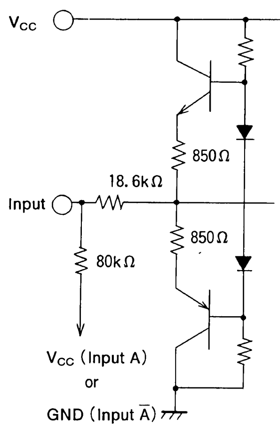
A	$\overline{A}$	OC	Y
$V_{ID} > V_{TH}$		H	H
$V_{TL} < V_{ID} < V_{TH}$		H	*
$V_{ID} < V_{TL}$		H	L
X		L	Z

Note 1 : V_{ID} : (applied voltage A)−(applied voltage $\overline{A}$)
V_{TH} : 0. 2V
V_{TL} : −0. 2V
X : irrelevant
* : indeterminate
Z : high-impedance

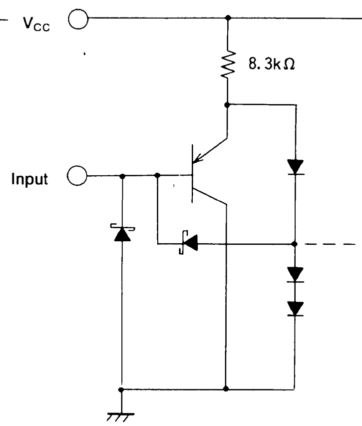
QUADRUPLE DIFFERENTIAL LINE RECEIVER

INPUT EQUIVALENT CIRCUIT

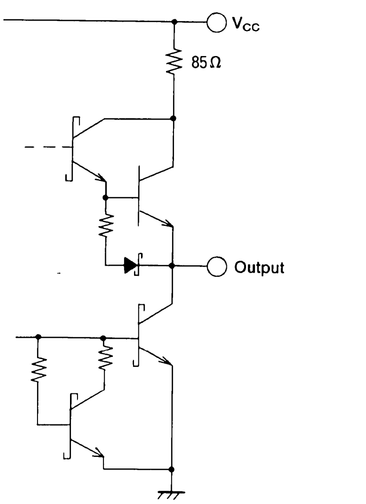
OUTPUT EQUIVALENT CIRCUIT



a) Input A, Ā



b) Output control input OC



ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+7	V
V_I	Input voltage	A, Ā		−25~+25	V
		OC		−0.5~+7	
V_{ID}	Voltage difference between inputs	A, Ā		−25~+25	V
I_{OL}	Low-level output current			0~50	mA
P_d	Power dissipation	DIP	T_a=25℃ (Note 2)	1000	mW
		SOP	T_a=25℃ (Note 3)	640	
Tstg	Storage temperature range			−65~+150	℃

Note 2 : A derating of 9mW/℃ should be made when T_a≧40℃
3 : A derating of 5.1mW/℃ should be made when T_a≧25℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IC}	Common mode input voltage (Note 4)	A, Ā	−12		+12	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.5V	0		16	mA
Topr	Ambient temperature range		−20		+75	℃

Note 4 : Common mode input voltage A, Ā is the average value of the voltages applied on A, Ā.

QUADRUPLE DIFFERENTIAL LINE RECEIVER

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, V_{IC}=−12~+12V, T_a=−20~+75℃)

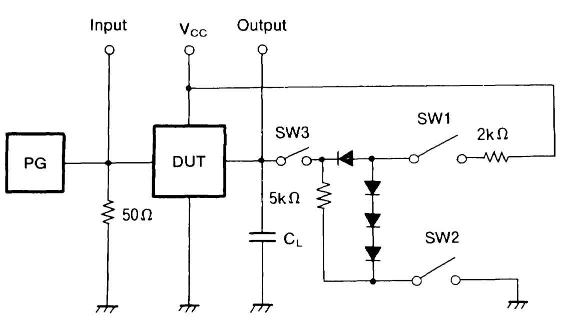
Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{TH}	High threshold voltage	A, $\overline{A}$	V_{OH}=2.7V, I_{OH}=−400μA				0.2	V
V_{TL}	Low threshold voltage	A, $\overline{A}$	V_{OL}=0.5V, I_{OL}=16mA		−0.2			V
$V_{T+}-V_{T-}$	Hysterisis (Note 5)	A, $\overline{A}$				50		mV
V_{IH}	High-level input voltage	OC			2			V
V_{IL}	Low-level input voltage	OC					0.8	V
V_{IK}	Input clamp voltage	OC	I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID}=0.2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{ID}=−0.2V	I_{OL}=8mA		0.31	0.45	V
				I_{OL}=16mA		0.40	0.5	
I_{OZH}	Off-state high-level output current		V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_O=0.4V				−20	μA
I_I	Input current	A, $\overline{A}$	Other inputs 0V	V_I=12V			1	mA
				V_I=−7V			−0.8	
I_{IH}	High-level input current	OC	V_I=2.7V				20	μA
I_{IL}	Low-level input current	OC	V_I=0.4V				−100	μA
r_I	Input resistance	A, $\overline{A}$			11(Note 6)	15		kΩ
I_{OS}	Output short circuit current (Note 7)				−15		−85	mA
I_{CC}	Supply current		All outputs in disable state			55	75	mA

* : Typical values are at V_{CC}=5V, T_a=25℃ and V_{IC}=0V.
Note 5 : Hysteresis is the difference between the positive input threshold voltage V_{T+} and negative input threshold voltage V_{T-}
6 : Minimum value is 12kΩ within T_a=0~75℃.
7 : All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A, $\overline{A}$ to output Y	C_L=15pF(Note 8)		17	35	ns
t_{PHL}				26	35	ns
t_{PZH}	High-level output enable time	C_L=15pF(Note 8)		13	30	ns
t_{PZL}	Low-level output enable time			16	30	ns
t_{PHZ}	High-level output disable time	C_L=5pF(Note 8)		16	35	ns
t_{PLZ}	Low-level output disable time			22	35	ns

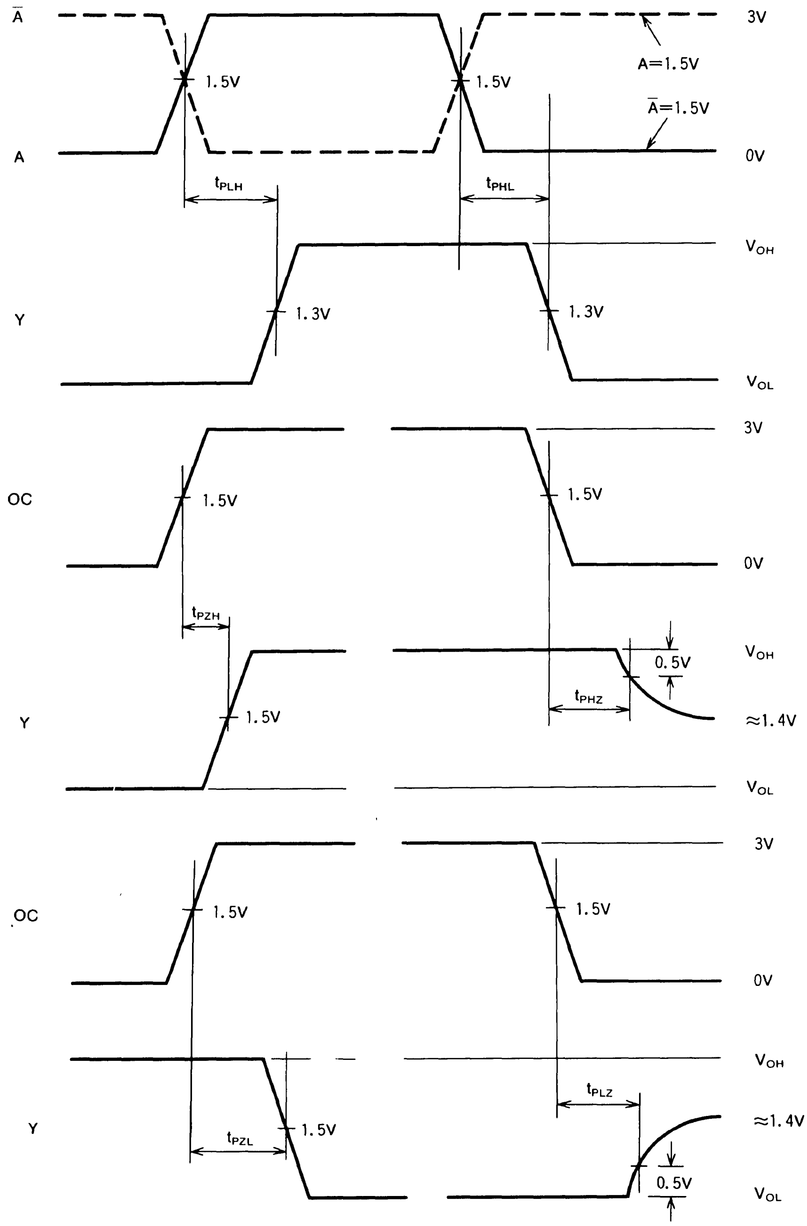
Note 8 : Test circuit



(1) The pulse generator(PG) has the following characteristiscs : PRR=1MHz, t_W=500ns, t_r≦ 5ns, t_f≦ 5ns, Z_O=50Ω
(2) All diodes are high-speed switching diodes (t_{rr}≦ 4ns)
(3) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

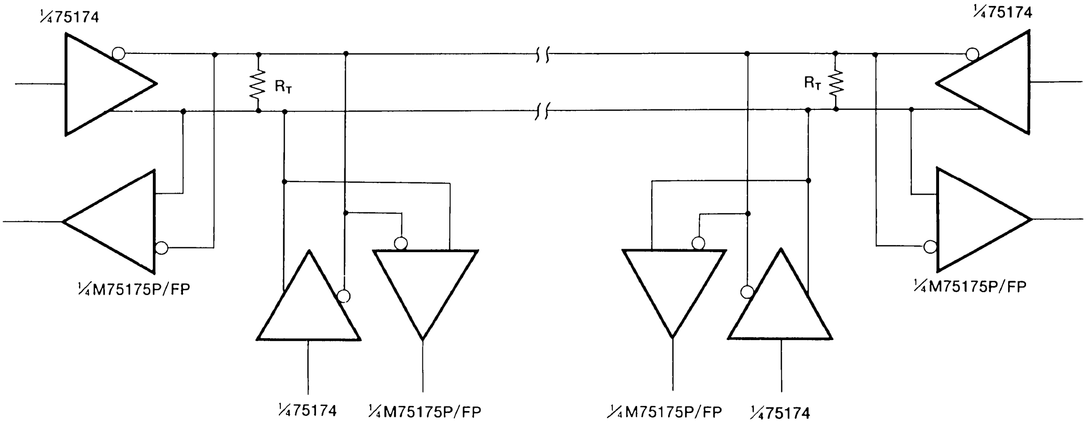
Parameter	SW 1	SW 2	SW3
t_{PLH}, t_{PHL}	—	—	Open
t_{PZH}	Open	Closed	Closed
t_{PZL}	Closed	Open	Closed
t_{PHZ}	Closed	Closed	Closed
t_{PLZ}	Closed	Closed	Closed

TIMING DIAGRAM



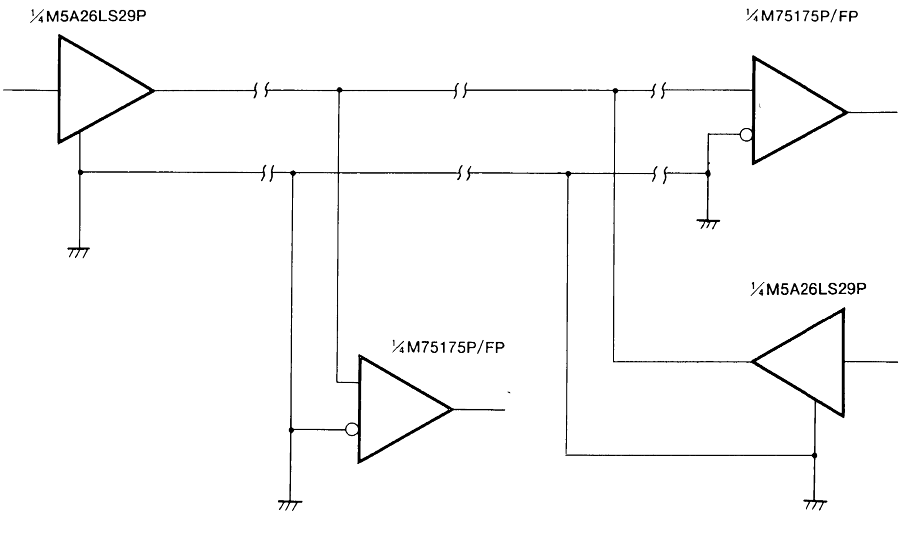
APPLICATION EXAMPLE

a) Balanced type



R_T=Characteristic impedance of transmission line

b) Unbalanced type



M75176P,M75177P M75178P,M75179P

RS-485 TRANSCEIVER

The specifications are subject to change without notice.

FEATURES

- Meets EIA Standards RS-485 and RS-422A
- Multi-point, long-distance, high-speed data transmission is possible
- Driver part, built-in output current limit circuit
- Receiver part, high-input impedance 12kΩ min.

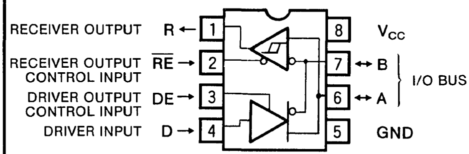
APPLICATION

Digital data transmission for personal computer, POS, and factory automation

Outline of EIA Standard RS-485

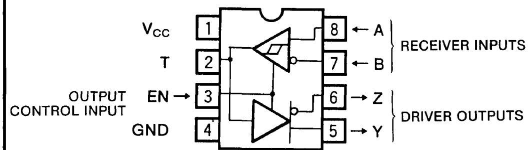
Operating mode		Balanced type
Number of connectable terminals		32 drivers 32 receivers
Maximum length of cable		1200m
Maximum transmission rate	12m	10Mbit/s
	120m	1Mbit/s
	1200m	90Kbit/s
Maximum common mode voltage		+12V −7V
Driver output voltage	loaded	±1.5V
Driver load resistance		54Ω
Driver output leakage current	Power on	±100μA(MAX)
	Power off	−7V≦ V_{com}≦ 12V
Receiver input common mode voltage range		−12V to 12V
Receiver input sensitivity		±200mV
Receiver input resistance		>12kΩ

PIN CONFIGURATION (TOP VIEW)



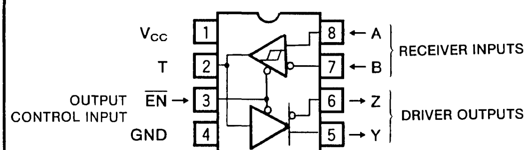
M75176P

Outline 8P4



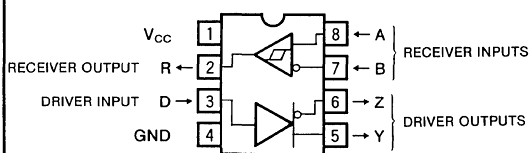
M75177P

Outline 8P4



M75178P

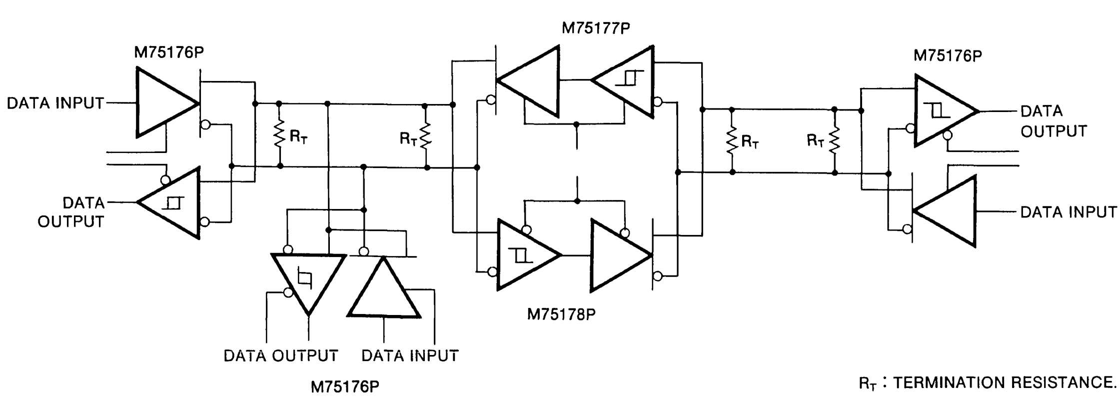
Outline 8P4



M75179P

Outline 8P4

APPRICATION EXAMPLE



R_T : TERMINATION RESISTANCE.

M75188P

QUADRUPLE LINE DRIVER

DESCRIPTION

The M75188P is a semiconductor integrated circuit containing 4 line drivers for use with unbalanced digital data transmission, which meets EIA Standards RS-232-C.

FEATURES

- Output characteristics meet EIA Standards RS-232-C
- Current-limited output ±10mA (typ)
- Power-off output impedance 300Ω (min)
- Slew rate control by output load capacitor
- Input characteristics are compatibe with TTL circuits
- Wide range of supply voltages (V_{CC+}=9~13.2V, V_{CC-}=−9V~13.2V)

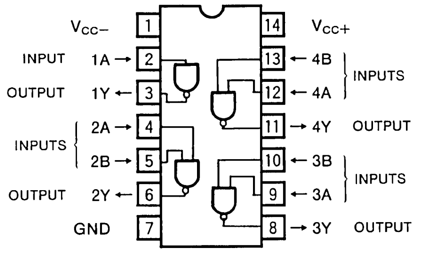
APPLICATION

For use as a data transmission interface in digital equipment

FUNCTIONAL DESCRIPTION

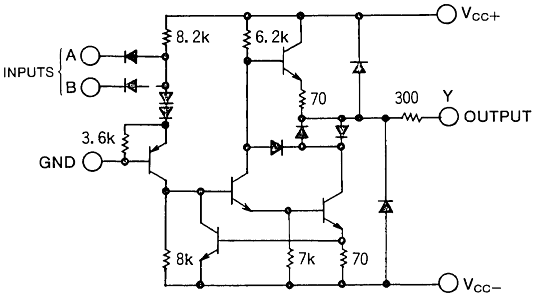
Inputs A and B can be driven directly with TTL circuits.
A resistor of 300Ω is connected in series with the output Y, and the output impedance is 350Ω (typ). Therefore, when use of a transmission line whose characteristic impedance is 100~300Ω, wave form distortion of the signals can be reduced. Connection of termination resistor enables extention of transmission line.
Connection of a capacitor between Y and GND enables slew rate adjustment. Refer to the specifications. Parasitic diodes are connected between Y and positive power supply V_{CC+}, and negative power supply V_{CC-}. Refer to the circuit diagram. Therefore, when voltages higher than V_{CC+} or lower than V_{CC-} are applied to Y, a protective circuit is required to avoid variation of power supply voltage connected to V_{CC+} and V_{CC-}. Refer to the TYPICAL APPLICATION a).
This integrated circuit is suitable for data transmission interface in digital equipment and the output characteristics meet EIA Standard RS-232-C. Refer to Table 1. The M75189P and M75189AP are available as receivers which meet RS-232-C. The transmission form is unbalanced. Refer to TYPICAL APPLICATION b).

PIN CONFIGURATION (TOP VIEW)



OUTLINE 14P4

CIRCUIT DIAGRAM (EACH DRIVER)



UNIT : Ω

FUNCTION TABLE (Note1)

A	B	Y
H	H	L
L	X	H
X	L	H

Note 1 : X : irrelevant

Table 1 Eia standards RS-232-C

	Parameter	RS-232-C	M75188P Corresponding Parameters (Symbol)
Common	Transmission form	Unbalanced	Output Y
	Maximum transmission distance	15m	Extention is possible by connecting C_L
	Maximum transmission speed	20kbit/s	t_{TLH}, t_{THL}, when C_L=2500pF
Driver	Maximum output voltage (no load)	±25V	With V_{CCmax}=13.2V, output voltages never become higher than +25V or lower than −25V.
	Minimum output voltage (loaded)	±5~±15V	V_{OH}, V_{OL}
	Minimum output resistance (power off)	R_O=300Ω	r_O
	Maximum short-circuit output current	±500mA	$I_{OS(H)}$, $I_{OS(L)}$
	Slew rate	Maximum 30V/μs	t_{TLH}, t_{THL}
Receiver	Input resistance	3k~7kΩ	
	Maximum input threshold	−3~+3V	
	Maximum input voltage	−25~+25V	

QUADRUPLE LINE DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC+}	Positive supply voltage		0 ~15	V
V_{CC-}	Negative supply voltage		0 ~−15	V
V_I	Input voltage		−15~+7	V
V_O	Output voltage		−15~+15	V
P_d	Power dissipation	When T_a=25℃ (Note 2)	1	W
Tstg	Storage temperature range		−65~+150	℃

Note 2 : Refer to typical characteristics when T_a>25℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC+}	Positive power supply	9		13.2	V
V_{CC-}	Negative power supply	−9		−13.2	V
V_I	Input voltage	0		5.5	V
Topr	Operating free-air ambient temperature range	0		75	℃

ELECTRICAL CHARACTERISTICS (V_{CC+}=9V, V_{CC-}=−9V, T_a= 0 ~75℃, unless otherwise noted)

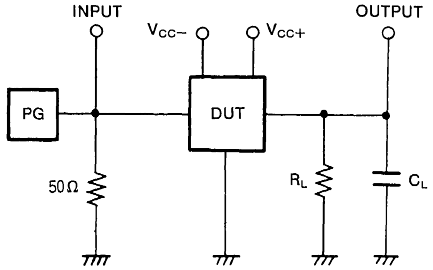
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IL}=0.8V	V_{CC+}=9V, V_{CC-}=−9V	6	7		V
		R_L=3kΩ	V_{CC+}=13.2V, V_{CC-}=−13.2V	9	10.5		
V_{OL}	Low-level output voltage	V_{IL}=1.9V	V_{CC+}=9V, V_{CC-}=−9V		−7	−6	V
		R_L=3kΩ	V_{CC+}=13.2V, V_{CC-}=−13.2V		−10.5	−9	
I_{IH}	High-level input current	V_I=5V				10	μA
I_{IL}	Low-level input current	V_I=0V			−1	−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (Note 3)	V_I=0.8V, V_O=0V		−6	−10	−12	mA
$I_{OS(L)}$	Low-level short-circuit output current (Note 3)	V_I=1.9V, V_O=0V		6	10	12	mA
r_O	Output resistance (power off)	V_{CC+}=0V, V_{CC-}=0V, V_O=−2~+2V		300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+}=9V	V_I=1.9V		15	20	mA
		No load	V_I=0.8V		3.7	6	
		V_{CC+}=12V	V_I=1.9V		19	25	
		No load	V_I=0.8V		5.2	7	
		V_{CC+}=15V No load Ta=25℃	V_I=1.9V			34	
			V_I=0.8V			12	
I_{CC-}	Supply current from V_{CC-}	V_{CC-}=−9V	V_I=1.9V		−13	−17	mA
		No load	V_I=0.8V			−0.015	
		V_{CC-}=−12V	V_I=1.9V		−18	−23	
		No load	V_I=0.8V			−0.015	
		V_{CC-}=−15V No load Ta=25℃	V_I=1.9V			−34	
			V_I=0.8V			−2.5	
P_d	Total power dissipation	V_{CC+}=9V, V_{CC-}=−9V, No load				333	mW
		V_{CC+}=12V, V_{CC-}=−12V, No load				576	

* : All typical values are at T_a=25℃.
Note 3 : All measurements should be done quickly and not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS (V_{CC+}=9V, V_{CC-}=−9V, T_a=25℃, unless otherwise noted)

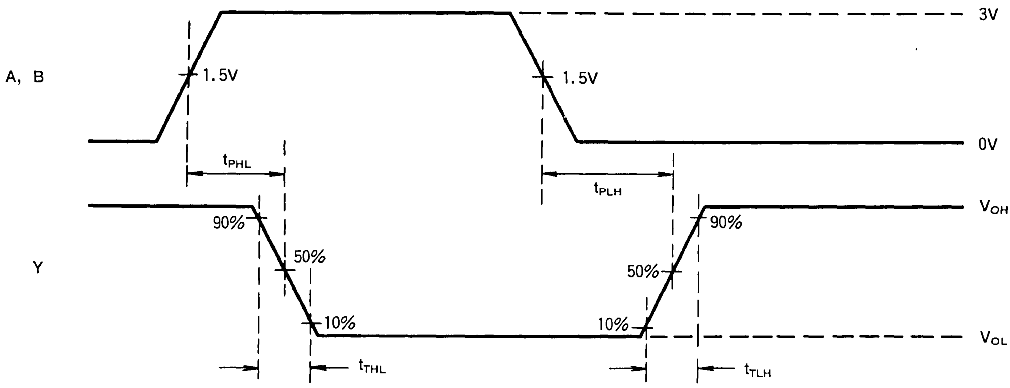
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time, from input A, B to output Y	R_L=3kΩ C_L=15pF (Note 4)		285	350	ns
t_{PHL}				60	175	ns
t_{TLH}	Low-to-high, high-to-low output transition time, from input A, B to output Y			65	100	ns
t_{THL}				36	75	ns
t_{TLH}	Low-to-high, high-to-low output transition time, from input A, B to output Y	R_L=3k~7kΩ, C_L=2500pF (Note 4) Transition time between +3 V and −3 V		3.6	5	μs
t_{THL}				3.4	5	μs

Note 4 : Test circuit



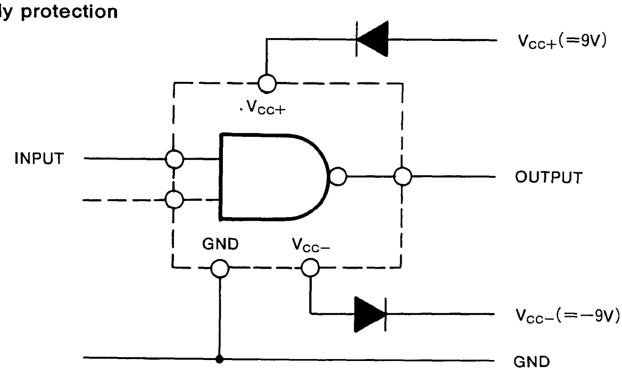
(1) The pulse generator (PG) has the following characteristics : PRR=1MHz, t_W=500ns, V_P=3V_{P-P}, Z_O=50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

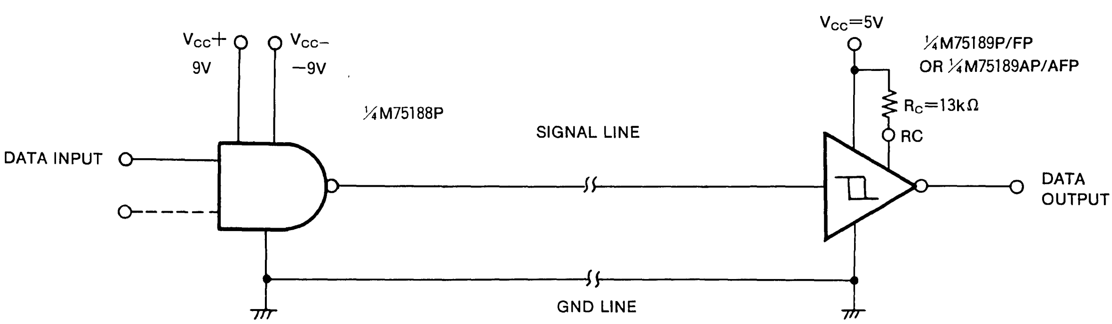


TYPICAL APPLICATION

a) Power supply protection

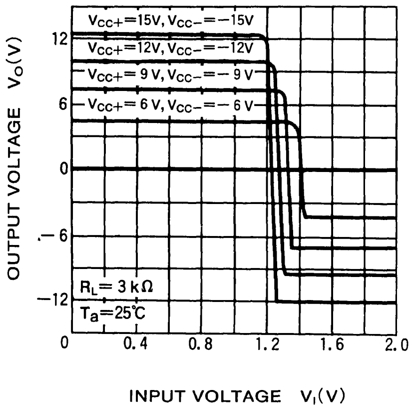


b) Combination of a driver with a receiver

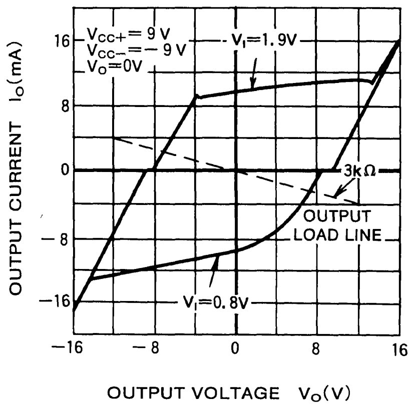


TYPICAL CHARACTERISTICS

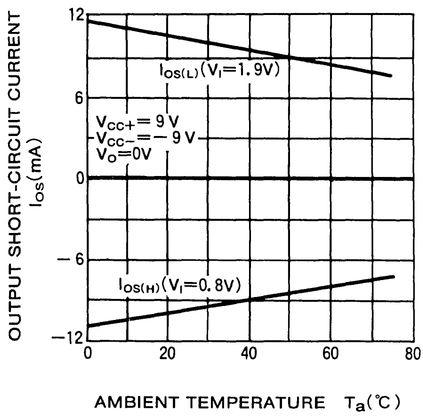
OUTPUT VOLTAGE VS INPUT VOLTAGE



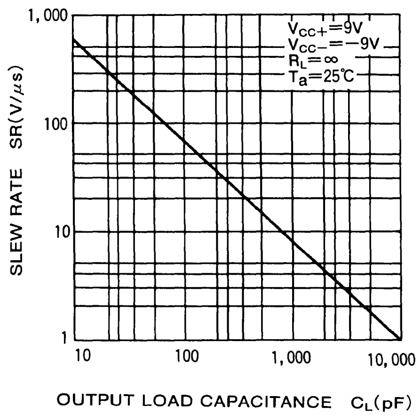
OUTPUT CURRENT VS OUTPUT VOLTAGE



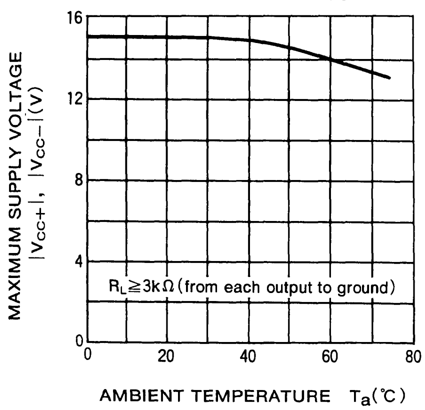
OUTPUT SHORT-CIRCUIT CURRENT VS AMBIENT TEMPERATURE



SLEW RATE VS OUTPUT LOAD CAPACITANCE



MAXIMUM SUPPLY VOLTAGE VS AMBIENT TEMPERATURE



M75189P/FP

QUADRUPLE LINE RECEIVER

DESCRIPTION

The M75189P/FP is a semiconductor integrated circuit containing 4 line receivers for use with unbalanced digital data transmission, which meets EIA Standards RS-232-C.

FEATURES

- Input characteristics meet EIA Standards RS-232-C
- Input resistance of 3k to 7kΩ (V_I=−3 to −25V/3 to 25V)
- Input voltage range from −30 to +30V
- Input hysteresis is 0.25V typ.
- Response control provides :
  input threshold shifting,
  input noise filtering.
- Output characteristics are compatible with TTL circuits
- Operates from single 5V power supply

APPLICATION

For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

A 4kΩ (typ) resistor is connected in series with input I and the input impedance is 3k to 7kΩ, (the applied input voltage V_I equalling −3 to −25V or 3 to 25V).

A resistor or a resistor and bias voltage can be connected between RC and GND to shift the input threshold voltage levels.

The input hysteresis is set to 0.25V (typ).

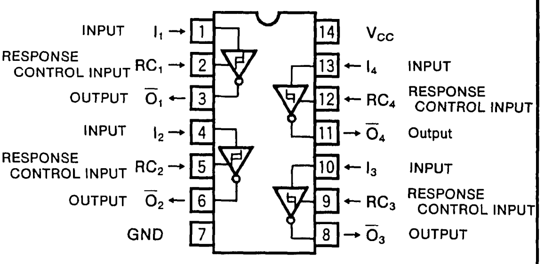
Input noise can be rejected by connecting a capacitor between RC and GND. Refer to TYPICAL APPLICATION b).

Output $\overline{O}$ is pulled up by 2kΩ resistor to V_{CC} so that the AND tie can be made, and can drive TTL circuits directly.

The supply voltage is from a single 5V power supply.

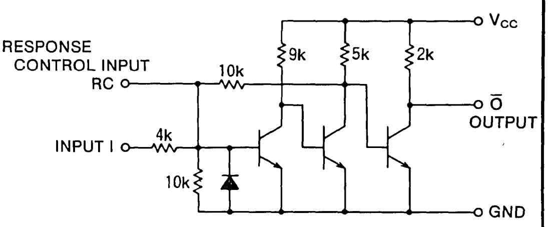
This integrated circuit is suitable for data transmission interface in digital equipment since the input characteristics meet EIA Standards RS-232-C. Refer to Table 1, which shows the EIA Standards RS-232-C. M75188P may be used as a driver which meets these standards. An unbalanced form of transmission is used. Refer to TYPICAL APPLICATION a) for further information.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4
14P2N

CIRCUIT DIAGRAM (EACH CIRCUIT)



UNIT : Ω

Table 1 Eia standards RS-232-C

	Parameter	RS-232-C	M75189P Corresponding Parameters (Symbol)
Common	Transmission form	Unbalanced	Input I
	Maximum transmission distance	15m	
	Maximum transmission speed	20kbit/s	
Driver	Maximum output voltage (no load)	±25V	
	Minimum output voltage (loaded)	±5～±15V	
	Minimum output resistance (power off)	R_O=300Ω	
	Maximum short-circuit output current	±500mA	
	Slew rate	Maximum 30V/μs	
Receiver	Input resistance	3k～7kΩ	
	Maximum input threshold	−3～+3V	V_{T+}, V_{T-}
	Maximum input voltage	−25～+25V	I_{IH}, I_{IL}

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+10	V
V_I	Input voltage			−30~+30	V
I_O	Output current		When output is low	20	mA
P_d	Power dissipation	DIP	T_a=25℃ (Note 1)	1000	mW
		SOP	T_a=25℃ (Note 2)	570	
T_{stg}	Storage temperature range			−65~+150	℃

Note 1 : A derating of 9.1mW/℃ should be made when T_a≧40℃
2 : A derating of 4.5mW/℃ should be made when T_a≧25℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_I	Input voltage	−15		15	V
T_{opr}	Operating free-air ambient temperature range	0		75	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit	Measurement circuit
				Min	Typ*	Max		
V_{T+}	Positive-going theshold voltage	T_a=25℃		1		1.5	V	1
				0.9		1.6		
V_{T-}	Negative-going theshold voltage	T_a=25℃		0.75		1.25	V	1
				0.65		1.25		
$V_{T+}-V_{T-}$	Hysteresis	T_a=25℃		0	0.25	0.75	V	1
V_{OH}	High-level output voltage	V_I=0.75V, I_{OH}=−0.5mA		2.6	4	5	V	1
		V_I : Open, I_{OH}=−0.5mA		2.6	4	5		
V_{OL}	Low-level output voltage	V_I=3V, I_{OL}=10mA			0.2	0.45	V	1
I_{IH}	High-level input current	V_I=25V	DIP	3.6		8.3	mA	2
		V_I=15V	SOP			5.0		
		V_I=3V		0.43				
I_{IL}	Low-level input current	V_I=−25V	DIP	−3.6		−8.3	mA	2
		V_I=−15V	SOP			−5.0		
		V_I=−3V		−0.43				
I_{OS}	Short-circuit output current	V_I=0V, V_O=0V		−1.6	−2.5	−5	mA	3
I_{CC}	Supply current	V_{CC}=5V, V_I=5V			20	26	mA	2

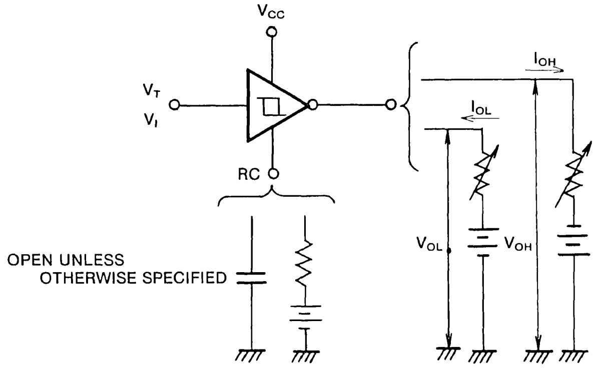
* : All typical values are at V_{CC1}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	Measurement circuit
			Min	Typ	Max		
t_{PLH}	Low-to-high-level, high-to-low-level output	C_L=15pF, R_L=3.9KΩ		25	85	ns	4
t_{PHL}	propagation time, from input I to output O	C_L=15pF, R_L=390Ω		25	50	ns	
t_{TLH}	Low-to-high-level output transition time	C_L=15pF, R_L=3.9kΩ		120	175	ns	
t_{THL}	High-to-low-level output transition time	C_L=15pF, R_L=390Ω		10	20	ns	

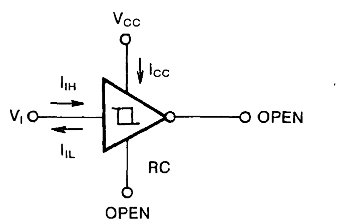
MEASUREMENT CIRCUITS

1



Measurement Circuit for V_{T+}, V_{T-}, V_{OH}, V_{OL}

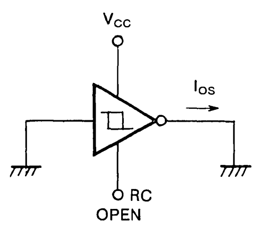
2



Note : I_{CC} is measured for all 4 circuits simultaneously

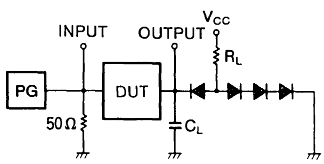
Measurement Circuit for I_{CC}, I_{IH}, I_{IL}

3

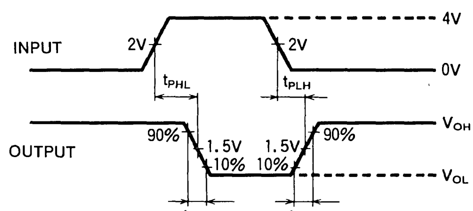


Measurement Circuit for I_{OS}

4



Measurement Circuit



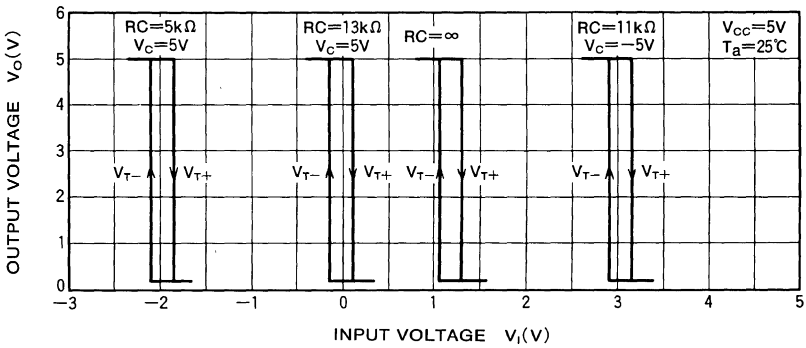
VOLTAGE WAVEFROM

1. The pulse generator (PG) has the following characteristics : PRR=1MHz, $t_r \leq 10ns$, $t_f \leq 10ns$, $t_{PW}=500ns$, $V_P=4V_{P-P}$, $Z_O=50\Omega$
2. All diodes are switching diodes ($t_{rr} \leq 4ns$)
3. C_L includes probe and jig capacitance.
4. RC is open.

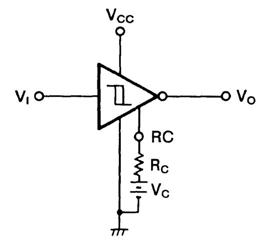
Measurement circuit for switching characteristics and voltage wave form.

TYPICAL CHARACTERISTICS

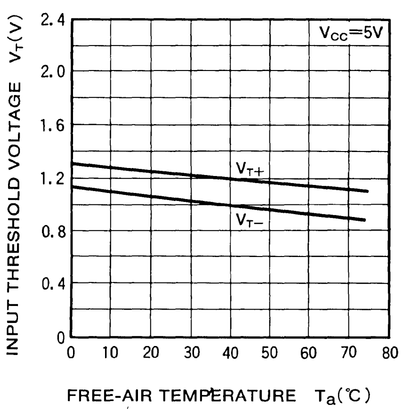
OUTPUT VOLTAGE VS INPUT VOLTAGE



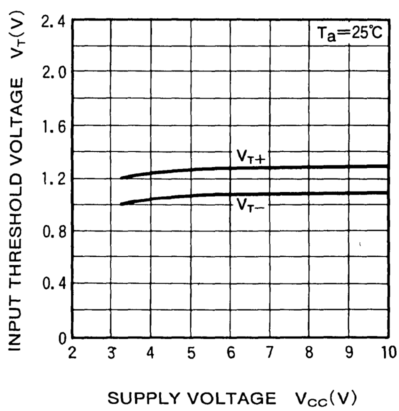
MEASUREMENT CIRCUIT



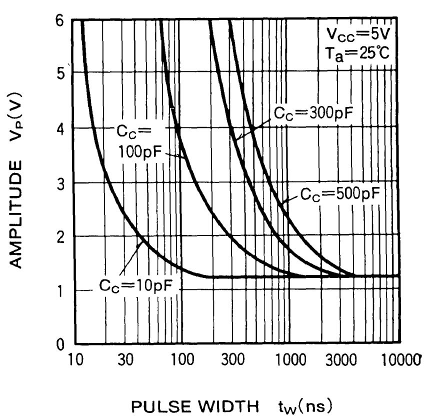
INPUT THRESHOLD VOLTAGE VS FREE-AIR TEMPERATURE



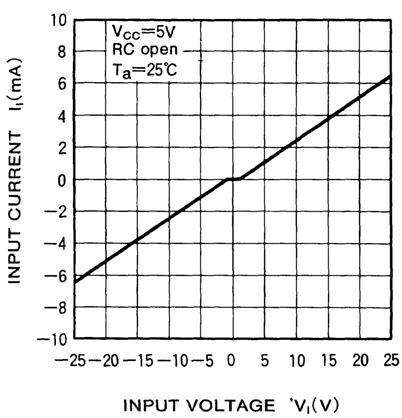
INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



NOISE REJECTION CHARACTERISTICS

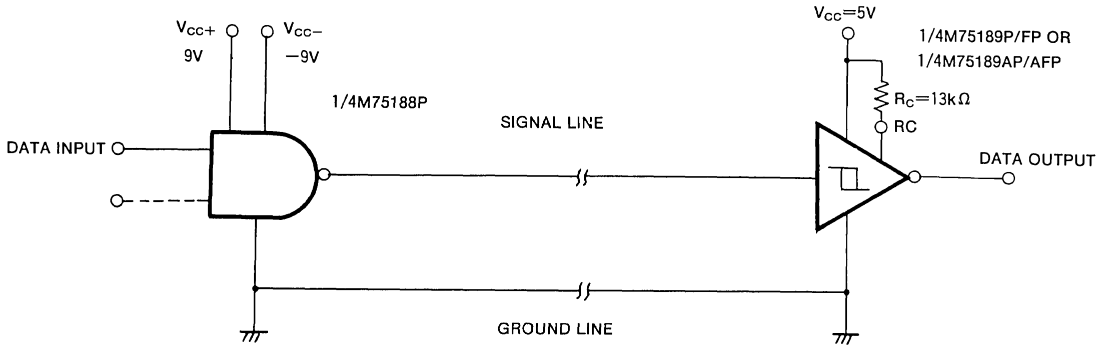


INPUT CURRENT VS INPUT VOLTAGE

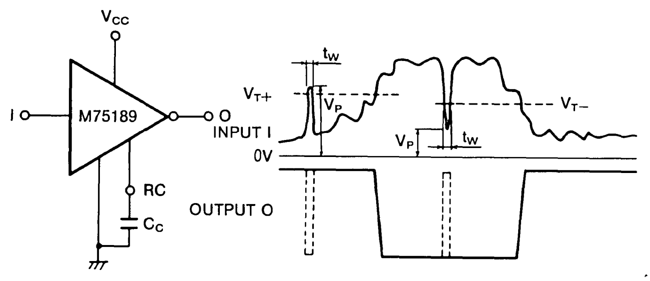


TYPICAL APPLICATION

a) COMBINATION OF DRIVER AND RECEIVER



b) WAVEFORM RESTORATION AND NOISE REJECTION



As in the above diagram, in preventing inversion of output $\overline{O}$ by input pulse, whose width t_W and amplitude greater than V_{T+} or less than V_{T-}, connect capacitor C_C, the value of which can be obtained from a noise rejection characteristics table. Shorten the rise and fall time of input I if C_C is connected.

M75189AP/AFP

QUADRUPLE LINE RECEIVER

DESCRIPTION

The M75189AP/AFP is a semiconductor integrated circuit containing 4 line receivers for use with unbalanced digital data transmission, which meets EIA Standards RS-232-C.

FEATURES

- Input characteristics meet EIA Standards RS-232-C
- Input resistance of 3k to 7kΩ (V_I=−3 to −25V/3 to 25V)
- Input voltage range from −30 to +30V
- Input hysteresis is 1.0V typ.
- Response control provides :
  input threshold shifting,
  input noise filtering.
- Output characteristics are compatible with TTL circuits
- Operates from single 5V power supply

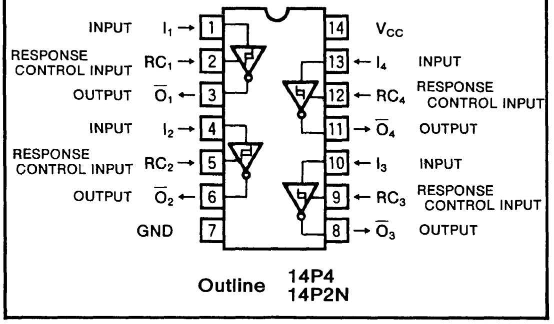
APPLICATION

For use as a data transmission interface in digital equipment.

FUNCTIONAL DESCRIPTION

A 4kΩ (typ) resistor is connected in series with input I and the input impedance is 3k to 7kΩ, (the applied input voltage V_I equalling −3 to −25V or 3 to 25V).
A resistor or a resistor and bias voltage can be connected between RC and GND to shift the input threshold voltage levels.
The input hysteresis is set to 1.0V (typ).
Input noise can be rejected by connecting a capacitor between RC and GND. Refer to TYPICAL APPLICATION b).
Output $\overline{O}$ is pulled up by 2kΩ resistor to V_{CC} so that the AND tie can be made, and can drive TTL circuits directly.
The supply voltage is from a single 5V power supply.
This integrated circuit is suitable for data transmission interface in digital equipment since the input characteristics meet EIA Standards RS-232-C. Refer to Table 1, which shows the EIA Standards RS-232-C. M75188P may be used as a driver which meets these standards. An unbalanced form of transmission is used. Refer to TYPICAL APPLICATION a) for further information.

PIN CONFIGURATION (TOP VIEW)



CIRCUIT DIAGRAM (EACH CIRCUIT)

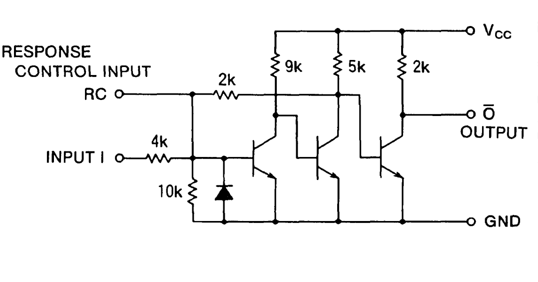


Table 1 Eia standards RS-232-C

	Parameter	RS-232-C	M75189AP Corresponding Parameters (Symbol)
Common	Transmission form	Unbalanced	Input I
	Maximum transmission distance	15m	
	Maximum transmission speed	20kbit/s	
Driver	Maximum output voltage (no load)	±25V	
	Minimum output voltage (loaded)	±5～±15V	
	Minimum output resistance (power off)	R_O=300Ω	
	Maximum short-circuit output current	±500mA	
	Slew rate	Maximum 30V/μs	
Receiver	Input resistance	3k～7kΩ	
	Maximum input threshold	−3～+3V	V_{T+}, V_{T-}
	Maximum input voltage	−25～+25V	I_{IH}, I_{IL}

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5~+10	V
V_I	Input voltage			−30~+30	V
I_O	Output current		When output is low	0~20	mA
P_d	Power dissipation	DIP	T_a=25℃ (Note 1)	1000	mW
		SOP	T_a=25℃ (Note 2)	570	
T_{stg}	Storage temperature range			−65~+150	℃

Note 1 : A derating of 9.1mW/℃ should be made when $T_a \geq 40$℃
2 : A derating of 4.5mW/℃ should be made when $T_a \geq 25$℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_I	Input voltage	−15		15	V
T_{opr}	Operating free-air ambient temperature range	0		75	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit	Measurement circuit
				Min	Typ*	Max		
V_{T+}	Positive-going theshold voltage	T_a=25℃		1		1.5	V	1
				0.9		1.6		
V_{T-}	Negative-going theshold voltage	T_a=25℃		0.75		1.25	V	1
				0.65		1.25		
$V_{T+}-V_{T-}$	Hysteresis	T_a=25℃		0	0.25	0.75	V	1
V_{OH}	High-level output voltage	V_I=0.75V, I_{OH}=−0.5mA		2.6	4	5	V	1
		V_I : Open, I_{OH}=−0.5mA		2.6	4	5		
V_{OL}	Low-level output voltage	V_I=3V, I_{OL}=10mA			0.2	0.45	V	1
I_{IH}	High-level input current	V_I=25V	DIP	3.6		8.3	mA	2
		V_I=15V	SOP			5.0		
		V_I=3V		0.43				
I_{IL}	Low-level input current	V_I=−25V	DIP	−3.6		−8.3	mA	2
		V_I=−15V	SOP			−5.0		
		V_I=−3V		−0.43				
I_{OS}	Short-circuit output current	V_I=0V, V_O=0V		−1.6	−2.5	−5	mA	3
I_{CC}	Supply current	V_{CC}=5V, V_I=5V			20	26	mA	2

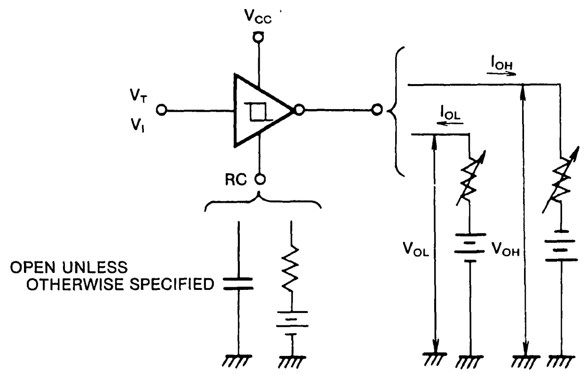
* : All typical values are at V_{CC1}=5V, T_a=25℃

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	Measurement circuit
			Min	Typ	Max		
t_{PLH}	Low-to-high-level, high-to-low-level output	C_L=15pF, R_L=3.9KΩ		25	85	ns	4
t_{PHL}	propagation time, from input I to output O	C_L=15pF, R_L=390Ω		25	50	ns	
t_{TLH}	Low-to-high-level output transition time	C_L=15pF, R_L=3.9kΩ		120	175	ns	
t_{THL}	High-to-low-level output transition time	C_L=15pF, R_L=390Ω		10	20	ns	

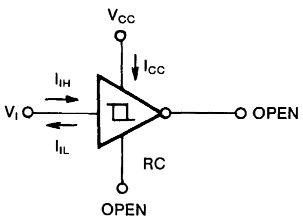
MEASUREMENT CIRCUITS

1



Measurement Circuit for V_{T+}, V_{T-}, V_{OH}, V_{OL}

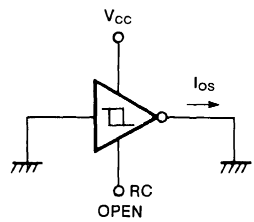
2



Note : I_{CC} is measure for all 4 circuits simultaneously.

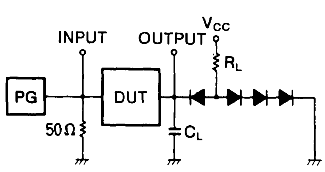
Measurement Circuit for I_{CC}, I_{IH}, I_{IL}

3

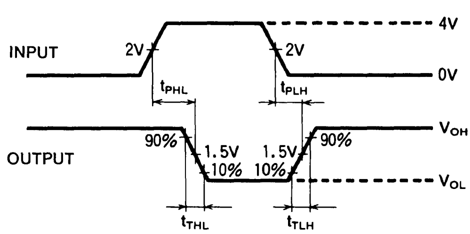


Measurement Circuit for I_{OS}

4



Measurement Circuit



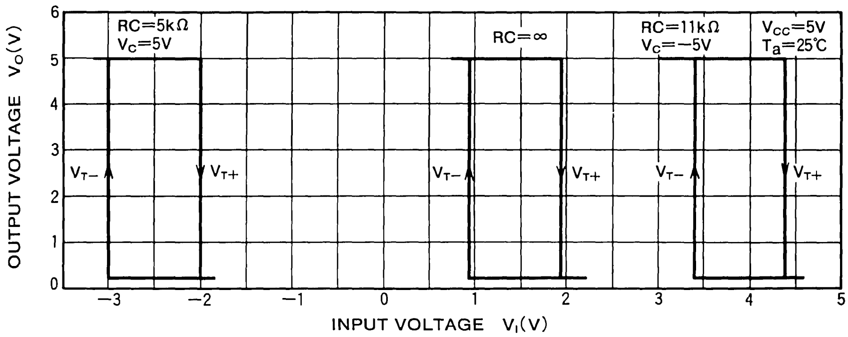
VOLTAGE WAVEFROM

1. The pulse generator (PG) has the following characteristics : PRR=1MHz, $t_r \leq 10$ns, $t_f \leq 10$ns, t_{PW}=500ns, $V_P=4V_{P-P}$, $Z_O=50\Omega$
2. All diodes are high- speed switching diodes ($t_{rr} \leq 4$ns)
3. C_L includes probe and jig capacitance.
4. RC is open.

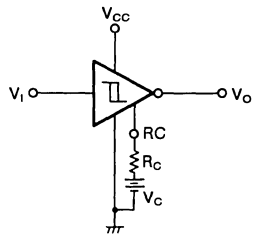
Measurement Circuit for switching characteristics and voltage waveform.

TYPICAL CHARACTERISTICS

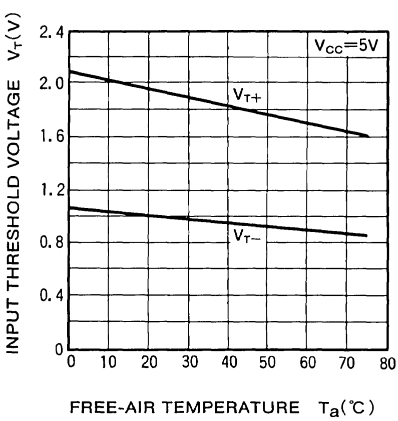
OUTPUT VOLTAGE VS INPUT VOLTAGE



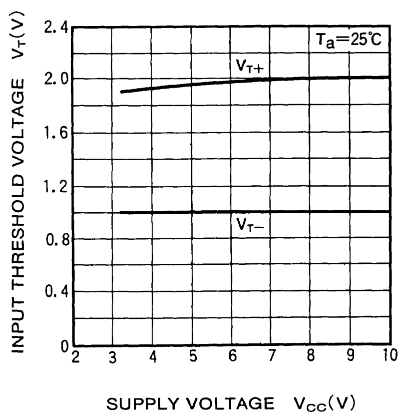
MEASUREMENT CIRCUIT



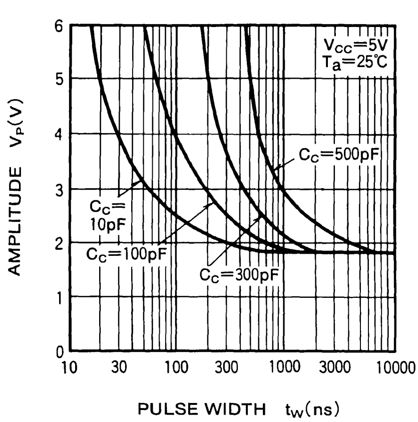
INPUT THRESHOLD VOLTAGE VS FREE-AIR TEMPERATURE



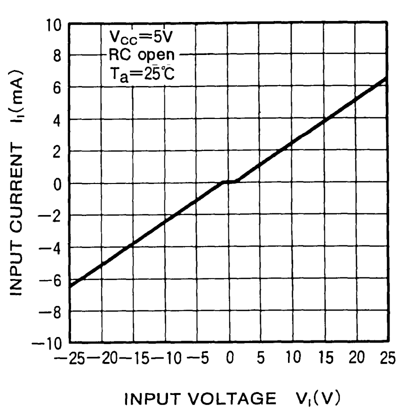
INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



NOISE REJECTION CHARACTERISTICS

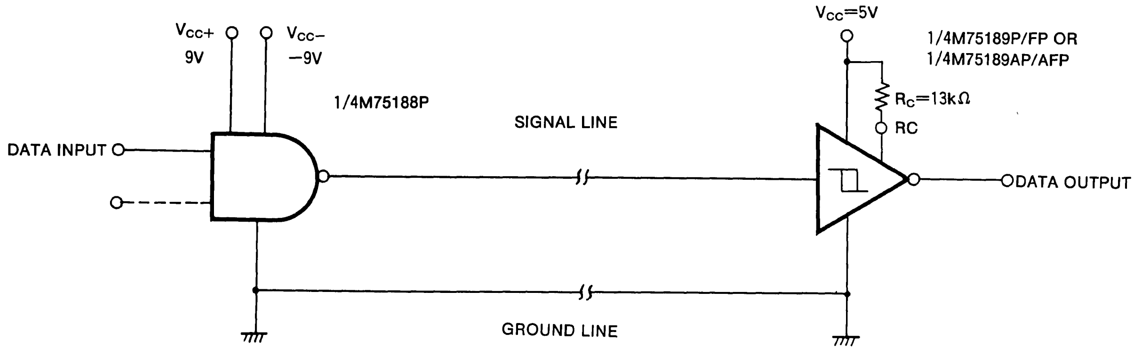


INPUT CURRENT VS INPUT VOLTAGE

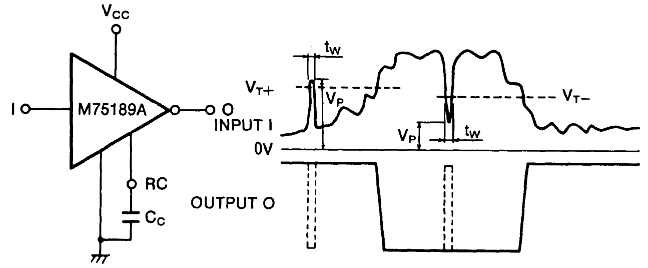


TYPICAL APPLICATION

a) COMBINATION OF DRIVER AND RECEIVER



b) WAVEFORM RESTORATION AND NOISE REJECTION



As in the above diagram, in preventing inversion of output O by input pulse, whose width t_W and amplitude greater than V_{T+} or less than V_{T-}, connect capacitor C_C, the value of which can be obtained from a noise rejection characteristics table. Shorten the rise and fall time of input I if C_C is connected.

M751701P

RS-232C LINE DRIVER and RECEIVER

DESCRIPTION

The M751701P is a semiconductor integrated circuit with one digital data transmission line driver and one digital data transmission line receiver, both of which satisfy EIA Standard RS-232C.

FEATURES

<Common>

- Wide supply voltage range (±4.5~±15V)

<Driver Section>

- When power is off, output impedance is 300Ω(min.)
- Output limit current is ±11mA(typ.)
- Through rate control by output load capacity
- Input characteristic is TTL level

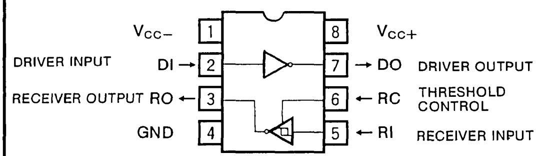
<Receiver Section>

- Wide input voltage range (±3~±25V)
- Input resistance is 3 to 7kΩ (V_I=±3~±25V)
- Input hysterisis width is 1.0V(typ.)
- Threshold control input included
- Output characteristic is TTL level

APPLICATION

Data transmission interface for digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

FUNCTIONAL DESCRIPTION

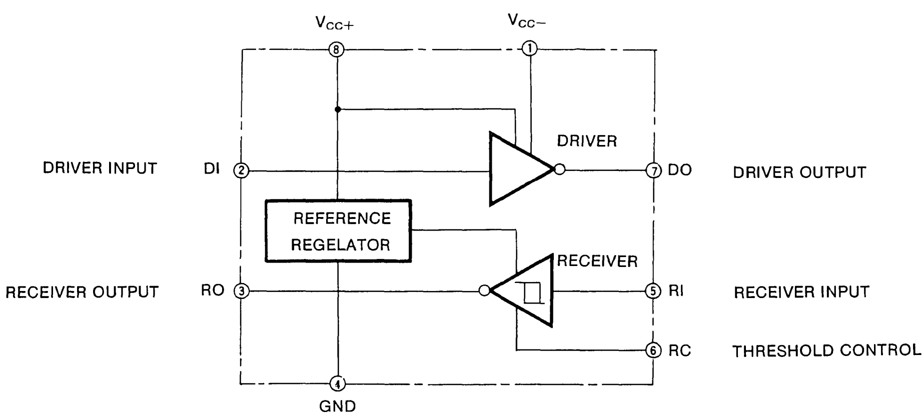
The driver section and the receiver section have the same characteristics as the M75188P and the M75189AP, respectively.

With a reference regulator circuit included, M751701P can be used over a wide range of supply voltages ±4.5~±15V.

Connecting a load capacity between the driver output and ground enables through-rate control.

The receiver section has a threshold control terminal RC and a resistor or a resistor together with a bias power supply serial circuit can be connected between RC and ground to enable variation of input threshold voltage.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=0～+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC+}	Positive supply voltage		−0.4～+18	V
V_{CC-}	Negative supply voltage		−18～+0.4	V
$V_{I(D)}$	Driver input voltage		−5～+18	V
$V_{I(R)}$	Receiver input voltage		−30～+30	V
$V_{O(D)}$	Driver output voltage		−15～+15	V
$V_{O(R)}$	Receiver output voltage		−0.4～+7	V
$I_{O(D)}$	Driver output current		50	mA
I_{RC}	Threshold control input current		−10～+10	mA
T_{stg}	Storage temperature range		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max	
V_{CC+}	Positive power voltage	4.5		15	V
V_{CC-}	Negative power voltage	−4.5		−15	V
I_{RC}	Threshold control input current	−5.5		+5.5	mA
$V_{I(D)}$	Driver input voltage			15	V
$V_{I(R)}$	Receiver input voltage	−25		+25	V
$V_{O(R)}$	Driver output current			24	mA
T_{opr}	Operating temperature range	0		75	℃

ELECTRICAL CHARACTERISTICS

Common (T_a=0～75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ.*	Max	
I_{CC+}	Positive power supply current	V_{CC+}=5V	$V_{I(D)}$=2.0V		6.5	8.4	mA
		V_{CC+}=9V	$V_{I(R)}=V_{T+(max)}$		9.2	11.9	
		V_{CC+}=12V	Unloaded		10.2	14.0	
		V_{CC+}=5V	$V_{I(D)}$=0.8V		2.5	3.4	
		V_{CC+}=9V	$V_{I(R)}=V_{T-(min)}$		3.7	5.1	
		V_{CC+}=12V	Unloaded		3.9	5.6	
I_{CC-}	Negative power supply current	V_{CC-}=−5V	$V_{I(D)}$=2.0V		−2.5	−3.1	mA
		V_{CC-}=−9V	$V_{I(R)}=V_{T+(max)}$		−3.8	−4.9	
		V_{CC-}=−12V	Unloaded		−4.7	−6.1	
		V_{CC-}=−5V	$V_{I(D)}$=0.8V		−0.8	−1.2	
		V_{CC-}=−9V	$V_{I(R)}=V_{T-(min)}$		−1.0	−2.0	
		V_{CC-}=−12V	Unloaded		−1.0	−2.0	
I_{CC+}	Positive power supply current	V_{CC+}=5V	$V_{I(R)}=V_{T+(max)}$, $V_{I(D)}$=0V		5.1	6.4	mA
		V_{CC+}=12V	V_{CC-}=0V, Unloaded		7.0	9.1	

* : All typical values are at T_a=25℃

Driver Section (V_{CC+}=12V, V_{CC-}=−12V, and T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Typ.*	Max	Unit
V_{IH}	"H" input voltage			2.0			V
V_{IL}	"L" input voltage					0.8	V
V_{OH}	"H" output voltage	V_{CC}=±5V	$V_{I(D)}$=0.8V, R_L=3kΩ	3.2	3.7		V
		V_{CC}=±9V		6.5	7.2		
		V_{CC}=±12V		8.9	9.8		
V_{OL}	"L" output voltage	V_{CC}=±5V	$V_{I(D)}$=2.0V, R_L=3kΩ		−3.6	−3.2	V
		V_{CC}=±9V			−7.1	−6.4	
		V_{CC}=±12V			−9.7	−8.8	
I_{IH}	"H" input current		$V_{I(D)}$=7V			5	μA
I_{IL}	"L" input current		$V_{I(D)}$=0V		−0.14	−0.4	mA
$I_{OS(H)}$	"H" output short current		$V_{I(D)}$=0.8V, $V_{O(D)}$=0V	−6.0	−11.5	−14.0	mA
$I_{OS(L)}$	"L" output short current		$V_{I(D)}$=2.0V, $V_{O(D)}$=0V	6.0	9.5	14.0	mA
r_O	Output resistance		V_{CC}=±0V, $V_{O(D)}$=−2~+2V	300			Ω

* : All typical volues are at T_a=25℃.

Receiver Section (V_{CC+}=12V, V_{CC-}=−12V, and T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min	Typ.*	Max	Unit
V_{T+}	Positive direction threshold voltage			1.2	1.9	2.3	V
V_{T-}	Negative direction threshold voltage			0.6	0.95	1.2	V
$V_{T+}-V_{T-}$	Hysterisis width			0.6	1.0		V
V_{OH}	"H" output voltage	V_{CC}=±5V	$V_{I(R)}=V_{T-(min)}$, I_{OH}=−10μA	3.7	4.1	5.0	V
		V_{CC}=±12V		4.4	4.7	5.5	
		V_{CC}=±5V	$V_{I(R)}=V_{T-(min)}$, I_{OH}=−0.4mA	3.1	3.4	4.3	
		V_{CC}=±12V		3.6	4.0	4.8	
V_{OL}	"L" output voltage		$V_{I(R)}=V_{T+(max)}$, I_{OL}=24mA		0.2	0.3	V
I_{IH}	"H" input current		$V_{I(R)}$=25V	3.6	6.2	8.3	mA
			$V_{I(R)}$=3V	0.43	0.7	1.0	
I_{IL}	"L" input current		$V_{I(R)}$=−25V	−3.6	−6.2	−8.3	mA
			$V_{I(R)}$=−3V	−0.43	−0.7	−1.0	
I_{OS}	Output short current		$V_{I(R)}=V_{T-(min)}$		−2.8	−3.7	mA

* : All typical values are at T_a=25℃.

SWITCHING CHARACTERISTICS (V_{CC+}=12V, V_{CC-}=−12V, and T_a=25℃, unless otherwise noted)

Driver Section

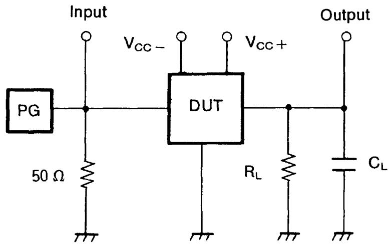
Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{PLH}	Outputs "L−H", "H−L" propagation time	R_L=3kΩ, C_L=50pF		250	480	ns
t_{PHL}				60	150	ns
t_{TLH}	Outputs "L−H", "H−L" transition time			100	180	ns
t_{THL}				100	160	ns
t_{TLH}	Outputs "L−H", "H−L" transition time	R_L=3kΩ~7kΩ, C_L=2500pF, Output between −3 and +3V		1.4	3.0	μs
t_{THL}				1.6	3.0	μs

Receiver Section

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{PLH}	Outputs "L−H", "H−L" propagation time	R_L=400Ω, C_L=50pF		200	240	ns
t_{PHL}				45	100	ns
t_{TLH}	Outputs "L−H", "H−L" transition time			190	360	ns
t_{THL}				18	35	ns

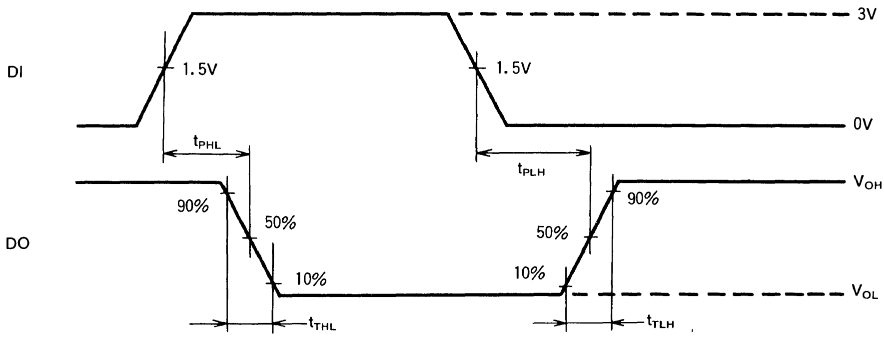
SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT

Driver Section

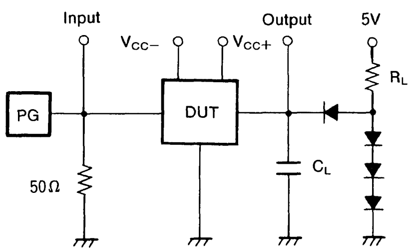


(1) Pulse generator (PG) performance
PRR=1MHz, t_W=500ns, V_P=3$V_{P\text{-}P}$, Z_O=50Ω
(2) C_L includes stray capacitance and jig capacitance.

Timing Diagram



Receiver Section



(1) Pulse generator (PG) performance
PRR=1MHz, t_W=500ns, V_P=4$V_{P\text{-}P}$, Z_O=50Ω
(2) C_L includes stray capacitance and jig capacitance.
(3) RC terminal is open.

Timing Diagram

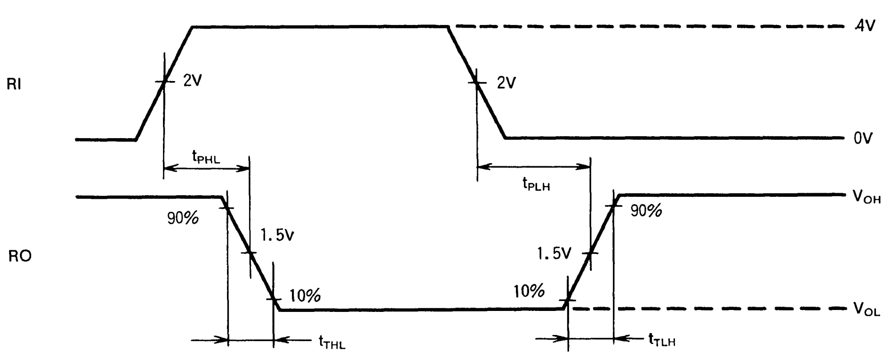


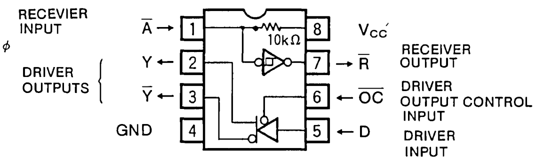
PHOTO-COUPLER DRIVER AND RECEIVER

DESCRIPTION

The M753114P is a semiconductor integrated circuit that includes a set of high-current driver and Schmitt trigger inverter receiver. Combining it with a high-speed photocoupler enables high-speed, long-distance transmissions with excellent noise resistance. Please refer to the application example.

The driver input and receiver output are TTL level, enabling direct connection to TTL digital systems.

PIN CONFIGURATION (TOP VIEW)



OUTLINE 8P4

FEATURES

<Common>

- High-speed operation (can handle 10 Mbps)
- Data flow pin arrangement enabling easy mounting
- Single 5V power supply

<Driver Section>

- Differential output (balanced transmission)
- High-current drive capacity ($I_O = \pm 20mA$)
- Output three-state control input
- Input can be directly connected to TTL

<Receiver Section>

- Hysterisis built in (0.8V typ)
- Fail-safe function
- TTL compatible output

FUNCTION TABLE

Driver section				Receiver section	
Input		Output		Input	Output
$\overline{OC}$	D	Y	$\overline{Y}$	$\overline{A}$	$\overline{R}$
L	H	H	L	H	H
L	L	L	H	L	L
H	X	Z	Z	Open	H

Note : X : Irrelevant
Z : High impedance

APPLICATION

High-speed Photocoupler Interface

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim +V_{CC}$	V
V_O	Output voltage	When output is "H" or high impedance	$-0.5 \sim +5.5$	V
Tstg	Storage temperature		$-65 \sim +150$	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75$℃ unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Nom	Max	
V_{CC}	Supply voltage			4.75	5.0	5.25	V
I_{OH}	"H" output current	Driver	$V_{OH} \geq 2.5V$			−20	mA
		Receiver	$V_{OH} \geq 2.7V$			−0.4	
I_{OL}	"L" output current	Driver	$V_{OL} \leq 0.5V$			20	mA
		Receiver	$V_{OL} \leq 0.5V$			8	
Topr	Operating temperature range			−20		+75	℃

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃ unless otherwise noted)

Driver Section

Symbol	Parameter	Test conditions		Limits Min	Limits Typ.*	Limits Max.	Unit
V_{IH}	"H" input voltage			2			V
V_{IL}	"L" input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC}=4.75V, I_{IK}=−18mA				−1.5	V
V_{OH}	"H" output voltage	V_{CC}=4.75V, I_{OH}=−20mA		2.5	3.1		V
V_{OL}	"L" output voltage	V_{CC}=4.75V, I_{OL}=20mA			0.3	0.5	V
I_{OZL}	"L" output current when off	V_{CC}=5.25V, V_O=0.5V				−20	μA
I_{OZH}	"H" output current when off	V_{CC}=5.25V, V_O=2.5V				20	μA
I_{X+}	Output leak current when power off	V_{CC}=0V	V_O=6V			50	μA
I_{X-}			V_O=−0.25V			−50	μA
I_{IH}	"H" input current	V_{CC}=5.25V, V_I=7V				0.1	mA
		V_{CC}=5.25V, V_I=2.7V				20	μA
I_{IL}	"L" input current	V_{CC}=5.25V, V_I=0.4V			−0.04	−0.36	mA
I_{OS}	Output short current	V_{CC}=5.25V		−30		−150	mA

Receiver Section

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ *	Limits Max.	Unit
V_{T+}	Positive-direction threshold voltage	V_{CC}=5V		1.4	1.6	1.9	V
V_{T-}	Negative-direction threshold voltage	V_{CC}=5V		0.5	0.8	1	V
$V_{T+}-V_{T-}$	Hysterisis width	V_{CC}=5V		0.4	0.8		V
V_{OH}	"H" output voltage	V_{CC}=4.75V, V_I=1.9V I_{OH}=−400μA		2.7	3.5		V
V_{OL}	"L" output voltage	V_{CC}=4.75V	I_{OL}=4mA			0.4	V
		V_I=0.5V	I_{OL}=8mA		0.37	0.5	
I_{IH}	"H" input current	V_{CC}=5.25V, V_I=2.7V			−0.24	−0.36	mA
I_{IL}	"L" input current	V_{CC}=5.25V, V_I=0.4V			−0.7	−1.2	mA
I_{OS}	Output short current	V_{CC}=5.25V, V_O=0V		−20		−100	mA

Power Supply

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ *	Limits Max.	Unit
I_{CC}	Supply current	V_{CC}=5.25V, other inputs are 0V		23	32	mA

* : All typical values are at V_{CC}=5V and T_a=25℃.

SWITCHING CHARACTERISTICS (V_{CC}=5V and T_a=25℃)

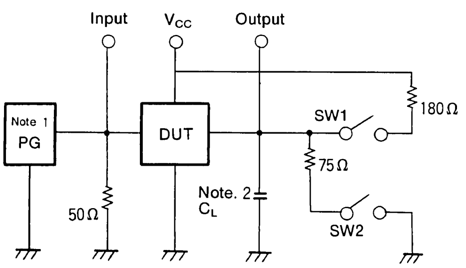
Driver Section

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
t_{PLH}	Outputs "L—H", "H—L"	C_L=30pF		11	20	ns
t_{PHL}	propagation time			11	20	ns
SKew	From input D to outputs Y, $\overline{Y}$				6	ns
t_{PZH}	"H" output enable time	C_L=30pF, R_L=75Ω		9	40	ns
t_{PZL}	"L" output enable time	C_L=30pF, R_L=180Ω		17	45	ns
t_{PHZ}	"H" output disable time	C_L=10pF, R_L=75Ω		6	30	ns
t_{PLZ}	"L" output disable time	C_L=10pF, R_L=180Ω		7	35	ns

Receiver Section

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Outputs "L—H", "H—L"	C_L=15pF		19	30	ns
t_{PHL}	propagation time			15	30	ns

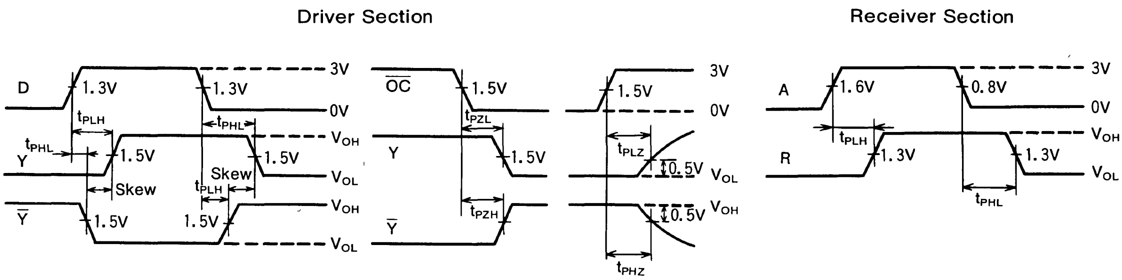
TEST CIRCUIT



Parameter	SW1	SW2
t_{PLH}	Open	Open
t_{PHL}	Open	Open
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Open	Closed
t_{PLZ}	Closed	Open

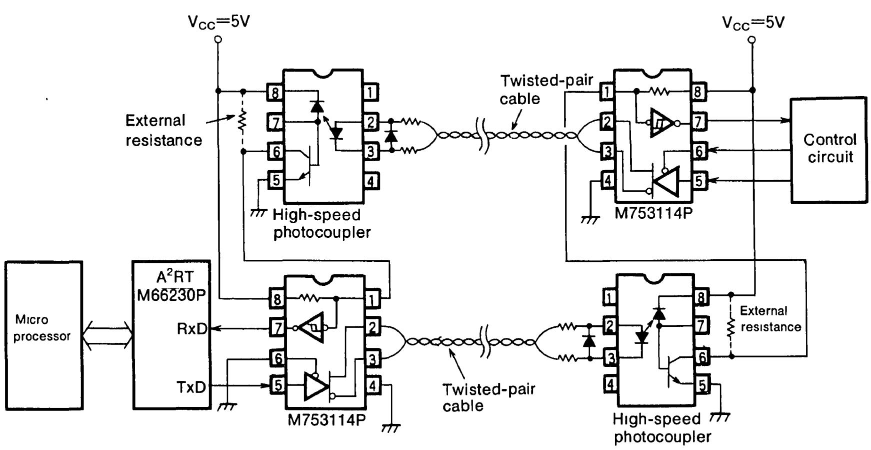
Note 1 : PG (pulse generator) output conditions are as follows.
$t_r \leqq$ 15ns
$t_f \leqq$ 6 ns
PRR= 1 MHz
V_P= 3 V_{P-P}
2 : C_L includes the stray capacitance and jig capacitance.

TIMING DIAGRAM



Voltage waveforms

APPLICATION EXAMPLE (High-speed Serial Data Transmission System)



MITSUBISHI ELECTRIC

CROSSPOINT SWITCH

6

M402100BP/BFP

4×4 CROSSPOINT SWITCH WITH CONTROL MEMORY

DESCRIPTION

The M402100BP/BFP is a semiconductor integrated circuit consisting of a 4×4 crosspoint switch capable of selecting 16 analog switches in a 4×4 array with 4 address inputs as well as 2 types of control signals.

FEATURES

- Internal 16-bit latch circuit
- Has power on/reset function
- Low on-state resistance 60Ω typical (V_{DD}=15V)
- High off-state resistance more than 10^9Ω typical
- Good linearity transfer characteristics distortion 0.07% typical (R_L=1kΩ, V_{DD}=5V, V_{SS}=−5V)

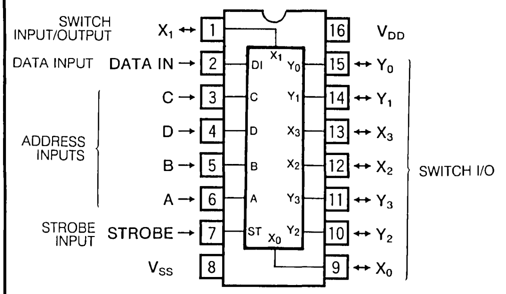
APPLICATION

Line switching of telephone and communications equipments.

FUNCTIONAL DESCRIPTION

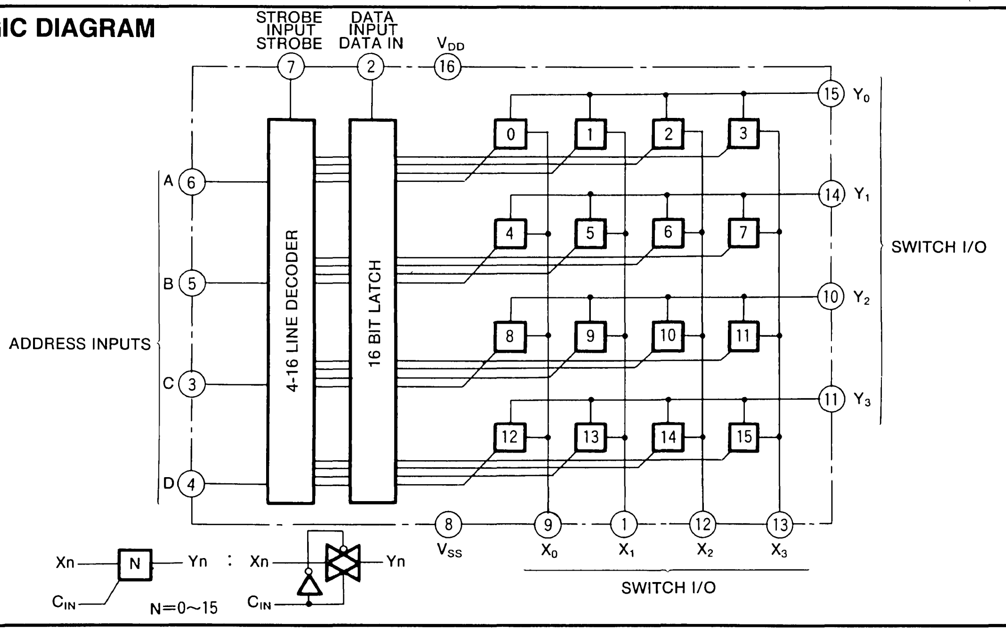
The input address signals (A, B, C, D) are four-bit binary coded. When the strobe input is high-state the switch that corresponds to the value of the input address signals is selected. If, at this time, the data-in signal becomes high-state, the switch is turned on and for the duration of the input/output period remains in low-impedance state. If the data-in signal becomes low-state then the switch is turned off and for the duration of the input/output period remains in high-impedance state. When the strobe becomes low-state, the switch condition that existed immediately prior to the strobe signal is maintained. As there is an internal power on/reset function, all switches can be set to the off-state when the power is applied.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N

LOGIC DIAGRAM



FUNCTION TABLE

Strobe input	Address input				Data input	Selection channels															
						Y_0				Y_1				Y_2				Y_3			
ST	D	C	B	A	DI	X_0	X_1	X_2	X_3	X_0	X_1	X_2	X_3	X_0	X_1	X_2	X_3	X_0	X_1	X_2	X_3
L	X	X	X	X	X	←							NC								→
H	L	L	L	L	L	OFF	←						NC								→
H	L	L	L	L	H	ON	←						NC								→
H	L	L	L	H	L	NC	OFF	←					NC								→
H	L	L	L	H	H	NC	ON	←					NC								→
H	L	L	H	L	L	NC	NC	OFF	←				NC								→
H	L	L	H	L	H	NC	NC	ON	←				NC								→
H	L	L	H	H	L	←	NC	→	OFF	←			NC								→
H	L	L	H	H	H	←	NC	→	ON	←			NC								→
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	L	←							NC							→	OFF
H	H	H	H	H	H	←							NC							→	ON

Note 1 : X : Either high-or low-state
ON : Low impedance during Xn-Yn(n : 0~3)
OFF : High impedance during Xn-Yn(n : 0~3)
NC : No change, maintanins prior condition
←NC→ : While ↔ all are NC

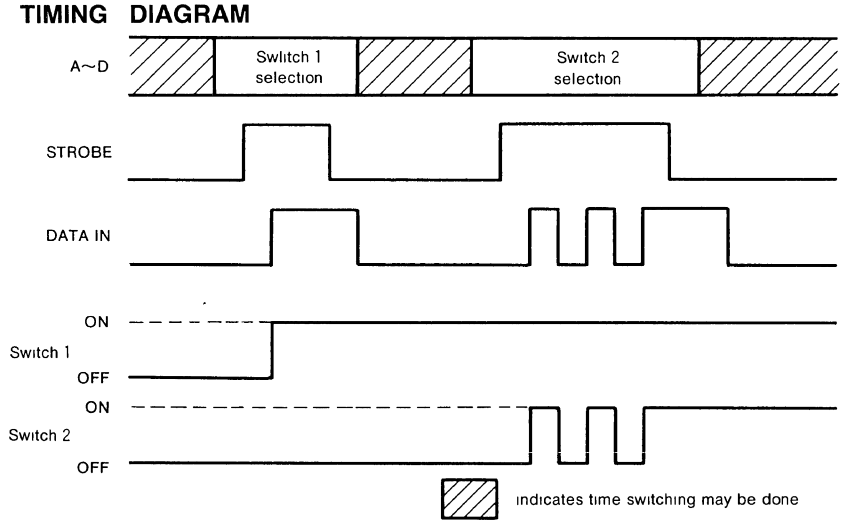
POWER ON/RESET FUNCTION

The M402100BP/BFP has an internal power on/reset function that turns all switches off. This function was made possible by internally fabricated capacity. When the power on/reset function is used it is nesessary that power supply rise-time satisfy the specifications given in Table 1 (see application example). If, while some switch is in the on-state, the supply voltage should be turned off, the power on/reset function can be avoided by reapplying the supply voltage within approximately 10 seconds. In such a case set all switches to off prior to turning the supply voltage off.
When using the power on/reset function, give careful consideration as to whether or not the supply voltage should be used to activate this function.

Table 1 SUPPLY VOLTAGE RISE-TIME REQUIREMENT

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
$t_r(V_{DD})$	Supply voltage rise-time	Data in=low-state		25	ms/V

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		$V_{SS}-0.5 \sim V_{SS}+20$	V
V_I	Input voltage		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
$V_{I/O}$	On-state voltage difference between input and output		±0.5	V
V_O	Output voltage		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
I_I	Input current	A~D, STROBE, DATA IN	±10	mA
I_O	Output current	Switch off	±10	mA
Topr	Operating temperature range		−40~+85	℃
Tstg	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit
V_{DD}	Supply voltage	3		18	V
V_I	Input voltage	V_{SS}		V_{DD}	V
V_O	Output voltage	V_{SS}		V_{DD}	V

ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

Symbol	Parameter	Test conditions	V_{DD}(V)	−40℃ Min	−40℃ Max	25℃ Min	25℃ Typ	25℃ Max	85℃ Min	85℃ Max	Unit
V_{IH}	High-level input voltage (A~D, STROBE, DATA IN)	Switch on $R_{ON} < R_{ON\ MAX}$	5	3.5		3.5			3.5		V
			10	7.0		7.0			7.0		
			15	11.0		11.0			11.0		
V_{IL}	Low-level input voltage (A~D, STROBE, DATA IN)	Switch off $I_L < 0.2\mu A$	5		1.5			1.5		1.5	V
			10		3.0			3.0		3.0	
			15		4.0			4.0		4.0	
R_{ON}	On resistance Measurement circuit 1	$V_I = \frac{V_{DD}-V_{SS}}{2}$	5		520			650		820	Ω
			10		125			150		185	
			12		105			125		160	
			15		95			115		145	
ΔR_{ON}	On resistance difference (between switches of the 16 switches)	$V_I = \frac{V_{DD}-V_{SS}}{2}$	5				35				Ω
			10				20				
			12				18				
			15				15				
I_{OFF}	Input-to-output off-state leakage current	All switches off	18		±300			±300		±1000	nA
I_{DD}	Quiescent supply current	$V_I = V_{DD}, V_{SS}$	5		5			5		150	μA
			10		10			10		300	
			15		20			20		600	
I_{IH}	High-level input current (A~D, ST, DI)	$V_{IH} = 18V$	18		0.3			0.3		1.0	μA
I_{IL}	Low-level input current (A~D, ST, DI)	$V_{IL} = 0V$	18		−0.3			−0.3		−1.0	μA

SWITCHING CHARACTERISTICS ($T_a = 25°C$)

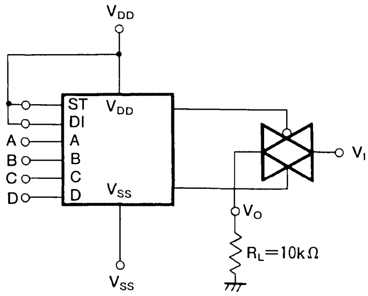
Symbol	Parameter	Test conditions	V_{SS}(V)	V_{DD}(V)	Limits Min	Limits Typ	Limits Max	Unit
f_{max}(I/O)	Maximum transfer frequency	R_L=1kΩ Measurement circuit 2	−5	5		50		MHz
f_{max}(C_{IN})	Maximum control frequency	R_L=1kΩ C_L=50pF Measurement circuit 3	0 0 0	5 10 15	0.6 1.6 2.5			MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Xn/Yn−Yn/Xn)	R_L=10kΩ C_L=50pF Measurement circuit 4	0 0 0	5 10 15			60 30 20	ns
t_{PHL}			0 0 0	5 10 15			60 30 20	ns
t_{PHZ}	Output disable time from high-level (STROBE−Yn/Xn)	R_L=1kΩ C_L=50pF Measurement circuit 5	0 0 0	5 10 15			330 170 140	ns
t_{PZH}	Output enable time to high-level (STROBE−Yn/Xn)		0 0 0	5 10 15			600 250 160	ns
t_{PZH}	Output enable time to high-level and low-level (DATA IN−Yn/Xn)	R_L=1kΩ C_L=50pF Measurement circuit 6	0 0 0	5 10 15			420 220 150	ns
t_{PZL}			0 0 0	5 10 15			420 220 150	ns
t_{PHZ}	Output disable time from high-level (A∼D−Yn/Xn)	R_L=1kΩ C_L=50pF Measurement circuit 7	0 0 0	5 10 15			870 420 320	ns
t_{PZH}	Output enable time to high-level (A∼D−Yn/Xn)		0 0 0	5 10 15			700 270 180	ns
−	Sinewave distortion	R_L=1kΩ f_i=1kHz Measurement circuit 2	−5	5		0.07		%
−	Feedthrough (switch off)	R_L=1kΩ Measurement circuit 8	−5	5		−100		dB
−	Crosstalk	R_L=10kΩ Measurement circuit 9	0	10		150		mV
−	Crosstalk frequency	R_L=1kΩ, SW(A)=On, SW(B)=Off, Measurement circuit 10; $20\log\frac{V_O(B)}{V_I(A)}=-40dB$	−5	5		1.5		MHz
		$20\log\frac{V_O(B)}{V_I(A)}=-110dB$	−5	5		0.1		kHz
C_I	Input capacitance	A∼D, STROBE, DATA IN					7.5	pF
		Signal input Xn				40		pF
		Signal input Yn				40		pF
$C_{Xn/Yn}$	Input/output capacitance					0.4		pF

TIMING REQUIREMENTS ($T_a = 25°C$, $V_{SS} = 0V$)

Symbol	Parameter	Test conditions	V_{DD}(V)	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(ST)}$	Strobe pulse width		5 10 15	600 240 190			ns
t_{SU}	Data setup time respect to A∼D, strobe		5 10 15	190 50 30			ns
t_h	Data hold time respect to A∼D, strobe		5 10 15	360 220 120			ns

MEASUREMENT CIRCUIT (Capacitance C_L includes stray probe and wiring capacitance)

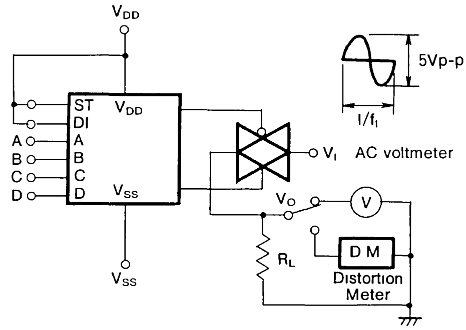
1 On-state resistance (R_{ON})



$$R_{ON}=10\times\frac{(V_I-V_O)}{V_O}\,[\mathrm{k}\Omega]$$

See function table for condition of address inputs A through D

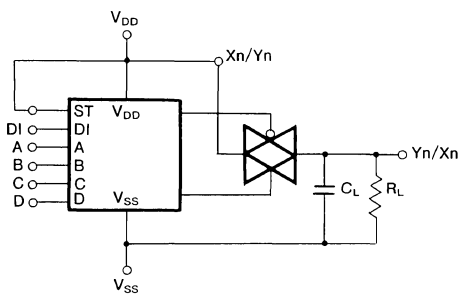
2 Maximum transfer frequency (f_{max}(I/O)) Sinewave distortion



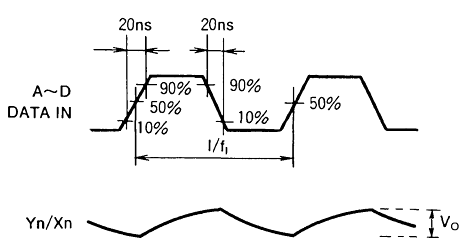
With an input sinewave of ±2.5$V_{P\text{-}P}$, f_{max}(I/O) is equal to frequency (f_I) when $20\log_{10}\frac{V_O}{V_I}=-3\mathrm{dB}$

See function table for condition of address inputs A through D

3 Maximum control frequency (f_{max}(C_{IN}))



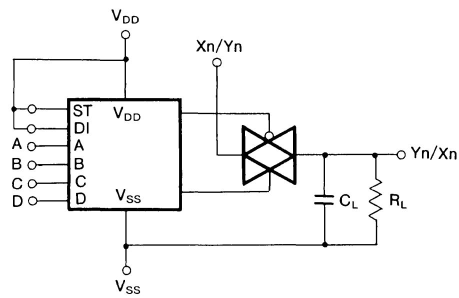
Timing diagram



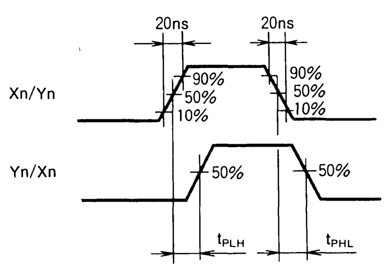
f_{max} (C_{IN}) is the value of f_I when output amplitude has become half value of its original value at the time the input frequency f_I=1kHz

See function table for condition of address inputs A through D.

4 Low-level to high-level and high-level to low-level output propagation time

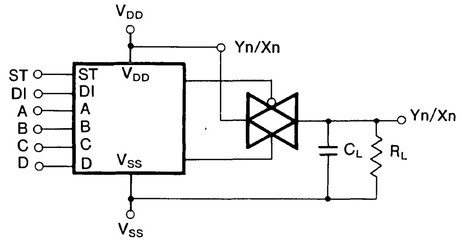


Timing diagram

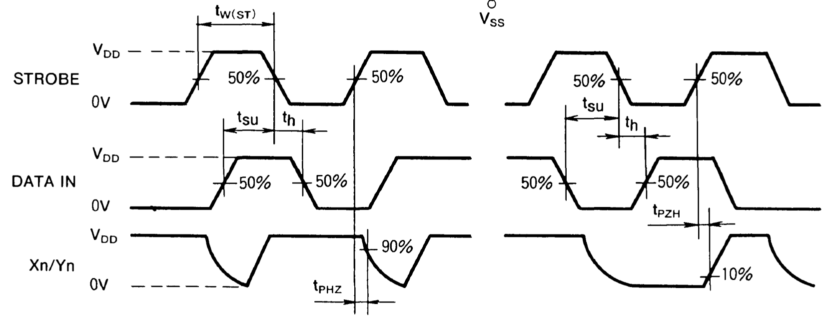


See function table for condition of address inputs A through D

5 Output disable/enable time from/to high-level (STROBE—Yn/Xn)

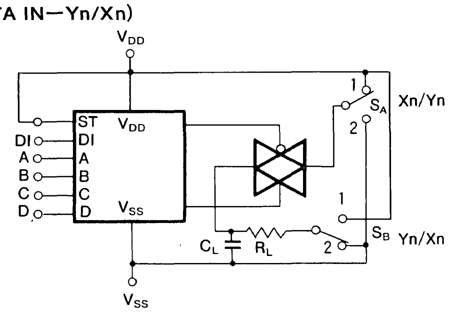


Timing diagram

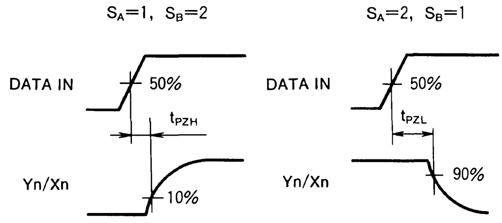


See function table for condition of address inputs A through D

6 Output enable time to high-level and low-level (DATA IN—Yn/Xn)

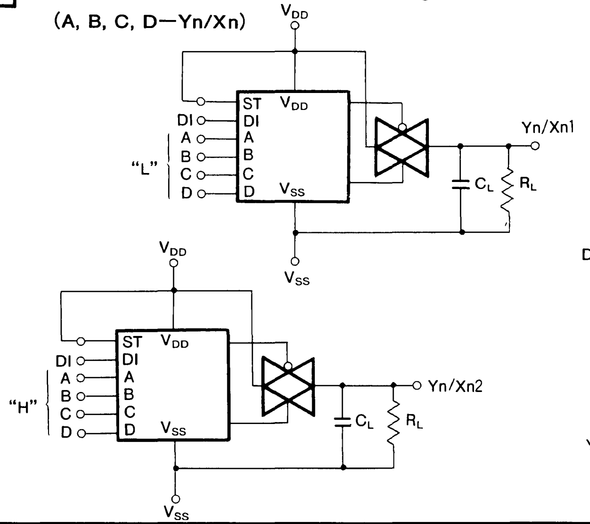


Timing diagram

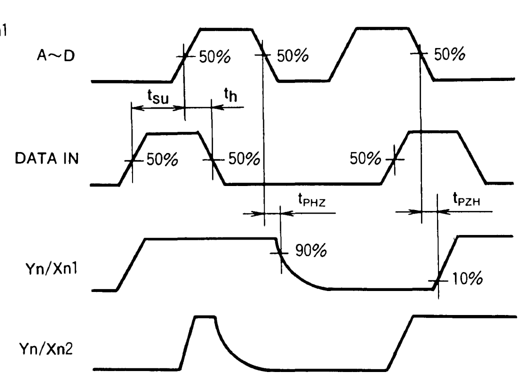


See function table for condition of address inputs A through D.

7 Output disable/enable time from/to high-level (A, B, C, D—Yn/Xn)



Timing diagram



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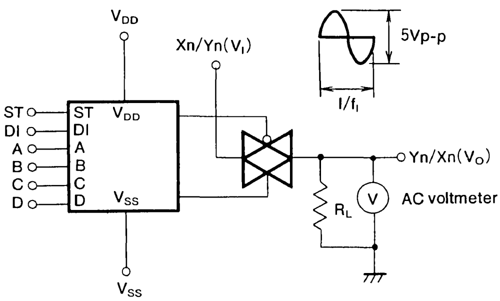
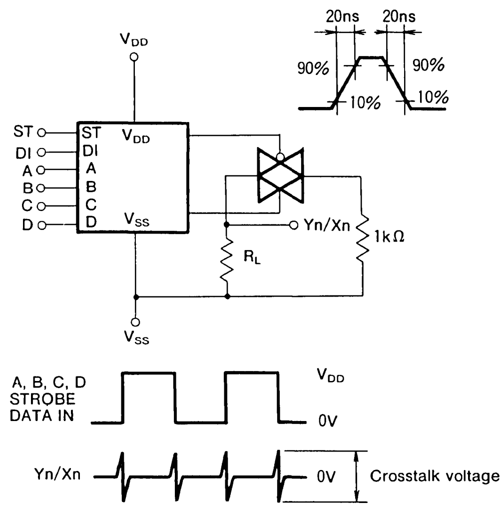
8 Feedthrough



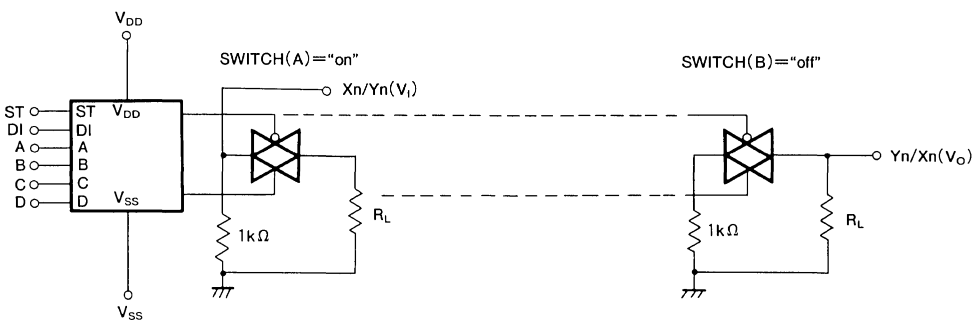
Using a ±2 5V_{P-P} sinewave input, feed through is 20 $\log_{10}\frac{V_O}{V_I}$ when f_I=1 6kHz

See function table for condition of address inputs A through D, strobe and DATA IN.

9 Crosstalk



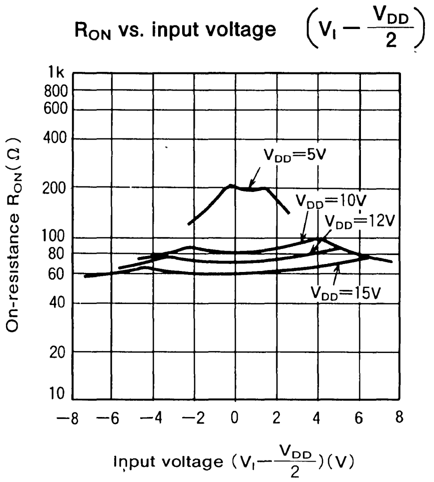
10 Crosstalk frequency

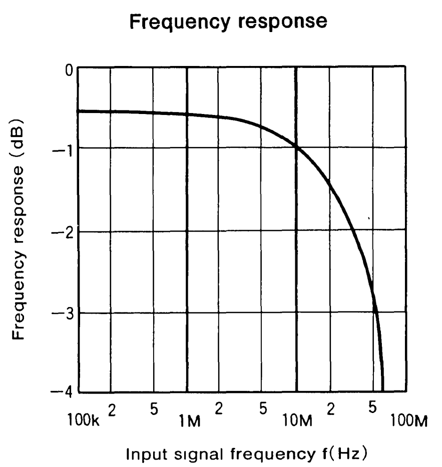


Using a ±2.5V_{P-P} sinewave input, crosstalk frequency is the frequency at −110dB and when 20 $\log_{10}\frac{V_O}{V_I}$=−40dB.

See function table for condition of address inputs A through D, strobe and data in

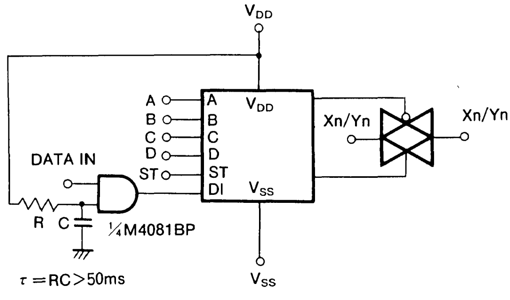
TYPICAL CHARACTERISTICS





TYPICAL APPLICATION

Power on/reset usage



MITSUBISHI ELECTRIC

M402101BP/BWP

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

DESCRIPTION

The M402101BP/BWP is a semiconductor integrated circuit consisting of a 4×8 cross point switch capable of selecting 32 analog switches with 5 address inputs as well as 2 types of control signals.

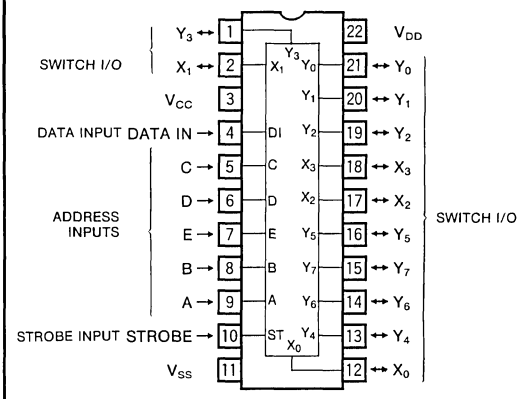
FEATURES

- Internal control latch circuit
- Internal level- shifter circuit
- Good crosstalk characteristics −100dB (@f=3kHz)
- Low on-state resistance 60Ω typical (@V_{DD}=15V)
- High off-state resistance more than 10^9Ω typ.
- Excellent transfer linearity Distortion 0.05% typ. (@R_L=1kΩ, V_{DD}=5V, V_{SS}=−5V)
- 5V control logic

APPLICATION

Line switching of telephone and communication equipments.

PIN CONFIGURATION (TOP VIEW)

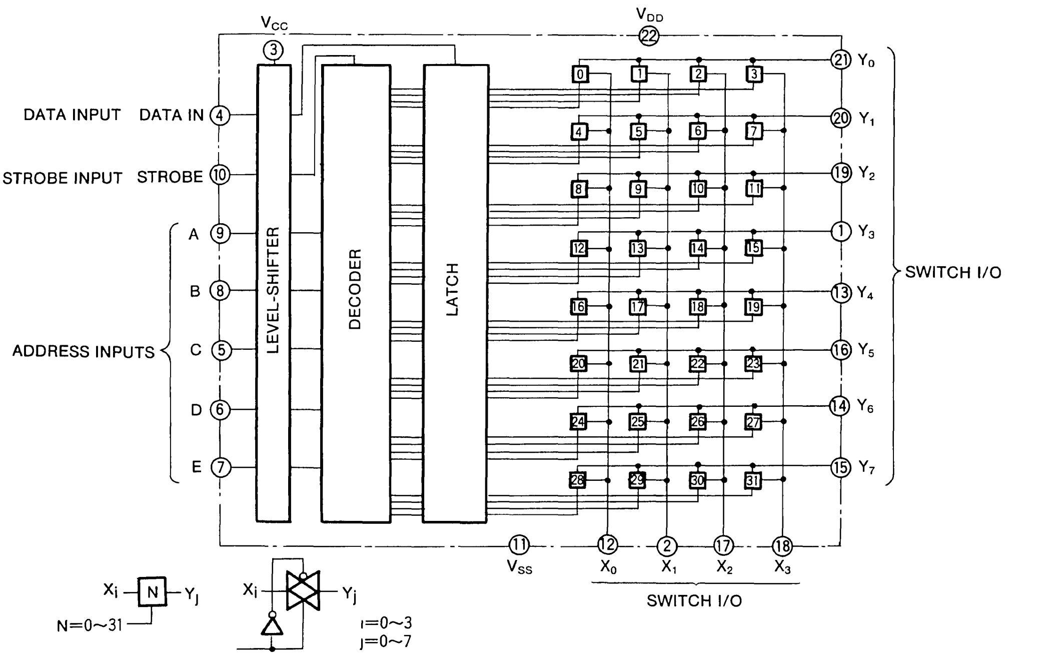


Outline 22P4H (BP)
22P4 (BWP)

FUNCTIONAL DESCRIPTION

The input address signals (A, B, C, D, E) are five-bit binary coded. When the STROBE input is high, the switch that corresponds to the value of the input address signals is selected. If, at this time, the DATA IN input is high, the switch is turned on and until DATA IN is pulled low. If the DATA IN is low, the switch is turned off and becomes in high-impedance state. When the STROBE becomes low, any of the switch conditions are not changed. The internal level-shifter makes possible to handle $15V_{p-p}$ analog signals by 5V control logic signals.

LOGIC DIAGRAM

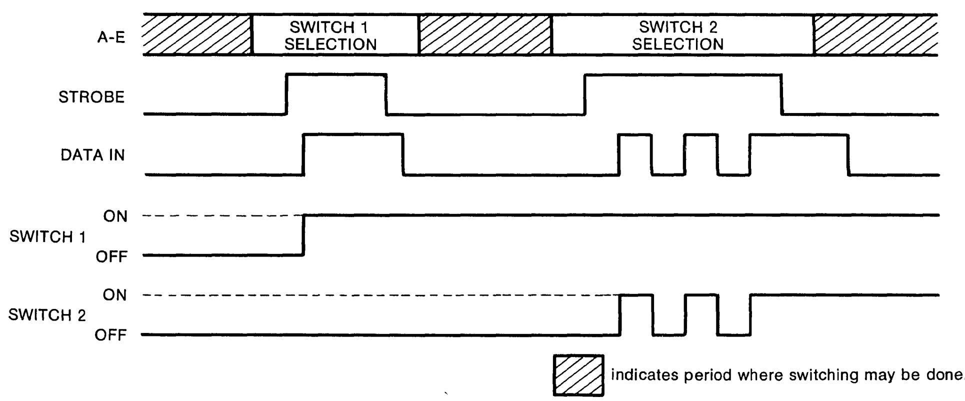


FUNCTION TABLE (Note : 1)

			0		1		2		3		4		5		6		7		8		…	30		31	
Control input	A	X	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	…	L	L	H	H
Control input	B	X	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	…	H	H	H	H
Control input	C	X	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	…	H	H	H	H
Control input	D	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	…	H	H	H	H
Control input	E	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	…	H	H	H	H
	STROBE	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	…	H	H	H	H
	DATA IN	X	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	…	L	H	L	H
0	X0Y0	NC	OFF	ON ←																					NC
1	X1Y0	NC →			OFF	ON ←																			NC
2	X2Y0	NC →					OFF	ON ←																	NC
3	X3Y0	NC →							OFF	ON ←															NC
4	X0Y1	NC →									OFF	ON ←													NC
5	X1Y1	NC →											OFF	ON ←											NC
6	X2Y1	NC →													OFF	ON ←									NC
7	X3Y1	NC →															OFF	ON ←							NC
8	X0Y2	NC →																	OFF	ON ←					NC
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
30	X2Y7	NC →																				OFF	ON ←		NC
31	X3Y7	NC →																						OFF	ON

Note 1 : X : Irrelevant
ON : Low impedance between X_i-Y_j ($i=0\sim3$, $j=0\sim7$)
OFF : High impedance between X_i-Y_j ($i=0\sim3$, $j=0\sim7$)
NC : No change and previous state is maintained.

OPERATING TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage 1		−0.5∼20	V
V_{CC}	Supply voltage 2		−0.5∼20	V
$V_{DD}-V_{CC}$	Supply voltage 1−supply voltage 2		−0.5∼20	V
V_I	Input voltage	A∼E, STROBE, DATA IN	V_{SS}−0.5∼V_{DD}+0.5	V
V_I	Input voltage	X_0∼X_3, Y_0∼Y_7	V_{SS}−0.5∼V_{DD}+0.5	V
$V_{I/O}$	On-state voltage diffrence between input and output	X_0∼X_3, Y_0∼Y_7	+0.5	V
V_O	Output voltage	X_0∼X_3, Y_0∼Y_7	−0.5∼V_{CC}+0.5	V
I_I	Input current	A∼E, STROBE, DATA IN	±10	mA
I_O	Output current	Switch off	±10	mA
Tstg	Storage temperature		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage 1	V_{CC}	15	18	V
V_{CC}	Supply voltage 2	4.5	5	5.5	V
V_I	Input voltage (A∼E, STROBE, DATA IN)	V_{SS}		V_{CC}	V
V_I	Input voltage (X_0∼X_3, Y_0∼Y_7)	V_{SS}		V_{DD}	V
V_O	Output voltage (X_0∼X_3, Y_0∼Y_7)	V_{SS}		V_{DD}	V
T_{opr}	Operating free air temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{DD}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage (A∼E, STROBE, DATA IN)	Switch on R_{ON}<$R_{ON\ MAX}$ Switch off I_L<0.2μA V_{CC}=5V	5	4.0			4.0		V
			10	3.5			3.5		
			15	3.5			3.5		
V_{IL}	Low-level input voltage (A∼E, STROBE, DATA IN)		5			1.5		1.5	V
			10			1.5		1.5	
			15			1.5		1.5	
R_{ON}	On-resistance (Test circuit 1)	$V_I=\frac{V_{DD}-V_{SS}}{2}$	5		170	650		820	Ω
			10		75	150		185	
			15		60	100		130	
ΔR_{ON}	On-resistance difference (between 2 switches of the 32 switches)	$V_I=\frac{V_{DD}-V_{SS}}{2}$	5		16				Ω
			10		17				
			15		17				
I_O	Output off-leak current	Switch off	±0.3			±0.3		±1.0	μA
I_{DD}	Quiescent supply current (per package)	V_I=V_{DD}, V_{SS}	5			10		150	μA
			10			20		300	
			15			40		600	
		V_I=3.5, 1.5V(Note 2)	15		2.2				
I_{IH}	High-level input current (A∼E, ST, DI)	V_{CC}=6V V_{IH}=6V	18			0.3		1.0	μA
I_{IL}	High-level input voltage (A∼E, ST, DI)	V_{CC}=6V V_{IL}=0V	18			−0.3		−1.0	μA

Note 2 : Only one input is set to this value and all other inputs are tied to V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions			Limits			Unit
			V_{SS}(V)	V_{DD}(V)	Min	Typ	Max	
f_{max}(I/O)	Maximum frequency	R_L=1kΩ Test circuit 2	−5	5		50		MHz
f_{max}	Maximum control frequency	R_L=1kΩ C_L=50pF Test circuit 3	0	5	0.6	5		MHz
			0	10	1.6	10		
			0	15	2.5	11		
t_{PLH}	Low- to high-level and high- to low-level output propagation time (Xn/Yn−Yn/Xn)	R_L=10kΩ C_L=50pF Test circuit 4	0	5		15	60	ns
			0	10		7	30	
			0	15		6	20	
t_{PHL}			0	5		10	60	ns
			0	10		6	30	
			0	15		5	20	
t_{PHZ}	High-level output disable time (STROBE−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 5	0	5		200	530	ns
			0	10		115	370	
			0	15		100	340	
t_{PZH}	High-level output enable time (STROBE−Yn/Xn)		0	5		180	800	ns
			0	10		95	450	
			0	15		80	360	
t_{PZH}	High-level, low-level output enable time (DATA IN−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 6	0	5		125	620	ns
			0	10		80	440	
			0	15		70	400	
t_{PZL}			0	5		130	620	ns
			0	10		80	440	
			0	15		70	400	
t_{PHZ}	High-level output disable time (A∼E−Yn/Xn)	R_L=1kΩ C_L=50pF Test circuit 7	0	5		140	1070	ns
			0	10		80	720	
			0	15		75	520	
t_{PZH}	High-level output enable time (A∼E−Yn/Xn)		0	5		125	900	ns
			0	10		65	470	
			0	15		60	380	
—	Sinewave distortion	R_L=1kΩ f_I=1kHz Test circuit 2	−5	5		0.05		%
—	Feedthrough (switch off)	R_L=1kΩ Test circuit 8	−5	5		−80		dB
—	Crosstalk	R_L=10kΩ Test circuit 9	0	(Note:5) 10		150		mV
—	Crosstalk frequency	R_L=1kΩ (Note:3) SW(A)=on, SW(B)=off	−5	5		1.5		MHz
		Test circuit 10 (Note:4)	−5	5		0.1		kHz
C_I	Input capacitance	A∼E, STROBE, DATA IN, RESET				5	7.5	pF
		Signal input	Xn			75		pF
			Yn			48		
$C_{Xn/Yn}$	Input/output capacitance					0.6		pF

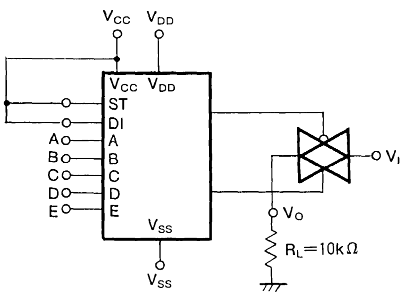
Note 3: $20 \cdot \log\frac{V_O(B)}{V_I(A)}=-40\text{dB}$, Note 4: $20 \cdot \log\frac{V_O(B)}{V_I(A)}=-110\text{dB}$, Note 5: V_{CC}=10V

TIMING REQUIREMENT (V_{CC}=5V, V_{SS}=0V)

Symbol	Parameter	Test conditions		Limits			Unit
			V_{DD}(V)	Min	Typ	Max	
$t_{W(ST)}$	Strobe pulse width		5	600	135		ns
			10	240	60		
			15	190	45		
t_{SU}	Data setup time before A∼E, STROBE		5	280	70		ns
			10	140	35		
			15	120	25		
t_h	Data hold time after A∼E, STROBE		5	420	60		ns
			10	280	35		
			15	180	25		

4×8 CROSSPOINT SWITCH WITH CONTROL MEMORY

1 On-state resistance (R_{ON})

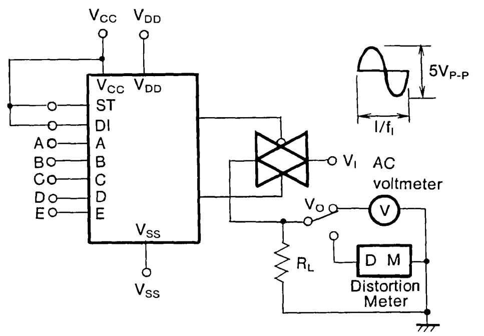


$$R_{ON}=10\times\frac{(V_I-V_O)}{V_O}\ [k\Omega]$$

* Only one switch is on

See function table for conditions of address inputs A through E

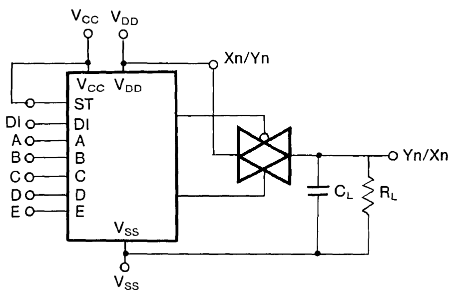
2 Maximum frequency (f_{max}(I/O)) sinewave distortion



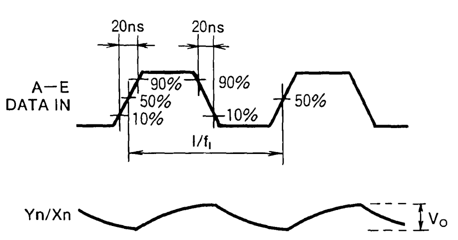
With an input sinewave of $+2.5V_{P\text{-}P}$, f_{max}(I/O) is equal to frequency (f_I) when $20\cdot\log_{10} V_O/V_I=-3dB$.

See function table for conditions of address inputs A through E.

3 Maximum control frequency (f_{max}(C_{IN}))



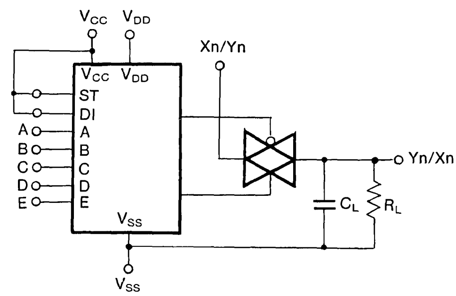
Timing diagram



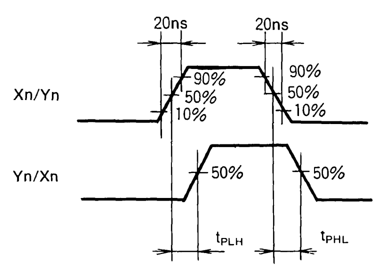
f_{max}(C_{IN}) is the value of f_I when output amplitude reaches half the value of its original value at the time the input frequency f_I = 1kHz

See function table for conditions of address inputs A through E

4 Low- to high-level and high- to low-level output propagation time (Xn/Yn—Yn/Xn)

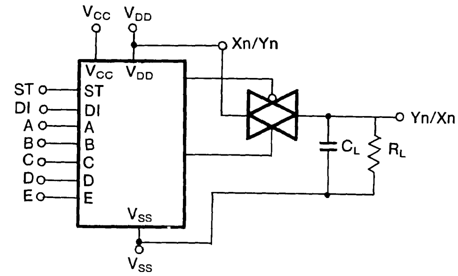


Timing diagram

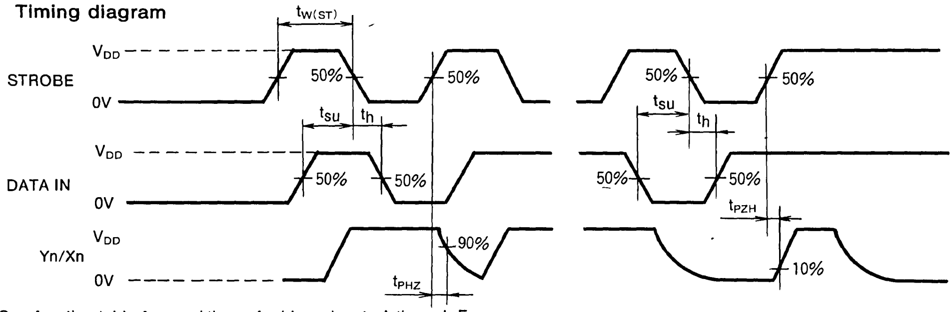


See function table for conditions of address inputs A through E

5 **High-level output disable/enable time (STROBE—Yn/Xn)**

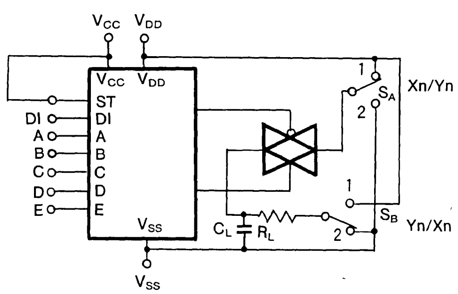


Timing diagram



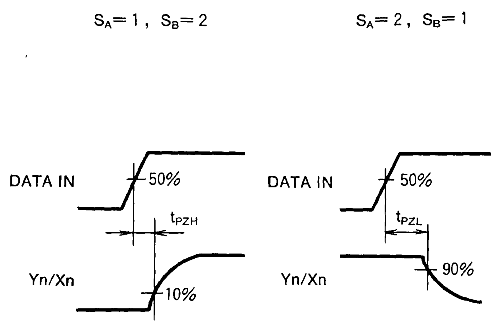
See function table for conditions of address inputs A through E

6 **High-level, low-level enable time (DATA IN—Yn/Xn)**

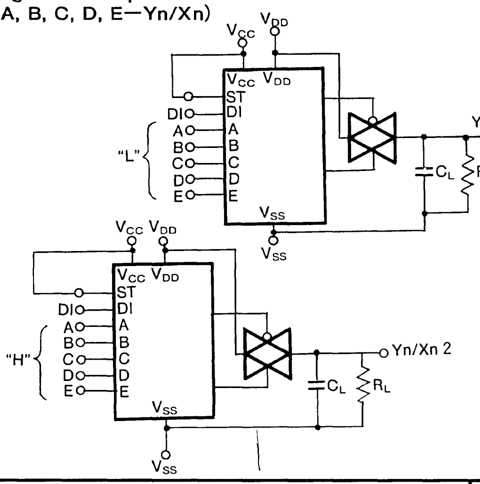


See function table for conditions of address inputs A through E.

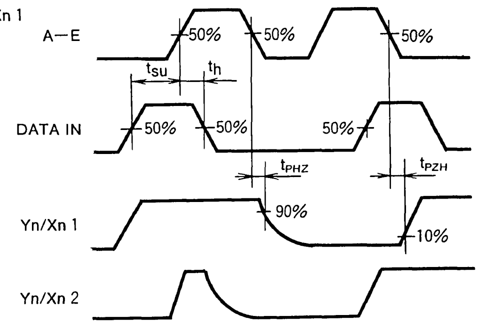
Timing diagram



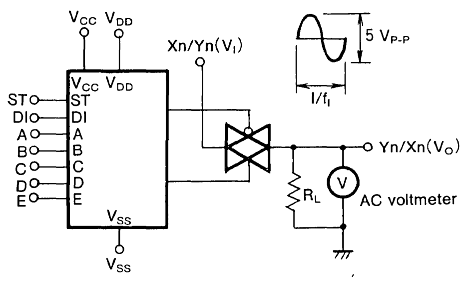
7 High-level output disable/enable time (A, B, C, D, E—Yn/Xn)



Timing diagram

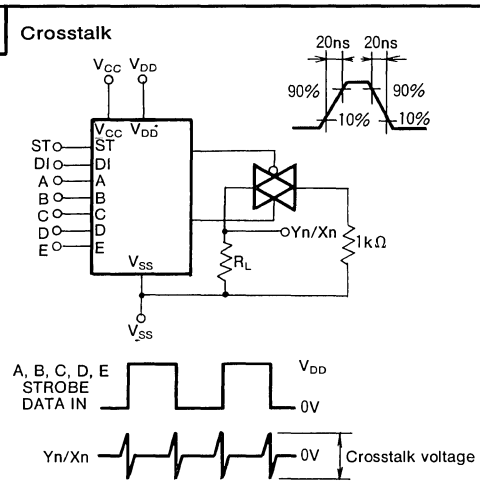


8 Feedthrough

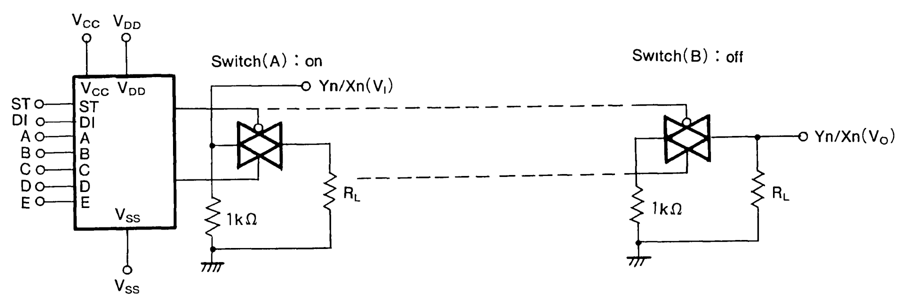


Using a $+2.5V_{P\text{-}P}$ sinewave input, feedthrough is $20 \cdot \log_{10} V_O/V_I$ when $f_I = 1.6$kHz. See function table for conditions of strobe, data-in and address inputs A through E.

9 Crosstalk



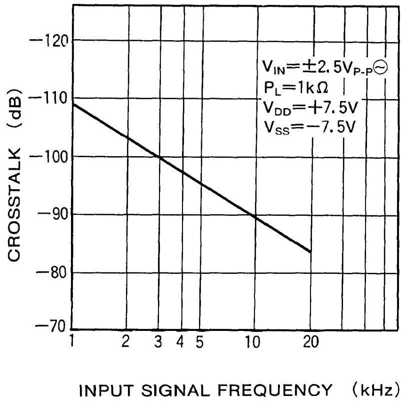
10 Crosstalk frequency



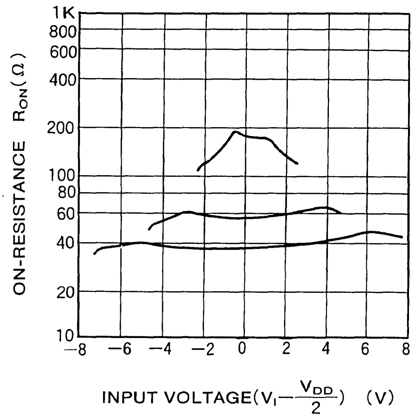
Using a $+2.5V_{P\text{-}P}$ sinewave input, cross talk frequency is to be measured as the frequency where $20 \cdot \log_{10} V_O/V_I$ equals -40dB and -110dB. See function table for conditions of strobe data-in and A through E.

TYPICAL CHARACTERISTICS

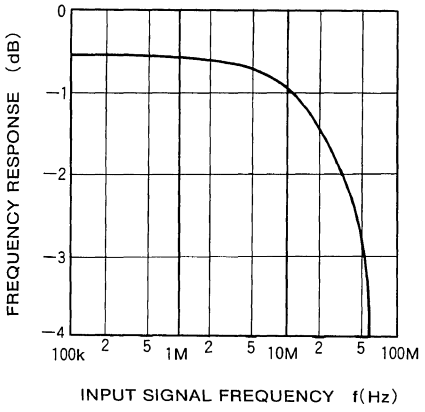
CROSSTALK—INPUT SIGNAL FREQUENCY



R_{ON}—INPUT VOLTAGE ($V_I - \frac{V_{DD}}{2}$)



FREQUENCY RESPONSE



M74HC-1 SERIES

M74HC138-1P/FP

1-OF-8 DECODER/DEMULTIPLEXER

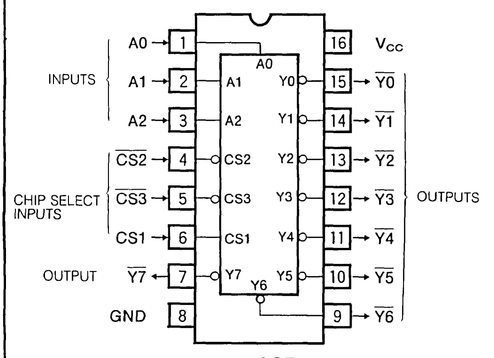
DESCRIPTION

The M74HC138-1 is a semiconductor integrated circuit consisting of a 3-bit binary to 8-line decoder/demultiplexer with chip select inputs.

FEATURES

- High-fanout output:(I_{OL}=24mA, I_{OH}=−24mA)
- Three types of chip select inputs
- Expandable to 24 outputs without externally connected components
- High-speed: 12ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40∼+85℃

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC138-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

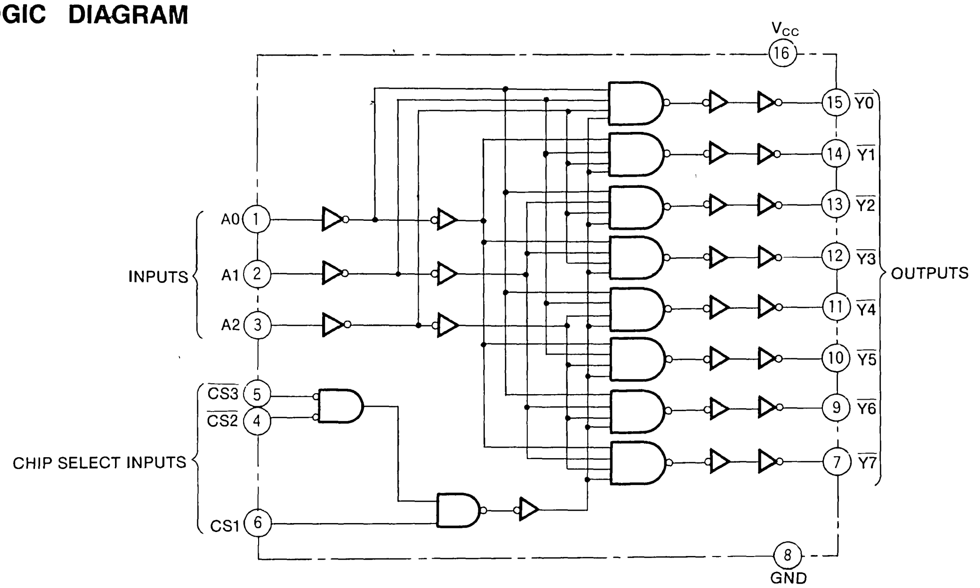
When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$, or $\overline{CS3}$ is used as data input and A0 through A2 input are used as selecting input.

LOGIC DIAGRAM



FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HC138-1FP, $T_a = -40 \sim +70$℃ and $T_a = 70 \sim 85$℃ are derated at -6mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		-40		$+85$	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 2.0V$	0		500	ns/V
		$V_{CC} = 4.5V$	0		50	
		$V_{CC} = 6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$	2.0			0.1		0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1		0.1	
			$I_{OL} = 20\mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I = 6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($V_{CC} = 2\sim6V$, $T_a = -40\sim+85$℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L = 50pF$ (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)		2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
t_{PHL}			2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)		2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
t_{PHL}			2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)		2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
t_{PHL}			2.0			105		150	ns
			4.5			21		30	
			6.0			18		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

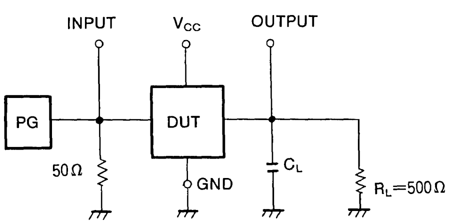
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

1-OF-8 DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

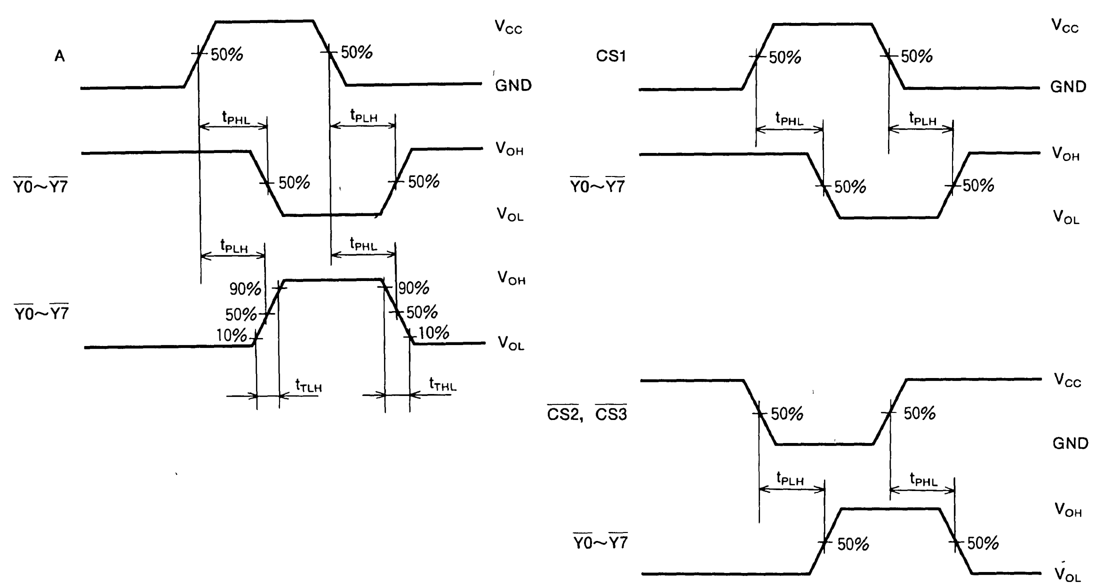
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 4)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (A − $\overline{Y}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (CS1 − $\overline{Y}$)				20	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				20	ns

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT138-1P/FP

1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT138-1 is a semiconductor integrated circuit consisting of a 3-bit binary-to 8-line decoder/demultiplexer with chip select inputs.

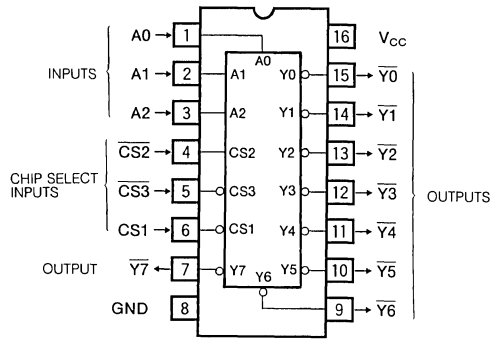
FEATURES

- TTL level input V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout output:(I_{OL}=24mA, I_{OH}=−24mA)
- Three types of chip select inputs
- High-speed: 14ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40～+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT138-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS138.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

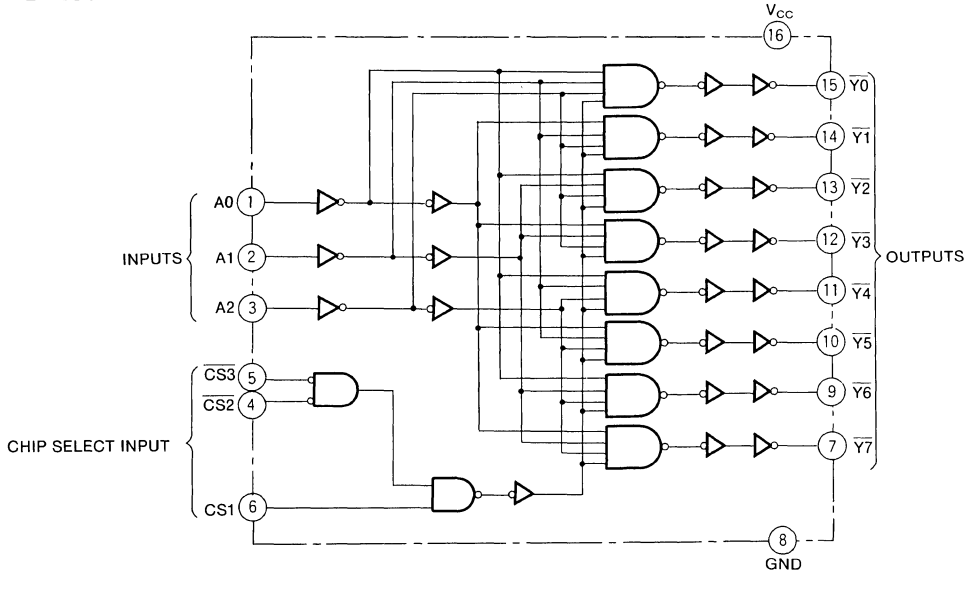
When operated as a decoder, a 3-bit binary code are applied to inputs A0, A1 and A2, one of outputs $\overline{Y0}$ through $\overline{Y7}$ corresponding to this value will become low and the other outputs will all become high.

In this case, chip select input CS1 should be maintained at high while $\overline{CS2}$ and $\overline{CS3}$ should be maintained at low.

When CS1, $\overline{CS2}$ and $\overline{CS3}$ are in conditions other than those given above, all outputs will become high irrespective of A0 through A2.

When operated as a 1-of-8 demultiplexer, CS1, $\overline{CS2}$, or $\overline{CS3}$ is used as data input and A0 through A2 input are used as selecting input.

LOGIC DIAGRAM



1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs					Outputs							
CS1	$\overline{CSX}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{CSX} = \overline{CS2} + \overline{CS3}$
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current, per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HCT138-1FP, $T_a = -40 \sim +70$℃ and $T_a = 70 \sim 85$℃ are derated at −6mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input rise-time, fall-time	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = 5.5V				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V				−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent state supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all others are fixed at V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)				22	ns
t_{PHL}					24	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1 − $\overline{Y}$)				22	ns
t_{PHL}					24	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$ − $\overline{Y}$)				22	ns
t_{PHL}					24	ns

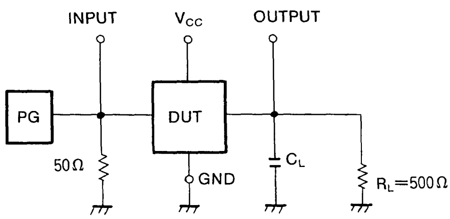
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40∼+85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A−$\overline{Y}$)				23		29	ns
t_{PHL}					25		31	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CS1−$\overline{Y}$)				23		29	ns
t_{PHL}					25		31	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS2}$, $\overline{CS3}$−$\overline{Y}$)				23		29	ns
t_{PHL}					25		31	ns
C_I	Input capacitance				10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)							pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

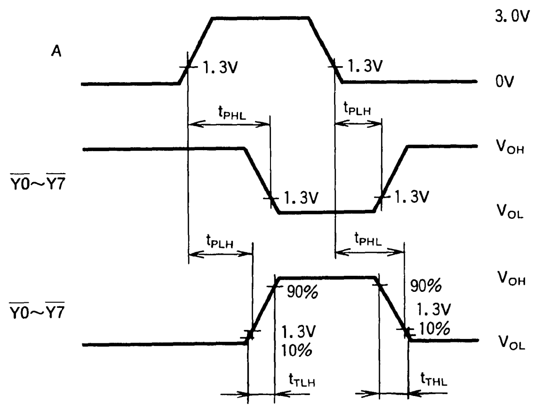
1-OF-8 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

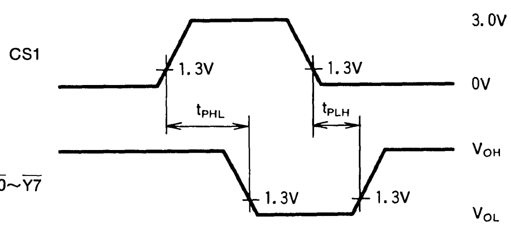
Note 5 : Test Circuit

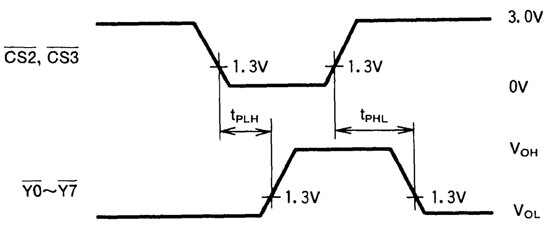


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM







MITSUBISHI ELECTRIC

M74HC139-1P/FP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

DESCRIPTION

The M74HC139-1 is a semiconductor integrated circuit consisting of a 2-bit binary to divide-by-4 decoder/demultiplexer with chip select inputs.

FEATURES

- High-fanout output: (I_{OL}=24mA, I_{OH}=−24mA)
- Chip select inputs
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

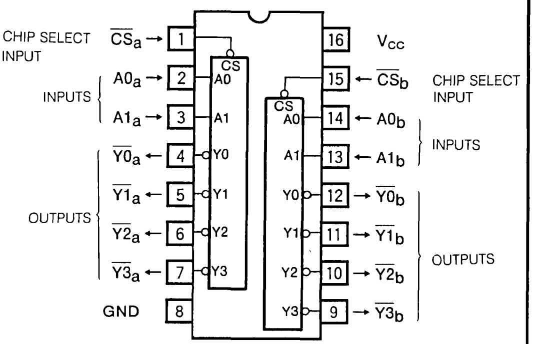
Use of silicon gate technology allows the M74HC139-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS139.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

When operated as a decoder, a 2-bit binary code are applied to inputs A0 and A1, one of outputs $\overline{Y0}$ through $\overline{Y3}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select input $\overline{CS}$ should be maintained at low. When $\overline{CS}$ is high, all outputs will become high irrespective of A0 and A1.

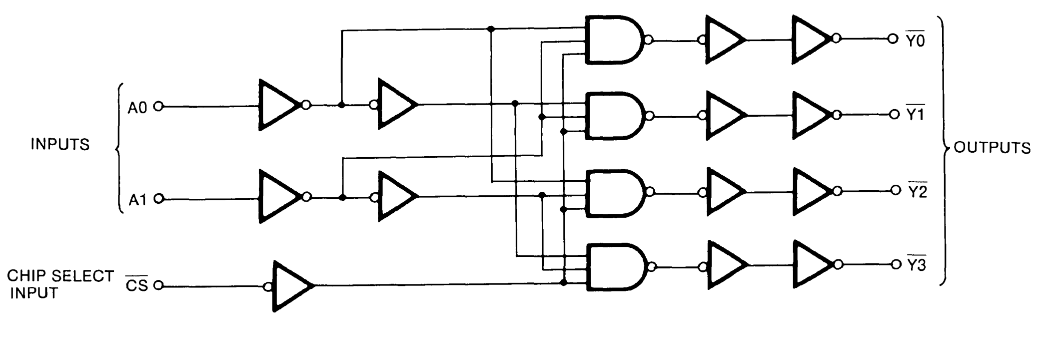
When operated as a 1-of-4 demultiplexer, $\overline{CS}$ is used as a data input and A0 and A1 are used as selecting inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N

LOGIC DIAGRAM (EACH DECODER/DEMULTIPLEXER)



FUNCTION TABLE (Note 1)

Inputs			Outputs			
$\overline{CS}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2 : M74HC139-1FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

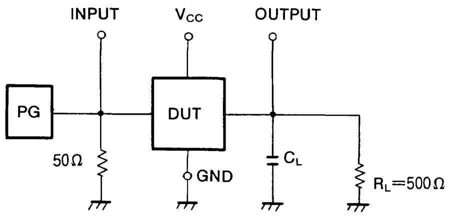
Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)				10	ns
t_{THL}						10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}-\overline{Y}$)					20	ns
t_{PHL}						20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($A-\overline{Y}$)	Number of delay gate stages 4				20	ns
t_{PHL}						20	ns
t_{PLH}		Number of delay gate stages 5				21	ns
t_{PHL}						21	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85°C)

Symbol	Parameter	Test conditions		V_{CC}(V)	25°C Min	25°C Typ	25°C Max	−40~+85°C Min	−40~+85°C Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)		2.0			60		75	ns
				4.5			12		15	
				6.0			10		13	
t_{THL}				2.0			60		75	ns
				4.5			12		15	
				6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}-\overline{Y}$)			2.0			105		130	ns
				4.5			21		26	
				6.0			18		22	
t_{PHL}				2.0			105		130	ns
				4.5			21		26	
				6.0			18		22	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($A-\overline{Y}$)	Number of delay gate stages 4		2.0			105		130	ns
				4.5			21		26	
				6.0			18		22	
t_{PHL}				2.0			105		130	ns
				4.5			21		26	
				6.0			18		22	
t_{PLH}		Number of delay gate stages 5		2.0			110		140	ns
				4.5			22		28	
				6.0			19		24	
t_{PHL}				2.0			110		140	ns
				4.5			22		28	
				6.0			19		24	
C_I	Input capacitance						10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)									pF

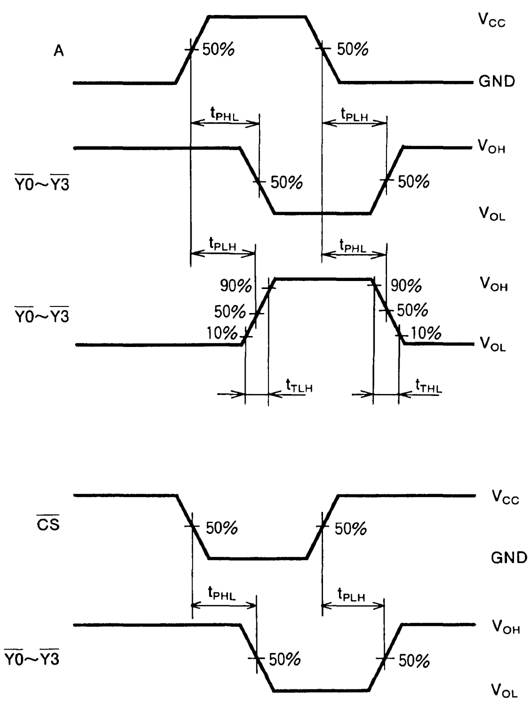
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per decoder)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HCT139-1P/FP

DUAL 1-OF-4 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT139-1 is a semiconductor integrated circuit consisting of a 2-bit binary to divide-by-4 decoder/demultiplexer with chip select inputs.

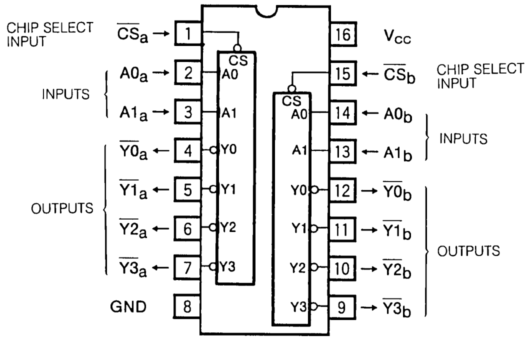
FEATURES

- TTL level inputs V_{IL}=0. 8V max, V_{IH}=2. 0V min
- High-fanout output:(I_{OL}=24mA, I_{OH}=−24mA)
- Chip select inputs
- High-speed: 14ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 16P2N

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT139-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS139.

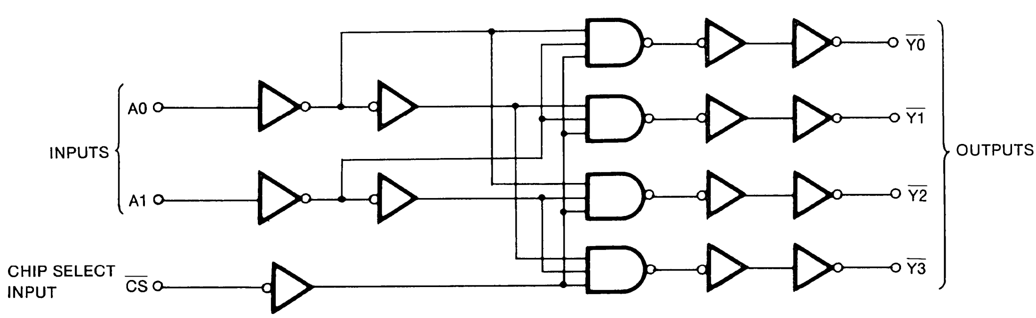
The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

When operated as a decoder, a 2-bit binary code are applied to inputs A0 and A1, one of outputs $\overline{Y0}$ through $\overline{Y3}$ corresponding to this value will become low and the other outputs will all become high. In this case, chip select input $\overline{CS}$ should be maintained at low. When $\overline{CS}$ is high, all outputs will become high irrespective of A0 and A1.

When operated as a 1-of-4 demultiplexer, $\overline{CS}$ is used as a data input and A0 and A1 are used as selecting inputs

LOGIC DIAGRAM (EACH DECODER/DEMULTIPLEXER)



DUAL 1-OF-4 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Outputs			
$\overline{CS}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

Note 1 : X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HCT139-1FP, $T_a = -40 \sim +70$℃ and $T_a = 70 \sim 85$℃ are derated at -6mW/℃.

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		-40		$+85$	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$, $\|I_O\| = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$, $\|I_O\| = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IL}$	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = 5.5V$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$				-0.1		-1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent state supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all others are fixed at V_{CC} or GND

MITSUBISHI ELECTRIC

DUAL 1-OF-4 DECODER/DEMULTIPLEXER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

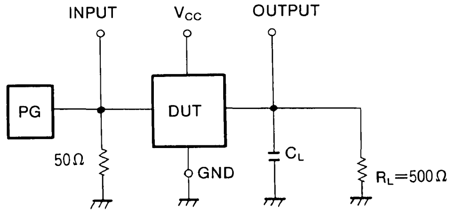
Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)				10	ns
t_{THL}						10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}-\overline{Y}$)					22	ns
t_{PHL}						24	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4				22	ns
t_{PHL}						24	ns
t_{PLH}		Number of delay gate stages 5				22	ns
t_{PHL}						25	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)				12		15	ns
t_{THL}						12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CS}-\overline{Y}$)					23		29	ns
t_{PHL}						25		31	ns
t_{PLH}	Low-level to high-level and High-level to low-level output propagation time (A − $\overline{Y}$)	Number of delay gate stages 4				23		29	ns
t_{PHL}						25		31	ns
t_{PLH}		Number of delay gate stages 5				24		30	ns
t_{PHL}						26		33	ns
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

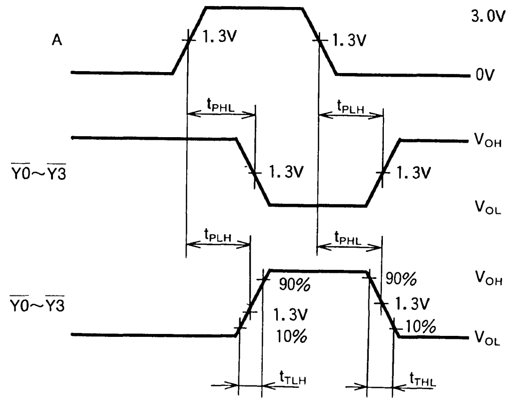
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per decoder)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D' = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

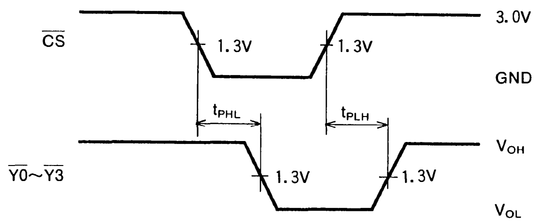
Note 5 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HC240-1P/FP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC240-1 is an integreted circuit chip consisting of two blocks of 3-state inverting buffers with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3 state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2∼6V
- Wide opreating temperature range : T_a=−40∼+85℃

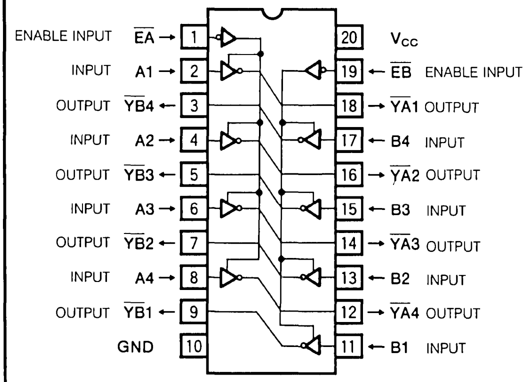
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

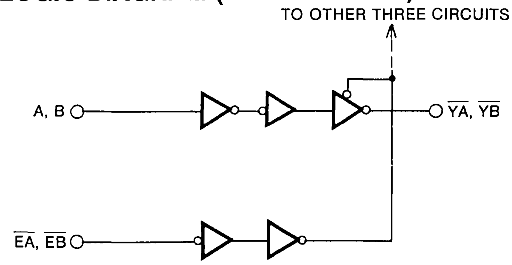
Use of silicon gate technology allows the M74HC240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. The M74HC240-1 consists of two independent blocks with each block containing four buffers. When enable input $\overline{E}$ is low and input A (or B) is low, then output $\overline{Y}$ will be set high. However, if A (or B) is high, then $\overline{Y}$ will be set low. When $\overline{E}$ is high, all outputs within the block will become high-impedence state, irrespective of A (or B). All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Input		output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2: M74HC240-1FP; T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40∼+85℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=2.0V	0		500	ns/V
		V_{CC}=4.5V	0		50	
		V_{CC}=6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, $\|I_O\|$=20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\|I_O\|$=20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IL}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

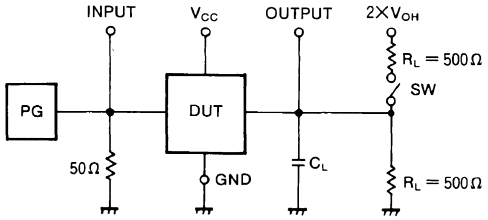
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—$\overline{YA}$, B—$\overline{YB}$)				14	ns
t_{PHL}					14	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—$\overline{YA}$, $\overline{EB}$—$\overline{YB}$)	C_L= 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—$\overline{YA}$, $\overline{EB}$—$\overline{YB}$)	C_L=50pF (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	2.0		13	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		14	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—$\overline{YA}$, B—$\overline{YB}$)		2.0		23	75		95	ns
			4.5		8	15		19	
			6.0		6	13		16	
t_{PHL}			2.0		21	75		95	ns
			4.5		8	15		19	
			6.0		6	13		16	
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—$\overline{YA}$, $\overline{EB}$—$\overline{YB}$)		2.0		11	105		130	ns
			4.5		6	21		26	
			6.0		5	18		22	
t_{PHZ}			2.0		16	105		130	ns
			4.5		9	21		26	
			6.0		8	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—$\overline{YA}$, $\overline{EB}$—$\overline{YB}$)		2.0		21	105		130	ns
			4.5		7	21		26	
			6.0		6	18		22	
t_{PZH}			2.0		24	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$=V_{CC}, $\overline{EB}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				39.7				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during opration under no-load condition is calculated using the follwing formula :
$P_D=C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

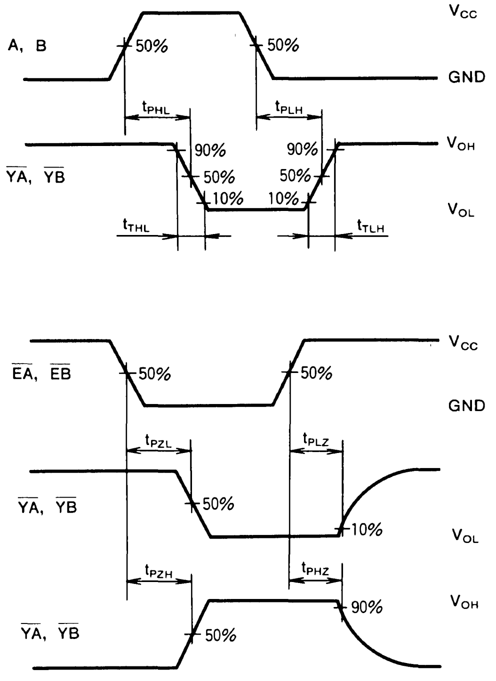
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT240-1P/FP

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT240-1 is an integrated circuit chip consisting of two blocks of 3-state inverting buffers with four independent circuits that share a common enable input.

FEATURES

- TTL level input : V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μ W/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

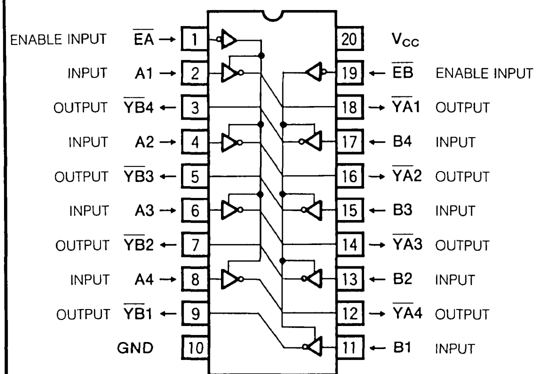
Use of sillicon gate technology allows the M74HCT240-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS240. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.

The M74HCT240-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A (or B) is low, then output $\overline{Y}$ will be set high. However, if A (or B) is high, then $\overline{Y}$ will be set low.

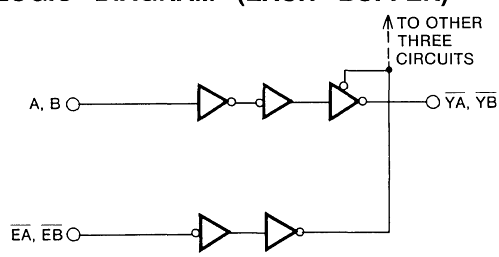
When $\overline{E}$ is high, then all outputs within the block become high-impedance state, irrespective of A (or B). All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	$\overline{YA}$, $\overline{YB}$
L	L	H
H	L	L
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HCT240-1FP , T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=4.5V	0		25	ns/V
		V_{CC}=5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V |I_O| =20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V |I_O| =20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I=V_{IH}, V_{IL}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−24mA, V_{CC}=4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=24mA, V_{CC}=4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I=GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I=V_{CC}, GND, I_0=0μA				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	V_I=2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value All others inputs are fixed at V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output	C_L=50pF (Note 5)			10	ns
t_{THL}	transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level				16	ns
t_{PHL}	output propagation time (A−$\overline{YA}$, B−$\overline{YB}$)				18	ns
t_{PLZ}	Low-level and high-level output	C_L= 5 pF (Note 5)			20	ns
t_{PHZ}	disable time ($\overline{EA}$−$\overline{YA}$, $\overline{EB}$−$\overline{YB}$)				20	ns
t_{PZL}	Low-level and high-level output	C_L=50pF (Note 5)			22	ns
t_{PZH}	enable time ($\overline{EA}$−$\overline{YA}$, $\overline{EB}$−$\overline{YB}$)				22	ns

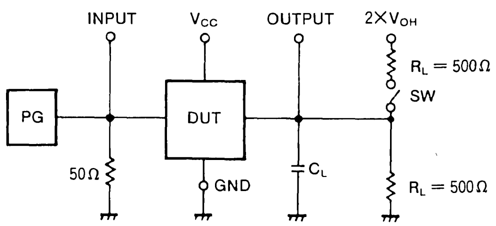
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=−40~85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40~+85℃ Min	Limits −40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−$\overline{YA}$, B−$\overline{YB}$)			9	17		21	ns
t_{PHL}				12	19		24	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$−$\overline{YA}$, $\overline{EB}$−$\overline{YB}$)			8	23		29	ns
t_{PHZ}				10	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$−$\overline{YA}$, $\overline{EB}$−$\overline{YB}$)			11	23		29	ns
t_{PZH}				9	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$=V_{CC}, $\overline{EB}$=GND			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			41.7				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

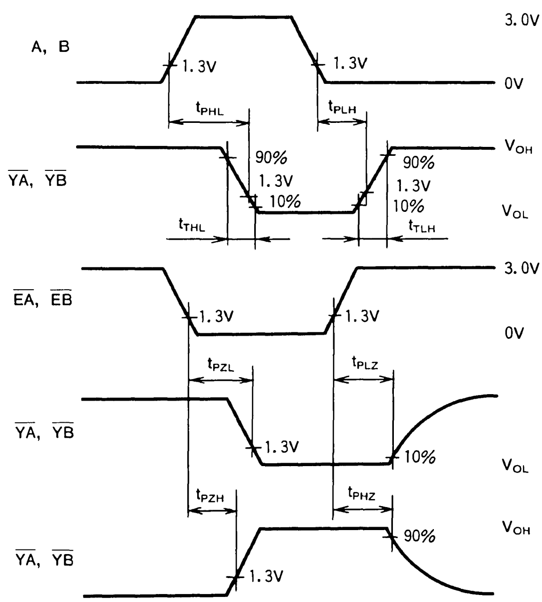
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%)t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC241-1P/FP

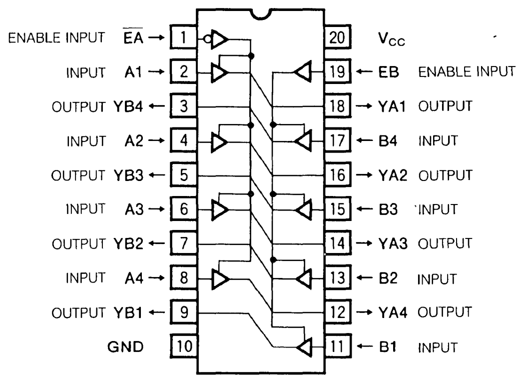
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION
The M74HC241-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~85℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

FUNCTION
Use of silicon gate technology allows the M74HC241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. The M74HC241-1 consists of two independent blocks with each block containing for buffers.

When enable input $\overline{EA}$ is low and input A is low, then output YA will become low However, if A is high, then YA will become high. Inverted in the other block, a high enable input EB signal causes opreation the same as that just described with input B signal output at YB.

When $\overline{EA}$ is high or EB is low then all the output within the block will become high-impedance state, irrespective A or B.

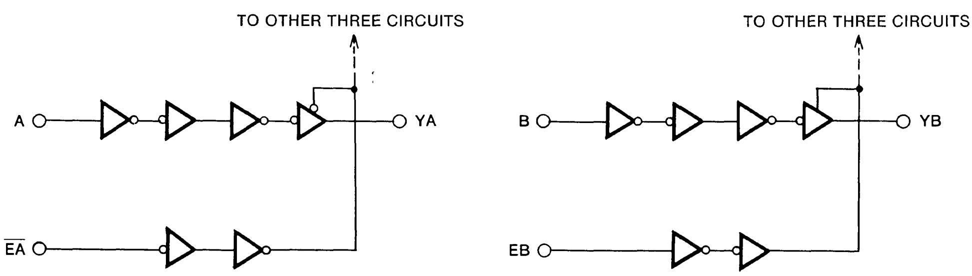
FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2: M74HC241-1FP, T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=2.0V	0		500	ns/V
		V_{CC}=4.5V	0		50	
		V_{CC}=6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}=0.1V, $\|I_O\|$=20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\|I_O\|$=20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IH}, V_{IL}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

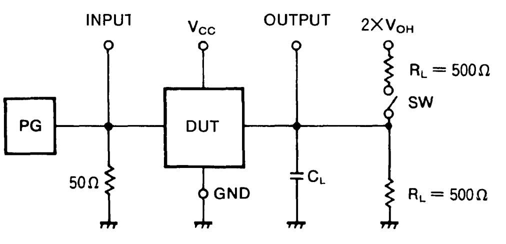
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—YA, B—YB)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—YA, EB—YB)	C_L= 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—YA, EB—YB)	C_L=50pF (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	2.0		13	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		21	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—YA, B—YB)		2.0		25	80		100	ns
			4.5		9	16		20	
			6.0		6	14		17	
t_{PHL}			2.0		24	80		100	ns
			4.5		9	16		20	
			6.0		7	14		17	
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—YA, EB—YB)		2.0		13	105		130	ns
			4.5		6	21		26	
			6.0		5	18		22	
t_{PHZ}			2.0		15	105		130	ns
			4.5		10	21		26	
			6.0		8	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—YA, EB—YB)		2.0		22	105		130	ns
			4.5		7	21		26	
			6.0		6	18		22	
t_{PZH}			2.0		24	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$=V_{CC}, EB=GND				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				43.7				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer) The power dissipated during opration under no-load condition is calculated using the follwing formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

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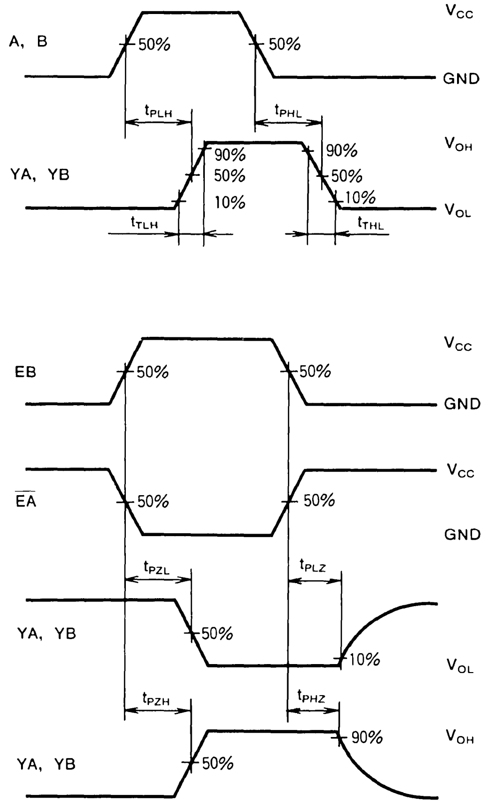
TIMING DIAGRAM



M74HCT241-1P/FP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT241-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES

- TTL level input V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, Ta=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : Ta=−40~+85℃

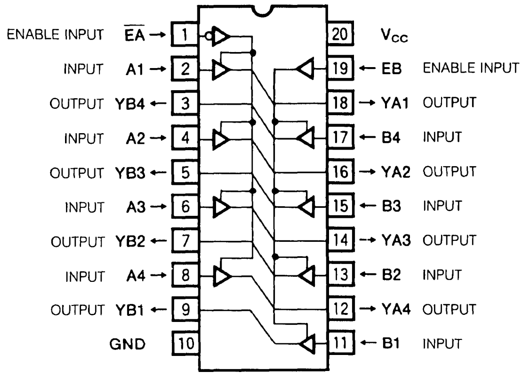
APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HCT241-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS241.The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.
The M74HCT241-1 consists of two independent blocks with each block containing four buffers.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N

When enable input $\overline{EA}$ is low and input A is low, then output YA will be set low. However, if A is high, then YA will be set high. Inverted in the other block, a high enable input EB signal causes operation the same as that just described with input B signal output at YB.
When $\overline{EA}$ is high or EB is low, all output within the block become high-impedance state, irrespective A or B.

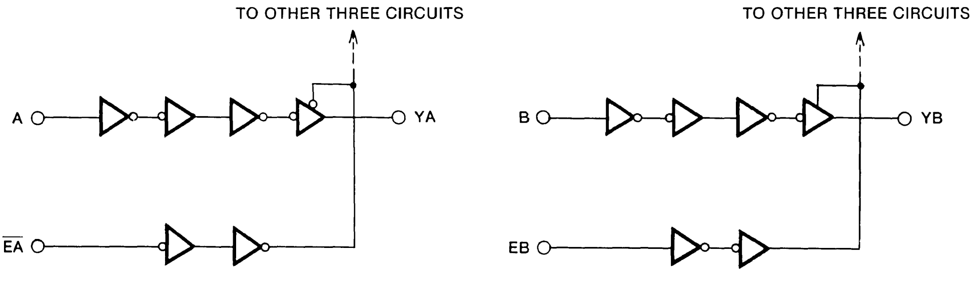
FUNCTION TABLE (Note 1)

Inputs		Output
A	$\overline{EA}$	YA
L	L	L
H	L	H
X	H	Z

Inputs		Output
B	EB	YB
L	H	L
H	H	H
X	L	Z

Note 1 : Z : High impedance
X : Irrelevant

LOGIC DIAGRAM (EACH BUFFER)



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HCT241-1FP , T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Static supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value All others are fixed to V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level	C_L=50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level				17	ns
t_{PHL}	output propagation time (A−YA, B−YB)				19	ns
t_{PLZ}	Low-level and high-level output	C_L= 5 pF (Note 5)			20	ns
t_{PHZ}	disable time ($\overline{EA}$−YA, EB−YB)				20	ns
t_{PZL}	Low-level and high-level output	C_L=50pF (Note 5)			22	ns
t_{PZH}	enable time ($\overline{EA}$−YA, EB−YB)				22	ns

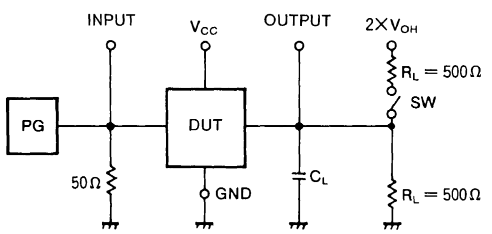
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=−40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−YA, B−YB)			8	18		23	ns
t_{PHL}				11	20		25	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$−YA, EB−YB)			8	23		29	ns
t_{PHZ}				10	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$−YA, EB−YB)			9	23		29	ns
t_{PZH}				7	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$ = V_{CC}, EB = GND			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			43.8				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during opration under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

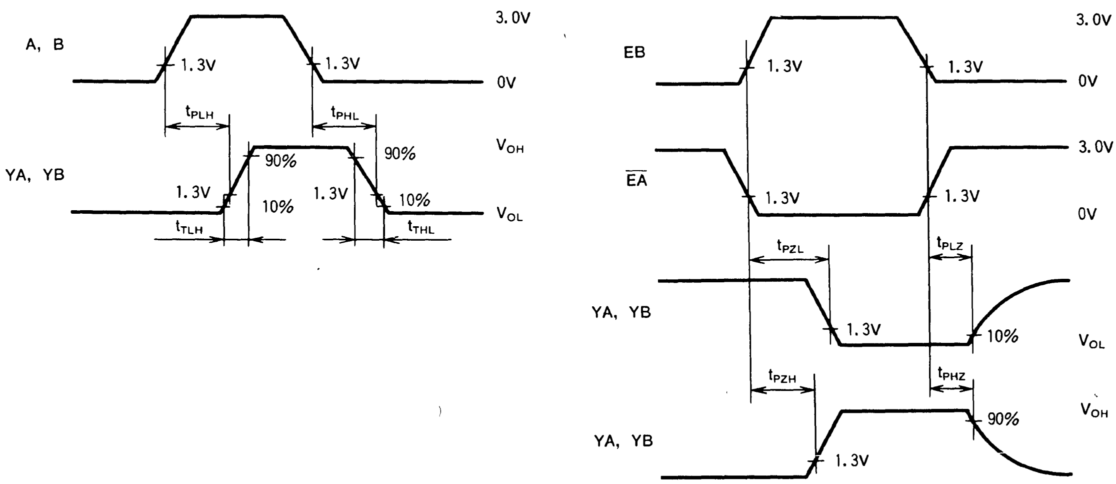
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%～90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC244-1P/FP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μ/W/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2～6V
- Wide operating temperature range : T_a=−40～+85℃

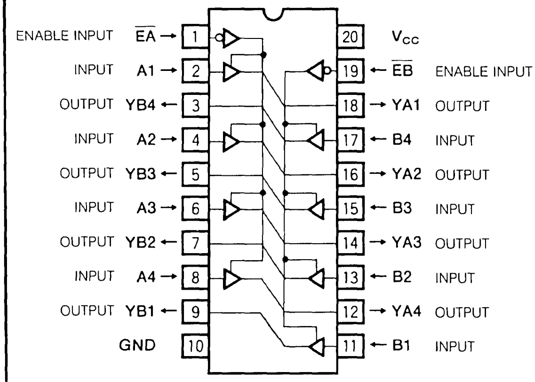
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

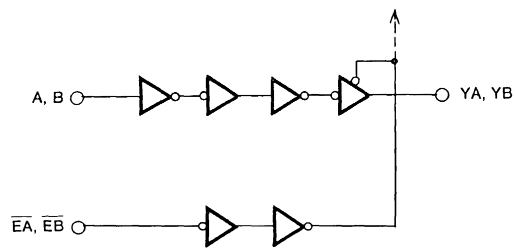
Use of silicon gate technology allows the M74HC244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.
The M74HC244-1 consists of two independent blocks with each block containing four buffers.
When enable input $\overline{E}$ is low and input A or B is low, output Y will be set low, However, if A or B is high, then Y will be set high. When $\overline{E}$ is high, all outputs within the block will become high-impedance state, irrespective A or B. All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC244-1FP ; T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40∼+85℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=2.0V	0		500	ns/V
		V_{CC}=4.5V	0		50	
		V_{CC}=6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=V_{CC}−0.1V, |I_O|=20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O|=20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IL}, V_{IH}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

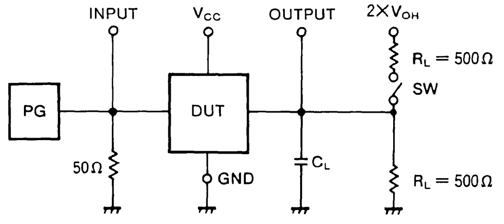
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—YA, B—YB)				15	ns
t_{PHL}					15	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—YA, $\overline{EB}$—YB)	C_L= 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—YA, $\overline{EB}$—YB)	C_L=50pF (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	2.0		13	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		18	60		75	ns
			4.5		4	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—YA, B—YB)		2.0		24	80		100	ns
			4.5		8	16		20	
			6.0		7	14		17	
t_{PHL}			2.0		22	80		100	ns
			4.5		8	16		20	
			6.0		7	14		17	
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$—YA, $\overline{EB}$—YB)		2.0		12	105		130	ns
			4.5		6	21		26	
			6.0		5	18		22	
t_{PHZ}			2.0		16	105		130	ns
			4.5		9	21		26	
			6.0		8	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$—YA, $\overline{EB}$—YB)		2.0		21	105		130	ns
			4.5		7	21		26	
			6.0		6	18		22	
t_{PZH}			2.0		24	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}$=V_{CC}, $\overline{EB}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				42.4				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

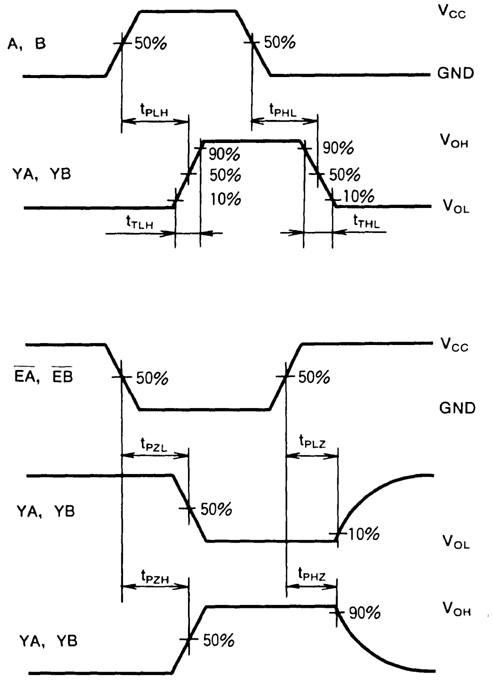


Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT244-1P/FP

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION
The M74HCT 244-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES
- TTL level input V_{IL}=0.8V max., V_{IH}=2.0V min.
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment

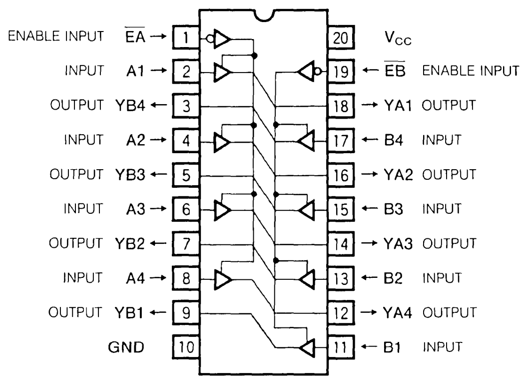
FUNCTION
Use of silicon gate technology allows the M74HCT244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.

The M74HCT244-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A or B is low, then output Y will be set to low. However, if A or B is high, then Y will be set to high.

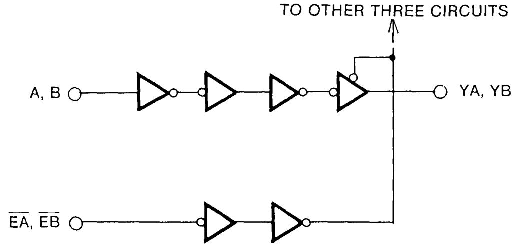
When $\overline{E}$ is high, then all output within the block will become high-impedance state, irrespective of A (or B). All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$ of the two blocks.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH BUFFER)



FUNCTION TABLE (Note 1)

Inputs		Output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65～+150	℃

Note 2 : M74HC244-1FP , T_a=−40～+75℃ and T_a=75～85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40～+85℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=4.5V	0		25	ns/V
		V_{CC}=5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40～+85℃ Min	−40～+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=V_{CC}−0.1V, |I_O|=20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O|=20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I=V_{IH}, V_{IL}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−24mA, V_{CC}=4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=24mA, V_{CC}=4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I=GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND				−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	V_I=2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value All other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level	C_L=50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level				17	ns
t_{PHL}	output propagation time (A−YA, B−YB)				19	ns
t_{PLZ}	Low-level and high-level output	C_L= 5 pF (Note 5)			20	ns
t_{PHZ}	disable time ($\overline{EA}$−YA, $\overline{EB}$−YB)				20	ns
t_{PZL}	Low-level and high-level output	C_L=50pF (Note 5)			22	ns
t_{PZH}	enable time ($\overline{EA}$−YA, $\overline{EB}$−YB)				22	ns

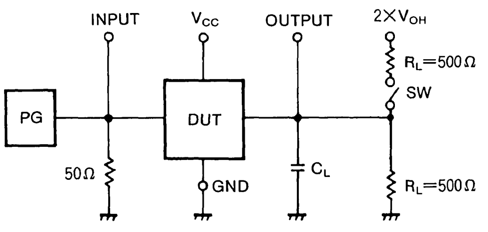
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=−40~+85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40~+85℃ Min	Limits −40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−YA, B−YB)			8	18		23	ns
t_{PHL}				10	20		25	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{EA}$−YA, $\overline{EB}$−YB)			8	23		29	ns
t_{PHZ}				11	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{EA}$−YA, $\overline{EB}$−YB)			8	23		29	ns
t_{PZH}				8	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{EA}=V_{CC}$, $\overline{EB}$=GND			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			43.6				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D=C_{PD} \cdot V_{CC}^2 \cdot f_i+I_{CC} \cdot V_{CC}$

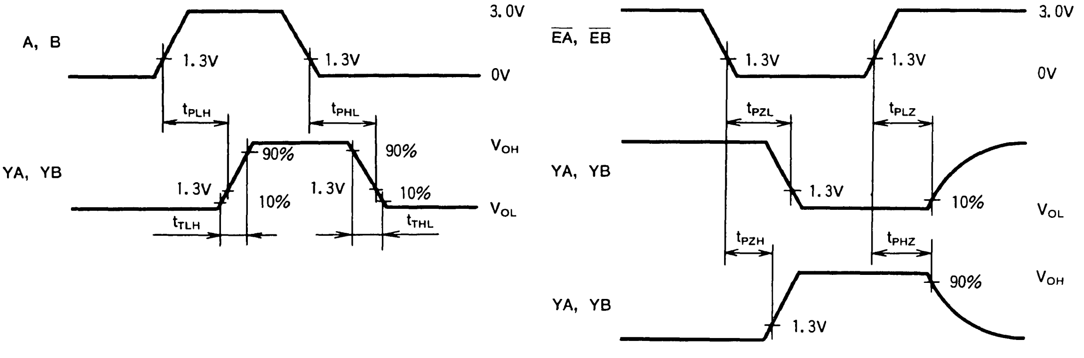
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%)t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC245-1P/FP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION
The M74HC245-1 is an integrated circuit chip consisting of eight transceivers with noninverted outputs.

FEATURES
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

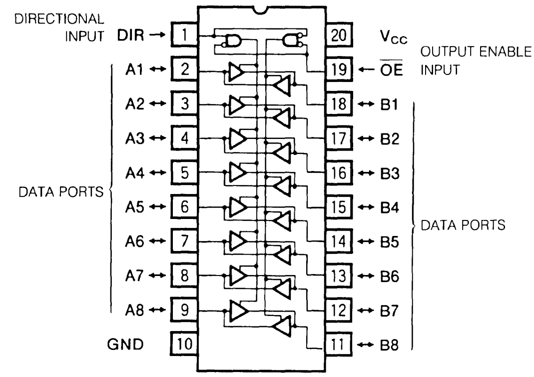
FUNCTION
Use of silicon gate technology allows the M74HC245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.
The input/output direction is controlled by direction input DIR.
When DIR is high, the A data ports will become input terminals and the B data ports will become output terminals.
When DIR is low, B will become input terminals and A will become output terminals.
When output enable $\overline{OE}$ is high, A and B will both become high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

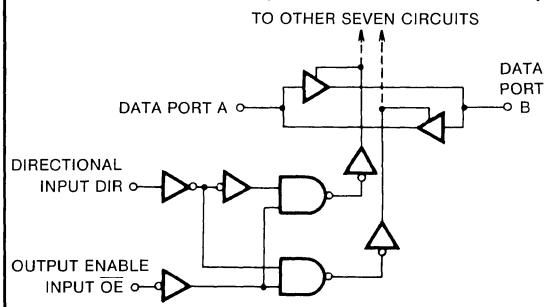
Note 1 : I : Input pin
O : Output pin
Z : High impedance (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



MITSUBISHI ELECTRIC

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC245-1FP : T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40∼+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=2.0V	0		500	ns/V
		V_{CC}=4.5V	0		50	
		V_{CC}=6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O| =20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O| =20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IL}, V_{IH}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C)

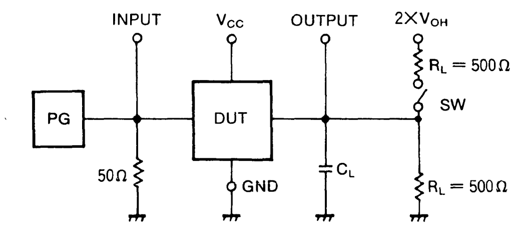
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−B, B−A)				16	ns
t_{PHL}					16	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$−A, B)	C_L= 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$−A, B)	C_L=50pF (Note 4)			27	ns
t_{PZH}					27	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85°C)

Symbol	Parameter	Test conditions	V_{CC}(V)	25°C Min	25°C Typ	25°C Max	−40~+85°C Min	−40~+85°C Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	2.0		16	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{THL}			2.0		23	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−B, B−A)		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PHL}			2.0		27	85		105	ns
			4.5		10	17		21	
			6.0		8	14		18	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$−A, B)		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}			2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		11	24		30	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$−A, B)		2.0		32	140		175	ns
			4.5		11	28		35	
			6.0		10	24		30	
t_{PZH}			2.0		33	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				56.3				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

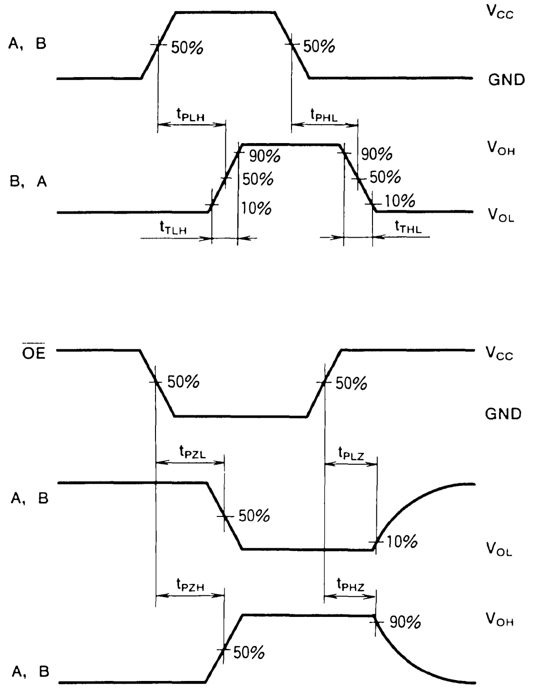
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HCT245-1P/FP

OCTAL 3-STATE NONIVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION
The M74HCT 245-1 is an integrated circuit chip consisting of eight transceivers with noninverted outputs.

FEATURES
- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

FUNCTION
Use of silicon gate technology allows the M74HCT245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.

Two buffers with 3-state noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by directions input DIR.

When DIR is high, the A data ports will become input terminals and the B data ports will become output terminals.

When DIR is low, B will become input termilnals and A will become output terminals.

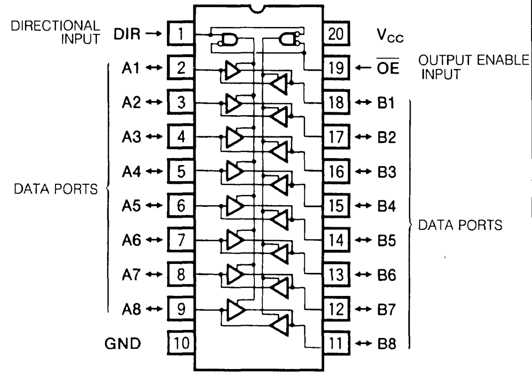
When output enable $\overline{OE}$ is high, A and B will both become high-impedance state and they will be separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

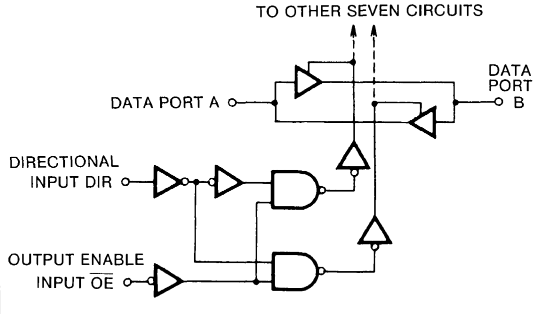
Note 1 : I : Input pin
O : Output pin
Z : High impedance (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



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OCTAL 3-STATE
NONIVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS (T_a=−40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I<0V	−20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65～+150	℃

Note 2 : M74HCT245-1FP : T_a=−40～+75℃ and T_a=75～85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40～+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC}=4.5V	0		25	ns/V
		V_{CC}=5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40～+85℃ Min	−40～+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$=20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$=20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I=V_{IH}, V_{IL}	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH}=−24mA, V_{CC}=4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IL}	I_{OL}=20μA			0.1		0.1	V
			I_{OL}=24mA, V_{CC}=4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I=V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I=GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND				−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	V_I=2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value All others are fixed to V_{CC} and GND

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

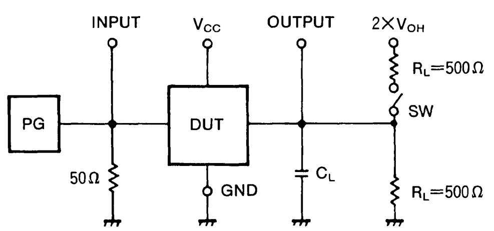
Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level	C_L=50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level				18	ns
t_{PHL}	output propagation time (A−B, B−A)				20	ns
t_{PLZ}	Low-level and high-level output	C_L= 5 pF (Note 5)			27	ns
t_{PHZ}	disable time ($\overline{OE}$−A, B)				27	ns
t_{PZL}	Low-level and high-level output	C_L=50pF (Note 5)			29	ns
t_{PZH}	enable time ($\overline{OE}$−A, B)				29	ns

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=−40∼+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40∼+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}	low-level output transition time			5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time			9	19		24	ns
t_{PHL}	(A−B, B−A)			12	21		26	ns
t_{PLZ}	Low-level and high-level output disable time			10	30		38	ns
t_{PHZ}	($\overline{OE}$−A, B)			13	30		38	ns
t_{PZL}	Low-level and high-level output enable time			12	30		38	ns
t_{PZH}	($\overline{OE}$−A, B)			11	30		38	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$=V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			62.0				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

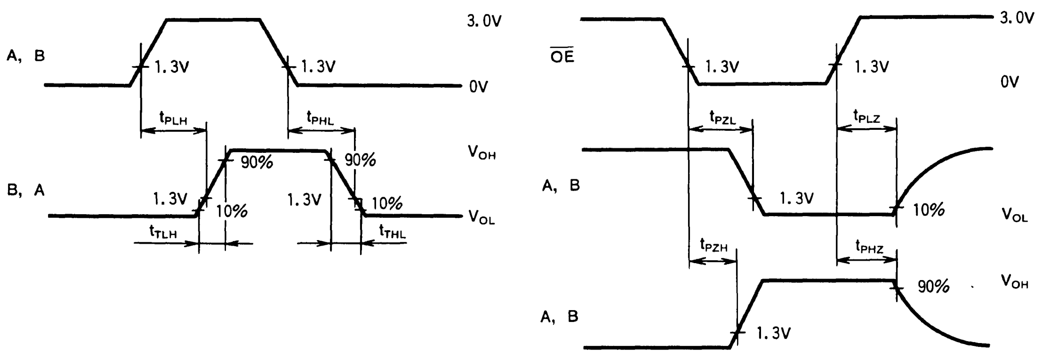
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%∼90%)t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC273-1P/FP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC273-1 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- High-fanout output:($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed: (clock frequency) 50MHz typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation: 25μW/package, max ($V_{CC}=5V$, $T_a=25$℃, quiescent state)
- High noise margin: 30% of V_{CC}, min ($V_{CC}=4.5V$, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: $V_{CC}=2\sim6V$
- Wide operating temperature range: $T_a=-40\sim+85$℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC273-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS273.

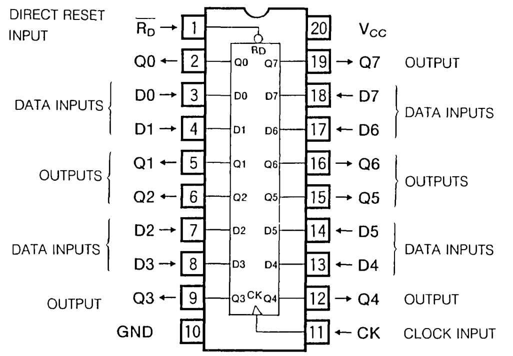
The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC273-1 contains eight edge-triggered D-type flip flops with common direct reset input $\overline{R_D}$ and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at output Q in accordance with the function table given.

When $\overline{R_D}$ is low, all outputs Q will become low, irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained high.

PIN CONFIGURATION (TOP VIEW)



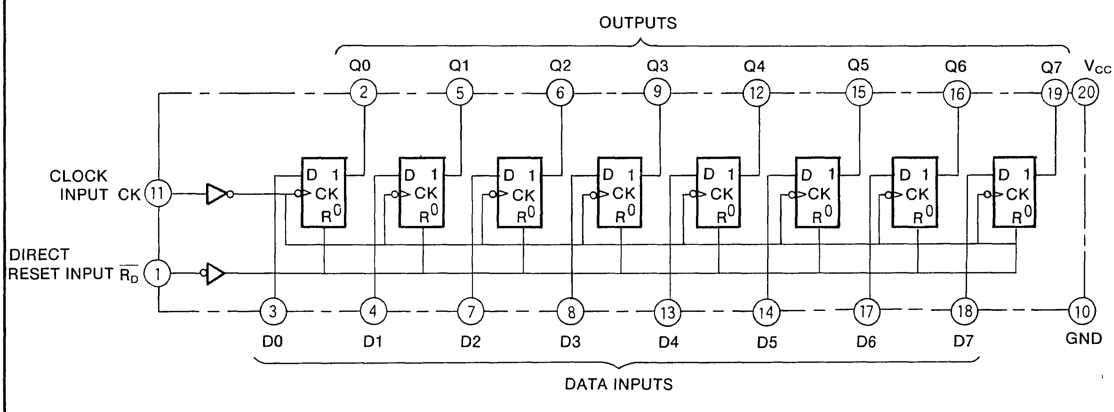
Outline 20P4
20P2N

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0
H	↓	X	Q^0

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q before clock input changed
X : Irrelevant

LOGIC DIAGRAM



OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HC273-1FP, $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 2.0V$	0		500	ns/V
		$V_{CC} = 4.5V$	0		50	
		$V_{CC} = 6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$	2.0			0.1		0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1		0.1	
			$I_{OL} = 20\mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I = 6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				20	ns
t_{PHL}					20	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

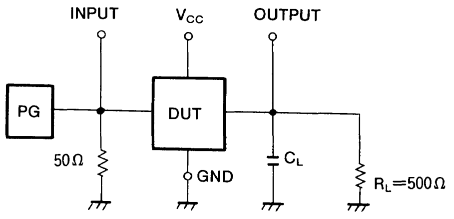
Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHL}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)		2.0			125		155	ns
			4.5			25		31	
			6.0			21		26	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

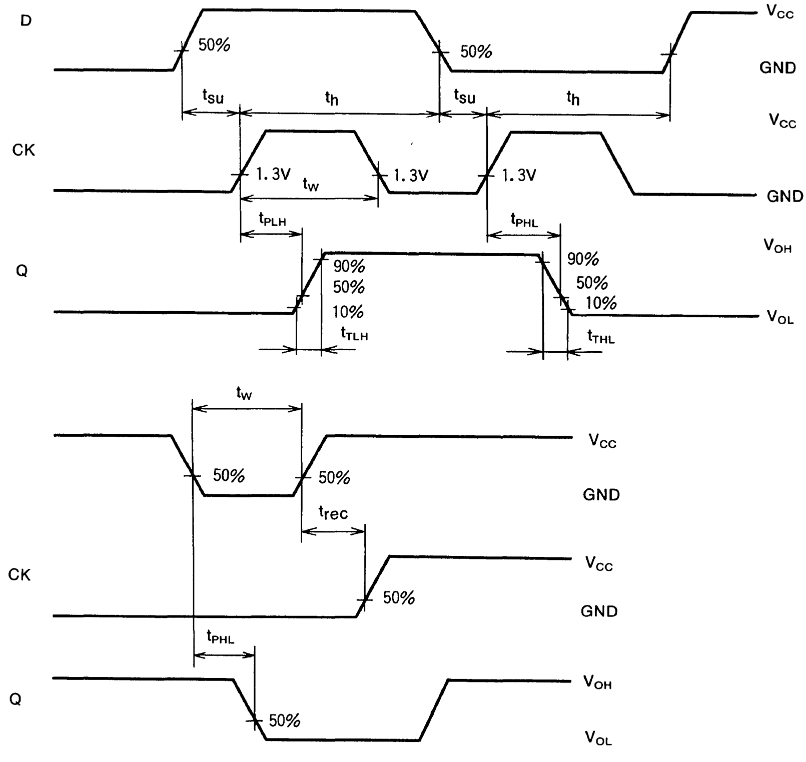
Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_W	CK, $\overline{R_D}$ pulse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{su}	D setup time with respect to CK		2.0	75			95		ns
			4.5	15			19		
			6.0	13			16		
t_h	D hold time with respect to CK		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		2.0	75			95		ns
			4.5	15			19		
			6.0	13			16		

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HCT273-1P/FP

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT273-1 is a semiconductor integrated circuit consisting of eight positive-edge triggered D-type flip flops with common clock and direct reset inputs.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout output:(I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: (clock frequency) 50MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range. T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT273-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS273.

The M74HCT273-1 contains eight edge-triggered D-type flip flops with common direct reset input $\overline{R_D}$ and common clock input CK.

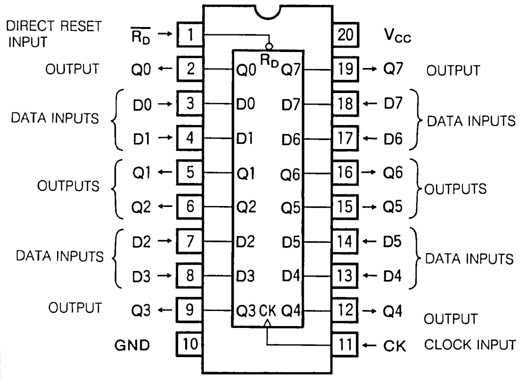
When CK changes from low-level to high-level, the signals just previously input at D appears at output Q in accordance with the function table given.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

When $\overline{R_D}$ is low, all outputs Q will become low, irrespective of other inputs. When used as a D-type flip flop, $\overline{R_D}$ should be maintained high.

PIN CONFIGURATION (TOP VIEW)



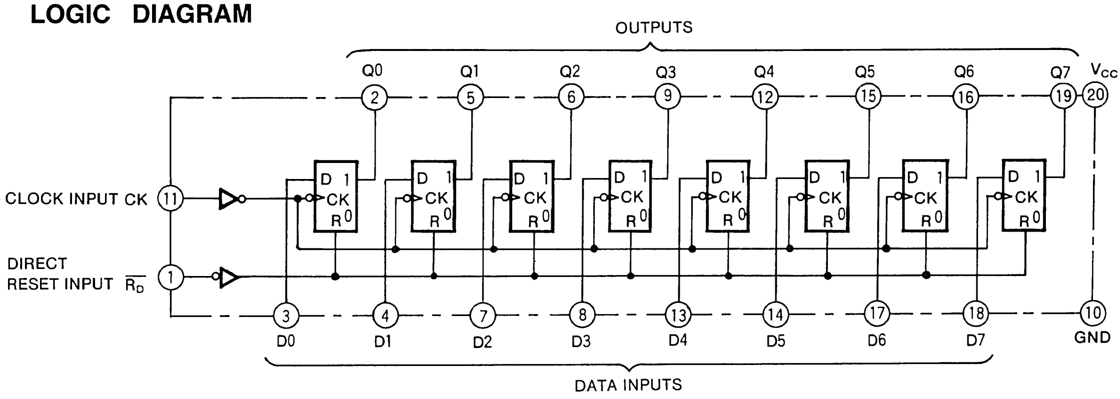
Outline 20P4 20P2N

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{R_D}$	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0
H	↓	X	Q^0

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
Q^0 : Output state Q before clock input changed
X : Irrelevant

LOGIC DIAGRAM



OCTAL D-TYPE FLIP-FLOP
WITH COMMON CLOCK AND RESET WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HCT273-1FP, $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$, $\|I_O\| = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$, $\|I_O\| = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IL}$	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC}=4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC}=4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = 5.5V$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$				−0.1		−1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent state supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all others are fixed at V_{CC} or GND

OCTAL D-TYPE FLIP-FLOP
WITH COMMON CLOCK AND RESET WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	C_L = 50pF (Note 5)	35			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				22	ns
t_{PHL}					24	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 5)		32			26		MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time					12		15	ns
t_{THL}						12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)					23		29	ns
t_{PHL}						25		31	ns
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)					29		36	ns
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 4)								pF

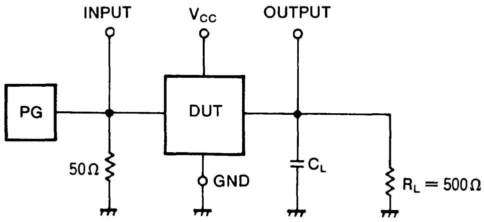
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	CK, $\overline{R_D}$ pulse width		4.5	12			15		ns
t_{su}	D setup time with respect to CK		4.5	15			19		ns
t_h	D hold time with respect to CK		4.5	5			6		ns
t_{rec}	$\overline{R_D}$ recovery time with respect to CK		4.5	15			19		ns

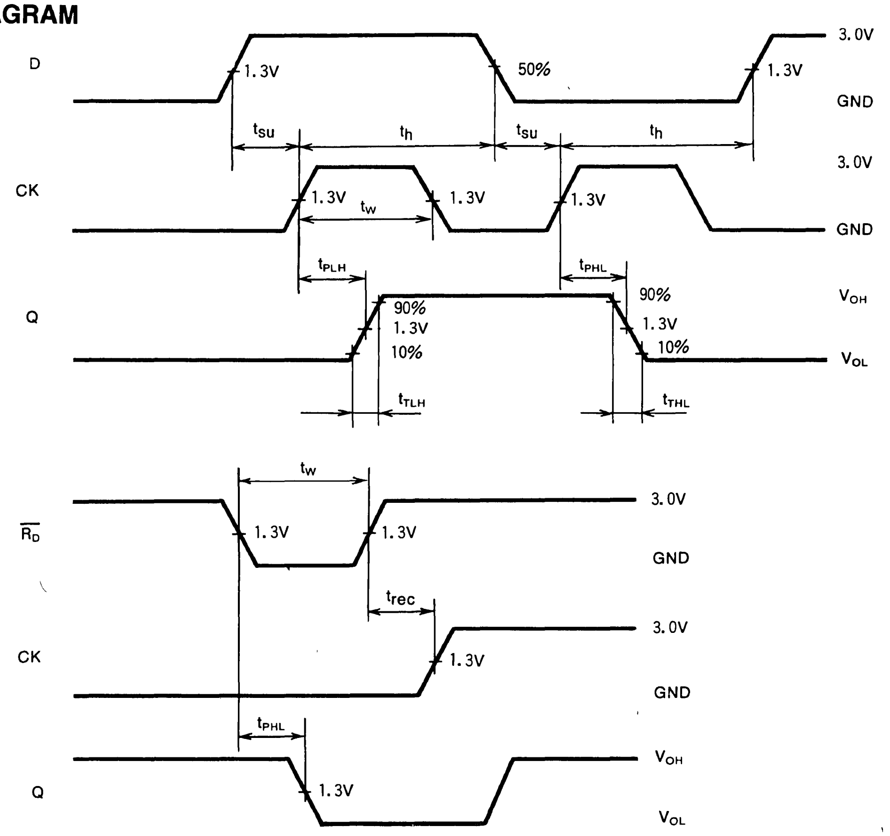
**OCTAL D-TYPE FLIP-FLOP
WITH COMMON CLOCK AND RESET WITH LSTTL-COMPATIBLE INPUTS**

Note 5 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HC373-1P/FP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373-1 is an integrated circuit chip consisting of eight 3-state output D-type latches with common-enable input and output-enable input.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2～6V
- Wide operating temperature range : T_a=−40～+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

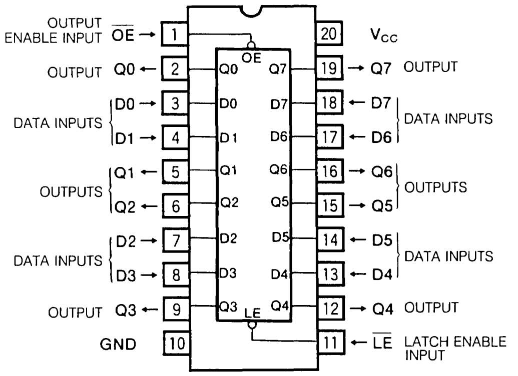
Use of silicon gate technology allows the M74HC373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC373-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

When $\overline{LE}$ is high-level, the data input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high to low-level, the data immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low-level, the contents stored in the latch will not be affected.

PIN CONFIGURATION (TOP VIEW)



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When $\overline{OE}$ is high-level, all outputs Q will become high-impedance states.

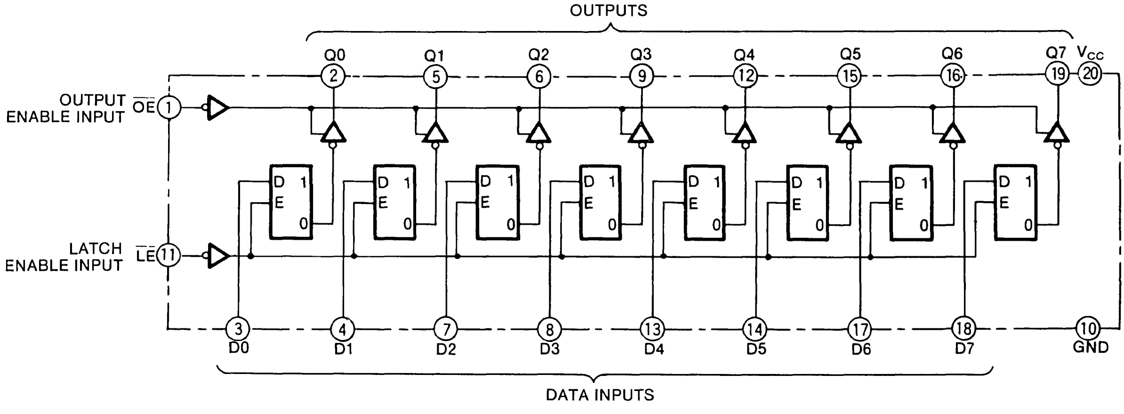
A version of the M74HC373-1 with the same pin connection and an inverted output, the M74HC533-1, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before $\overline{LE}$ changed.
Z : High impedance
X : Irrelevant

LOGICAL DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2: M74HC373-1FP : T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-levl input voltage	V_O = 0.1V, V_{CC} − 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L=50pF$ (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − Q)				17	ns
t_{PHL}					17	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − Q)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − Q)	$C_L=5pF$ (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)	$C_L=50pF$ (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS ($V_{CC}=2\sim6V$, $T_a=-40\sim+85°C$)

Symbol	Parameter	Test conditions		Limits					Unit
				25°C			−40∼+85°C		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L=50pF$ (Note 4)	2.0		12	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		18	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − Q)		2.0		36	90		115	ns
			4.5		9	18		23	
			6.0		7	15		20	
t_{PHL}			2.0		28	90		115	ns
			4.5		10	18		23	
			6.0		9	15		20	
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − Q)		2.0		32	105		130	ns
			4.5		11	21		26	
			6.0		9	18		22	
t_{PHL}			2.0		33	105		130	ns
			4.5		11	21		26	
			6.0		9	18		22	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − Q)		2.0		15	105		130	ns
			4.5		7	21		26	
			6.0		7	18		22	
t_{PHZ}			2.0		16	105		130	ns
			4.5		10	21		26	
			6.0		9	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)		2.0		22	105		130	ns
			4.5		8	21		26	
			6.0		6	18		22	
t_{PZH}			2.0		24	105		130	ns
			4.5		9	21		26	
			6.0		7	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}=V_{CC}$				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				44.5				pF

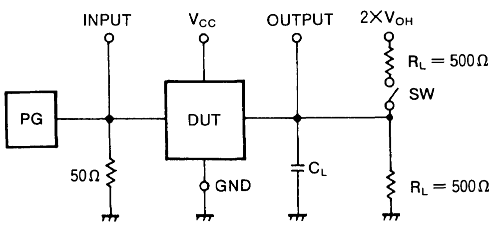
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D=C_{PD}\cdot V_{CC}^2\cdot f_I+I_{CC}\cdot V_{CC}$

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	Latch-enable pulse width		2.0	60	8		75		ns
			4.5	12	3		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	50	3		65		ns
			4.5	10	1		13		
			6.0	9	1		11		
t_h	D hold time with respect to $\overline{LE}$		2.0	25	−2		30		ns
			4.5	5	0		6		
			6.0	5	0		6		

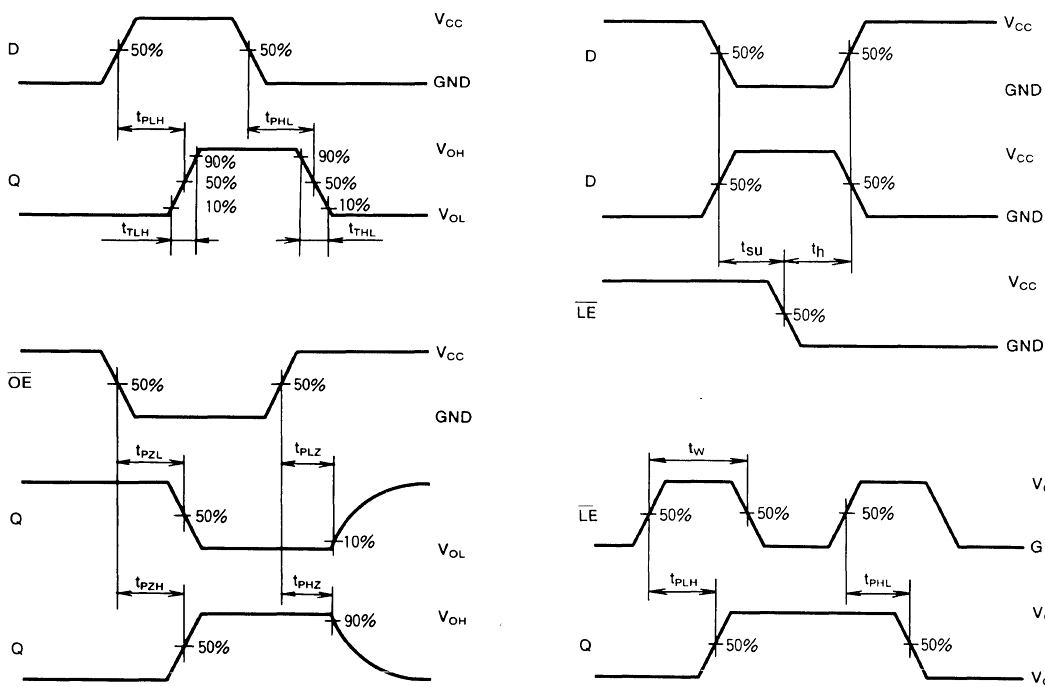
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT373-1P/FP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT373-1 is an integrated circuit chip consisting of eight 3-state output-D-type latches with common-enable input and output-enable input.

FEATURES

- TTL level inputs V_{IL}=0.8V max, V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74 LSTTL loads
- Wide opreating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HCT373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series While giving high-speed performance equivalent to the 74LS373. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. Used as such, no pull-up resistors are required.

The M74HCT373-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

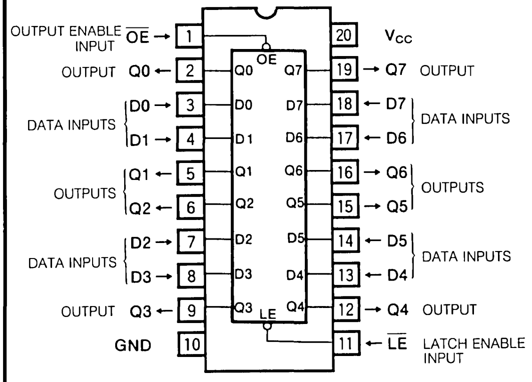
When $\overline{LE}$ is high-level, the data input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low-level, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs Q will become high-impedance states.

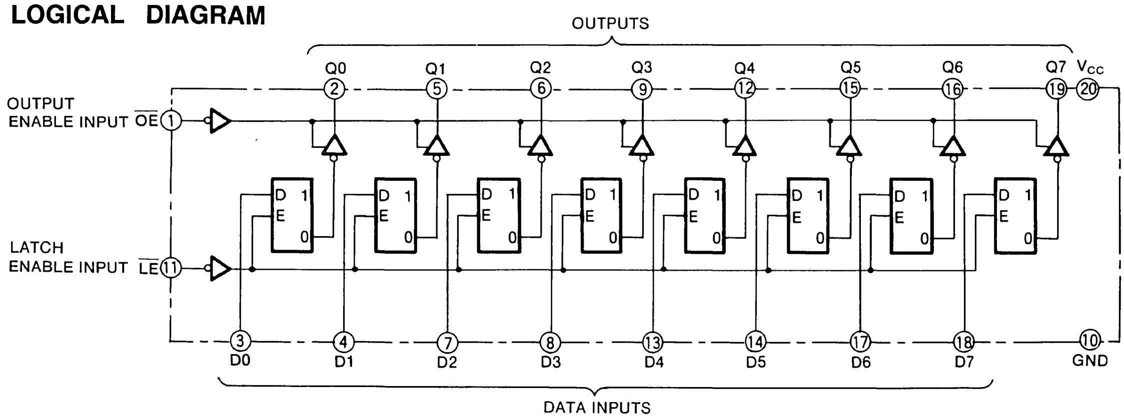
A version of the M74HCT373-1 with the same pin connection and an inverted output, the M74HCT533-1, is also available.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

LOGICAL DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2 : M74HCT373-1FP : $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at -7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$ $\lvert I_O \rvert = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = GND$				-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = GND$				-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set to this value All others are fixed to V_{CC} or GND

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − Q)				19	ns
t_{PHL}					21	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − Q)				22	ns
t_{PHL}					24	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − Q)	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 5)			22	ns
t_{PZH}					22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

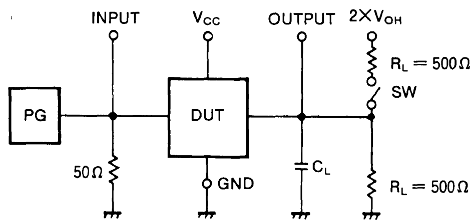
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-levl output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − Q)			9	20		25	ns
t_{PHL}				12	22		28	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − Q)			11	23		29	ns
t_{PHL}				13	25		31	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − Q)			9	23		29	ns
t_{PHZ}				11	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)			11	23		29	ns
t_{PZH}				8	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			47.1				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch) The power dissipated during opration under no-load condition is calculated using the follwing formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_W	Latch-enable pulse width		12	7		15		ns
t_{SU}	D set up time with respect to $\overline{LE}$		10	1		13		ns
t_h	D hold time with respect to $\overline{LE}$		5	1		6		ns

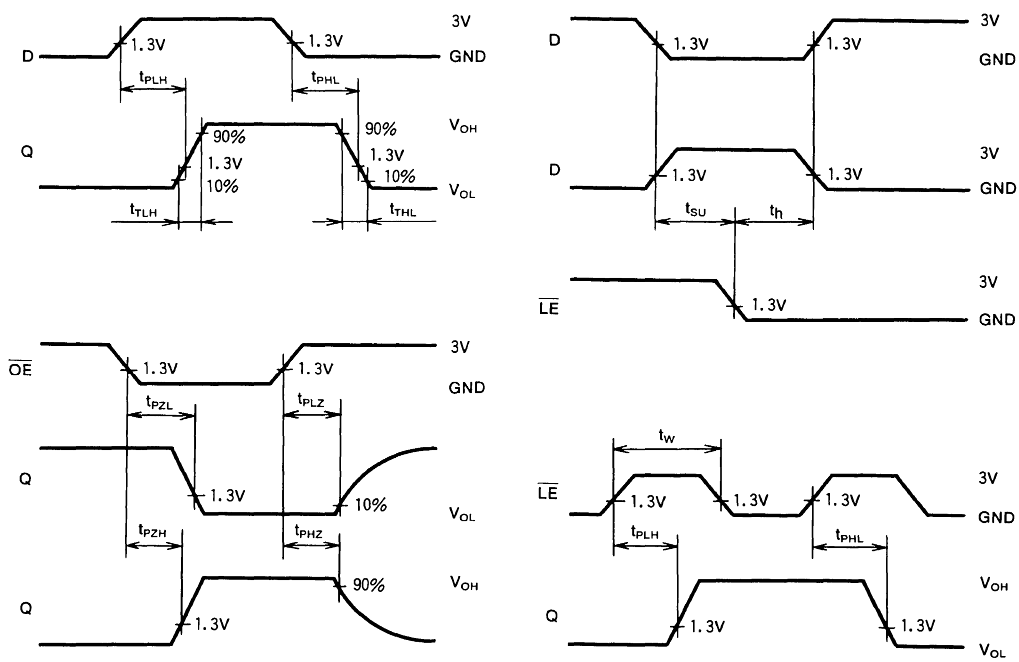
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI
ELECTRIC

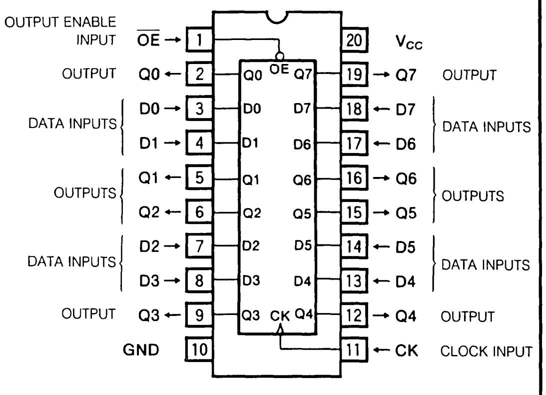
M74HC374-1P/FP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

DESCRIPTION
The M74HC374-1 is an integrated circuit chip consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : (Clock frequency) 80MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

FUNCTION
Use of silicon gate technology allows the M74HC374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC374-1 consists of eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

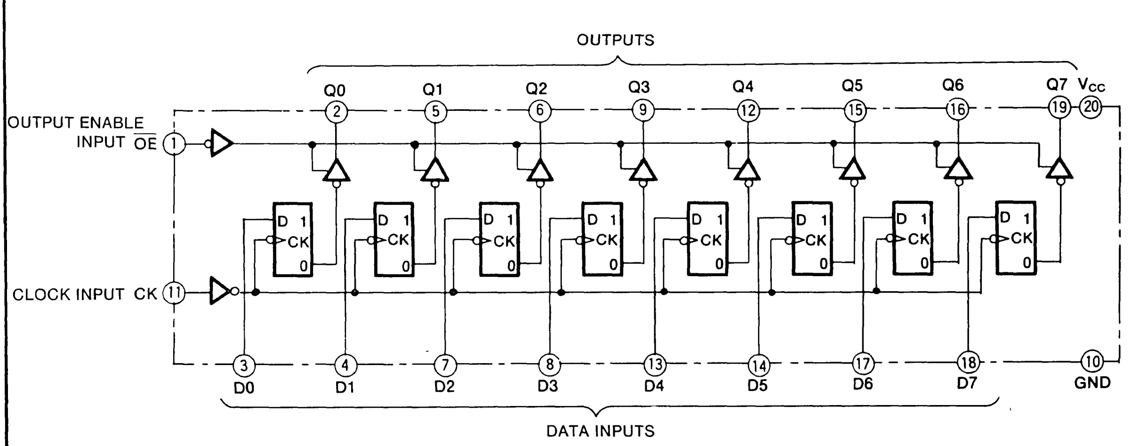
When CK changes from low-level to high-level, the signal just previously input D is stored in the flip-flop.

When $\overline{OE}$ is low-level, the signal stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high-level, all outputs Q will become high impedance states. The contents stored in the flip-flop will not be affecterd even if $\overline{OE}$ changes.

A version of the M74HC374-1 with the same pin connection and an inverted output, the M74HC534-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before CK changed
Z : High impedance
X : Irrelevant
↑ : Change from low-to high-level
↓ : Change from high-to low-level

ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HC374-1FP : T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\|I_O\|$ =20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, $\|I_O\|$ =20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IL}, V_{IH}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)			20	ns
t_{PHL}					20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85℃)

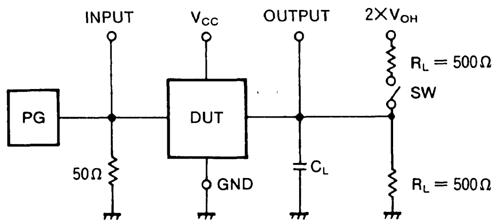
Symbol	Paramerter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum repetitive frequncy	C_L=50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-to high-level and high-to low-level output transition time		2.0		12	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		17	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK−Q)		2.0		35	105		130	ns
			4.5		12	21		26	
			6.0		10	18		22	
t_{PHL}			2.0		35	105		130	ns
			4.5		12	21		26	
			6.0		10	18		22	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$−Q)		2.0		16	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PHZ}			2.0		17	105		130	ns
			4.5		10	21		26	
			6.0		9	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$−Q)		2.0		23	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PZH}			2.0		24	105		130	ns
			4.5		10	21		26	
			6.0		8	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				61.0				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop). The power dissipated during operation under no-load condition is calculated using the following formura :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CLock pulse width		2.0	60	10		75		ns
			4.5	12	4		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to CK		2.0	50	4		65		ns
			4.5	10	2		13		
			6.0	9	1		11		
t_h	D hold time with respect to CK		2.0	25	0		30		ns
			4.5	5	0		6		
			6.0	5	0		6		

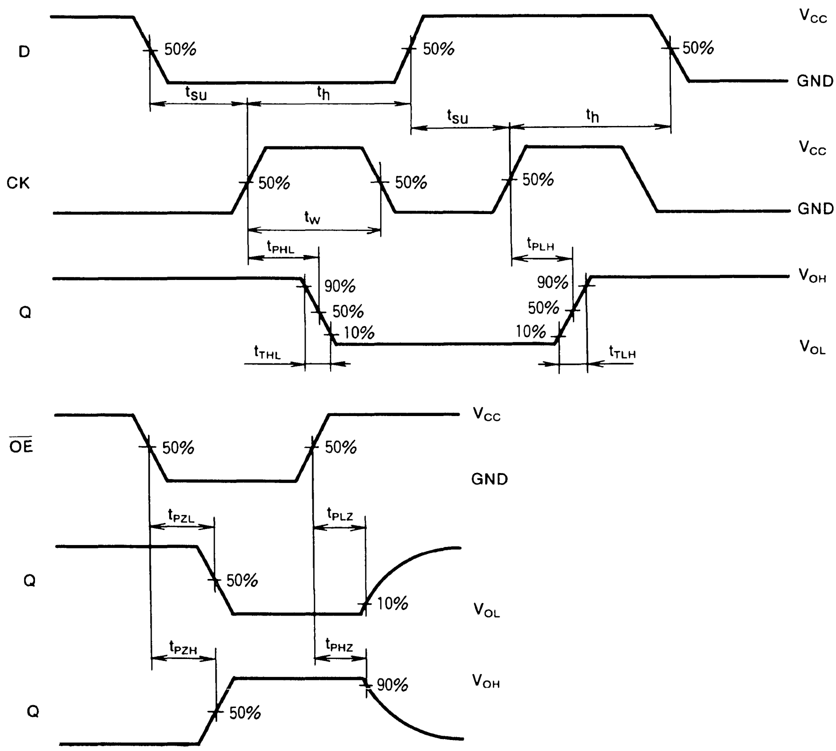
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



M74HCT374-1P/FP

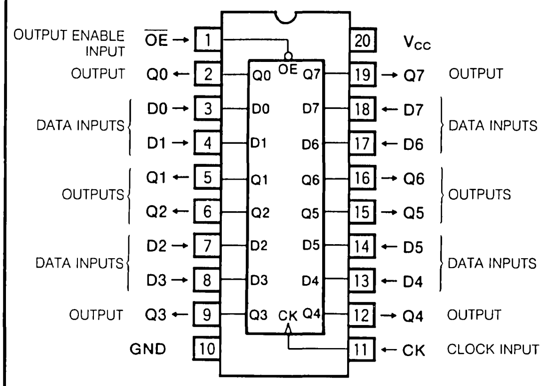
OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION
The M74HCT374-1 is an integrated circuit chip consisting of eight positive-edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES
- TTL level input $V_{IL}=0.8V$ max $V_{IH}=2.0V$ min
- High-fanout 3-state output : ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed : (Clock frequency) 70MHz typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation : 25μW/package, max ($V_{CC}=5V$, $T_a=25℃$, quiescent state)
- Capable of driving 60 74 LSTTL loads
- Wide operating temperature range : $T_a=-40\sim+85℃$

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

FUNCTION
Use of silicon gate technology allows the M74HCT374-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS374. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. Used as such, no pull-up resistors are required.

The M74HCT374-1 consists of eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

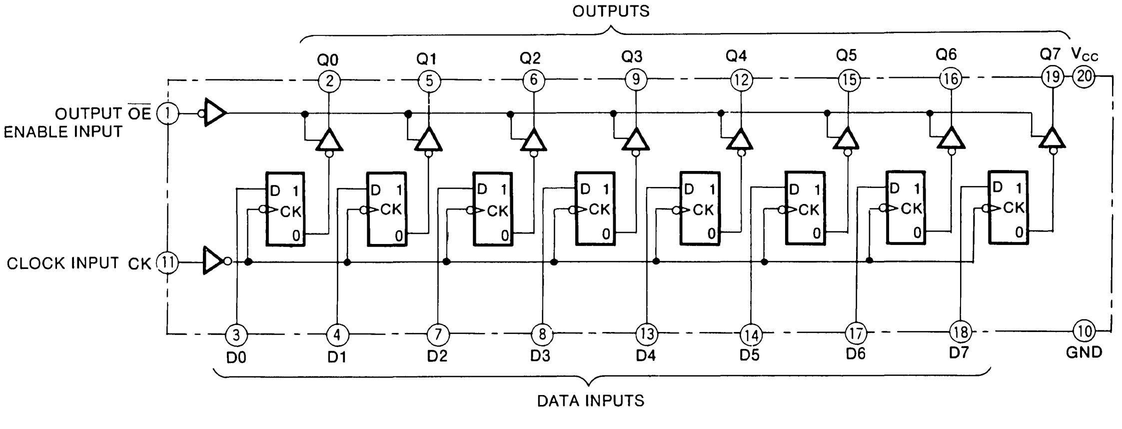
When CK changes from low-level to high-level, the signal just previously input at D is stored in the flip-flop.

When $\overline{OE}$ is low-level, the signal stored in the flip-flop will be output to Q.

When $\overline{OE}$ is high-level, all outputs Q will become high impedance states. The contents stored in the flip-flop will not be affecterd even if $\overline{OE}$ changes.

A version of the M74HCT374-1 with the same pin connection and an inverted output, the M74HCT534-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q^0
L	H	X	Q^0
L	↓	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before CK changed.
Z : High impedance
X : Irrelevant
↑ : Change from low-to high-level
↓ : Change from high-to low-level

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HCT374-1FP : T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless othrwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC} − 0.1V, $\lvert I_O \rvert$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set to this value All others are fixed to V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 5)	35			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − Q)				22	ns
t_{PHL}					24	ns
t_{PLZ}	Low-level and high- level output disable time ($\overline{OE}$ − Q)	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 5)			22	ns
t_{PZH}					22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40~+85℃)

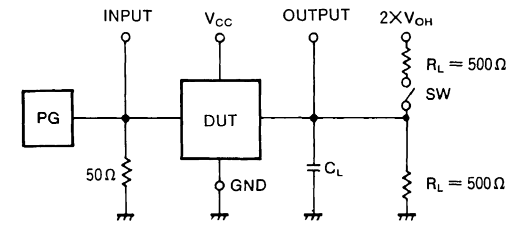
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 5)	32			26		MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time			4	12		15	ns
t_{THL}				4	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − Q)			11	23		29	ns
t_{PHL}				14	25		31	ns
t_{PLZ}	Low-level and high-level outpt disable time ($\overline{OE}$ − Q)			10	23		29	ns
t_{PHZ}				11	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − Q)			11	23		29	ns
t_{PZH}				9	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			61.3				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_W	Clock pulse width		12	3		15		ns
t_{su}	D setup time with respect to CK		10	1		13		ns
t_h	D hold time with respect to CK		5	1		6		ns

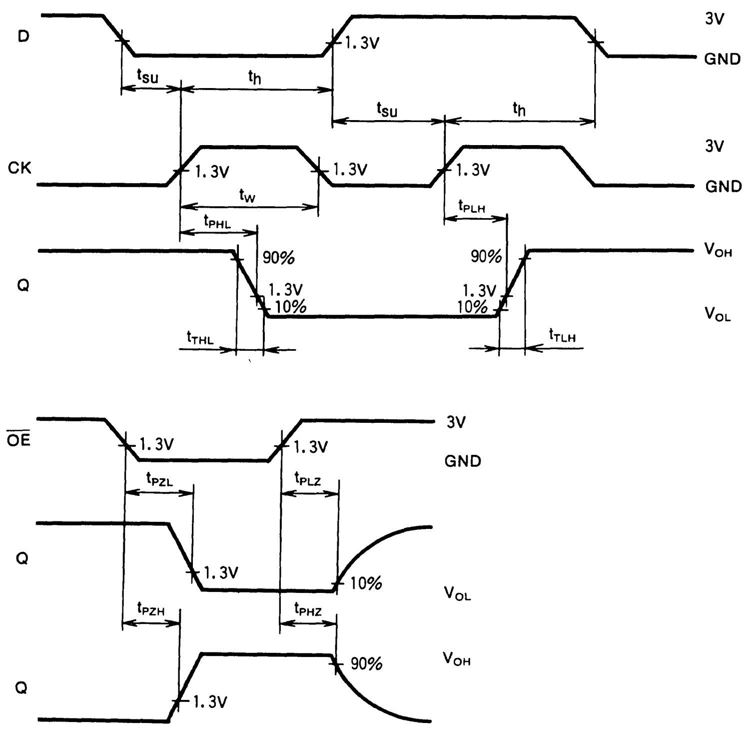
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC533-1P/FP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC533-1 is an integrated circuit chip consisting of eight 3-state output D-type latches with common-enable input and output-enable input.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

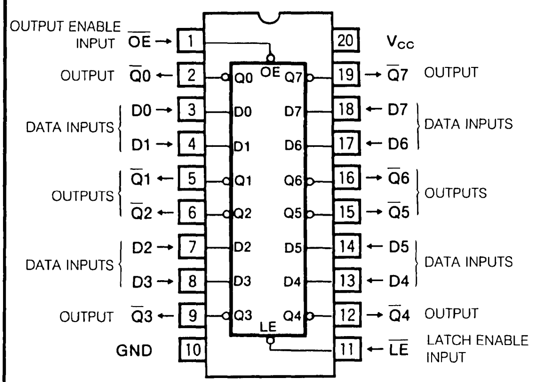
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HC533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.
The M74HC533-1 consists of eight D-type latches with latch-enable input LE and output-enable input $\overline{OE}$ common to all circuits.
When LE is high-level, the data input D appears at output $\overline{Q}$ through the latch and the $\overline{Q}$ state follows changes in the D state. When LE changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.
Even if other inputs are changed when LE is low-level, the contents stored in the latch will not be affected.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

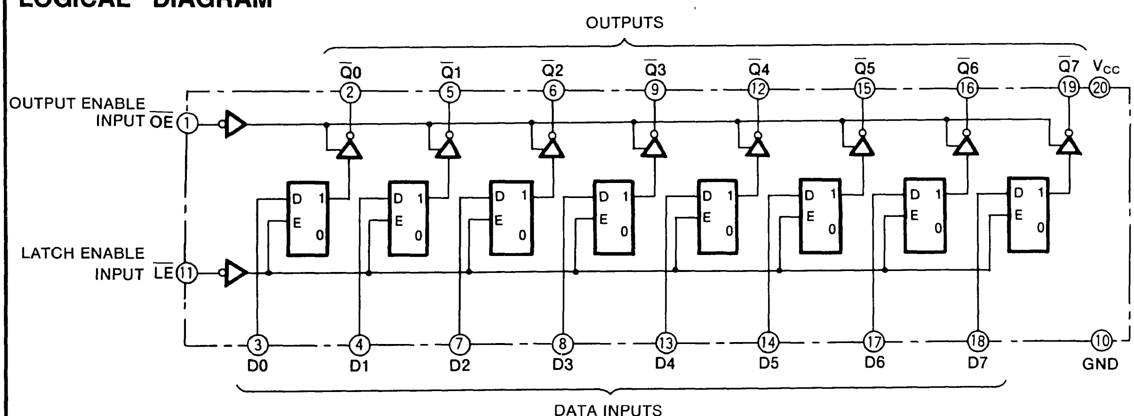
When $\overline{OE}$ is high-level, all outputs $\overline{Q}$ will become high-impedance state.
A version of the M74HC533-1 with the same pin connection and a noninverted output, the M74HC373-1, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before LE changed
Z : High impedance
X : Irrelevant

LOGICAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	°C

Note 2: M74HC533-1FP ; $T_a = -40 \sim +75°C$ and $T_a = 75 \sim 85°C$ are derated at $-7mW/°C$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85°C$)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		-40		$+85$	°C
t_r, t_f	Input rise time, fall time	$V_{CC} = 2.0V$	0		500	ns/V
		$V_{CC} = 4.5V$	0		50	
		$V_{CC} = 6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25°C Min	25°C Typ	25°C Max	$-40 \sim +85°C$ Min	$-40 \sim +85°C$ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$, V_{IH}	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$	2.0			0.1		0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1		0.1	
			$I_{OL} = 20\mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I = 6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$		6.0			-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = GND$		6.0			-0.5		-5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output	C_L = 50pF (Note 4)			10	ns
t_{THL}	transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level output				18	ns
t_{PHL}	propagation time (D − $\overline{Q}$)				18	ns
t_{PLH}	Low-to high-level and high-to low-level output				20	ns
t_{PHL}	propagation time ($\overline{LE}$ − $\overline{Q}$)				20	ns
t_{PLZ}	Low-level and high-level output disable time	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)				18	ns
t_{PZL}	Low-level and high-level output enable time	C_L = 50pF (Note 4)			20	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)				20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

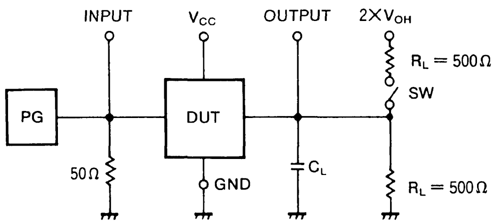
Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)	2.0		12	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		16	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − $\overline{Q}$)		2.0		30	95		120	ns
			4.5		11	19		24	
			6.0		9	16		20	
t_{PHL}			2.0		30	95		120	ns
			4.5		11	19		24	
			6.0		9	16		20	
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)		2.0		33	105		130	ns
			4.5		12	21		26	
			6.0		9	18		22	
t_{PHL}			2.0		33	105		130	ns
			4.5		12	21		26	
			6.0		10	18		22	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)		2.0		15	105		130	ns
			4.5		7	21		26	
			6.0		6	18		22	
t_{PHZ}			2.0		18	105		130	ns
			4.5		11	21		26	
			6.0		8	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)		2.0		22	105		130	ns
			4.5		9	21		26	
			6.0		7	18		22	
t_{PZH}			2.0		25	105		130	ns
			4.5		10	21		26	
			6.0		9	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				45.9				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch-enable pulse width		2.0	60	7		75		ns
			4.5	12	2		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	50	3		65		ns
			4.5	10	1		13		
			6.0	9	1		11		
t_h	D hold time with respect to $\overline{LE}$		2.0	25	−2		30		ns
			4.5	5	0		6		
			6.0	5	0		6		

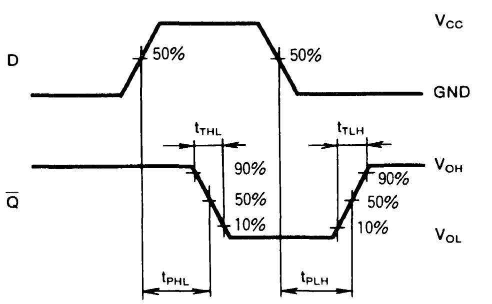
Note 4 : Test Circuit

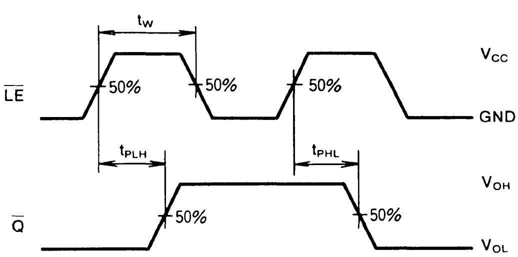


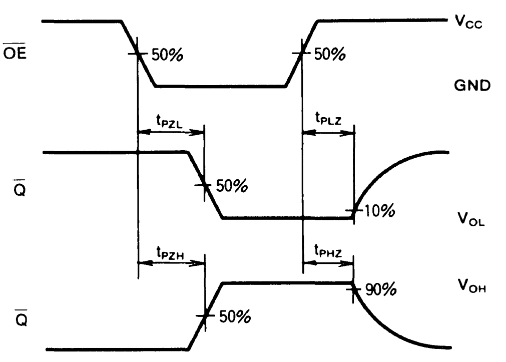
Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

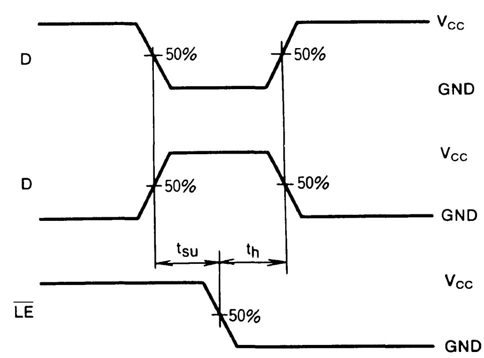
(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM









M74HCT533-1P/FP

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

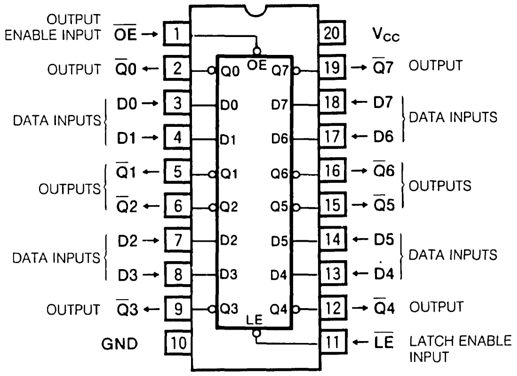
DESCRIPTION
The M74HCT533-1 is an integrated circuit chip consisting of eight 3-state output D-type latches with common-enable input and output-enable input.

FEATURES
- TTL level inputs $V_{IL}=0.8V$ max, $V_{IH}=2.0V$ min
- High-fanout 3-state output : ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed : 12ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation : 25μW/package, max ($V_{CC}=5V$, $T_a=25$℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : $T_a=-40\sim+85$℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

FUNCTION
Use of silicon gate technology allows the M74HCT533-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS533. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.
The M74HCT533-1 consists of eight D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.
When $\overline{LE}$ is high-level, the data input D appears at output $\overline{Q}$ through the latch and the $\overline{Q}$ state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

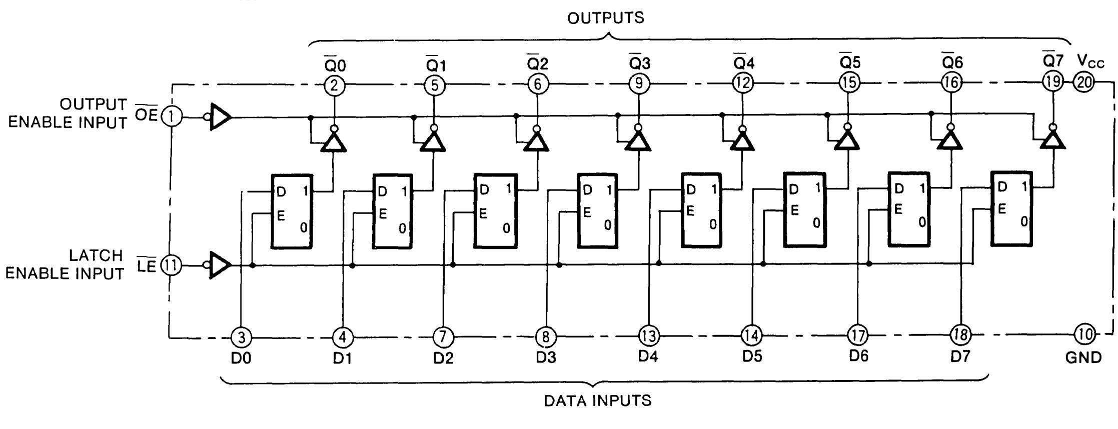
PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

Even if other inputs are changed when $\overline{LE}$ is low-level, the contents stored in the latch will not be affected.
When $\overline{OE}$ is high-level, all outputs $\overline{Q}$ will become high-impedance state.
A version of the M74HCT533-1 with the same pin connection and a non-inverted output, the M74HCT373-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65～+150	℃

Note 2 : M74HCT533-1FP : T_a=−40～+75℃ and T_a=75～85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40～+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40～+85℃ Min	−40～+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC} − 0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set to this value All others are fixed to V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − $\overline{Q}$)				20	ns
t_{PHL}					22	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				22	ns
t_{PHL}					24	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 5)			22	ns
t_{PZH}					22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

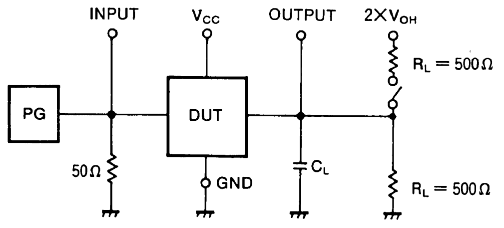
Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40～+85℃ Min	Limits −40～+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D − $\overline{Q}$)			10	21		26	ns
t_{PHL}				13	23		29	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)			12	23		29	ns
t_{PHL}				14	25		31	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)			9	23		29	ns
t_{PHZ}				12	23		29	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)			13	23		29	ns
t_{PZH}				10	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			48.1				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40～+85℃ Min	Limits −40～+85℃ Max	Unit
t_W	Latch-enable pulse width		12	2		15		ns
t_{SU}	D setup time with respect to $\overline{LE}$		10	2		13		ns
t_h	D hold time with respect to $\overline{LE}$		5	−1		6		ns

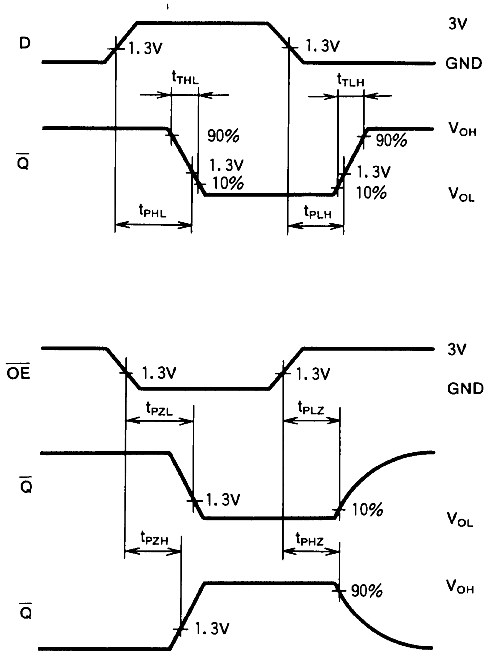
Note 5 : Test Circuit

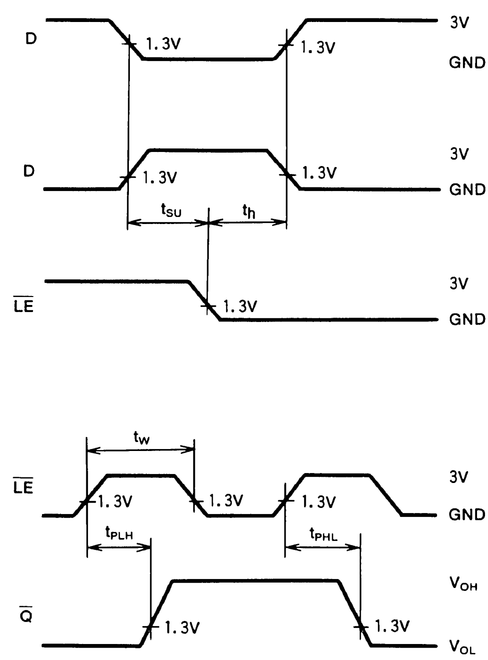


Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





MITSUBISHI
ELECTRIC

M74HC534-1P/FP

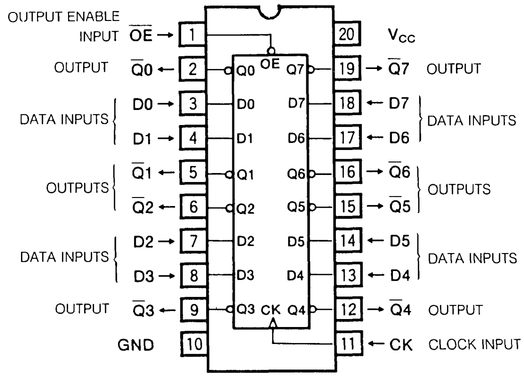
OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION
The M74HC534-1 is an integrated circuit chip consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

FEATURES
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : (Clock frequency) 80MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, Ta=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2∼6V
- Wide operating temperature range : Ta=−40∼+85℃

APPLICATION
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

FUNCTION
Use of silicon gate technology allows the M74HC534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. The M74HC534-1 consists of eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

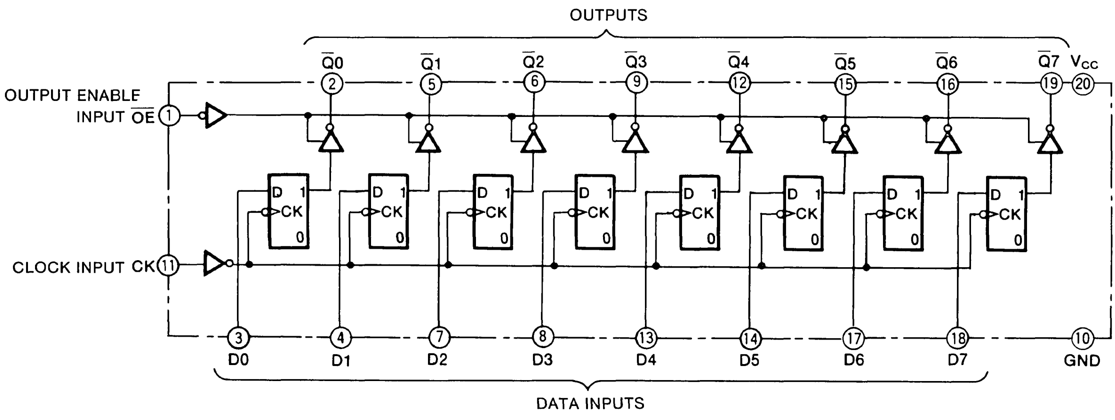
When CK changes from low-level to high-level, the signals just previously data input D is stored in the flip-flop.

When $\overline{OE}$ is low-level, the signal stored in the flip-flop will be output to $\overline{Q}$.

When $\overline{OE}$ is high-level, all outputs $\overline{Q}$ will become high impedance state. The contents stored in the flip-flop will not be affecterd even if $\overline{OE}$ changes.

A version of the M74HC534-1 with the same pin connection and a noninverted output, the M74HC374-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{CK}$ changed
Z : High impedance
X : Irrelevant
↑ : Chnage from low-to high-level
↓ : Change from high-to low-level

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2 : M74HC534-1FP : $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at -7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC} = 2.0V$	0		500	ns/V
		$V_{CC} = 4.5V$	0		50	
		$V_{CC} = 6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits 25℃			Limits $-40 \sim +85$℃		Unit
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC} = 0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$ $\lvert I_O \rvert = 20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$, V_{IH}	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$	2.0			0.1		0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1		0.1	
			$I_{OL} = 20\mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I = 6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$		6.0			-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = GND$		6.0			-0.5		-5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PHL}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PZH}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

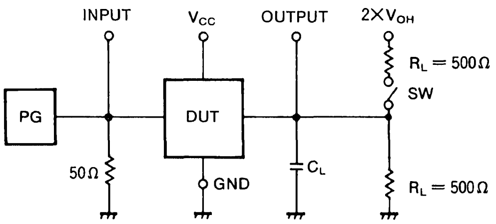
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-to high-level and high-to low-level output transition time		2.0		13	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		16	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)		2.0		35	105		130	ns
			4.5		12	21		26	
			6.0		10	18		22	
t_{PHL}			2.0		34	105		130	ns
			4.5		13	21		26	
			6.0		10	18		22	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)		2.0		16	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PHZ}			2.0		17	105		130	ns
			4.5		10	21		26	
			6.0		10	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)		2.0		22	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PZH}			2.0		27	105		130	ns
			4.5		11	21		26	
			6.0		9	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				61.6				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	60	10		75		ns
			4.5	12	3		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to CK		2.0	50	2		65		ns
			4.5	10	1		13		
			6.0	9	0		11		
t_h	D hold time with respect to CK		2.0	25	1		30		ns
			4.5	5	1		6		
			6.0	5	0		6		

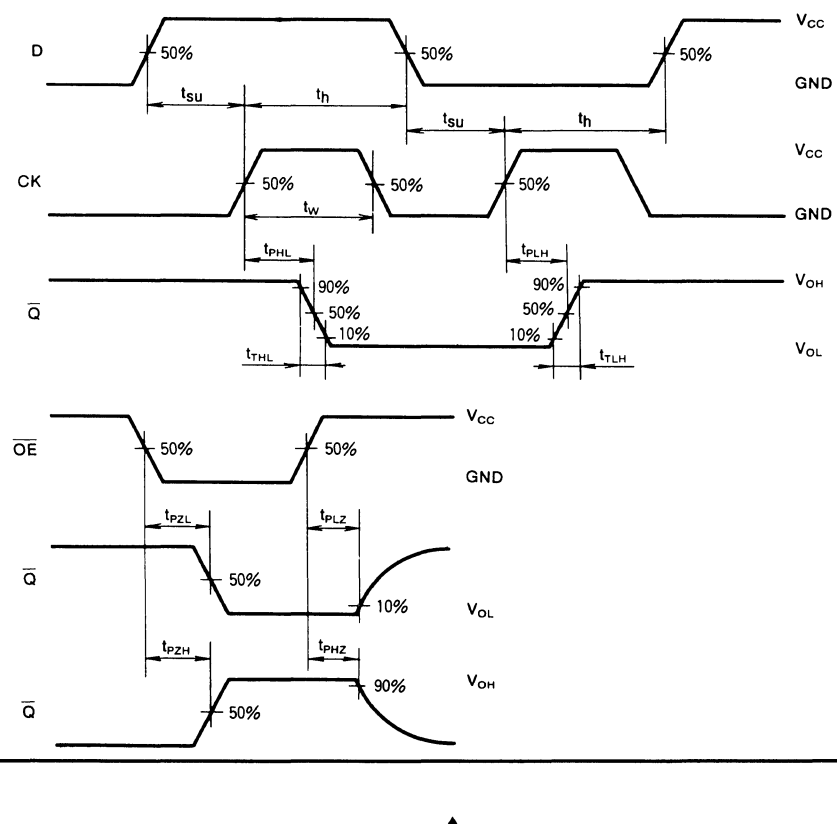
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HCT534-1P/FP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT534-1 is an integrated circuit chip consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

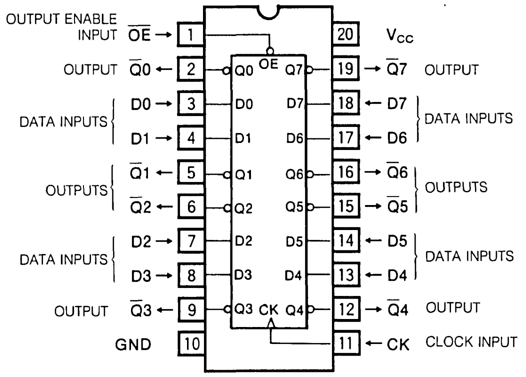
FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : (Clock frequency) 70MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40～+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

PIN CONFIGURATION (TOP VIEW)



Outline 20P4, 20P2N

FUNCTION

Use of silicon gate technology allows the M74HCT534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. When used as such, no pull-up resistors are required.

The M74HCT534-1 consists of eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

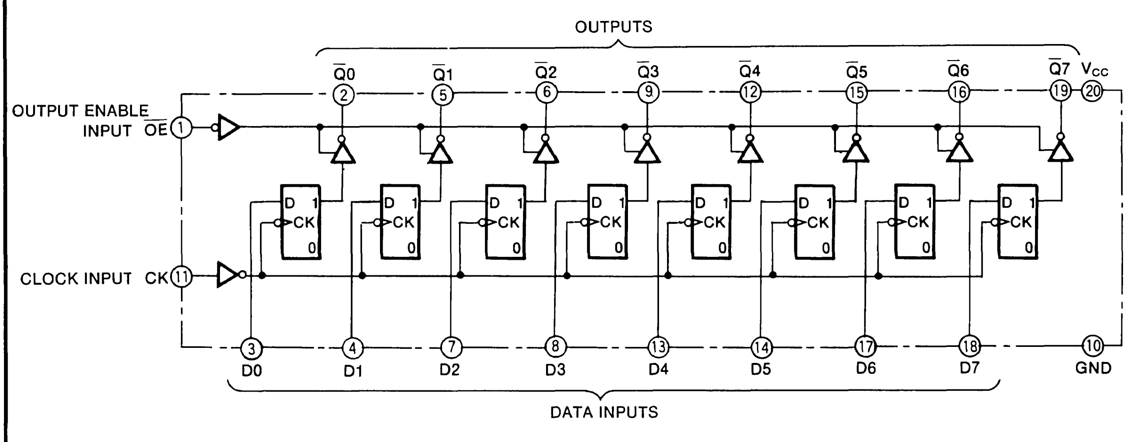
When CK changes from low-level to high-level, the signals just previously input D is stored in the flip-flop.

When $\overline{OE}$ is low-level, the signal stored in the flip-flop will be output to $\overline{Q}$.

When $\overline{OE}$ is high-level, all outputs $\overline{Q}$ will become high impedance state. The contents stored in the flip-flop will not be affecterd even if $\overline{OE}$ changes.

A version of the M74HCT534-1 with the same pin connection and a non-inverted output, the M74HCT374-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE
INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1: $\overline{Q}^0$: Output state $\overline{Q}$ before CK changed
Z : High impedance
X : Irrelevant
↑ : Change from low-to high-level
↓ : Change from high-to low-level

ABSOLUTE MAXIMUM RATINGS (T_a = −40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65～+150	℃

Note 2: M74HCT534-1FP : T_a=−40～+75℃ and T_a=75～85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40～+85℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 4.5V	0		25	ns/V
		V_{CC} = 5.5V	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	−40～+85℃ Min	−40～+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC} − 0.1V, $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3: Only one input is set to this value All others are fixed to V_{CC} or GND.

**OCTAL 3-STATE
INVERTING D-TYPE FLIP-FLOP WITH LSTTL-COMPATIBLE INPUTS**

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 5)	35			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time				22	ns
t_{PHL}	(CK − $\overline{Q}$)				24	ns
t_{PLZ}	Low-level and high-level output disable time	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)				20	ns
t_{PZL}	Low-level and high-level output enable time	C_L = 50pF (Note 5)			22	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)				22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

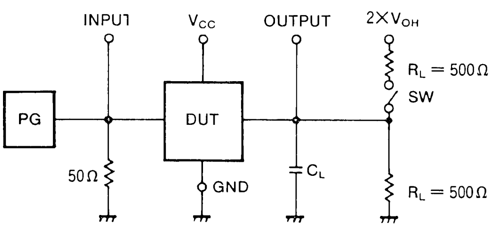
Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 5)	32			26		MHz
t_{TLH}	Low-to high-level and high-to			4	12		15	ns
t_{THL}	low-level output transition time			4	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time			12	23		29	ns
t_{PHL}	(CK − $\overline{Q}$)			13	25		31	ns
t_{PLZ}	Low-level and high-level output disable time			10	23		29	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)			12	23		29	ns
t_{PZL}	Low-level and high-level output enable time			11	23		29	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)			10	23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			61.2				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_W	Clock pulse width		12	3		15		ns
t_{su}	D setup time with respect to CK		10	1		13		ns
t_h	D hold time with respect to CK		5	1		6		ns

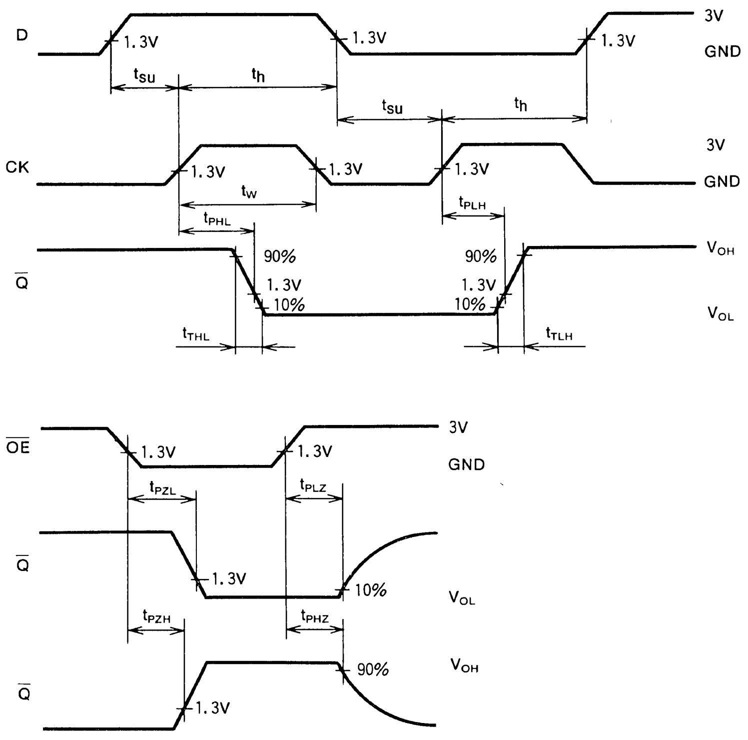
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%～90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC640-1P/FP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC640-1 is an integrated circuit chip consisting of eight bus transceivers with inverted outputs.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2∼6V
- Wide operating temperature range : T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HC640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state inverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

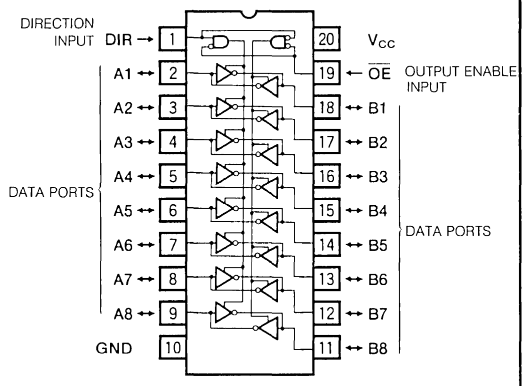
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, the B data ports are set as input terminals and the A data ports are set as output terminals. When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

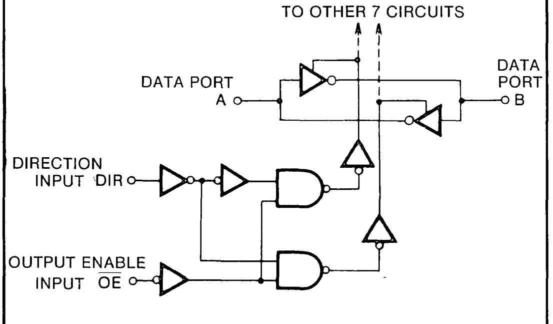
Note 1 : I : Input pin
$\overline{O}$: Output pin (inverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE INVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC640-1FP : T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\lvert I_O \rvert$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

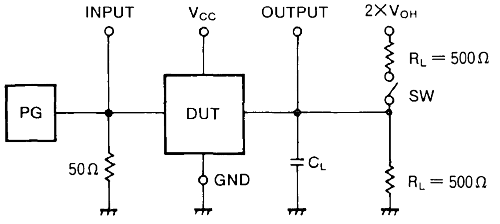
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time				15	ns
t_{PHL}	(A − B, B − A)				15	ns
t_{PLZ}	Low-level and high-level output disable time	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − A, B)				25	ns
t_{PZL}	Low-level and high-level output enable time	C_L = 50pF (Note 4)			27	ns
t_{PZH}	($\overline{OE}$ − A, B)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85°C)

Symbol	Parameter	Test conditions	V_{CC}(V)	25°C Min	25°C Typ	25°C Max	−40~+85°C Min	−40~+85°C Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)	2.0		14	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		21	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−B, B−A)		2.0		24	80		100	ns
			4.5		8	16		20	
			6.0		7	14		17	
t_{PHL}			2.0		23	80		100	ns
			4.5		9	16		20	
			6.0		7	14		17	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)		2.0		20	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}			2.0		23	140		175	ns
			4.5		12	28		35	
			6.0		11	24		30	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)		2.0		33	140		175	ns
			4.5		12	28		35	
			6.0		10	24		30	
t_{PZH}			2.0		33	140		175	ns
			4.5		12	28		35	
			6.0		10	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				52.7				pF

Note 3: C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

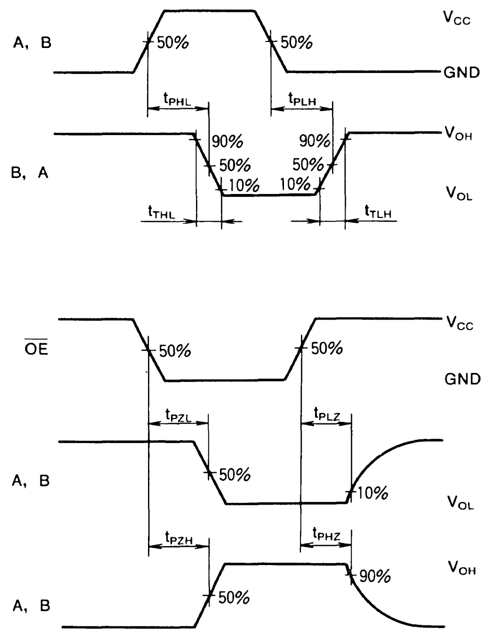
Note 4: Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT640-1P/FP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT640-1 is an integrated circuit chip consisting of eight bus transceivers with inverted outputs.

FEATURES

- TTL level input $V_{IL}=0.8V$ max $V_{IH}=2.0V$ min
- High-fanout 3-state output : ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed : 10ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation : 25μW/package, max ($V_{CC}=5V$, $T_a=25$℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : $T_a=-40\sim+85$℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

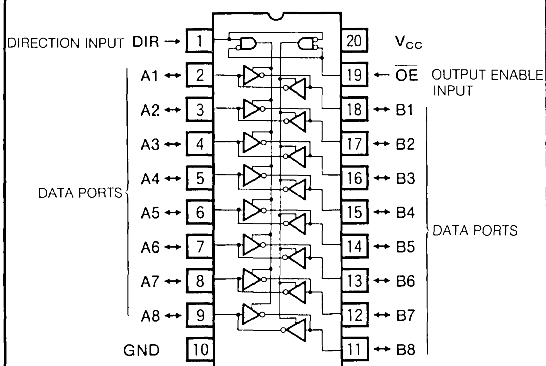
Use of silicon gate technology allows the M74HCT640-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS640. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.
As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS Used as such, no pull-up resistors are required.
Two buffers with 3-state inverted outputs have their inputs and outputs connected and can be used as buffers in both directions
The input/output direction is controlled by direction input DIR.
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals.
When DIR is low-level, the B data ports are set as input terminals and the A data ports are set as output terminals.
When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

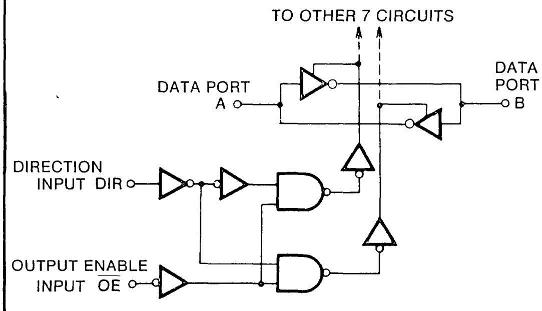
Note 1 : I : Input pin
$\overline{O}$: Output pin (inverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE
INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2: M74HCT640-1FP: $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at -7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\|I_O\| = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\|I_O\| = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, V_O = GND				-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3: Only one input is set at this value All other inputs are fixed at V_{CC} or GND

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25$℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L = 50pF$ (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)				17	ns
t_{PHL}					19	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)	$C_L = 5pF$ (Note 5)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)	$C_L = 50pF$ (Note 5)			29	ns
t_{PZH}					29	ns

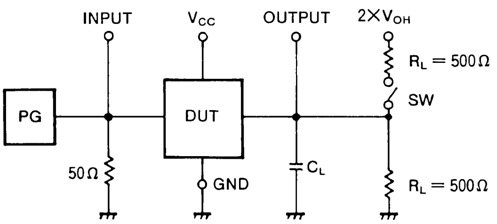
OCTAL 3-STATE
INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)			8	18		23	ns
t_{PHL}				11	20		25	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)			10	30		38	ns
t_{PHZ}				13	30		38	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)			17	30		38	ns
t_{PZH}				12	30		38	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			52.0				pF

Note 4 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

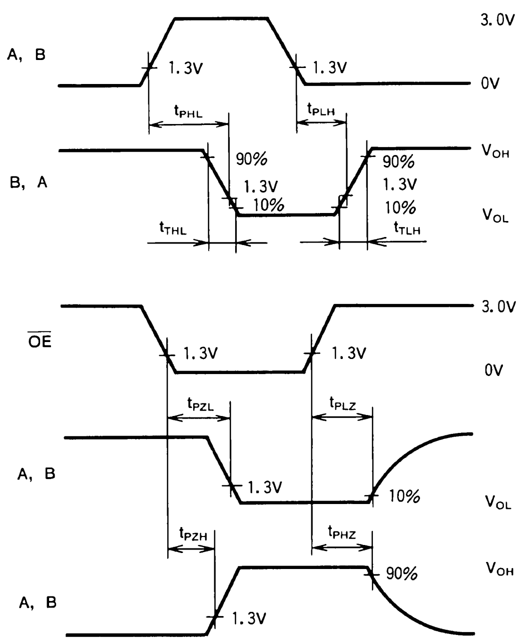
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC643-1P/FP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643-1 is an integrated circuit chip consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 8ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HC643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state inverted and noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

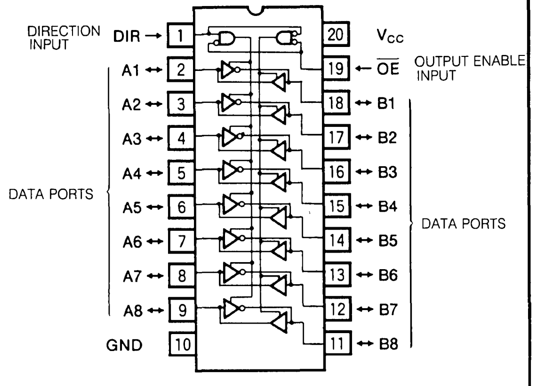
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, the B data ports are set as input terminals and the A data ports are set as output terminals. When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

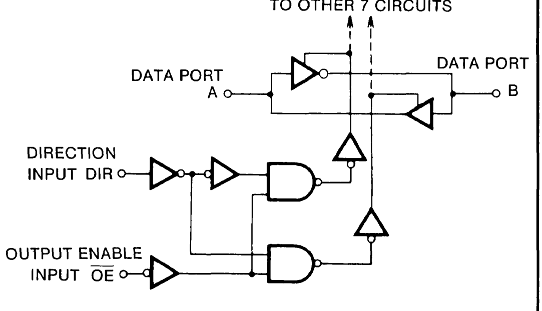
Note 1 : I : Input pin
O : Output pin (noninverted output)
$\overline{O}$: Output pin (inverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2: M74HC643-1FP : T_a=−40∼+75℃ and T_a=75∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			.5.0		50.0	μA

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

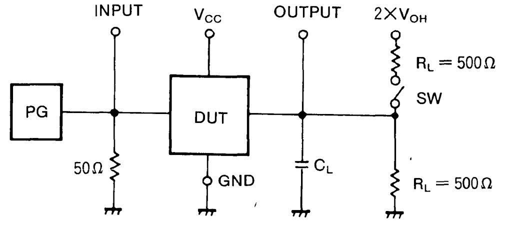
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time				16	ns
t_{PHL}	(A − B, B − A)				16	ns
t_{PLZ}	Low-level and high-level output disable time	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}	($\overline{OE}$ − A, B)				25	ns
t_{PZL}	Low-level and high-level output enable time	C_L = 50pF (Note 4)			27	ns
t_{PZH}	($\overline{OE}$ − A, B)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)	2.0		17	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{THL}			2.0		24	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A−B, B−A)		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PHL}			2.0		25	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PLZ}	Low-level andhigh-level output disable time ($\overline{OE}$ − A, B)		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}			2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		10	24		30	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)		2.0		35	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
t_{PZH}			2.0		36	140		175	ns
			4.5		13	28		35	
			6.0		10	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				53.5				pF

Note 3 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit

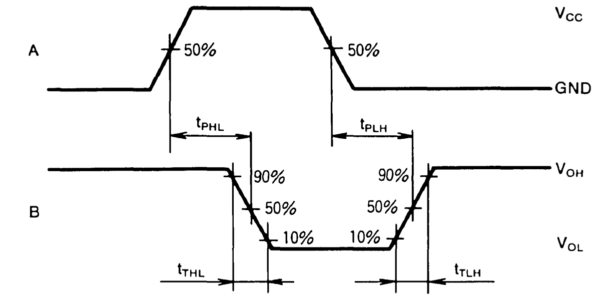


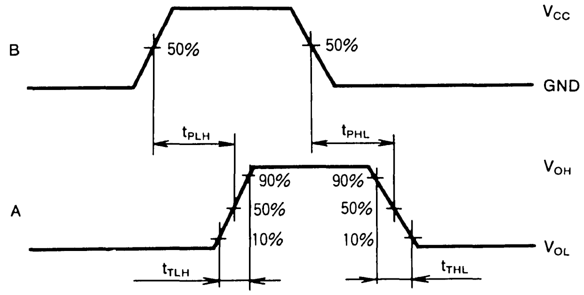
Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

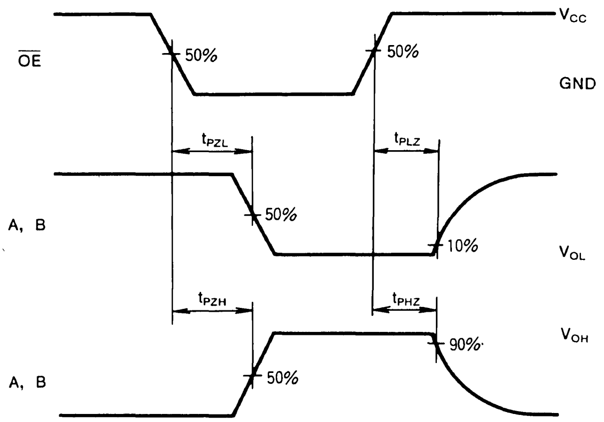
(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

MITSUBISHI ELECTRIC

TIMING DIAGRAM







M74HCT643-1P/FP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT643-1 is an integrated circuit chip consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HCT643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. Used as such, no pull-up resistors are required.

Two buffers with 3-state inverted and noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

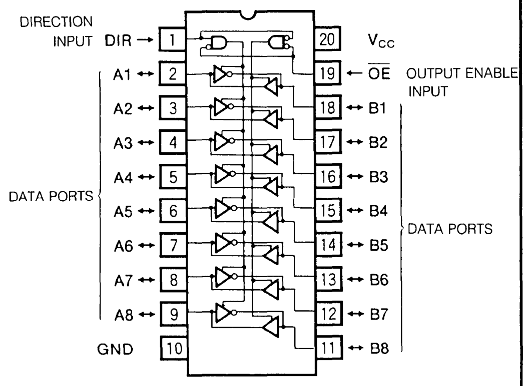
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, the B are set as input terminals and the A are set as output terminals. When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

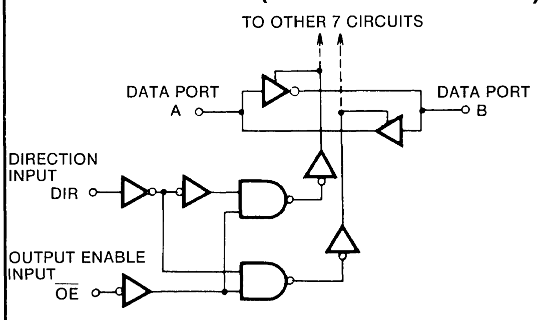
Note 1 : I : Input pin
O : Output pin (noninverted output)
$\overline{O}$: Output pin (inverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



MITSUBISHI ELECTRIC

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2 : M74HCT643-1FP : $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at -7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\lvert I_O \rvert = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC}-0.1V$, $\lvert I_O \rvert = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = GND$				-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = GND$				-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum static supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value All other inputs are fixed at V_{CC} or GND

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25$℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L = 50pF$ (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)				18	ns
t_{PHL}					20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)	$C_L = 5pF$ (Note 5)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)	$C_L = 50pF$ (Note 5)			29	ns
t_{PZH}					29	ns

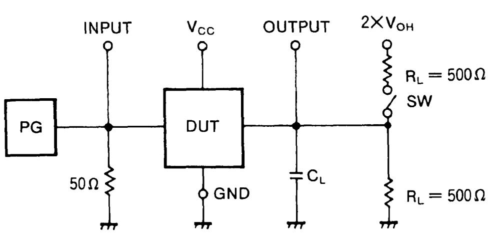
OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40～+85℃		
			Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)			10	19		24	ns
t_{PHL}				12	21		26	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)			10	30		38	ns
t_{PHZ}				14	30		38	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)			17	30		38	ns
t_{PZH}				13	30		38	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			55.9				pF

Note 4 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

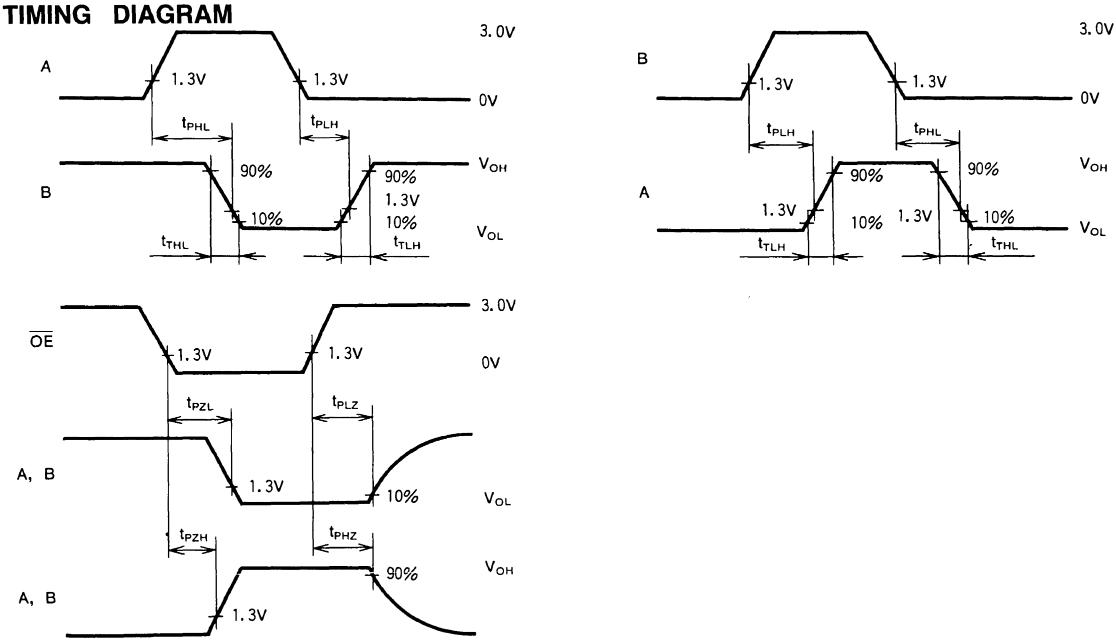
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%～90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HC645-1P/FP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC645-1 is an integrated circuit chip consisting of eight bus transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2∼6V
- Wide operating temperature range : T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HC645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

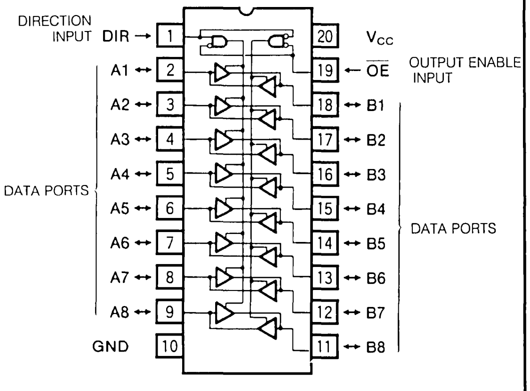
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, B will become input terminals and A will become output terminals. When output enable input $\overline{OE}$ is high-level, A and B will become high impedance state and they and they are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

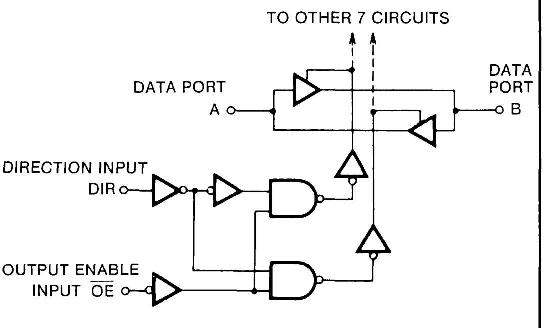
Note 1 : I : Input pin
O : Output pin (noninverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a=−40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2: M74HC645-1FP: T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a=−40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC}=4.5V	0		50	
		V_{CC}=6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits 25℃			−40~+85℃		Unit
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O| = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}−0.1V, |I_O| =20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I=V_{IL}, V_{IH}	I_{OH}=−20μA	2.0	1.9			1.9		V
			I_{OH}=−20μA	4.5	4.4			4.4		
			I_{OH}=−20μA	6.0	5.9			5.9		
			I_{OH}=−24mA	4.5	3.83			3.70		
V_{OL}	Low-level output current	V_I=V_{IH}, V_{IL}	I_{OL}=20μA	2.0			0.1		0.1	V
			I_{OL}=20μA	4.5			0.1		0.1	
			I_{OL}=20μA	6.0			0.1		0.1	
			I_{OL}=24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I=6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I=0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I=V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I=V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Static supply current	V_I=V_{CC}, GND, I_O=0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

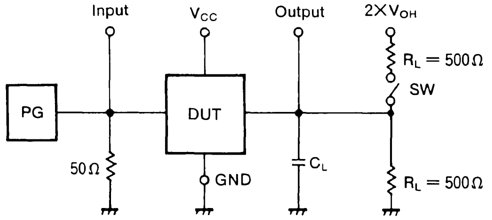
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—B, B—A)				16	ns
t_{PHL}					16	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$—A, B)	C_L= 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$—A, B)	C_L=50pF (Note 4)			27	ns
t_{PZH}					27	ns

SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)	2.0		16	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{THL}			2.0		23	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—B, B—A)		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PHL}			2.0		27	85		105	ns
			4.5		10	17		21	
			6.0		8	14		18	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$—A, B)		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}			2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		11	24		30	
t_{PZL}	Low-level and high-level output enble time ($\overline{OE}$—A, B)		2.0		32	140		175	ns
			4.5		11	28		35	
			6.0		10	24		30	
t_{PZH}			2.0		33	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				56.3				pF

Note 3 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

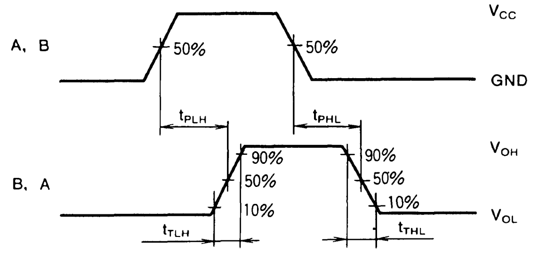
Note 4 : Test Circuit

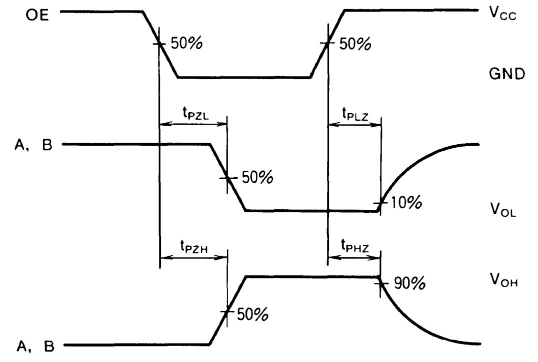


Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM





M74HCT645-1P/FP

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT645-1 is an integrated circuit chip consisting of eight bus transceivers with noninverted outputs.

FEATURES

- TTL level input V_{IL}=0.8V max V_{IH}=2.0V min
- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed 11ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range : T_a=−40～+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HCT645-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS645. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. Used as such, no pull-up resistors are required.

Two buffers with 3-state noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

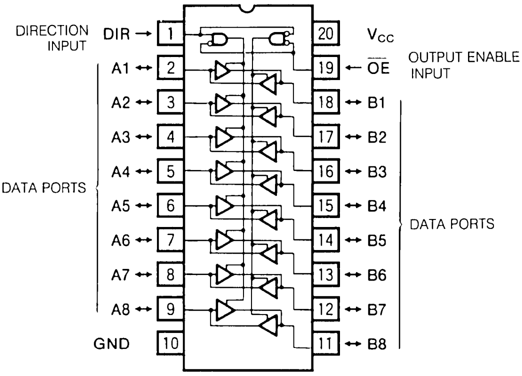
When DIR is high-level, the A data ports will become input terminals and the B data ports will become output terminals. When DIR is low-level, the data ports B are set as input terminals and the data ports A are set as output terminals. When output enable input $\overline{OE}$ is high-level, A and B both become high impedance state and they are separated.

FUNCTION TABLE (Note 1)

Inputs		Data ports	
$\overline{OE}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

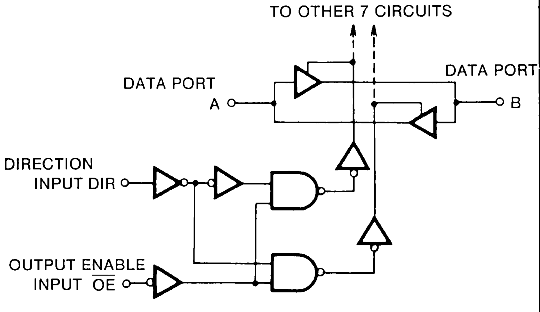
Note 1 : I : Input pin
O : Output pin (noninverted output)
Z : High impedance state (A and B are separated)
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE
NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2: M74HCT645-1FP: $T_a = -40 \sim +75$℃ and $T_a = 75 \sim 85$℃ are derated at $-7mW/$℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	25℃ Typ	25℃ Max	$-40 \sim +85$℃ Min	$-40 \sim +85$℃ Max	Unit
V_{IH}	High-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\lvert I_O \rvert = 20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\lvert I_O \rvert = 20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OH} = -20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH} = -24mA$, $V_{CC} = 4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$, V_{IL}	$I_{OL} = 20\mu A$			0.1		0.1	V
			$I_{OL} = 24mA$, $V_{CC} = 4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I = V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = GND$				-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}$, V_{IL}, $V_O = GND$				-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	$V_I = 2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3: Only one input is set at this value All other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25$℃)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L = 50pF$ (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)				18	ns
t_{PHL}					20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)	$C_L = 5pF$ (Note 5)			27	ns
t_{PHZ}					27	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)	$C_L = 50pF$ (Note 5)			29	ns
t_{PZH}					29	ns

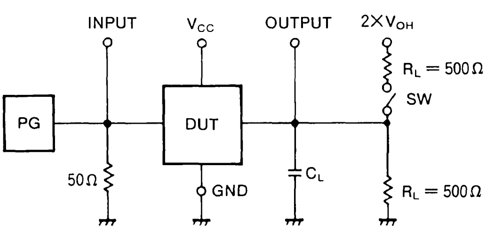
OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40～+85℃ Min	Limits −40～+85℃ Max	Unit
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 5)		5	12		15	ns
t_{THL}				5	12		15	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A − B, B − A)			9	19		24	ns
t_{PHL}				12	21		26	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − A, B)			10	30		38	ns
t_{PHZ}				13	30		38	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − A, B)			12	30		38	ns
t_{PZH}				11	30		38	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)			62.0				pF

Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver) The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

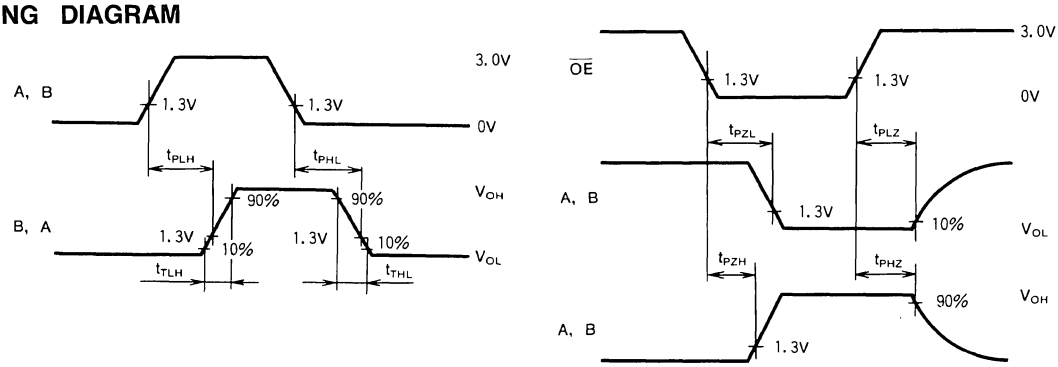
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%～90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC841-1P/FP

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC841-1 is a semiconductor integrated circuit consisting of ten 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2∼6V
- Wide operating temperature range: T_a=−40∼+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC841-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LSTTL.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC841-1 consists of ten D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

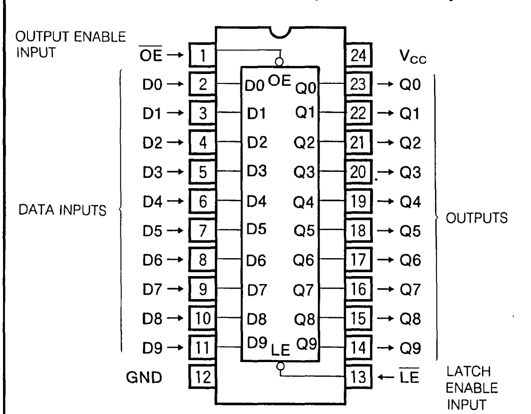
When $\overline{LE}$ is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

A version of the M74HC841-1 with the same pin connections and an inverted output, the M74HC842-1, is also available.

PIN CONFIGURATION (TOP VIEW)



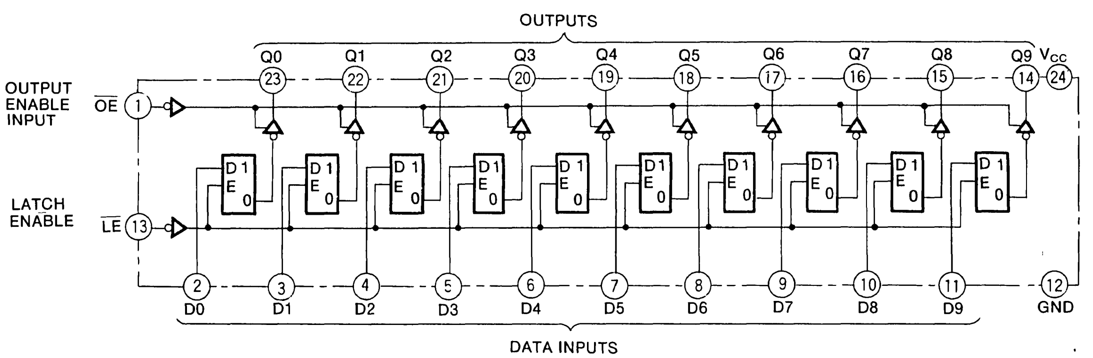
Outline 24P4D 24P2

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0: Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC841-1FP , T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40∼+85℃ Min	−40∼+85℃ Max	Unit
V_{IH}	High-level input voltnge	V_O = 0.1V, V_{CC} − 0.1V, $\|I_O\|$ = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, $\|I_O\|$ = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltnge	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				17	ns
t_{PHL}					17	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			90		115	ns
			4.5			18		23	
			6.0			15		20	
t_{PHL}			2.0			90		115	ns
			4.5			18		23	
			6.0			15		20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHL}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHZ}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PZH}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

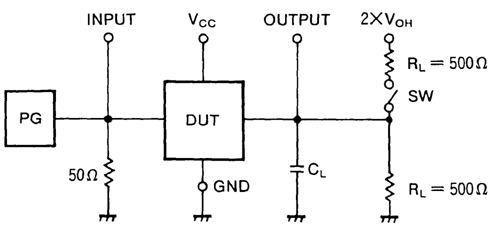
MITSUBISHI ELECTRIC

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	Latch enable pulse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to $\overline{LE}$		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		

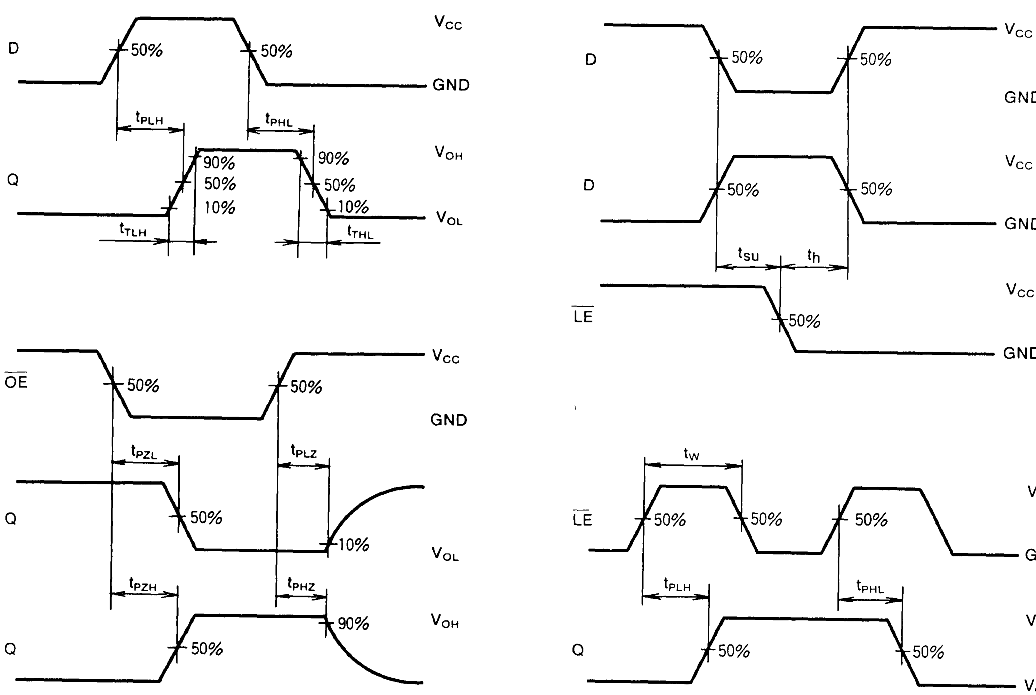
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

TIMING DIAGRAM



M74HCT841-1P/FP

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT841-1 is a semiconductor integrated circuit consisting of ten 3-state output D-type latches with common latch-enable input and output-enable input.

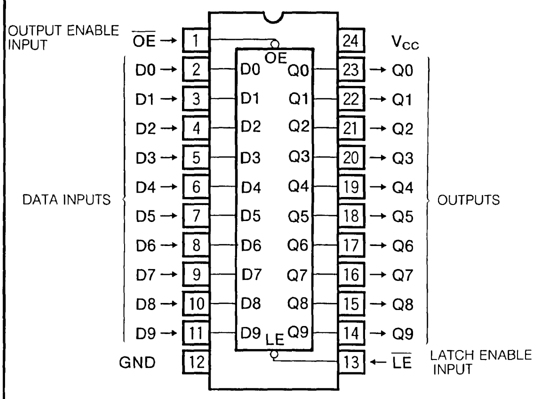
FEATURES

- TTL level inputs $V_{IL}=0.8V$ max, $V_{IH}=2.0V$ min
- High-fanout 3-state output: ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed: 11ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation: 25μW/package, max ($V_{CC}=5V$, $T_a=25℃$, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range: $T_a=-40\sim+85℃$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D
24P2

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT841-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LSTTL.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT841-1 consists of ten D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

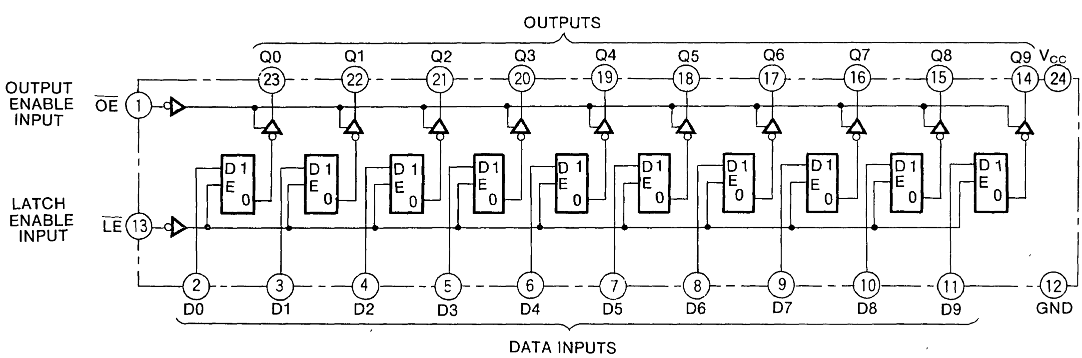
When $\overline{LE}$ is high, the data at input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

A version of the M74HCT841-1 with the same pin connections and an inverted output, the M74HCT842-1, is also available.

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q_0: Output state Q before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Not 2)	500	mW
Tstg	Storage temperature range		$-65 \sim +150$	℃

Note 2 : M74HCT841-1FP, $T_a = -40 \sim +80$℃ and $T_a = 80 \sim 85$℃ are derated at -7mW/℃.

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Ambient operating temperature		-40		$+85$	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	Typ	Max	−40~+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$, $\|I_O\|=20\mu A$		2.0			2.0		V
V_{IL}	Low-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$, $\|I_O\|=20\mu A$				0.8		0.8	V
V_{OH}	High-level output voltage	$V_I=V_{IL}$	$I_{OH}=-20\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$		V
			$I_{OH}=-24mA$, $V_{CC}=4.5V$	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I=V_{IH}$, V_{IL}	$I_{OL}=20\mu A$			0.1		0.1	V
			$I_{OL}=24mA$, $V_{CC}=4.5V$			0.44		0.53	
I_{IH}	High-level input current	$V_I=V_{CC}$				0.1		1.0	μA
I_{IL}	Low-level input current	$V_I=GND$				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=V_{CC}$				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=GND$				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	$V_I=V_{CC}$, GND, $I_O=0\mu A$				5.0		50.0	μA
ΔI_{CC}	Maximum quiescent supply current	$V_I=2.4V$, $0.4V$ (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25℃$)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L=50pF$ (Note 5)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				19	ns
t_{PHL}					21	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				22	ns
t_{PHL}					24	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	$C_L=5pF$ (Note 5)			20	ns
t_{PHZ}					20	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	$C_L=50pF$ (Note 5)			22	ns
t_{PZH}					22	ns

SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_a=-40\sim+85℃$)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Typ	Max	−40~+85℃ Min	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L=50pF$ (Note 5)			12		15	ns
t_{THL}					12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				20		25	ns
t_{PHL}					22		28	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				23		29	ns
t_{PHL}					25		31	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)				23		29	ns
t_{PHZ}					23		29	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)				23		29	ns
t_{PZH}					23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}=V_{CC}$			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)							pF

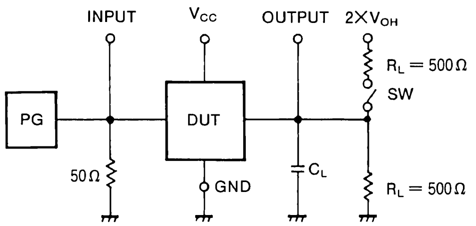
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D=C_{PD}\cdot V_{CC}^2\cdot f_I+I_{CC}\cdot V_{CC}$

10-BIT 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		12			15		ns
t_{su}	D setup time with respect to $\overline{LE}$		10			13		ns
t_h	D hold time with respect to $\overline{LE}$		5			6		ns

Note 4 : Test Circuit

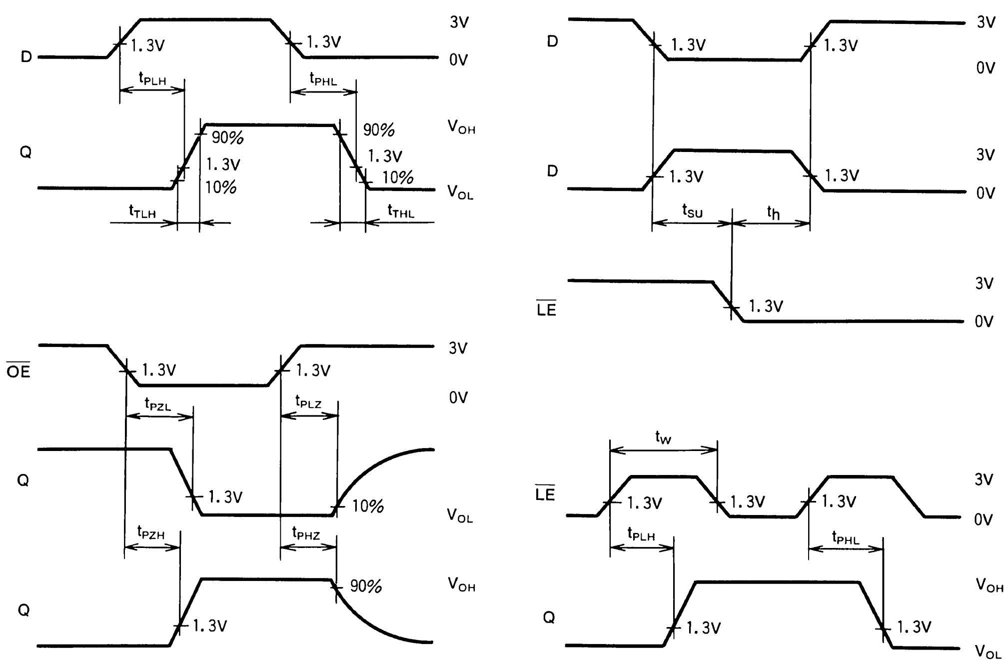


Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 3ns, t_f = 3ns

(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance

TIMING DIAGRAM



M74HC842-1P/FP

10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC842-1 is a semiconductor integrated circuit consisting of ten 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed: 10ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC842-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LSTTL.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC842-1 consists of ten D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

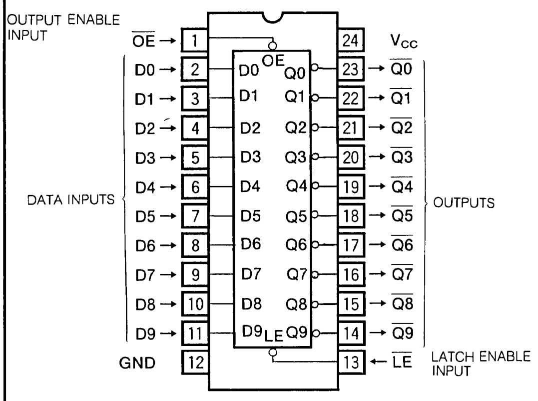
When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$ When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

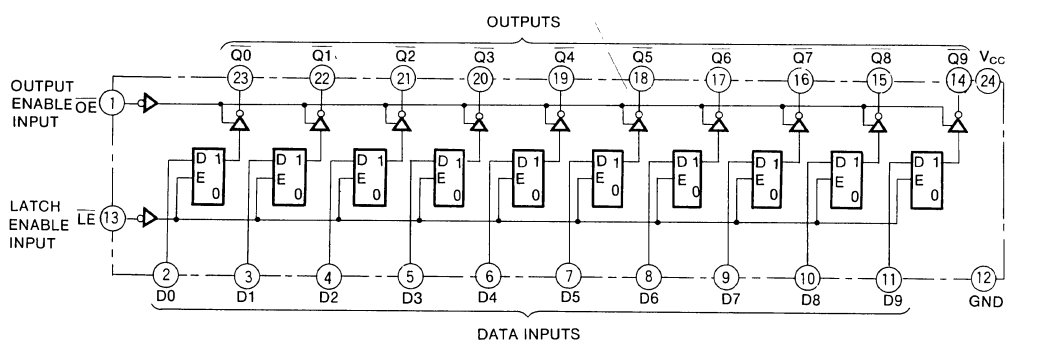
A version of the M74HC842-1 with the same pin connections and a noninverted output, the M74HC841-1, is also available.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D 24P2

LOGIC DIAGRAM



10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	H
L	H	L	L
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		$-65 \sim +150$	℃

Note 2 : M74HC842-1FP , $T_a = -40 \sim +80$℃ and $T_a = 80 \sim 85$℃ are derated at -7mW/℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		-40		$+85$	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 2.0V$	0		500	ns/V
		$V_{CC} = 4.5V$	0		50	
		$V_{CC} = 6.0V$	0		30	

10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40～+85℃ Min	Max	Unit
V_{IH}	High-level input voltnge	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\|I_O\| = 20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O = 0.1V$, $V_{CC} - 0.1V$, $\|I_O\| = 20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}, V_{IH}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4		
			$I_{OH} = -20\mu A$	6.0	5.9			5.9		
			$I_{OH} = -24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltnge	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20\mu A$	2.0			0.1		0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1		0.1	
			$I_{OL} = 20\mu A$	6.0			0.1		0.1	
			$I_{OL} = 24mA$	4.5			0.44		0.53	
I_{IH}	High-level inputcurrent	$V_I = 6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = 0V$		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}, V_{IL}, V_O = V_{CC}$		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}, V_{IL}, V_O = GND$		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$, GND, $I_O = 0\mu A$		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25℃$)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L = 50pF$ (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				18	ns
t_{PHL}					18	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	$C_L = 5pF$ (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)	$C_L = 50pF$ (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

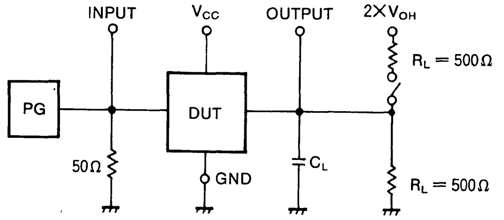
Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40~+85℃ Min	Limits −40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)		2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PHL}			2.0			95		120	ns
			4.5			19		24	
			6.0			16		20	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHL}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PHZ}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)		2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
t_{PZH}			2.0			105		130	ns
			4.5			21		26	
			6.0			18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula.
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40~+85℃ Min	Limits −40~+85℃ Max	Unit
t_W	Latch enable pulse width		2.0	60			75		ns
			4.5	12			15		
			6.0	10			13		
t_{SU}	D setup time with respect to $\overline{LE}$		2.0	50			65		ns
			4.5	10			13		
			6.0	9			11		
t_h	D hold time with respect to $\overline{LE}$		2.0	25			30		ns
			4.5	5			6		
			6.0	5			6		

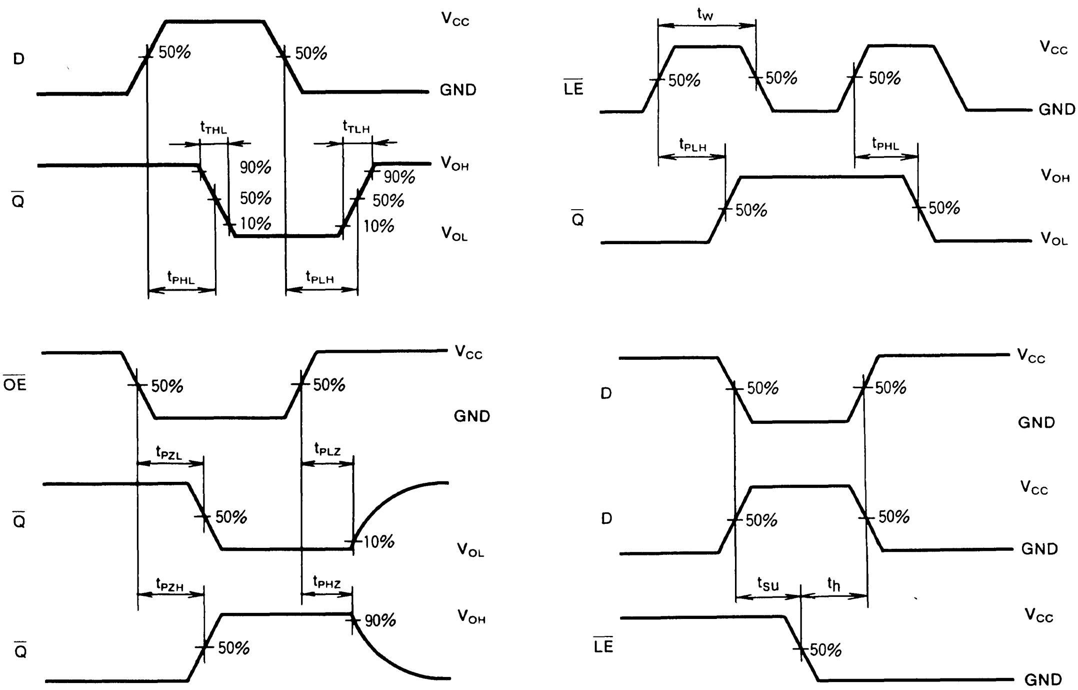
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 3ns$, $t_f = 3ns$
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74HCT842-1P/FP

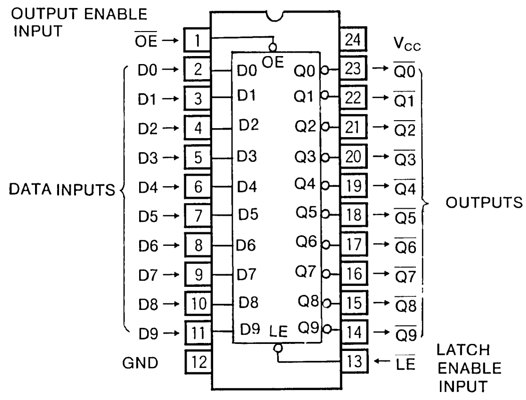
10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

DESCRIPTION

The M74HCT842-1 is a semiconductor integrated circuit consisting of ten 3-state output D-type latches with common latch-enable input and output-enable input.

FEATURES

- TTL level inputs $V_{IL}=0.8V$ max, $V_{IH}=2.0V$ min
- High-fanout 3-state output: ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed: 12ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation: 25μW/package, max ($V_{CC}=5V$, $T_a=25$℃, quiescent state)
- Capable of driving 60 74LSTTL loads
- Wide operating temperature range· $T_a=-40\sim+85$℃



Outline 24P4D 24P2

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HCT842-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LSTTL.

The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

As the inputs are TTL level, the device can be used as a level converter from LSTTL to high-speed CMOS. In that case, no pull-up resistors are required.

The M74HCT842-1 contains of ten D-type latches with latch-enable input $\overline{LE}$ and output-enable input $\overline{OE}$ common to all circuits.

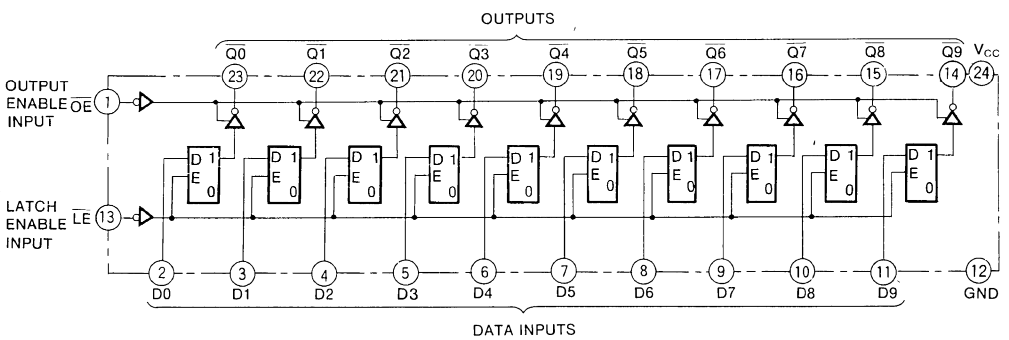
When $\overline{LE}$ is high, the signals of data input D will go through the latch and be output to inverted output $\overline{Q}$. When the state of D changes, the state of $\overline{Q}$ will also change. When $\overline{LE}$ changes from high-level to low-level, the data existing immediatry prior to the change at D will be stored in the latch

Even if other inputs are changed when $\overline{LE}$ is low, the contents stored in the latch will not be affected .

When $\overline{OE}$ is high, all outputs $\overline{Q}$ will become high-impedance state.

A version of the M74HCT842-1 with the same pin connections and a noninverted output, the M74HCT841-1, is also available.

LOGIC DIAGRAM



10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
L	H	H	H
L	H	L	L
L	L	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}_0$: Output state $\overline{Q}$ before $\overline{LE}$ changed
Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40\sim+85$℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5\sim+7.0$	V
V_I	Input voltage		$-0.5\sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5\sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current per output pin		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Not 2)	500	mW
Tstg	Storage temperature range		−65～+150	℃

Note 2 : M74HCT842-1FP, $T_a = -40\sim+80$℃ and $T_a = 80\sim85$℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS ($T_a = -40\sim+85$℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	$V_{CC} = 4.5V$	0		25	ns/V
		$V_{CC} = 5.5V$	0		15	

10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40～+85℃ Min	Limits −40～+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA		2.0			2.0		V
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA				0.8		0.8	V
V_{OH}	High-level output voltage	V_I = V_{IL}	I_{OH} = −20μA	V_{CC}−0.1			V_{CC}−0.1		V
			I_{OH} = −24mA, V_{CC} = 4.5V	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA			0.1		0.1	V
			I_{OL} = 24mA, V_{CC} = 4.5V			0.44		0.53	
I_{IH}	High-level input current	V_I = V_{CC}				0.1		1.0	μA
I_{IL}	Low-level input current	V_I = GND				−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}				0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND				−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA				5.0		50.0	μA
$\triangle I_{CC}$	Maximum quiescent supply current	V_I = 2.4V, 0.4V (Note 3)				2.7		2.9	mA

Note 3 : Only one input is set at this value and all other inputs are fixed at V_{CC} or GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 5)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				20	ns
t_{PHL}	output propagation time (D − $\overline{Q}$)				22	ns
t_{PLH}	Low-level to high-level and high-level to low-level				22	ns
t_{PHL}	output propagation time ($\overline{LE}$ − $\overline{Q}$)				24	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5 pF (Note 5)			20	ns
t_{PHZ}	($\overline{OE}$ − $\overline{Q}$)				20	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 5)			22	ns
t_{PZH}	($\overline{OE}$ − $\overline{Q}$)				22	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −40～+85℃)

Symbol	Parameter	Test conditions	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40～+85℃ Min	Limits −40～+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 5)			12		15	ns
t_{THL}					12		15	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				21		26	ns
t_{PHL}					23		29	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − $\overline{Q}$)				23		29	ns
t_{PHL}					25		31	ns
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				23		29	ns
t_{PHZ}					23		29	ns
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − $\overline{Q}$)				23		29	ns
t_{PZH}					23		29	ns
C_I	Input capacitance				10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}			15		15	pF
C_{PD}	Power dissipation capacitance (Note 4)							pF

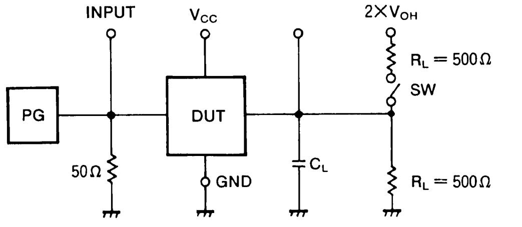
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

10-BIT 3-STATE INVERTING D-TYPE TRANSPARENT LATCH WITH LSTTL-COMPATIBLE INPUTS

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			Min	Typ	Max	Min	Max	
t_W	Latch enable pulse with		12			15		ns
t_{SU}	D setup time with respect to $\overline{LE}$		10			13		ns
t_h	D hold time with respect to $\overline{LE}$		5			6		ns

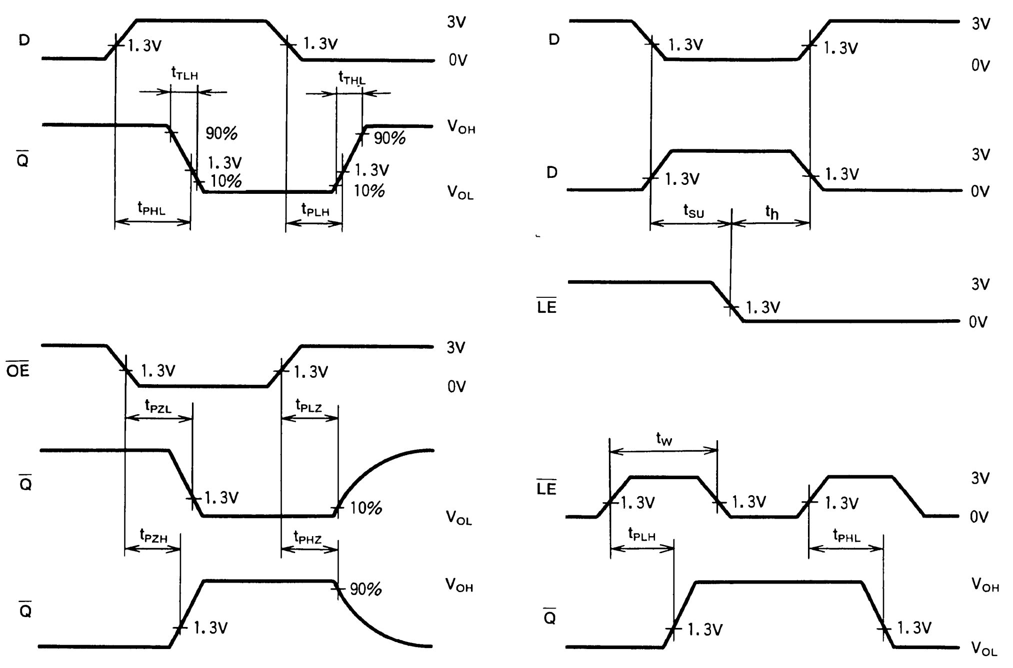
Note 5 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) t_r = 3ns, t_f = 3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



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