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MDX-CPU3

DATA SHEET

PRELIMINARY

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1. FEATURES

PRELIMINARY

[] Utilizes the powerful Z80A Microprocessor.

[] A single 28 Pin socket which may be strapped to accept any of the following industry-standard memory devices.

EPROM	ROM
MK2716 (2K x 8)	MK34000 (2K x 8)
2732 (4K x 8)	
2764 (8K x 8)	MK37000 (8K x 8)
	MK38000 (32K x 8)

[] 64K x 8 of dynamic memory capacity.

[] 2K to 32K of ROM memory capacity.

[] Flexible memory decoding of ROM memory on any 2k boundary.

[] Phantom ROM capability.

[] Bidirectional address, data and control busses to permit external DMA.

[] 8 bit output port with handshake for interfacing to a Centronics printer.

[] Full handshake serial RS232 I/O Port.

[] Software programable baud rate.

[] Power on reset logic.

[] STD-Z80 BUS compatible.

[] 2 timer channel outputs.

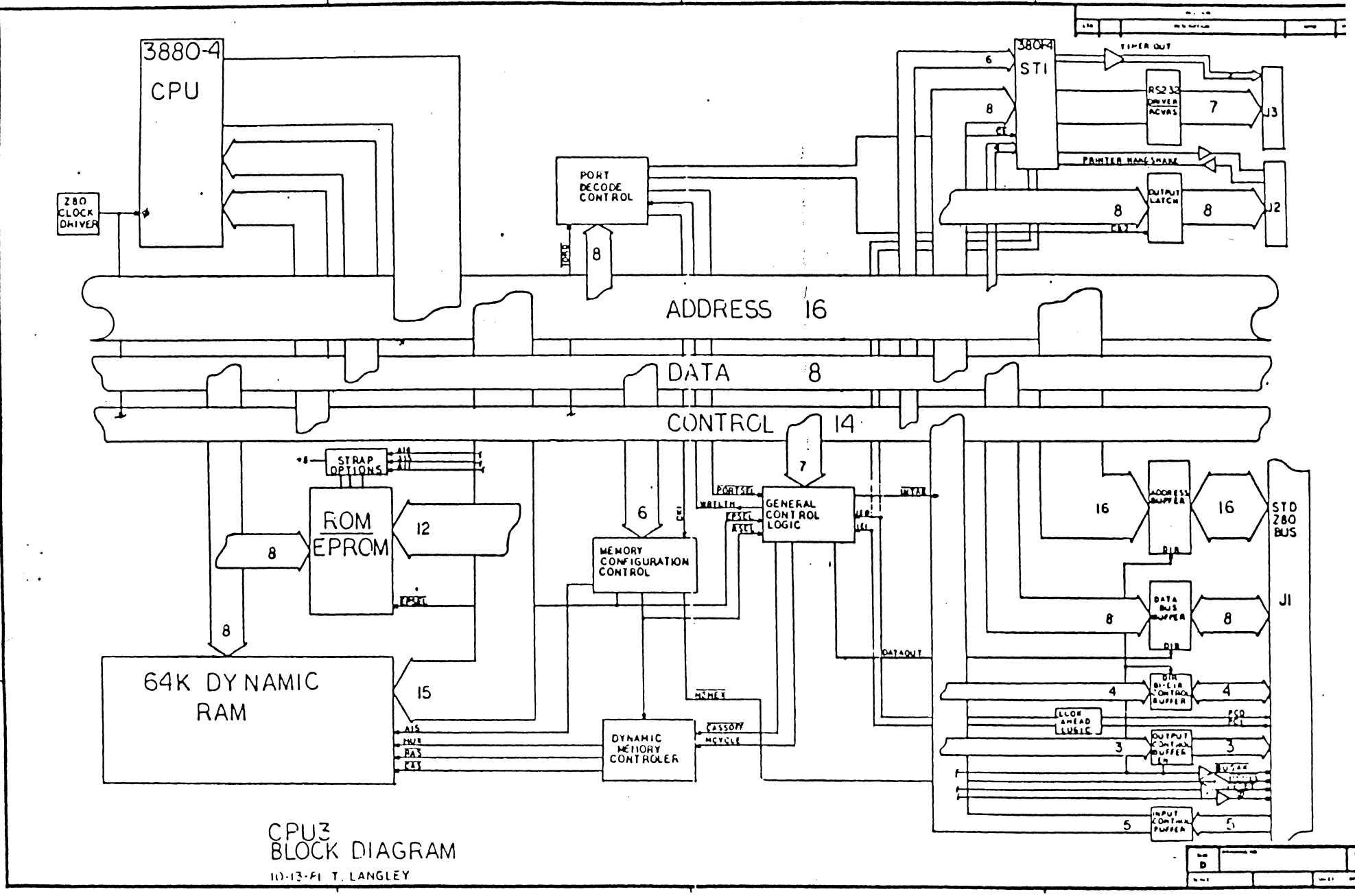
[] Fully buffered signals for system expandability.

[] Bidirectional reset which allows operation with the MDX-PFD.

[] Supports multiple memory banks for multiple operating systems.

[] Supports MEMEX capability

PRELIMINARY



CPU3
BLOCK DIAGRAM

10-13-81 T. LANGLEY

2. MDX-CPU3 DESCRIPTION

The MDX-CPU3 features a RS232 serial port, an 8 bit output with handshake for connection to a printer, 64K of dynamic Ram, and 2K to 32K of ROM/EPROM. The CPU3 supports a very flexible memory map configuration by the use of a memory configuration PROM (U24). This allows the user to map this ROM anywhere on 2K boundaries in the 64K memory map. This PROM also allows up to 16 different configurations selectable from software. If desired, the user may, by programming this PROM, be configured to support multiple pages of memory. Address, data and control busses have been made bidirectional to allow external masters to directly access CPU memory.

The 8 bit parallel output port with handshake lines have been configured to easily accomodate direct connection to a centronics type printer interface.

The RS232 serial port has been configured to accomodate full handshake cpapbilites.

3. I/O CAPACITY

The MDX-CPU3 utilizes 18 of the possible 256 port addresses leaving 238 port addresses avaliable to the user for expansion.

4. MEMORY REFRESH

The MDX-CPU3 generates all address and control signals necessary to refresh external dynamic RAM modules.

5. I/O ADDRESSING

The onboard ports are programmed to the following port addresses:

Device	Port Address (Hex)
MK3801 STI	B0 - BF
PARALLEL OUTPUT LATCH	D0
MEMORY CONFIGURATION	FF

6. INTERUPTS

The MDX-CPU3 will process interupts in any of the three different Z80-CPU interrupt modes.

7. CONNECTORS AND HEADERS

7.1. BUS CONNECTOR

J1 SIGNAL DEFINITIONS

BUS PIN	MNEMONIC	DESCRIPTION
1	+5V	+5V DC LOGIC POWER
2	+5V	+5V DC LOGIC POWER
3	GND	DIGITAL SYSTEM GROUND
4	GND	DIGITAL SYSTEM GROUND
5	-5V	Logic Bias Voltage (-5vdc) NOT USED
6	-5V	Logic Bias Voltage (-5vdc) NOT USED
7	D3	The data bus is an 8-bit, bidirectional, 3-state
8	D7	bus. (Bidirectional means signals may flow either
9	D2	into or out of any card on the bus.) Direction of
10	D6	data is normally controlled by the processor card
11	D1	with the control bus. The data direction is normally
12	D5	affected by such signals as (RD), (WR), and
13	D0	interrupt acknowledge (INTAK). The data bus uses
14	D4	high-active logic. All cards are required to release the bus to high-impedance state when not in use. The processor card releases the data bus in response to bus request (BUSRQ) input from an alternate syste controller as in DMA transfers.
15	A7	The address bus is a 16-bit, 3-state, high-level
16	A15	active bus. Normally, the address originates at the
17	A6	processor card. The card releases the address bus in
18	A14	response to a BUSRQ input from and alternate
19	A5	controller. The address bus provides 16 address
20	A13	lines for decoding by either memory or I/O. Memory
21	A4	request (MEMRQ) and I/O request (IORQ) control lines
22	A12	distinguish between the two operations. The 16-bit
23	A3	Z80 address is applied directly to the 16 STD BUS
24	A11	address lines. The address bus provides a 16-bit
25	A2	memory address, an 8-bit I/O address or a 7-bit
26	A10	refresh address. I/O addressing uses the lower 8
27	A1	address bits of the 16-bit address bus, and occurs
28	A9	during I/O instruction execution. Refresh addressing
29	A0	for dynamic RAMs uses the lower 7 address bus lines.
30	A8	The refresh address occurs during the T3 and T4 time states of an M1 machine cycle.
31	/WR	This signal indicates that the BUS holds valid data to be written in the addressed memory or output device. WR is the clock pulse, which writes data to memory or output port latches. The signal originates from the processor, which also provides the output data on the BUS.

32	/RD	This signal indicates that the CPU wants memory or an I/O device to place data on the BUS. RD is the clock pulse, which causes memory or I/O device to gate data outward onto the data bus. The signal originates from the processor, which is the receiver of the data on the BUS.
33	/IORQ	This signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. The IORQ signal is also generated with an M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M1 time, while I/O operations never occur during M1 time.
34	/MEMRQ	This signal indicates that the address bus holds a valid address for a memory read or memory write operation.
35	IOEXP	Not supported on this card.
36	MEMEX	This signal indicates to external memory cards that secondary memory should be allowed access by the CPU.
37	/REFRESH	This signal indicates that the lower seven (7) bits of the address bus contain a refresh address for dynamic memories and the MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle an eighth bit (A7) which is the R registers most significant bit is program-settable in the high or low state.
38	/MCSYNC	Not supported on this card.
39	/STATUS1	This signal indicates that the current machine cycle is in the op code fetch cycle of an instruction or is performing an interrupt acknowledge cycle (M1 is ANDed with IORQ internally to produce INTAK). Note that the Z80 has both one and two byte opcodes (2-byte opcodes are identified by a first byte equal to CB, DD, ED, or FD hexadecimal). Accordingly, the processor asserts M1 in each opcode byte, or twice per instruction cycle for these instructions.
40	/STATUS0	Not supported on this card.
41	/BUSAK	This signal is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

42	/BUSRQ	This signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When BUSRQ is asserted the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated and the BUSAK signal will be asserted.
43	/INTAK	This signal is used to indicate that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus. The INTAK signal is equivalent to an IORQ during an M1 cycle.
44	/INTRQ	This signal is generated by an I/O device. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an interrupt acknowledge signal INTAK (IORQ during an M1) is sent out at the beginning of the next instructions.
45	/WAITRQ	This input signal to the processor indicates that the addressed memory or I/O device is not ready for a data transfer and therefore the CPU should maintain a valid address for extra cycles as long as WAITRQ remains valid. This signal allows memory or I/O devices of any speed to be synchronized to the CPU. Use of this signal postpones refresh as long as it is held active.
46	/NMIRQ	This signal is a processor-card interrupt input of the highest priority. The NMIRQ automatically forces the CPU to restart to location 0066h. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a /BUSRQ will override a /NMIRQ.
47	/SYSRESET	This signal is an output from the system reset circuit, which is triggered by power-on detection, or by the push-button reset. The system reset bus line should be applied to all bus cards that have latch circuits requiring initialization. A system reset will force the CPU program counter to zero, disable interrupts, set the I register to 00h, set the r register to 00h, and set Interrupt Mode 0. Mostek MD CPU boards also support this signal in an input mode for use with a power fail detect controller.
48	/PBRESET	This signal is an input line to the system reset

circuit which will generate a debounced system reset. This input will support 15 74LS loads or a push-button switch input.

49	/CLOCK	This signal is a buffered, processor clock signal, for use in system synchronization or as a general clock source.
50	/CNTRL	Not supported on this card.
51	PCO	This signal is sent to the PCI input of the next lower card in priority. A card that needs priority should hold PCO low. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
52	PCI	This signal is provided directly from the PCO of the next higher card in priority. A card that needs priority should hold PCO low. A high level on this pin indicate that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Power Return Bus (not used)
54	AUX GND	Auxiliary Power Return Bus (not used)
55	+12V	Positive DC System Supply Power (+12vdc)
56	-12V	Negative DC System Supply Power (-12vdc)

7.2. PRINTER CONNECTOR

J2 The printer port data and control signals are brought out to a 26 pin connector as shown:

SIGNAL NAME	PIN	J2	PIN	SIGNAL NAME
/STB	1	X X	14	GND
D1	2	X X	15	GND
D2	3	X X	16	NC
D3	4	X X	17	NC
D4	5	X X	18	NC
D5	6	X X	19	NC
D6	7	X X	20	NC
D7	8	X X	21	NC
D8	9	X X	22	NC
NC	10	X X	23	NC
BUSY	11	X X	24	NC
PE	12	X X	25	NC
NC	13	X X	26	NC

7.3. SERIAL CONNECTOR

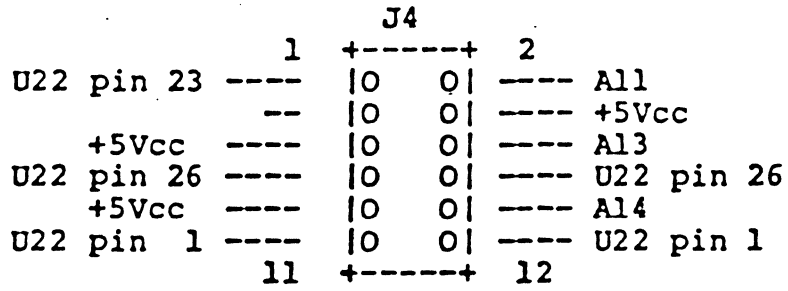
J3 The serial communication signals and handshake to perform an RS232 type interface are buffered and brought out to a 26 pin connector as shown:

SIGNAL NAME	PIN	J3	PIN	SIGNAL NAME
GND	1	|X X|	14	NC
RX	2	|X X|	15	NC
TX	3	|X X|	16	NC
RTS	4	|X X|	17	NC
CTS	5	|X X|	18	TA0
DSR	6	|X X|	19	NC
GND	7	|X X|	20	DTR
RSLD	8	|X X|	21	NC
NC	9	|X X|	22	NC
NC	10	|X X|	23	NC
TC0	11	|X X|	24	NC
NC	12	|X X|	25	NC
NC	13	|X X|	26	NC

Note aslo that the timer outputs are buffered and brought out this connector on pins 18 and 11.

7.4. ROM/EPROM STRAPPING

J4 This header allows the ROM/EPROM socket U22 to be configured to accept various type devices. The following table shows the strapping needed for each device.



DEVICE TYPE	STRAPS REQUIRED
MK2716	J4 (3-4),(5-7)
INTEL 2732	J4 (1-2),(5-7)
INTEL 2764	J4 (1-2),(9-11)
MK34000	J4 (5-7)
MK37000	J4 (1-2)
MK38000	J4 (1-2),(6-8),(10-12)

Fig. 7-1: Memory strapping

7.5. TEST CONNECTOR

J5 This header is used for testing purposes only and is strapped at the factory. DO NOT REMOVE

8. ELECTRICAL SPECIFICATINS

STD BUS COMPATIBLE

SYSTEM INTERUPT UNITS:
1 SIU

SYSTEM CLOCK:
3.6864Mhz ±0.05%

OPERATING TEMPERATURE:
0oC to 60oC

POWER SUPPLY REQUIREMENTS

+5V ±5%	@	2.3A max
+12V ±5%	@	25ma max
-12V ±5%	@	-23ma max

9. SOFTWARE PROGRAMING GUIDELINES

The CPU3 can support a phantom ROM type of operation where the ROM has just enough code to bring a larger operating system into RAM, then by switching to another memory map, dynamically disables the ROM and begins operation in a purely RAM configuration. A very simple method to do this is to have memory map 0 in the configuration PROM which will allow the Prom to appear at both 0000H and E000H addresses. Then the following procedure is followed:

A. Perform a jump to Bootstrap at E003H. This sets the CPU program counter to point to the second image area of the ROM.

B. Perform a self copy of the ROM code into the RAM at the same address range as the ROM.

C. Switch maps by outputting a mew map number to the Memory Configuration port.

D. Execution of the program will continue at the next instruction now in RAM.

An example of the programing required to accomplish this procedure is shown below:

```
;*****************************************************************
;*                                                               *
;*          PHANTOM BOOT                                         *
;*                                                               *
;*****************************************************************
;
BOOTSP    EQU       $
;
          JP        BOOTSO          ;SET ADDRESS IN CPU
;
BOOTSO:   LD        HL,BOOTSP       ;GET START OF BOOTSTRAP PGM
          LD        D,H             ;MOVE TO DESTINATION
          LD        E,L             ;ADDRESS
          LD        BC,BOOTEND-BOOTSP  ;GET # OF BYTES
          LDIR                      ;TRANSFER DATA
;
BOOTS1:   LD        A,MAP1          ;GET MAP1 BYTE
          OUT       (MAPPRT),A      ;OUTPUT TO MAP PORT
```

At this point the program will begin execution out of RAM.

10. PROM PROGRAMING GUIDELINES

The following is an example of how to define the code necessary to custom program a memory map into the Memory Configuration PROM.

STEP 1.
Define the areas where RAM, ROM, or Blank areas should be located.

STEP 2.
Determine which of the Maps is desired to be used. The following chart shows the boundaries of each Map.

MAP NO.	WORD NO.	MAP NO.	WORD NO.
0	000-01F	8	100-11F
1	020-03F	9	120-13F
2	040-05F	10	140-15F
3	060-07F	11	160-17F
4	080-09F	12	180-19F
5	0A0-0BF	13	1A0-1BF
6	0C0-0DF	14	1C0-1DF
7	0E0-0FF	15	1E0-1FF

STEP 3.
Using the following bit definition chart select the proper bits for each word necessary to support the desired Map.

OUTPUT BIT DEFINITIONS	ACTIVE STATE
O1 - SELECT EPROM	LOW
O2 - A15 ADDRESS LINE OUTPUT	SEE A15 ADDRESS CHART
O3 - SELECT RAM	LOW
O4 - MEMORY EXPAND OUTPUT	LOW

1. SELECT EPROM This bit generates the signal which enables the ROM/EPROM for reading.

2. A15 ADDRESS LINE OUTPUT This bit generates the uppermost address line to the onboard RAM memory. This allows the interchanging of the upper and lower 32K halves of RAM. Normally this line is programed to give a true image of A15.

3. SELECT RAM This bit generates the signal which enables the RAM.

4. MEMORY EXPAND OUTPUT This bit generates a signal which is defined by the STD-Bus specification for the MEMEX signal. In most single board configurations this bit is programmed high.

A15 ADDRESS CHART

WORD NO.	A15 STATE	WORD NO.	A15 STATEO
XX0	0	XX8	1
XX1	0	XX9	1
XX2	0	XXA	1
XX3	0	XXB	1
XX4	0	XXC	1
XX5	0	XXD	1
XX6	0	XXE	1
XX7	0	XXF	1

This is an example of the above procedure:

MEMORY ADDRESS	MAP NO. 0
FFFF	RAM
F000	ROM
E000	RAM
D000	
C000	
B000	
A000	
9000	
8000	RAM
7000	
6000	
5000	
4000	
3000	
2000	RAM
1000	
0000	ROM

PROM LISTING WORD NUMBER	BIT NO. 1 2 3 4	HEX VAL
00	0 0 1 1	(C)
01	1 0 0 1	(9)
02	1 0 0 1	(9)
03	1 0 0 1	(9)
04	1 0 0 1	(9)
05	1 0 0 1	(9)
06	1 0 0 1	(9)
07	1 0 0 1	(9)
08	1 1 0 1	(B)
09	1 1 0 1	(B)
0A	1 1 0 1	(B)
0B	1 1 0 1	(B)
0C	1 1 0 1	(B)
0D	1 1 0 1	(B)
0E	0 1 0 1	(A)
0F	1 1 0 1	(B)
10	0 0 1 1	(C)
11	1 0 0 1	(9)
12	1 0 0 1	(9)
13	1 0 0 1	(9)
14	1 0 0 1	(9)
15	1 0 0 1	(9)
16	1 0 0 1	(9)
17	1 0 0 1	(9)
18	1 1 0 1	(B)
19	1 1 0 1	(B)
1A	1 1 0 1	(B)
1B	1 1 0 1	(B)
1C	1 1 0 1	(B)
1D	1 1 0 1	(B)
1E	0 1 0 1	(A)
1F	1 1 0 1	(B)

11. MECHANICAL SPECIFICATINS

CARD DIMENSIONS
- 4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
- 0.675 in. (1.71 cm.) maximum profile thickness
- 0.062 in. (0.16 cm.) printed circuit board thickness

STD BUS EDGE CONNECTOR
- 56 Pin Dual Readout; 0.125 in. centers

12. ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-CPU3	3.6864Mhz CPU3 module with Operations Manual (less EPROM and mating connectors)	MK77857

13. WARRANTY INFORMATION

To be supplied later.

APPLICATION BRIEF

THE
MOSTEK MDX-CPU3
SINGLE BOARD MICROCOMPUTER

...a power-packed, compact, cost-effective single board microcomputer...

THE
MOSTEK MDX-CPU3
SINGLE BOARD MICROCOMPUTER...

the STD-Z80 BUS compatible
CPU (Central Processor Unit)

[] is a complete Z80 microprocessor system on one 4.5 x 6.5 inch circuit board.

[] has 64K bytes of dynamic memory on-board. (no other memory cards are required, but can be used if necessary.)

[] has a RS232C serial I/O port (with modem control) for two-way flow of data between the computer and a user terminal or other computer equipment.

[] has an 8-Bit parallel printer port that is Centronics interface compatible.

[] has a red light emitting diode (LED) that is user programmable. (could be used as a diagnostic test indicator, CPU run light etc.)

[] provides phantom capability for the single 28-pin socket for a total RAM operating mode.

HIGHLIGHTS

[] Allows the user to build a more compact system. (single board system)

[] Permits the user to use existing 8080A software without modifications. (The Z80 processor includes all of the 8080A instructions as a subset; adds Bit, Relative, and Indexed addressing modes; powerful data block search and move instructions; and a duplicate set of internal registers for quick execution time in many applications.)

[] Permits easy maintanance...only one board to replace.

[] Eliminates the need for large inventory requirements.

[] Has ability to perform a user defined diagnostics of the system and indicate the results by the onboard red LED.

FEATURES

[] The MDX-CPU3 is STD BUS compatible which will permit it to work with other STD boards if so required.

[] The MDX-CPU3 board has a single 28-Pin socket which may be strapped to accept any of the following industry-standard memory devices.

EPROM	ROM
MK2716 (2K x 8)	MK34000 (2K x 8)
2732 (4K x 8)	
2764 (8K x 8)	MK37000 (8K x 8)
	MK38000 (32K x 8)

[] Phantom ROM capability is provided and desired if the user wishes to maximize the transient program RAM area of memory.

[] Bidirectional address, data, and control busses to permit external Direct Memory Access (DMA).

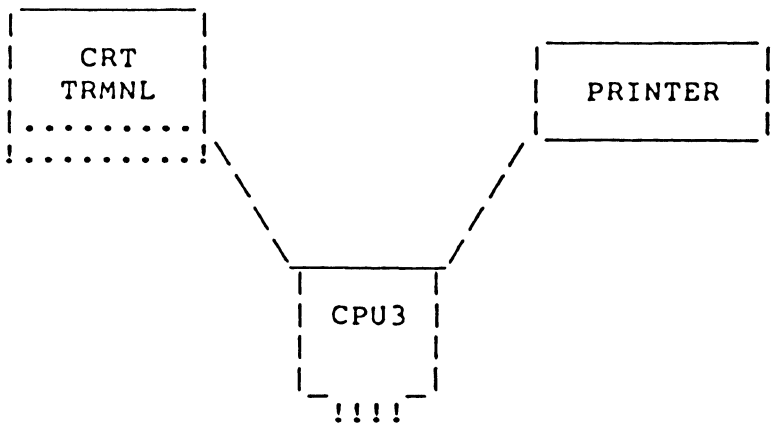
[] Software programmable baud rate. (minimal configuring straps required during manufacturing phase of your product)

[] Printer port pinout is configured for direct connection to Centronics interface using mass terminated connectors and flat ribbon cabling. (no scrambling or use of discrete wire is required.)

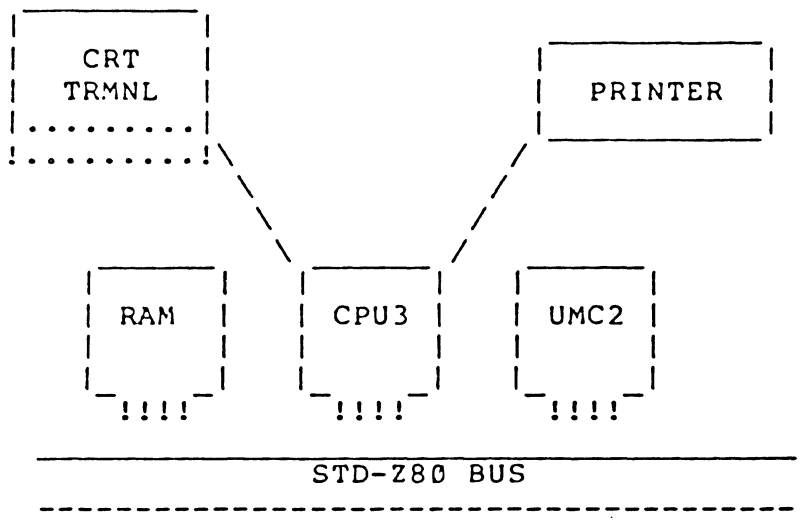
[] Supports multiple memory banks for multiple operating systems.

[] User programmable LED indicator to signal faulty or other condition.

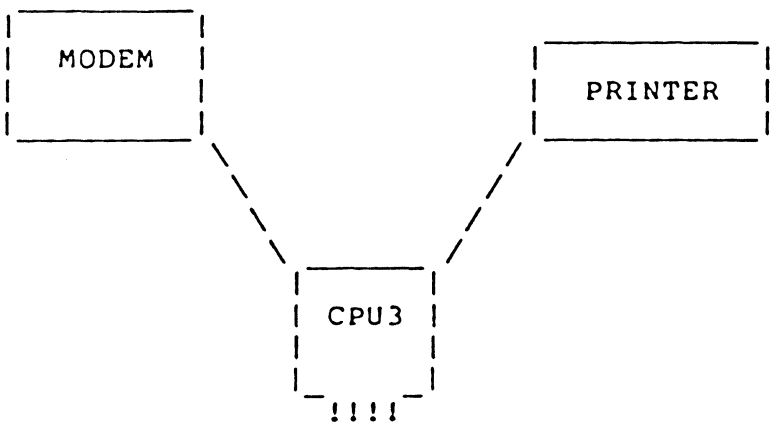
MOSTEK MDX-CPU3 CONFIGURATIONS



Single Board System



Multi-board System



Remote Stand Alone System

APPLICATIONS

The MDX-CPU3 board is a versatile single board microcomputer system. Its use spans a wide range of applications. An attempt is made to catagorize its uses below:

-Manufacturing

-Business Data Processing

-Product Development

Within these broad catagories, the MDX-CPU3 can be used specifically in the following applicaitons.

Manufacturing
* Test Equipment
* Process Control
* Instrumentation
* Data Logging
* Quality Control
* Process Monitoring
* Remote Machine Control

Business Data Processing
* Word Processing
* Report Generation
* Executive Work Stations
* Small Business Accounting
* Inventory Control
* Point of Sale Processing
* Hotel Phone Call Accounting
* Communication Control

Product Development
* Software Development
* Software Evaluation
* PC Design Support
* Microcomputer Board Development
* Target System Emulation

TECHNICAL INFORMATION

I/O CAPACITY

The MDX-CPU3 utilizes 18 of the possible 256 port addresses available to the user for expansion.

MEMORY REFRESH

The MDX-CPU3 generates all address and control signals necessary to refresh external dynamic RAM modules.

I/O ADDRESSING

The on-board ports are programmed to the following addresses:

Device	Port Hex Address
MK3801 STI	B0 - BF
Parallel Output Latch	D0
Memory Configuration	FF

INTERRUPTS

The MDX-CPU3 will process interrupts in any of the three different Z80 Modes.

CONNECTORS & HEADERS

J1 STD BUS CONNECTOR

J2 PARALLEL PORT CONNECTOR

The printer port data and control signals are brought out to a 26-Pin connector as shown below.

SIGNAL NAME	PIN	J2	PIN	SIGNAL NAME
/STB	1	|o o|	14	GND
D1	2	|o o|	15	GND
D2	3	|o o|	16	NC
D3	4	|o o|	17	NC
D4	5	|o o|	18	NC
D5	6	|o o|	19	NC
D6	7	|o o|	20	NC
D7	8	|o o|	21	NC
D8	9	|o o|	22	NC
NC	10	|o o|	23	NC
BUSY	11	|o o|	24	NC
PE	12	|o o|	25	NC
NC	13	|o o|	26	NC

J3 SERIAL PORT CONNECTOR

The serial communication signals and control lines to perform an RS232C type interface are buffered and brought out to a 26 pin connector as shown. Note that timer outputs are brought out as well.

SIGNAL NAME	PIN	J3	PIN	SIGNAL NAME
GND	1	|o o|	14	NC
RX	2	|o o|	15	NC
TX	3	|o o|	16	NC
RTS	4	|o o|	17	NC
CTS	5	|o o|	18	TA0
DSR	6	|o o|	19	NC
GND	7	|o o|	20	DTR
RSLD	8	|o o|	21	NC
NC	9	|o o|	22	NC
NC	10	|o o|	23	NC
TC0	11	|o o|	24	NC
NC	12	|o o|	25	NC
NC	13	|o o|	26	NC

ROM/EPROM STRAPPING

The J4 header allows the ROM/EPROM socket U22 to be configured to accept various type devices. See table below.

DEVICE TYPE	J4 STRAPS REQUIRED
MK2716	3-4, 5-7
INTEL 2732	1-2, 5-7
INTEL 2764	1-2, 9-11
MK34000	5-7
MK37000	1-2
MK38000	1-2, 6-8, 10-12

TEST CONNECTOR

The J5 connector is used for testing purposes only and is strapped at the factory. Do not remove this strap.

ELECTRICAL SPECIFICATIONS

STD BUS COMPATIBLE

SYSTEM INTERRUPT UNITS: 1 SIU

SYSTEM CLOCK: 3.6864 MHz ± 0.05 %

OPERATING TEMPERATURE: 0°C to 50°C

POWER SUPPLY REQUIREMENTS: + 5 VDC ±5% @ 2.3A max
+12 VDC ±5% @ 25ma max
-12 VDC ±5% @ 23ma max

MECHANICAL SPECIFICATIONS

CARD DIMENSIONS:
4.50 in. (11.43 cm) wide by 6.50 in. (16.51 cm) long.
0.675 in. (1.71 cm) maximum profile thickness.
0.062 in. (0.16 cm) printed circuit board thickness.

STD BUS CARD EDGE CONNECTOR J1:
56 Pin Dual Readout; 0.125 in. centers

MATING CONNECTORS: (User provided)
for J1: VIKING 3VH28/1CE5 (printed circuit type)
VIKING 3VH28/1CND5 (wire-wrap type)
VIKING 3VH28/1CN5 (solder lug type)

for J2 & J3:
Mass terminated:
T & B Ansley #609-2601M
Winchester Electronics #51-1126-01
3M #3399-6026

Discrete wires:
Winchester Electronics
Housing: #PGB-13-A
Contacts: Crimp #100-72020S (20-24 AWG)
#100-72026S (26-30 AWG)

ORDERING INFORMATION:

DESIGNATOR	DESCRIPTION	PART NO.
MDX-CPU3	3.6864 MHz CPU3 module with Data Sheet (less EPROM and mating connectors)	MK77857