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DSP5630x FSRAM Module Interfacing

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INTRODUCTION

Due to ever increasing complexity of executable code, several applications based on digital signal processors (DSPs) are requiring higher and higher performance in terms of execution speed. To accommodate these requirements, Motorola has developed a 24–bit DSP family and several memory support chips to provide cost–effective, high–performance solutions.

This document describes several options of interfacing different asynchronous fast static RAM modules to the Motorola 24–bit DSP5630x family.

DSP56300 CORE DESCRIPTION

The DSP56300 is a powerful new DSP engine (NDE) core capable of executing an instruction on every clock cycle, thus yielding a twofold performance increase compared to the 56K core while maintaining 100% object code compatibility with it.

The DSP56300 CMOS core is composed of an expansion port and DRAM controller, data ALU, address generation unit, instruction cache controller, program control unit, DMA controller, PLL clock oscillator, On–Chip Emulation Port (OnCE™), and the peripheral and memory expansion bus.

To minimize the total system cost, the DSP56300 core incorporates a versatile external memory interface that provides glueless interface to a variety of memories such as dynamic RAMs (DRAMs), static RAMs (SRAMs), and synchronous static RAMs (SSRAMs).

PORT A INTRODUCTION

Port A of the DSP56301 core is the memory expansion port that can be used either for memory expansion or for memory–mapped I/O. A number of features make port A versatile and easy to use. These features provide a low part–count connection with fast static memories, dynamic memories, I/O devices, and multiple bus master systems.

PORT A OPERATION

The port A data bus is 24 bits wide with a separate 24–bit wide address bus capable of a sustained rate of 1 memory access per clock cycle for data space accesses (using synchronous static memory). External memory is divided into three 16M x 24 bit spaces — X, Y, and P. An internal wait state generator can be programmed to insert up to 31 wait states, if access to slower memory or I/O devices is required. A bus wait signal allows an external device to control the number of wait states inserted in a bus access operation. Bus arbitration signals allow an external device to use the bus while internal operations continue using the internal memory.

EXTERNAL STATIC RAM CONTROL

External bus timing is controlled by the $\overline{TA}$ control signal and by the bus control register (BCR) (see Table 1). Insertion of wait states is controlled by BCR to provide constant bus access timing, and by the TA control signal to provide dynamic bus access timing. The number of wait states for each external access is determined by input TA or by BCR, whichever is longest.

Table 1. BCR Register Programming

BCR Bits 23 – 0	Configuration
01X000010010010000100001	Areas 3, 2, 1, and the default area = 1 wait state. BLH and BRH are cleared.

Using the configuration in Table 1, all external memory areas (3, 2, 1, and default) are programmed to 1 wait state. Using the suggested modules shown in Figure 1, areas 3, 2, and 1 are used depending on the configuration. If other types of memory or external devices are required, the relevent areas should be programmed for the required wait states. The external memory address is defined by the address bus A23 – A0 and the memory address attribute signals AA3 – AA0. The AA signals have the same timing as the address bus and may be used as additional address lines. The AA signals are also used to generate chip select signals for the appropriate memory chips. These chip select signals change the memory chips from low power standby mode to active mode and begin the access time. This allows slower memories to be used since the AA signals are address based rather than read or write enable based.

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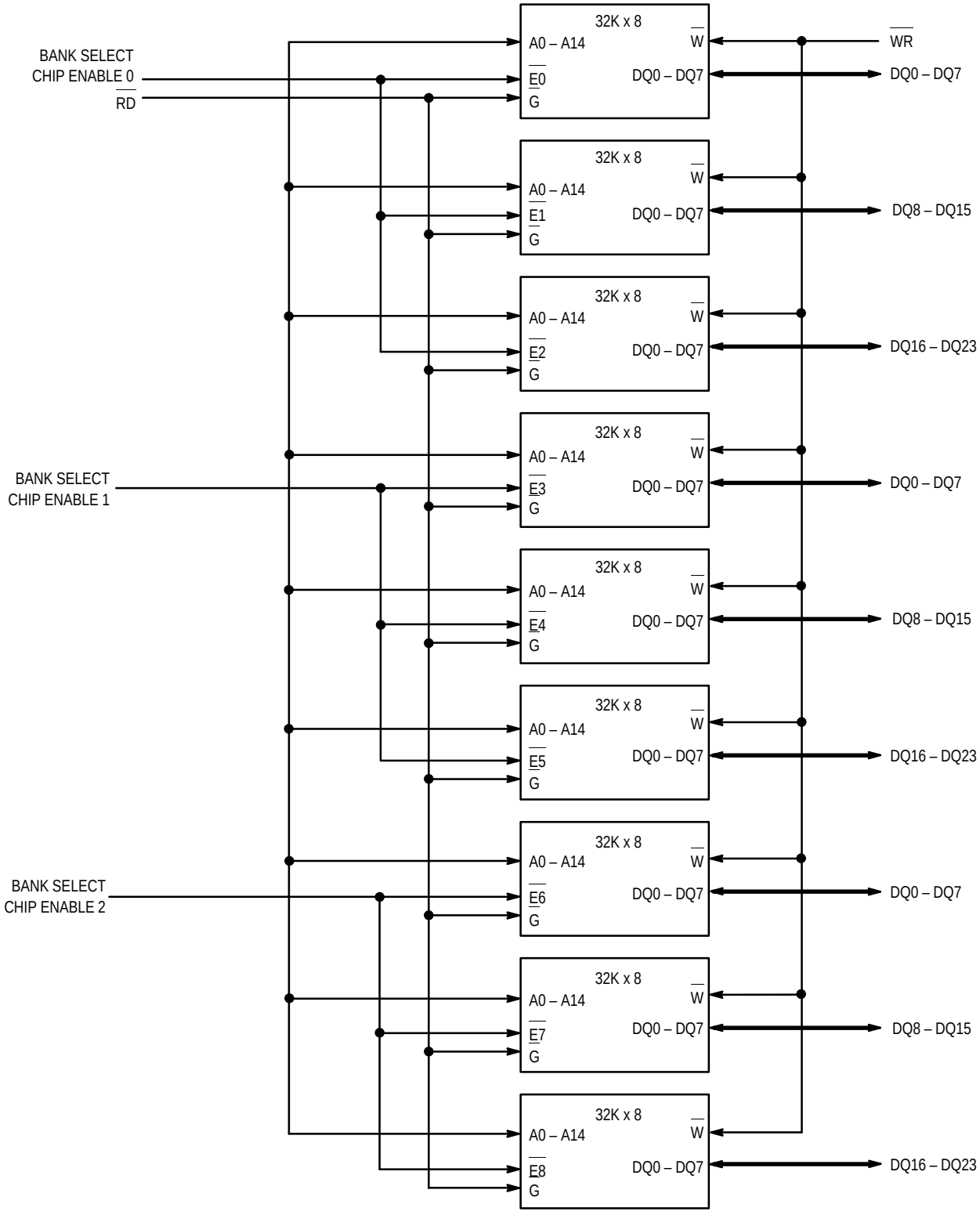

NOTE: The chip enables are connected to the AA pins of the DSP.

Figure 1. Proposed Module Solution Using 32K x 8 FSRAMs

ADDRESS ATTRIBUTE CONTROL REGISTERS (AAR) (ONE FOR EACH AA PIN)

The four control registers (AAR3, AAR2, AAR1, and AAR0) are 24–bit read write registers used to control the activity of the AA3 – AA0/RAS3 – RAS0 pins. An AA/RAS pin is asserted if the address in its appropriate AAR (BAC bits) matches the external address where the exact number of address bits that are compared is determined by the BNC bits, and if the external access is aimed to a space X, Y, or P, enabled in the appropriate AAR. All AARs are disabled (all AAR bits cleared) during hardware reset. The AAR bits are shown in Figure 2 and described in the following paragraphs.

A priority mechanism exists among the four AARs in order to resolve selection conflicts. AAR3 has the highest priority and AAR0 has the lowest (e.g., if the external address matches the address and the space that is specified in both AAR1 and AAR2, the external access type will be selected according to the AAR2 register). The priority mechanism allows continued partition of the external address space.

When the AA/RAS pin functions as the AA pin, it is negated at the start of the next clock cycle only if there is no external access that uses the same AA pin (i.e., the AA pin will be kept asserted in a sequence of two consecutive external accesses that access the same memory bank). This method enables the use of low power standby mode in the external memories (these memories should be accessed first by a dummy access).

The programmer should guarantee that an AAR is not changed while accessing the memory selected by this AAR, otherwise improper operation may result.

MODULE SOLUTIONS

The proposed module in Figure 1 is composed of nine 3.3 V, 32K x 8 based FRAMS. The RAMs are used in groups of 3 to accommodate the 24–bit bus architecture of the DSP. Selection is segmented into 3 banks, providing a total memory depth of 96K. Bank selection for use of X data space, Y data space, and program memory is facilitated by means of DSP56301 AA control pins. Three AA control lines define which banks (memory type) are selected (see Figure 3). The address pins are directly connected to the address bus partitioned among the nine FSRAMs. The DSP output enable (RD) is directly connected to each FSRAM output enable, while the DSP write enable is connected to the nine FSRAM write enables. The data bus is connected sequentially across each bank of memory.

If the components are 5 V, the data bus can be clamped to 3.3 V using a voltage regulator (see Figure 4). The voltage regulator circuit uses a 3.3 V EZDropper shunt regulator device (EZ5Z3L–S3.3V), depicted in Figure 5. This voltage regulator circuit is incorporated and supplied on the module and does not impact the user's design.

If one particular memory type (X, Y, or P) needs greater allocation of available external memory, it can be accomplished by using AA control pins and partitioning the external memory by means of one or two extra address bits.

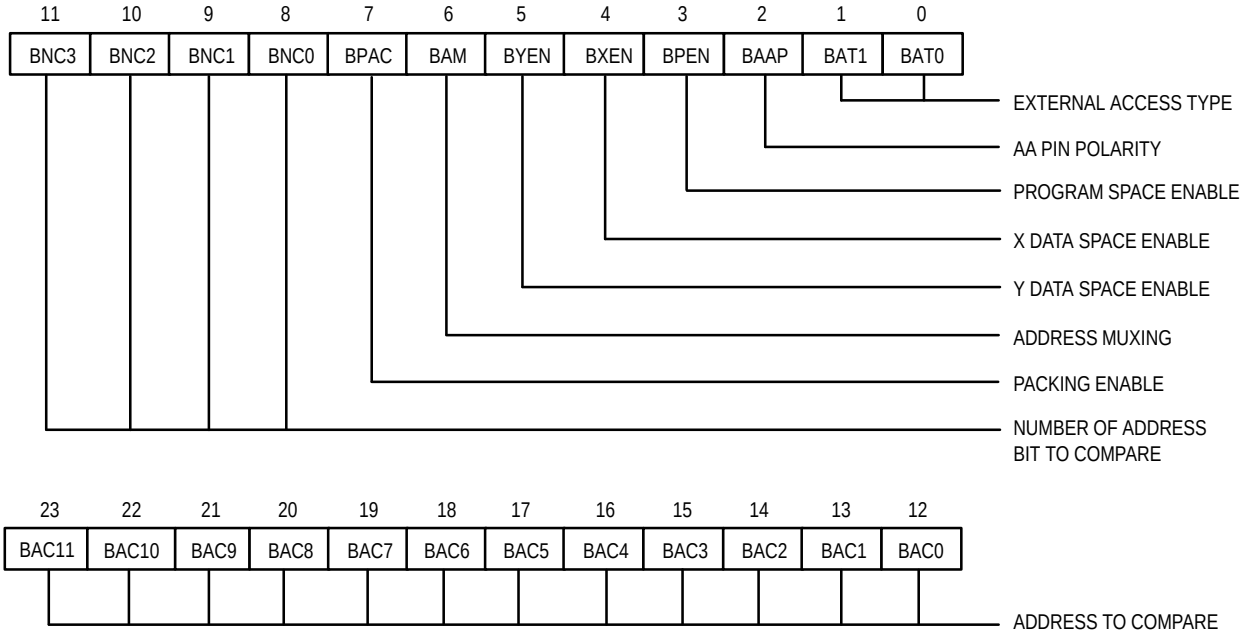

Figure 2. Address Attribute Registers (AAR3 – AAR0)

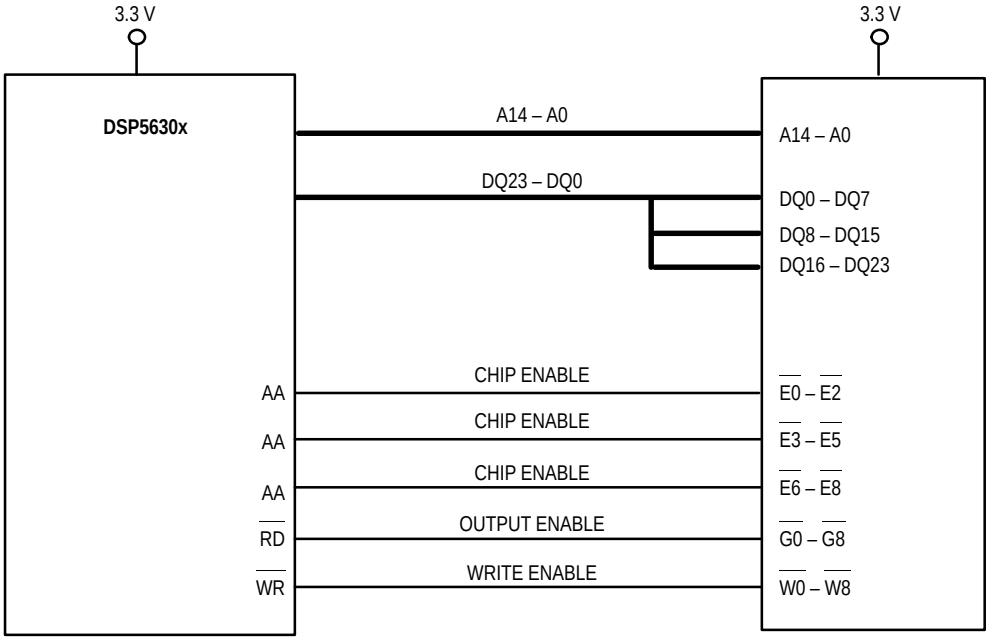

Figure 3. DSP5630x Connection to (32K x 8) Based Module on X, Y, and P Memory

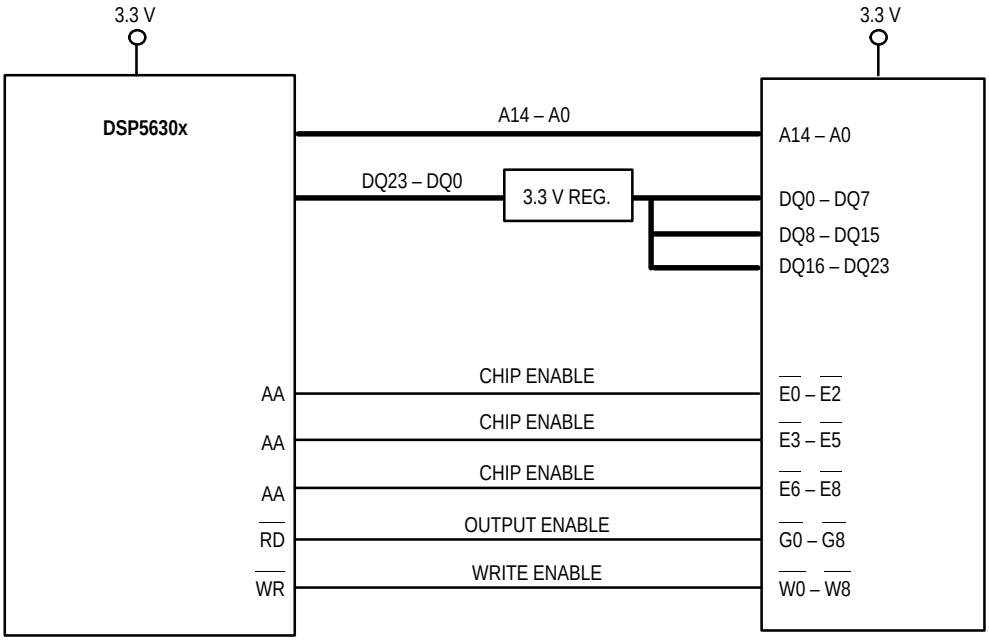

Figure 4. DSP5630x Connection to (32K x 8) Based Module on X, Y, or P Memory

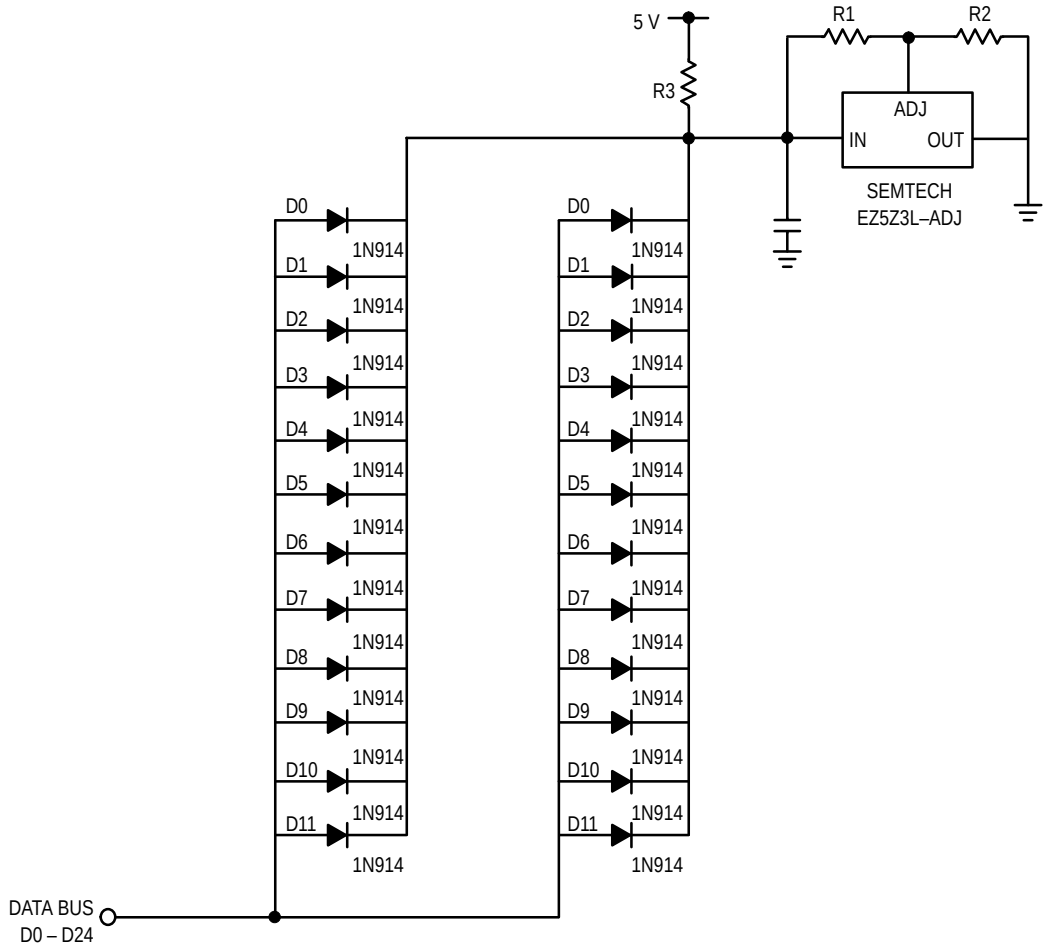

Figure 5. 5 V to 3.3 V Regulator Circuit

Here, the AARs would be configured for the required external memory types; X data space, Y data space, or program memory, and addresses A15, A16 for bank selection by incorporating the address to compare capability. Table 2 details the bank's selection configuration. If only two types of memory are required as in options 2, 3, and 4, the banks can be split in a ratio of two to one. Taking option 2 as an example, the Y memory selects two banks and program memory selects the remaining bank. The program memory does not require comparing the address, and the AA1 pin is connected to chip enables E6, E7, and E8. Y memory selects two banks by means of two AA pins. The high order Y memory bank is selected using AA3 and comparing for a set or 1 value of bit 15 (or BAC3) in AAR3. If this bit is set, the AA3 pin activates the high order Y memory bank. If this bit is not set, a comparison is performed on bit 15 (or BAC3) of AAR2. If this bit is not set or has a 0 value, the low order Y memory bank is selected by the AA2 pin. This process is also valid for options 3 and 4.

Option 5 is unique in that only one type of external memory is selected. In this case, the memory is sequential and the partitioning (bank selection) is selected by means of comparing address bits A16 and A15 (BAC4 and BAC3). The high order addressing is compared using the highest priority AAR3. If the address bits 16 (BAC4) and 15 (BAC3) are set to 10, the highest order bank is selected. If this is not true, address comparison will be made in AAR2 for bits 16 and 15 to be equal to 01. Validation will select the middle addressing bank, otherwise a comparison will be made of bits 16 and 15 (BAC4 and BAC3) of AAR1 (the lowest address bank) being equal to 00. Confirmation selects the low address bank. In this way, the full external 96K memory map can be utilized.

Consequently, programming the AARs for async FSRAM modules with one wait state and the AA pin active low is configured as shown in Table 4. Table 4 depicts examples of different options of compare and no compare addressing for external memory segregation.

Table 2. DSP to FSRAM Bank Configuration

Option	Memory	AA Pin	Connect	Compare	BAC Bit	Address Bit
1	X	AA3	AA3 – E0, E1, E2	No	NA	NA
	Y	AA2	AA2 – E3, E4, E5	No	NA	NA
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
2	Y	AA3	AA3 – E0, E1, E2	Yes	BAC3	15
	Y	AA2	AA2 – E3, E4, E5	Yes	BAC3	15
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
3	X	AA3	AA3 – E0, E1, E2	Yes	BAC3	15
	X	AA2	AA2 – E3, E4, E5	Yes	BAC3	15
	P	AA1	AA1 – E6, E7, E8	No	NA	NA
4	X	AA1	AA1 – E0, E1, E2	No	NA	NA
	P	AA3	AA3 – E3, E4, E5	Yes	BAC3	15
	P	AA2	AA2 – E6, E7, E8	Yes	BAC3	15
5* Refer to Table 3 for compares	P	AA3	AA3 – E0, E1, E2	Yes	BAC4, BAC3	16, 15
	P	AA2	AA2 – E3, E4, E5	Yes	BAC4, BAC3	16, 15
	P	AA1	AA1 – E6, E7, E8	Yes	BAC4, BAC3	16, 15

* This option is also applicable for X or Y data memory as a single selection.

Table 3. Address Bank Selection (See Option 5 in Table 2)

AA Bit	BAC4 (A16)	BAC3 (A15)	Module A14 – A0	Address	Bank Selection
AA3	1	0	111111111111111	Max Address	3 (Highest Addressing)
AA3	1	0	000000000000000	Min Address	3 (Highest Addressing)
AA2	0	1	111111111111111	Max Address	2 (Middle Addressing)
AA2	0	1	000000000000000	Min Address	2 (Middle Addressing)
AA1	0	0	111111111111111	Max Address	1 (Lowest Addressing)
AA1	0	0	000000000000000	Min Address	1 (Lowest Addressing)

Table 4. AAR Programming Options

A23 – A12	A11 – A0	Configuration
000000000000	000000001010	No Addr Compare, Pack or Mux. Program Memory, Active Low, Async SRAM.
000000000000	000000010010	No Addr Compare, Pack or Mux. X Data Space, Active Low, Async SRAM.
000000000000	000000100010	No Addr Compare, Pack or Mux. Y Data Space, Active Low, Async SRAM.
000000000000	100100001010	No Pack or Mux. A15 Compare, Program Memory, Active Low, Async SRAM.
000000000000	100100010010	No Pack or Mux. A15 Compare, X Data Space, Active Low, Async SRAM.
000000000000	100100100010	No Pack or Mux. A15 Compare, Y Data Space, Active Low, Async SRAM.
000000001000	100100001010	No Pack or Mux. A15 Compare, High Order Address, Program Memory, Active Low, Async SRAM.
000000001000	100100010010	No Pack or Mux. A15 Compare, High Order Address, X Data Space, Active Low, Async SRAM.
000000001000	100100100010	No Pack or Mux. A15 Compare, High Order Address, Y Data Space, Active Low, Async SRAM.
000000000000	100100001010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, Program Memory, Active Low, Async SRAM.
000000000000	100100010010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, X Data Space, Active Low, Async SRAM.
000000000000	100100100010	No Pack or Mux. A16, A15 Compare, Lowest Order Address, Y Data Space, Active Low, Async SRAM.
000000001000	100100001010	No Pack or Mux. A16, A15 Compare, Middle Order Address, Program Memory, Active Low, Async SRAM.
000000001000	100100010010	No Pack or Mux. A16, A15 Compare, Middle Order Address, X Data Space, Active Low, Async SRAM.
000000001000	100100100010	No Pack or Mux. A16, A15 Compare, Middle Order Address, Y Data Space, Active Low, Async SRAM.
000000010000	100100001010	No Pack or Mux. A16, A15 Compare, Highest Order Address, Program Memory, Active Low, Async SRAM.
000000010000	100100010010	No Pack or Mux. A16, A15 Compare, Highest Order Address, X Data Space, active Low, Async SRAM.
000000010000	100100100010	No Pack or Mux. A16, A15 Compare, Highest Order Address, Y Data Space, Active Low, Async SRAM.

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