

For Microcomputer Systems



EXORciser data sheets

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M6800 EXORciser

The M6800 EXORciser, through its ability to emulate a user's system, provides an efficient and economical mean to develop M6800 Microprocessor Systems. Through its optional modules, the EXORciser sweet the engineer hardware design and development in since he can arrange these modules to represent his system rather than build a system prototype.

The M6800 EXORciser optional Resident Software provides the programmer with a functional system on which to develop his system software. This software permits him to edit, assemble, and modify his programs in real time on the actual hardware with his peripheral devices incorporated in the system.

The M6800 EXORcise with its EXbug Firmware enables the engineer or programmer to evaluate and debug his system — both hardware and software — in its actual working environment. It also permits the user to make any hardware and software adjustments required in finalizing his system design.

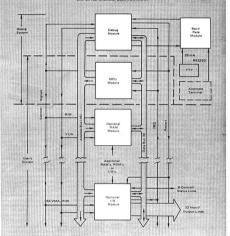
FEATURES:

- Fasy To Use
- · Saves System Design and Development Time
- Decreases System Design and Development Costs
- . Builds Confidence in the User's System
- Modular Design Allows Exact Duplication of Final System Function and Performance
 Expandability in Design Allows Duplication of Final System
- Capability

 Data Terminal Connects to EXORciser Permitting Development
- of Software and Firmware Programs

 Evaluates and Debugs Final System Software/Firmware
- Module's Firmware Performs Tests and Diagnostics on Production
 Systems
- Has Dynamic Memory Refresh Capability
- · Has Capability of Working with Slow Memories

SIMPLIFIED EXORGISER BLOCK DIAGRAM



3

M68SDT

Advance Information

RASIC FXORciser

The basic EXOR-circr IM68SDTI consists of the MPU Module, the Debag Module, the Baud Rate Module, the Power Supply and the chasis. These modules are built around the M6800 Microcomputer Family of Parts IMC6800 Microprocessing Unit, MCM6810 Ramond Access Memory, MC6820 Peripheral Interface Adapter, MCM6830 Read Only Memory, and MC6850 Asynchronous Communications.

Interface Adapter devices.

The MPU Medicine incorporates the MCGB00 Microporatesis plant. The MPU Medicine incorporates the MCGB00 Microporates plant in that it provides the MPU and clock for both the EXDRGence Delay and the user's synthem. With the exception of the EXDRGence Color, the system researt and the DPE displail felsioped, the MPU Model and the Land Color of the EXDRGence Color, the system researt and the DPE displain of the EXDRGence Color, the system researt and the DPE displain of the EXDRGence Color of the E

responding to real time interrupt signals.

The Debug Module provides the EXORciser with the capability to evaluate and debug the user's program. The three MCMB830 ROM memories on this module contain the EXDug Firemware that provides the EXORciser with its unique software control features. The module loan has two MCMB8310 RAM memories to provide a scratch-paid also has two MCMB8310 RAM memories to provide a scratch-paid

memory to the EXbug Firmware.

The Debug Module working with the Baud Rate Module provides the EXORciser with eight standard baud rates between 110 and 9500 Baud. These modules also interface the EXORciser with a TTY or RS-232C compatible terminal and provide a reader control signal for re-

mote control of modified manual TTY terminals.

The Power Supply provides the EXORciser with the +5 Vdc, +12 Vdc, and -12 Vdc power sources to support a full EXORciser rack of

modules.

The chassis is capable of holding 14 plug-in modules. The Power Supply and Baud Rate Modules are not plug-in modules but mount directly to the chassis. Two versions of the chassis are available — the

BASIC

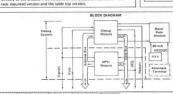




DIMENSIONS

Table Top Model	
M68SDT-T	
Width	19.25 in.
Depth	17.50 in.
Height	7,00 in.
Rack Mounted Mo	del
M68SDT-R	

Width 19,00 in.
Depth 17,00 in.
Height 7,00 in.



Specification	Value
Power Requirements	95-135/205-250 Vac 47-420 Hz, 250 W
Word Size Data Address Instruction	8 bits 16 bits 8, 16, and 24 bits
Memory Capability	65,536 bytes
Instruction Set	72 variable length instructions
Clock Cycle Time	Selectable: 1µs crystal control clock or an external clock between 1 µs and 10 µ
Interrupt	Maskable real time interrupt
Data Terminal Interface Characteristics Baud Rates (Switch selectable)	110, 150, 300, 600, 1200, 2400, 4800, and 9600
Signal Characteristics	TTY 120 mA neutral current loop! or EIA RS-232C compatible
Reader Control Signal	Control signal for TTY devices modified for external control
Operating Temperature	0 to 55°C

EXORciser OPTIONS

The M6800 EXOReiser derives its flexibility from its optional hardware, modules, and software. Two models of the EXORciser are available - a rack mounted model and a table top model. When ordering, use the appropriate part number. In addition, specify the kit number for proper in-

stallation in the chosen location. M68SDT-T EXORciser, Table Top Model

M68SDT-R EXORciser, Rack Mounted Model

MEYSSTT Table Top Kit MEXERRK Rack Mounting Kit

Optional assemblies permit the user to adapt his EXORriser to various system configurations with memory size and input/output configuration selected to meet system

needs. The optional modules include: · MEY6912.1 2K Static RAM Module

 MEX6815.1 8K Dynamic RAM Module MEX6820 Input/Output Module · MEXERIC I/O Flatribbon Interconnection Cable

 MEX68WW Universal Wirewrap Module MEX68XT Extender Module

Motorola supplies a variety of software programs to support the M6800 Microcomputer Family of Parts. These programs include Cross-Assemblers and Editors, Simulators, Build-Virtual Machine, and Help programs as well as the EXORciser Resident Editor and Assembler programs.

EXbug FIRMWARE

The EXhun Firmware is an integral part of the EXORciser, which provides system development program capability for debugging both the system hardware and software by enabling the user to perform the following functions:

- Load data into the EXORciser
- · Verify that the data in the EXORciser or on tape is valid
- · Search a tane for a specific file
- · Print the contents of the memory · Punch (record) the contents of the memory on tage Perform the MAID (Motorola Active Interface Debug)
- The MAID functions enable the EXORciser to: · Examine and, if required, change the contents in a
- memory location · Examine and, if required, change the data in an MPU resister
- · Calculate the offset in the relative addressing mode · Insert, display, and remove breakpoints in a user's
- program Free run or trace through a user's program under MAID. control
- · Stop the user's program on a specific program step · Provide an oscilloscope tripper pulse at a selected program step
- · Search memory for a specific bit pattern Perform decimal-octal-hexadecimal conversions



EXORciser BUS SIGNALS

The EXORciser bus interfaces the MPU Module with other modules being used in the EXORciser. This bus permits the EXORciser to be configured to meet a user's

specific application.

Data Bus (DoD7) — These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bushives on the modules are three-state loois devices.

Address Bus (A0-A15) — These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three state bus drivers.

Read/Write (R/W) — This MPU output signal indicates (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MCBBOD MPL of this line is read (high). Also, when the MCBBOD MPL he module is hatted, this signal will be in the read state. Valid Memory Address (VMA) — This line, when high, indicates that the address on the bus is salid.

Valid User's Address (VUA) — This line, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program. Memory Clock (MEMCLK) — This is the basic clock.

signal used by the MPU Module to generate its \$1 and \$2 non-overlapping clock signals.

Phase 1 (\$1) Clock — This signal is derived from the Memory Clock and is present during the MPU addressing

time. This signal is controlled by the MPU Module.

Phase 2 (¢2) Clock — This signal also is derived from the
Memory Clock and used to synchronize the transfer of

Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bin Available (BA) — The Bin Available signal will promally be a low level, When activated, it will go high indiscring that the address has it available. This will occur if the FBT line is slow or the MOSBO MPI is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPI Modale three-rates output drivers will go to their off state and other output to their normally in-sective state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the

Interrupt Request (IRQ) — This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU

will begin the interrupt sequence.

Non-Maskable Interrupt (RMII) — This level sensitive input, on going low, requests that an interrupt sequence be

BUS (

It is possible for a module other than the MPU Module

to gain control of the bus. This module would place a low

generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

well begin its non-mask-able interrupt routine.

Reset – This deg ensitive signal initiates an MC6800
MPU power-on vectored interrupt initialize routine when
power is first applied to the EXORciser and each time the
EXORciser's RESTART switch is actuated. This signal, in
addition to resetting the module's MPU, is used to reset

and initialize the rest of the EXORciser.

These-State Control ITSCJ - This input, when high,
causes all of the NPU Module's Address Bus lines and RVM
line to go to their off or high-impedance state. They
it is to go to their off or high-impedance state. They
did Memory Address and Valid User's Address signal will be
forced low. The Date Bus in not affected by the TheeState Control. This signal is initially jumpered to ground
on the MPU Moder.

Refresh Request (REFREQ) — This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the ol and o2 clock signals with ol high and, through the Refresh Grant command, instructs the initiating memory module to re-

fresh itself.

Refresh Grant (REFGRANT) — The MPU Module, on receiving a Refresh Request input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) — This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the ô1 and ô2 clock signals with 62 high. The imitating module, on completing its memory operation, returns the Memory Ready signal to a high level. Half — When this input is low all activity in the MC6800

MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at 'the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the Halt line must not occur during the last 250 ns of \$\phi\$1. To insure single instruction operation, the Halt line must go high for one \$\phi\$1 clock pulse.

Refresh Clock (REFCLK) — This signal is generated by the dynamic memory module being used as the master efferah module. This signal is used to intilate a memory refresh operation on the dynamic modules functioning as slave refresh modules.

Stand By (STDBY) — This line is a low level during a power-fail condition and a high level during normal EXORciser operation.

BUS CONTROL

module requesting control of the bus now must pull the Three-State Control line low, forcing the MPU Module address bus drivers to their high-impedance state. The requesting module now has control of the EXORciser bus until it elects to relinquish control.





MFX6800

Advance Information

MPII MODIII E

The MEX6800 MPU Module is the heart of both the EXORciser Debug system and the user's system under development. That is, the MPU Module provides both the system-clock and the Mc6800 Micro-processing Unit (MPU) for the EXORciser Debug and the user's system. The MPU Module also automatically initiates are EXORciser restart.

operation when power is first applied to the EXORciser.

The clock circuit, in addition to generating the basic EXORciser timine signals, roundes the EXORciser with the capability of refreshing dynamic memories and working with slow memories. The dynamic memories are refreshed on a cycle stealing basis. In working with slow memories, the MPU Module stretches the clock pulse to allow the two-way transfer of data.

The McSe000 Microprocessing Unit is an 8-bit parallel decirc capable of addressing 645 bytes of memory. It addresses its input and output devices as memory. The MPU provides the EXORciser with 72 variable length instructions and the capability of responding to real time interrupt signals. With the exception of the EXORciser clock, the system restart, and the Data Bus Erable signal (delayed), the MPU Module aponesy executivities and McSe00 Microprocessing.

- Unit with unlimited drive capability.

 Provides MPU and Clock for the EXORciser Debug and User's
- Crystal-Controlled 1 MHz Clock
- Provisions for an External Clock Input
- Provisions for an External Clock Input
 Automatic Restart Capability
- Dynamic Refresh Capability on a Cycle Stealing Basis
- Canable of Working with Slow Memories Through Stretching the

EXORciser MPU MODUL E

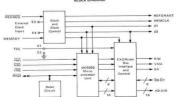
EYOReine



MPU MODULE



BLOCK DIAGRAM



MODULE SPECIFICATIONS

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification Memory Size Capability		Value 65,536 bytes muximum	
Instruction Set		72 variable length instructions	
Interrupts		Maskable and non-maskable real-time interrupts Software interrupt	
Clock Signal		1 MHz; provision for external clock between 100 kHz and 1 MHz	
Input Control Sign Logic "0" Logic "1"	als	TTL Voltage Compatible 0.0-0.8 V 2.0-5.25 V	
Address Bus and R Logic "0" Logic "1" Off-State Leaks		0.005 V 2.45.25 V -40 µA	
Data Bus Input Logic "0 Input Logic "1 Output Logic " Output Logic " Output Off-Sta	0.	Three-tasts TTL voltage compatible (0.00.8 V -7.000 µ at 0.4 V 1 2.05.25 V 2.05.25 V 25.62 V 25.	
Output Control Si Logic "0" Logic "1"		TTL voltage computible 0.0 0.4 V 2.45.25 V	
Operating Temper	ature	0 to 70°C	
Power Requireme		5 Vdc at 700 mA	
Dimensions Width Height		9.75 in. 5.75 in. 0.062 in.	

FXORciser INTERFACE SIGNALS

The MEX6800 MPU Interface Module interfaces directly with the EXORciser bususing the following signals. The MPU Module, through these signals, controls the operation of the EXORciser.

Data But (ÎO-D7) — These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers and receivers on the MPU Module are three state devices. The data bus drivers and receiver on the MPU Module are their off or high impedance state except when this module is performing a memory read or write operation.

Address Bus (A0-A15) — These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers. Read/Write (R.W) — This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state. Valid Memory Address (VMA) — This line, when high,

indicates that the address on the bus is valid.

Memory Clock (MEMCLK) — This is the basic clock
signal used by the MPU Module to generate its \$1 and \$2
non-overlapping clock signals.

Phase 1 (o1) Clock — This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.



Phase 2 (¢2) Clock — This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module

Bux Available (BA) — The Bux Available signed will commally be a low level. When activate, it will go high indicating that the address has it available. This will occur if the HBII line is 1500 or the McO800 MPI in in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU double three-state output drivers will go to their off state and other outputs to their normally insertive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

Interrupt Request (IRQ) — This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU.

will begin the interrupt sequence.

Non-Maskable Interrupt (NMI) — This level sensitive inport, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

Reset — This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser Debug and the user's

system.

Three-State Control (TSC) — This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is strapped to ground on this module, but is available for

Refresh Request (REFREQ) — This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the 61 and 62 clock signals with 61 high and, through the Refresh Grant command, instructs the initiating memory module to refresh isself.

Refresh Grant (REFGRANT) — The MPU Module, on receiving a Refresh Request input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Rody (MEMROY) — This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the 01 and 02 clock signals with 02 high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level, Half — When this input is low, all activity in the MC6800.

MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the Halt line must not occur during the last 250 ns of \$01. To insure single instruction operation, the Halt line must go high for one \$01 clock pulse.





MEX6812-1

Advance Information

2K STATIC RAM MODILI F

The MEXB812-1 2K Static RAM Module, consisting of 16 Hischand MOS memory devices, provides the EXDR6sies with 2088 x 8 bits of earlbom access memory. This memory is organreceivers and the base address selection southers between the Static RAM Module with the EXDR6sies bus. The address selection southers permit the user to select the base location address of memory array in 1K forte increments (1000; 100; 2004, etc.). The collection of the control of the control of the control of our selection of the control of the control of our selection of our sele

- ory contents by inhibiting the memory write function).

 TTI Voltage Compatible High Impedance Inputs
- TTL Voltage Compatible High Impedance In
- Three-State Data Outputs
- 2048 x B Bits of Static N-Channel MOS Memory in Two 1024-Byte Arrays
- Switch-Selectable Base Location Address for Each Memory Array
- 500 ns Memory Access Time
 Each Array Switch-Selectable as a RAM or ROM (RAM Protected by Inhibiting Memory Write Function)

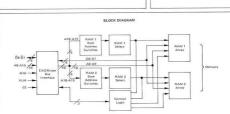
EXORciser 2K STATIC RAM MODULE

EXORciser



2K STATIC RAM MODULE





MODILI E SPECIFICATIONS

(Mars: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification	Value
Memory Type	N-channel MOS static RAM
Memory Organization	2048 x 8 bits organized into two 1024 x 8 bit arrays
Access Time	500 ns
Input Signals Logic "0" Logic "1"	TTL voltage comparible 0.0-0.55 V (-200 µA max at 0.4 V) 2.0-5.25 V (25 µA max at 5.25 V)
Data Bus Input Logic "0" Input Logic "1" Output Logic "0" Output Logic "0" Output Logic "1" Output Off State Leakage Current	Three-state TTL, voltage compatible (0.0 85 V I 1.000 JA max at 0.4 VI 2.0 5.25 V I 25 JA max at 0.4 VI 2.0 5.25 V I 25 JA max at 5.25 VI 2.5 V max at 40 mA through a resistor to ground 2.6 V min at 10 mA through a resistor to V _{CC} 100 JA max at 2.6 V
Operating Temperature	0 to 70°C
Power Requirements	5 Vdc at 1 A max
Dimensions Width Height Thickness	9.75 in. 5.75 in. 0.062 in.

EXORciser INTERFACE SIGNALS

The MEX6812-1 2K Static RAM Module interfaces directly with the EXORciser bus using the 8-bit bi-directional data bus, the 16-bit address bus, read/write fine, 62 clock line and valid user's address line. These lines permit the EXORciser to have complete control over the 2K Static RAM Module.

Data Bus (DD-D7) — These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the 2K Static RAM Module. The data bus receives on the 2K Static RAM Module are continually enabled to receive data. The data bus drivers on this module are continually enabled to receive data. The data bus drivers on this module are in their off or high impedance state except when the module is selected during a memory read operation.

Address Bus (A0-A15) — These 16 lines, when enabled, transfer the selected memory address to the 2K Static RAM Module. The MPU Module controls the operation of these three-state lines. Read/Write (R/W) — This MPU Module output signal

indicates to the 2K Static RAM Module whether the EXORciser is performing a memory read operation (high) or write operation (low). The normal standby state of this signal is read (high). Also, when the MC6800 MPU on the MPU Module is halted, this signal will be in a read state.

Valid User's Address (VUA) — This signal indicates that the address on the address bus is valid and the EXORciser is not addressing EXbug Jupper 4K bytes of

memory).
Phase 2 (o2) Clock Signal — This signal is between 100 kHz and 1 MHz, and is used to synchronize the transfer of data on the data bus. This signal is controlled by the MPI1 Mindules.



MFX6815-1

Advance Information

SK DANVMIC BAW WODIN E

The MEXBITS 18 Cryvame RAM Models consisting of 18 MCMM0502L. No Channel memory circuit, provides the EXPORTION with 8187 at 8 bits of dynamic another access memory arrays. This memory is cryparallel risks to seem only address selection with the control of the

In systems using multiple 8K Dynamic RAM Modules, one module (master refresh module) is used to control the memory refresh operation of the

other modules (slave refresh modules).

The 8K Dynamic RAM Module can be used with an external battery backup circuit to provide refreshing when power is removed from the primary of the EXORciser power supply transformer. This refresh capability

- enables the module to retain its data during a power off condition.

 TTL Voltage Compatible
- Three-State Data Bus
- 8192 x 8 Bits of Dynamic MOS Memory in Two 4096-Byte Arrays
 Switch-Selectable Base Location Address for Each Array
- Each Array Switch-Selectable as a RAM or ROM (RAM Protected by Inhibiting Memory Write Function)
- Inhibiting Memory Write Function)

 Cycle-Stealing Memory Refresh

 Memory Refresh Capability During Power-Fail Condition when Using
- External Battery Backup
 Bus Driver Capability

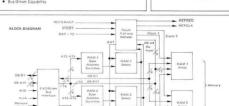
EXORciser 8K DYNAMIC RAM





SK DYNAMIC RAM MODULE





MODULE SPECIFICATIONS

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification	Value	
Memory Type	N-channel MOS dynamic RAM	
Memory Organization	8192 x 8 bits organized into two 4096 x 8 bit arrays	
Read Access Time	350 ns from memory clock typical, 400 ns maximum	
Cycle Time	750 ns typical, 1 µs minimum	
Input Signals AO-ATI Logic "O" Logic "1" AT2-AT5 and Control Lines Logic "0" Logic "1"	TTL unlarger compatible 0.5 0.8 V (400 µA max at 0.5 V) 2.05.25 V (10 µA max at 4.5 V) 0.0 0.85 V (200 µA max at 0.4 V) 2.05.25 V (15 µA max at 0.4 V)	
Data Bus Input Logic "0" Input Logic "1" Output Logic "0" Output Logic "0" Output Logic "1" Output Logic "1"	Three-state TTL voltage compatible (0.0.85 V I . 200 J. Ama vas (0.4 V) 2.0.5.25 V (35 J.A max at 5.2 V) (0.5 V max at -0.0 An through a resistor to ground 2.6 V min at -10 mA through a resistor to VCC (100 J.A max at 2.6 V	
Operating Temperature	0 to 70°C	
Power Requirements	5 Vdc at 860 mA 12 Vdc at 300 mA*	
Powerfail Refresh	5 Vdc not used 12 Vdc at 25 mA maximum	
Dimensions Width Height Thickness	9.75 in. 5.75 in. 0.002 in.	

*Power consumption is dependent on the number of memory accesses of the module.

EXORciser INTERFACE SIGNALS

The MEX6815-1 8K Dynamic RAM Module interfaces directly with the EXORciser bus using the following signals. These signals permit the EXORciser to have complete control over the BK Dynamic RAM Module.

Data Star (ID-D7) – These eight bidirectional lines when enabled, provide a two way transfer of data between the MPU Modale and Next Yuranfer of data between the MPU Modale and Next Receivers and the SK Dynamic RAM Module are three-tate devices. The data bus drivers and receivers on the BK Dynamic RAM Module are three-tate devices. The data bus drivers and receivers are in their off or high impedance state except when this module is selected in a memory read or a memory virite operation.

Address Bus (A0-A15) — These 16 lines, when enabled, transfer the selected memory address to the BK Dynamic RAM Module. The MPU Module controls the operation of these three-state lines.

Read/Write (R/W) — This MPU Module output signal indicates to the BK Dynamic RAM Module whether the EXOREiser is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the MPU Module is halted, this signal will be in the read state.

Valid User's Address (VUA) — This signal indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program (upper 4K bytes of memory). Memory Clock (MEMCLK) — This is the basic clock signal used by the MPU Module to generate its \$1 and \$2 clock signals. The BK Dynamic RAM Module uses this signal to control its timing.

Refresh Clock (REFCLK) — This clock signal is generated by the BK Dynamic RAM Module to refresh its memory. In systems using multiple BK Dynamic Modules, the master refresh module uses this signal to refresh the slave refresh modules.

Stand By (STDBY) — This line is a low level during a powerfail condition and a high level during normal EXORciser operation.

Refresh Request (REFREQ) — This signal, when present, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the ol and of clock signals with of high and, through the Refresh Grant command, ristructs the RK Dynamic RAM Module to refresh its memories. The 8K Dynamic RAM Module onereates this cubic acrossimately once every 60 gs.

Refresh Grant (REFGRANT) — This signal, when present, instructs the 8K Dynamic RAM Module to refresh its memories. Battery + 12 (BAT + 12) — This is the 12-volt source

for the MCM6605-1 memory circuits.



MEX6820 MEX681C

EXORciser
INPUT/OUTPUT
MODULE
and
I/O INTERCONNECTION

CABLE





Advance Information

INPUT/OUTPUT MODULE

AND I/O INTERCONNECT CABLE

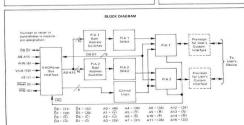
The MEX6820 Input/Output Module and the MEX68IC I/O Interconnection Cables provide the user with an integral means of interfacing his defined process or peripheral device to the EXORciser.

- Four 8-Bit Input/Output Ports for Peripheral Interfacing
 Eight Individually Controlled Interrupt Lines Four of Which
 - May Be Used as Peripheral Control Output Lines
- Three-State TTL Voltage Compatible Inputs and Outputs
 Switch-Selectable Base Location Address for Each of the Two
- MC6820 Peripheral Interface Adapter Devices

 Program Controlled Maskable Interrupt Capability
- Four Programmable Control Registers
- Four Programmable Data Direction Registers
- Each MC6820 Peripheral Interface Adapter Addressed as Memory
- Bus Drive Capability
 Predrilled Wirewrap Area on Module for 14, 16, and 24-Pin Wire-
- wrap Sockets with 300 or 600-Mil Spacing on Pin Centers

ORDERING INFORMATION

Order two MEX68IC Input/Output Interconnection cables with each MEX6820 Input/Output Module.



MODULE SPECIFICATIONS

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification	Value		
Input Signals Logic "0" Logic "1"	TTL voltage compatible 0.0-0.85 V (-200 µA max at 0.4 V) 2.0-5.25 V (25 µA max at 5.25 V)		
Data Bus Input Logic "0" Input Logic "1" Output Logic "1" Output Logic "0" Output Logic "1" Output If:State Leakage Current	Three-state TTL voltage compatible 0.0-0.85 V (-200 µA max at 0.4 V) 2.0-5.25 V (28 A max at 5.25 V) 0.5 V max at 40 mA through a resistor to ground 2.6 V min at -10 mA through a resistor to V _{CC} 100 µA max at 2.6 V		
MC6820 Peripheral Interface Adapter Signals* PAO-PAT Input/Output Lines PBO-PBT Input/Output Lines CA1, CA2, and CB1 Control Signals CB2 Control Signal IROA and IROB Signals	TTL voltage compatible Three-state TTL voltage compatible TTL voltage compatible Three-state TTL voltage compatible TTL voltage compatible		
Operating Temperature	0 to 70°C		
Power Requirements	5 Vdc at 2 A max		
Dimensions Width Height Thickness	9.75 in. 5.75 in. 0.062 in.		

*See MC6820 data sheet for specifications on these signals.

INPUT/OUTPUT MODULE

The MEX6820 Input/Chupat Module provides the use with a flexible means of interfacing the EXORGES with his defined process or peripheral device, either by directly interfacing with the two MC6820 Peripheral Interface Adapters (PlAst in the module or by constructing outstom-tice interface consists between the PlAst And the user's device. This interface is simplified by the TTL voltage computing of the Plant to moderate the process of the

The EXORciser's MC6800 Microprocessor addresses each PIA on the Input/Output Module as if it were memory. Switches on the module allow the user to select the base memory address for each PIA.

I/O INTERCONNECT CABLE

The MEXSBIC I/O Interconnect Cable permits the user to connect an Input/Output Module to a peripheral One end of this flatribbon cable is terminated with a 50-pin flatribbon connector; the other end is not terminated. Each I/O Module requires two cables.

EXORciser INTERFACE SIGNALS

The MEX6820 Input/Output Module interfaces directly with the EXORciser bus using the eight-bit bi-directional data bus, the 16-bit address bus, an interrupt request line, read/write line, \$2 clock line, valid user's address line and

reset line. These lines permit the EXORciser to have complete control over the Input/Output Module.

Bi-Directional Data Bus (Do-D7) — These eight bi-

directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the I/O Module. The data bus drivers and receivers on the I/O Module are three-state logic devices. The data bus drivers and receivers are in their off or high-impedance state except when this module is selected in a memory read operation or remover write operation.

Address Bus (A0-A15) — These 16 lines, when enabled, transfer the selected memory address to the I/O Module. The MPU Module controls the operation of these threestate lines.

Read/Write (R/NI) — This MPU Module output signal indicates to the I/O Module whether the EXORciser is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MC6800 MPU on the MPU Module is halted, this signal will be in the read state.

Valid User's Address (VUA) — This signal indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.

Phase 2 (¢2) Clock Signal — This signal is between 100 kHz and 1 MHz and is used to synchronize the transfer of data on the data bus. This signal is generated by the MPU Module.

Reset — This signal is used to restart the MC6800 MPUand reset the EXORciser from a power down condition or when the EXORciser RESTART switch is actuated. This signal resets and initializes the two MC6820 PIAs on the I/O Module.

Interrupt Request (IROI) — This level sensitive input, on going love, requests that an interrupt sequence be generated within the machine. The MCOSBO MPU will wait until it complets the current instruction that it is executing before it recognizes the request. At that time, if the interrupt mask bit in the MPU condition code returns in our set (interrupt masked), the MPU will begin the interrupt than the machine of the MPU will begin the interrupt masked), the MPU will begin the interrupt masked.

user's option, are capable of generating an TRQ signal.

PERIPHERAL INTERFACE LINES

The user has the option of connecting the MC6820 PIA interface lines directly to the user's peripheral feederies or of constructing custom interface circuitry between the PIA and the user's peripheral device. These lines are the eight peripheral imputious to lines PBO-PBF2, and the four control lines CAF, CAC, CBI, and CBI2 for each PAF. Returned for a description and detailed specifications of these signals.



MEX68WW

Advance Information

UNIVERSAL WIREWRAP MODULE

The MEX68WW Universal Wirewrap Module permits the user to construct and incorporate his custom circuits into an EXORciser emulated system. The power bus and ground bus printed wiring are incorporated on the module. The power bus connects to pins A, B, C, 1, 2, and 3. The ground bus uses pins W, X, Y, 41, 42, and 43.

The module has provision for standard 14 16 and 24-pin wirewrap sockets with 300-mil spacing on pin centers. These sockets may be installed in any combination including 75 14-pin sockets. The module also has provision for mounting two 50-pin flatribbon wirewrap connectors.

- Standard Size EXORciser Plug-In Module
 - · Compatible with the EXORciser Bus
- · Standard Pin Spacing for 75 14-Pin Wirewrap Sockets
- Provisions for Two 50-Pin Flatribbon Cable Connectors Permits User to Incorporate Custom Circuits into a System

EXORciser WIREWRAP MODULE





MODULE SPECIFICATIONS

Width	9.75 in.	
Height	5.75 in.	
Thickness	0.062 in.	







Advance Information

EXTENDER MODULE

The MEX6BXT Extender Module permits the user to extend any EXORciser Plug-in Module for servicing, testing, troubleshooting, or debugging. This module has clip-on test points to provide the user access to the EXORciser bus.

- Extends Any EXORciser Plug-in Module for Testing, Trouble-shooting, and Debugging
- . Interfaces with All EXORciser Plug-In Modules
- Compatible with the EXORciser Bus
- Provides Clip-on Test Points for All EXORciser Bus Signals

EXORciser EXTENDER MODULE

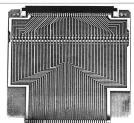
EXORciser



MODULE SPECIFICATIONS

Width	
Height	

t 9.00 in ness 0.062 in





M6800 RESIDENT SOFTWARE

Advance Information

EXORciser RESIDENT EDITOR and RESIDENT ASSEMBLES

M6800 RESIDENT SOFTWARE

The optional M6800 Resident Software, along with the M6800 ReVORcien's EXUDE Firmaure, allows the EXORicien user to develop his system software in real-time with his pringheral devices incorporated into the system. This means that the user can prepare, assemble, and debug his system software in its actual working empearance of the system of the system software, while the EXORcien's EXUDE Firmaure is used to debug the system handware as well as the software.





M6800 RESIDENT EDITOR

The M6800 Resident Editor may be used to create or modify alphanumeric text. In particular, the Editor gives the user an easy means to create and modify source programs for input into the M6800 Resident Assembler. This interactive Editor offers character, line, and character string commands.

- mig commission
- Memory Sizing Capability
- Insert or Delete Lines
 Insert. Delete or Modify Character Strings
- Command Chaining
- Co-Resident with the M6800 Assembler or Stand Alone

M6800 RESIDENT ASSEMBLER

The MBGIO Resident Assembler may be used with the MBGIO EXPOSITION to translate MBGIO SCOT Programs to machine legisjuer, This assembler is a two-pass assembler programs trace — once to build a yeller legislate of the many conditions to the program trace — once to build a yeller legislate and a second street to produce the assembled output. Only pass two with a series and the use of the many conditions the programs, the forward references will be flagged with a nerry and the user is required to pass to the other programs, the forward references will be flagged to the programs, the forward references with a refer and the user is required to pass to the other programs, the forward references with the flagged to the programs, the forward references with the representation of the programs of

- Two-Pass Assembler
- Limited One-Pass Capability
 Can Be Co-Resident with the M6800 Resident Editor
- or Stand Alone
 Compatible with Motorola's Cross Assemblers

EXbuo FIRMWARE

The EXbug Firmware is an integral part of the M6800 EXORciser. This firmware allows the user to load the M6800 Resident Assembler and Editor into the EXOR-ciser and to verify that the Resident Software was correctly loaded, and to debug the user's system hardware and software. Also, this Firmware is used to print and/or punch the data stored in the EXORCISER memory.

RESIDENT SOFTWARE REQUIREMENTS

- EXORciser
- 8K bytes of RAM minimum
- TTY (20 mA neutral loop current) or RS-232C data terminal with automatic reader/punch control

ORDERING INFORMATION

The user has the option of ordering the Resident Software in a stand-alone package or ordering the software with 8K bytes of memory. The user can also select the media on which he wishes to receive his Resident Software. Table 1 shows the complete range of options, and the Part Number to be used when ordering.

TABLE 1 - M6800 RESIDENT SOFTWARE OPTIONS

Option	Description	Media	Part Number
1	Resident Assembler/Editor (Stand Alone)	Cassette	M68X AE6812A0
2	Resident Assembler/Editor with four 2K Static RAM Modules	Cassette	M68XAE6812A2
3	Resident Assembler/Editor with one 8K Dynamic RAM Module	Cassette	M68XAE6812A8
4	Resident Assembler/Editor (Stand Alone)	Paper Tape	M68XAE681286
5	Resident Assembler/Editor with four 2K Static RAM Modules	Paper Tape	M68XAE681282
6	Resident Assembler/Editor with one 8K Dynamic RAM Module	Paper Tape	M68X AEGR12RS
7	Resident Assembler/Editor (Stand Alone)	G.E. Timeshare	M68XAE6812C0
8	Resident Assembler/Editor with four 2K Static RAM Modules	G.E. Timeshare	M68XAF6812C2
9	Resident Assembler/Editor with one 8K Dynamic RAM Module	G.E. Timeshare	M68XAE6812C8
10	Resident Assembler/Editor (Stand Alone)	Floppy Disk	M68XAE6812D0
11	Resident Assembler/Editor with four 2K Static RAM Modules	Floppy Disk	M68XAE6812D2
12	Resident Assembler/Editor with one 8K Dynamic RAM Module	Floppy Disk	M68XAF681208