MOTOROLA
Semiconductor Products Inc.

AN-803
Application Note

THE EFFECT OF EMITTER-BASE AVALANCHING ON HIGH-VOLTAGE POWER SWITICHING TRANSISTORS

Prepared by
Al Pshaenich
Senior Applications Engineer

Reverse biasing the base of a power transistor during turn-off decreases its turn-off switching losses. This application note investigates the effect of increasing the bias into avalanche on the life, switching speeds and inductive turn-off stresses on several types of high-voltage switching power transistors.

With the advent of a new generation of high-voltage, high-speed silicon power switching transistors, applications of greater than 20kHz operation are readily achievable. To obtain these bandwidths, certain circuit techniques have been developed to reduce the switching times and thus switching losses, the major dissipative effect in high frequency applications. Of the two switching times, turn-off time (t_{off}) is greater than turn-on time (t_{on}) and its reduction is of greater importance. The usual techniques described in the literature to minimize t_{off} are to reverse bias the emitter-base junction and allow a low impedance path for depleting or "sweeping out" the stored charge in the collector-base region. The result can be a great reduction in storage time (t_s) and also a substantial reduction in fall time (t_f). Minimizing storage time is of importance in pulse width modulation circuits such as switching regulators where regulation limits can require defined pulse width variations. Also, in switching applications requiring two or more transistors, (½ bridges, full bridges, push-pull inverters, etc.), low t_s (and many times matched t_s) is required to prevent transformer biasing. Since the turn-off switching losses are proportional to fall time, its need for reduction is apparent.

In addition to effecting turn-off times, reverse biasing the emitter-base also effects the RBSOA (Reverse Bias Safe Operating Area) capability of a transistor when switching clamped inductive loads. Depending on the process type and the current levels involved, this capability can increase with increasing off biases.

"Reverse bias" can be derived by applying a reverse voltage to the base through a low impedance source, resulting in a negative base current I_{B2} flowing, or through a reverse constant current source. Some transistor manufacturers specify turn-off switching times with a specified reverse voltage $V_{BE\ (off)}$, others with a reverse current I_{B2}. Either method can simulate the "real world" as some applications use a base-emitter clamp (to a negative supply for NPN transistors) to reduce turn-off times and others use a voltage source through a base-limiting resistor, as in transformer coupled circuits. $V_{BE(off)}$ is generally specified at -5.0V, however, for some devices, RBSOA can be derived with off biases up to the specified maximum emitter-base voltage rating of -9.0V. I_{B2} is usually selected at some multiple of I_{B1} (the forward base current), be it I_{B1} or two or four I_{B1}, etc. By increasing the off bias, even faster turn-off times can be obtained.

The question arises as to how much reverse bias can be applied to the device before adverse effects, if any, occur. Most power devices have maximum emitter-base voltage rating V_{EBO} of from 5 to 9V, implying that these ratings should not be exceeded. Some of the literature state that the emitter-base junction can be reversed biased into avalanche without degrading the device, but this premise is not supported with any documentation or test results.

Other literature states not to avalanche as this could possibly cause degradation of the device over a long period of time, particularly in a reduction of gain. Yet in some applications, notably TV horizontal deflection circuits, avalanching of the emitter-base is commonplace, although this is the result of generating a controlled storage time and not as a planned design.

It is the intent of this article to clarify this question by life testing a number of devices under emitter-base

avalanche conditions and determine if any detrimental effects occur.

Five different high-voltage "switchmode" devices were tested, three discretes and two darlingtons, encompassing two different but similar processes — triple diffused and epi-collector double diffused.

The parameters measured are h_{FE}, collector-emitter breakdown voltage $V_{CEO(sus)}$, emitter-base breakdown voltage (BV_{EBO}) and collector cutoff currents (I_{CEO} and I_{CBO}), and emitter cut-off current (I_{EBO}).

Additionally, turn-off times for resistive and inductive loads and RBSOA curves as a function of off-bias are shown, allowing circuit design optimization. And finally, seven base drive circuits which can avalanche the device under test (D.U.T.) are described with their cost/performance trade-offs.

LIFE TEST

All of the five product lines were life tested in the test circuit of Figure 1 using a resistive 10 ohm load. Additionally, an inductive load life test was performed using the 2N6250. The fixture consists of a CMOS oscillator (G_1 and G_2) clocking a CMOS decade counter whose outputs sequentially address the ten drivers and devices under test (D.U.T.). Thus, each D.U.T. is pulsed at a 10% duty cycle for approximately 30 μs, the period of the oscillator frequency (33kHz). Base currents I_{B1} were as listed in the following Table 1 to drive the 5A collector current and off bias was set large enough to ensure E-B avalanching. The resulting I_{B2} pulse was about 10μs wide at its base (as determined by the R_1C_1 differentiating circuit); thus the devices were avalanched for about a 3% duty cycle.

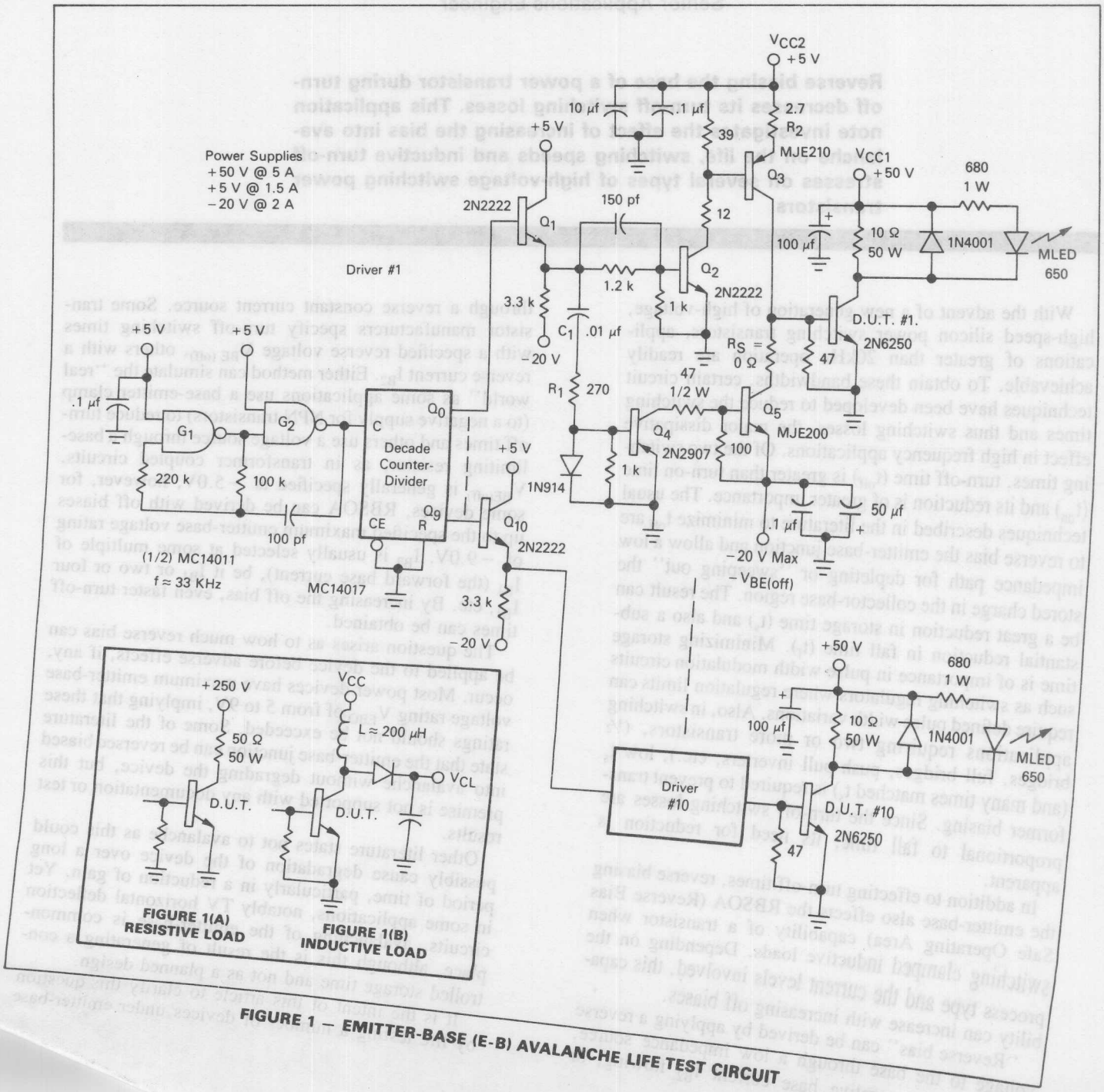


FIGURE 1 — EMITTER-BASE (E-B) AVALANCHE LIFE TEST CIRCUIT

Eight of the ten devices were emitter-base (E-B) avalanched with the listed reverse bias; the two remaining transistors were not biased and were used as a parameter standard. Additionally, another transistor was used as a measurement standard, never being powered, but always remeasured when the test devices were measured. This ensured measurement repeatability. For all tests, h_{FE} (and the other parameters) were remeasured after 1 day, 1 week, 3 weeks, 6 weeks, etc.

As expected, for the discrete devices, the greatest reduction in h_{FE} occurred at low collector currents with high-current h_{FE} having minimal change (Figures 2A, B&C). About 50% of this change occurred within the first 24-hour test period. In general, the two non-avalanched devices also had a proportional reduction in h_{FE} after life testing indicating a transistor "burn-in" period. Any reduction in h_{FE} beyond the life test periods of from 500 hours to 1160 hours respectively can be assumed to be due to "aging" since the non-avalanche devices also had reduced h_{FE}.

Measurement repeatability on the one standard, non-powered device was within 1 to 4% for the five product lines. After all these corrections were factored in, the approximate overall reduction of h_{FE} as a function of collector current is illustrated in Table 2. Note that the discrete devices have a relatively large reduction in h_{FE} at 10mA — about 15 to 25% — and a small change, if any, beyond 1A. The Darlingtons, on the other hand, showed a minimal change in h_{FE} (Figures 2D & E) with the two respective non-avalanche units showing similar reductions in h_{FE}. Thus, any change in the illustrated h_{FE} is the result of the differences between the avalanched and non-avalanched devices and will only be as accurate as the respective measurements. With the limited sample size (two) of the non-avalanched units, there can be some question as to the accuracy of the "modified" h_{FE}. However, based on the life testing of these five high-voltage double and triple diffused power transistors where burn-in and aging effects were noted, it could be concluded that no appreciable change in medium- and high-current h_{FE} will occur when the devices are emitter-base avalanched.

The other parameters measured proved even more consistent. Collector emitter breakdown voltages, $V_{CEO(sus)}$, were measured prior to testing and remained within about ± 5V after testing, any change being attributed to measurement accuracy. Similarly, the emitter-base breakdown voltage (BV_{EBO}) showed no degradation being within ± 0.1V of the initial reading. No drastic changes in cut-off currents, I_{CBO} and I_{EBO}, were noted, varying at the most by ± 20% from the typical value of about 1μA.

E-B AVALANCHE LIFE TEST CONDITIONS

TABLE 1

D.U.T.	TYPE	Spec I_C (A)	Spec V_{EB} (V)	Spec $V_{CEO(sus)}$ (V)	$V_{BE(off)}$ (V)	I_{B1} (A)	$I_{B2(pk)}$ (A)	Hours
2N6250	NPN H.V. Discrete	15	6	275	−20	1	7	1130
2N6545	NPN H.V. Discrete	8	9	400	−15	1	6	530
2N6547	NPN H.V. Discrete	15	9	400	−12	1	6	1570
MJ10011	Darlington Horiz. Defl.	8	5	700	−12	0.25	5	1160
MJ10001	Darlington H.V.	8	8	400	−14	0.25	4	500

% REDUCTION IN h_{FE} DUE TO E-B AVALANCHING

TABLE 2

D.U.T. \ I_C	10 mA	100 mA	500 mA	1 A	3 A	4 A	5 A	8 A	10 A	15 A
2N6250	−25	−5	—	−1	0	—	0	—	0	—
2N6545	−20	−20	—	−5	0	—	0	0	—	—
2N6547	−15	−10	—	−3	0	—	0	—	0	0
MJ10011	—	0	0	0	—	0	—	0	—	—
MJ10001	—	0	—	0	0	—	0	0	—	—

FIGURE 2(A) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1130 HRS.

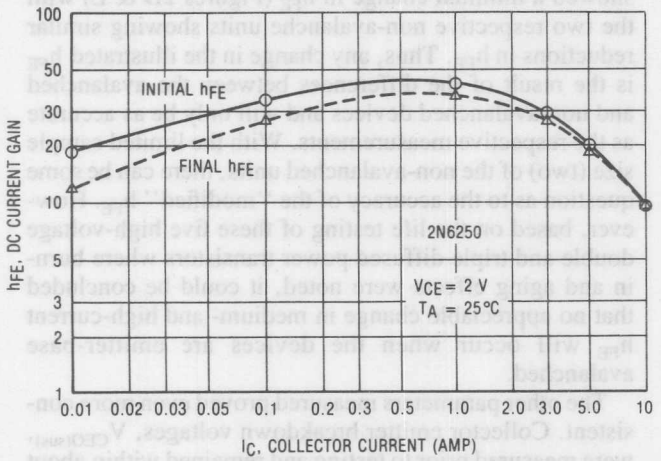


FIGURE 2(B) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 530 HRS.

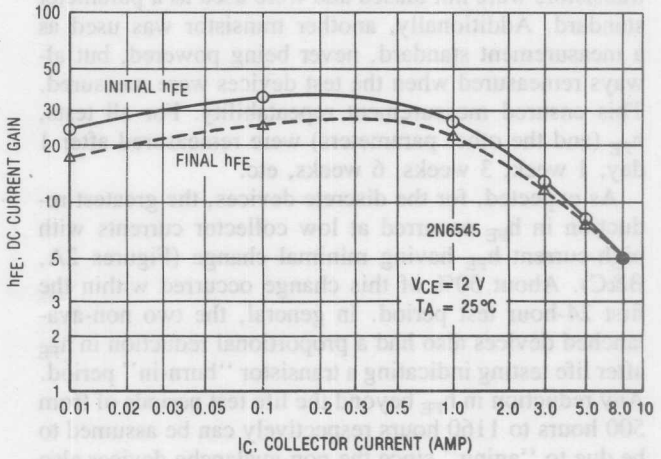


FIGURE 2(C) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1570 HRS.

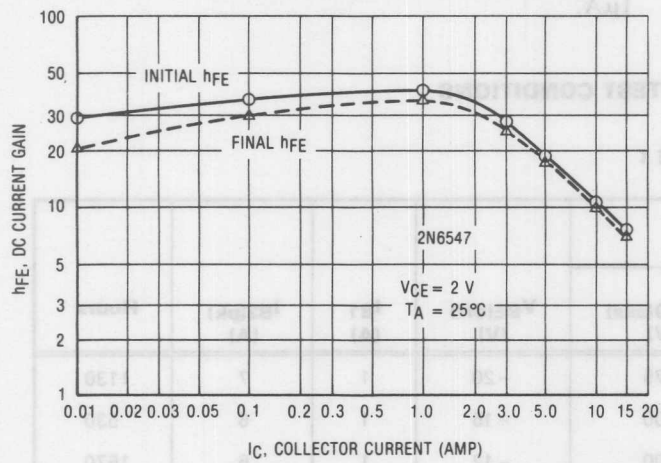


FIGURE 2(D) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1160 HRS.

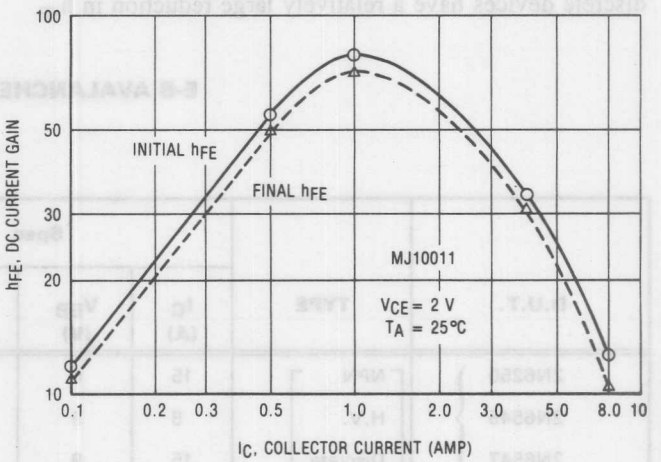
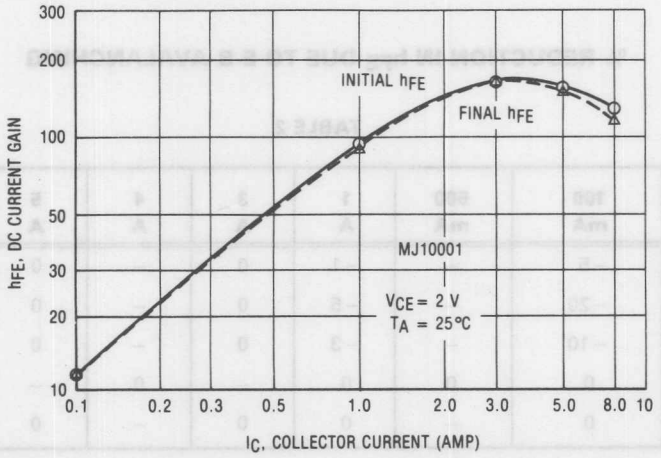


FIGURE 2(E) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 500 HRS.



RBSOA TEST

In addition to performing life tests with a resistive load, a 330 hour clamped inductive load life test was performed on 10 samples of the 2N6250 to determine if avalanching had any effect on this type of load. The test circuit was similar to the resistive load life test circuit (Figure 1) with the load now being a 100μH inductor (collector current was ramped up to 5A pk) clamped by a fast recovery rectifier to a 250V supply. Five pairs of drivers were driven by a 5-stage counter resulting in a 20% duty cycle operation. As in the previous test, two of the D.U.T.'s (standard) had zero volts off-bias and of the remaining eight devices, three had $V_{BE(off)}$ of −5.0V and five were run well into avalanche with $V_{BE(off)}$ of −20V. RBSOA characterization was performed before and after the life test to see what effect off-bias had on the turn-off energy capability. This test was performed with off-biases of −5V, −15V and −20V. Additionally, three non-life test devices were similarly characterized for RBSOA and two devices were not tested at all but simply used as an h_{FE} measurement/aging standard. Using the same normalized h_{FE} correction as previously, it was found that h_{FE} degraded similar to the resistive load case, i.e., greater low current h_{FE} degradation which was proportional to off-bias, as follows:

I_C / $V_{BE(off)}$	Δ h_{FE}		
	100mA	5A	10A
0 V	0	0	0
−5 V	−3%	0	0
−20 V	−20%	0	0

There also was no change in collector leakage current I_{CES} and collector-emitter sustaining voltage $V_{CEO(sus)}$ within measurement repeatability limits but the change in collector-emitter breakdown voltage (at 100μA) showed some increase after life test. For this small sample size, BV_{CEO} increased after life testing by about 4V, 10V and 50V at $V_{BE(off)}$ of 0V, −5V and −20V respectively.

RBSOA after life testing showed little change; if anything, it increased slightly for the $V_{BE(off)}$ conditions of −15V and −20V.

It should be pointed out that the typical RBSOA capability of the 2N6250 was measured at only one collector current (5A) with the aforementioned off-bias voltages. A detailed RBSOA curve or family of curves should be performed at various collector currents with various off-biases to fully characterize the device. These type of curves are illustrated in Figures 3(A) and (B) for the "Switchmode" transistor 2N6545, Figure 3(A) showing the $V_{BE(off)}$ being the variable and 3(B), I_{B2} the variable. Note that at high collector-emitter voltages, the RBSOA capability increases with off-biases and at high collector currents, it decreases. This is due to switching speed/loss predominating over current crowding (hot spot) effects at high voltage whereas at high current, the opposite results. For this device, using $V_{BE(off)}$ as the variable, the large increase in RBSOA capability at high voltage, nominal currents is readily observable. Both figures were derived with one D.U.T. using a 200μH inductor in a non-destruct RBSOA fixture, a circuit that detects the advent of second breakdown and quickly turns off the power to the D.U.T.

FIGURE 3(A) — TYPICAL CLAMPED INDUCTIVE LOAD REVERSE BIAS SAFE OPERATING AREA (RBSOA) AS A FUNCTION OF REVERSE BIAS VOLTAGE ($V_{BE(off)}$) FOR THE 2N6545

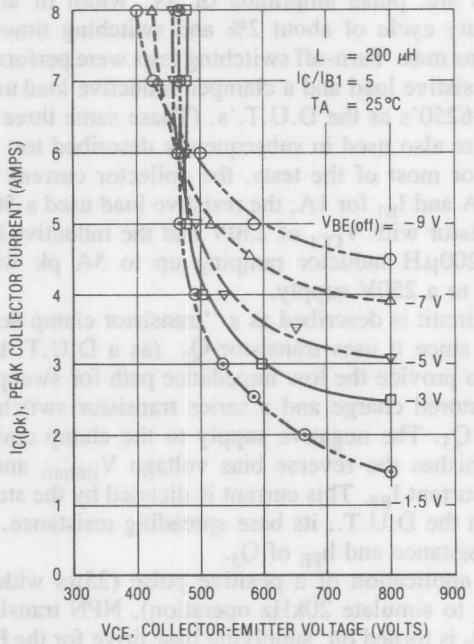
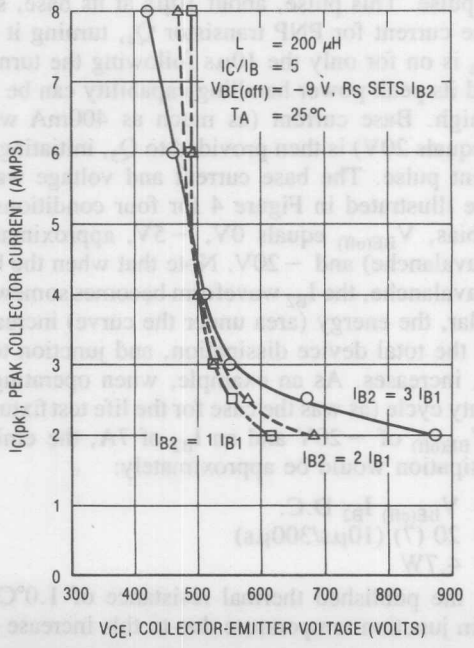


FIGURE 3(B) — TYPICAL CLAMPED INDUCTIVE LOAD REVERSE BIAS SAFE OPERATING AREA (RBSOA) AS A FUNCTION OF REVERSE BASE CURRENT (I_{B2}) FOR THE 2N6545



TURN-OFF TEST, TRANSISTOR CLAMP SERIES SWITCH

Thus far, the effect of $V_{BE(off)}$ including avalanching has been illustrated through life testing and RBSOA characterizing. The initial purpose of this excercise was to show the effect of off-bias on turn-off switching times. This switching evaluation was performed in detail with a circuit identical to one stage of the ten stage life test circuit (Figure 1). Instead of using an input drive pulse derived from the decade counter and emitter follower Q1, a pulse generator was used at the Q1 output node; its specs are: pulse amplitude of 5V, width of about 25μs, duty cycle of about 2% and switching times of about 10ns max. Turn-off switching tests were performed with a resistive load and a clamped inductive load using three 2N6250's as the D.U.T.'s. (These same three devices were also used in subsequently described test circuits). For most of the tests, the collector current was set for 5A and I_{B1} for 1A; the resistive load used a 50Ω, 50W resistor with V_{CC1} of 250V and the inductive load used a 200μH inductor ramping up to 5A pk while clamped to a 250V supply.

This circuit is described as a "transistor clamp series switch" since it uses transistor Q_5 (as a D.U.T. base clamp) to provide the low impedance path for sweeping out the stored charge and a series transistor switch Q_4 to drive Q_5. The negative supply to the clamp emitter (Q_5) furnishes the reverse bias voltage $V_{BE(off)}$ and/or reverse current I_{B2}. This current is dictated by the stored charge in the D.U.T., its base spreading resistance, the series resistance and h_{FE} of Q_5.

Upon application of a positive pulse (25μs wide in this case to simulate 20kHz operation), NPN transistor switch Q_2 is turned on, supplying base drive for the PNP constant current switch Q_3. Transistor Q_3 is operated in this mode to prevent device saturation and thus reduce its own storage time. The emitter resistor R_2 sets the emitter current, and hence, the forward base current for the D.U.T., to about 1.0A. As the applied pulse switches to ground, the R_1, C_1 network produces a negative going, differentiated pulse derived from the trailing edge of the positive pulse. This pulse, about 10μs at its base, supplies base current for PNP transistor Q_4, turning it on. Thus, Q_4 is on for only the 10μs following the turn on pulse and its peak power handling capability can be relatively high. Base current (as much as 400mA when $V_{BE(off)}$ equals 20V) is then provided to Q_5, initiating the I_{B2} current pulse. The base current and voltage waveforms are illustrated in Figure 4 for four conditions of reverse bias, $V_{BE(off)}$ equals 0V, −5V, approximately −15V (avalanche) and −20V. Note that when the bias exceeds avalanche, the I_{B2} waveform becomes somewhat rectangular, the energy (area under the curve) increases and thus the total device dissipation, and junction temperature, increases. As an example, when operating at a 10% duty cycle (as was the case for the life test fixture), with a $V_{BE(off)}$ of −20V and an I_{B2} of 7A, the emitter base dissipation would be approximately:

$$P_{D(E\text{-}B)} = V_{BE(off)}\, I_{B2}\, D.C.$$
$$= 20\ (7)\ (10\mu s/300\mu s)$$
$$= 4.7W$$

Using the published thermal resistance of 1.0°C/W, the rise in junction temperature due to this increase dissipation would be:

$$\Delta t = t_j - t_c = R_{\theta JC}\, P_D = 1.0°C/W\ (4.7W)$$
$$= 4.7°C$$

This calculated temperature rise of about 5°C agrees with the measured temperature of about 6°C for the avalanched devices.

A limited life test of 200 hours was also performed using an inductive load where the I_{B2} duty cycle was increased to about 20%. The results, as expected, was an increase in case temperature and the decrease in low-current h_{FE} was of the same magnitude as prior examples. Thus, when operating at higher E-B duty cycles, the increased dissipation due to emitter-base avalanching should be considered in regard to total device dissipation.

The effect of reverse bias and I_{B2} current limiting resistance on switching times t_s and t_f is illustrated in Figures 5(a) through (e), 6, 7(a) & (b) and 8(a) & (b). Figure 5 defines the turn-off switching times of the 2N6250 with a resistive load and collector current of 5A, Figure 6 shows t_f versus I_B with I_C equal to 2.5A and Figure 7 shows the inductive load conditions. The resistive load switching times for another transistor type, the 2N6547, is illustrated in Figure 8. For all resistive curves, the current limiting resistor R_S is varied from 0 to 8.2 ohms. Figure 5(a) depicts the reduction of storage time t_s as a function of reverse bias and clamp circuit resistance, Figure 5(b) shows the relationship of reverse bias voltage and the resulting reverse base current I_{B2} and Figure 5(c) the change of t_s versus I_{B2}. Note that the I_{B2} − t_s curve is derived from the conditions of Figure 5(a) and is completely independent of R_s as I_{B2} dictates the storage time for this circuit. As could be expected, the lowest storage time occurs for maximum I_{B2}, which in this case is limited by h_{FE} of the clamp transistor Q_5, maximum $V_{BE(off)}$ and minimum clamp circuit impedance. It is also of interest that there is relatively little decrease in t_s beyond about −9V of back bias (Figure 5(a)), 0.9μs compared to 0.7μs at −15V when R_S equals zero. As a relative measurement, t_s was about 16.5μs and 1.7μs with biases of 0V and −5V respectively.

Fall-time t_f curves as a function of $V_{BE(off)}$ and I_{B2} are shown in Figures 5(d) and 5(e) respectively. Of particular interest is that fall-time does initially decrease with increasing bias voltage $V_{BE(off)}$ but actually starts to increase (under low clamp resistance conditions) beyond a particular bias. When R_S equals zero ohms, the valley point was about −9V (relative to where the device avalanched at about −14V). This phenomena is more pronounced when viewing t_s versus I_{B2} (Figure 5(e)); the valley point occurs at about I_{B2} equals −5A peak. The collector current was 5A for this test.

When the collector current was reduced to 2.5A (Figure 6), the valley point was around an I_{B2} of about 3A. And thirdly, this condition is also observable in Figure 7(b), the inductive fall-time test and Figure 8(a), the 2N6547 resistive test.

This increase in collector current fall-time at the point where the reverse base current is approximately equal to the peak collector current is attributed to the emitter having no further influence on the collector current. When I_{B2} equals I_C, I_E is zero, transistor action ceases and t_f is now governed by the reverse recovery process of the collector-base junction.

Also of interest is that the fall-time is minimized when driven by a more ideal current source as shown by the curves of Figures 5(e), 6 & 8(a). Note that for the same I_{B2}, t_f is less for increasing series resistance R_S. Obviously, $V_{BE(off)}$ must be increased accordingly to maintain this current.

Storage time is related to a carrier recombination process and is a measure of the minority carrier lifetime in the base and collector regions[3]; thus, it should be independent of the type of load (inductive or resistive) for the same bias conditions (I_{B1}, I_{B2}, I_C). This is illustrated in the t_s versus I_{B2} curves of the resistive and inductive loads (Figures 5(c) and 7(a)) being approximately equal.

Collector current fall-time for the inductive load proved to be somewhat faster than for the resistive load (Figures 5(e) & 7(b)) for comparable operating conditions (V_{CC} = 250V, R_L = 50Ω, I_C = 5A for the resistive load relative to V_{CL} = 250V, $I_{C(pk)}$ = 5A for the inductive load). This is due to the difference in the transistor effective base widths for the two circuits. For the resistive load line case, the average collector-emitter voltage ($V_{CE(ave)} \approx V_{CC/2}$ for C1 A) is lower than the inductive load line which swings out to V_{Clamp} and thus the depletion layer is narrower, the base width is wider resulting in slower t_{fi}.

2N6250

CONDITIONS: I_{B1} = 1.0 A, I_C = 5.0 A, V_{CC} = 250 V, R_L = 50 Ω, R_S = 0 Ω

(CIRCUIT OF FIG. 1A)

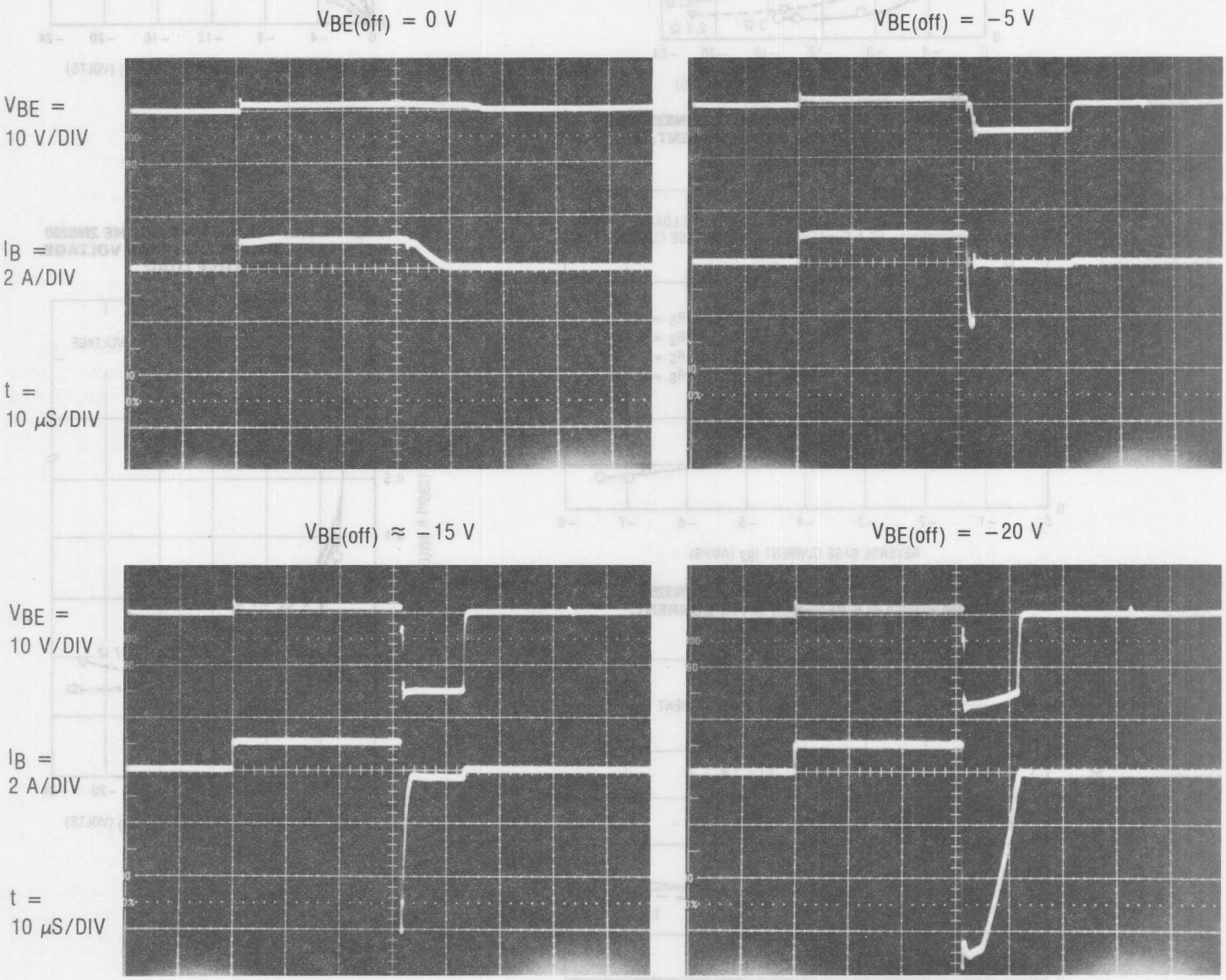


FIGURE 4 — BASE WAVEFORMS OF D.U.T. FOR VARIOUS REVERSE BIASES

FIGURE 5(A) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BIAS VOLTAGE. RESISTIVE LOAD

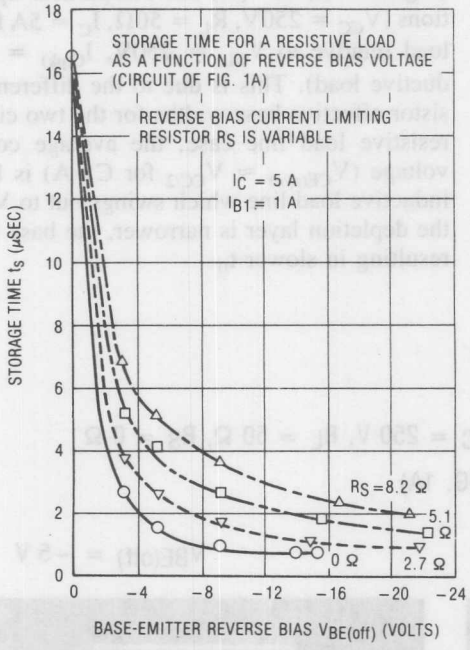


FIGURE 5(B) — BASE INPUT CHARACTERISTICS FOR THE 2N6250

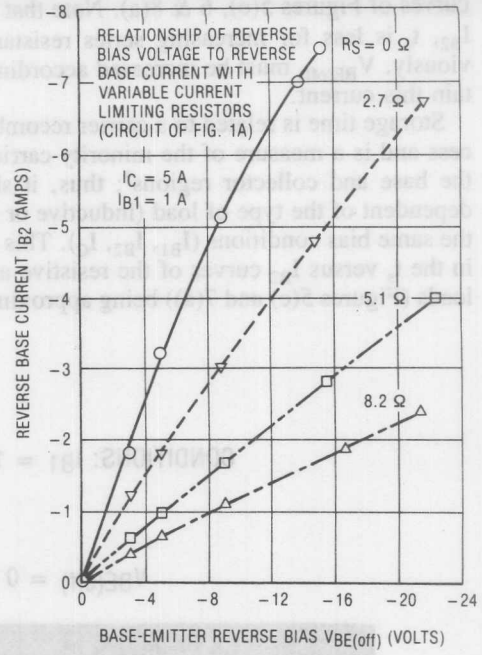


FIGURE 5(C) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. RESISTIVE LOAD

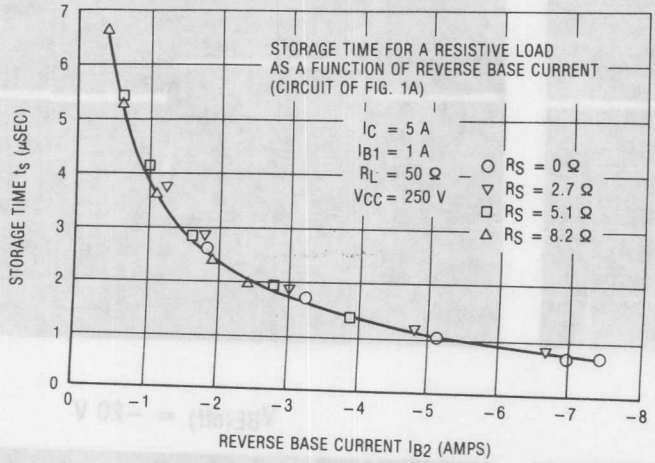


FIGURE 5(D) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BIAS VOLTAGE. RESISTIVE LOAD

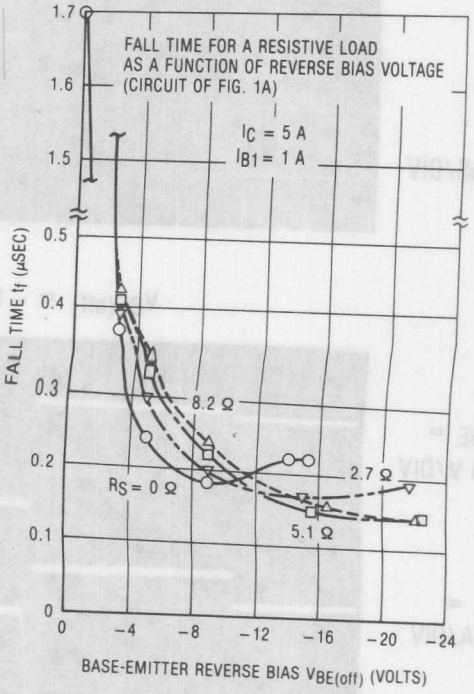


FIGURE 5(E) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. RESISTIVE LOAD

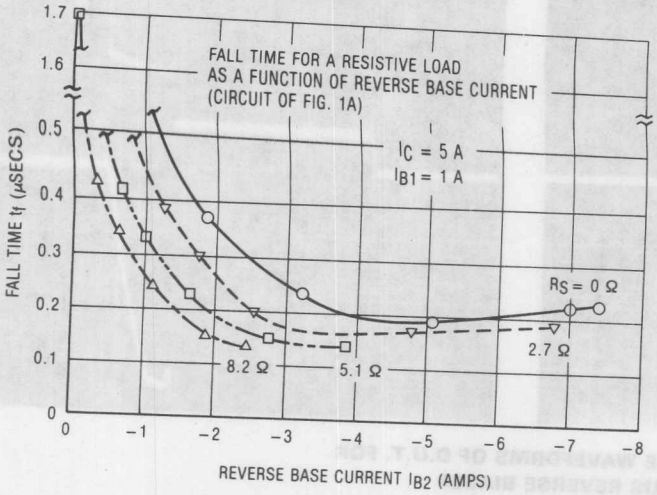


FIGURE 6 — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT AND LOWER COLLECTOR CURRENT

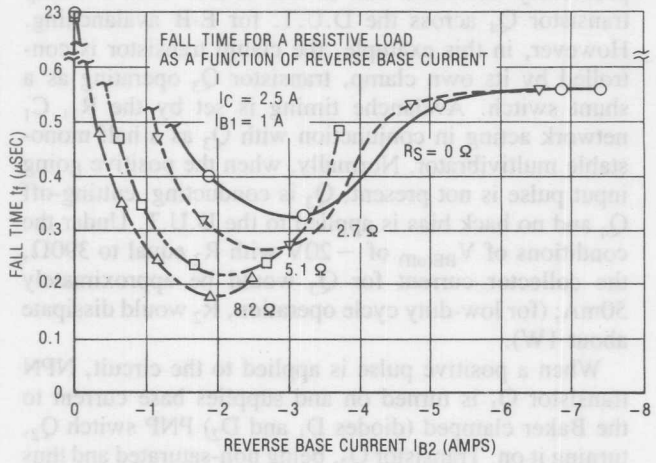


FIGURE 7(B) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. INDUCTIVE LOAD

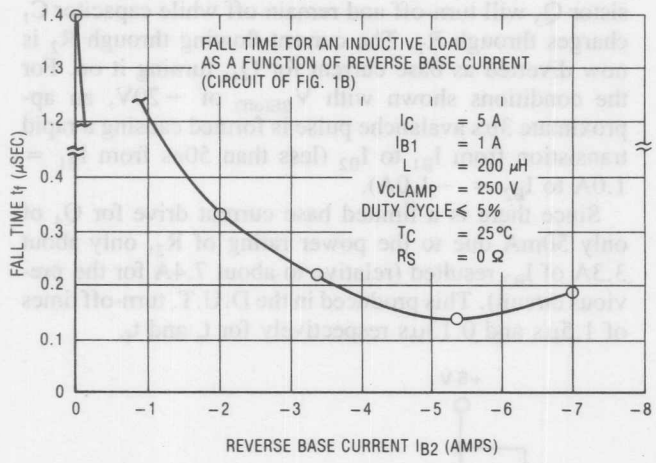


FIGURE 8(B) — 2N6547 STORAGE TIMES

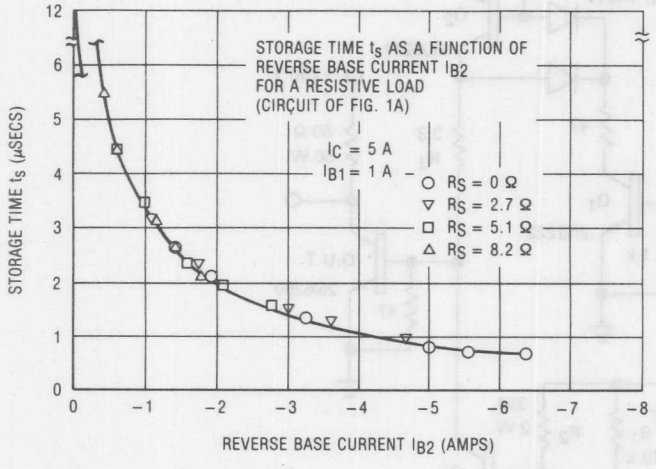


FIGURE 7(A) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. INDUCTIVE LOAD

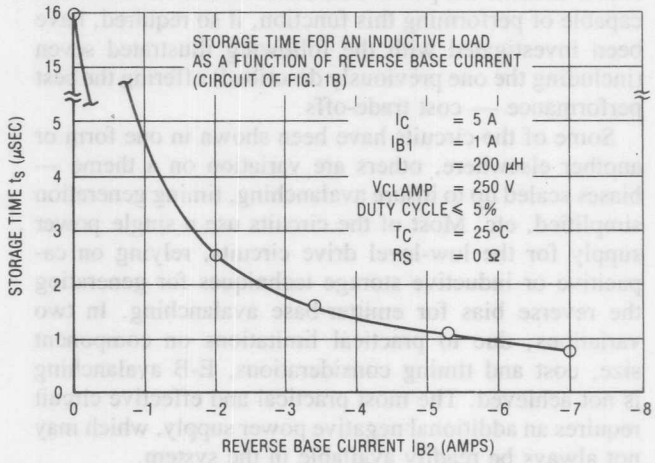
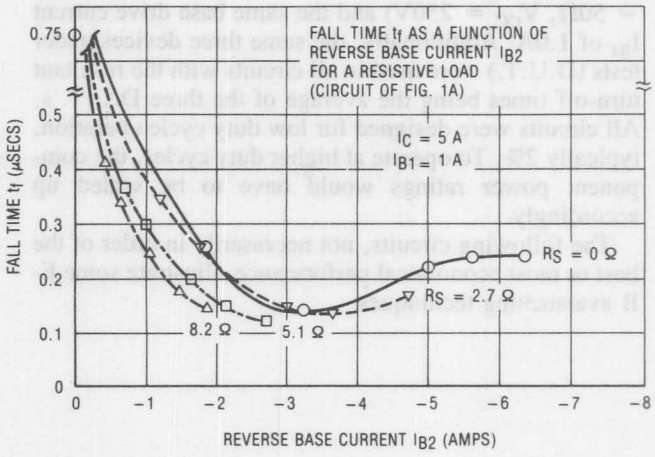


FIGURE 8(A) — 2N6547 FALL TIMES



CONCLUSIONS

After the completion of the characterization of switch-mode transistors with off biases, including E-B avalanching, the following conclusions can be noted.

1. Storage time can be greatly reduced with increasing off bias.
2. Collector current fall-time decreases with increasing off-bias until transistor action ceases ($I_{B2} \approx I_C$) and increases thereafter.
3. Base circuit impedance effects turn-off time; for the same off bias voltage, t_s increases with increasing R_s (I_{B2} decreases) and t_f can be minimized with a constant current drive for the same I_{B2} (higher R_S & $V_{BE(off)}$).
4. E-B avalanching causes a reduction in low-current h_{FE} and that the degree of h_{FE} degradation is proportional to the amount of off bias;
5. E-B power dissipation during avalanching should be considered in the total power capability of the device;
6. E-B avalanching does not change the RBSOA capability;
7. RBSOA capability increases at the high voltage, nominal current portion of the curve with increasing bias.

Knowing these effects of reverse biasing, the designer can now optimize his base drive circuit to minimize t_f, if that is his requirement, or decrease t_s or increase RBSOA. If the drive circuit avalanches the emitter-base junction, the long-term results are now known (low current h_{FE} degradation) and adequate design precautions taken.

EMITTER-BASE AVALANCHE TEST CIRCUITS

The extreme case in reverse biasing the emitter-base is to avalanche the power transistor. A number of circuits capable of performing this function, if so required, have been investigated with the following illustrated seven (including the one previously described) offering the best performance — cost trade-offs.

Some of the circuits have been shown in one form or another elsewhere, others are variation on a theme — biases scaled up to insure avalanching, timing generation simplified, etc. Most of the circuits use a single power supply for the low-level drive circuits, relying on capacitive or inductive storage techniques for generating the reverse bias for emitter-base avalanching. In two variations, due to practical limitations on component size, cost and timing considerations, E-B avalanching is not achieved. The most practical and effective circuit requires an additional negative power supply, which may not always be readily available in the system.

To standardize the results of the seven circuits, all circuits had the same collector load current of 5.0A (R_L = 50Ω, V_{CC} = 250V) and the same base drive current I_{B1} of 1.0A. Additionally, the same three devices under tests (D.U.T.) were used in all circuits with the resultant turn-off times being the average of the three D.U.T.'s. All circuits were designed for low duty cycle operation, typically 2%. To operate at higher duty cycles, the component power ratings would have to be scaled up accordingly.

The following circuits, not necessarily in order of the best or most economical performance, illustrate some E-B avalanching techniques.

TRANSISTOR CLAMP, SHUNT SWITCH

This circuit, as illustrated in Figure 9, is similar to the previously described one in that it also uses a clamp transistor Q_4 across the D.U.T. for E-B avalanching. However, in this example, the clamp transistor is controlled by its own clamp, transistor Q_3 operating as a shunt switch. Avalanche timing is set by the R_1, C_1 network acting in conjunction with Q_3 as a half monostable multivibrator. Normally, when the positive going input pulse is not present, Q_3 is conducting, cutting-off Q_4 and no back bias is applied to the D.U.T. Under the conditions of $V_{BE(off)}$ of −20V with R_2 equal to 390Ω, the collector current for Q_3 would be approximately 50mA; (for low-duty cycle operation, R_2 would dissipate about 1W).

When a positive pulse is applied to the circuit, NPN transistor Q_1 is turned on and supplies base current to the Baker clamped (diodes D_1 and D_2) PNP switch Q_2, turning it on. Transistor Q_2, being non-saturated and thus not contributing appreciable storage time to the circuit, supplies base current of 1.0A (as set by R_3) to the D.U.T.

At the trailing edge of the applied positive pulse, transistor Q_3 will turn-off and remain off while capacitor C_1 charges through R_1. The current flowing through R_2 is now diverted as base current for Q_4, turning it on. For the conditions shown with $V_{BE(off)}$ of −20V, an approximate 3μs avalanche pulse is formed causing a rapid transistion from I_{B1} to I_{B2} (less than 50ns from I_{B1} = 1.0A to I_{B2} = −1.0A).

Since there is a limited base current drive for Q_4 of only 50mA due to the power rating of R_2, only about 3.3A of I_{B2} resulted (relative to about 7.4A for the previous circuit). This produced in the D.U.T. turn-off times of 1.5μs and 0.13μs respectively for t_s and t_f.

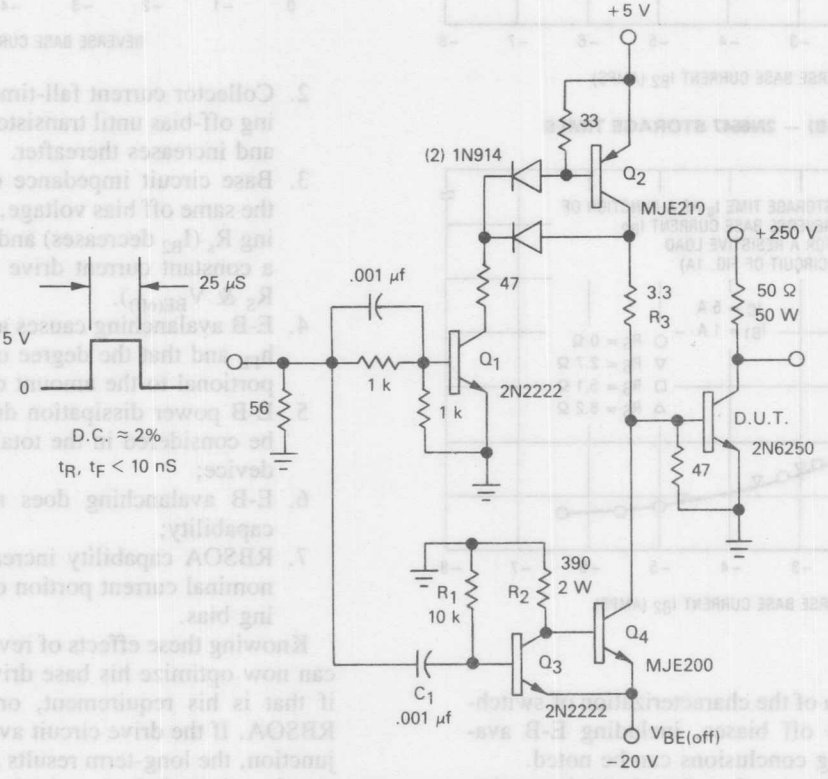


FIGURE 9 — TRANSISTOR CLAMP, SHUNT SWITCH E-B AVALANCHE CIRCUIT

TOTEM POLE DRIVE (TTL)

When only a single power supply is available, then the totem-pole circuit of Figures 10(a) and (b) can be used to generate the reverse bias voltage. For this TTL configured driver, two approaches were used to produce the $V_{BE(off)}$, an RC network in the base of the D.U.T. (Figure 10(a)) and a zener in the emitter of the D.U.T. (Figure 10(b)). Activation is started by applying a positive pulse to the base of transistor Q_1 turning it on and clamping Q_2 off. Base current is then supplied through R_1 to transistor Q_3 (acting as an emitter-follower), turning it on. This stage supplies the 1.0A base current, as set by resistors R_2 and R_3, to the D.U.T.. When the initiate pulse is removed, transistor Q_1 turn off, Q_2 turns on which activates the clamp transistor Q_4. Concurrent with this action Q_3 is turned off by the clamping of Q_2, removing base drive to the D.U.T.. For the circuit of Figure 10(a), the capacitor C_1 is initially charged to the voltage drop across R_3 — approximately 15V — and when Q_4 is energized, the clamping of the positive side of the capacitor to ground will cause a reverse bias to the D.U.T.. The amount of bias is dependent on the charge on C_1. As an example, when C_1 is 1.0μf, a bias of about −14V resulted. The time for this capacitor to recover, however, was about 100μs, which would be too long for 20kHz operation. A more practical recovery time of 30μs was achieved when C_1 was 0.33μf. This, however, resulted in lower $V_{BE(off)}$ (about −8V), and longer turn-off times (1.4μs relative to 1.1μs). The other extreme is when C_1 was zero — the resulting t_s was about 16μs.

Similar results were obtained when a 15V zener was used as a coupling element in place of R_3.

The second approach of using a 15V zener in the emitter of the D.U.T. to produce the back bias also resulted in comparable turn-off times, with t_f being slightly faster — about 0.2μs relative to 0.3μs for the first example. This zener, however, must be large enough to sustain the emitter current under load conditions and secondly, the output will now swing down to the zener voltage plus saturation voltage. The high-power (and high cost) zener can be alternatively implemented with a power transistor and low-power zener, as shown in Figure 10 (c).

Transistors Q_3 and Q_4 (MJE200) are relatively fast (f_t (min) = 65 MHz) but have V_{CEO} rating of only 25V maximum; thus V_{CE} should not exceed this value. After allowing for all voltage drops, this then puts a limit on how much reverse bias can be applied. The dropping resistor R_1, or the zener, are therefore designed for 15V rather than 20V used in the other illustrated examples. On a comparative basis, the resulting turn-off times should be slightly longer for the 15V bias condition.

Diodes D_1 and D_2 are Baker clamp diodes for transistor Q_4. Diode D_3 insures that Q_3 is turned off when Q_2 saturates by compensating for the voltage drop of D_2.

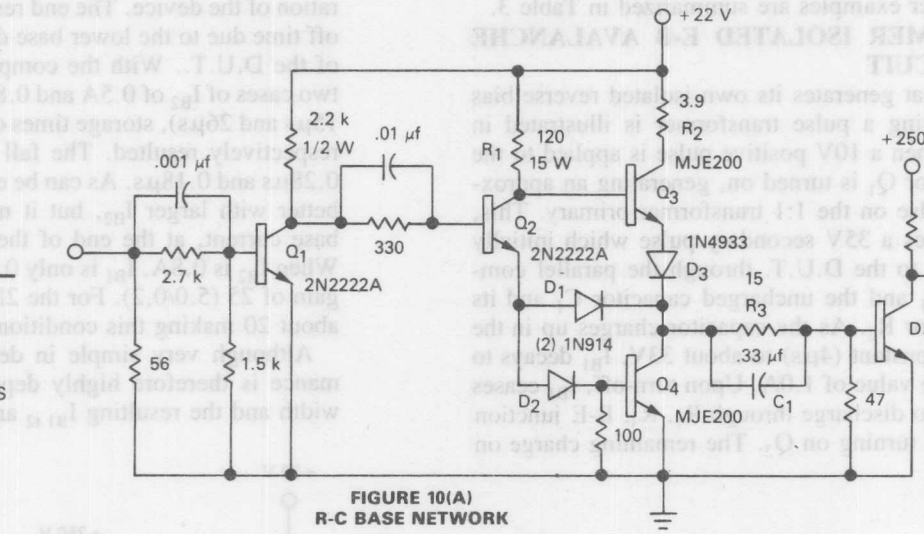


FIGURE 10(A)
R-C BASE NETWORK

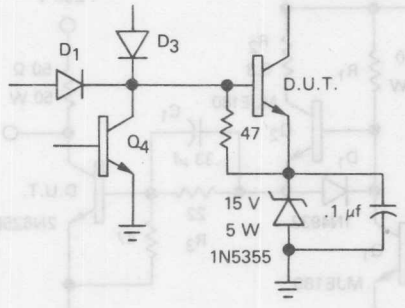


FIGURE 10(B)
ZENER IN EMITTER
HIGH POWER

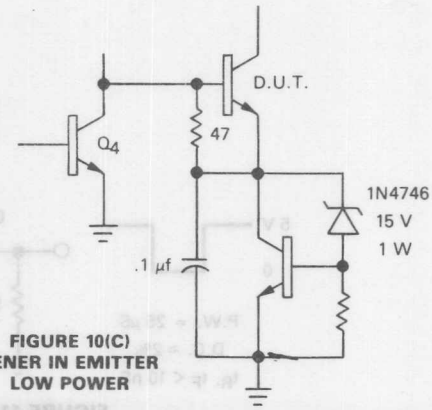


FIGURE 10(C)
ZENER IN EMITTER
LOW POWER

FIGURE 10 — TOTEM-POLE (TTL)
DRIVE E-B AVALANCHE CIRCUIT

TOTEM-POLE DRIVE (HTL)

The circuit of Figure 11 is basically a power scaled up version of the output stage of a High Threshold Logic (HTL) gate and is quite similar to the previously described TTL version. For this example, higher voltage, but lower bandwidth, driver transistors are used, the MJE180 (V_{CEO} (max) = 40V. f_t (min) = 50 MHz). In the absence of a turn-on pulse, transistor Q_1 is conducting, clamping off Q_2 and the D.U.T.. When a negative pulse is applied to the input, Q_1 turns off and Q_2 turns on by means of the base current through R_1. This resistor is designed to supply adequate base current to insure Q_2 saturation and thus must be able to sustain the power dissipated when Q_1 is on (approximately 7.5W for low-duty cycle operation). Transistor Q_2 then supplies the 1.0A I_{B1} to the D.U.T., limited by R_2 and R_3. The voltage drop across R_3 (approximately 22V) produces the reverse bias by means of the switched (when Q_1 turns on) charged capacitor C_1. For values of C_1 of 1.0μf and 0.33μf, peak reverse biases of about −14V and −4V resulted which produced storage times of about 1.8 and 1.9μs respectively. Fall times read 0.18 and 0.50μs respectively with the capacitor recovery times being about 70μs and 15μs respectively. These times are slower than the TTL version and are attributed to the lower base current to the clamp transistor Q_1, being about 11mA for this version relative to about 200mA for the other. This produced about a −3A I_{B2} relative to about −8A. Switching characteristics for this circuit as well as all the other examples are summarized in Table 3.

TRANSFORMER ISOLATED E-B AVALANCHE DRIVE CIRCUIT

A circuit that generates its own isolated reverse bias voltage by using a pulse transformer is illustrated in Figure 12. When a 10V positive pulse is applied to the input, transistor Q_1 is turned on, generating an approximate 35V pulse on the 1:1 transformer primary. This, in turn, induces a 35V secondary pulse which initially creates an I_{B1} to the D.U.T. through the parallel combination of R_1 and the uncharged capacitor C_1 and its limiting resistor R_2. As the capacitor charges up in the R_2, C_1 time constant (4μs) to about 33V, I_{B1} decays to its steady state value of 1.0A. Upon turn-off, I_{B1} ceases and C_1 starts to discharge through R_1, R_3. B-E junction of Q_2 and D_2, turning on Q_2. The remaining charge on C_1 is then switched across the E-B of the D.U.T., avalanching this junction. The result is a peak I_{B2} of about −6A which produces a t_s and t_f of about 1.1μs and 0.33μs respectively. Diode D_1 blocks the discharge path of C_1 and D_2 prevents E-B avalanching of Q_2 while C is charging up. A voltage scaled down version of this circuit was also tested resulting in lower capacitor voltage, reverse bias voltage and I_{B2} with somewhat higher turn-off times.

SPEED-UP INDUCTOR

Speed-up circuits using capacitors are well known. What is not common knowledge, but has been published in several sources, is a technique using a shunt inductor across the E-B of the D.U.T., as shown in Figure 13. When a constant current pulse is applied to the base of the D.U.T., initially, all of the current is base current (since the inductor requires a finite time to charge up) and the transistor is turned on hard. As the pulse time progresses, the inductor current ramps up and the base current is proportionally reduced; thus, the transistor is not driven as hard into saturation. When the applied current pulse is removed, the energy stored in the inductor can induce a voltage pulse (e = L di/dt), with proper design, to avalanche the E-B of the D.U.T.. The resulting I_{B2} that flows will be the difference between the applied current (1.0A) and the base current at the end of the pulse; i.e., $I_{B2} = I_{IN} - I_{B1\,t2}$. The base current at this time should be large enough to still ensure saturation of the device. The end result is a reduction of turn-off time due to the lower base drive and the avalanching of the D.U.T.. With the component values shown, for two cases of I_{B2} of 0.5A and 0.8A (pulse widths of about 15μs and 26μs), storage times of about 3.6μs and 1.8μs respectively resulted. The fall times were respectively 0.28μs and 0.18μs. As can be expected, the results were better with larger I_{B2}, but it must be recalled that the base current, at the end of the pulse time, is reduced. When I_{B2} is 0.8A, I_{B1} is only 0.2A, resulting in a forced gain of 25 (5.0/0.2). For the 2N6250, the typical h_{FE} is about 20 making this condition extremely marginal.

Although very simple in design, the circuit performance is therefore highly dependent on applied pulse width and the resulting $I_{B1\,t2}$ and I_{B2}.

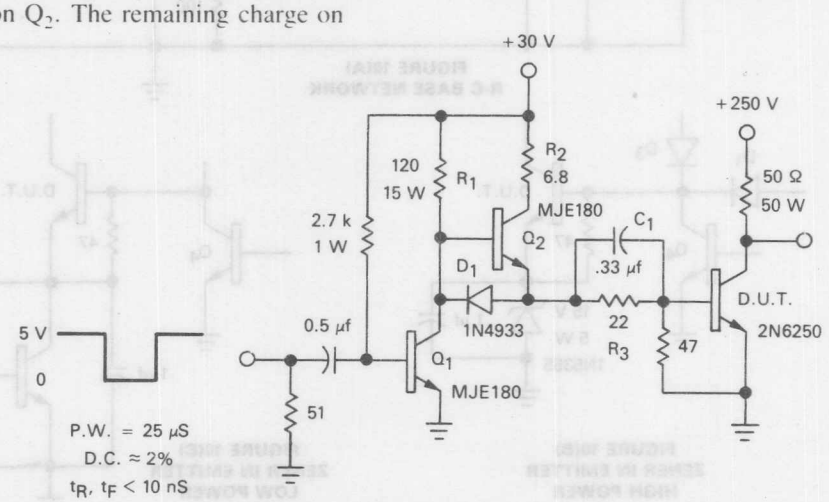
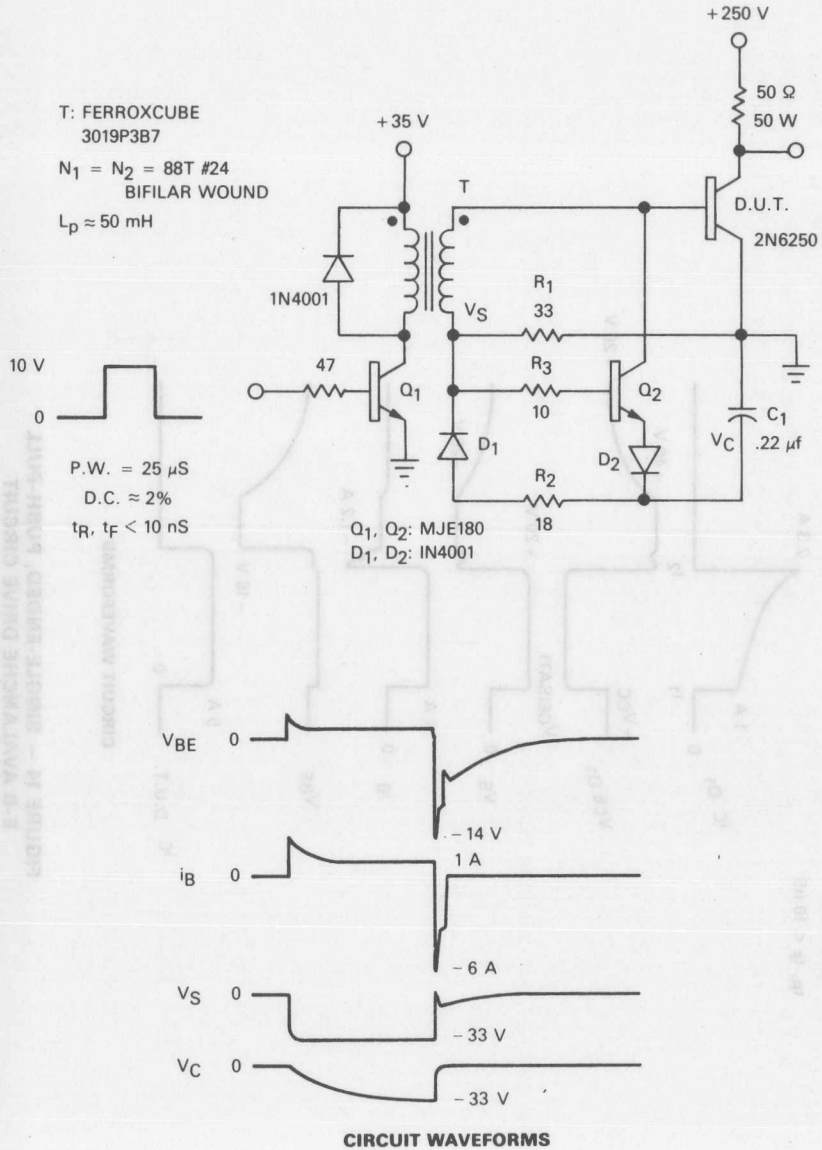
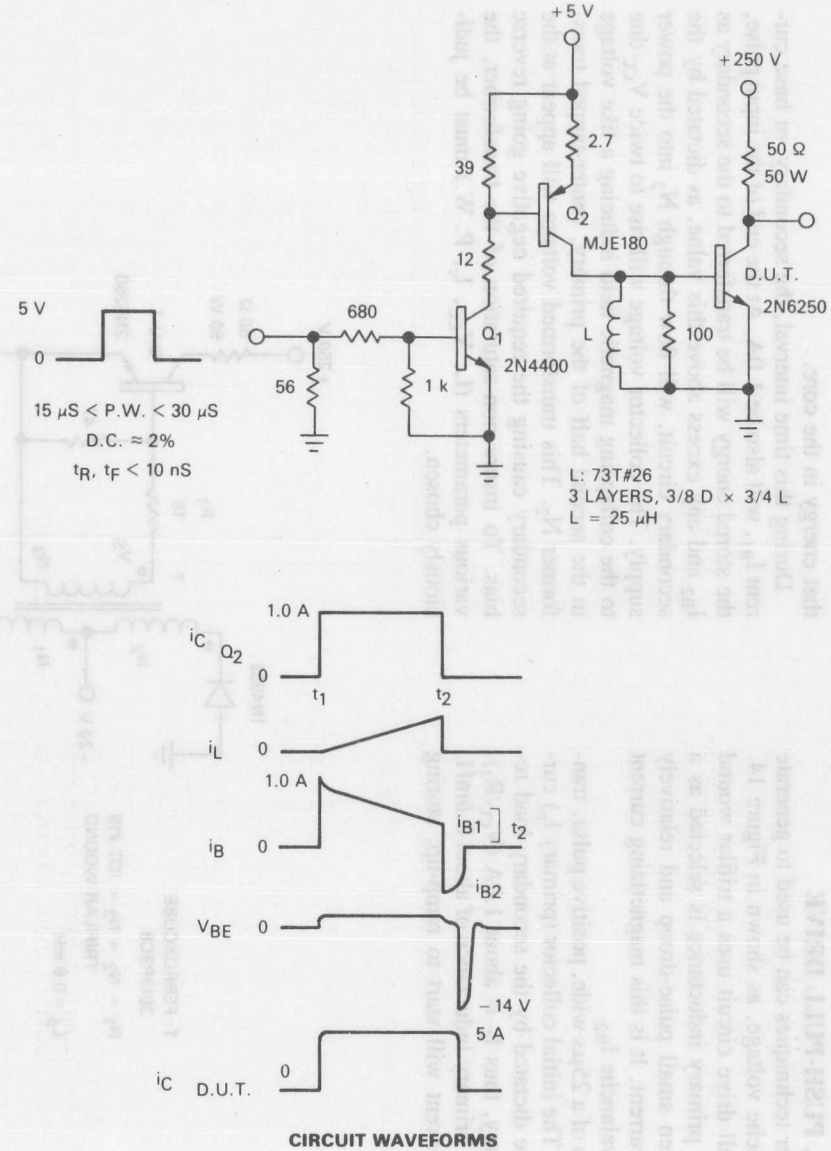


FIGURE 11 — TOTEM-POLE (HTL) DRIVE E-B AVALANCHE CIRCUIT



CIRCUIT WAVEFORMS

FIGURE 12 — TRANSFORMER ISOLATED E-B AVALANCHE DRIVE CIRCUIT



CIRCUIT WAVEFORMS

FIGURE 13 — SPEED-UP INDUCTOR E-B AVALANCHE CIRCUIT

SINGLE-ENDED, PUSH-PULL DRIVE

Flyback converter techniques can be used to generate the required avalanche voltage, as shown in Figure 14. This quasi push-pull drive circuit uses a trifilar wound transformer whose primary inductance is selected as a compromise between small pulse-droop and relatively high magnetizing current. It is this magnetizing current that supplies the avalanche I_{B2}.

Upon application of a 25μs wide, positive pulse, transistor Q1 turns on. The initial collector (primary I_p) current flowing will be dictated by the secondary load reflected to the primary, thus I_C is about 1.0A (V_{CC}/R_1). Because of the low primary inductance of about 0.6mH, the magnetizing current will start to ramp-up, storing that energy in the core.

During this time interval, the secondary, or base current I_{B1}, will also be 1.0A. At the end of the input pulse, the stored energy will be transferred to the secondary as I_{B2} and any excess above this value, as dictated by the secondary circuit, will flow through N_2 into the power supply. The collector voltage will rise to twice V_{CC} due to the collapsing magnetic field inducing a like voltage in the second half of the primary, center-tapped transformer N_2. This transformed voltage will appear at the secondary causing the required negative going reverse bias. To insure non-saturation of the transformer, the various parameters (L, V_{CC}, I_c, P. W.) must be judiciously chosen.

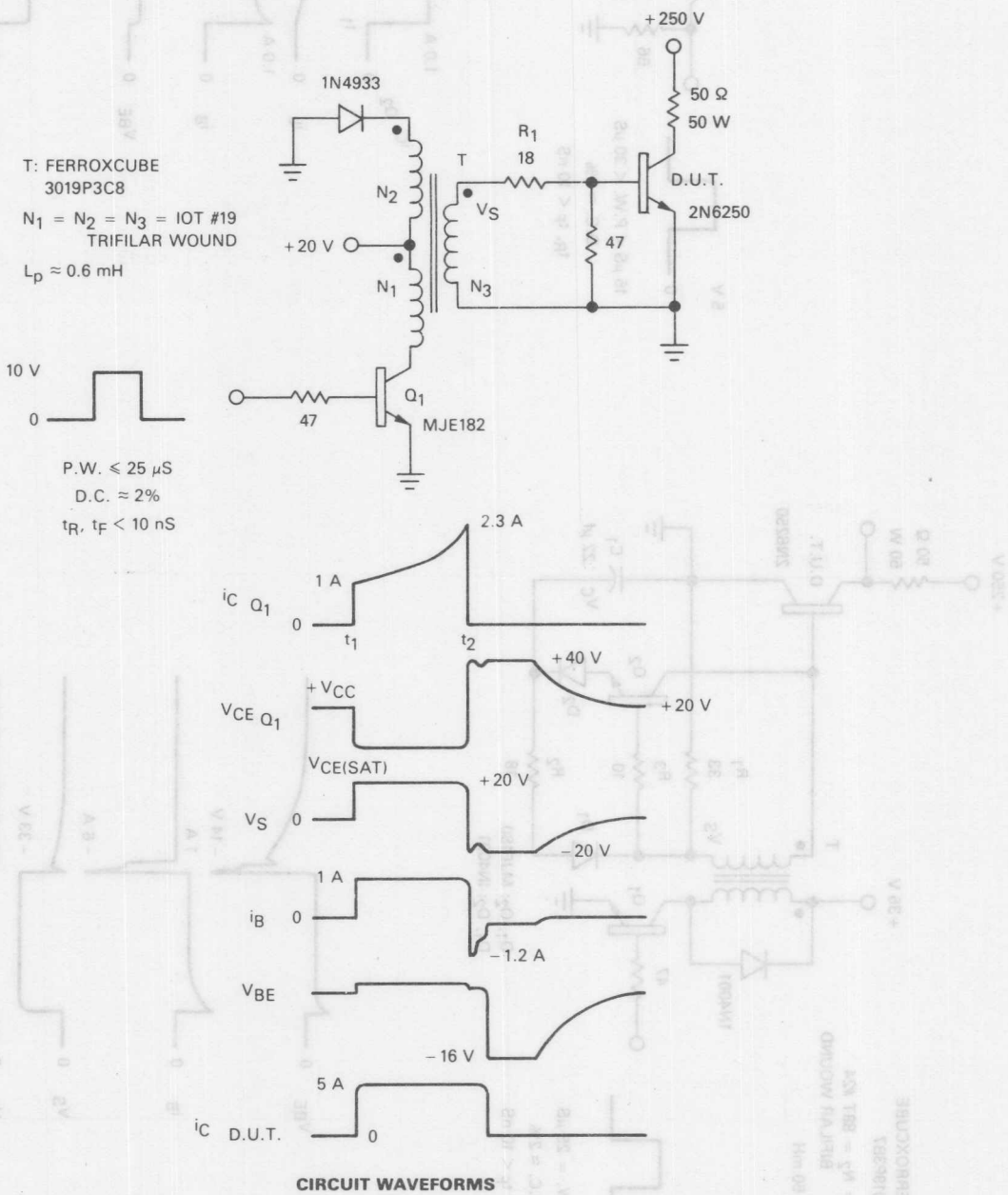


FIGURE 14 — SINGLE-ENDED, PUSH-PULL E-B AVALANCHE DRIVE CIRCUIT

COMPARISON OF E-B AVALANCHE CIRCUITS

Table 3 summarizes the results of the turn-off tests on the seven avalanche circuits and their relative costs. With the exception of the two circuit variations with small speed-up capacitors (0.33μf), all other circuits were avalanched as noted by the $-V_{BE(pk)}$ readings. The effect of storage times from the resulting I_{B2} is also illustrated — irrespective of the circuit, t_s tends to decrease with increasing I_{B2}.

Although all of the circuits do not have comparable power gain, pricing is based on normalized gain and is accomplished by adding the cost of an emitter-follower to the input of the two examples with lower power gain. Costing estimates are based on component quantity buys of 250-999 and do not include assembly costs. The cost of the required negative power supply for the two Transistor Clamp examples are not factored in this exercise. Discounting this supply, on a cost/performance basis, the Transistor Clamp, Series Switch results in the best of the illustrated E-B avalanche circuits.

The author wishes to acknowledge Zane Romaniuk for his contribution in preparing this article.

TABLE 3 — COMPARISON OF E-B AVALANCHE DRIVE CIRCUITS

Circuit		Power Supplies	Conditions		$-i_{B2(pk)}$ (A)	$-V_{BE(pk)}$ (V)	t_s (μS)	t_f (μS)	Remarks	Normal. Cost
Transistor Clamp, Series Switch		+5 V, −20 V	R_S = 0		7.4	≈ 14	0.80	0.22	Requires Negative Power Supply	1.0
Transistor Clamp, Shunt Switch		+5 V −20 V	R_S = 0		3.3	≈ 14	1.5	0.13	Requires − P.S.	1.0
Totem-Pole Drive, TTL	R//C in Base	+25 V	R_3 = 18	C_1 = 1 μf	8.0	≈ 14	0.77	0.30	$t_{rr_{C_1}}$ ≈ 100 μS	1.5
				C_1 = .33 μf	7.5	≈ 8	0.88	0.50	$t_{rr_{C_1}}$ ≈ 30 μS	1.4
	Zener in Emitter		D.C. ⩽ 2%		8.0	≈ 14	0.84	0.23	15 V Zener 5 W = $1.50	2.0
Totem-Pole Drive, HTL		+30 V	R_3 = 22	C_1 = 1 μf	3.2	≈ 14	1.83	0.18	$t_{rr_{C_1}}$ ≈ 70 μS	1.1
				C_1 = .33 μf	3.1	4.0	1.92	0.50	$t_{rr_{C_1}}$ ≈ 15 μS	1.0
Transformer Isolated E-B Avalanche Drive		+35 V	—		6.0	≈ 14	1.1	0.33	Emitter Follower Added to Cost	1.8
Speed-Up Inductor		+5 V	P.W. = 15 μS		0.5	≈ 14	3.6	0.28	L = 25 μH i_{B2} α P.W., L	$I_{B1}]_{t_2}$ = 0.5A	0.8
			P.W. = 26 μS		0.8	≈ 14	1.8	0.18		$I_{B1}]_{t_2}$ = 0.2A
Single-Ended, Push-Pull		+20 V	L_p ≈ 0.6 mH		1.2	≈ 14	3.8	0.18	E.F. Added to Cost	1.5

REFERENCES:

1) Gutmann, J. A. and Suva, R. T.: A line Operated Regulated 50V/50A Switching Power Supply, AN-767 Motorola Semiconductor Products Inc.
2) Bailey, R.: Reverse Bias Safe Operating Area, AN-785 Motorola Semiconductor Products Inc.
3) Roark, D.: Base Drive Considerations in High-Power Switching Transistors, AN-120 TRW.
4) Ollandorf, J.: Speed-up Inductor Increases Switching Speed of High-Current Power Transistors, Application Note, Power Tech.
5) Unitrobe: Inductive Turn-off Technique Minimizing Transistor Storage Time, New Design Idea No. 10.
6) Walker, R. J. and Yu, R.: Horizontal Output Transistor Base Circuit Design, G.E. Co., I.E.E.E. Chicago Spring Conference, June 10, 1974.
7) Hetterscheid, W.: Mains Operated Switched Mode Power Supplies, Philips Laboratory Report NP07407, October 21, 1974.
8) Plaisted, J.: How to Speed Up a Power Transistor Without Blowing It Up, EDN, October 5, 1975.

MOTOROLA *Semiconductor Products Inc.*

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

Printed in Switzerland