Data Acquisition Using INS8048

National Semiconductor
Application Note 281
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Abstract: *This application note describes techniques for interfacing National Semiconductor's ADC0833 serial I/O, and ADC0804 parallel I/O A/D converters to the INS8048 family of microprocessors. A hardware and software interface example is provided for each A/D, along with a brief theory of operation.*

INTRODUCTION

Since the INS8048 series microprocessors are single-chip, multiple I/O line, high speed devices designed as efficient controllers, the capacity to interface with analog peripherals is obvious. That the conversion be fast, inexpensive and easily expanded to accommodate a number of I/O devices is desirable.

The INS8048 is a self-contained, 8-bit processor in a 40-pin dual-in-line package. It contains its own system timing, control logic and memory. All parts contain RAM (64, 128, 256 bytes) and offer the option of on-board ROM (1k, 2k, 4k depending on part). It provides extensive bit-handling capabilities, 97 instructions, and offers easy expansion for I/O and memory.

The ADC0833 A/D converter is an 8-bit successive-approximation device with serial I/O and conversion time of 25 μs. This family of converters offers various configurations of multiplexed analog inputs which can be software programmed as single-ended, or as differential inputs, or both. Single-ended inputs are referenced to a common pin which is either referred to analog ground or to a fixed reference voltage. Like the INS8048 family, a single 5V power supply is all that is needed. The inputs will accept a 0V-5V range. No zero adjust is necessary. It is compatible with TTL and MOS at both input and output. The output can be selected as either MSB or LSB first.

The ADC0804 is a CMOS 8-bit successive-approximation A/D converter with parallel I/O. This A/D can be mapped into memory space or can be controlled as an I/O device. No external logic is needed to interface with the INS8048. A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding smaller voltage spans to the full 8 bits of resolution.

ADC0833 IMPLEMENTATION

Before explaining the system configuration, it is worthwhile for one to understand the operation of the INS8048 processor's I/O ports. Ports 1 and 2 are quasi-bidirectional; that is, they can be used as inputs or outputs while being statically latched. If a ''1'' is written into any port bit, that bit can function as an input or as a high level output. If a ''0'' is written into any port bit, that bit can function only as a low level output. Outputs are latched until changed and inputs are unlatched and must be read immediately. When used with the ANL Pp,A (AND accumulator to port) or the ORL Pp,A (OR accumulator to port) instructions, these ports provide an efficient means of handling single line inputs and outputs. Port expansion, if anticipated, is handled via the lower four bits of Port 2. These four bits fulfill three distinct functions:

(1) A quasi-bidirectional static port

(2) The four high order address bits for external memory

(3) An expander port interface

Only four pins of the processor's Port 1 or Port 2 are needed for physical interfacing (see *Figure 1*). The ANL or ORL instructions set up the port pins to produce the proper outputs (CS, CLK, and the multiplex address) or to allow for data input from the A/D converter.

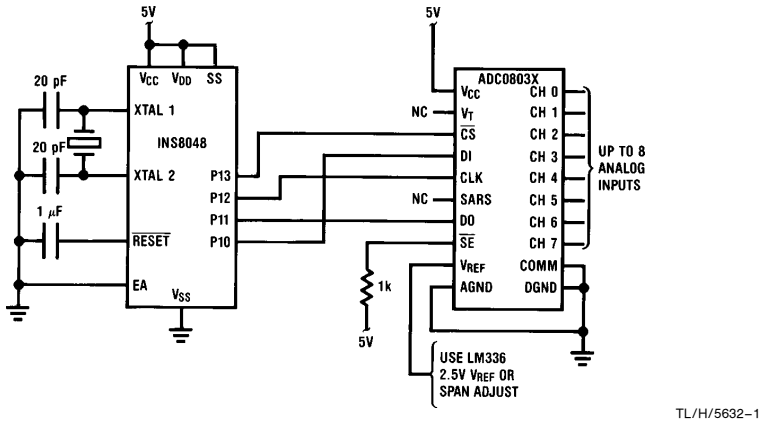

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FIGURE 1. A/D Conversion Circuit for Single-Ended MSB First Mode

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The following description of the program can be used with the listing or flow chart to understand the procedure. To begin conversion, the processor must drive CS low, resetting the multiplex address shift register, the successive-approximation register and the 9-bit shift register. After the A/D converter has been selected, the multiplexer address is shifted out serially to the converter. The 4-bit multiplexer address is always preceded by a start bit, a ''1''. The program loads the multiplexer address, start bit and mode bit into the accumulator as a single byte which is processed and shifted out to the converter. By shifting this byte into the carry, each bit is tested and the appropriate ''1'' or ''0'' is output to the port. After five such operations, the start bit is shifted on the rising edge of the clock pulse through the A/D's 5-bit shift register (see *Figures 2* and *3*, Tables 1 and 2). At this point, the digital data input is disabled, and the digital data output enabled. One more clock pulse is needed to synchronize the output on the falling edge of the clock pulse. On each successive clock pulse, data is shifted serially to the processor. The data bits are then shifted, upon reception, into the accumulator to form the digitized analog input.

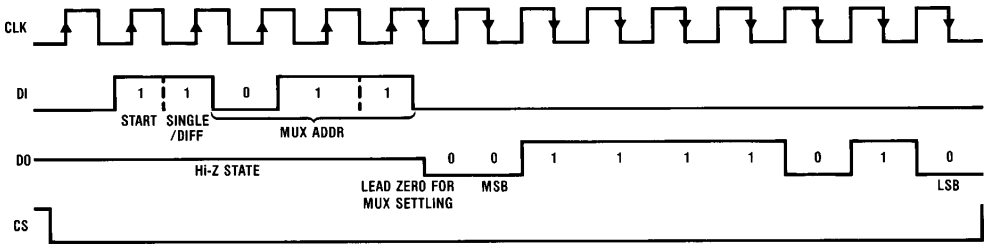

FIGURE 2. Example I/O Transaction (A/D Output = 7A; Channel 2, Single-Ended Selected)

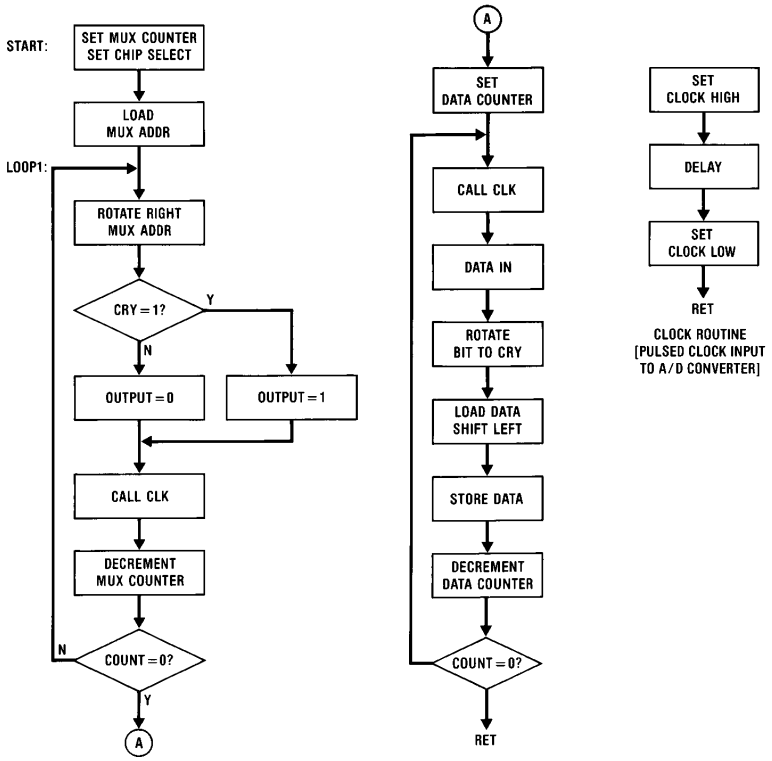

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FIGURE 3. A/D Conversion Flow Chart

TABLE I. Single-Ended Mux Mode

LSB		MSB	S/D	Start	Single-Ended 0	1	2	3	HEX Code
1	0	0	1	1	+				13
1	1	0	1	1			+		1B
1	0	1	1	1		+			17
1	1	1	1	1				+	1F

TABLE II. Differential Mux Mode

LSB		MSB	S/D	Start	Differential 0	1	2	3	HEX Code
1	0	0	0	1	+	−			11
1	1	0	0	1			+	−	19
1	0	1	0	1	−	+			15
1	1	1	0	1			−	+	1D

```
START:    ANL     P1, #0F3H       ;SELECT A/D, SET CS0 to 0
          MOV     R2 #5           ;BIT COUNTER ← 5
          MOV     A, #DATA        ;A ← MUX ADDR
          MOV     R3, #0          ;CLEAR R3
LOOP 1:   RRC     A               ;CY ← ADDR BIT
          JC      ONE             ;IF CY = 1 GO TO ONE
ZERO:     ANL     P1, #0FEH       ;SET DI = 0
          JMP     CONT            ;CONTINUE IF 0
ONE:      ORL     P1, #1          ;SET DI = 1
CONT:     CALL    PULSE           ;PULSE CLK 0 → 1 → 0, CLK IN DATA
          DJNZ    R2, LOOP 1      ;LOOP, TO SHIFT AND OUTPUT MUX
                                  ;ADDR AND SENTINEL
          MOV     R2, #8          ;BIT COUNTER ← 8, FOR SERIAL IN
LOOP2:    CALL    PULSE           ;PULSE CLK 0 → 1 → 0
          IN      A, P1           ;A ← (D0), BIT SHIFTED TO CARRY
          RRC     A
          RRC     A
          MOV     A, R3           ;A ← RESULT
          RLC     A               ;A(0) ← CY, SHIFT LEFT
          MOV     R3, A           ;R1 ← RESULT
          DJNZ    R2, LOOP 2      ;LOOP THRU FOR ALL 8 BITS
          RETR
PULSE:    ORL     P1, #04         ;CLK ← 1
          NOP                     ;DELAY
          ANL     P1, #0FBH       ;CLK ← 0
          RET
          END     START
```

FIGURE 4. Single-Ended A/D Conversion Routine

Easy expansion, mentioned earlier, has not been forgotten. With the addition of the one chip (see *Figure 5*), the number of peripherals can be expanded TEN-FOLD! The INS8243 I/O expander consists of five 4-bit bidirectional ports. One port provides the interface with the processor, the other four provide the I/O expansion. The INS8243 I/O expander serves as a direct extension for the resident I/O port of the INS8048 family of processors. The INS8048 instruction set provides four instructions solely for use with this chip. They are:

MOVD Pp,A—Shift accumulator data to addressed port

MOVD A,Pp—Shift addressed port data to accumulator

ANLD Pp,A—ANDing accumulator data to addressed port

ORLD Pp,A—ORing accumulator data to addressed port

The last two instructions can be used in the same way as the ANL and ORL instructions in the first example. It should be noted that only one pin can be used in Port 7, since the INS8243, unlike the INS8048 series, has true bidirectional ports and thus requires that each port be either input or output. *Figure 5* shows how 10 A/D converters could be connected to allow up to 80 analog inputs to be monitored at the expense of only four I/O pins on the INS8048 itself.

ADC0804 IMPLEMENTATION

The ADC0801/2/3/4/5 A/D converters have been designed to directly interface with processors similar to the INS8048 family. The A/D is memory mapped into the external data memory space of the INS8048 system. The RD, WR and INTR signals of the A/D, and the processor are tied directly. In the example circuit, an arbitrarily chosen address, E0, is assigned to the A/D, and CS is decoded by a bus comparator, the DM8131. Since the address and the data of the INS8048 processor are multiplexed on the same bus, an inverted ALE signal from the INS8048 is tied to the strobed input of the bus comparator in order to latch the address output from the processor. If no other devices are attached to the INS8048's bus, this decoding can be left off and the CS input to the ADC0804 is simply grounded.

A sample program is shown in *Figure 6*. The processor starts the A/D, reads and stores the result of an analog-to-digital conversion through an interrupt service routine. This subroutine starts at address 30H, and the external interrupt vector is located at address 03H. The converted data word is stored at on-chip RAM location, 10H. The following is a line by line description of the parallel A/D conversion subroutine.

BEGIN: This is where the program starts execution after having been reset. R0 and R1 are set up with addresses to point to the A/D converter and the address where data is to be stored.

AGAIN: Interrupts are enabled to allow the A/D to signal that it has completed its conversion; arbitrary data is written to the device to start its conversion process.

LOOP: The processor waits here for an interrupt to occur. The interrupt service routine returns with a zero in the accumulator to allow the program to continue at CONT.

CONT: This is where the analog input received earlier is processed.

INDATA: Upon the occurrence of an interrupt, this routine is entered. It reads data from the A/D converter (with a MOVX A,@R0) and puts it into the RAM location pointed to by R1 (MOV @R1, A). The accumulator is cleared in order to pass location LOOP:, (see *Figure 6*) and control is returned to the user's program.

Upon inspection, it can be seen that each system has its strengths and limitations. Because of the need to handle serial data with loops for input and output, the ADC0833 is approximately five times slower than the ADC0804. Therefore, for raw speed, the ADC0804, at 100 μs conversion time plus minimal processor service time, is preferable. Faster processors can be used to decrease the response time from any given analog input. All INS8048 series devices are available with clock rates up to 11 MHz. Though slower, the ADC0833 provides up to eight multiplexed inputs configurable in single-ended or differential modes, and uses only four processor I/O pins. In either case, the implementation is not formidable and, with only 2 or 3 chips per system, not expensive.

Expander	Outputs
Port 4	DI
	SK
	$\overline{CS}$1
	$\overline{CS}$2
Port 5	$\overline{CS}$3
	$\overline{CS}$4
	$\overline{CS}$5
	$\overline{CS}$6
Port 6	$\overline{CS}$7
	$\overline{CS}$8
	$\overline{CS}$9
	$\overline{CS}$10
Port 7	D0

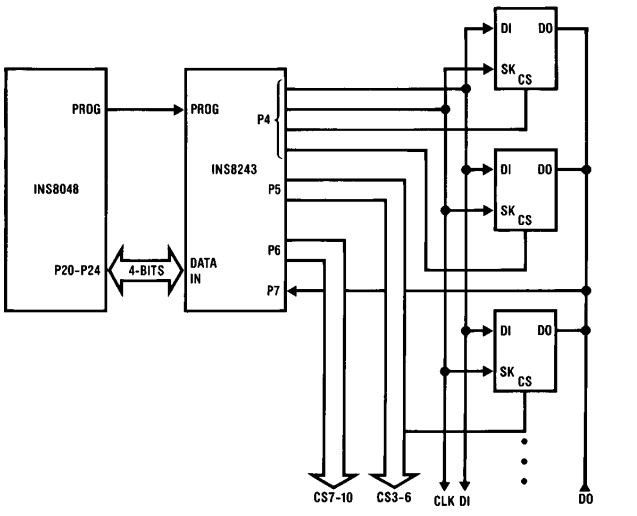

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FIGURE 5. I/O Expansion

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                        ;TEST ROUTINE FOR INTERFACING INS8048 WITH ADC0804
                        ;PROGRAM STARTS AT MEMORY LOCATION 10H
                        ;INTERRUPT SUBROUTINE STARTS AT LOCATION 30H
                        ;DATA WILL BE STORED IN MEMORY LOCATION AT 20H
                        ;
ADDRESS     OBJECT CODE
                                    ORG     0H
0000        04 10                   JMP     10H         ;PROGRAM STARTS AT 10H
                                    ORG     3H          ;INTERRUPT VECTOR
0003        04 30                   JMP     30H
                                    ORG     10H         ;MAIN PROGRAM
0010        B8 E0       BEGIN:      MOV     R0, #0E0H   ;R0 POINTS TO A/D
0012        B9 20                   MOV     R1, #20H    ;R1 POINTS TO DATA ADDRESS
0014        05          AGAIN:      EN I
0015        23 FF                   MOV     A, #0FFH    ;SET THE ACC FOR INTR LOOP
0017        90                      MOVX    @R0, A      ;START A/D
0018        96 18       LOOP:       JNZ     LOOP        ;LOOP UNTIL INTR FROM A/D
001A        00                      NOP                 ;GO TO USER'S PROGRAM
                                                        ;
001B        00          CONT:       NOP                 ;USER'S PROGRAM TO PROCESS
                                                        ;CONVERTED DATA
                                                        ;
                                                        ;INTERRUPT ROUTINE STARTS
                                    ORG     30H         ;AT 30H
0030        80          INDATA:     MOVX    A, @R0      ;INPUT CONVERTED DATA
0031        A1                      MOV     @R1, A      ;STORE IN DATA ADDRESS
0032        27                      CLR     A           ;CLEAR ACC TO GET OUT OF
0033        93                      RETR                ;THE INTERRUPT LOOP
                                    END
```

FIGURE 6. A/D Conversion Routine

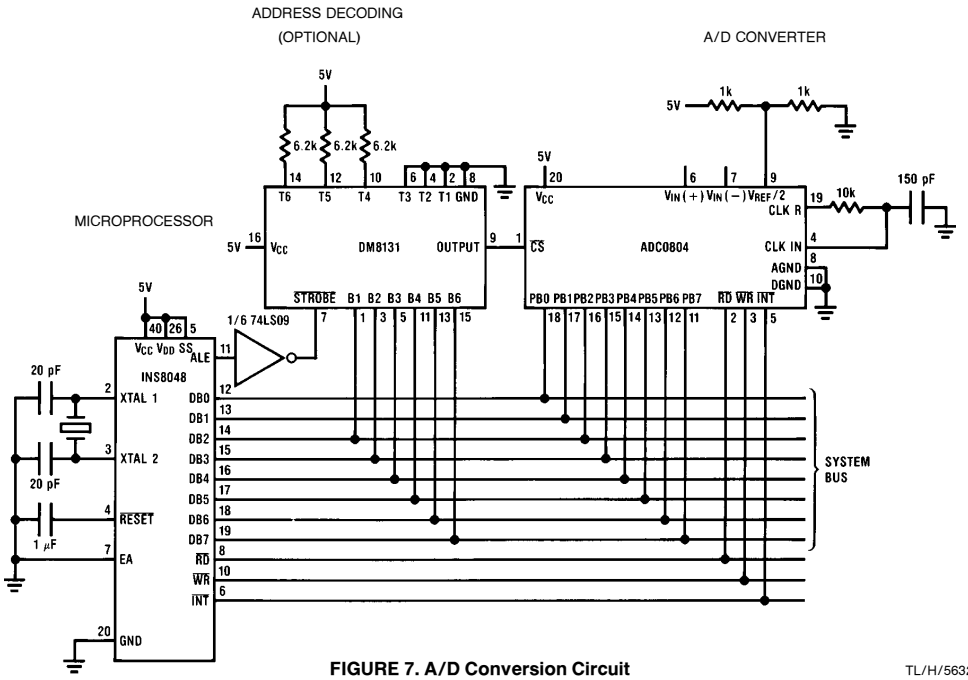

FIGURE 7. A/D Conversion Circuit

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