Receiving 5250 Protocol Messages with the Biphase Communications Processor

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In 5250 protocol, station address recognition and the lack of any easily detectable ending sequence as in 3270 protocol make the hardware and software tasks challenging. This article discusses how to use the DP8344 in a typical 5250 environment with both the current and forthcoming revisions of silicon.

The receiver works in two modes of operation for 5250 protocol. In promiscuous mode, the receiver accepts data for all addresses on the network giving the user the ability to support multiple or single sessions in one's software. The program can simply reset the transceiver upon receiving a station address of no interest. The received station address is stored in the Transceiver Status Register {TSR} bits 2–0 and is valid when the data Available [DA] flag is high. The received station address should be used prior to reading {RTR}. When {RTR} is read, the receiver FIFO advances and the current word is replaced by the next available word. If another word is in the FIFO, it will be reflected in {RTR} and {TSR} in instructions there after. In nonpromiscuous mode, the receiver only loads data in the FIFO in messages where the first frame address matches {NAR} bits 2–0. The receiver logic compares {NAR} bits 2–0 with the station address received in the first frame to decide whether to load data. However, error detection is enabled in all addresses for all frames of a message and the software must determine how the error is to be handled.

The end of message determination should be handled in software. The 5250 protocol requires an end of message delimiter (a station address of 111) to be sent in the last frame of a multiframe message or at the end of a single frame message to the system. For single frame messages from the system to a device, bit 14 (the first bit after the sync bit; [RTR0]) in the command frame will determine if the message has ended. If bit 14 is off in a command frame, the message is a single frame. Once the end of message determination is made in software, the receiver should be reset. The receiver will flag a loss of midbit error and inhibit the setting of the Line Turn Around [LTA] interrupt if the line is not free of transitions for up to 3 μs after the last valid fill bit is received. The [LTA] interrupt should not be used since it may or may not go high at the end of received messages. By resetting the receiver at the end of the message, any false loss of midbit errors will be avoided.

An efficient way to decode the received address and end of message delimiter is to use the JRMK instruction with {TSR} as the source. By selecting to ''rotate'' right six positions and to 'mask' bits five through seven in {TSR}, a unique branch offset into a jump table is formed for each of the received addresses. Assuming that [TFF] is low in {TSR}, the offset from the ADDECDR address will allow four instruction slots for each address. By using the JMPB and LJMP instructions, all four slots are used for each address. Each branch from the table will contain the appropriate action for that particular address. The code example in *Figure 1* is the Data Available interrupt service routine with the receiver in 5250 promiscuous mode. The code presented in this article is intended for example only and may not be suitable in an actual working environment. GP6′ is used to turn sessions on or off and has been loaded with H#08 to turn on the 011 station address and turn off all others. Each bit in the register corresponds to a station address. GP5′ has been initialized to H#00 in the foreground program and is used to store a multiframe flag and end of message flag. The multiframe flag is set when the software has determined that a multiframe message is being received. The end of message flag is set when the software determines that the last frame in the message was received.

This code first checks to see whether an error or the reception of a data frame caused the interrupt. If not, a check to see if the message is multiframe or not is done. Bit 0 of GP5′ is set high for multiframe messages. The ADDECDR address is where the received address is decoded using the JRMK instruction. Notice in the code that station address 3 is supported and all others ignored. By changing the value in GP6′, different station addresses can be turned ''on'' or ''off''. The key point to make for ensuring clean operation is to reset the transceiver once the last frame is received to avoid any false loss of midbits errors flagged when the message ends.

With the upcoming silicon revision, the receiver hardware in 5250 and 8BIT nonpromiscuous modes will reset if no address match is made (i.e. the received station address does not match the address in the Network Address Register {NAR}) and no errors are detected during the first frame of the message. Error detection will be enabled during the first frame of messages independent of the received station address. If an error is detected during the first frame, all devices will report the error. On subsequent frames, errors will only be reported if the first frame contained a matching address. In 5250 mode, {NAR} bits 2–0 are compared to the received address. In 8BIT mode, all {NAR} bits are compared. The receiver's end of message reset has been modified to avoid flagging false loss of midbit errors in 5250 modes of operation.

To reset cleanly at the end of the message, the receiver hardware will look for abit time wihtout a transition (a ''loss of midbit'') during the fill bit portion of the received message as an indication that the message has ended. Once this occurs, the receiver will reset and [LTA] will go high to flag the CPU that the receiver has received a complete message. Since a loss of midbit during fill bits could be a real error (i.e. not an end of message), the software will need to check for an end of message indication in the last data byte received. In situations where a sync bit is followed by inactivity on the line, the receiver hardware will consider the message to be continuing and shift data in accordingly. The receiver monitors Line Active [LA], in the Network Command Flag Register {NCF} to determine if the line has died. [LA] goes high on any detected transition on the line and will return low after 16 transceiver clocks of no activity. If [LA] times out, [LTA] will go high and the receiver will reset. Note again that the software will still need to check for an end of message, for this could be an error situation. If [LA] does not time out, the receiver shifts in the data and checks for errors in the usual manner.

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***************DA ISR*********************************************
** Foreground TMR=H#1D ICR=01HHHHH0 GP5'=H#00 GP6'=H#08           **
** Data available Interrupt Service Routine                       **
;
DAISA:    EHH     MA,AB,NAI                 ;set appropriate banks.
          JMPF    S,RERR,ERRHDLR            ;branch to error handler
                                            ;if error flag set.
          JMPB    GP5,S,B#000,ADDECDR       ;if multiframe, go to address
                                            ;decoder.
          JMPB    RTR,NS,B#000,EOM          ;check B14 in message, if
                                            ;low, single frame message
          ORI     H#01,GP5                  ;set multiframe flag
ADDECDR:  JRMK    TSA,B#110,B#011           ;decode received address
          JMPB    GP6,NS,B#000,RST          ;
          LJMP    A0                        ;jump table for all network
          JMPB    GP6,NS,B#001,RST          ;addresses.
          LJMP    A1                        ;in this configuration,
          JMPB    GP6,NS,B#010,RST          ;address 3 is supported
          LJMP    A2                        ;and all others ignored
          JMPB    GP6,NS,B#011,RST          ;after first frame.
          LJMP    A3                        ;
          JMPB    GP6,NS,B#100,RST          ;
          LJMP    A4                        ;
          JMPB    GP6,NS,B#101,RST          ;
          LJMP    A5                        ;
          JMPB    GP6,NS,B#110,RST          ;
          LJMP    A6                        ;
          JMPB    GP6,NS,B#111,RST          ;
          LJMP    AEOMD                     ;go to end of message routine
EOM:      ORI     H#02,GP5                  ;set end of message flag
          JMP     ADDECDR                   ;go to address decoder
RST:      ORI     H#80,TMR                  ;reset transceiver on
          ANDI    H#7F,TMR                  ;don't care addresses.
          ANDI    H#FC,GP5                  ;clear flags and return.
          RET     RI,RF                     ;
A3:    ..handle received data for address 3. If end of
             message flag set, reset transceiver, clear flags
             and return. If end of message flag not set, return.
AEOMD: ..the last frame of the message was just received,
             handle data then reset transceiver, prepare to
             transmit by loading and starting the timer for
             frame timing, enable timer interrupt, clear
             flags, return.
```

FIGURE 1. Multi-Session Application

To minimize software overhead, a new flag [DEME] has been added to {NCF] at bit 3 to indicate the reception of the end of message delimiter in 5250 modes. [DEME] will go high when the currently accessible word in the receiver FIFO contains the 111 address. In 3270/3299 modes, [DEME] will go high when local odd byte parity [TSR2] does not match odd byte parity received [TSR0].

Some of the software overhead will not be required for the forthcoming silicon revision. It will no longer be necessary to reset the receiver to avoid false loss of midbit errors at the end of the message. The [LTA] interrupt can be used allowing the software to be interrupted when the receiving task is complete. In the [LTA] interrupt routine, the timer can be loaded and started to timeout in the response window (45 ±15 ns) before starting the transmitting task.

The code shown in *Figure 2* is an example for a single session application with the receiver in the nonpromiscuous 5250 mode. Address 1 will be supported. The Data Available interrupt and the LTA interrupt are enabled in the foreground program. GP5′ is used for software flags in the interrupt routine of a multiframe indicator in bit0 and an end of message indicator in bit1.

The [LTA] routine is not absolutely necessary. The actions taken in the routine could have been handled in the Data Available routine once the determination of the end of mes-

sage was made. As seen above, the software requirement for the transceiver task can be totally interrupt driven allowing the processing power of the BCP to be used for other tasks. The 1 Mbs data rate used in the 5250 protocol leaves more CPU bandwidth available for other tasks than either the 3270 or 3299 protocols.

```
************ DA ISR ***********************************************
* Foreground program TMR=H#1C ICR=01HHH0H0 GP5'=H#00 NAR=H#01      **
* Data available Interrupt Service Routine                        **
DAISR:     EHH     MA,AB,NAI                 ;set appropriate banks.
JMPF       S,RERR,ERRHDLR
                                             ;branch to error handler
                                             ;if error flag set.
           JMPB    GP5,S,B#000,E0MCHK        ;if multiframe, skip check
                                             ;for single frame message.
           JMPB    RTR,NS,B#000,SEOMF        ;check B14 in message, if
                                             ;low, single frame message.
           ORI     H#01,GP5                  ;set multiframe flag.
           JMP     DATA
SEOMF:     ORI     H#02,GP5                  ;set end of message flag
           JMP     DATA
EOMCHK:    JMPB    NCF,S,B#011,SEOMF
DATA:     ... handle received data for address 1, return
;
************ LTA ISR ***********************************************
* Line Turn Around Interrupt Service Routine                      **
LTAISR:    EHH MA,AB,NAI                     ;set appropriate banks.
           JMPB GP5,NS,B#010,ERRCOND         ;if end of message flag
                                             ;not set, error condition.
           ... load and start timer to timeout at necessary time
           required before transmitting, enable timer interrupt,
           clear GP5' flags and LTA, return.
ERRCOND: ... an error condition occurred in the message
           (i.e. the line died after a sync bit was detected or
           a loss of synchronization occurred during fill bits),
           take appropriate action and return.
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FIGURE 2. Single-Session Application

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