A Dual Access NS32532 Error Detecting and Correcting Memory System

National Semiconductor
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I. INTRODUCTION

This appendix describes how to interface two NS32532 microprocessors, both synchronous to the same system clock, to a DP8422A DRAM controller and a 74F632 EDAC chip. It is assumed that the reader is already familiar with NS32532, the DP8422A, and the 74F632 modes of operation. The National Semiconductor DP8420A can be used in place of the 74F632, though its timing is slower.

This application note supports the following types of memory accesses:

1. Read accesses with 6 wait states inserted (8 clock periods total in the synchronous mode read access), any single bit errors are automatically corrected before sending the data to the CPU (EDAC unit in always correct mode);
2. Write accesses with 3 wait states inserted (5 clock periods total in the synchronous mode write access);
3. Byte write accesses with 7 wait states inserted (9 clock periods total in the synchronous mode byte write access);
4. Burst read accesses with 3 wait states in the burst portion of the access (4 clock periods total per synchronous mode burst read memory access);
5. Scrubbing during DRAM refreshes (6 clock periods total during the refresh if no errors, 8 clock periods total during the refresh if any errors), any single bit errors are corrected. The corrected word is then written back to the DRAM.

II. DESCRIPTION OF 25 MHz DUAL ACCESS NS32532 SYSTEM INTERFACED TO THE DP8422A AND THE 74F632

This design allows two NS32532 microprocessors to access a common error corrected dynamic memory system. The error corrected memory system is implemented using the 74F632 EDAC chip in the always correct mode. Whichever NS32532 accessed the memory last has a higher priority. Both NS32532s are interfaced to the DRAM and allow the DRAM system to support burst mode accesses.

This design is very similar to the 68030 dual access EDAC design and the PALs will be very similar. The reader can refer to that design to see the timing waveforms, block diagrams, and simulations. The only necessary changes to the 68030 design are that the $\overline{\text{STERMA}}$,B PAL outputs will have to be modified to support the NS32532 $\overline{\text{RDY}}$ inputs, and the $\overline{\text{AREQ}}$, $\overline{\text{AREQB}}$ outputs of the PALs will have to take $\overline{\text{ADS}}$, $\overline{\text{CS}}$, and $\overline{\text{CONF}}$ into consideration (not just $\overline{\text{ADS}}$, $\overline{\text{CS}}$ as in the 68030 design). The user should also be careful not to violate the DP8422A parameter #416 ($\overline{\text{AREQ}}$ negated to $\overline{\text{ADS}}$ asserted to guarantee tASR = 0 ns) when generating the $\overline{\text{AREQ}}$, $\overline{\text{AREQB}}$ PAL outputs.

During read accesses the data is always processed through the EDAC chip (always correct type of system). If a single bit error occurs during a read access this design guarantees correct data to the CPU, but does not write the corrected data back to the DRAM. Single bit soft errors in memory are only corrected (written back to memory) during scrubbing type refreshes. The memory is scrubbed often enough that the probability of accumulating two soft errors in memory is very unlikely.

During read accesses the data is always processed through the 74F632 EDAC chip (i.e., the EDAC data buffers are enabled to provide the data to the CPU). The 74F632 is always put into latch and correct mode during read accesses, even though the data from the memory may be correct. This allows $\overline{\text{CAS}}$ to be toggled early (before the CPU has sampled the data), during burst mode accesses, to start accessing the next word of the burst access.

This design drives two banks of DRAM, each bank being 39 bits in width (32 data bits plus 7 check bits) giving a maximum memory capacity of 32 Mbytes of error corrected memory (using 4 Mbit x 1 DRAMs). By choosing a different $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ configuration mode (see programming mode bits section of DP8422A data sheet) this application can support 4 banks of DRAM, giving a memory capacity of 64 Mbytes (using 4 Mbit x 1 DRAMs, NOTE that when driving 64 Mbytes the timing calculations will have to be adjusted to the greater capacitive load).

The memory banks are interleaved on every four word (32-bit word) boundary. This means that the address bit (A4) is tied to the bank select input of the DP8422A (B1).

Address bits A3,2 are tied to the least significant column address inputs (C1,0) to support burst accesses using nibble mode DRAMs.

Address bits A1,0 are used to produce the four byte select data strobes, used in byte reads and writes. If the majority of accesses made by the NS32532 are sequential, the NS32532 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks (address bit A4 tied to DP8422A pin B1), allowing one memory bank to be precharging ($\overline{\text{RAS}}$ precharge) while the other bank is being accessed. This is a higher performance memory system than a non-interleaved memory system (bank select on the higher address bits). Each separate memory access to the same memory bank will generally require extra wait states to be inserted into the CPU access cycles to allow for the $\overline{\text{RAS}}$ precharge time.

The logic shown in this application note forms a complete NS32532 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, Port B, and refreshing the DRAM;
B. the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{\text{RAS}}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc.);
C. performing bytes write and reads to the 32-bit words in memory;
D. normal and burst access operations.

By making use of the enable input on the 74AS244 buffer, this application allows dual access applications. The addresses and chip select are TRI-STATE through this buffer, the write input ($\overline{\text{WIN}}$), lock input ($\overline{\text{LOCK}}$) and $\overline{\text{ECAS0}}$–3 inputs must also be able to be TRI-STATE (another 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A allows dual accessing to be performed.

III. NS32532 25 MHz DUAL ACCESS EDAC DESIGN: THE EDAC ERROR MONITORING METHOD IN CONJUNCTION WITH THE NS32532 BUS RETRY FEATURE

The NS32532 dual access EDAC system design can use the error monitoring method in conjunction with the NS32532 bus retry feature, instead of the always correct method (design shown in the NS32532 application note). The error monitoring method can yield a slight improvement in system performance.

By using the error monitoring method of error correction single read accesses or the first read access during a burst access can be shortened by one clock period, allowing a synchronous read access to have only 5 wait states inserted, 7 clock periods total (compared to 6 wait states, 8 clock periods total when doing the always correct method). All other types of accesses (burst reads, bytes writes, word writes, refresh scrubbing) will execute in the same number of clock cycles, and in the same manner as described in this application note.

Read accesses can save one wait state because the data from the DRAM memory is assumed to be correct in the error monitoring system design. Therefore the DRAM data is given directly to the CPU instead of running it through the EDAC chip as was done in the always correct method.

In order to do this design it is required that the bus retry feature of the NS32532 and registered transceivers be employed.

The bus retry feature of the NS32532 involves pulling the NS32532 input signal ''$\overline{\text{BRT}}$'' low before the end of state T2 or T2B. Given that this is done the NS32532 will complete the bus cycle normally, but will ignore the data read in the case of a read cycle. The CPU will then wait for $\overline{\text{BRT}}$ to transition high before repeating the bus cycle (unless that access is not currently needed by the CPU). This feature is useful for the case where an error is detected in the DRAM data. In this case $\overline{\text{BRT}}$ is brought low until the data from the DRAM is corrected (by the EDAC chip) and written back to the DRAM. $\overline{\text{BRT}}$ is then brought high to continue CPU processing.

Registered transceivers are necessary (in place of the 74F245's shown in the block diagram) during burst mode read accesses because $\overline{\text{CAS}}$ transitions high before the CPU has sampled the DRAM data. The registered transceivers hold the data valid until the CPU samples it during these cases.

A read, read with a single bit error, and burst read access timing are shown at the end of this appendix implementing the error monitoring method. The user can see how these access cycles differ from the always correct method access cycles shown in the 68030 dual access EDAC application note.

IV. NS32532 25 MHz DUAL ACCESS DESIGN, PROGRAMMING MODE BITS

Programming Bits	Description
R0 = 1 R1 = 1	$\overline{\text{RAS}}$ low four clocks, $\overline{\text{RAS}}$ precharge of three clocks
R2 = 1 R3 = 0	$\overline{\text{DTACK1}}$ is chosen. $\overline{\text{DTACK}}$ low first rising CLK edge after access $\overline{\text{RAS}}$ is low.
R4 = 0 R5 = 0	No WAIT states during burst accesses
R6 = 0	If $\overline{\text{WAITIN}}$ = 0, add one clock to $\overline{\text{DTACK}}$. $\overline{\text{WAITIN}}$ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access.
R7 = 1	Select $\overline{\text{DTACK}}$
R8 = 1 R9 = X	Non-interleaved Mode
C0 = 1 C1 = X C2 = X	Selected based upon the input ''DELCLK'' frequency. Example: if the input clock frequency is 20 MHz, then choose C0,1,2 = 0,0,0 (divide by ten, this will give a frequency of 2 MHz). If DELCLK of the DP8422A is over 20 MHz do an initial divide by two externally and then run that output into the DELCLK input and choose the correct divider.
C3 = X	
C4 = 0 C5 = 0 C6 = 1	$\overline{\text{RAS}}$ groups select by ''B1''. This mode allows two $\overline{\text{RAS}}$ outputs to go low during an access, and allows byte writing in 32-bit words.
C7 = 1	Column address setup time of 0 ns
C8 = 1	Row address hold time of 15 ns
C9 = 1	Delay $\overline{\text{CAS}}$ during write accesses to one clock after $\overline{\text{RAS}}$ transitions low
B0 = 1	Fall-thru latches
B1 = 1	Access mode 1
$\overline{\text{ECAS}}$0 = 0	Non-extend $\overline{\text{CAS}}$ mode

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either high or low voltage level (don't care condition)

V. NS32532 25 MHz WORST CASE TIMING CALCULATIONS

The worst case access is an access from Port B. This occurs because the time to $\overline{RAS}$ and $\overline{CAS}$ low is longer for the Port B access than a Port A access, a refresh with scrubbing access, or an access which has been delayed from starting (due to refresh, $\overline{RAS}$ precharge time, or the other Port accessing memory).

A. Worst case time to $\overline{RAS}$ low from the beginning of an access cycle:

40 ns (T1 clock period of NS32532) + 10 ns (PAL16R4D maximum combinational output delay to produce $\overline{AREQB}$) + 41 ns (DP8422A-25 parameter #102, $\overline{AREQ}$ to $\overline{RAS}$ delay maximum) = 91 ns

B. Worst case time to $\overline{CAS}$ low from the beginning of an access cycle:

40 ns + 10 ns + 94 ns (DP8422A-25 parameter #118a, $\overline{AREQB}$ to $\overline{CAS}$ delay maximum) = 144 ns

C. Worst case time to DRAM data valid:

144 ns (from ''B'' above, maximum time to $\overline{CAS}$) + 50 ns ($\overline{CAS}$ access time ''tCAC'' for a typical 100 ns DRAM) = 194 ns

D. Worst case time to data valid on the EDAC data bus:

194 ns (from ''C'' above) + 7 ns (74AS244 maximum delay) = 201 ns

E. Worst case time until the error flags are valid from the 74F632:

201 ns (from ''D'' above) + 31 ns (74F632 maximum time to error flags valid) = 232 ns

F. Worst case time until corrected data is valid from the 74F632:

201 ns (from ''D'' above) + 28 ns (74F632 maximum time from data in to correct data out) = 229 ns

G. Worst case time until corrected data is available at the CPU:

229 ns (from ''F'' above) + 7 ns (74F245 maximum delay) = 236 ns

EDAC Memory—Control Logic in this System Needs the Following:
3 PALS and Some Logic Gates

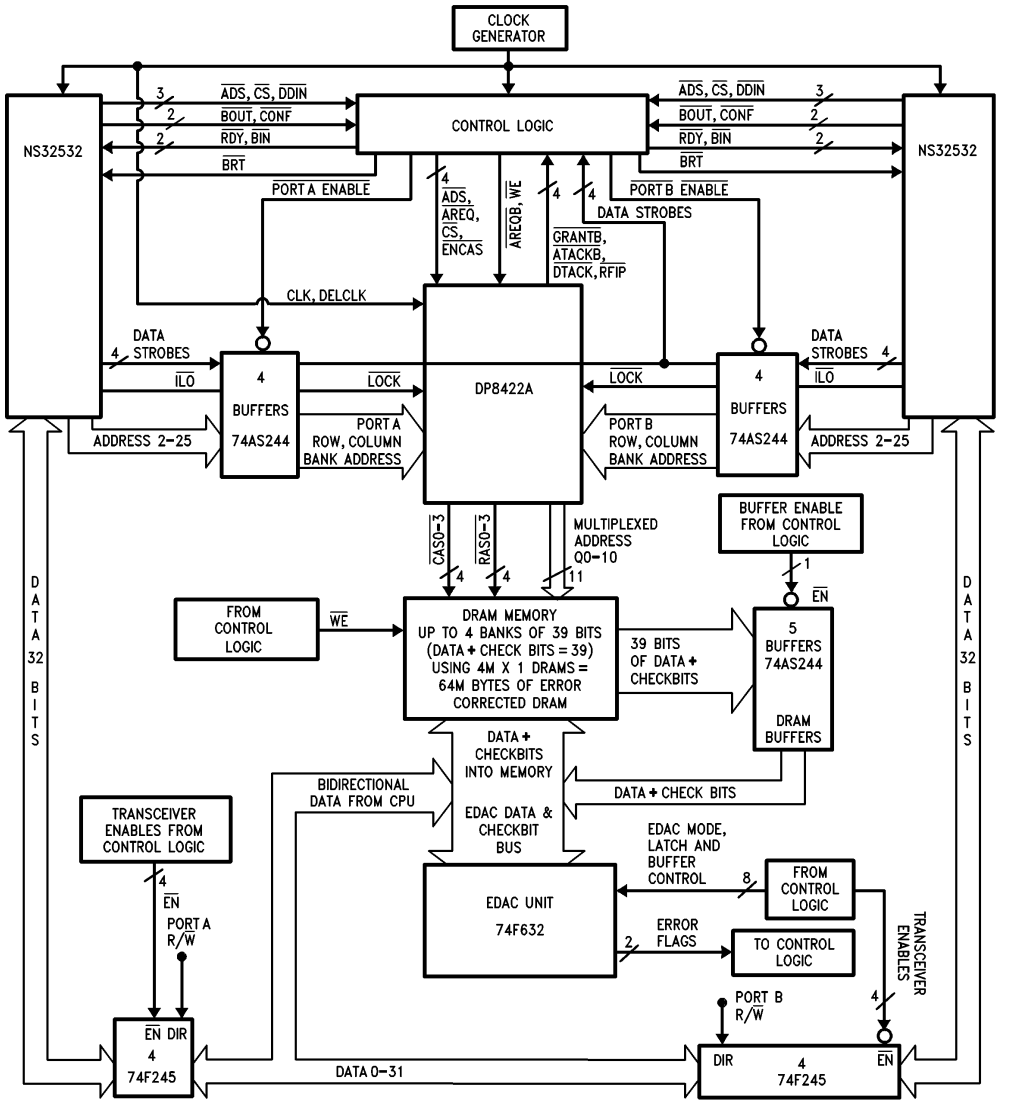

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FIGURE 1.NS32532 Dual Access EDAC Memory System Using the Always Correct Method (see Section III for how Block Diagram Changes for Error Monitoring Method)

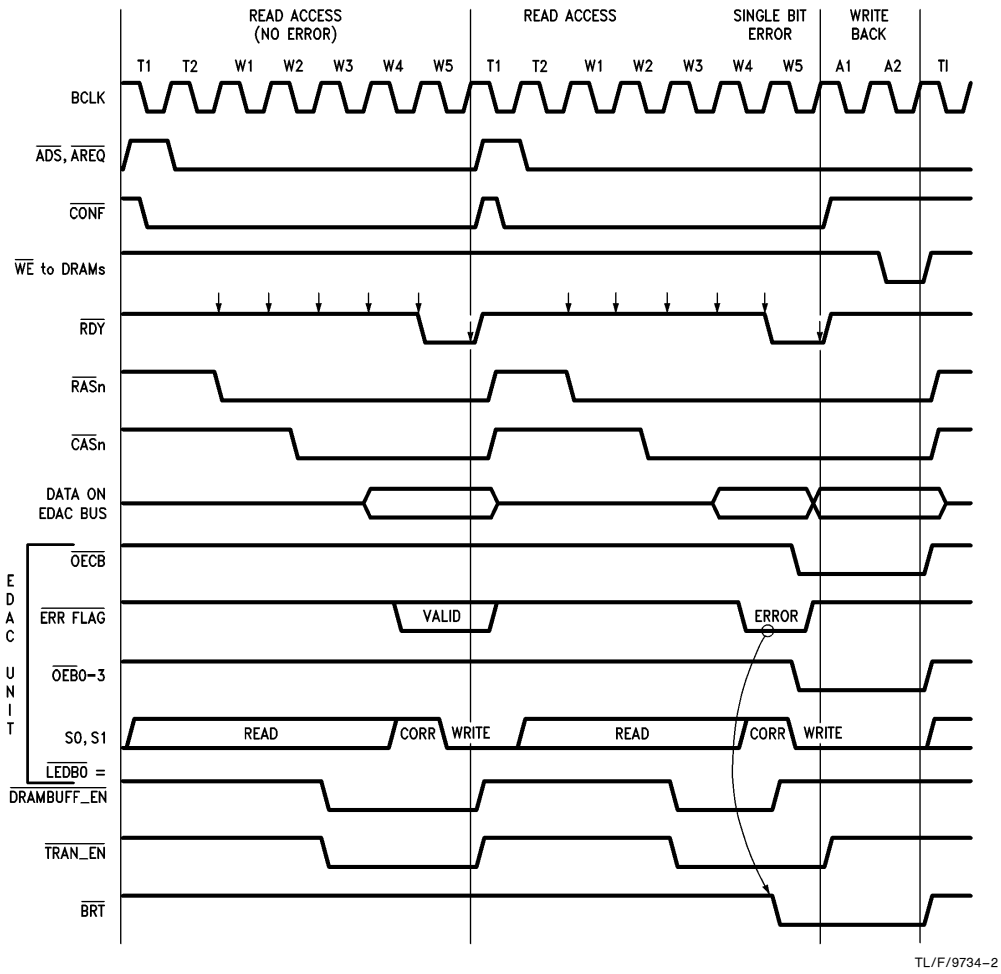

FIGURE 2. NS32532 Dual Access EDAC System Timing @ 25 MHz (DP8422A-25 74F632)
Error Monitoring Method Using the Bus Retry Input of the NS32532 and Registered Transceivers

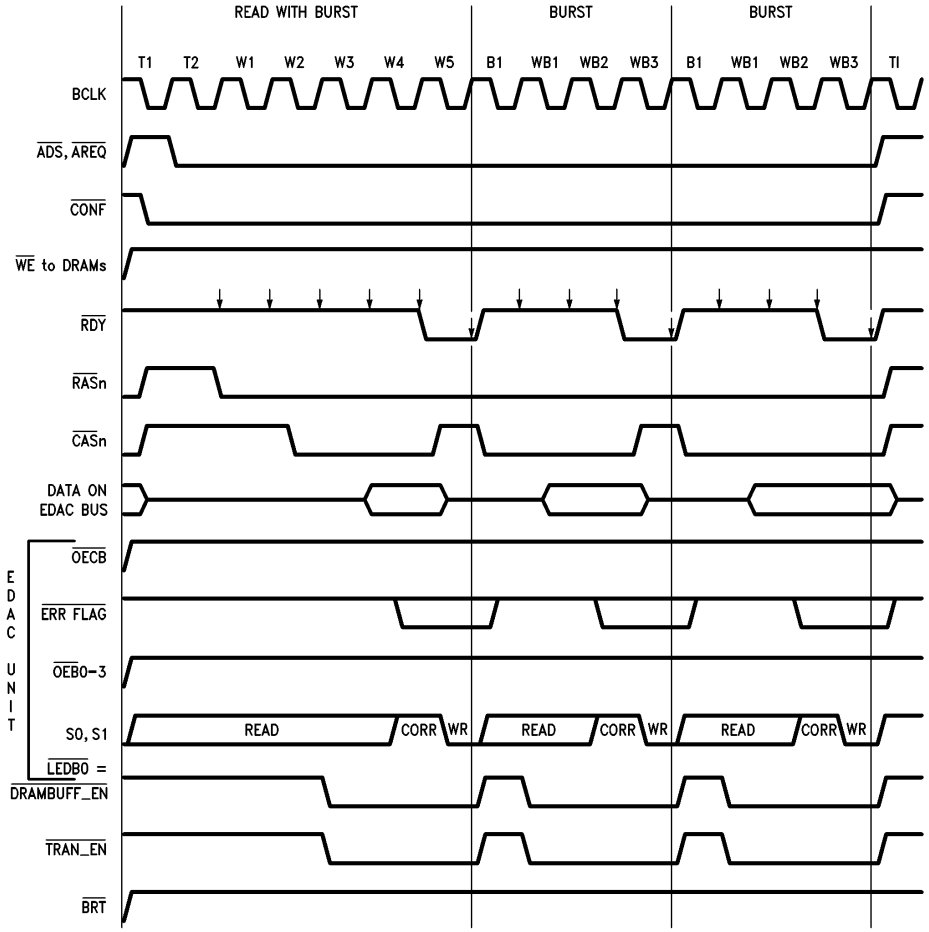

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FIGURE 3. NS32532 Dual Access EDAC System Timing @ 25 MHz (DP8422A-25, 74F632)
Error Monitoring Method Using the Bus Retry Input of the NS32532 and Registered Transceivers

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