Fast Eye-Pattern Generator (EPG) Board—Using the DAC0890

National Semiconductor
Application Note 750
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December 1990

INTRODUCTION

This application note describes the Eye-Pattern Generator (EPG) board that can be used to provide a variety of detailed diagnostic information for the modem design engineer. This data is extremely useful in the evaluation of the modem performance and line conditions.

GENERAL

The eye pattern generator board is a ''Plug-In Board'' to the XT compatible slots of National's Evaluation Development Boards. (In this application note the addresses match only to the NSV-FX-EDB, but a simple change of the address decoder can fit the EPG to the NSV-CG160EDB—running with the NS32FZ16, or the NSV-GX320EDB.) It converts digital data to an analog voltage that can be measured and displayed on a scope. The purpose of this board is to support debugging of the modem by displaying the complex numbers that have been received from the modem, in real time, showing the constellation points. The modem SW writes data to the EPG. The user selects which data is displayed on the scope.

EYE PATTERN

A quadrature eye pattern is an extremely useful diagnostic tool. The visual display of an eye pattern can be monitored to identify common line disturbances, as well as defects in the modem process. The ideal eye patterns or signal constellations for the various encoding methods are illustrated in *Figure 1* to *Figure 6*. In the polar coordinates each point represents a magnitude and a differential phase shift. Eye pattern data is updated at the baud rate so the oscilloscope display appears as a continuous signal constellation.

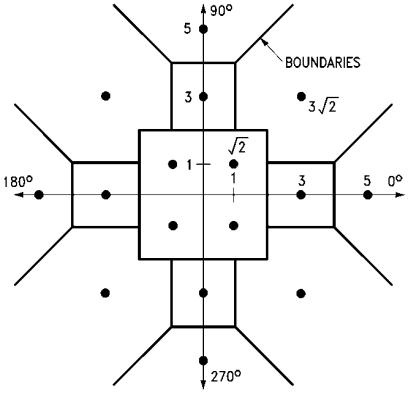

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FIGURE 1. Ideal Eye Pattern—V.29/9600 bps

Q2	Q3	Q4	Phase Change	Absolute Phase	Q1	Relative Amplitude
0	0	1	0°	0°, 90°, 180°, 270°	0	3
0	0	0	45°			
0	1	0	90°		1	5
0	1	1	135°			
1	1	1	180°	45°, 135°, 225°, 315°	0	$\sqrt{2}$
1	1	0	225°			
1	0	0	270°		1	$3\sqrt{2}$
1	0	1	315°			

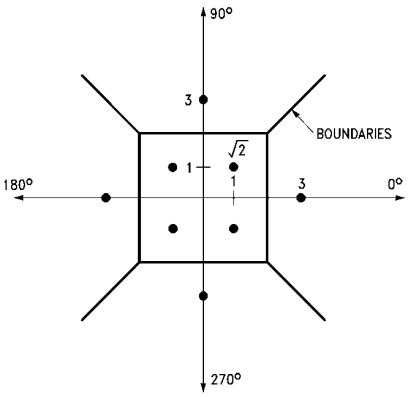

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FIGURE 2. Ideal Eye Pattern—V.29/7200 bps

TRIBIT Encoding

In V.29/7200 bps fallback mode, data is encoded in groups of 3 bits or tribits. The encoding is as for V.29/9600 bps above except that: The first data bit in time determines Q2 of the modulator quadbit. The second and third bits in time determine Q3 and Q4, respectively. Q1 = 0 for all eight signal elements.

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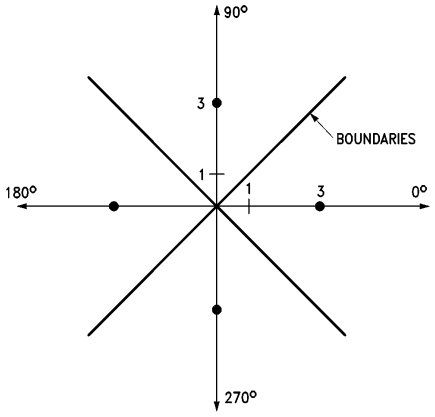

DIBIT Encoding

Data Bits	Phase Change	Relative Amplitude
0 0	0°	Constant
0 1	90°	
1 1	180°	
1 0	270°	

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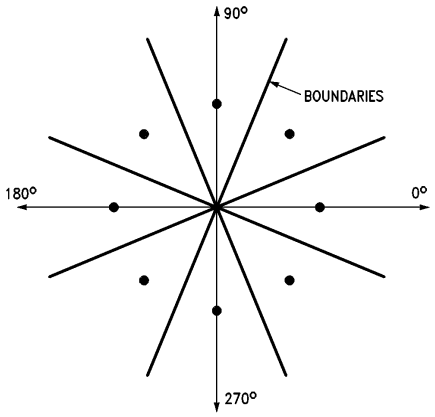
FIGURE 3. Ideal Eye Pattern—V.29/4800 bps and V.27/BIS/TER/2400 bps



TRIBIT Encoding

TRIBIT Value	Phase Change	Relative Amplitude
0 0 1	0°	Constant
0 0 0	45°	
0 1 0	90°	
0 1 1	135°	
1 1 1	180°	
1 1 0	225°	
1 0 0	270°	
1 0 1	315°	

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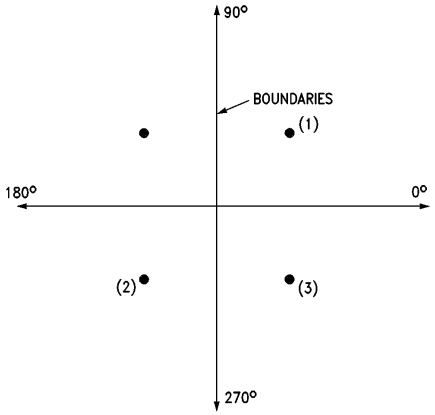
FIGURE 4. V.27 BIS/TER/4800 bps



DIBIT Values (1200)	Bit Values (600 bps)	Phase Change
0 0	0	+90°
0 1	—	0°
1 1	1	+270°
1 0	—	+180°

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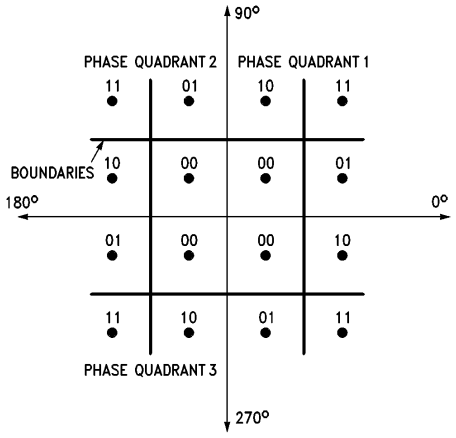
FIGURE 5. V.22 A/B 1200 bps/600 bps



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Data is encoded in QUADBITS. The first two bits or DIBIT select one of four quadrants. The second DIBIT selects one of four points in that quadrant, as shown below.

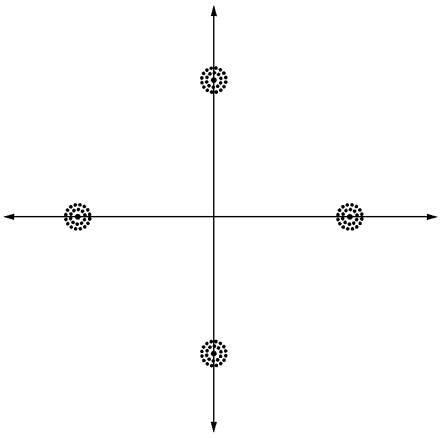
First Two Bits in QUADBIT [2400 Bit(s)] or DIBIT Values [1200 Bit(s)]	Phase Quadrant Change	
0 0	1 → 2 2 → 3 3 → 4 4 → 1	90°
0 1	1 → 1 2 → 2 3 → 3 4 → 4	0°
1 1	1 → 4 2 → 1 3 → 2 4 → 3	270°
1 0 0	1 → 3 2 → 4 3 → 1 4 → 2	180°

FIGURE 6. V.22 BIS/4800 bps

LINE DISTURBANCES

The received signal is distorted by one or more types of line disturbances and distortions, such as white noise, phase and amplitude jitter, harmonic distortions, phase and amplitude hits and drop-outs (out of boundaries).

1. White noise produces a smearing of each signal constellation point around its ideal location (see *Figure 7a*).
2. Phase jitter produces periodic phase smearing with little or no amplitude effect (see *Figure 7b*).
3. Amplitude jitter produces an effect similar to harmonic distortion, but in this case the distortion is periodic.
4. Harmonic distortion produces a non-periodic amplitude smearing with little phase effect (see *Figure 7c*).
5. An amplitude or phase hit is associated with an instantaneous big error in the amplitude or the phase of the signal.
6. The degree of smearing in the eye pattern is proportional to the severity of the particular disturbance. Several disturbances may occur simultaneously producing a complex smearing of the eye pattern. A point falling within the signal space delimited by boundaries is decoded by the modem as if it were located at the ideal point within that space. When a line disturbance causes the signal point to cross a decision boundary, the received signal is incorrectly decoded.



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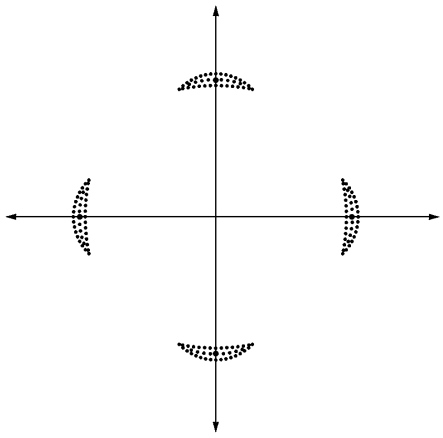
a. White Noise



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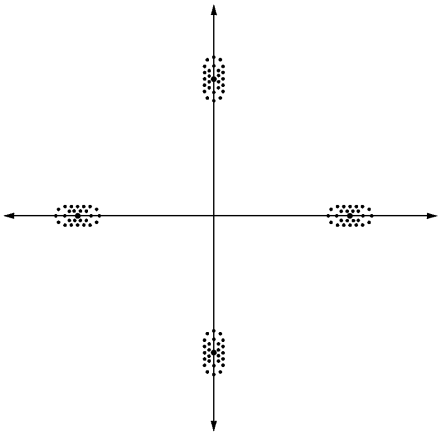
b. Phase Jitter



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c. Harmonic Distortion (Non-Periodic)
Amplitude Jitter (Periodic)

FIGURE 7. Typical Line Disturbances

DATA FORMAT

There are two channels on the card. Each of them displays a single byte. The bytes should contain numbers, represented by a 2's complement format, and they must be transferred to the EPG by ''move byte'' operation.

DISPLAY

The bytes can be displayed using the X ⟷ Y function of the scope (for eye-pattern display, where the data is two complex numbers), or X and Y as a function of time. It is possible to display up to 16 bytes (two bytes at the same time—one on each channel). The selector on the card selects the two bytes that will be displayed. The 16 addresses are in the addresses table below.

CONFIGURATION

The EPG board is a plug in board to the XT-compatible slots of National's Evaluation Development Boards. It has two connectors:

P1— Standard PC-XT connector.

J1, J2— Two BNC connectors on the mounting bracket (the connector lies outside the mother-board case).

The board has a thumbwheel-switch that can be set from outside the mother-board's case as well.

USAGE

To display the channels on the scope you have to connect the scope using a BNC to BNC cable, to the BNC connectors (J1 and J2) of the EPG. The selector controls the two bytes that will be displayed, by selecting a number from 0 to 7. (If the selector selects numbers from 8 to F, no byte will be displayed.) Displaying more then 8 points requires PAL changes. If the bytes are samples of the data it is possible to display them using the X ⟷ Y mode of the scope, and in that way to get the eye-pattern and the constellation points.

NS—MODEM

The NS Modem uses some channels of the EPG for debug. Position ''0'' of the selector is used to measure the CPU utilization. Channel 1 is used to show the timing of the modem routine including the overhead of the interrupt handler, which is written in assembly. Channel 2 is used to show the timing of the ''internal C-code'' of the modem alone without the overhead of the assembly interrupt handler (both work only during reception). In both cases, a value of 0x7f is written to the port upon entering the inspected code, and a value of 0x0 upon exit. So, the display that appears on the scope is a square wave that is high during the execution of the MODEM-SW (internal C-code of the modem). The duty cycle shows the CPU utilization of the MODEM. Position ''1'' of the selector is used for displaying a complex-plane representation of the received/transmitted points (both real and imaginary components are used together).

ADDRESSES

The addresses that are used for this board, match only the NSV-FX-EDB. The table below shows the addresses and their selected number on the selector. They must be asserted as byte addresses (movb).

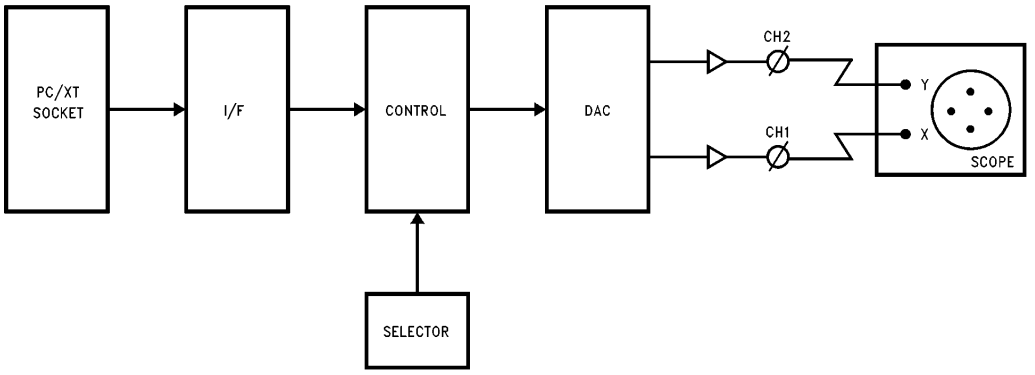
Eye Pattern Select-Address Table

Select Number	Address	Channel Number
0	0c00100	1
0	0c00102	2
1	0c00104	1
1	0c00106	2
2	0c00108	1
2	0c0010a	2
3	0c0010c	1
3	0c0010e	2
4	0c00110	1
4	0c00112	2
5	0c00114	1
5	0c00116	2
6	0c00118	1
6	0c0011a	2
7	0c0011c	1
7	0c0011e	2
8–f	xxxxxxx	—

CIRCUIT DESCRIPTION

The data bus and the address bus are buffered on the board. The DAC Controller PAL (DACCON), compares between the address and the selected pair of channels from the selector (the thumbwheel-switch). If they match, the appropriate CS is asserted and the DAC0890 latches the data from the data bus. The MSB (D7) is inverted because the data is in 2's complement format. The analog signal output is biased around 0 V_{DC} by operational amplifiers. The potentiometers (PR1 and PR2) are used to calibrate the board's output (at J1 and J2) to 0 V_{DC} while 0 is transferred to the DAC. The RESET signal of the mother-board, resets the EPG as well. Since the DAC0890 is a fast chip, it can work faster then the P996 standard. The DACCON generates a signal ZWS that can be used to shorten the access to the EPG. This signal is asserted when there is an access to the selected channel of the EPG. This signal is inverted with an open-collector inverter and asserted to the mother-board through a jumper W1. In case that this option is requested W1 must be close. If this option is not requested at all, don't install the inverter (U7).

Block Diagram



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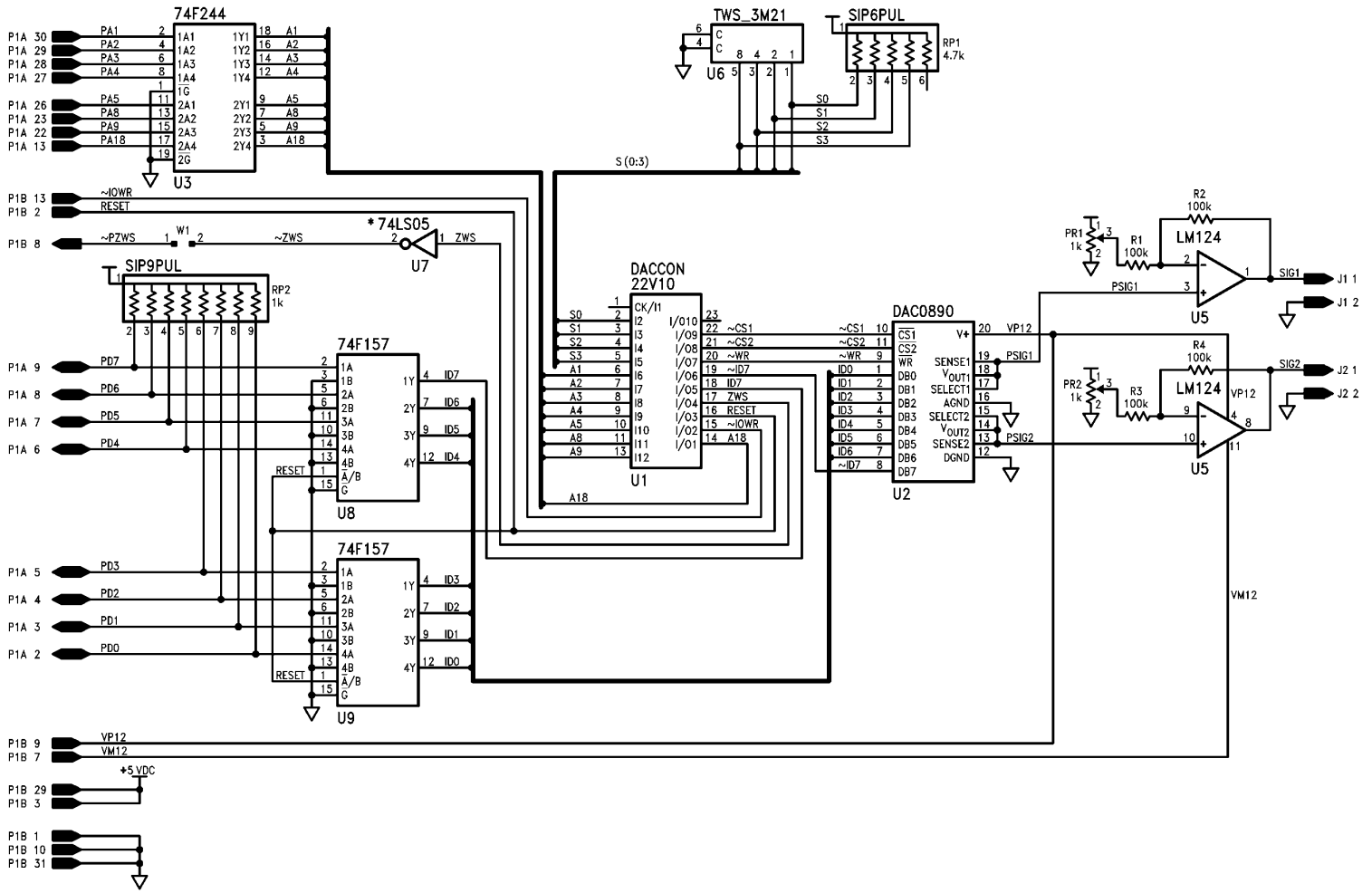

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*Install only in case of zero wait states

PAL EQUATIONS

```
module daccon
flag '-r3' , '-t2'
title ' DAC0890 control              EREZ BAR-NIV'

" The GAL generates two enable signals
"The signals are :!~CS1 - to enable DAC-LATCH1
"                 !~CS2 - to enable DAC-LATCH2
"The GAL get addresses from A1 to A5 and A8,A9,A18.
"The GAL get addresses select from S0 to S3
"The enable signals are asserted if the write to the address of the
"DAC is the same as the address that the selector is select.
"The GAL get : !~IOWR & RESET signals
"The GAL generate the ~WR signal to the DACs when IOWR is asserted and when
"there is a reset (so the DACs will reset to).

"**************************************
" Date:   Thu Nov 15 11:11:21 EET 1990
" Checksum:   8A76
"**************************************

    DACCON          device 'p22v10';

"INPUTS


S0        pin  2; " address select 0
S1        pin  3; " address select 1
S2        pin  4; " address select 2
S3        pin  5; " address select 3
A1        pin  6; " address 1
A2        pin  7; " address 2
A3        pin  8; " address 3
A4        pin  9; " address 4
A5        pin 10; " address 5
A8        pin 11; " address 8
A9        pin 13; " address 9
A18       pin 14; " address 18
~IOWR     pin 15; " ~IOWR of CG16
RESET     pin 16; " reset of CG16
ID7       pin 18; " Data bit D7

"OUTPUTS

ZWS       pin 17; " Zero Wait State to the EDB
~ID7      pin 19; " Opposite of data bit D7
~WR       pin 20; " Write to the DAC
~CS2      pin 21; " Latch Enable of DAC2
~CS1      pin 22; " Latch Enable of DAC1

x = .X.;

ADD = [x,x,x,x,x,A18,x,x,x,x,x,x,x,x,A9,A8,x,x,A5,A4,A3,A2,A1,x];

SELECT = [!S2,!S1,!S0];

equations

~ID7 = !ID7 # RESET;

!~CS1 = RESET #(!~IOWR & ((S3 &(A2 == !S0)&(A3 == !S1)&(A4 == !S2)) &
       ((ADD == ^h0c00100)#(ADD == ^h0c00104)#(ADD == ^h0c00108)#
        (ADD == ^h0c0010c)#(ADD == ^h0c00110)#(ADD == ^h0c00114)#
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```
        (ADD == ^h0c00118)#(ADD == ^h0c0011c))));

!~CS2 = RESET #(!~IOWR & ((S3 &(A2 == !S0)&(A3 == !S1)&(A4 == !S2)) &
       ((ADD == ^h0c00102)#(ADD == ^h0c00106)#(ADD == ^h0c0010a)#
        (ADD == ^h0c0010e)#(ADD == ^h0c00112)#(ADD == ^h0c00116)#
        (ADD == ^h0c0011a)#(ADD == ^h0c0011e))));

!~WR = !~IOWR # RESET;     "This signal is different from ~IOWR only during
                           "reset so the DAC will reset to

ZWS = !~CS1 # !~CS2;


test_vectors ([ADD ,SELECT,!S3,~IOWR]->[~CS1,~CS2])
              [^h0c00100,0,0 ,  0  ]->[0 , 1 ];
              [^h0c00102,0,0 ,  0  ]->[1 , 0 ];
              [^h0c00100,1,0 ,  0  ]->[1 , 1 ];
              [^h0c00100,0,1 ,  0  ]->[1 , 1 ];
              [^h0c00100,0,0 ,  1  ]->[1 , 1 ];
              [^h0c00104,1,0 ,  0  ]->[0 , 1 ];
              [^h0c00106,1,0 ,  0  ]->[1 , 0 ];
              [^h0c00106,4,0 ,  0  ]->[1 , 1 ];
              [^h0c00104,1,1 ,  0  ]->[1 , 1 ];
              [^h0c00104,1,0 ,  1  ]->[1 , 1 ];
              [^h0c00108,2,0 ,  0  ]->[0 , 1 ];
              [^h0c0010a,2,0 ,  0  ]->[1 , 0 ];
              [^h0c0011a,7,0 ,  0  ]->[1 , 1 ];
              [^h0c00118,2,1 ,  0  ]->[1 , 1 ];
              [^h0c0011a,6,0 ,  1  ]->[1 , 1 ];
              [^h0c0011a,6,0 ,  0  ]->[1 , 0 ];

end
```

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