IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications

National Semiconductor
Application Note 829
Joel Martinez
Application Engineer
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INTRODUCTION

IEEE 1194.1 Standard for Electrical Characteristics of Backplane Transceiver Logic Interface Circuits validates BTL as the enabling technology for high speed busses. Driving backplanes with BTL means higher data rates and better noise margins than previously available.

BTL solves, for the first time, the fundamental problem associated with driving a densely populated backplane. As a result, it provides significant improvements in both speed and data integrity. BTL evolved from many years of work within the IEEE committee, leading to a deeper understanding of the physics of the backplane bus and an ingenious solution to the bus driving problem.

Speed is probably the most important feature for any bus standard. In many cases the backplane becomes the bottleneck in systems where increasing processor speed and shared resources are common. In asynchronous systems, the maximum data transfer rate between any two plug-in cards is determined simply by the sum of the response times of the two cards and the bus delay. Ultimately, as logic devices get faster, bus delay will be the dominating factor limiting bus speed. In synchronous systems, the maximum achievable clock rate on the bus will also depend on the bus delay.

There are two components to the bus delay in a typical system, namely, the settling time and the propagation delay. The settling time is the time needed for reflections and crosstalk to subside before data are sampled; it is usually several times longer than the backplane propagation delay. As will be shown later, the settling time is the price the user pays for not driving the bus properly.

By using BTL, backplane busses not only eliminate the settling time delay but also reduce the propagation delay of the loaded backplane to provide maximum possible bus throughput.

THE PHYSICS OF THE BACKPLANE BUS

For high-speed bus signals where the signal rise and fall times are less than the round-trip delay, the bus acts as a transmission line with an associated characteristic impedance and propagation delay whose unloaded values, Z_o and tp_o are given by

$$Z_o = \sqrt{\frac{L_o}{C_o}} \quad (1)$$

$$tp_o = \sqrt{L_o C_o} \quad (2)$$

where,

L_o = Distributed intrinsic inductance per unit length

C_o = Distributed intrinsic capacitance per unit length [1]

These values can be calculated for a typical stripline backplane (*Figure 1*) by means of the following equations;

$$Z_o = \frac{60}{\sqrt{\epsilon_e}} \ln\left[\frac{4h}{0.67\pi\,(0.8w + t)}\right] \quad (3)$$

$$tp_o = 1.017\sqrt{\epsilon_r} \quad (4)$$

where,

ϵ_r = relative dielectric constant of the board material

h = height between ground planes

w = width of signal trace

t = thickness of signal trace [5]

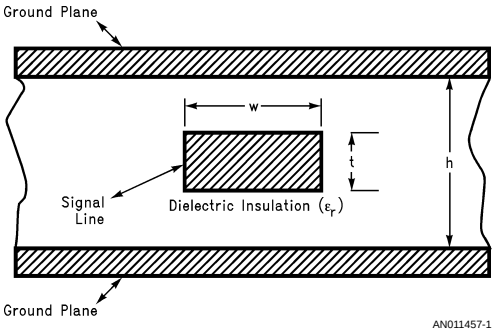

FIGURE 1. Stripline

For a typical backplane, h = 52 mils, w = 12 mils, t = 1.4 mils (1 oz. Copper), ϵ_r = 3.5 (epoxy-glass). By substituting these values we get Z_o = 70Ω and tp_o = 1.9 ns/ft.

These values correspond to an unloaded backplane. When the backplane is uniformly loaded with the capacitance of plug-in cards and connectors at frequent intervals, the loaded values of the impedance, Z_L, and the propagation delay, tp_L, are given by

$$Z_L = \frac{Z_o}{\sqrt{1 + \frac{C_L}{C_o}}} \quad (5)$$

$$tp_L = tp_o\sqrt{1 + \frac{C_L}{C_o}} \quad (6)$$

where,

C_L = distributed load capacitance per unit length[1]

The distributed capacitance, C_o, of the unloaded backplane can be derived from *Equation (1)* and *Equation (2)*.

$$C_o = \frac{tp_o}{Z_o} \quad (7)$$

For our stripline,

$$C_o = \frac{1.9\,\frac{ns}{ft}}{70\Omega} = 27\,\frac{pF}{ft}$$

This does not include, however, the capacitance of the connectors mounted on the backplane and the associated plated-through holes, which can amount to 5 pF per card slot.

The loading capacitance of the plug-in card, however, is dominated by the loading capacitance of the transceiver, which may be 12–20 pF for TTL devices. Allowing another 3–5 pF for printed-circuit traces and the connector, the total loading per card slot may add up to 25 pF. For a backplane where the spacing between adjacent slots is 0.8 inch, the capacitance per unit length is given as

$$C_L = \frac{1}{d_{slot}} \left(\frac{12 \text{ in}}{1 \text{ ft}} \right) (C_{slot})$$

where,

d_{slot} = slot to slot spacing

C_{slot} = capacitance per slot

For the example above,

$$C_L = \frac{1}{0.8 \text{ in}} \left(12 \frac{\text{in}}{\text{ft}} \right) (25 \text{ pF}) = 375 \frac{\text{pF}}{\text{ft}}$$

Therefore,

$$Z_L = \frac{70\Omega}{\sqrt{1 + \frac{375 \frac{\text{pF}}{\text{ft}}}{27 \frac{\text{pF}}{\text{ft}}}}} = 18\Omega$$

From *Equation (5)*

$$tp_L = 1.9 \frac{\text{ns}}{\text{ft}} \times \sqrt{1 + \frac{375 \frac{\text{pF}}{\text{ft}}}{27 \frac{\text{pF}}{\text{ft}}}} = 7.3 \frac{\text{ns}}{\text{ft}}$$

From *Equation (6)*

As can be seen above, the capacitive loading drastically alters both the impedance and the propagation delay of the bus. This reduces the bus throughput in two ways. One obvious impact is the increased propagation delay. But the not so obvious and even more serious problem is the reduced bus impedance, which is much harder to drive.

For example, to drive the loaded bus properly with a TTL driver which has a 3V nominal swing, the required drive current, I_D, must be

$$I_D = \frac{3V}{\left(\frac{Z_L}{2} \right)}$$

The impedance seen by the driver is half of Z_L, since from a given board two transmission lines are being driven in parallel towards each terminator (*Figure 2*). Therefore,

$$I_D = \frac{3V}{\left(\frac{18\Omega}{2} \right)} = 333 \text{ mA}$$

This is much higher than the standard TTL's drive capability of 50 mA to 100 mA. *Figure 3* shows the effect of using a 50 mA driver, in this situation, on the bus waveform. The voltage swing on the bus has its first transition at 0.45V, the product of the drive current and the $Z_L/2$ (loaded impedance in parallel). This value falls well below the upper threshold limit of the TTL receiver. Therefore, several round-trip delays to the nearest termination are required for the waveform to cross the receiver threshold region. In our example, one round-trip delay for a 19 inch backplane is given by

$$t_{(2\ d)} = 2\ (tp_L)\ (\text{length})$$

$$t_{(2\ d)} = 2 \left(7.3 \frac{\text{ns}}{\text{ft}} \right) (19 \text{ in}) \left(\frac{1 \text{ ft}}{12 \text{ in}} \right) = 23 \text{ ns}$$

Therefore, settling times can exceed 100 ns even for relatively short buses. This long settling time drastically affects bus throughput at high speeds. Even worse, the voltage steps in the threshold region may cause multiple triggering in the clock and strobe cases.

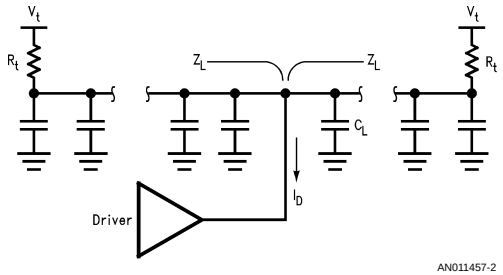

FIGURE 2. Driver Sees Two lines in Parallel ($Z_L \parallel Z_L = Z_L/2$)

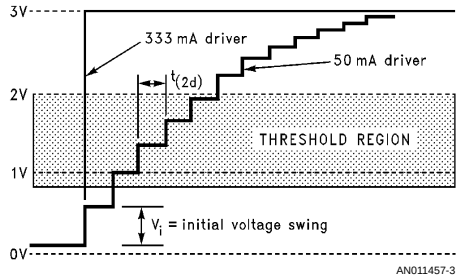

FIGURE 3. TTL Bus Waveforms (50 mA vs 333 mA Driver)

One way to solve these problems is to use high current drivers with precision receivers that have a narrow threshold region such that the first transition crosses well over the threshold. This technique is widely used for clock lines to avoid multiple triggering. Its use on data/address lines is limited because of the significantly higher power requirements arising from the large number of lines involved (32 or 64 address/data lines).

Even if power is not a limitation, switching to higher current drivers provides only a marginal improvement. The reason for this is quite simple. A high current driver unfortunately has a higher output capacitance, which reduces the bus impedance further. This in turn requires an even higher current drive for proper operation.

IEEE 1194.1 — BTL

A more elegant solution — one that is now IEEE 1194.1 Backplane Transceiver Logic — directly attacks the root of the problem, namely, the large output capacitance of the driver. IEEE 1194.1 specifies the maximum input/output ca-

pacitance to less then 5 pF. One BTL implementation is to add a Schottky diode in series with an open-collector driver output. The capacitance of the drive transistor is isolated by the small reverse-biased capacitance of the diode in the non-transmitting state (*Figure 4*). The Schottky diode capacitance is typically less than 2 pF and is relatively independent of the drive current. Allowing for a receiver capacitance of another 2 pF, the total loading of a BTL transceiver is kept under 5 pF.

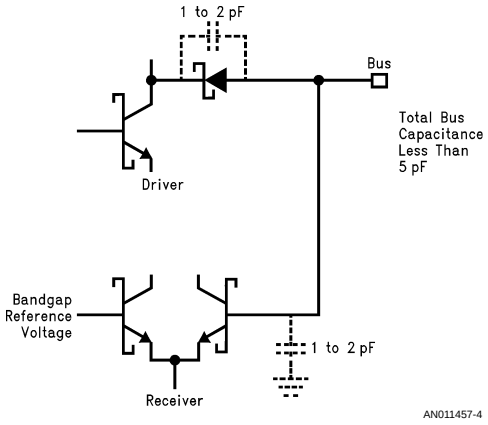

FIGURE 4. Typical BTL Input/Output Structure

In addition to reducing the loading on the bus, BTL features several other enhancements over a conventional TTL transceiver that drastically reduce power consumption and improve system reliability.

A major portion of the power saving comes from a reduced voltage swing (1V) on the bus. Contrary to popular belief, the lower swing does not reduce crosstalk immunity (provided the receiver threshold is tightly controlled). The induced crosstalk from other lines on the bus scales down with the amplitude of the signal transition causing it. Consequently, if a line receiver has a precision threshold, the noise margin, expressed as the percentage of signal amplitude, remains the same, as does the crosstalk immunity. However, the absolute noise margin, with reference to a noise source external to the bus, does shrink linearly with amplitude. Fortunately, the low impedance and the relatively short length of the bus make this externally generated noise component insignificant in high-speed backplanes. Nevertheless, it is recommended that the backplane be shielded from strong noise sources external to the bus. Strip-line construction for backplanes provide excellent shielding from the environment but also aids in reducing crosstalk.

NOISE IMMUNITY AND EMI

IEEE 1194.1-BTL specifies a precision receiver threshold centered between the low and high bus levels of 1V and 2.1V, respectively (*Figure 5*). Confined to a narrow region of 1.55V ±75 mV (1.47V to 1.62V), the threshold voltage is independent of V_{CC} and temperature. This tight threshold control is achieved by using an internal bandgap reference at the receiver input *Figure 4*). And with a smaller 1V swing, EMI is also reduced threefold compared with TTL.

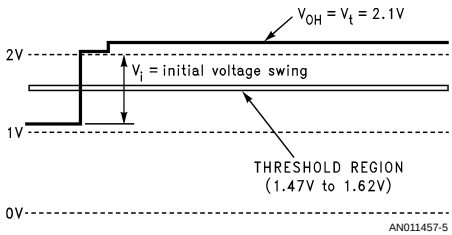

FIGURE 5. BTL Bus Waveforms — IEEE 896 Electrical Environment

IEEE 896 — Futurebus+ ELECTRICAL

The bus termination, backplane impedance and module capacitance tolerance are found within IEEE 896.2 Physical Layer and Profile Specifications. The electrical specification for Profiles A, B and F are found in chapters 6, 7 and 8, respectively. The nominal backplane impedance for the profiles listed above is specified as 60Ω for an unloaded backplane with vias. Without the vias, the backplane impedance Z_o is 67Ω with C_o = 29 pF/ft. The load capacitance per slot is the sum of the backplane via and backplane connector capacitance plus the board capacitance. C_{slot} is calculated below,

$C_{slot} = C_{via} + C_{connector} + C_{board}$

C_{slot} = 0.75 pF + 0.45 pF + 10 pF

C_{slot} = 11.2 pF

The load capacitance C_L is

$$C_L = 11.2\,pF\left(\frac{1}{1.2\,in}\right)\left(\frac{12\,in}{1\,ft}\right) = 112\,\frac{pF}{ft}$$

Note: d_{slot} = 30mm (about 1.2 inches)

The fully loaded Futurebus+ backplane therefore, has an impedance value given by

$$Z_L = \frac{67\Omega}{\sqrt{1 + \frac{112\,\frac{pF}{ft}}{29\,\frac{pF}{ft}}}} = 30\Omega$$

From *Equation (6)*

The drive current required for a 1V swing is

$$I_D = \frac{1V}{\left(\frac{30\Omega}{2}\right)} = 67\,mA$$

The current drive capability for BTL with V_t = 2.1V, R_t = 33Ω as specified in IEEE 896.2, is

$$I_D = \frac{\mathbf{2.1V} - \mathbf{1.1V}}{\left(\frac{\mathbf{33\Omega}}{2}\right)} = \mathbf{61}\ \text{mA}$$

The current drive capability of BTL is finely tuned to accomplish incident wave switching even for worse case loading situations. On the first transition, the signal passes threshold with a very comfortable noise margin as shown on *Figure 5*.

OTHER HIGHLIGHTS

As a result of reducing capacitive loading, the propagation delay decreased which further improves the bus speed.

Recalculating the loaded propagation delay for the Futurebus+ example yields

$$tp_L = \mathbf{1.9}\,\frac{\text{ns}}{\text{ft}} \times \sqrt{1 + \frac{\mathbf{112}\,\frac{\text{pF}}{\text{ft}}}{\mathbf{29}\,\frac{\text{pF}}{\text{ft}}}} = \mathbf{4.2}\,\frac{\text{ns}}{\text{ft}}$$

From *Equation (7)*

This is a 40-percent improvement over the TTL example given earlier.

It should be noted that this is the worst-case delay per foot and that the asynchronous nature of the Futurebus+ protocol will take full advantage of lower propagation delays in a typical system, either due to lower loading levels or the closer spacing of two plug-in boards that are in communication.

TERMINATION AND DRIVE CURRENT

IEEE 1194.1 specifies that BTL drivers shall be capable of sinking 80 mA (I_{OL}) at V_{OL} levels within 0.75V to 1.1V. In practice, the backplane is terminated such that the driver I_{OL} is less than 80 mA.

The drive current and the signal swing requirements determine the termination resistor value. If the drive current is derived properly, the termination will match the bus impedance under the given loading. For IEEE 896.2, the value of each of the two termination resistors (R_t) is derived below

$$R_t = \left(\frac{\mathbf{1V}}{\mathbf{67}\ \text{mA}}\right) 2 = \mathbf{30\Omega} \approx \mathbf{33\Omega}$$

The value chosen by the Futurebus+ electrical task group was 33Ω. The Futurebus+ Electrical Task Group performed many hours of simulation and deduced 33Ω to be the optimum value for the range of loaded and unloaded impedance of the backplane. Their thorough analysis included the effects of crosstalk, reflections, ground shift, ground bounce, termination shift, termination tolerance and multiple switching.

IEEE 896.2 requires the resistor tolerance to be within plus or minus 1% and the termination voltage (V_t) be within plus or minus 2%. Both ends of the backplane are terminated with active terminations as shown in *Figure 6*. This arrangement has significantly lower power dissipation than a "Thevenin-equivalent" two-resistor termination connected to ground and the 5V rail. The source may be shared among bus lines as long as it is properly bypassed for alternating current close to each resistor. Bypass networks should be capable of maintaining V_t within the specified tolerance during multiple switching where each bus line will source and sink at least 61 mA. Finite resistance, although small, should be taken into account when designing the termination network to compensate for voltage drops on terminations farthest from the source.

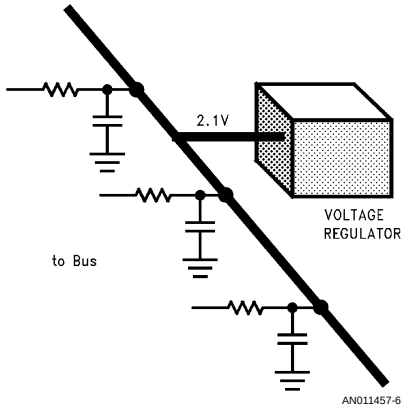

FIGURE 6. BTL Termination

WIRED-OR GLITCH

One of the advantages of an open-collector type bus is a wired-OR capability. This feature is fully exploited in Futurebus+, particularly in its sophisticated arbitration protocol, broadcast and handshake mechanism. Unfortunately, due to the fundamental nature of transmission lines, WiredORing on the bus may cause erroneous glitches having pulse widths of up to the round-trip delay of the bus. The analysis of the wired-OR glitch is covered well in Application Note 744, "Futurebus+ Wired-OR and Glitch Effects and Filter".[(2)]

TRANSITION TIME

The rise and fall times affect the amount of unwanted noise and reflection present in a system. When it comes to transition times, faster is not always better. Drivers with fast rise and fall times induce more noise and reflections in a system than do drivers with slower rise and fall times. Some of the noise will come from voltage spikes caused by parasitic inductance in the system described by

$$V = L\frac{di}{dt}$$

where,

V = Amplitude of voltage spike

L = Inductance

di = Current through the inductor

dt = rise time

Slower rise times will reduce the amplitude of voltage spike from inductance in the current paths. Futurebus+ minimizes this problem by specifying a maximum slew rate, slew rate is the inverse of rise time. IEEE 896.2 specifies that BTL drivers shall have a maximum slew rate of 0.5V/ns or a minimum rise and fall time of 1 ns measured between 1.3V and 1.8V.

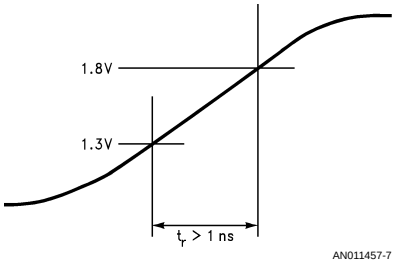

FIGURE 7. IEEE 896.2 Rise and Fall Time Specification

MORE ON FUTUREBUS+

Geographic addressing, live insertion and withdrawal capability are some of the other highlights of Futurebus+.

The use of BTL within the Futurebus+ Electrical environment is based on a thorough knowledge of backplane operation and transmission line physics. A combination of theoretical analysis, extensive simulations and bench measurements has been used to create an electrically clean bus environment. Significant improvements have been made in favor of higher performance — at the expense of only a slight increase in today's cost and complexity — to assure a long design lifetime for the standard. The result is a robust standard that has the performance, in terms of both speed and reliability, to justify the name "Futurebus+".

PROPRIETARY BACKPLANES

The examples given above were based on the use of BTL in a Futurebus+ electrical environment. BTL is also found in many proprietary backplanes which have different requirements than those of Futurebus+. The termination resistor should be optimized to specific backplane parameters such as slot-to-slot spacing, backplane length, bus configuration, module capacitance and backplane impedance.

National also offers BTL transceivers that are similar to IEEE 1194.1 and offer other important features, such as trapezoidal drivers. The output waveform from BTL trapezoidal drivers have controlled rise and fall times which resemble a trapezoid as shown in *Figure 8*. The 6 ns transition times lead to reduced crosstalk, ground bounce and reflections. The drawback is a slower propagation delay compared to non-trapezoidal BTL drivers.

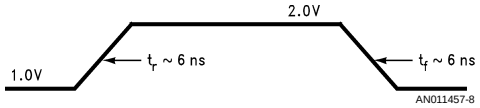

FIGURE 8. Trapezoidal Drivers Output Waveform

ACKNOWLEDGEMENT

Special thanks to R.V. Balakrishnan for his earlier article "IEEE 896 Futurebus — A Solution to the Bus Driving Problem" of which much of this is based upon.(1)

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