LM3001/LM3101 A 1 MHz Off-Line PWM Controller Chipset with Pulse Communication for Voltage-Current- or Charge-Mode Control

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1.0 INTRODUCTION

In isolated DC/DC converters the output voltage is controlled either via a tertiary winding on the main flyback transformer or via direct feedback from the secondary side. If good load-regulation is required the second method is used. In this case two ICs are necessary to control the converter. Typically opto-coupler communication is used which requires a reference and an error amplifier on the secondary side. In effect, a chipset is used to control the isolated DC/DC converter. The actual PWM controller resides on the primary side. Its reference and error amplifier are not used. One of the disadvantages of the opto-coupler solution is that it introduces an extra time-constant in the control loop. This is not a problem in conventional converters operating in the 100 kHz frequency range. However, at 500 kHz to 1 MHz, in typical modern high frequency designs, the opto-coupler may limit the control loop's speed significantly. The standard 1N27 opto-coupler for example has a typical −3 dB frequency of 15-30 kHz, depending on the DC operating point. This yields a phase shift of 30 to 50 degrees at 30 kHz. Generally, a flyback converter operating at 500 kHz has a loop crossover frequency in this range. This excess phase shift forces the designer to slow down the loop by pushing down the crossover frequency below 10 kHz. The well-known aging of typical opto-couplers accentuates the problem by requiring significant overdesign of the control loop.

The LM3001/LM3101 new chipset, uses pulse communication for the first time in a high frequency off-line environment(1). It is essentially a digital communication method which does not introduce any extra time-constants into the control loop, yielding the highest possible bandwidth. The pulse transformer, used for communication, requires only very few turns (typically 2T:2T) resulting in small size and low cost, comparable with the opto-coupler solution. Due to the ''chipset philosophy'' that was used from the inception of the controllers, both chips are optimized for their specific functions in the system. The Primary Side Driver is optimized for speed, while the Secondary Side Controller is optimized for precision, flexibility and special functions.

2.0 FUNCTIONAL DESCRIPTION

The Primary Side Driver chip has all the functions necessary to start up an isolated DC/DC converter with the standard bootstrap method. Its startup current is 200 μA typically, low enough for resistive startup in off-line supplies. When the output voltage reaches the undervoltage lockout level of the Secondary Side Controller it starts sending pulses to the primary side via the small pulse transformer. At this point, the control is taken over by the secondary chip and the primary IC acts as a slave. It turns on and off in response to the positive and negative pulses from the secondary controller. There is no handshake between the primary and secondary side, yielding maximum speed.

Moreover, it is very important that the system be well-behaved under output short and open circuit conditions. In short circuit the supply voltage of the secondary controller chip gradually disappears. The same is true for the primary chip which is powered from a tertiary winding in a typical flyback application. When the tertiary voltage reaches the lower threshold of the undervoltage lockout the IC is disabled and it draws only 200 μA, enabling the tertiary capacitor to charge up. In sustained short circuit the system oscillates in the startup mode, charging and discharging the tertiary filter/buffer capacitor. The power MOSFET and the IC are fully protected in this mode.

In no-load condition the secondary controller does not send any pulses to the primary side if the output voltage is higher than nominal. The primary driver does not turn on the power MOSFET as long as no pulses from the secondary are present. This yields the well-known burst mode operation, or pulse skipping. As a result, the converter operates down to zero load without loss of regulation in both voltage and current-mode operation.

3.0 LM3001—THE PRIMARY SIDE DRIVER IC

The Primary Side Driver is optimized for operating speed. It slews a 1 nF load-capacitor in 11 ns, typically. Its output stage has no shoot-through, yielding operation well beyond the specified 1 MHz. Its rise and fall time with a 20 nF load are typically 100 ns. This enables the chip to drive large power MOSFETs (size 6) directly, without a separate driver IC. To fully realize the above feature, the driver provides a typical sink capability of 400 mA at 1.5V, more than twice the industry standard.

Figure 1 shows the block diagram of the Primary Side Driver IC. The oscillator frequency is set by R_T and C_T. The control pulses from the secondary are coupled in via the PIN pin. The fast interface and logic circuitry yields short input to output propagation delay (typically 33 ns at turn-on and 30 ns at turn-off) with a reasonable power consumption.

The current limit circuitry has dual thresholds at 400 mV and 600 mV. The second level current limit activates a timed shut-down, controlled by the capacitor on the C_{SD} pin. This feature eliminates the possibility of short circuit run-away. The comparator circuit, used for both current limit levels, use the fast (ft = 30 MHz) lateral PNP transistors, available on this process, as level shift devices. This yields a very respectable speed-power product: 100 mW ns with 30 mV overdrive. It corresponds to a 50 μs typical current limit to output delay.

The output voltage's slew-rate during startup is controlled by a soft-start capacitor connected to the C_{SS} pin. The charge current for both the soft-start capacitor and the shut-down time-out capacitor (C_{SD}) are set by the external oscillator timing resistor R_t and the internal bandgap reference.

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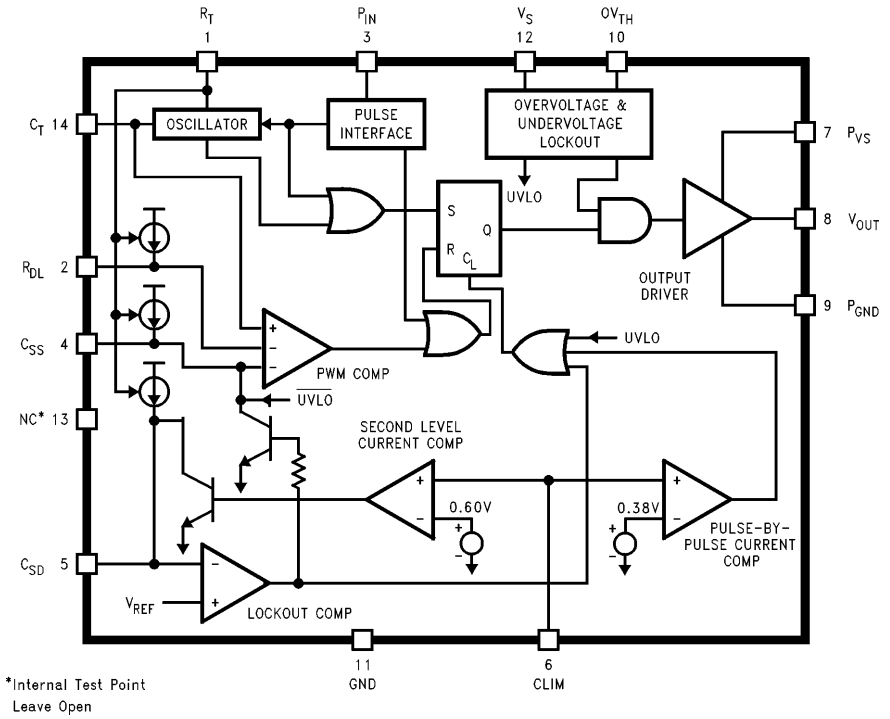

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FIGURE 1. Block Diagram of the LM3001 Primary Side Driver IC

This results in a stable timing that is scaled to the operating frequency. The IC has an over-voltage shut down input (OV_{TH}) that can be used either to protect the IC from higher than 20V of voltage on the tertiary winding, or to protect the system from higher than specified off-line supply voltage, depending on how the voltage divider on the OV_{TH} pin is connected.

R_{DL} (Pin 2) serves as a programmable duty-cycle limit input. *Figure 2* shows the chip's output waveforms driving a 1 nF capacitor at 1 MHz. The top waveform is the input signal of the pulse transformer driving the P_{IN} pin. The second waveform is the output signal. Five percent of duty-cycle was chosen to show the rise and fall time on the same trace. *Figure 3* shows the same waveforms with a 20 nF capacitive load, at 300 kHz.

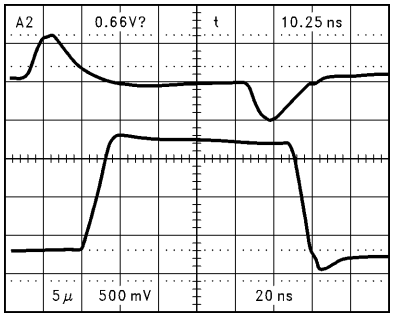

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FIGURE 2. Output Waveform of the LM3001 with 1 nF Load

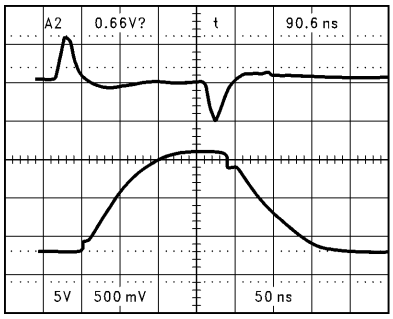

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FIGURE 3. Output Waveform f the LM3001 with 20 nF Load

4.0 LM3101—THE SECONDARY SIDE CONTROLLER IC

The Secondary Side Controller IC is a full PWM controller, plus an integrated power supply monitor, but without an output driver. The block diagram of the IC is shown in *Figure 4.* It has a trimmed, curvature corrected 1%+1% bandgap reference. Its oscillator has an internal timing capacitor, and its oscillator frequency is set by a resistor connected to pin R_{FS}. This same resistor also sets up the bias currents of the speed-critical circuit blocks on the chip, optimizing the speed-power product.

During output short circuit, the chip's operating frequency can be reduced in a gradual programmable way. The frequency shift and the threshold where the frequency shift starts can be programmed by two external resistors, $R_{FS}1$ and $R_{FS}2$, connected to the F_{SC} pin. The simplified internal circuit is shown in *Figure 5.* As long as the $R_{FS}1-R_{FS}2$ divider holds the emitter of Q2 higher than the internal reference voltage, V_{REF}, the oscillator operates at its nominal frequency. If, due to overload, V_{OUT} drops and $V_{OUT}*(R_{FS}1/(R_{FS}1+R_{FS}2)) < V_{REF}$, a current starts to flow through Q2. $1/_{10}$-th of this current is subtracted from the timing capacitor's charge current, decreasing the oscillator frequency. The breakpoint, where the frequency-shift starts is programmed by the ratio of the two resistors, while the value of the shift is set by their absolute value, according to the following formulas:

$$I_{OSC} = \frac{(0.25)(1.242V)}{R_T} \quad \text{(I)}$$

$$F_{OSC}(V_O) = \left(\frac{1}{20\ pF * 1.242V}\right)\left[I_{OSC} - 0.1 * \left(\frac{1.242V}{R_{FS}1} + \frac{1.242V}{R_{FS}2} + \frac{V_O}{R_{FS}1}\right)\right] \quad \text{(II)}$$

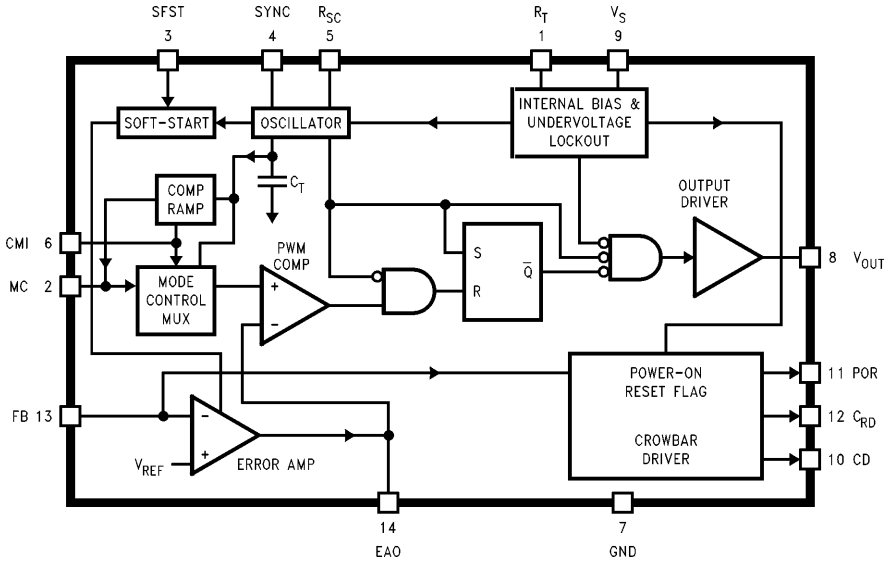

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FIGURE 4. Block Diagram of the LM3101 Secondary Side Controller IC

This short circuit frequency-shift feature, prevents the system from reaching the secondary current limit of the Primary Side Driver chip during a temporary short circuit condition, yielding a straight short circuit current limit. Under a protracted output short circuit, the supply voltage of the secondary side controller gradually disappears and the primary side second level current limit circuit is triggered in a runaway condition. This initiates a time-out, yielding a foldback short circuit characteristic.

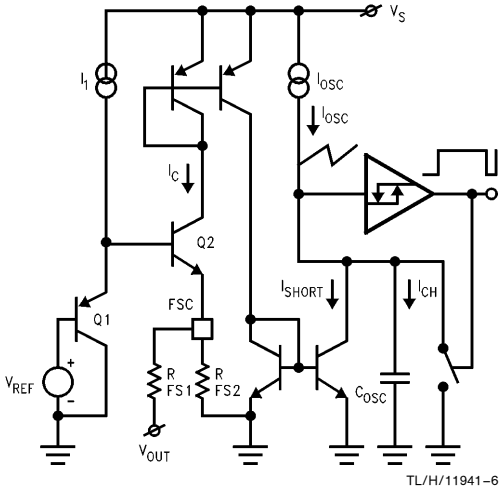

FIGURE 5. Simplified Schematic Diagram of the Frequency Shift Circuitry

4.1 Control Modes

The system's operating mode is controlled by the MCR pin. If this pin is tied to the supply voltage the chip operates in voltage-mode control. On the other hand, both current-mode control and charge-mode control operation is selected by pulling the MCR pin to ground via a resistor. The resistor also sets the slope of the compensating ramp which is needed to stabilize the converter in current-mode above 50% duty-cycle, and in charge-mode below a certain input voltage [2]. *Figure 6* shows the simplified internal circuitry connected to the MCR pin. The mode comparator senses the MCR pin's voltage and sets the mode control multiplexer (see *Figure 5*). In current or charge-mode control R_{CR} sets the slope of a current that flows out of the CMI current sense input pin. The compensating ramp's slope can be scaled by a resistor, R_F, connected between the CMI pin and the terminating resistor (R_S) of the current sense transformer. R_F resistor also serves as a component for the leading edge spike RC filter (R_F–C_F). The slope of the compensating ramp is given by the following equation:

$$\frac{\Delta I_{CMI}}{\Delta t} = \frac{24\ E+3}{R_{FS} * R_{CR}}\ [\mu A/\mu s] \qquad \text{(III)}$$

Under charge-mode control[3] the current sense transformer drives a capacitor that integrates the sensed switch current on a cycle-by-cycle basis. *Figure 7* shows the integrating current sense circuitry and the simplified details of the associated internal circuitry of the LM3101. Q1 discharges the C1 integrating capacitor in every switch cycle during the switch's off-time. Q1 is also active in current-mode, although it was not shown in *Figure 6*. The charge-mode control yields the fastest possible average current control loop. The LM3101 secondary side controller is the first commercially available chip to provide the option of charge-mode control.

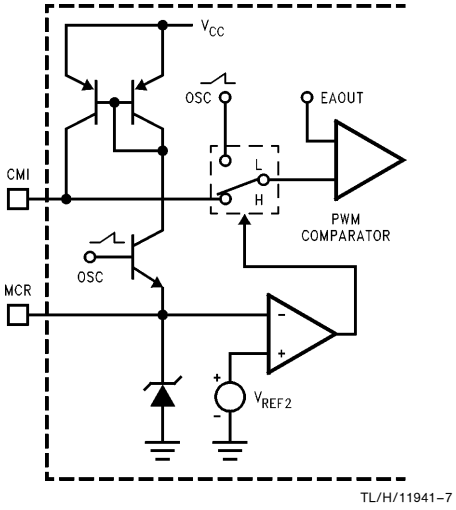

FIGURE 6. Simplified Schematic Diagram of the Mode-Control Circuitry

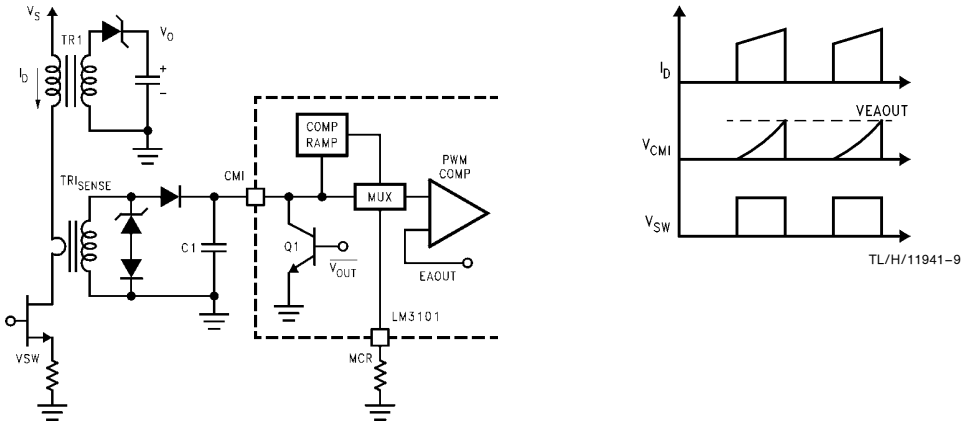

FIGURE 7. Charge-Mode Control with the LM3101

4.2 Power Supply Monitor Functions

The monitor section is shown in the right lower corner of the block diagram *(Figure 4)*. Two monitor functions are provided. The first is power-on reset with programmable delay. The reset pin, POR, is an open collector, pulled up by an external resistor. It is valid down to 1V supply voltage, sinking 1.6 mA of current. The reset delay can be programmed with an external capacitor connected to the C_{RD} pin. The practical delay ranges from 10 μs to 5 ms. The reset threshold is internally fixed at 95% of the nominal output voltage. The second monitor function is a crowbar driver output. If the output voltage gets higher than 120% of the nominal value (due to loss of control), the CBR pin can fire an external SCR that shorts the output of the regulator, saving the ICs connected to it. The CBR pin can supply more than 200 mA of current for the SCR's trigger input.

5.0 A 50W OFF-LINE DC/DC CONVERTER

Figure 8 shows a voltage-mode 50W flyback converter utilizing the chipset. The output voltage is 5V at 10A max., the input voltage range is 80V AC to 132V AC, which corresponds to a 113V to 186V DC range for the converter. The figure does not show the input diode bridge and EMI filter for simplicity, they are included on the actual test circuit. The converter operates at 500 kHz nominal frequency with 78% efficiency. The main transformer, TR1 is Pulse Engineering PE 6823, with 40 μH primary inductance and 1 μH primary leakage inductance. It is surface mountable.

The LM3001 is supplied from the tertiary winding in the traditional way. The nominal voltage of the tertiary output is 12.5V. The 3 μH inductor (L1) averages out the the 200 ns long voltage spike on the tertiary winding after the FET turns off. This spike is caused by the secondary leakage and wiring inductance and the high dI/dT of the secondary winding when the output diode turns on. The spike can be easily 3V at 10A load, even with very careful secondary side board layout. This spike transformed by the 2.5:1 secondary to tertiary turns ratio would raise the LM3001's supply voltage to 20V (the max operating limit) if L1 was not used. Increasing the load to the 12A current limit the tertiary rectified voltage would exceed the chip's max supply voltage rating. Inserting L1, in series with the teriary diode, integrates the spike, yielding a 17.5V maximum rectified tertiary voltage.

The rest of the control circuit on the primary side is standard. The primary-secondary communication is facilitated by the TR2, the pulse communication transformer. It is wound on a 40200TCW 2.5 mm diameter toroid core (ur = 10000), manufactured by Magnetics Inc. Both the primary and the secondary have 2 turns, yielding a 7 μH primary inductance. The secondary winding is wound by triple isolated Rubadue wire to provide 2500V primary to secondary isolation. The primary of TR2 is driven by the secondary side controller via a 100 pF DC blocking capacitor. The LM3101 secondary side controller is supplied from the output voltage through a diode. The diode ensures that the chip's supply voltage does not immediately collapse in a temporary output short circuit condition. R_T sets the operating frequency to 500 kHz. The free running frequency of the primary chip is set to the same nominal value by R_T and C_T.

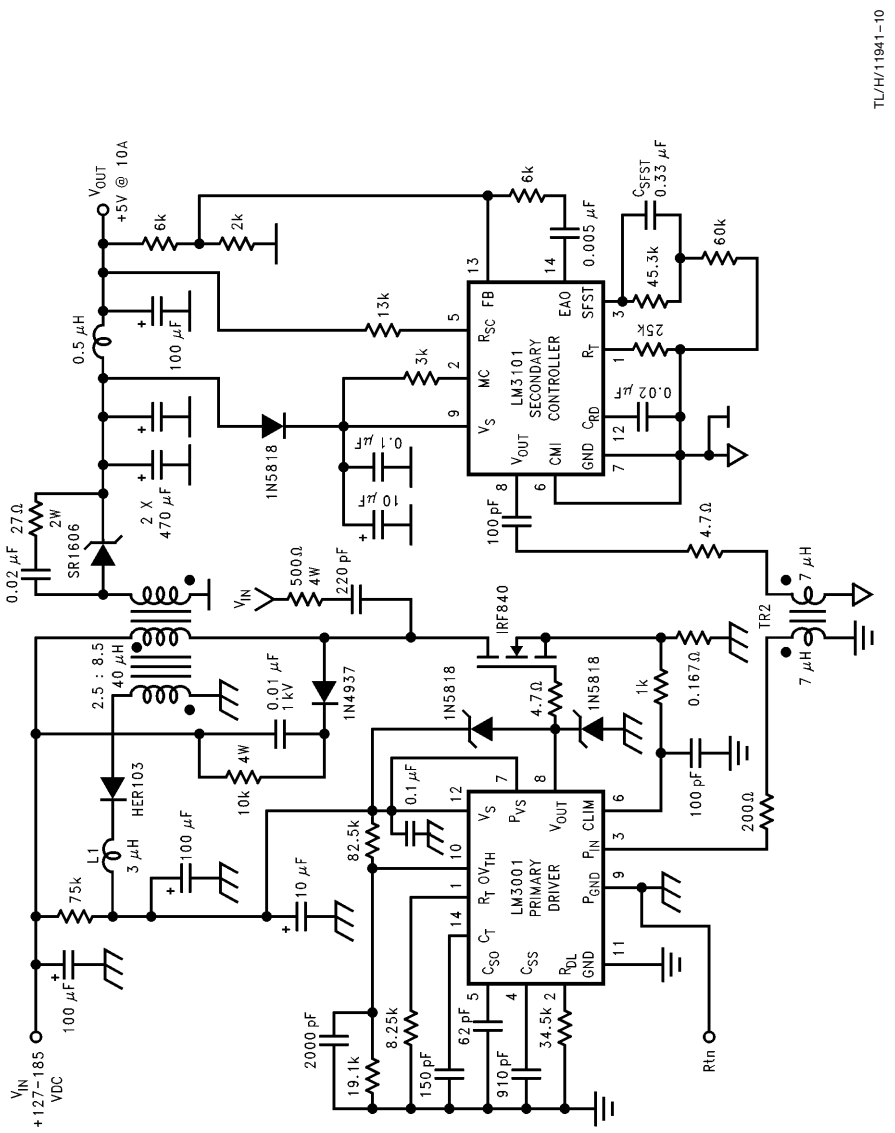

FIGURE 8. Off-Line Voltage Mode Flyback Regulator

Figure 9 illustrates the dynamic range of the converter. It shows the output voltage of the secondary side controller IC and the Drain voltage of the power MOSFET under light load operation, yielding 5% duty-cycle.

At start-up, the secondary soft-start capacitor, C_{SFST}, is not charged, and the SFST pin pulls down the chip's reference voltage to 0.99V, from the nominal 1.242V, with resistor values shown. The reference voltage gradually increases during the startup transient depending on the value of C_S. This feature ensures that the error amplifier of the secondary side controller is in its linear active region before the output voltage reaches its nominal value, yielding a smooth output startup waveform without overshoot. *Figure 10* shows the output voltage at startup with a light 100 mA load current, while *Figure 11* shows the startup transient at a 10A maximum load. In both cases the startup is well behaved and monotonous.

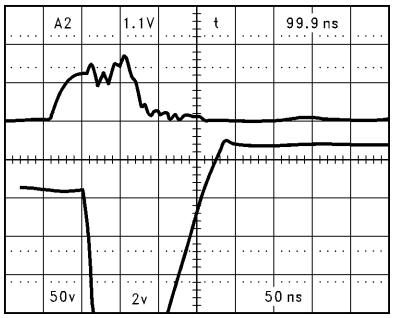

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FIGURE 9. Waveforms of the Off-Line Converter under Light Load

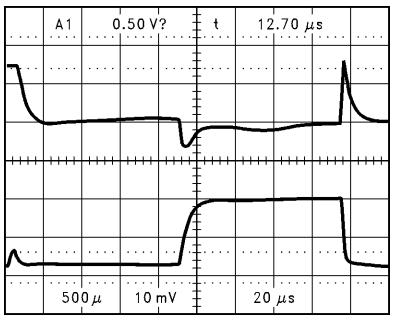

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FIGURE 12. Load Transient Response of the Off-Line Converter

The converter's line-regulation is 0.002%/V, while load-regulation for a 100 mA to 10A load change is 5 mV. The control loop of the converter has a 31 kHz crossover frequency at nominal input voltage and full load. *Figure 12* shows the output load transient response with a load change from 1A to 10A. The maximum excursion is about 400 mV, the settling time to within 2% is below 15 µs. The small output LC filter brings down the output ripple voltage to 50 mV.

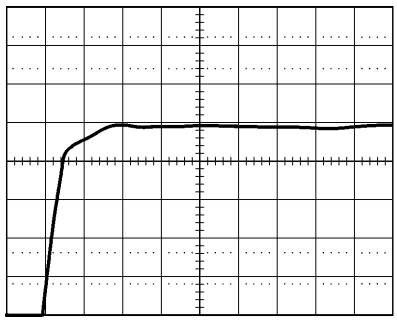

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FIGURE 10. Startup Transient of the Off-Line Converter under Light Load

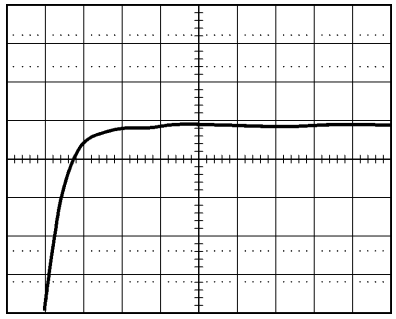

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FIGURE 11. Startup Transient of the Off-Line Converter under Maximum Load

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