Comparison of COP82xCJ to the Enhanced COP8SAx7 Family—Hardware/ Software Considerations

National Semiconductor
Application Note 1044
Abdul Aleaf
July 1996

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INTRODUCTION

The COP820CJ, COP822CJ and COP823CJ are members of the COP8 Basic Family that contain ROM, RAM, a 16-bit multi-function timer with a single 16-bit autoreload/capture register, 3 interrupt sources with polling scheme, WATCHDOG™ Timer, Modulator/Timer, Brown Out detection, Multi-Input Wakeup, and the MICROWIRE/PLUS™ serial interface. These devices are offered in 28-pin SO/DIP, 20-pin SO/DIP, 16-pin SO packages. The operating voltage range is from 2.5V to 6.0V.

The COP8SAA7, COP8SAB7 and COP8SAC7 (COP8SAx7 family) devices, on the other hand, are members of the COP8 Feature Family that contain EPROM, RAM, a 16-bit multi-function timer with two autoreload/capture registers, eight interrupt sources supporting vectored interrupt scheme, and the enhanced MICROWIRE/PLUS serial interface. In addition, these devices contain features such as Multi-Input Wakeup, WATCHDOG/Clock Monitor, Idle timer supporting Idle mode, internal Power-On Reset, on-chip RC oscillator, 8 bytes of user storage space in EPROM, and on-chip EMI reduction circuitry. The devices are offered in 44-pin PLCC, 40-pin DIP, 28-pin SO/DIP, 20-pin SO/DIP, and 16-pin SO/DIP packages. The operating voltage range is from 2.7V to 5.5V. See the datasheet for more details.

The purpose of this Application Note is to provide a detailed comparison and feature analysis of these two family of devices. Where applicable, this report can be used to assist in converting the code written for the COP82xCJ device to operate on an equivalent COP8SAx7 device.

As suggested, the COP8SAx7 family offers additional useful and enhanced features as compared to the COP82xCJ family. With the additional features, the COP8SAx7 family may appear much different, but this family is designed to maintain downward compatibility with the COP82xCJ family as much as possible.

The COP82xCJ family offers some features that are not supported by the COP8SAx7 family. Examples of such features are Brown Out detection, comparator, Modulator, and a second 8-bit timer with 8-bit prescaler (if WATCHDOG function is not used). If these features are already used on the COP82xCJ design, the conversion to the COP8SAx7 family will be more involved and may require additional external components and code changes.

HIGHLIGHTS OF COP8SAx7 ENHANCEMENTS OVER COP82xCJ

1. The operating voltage range is wider (2.7V–5.5V).
2. The R/C oscillator option is expanded to include the choice of selecting on-chip R/C components. The use of on-chip R/C eliminates the cost associated with external R/C oscillator components.
3. The crystal oscillator option is expanded to include the choice of selecting on-chip biasing resistor.
4. COP82xCJ's Port I is replaced with a bi-directional Port F.
5. Stack Pointer is automatically initialized by hardware.
6. The HALT feature is made user selectable.
7. The interrupt handling is enhanced to support a versatile vectored interrupt scheme. It has a total of eight interrupt sources with independent vectors. The COP82xCJ has a polled interrupt scheme.
8. The Software Trap scheme is enhanced to include its own pending flag.
9. The MICROWIRE/PLUS serial interface is enhanced to include shifting on the alternate clock edge and programmable idle polarity for the shift clock. This allows compatibility with SPI peripherals.
10. The 16-bit multi-function timer/counter is improved to include two autoreload/capture registers. The timer block contains two separate interrupt vectors and two I/O pins. The COP82xCJ timer has a single autoreload/capture register, a single interrupt source, and a single I/O pin.
11. Added a free running IDLE timer.
12. Added the power saving IDLE mode.
13. Nine instructions are added to the basic instruction set. The instructions are ANDSZ, IFNE, RLCA, VIS, POP A, PUSH A, RPND, LD B and IFEQ Mem,Imm.
14. The device is offered in 44-pin PLCC, 40-pin DIP, and 16-pin DIP, in addition to 28-pin SO/DIP, 20-pin SO/DIP, and 16-pin SO packages.
15. EMI reduction circuitry is added to achieve low radiated emissions.

RRD-B30M96/Printed in U. S. A.

SUMMARY OF DIFFERENCES BETWEEN COP82xCJ AND COP8SAx7

The following table provides a detailed summary of differences between the COP82xCJ and COP8SAx7.

TABLE I

Features	COP82xCJ Family	COP8SAx7
Operating Voltage	2.5V–6.0V	2.7V–5.5V
Dynamic Supply Current CKI = 10 MHz	6 mA	7 mA
Typical HALT Current	$< 1\ \mu A$ (Brown Out Disabled)	$< 4\ \mu A$
R/C Oscillator	External RC Components.	On-Chip RC or On-Chip RC with External C.
R/C Oscillator Frequency Tolerance	R/C Oscillator tolerance is different than COP8SAx7. For example: for CKI = 1 MHz, R = ±1%, C = ±5%, frequency tolerance is approximately ±25% (see Datasheet for more data points).	R/C Oscillator tolerance is different than COP82xCJ. For example: for CKI = 1 MHz, using on-chip R/C or on-chip RC with external C, frequency tolerance is approximately ±35% (see Datasheet for more data points).
Crystal Oscillator	External crystal circuitry with external bias Resistor.	External crystal circuitry with the option of choosing external or internal bias resistor.
Input Only Port	Port I is an 8-bit input only port.	Port I is replaced with an 8-bit I/O (Port F).
Pin G1	Pin G1 is an I/O pin.	Pin G1 is a dedicated WATCHDOG output pin if WATCHDOG logic enabled. It is a general purpose I/O if WATCHDOG is not enabled.
Pin G2	Pin G2 is a general purpose I/O.	Pin G2 is a general purpose I/O or the timer second input capture.
Stack Pointer	The Stack Pointer must be initialized with software.	The Stack Pointer is initialized by hardware internally on reset.
RAM Map	1. Location 0FF Hex is a general purpose RAM register. 2. Location 0D7 hex is for Port I input pins.	1. Location 0FF Hex is reserved for future RAM expansion. If compatibility with future devices (with more RAM) is not desired, this location can be used as a general purpose RAM location. 2. Location 0D7 Hex is reserved. Port I is replaced by Port F. Port F is read into RAM location 96 Hex instead of location D7 Hex.
Reset	External reset or Brown Out reset. Brown Out reset can be used as a Power-On Reset.	External reset or using on-chip user selectable Power-On Reset. The external RC delay must be greater than 5x Power Supply Rise time or 15 μs, whichever is greater.
HALT Mode	HALT mode is always enabled.	HALT can be enabled or disabled through ECON control bit.
Interrupt Handling	Polled Interrupts	Vectored Interrupts
Interrupt Sources	Software Trap External Interrupt Timer Interrupt	Software Trap External Interrupt Timer Interrupt (2) Multi-Input Wakeup IDLE MICROWIRE/PLUS Default VIS
Software Trap	Software Trap does not set a pending flag.	Software Trap sets a pending flag.

SUMMARY OF DIFFERENCES BETWEEN COP82xCJ AND COP8SAx7 (Continued)

The following table provides a detailed summary of differences between the COP82xCJ and COP8SAx7. (Continued)

TABLE I (Continued)

Features	COP82xCJ Family	COP8SAx7
MICROWIRE/PLUS	1. Does not allow shifting at alternate clock edge. 2. Does not support programmable idle polarity for the shift clock. 3. In Slave mode, the shift clock does not stop after 8 clock pulses.	1. Allows shifting at alternate clock edge. 2. Supports programmable idle polarity for the shift clock for SPI compatibility. 3. In Slave mode, the shift clock stop after 8 clock pulses.
Multifunction 16-Bit Timer	The timer has: 1. One 16-bit counter with a single 16-bit register. 2. One I/O pin. 3. One interrupt source. 4. No underflow interrupt pending flag in the capture mode.	The timer has: 1. One 16-bit counter with two 16-bit registers. 2. One output and two input pins. 3. Two interrupt sources. 4. Underflow interrupt pending flag in the capture mode.
Program Memory Security	COP82xCJ are mask ROMed devices. Program memory contents cannot be read in an EPROM programmer environment.	Contains EPROM security feature.
ECON Register	No ECON register. Clock configuration is selected by a mask option. RAM size is fixed. WATCHDOG is enabled by software. Brown Out detection (can be used as Power-On-Reset) is a mask option. No ROM security feature.	ECON register selects the security, clock, WATCHDOG, Power-On Reset, and HALT options. Bit functions for the clock option and bit polarity for the security option are different. RAM size is selected by device.
Idle Timer/Idle Mode	Does not contain an Idle Timer. Does not support Idle Mode.	Contains an Idle Time. Supports Idle Mode.
WATCHDOG/Clock Monitor	WATCHDOG is enabled by software. WATCHDOG window is programmable through an 8-bit timer preceeded by an 8-bit prescaler. WATCHDOG trigger generates internal reset. No Clock Monitor logic.	WATCHDOG is active upon Power-up. WATCHDOG has a programmable upper window (4 choices) and a fixed lower window. WATCHDOG pin goes active low upon WATCHDOG trigger condition. Contains Clock Monitor logic.
Brown Out Detection	Contains on-chip Brown Out detection circuit.	Does not contain on-chip Brown Out detection circuit.
Comparator	Contains an on-chip comparator.	No on-chip comparator.
Modulator Timer	Contains a Modulator Timer	No Modulator Timer.
WATCHDOG Timer	If WATCHDOG function is not used, the WATCHDOG timer can be used as a general purpose timer for internal time keeping.	The Idle timer provides timing for the WATCHDOG logic. Cannot use Idle timer as a general purpose internal timer.
Instruction Set	COP8 Basic family instruction set.	COP888 Feature family instruction set (9 additional instructions as compared to Basic family). The instructions are ANDSZ, IFNE, RLCA, VIS, POP A, PUSH A, RPND, LD B, and IFEQ Mem,Imm.
Packages	28-pin SO/DIP, 20-pin SO/DIP, 16-pin SO.	44-pin PLCC, 40-pin DIP, 28-pin SO/DIP, 20-pin SO/DIP, 16-pin SO/DIP.
EMI	Does not include EMI reduction circuitry.	Contains EMI reduction circuitry.

COMPATIBILITY—CONVERTING FROM COP82xCJ TO COP8SAx7

The review of differences outlined in Table I, leads to the following steps to be followed in converting from the COP82xCJ to COP8SAx7:

Hardware/ECON Register Considerations

1. R/C Oscillator

Bits 3 and 4 of ECON register must be programmed with 1 and 0 respectively. This will select the on-chip R/C components. External R/C components are not needed unless different operating frequency is required. For a different operating frequency, only a small external capacitor needs to be added from the CKI to the GND pin. See the datasheet for the appropriate capacitor value. There are differences in R/C oscillator tolerances between the COP82xCJ and COP8SAx7. For comparison, see the datasheets for these devices.

2. Crystal Oscillator

Bits 3 and 4 of ECON register must be programmed with 0 and 1 respectively. This will select the crystal oscillator with external biasing resistor. No change to the external crystal oscillator circuitry is required.

3. External Oscillator

Bits 3 and 4 of ECON register must be both programmed with 0.

4. Security Feature

Bit 5 of ECON register (COP8SAx7) must be programmed with 1 to enable the EPROM security feature, otherwise must contain a 0 for the security feature to be disabled. COP82xCJ devices are mask ROMed. Program memory (ROM) cannot be read in an EPROM programmer environment.

5. Reset

Bit 6 of the COP8SAx7 ECON register can be programmed with ''0'' to disable the on-chip Power-On-Reset. By doing this, external reset can be used and the device will perform the same as the COP82xCJ except that RC delay must be greater than 5x Power Supply rise time or 15 μs, whichever is greater.

If Brown Out detection feature is selected on the COP82xCJ (by mask option) as a Power-On-Reset, bit 6 of the COP8SAx7 ECON register must be programmed with ''1'' to enable the on-chip Power-On-Reset.

If Power-On-Reset is selected, the user needs to consider the V_{CC} rise time specification of 10 ns to 50 ms. There is no spec limitation on COP82xCJ Brown Out detection feature.

6. HALT Mode

Bit 0 of ECON register must be programmed with 0 to enable the HALT mode.

7. WATCHDOG

The COP82xCJ has an on-chip 8-bit WATCHDOG timer. The timer contains an 8-bit READ/WRITE down counter clocked by an 8-bit prescaler. The WATCHDOG can be enabled or disabled (only once) after the device is reset as a result of brown out reset or external reset. On power-up the WATCHDOG is disabled. The WATCHDOG is enabled by writing a ''1'' to a bit in WATCHDOG register (WDREG). Once enabled, the user program should write periodically into the 8-bit counter before the counter underflows. An internal reset is generated if the user programs fail to do so.

The COP8SAx7 family, on the other hand, contains a user selectable WATCHDOG and Clock Monitor. The WATCHDOG is enabled by bit 2 of the ECON register. When this bit is 0, the WATCHDOG is enabled and pin G1 becomes the WATCHDOG output pin with a weak pullup. The WATCHDOG logic contains two separate service windows. While the user selectable upper window selects the WATCHDOG service time, (four choices of 8k t_C, 32k t_C, 64k t_C, where t_C = instruction cycle time), the lower window (fixed time of 256 instruction cycles) provides protection against an infinite program loop that contains the WATCHDOG service instruction. The Clock Monitor is used to detect the absence of a clock or a very slow clock below a specified rate on the CKI pin. The WATCHDOG and Clock Monitor are disabled during reset. The devices comes out of reset with the WATCHDOG armed, and the Clock Monitor enabled. Servicing the WATCHDOG consists of writing a specific value to a WATCHDOG Service Register (WDSVR) which is memory mapped in the RAM. The service value is composed of three fields, consisting of a 2-bit Window Select, a 5-bit Key Data field, and the 1-bit Clock Monitor Select field. The WDSVR register can be written to only once after reset to select the proper upper window and the Clock Monitor feature. Upon triggering the WATCHDOG, to the logic will pull the WATCHDOG output pin (G1) low for 16 t_C–32 t_C. The WATCHDOG pin may be connected to the Reset pin externally to reset the device upon WATCHDOG trigger condition.

If the WATCHDOG feature is used on the COP82xCJ, the following steps need to be considered to convert to COP8SAx7.

a. Clear bit 2 of the ECON register to select WATCHDOG feature.

b. Select the proper values for bit 6 and bit 7 of the WDSVR (WATCHDOG Service Register) to obtain the appropriate upper window service time. Select one of the four choices that is as close to the COP82xCJ service time as possible. If there is mismatch between the service times, adjust the code to service the WATCHDOG within the new selected upper window.

c. Locate the instruction that enables the WATCHDOG and is placed in the beginning of the COP82xCJ code. Replace this instruction with a new one to perform a write to the COP8SAx7 WATCHDOG Service Register (WDSVR). This instruction should select the proper upper window, enable or disable Clock Monitor, and write a 5-bit data to match the Key Data.

d. The COP8SAx7 must be serviced at least once before the upper window expires and not more than once within a 256 instruction cycle window (lower window).

e. The WATCHDOG output (pin G1) must be connected externally to the Reset pin.

8. Bit 7 of ECON Register

It is a factory test bit. The polarity is ''Don't Care''.

Software Considerations

1. Stack Pointer

If the Stack Pointer (SP) is initialized to a value different than 2F Hex (64 bytes of RAM selected) or to 6F Hex (128 bytes of RAM selected), in the code written for COP82xCJ, the SP initialization instruction can be kept in the user program as is although the hardware initializes SP to 2F or 6F (depending on RAM size). If the COP82xCJ code is initializing the SP to 2F Hex or 6F (depending on the RAM size), the initializing instruction can be deleted. If no code changed is desired, the initialization instruction can stay as is (although redundant).

2. Port I/Port F Configuration

Since Port I is replaced by Port F on the COP8SAx7, Port F is configured as Hi-Z inputs upon reset. This means Port F data register (RAM location 94 Hex) and Port F configuration register (RAM location 95 Hex) both contain values of 0 upon reset and user code must ensure they stay at 0. In addition, Port F is read into RAM location 96 Hex instead of RAM location D7 Hex. The COP82xCJ code must be modified to reflect this change.

3. RAM Location FF Hex

RAM location FF Hex is a general purpose RAM location on the COP82xCJ, but it is reserved on the COP8SAx7 for future RAM expansion. If compatibility with future devices (with more RAM) is not desired, this location can be used as a general purpose RAM location to maintain compatibility with COP82xCJ.

4. Interrupt Handling

COP82xCJ supports the interrupt polling scheme and it has only three interrupt sources. With the polling scheme, all interrupts cause immediate jump to the single fixed program memory location 0FF Hex. The user program must poll all interrupt pending bits to determine the cause of the interrupt. Once the cause is determined, the user program may jump to an appropriate interrupt handling routine.

The COP8SAx7, with up to eight interrupt sources, supports both polled and vectored interrupt schemes. With the vectored interrupt scheme, a vector table is used. The vector table placed in the program memory, contains the start addresses for each of the user's interrupt routines. This table is used by the device to determine where to jump when a particular interrupt occurs. When an interrupt occurs, the device initially jumps to the single fixed program memory location 0FF Hex. Then user program may call a special instruction (VIS) to cause a jump to the vector table followed by a jump to user specified interrupt service routine. The user may elect not to use the VIS instruction, not place the vector table in the program memory, and simply poll each interrupt pending bit as described for the COP82xCJ.

In order to keep the COP82xCJ interrupt handling code compatible with the COP8SAx7, all additional interrupt sources that are available on the COP8SAx7 must be disabled. These additional sources include interrupts associated with the Idle timer, MICROWIRE/PLUS, and Multi-Input Wakeup. Since the COP8SAx7 multi-function timer block contains two interrupt sources, to maintain compatibility with the COP82xCJ, the second interrupt source (Timer T1B Interrupt Enable) must be disabled. All the Enable bits associated with these additional interrupt sources reside in the ICNTRL register (RAM location E8 Hex) and are cleared upon reset. Therefore, there is no code modification required as long as the user keeps the new additional sources disabled, and not use the additional COP8SAx7 interrupt feature (VIS instruction and vector table).

Software Interrupt

The COP8SAx7 software interrupt has a pending flag. This flag is not memory mapped and is cleared by the special RPND instruction. To keep the COP82xCJ code compatible with that of the COP8SAx7 and vectored interrupt scheme is not used, upon entering the interrupt routine (program memory location 0FF Hex), the user program must execute the RPND instruction. This will reset the software interrupt pending flag. The next step is to check the timer and external interrupt pending bits. If none are set, it gives the indication that a software interrupt has occurred.

5. Timer

The timer block contains a second 16-bit register that can be used as an autoreload or capture register depending on the timer operating mode. The following steps need to be considered to run the code written for the COP82xCJ timer on the COP8SAx7.

PWM Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer PWM output pin. Pin G2 is available as a general purpose I/O.

c. The timer's second reload register (T1RB) must be loaded with the same value as the contents of T1RA. This means an instruction must be inserted into the COP8SAx7 code to initialize T1RB.

External Event Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer external event input pin. Pin G2 is available as a general purpose I/O.

c. The timer's second reload register (T1RB) must be loaded with the same value as the contents of T1RA. This means an instruction must be inserted into the COP8SAx7 code to initialize T1RB.

Capture Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer input capture pin. The alternate function of pin G2 (G2 is available as a general purpose I/O) and the capture register T1RB must be ignored. The user can simply read the capture register T1RA.

6. MICROWIRE/PLUS

The MICROWIRE/PLUS feature on the COP8SAx7, supports shifting serial data with the alternate edge of the shift clock and has the ability to select idle polarity for the shift clock. To ensure compatibility with COP82xCJ, bit 6 of Port G configuration register and bit 5 of Port G data register must both contain 0. Upon reset, these bits are cleared and the user code must ensure they stay at 0. In the slave mode, the shift clock on the COP8SAx7 does not stop after 8 clock pulses. The shift clock on the COP8SAx7, on the other hand, stops after 8 clock pulses. No change is required as a result of this difference.

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AN-1044

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408