National Semiconductor

400025

FACT™ Advanced CMOS Logic

Databook

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FACT
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Introduction

FACT™ (Fairchild Advanced CMOS Technology) is a very high-speed, low power CMOS Logic family utilizing a 1.3 μM Isoplanar silicon gate CMOS process. FACT logic functions can attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic: Ultra low static power and high noise immunity. FACT offers the system designer the added benefit of superior line driving characteristics and excellent ESD and Latch-up immunity.

The FACT family consists of devices in two categories:

1. AC—standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
2. ACT—standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

Product Index and Selection Guide

Lists 54AC/74AC and 54ACT/74ACT circuits currently available, in design or planned. The selection guide groups the circuits by function.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Alpha-Numeric Index

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

National Semiconductor

FACT™ Selection Guide

Gates

Function	Device
NAND	
Quad 2-Input	54AC/74AC00
Quad 2-Input	54ACT/74ACT00
Triple 3-Input	54AC/74AC10
Triple 3-Input	54ACT/74ACT10
Dual 4-Input	54AC/74AC20
AND	
Quad 2-Input	54AC/74AC08
Quad 2-Input	54ACT/74ACT08
Triple 3-Input	54AC/74AC11
OR/NOR/Exclusive-OR	
Quad 2-Input OR	54AC/74AC32
Quad 2-Input OR	54ACT/74ACT32
Quad 2-Input NOR	54AC/74AC02
Quad 2-Input Exclusive-OR	54AC/74AC86
Quad 2-Input Exclusive-OR	54ACT/74ACT86
Inverter	
Hex Inverter	54AC/74AC04
Hex Inverter	54ACT/74ACT04
Hex Schmitt Trigger Inverter	54AC/74AC14
Hex Schmitt Trigger Inverter	54ACT/74ACT14

Registers

Function	Device	Clock Inputs
Quad 2-Port Register	54ACT/74ACT399	1(⌐)
Diagnostic and Pipeline Register	54ACT/74ACT818	2

Parity Generator/Checkers

Function	Device
Parity Generator/Checker	54AC/74AC280
Parity Generator/Checker	54ACT/74ACT280
Video Sync Generator	54ACT/74ACT715

Flip-Flops

Function	Device	TRI-STATE® Outputs	Master Reset
Dual D	54AC/74AC74	No	Yes
Dual D	54ACT/74ACT74	No	Yes
Dual J$\overline{K}$	54AC/74AC109	No	Yes
Dual J$\overline{K}$	54ACT/74ACT109	No	Yes
Dual JK	54AC/74AC112	No	No
Dual JK	54ACT/74ACT112	No	No
Quad D	54AC/74AC175	No	Yes
Quad D	54ACT/74ACT175	No	Yes
Hex D	54AC/74AC174	No	Yes
Hex D	54ACT/74ACT174	No	Yes
Octal D	54AC/74AC273	No	Yes
Octal D	54ACT/74ACT273	No	Yes
Octal D	54AC/74AC374	Yes	No
Octal D	54ACT/74ACT374	Yes	No
Octal D	54AC/74AC377	No	No
Octal D	54ACT/74ACT377	No	No
Octal D	54ACT/74ACT534	Yes	No
Octal D	54ACT/74ACT564	Yes	No
Octal D	54AC/74AC574	Yes	No
Octal D	54ACT/74ACT574	Yes	No
Octal D	54ACT/74ACT825	Yes	Yes
9-Bit D	54ACT/74ACT823	Yes	Yes
10-Bit D	54ACT/74ACT821	Yes	Yes

ALUs

Function	Device	No. of Bits	Arithmetic Functions	Logic Functions
Arithmetic Logic Unit	54ACT/74ACT181	4	16	16
Arithmetic Logic Unit	54ACT/74ACT381	4	3	3

Latches

Function	Device	TRI-STATE Outputs	Broadside Pinout
Octal	54AC/74AC373	Yes	No
Octal	54ACT/74ACT373	Yes	No
Octal D	54ACT/74ACT563	Yes	Yes
Octal D	54AC/74AC573	Yes	Yes
Octal D	54ACT/74ACT573	Yes	Yes
Octal Transparent	54AC/74AC845	Yes	Yes
Octal Transparent	54ACT/74ACT845	Yes	Yes
9-Bit Transparent	54AC/74AC843	Yes	Yes
9-Bit Transparent	54ACT/74ACT843	Yes	Yes
10-Bit Transparent	54AC/74AC841	Yes	Yes
10-Bit Transparent	54ACT/74ACT841	Yes	Yes

Counters

Function	Device	Parallel Entry	Reset	U/D	TRI-STATE Outputs
4-Bit Binary	54AC/74AC161	S	A	No	No
4-Bit Binary	54ACT/74ACT161	S	A	No	No
4-Bit Binary	54AC/74AC163	S	S	No	No
4-Bit Binary	54ACT/74ACT163	S	S	No	No
4-Bit Binary	54AC/74AC169	S	—	Yes	No
4-Bit Binary	54AC/74AC191	A	—	Yes	No
8-Bit Binary	54ACT/74ACT269	S	—	Yes	No
7-Stage Binary Ripple	54AC/74AC4024	—	A	No	No

S = Synchronous
A = Asynchronous

ALU Support

Function	Device	No. of Bits
Carry Lookahead	54ACT/74ACT182	4

Buffers/Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Non-Inverting	Broadside Pinout
Octal	54AC/74AC240	2(L)	I	No
Octal	54ACT/74ACT240	2(L)	I	No
Octal	54AC/74AC241	1(H) & 1(L)	N	No
Octal	54ACT/74ACT241	1(H) & 1(L)	N	No
Octal	54AC/74AC244	2(L)	N	No
Octal	54ACT/74ACT244	2(L)	N	No
Octal	54AC/74AC540	2(L)	I	Yes
Octal	54ACT/74ACT540	2(L)	I	Yes
Octal	54AC/74AC541	1(H) & 1(L)	N	Yes
Octal	54ACT/74ACT541	1(H) & 1(L)	N	Yes
10-Bit	54ACT/74ACT827	2(L)	N	Yes

L = LOW
H = HIGH

FIFOs

Function	Device	Input	Output	TRI-STATE Outputs
64 x 9 FIFO Memory	54AC/74AC2708	Parallel	Parallel	Yes
64 x 9 FIFO Memory	54ACT/74ACT2708	Parallel	Parallel	Yes
512 x 9 FIFO	54ACT/74ACT725	Parallel	Parallel	Yes

Decoders/Demultiplexers

Function	Device	LOW Enable	Active-HIGH Enable	Active-LOW Outputs	Active-Address Inputs
1-of-8	54AC/74AC138	2	1	8	3
1-of-8	54ACT/74ACT138	2	1	8	3
Dual 1-of-4	54AC/74AC139	1 & 1	No	4 & 4	2 & 2
Dual 1-of-4	54ACT/74ACT139	1 & 1	No	4 & 4	2 & 2

Arithmetic Functions

Function	Device	Features
16 x 16 Multiplier	54ACT/74ACT1016	2s Complement & Unsigned Arithmetic
Arithmetic Logic Unit for DSP	54ACT/74ACT705	16-Bit ALU and 8 x 8 Parallel Multiplier/Accumulator
16-Bit Single Port Multiplier	54ACT/74ACT1110	Pipeline Capability

Shift Registers

Function	Device	No. of Bits	Reset	Serial Inputs	TRI-STATE Outputs
Octal Shift/Storage	54AC/74AC299	8	A	2	Yes
Octal Shift/Storage	54ACT/74ACT299	8	A	2	Yes
Octal Shift/Storage	54AC/74AC323	8	S	2	Yes
Octal Shift/Storage	54ACT/74ACT323	8	S	2	Yes
Serial In, Parallel-Out	54AC/74AC164	8	A	2	No
Serial In, Parallel-Out	54ACT/74ACT164	8	A	2	No

A = Asynchronous
S = Synchronous

Multiplexers

Function	Device	Enable Inputs (Level)	True Output	Complement Output
8-Input	54AC/74AC151	1(L)	Yes	Yes
8-Input	54ACT/74ACT151	1(L)	Yes	Yes
8-Input	54AC/74AC251	1(L)	Yes	Yes
8-Input	54ACT/74ACT251	1(L)	Yes	Yes
Dual 4-Input	54AC/74AC153	2(L)	Yes	No
Dual 4-Input	54ACT/74ACT153	2(L)	Yes	No
Dual 4-Input	54AC/74AC253	2(L)	Yes	No
Dual 4-Input	54ACT/74ACT253	2(L)	Yes	No
Quad 2-Input	54AC/74AC157	1(L)	Yes	No
Quad 2-Input	54ACT/74ACT157	1(L)	Yes	No
Quad 2-Input	54AC/74AC158	1(L)	No	Yes
Quad 2-Input	54ACT/74ACT158	1(L)	No	Yes
Quad 2-Input	54AC/74AC257	1(L)	Yes	No
Quad 2-Input	54ACT/74ACT257	1(L)	Yes	No
Quad 2-Input	54AC/74AC258	1(L)	No	Yes
Quad 2-Input	54ACT/74ACT258	1(L)	No	Yes
4 Input w/Shift	54AC/74AC350	1(L)	Yes	No
4 Input w/Shift	54ACT/74ACT350	1(L)	Yes	No

Comparators

Function	Device	Features
Octal Identity Comparator	54AC/74AC520	Expandable
Octal Identity Comparator	54ACT/74ACT520	Expandable
Octal Identity Comparator	54AC/74AC521	Expandable
Octal Identity Comparator	54ACT/74ACT521	Expandable
4-Bit Magnitude Comparator	54AC/74AC85	
4-Bit Magnitude Comparator	54ACT/74ACT85	

Adders

Function	Device	No. of Bits	Carry Lookahead
Binary Full Adder	54AC/74AC283	4	Yes
Binary Full Adder	54ACT/74ACT283	4	Yes

Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs (Level)	TRI-STATE Output
Octal Bidirectional Transceiver	54AC/74AC245	No	1(L)	Yes
Octal Bidirectional Transceiver	54ACT/74ACT245	No	1(L)	Yes
Octal Bus Transceiver & Register	54AC/74AC646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54ACT/74ACT646	Yes	I(L) & I(H)	Yes
Octal Bus Transceiver & Register	54AC/74AC648	Yes	1(L) & 1(H)	Yes
Octal Register Transceiver	54ACT/74ACT543	Yes	2(L)	Yes
Octal Register Transceiver	54ACT/74ACT544	Yes	2(L)	Yes
Octal Bus Transceiver	54ACT/74ACT657		1(L) & 1(H)	

Section 1

Descriptions and Family Characteristics

Section 1 Contents

National Semiconductor

FACT™ Descriptions and Family Characteristics

National Semiconductor Advanced CMOS Technology—FACT™—Logic

Fairchild Semiconductor introduced FACT (Fairchild Advanced CMOS Technology) logic, a family of high speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 54ACTXXX/74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - — Common Output Structure for Standard and Buffer Drivers
  - — Output Sink/Source Current of 24 mA
  - — Transmission Line Driving 50Ω (Commercial)/75Ω (Military) Guaranteed
- Operation from 2V–6V Guaranteed
- Temperature Range
  - — Commercial −40°C to +85°C
  - — Military −55°C to +125°C
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range (V_{CC} = 2 V_{DC} to 6 V_{DC}) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC— This is a high speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.

'ACT— This is a high speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5V ±0.5V with V_{OH} = 2.4V and V_{OL} = 0.4V, but are functional over the entire FACT operating voltage range of 2.0 V_{DC} to 5.5 V_{DC}. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	= 0.1 mW/Gate
ALS	= 1.2 mW/Gate
LS	= 2.0 mW/Gate
HC	= 0.1 mW/Gate

Low Power CMOS Operation (Continued)

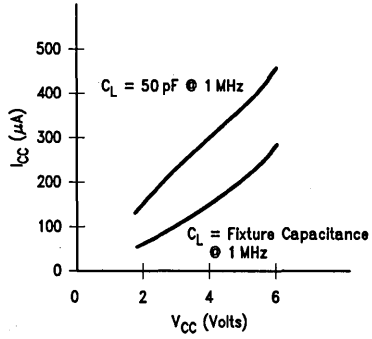

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FIGURE 1-1. I_{CC} vs V_{CC}

Figure 1-1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT	= 6.0 ns @ C_L = 50 pF
ALS	= 12.0 ns @ C_L = 50 pF
LS	= 22.0 ns @ C_L = 15 pF
HC	= 17.5 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5.0V ±0.5V and 3.3V ±0.3V. For worst case design at 2.0V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V V_{CC} = 1.9 × AC specification at 3.3V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0V ±10% V_{CC}.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at 4.5V V_{CC}.

FACT	= 1.25V/1.25V
ALS	= 0.4V/0.7V
LS	= 0.3V/0.7V @ 4.75V V_{CC}
HC	= 0.8V/1.25V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC and 'ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SSI and MSI devices ('AC or 'ACT) are guaranteed to source and sink 24 mA. Commercial devices, 74AC/ACTXXX, are capable of driving 50Ω transmission lines, while military grade devices, 54AC/ACTXXX, can drive 75Ω transmission lines.

I_{OL}/I_{OH} Characteristics

FACT	= 24 mA/−24 mA
ALS	= 24 mA/−15 mA
LS	= 8 mA/−0.4 mA @ 4.75V V_{CC}
HC	= 4 mA/−4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, FACT has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50Ω for the commercial temperature range and 75Ω for the military temperature range.

Figure 1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{OUT} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{OUT} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Dynamic Output Drive (Continued)

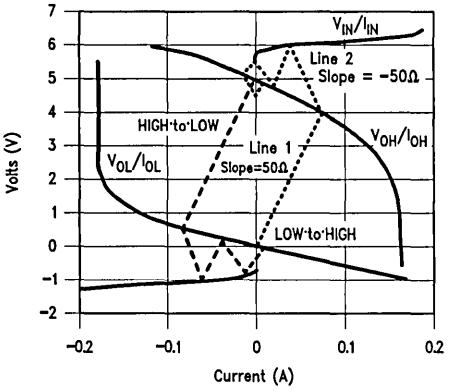

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FIGURE 1-2. Gate Driving 50Ω Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95V. Then draw a line with a slope of −50Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 1-3a and *1-3b* show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

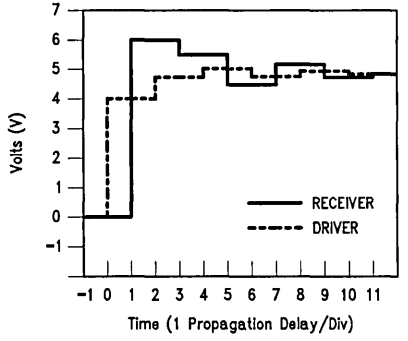

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FIGURE 1-3a. Resultant Waveforms Driving 50Ω Line—Theoretical

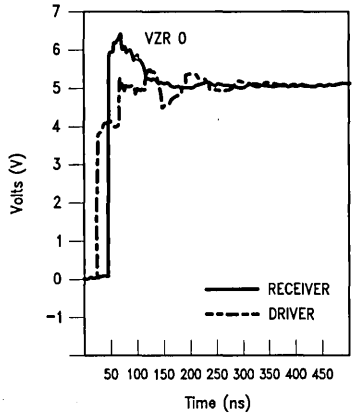

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FIGURE 1-3a. Resultant Waveforms Driving 50Ω Line—Actual

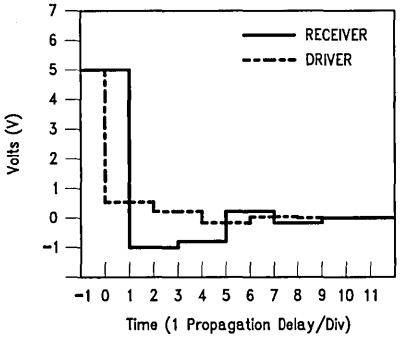

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FIGURE 1-3b. Resultant Waveforms Driving 50Ω Line—Theoretical

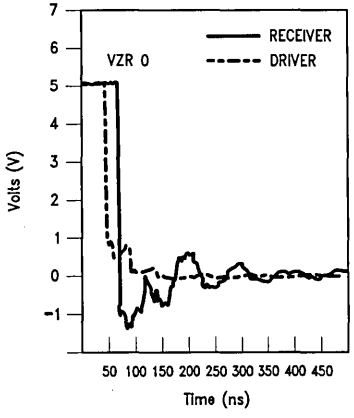

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FIGURE 1-3b. Resultant Waveforms Driving 50Ω Line—Actual

Dynamic Output Drive (Continued)

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC}. The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_O|$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85V, V_{CC} = 5.5V and Z_O = 50Ω, the required I_{OH} at 3.85V is 75 mA. For the HIGH-to-LOW transition, V_{OQ} = 5.4V, V_{IL} = 1.35V and Z_O = 50Ω, I_{OL} is 75 mA at 1.65V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50Ω, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

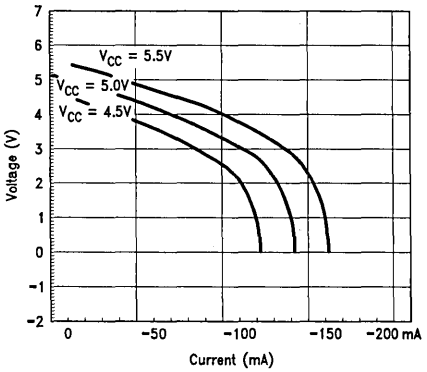

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FIGURE 1-4. Output Characteristics V_{OH}/I_{OH}, 'AC00

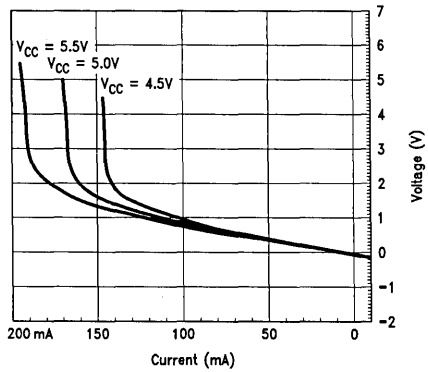

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FIGURE 1-5. Output Characteristics V_{OL}/I_{OL}, 'AC00

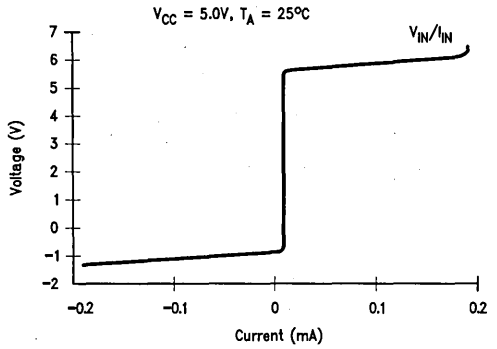

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FIGURE 1-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3V ±0.3V. To this end, National Semiconductor guarantees all of its devices operational at 3.3V ±0.3V. Note also that AC and DC specifications are guaranteed between 3.0V and 5.5V. Operation of FACT logic is also guaranteed from 2.0V to 6.0V on V_{CC}.

Operating Voltage Ranges

FACT	= 2.0V to 6.0V
ALS	= 5.0V ±10%
LS	= 5.0V ±5%
HC	= 2.0V to 6.0V

FACT Replaces Existing Logic

National Semiconductor's Advanced CMOS family is specifically designed to outperform existing CMOS and Bipolar logic families. *Figure 1-7* shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

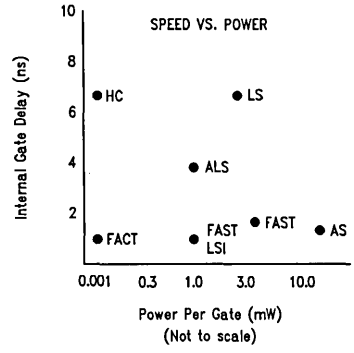

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FIGURE 1-7. Internal Gate Delays

General Characteristics (All Max Ratings)

Symbol	Characteristics	LS	ALS	HCMOS	FACT		Units
					'AC	'ACT	
$V_{CC/EE/DD}$	Operating Voltage Range	5±5%	5±10%	2.0 to 6.0	2.0 to 6.0	2.0 to 6.0	V
T_A 74 Series T_A 54 Series	Operating Temperature Range	0 to +70 −55 to +125	0 to +70 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	°C
V_{IH} (Min)	Input Voltage (Limits)	2.0	2.0	3.15	3.85	2.0	V
V_{IL} (Max)		0.8	0.8	0.9	1.65	0.8	V
V_{OH} (Min)	Output Voltage (Limits)	2.7	2.7	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
V_{OL} (Max)		0.5	0.5	0.1	0.1	0.1	V
I_{IH}	Input Current	20	20	+1.0	+1.0	+1.0	μA
I_{IL}		−400	−200	−1.0	−1.0	−1.0	μA
I_{OH}	Output Current at V_O (Limit)	−0.4	−0.4	−4.0 @ V_{CC} − 0.8	−24 @ V_{CC} − 0.8	−24 @ V_{CC} − 0.8	mA
I_{OL}		8.0	8.0	4.0 @ 0.4V	24 @ 0.44V	24 @ 0.44V	mA
DCM	DC Noise Margin LOW/HIGH	0.3/0.7	0.4/0.7	0.8/1.25	1.55/1.55	0.7/2.4	V

Note: All DC parameters are specified over the commercial temperature range.

Speed/Power Characteristics (All Typical Ratings)

Symbol	Characteristics	LS	ALS	HCMOS	FACT	Units
I_G	Quiescent Supply Current/Gate	0.4	0.2	0.0005	0.0005	mA
P_G	Power/Gate (Quiescent)	2.0	1.2	0.0025	0.0025	mW
t_P	Propagation Delay	7.0	5.0	8.0	5.0	ns
	Speed Power Product	14	6.0	0.02	0.01	pJ
f_{max}	Clock Frequency D/FF	33	50	50	160	MHz

FIGURE 1-8. Logic Family Comparisons

Propagation Delay (Commercial Temperature Range)

Symbol	Product		LS	ALS	HCMOS	FACT	Units
t_{PLH}/t_{PHL}	74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	—	11.0	23.0	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	30.0	12.0	12.0	8.0	ns
		Max	—	18.0	44.0	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	27.0	10.0	20.0	5.0	ns
		Max	—	20.0	52.0	10.0	ns

Conditions: (LS) V_{CC} = 5.0V, C_L = 15 pF, 25°C;
(ALS/HC/FACT) V_{CC} = 5.0V ±10%, C_L = 50 pF, Over Temp, Max values at 0°C to +70°C for ALS, −40°C to +85°C for HC/FACT.

FIGURE 1-8. Logic Family Comparisons (Continued)

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of FACT device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a FACT device will dissipate power in the quiescent or static condition. This can be calculated by using the formula:

Eq. 1 $PD_Q = I_{CC} \bullet V_{CC}$

PD_Q = Quiescent Power Dissipation
I_{CC} = Quiescent Power Supply Current Drain
V_{CC} = Power Supply Voltage

Secondly, a FACT device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using the formula:

Eq. 2 $PD_{INT} (C_{PD} \bullet V_S \bullet f) \bullet V_{CC}$

PD_{INT} = Internal Dynamic Power Dissipation
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation
V_{CC} = Power Supply Voltage

C_{PD} values are specified for each FACT device and are measured per JEDEC standards as described later on in Section 2. On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. See Section 2. For FACT devices, V_S and V_{CC} are the same value and can be replaced by V_{CC}^2 in the above formula.

Thirdly, a FACT device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 $PD_{OUT} = (C_L \bullet V_S \bullet f) \bullet V_{CC}$

PD_{OUT} = Output Power Dissipation
C_L = Load Capacitance
V_S = Output Voltage Swing
f = Output Operating Frequency
V_{CC} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{CC} and can be replaced by V_{CC}^2. In the case of internal and output frequencies being identical Eq. 2 and Eq. 3 may be combined as follows:

Eq. 4 $PD = (C_L + C_{PD}) \bullet V_{CC}^2 \bullet f$

The total FACT device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 5 $PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$ or
$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

Circuit Characteristics (Continued)

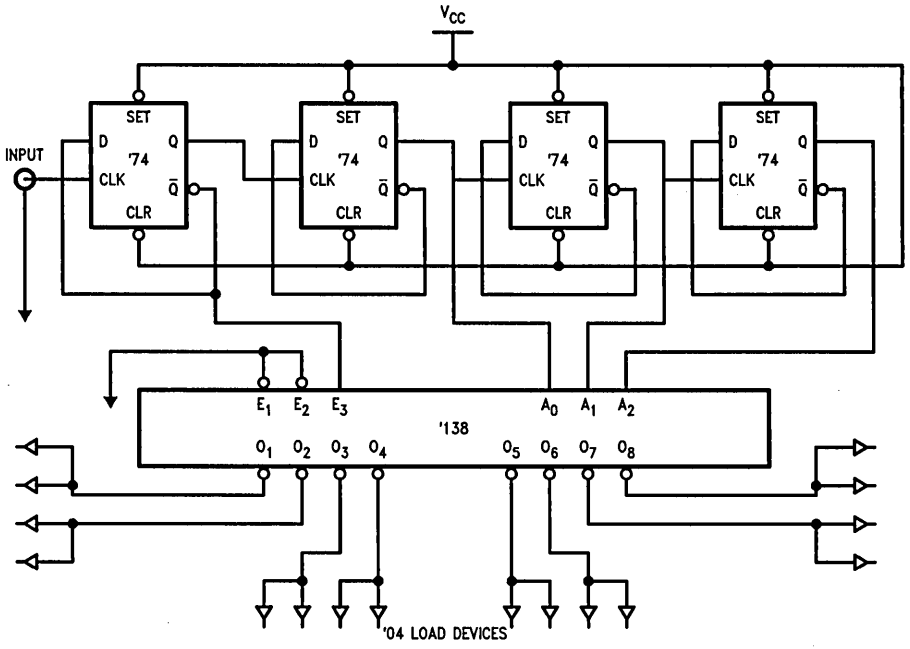

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FIGURE 1-9. Power Demonstration Circuit Schematic

The circuit shown in *Figure 1-9* was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. *Figure 1-10* illustrates the results of these measurements.

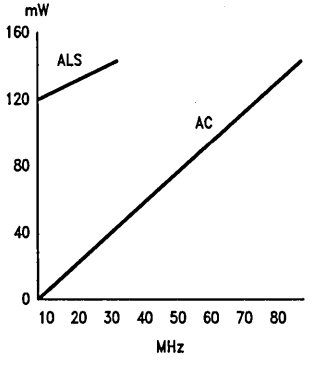

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FIGURE 1-10. FACT vs ALS Circuit Power

Circuit Characteristics (Continued)

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities well above 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

SPECIFICATION DERIVATION

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 1-11a through *1-11e* illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'AC245.

Figure 1-11a shows the data taken (from one part) on a typical, single path, t_{PHL} from A_n to B_n, over temperature at 5.0V; there is negligible variation in the value of t_{PHL}. The next graph, *Figure 1-11b*, depicts data taken on the same device; this set of curves represents the data on all paths A to B and B to A. The data on this plot indicates only a small variation for t_{PHL}.

The graphs in *Figures 1-11a* and *1-11b* include data at 5.0V; *Figure 1-11c* shows the variation of delay times over the standard 5.0V ±0.5V voltage range. Note there is only a ±6% variation in delay time due to voltage effects.

Now refer to *Figure 1-11d* which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ±3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

With voltage and process effects added *(Figure 1-11e)*, the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

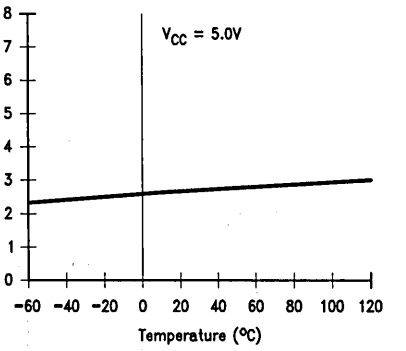

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FIGURE 1-11a. t_{PHL}, A_n to B_n, Single Path

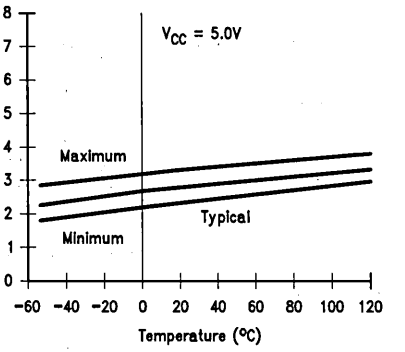

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FIGURE 1-11b. t_{PHL} A to B, All Paths

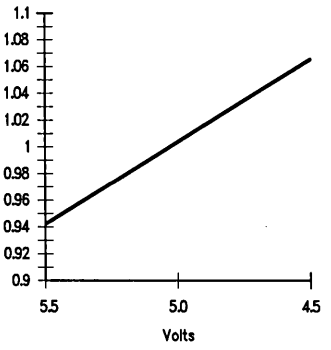

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FIGURE 1-11c. Voltage Effects on Delay Times

Circuit Characteristics (Continued)

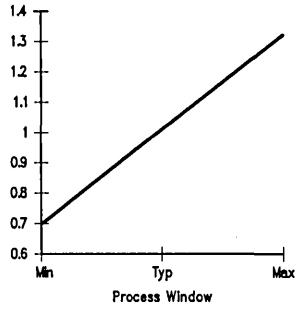

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FIGURE 1-11d. FACT Process Effects on Delay Times

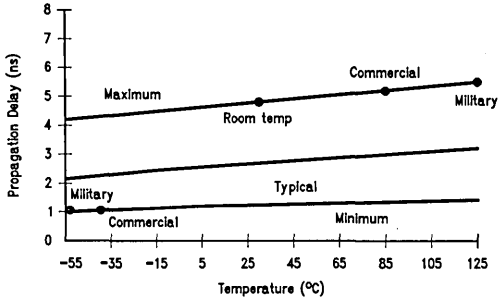

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FIGURE 1-11e. t_{PHL}, A to B, with Voltage and Process Variation

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3.0 ns while the hold time is 0 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0V, the setup time is 1.5 ns while the hold time is −1.5 ns. They are the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

CAPACITIVE LOADING EFFECTS

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

Parameter	Voltage (V)			Units
	3.0	4.5	5.5	
t_{PLH}	31	22	19	ps/pF
t_{PHL}	18	13	12.5	ps/pF

T_A = 25°C

The two graphs following, *Figures 1-12* and *1-13*, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). *Figures 1-14* and *1-15* show the effects of lumped load capacitance on rise and fall times for FACT devices.

Circuit Characteristics (Continued)

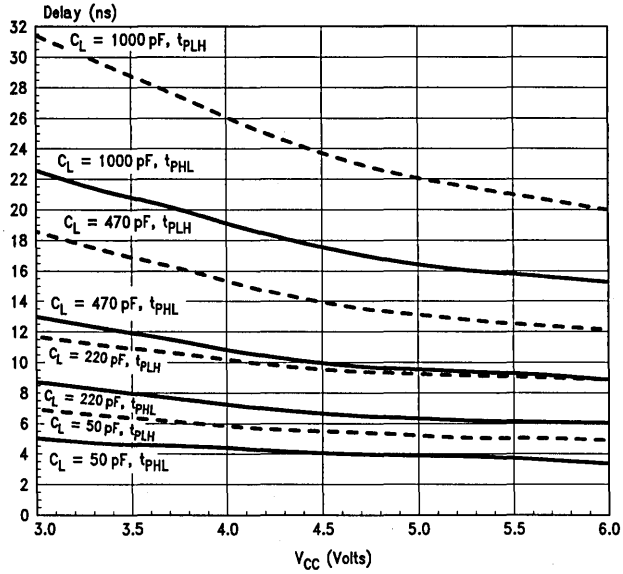

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FIGURE 1-12. Propagation Delay vs V_{CC} ('AC00)

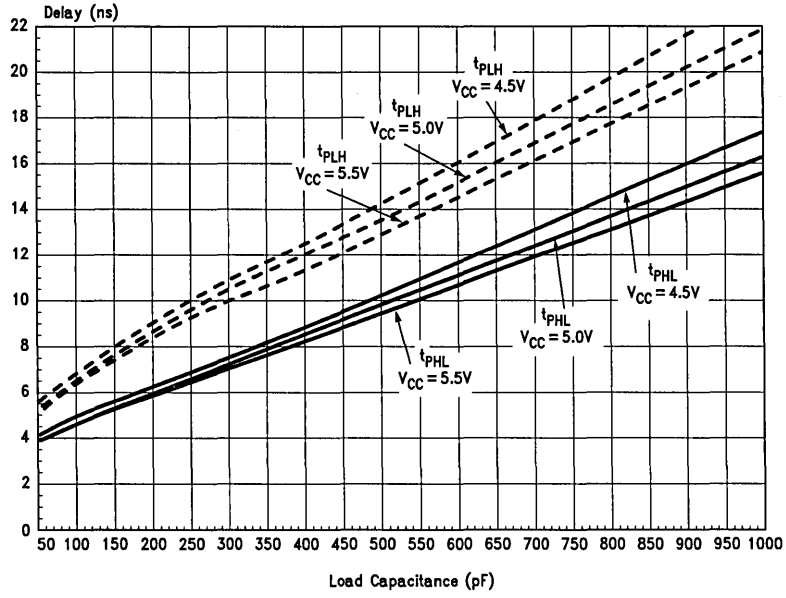

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FIGURE 1-13. Propagation Delay vs C_L ('AC00)

Circuit Characteristics (Continued)

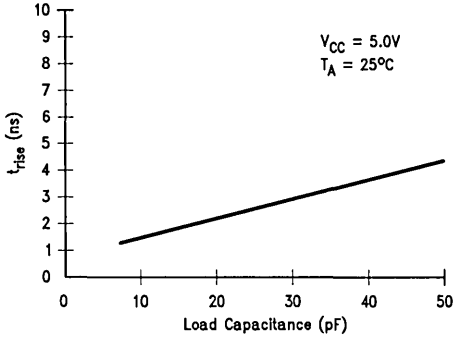

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FIGURE 1-14. t_{rise} vs Capacitance

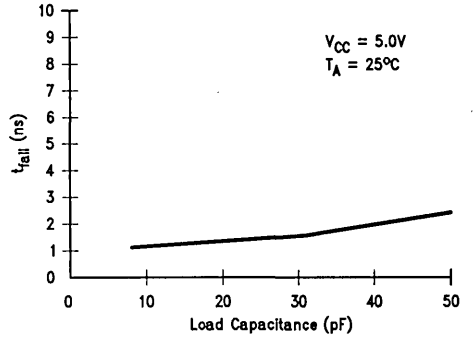

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FIGURE 1-15. t_{fall} vs Capacitance

LATCH-UP

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{CC} = 5.5 V_{DC}). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

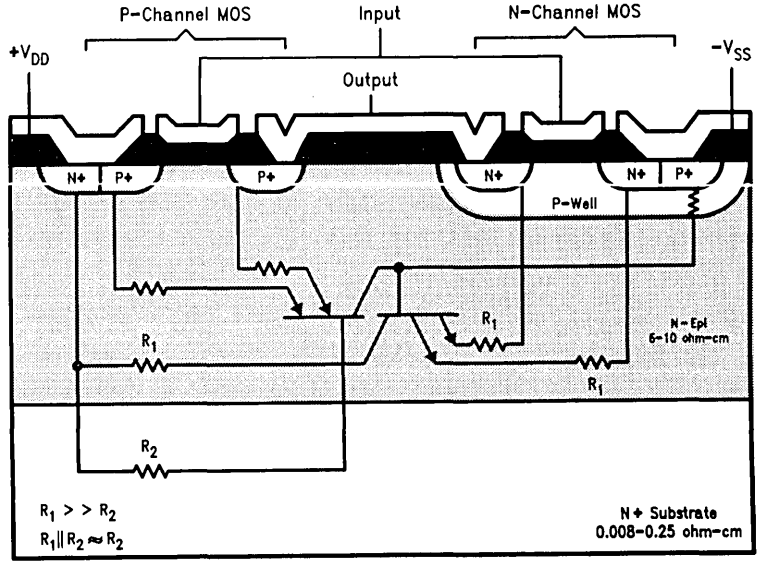

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FIGURE 1-16. FACT EPI Process Cross Section with Latch-up Circuit Model

Circuit Characteristics (Continued)

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883C, test method 3015, and withstand 4000V typically. FACT logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 1-17 shows the ESD test circuit used in the sensitivity analysis for this specification. *Figure 1-18* is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows; five pulses, each of 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

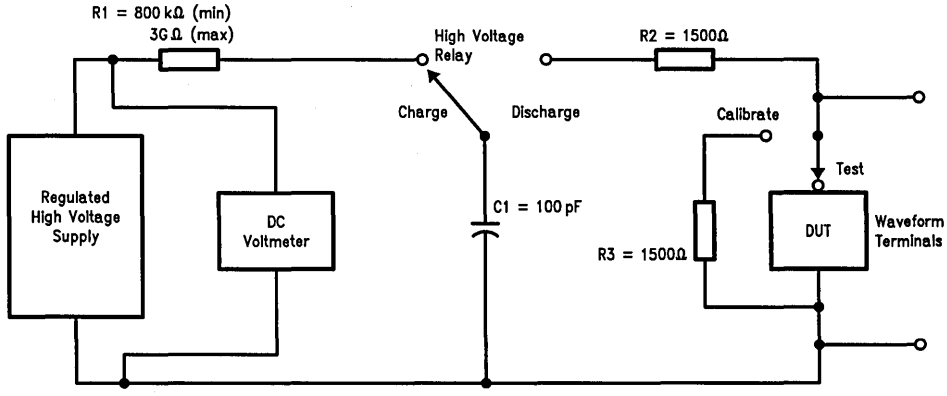

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FIGURE 1-17. ESD Test Circuit

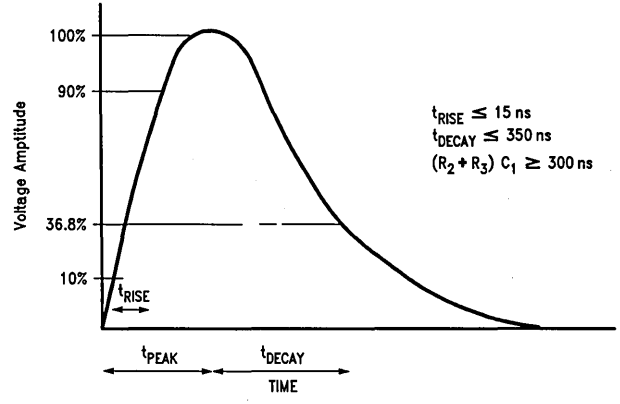

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FIGURE 1-18. ESD Pulse Waveform

Circuit Characteristics (Continued)

RADIATION TOLERANCE

Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. National is meeting this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future rad-hard needs. Such applications include:

- Space
  - — Satellites
  - — Space Stations
- Airborne and Military
  - — Fighters/Bombers
  - — Missile Systems
  - — Ground Based Systems
  - — Navigation & Communications
- Commercial
  - — Power Stations
  - — Medical
  - — Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which they are incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

RADIATION TEST LIMITS

Listed below are National proposed procedures to test and guarantee FACT devices for radiation exposure limits:

- Total Dose
  - — Method 1019 per MIL-STD-883
  - — Individual limits per FACT radiation tolerant data sheet specification
  - — No functional failures
  - — Gamma rays
- Transient Dose/Latchup
  - — Methods 1020, 1021 per MIL-STD-883
  - — Minimum transient upset threshold specification
  - — Minimum latchup threshold specification
  - — Device burnout specification
  - — Gamma rays/Flash X-ray
- Neutron
  - — Test not required for CMOS product
- Single Event Upset
  - — To be announced in the future

SUMMARY OF TESTING

To demonstrate and verify FACT's radiation tolerance, we have characterized several standard FACT device types in a "total dose" irradiation test environment. Standard manufacturing techniques were used in the production of all circuits. Devices of the same type were manufactured from the same wafer.

Test results offer an indication of how various radiation environments affect specific standard FACT product. In most instances the standard FACT devices that were exposed to varying levels of total dose radiation showed reduced power consumption over functionally similar FAST and Schottky device types in non-radiation environments. *Figure 1-19* shows a FACT device's 54AC245 power consumption at various dose levels.

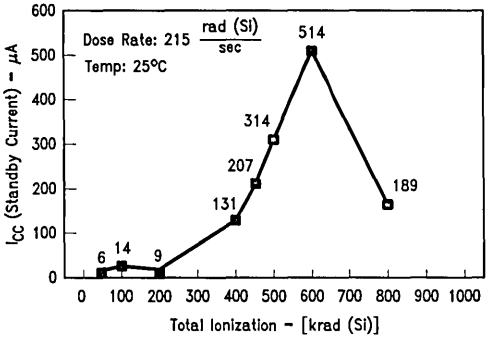

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FIGURE 1-19. Total Dose Response (54AC245)

Total dose irradiation is presently performed "in-house" using a AECL Gamma Cell 220, Cobalt-60, source (National Bureau of Standards certified). Step-stress radiation testing is performed on each part-type. After each total dose level, a complete parametric test (DC and AC) is done and the parametric values evaluated. Because of circuit design and layout differences, each part type has its own unique radiation response.

FACT IS RADIATION TOLERANT

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

We are conducting additional testing and are evaluating further design enhancements for increased radiation tolerance levels of our FACT devices. Our current goal is a radiation tolerant FACT product line which exceeds the U.S. Government's VHSIC Phase II radiation requirements. At that time, National radiation tested products are guaranteed at various total dose tolerance levels ranging between 50 krads(Si) and 1 Mrad(Si).

Section 2

Ratings, Specifications and Waveforms

Section 2 Contents

National Semiconductor

Ratings, Specifications and Waveforms

Specifying FACT™ Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. National Semiconductor realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, National Semiconductor devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than three years of experience manufacturing FACT logic, National Semiconductor can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

During the C_{PD} measurements, each output that is being switched should be loaded with the standard 50 pF and 500Ω load. All device measurements are made with V_{CC} = 5.0V at 25°C, with TRI-STATE® outputs enabled.

Gates/Buffers/ Line Drivers:	Switch one input. Bias the remaining inputs such that one output switches.
Latches:	Switch the Enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock pin with other inputs biased such that the device counts.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generator:	Switch one input.
Priority Encoders:	Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

AC Loading and Waveforms (Continued)

The use of this load, which is equivalent to the FAST™ (Fairchild Advanced Schottky TTL) test jig, differs somewhat from previous (HCMOS) practice. This provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in avarage applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500Ω resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500Ω resistor to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See *Figure 1*.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the 2 × V_{CC} supply voltage establish a quiescent HIGH level.

Test Conditions

Figures 2a and *2b* describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0V for a logic LOW to 3.0V for a logic HIGH for 'ACT devices and 0V to V_{CC} for 'AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5.0V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL}, then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave-

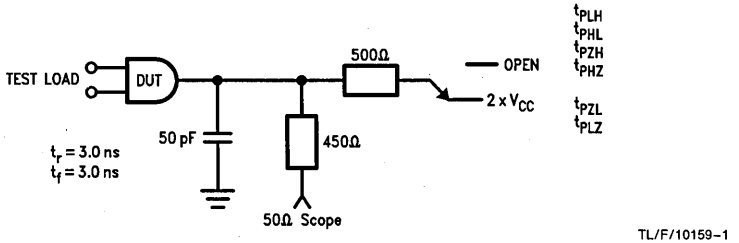

FIGURE 1. AC Loading Circuit

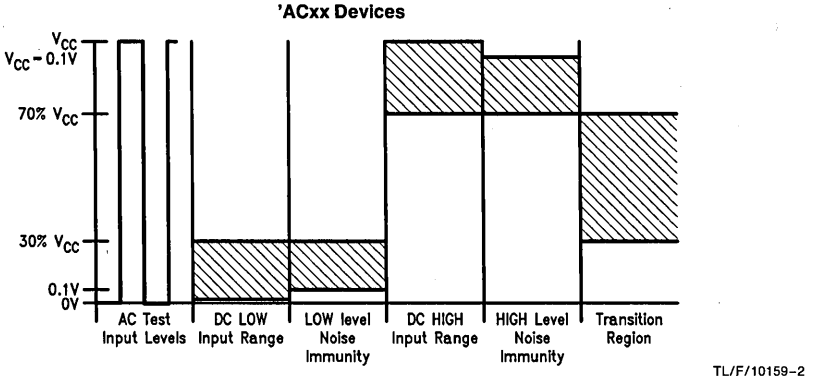

FIGURE 2a. Test Input Signal Levels

Test Conditions (Continued)

'ACTxx Devices

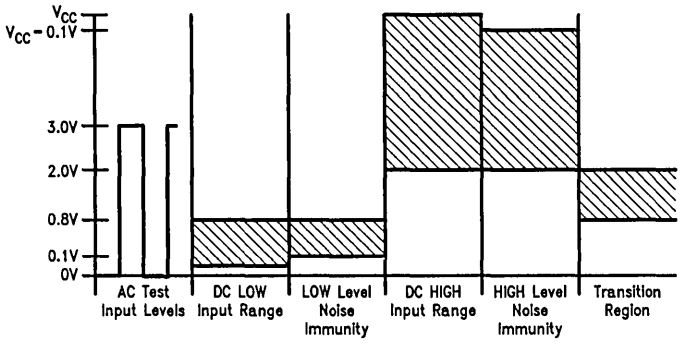

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FIGURE 2b. Test Input Signal Levels

form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0V to 3.0V V_{CC} for 'ACT devices or 0V to V_{CC} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

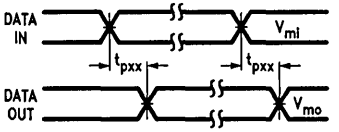

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FIGURE 3. Waveform for Inverting and Non-Inverting Functions

*V_{mi} = 50% V_{CC} for 'AC devices; 1.5V for 'ACT devices
V_{mo} = 50% V_{CC} for 'AC/'ACT devices

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it recrosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5V swing on the output.

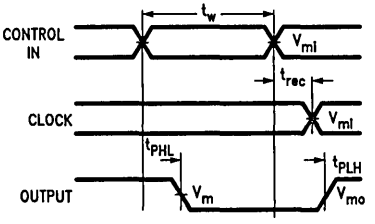

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FIGURE 4. Propagation Delay, Pulse Width and t_{rec} Waveforms

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Enable and Disable Times

Figures 5 and *6* show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from V_{OL} or V_{OH}, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the previous 10% and 90% points. This better reflects actual test points and does not change specification limits.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

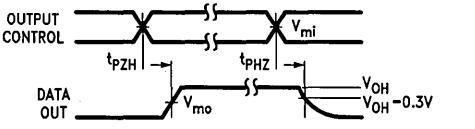

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FIGURE 5. TRI-STATE Output High Enable and Disable Times

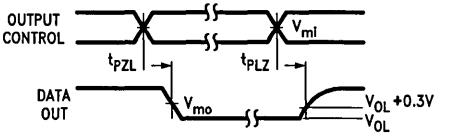

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FIGURE 6. TRI-STATE Output Low Enable and Disable Times

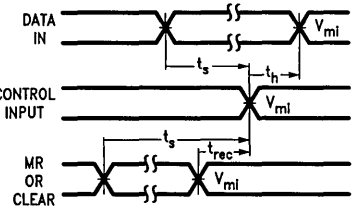

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FIGURE 7. Setup Time, Hold Time and Recovery Time

*V_{mi} = 50% V_{CC} for 'AC devices; 1.5V for 'ACT devices
V_{mo} = 50% V_{CC} for 'AC/'ACT devices

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.

FACT Noise Characteristics (Continued)

5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

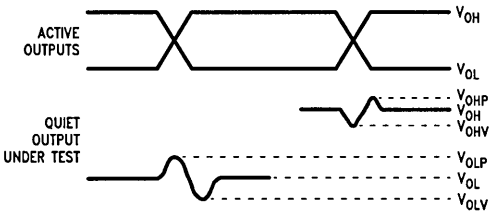

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FIGURE 8. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

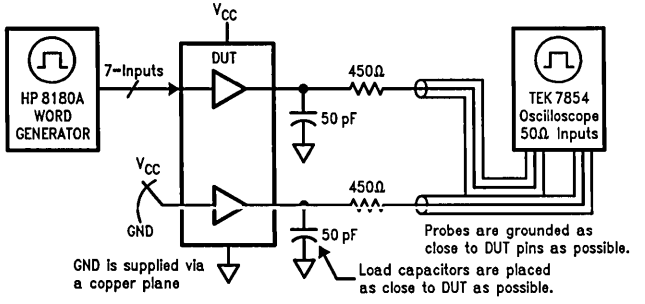

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FIGURE 9. Simultaneous Switching Test Circuit

Section 3

Design Considerations

Section 3 Contents

National Semiconductor

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. National Semiconductor's CMOS helps designers achieve these goals.

FACT™ (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50Ω transmission line drive capability (comparable to National Semiconductor's FAST bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling—Maximize ground and V_{CC} traces to keep V_{CC}/ground impedance as low as possible; full ground/V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Electromagnetic Interference

Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive FAST®, ALS, AS, LS, HC and HCT devices.

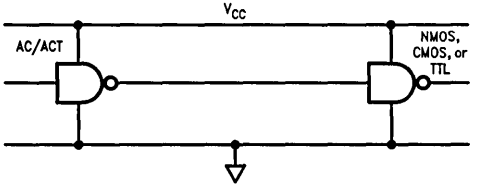

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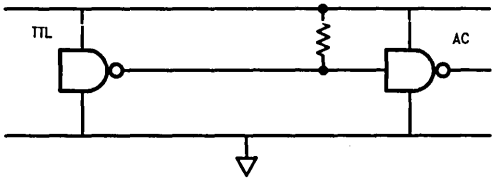
FIGURE 3-1. Interfacing FACT to NMOS, CMOS and TTL

FACT devices can be directly driven by both NMOS and CMOS families, as shown in *Figure 3-1*, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

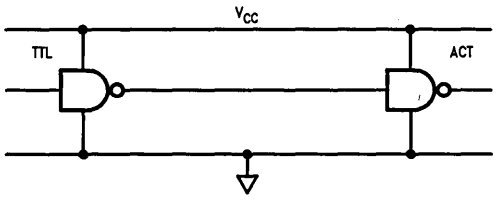
Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{CC} of approximately 4.7 kΩ, which is depicted in *Figure 3-2*. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.



TL/F/10160–2

FIGURE 3-2. V_{IH} Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, National Semiconductor has designed devices which offer thresholds that are TTL-compatible *(Figure 3-3)*. These interfaces tend to be slightly slower than their CMOS-level counterparts due to an extra buffer stage required for level conversion.

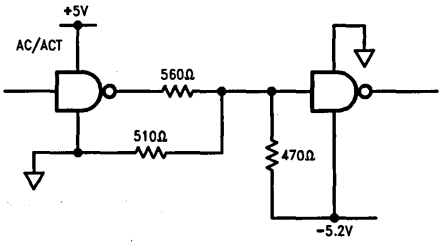


TL/F/10160–3

FIGURE 3-3. TTL Interfacing to 'ACT

Interfacing (Continued)

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{CC} of approximately 4.7 kΩ). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in *Figure 3-4a*. *Figures 3-4b* and *3-4c* show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.



TL/F/10160–4

FIGURE 3-4a. Resistive FACT-to-ECL Translation

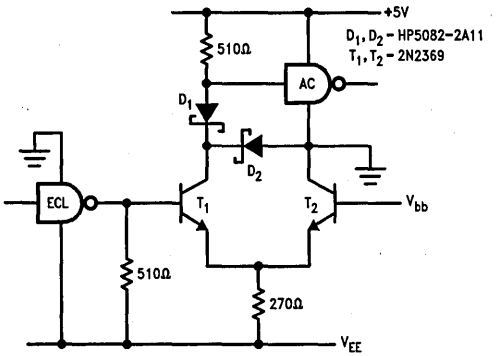


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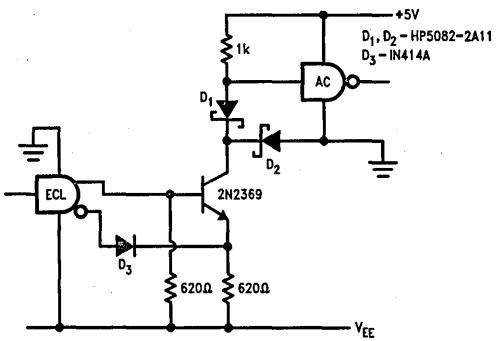
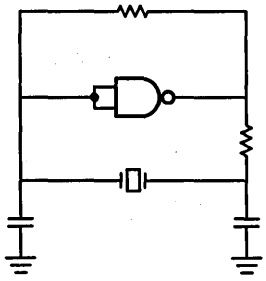
FIGURE 3-4b. Single-Ended ECL-to-'AC Circuit



TL/F/10160–6

FIGURE 3-4c. Differential Output ECL-to-'AC Circuit

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.



TL/F/10160–7

FIGURE 3-5. Crystal Oscillator Circuit Implemented with FACT 'AC00

Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = \frac{Z_o}{\sqrt{1 + C_t/C_l}}$$

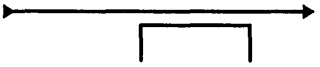
$$t_{pde} = t_{pd}\sqrt{1 + C_t/C_l}$$

where C_l = intrinsic line capacitance and C_t = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

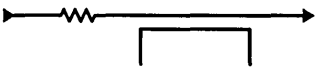
Line Driving and Termination (Continued)

There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.



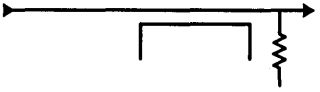
TL/F/10160–8

a. No Termination



TL/F/10160–9

b. Series Termination

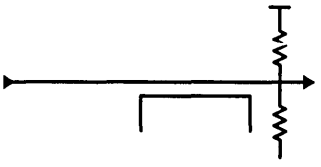


TL/F/10160–10

c. Parallel Termination

TL/F/10160–11

d. AC Parallel Termination



TL/F/10160–12

e. Thevenin Termination

FIGURE 3-6a. Termination Schemes

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \bullet Z_{oe}/(Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination

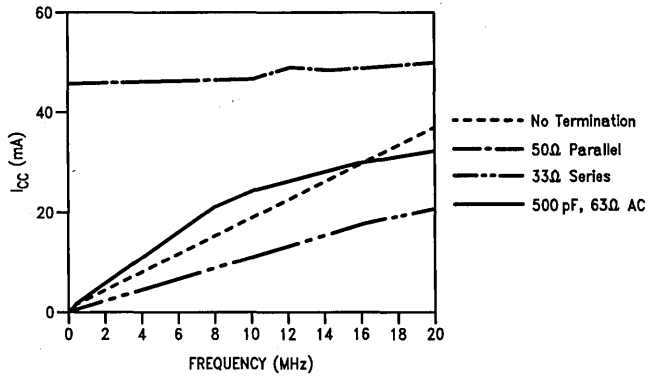
Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

- Parallel: Resistor = Z_o
- Thevenin: Resistor = $2 \times Z_o$
- Series: Resistor = $Z_o - Z_{out}$
- AC: Resistor = Z_o

  Capacitor = $C \geq \frac{3td}{Z_o}$
- Active: Resistor = $2 \times Z_o$

Figure 3-6b. Suggested Termination Values

Thevenin Termination (Continued)



TL/F/10160–13

FIGURE 4-6c. FACT I_{CC} vs Termination

FACT circuits have been designed to drive 50Ω transmission lines over the full commercial temperature range and 75Ω transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in *Figure 3-7*.

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FIGURE 3-7. Input Threshold

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 3-8 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line.

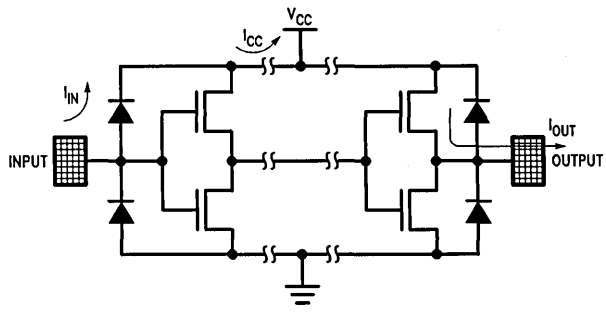

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FIGURE 3-8. Noise Effects

Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC}. At 5V V_{CC}, FACT's specified input and output levels give almost 1.5V of noise margin for both ground- and V_{CC}-born noise. With realistic input thresholds closer to 50% of V_{CC}, the actual margins approach 2.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

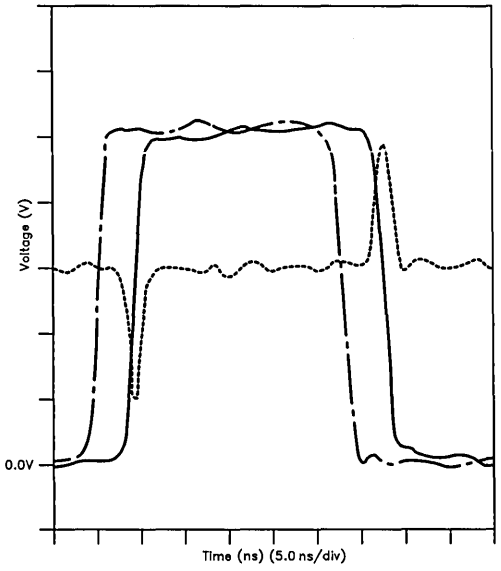
Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, *Figure 3-9a*, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (ϵ_r = 1.0) and epoxy glass (ϵ_r = 4.7). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, *Figure 3-9b*, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in *Figures 3-10a* and *3-10b*, exemplify the outstanding immunity to everyday noise which can effect system reliability.



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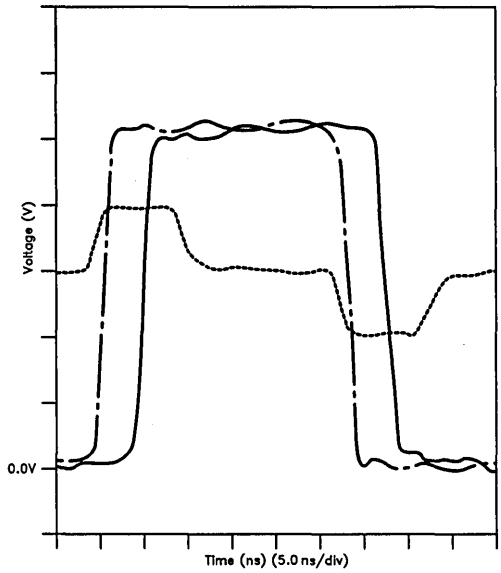
This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9a. Forward Crosstalk on PCB Traces

Crosstalk (Continued)

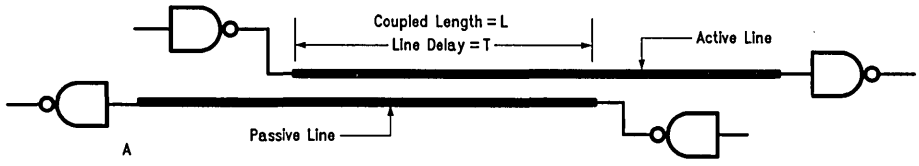


TL/F/10160–17

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

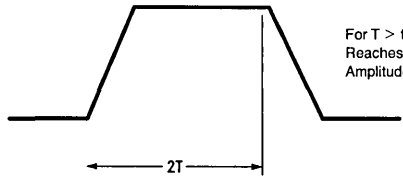
FIGURE 3-9b. Reverse Crosstalk on PCB Traces

Crosstalk (Continued)



TL/F/10160–18

Noise Pulses at A:



For T > t_r Noise Reaches Max Amplitude

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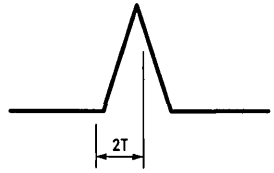

For T = 0.5 t_r Noise Just Reaches Max at Peak

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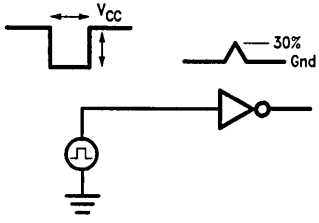
For T < 0.5 t_r Noise Never Reaches Full Amplitude

TL/F/10160–21

FIGURE 3-9c. Partially Coupled Lines



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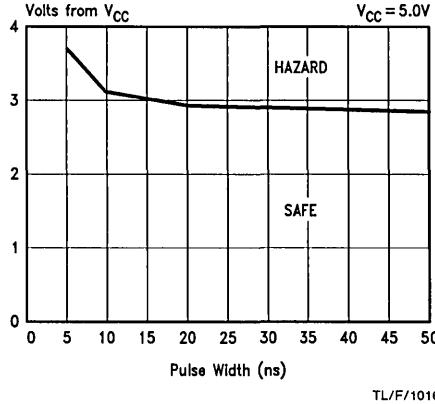

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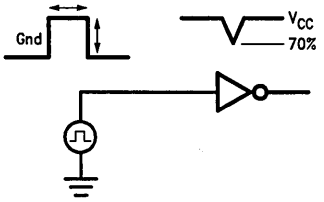
FIGURE 3-10a. High Noise Margin

Crosstalk (Continued)



TL/F/10160–24

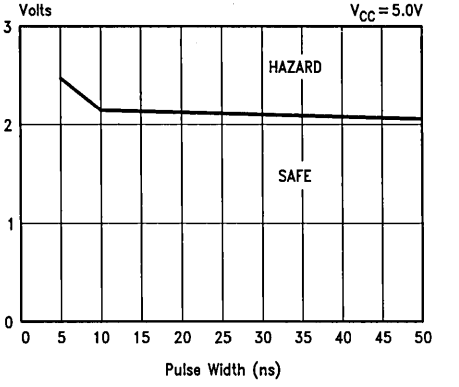


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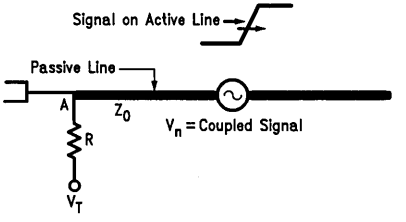
FIGURE 3-10b. Low Noise Margin

With over 2.0V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.



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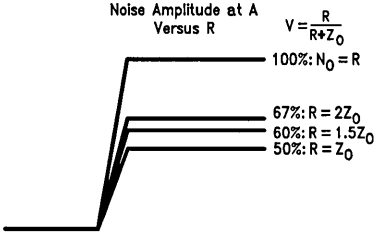

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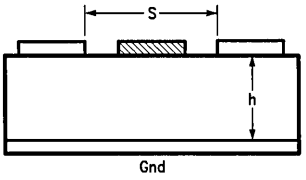
FIGURE 3-11a. Effects of Termination on Crosstalk



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace ▨ between signal traces
- Minimize distance h to keep line impedance low

TL/F/10160–32

FIGURE 3-11b. PCB Layout Tips for Crosstalk Avoidance

Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 3-12a shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the ouput of the device.

Ground Bounce (Continued)

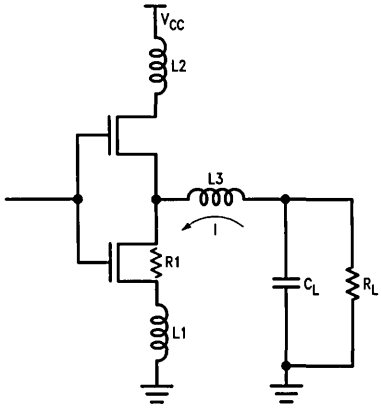


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FIGURE 3-12a. Output Model

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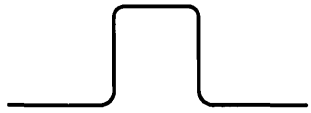
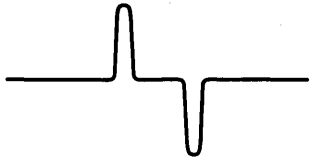
FIGURE 3-12b. Output Voltage



TL/F/10160–30

FIGURE 3-12c. Output Current



TL/F/10160–31

FIGURE 3-12d. Inductor Voltage

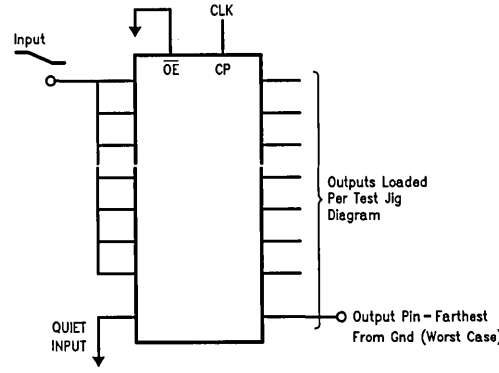
The three waveforms shown in *Figures 3-12b, c* and *d*, depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \bullet dV/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{gb} = -L \bullet (dI/dt)$].

Note: These models are included in order to assist in generating an understanding of where Ground Bounce originates. They are not intended to be used to predict the amplitude or duration of Ground Bounce noise. To use them as such will give inaccurate results. If all factors are taken into account, highly complex equations will result. Since these models are so complex, we shall use empirical results to develop an understanding of Ground Bounce.

There are many factors which affect the amplitude of the ground bounce. Included are:

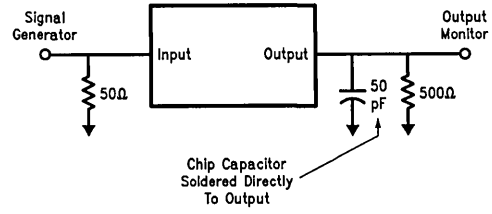
- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60 pF–70 pF increases ground noise. Beyond 70 pF, ground noise drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30% to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Quiet Output Test



TL/F/10160–33

Test Jig I/O Loading



TL/F/10160–34

FIGURE 3-13a. Test Jig Ground Bounce

Ground Bounce (Continued)

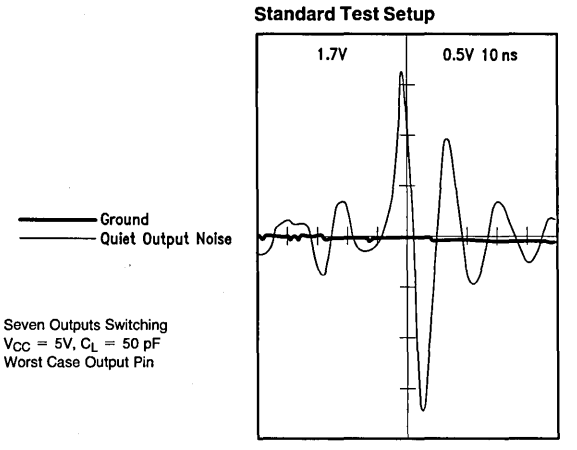
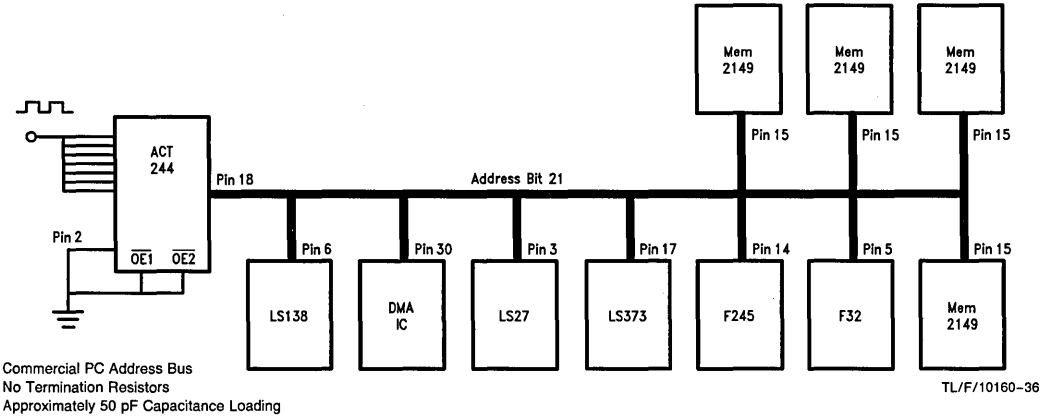


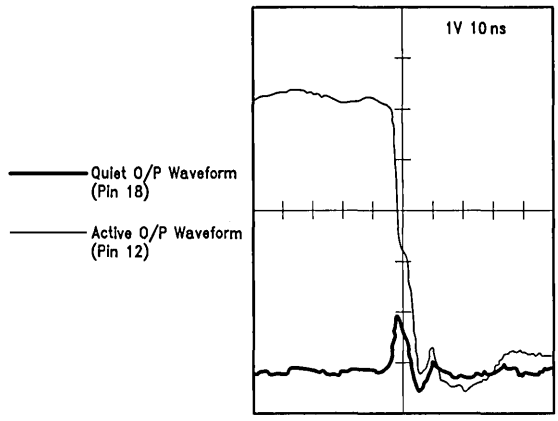
FIGURE 3-13b. Test Fixture Quiet Output Noise FACT AC374



- Commercial PC Address Bus
- No Termination Resistors
- Approximately 50 pF Capacitance Loading
- Replaced F244 with ACT244

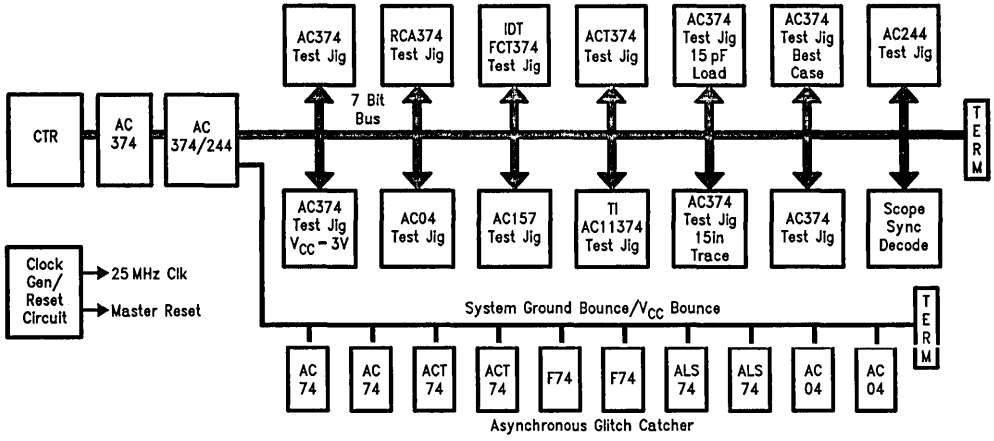
FIGURE 3-14a. Ground Bounce in a System

Ground Bounce (Continued)



TL/F/10160–37

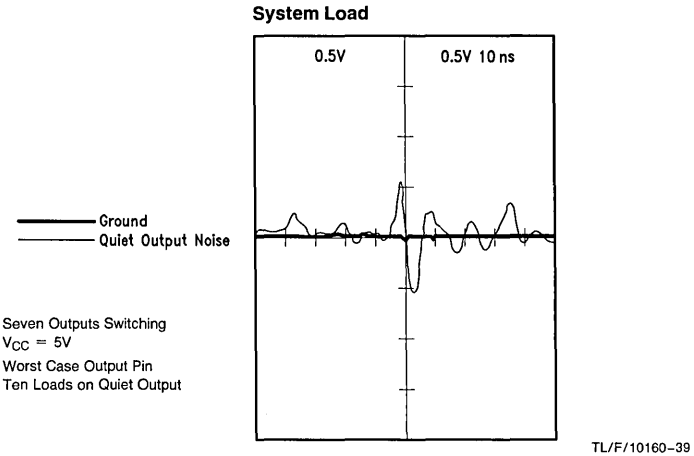
FIGURE 3-14b. System Ground Bounce



TL/F/10160–38

FIGURE 3-15a. Ground Bounce Demo Board Block Diagram

Ground Bounce (Continued)

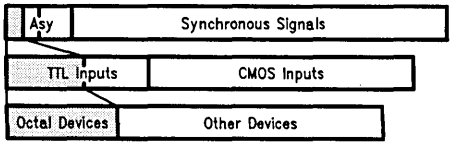


TL/F/10160–39

Figure 3-15b. System Quiet Output Noise FACT AC244

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are specified not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500 mV–1100 mV in actual system applications.



TL/F/10160–40

Use caution when using FACT octals to drive asynchronous signals into TTL level inputs.

FIGURE 3-16. Design Recommendation

Looking at the entire spectrum of logic applications, we can break them up into two distinct categories: Synchronous Signals and Asynchronous Signals. Only asynchronous signals could be affected because device generated noise is concurrent with active edges and is within the device's specified maximum propagation delay. These signals include Clock Pulses, Resets, Presets, Write Enable, etc. Asynchronous signals typically represent only about 10% of the overall spectrum of applications.

These asynchronous signal applications may be broken into two categories: TTL Input Thresholds and CMOS Input Thresholds. FACT inputs typically switch at 3.0V, for a 2.0 ns pulse width, and TTL inputs will switch at 1.7V (FAST and ALS), for the same pulse width. Because of this additional noise margin, ground bounce on asynchronous signals into FACT inputs is not a concern.

Again breaking up the TTL inputs group of applications into two groups, only those inputs being driven by FACT devices with eight or more outputs may be affected. Ground bounce created by 6 or less outputs switching simultaneously is small when compared to noise levels generated by octals. In many cases, the need for buffers can be eliminated because all FACT devices feature 24 mA outputs.

Therefore only a small segment (about 5%) of applications may be affected by device generated noise, that is, FACT octal devices driving asynchronous signals into TTL input thresholds. Although in a system, ground bounce levels, if isolated, will not be great enough to switch TTL inputs. However, when summed with the overall possible system noise that may couple onto the signal trace line, device generated noise becomes a concern. That is why good, low noise design techniques play a valuable role in eliminating noise generated system problems.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

The set of design rules listed below is recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

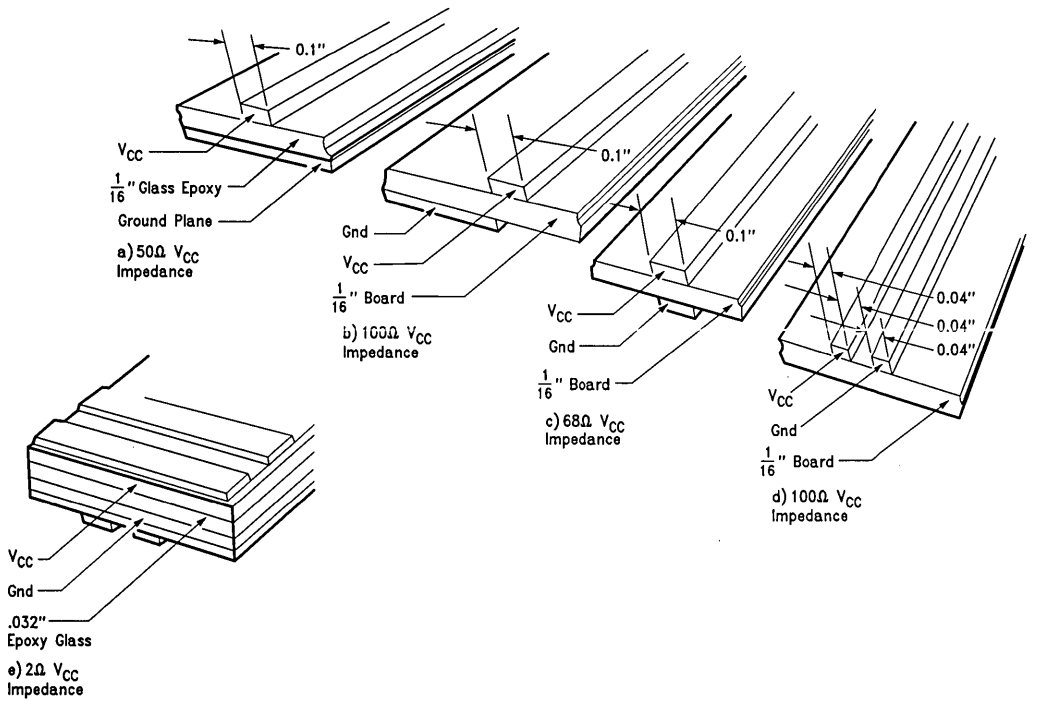
- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 μF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 3-18* displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50Ω and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in *Figure 3-19* to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100Ω bus from a point somewhere in the middle.



TL/F/10160–42

FIGURE 3-18. Power Distribution Impedances

Decoupling Requirements (Continued)

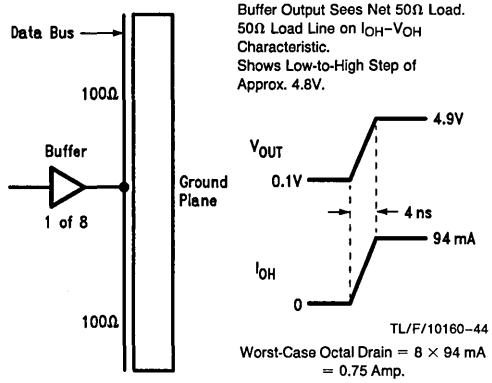
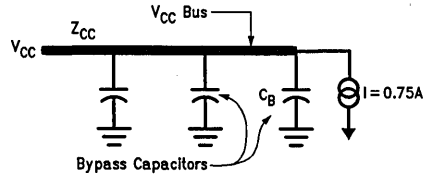


FIGURE 3-19. Octal Buffer Driving a 100Ω Bus

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 3-20*.

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, a 0.030 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



$Q = CV$

$I = C\Delta V/\Delta t$

$C = I\Delta t/\Delta V$

$\Delta t = 4 \times 10^{-9}$

Specify V_{CC} Droop = 0.1V Max

$$C = \frac{0.750 \times 4 \times 10^{-9}}{0.1} = 30 \times 10^{-9} = 0.030\ \mu F$$

Select $C_B \geq 0.047\ \mu F$

Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly throughout the logic. One capacitor per three packages.

FIGURE 3-20. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted. Radio Frequency Interference, or RFI, is simply a subset of EMI. EMI components that radiate within the broadcast broadband, consequently interfering with these broadcast frequencies, are generally referred to as RFI. Since FCC regulations are intended to protect broadcast frequencies from this interference, most emphasis has been placed on RFI. The terms RFI and EMI can often be used interchangeably.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

Electromagnetic Interference (Continued)

As *Figure 3-21* illustrates, EMI in a typical electronic circuit is generated by a current flowing in a loop configured within the circuit. These paths can be either V_{CC}-to-GND loops or output-to-GND loops. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The loop material inself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. *Figure 3-22* illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating loop area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{CC}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

Figures 3-23a and *3-23b* illustrate results from an EMI radiation predication model of logic ICs with standard (corner V_{CC} and GND) pinout and non-standard (central V_{CC} and GND) pinout, respectively. The V_{CC}-to-GND loop was analyzed. The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet Freq^2}{D}\left[1 + \left(\frac{\lambda}{2\pi D}\right)^2\right]^{1/2} \frac{\mu V}{m}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the loop area in square cm

λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figure 3-23c illustrates the predicted radiation from signals propagating on eight typical PCB transmission lines. Note the difference in the levels of radiated EMI between the IC packages and the signal traces. The difference between package pinout becomes negligible.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data transmission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 6 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

Electromagnetic Interference (Continued)

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undersirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 1.0 μF to 10.0 μF, provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF to 0.01 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

BACKPLANE CONSIDERATIONS

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

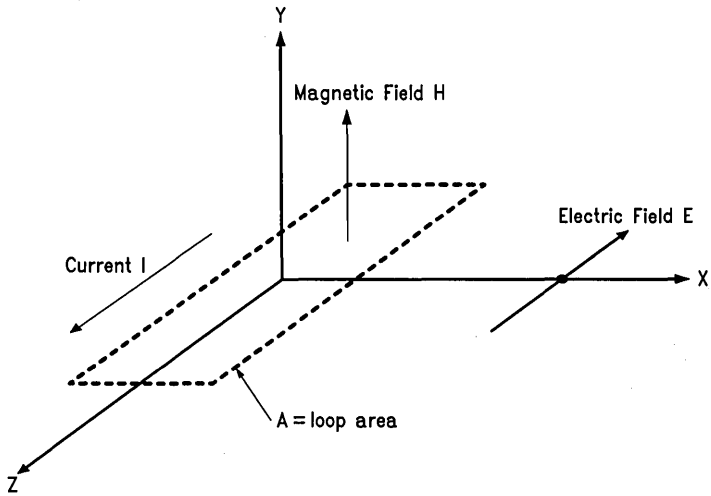


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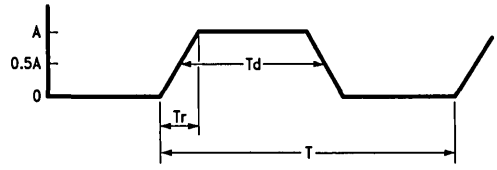
FIGURE 3-21. EMI Is Generated by a Current Flowing in a Loop

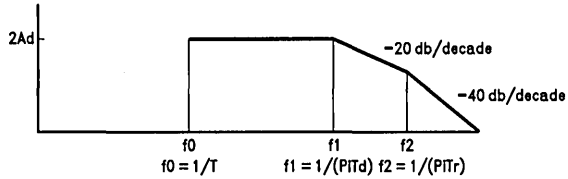
Electromagnetic Interference (Continued)

Time Domain



TL/F/10160–47

Frequency Domain



TL/F/10160–48

FIGURE 3-22. Output Characteristics

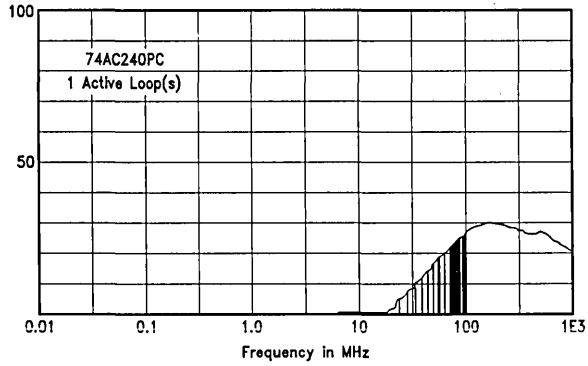


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FIGURE 3-23a. Electric Field Radiation in dBμV/m from 1 Loop(s) of Area 0.6 square cm

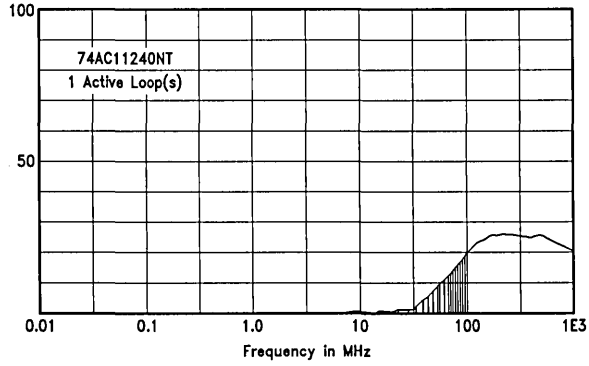

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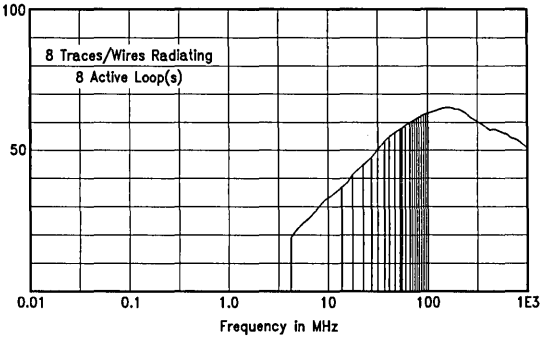
FIGURE 3-23b. Electric Field Radiation in dBμV/m from 1 Loop(s) of Area 0.19 square cm

Electromagnetic Interference (Continued)



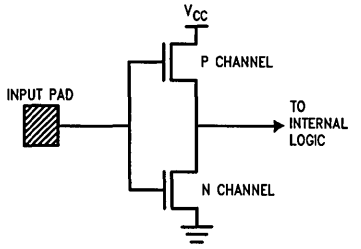
TL/F/10160–51

FIGURE 3-23c. Electric Field Radiation in dBμV/m from 8 Loop(s) of Area 10 square cm

TTL-Compatible CMOS Designs Require Delta I_{CC} Consideration

The FACT product line is comprised of two types of advanced CMOS circuits: 'AC and 'ACT devices. 'ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this 'ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

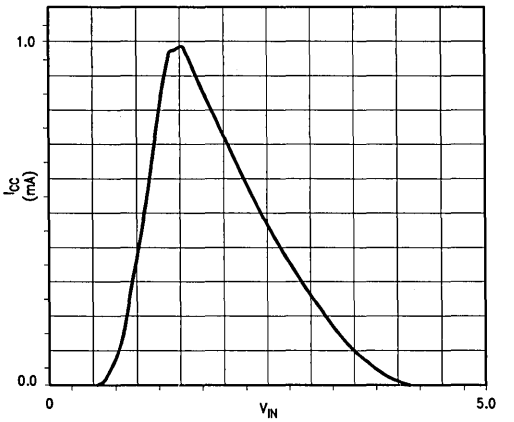
It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.



TL/F/10160–52

FIGURE 3-24. CMOS Input Structure

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 4 kΩ while the resistance of an OFF transistor is generally greater than 500 MΩ. When the input to this structure is at either ground or V_{CC}, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 500 MΩ. The leakage current will then be less than 1 μA. When the input is between ground and V_{CC}, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600Ω. This reduction in series resistance of the input structure will cause a corresponding increase in I_{CC} as current flows through the input structure. The following graph depicts typical I_{CC} variance with input voltage for an 'ACT device.



TL/F/10160–53

FIGURE 3-25. I_{CC} versus Input Voltage for 'ACT Devices

The Delta I_{CC} specification is the increase in I_{CC}. For each input at V_{CC} − 2.1V (approx. TTL V_{OH} level), the Delta I_{CC} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{CC} value.

Fortunately, there are several factors which tend to reduce the increase in I_{CC} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5V. Additionally, the typical I_{CC} increase per input will be less than the specified limit. As shown in the graph above, the I_{CC} increase at V_{CC} − 2.1V is less than 200 μA in the typical system. Experiments have shown that the I_{CC} of an 'ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or V_{CC}.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{CC} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

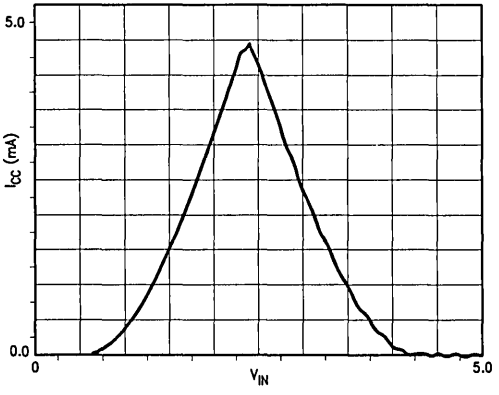
There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{CC} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{CC} specification orders of magnitude less than standard load currents. Most CMOS I_{CC} specifications are usually less than 100 μA. When conducting an I_{CC} test, greater care must be taken so that other currents will not mask the actual I_{CC} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{CC} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{CC} test. Even a standard 500Ω load resistor will sink 10 mA at 5V, which is more than twice the I_{CC} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{CC} tests.

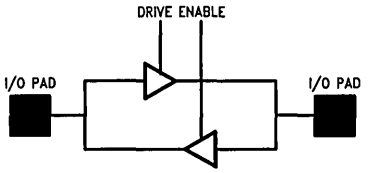
Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{CC} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from V_{CC} to ground. This conduction path leads to the increased I_{CC} current seen in the I_{CC} vs V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most I_{CC} testing is done with all of the inputs tied to either V_{CC} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{CC} of the device under test which is being measured by the tester.



TL/F/10160–54

FIGURE 3-26. I_{CC} versus I_{IN}

When testing the I_{CC} of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.



TL/F/10160–55

FIGURE 3-27. '245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{CC} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{CC} to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{CC} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. This combined leakage test is defined as IOZ_T. For FACT devices, I_{IN} is specified at ± 1 μA while I_{OZ} is specified at ± 5 μA. Combining these gives a limit of ± 6 μA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

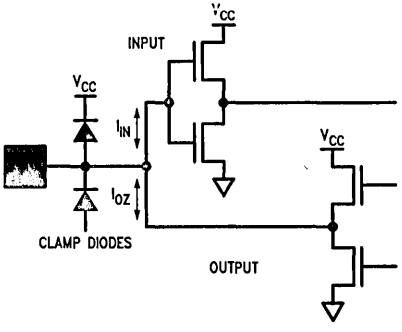


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FIGURE 3-28. I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning

Testing Advanced CMOS Devices with I/O Pins (Continued)

to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment

Traditionally, the disable time of a TRI-STATE buffer has been measured from the 50% point on the disable input, to the (V_{OL} + 0.3V) or (V_{OH} − 0.3V) point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

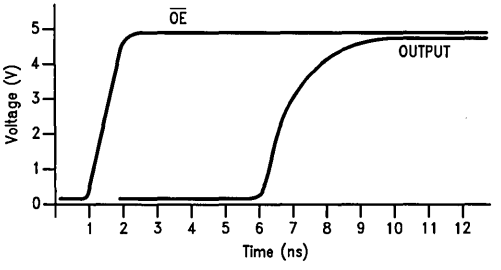

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FIGURE 3-29. Typical Bench TRI-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

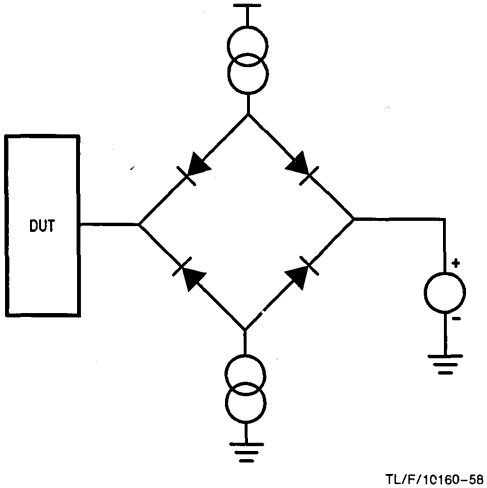

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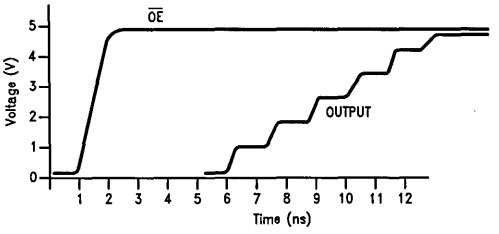
FIGURE 3-30. MCT Wheatstone Bridge Test Load

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the (V_{OL} + 0.3V) level or fallen to the (V_{OH} − 0.3V) level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in *Figure 3-31*.



TL/F/10160–59

FIGURE 3-31. Typical ATE TRI-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50Ω to 60Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 575 mV at 5.5V V_{CC}. Three reflections of the current pulse would be required before the com-

Testing Disable Times of TRI-STATE Outputs in a Transmission Line Environment (Continued)

parator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.

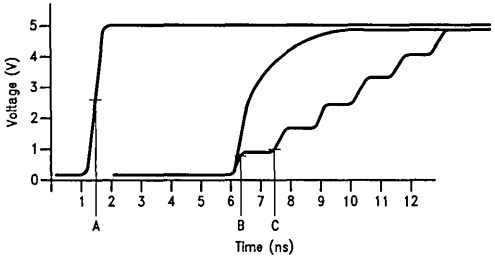


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FIGURE 3-32. Measurement Stepout

Understanding Latch-Up in Advanced CMOS Logic

National Semiconductor
Application Note 600

Latch-up has long been a bane to CMOS IC applications; its occurence and theory have been the subjects of numerous studies and articles. The applications engineer and systems designer, however, are not so much concerned with the theory and modeling of latch-up as they are with the consequences of latch-up and what has been done by the device designer and process engineer to render ICs resistant to latch-up.

Of equal interest are those precautions, if any, which must be observed to limit the liability of designs to latch-up.

WHAT IS LATCH-UP?

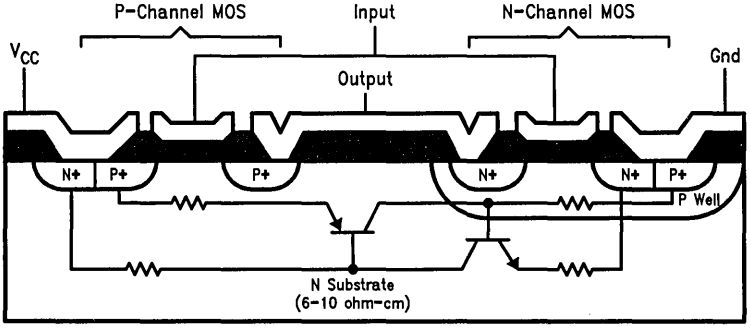
Latch-up is a failure mechanism of CMOS (and bipolar) integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction. It may be a temporary condition that terminates upon removal of the exciting stimulus, a catastrophic condition that requires the shutdown of the system to clear or a fatal condition that requires replacement of damaged parts. Regardless of the severity of the condition, latch-up is an undesirable but controllable phenomenon. In many cases, latch-up is avoidable.

The cause of the latch-up exists in all junction-isolated or bulk CMOS processes: parasitic PNPN paths. *Figure 1*, a basic CMOS cross section, shows the parasitic NPN and PNP bipolar transistors which most frequently participate in latch-up. The P+ sources and drains of the P-channel MOS devices act as the emitters (and sometimes collectors) of lateral PNP devices; the N-substrate is the base of this device and collector of a vertical NPN device. The P-well acts as the collector of the PNP and the base of the NPN. Finally, the N+ sources and drains of the N-channel MOS devices serve as the emitter of the NPN. The substrate is normally connected to V_{CC}, the most positive circuit voltage, via an N+ diffusion tap while the P-well is terminated at Gnd, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and P-well.

Normally, only a small leakage current flows between the substrate and P-well causing only a minute bias to be built up across the bulk due to the resistivity of the material. In this case the depletion layer formed around the reverse-biased PN junction between P-well and the substrate supports the majority of the V_{CC}-Gnd voltage drop. As long as the MOS source and drain junctions remain reverse-biased, CMOS is well behaved. In the presence of intense ionizing radiation, thermal or over-voltage stress, however, current can be injected into the PNP emitter-base junction, forward-biasing it and causing current to flow through the substrate and into the P-well. At this point, the NPN device turns on, increasing the base drive to the PNP. The circuit next enters a regenerative phase and begins to draw significant current from the external network thus causing most of the undesirable consequences of latch-up. Once established, a latch-up site, through the fields generated by the currents being conducted, may trigger similar action in both elements of the IC.

WHAT TO DO

As might be expected, latch-up is highly dependent on the characteristics of the bipolar devices involved in the latch-up loop. Device current gains, emitter efficiencies, minority carrier life times and the degree of NPN-PNP circuit coupling are all important factors relating to both the sensitivity of the particular latch-up device and to the severity of the failure once it has been excited. Layout geometry and process both contribute significantly to these parameters; CMOS, like other technologies, has been shrunk to provide more function per unit area, increasing susceptibility to latch-up. All major CMOS vendors have upgraded their processes and/or design rules to compensate for this increased susceptibility, some with more success than others. The lateral PNP is typically the weak link in the latch-up loop. As such, various devices can be exploited toward reducing the effectiveness of the PNP to participate in latch-up. Guard banding, device placement, the installation of pseudo-collectors between the P-channel devices and the P-well, and the use of a low resistivity substrate under an epitaxial layer are a few of the IC design tactics now being practiced to reduce the current gain or to control the action of the lateral PNP structures in state-of-the-art CMOS devices.



TL/F/10192-1

FIGURE 1. Basic CMOS Inverter Cross Section with Latch-Up Circuit Model

Vendors of CMOS ICs have always been aware of the latch-up phenomenon and have considerably improved their designs and processes to reduce the danger of latch-up occuring under normal usage. Abnormal applications and misuse of CMOS ICs may still pose problems that the CMOS vendor has little control over. Hence, CMOS users must be aware of what they are doing and those measures which must be taken to reduce the susceptibility to latch-up. The use of CMOS at or beyond its rated maximum voltage range and the presence of inductive transients are applications-related situations which can trigger latch-up. Environment, including thermal stress, poorly regulated or noisy supplies and radiation incidence can also contribute to or cause latch-up. The system engineer must consider these situations when using CMOS in designs.

While latch-up is generally recognized as resulting from regenerative switching along a PNPN path, many designers incorrectly assume that this regenerative action places the device in a state that can only be recovered from if the system is powered down. The fact is that there is probably an equal, if not greater, chance that the regenerative switching, when encountered, will be non-sustaining (the condition, more accurately referred to as current amplification, will disappear when the triggering stimulus is removed); over-voltage applied to properly designed input protection networks is one example of controlled current amplification. For sustained latch-up to occur, the regeneration loop must have sufficient gain and the power source must be able to supply a minimum current. From this we can see that current-limited power supplies might be used to recover from or reduce the effects of latch-up. Another method uses current-limiting series resistors in the power connections of offending ICs in conjunction with storage capacitors shunting the devices. Normal switching current will be drawn from the capacitors while DC current will be limited by the resistors.

In the loop of positive current feedback formed by the parasitic PNP and NPN transistors of the latch-up structures, regenerative switching may result if sufficient loop gain is available. One must remember, though, that three conditions are necessary for latch-up to occur.

1) both parasitic bipolars must be biased into the active state;
2) the product of the parasitic bipolar transistor current gains ($B_{npn} \cdot B_{pnp}$) must be sufficient to allow regeneration, i.e., greater than or equal to one;
3) the terminal network must be capable of supplying a current greater than the holding current required by the PNPN path. In processes utilizing an epitaxial silicon, this current is usually in excess of 1A.

If any of these conditions is not met both during the initiation and in the steady state, then the latch-up condition is either non-sustaining or cannot be initiated. If the current to the latched structure is not limited, permanent damage may result. Again, any means to prevent any of these conditions from being satisfied will protect the circuit from exhibiting sustained latch-up.

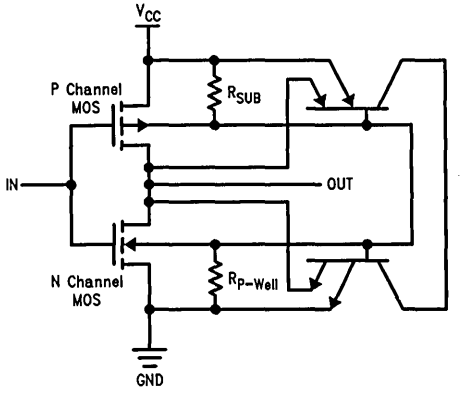
The prevention of biasing the bipolars into the active region and the limiting of the current which may be supplied by the network are the two factors which system designers have under their control. Many of the protective measures long exercised in discrete and TTL designs may also be applied to CMOS designs to reduce susceptibility and prevent damage to these systems. Diode clamping of inductive loads, signal and supply level regulation, and sharing of large DC loads by several devices with suitable series limiting resistors to distribute thermal stress over a larger area or multiple ICs are all positive-preventive measures to exploit.

While we have been considering the CMOS device in a generic manner, there are two primary structures used in all CMOS ICs which have latch-up paths associated with them; these are the inverter or gate and the transmission switch. Both structures may be susceptible under the right conditions. While the CMOS inverter can exhibit latch-up independent of circuit configuration, the transmission switch usually has lower holding current, and thus, a lower threshold for latch-up, but is dependent on its external connections for latch-up to occur. *Figure 2* shows the lumped equivalent circuit of the inverter. Notice the shunting resistors across the base-emitter junctions of the bipolar transistors: these resistors divert base drive from the bipolars and as a result increase both the trigger current and holding current levels required for the structures to participate in latch-up. A further increase in these current levels can be achieved by further decreasing the shunt resistance. Diffusing all active components into an epitaxial silicon, under which would lie a substrate of substantially less resistivity, will have a dramatic effect on decreasing the shunt resistance, therefore increasing the trigger current and holding current levels required for latch-up.

THE CIRCUIT CONNECTION

As we have seen above, the external circuit connections are regular participants in the latch-up process. The current for latch-up comes from these connections and often the triggering mechanism is external to the latching device. All three classes of external connections (power, input and output) are important in latch-up. We will now look at how these connections relate to this process.

Current injection through the power terminals when the power supply voltage is beyond the maximum rated for the CMOS device can directly cause latch-up through base collector leakage or breakdown mechanisms. One aspect of high power supply voltages that is not often recognized is the effect of field-aiding lateral currents under the emitters of the PNP devices. This can effect a significant increase in the beta of these devices, making internally trigger latch-up much more prevalent. Again, the warning to the the system designer is to avoid using CMOS at maximum rated supply voltages unless precautions are taken to insure latch-up is unlikely or is at least acceptable and recoverable. Switching transients coupled onto power lines has become a problem



TL/F/10192–2

FIGURE 2. CMOS Inverter with Parasitic Bipolars

now that CMOS has become a high-speed logic technology. Attention to power supply decoupling is now a necessity when designing with high-speed CMOS. Of course, CMOS processes incorporating an epitaxial silicon over a substrate of very low resistivity is less prone to latch-up under these conditions. These recommended precautions should be taken just the same.

Latch-up involving input terminals, next to gate oxide rupture, used to be one of the most common failure mechanisms of CMOS. Transients exceeding the power supply routinely caused either or both of these effects to occur. Fortunately, CMOS vendors have learned to make better input protection networks and have learned that proper placement of these components with respect to the rest of the chip circuitry is necessary to reduce susceptibility to latch-up. The system designer should review foreign input signals to CMOS systems and take precautions necessary to limit the severity of over/undershoot from these sources. Measures which could be used to reduce the possibility of latch-up induced by input signals are: proper termination of transmission lines driving CMOS, series current limiting resistors, AC coupling with DC restoration to the CMOS supplies, and the addition of Schottky diode clamps to the CMOS power rails. As an additional measure there are several CMOS circuits which have input protection networks that can handle overvoltage in one direction or the other and which are specifically designed to act as interface circuits between other logic families and CMOS. Judicious application of these will also aid in suppressing any tendencies of CMOS systems to latch-up.

Finally, attention to CMOS outputs, their loading and the stresses applied to them will also enable the designer to generate latch-up free systems. Historically, output terminals of CMOS have been least likely to cause latch-up though they can participate in latch-up once it is initiated. The normal mode of failure in this respect is, again, the application of voltages beyond the CMOS supplies or the maximum limit for the devices though excessive current has also been linked to latch-up failure at elevated temperatures. Inductive surges and transmission line reflections are the most likely sources of output latch-up in CMOS and should be attended to in the most applicable method, i.e., by clamping, termination or through dissipative measures.

WHAT WE HAVE DONE

National Semiconductor, as an important supplier of advanced CMOS to all segments of the industry, has made a commitment to provide IC designs which make use of state-of-the-art latch-up suppression techniques in an effort to support its customers before they need support. The three most important actions which we have taken to guard our customers from latch-up are in the areas of layout, power distribution and process design. These techniques, along with recognized good design practice, yield a product line that lives up to the intent of an advanced CMOS family. In brief review, National Semiconductor's attack on latch-up is summarized in the following.

Latch-Up Protection Geometries

Every FACT™ IC employs special geometries to isolate every input protection device and every output from active areas on the chip. In this way, structures which would normally participate in latch-up loops are decoupled and are thus less troublesome. All devices are scrutinized for potential latch-up sites and are protected by similar geometries where any risk is significant.

Power Distribution

Careful attention to on-chip power distribution and enhanced termination of P-wells and substrate is used by National Semiconductor to improve latch-up resistance. Our double metal process affords the advantage in maintaining low impedance distribution of power and ground potentials over the entire chip; the potential gradient-caused fields which often induce or enhance latch-up are thus minimized while functional performance is enhanced by cleaner on-chip power supplies.

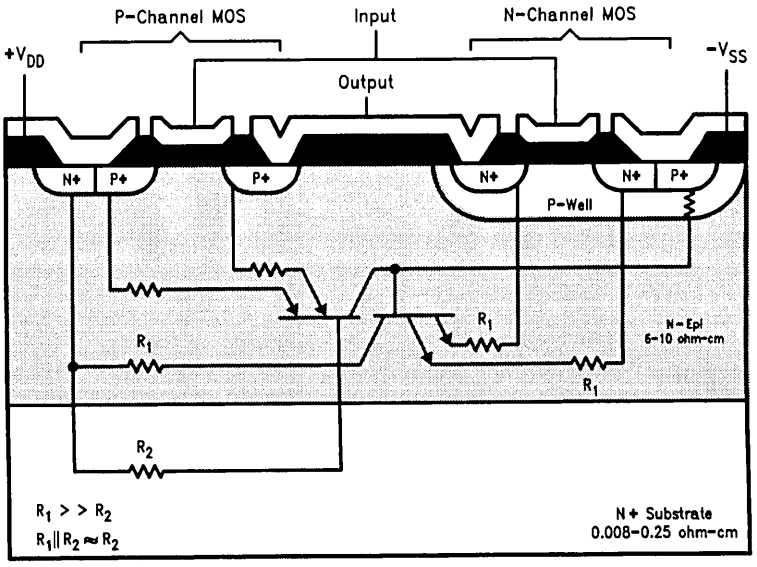
Process Design

By design, the FACT process is better both in low latch-up susceptibility and in enhanced device performance. The most significant advancement of the FACT process has been the incorporation of an epitaxial silicon layer. *Figure 3* illustrates a modified version of *Figure 1*, utilizing an epitaxial layer of silicon to contain all of the active components of the CMOS circuit. This epitaxial layer allows the use of a separate layer of substrate silicon, of a resistivity some three orders of magnitude lower than the epitaxial layer. The effect is also modeled in *Figure 3*.

As illustrated, the resistivity of the epitaxial silicon, R_1, is on the order of 6 ohm-cm to 10 ohm-cm. The underlying substrate resistivity, R_2, is as low as 0.008 ohm-cm to 0.025 ohm-cm. The result is a parallel combination of resistivities, R_1 and R_2, that is equivalent to R_2. What has now happened is that the gain of the parasitic PNP-NPN circuit has been dramatically slashed. Under the same latch-up conditions described earlier, the introduction of the low resistivity substrate now means that at least 10 times more current is needed to trigger the parasitic PNP-NPN combination.

The active components within the epitaxial layer maintain the same performance characteristics as those of the active area illustrated in the non-epitaxial CMOS circuit of *Figure 1*. Therefore the introduction of the epitaxial layer to the FACT process does not reduce any AC, DC, functional or ESD performance. However, what we have is an advanced CMOS logic family that is now virtually latch-up immune.

Thus, through innovative and careful layout, attention to eliminating circuit situations which could be latch-up prone and by careful selection and maintenance of our advanced CMOS process, FACT sets the standard for latch-up resistance.



TL/F/10192-3

FIGURE 3

Section 4

Advanced CMOS Datasheets

Section 4 Contents

Section 4 Contents (Continued)

Section 4 Contents (Continued)

National Semiconductor

54AC/74AC00 • 54ACT/74ACT00
Quad 2-Input NAND Gate

General Description

The 'AC/'ACT00 contains four 2-input NAND gates.

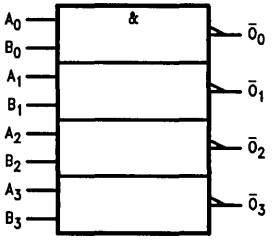
Features

- Outputs source/sink 24 mA
- 'ACT00 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol

IEEE/IEC



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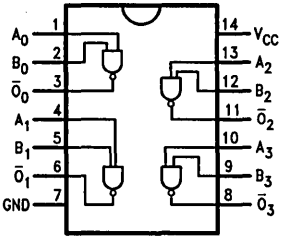
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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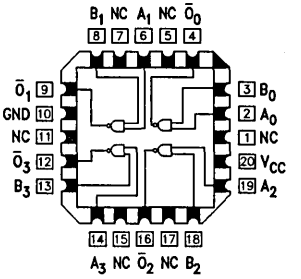
Pin Assignment for LCC



TL/F/9911–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5		I_{OL} 24 mA
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	1.0	11.0	2.0	10.0	ns	2-5
		5.0	1.5	6.0	8.0	1.0	8.5	1.5	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	9.0	1.0	8.5	ns	2-5
		5.0	1.5	4.5	6.5	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	1.0	9.5	ns	2-5
t_{PHL}	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	1.0	8.0	ns	2-5

Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC02
Quad 2-Input NOR Gate

General Description

The 'AC02 contains four, 2-input NOR gates.

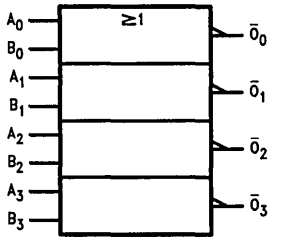
Features

- Outputs source/sink 24 mA

Ordering Code: See Section 5

Logic Symbol

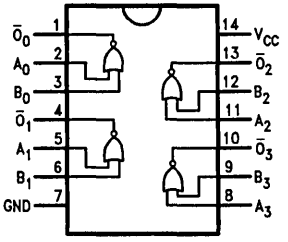
IEEE/IEC



TL/F/9912–1

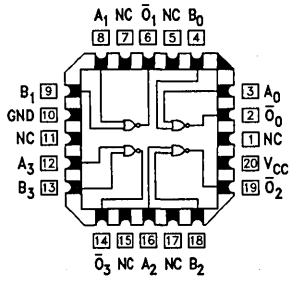
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9912–3

Pin Assignment for LCC



TL/F/9912–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	2-5
		5.0	1.5	4.5	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC04 • 54ACT/74ACT04 Hex Inverter

General Description

The 'AC/'ACT04 contains six inverters.

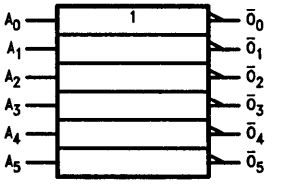
The information for the 'ACT04 is Advanced Information only.

Features

- Outputs source/sink 24 mA
- 'ACT04 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol



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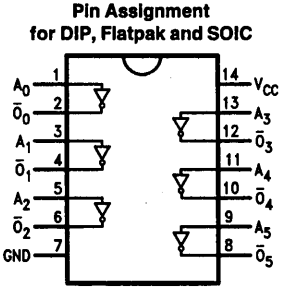
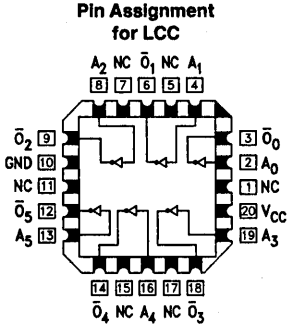
Connection Diagrams



TL/F/9913–3



TL/F/9913–2

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT $-40°C$ to $+85°C$
- 54AC/ACT $-55°C$ to $+125°C$

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -12 mA
		4.5		3.86	3.7	3.76		I_{OH} -24 mA
		5.5		4.86	4.7	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	4.5	9.0	1.0	11.0	1.0	10.0	ns	2-5
		5.0	1.5	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay	3.3	1.5	4.5	8.5	1.0	10.0	1.0	9.5	ns	2-5
		5.0	1.5	3.5	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC08 • 54ACT/74ACT08
Quad 2-Input AND Gate

General Description

The 'AC/'ACT08 contains four, 2-input AND gates.

Features

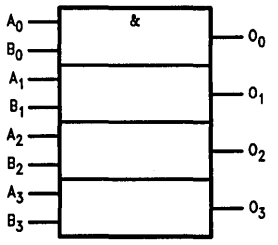
- Outputs source/sink 24 mA
- 'ACT08 has TTL-compatible inputs

The information for the 'ACT08 is Advanced Information only.

Ordering Code: See Section 5

Logic Symbols

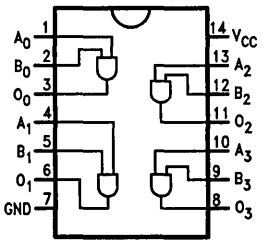
IEEE/IEC



TL/F/9914–1

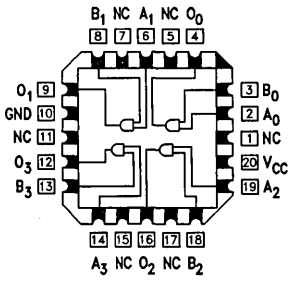
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9914–3

Pin Assignment for LCC



TL/F/9914–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT $-40°C$ to $+85°C$
- 54AC/ACT $-55°C$ to $+125°C$

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC / 54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} -12 mA
		4.5		3.86	3.76		I_{OH} -24 mA
		5.5		4.86	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} 12 mA
		4.5		0.36	0.5		I_{OL} 24 mA
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	12.5	1.0	10.0	ns	2-5
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	2-5
		5.0	1.5	5.5	7.0	1.0	8.5	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC10
Triple 3-Input NAND Gate

General Description

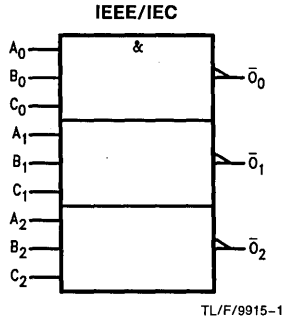
The 'AC10 contains three, 3-input NAND gates.

Features

- Outputs source/sink 24 mA

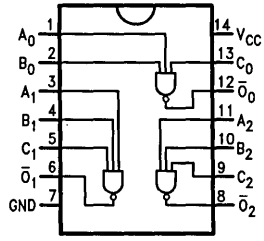
Ordering Code: See Section 5

Logic Symbol

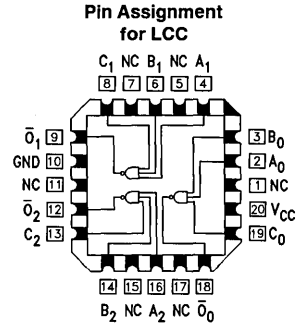


TL/F/9915–1

Connection Diagrams



TL/F/9915–3



TL/F/9915–2

Pin Names	Description
A_n, B_n, C_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	6.0	9.5	1.0	11.0	1.0	10.5	ns	2-5
		5.0	1.5	4.5	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.0	1.0	10.0	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC11
Triple 3-Input AND Gate

General Description

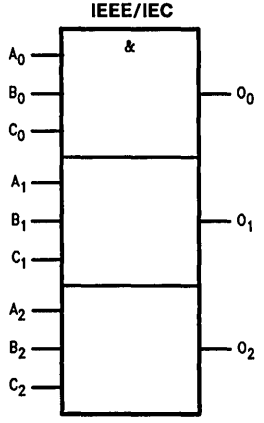
The 'AC11 contains three 3-input AND gates.

Features

- Outputs source/sink 24 mA

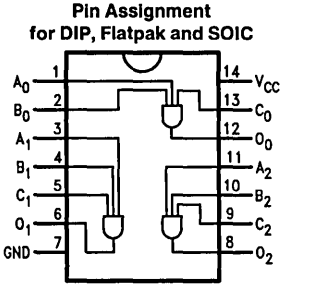
Ordering Code: See Section 5

Logic Symbol

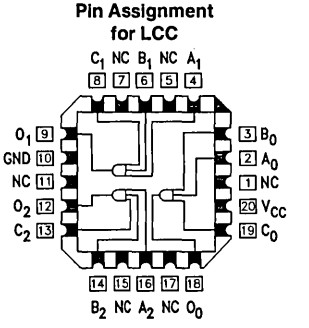


TL/F/9916–1

Connection Diagrams



TL/F/9916–3



TL/F/9916–2

Pin Names	Description
A_n, B_n, C_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		
		5.5		0.36	0.5	0.44		24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	5.5	9.5	1.0	11.0	1.0	10.0	ns	2-5
		5.0	1.5	4.0	8.0	1.0	8.5	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.5	1.0	9.5	ns	2-5
		5.0	1.5	4.0	7.0	1.0	8.0	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC14 • 54ACT/74ACT14
Hex Inverter with Schmitt Trigger Input

General Description

The 'AC/'ACT14 contains six inverter gates each with a Schmitt trigger input. The 'AC/'ACT14 contains six logic inverters which accept standard CMOS input signals (TTL levels for 'ACT14) and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 'AC/'ACT14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

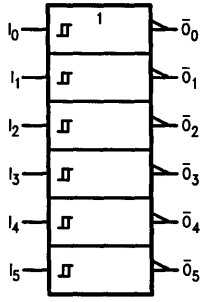
- Outputs source/sink 24 mA
- 'ACT14 has TTL-compatible inputs

The Information for the 'ACT14 is Advanced Information only.

Ordering Code: See Section 5

Logic Symbol

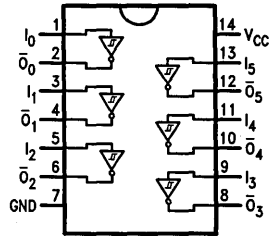
IEEE/IEC



TL/F/9917–1

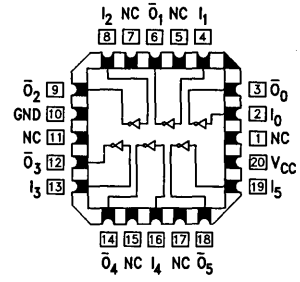
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9917–2

Pin Assignment for LCC



TL/F/9917–3

Function Table

Input	Output
A	$\overline{O}$
L	H
H	L

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
V_{t+}	Maximum Positive Threshold	3.0	2.2		2.2		V	T_A = Worst Case
		4.5	3.2	2.0	3.2	2.0		
		5.5	3.9		3.9			
V_{t-}	Minimum Negative Threshold	3.0	0.5		0.5		V	T_A = Worst Case
		4.5	0.9	0.8	0.9	0.8		
		5.5	1.1		1.1			

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
$V_{h(max)}$	Maximum Hysteresis	3.0	1.2		1.2			T_A = Worst Case
		4.5	1.4	1.2	1.4	1.2	V	
		5.5	1.6		1.6			
$V_{h(min)}$	Minimum Hysteresis	3.0	0.3		0.3			T_A = Worst Case
		4.5	0.4	0.4	0.4	0.4	V	
		5.5	0.5		0.5			
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.0	16.0	1.5	15.0	ns	2-5
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.0	14.0	1.5	13.0	ns	2-5
		5.0	1.5	6.0	8.5	1.0	10.0	1.5	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC20
Dual 4-Input NAND Gate

General Description

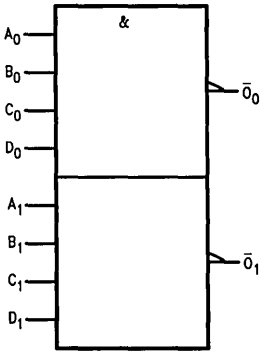
The 'AC20 contains four 4-input NAND gates.

Features

- Outputs source/sink 24 mA

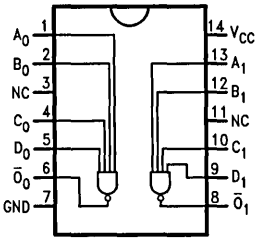
Ordering Code: See Section 5

Logic Symbol

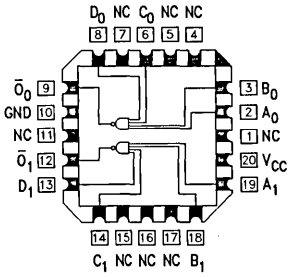


TL/F/9918–1

Connection Diagrams



TL/F/9918–3



TL/F/9918–2

Pin Names	Description
A_m, B_n, C_n, D_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	V	2.46 −12 mA
		4.5		3.86	3.7		3.76 I_{OH} −24 mA
		5.5		4.86	4.7		4.76 −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	V	0.44 12 mA
		4.5		0.36	0.5		0.44 I_{OL} 24 mA
		5.5		0.36	0.5		0.44 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note : I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	2.0	6.0	8.5	1.0	11.0	1.5	10.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.5	5.0	7.0	1.0	10.5	1.0	9.0	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC32 • 54ACT/74ACT32
Quad 2-Input OR Gate

General Description

The 'AC/'ACT32 contains four, 2-input OR gates.

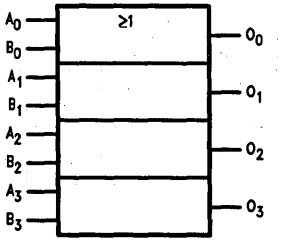
Features

- Outputs source/sink 24 mA
- 'ACT32 has TTL-compatible inputs

The information for the 'ACT32 is Advanced Information only.

Ordering Code: See Section 5

Logic Symbol



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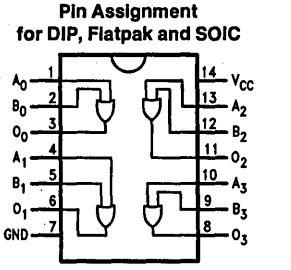
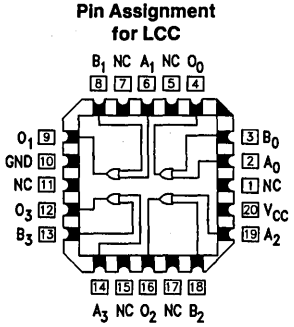
Connection Diagrams



TL/F/9919–3



TL/F/9919–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	0.44		12 mA
		4.5		0.36	0.5	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.0	9.0	1.0	12.0	1.5	10.0	ns	2-5
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	8.5	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC74 • 54ACT/74ACT74
Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

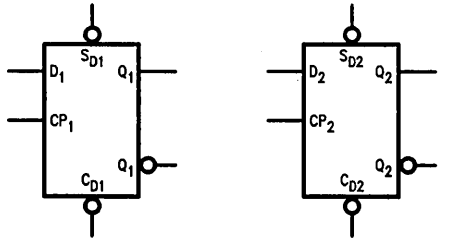
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs

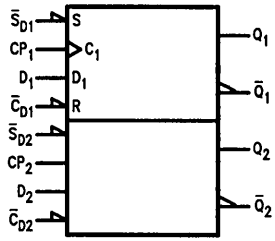
Ordering Code: See Section 5

Logic Symbols



TL/F/9920–1 TL/F/9920–2

IEEE/IEC

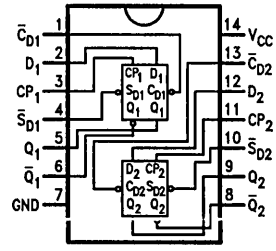


TL/F/9920–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

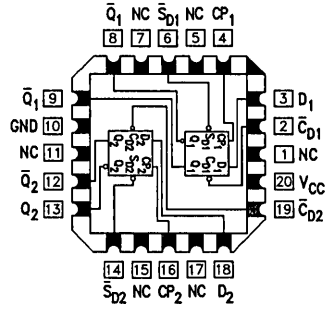
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9920–4

Pin Assignment for LCC



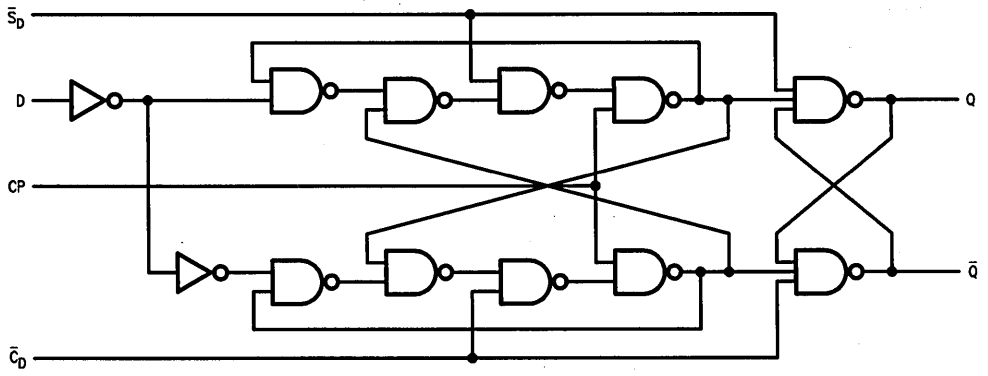
TL/F/9920–5

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



TL/F/9920–6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		70 95		95 125		MHz	2–3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	5.0 3.5	8.0 6.0	12.0 9.0	1.0 1.0	13.0 9.5	4.0 3.0	13.0 10.0	ns	2–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	1.0 1.0	14.0 10.5	3.5 2.5	13.5 10.5	ns	2–6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	1.0 1.0	17.5 12.0	4.0 3.0	16.0 10.5	ns	2–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	1.0 1.0	13.5 10.0	3.5 2.5	14.5 10.5	ns	2–6

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3 5.0	1.5 1.0	4.0 3.0	5.0 4.0	4.5 3.0	ns	2–9
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3 5.0	−2.0 −1.5	0.5 0.5	0.5 0.5	0.5 0.5	ns	2–9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	8.0 5.5	7.0 5.0	ns	2–6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0.5 0.5	0 0	ns	2–9

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz	2-3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	5.5	9.5	1.0	11.5	2.5	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	1.0	12.5	3.0	11.5	ns	2-6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.5	11.0	1.0	14.0	4.0	13.0.	ns	2-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.5	6.0	10.0	1.0	12.0	3.0	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	4.0	3.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	1.0	ns	2-9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	7.0	6.0	ns	2-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0.5	0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54AC/74AC85 • 54ACT/74ACT85
4-Bit Magnitude Comparator

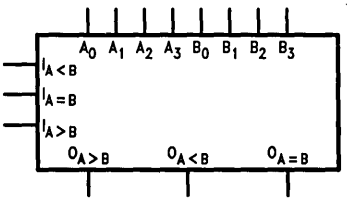
General Description

The 'AC/'ACT85 is a high speed, expandable 4-bit magnitude comparator which compares two 4-bit words in any monotonic code (binary, BCD or other) and generates three outputs: A less than B, A greater than B, and A equal to B. Three expansion inputs allow serial (ripple) expansion over any word length without external gates.

Features

- Easily expandable
- Binary or BCD comparison
- A > B, A < B, A = B output available
- 'ACT85 has TTL-compatible inputs

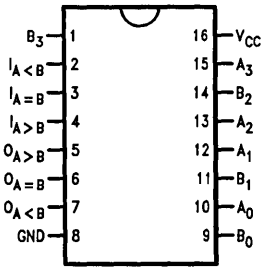
Logic Symbol



TL/F/9921–2

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/9921–1

Pin Names	Description
A_0–A_3	Word A Inputs
B_0–B_3	Word B Inputs
$I_{A=B}$	A = B Expansion Input
$I_{A<B}$, $I_{A>B}$	A < B, A > B Expansion Inputs
$O_{A>B}$	A Greater Than B Output
$O_{A<B}$	A Less Than B Output
$O_{A=B}$	A Equal B Output

National Semiconductor

54AC/74AC86
Quad 2-Input Exclusive-OR Gate

General Description

The AC/ACT 86 contains four, 2-input exclusive-OR gates.

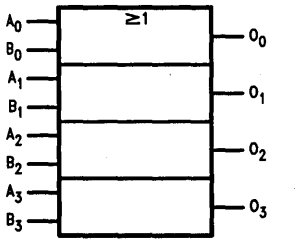
Features

- Outputs source/sink 24 mA

Ordering Code: See Section 5

Logic Symbol

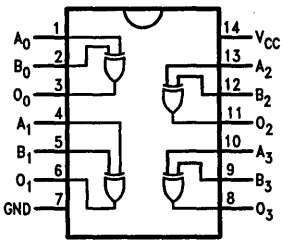
IEEE/IEC



TL/F/9909-3

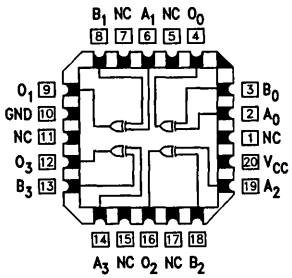
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9909-2

Pin Assignment for LCC



TL/F/9909-1

Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- V_I = 0.5V −20 mA
- V_I = V_{CC} +0.5V +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- V_O = −0.5V −20 mA
- V_O = V_{CC} +0.5V +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- CDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE®							V_I (OE) = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80	40	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay Inputs to Outputs	3.3	2.0	6.0	11.5	1.0	14.0	1.5	12.5	ns	2-5
		5.0	1.5	4.5	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay Inputs to Outputs	3.3	2.0	6.5	11.5	1.0	14.0	1.5	12.5	ns	2-5
		5.0	1.5	4.5	8.5	1.0	10.0	1.0	9.0		

*Voltage Range 3.3V is 3.3V ±0.3V

Voltage Range 5.0V is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC109 • 54ACT/74ACT109
Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

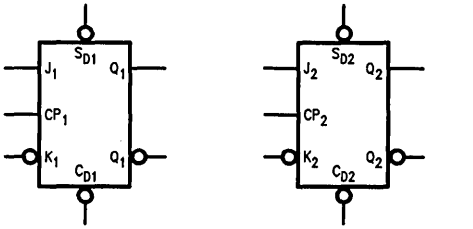
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Outputs source/sink 24 mA
- 'ACT109 has TTL-compatible inputs

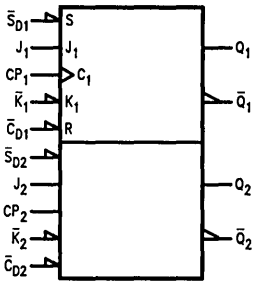
Ordering Code: See Section 5

Logic Symbols



TL/F/9923–1 TL/F/9923–2

IEEE/IEC

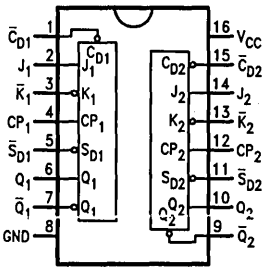


TL/F/9923–7

Pin Names	Description
$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

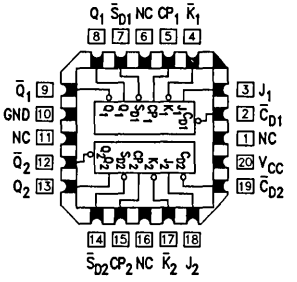
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9923–3

Pin Assignment for LCC



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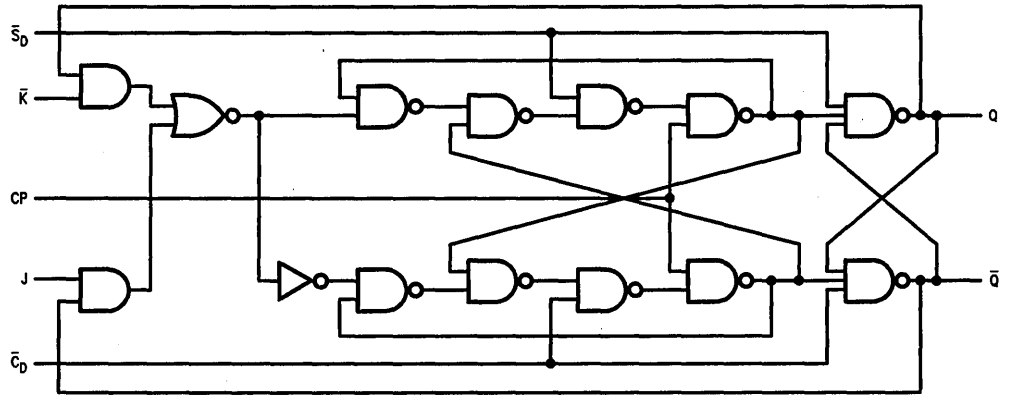
Truth Table (each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↗	L	L	L	H
H	H	↗	H	L	Toggle	
H	H	↗	L	H	Q_0	$\overline{Q}_0$
H	H	↗	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
↗ = LOW-to-HIGH Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	125	150		65		100		MHz	2-3
		5.0	150	175		95		125			
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	4.0	8.0	13.5	1.0	17.5	3.5	16.0	ns	2-6
		5.0	2.5	6.0	10.0	1.0	12.0	2.0	10.5		
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	3.0	8.0	14.0	1.0	13.5	3.0	14.5	ns	2-6
		5.0	2.0	6.0	10.0	1.0	10.0	1.5	10.5		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.0	8.0	12.0	1.0	13.0	2.5	13.0	ns	2-6
		5.0	2.5	6.0	9.0	1.0	9.5	2.0	10.0		
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.0	10.0	12.0	1.0	14.0	3.0	13.5	ns	2-6
		5.0	2.0	7.5	9.5	1.0	10.5	2.0	10.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3	3.5	6.5	8.0	7.5	ns	2-9
		5.0	2.0	4.5	5.5	5.0		
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3	−1.5	0	0	0	ns	2-9
		5.0	−0.5	0.5	0.5	0.5		
t_w	Pulse Width $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3	2.0	4.0	8.0	4.5	ns	2-6
		5.0	2.0	3.5	5.5	3.5		
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	3.3	−2.5	0	0.5	0	ns	2-9
		5.0	−1.5	0	0.5	0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz	2-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.0	11.0	1.0	14.0	3.5	13.0	ns	2-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	1.0	12.0	2.5	11.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	6.0	10.0	1.0	12.5	2.0	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	2.0	ns	2-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	7.0	6.0	ns	2-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	−2.5	0	0.5	0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54AC/74AC112 • 54ACT/74ACT112
Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT112 contain two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

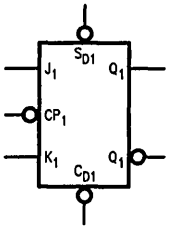
Asynchronous Inputs:

LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

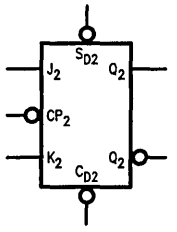
Features

- 'ACT112 has TTL-compatible inputs

Logic Symbols

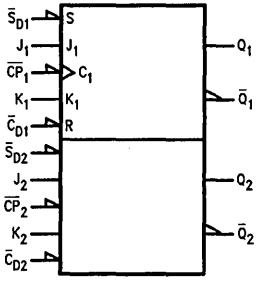


TL/F/9924–1



TL/F/9924–2

IEEE/IEC

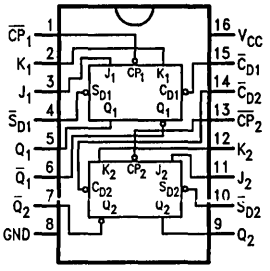


TL/F/9924–4

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs (Active LOW)
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

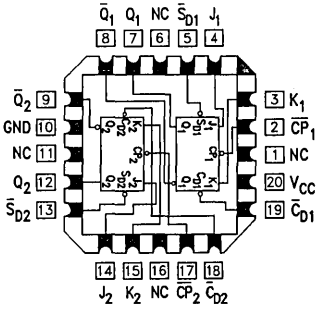
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9924–3

Pin Assigment for LCC



TL/F/9924–5

National Semiconductor

54AC/74AC138 • 54ACT/74ACT138
1-of-8 Decoder/Demultiplexer

General Description

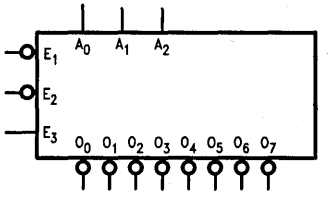
The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

Features

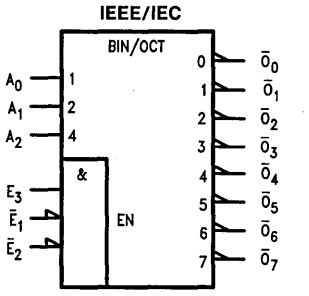
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT138 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol



TL/F/9925–1

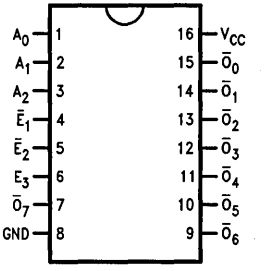


TL/F/9925–7

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

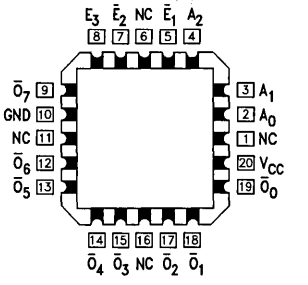
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9925–2

Pin Assignment for LCC



TL/F/9925–3

Functional Description

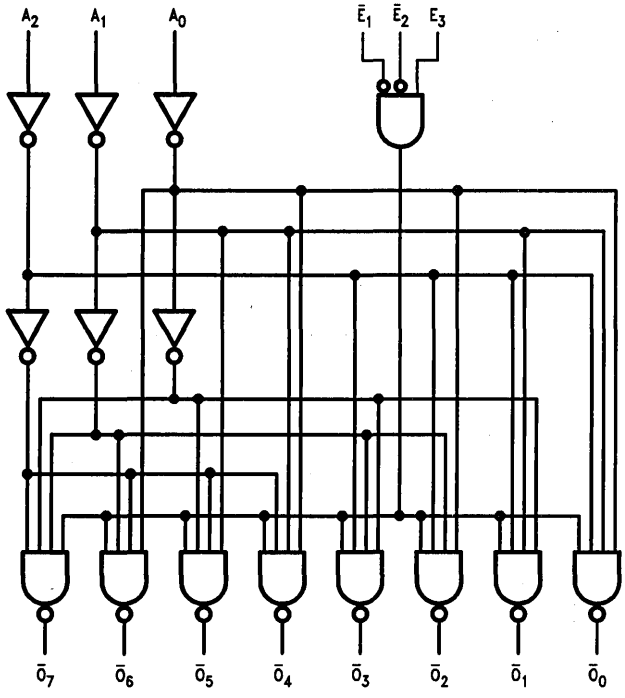
The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The 'AC/'ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/'ACT138 devices and one inverter (see *Figure 1*). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

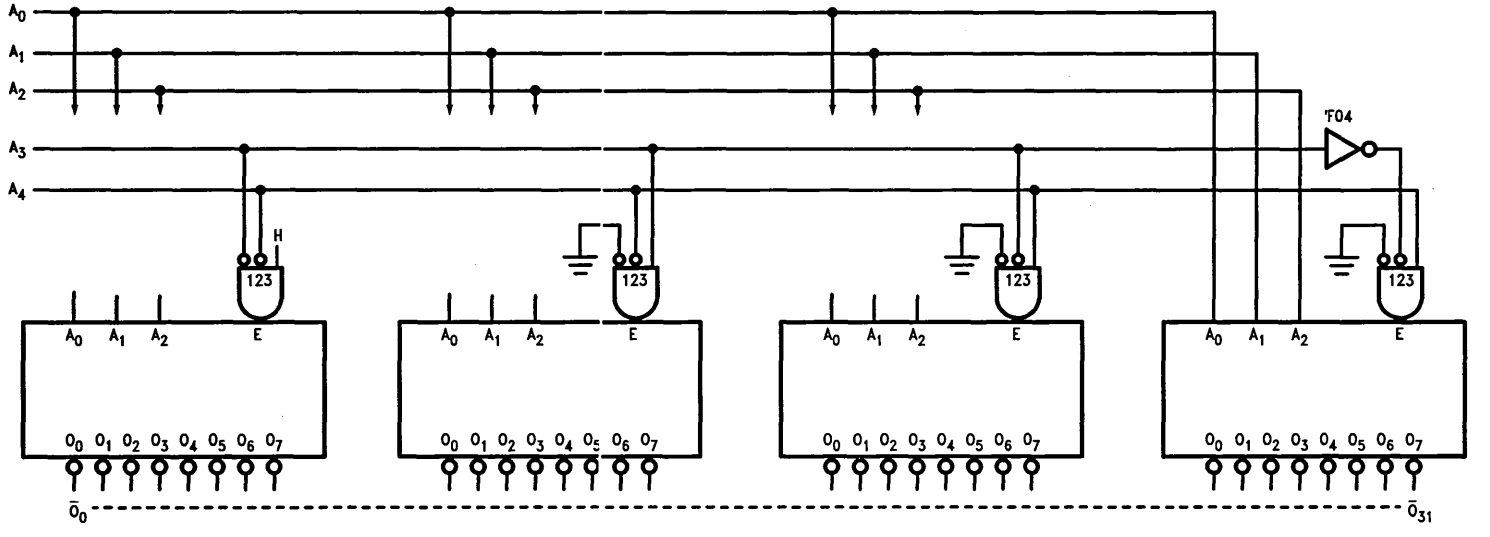
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9925–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



TL/F/9925–5

FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	16.0	1.5	15.0	ns	2-6
		5.0	1.5	6.5	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.0	12.5	1.0	15.0	1.5	14.0	ns	2-6
		5.0	1.5	6.0	9.0	1.0	11.5	1.5	10.5		
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	11.0	15.0	1.0	16.5	1.5	16.0	ns	2-6
		5.0	1.5	8.0	11.0	1.0	13.0	1.5	12.0		
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	9.5	13.5	1.0	15.5	1.5	15.0	ns	2-6
		5.0	1.5	7.0	9.5	1.0	12.0	1.5	10.5		
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	11.0	15.5	1.0	17.0	1.5	16.5	ns	2-6
		5.0	1.5	8.0	11.0	1.0	13.5	1.5	12.5		
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	15.0	1.5	14.0	ns	2-6
		5.0	1.5	6.0	8.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.5	10.5	1.0	12.5	1.5	11.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.5	8.0	11.5	1.0	13.5	2.0	12.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.0	7.5	11.5	1.0	12.5	2.0	12.5	ns	2-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}n$	5.0	2.5	8.0	12.0	1.0	14.0	2.0	13.0	ns	2-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}n$	5.0	2.0	6.5	10.5	1.0	12.0	1.5	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC139 • 54ACT/74ACT139
Dual 1-of-4 Decoder/Demultiplexer

General Description

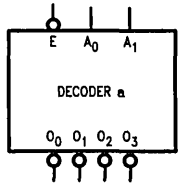
The 'AC/'ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC/'ACT139 can be used as a function generator providing all four minterms of two variables.

Features

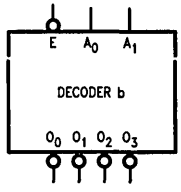
- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT139 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

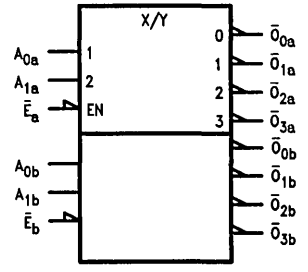


TL/F/9926-8



TL/F/9926-1

IEEE/IEC

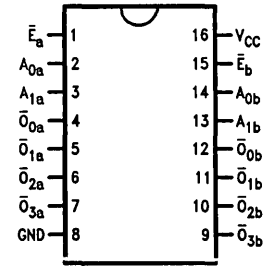


TL/F/9926-2

Pin Names	Description
A_0, A_1	Address Inputs
$\bar{E}$	Enable Inputs
$\bar{O}_0$–$\bar{O}_3$	Outputs

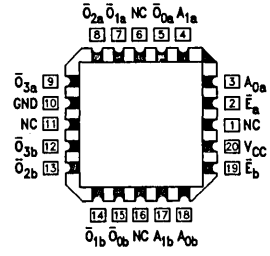
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9926-3

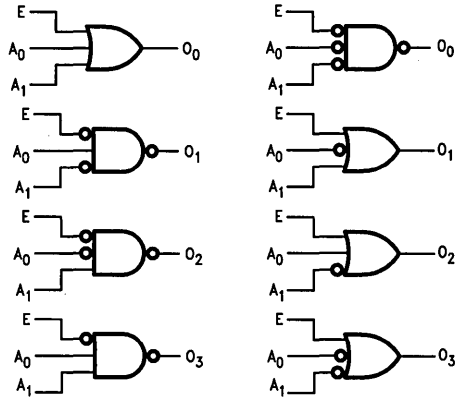
Pin Assignment for LCC



TL/F/9926-4

Functional Description

The 'AC/'ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0–A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active-LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC/'ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure a*, and thereby reducing the number of packages required in a logic network.



TL/F/9926–6

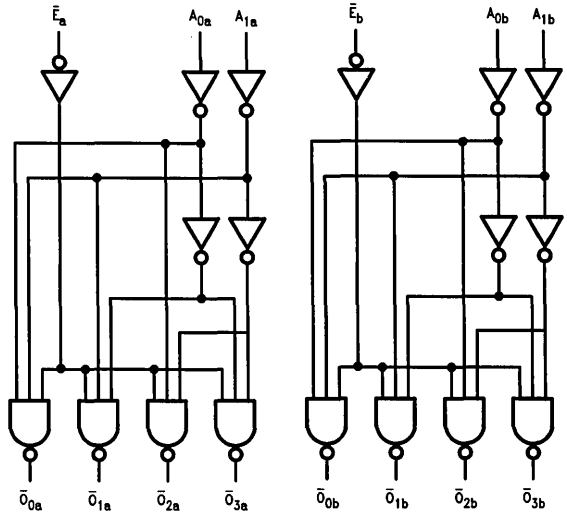
FIGURE a. Gate Functions (Each Half)

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9926–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		−12 mA
		4.5		3.86	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50		12 mA
		4.5		0.36	0.50	V	I_{OL} 24 mA
		5.5		0.36	0.50		24 mA

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	4.0	8.0	11.5	1.0	14.5	3.5	13.0	ns	2-6
		5.0	3.0	6.5	8.5	1.0	11.0	2.5	9.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	3.0	7.0	10.0	1.0	12.5	2.5	11.0	ns	2-6
		5.0	2.5	5.5	7.5	1.0	10.0	2.0	8.5		
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	4.5	9.5	12.0	1.0	14.5	3.5	13.0	ns	2-6
		5.0	3.5	7.0	8.5	1.0	11.0	3.0	10.0		
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	4.0	8.0	10.0	1.0	12.5	3.0	11.0	ns	2-6
		5.0	2.5	6.0	7.5	1.0	10.0	2.5	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.0	8.5	1.0	12.0	1.5	9.5	ns	2-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.0	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	2.5	7.0	10.0	1.0	12.5	2.0	11.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	2.0	7.0	9.5	1.0	12.0	1.5	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC151 • 54ACT/74ACT151
8-Input Multiplexer

General Description

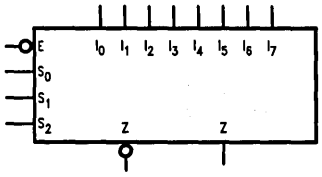
The 'AC/'ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'AC/'ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Outputs source/sink 24 mA
- 'ACT151 has TTL-compatible inputs

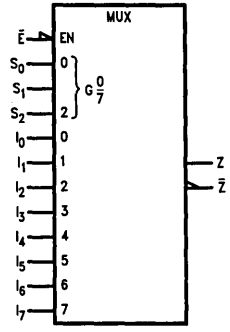
Ordering Code: See Section 5

Logic Symbol



TL/F/9927–1

IEEE/IEC

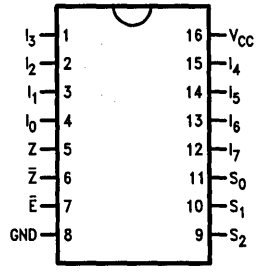


TL/F/9927–6

Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\bar{E}$	Enable Input
Z	Data Output
$\bar{Z}$	Inverted Data Output

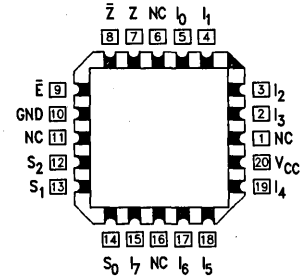
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9927–2

Pin Assignment for LCC



TL/F/9927–3

Truth Table

Inputs				Outputs	
$\bar{E}$	S_2	S_1	S_0	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	I_0
L	L	L	H	$\bar{I}_1$	I_1
L	L	H	L	$\bar{I}_2$	I_2
L	L	H	H	$\bar{I}_3$	I_3
L	H	L	L	$\bar{I}_4$	I_4
L	H	L	H	$\bar{I}_5$	I_5
L	H	H	L	$\bar{I}_6$	I_6
L	H	H	H	$\bar{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

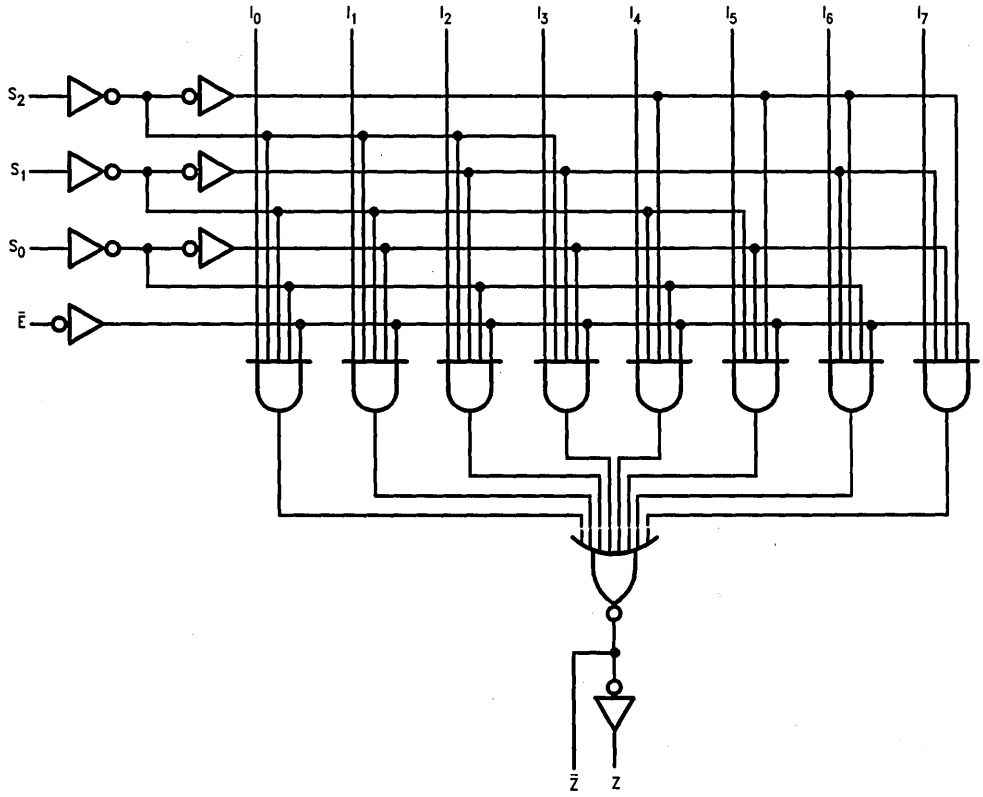
Functional Description

The 'AC/'ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'AC/'ACT151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'AC/'ACT151 can provide any logic function of four variables and its complement.

Logic Diagram



TL/F/9927–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	3.0	11.5	18.0	1.0	22.0	3.0	20.0	ns	2-6
		5.0	2.5	8.5	13.0	1.0	15.5	2.0	15.0		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	2.5	12.0	18.0	1.0	22.0	2.5	20.0	ns	2-6
		5.0	2.0	8.5	13.0	1.0	15.5	1.5	15.0		
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	2.5	8.0	13.0	1.0	15.5	2.0	14.0	ns	2-6
		5.0	2.0	6.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	1.5	8.5	13.0	1.0	15.5	1.5	14.0	ns	2-6
		5.0	1.5	6.5	10.0	1.0	12.0	1.5	11.0		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	14.0	1.0	16.0	2.0	15.5	ns	2-5
		5.0	1.5	7.0	10.5	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	2.5	9.5	15.0	1.0	18.0	2.0	16.0	ns	2-5
		5.0	1.5	7.0	11.0	1.0	13.0	1.5	12.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z	5.0	3.5	12.5	15.5	1.0	19.5	3.0	17.0	ns	2-6
t_{PHL}	Propagation Delay S_n to Z	5.0	3.5	12.5	15.5	1.0	20.0	3.0	16.5	ns	2-6
t_{PLH}	Propagation Delay S_n to $\overline{Z}$	5.0	3.5	12.5	15.0	1.0	19.5	3.0	16.5	ns	2-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}$	5.0	4.0	12.5	16.5	1.0	20.0	3.5	18.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z	5.0	2.5	10.0	9.5	1.0	12.0	2.5	10.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0	2.5	10.5	9.0	1.0	12.5	2.5	10.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	2.5	10.0	8.5	1.0	12.0	2.5	9.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	3.0	10.5	10.0	1.0	12.5	2.5	10.5	ns	2-6
t_{PLH}	Propagation Delay I_n to Z	5.0	3.5	11.0	11.5	1.0	15.0	3.0	12.5	ns	2-6
t_{PHL}	Propagation Delay I_n to Z	5.0	3.5	11.0	12.0	1.0	16.0	3.0	13.5	ns	2-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}$	5.0	3.5	11.0	12.0	1.0	15.0	3.0	13.0	ns	2-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}$	5.0	4.0	11.0	12.5	1.0	16.0	3.0	14.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC153 • 54ACT/74ACT153
Dual 4-Input Multiplexer

General Description

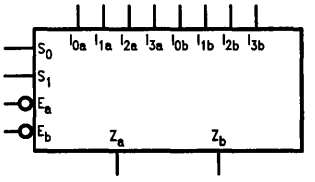
The 'AC/'ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'AC/'ACT153 can act as a function generator and generate any two functions of three variables.

Features

- Outputs source/sink 24 mA
- 'ACT153 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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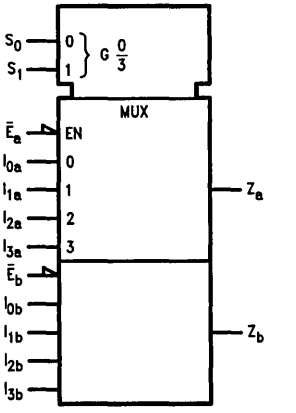
IEEE/IEC



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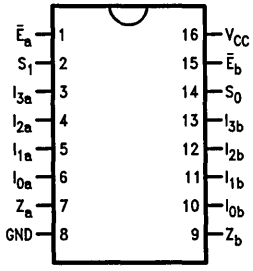
Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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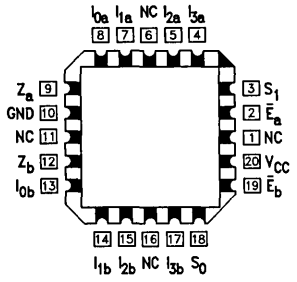
Pin Assignment for LCC



TL/F/9928–4

Functional Description

The 'AC/'ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs indepedently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'AC/'ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet S_0 + I_{3a} \bullet S_1 \bullet S_0)$$

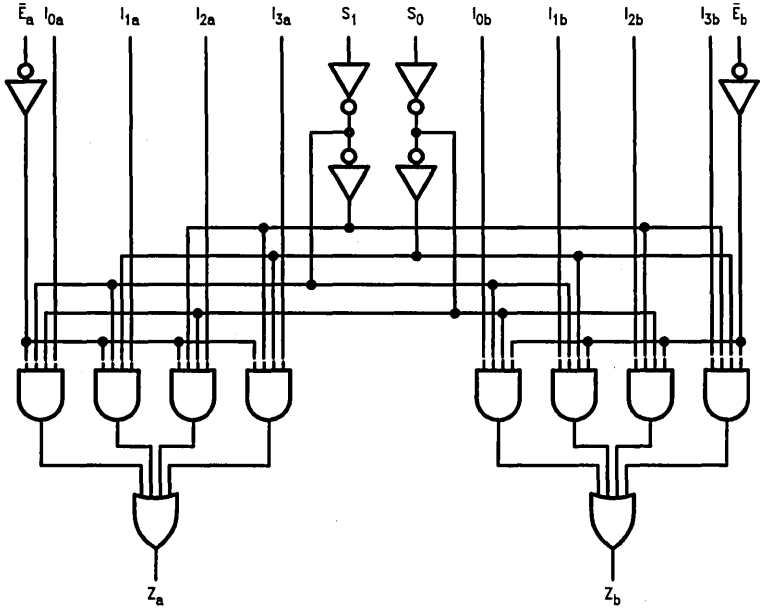
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet S_0 + I_{3b} \bullet S_1 \bullet S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9928–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	2.5	9.5	15.0	1.0	19.5	2.5	17.5	ns	2-6
		5.0	2.0	6.5	11.0	1.0	14.0	2.0	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	3.0	8.5	14.5	1.0	18.0	2.5	16.5	ns	2-6
		5.0	2.5	6.5	11.0	1.0	13.5	2.0	12.0		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	2.5	8.0	13.5	1.0	16.5	2.0	16.0	ns	2-6
		5.0	1.5	5.5	9.5	1.0	12.5	1.5	11.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	2.5	7.0	11.0	1.0	14.0	2.0	12.5	ns	2-6
		5.0	2.0	5.0	8.0	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	2.5	7.5	12.5	1.0	16.0	2.0	14.5	ns	2-5
		5.0	1.5	5.5	9.0	1.0	11.5	1.5	10.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	7.0	11.5	1.0	14.5	1.5	13.0	ns	2-5
		5.0	1.5	5.0	8.5	1.0	10.5	1.5	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5	1.0	15.0	2.0	13.5	ns	2-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5	1.0	14.5	2.5	13.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	2.0	6.5	10.5	1.0	13.5	2.0	12.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	3.0	6.0	9.5	1.0	11.5	2.5	11.0	ns	2-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	9.5	1.0	12.5	2.0	11.0	ns	2-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	2.0	5.5	9.5	1.0	12.0	2.0	11.0	ns	2-5

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC157 • 54ACT/74ACT157
Quad 2-Input Multiplexer

General Description

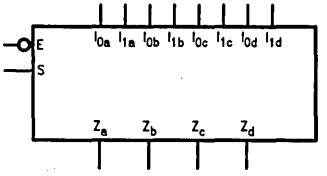
The 'AC/'ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

Features

- Outputs source/sink 24 mA
- 'ACT157 has TTL-compatible inputs

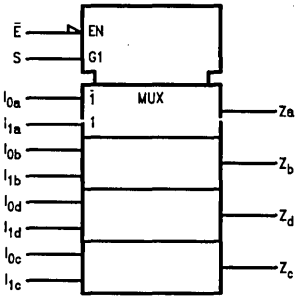
Ordering Code: See Section 5

Logic Symbols



TL/F/9929–1

IEEE/IEC



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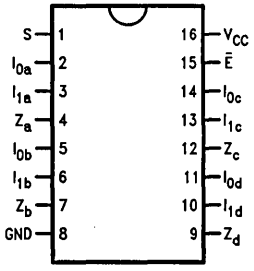
Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\bar{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

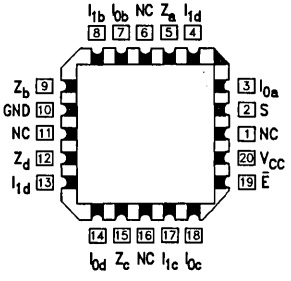
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9929–3

Pin Assignment for LCC



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Functional Description

The 'AC/'ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/'ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

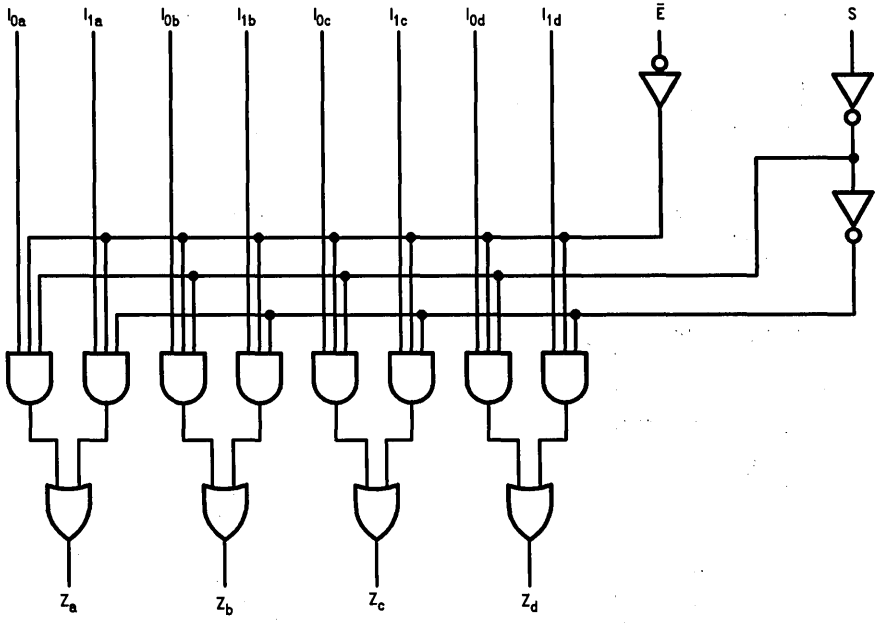
A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	2-6
		5.0	1.5	5.5	9.0	1.0	12.0	1.5	10.0		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	2-6
		5.0	1.5	5.0	8.5	1.0	11.5	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	2-6
		5.0	1.5	5.5	9.0	1.0	12.0	1.5	10.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	9.0	1.0	11.5	1.0	9.5		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	11.0	1.0	9.0	ns	2-5
		5.0	1.5	4.0	6.5	1.0	9.0	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.0	1.0	11.0	1.0	9.0	ns	2-5
		5.0	1.5	4.0	6.5	1.0	9.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	5.0	2.0	5.5	9.0	1.0	11.5	1.5	10.0	ns	2-6
t_{PHL}	Propagation Delay S to Z_n	5.0	2.0	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.5	6.0	10.0	1.0	12.0	1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.0	ns	2-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.5	4.0	7.0	1.0	8.5	1.0	8.5	ns	2-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.5	4.5	7.5	1.0	9.0	1.0	8.5	ns	2-5

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC158 • 54ACT/74ACT158
Quad 2-Input Multiplexer

General Description

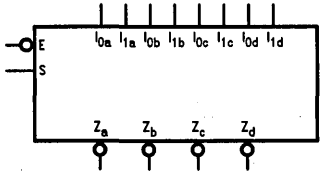
The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

Features

- Outputs source/sink 24 mA
- 'ACT158 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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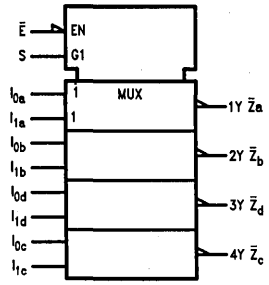
IEE/IEC

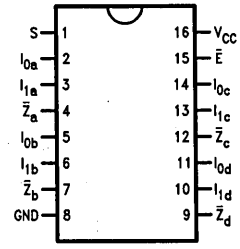


TL/F/9930–2

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$–$\overline{Z}_d$	Inverted Outputs

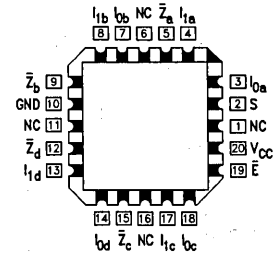
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9930–3

Pin Assignment for LCC



TL/F/9930–4

Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

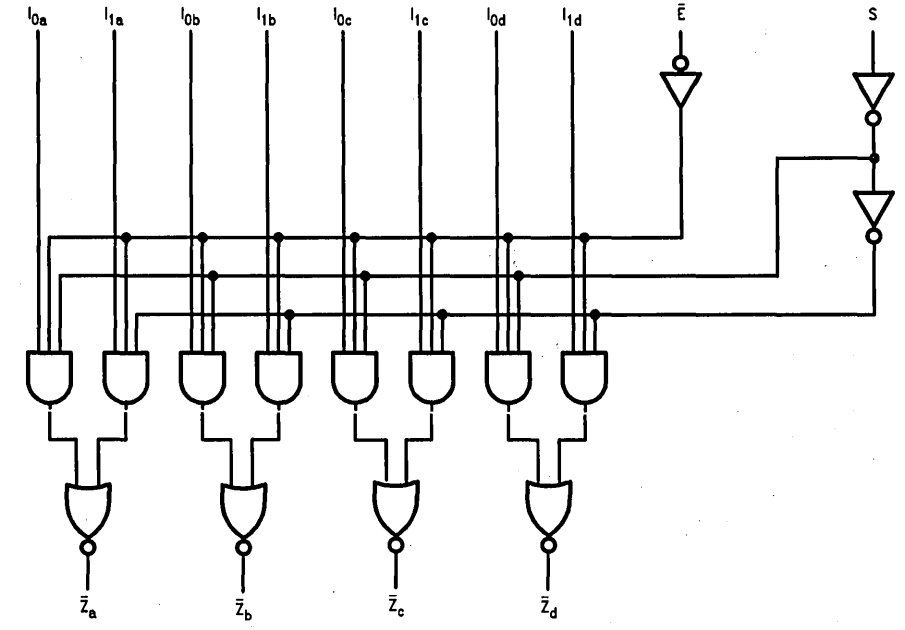
A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9930–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	1.5	7.0	11.5	1.0	14.0	1.5	12.5	ns	2-6
		5.0	1.5	5.5	9.0	1.0	11.0	1.0	9.5		
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	1.5	7.0	11.5	1.0	14.0	1.5	12.5	ns	2-6
		5.0	1.5	5.5	9.0	1.0	11.0	1.5	10.0		
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.5	7.5	12.0	1.0	15.0	1.5	13.0	ns	2-6
		5.0	1.5	6.0	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.5	7.0	11.0	1.0	14.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.5	5.5	9.0	1.0	11.0	1.5	10.0	ns	2-5
		5.0	1.5	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.5	5.0	8.0	1.0	10.0	1.0	8.5	ns	2-5
		5.0	1.5	4.0	6.5	1.0	7.5	1.0	6.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	2.5	6.0	9.5	1.0	12.0	2.0	11.0	ns	2-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.5	5.5	9.0	1.0	11.5	1.5	10.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.5	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.5	4.0	6.5	1.0	8.0	1.0	7.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC161 • 54ACT/74ACT161
Synchronous Presettable Binary Counter

General Description

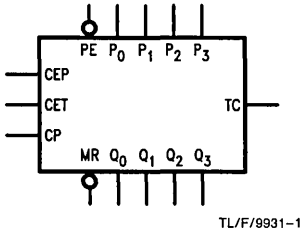
The 'AC/'ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT161 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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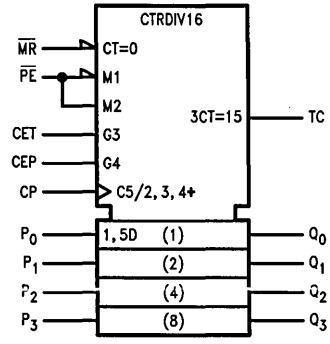
IEEE/IEC



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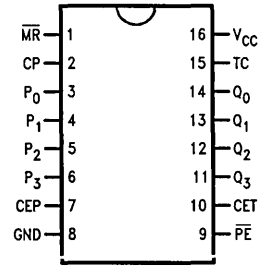
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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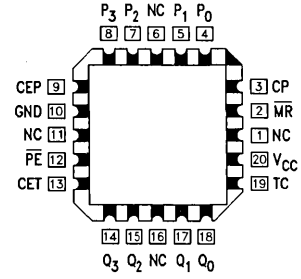
Pin Assignment for LCC



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Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	Asynchronous Master Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Inputs
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The 'AC/'ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs—Master Reset, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 use D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

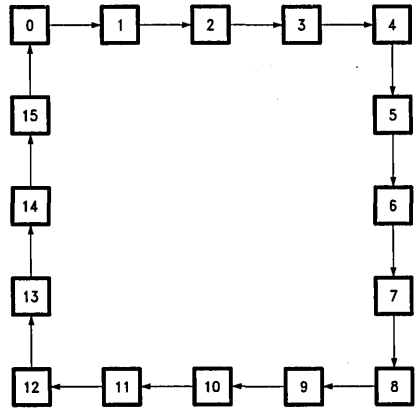
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
X	X	X	Reset (Clear)
L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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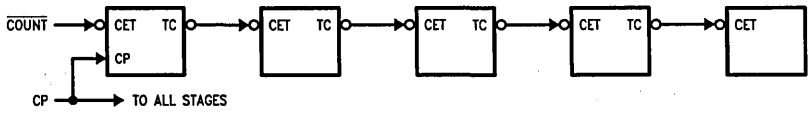

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FIGURE 1. Multistage Counter with Ripple Carry

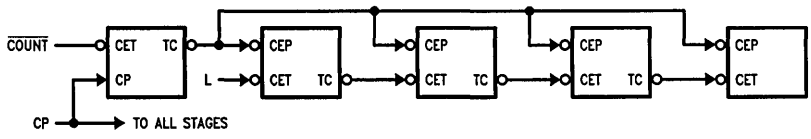

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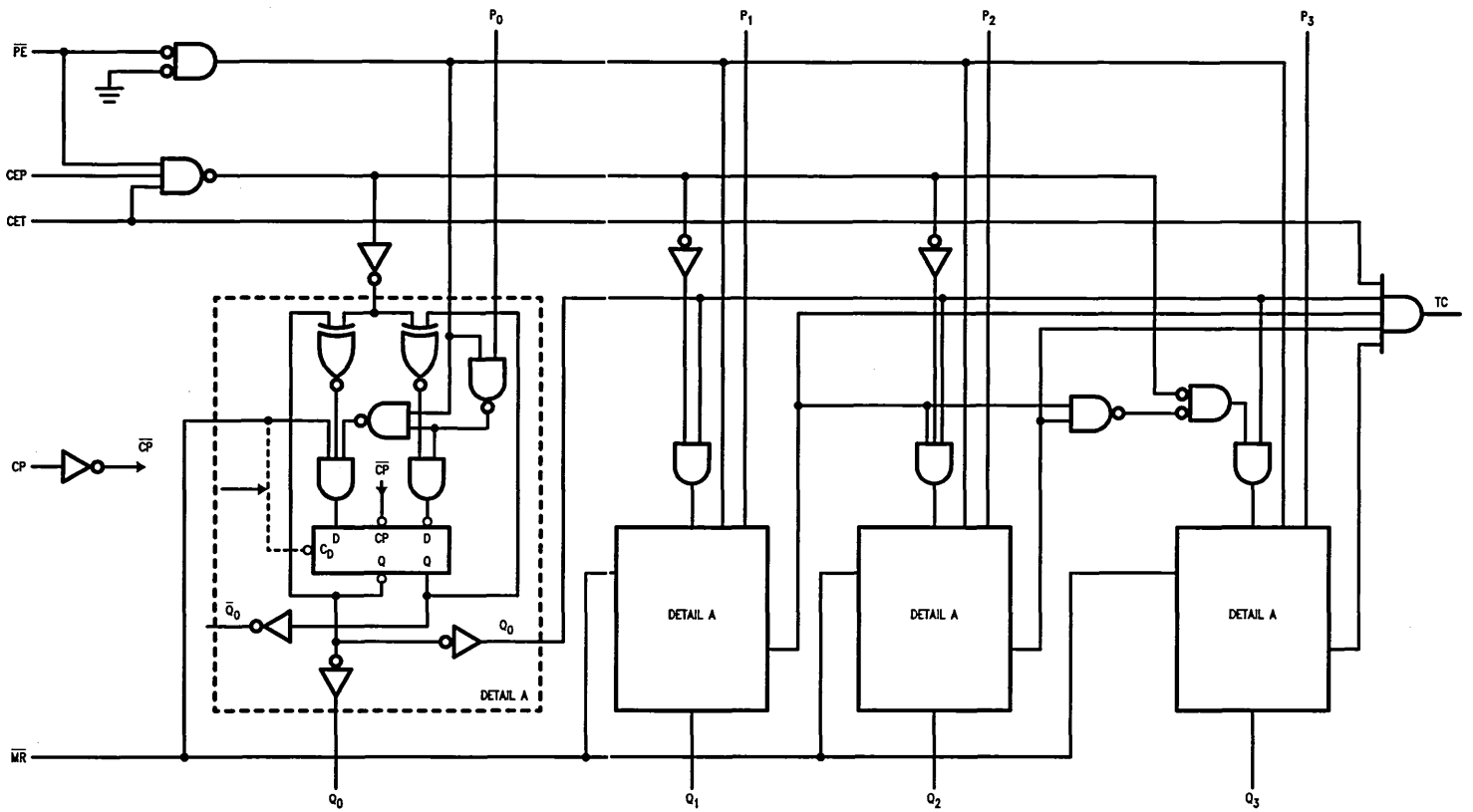
FIGURE 2. Multistage Counter with Lookahead Carry

Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		I_{OH} −24 mA
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5		I_{OL} 24 mA
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167		55 80		60 95		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12 9.0	1.0 1.0	15.0 11.0	1.5 1.0	13.5 9.5	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12 9.5	1.0 1.0	15.0 11.0	1.5 1.5	13 10	ns	2-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9 6	15 10.5	1.0 1.0	18.5 13.0	2.5 1.5	16.5 11.5	ns	2-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14 11	1.0 1.0	17.5 13.0	2.5 2.0	15.5 11.5	ns	2-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.0 1.0	13.0 8.5	1.5 1.0	11 7.5	ns	2-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5	11 8.5	1.0 1.0	14.5 11.0	2.0 1.5	12.5 9.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.0 1.5	6.5 5.5	12 9.5	1.0 1.0	14.5 10.5	1.5 1.5	13.5 10	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0	3.5 2.5	10 8.5	15 13	1.0 1.0	18.5 14.0	3.0 2.5	17.5 13.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	16 10.5	ns	2-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −4.0	−1 0	0.5 1.5	−0.5 0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	6.5 4.0	11.5 7.5	15.0 10.5	14 8.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−6.0 −3.5	0 0.5	−1.0 0.0	0 1	ns	2-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.5 5.5	7 5	ns	2-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−3.5 −2	0 0	2.0 2.0	0 0.5	ns	2-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	5.0 5.0	4 3	ns	2-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	5.0 5.0	7.5 6.0	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP		−2 −1	−0.5 0	1.5 2.0	0 0.5	ns	2-9

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125				100		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	10.0			1.5	13.5	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	8.0	10.0			1.5	12.5	ns	2-6
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	11.0	13.5			1.5	16.5	ns	2-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	11.0	13.0			1.5	15.5	ns	2-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	7.5	9.0			1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	8.0	10.0			1.5	13.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	8.0	9.5			1.5	12.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	2.5	10.0	11.5			2.0	14.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	7.0	8.5		11.5	ns	2-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−3.0	−1		0.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	6.0	7.5		10.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−3.5	0		0.5	ns	2-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	4.0	5.5		9.5	ns	2-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−2.0	0		0.5	ns	2-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	4.5		6.5	ns	2-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	4.5		6.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	4.5		6.5	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0		0.5	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC163 • 54ACT/74ACT163
Synchronous Presettable Binary Counter

General Description

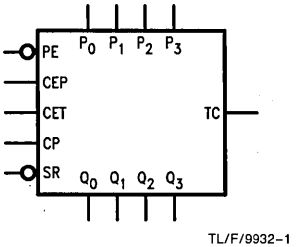
The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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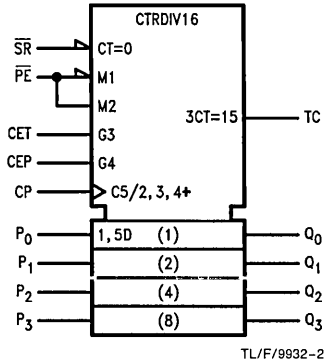
IEEE/IEC



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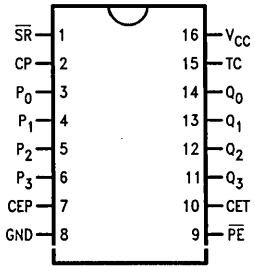
Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{SR}$	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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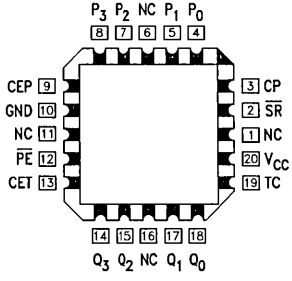
Pin Assignment for LCC



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Functional Description

The 'AC/'ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs—Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{SR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT163 uses D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

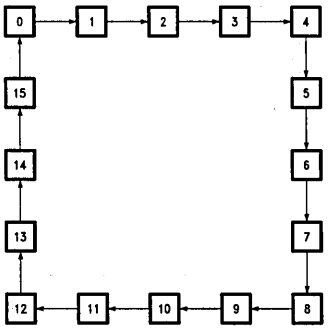
$\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CET}$

Mode Select Table

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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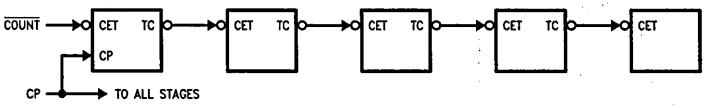

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FIGURE 1

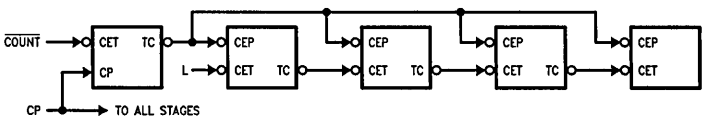

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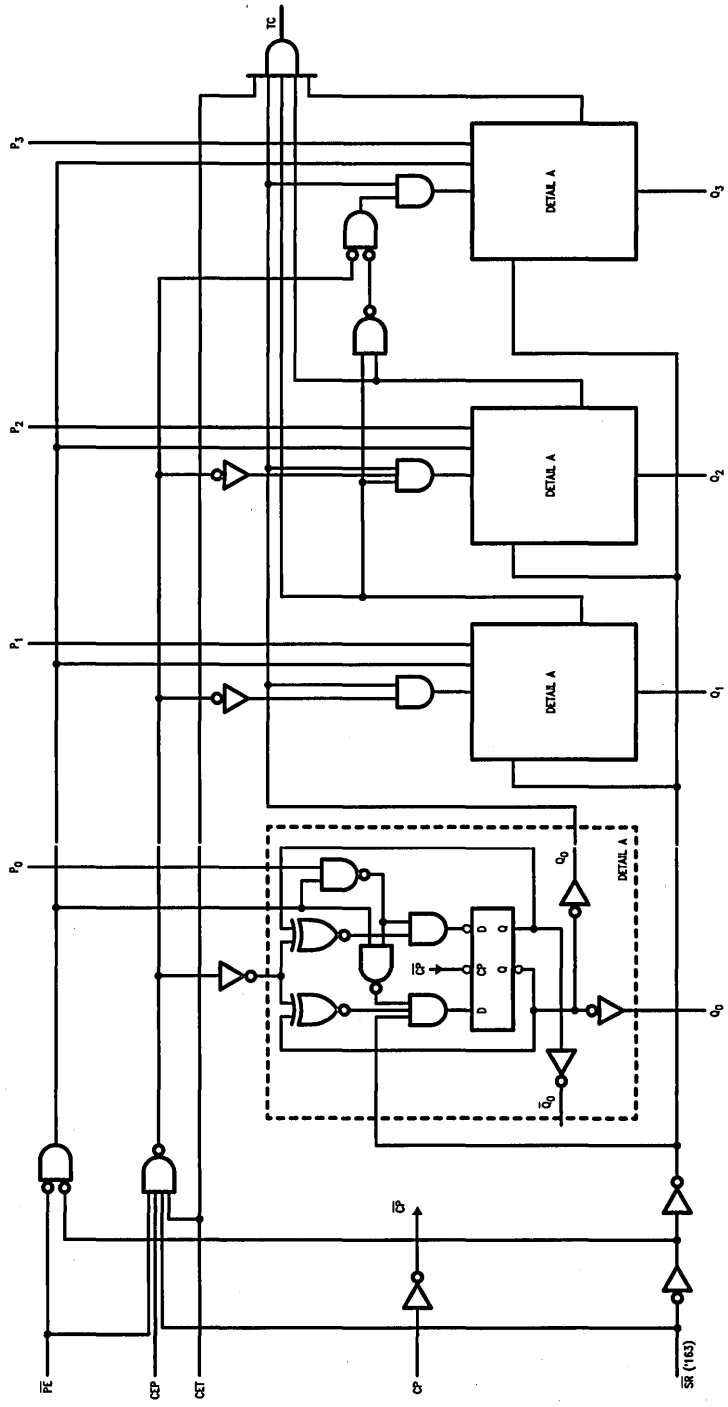
FIGURE 2

Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	70 110	95 140		55 90		60 95		MHz	2-3
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.0 1.0	13.5 9.5	1.5 1.0	13.5 9.5	ns	2-6
t_{PHL}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.0 1.0	12.5 9.5	1.5 1.5	13.0 10.0	ns	2-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	1.0 1.0	16.5 11.0	2.5 1.5	16.5 11.5	ns	2-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	1.0 1.0	15.0 11.0	2.5 2.0	15.5 11.5	ns	2-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.0 1.0	11.0 7.5	1.5 1.0	11.0 7.5	ns	2-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	1.0 1.0	12.0 9.0	2.0 1.5	12.5 9.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5	17.0 11.0	16.0 10.5	ns	2-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	−0.5 0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14.0 9.5	17.0 12.0	16.5 11.0	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	−0.5 0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	16.0 9.5	14.0 8.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	−0.5 0	ns	2-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	8.0 5.5	7.0 5.0	ns	2-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	0 0.5	ns	2-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	5.0 5.0	4.0 3.0	ns	2-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	140				105		MHz	2-3
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0			1.5	11.0	ns	2-6
t_{PHL}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0			1.5	12.0	ns	2-6
t_{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5			2.0	13.5	ns	2-6
t_{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5			2.0	15.0	ns	2-6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0			1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0			2.0	11.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0		12.0	ns	2-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5		0.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0		11.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		10.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		0	ns	2-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	2-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0.5	ns	2-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.5		3.5	ns	2-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		3.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

National Semiconductor

ADVANCE INFORMATION

54AC/74AC164 • 54ACT/74ACT164
Serial-In, Parallel-Out Shift Register

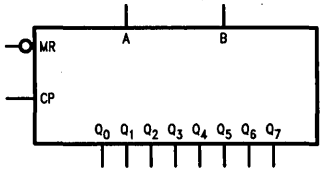
General Description

The 'AC/'ACT164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

Features

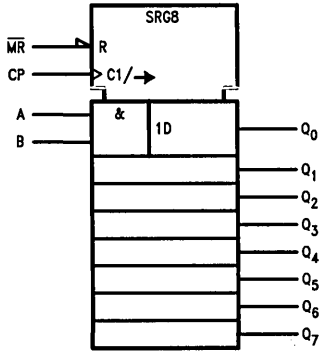
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 'ACT164 has TTL-compatible inputs

Logic Symbols



TL/F/9933–1

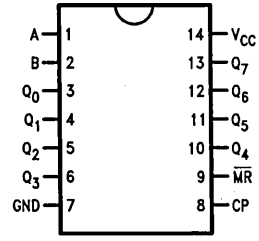
IEEE/IEC



TL/F/9933–4

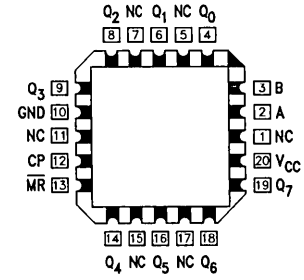
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9933–2

Pin Assignment for LCC



TL/F/9933–3

Pin Names	Description
A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0–Q_7	Outputs

National Semiconductor

54AC/74AC169
4-Stage Synchronous Bidirectional Counter

General Description

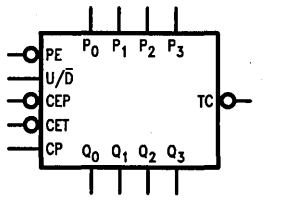
The 'AC169 is fully synchronous 4-stage up/down counter. The 'AC169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

Features

- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA

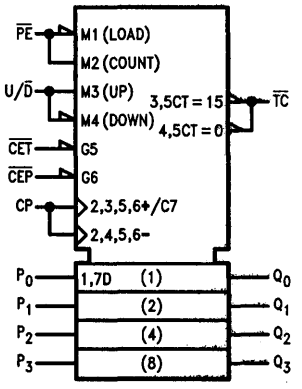
Ordering Code: See Section 5

Logic Symbol



TL/F/9934-1

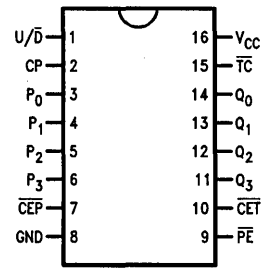
IEEE/IEIC



TL/F/9934-2

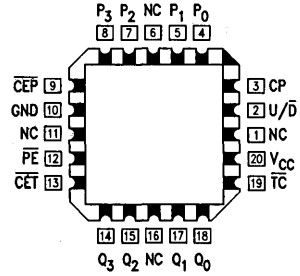
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9934-3

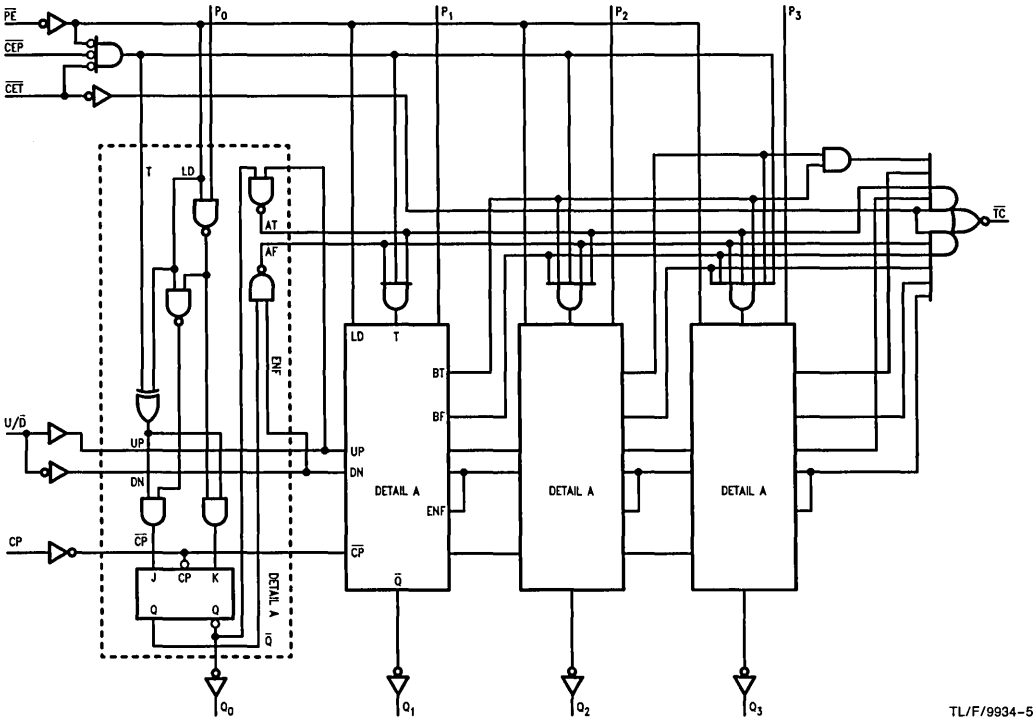
Pin Assignment for LCC



TL/F/9934-4

Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

Logic Diagram



TL/F/9934-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the $U/\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$

2) Up: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 Q_3 \cdot (\text{Up}) \cdot \overline{CET}$

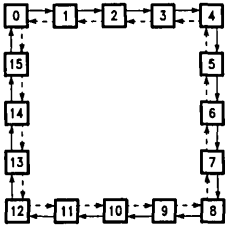
3) Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\text{Down}) \cdot \overline{CET}$

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams



TL/F/9934-6

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH}, I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH}, I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	5.5		50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5		−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC169 T_A = +25°C, C_L = 50 pF			54AC169 T_A = −55°C to +125°C, C_L = 50 pF		74AC169 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	75	118		55		65		MHz	2-3
		5.0	100	154		75		90			
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3	2.5	9.5	13.0	1.0	15.0	2.0	14.5	ns	2-6
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3	2.5	10.5	14.5	1.0	16.5	2.0	16.0	ns	2-6
		5.0	1.5	7.5	11.0	1.0	13.0	1.5	12.0		
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3	4.5	13.5	18.0	1.0	22.0	3.5	22.0	ns	2-6
		5.0	3.0	9.5	13.0	1.0	16.0	2.0	14.0		
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3	3.5	13.5	18.0	1.0	22.0	3.0	20.5	ns	2-6
		5.0	2.5	9.5	13.0	1.0	16.0	2.0	14.5		
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3	3.5	11.0	15.0	1.0	18.5	3.0	16.5	ns	2-6
		5.0	3.0	8.0	10.5	1.0	13.0	2.5	12.0		
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3	3.0	9.5	12.5	1.0	16.0	2.5	14.5	ns	2-6
		5.0	2.0	7.0	9.0	1.0	11.0	1.5	10.0		
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3	3.5	11.0	15.0	1.0	18.5	3.0	17.0	ns	2-6
		5.0	2.5	8.0	10.5	1.0	13.0	2.0	12.0		
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3	2.5	10.0	13.5	1.0	16.5	2.0	15.5	ns	2-6
		5.0	1.5	7.0	9.5	1.0	12.0	1.5	10.5		

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC169 $T_A = +25°C$ $C_L = 50$ pF		54AC169 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC169 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	7.0 4.5	5.0 2.5	ns	2-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5	0.5 1.5	2.0 2.5	0.5 1.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	13.5 9.0	12.5 8.0	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0	0 0.5	0.5 2.5	0 1.0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10.0 6.5	13.5 9.5	12.0 8.0	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0	0 0.5	0.5 2.5	0 1.0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	8.5 6.5	6.5 4.0	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5	0 0.5	0.5 2.0	0 0.5	ns	2-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10.0 6.5	13.0 9.0	11.5 7.5	ns	2-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0	0 0.5	0.5 2.0	0 0.5	ns	2-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	5.0 5.0	4.0 3.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC174 • 54ACT/74ACT174
Hex D Flip-Flop with Master Reset

General Description

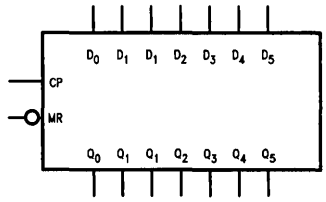
The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Outputs source/sink 24 mA
- 'ACT174 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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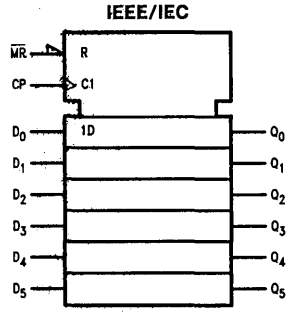
IEEE/IEC

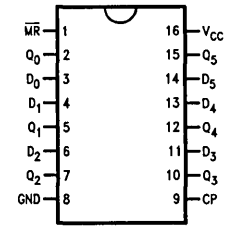


TL/F/9935-2

Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

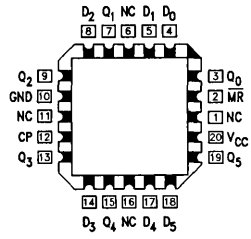
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9935-3

Pin Assignment for LCC



TL/F/9935-4

Functional Description

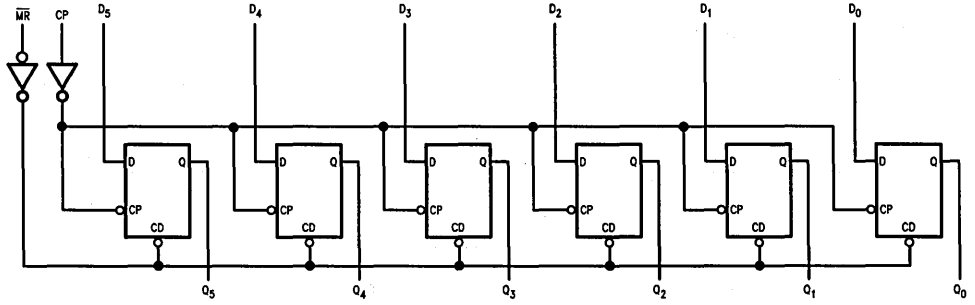
The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9935–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		65 90		70 100		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.0 1.0	14.0 10.5	1.5 1.0	12.5 9.5	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5	8.5 6.0	11.0 8.0	1.0 1.0	13.0 10.0	1.5 1.0	12.0 9.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	1.0 1.0	13.5 11.0	2.0 1.5	12.5 10.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.5 5.5	7.0 5.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	3.0 3.0	ns	2-9
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	2-6
t_w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	2.5 2.0	3.0 2.0	2.5 2.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	165	200		95		140		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.5	7.0	10.5	1.0	13.0	1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	6.5	9.5	1.0	12.0	1.5	11.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	1.5	3.0	1.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	2.0	2.0	2.0	ns	2-9
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	1.5	3.0	5.0	3.5	ns	2-6
t_w	CP Pulse Width, HIGH OR LOW	5.0	1.5	3.0	5.0	3.5	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0	0.5	1.0	0.5	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	85.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC175 • 54ACT/74ACT175 Quad D Flip-Flop

General Description

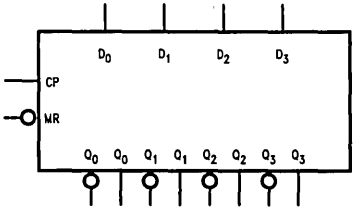
The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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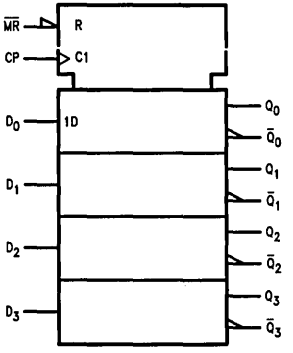
IEEE/IEC



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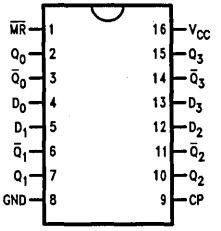
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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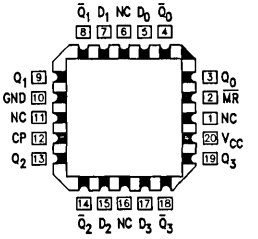
Pin Assignment for LCC



TL/F/9936-4

Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

Functional Description

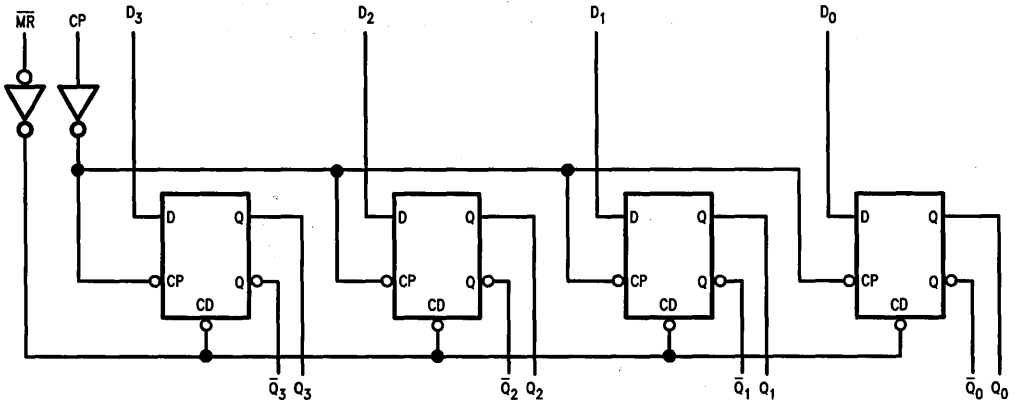
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



TL/F/9936–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT $-40°C$ to $+85°C$
- 54AC/ACT $-55°C$ to $+125°C$

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -12 mA
		4.5		3.86	3.7	3.76		I_{OH} -24 mA
		5.5		4.86	4.7	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	149 187	214 244		95 95		139 187		MHz	2-3
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0	2.0 1.5	9.5 7.0	12.0 9.0	1.0 1.0	15.0 11.5	2.0 1.0	13.5 9.5	ns	2-6
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0	2.5 1.5	8.5 6.0	13.0 9.5	1.0 1.0	14.5 10.5	2.0 1.5	14.5 10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	3.0 2.0	7.5 5.5	12.5 9.0	1.0 1.0	13.5 10.5	2.5 1.5	13.5 10.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3 5.0	3.0 2.0	8.5 6.0	11.0 8.5	1.0 1.0	15.0 11.0	2.5 1.5	12.5 9.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0	4.5 3.0	5.0 3.5	4.5 3.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 1.0	1.0 1.0	2.0 2.5	1.0 1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0	4.5 3.5	6.0 5.0	4.5 3.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	5.5 4.0	4.5 3.5	5.5 5.0	5.0 3.5	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	0 0	1.5 1.5	0 0	ns	2-9

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	236		95		145		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	2.0	6.0	10.0	1.0	11.5	1.5	11.0	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	2.0	7.0	11.0	1.0	12.5	1.5	12.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	5.0	2.0	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s (H) t_s (L)	Setup Time D_n to CP	5.0	3.0 3.0	2.0 2.5	3.5 3.5	2.0 2.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.0	1.5	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0	3.0	5.0	3.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.0	5.0	4.0	ns	2-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	0	0	1.5	0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

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ADVANCE INFORMATION

54ACT/74ACT181
4-Bit Arithmetic Logic Unit

General Description

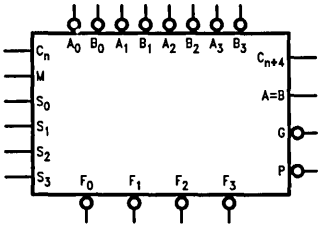
The 'ACT181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

Features

- Full lookahead for high-speed arithmetic operation on long words
- 'ACT181 has TTL-compatible inputs

Logic Symbols

Active-HIGH Operands



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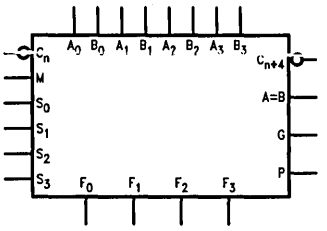
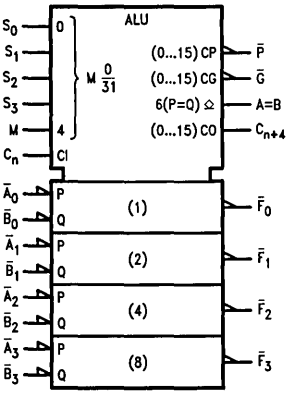
Active-LOW Operands



TL/F/9938–2

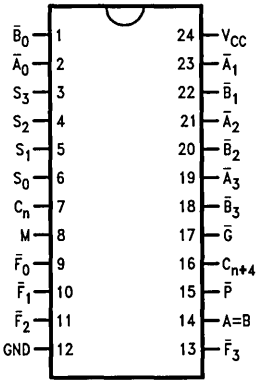
IEEE/IEC



TL/F/9938–4

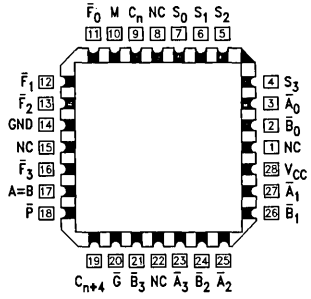
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9938–3

Pin Assignment for LCC



TL/F/9938–5

Pin Names	Description
$\bar{A}_0$–$\bar{A}_3$	A Operand Inputs (Active LOW)
$\bar{B}_0$–$\bar{B}_3$	B Operand Inputs (Active LOW)
S_0–S_3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\bar{F}_0$–$\bar{F}_3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\bar{G}$	Carry Generate Output (Active LOW)
$\bar{P}$	Carry Propagate Output (Active LOW)
$C_n + 4$	Carry Output

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT182
Carry Lookahead Generator

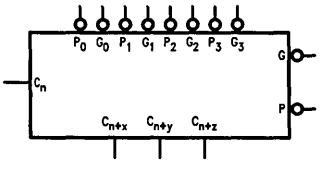
General Description

The 'ACT182 is a high-speed carry lookahead generator.

Features

- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths
- 'ACT182 has TTL-compatible inputs

Logic Symbols



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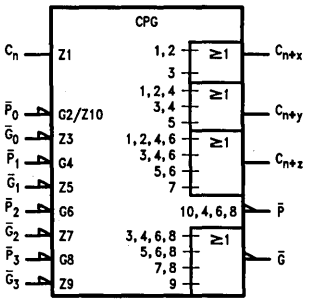
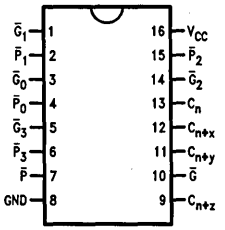
IEEE/IEC



TL/F/9939-1

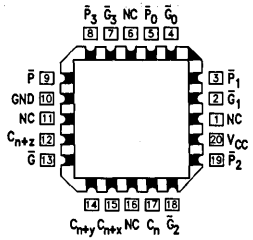
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9939-2

Pin Assignment for LCC



TL/F/9939-3

Pin Names	Description
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}–C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

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54AC/74AC191
Up/Down Counters with Preset and Ripple Clock

General Description

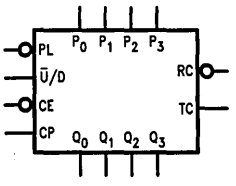
The 'AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

- High speed—133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable
- Outputs source/sink 24 mA

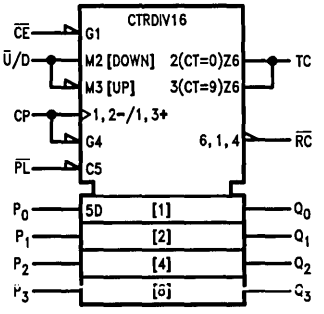
Ordering Code: See Section 5

Logic Symbols



TL/F/9940-1

IEEE/IEC

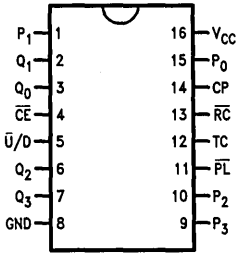


TL/F/9940-2

Pin Names	Description
$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}$/D	Up/Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

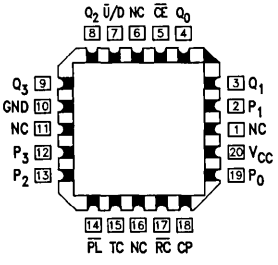
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9940-3

Pin Assignment for LCC



TL/F/9940-4

Functional Description

The 'AC191 is a synchronous up/down counter. The 'AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}/D$ input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}/D$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}/D$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output wil go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in *Figures A* and *B*. In *Figure A*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in *Figure B*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure C* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures A* and *B* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Mode Select Table

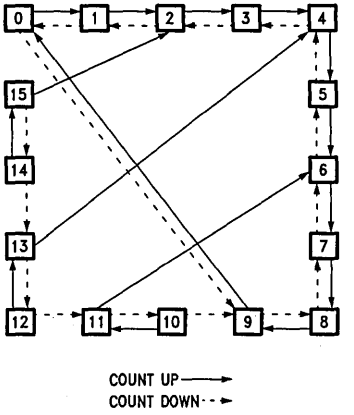
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs				Outputs
$\overline{PL}$	$\overline{CE}$	TC*	CP	$\overline{RC}$
H	L	H	⌐⌙	⌐⌙
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

State Diagram



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Functional Description (Continued)

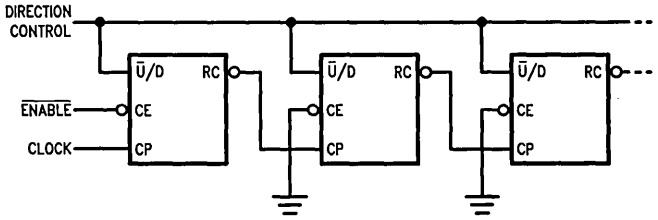

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FIGURE A. N-Stage Counter Using Ripple Clock

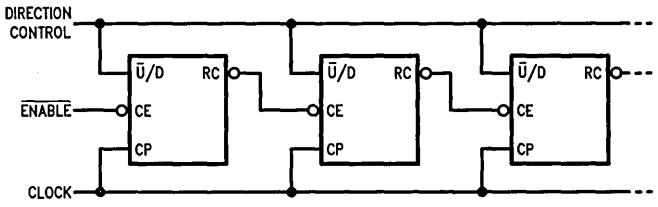

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FIGURE B. Synchronous N-Stage Counter Using Ripple Carry/Borrow

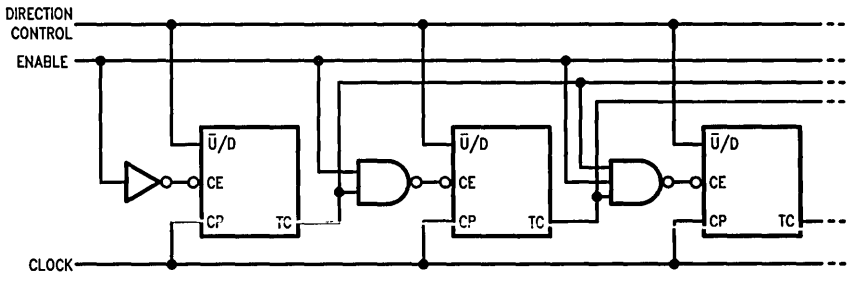

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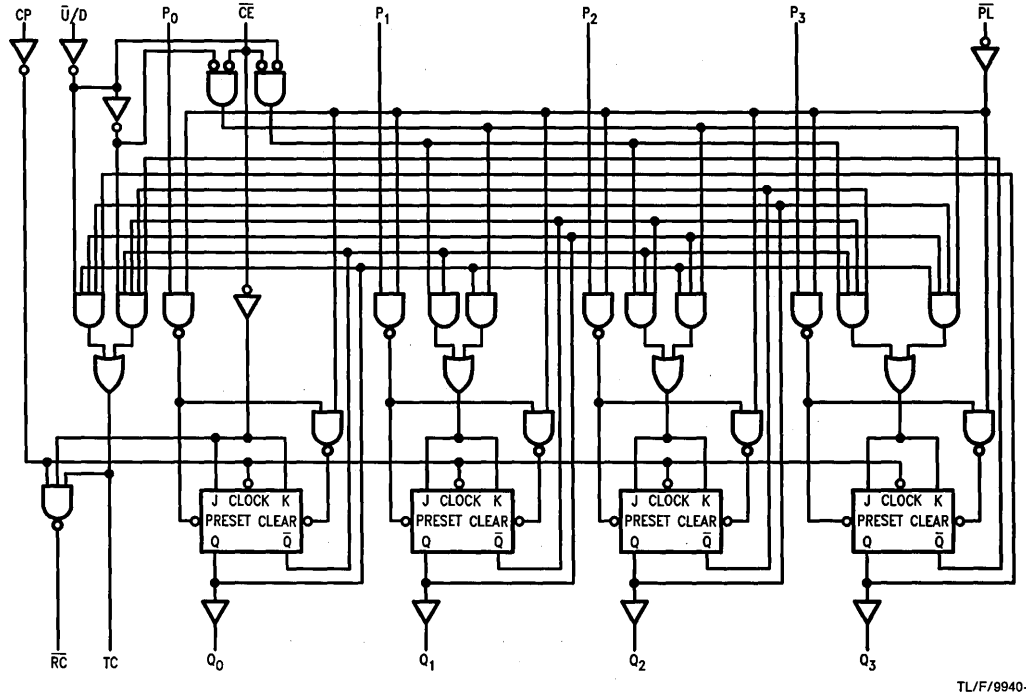
FIGURE C. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
f_{max}	Maximum Count Frequency	3.3	70	105		55		65		MHz	2-3
		5.0	90	133		80		85			
t_{PLH}	Propagation Delay CP to Q_n	3.3	2.0	8.5	15.0	1.0	16.5	1.5	16.0	ns	2-6
		5.0	1.5	6.0	11.0	1.0	12.0	1.5	12.0		
t_{PHL}	Propagation Delay CP to Q_n	3.3	2.5	8.5	14.5	1.0	16.0	2.0	16.0	ns	2-6
		5.0	1.5	6.0	10.5	1.0	12.0	1.5	11.5		
t_{PLH}	Propagation Delay CP to TC	3.3	3.5	10.5	18.0	1.0	19.5	2.5	20.0	ns	2-6
		5.0	2.5	7.5	12.0	1.0	14.0	1.5	14.0		
t_{PHL}	Propagation Delay CP to TC	3.3	4.0	10.5	17.5	1.0	19.0	3.0	19.0	ns	2-6
		5.0	2.5	7.5	12.5	1.0	14.5	2.0	13.5		
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3	2.5	7.5	12.0	1.0	14.0	2.0	13.5	ns	2-6
		5.0	2.0	5.5	9.5	1.0	10.5	1.0	10.5		
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3	2.5	7.0	11.5	1.0	12.5	2.0	12.5	ns	2-6
		5.0	1.5	5.0	8.5	1.0	9.5	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3	2.5	7.0	12.0	1.0	14.0	1.5	13.5	ns	2-6
		5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.5		
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3	2.0	6.5	11.0	1.0	12.5	1.5	12.5	ns	2-6
		5.0	1.5	5.0	8.0	1.0	9.5	1.0	9.0		
t_{PLH}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3	2.5	6.5	12.5	1.0	14.5	2.0	14.5	ns	2-6
		5.0	1.5	5.0	9.0	1.0	11.0	1.0	10.0		
t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3	2.5	7.0	12.0	1.0	15.0	2.0	13.5	ns	2-6
		5.0	1.5	5.0	8.5	1.0	11.0	1.0	10.0		
t_{PLH}	Propagation Delay $\overline{U}/D$ to TC	3.3	2.0	7.0	11.5	1.0	14.0	1.5	13.5	ns	2-6
		5.0	1.5	5.0	8.5	1.0	13.5	1.0	9.5		
t_{PHL}	Propagation Delay $\overline{U}/D$ to TC	3.3	2.0	6.5	11.0	1.0	13.5	1.5	12.5	ns	2-6
		5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay P_n to Q_n	3.3	2.5	8.0	13.5	1.0	16.5	2.0	15.5	ns	2-6
		5.0	2.0	5.5	9.5	1.0	11.5	1.0	10.5		

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay P_n to Q_n	3.3	2.5	7.5	13.0	1.0	15.5	1.5	14.5	ns	2-6
		5.0	1.5	5.5	9.5	1.0	10.5	1.0	10.5		
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3	3.5	9.5	14.5	1.0	18.0	2.5	17.5	ns	2-6
		5.0	2.0	5.5	9.5	1.0	12.5	1.0	10.5		
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3	3.0	8.0	13.5	1.0	15.5	2.0	15.5	ns	2-6
		5.0	2.0	6.0	10.0	1.0	11.5	1.5	11.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3	1.0	3.0	4.0	3.0	ns	2-9
		5.0	0.5	2.0	3.0	2.5		
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3	−1.5	0.5	1.5	1.0	ns	2-9
		5.0	−0.5	1.0	2.0	1.0		
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3	3.0	6.0	9.0	7.0	ns	2-9
		5.0	1.5	4.0	6.0	4.5		
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3	−4.0	−0.5	0	−0.5	ns	2-9
		5.0	−2.5	0	0.5	0		
t_s	Setup Time, HIGH or LOW $\overline{U}/D$ to CP	3.3	4.0	8.0	10.5	9.0	ns	2-9
		5.0	2.5	5.5	7.5	6.5		
t_h	Hold Time, HIGH or LOW $\overline{U}/D$ to CP	3.3	−5.0	0	0	0	ns	2-9
		5.0	−3.0	0.5	1.0	0.5		
t_w	$\overline{PL}$ Pulse Width, LOW	3.3	2.0	3.5	5.0	4.0	ns	2-6
		5.0	1.0	1.0	5.0	1.0		
t_w	CP Pulse Width, LOW	3.3	2.0	3.5	6.0	4.0	ns	2-6
		5.0	2.0	3.0	6.0	4.0		
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3	−0.5	0	1.5	0	ns	2-9
		5.0	−1.0	0	1.0	0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	75.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC240 • 54ACT/74ACT240
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

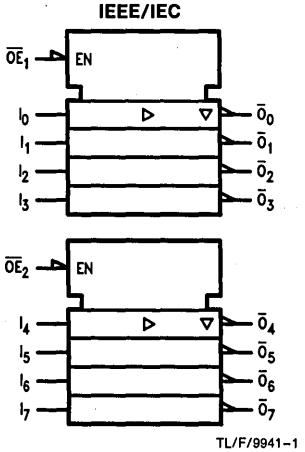
The 'AC/'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT240 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol



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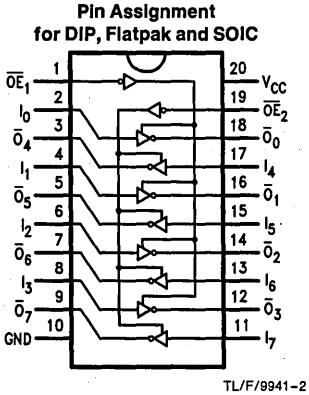
Connection Diagrams



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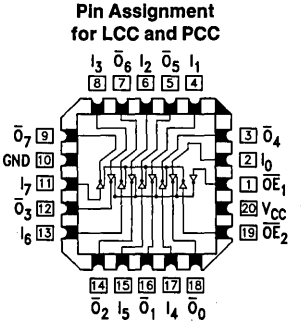


TL/F/9941–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}1$	D	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}2$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	6.0	8.0	1.0	11.0	1.0	9.0	ns	2-5
		5.0	1.5	4.5	6.5	1.0	8.5	1.0	7.0		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	5.5	8.0	1.0	10.5	1.0	8.5	ns	2-5
		5.0	1.5	4.5	6.0	1.0	8.0	1.0	6.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.0	10.5	1.0	11.5	1.0	11.0	ns	2-7
		5.0	1.5	5.0	7.0	1.0	9.0	1.0	8.0		
t_{PZL}	Output Enable Time	3.3	1.5	7.0	10.0	1.0	13.0	1.0	11.0	ns	2-8
		5.0	1.5	5.5	8.0	1.0	10.5	1.0	8.5		
t_{PHZ}	Output Disable Time	3.3	1.5	7.0	10.0	1.0	12.5	1.0	10.5	ns	2-7
		5.0	1.5	6.5	9.0	1.0	10.5	1.0	9.5		
t_{PLZ}	Output Disable Time	3.3	1.5	7.5	10.5	1.0	13.5	1.0	11.5	ns	2-8
		5.0	1.5	6.5	9.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.5	6.0	8.5	1.0	9.5	1.5	9.5	ns	2-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.5	5.5	7.5	1.0	9.0	1.5	8.5	ns	2-5
t_{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.0	10.0	1.0	9.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.5	1.5	10.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.0	8.0	9.5	1.0	11.0	2.0	10.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.5	6.5	10.0	1.0	11.5	2.0	10.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC241 • 54ACT/74ACT241
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

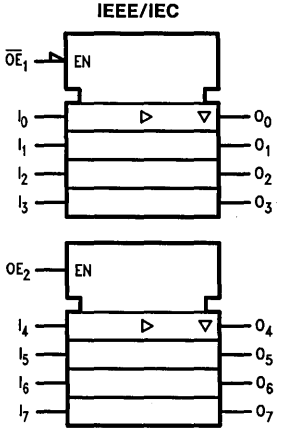
The 'AC/'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

Features

- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT241 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol



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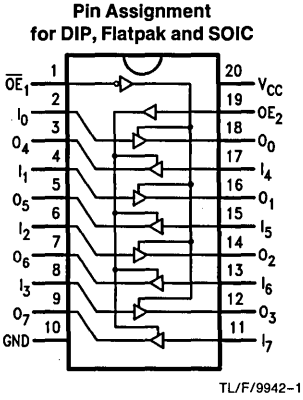
Connection Diagrams



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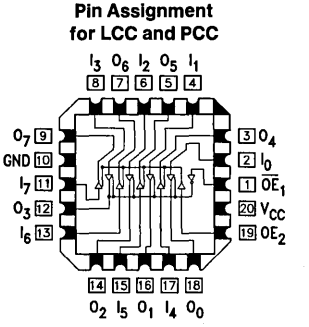


TL/F/9942-3

Pin Names	Description
$\overline{OE}_1$,	TRI-STATE Output Enable Input
OE_2	TRI-STATE Output Enable Input (Active HIGH)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	D	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC / 54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	6.0	9.0	1.0	12.0	1.5	10.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	6.0	9.0	1.0	11.5	1.0	10.5	ns	2-5
		5.0	1.5	4.5	7.0	1.0	9.0	1.0	7.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.5	12.5	1.0	13.0	1.0	13.0	ns	2-7
		5.0	1.5	5.5	9.0	1.0	10.0	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	1.5	7.0	12.0	1.0	13.0	1.5	13.0	ns	2-8
		5.0	1.5	5.5	9.0	1.0	10.0	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	2.0	8.0	12.0	1.0	13.0	2.0	12.5	ns	2-7
		5.0	1.5	6.5	10.0	1.0	11.5	1.0	10.5		
t_{PLZ}	Output Disable Time	3.3	1.5	7.0	12.5	1.0	13.0	1.0	13.5	ns	2-8
		5.0	1.5	6.0	10.0	1.0	11.5	1.0	10.5		

*Voltage Range 3.3 is 3.3V ±3.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.5	6.5	9.0	1.0	10.0	1.5	10.0	ns	2-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.5	7.0	9.0	1.0	10.0	1.5	10.0	ns	2-5
t_{PZH}	Output Enable Time	5.0	1.5	6.0	9.0	1.0	11.5	1.0	10.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	1.5	7.0	10.0	1.0	12.5	1.5	11.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	8.0	10.5	1.0	12.5	1.5	11.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC244 • 54ACT/74ACT244
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

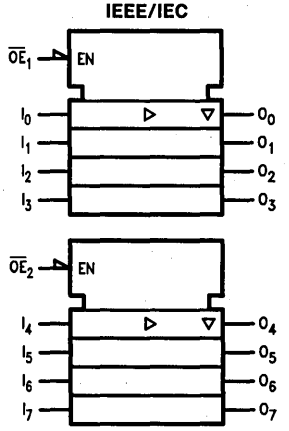
The 'AC/'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT244 has TTL-compatible inputs

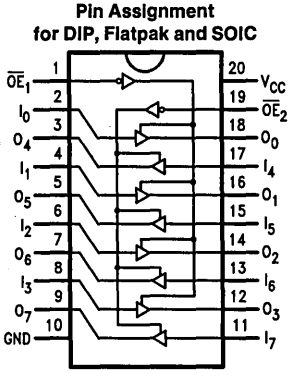
Ordering Code: See Section 5

Logic Symbol



TL/F/9943–1

Connection Diagrams



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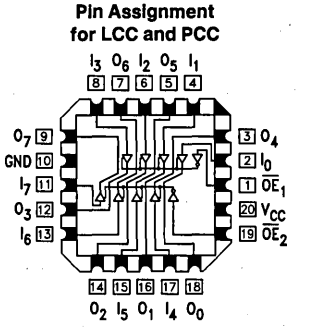


TL/F/9943–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	D	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ -20 mA
- $V_I = V_{CC} + 0.5V$ $+20$ mA

DC Input Voltage (V_I) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ -20 mA
- $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65°C$ to $+150°C$

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT $-40°C$ to $+85°C$
- 54AC/ACT $-55°C$ to $+125°C$

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -12 mA
		4.5		3.86	3.7	3.76		I_{OH} -24 mA
		5.5		4.86	4.7	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0	1.0	12.5	1.5	10.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5		
t_{PHL}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0	1.0	12.0	2.0	10.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	9.0	1.0	7.5		
t_{PZH}	Output Enable Time	3.3	2.0	6.0	10.5	1.0	11.5	1.5	11.0	ns	2-7
		5.0	1.5	5.0	7.0	1.0	9.0	1.5	8.0		
t_{PZL}	Output Enable Time	3.3	2.5	7.5	10.0	1.0	13.0	2.0	11.0	ns	2-8
		5.0	1.5	5.5	8.0	1.0	10.5	1.5	8.5		
t_{PHZ}	Output Disable Time	3.3	3.0	7.0	10.0	1.0	12.5	1.5	10.5	ns	2-7
		5.0	2.5	6.5	9.0	1.0	10.5	1.0	9.5		
t_{PLZ}	Output Disable Time	3.3	2.5	7.5	10.5	1.0	13.0	2.5	11.5	ns	2-8
		5.0	2.0	6.5	9.0	1.0	11.0	2.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	2.0	6.5	9.0	1.0	10.0	1.5	10.0	ns	2-5
t_{PHL}	Propagation Delay Data to Output	5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	ns	2-5
t_{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	1.0	9.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	1.0	11.5	2.0	10.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC245 • 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

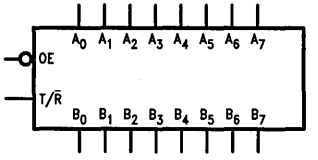
The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

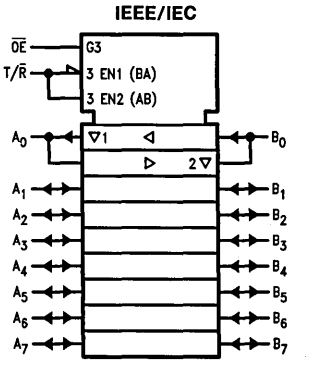
- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- 'ACT245 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



TL/F/9944–1



TL/F/9944–2

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

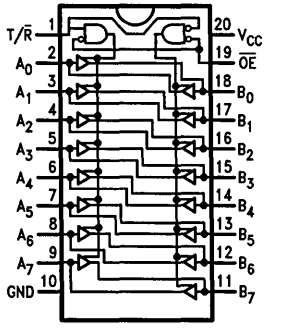
Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

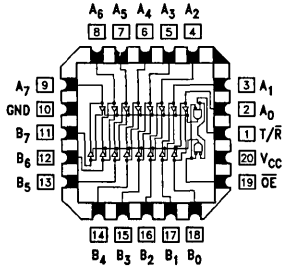
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9944–3

Pin Assignment for LCC and PCC



TL/F/9944–4

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		I_{OH} −24 mA
					4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50		I_{OL} 24 mA
		5.5		0.36	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	11.5	1.0	9.0	ns	2-5
		5.0	1.5	3.5	6.5	1.0	8.5	1.0	7.0		
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	10.0	1.0	9.0	ns	2-5
		5.0	1.5	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	1.0	13.5	2.0	12.5	ns	2-7
		5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.0		
t_{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	1.0	14.5	2.0	13.5	ns	2-8
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	13.5	1.0	12.5	ns	2-7
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.0	14.0	1.5	13.0	ns	2-8
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	7.5	1.0	9.0	1.5	8.0	ns	2-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	8.0	1.0	10.0	1.0	9.0	ns	2-5
t_{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.0	12.0	1.5	11.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.0	13.0	1.5	12.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	12.0	1.0	11.0	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.0	12.0	1.5	11.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC251 • 54ACT/74ACT251
8-Input Multiplexer with TRI-STATE® Output

General Description

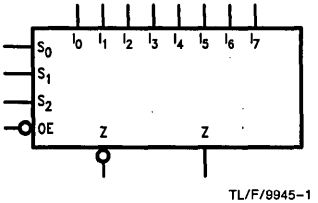
The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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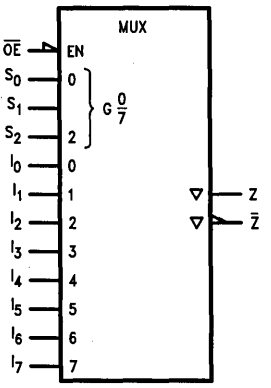
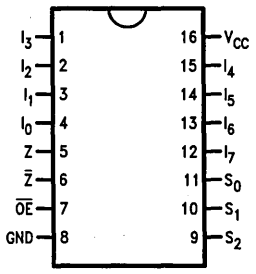
IEEE/IEC



TL/F/9945–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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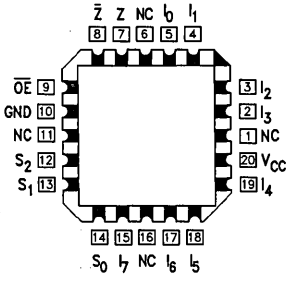
Pin Assignment for LCC



TL/F/9945–4

Pin Names	Description
S_0–S_2	Select Inputs
$\overline{OE}$	TRI-STATE Output Enable Input
I_0–I_7	Multiplexer Inputs
Z	TRI-STATE Multiplexer Output
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

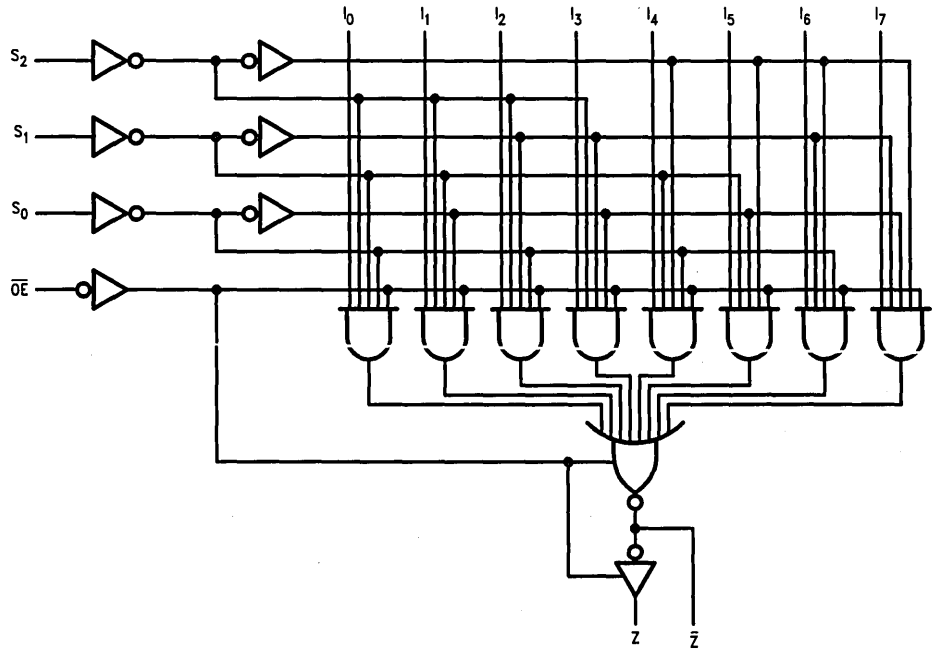
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9945–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.5	17.5	1.0	21.0	1.5	19.0	ns	2-6
		5.0	1.5	8.5	12.5	1.0	15.5	1.5	13.5		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.0	17.5	1.0	21.0	1.5	19.0	ns	2-6
		5.0	1.5	8.0	12.5	1.0	15.5	1.5	13.5		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	10.0	14.0	1.0	17.0	1.5	15.5	ns	2-5
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	9.0	14.0	1.0	16.5	1.5	15.5	ns	2-5
		5.0	1.5	6.5	10.0	1.0	12.0	1.5	11.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-7
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-8
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	8.5	11.5	3.5	14.0	1.5	13.0	ns	2-7
		5.0	1.5	7.0	9.5	2.5	11.0	1.5	10.0		
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.0	11.0	4.0	13.0	1.5	12.0	ns	2-8
		5.0	1.5	5.5	8.0	3.0	10.0	1.5	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.0	15.5	1.0	18.5	2.0	17.0	ns	2-6
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.5	16.5	1.0	19.5	2.5	18.5	ns	2-6
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	5.5	12.0	1.0	14.0	2.0	13.0	ns	2-5
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	6.5	12.5	1.0	15.0	2.5	14.0	ns	2-5
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	5.0	8.5	1.0	10.0	1.5	9.0	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	4.5	8.5	1.0	10.0	1.5	9.5	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	2.0	6.0	12.0	1.0	13.5	2.0	13.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	3.0	4.5	8.5	1.0	9.5	3.0	9.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC253 • 54ACT/74ACT253
Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

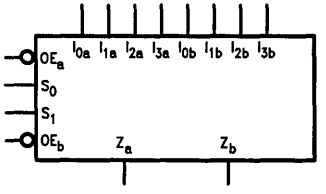
The 'AC/'ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Features

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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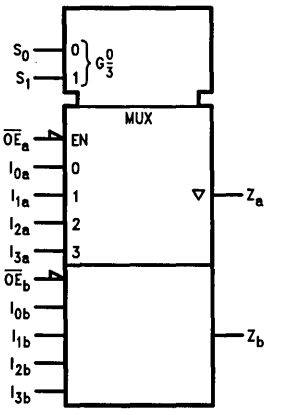
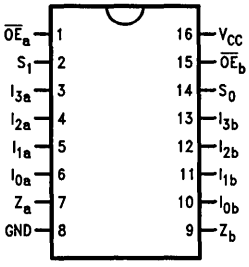


TL/F/9946–2

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	TRI-STATE Outputs

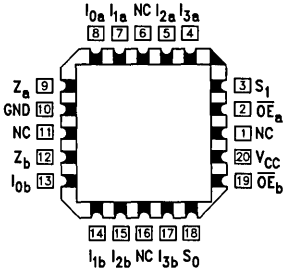
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9946–3

Pin Assignment for LCC



TL/F/9946–4

Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

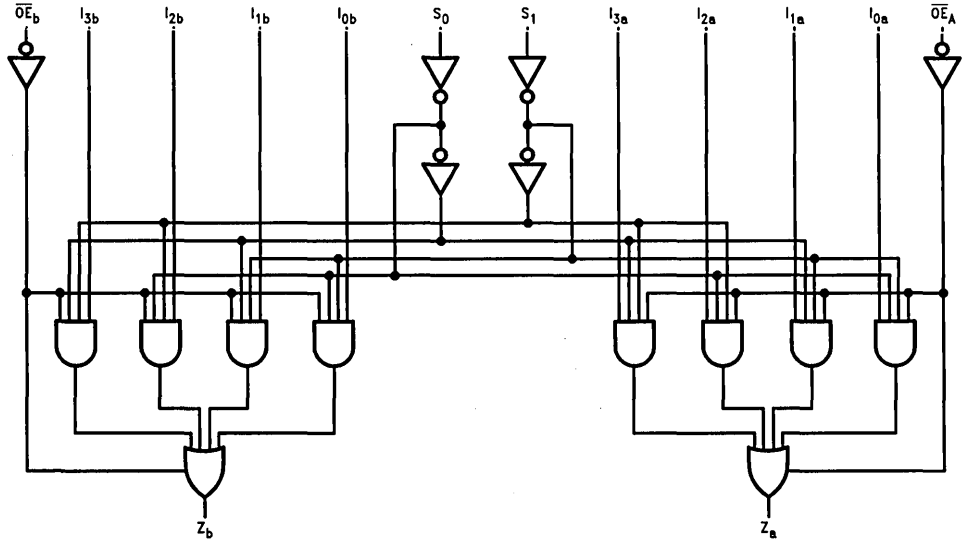
Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9946–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	2.0	8.5	15.5	1.0	19.5	2.0	17.5	ns	2-6
		5.0	2.0	6.5	11.0	1.0	13.5	1.5	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	2.5	9.5	16.0	1.0	20.0	2.0	18.0	ns	2-6
		5.0	2.0	7.0	11.5	1.0	15.0	1.5	13.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	7.0	14.5	1.0	19.0	1.5	17.0	ns	2-5
		5.0	1.5	5.5	10.0	1.0	13.0	1.5	11.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	2.0	7.5	13.0	1.0	16.0	1.5	15.0	ns	2-5
		5.0	1.5	5.5	9.5	1.0	12.0	1.5	11.0		
t_{PZH}	Output Enable Time	3.3	1.5	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-7
		5.0	1.5	3.5	6.0	1.0	7.0	1.0	6.5		
t_{PZL}	Output Enable Time	3.3	1.5	5.0	8.0	1.0	10.0	1.0	9.0	ns	2-8
		5.0	1.5	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PHZ}	Output Disable Time	3.3	2.0	5.5	9.5	1.0	11.0	1.5	10.0	ns	2-7
		5.0	2.0	5.0	8.0	1.0	9.5	1.5	8.5		
t_{PLZ}	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.5	1.0	9.0	ns	2-8
		5.0	1.5	4.0	7.0	1.0	8.0	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	2.0	7.0	11.5	1.0	14.5	2.0	13.0	ns	2-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.5	13.0	1.0	16.0	2.5	14.5	ns	2-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	10.0	1.0	12.0	2.0	11.0	ns	2-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	3.5	6.5	11.0	1.0	13.5	3.0	12.5	ns	2-5
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.0	9.5	1.5	8.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.0	9.5	1.5	9.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	1.0	11.0	2.5	10.0	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	1.0	9.0	2.0	8.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC257•54ACT/74ACT257
Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

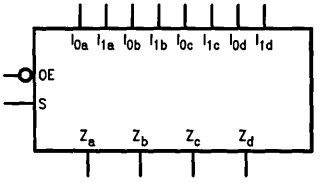
The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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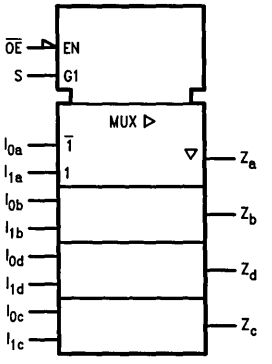
IEEE/IEC

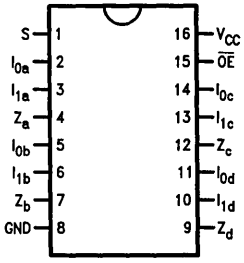


TL/F/9949–2

Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Z_a–Z_d	TRI-STATE Multiplexer Outputs

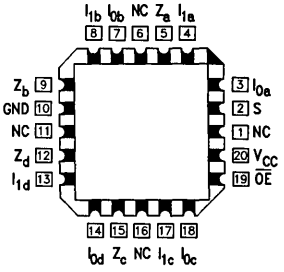
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9949–3

Pin Assignment for LCC



TL/F/9949–4

Functional Description

The 'AC/'ACT257 is quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

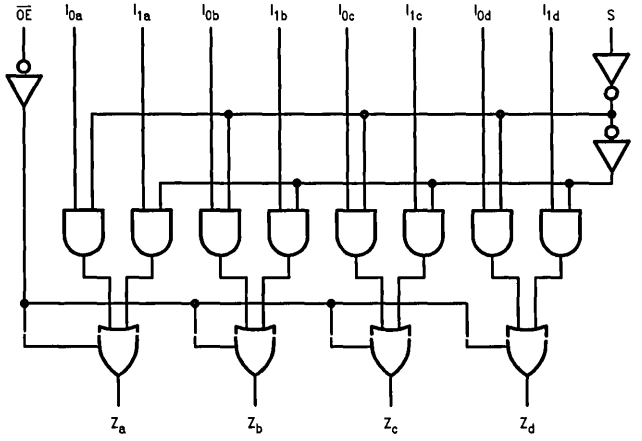
When the Output Enable ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9949–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70%, V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	11.0	1.0	9.0	ns	2-6
		5.0	1.5	4.0	6.0	1.0	8.0	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	6.0	8.5	1.0	11.0	1.0	9.0	ns	2-6
		5.0	1.5	4.5	6.0	1.0	8.5	1.0	7.0		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	10.5	1.0	14.5	1.5	11.5	ns	2-6
		5.0	1.5	5.0	7.5	1.0	11.0	1.0	8.5		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	7.5	10.5	1.0	14.5	1.5	11.5	ns	2-6
		5.0	1.5	5.5	7.5	1.0	11.0	1.0	8.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.5	9.5	1.0	13.0	1.0	10.5	ns	2-7
		5.0	1.5	5.0	7.5	1.0	10.0	1.0	8.5		
t_{PZL}	Output Enable Time	3.3	1.5	5.5	9.0	1.0	11.0	1.0	10.0	ns	2-8
		5.0	1.5	5.0	8.5	1.0	9.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.5	5.5	10.0	1.0	13.0	1.0	11.0	ns	2-7
		5.0	1.5	5.0	9.0	1.0	11.0	1.0	10.0		
t_{PLZ}	Output Disable Time	3.3	1.5	5.5	9.0	1.0	10.5	1.0	10.0	ns	2-8
		5.0	1.5	5.0	8.0	1.0	9.5	1.0	9.0		

*Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.5	5.0	7.0	1.0	8.0	1.0	7.5	ns	2-6
t_{PHL}	Propagation Delay I_n to Z_n	5.0	2.0	6.0	7.5	1.0	9.5	1.5	8.5	ns	2-6
t_{PLH}	Propagation Delay S to Z_n	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay S to Z_n	5.0	2.5	7.0	10.5	1.0	11.5	2.0	11.5	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	6.0	8.0	1.0	9.5	1.5	9.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	6.0	8.0	1.0	9.5	1.5	9.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.5	6.5	9.0	1.0	10.5	1.5	10.0	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	7.5	1.0	9.0	1.5	8.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC258 • 54ACT/74ACT258
Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

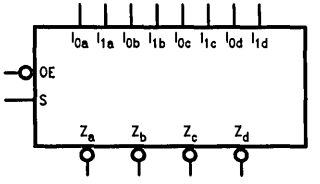
The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs

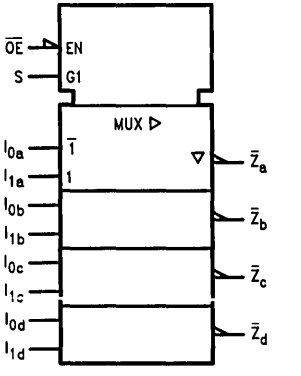
Ordering Code: See Section 5

Logic Symbols



TL/F/9950–1

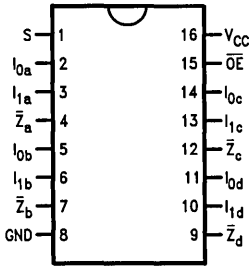
IEEE/IEC



TL/F/9950–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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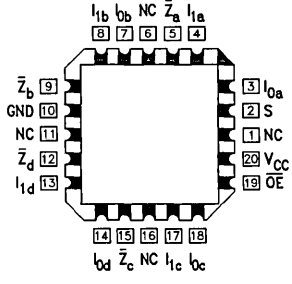
Pin Assignment for LCC



TL/F/9950–4

Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$–$\overline{Z}_d$	TRI-STATE Inverting Data Outputs

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

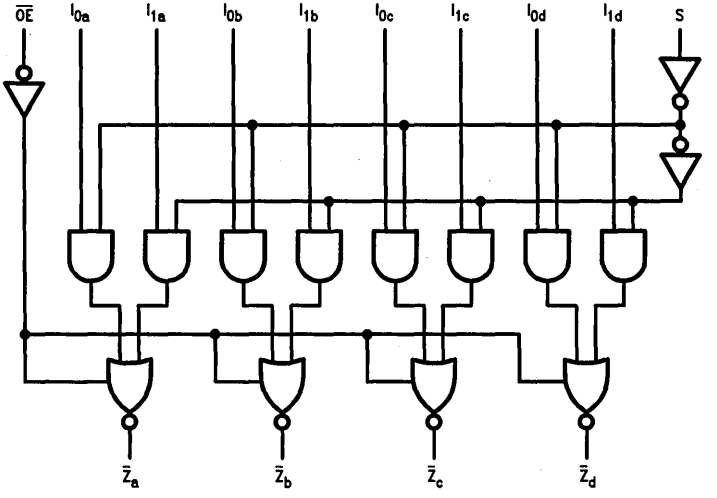
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	2.0 1.5	6.0 4.5	9.5 7.5	1.0 1.0	12.0 9.5	1.5 1.0	11.0 8.5	ns	2-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	2.0 1.5	5.0 4.0	8.5 6.5	1.0 1.0	10.5 7.5	1.5 1.0	9.5 7.0	ns	2-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	3.0 2.0	7.5 6.0	12.0 9.5	1.0 1.0	15.0 11.5	2.5 1.5	14.0 10.5	ns	2-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.0	1.0 1.0	14.0 10.5	2.0 1.5	13.0 10.0	ns	2-6
t_{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	6.0 4.5	9.5 7.5	1.0 1.0	11.5 9.0	2.0 1.5	10.5 8.5	ns	2-7
t_{PZL}	Output Enable Time	3.3 5.0	2.0 1.5	5.5 5.5	9.0 7.0	1.0 1.0	10.5 8.5	1.5 1.0	10.0 8.0	ns	2-8
t_{PHZ}	Output Disable Time	3.3 5.0	2.5 2.0	5.5 5.5	10.0 8.5	1.0 1.0	11.5 9.5	2.0 1.5	11.5 9.0	ns	2-7
t_{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	5.5 5.0	9.0 7.0	1.0 1.0	10.5 8.5	2.0 1.5	10.0 8.0	ns	2-8

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns	2-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	5.5	7.5	1.0	9.0	1.5	8.0	ns	2-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	3.0	7.5	10.5	1.0	13.0	2.0	11.5	ns	2-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.5	7.0	9.5	1.0	12.0	1.5	11.0	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.0	1.5	9.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.5	1.0	10.0	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.0	10.0	1.5	9.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	55.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54AC/74AC269
8-Bit Bidirectional Binary Counter

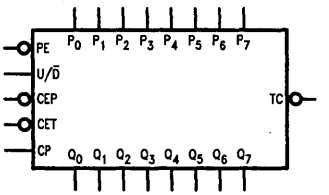
General Description

The 'AC269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

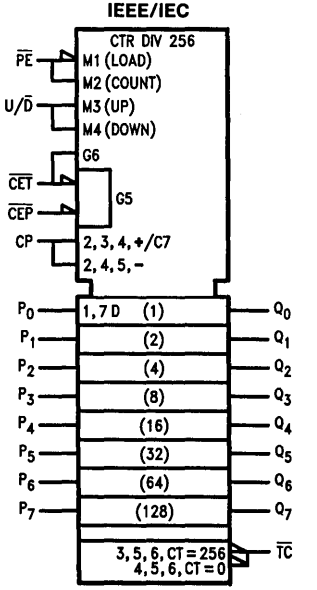
Features

- Synchronous counting and loading
- Built-in lookahead carry capability
- 300 mil slimline package

Logic Symbols



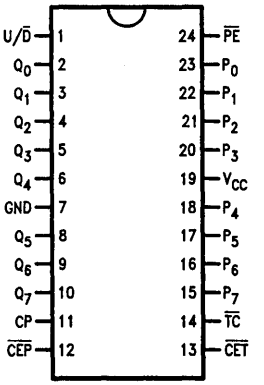
TL/F/9953-1



TL/F/9953-4

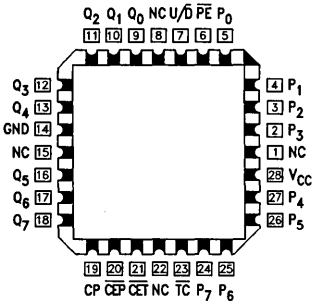
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9953-2

Pin Assignment for LCC



TL/F/9953-3

Function Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ($\overline{TC}$ Held HIGH)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = Transition LOW-to-HIGH

National Semiconductor

54AC/74AC273 • 54ACT/74ACT273
Octal D Flip-Flop

General Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

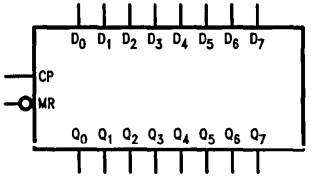
The Information for the ACT273 is Advanced Information only.

Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See '377 for clock enable version
- See '373 for transparent latch version
- See '374 for TRI-STATE version
- Outputs source/sink 24 mA
- 'ACT273 has TTL compatible inputs

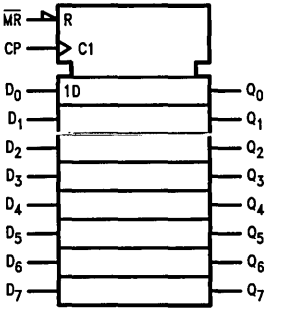
Ordering Code: See Section 5

Logic Symbols



TL/F/9954–1

IEEE/IEC

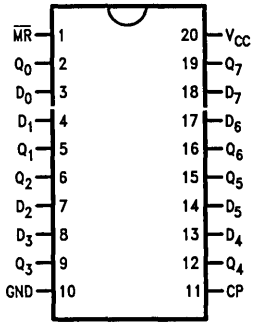


TL/F/9954–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

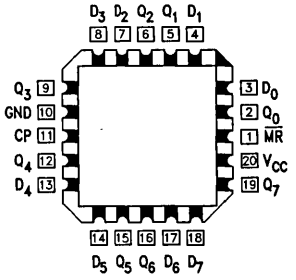
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9954–3

Pin Assignment for LCC



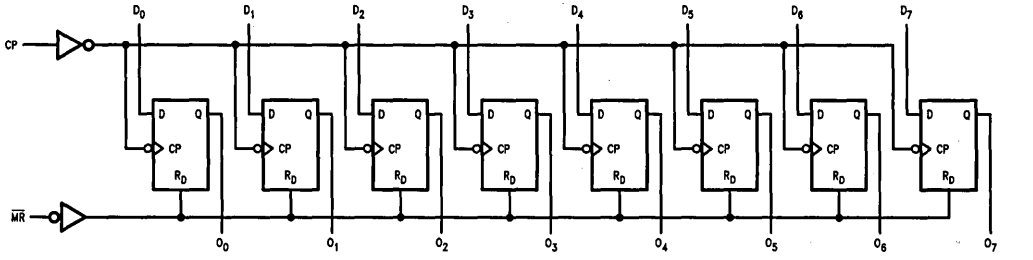
TL/F/9954–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9954–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5 to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		I_{OH} −24 mA
					2.46		
					3.76		
					4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		I_{OL} 24 mA
					0.44		
					0.44		
					0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
					±1.0		

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	90	125		75		75		MHz	2-3
		5.0	140	175		90		125			
t_{PLH}	Propagation Delay Clock to Output	3.3	4.0	7.0	12.5	1.0	15.0	3.0	14.0	ns	2-6
		5.0	3.0	5.5	9.0	1.0	11.0	2.5	10.0		
t_{PHL}	Propagation Delay Clock to Output	3.3	4.0	7.0	13.0	1.0	16.0	3.5	14.5	ns	2-6
		5.0	3.0	5.0	10.0	1.0	11.5	2.5	11.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	3.3	4.0	7.0	13.0	1.0	16.0	3.5	14.0	ns	2-6
		5.0	3.0	5.0	10.0	1.0	11.5	2.5	10.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW Data to CP	3.3	3.5	5.5	8.0	6.0	ns	2-9
		5.0	2.5	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW Data to CP	3.3	−2.0	0	0	0	ns	2-9
		5.0	−1.0	1.0	1.0	1.0		
t_w	Clock Pulse Width HIGH or LOW	3.3	3.5	5.5	6.5	6.0	ns	2-6
		5.0	2.5	4.0	5.0	4.5		
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	3.3	2.0	5.5	10.0	6.0	ns	2-6
		5.0	1.5	4.0	6.5	4.5		
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3	1.5	3.5	6.0	4.5	ns	2-9
		5.0	1.0	2.0	4.0	3.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC280 • 54ACT/74ACT280
9-Bit Parity Generator/Checker

General Description

The 'AC/'ACT280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

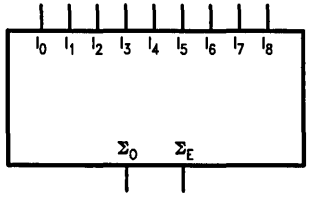
Features

- 9-bit width for memory applications
- 'ACT280 has TTL-compatible inputs

The Information for the 'ACT280 is Advanced Information only.

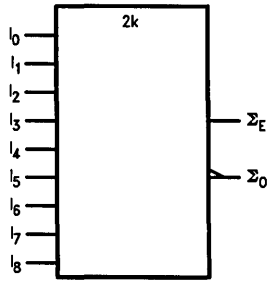
Ordering Code: See Section 5

Logic Symbols



TL/F/9955–1

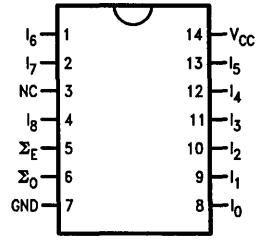
IEEE/IEC



TL/F/9955–4

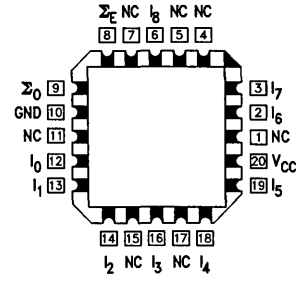
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9955–2

Pin Assignment for LCC



TL/F/9955–3

Pin Names	Description
I_0–I_8	Data Inputs
Σ_O	Odd Parity Output
Σ_E	Even Parity Output

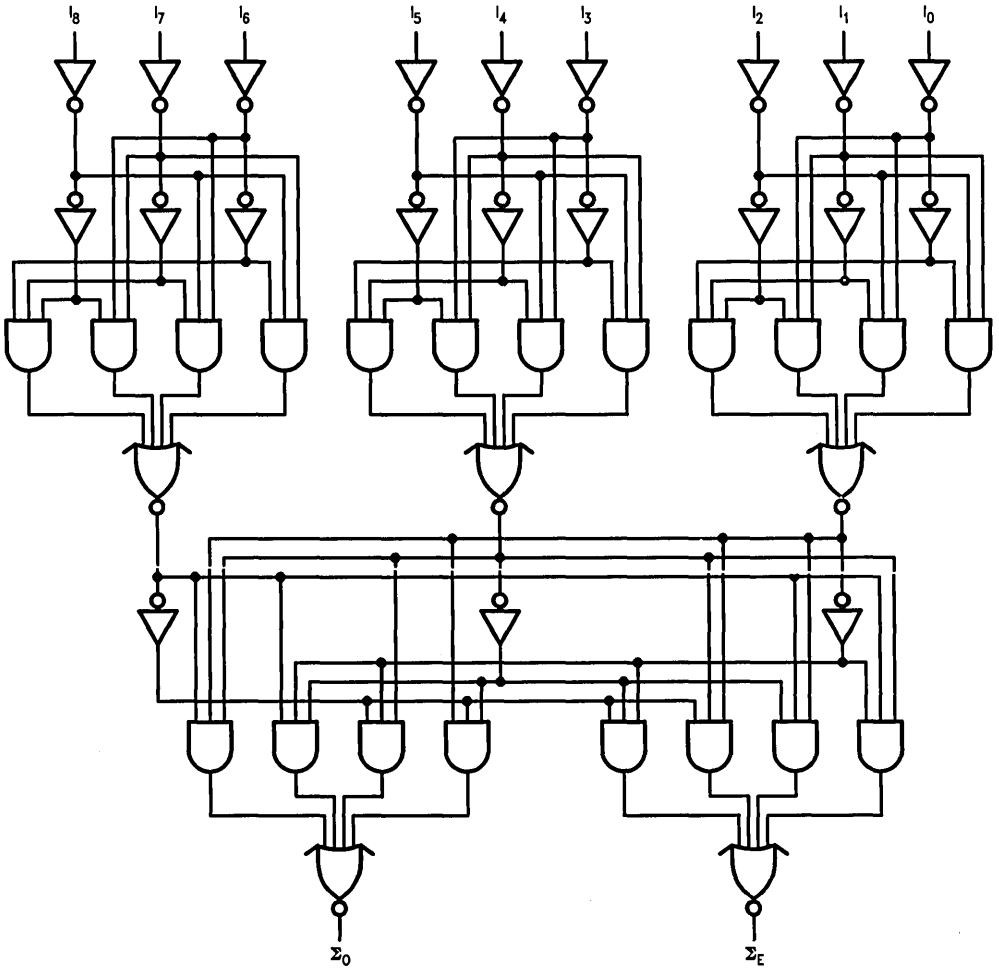
Truth Table

Number of HIGH Inputs I_0–I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Diagram



TL/F/9955–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74 AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	5.0	10.5	17.0			4.0	18.5	ns	2-5
t_{PHL}	I_n to Σ_E	5.0	3.0	7.5	13.0			2.0	14.5		
t_{PLH}	Propagation Delay	3.3	5.0	12.0	17.0			4.0	18.5	ns	2-5
t_{PHL}	I_n to Σ_O	5.0	3.0	8.5	13.0			2.0	14.5		

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	75.0	pF	V_{CC} = 5.0V

National Semiconductor

ADVANCE INFORMATION

54AC/74AC283 • 54ACT/74ACT283
4-Bit Binary Full Adder with Fast Carry

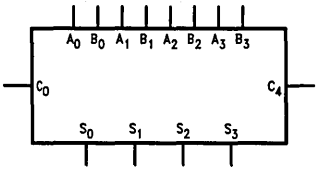
General Description

The 'AC/'ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0–A_3, B_0–B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0–S_3) and the Carry output (C_4) from the most significant bit. The 'AC/'ACT283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Features

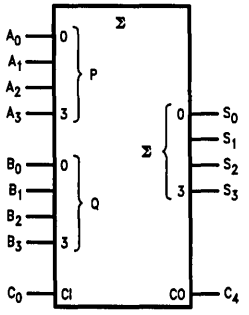
- 'ACT283 has TTL-compatible inputs

Logic Symbols



TL/F/9956–1

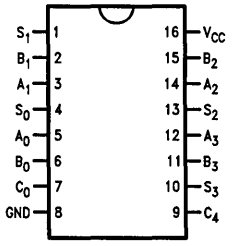
IEEE/IEC



TL/F/9956–4

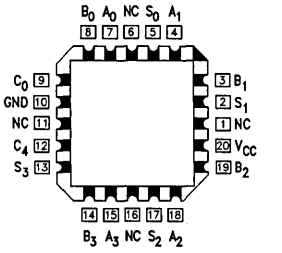
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9956–2

Pin Assignment for LCC



TL/F/9956–3

Pin Names	Description
A_0–A_3	A Operand Inputs
B_0–B_3	B Operand Inputs
C_0	Carry Input
S_0–S_3	Sum Outputs
C_4	Carry Output

National Semiconductor

54AC/74AC299 • 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

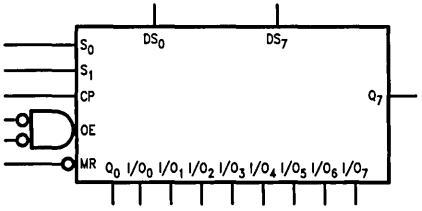
The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs

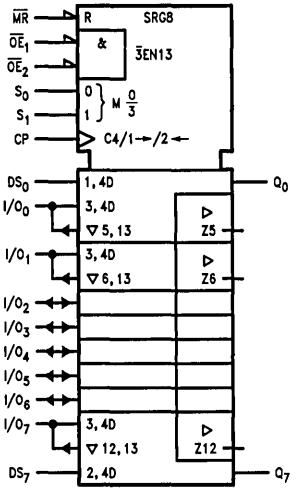
Ordering Code: See Section 5

Logic Symbols



TL/F/9893-1

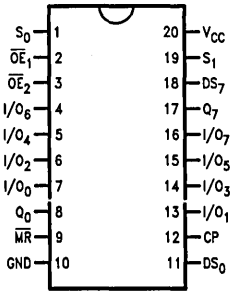
IEEE/IEC



TL/F/9893-4

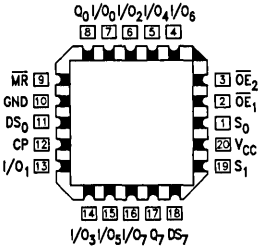
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9893-2

Pin Assignment for LCC



TL/F/9893-3

Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

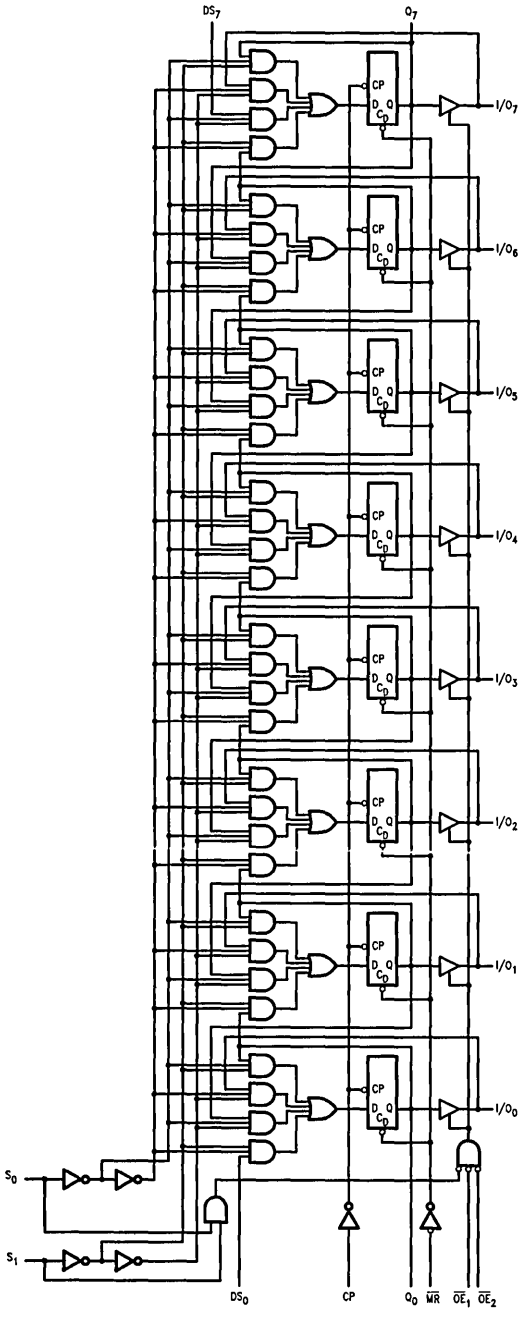
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	↗	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↗	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↗	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9893–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} 12 mA
		4.5		0.36	0.50	0.44		I_{OH} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			57	86	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; threshold on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.5V

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0	90 130	124 173		70 80		80 105		MHz	2-0
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3 5.0	8.5 5.5	14.0 9.5	20.5 14.0	1.0 1.0	25.5 17.5	7.0 4.5	22.0 15.0	ns	2-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3 5.0	8.5 5.5	14.5 10.0	21.5 14.5	1.0 1.0	26.5 18.0	7.0 5.0	23.0 16.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{CP}$ to I/O_n	3.3 5.0	9.0 6.0	14.5 10.0	20.5 14.5	1.0 1.0	24.5 17.0	7.5 5.0	22.5 16.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{CP}$ to I/O_n	3.3 5.0	10.0 6.5	16.0 11.0	23.0 16.0	1.0 1.0	26.5 18.5	8.5 6.0	24.5 17.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	3.3 5.0	9.0 5.5	15.5 10.5	22.5 15.5	1.0 1.0	27.0 18.5	7.5 5.0	25.0 17.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0	9.0 5.5	15.0 10.0	21.5 15.0	1.0 1.0	26.5 18.0	7.5 5.0	24.0 16.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0	7.0 4.5	12.0 8.5	18.0 12.5	1.0 1.0	22.0 15.0	6.0 4.0	19.5 13.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0	7.0 5.0	12.5 8.0	18.0 12.5	1.0 1.0	23.5 16.0	6.0 4.0	20.5 14.0	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0	6.5 3.5	13.0 9.5	18.5 14.0	1.0 1.0	22.5 17.0	5.5 3.0	19.5 15.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0	5.5 3.5	11.5 8.0	17.0 12.5	1.0 1.0	21.5 16.0	4.5 2.0	19.0 13.5	ns	2-8

*Voltage Range 3.3 is 3.3V ±0.3V.
Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	3.0 2.0	8.0 5.0	9.5 7.0	8.5 5.5	ns	2-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	−3.0 −1.5	0.5 1.0	2.0 2.5	0.5 1.0	ns	2-9
t_s	Setup Time, HIGH or LOW I/O_n to CP	3.3 5.0	2.0 1.0	5.5 3.5	6.0 4.0	6.0 4.0	ns	2-9
t_h	Hold Time, HIGH or LOW I/O_n to CP	3.3 5.0	−2.0 −1.0	0 1.0	1.5 2.0	0 1.0	ns	2-9
t_s	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	3.3 5.0	2.5 1.5	6.5 4.0	7.5 5.0	7.0 4.5	ns	2-9
t_h	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	3.3 5.0	−2.0 −1.0	0 1.0	1.5 1.5	0.5 1.0	ns	2-9
t_w	CP Pulse Width, LOW	3.3 5.0	3.5 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.0 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0.5	1.5 1.5	2.5 2.5	1.5 1.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0	120	170		70		110		MHz	2-0
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	8.5	12.5	1.0	15.5	3.0	14.0	ns	2-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	9.0	13.5	1.0	16.0	3.5	15.0	ns	2-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0	4.5	8.5	12.5	1.0	15.0	4.5	13.5	ns	2-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0	5.0	9.5	15.0	1.0	18.0	4.5	16.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	4.0	14.0	15.0	1.0	18.0	4.0	18.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0	4.0	13.0	14.5	1.0	17.5	3.5	17.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.5	8.0	12.0	1.0	14.0	1.5	13.0	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.0	8.0	12.0	1.0	14.5	1.5	13.5	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.5	2.0	8.5	12.5	1.0	14.5	2.0	13.5	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.0	2.5	8.0	11.5	1.0	14.0	2.0	12.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	6.5	5.5	ns	2-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	−2.0	1.0	1.5	1.0	ns	2-9
t_s	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	4.5	ns	2-9
t_h	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.5	1.0	ns	2-9
t_s	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.5	5.0	ns	2-9
t_h	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	−1.0	1.0	1.5	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.5	ns	2-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	5.0	3.5	ns	2-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	1.5	1.5	1.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V.

National Semiconductor

54ACT/74ACT323
8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

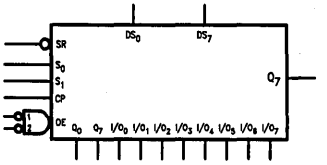
The 'ACT323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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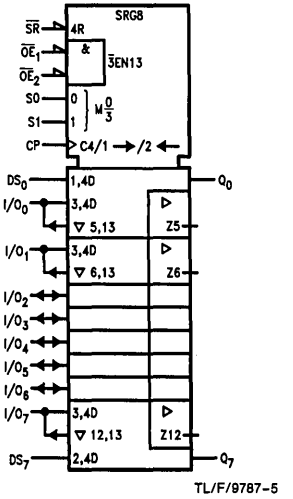
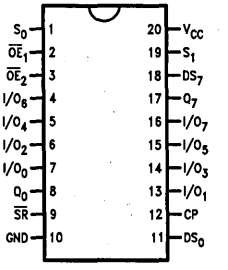


TL/F/9787-5

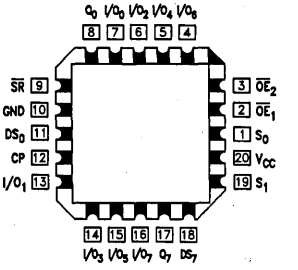
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9787-2

Pin Assignment for LCC



TL/F/9787-3

Pin Name	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Multiplexed Parallel Data Inputs or TRI-STATE Parallel Data Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The 'ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP.

Mode Select Table

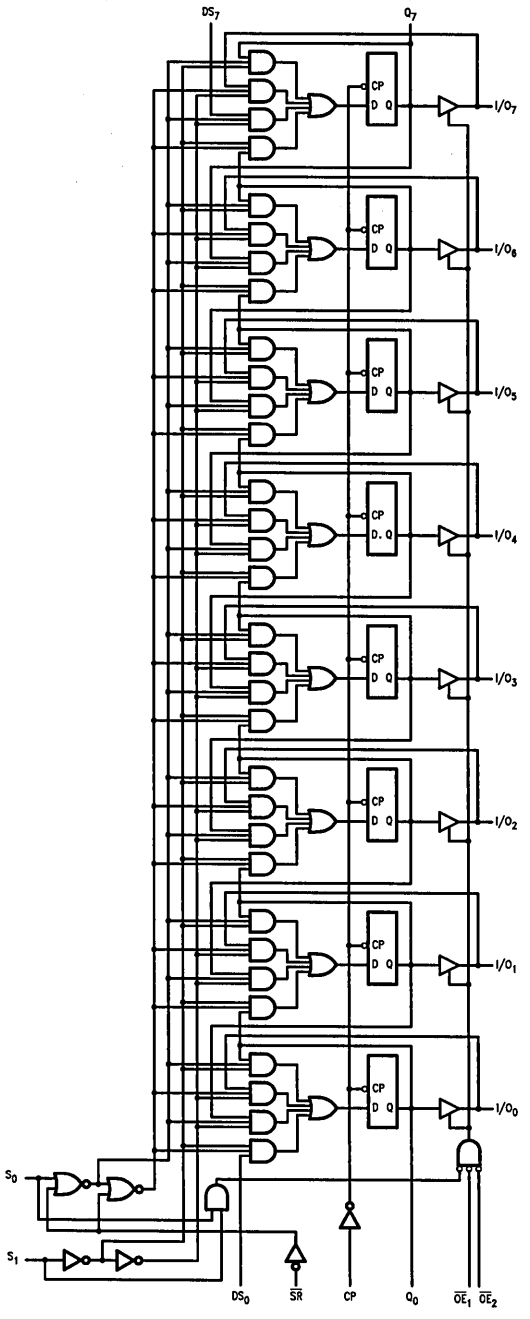
Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas}	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} −24 mA −24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_{I/O}$ = V_{CC} or GND V_{IN} = V_{IH}, V_{IL}
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND (Note 3)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 3: I_{CC} for 54ACT is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = 25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0	120	125		95		110		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	12.5	1.0	16.5	4.0	14.0	ns	2-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	13.5	1.0	17.0	4.5	15.0	ns	2-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0	5.0	8.5	12.5	1.0	16.5	4.5	14.5	ns	2-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0	6.0	10.0	14.5	1.0	18.0	5.0	16.0	ns	2-6
t_{PZH}	Output Enable Time	5.0	3.5	7.5	11.0	1.0	15.0	3.0	12.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	1.0	15.5	3.0	13.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	1.0	15.5	3.0	13.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	1.0	15.0	2.5	12.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = 25°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	6.0	5.0	ns	2-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	1.5	ns	2-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	1.0	4.0	4.5	4.5	ns	2-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0	1.0	1.0	1.0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	1.0	2.5	3.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0	1.0	1.0	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	170	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54AC/74AC350 • 54ACT/74ACT350
4-Bit Shifter with TRI-STATE® Outputs

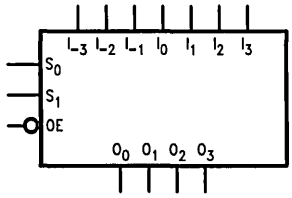
General Description

The 'AC/'ACT350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the TRI-STATE outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'AC/'ACT350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

Features

- Linking inputs for word expansion
- TRI-STATE ouputs for extending shift range
- 'ACT350 has TTL-compatible inputs

Logic Symbols



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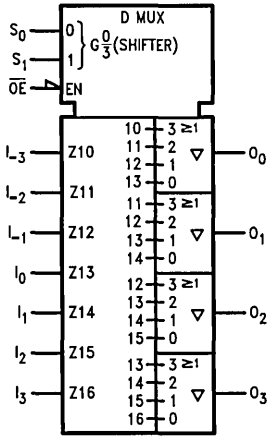
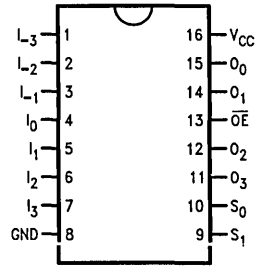
IEEE/IEC



TL/F/9957–4

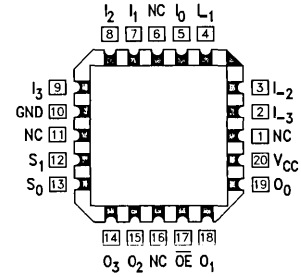
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9957–2

Pin Assignment for LCC



TL/F/9957–3

Pin Names	Description
S_0, S_1	Select Inputs
I_{-3}–I_3	Data Inputs
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_3	TRI-STATE Outputs

4

National Semiconductor

54AC/74AC373 • 54ACT/74ACT373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

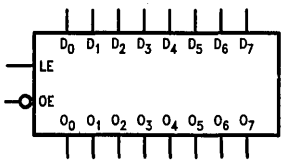
The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs

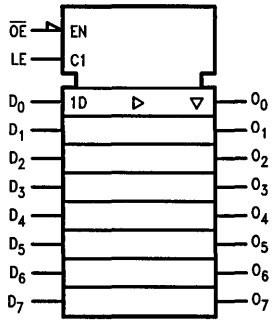
Ordering Code: See Section 5

Logic Symbols



TL/F/9958–1

IEEE/IEC

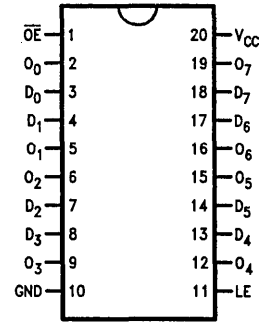


TL/F/9958–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

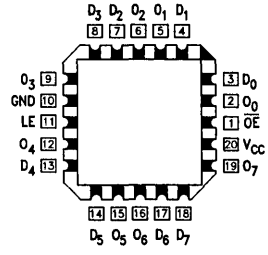
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9958–3

Pin Assignment for LCC



TL/F/9958–4

Functional Description

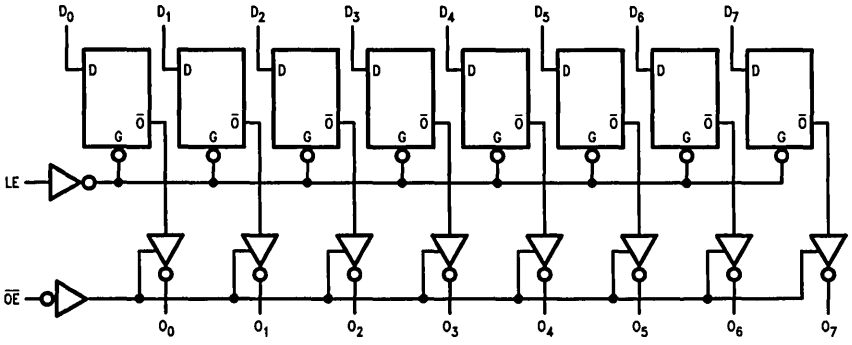
The 'AC/'ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3	1.5	10.0	13.5	1.0	16.5	1.5	15.0	ns	2-5
		5.0	1.5	7.0	9.5	1.0	11.5	1.5	10.5		
t_{PHL}	Propagation Delay D_n to O_n	3.3	1.5	9.5	13.0	1.0	16.0	1.5	14.5	ns	2-5
		5.0	1.5	7.0	9.5	1.0	11.5	1.5	10.5		
t_{PLH}	Propagation Delay LE to O_n	3.3	1.5	10.0	13.5	1.0	16.5	1.5	15.0	ns	2-6
		5.0	1.5	7.5	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay LE to O_n	3.3	1.5	9.5	12.5	1.0	15.0	1.5	14.0	ns	2-6
		5.0	1.5	7.0	9.5	1.0	11.0	1.5	10.5		
t_{PZH}	Output Enable Time	3.3	1.5	9.0	11.5	1.0	14.0	1.0	13.0	ns	2-7
		5.0	1.5	7.0	8.5	1.0	10.5	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	1.5	8.5	11.5	1.0	13.5	1.0	13.0	ns	2-8
		5.0	1.5	6.5	8.5	1.0	10.0	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.5	10.0	12.5	1.0	16.0	1.0	14.5	ns	2-7
		5.0	1.5	8.0	11.0	1.0	13.5	1.0	12.5		
t_{PLZ}	Output Disable Time	3.3	1.5	8.0	11.5	1.0	13.0	1.0	12.5	ns	2-8
		5.0	1.5	6.5	8.5	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	3.5	5.5	6.5	6.0	ns	2-9
		5.0	2.0	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	−3.0	1.0	1.0	1.0	ns	2-9
		5.0	−1.5	1.0	1.0	1.0		
t_w	LE Pulse Width, HIGH	3.3	4.0	5.5	6.5	6.0	ns	2-6
		5.0	2.0	4.0	5.0	4.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	8.5	10.0	1.0	12.5	1.5	11.5	ns	2-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.0	8.0	10.0	1.0	12.5	1.5	11.5	ns	2-5
t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	8.5	11.0	1.0	12.5	2.0	11.5	ns	2-6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.0	8.0	10.0	1.0	11.5	1.5	11.5	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.0	11.5	1.5	10.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.0	11.0	1.5	10.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.5	9.0	11.0	1.0	14.0	2.5	12.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.0	11.0	1.0	10.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	7.0	8.5	8.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	0	1.0	1.0	ns	2-9
t_w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.5	8.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC374 • 54ACT/74ACT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

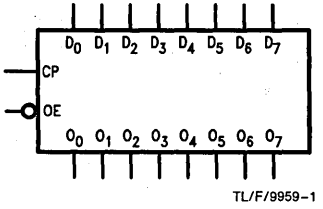
The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs

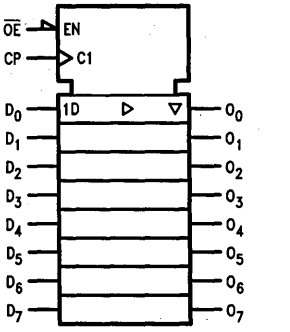
Ordering Code: See Section 5

Logic Symbols



TL/F/9959–1

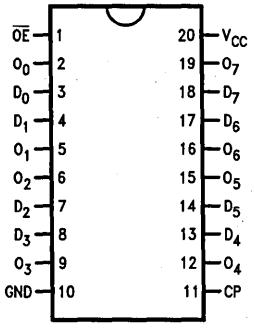
IEEE/IEC



TL/F/9959–2

Connection Diagrams

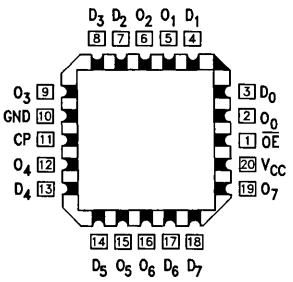
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9959–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC and PCC



TL/F/9959–4

Functional Description

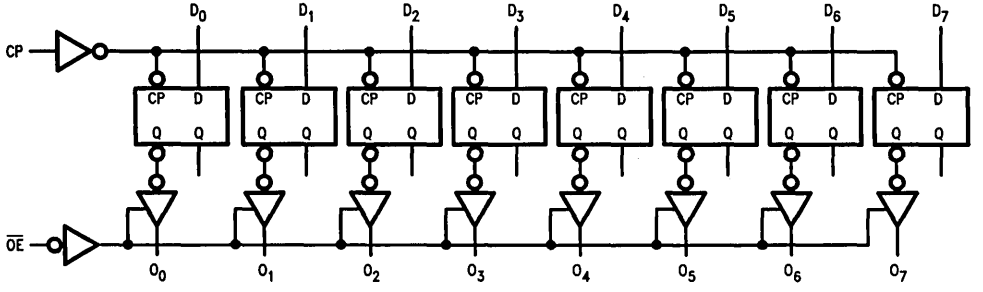
The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9959–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	60	110		60		60		MHz	2-3
		5.0	100	155		95		100			
t_{PLH}	Propagation Delay CP to O_n	3.3	3.0	11.0	13.5	1.0	16.5	1.5	15.5	ns	2-6
		5.0	2.5	8.0	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay CP to O_n	3.3	2.5	10.0	12.5	1.0	15.0	2.0	14.0	ns	2-6
		5.0	2.0	7.0	9.0	1.0	11.0	1.5	10.0		
t_{PZH}	Output Enable Time	3.3	3.0	9.5	11.5	1.0	14.0	1.5	13.0	ns	2-7
		5.0	2.0	7.0	8.5	1.0	10.5	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	2.5	9.0	11.5	1.0	14.0	1.5	13.0	ns	2-8
		5.0	2.0	6.5	8.5	1.0	10.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	3.0	10.5	12.5	1.0	16.0	2.0	14.5	ns	2-7
		5.0	2.0	8.0	11.0	1.0	12.5	2.0	12.5		
t_{PLZ}	Output Disable Time	3.3	2.0	8.0	11.5	1.0	13.0	1.0	12.5	ns	2-8
		5.0	1.5	6.5	8.5	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	2.0	5.5	6.5	6.0	ns	2-9
		5.0	1.0	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	−1.0	1.0	1.0	1.0	ns	2-9
		5.0	0	1.5	1.5	1.5		
t_w	CP Pulse Width, HIGH or LOW	3.3	4.0	5.5	6.5	6.0	ns	2-6
		5.0	2.5	4.0	5.0	4.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	160		70		90		MHz	2-3
t_{PLH}	Propagation Delay CP to O_n	5.0	2.0	8.5	10.0	1.0	12.0	2.0	11.5	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	8.0	9.5	1.0	11.5	1.5	11.0	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.0	11.5	1.5	10.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	1.5	8.0	9.0	1.0	11.5	1.5	10.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	8.5	11.5	1.0	13.0	1.0	12.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	1.5	7.0	8.5	1.0	11.0	1.0	10.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	7.0	8.5	8.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	1.5	ns	2-9
t_w	CP Pulse Width, HIGH or LOW	5.0	2.5	7.0	8.5	8.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	80.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC377 • 54ACT/74ACT377
Octal D Flip-Flop with Clock Enable

General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

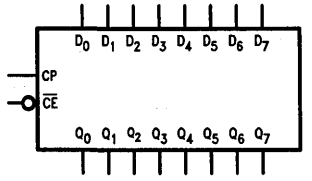
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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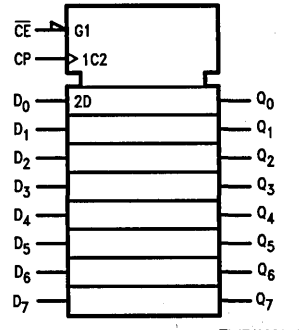
IEEE/IEC



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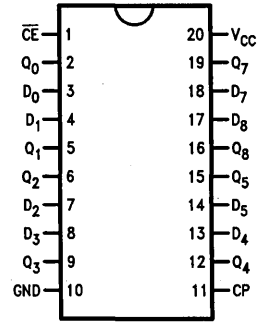
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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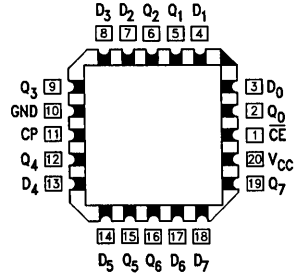
Pin Assignment for LCC



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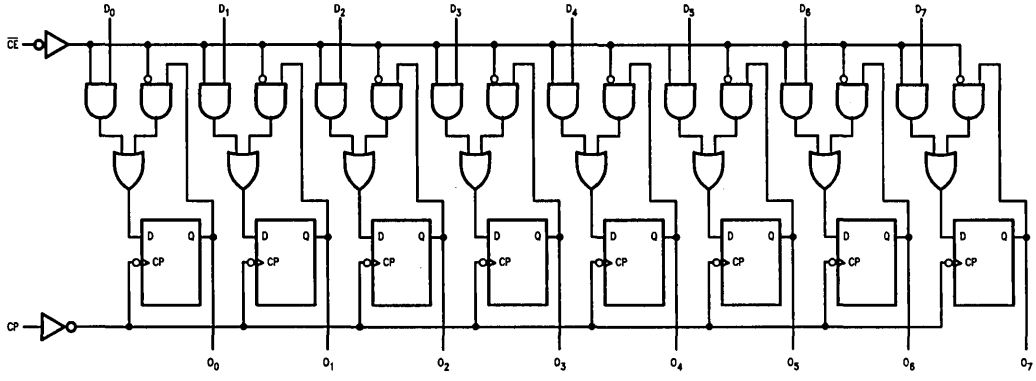
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	↗	L	H	H
Load '0'	↗	L	L	L
Hold (Do Nothing)	↗	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		I_{OH} −24 mA
					2.46		−24 mA
					3.76		
					4.76		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		24 mA
					0.44		24 mA
					0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
					±1.0		

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	90	125		75		75		MHz	2-3
		5.0	140	175		95		125			
t_{PLH}	Propagation Delay CP to Q_n	3.3	3.0	8.0	13.0	1.0	14.0	1.5	14.0	ns	2-6
		5.0	2.0	6.0	9.0	1.0	10.0	1.5	10.0		
t_{PHL}	Propagation Delay CP to Q_n	3.3	3.5	8.5	13.0	1.0	15.0	2.0	14.5	ns	2-6
		5.0	2.5	6.5	10.0	1.0	11.0	1.5	11.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	3.5	5.5	7.5	6.0	ns	2-9
		5.0	2.5	4.0	6.0	4.5		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	−2.0	0	1.5	0	ns	2-9
		5.0	−1.0	1.0	2.5	1.0		
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3	4.0	6.0	9.5	7.5	ns	2-9
		5.0	2.5	4.0	6.0	4.5		
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3	−3.5	0	1.0	0	ns	2-9
		5.0	−2.0	1.0	2.0	1.0		
t_w	CP Pulse Width HIGH or LOW	3.3	3.5	5.5	6.5	6.0	ns	2-6
		5.0	2.5	4.0	5.0	4.5		

*Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	140	175		85		125		MHz	2-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	3.0	6.5	9.0	1.0	11.0	2.5	10.0	ns	2-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	3.5	7.0	10.0	1.0	12.0	2.5	11.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	4.5	7.0	5.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	1.0	1.0	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0	2.5	4.5	7.0	5.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0	−1.0	1.0	1.0	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.5	4.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	90.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT381
4-Bit Arithmetic Logic Unit

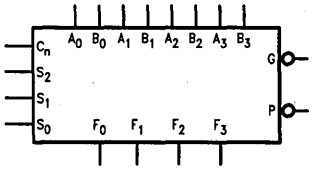
General Description

The 'ACT381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 'AC/'ACT182 carry lookahead generator for high-speed expansion to longer word lengths.

Features

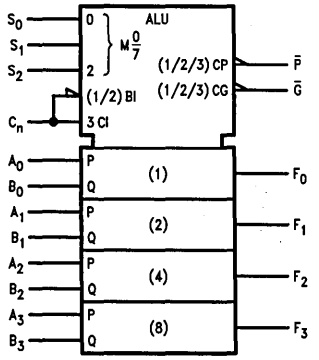
- Low input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Carry generate and propagate outputs for use with carry lookahead generator
- 'ACT381 has TTL-compatible inputs

Logic Symbols



TL/F/9962–1

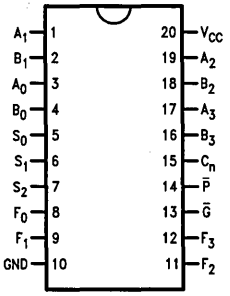
IEEE/IEC



TL/F/9962–4

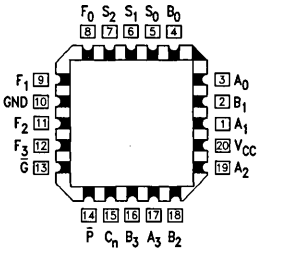
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9962–2

Pin Assignment for LCC



TL/F/9962–3

Pin Names	Description
A_0–A_3	A Operand Inputs
B_0–B_3	B Operand Inputs
S_0–S_2	Function Select Inputs
C_n	Carry Input
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
F_0–F_3	Function Outputs

National Semiconductor

54ACT/74ACT399
Quad 2-Port Register

General Description

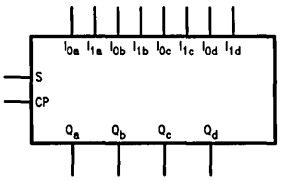
The 'ACT399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock.

Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Outputs source/sink 24 mA
- 'ACT399 has TTL-compatible inputs

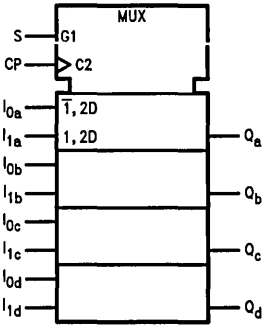
Ordering Code: See Section 5

Logic Symbols



TL/F/9789-1

IEEE/IEC

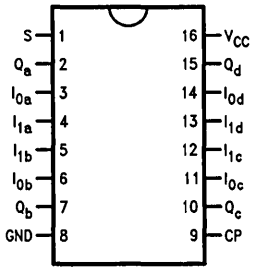


TL/F/9789-5

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Q_a–Q_d	Register True Outputs

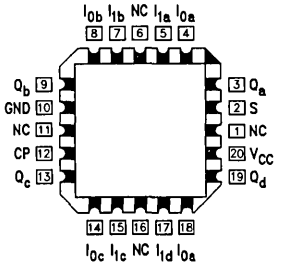
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9789-3

Pin Assignment for LCC



TL/F/9789-2

Functional Description

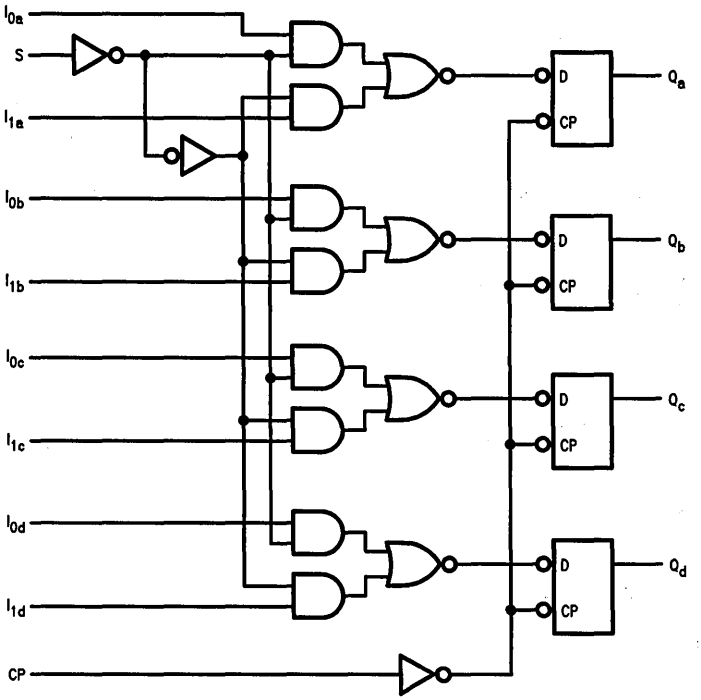
The 'ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

Function Table

Inputs				Outputs	
S	I_0	I_1	CP	Q	$\overline{Q}$
L	L	X	↗	L	H
L	H	X	↗	H	L
H	X	L	↗	L	H
H	X	H	↗	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9789–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	+175°C
PDIP	+140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.85	4.70	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or Ground (Note 3)

Note 3: I_{CC} for the 54ACT device is identical to the 74ACT device at 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ACT T_A, V_{CC} = Mil, $C_L = 50$ pF		74ACT T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Input Clock Frequency	5.0	165	160		90		160		MHz	2–3
t_{PLH}	Propagation Delay CP to Q	5.0	1.5	7.0	8.0		10.0	1.5	8.5	ns	2–6
t_{PHL}	Propagation Delay CP to Q	5.0	2.0	6.0	9.0		10.0	2.0	9.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW I_n to CP	5.0	3.0	2.5	3.5	2.5	ns	2–9
t_h	Hold Time, HIGH or LOW I_n to CP	5.0	0	1.0	3.0	1.0	ns	2–9
t_s	Setup Time, HIGH or LOW S to CP	5.0	3.0	4.0	6.0	4.0	ns	2–9
t_h	Hold Time, HIGH or LOW S to CP	5.0	−1.0	0.5	2.5	0.5	ns	2–9
t_w	CP Pulse Width HIGH or LOW	5.0	5.5	3.5	5.0	3.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC520 • 54ACT/74ACT520
8-Bit Identity Comparator

General Description

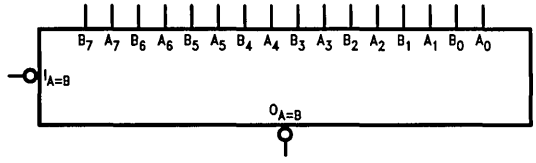
The 'AC/'ACT520 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT520 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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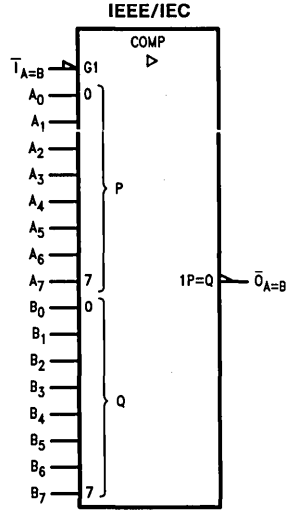
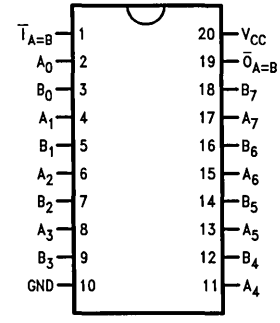


TL/F/10194–4

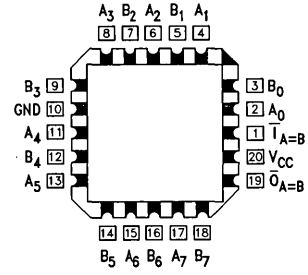
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10194–2

Pin Assignment for LCC



TL/F/10194–3

Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$T_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

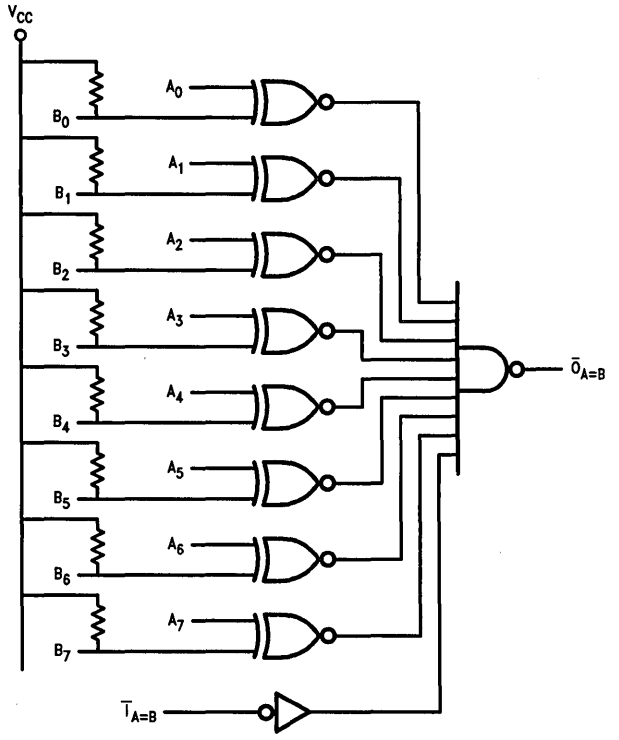
4

Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



TL/F/10194–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.0	7.5	11.5			3.0	13.0	ns	2-6
		5.0	2.5	5.5	8.5			2.0	9.5		
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.5	8.0	12.0			3.5	13.5	ns	2-6
		5.0	3.0	5.5	9.0			2.5	10.0		
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5			2.5	9.5	ns	2-6
		5.0	2.5	4.5	6.5			2.0	7.0		
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5			2.5	9.5	ns	2-6
		5.0	2.5	4.5	6.5			2.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	5.5	8.5			2.5	9.5	ns	2-6
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	6.0	10.0			2.5	11.5	ns	2-6
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.0	4.0	6.0			2.0	6.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.5	5.0	7.5			2.0	8.5	ns	2-6

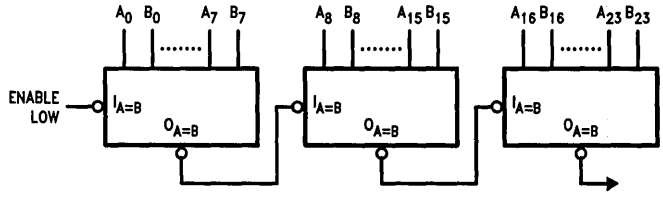
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V

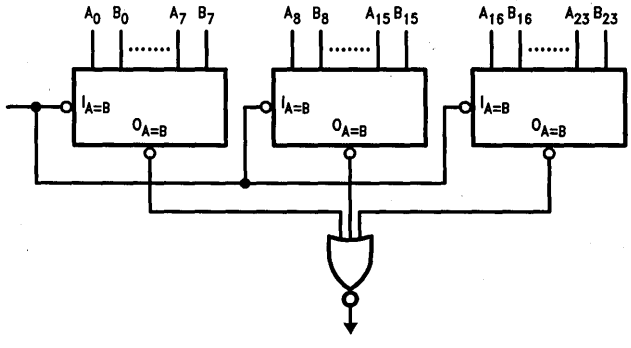
Applications

Ripple Expansion



TL/F/10194–6

Parallel Expansion



TL/F/10194–7

National Semiconductor

54AC/74AC521 • 54ACT/74ACT521
8-Bit Identity Comparator

General Description

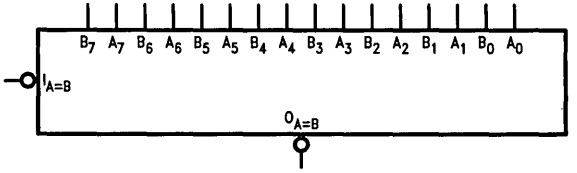
The 'AC/'ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT521 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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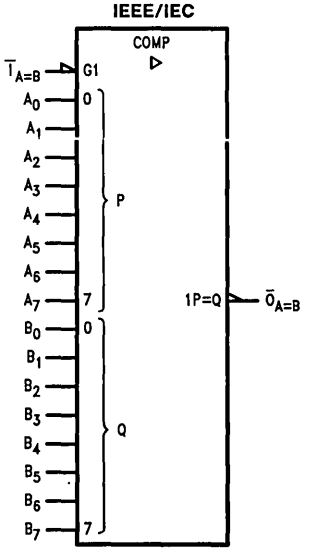
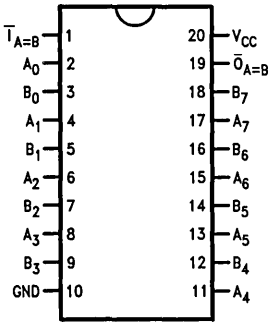


TL/F/9964-4

Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$\overline{T}_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

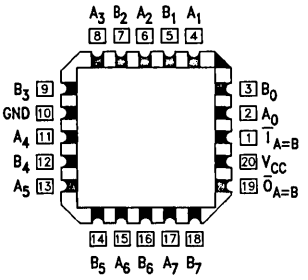
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9964-2

Pin Assignment for LCC



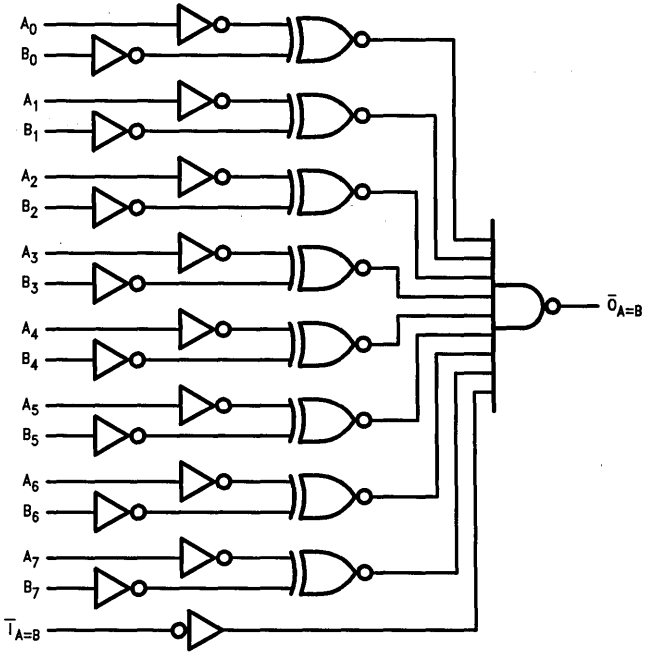
TL/F/9964-3

Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	3.5	7.0	11.0			3.0	12.0	ns	2-6
		5.0	2.5	5.0	8.0			2.0	9.0		
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.5	7.5	11.5			3.5	12.5	ns	2-6
		5.0	3.0	5.5	8.5			2.5	9.0		
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.0	5.5	8.0			2.5	9.0	ns	2-6
		5.0	2.5	4.0	6.0			2.0	7.0		
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.0	5.5	8.0			2.5	9.0	ns	2-6
		5.0	2.0	4.0	6.0			2.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	5.5	9.0			2.5	9.5	ns	2-6
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	6.0	10.0			2.5	11.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.0	4.0	6.5			2.0	7.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.5	5.0	7.5			2.0	8.0	ns	2-6

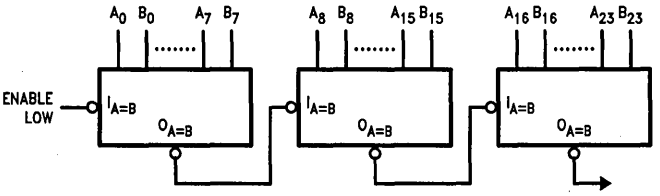
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0V$

Applications

Ripple Expansion



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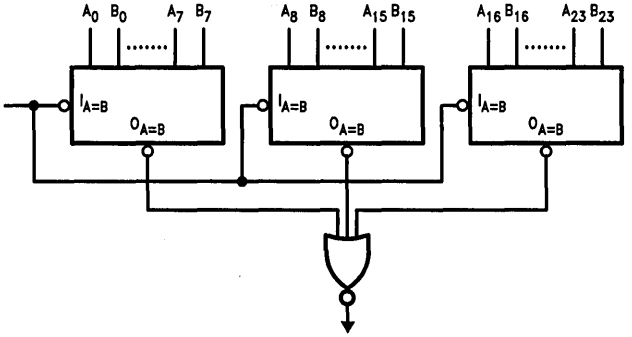
Parallel Expansion



TL/F/9964–7

National Semiconductor

54ACT/74ACT534
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

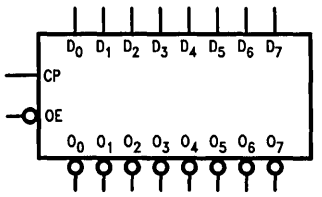
The 'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374

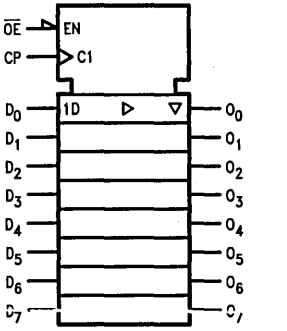
Ordering Code: See Section 5

Logic Symbols



TL/F/9965–1

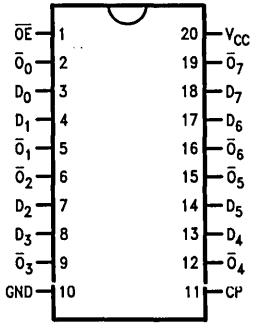
IEEE/IEC



TL/F/9965–2

Connection Diagrams

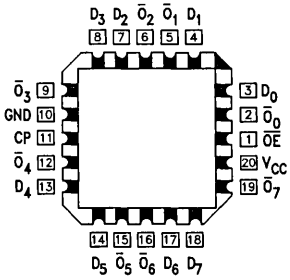
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9965–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Pin Assignment for LCC

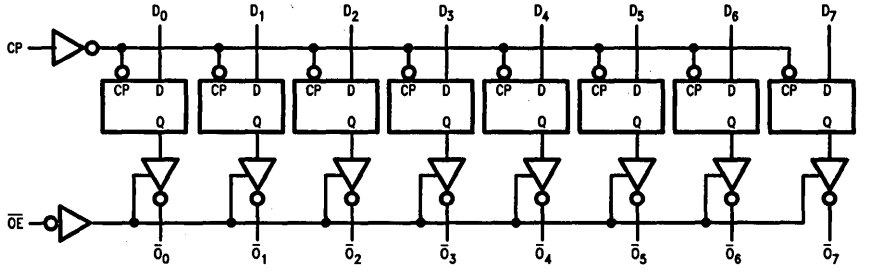


TL/F/9965–4

Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



TL/F/9965–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐	L	H	L
⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100		85		120		MHz	2-3
t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.5	6.5	11.5	1.0	14.0	2.0	12.5	ns	2-6
t_{PHL}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.0	6.0	10.5	1.0	13.0	2.0	12.0	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.5	6.5	12.0	1.0	14.0	2.0	12.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	6.0	11.0	1.0	13.0	2.0	11.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	12.5	1.0	14.5	1.0	13.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	1.5	5.5	10.5	1.0	11.5	1.0	10.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	3.5	5.0	4.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	3.0	1.5	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	3.5	5.0	3.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC540 • 54ACT/74ACT540
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 'AC/'ACT240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

The information for the 'ACT540 is Advanced Information only.

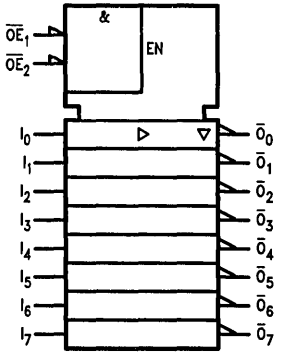
Features

- TRI-STATE inverting outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'ACT540 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol

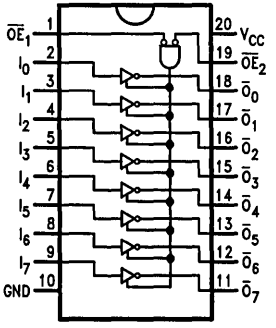
IEEE/IEC



TL/F/9966-1

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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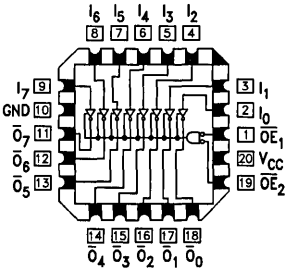
Pin Assignment for LCC



TL/F/9966-2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	5.5	7.5	1.0	9.0	1.0	8.0	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	5.0	7.0	1.0	8.0	1.0	7.5	ns	2-5
		5.0	1.5	4.0	5.5	1.0	6.5	1.0	6.0		
t_{PZH}	Output Enable Time	3.3	3.0	8.5	11.0	1.0	13.0	2.5	12.0	ns	2-7
		5.0	2.0	6.5	8.5	1.0	10.0	2.0	9.5		
t_{PZL}	Output Enable Time	3.3	2.5	7.5	10.0	1.0	12.0	2.0	11.0	ns	2-8
		5.0	2.0	6.0	7.5	1.0	9.0	1.5	8.5		
t_{PHZ}	Output Disable Time	3.3	2.5	8.5	13.0	1.0	15.5	1.5	14.0	ns	2-7
		5.0	1.5	7.5	10.5	1.0	12.0	1.0	11.0		
t_{PLZ}	Output Disable Time	3.3	2.5	7.0	10.0	1.0	12.0	2.0	11.0	ns	2-8
		5.0	1.5	6.0	8.0	1.0	10.0	1.5	9.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC541 • 54ACT/74ACT541
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'AC/'ACT541 is a noninverting option of the 'AC/'ACT540.

This device is similar in function to the 'AC/'ACT244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The Information for the ACT541 is Advanced Information only.

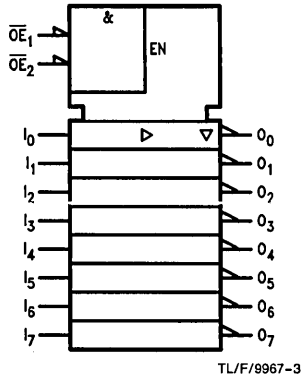
Features

- TRI-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'ACT541 has TTL-compatible inputs
- 'AC/'ACT540 provides inverted outputs

Ordering Code: See Section 5

Logic Symbol

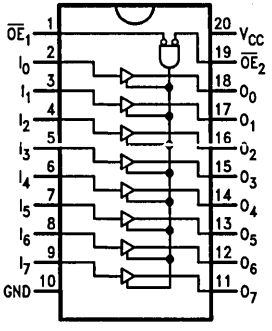
IEEE/IEC



TL/F/9967-3

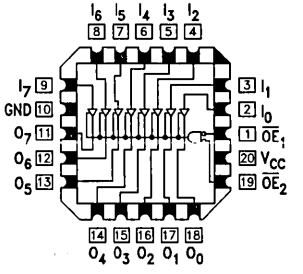
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9967-2

Pin Assignment for LCC



TL/F/9967-1

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	2.0	5.5	8.0	1.0	10.0	1.5	9.0	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay Data to Output	3.3	2.0	5.5	8.0	1.0	9.5	1.5	8.5	ns	2-5
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PZH}	Output Enable Time	3.3	3.0	8.0	11.5	1.0	13.5	3.0	12.5	ns	2-7
		5.0	2.0	6.0	8.5	1.0	10.0	1.5	9.5		
t_{PZL}	Output Enable Time	3.3	2.5	7.0	10.0	1.0	12.5	2.5	11.5	ns	2-8
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHZ}	Output Disable Time	3.3	3.5	9.0	12.5	1.0	15.0	2.5	14.0	ns	2-7
		5.0	2.0	7.0	9.5	1.0	12.0	1.0	10.5		
t_{PLZ}	Output Disable Time	3.3	2.5	6.5	9.5	1.0	11.0	2.0	10.5	ns	2-8
		5.0	2.0	5.5	7.5	1.0	9.0	1.0	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT543 Octal Registered Transceiver

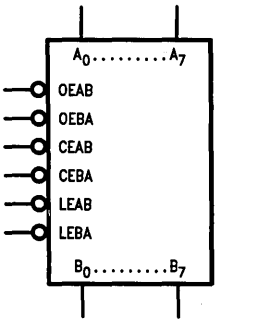
General Description

The 'ACT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Features

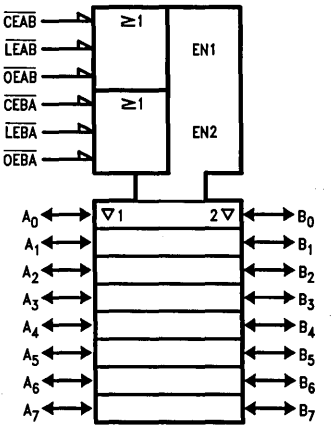
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 300 mil slim package
- 'ACT543 has TTL-compatible inputs

Logic Symbols



TL/F/9968-1

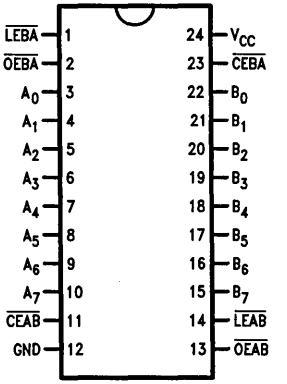
IEEE/IEC



TL/F/9968-2

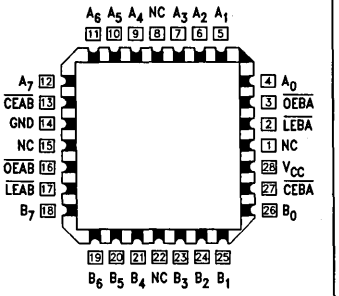
Connection Diagrams

Pin Assignment for DIP and SOIC



TL/F/9968-3

Pin Assignment for LCC



TL/F/9968-4

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT544
Octal Registered Transceiver

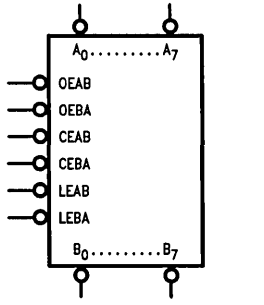
General Description

The 'ACT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'ACT544 inverts data in both directions.

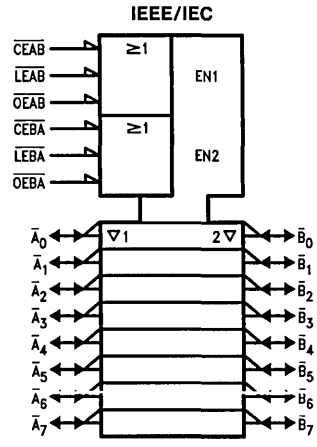
Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 300 mil slim package
- 'ACT544 has TTL-compatible inputs

Logic Symbols



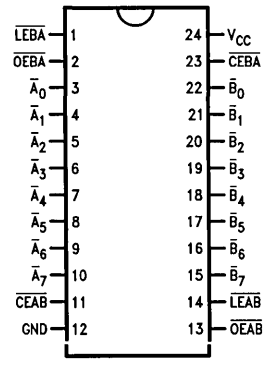
TL/F/9969–1



TL/F/9969–2

Connection Diagrams

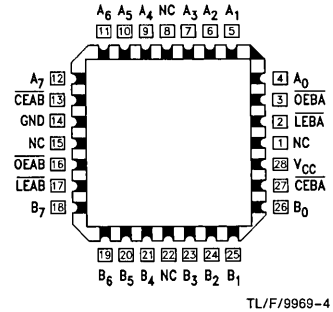
Pin Assignment for DIP and SOIC



TL/F/9969–3

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$\overline{A}_0$–$\overline{A}_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
$\overline{B}_0$–$\overline{B}_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Pin Assignment for LCC



TL/F/9969–4

National Semiconductor

54ACT/74ACT563
Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

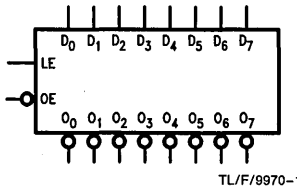
The 'ACT563 device is functionally identical to the 'ACT573, but with inverted outputs.

Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs

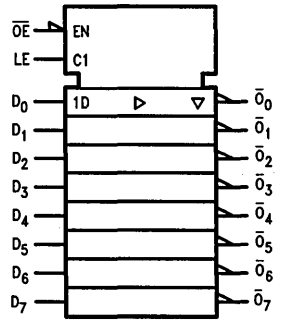
Ordering Code: See Section 5

Logic Symbols



TL/F/9970–1

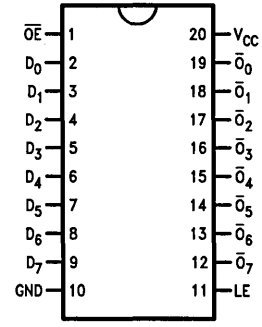
IEEE/IEC



TL/F/9970–2

Connection Diagrams

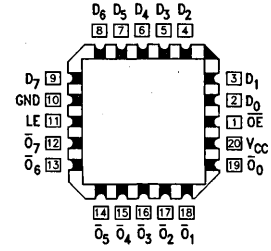
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9970–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/9970–4

Functional Description

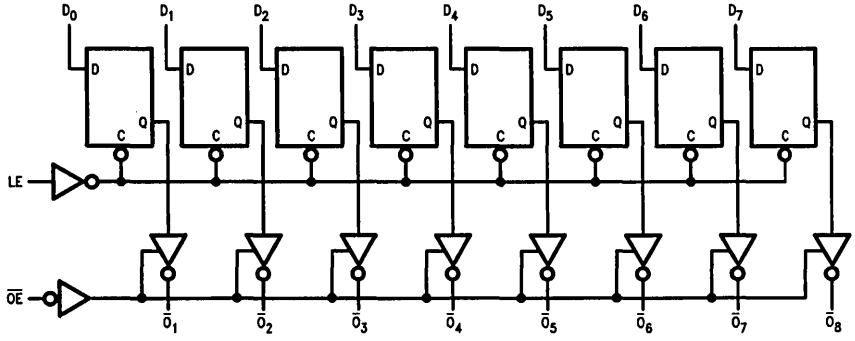
The 'ACT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9970–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	7.0	11.5	1.0	14.5	2.5	12.5	ns	2-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	6.0	10.0	1.0	12.0	2.5	11.0	ns	2-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	3.0	6.5	10.5	1.0	12.5	2.5	11.5	ns	2-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.5	5.5	9.0	1.0	11.5	2.0	10.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	5.5	8.5	1.0	11.0	2.0	9.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	3.5	6.5	10.5	1.0	12.0	2.5	11.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	4.0	4.5	4.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	1.5	0	ns	2-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	5.0	3.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54ACT/74ACT564
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

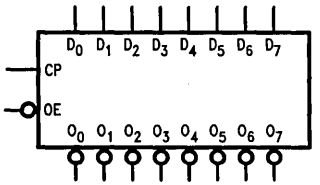
The 'ACT564 device is functionally identical to the 'ACT574, but with inverted outputs.

Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT574 but with inverted outputs
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT564 has TTL-compatible inputs

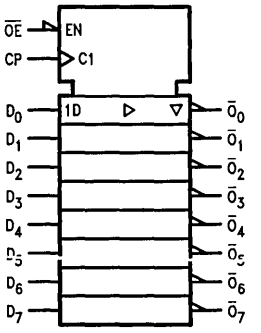
Ordering Code: See Section 5

Logic Symbols



TL/F/9972–1

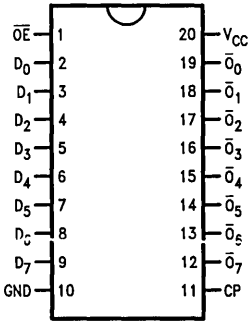
IEEE/IEC



TL/F/9972–2

Connection Diagrams

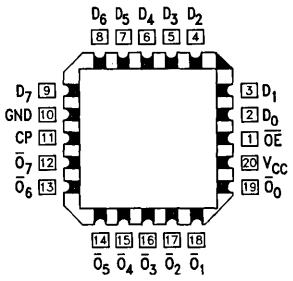
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9972–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/9972–4

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85	90		65		75		MHz	2-3
t_{PLH}	Propagation Delay, CP to $\overline{O}_n$	5.0	2.0	6.5	10.5	1.0	12.5	1.5	11.5	ns	2-6
t_{PHL}	Propagation Delay, CP to $\overline{O}_n$	5.0	1.5	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PZH}	Output Enable Time	5.0	1.5	5.5	9.0	1.0	10.5	1.5	9.5	ns	2-7
t_{PZL}	Output Enable Time	5.0	1.5	5.5	8.5	1.0	10.5	1.0	9.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	1.5	5.0	8.0	1.0	9.5	1.0	8.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	2.5	3.5	3.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	2.5	1.0	ns	2-9
t_w	LE Pulse Width, HIGH or LOW	5.0	2.5	3.0	5.0	3.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT573
Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

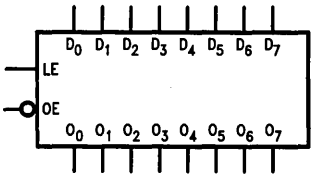
The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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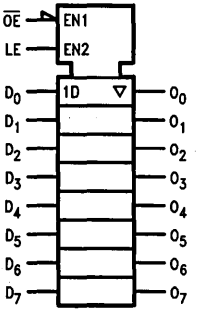
IEEE/IEC

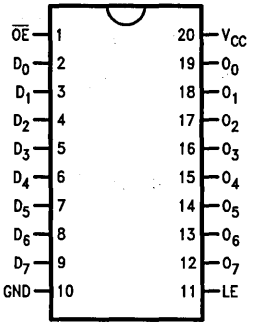


TL/F/9973–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

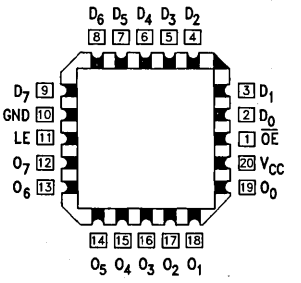
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9973–3

Pin Assignment for LCC



TL/F/9973–4

Functional Description

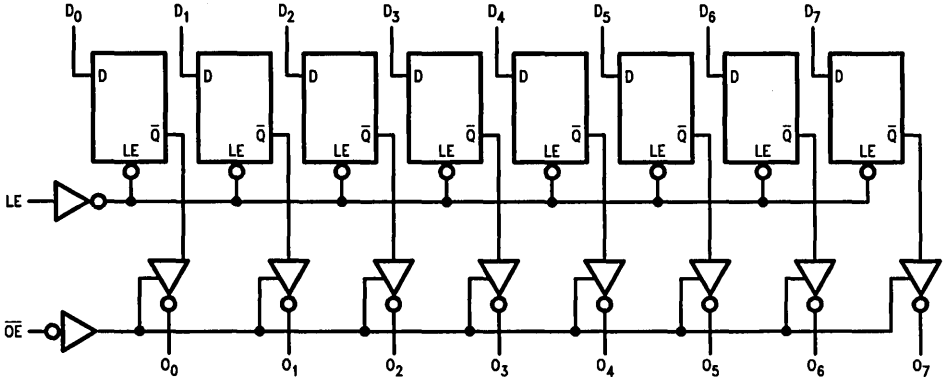
The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/9973–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.70	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_m to O_n	5.0	2.5	6.0	10.5	1.0	13.5	2.0	12.0	ns	2-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	6.0	10.5	1.0	13.5	2.0	12.0	ns	2-5
t_{PLH}	Propagation Delay LE to O_n	5.0	3.0	6.0	10.5	1.0	13.0	2.5	12.0	ns	2-6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.5	1.0	12.0	2.0	10.5	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	5.5	10.0	1.0	11.5	1.5	11.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.5	6.5	11.0	1.0	13.5	1.5	12.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	1.5	5.0	8.5	1.0	10.5	1.0	9.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	3.0	4.5	3.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5	0	1.0	0	ns	2-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	5.0	4.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	25.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC574 • 54ACT/74ACT574
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

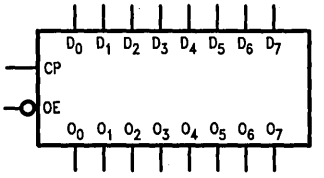
The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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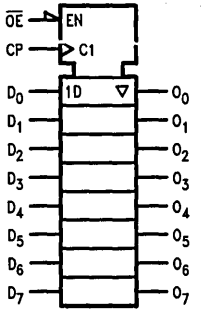
IEEE/IEC



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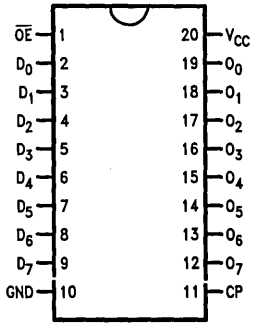
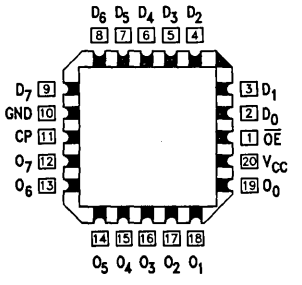
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9910–2

Pin Assignment for LCC



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Functional Description

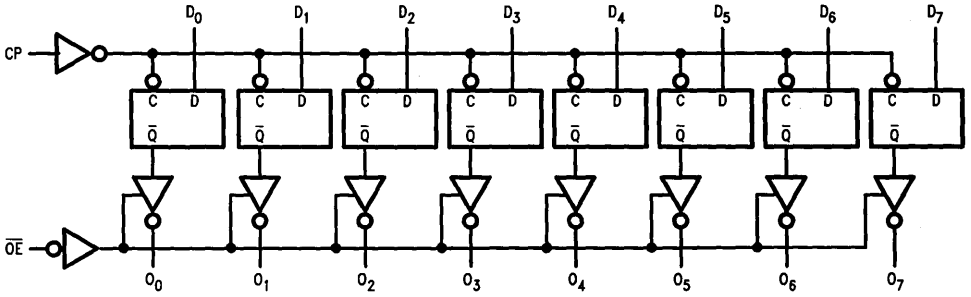
The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- (Unless Otherwise Specified) (AC) 2.0V to 6.0V
- (ACT) 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V,
V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.32	0.4	0.37	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.32	0.4	0.37		I_{OL} 24 mA
		5.5		0.32	0.4	0.37		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$ Typ	74AC $T_A = 25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			57	86	mA	V_{OLD} = 1.1V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = 25°C$ Typ	74ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.32 0.32	0.4 0.4	0.37 0.37	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			57	86	mA	V_{OLD} = 1.1V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3	75	112		55		60		MHz	
		5.0	95	153		80		85			
t_{PLH}	Propagation Delay CP to O_n	3.3	3.5	8.5	13.5	1.0	16.5	3.5	15.0	ns	2-6
		5.0	2.0	6.0	9.5	1.0	11.5	2.0	11.0		
t_{PHL}	Propagation Delay CP to O_n	3.3	3.5	7.5	12.0	1.0	15.0	3.5	13.5	ns	2-6
		5.0	2.0	5.5	8.5	1.0	10.5	2.0	9.5		
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.0	1.0	13.0	2.5	12.0	ns	2-7
		5.0	2.0	5.0	8.5	1.0	9.5	2.0	9.0		
t_{PZL}	Output Enable Time	3.3	3.0	6.5	10.5	1.0	12.5	3.5	11.5	ns	2-8
		5.0	1.5	5.0	8.0	1.0	9.5	2.0	9.0		
t_{PHZ}	Output Disable Time	3.3	4.0	7.5	12.0	1.0	14.0	4.5	13.0	ns	2-7
		5.0	2.0	6.0	9.5	1.0	11.0	2.0	10.5		
t_{PLZ}	Output Disable Time	3.3	2.0	5.5	9.0	1.0	10.5	2.5	10.0	ns	2-8
		5.0	1.5	4.5	7.5	1.0	9.0	1.5	8.5		

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-Up Time, HIGH or LOW D_n to CP	3.3	0.5	2.5	3.0	3.0	ns	2-9
		5.0	0	1.5	2.0	2.0		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	−0.5	1.5	1.5	1.5	ns	2-9
		5.0	0	1.5	1.5	1.5		
t_w	CP Pulse Width HIGH or LOW	3.3	3.5	6.0	7.5	7.0	ns	2-6
		5.0	2.0	4.0	5.5	5.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	5.0	100	110		70		85		ns	
t_{PLH}	Propagation Delay CP to O_n	5.0	2.5	7.0	11.0	1.0	13.5	2.0	12.0	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	6.5	10.0	1.0	12.5	1.5	11.0	ns	2-6
t_{PZH}	Output Enable Time	5.0	2.0	6.4	9.5	1.0	11.0	1.5	10.0	ns	2-7
t_{PZL}	Output Enable Time	5.0	2.0	6.0	9.0	1.0	11.0	1.5	10.0	ns	2-8
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.0	12.0	1.5	11.5	ns	2-7
t_{PLZ}	Output Disable Time	5.0	2.0	5.5	8.5	1.0	10.0	1.5	9.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-Up Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	3.5	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	2.0	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	5.0	4.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC646 • 54ACT/74ACT646
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

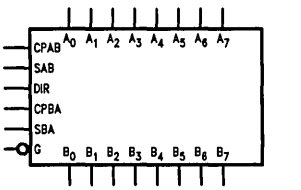
The 'AC/'ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1-4*.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs

Ordering Code: See Section 5

Logic Symbols



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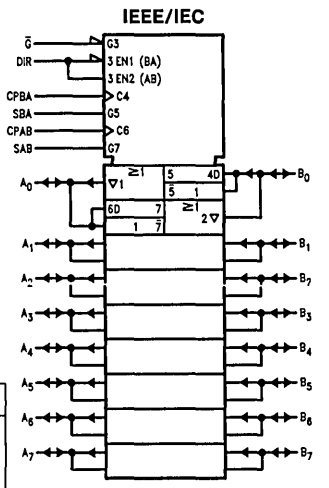
IEEE/IEC

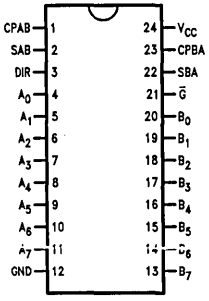


TL/F/10132–2

Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

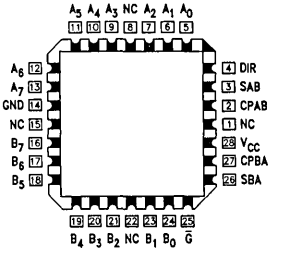
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



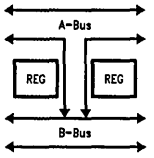
TL/F/10132–3

Pin Assignment for LCC and PCC



TL/F/10132–4

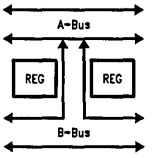
Real Time Transfer A-Bus to B-Bus



TL/F/10132–7

FIGURE 1

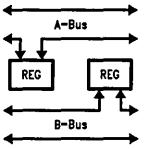
Real Time Transfer B-Bus to A-Bus



TL/F/10132–8

FIGURE 2

Storage from Bus to Register



TL/F/10132–9

FIGURE 3

Transfer from Register to Bus

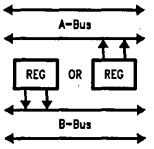


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FIGURE 4

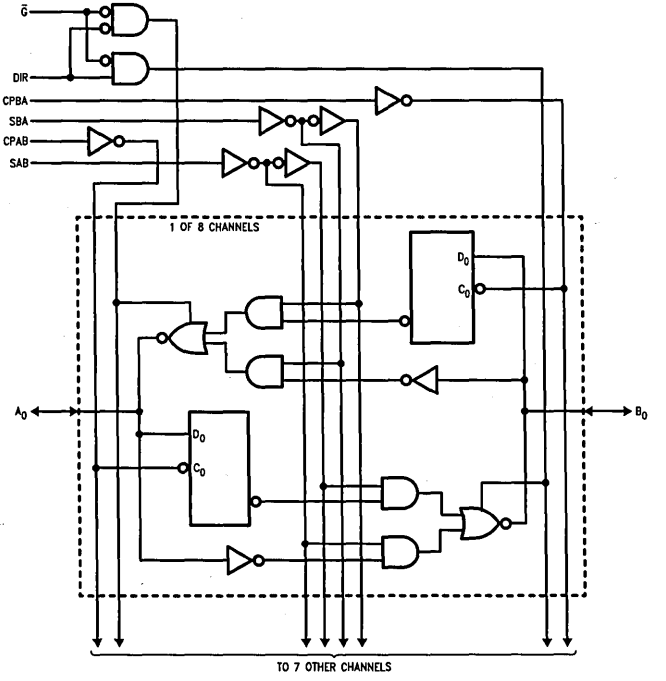
Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↓	X	X	X			Clock A_n Data into A Register
H	X	X	↓	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↓	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↓	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↓	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↓	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC $T_A = -55°C$ to $+125°C$	54AC $T_A = -40°C$ to $+85°C$	74AC	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	4.0 2.5	10.5 7.5	16.5 12.0	1.0 1.0	20.0 14.0	3.0 2.0	18.5 13.0	ns	2-6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.0 2.0	9.5 6.5	14.5 10.5	1.0 1.0	17.5 12.0	2.5 1.5	16.0 11.5	ns	2-6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	2.5 1.5	7.5 5.0	12.0 8.0	1.0 1.0	15.0 10.0	2.0 1.0	13.5 9.0	ns	2-5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	7.5 5.0	12.5 9.0	1.0 1.0	14.5 9.5	1.5 1.0	13.5 9.5	ns	2-5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	2.0 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.5 11.0	ns	2-6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.0 11.0	ns	2-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	1.0 1.0	13.0 9.5	2.0 1.5	12.5 9.0	ns	2-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	1.0 1.0	15.5 11.0	2.0 1.5	14.0 10.0	ns	2-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.0 2.0	8.0 6.5	12.5 10.0	1.0 1.0	14.0 11.5	2.5 2.0	13.5 11.0	ns	2-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.0 1.5	7.5 6.0	12.0 9.5	1.0 1.0	13.5 11.0	2.0 1.5	13.5 10.5	ns	2-8
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	2.0 1.5	6.5 5.0	11.0 7.5	1.0 1.0	14.5 10.5	1.5 1.0	12.0 8.5	ns	2-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.0	1.0 1.0	16.0 12.5	2.0 1.0	13.0 9.0	ns	2-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.5	1.0 1.0	14.5 12.0	1.5 1.5	12.5 10.0	ns	2-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.5	7.5 5.5	12.0 9.5	1.0 1.0	16.5 12.0	1.5 1.5	13.5 10.5	ns	2-8

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW Bus to Clock	3.3	2.0	5.0	6.0	5.5	ns	2-9
		5.0	1.5	4.0	4.5	4.5		
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3	−1.5	0	1.5	0	ns	2-9
		5.0	−0.5	0.5	2.0	1.0		
t_w	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	5.0	4.5	ns	2-6
		5.0	2.0	3.5	5.0	3.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.0	16.0	ns	2-6
t_{PHL}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.5	16.0	ns	2-6
t_{PLH}	Propagation Delay Bus to Bus	5.0	4.5	8.5	10.5			2.5	11.5	ns	2-5
t_{PHL}	Propagation Delay Bus to Bus	5.0	5.0	8.5	10.5			2.0	11.5	ns	2-5
t_{PLH}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-6
t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	5.0	6.0	9.0	11.0			1.5	12.0	ns	2-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	5.0	9.0	11.0			3.0	12.0	ns	2-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	7.5	10.5	13.0			4.5	14.5	ns	2-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	5.5	10.0	12.5			3.0	14.0	ns	2-8
t_{PZH}	Enable Time DIR to A_n or B_n	5.0	5.5	6.5	10.5			1.5	11.5	ns	2-7
t_{PZL}	Enable Time DIR to A_n or B_n	5.0	4.0	6.5	10.5			3.0	11.5	ns	2-8
t_{PHZ}	Disable Time DIR to A_n or B_n	5.0	5.5	8.5	12.5			4.5	13.5	ns	2-7
t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	4.0	8.5	12.5			3.0	13.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW BUS to Clock	5.0	2.5	7.0		8.0	ns	2-9
t_h	Hold Time, HIGH or LOW Bus to Clock	5.0	0	2.5		2.5	ns	2-9
t_w	Clock Pulse Width HIGH or LOW	5.0	4.5	7.0		8.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC648
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

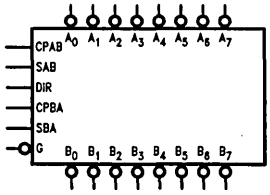
The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1* thru *4* (See Page 2).

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

Ordering Code: See Section 5

Logic Symbols



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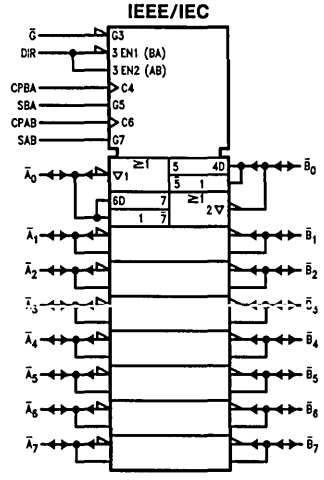
IEEE/IEC



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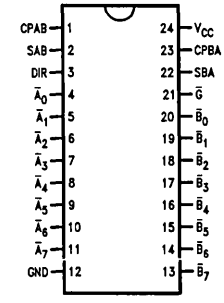
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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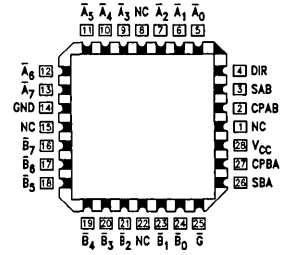
Pin Assignment for LCC and PCC



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Pin Names	Description
$\overline{A}_0$–$\overline{A}_7$	Data Register A Inputs, Data Register A TRI-STATE Outputs
$\overline{B}_0$–$\overline{B}_7$	Data Register B Inputs, Data Register B TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

Real Time Transfer
A-Bus to B-Bus

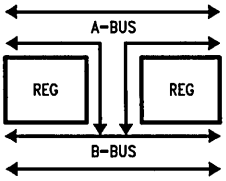

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FIGURE 1

Real Time Transfer
B-Bus to A-Bus

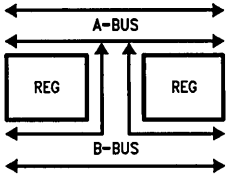

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FIGURE 2

Storage from
Bus to Register

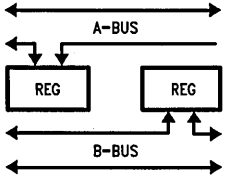

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FIGURE 3

Transfer from
Register to Bus

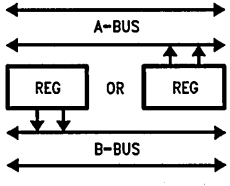

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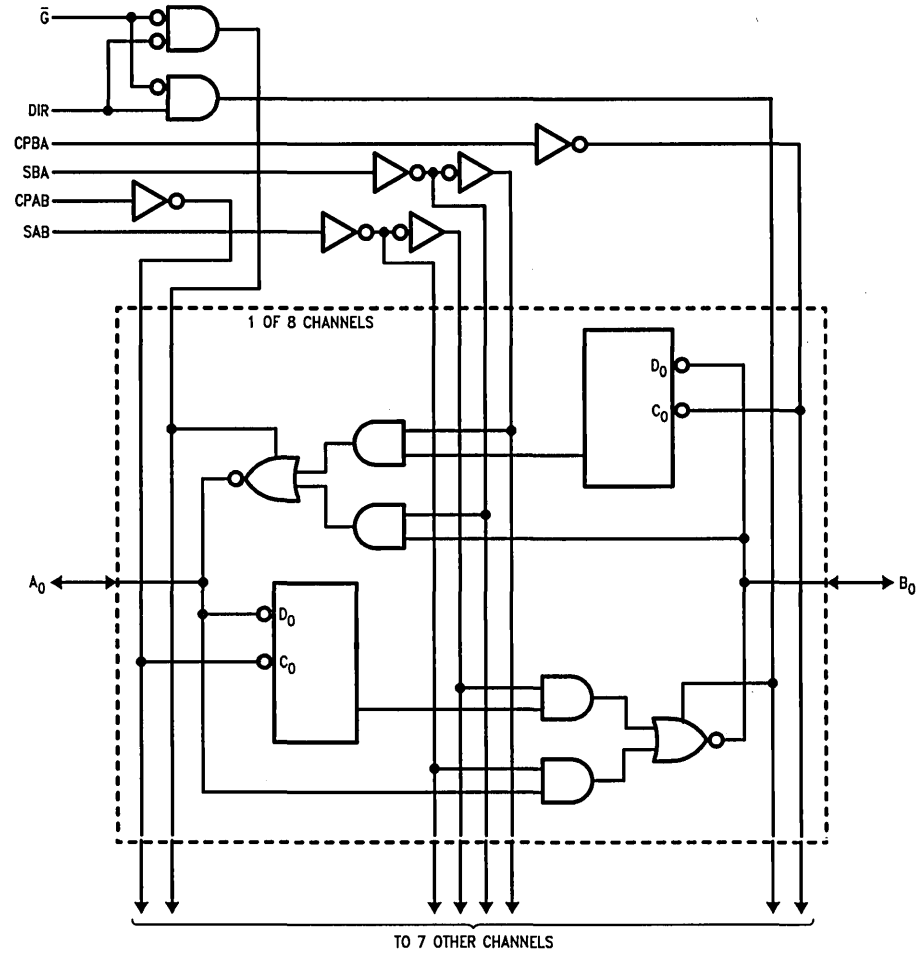
FIGURE 4

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3	1.5	10.0	15.5			1.5	17.0	ns	2-6
		5.0	1.5	7.0	11.0			1.5	12.0		
t_{PHL}	Propagation Delay Clock to Bus	3.3	1.5	8.5	13.5			1.5	14.5	ns	2-6
		5.0	1.5	6.0	10.5			1.5	11.5		
t_{PLH}	Propagation Delay Bus to Bus	3.3	1.5	6.0	10.0			1.5	11.0	ns	2-5
		5.0	1.5	4.0	7.0			1.0	7.5		
t_{PHL}	Propagation Delay Bus to Bus	3.3	1.5	5.5	9.0			1.5	10.0	ns	2-5
		5.0	1.5	3.5	7.5			1.0	8.0		
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.5	7.5	12.5			1.5	14.0	ns	2-6
		5.0	1.5	5.5	9.0			1.5	10.0		
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.5	7.5	12.5			1.5	14.0	ns	2-6
		5.0	1.5	5.5	9.5			1.5	10.5		
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.5	6.5	11.0			1.0	11.5	ns	2-7
		5.0	1.5	5.0	8.0			1.0	9.0		
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.0	11.0			1.0	12.5	ns	2-8
		5.0	1.5	5.0	8.0			1.0	9.0		
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.5	12.0			1.0	13.0	ns	2-7
		5.0	1.5	6.0	10.0			1.0	11.0		
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.0	11.5			1.0	12.5	ns	2-8
		5.0	1.5	5.5	9.0			1.0	10.0		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3	1.5	6.0	12.5			1.0	14.0	ns	2-7
		5.0	1.5	4.5	9.5			1.0	10.5		
t_{PZL}	Enable Time DIR to A_n or B_n	3.3	1.5	6.5	13.0			1.5	14.5	ns	2-8
		5.0	1.5	4.5	9.0			1.0	10.5		
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3	1.5	7.0	11.5			1.0	13.5	ns	2-7
		5.0	1.5	5.5	9.0			1.0	10.0		
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3	1.5	7.0	13.5			1.5	15.0	ns	2-8
		5.0	1.5	5.0	9.5			1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0		3.5 2.0	ns	2-9
t_h	Hold Time, HIGH or LOW, Bus to Clock	3.3 5.0	−1.5 −0.5	0 1.0		0 1.0	ns	2-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0		4.0 3.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT657
Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

General Description

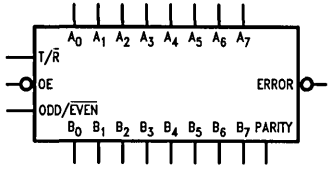
The 'ACT657 contains eight noninverting buffers with TRI-STATE outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input disables both the A and B ports by placing them in a High Z condition.

The parity generator detects whether an even or odd number of bits on the A port is HIGH, depending on the condition of the ODD/$\overline{EVEN}$ input, and the $\overline{ERROR}$ output is LOW if not equal.

Features

- 300 mil 24-pin Slimline DIP
- TRI-STATE outputs
- 'ACT657 has TTL-compatible inputs

Logic Symbols



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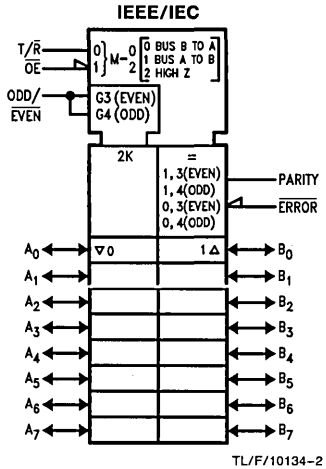
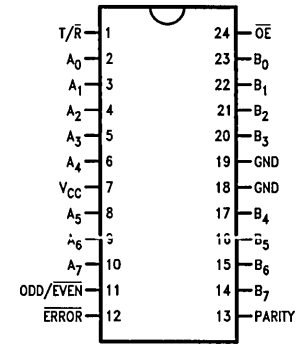


TL/F/10134-2

Pin Names	Description
A_0–A_7	Data Inputs
	Data Outputs
B_0–B_7	Data Inputs
	Data Outputs
$T/\overline{R}$	Transmit/Receive Input
$\overline{OE}$	Enable Input
PARITY	Parity Input/Output
ODD/$\overline{EVEN}$	ODD/$\overline{EVEN}$ Parity Input
$\overline{ERROR}$	Error Output

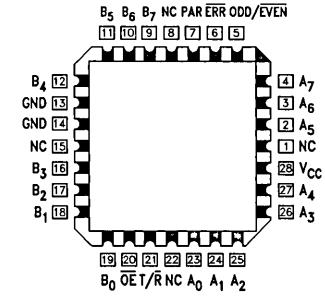
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10134-3

Pin Assignment for LCC



TL/F/10134-4

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT705 Arithmetic Logic Unit for Digital Signal Processing Applications

General Description

The 'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input buses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of TRI-STATE® output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

Features

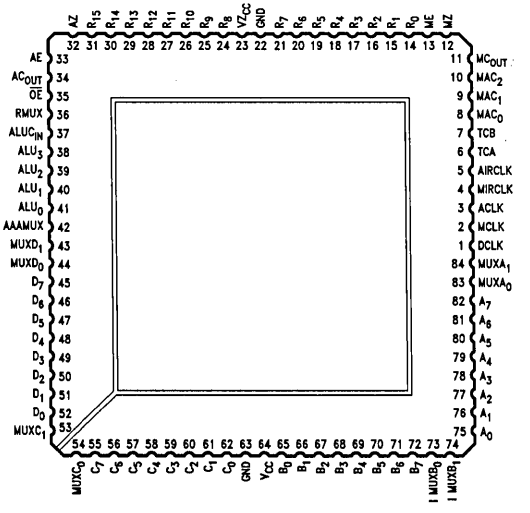
- 84-pin, PCC, CPGA
- Outputs source/sink 8 mA
- 'ACT705 has TTL-compatible inputs
- High throughput achieved with high degree of parallelism in the architecture
- Pipelined stages
- High-speed 16-bit ALU and an 8 x 8 complex multiplier
- 16-bit full ALU performs sixteen Boolean and arithmetic functions with carry-in and carry-out
- 8 x 8 parallel multiplier supports unsigned, signed, complex or mixed mode multiplications, produces 16-bit result with carry-out
- Separate data and instruction buses allow instruction fetches in parallel with execution—single cycle operation
- Accepts 8- or 16-bit data and delivers a 16-bit output
- Data register bank configured to accept a combination of 8- or 16-bit data
- Separate clocks for ALU instruction, multiplier instruction, data, ALU accumulator and multiplier accumulator registers
- Clustered clock pins for ease of board design
- 16-bit ALU/accumulator with feedback to ALU input
- Status of accumulator inputs is monitored: conditions monitored include twos complement overflow, underflow or equal-to-zero

Applications

- Voice-band signal processing
- Discrete Fourier transform applications
  - — FIR filters
  - — IIR filters
- Fast Fourier transform applications
  - — Spectrum analysis
  - — Speech recognition

Connection Diagram

Pin Assignment for PCC



TL/F/10135–1

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT715
Programmable Video Sync Generator

General Description

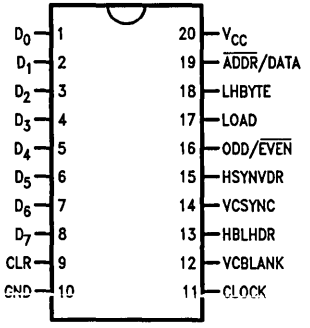
The 'ACT715 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal and vertical driving pulses, horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

The 'ACT715 makes no assumptions concerning the system that it will be used in. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

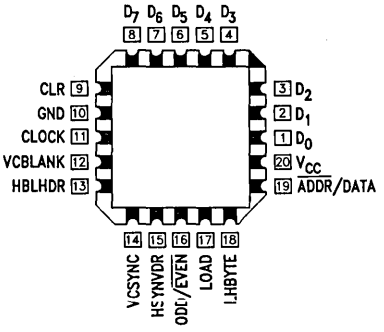
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10137–1

Pin Assignment for LCC



TL/F/10137–2

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT725
512 x 9 First In, First Out Memory (FIFO)

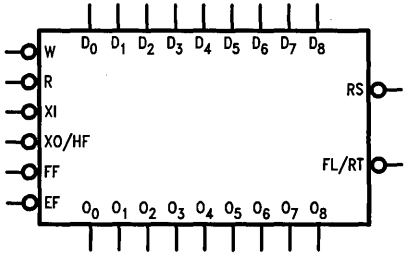
General Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for zero fall-through time; it is suited for high-speed applications.

Features

- First-in, first-out dual port memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- Outputs source/sink 8 mA
- 'ACT725 has TTL-compatible inputs
- Pin and functionality compatible with IDT7201

Logic Symbol



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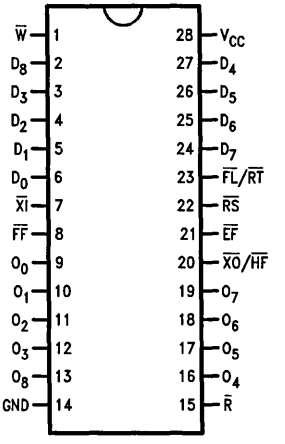
Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



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Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit

National Semiconductor

54ACT/74ACT818
8-Bit Diagnostic Register

General Description

The 'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

Features

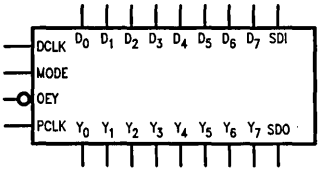
- On-line and off-line system diagnostics
- Swaps the contents of diagnostic register and output register
- Diagnostic register and diagnostic testing
- Cascadable for wide control words as used in microprogramming
- Edge-triggered D registers
- Outputs source/sink 24 mA
- 'ACT818 has TTL-compatible inputs
- 'ACT818 is functionally- and pin-compatible to AMD Am29818 and MMI 74S818

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter

Ordering Code: See Section 5

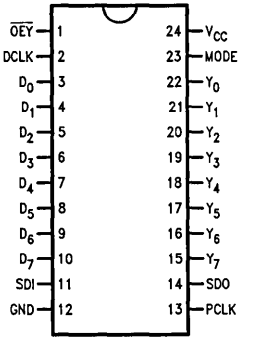
Logic Symbol



TL/F/9801–3

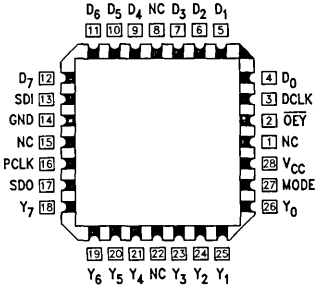
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9801–1

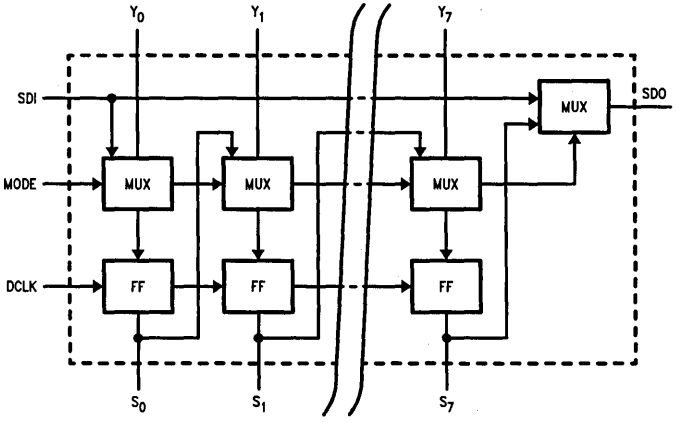
Pin Assignment for LCC and PCC



TL/F/9801–2

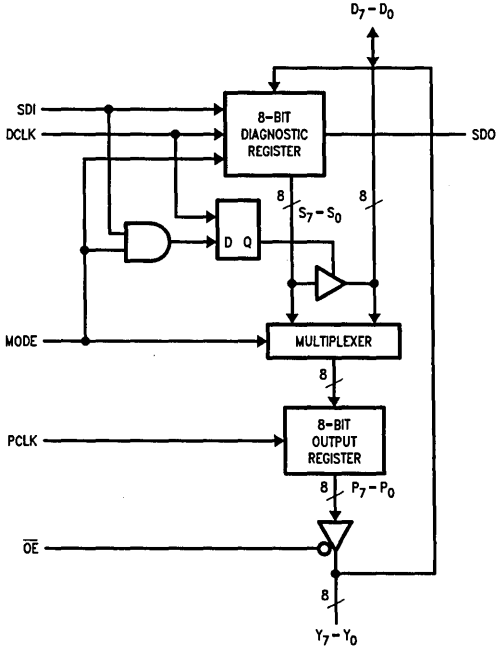
Pin Names	Description
D_0–D_7	Data Inputs
SDI	Serial Data Input
DCLK	Diagnostics Clock
MODE	Control Input
PCLK	Pipeline Register Clock
$\overline{OEY}$	Output Enable Input
SDO	Serial Data Output
Y_0–Y_7	Data Outputs

Diagnostic Register



TL/F/9801–4

Block Diagram



TL/F/9801–5

Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

Inputs				Outputs			Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic Reg.	Pipeline Reg.	
X	L	↑	X	S7	SI<SI − 1, SO<SD_I	NA	Serial Shift; D_7–D_0 Disabled
X	L	X	↑	S7	NA	PI<DI	Normal Load Pipeline Register
L	H	↑	X	L	SI<YI	NA	Load Diagnostic Register from Y; DI Disabled
X	H	X	↑	SDI	NA	PI<SI	Load Pipeline Register from Diagnostic Register
H	H	↑	X	H	Hold	NA	Hold Diagnostic Register; DI Enabled

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$	74ACT	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±10.0	±1.0	μA	V_{IN} = V_{CC}
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$\overline{OE}$ = V_{IH} V_{OUT} = 0V, V_{CC}
I_{CC}	Maximum Quiescent Supply Current	5.5		1.0			mA	V_{IN} = V_{CC} or GND
I_{CCT}	Maximum Additional I_{CC}/Input	5.5			1.6	1.5	mA	V_{IN} = V_{CC} − 2.1V V_{CC} = 5.5V
V_{OH}	Minimum HIGH Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA I_{OH} = −24 mA
	Minimum HIGH Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V V	I_{OH} = −8 mA I_{OH} = −8 mA
V_{OL}	Maximum LOW Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA I_{OL} = 24 mA
	Maximum LOW Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V V	I_{OL} = 8 mA I_{OL} = 8 mA
I_{OLD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5			50	75	mA	V_{OLD} = 1.65V Max

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OHD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{OLD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 1)	5.5			32	32	mA	V_{OLD} = 5.5V
I_{OHD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 1)	5.5			−32	−32	mA	V_{OHD} = 3.3V

*All outputs loaded; thresholds on input associated with output under test.

Note 1: Test load 50 pF, 500Ω to ground.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}	Propagation Delay PCLK to Y	5.0	3.0	6.0	9.0			2.5	9.5	ns	2–5
t_{PLH}	Propagation Delay PCLK to Y	5.0	3.0	6.5	9.0			2.5	10.0	ns	2–5
t_{PHL}	Propagation Delay MODE to SDO	5.0	4.0	8.0	11.0			3.5	12.0	ns	2–5
t_{PLH}	Propagation Delay MODE to SDO	5.0	4.0	8.0	11.5			4.0	12.5	ns	2–5
t_{PHL}	Propagation Delay SDI to SDO	5.0	3.5	7.5	10.5			3.0	12.0	ns	2–5
t_{PLH}	Propagation Delay SDI to SDO	5.0	3.5	7.5	10.5			3.5	12.0	ns	2–5
t_{PHL}	Propagation Delay DCLK to SDO	5.0	4.5	9.0	12.5			4.0	14.0	ns	2–5
t_{PLH}	Propagation Delay DCLK to SDO	5.0	4.5	9.5	13.0			4.0	14.5	ns	2–5
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	2.5	6.0	9.0			2.5	10.0	ns	2–8
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	1.5	5.5	8.0			1.0	9.0	ns	2–8
t_{PZL}	Output Enable Time DCLK to D_n	5.0	3.0	8.0	12.0			3.0	13.5	ns	2–8
t_{PLZ}	Output Disable Time DCLK to D_n	5.0	2.0	8.5	11.0			1.5	12.0	ns	2–8
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	3.0	8.0	10.0			2.5	11.0	ns	2–7
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	2.5	9.0	11.0			2.0	11.5	ns	2–7
t_{PZH}	Output Enable Time DCLK to D_n	5.0	3.0	6.5	11.5			3.0	13.0	ns	2–7
t_{PHZ}	Output Disable Time DCLK to D_n	5.0	3.0	7.5	12.0			2.0	13.0	ns	2–7

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time D to PCLK	5.0	1.0	4.0		5.0	ns	2-9
t_h	Hold Time D to PCLK	5.0	0.0	1.0		1.0	ns	2-9
t_s	Setup Time MODE to PCLK	5.0	2.5	4.5		5.5	ns	2-9
t_h	Hold Time MODE to PCLK	5.0	−1.0	0.0		0.0	ns	2-9
t_s	Setup Time Y to DCLK	5.0	0.5	2.5		2.5	ns	2-9
t_h	Hold Time Y to DCLK	5.0	0	1.0		1.5	ns	2-9
t_s	Setup Time MODE to DCLK	5.0	2.0	4.0		4.0	ns	2-9
t_h	Hold Time MODE to DCLK	5.0	−0.5	1.0		1.0	ns	2-9
t_s	Setup Time SDI to DCLK	5.0	2.0	3.5		4.5	ns	2-9
t_h	Hold Time SDI to DCLK	5.0	−0.5	1.0		1.0	ns	2-9
t_s	Setup Time DCLK to PCLK	5.0	6.0	9.0		10.5	ns	2-9
t_s	Setup Time PCLK to DCLK	5.0	6.0	11.0		11.5	ns	2-9
t_w	Pulse Width PCLK HIGH or LOW	5.0	2.0	3.0		3.0	ns	2-6
t_w	Pulse Width DCLK HIGH or LOW	5.0	2.0	3.0		3.0	ns	2-6

Note 1: Test load 50 pF, 500Ω to ground.

*Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	20	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC821 • 54ACT/74ACT821
10-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT821 is a 10-bit D flip-flop with TRI-STATE outputs arranged in a broadside pinout.

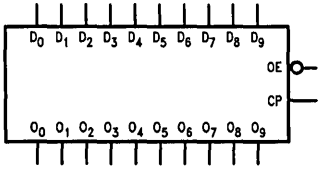
The 'AC/'ACT821 is functionally identical to the AM29821.

Features

- TRI-STATE outputs for bus interfacing
- Noninverting outputs
- Outputs source/sink 24 mA
- 'ACT821 has TTL-compatible inputs

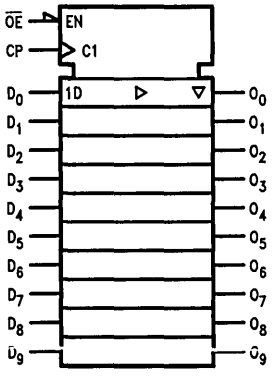
Ordering Code: See Section 5

Logic Symbols



TL/F/10139–1

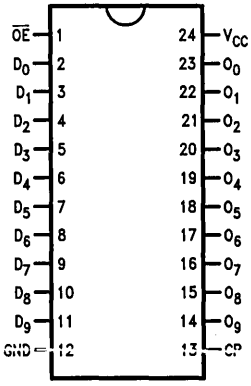
IEEE/IEC



TL/F/10139–2

Connection Diagrams

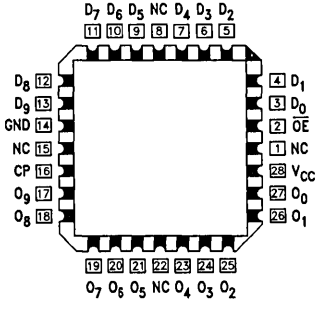
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10139–3

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

Pin Assignment for LCC



TL/F/10139–4

Functional Description

The 'AC/'ACT821 consists of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

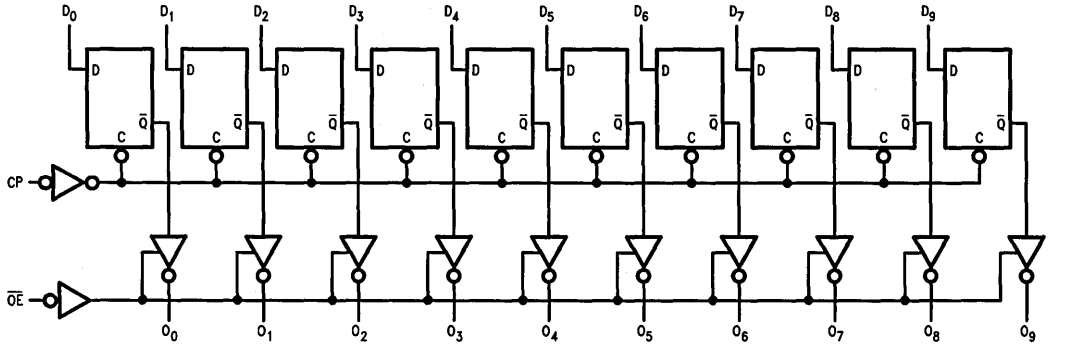
The 'AC/'ACT821 is functionally and pin compatible with the AM29821.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	⌐	L	L	Z	High Z
H	⌐	H	H	Z	High Z
L	⌐	L	L	L	Load
L	⌐	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10139–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f)	
(Note 2) (Typical)	
(Except Schmitt Inputs) 'ACT Devices	
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	110 120	145 160		95 100		100 110		MHz	2-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 6.0	13.0 9.5	1.0 1.0	16.0 11.5	3.0 2.0	15.0 10.5	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 5.5	13.0 9.5	1.0 1.0	16.0 11.5	3.0 2.0	15.0 10.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	11.0 8.0	1.0 1.0	13.0 10.0	2.5 1.5	12.0 9.0	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.0	1.0 1.0	13.5 10.0	2.5 1.5	12.0 9.0	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	10.5 8.0	1.0 1.0	12.0 10.0	2.5 1.5	11.0 8.5	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	10.5 8.0	1.0 1.0	12.0 10.0	2.5 1.5	11.0 8.5	ns	2-8

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −1.0	1.5 1.5	2.5 2.5	1.5 1.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −1.0	3.5 3.5	4.0 4.0	4.0 4.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.0 4.0	6.0 5.0	5.5 4.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	150		85		110		MHz	2-3
t_{PLH}	Propagation Delay CP to O_n	5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	5.0	2.5	6.0	9.5	1.0	11.5	2.0	10.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	1.0	12.5	2.0	11.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	1.0	13.0	2.0	12.0	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.5	12.0	1.0	13.5	1.0	13.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.0	10.5	1.0	12.5	1.0	11.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	2.0	4.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	2.0	3.0	2.5	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0	4.5	6.0	5.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC823 • 54ACT/74ACT823
9-Bit D Flip-Flop

General Description

The 'ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

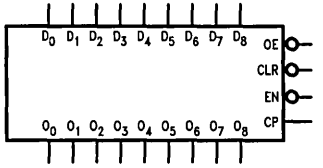
The Information for the 'AC823 is Advanced Information only.

Features

- Outputs source/sink 24 mA
- TRI-STATE® outputs for bus interfacing
- Inputs and outputs are on opposite sides
- 'ACT823 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



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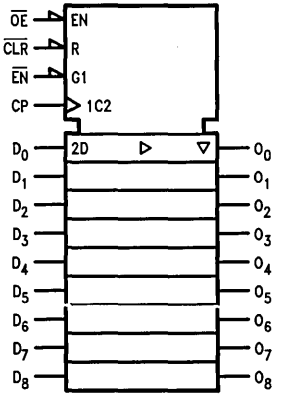
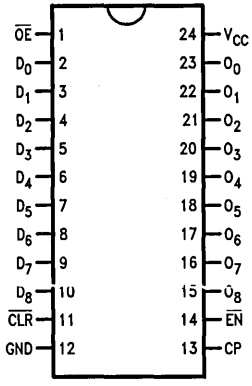
IEEE/IEC



TL/F/9894-2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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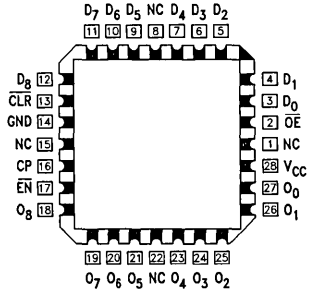
Pin Assignment for LCC



TL/F/9894-4

Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

Functional Description

The 'ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

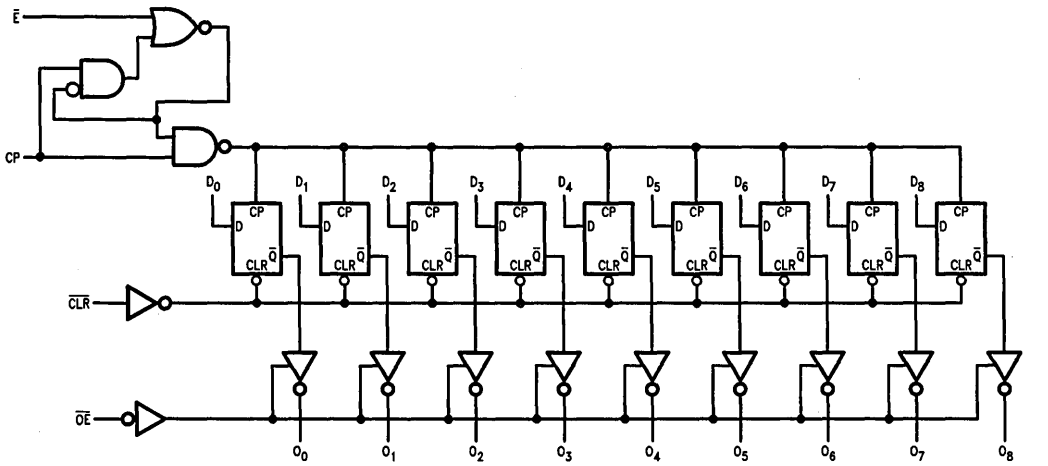
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High Z
H	X	L	↗	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to 7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current (Note 1)	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50pF$			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	158		95		109		MHz	2-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	5.5	9.5	1.0	12.0	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	5.5	9.5	1.0	12.0	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	8.0	13.5	1.0	18.0	2.0	15.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	11.5	1.5	11.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.0	12.0	1.5	12.0	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.5	11.0	1.0	13.5	1.5	12.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	12.0	1.5	11.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D to CP	5.0	0.5	2.5	4.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	2.5	3.0	2.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	2.0	4.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.0	3.0	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns	2-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns	2-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC825 • 54ACT/74ACT825
8-Bit D Flip-Flop

General Description

The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

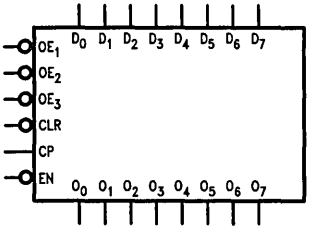
Features

- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- 'ACT825 has TTL-compatible inputs

The information for the 'AC825 is Advanced Information only.

Ordering Code: See Section 5

Logic Symbols



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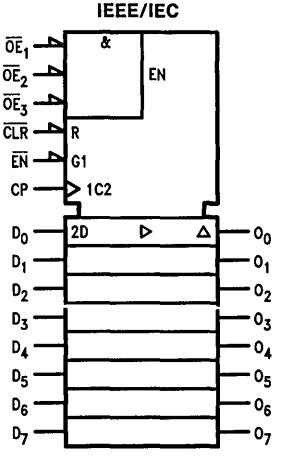

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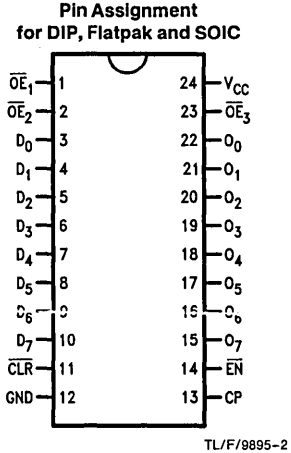
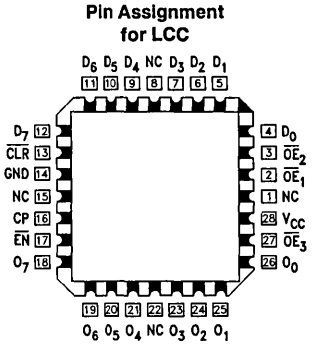
Connection Diagrams



TL/F/9895-2

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input



TL/F/9895-4

Functional Description

The 'AC/'ACT825 consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'AC/'ACT825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

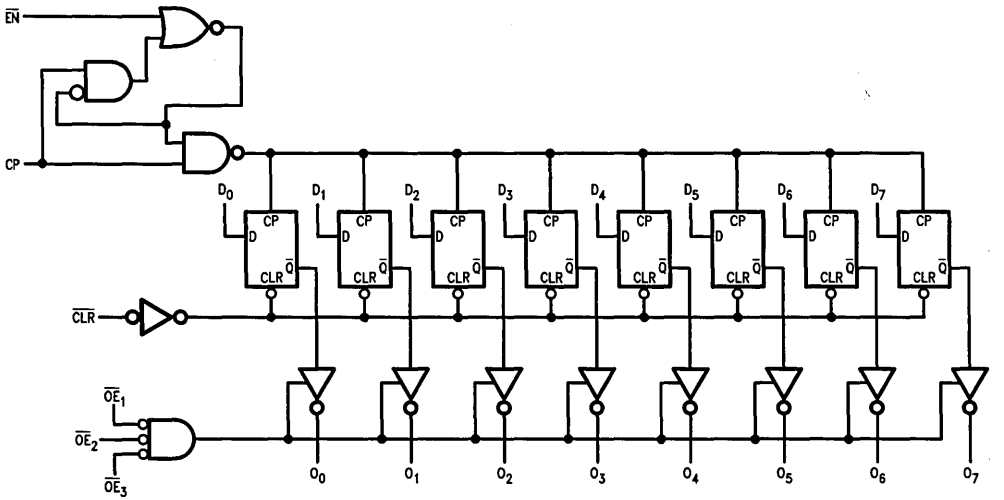
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D_n	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/9895–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to 7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70%, V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent (Note 1) Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	158		95		109		MHz	2-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	5.5	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	5.5	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	8.0	13.5	1.0	18.0	2.0	15.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	11.5	1.5	11.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.0	12.5	1.5	12.0	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.5	11.0	1.0	13.5	1.5	12.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	13.0	1.5	11.5	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	2.5	4.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	2.5	3.0	2.5	ns	2-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	2.0	4.0	2.5	ns	2-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.0	3.0	1.0	ns	2-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns	2-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns	2-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT827
10-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

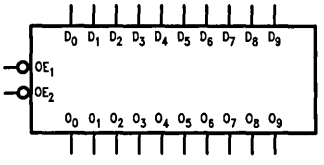
The 'ACT827 10-bit bus buffer provides high performance bus interface buffering for wide data/adress paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 'ACT827 is functionally- and pin-compatible to AMD's AM29827.

Features

- 'ACT827 has TTL-compatible inputs
- TRI-STATE® Outputs

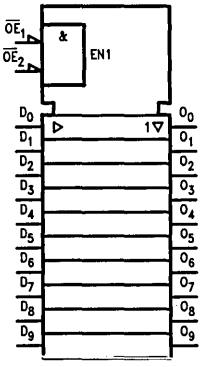
Logic Symbols



TL/F/10140–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs

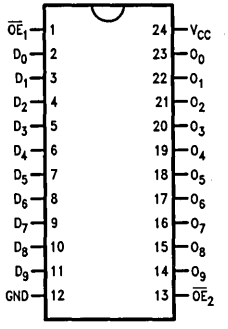
IEEE/IEC



TL/F/10140–4

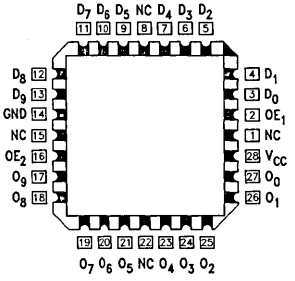
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10140–1

Pin Assignment for LCC



TL/F/10140–2

National Semiconductor

54ACT/74ACT841
10-Bit Transparent Latch with TRI-STATE® Outputs

General Description

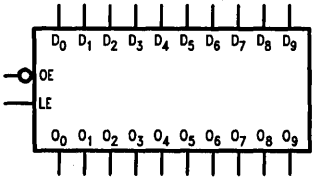
The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

Features

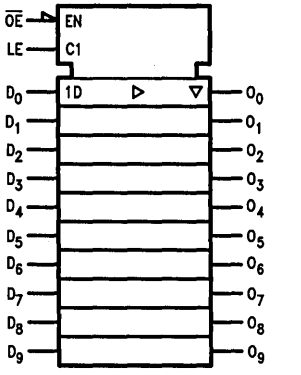
- 'ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

Ordering Code: See Section 5

Logic Symbols



TL/F/10156–1

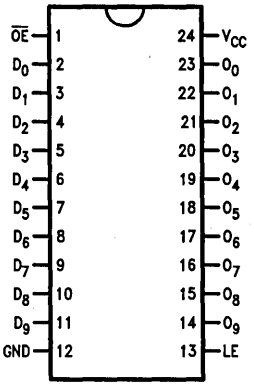


TL/F/10156–2

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

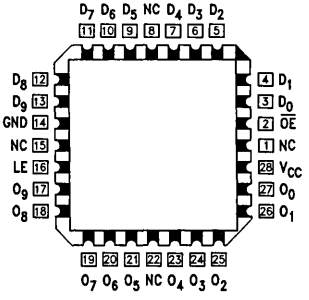
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10156–3

Pin Assignment for LCC



TL/F/10156–4

Functional Description

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

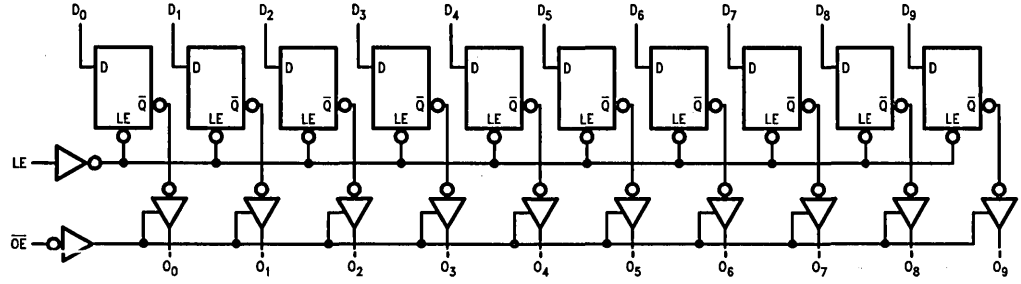
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10156–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V	150 ns/V
V_{CC} @ 4.5V	40 ns/V
V_{CC} @ 5.5V	25 ns/V
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	μA	V_I = V_{CC} − 2.1V

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.0	ns	2-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.0	ns	2-5
t_{PLH}	Propagation Delay LE to O_n	5.0	2.0	5.5	9.0	1.0	11.0	2.0	10.0	ns	2-6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.0	5.5	9.0	1.0	11.0	2.0	10.0	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.5	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.0	6.0	10.5	1.0	12.0	2.0	11.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.0	6.0	10.5	1.0	12.0	2.0	11.0	ns	2-8

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−0.5	0.5	3.0	1.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0.5	2.0	2.0	2.0	ns	2-9
t_w	LE Pluse Width, HIGH	5.0	2.0	3.5	5.0	3.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC843 • 54ACT/74ACT843
8-Bit Transparent Latch

General Description

The 'AC/'ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

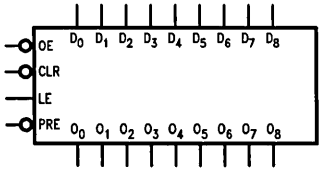
The 'AC/'ACT843 is functionally and pin compatible with AMD's Am29843.

Features

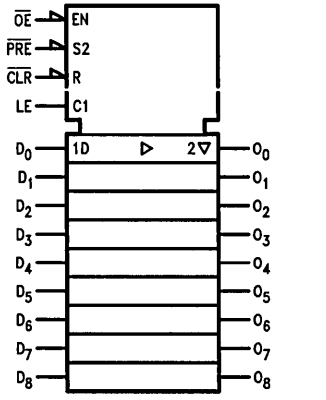
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

Ordering Code: See Section 5

Logic Symbols



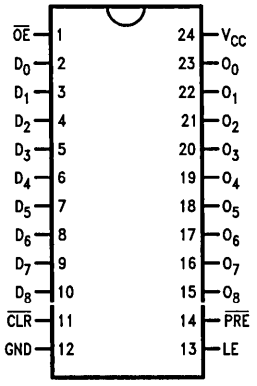
TL/F/9800-1



TL/F/9800-3

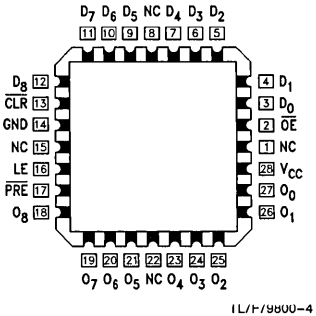
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9800-2

Pin Assignment for LCC



TL/F/9800-4

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Functional Description

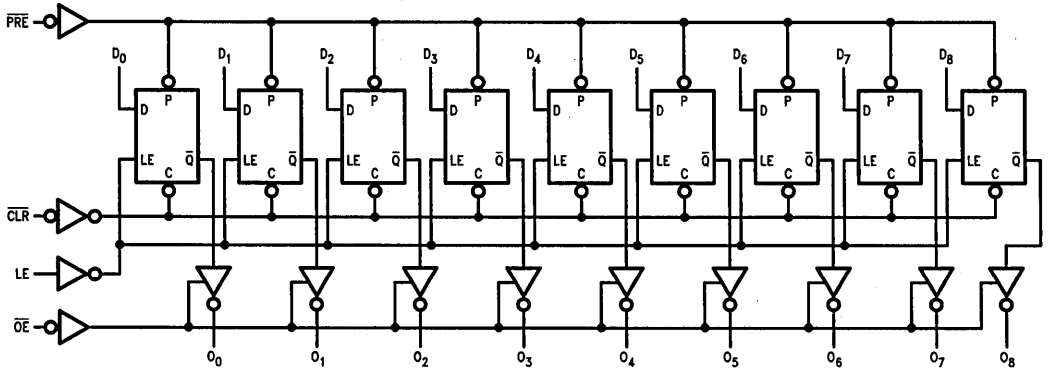
The 'AC/'ACT843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the 'AC/'ACT843 has a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

Function Tables

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9800–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
- V_{CC} @ 3.0V 150 ns/V
- V_{CC} @ 4.5V 40 ns/V
- V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: See Individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

DC Electrical Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3	3.5	6.5	12.0	1.0	14.0	2.5	13.0	ns	2–5
		5.0	2.0	4.5	8.5	1.0	10.0	1.5	9.0		
t_{PHL}	Propagation Delay D_n to O_n	3.3	4.0	7.0	12.0	1.0	14.0	3.0	13.0	ns	2–5
		5.0	2.5	5.0	8.5	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay LE to O_n	3.3	3.5	6.5	12.0	1.0	14.0	2.5	13.0	ns	2–6
		5.0	2.0	4.5	8.5	1.0	10.0	1.5	9.0		
t_{PHL}	Propagation Delay LE to O_n	3.3	4.0	7.0	12.0	1.0	14.0	3.0	13.0	ns	2–6
		5.0	2.5	5.0	8.5	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3	5.5	8.5	19.0	1.0	23.5	4.5	21.5	ns	2–6
		5.0	3.5	6.0	13.0	1.0	16.0	2.5	14.5		
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3	7.5	11.0	21.5	1.0	26.5	6.0	24.0	ns	2–6
		5.0	5.0	7.5	15.0	1.0	19.0	4.0	17.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3	3.5	6.0	11.0	1.0	13.0	3.0	12.0	ns	2–7
		5.0	2.0	4.5	8.0	1.0	10.0	1.5	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3	4.0	6.5	11.0	1.0	13.0	2.5	12.0	ns	2–8
		5.0	2.0	5.0	8.0	1.0	10.0	1.5	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3	4.0	6.5	10.5	1.0	12.0	3.5	11.0	ns	2–7
		5.0	3.0	5.0	8.0	1.0	9.0	2.5	8.5		
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3	3.0	6.0	10.5	1.0	12.0	2.5	11.0	ns	2–8
		5.0	2.0	4.5	8.0	1.0	9.0	1.5	8.5		
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	3.3	4.5	7.0	12.5	1.0	15.0	3.5	13.5	ns	2–6
		5.0	3.0	5.0	9.0	1.0	10.5	2.0	9.5		
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	3.3	4.5	7.0	12.5	1.0	15.0	3.5	13.5	ns	2–6
		5.0	3.0	5.0	9.0	1.0	10.5	2.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	0	3.0	3.5	3.5	ns	2–9
		5.0	−0.5	1.5	2.0	2.0		
t_h	Hold Time, HIGH or LOW D_n to LE	3.3		2.0	2.0	2.0	ns	2–9
		5.0	−0.5	2.5	2.5	2.5		
t_w	LE Pulse Width, HIGH	3.3	1.5	3.0	3.5	3.0	ns	2–6
		5.0	1.5	3.0	3.0	3.0		
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3	5.0	12.0	16.0	14.5	ns	2–6
		5.0	3.0	8.5	11.0	10.0		
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3	5.5	14.0	18.5	16.5	ns	2–6
		5.0	4.0	10.0	13.0	12.0		
t_{rec}	$\overline{PRE}$ Recovery Time	3.3	1.0	3.0	3.5	3.0	ns	2–9
		5.0	0	1.5	1.5	1.5		
t_{rec}	$\overline{CLR}$ Recovery Time	3.3	0	1.5	2.5	1.5	ns	2–9
		5.0	−0.5	0.5	1.5	0.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.0	ns	2-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.0	ns	2-5
t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.0	1.0	11.0	2.0	10.0	ns	2-6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.0	1.0	11.0	2.0	10.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0	2.5	6.5	14.0	1.0	17.5	2.0	16.0	ns	2-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	7.5	15.5	1.0	19.0	2.0	17.5	ns	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.5	ns	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.5	ns	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.0	2.0	11.0	ns	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.0	2.0	11.0	ns	2-8
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.5	2.0	11.0	ns	2-6
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−0.5	0.5	1.0	1.0	ns	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0.5	2.0	2.0	2.0	ns	2-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	3.5	3.5	ns	2-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	5.0	8.5	11.0	10.0	ns	2-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	5.5	9.5	12.5	11.0	ns	2-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	0.5	2.0	2.0	2.0	ns	2-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	−0.5	1.0	1.0	1.0	ns	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	44	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC845 • 54ACT/74ACT845
8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'AC/'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

The 'AC/'ACT845 is functionally and pin compatible with AMD's Am29845.

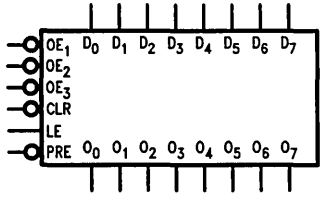
Features

- 'ACT845 has TTL-compatible inputs

The information for the 'AC845 is Advanced Information only.

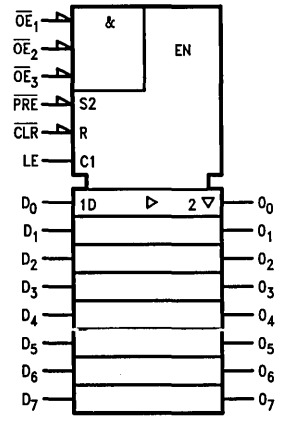
Ordering Code: See Section 5

Logic Symbols



TL/F/9896-3

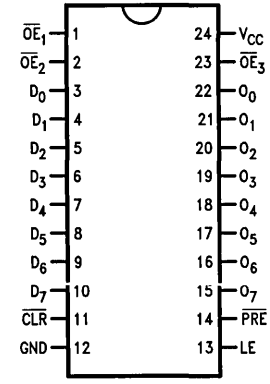
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
$\overline{LE}$	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset



TL/F/9896-5

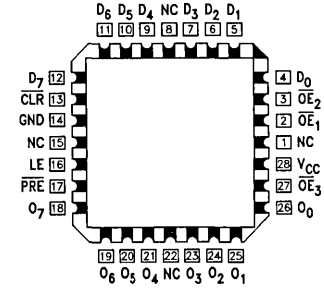
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9896-1

Pin Assignment for LCC



TL/F/9896-2

Functional Description

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

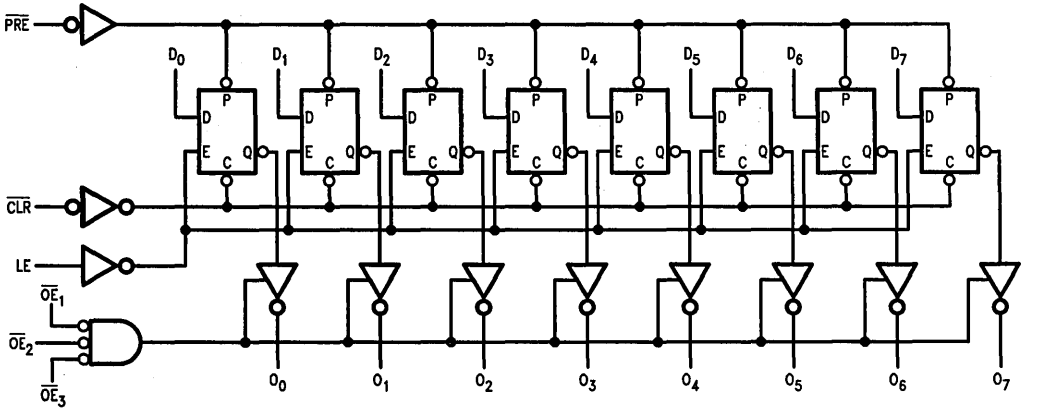
On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_n$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current
Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temerature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACT −40°C to +85°C
- 54ACT −55°C to +125°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Input Rise and Fall Time
(Note 2) (Typical)
(Except Schmitt Inputs) (t_r, t_f)
V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V
- V_{CC} @ 4.5V 10 ns/V
- V_{CC} @ 5.5V 8 ns/V

Note 2: Individual data sheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units (V)	V_{CC}	Conditions
		Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	4.5 5.5	I_{OUT} = −50 μA
			3.86 4.86	3.70 4.70	3.76 4.76	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	4.5 5.5	I_{OUT} = 50 μA
			0.36 0.36	0.50 0.50	0.44 0.44	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current		±0.1	±1.0	±1.0	μA	5.5	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current		±0.5	±10.0	±5.0	μA	5.5	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	0.6		1.6	1.5	mA	5.5	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current			50	75	mA	5.5	V_{OLD} = 1.65V Max
I_{OHD}				−50	−75	mA	5.5	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current		8.0	160	80	μA	5.5	V_{IN} = V_{CC} or Ground (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 or Waveforms and Load Configurations

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	V_{CC}* (V)	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0	2-5
t_{PHL}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0	2-5
t_{PLH}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0	2-6
t_{PHL}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0	2-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.5	14.0			2.0	16.0	ns	5.0	2-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	2.0	7.5	15.5			2.0	17.5	ns	5.0	2-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2-8
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2-6
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2-0

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	V_{CC}* (V)	Fig. No.
		Typ	Guaranteed Minimum					
t_s	Setup Time, HIGH or LOW D_n to LE	−0.5	0.5		1.0	ns	5.0	2-9
t_h	Hold Time, HIGH or LOW D_n to LE	0.5	2.0		2.0	ns	5.0	2-9
t_w	LE Pulse Width, HIGH	2.0	3.5		3.5	ns	5.0	2-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	8.5		10.0	ns	5.0	2-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.5	9.5		11.0	ns	5.0	2-6
t_{rec}	$\overline{PRE}$ Recovery Time	0.5	2.0		2.0	ns	5.0	2-9
t_{rec}	$\overline{CLR}$ Recovery Time	0	1.0		1.0	ns	5.0	2-9

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	54/74ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT1016
16 x 16 Parallel Multiplier

General Description

The 'ACT1016 is a high-speed, low power 16 x 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT™ technology, the 'ACT1016 offers a very low power alternative and exceptional performance.

The 'ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'ACT1016 operates from a single V_{CC} supply and is compatible with standard TTL logic levels.

The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by $\overline{OEL}$ and the output port TRI-STATE® control is controlled by $\overline{OEP}$. The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the two's complement X and Y mode controls, X_M and Y_M, respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

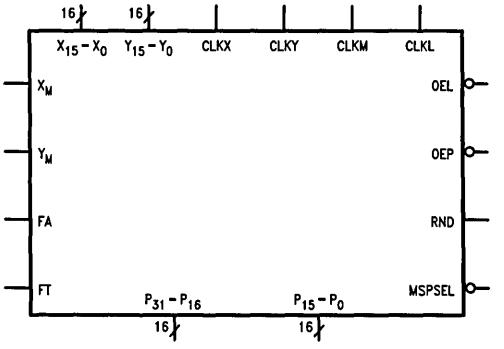
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

Features

- 16 x 16 parallel multiplier
- Selectable rounding modes
- Twos complement, unsigned magnitude and mixed mode multiplication
- Pin and functionally compatible with TRW MPY016H
- Provides low voltage, high-speed operation
- Single V_{CC} supply
- ±2000V ESD protection
- Outputs source/sink 8 mA
- TRI-STATE outputs
- 'ACT1016 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol



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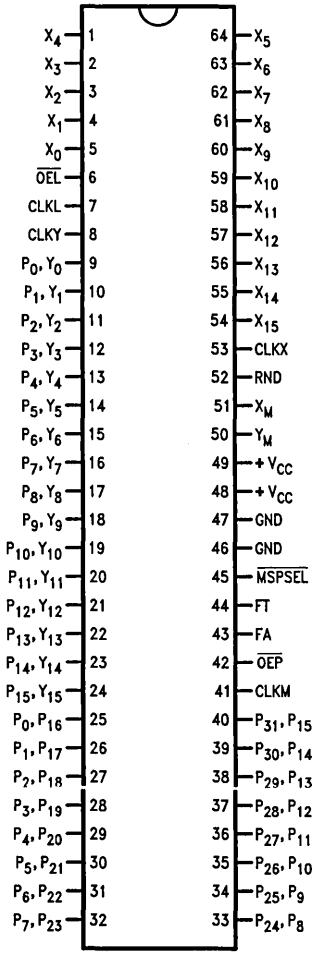
Pin Names	Description
X_{15}–X_0	Multiplicand Data Inputs
Y_{15}–Y_0	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
CLKM	Input Clock, MSP
CLKL	Input Clock, LSP
X_M, Y_M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{OEL}$	TRI-STATE Enable, LSP Routing
$\overline{OEP}$	TRI-STATE Enable, Product Output Port
RND	Round Control, MSP
$\overline{MSPSEL}$	MSP Select
P_{31}–P_{16}	MSP Outputs
P_{15}–P_0	LSP Outputs

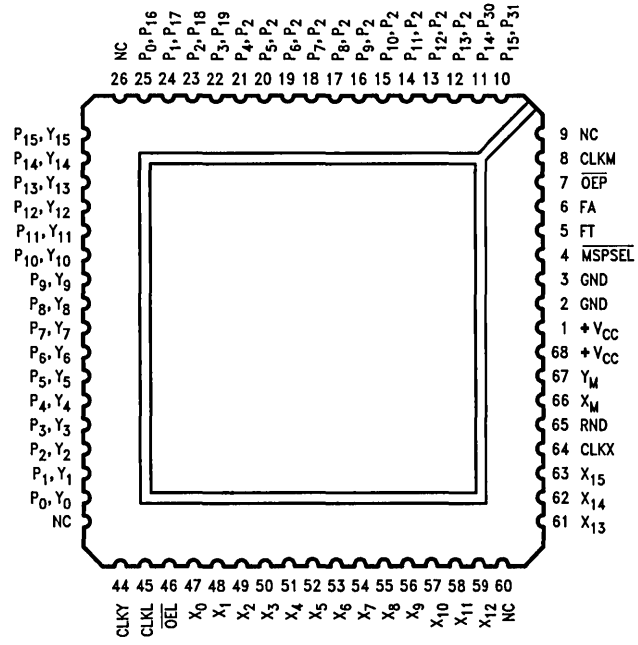
Connection Diagrams

Pin Assignment for DIP



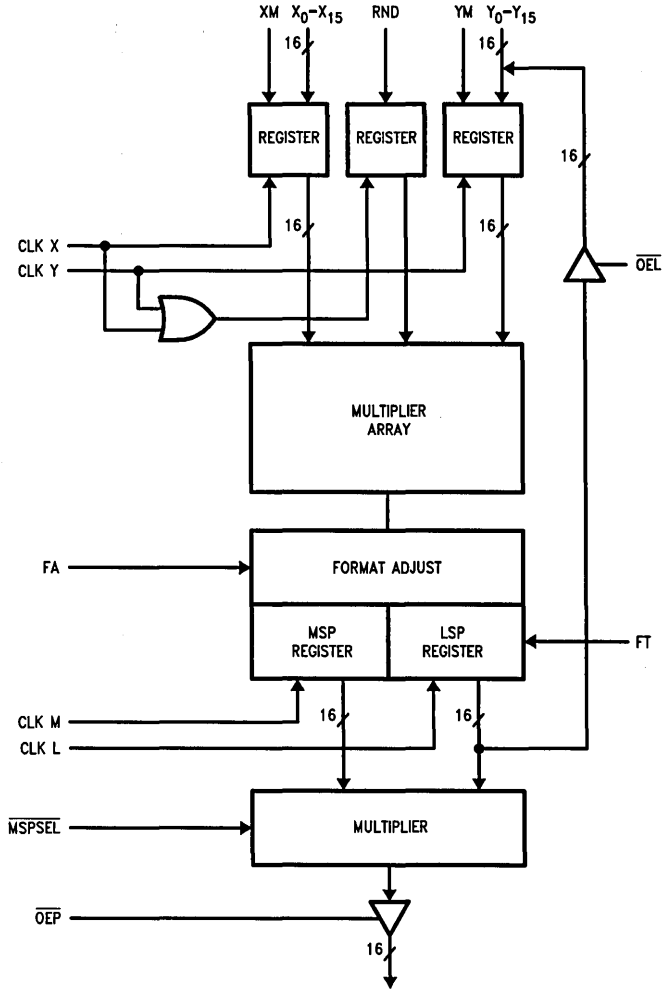
TL/F/10143–1

Pin Assignment for PCC



TL/F/10143–2

Logic Diagram



TL/F/10143–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

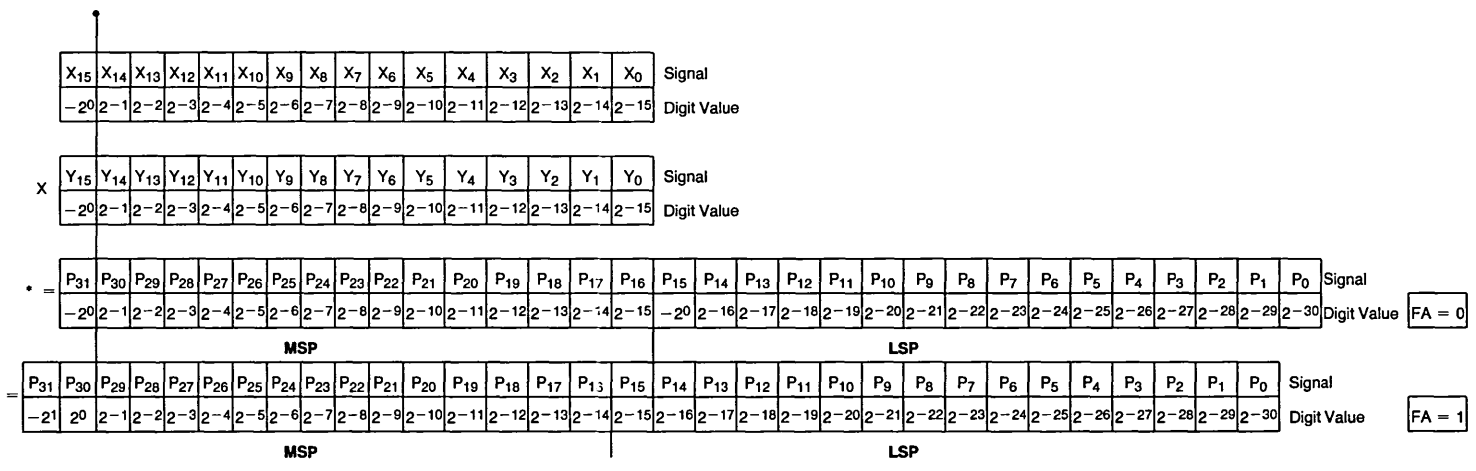


FIGURE 1. Fractional Twos Complement Notation

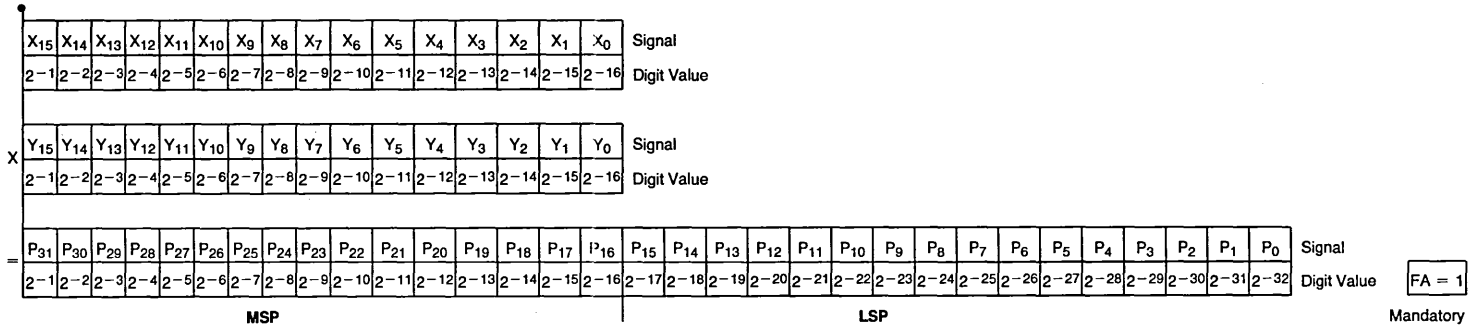


FIGURE 2. Fractional Unsigned Magnitude Notation

*In this format an overflow occurs in the attempted multiplication of the two complement number 1000 ... 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

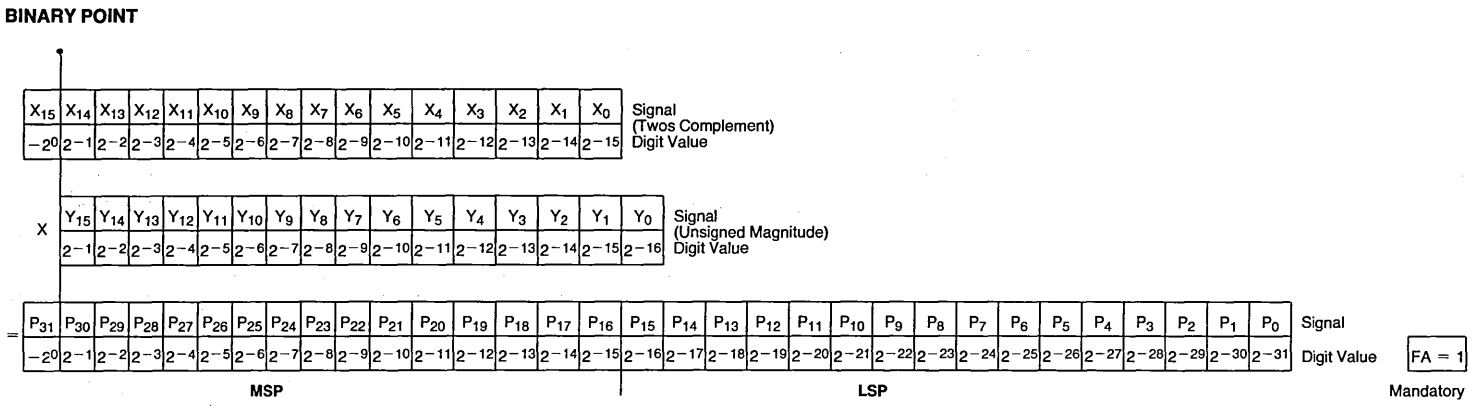


FIGURE 3. Fractional Mixed Mode Notation

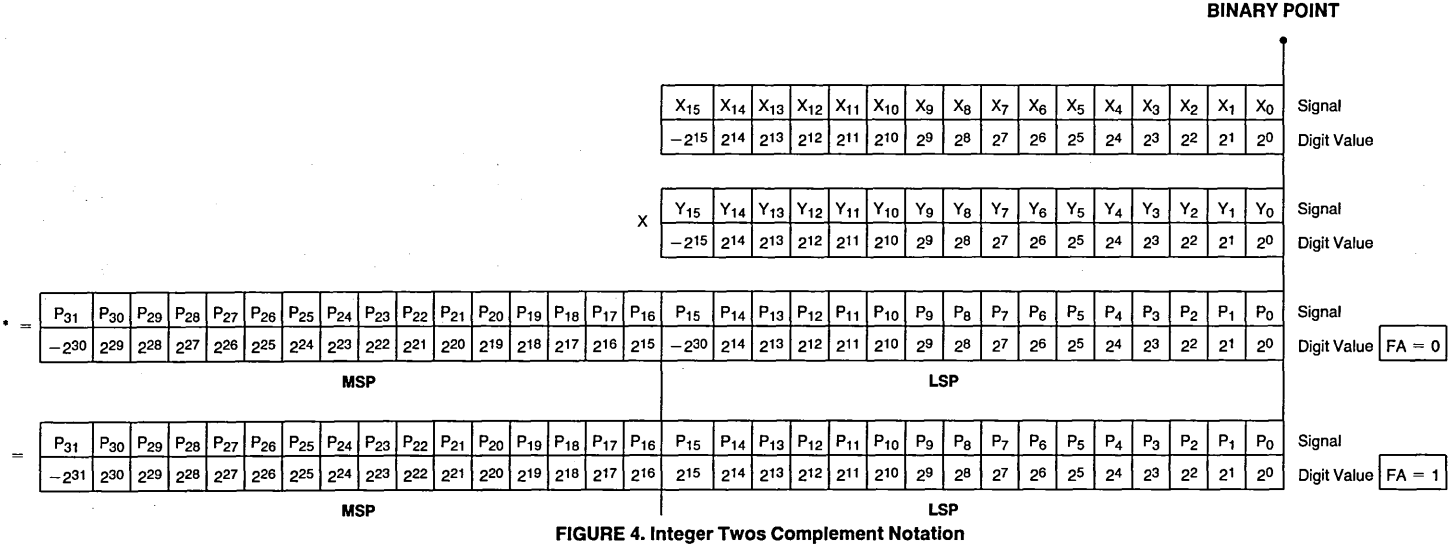


FIGURE 4. Integer Twos Complement Notation

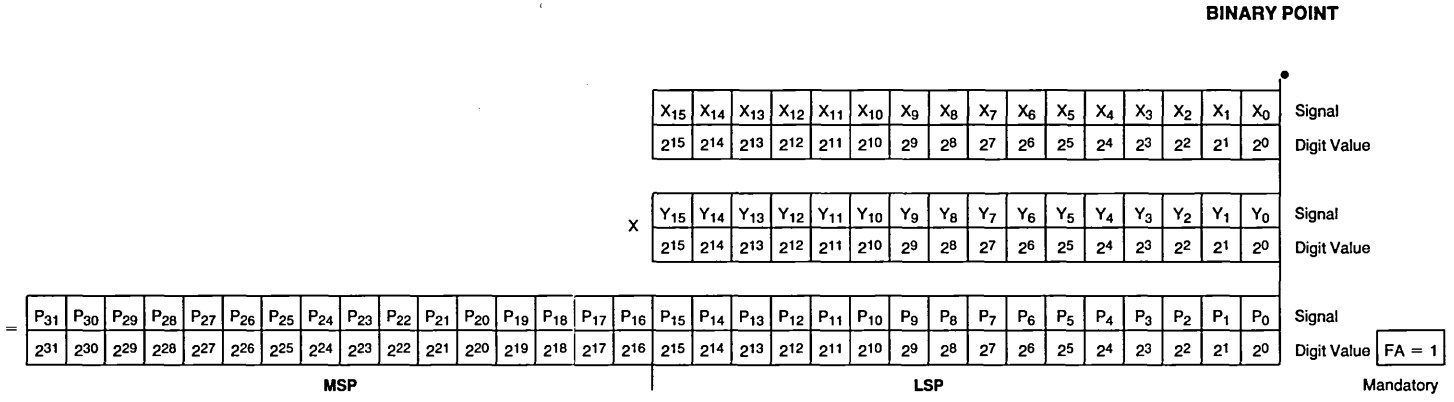


FIGURE 5. Integer Unsigned Magnitude Notation

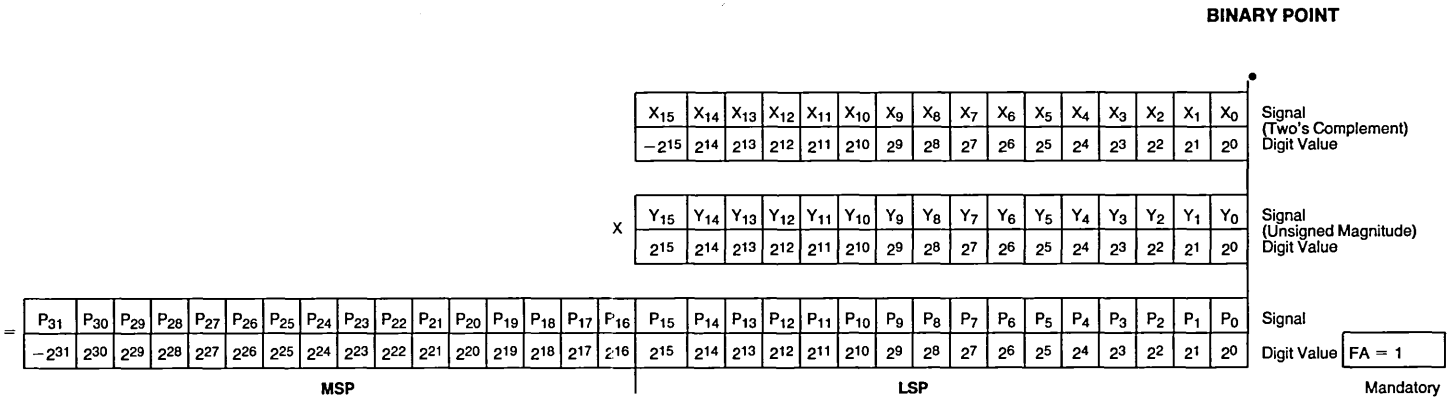


FIGURE 6. Integer Mixed Mode Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1000 . . . 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Signal Descriptions

Inputs

X_{IN} (X_{15}–X_0)

Sixteen multiplicand data inputs.

Y_{IN} (Y_{15}–Y_0)

Sixteen multiplier data inputs. This is also an output port for P_{15}–P_0.

Input Clocks

CLKX

The rising edge of this clock loads the X_{15}–X_0 data input register along with the X mode and round registers.

CLKY

The rising edge of this clock loads the Y_{15}–Y_0 data input register along with the Y mode and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL

The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

X_M, Y_M

Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA

When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT

When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

$\overline{OEL}$

The $\overline{OEL}$ input is the TRI-STATE enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$

The $\overline{OEP}$ is the TRI-STATE enable for the product output port.

RND

The Round control is used for the rounding of the MSP. When this control is HIGH, A '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a '1' will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MPSEL}$

When $\overline{MPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP (P_{31}–P_{16})

The MSP is the Most Significant Product output.

LSP (P_{15}–P_0)

The LSP is the Least Significant Product output.

Y_{15-0}/LSP_{OUT} (Y_{15}–Y_0 or P_{15}–P_0)

This is the Least Significant Product (LSP) output available when $\overline{OEL}$ is LOW. It is also an input port for Y_{15}–Y_0.

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = 0.5	−20 mA
V_I = V_{CC} + 0.5	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current; per Output Pin	±15 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC}) or (I_{GND})	±20 mA
Storage Temperature (T_{STG})	−65°C to +150°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Supply Voltage (V_{CC}) (Unless Otherwise Specified)	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Maximum Slew Rate (S_r) (except for Schmitt Inputs)	
V_{IN}	0.8V to 2.0V
V_{meas}	0.8V to 2.0V
V_{CC} @ 4.5V	10 ns
V_{CC} @ 5.5V	8 ns

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74ACT Typ	74ACT Guaranteed Limit	74ACT Guaranteed Limit	Units	Conditions
I_{IN}	Maximum Input Leakage Current		±0.1	±1.0	μA	V_{CC} = Max, V_{IN} = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current		±0.5	±5.0	μA	High Z, V_{CC} = Max, V_{OUT} = V_{CC}, GND
I_{CCQ}	Supply Current, Quiescent	0.5	2.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V TSL, TSM, TSX = Max
I_{CCD}	Supply Current, 12.4 MHz Loaded	300		325	mA	V_{CC} = Max, f = 12.4 MHz Test Load: See Note 1
I_{CCD}	Supply Current, 20 MHz Loaded	325		350	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}*	Minimum HIGH Level Output	4.49	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = −50 μA, V_{CC} = 4.5V
		5.49	5.4	5.4		V_{IN} = V_{IL} or V_{IH}, I_{OUT} = −50 μA, V_{CC} = 5.5V
			3.86	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5V
			4.86	4.76	B	I_{OH} = −8 mA, V_{CC} = 5.5V
V_{OL}*	Maximum HIGH Level Output	0.001	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 4.5V
		0.001	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 5.5V
			0.45	0.50	V	I_{OL} = 8 mA, V_{CC} = 4.5V
			0.45	0.50	B	I_{OL} = 8 mA, V_{CC} = 5.5V
I_{OLD}	Minimum Dynamic Output Current			32	mA	V_{CC} = 5.5V, V_{OLD} = 2.2V Max (Note 2)
I_{OHD}	Minimum Dynamic Output Current			−32	mA	V_{CC} = 5.5V, V_{OHD} = 3.3V Min (Note 2)
I_{CCT}	Maximum I_{CC}/Input	0.6		1.5	mA	V_{IN} = V_{CC} − 2.1V

Note 1: Test Load 50 pF, 500Ω to Ground.

Note 2: Only one output loaded at one time, maximum duration of test 2 ms.

*All outputs loaded.

AC Characteristics

Symbol	Parameter	74ACT $T_A = -40°C$ to $+85°C$				Units	Fig. No.
		1016-65		1016-55			
		Min	Max	Min	Max		
t_{MUC}	Unclocked Multiply Time		80.0		65.0	ns	2-3, -9
t_{MC}	Clocked Multiply Time		65.0		55.0	ns	2-3, -9, -10
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	1.5	13.0	1.5	13.0	ns	2-3, -9
t_{PDP}	Output Clock to P	1.5	20.0	1.5	20.0	ns	2-3, -9
t_{PDY}	Output Clock to Y	1.5	20.0	1.5	20.0	ns	2-3, -9
t_{ENA}	TRI-STATE Enable Time (Note 2)	1.5	10.0	1.5	10.0	ns	2-3, -8
t_{DIS}	TRI-STATE Disable Time (Note 2)	1.5	12.5	1.5	12.5	ns	2-3, -8
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML (Note 1)	0		0		ns	2-3, -9, -10
t_s	Setup Time X, Y, RND	5.5		5.5		ns	2-3, -7, -9
t_h	Hold Time X, Y, RND	1.0		1.0		ns	2-3, -7, -9
t_W	Clock Pulse Width HIGH or LOW	3.5		3.5		ns	2-3, -9

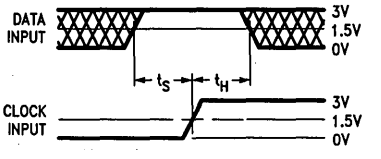
Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in *Figure 2-3.*

Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	5.0	pF	$V_{OUT} = 0V$

Timing Diagrams



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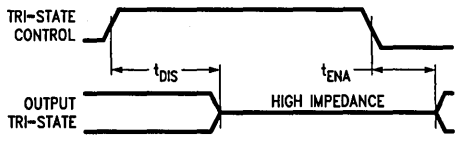
Note: Diagram shown for HIGH data only. Output transition may be opposite sense.

FIGURE 7. Setup and Hold Time



TL/F/10143–6

FIGURE 8. TRI-STATE Control Timing Diagram

Timing Diagrams (Continued)

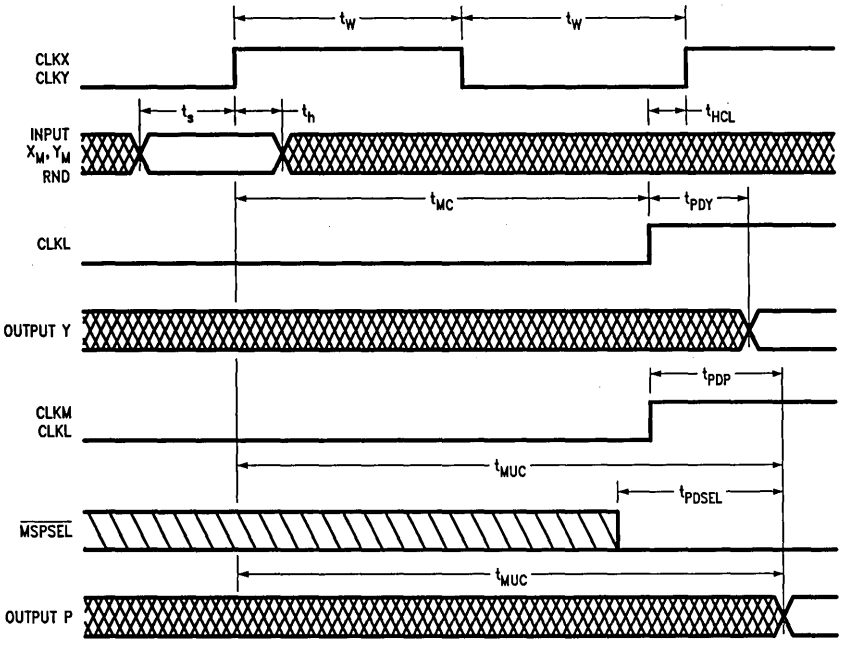


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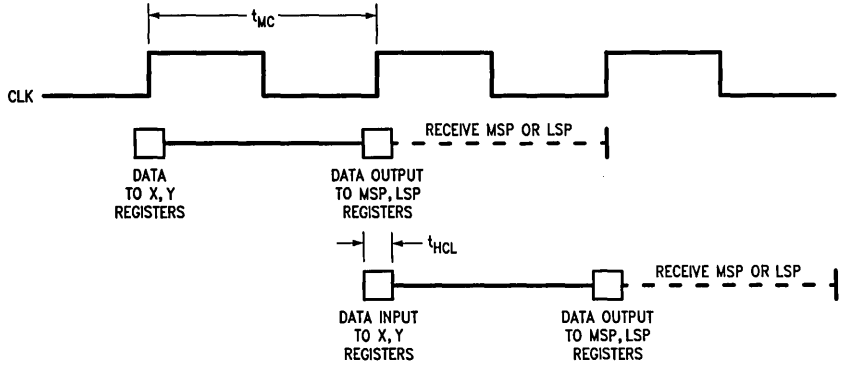
FIGURE 9. '1016 Timing Diagram



TL/F/10143–8

FIGURE 10. Simplified Timing Diagram—Typical Application

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT1110
Single Port 16 x 16 Bit Multiplier/Accumulator

General Description

The 'ACT1110 is pin and functionally compatible with the ADSP-1110 from Analog Devices. With a computational bandwidth exceeding 12 MHz, the 'ACT1110 is highly adapted to applications like digital filters, FFT's, and other signal processing applications. Its single bus structure also allows for the use of 28-pin DIP packages which significantly reduce cost as compared to existing 3-port multipliers.

All inputs to and outputs from the device pass through its single 16-bit I/O port. An internal pipeline register enables a new input to be loaded as the previous multiply/accumulate instruction is executed. A 6-bit microcoded word controls the device with I/O and MAC instructions. Data inputs to the 'ACT1110 can be 2's complement or unsigned magnitude numbers.

A multiply or MAC operation requires two cycles to complete. Multiplier products are accumulated in a 40-bit Multiplier Result Register. Overflow from the lower 32 bits of this register into the upper 8 extended bits can be monitored externally. The outputs can be saturated to full scale upon overflow. Two round control inputs implement rounding consistent with output formatting.

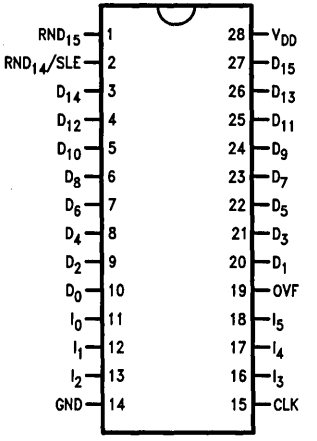
The device also offers the capability to left-shift the Multiplier Result Register upon output. This flexibility allows full 32-bit precision in 2's complement multiply. It also provides a means for maximizing resolution when using block floating point, and when upscaling or downscaling 2's complement results.

Features

- 16 x 16 Single port multiplier/accumulator
- High speed—computational bandwidth exceeding 12 MHz
- Selectable accumulation, subtraction, rounding and preloading with a 35-bit result
- Pin and functionally compatible with the analog devices ADSP-1110 high drive (8 mA) output capability
- Low power consumption (less than 250 mW typical)—less than 7% of the power of compatible bipolar and 14% of the power of NMOS designs
- Inputs and outputs directly TTL-compatible
- Single V_{CC} supply
- ±2000V ESD protection

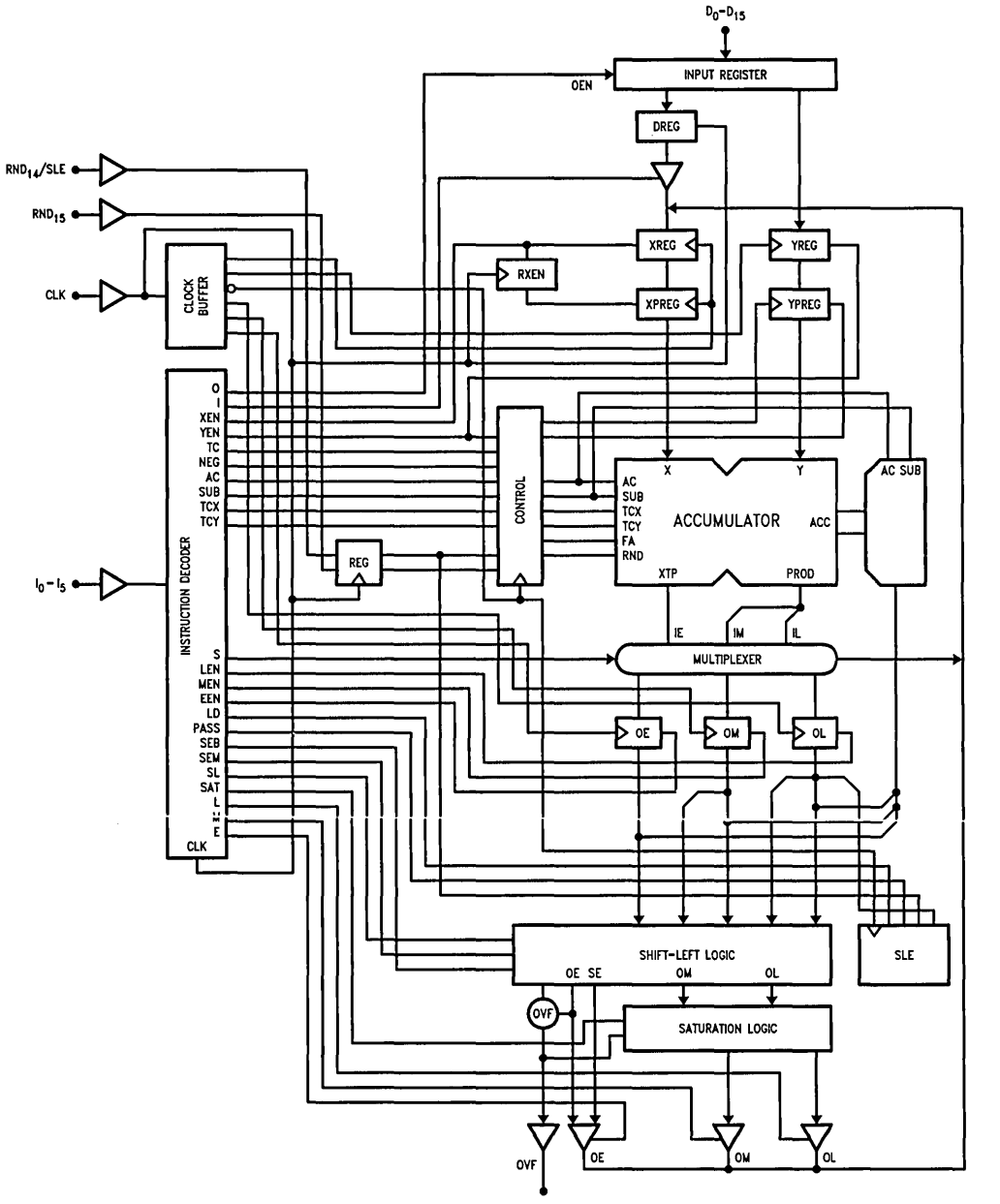
Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10142–1

Logic Diagram



TL/F/10142-2

National Semiconductor

54AC/74AC2708•54ACT/74ACT2708
64 x 9 First-In, First-Out Memory

General Description

The 'AC/'ACT2708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out typical data rate makes it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be TRI-STATE®. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to provide different word lengths by trying off unused data inputs.

Features

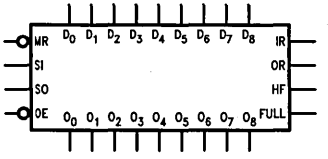
- 64-words by 9-bit dual port RAM organization
- 85 MHz shift-in, 60 MHz shift-out data rate, typical
- Expandable in word width only
- ACT2708 has TTL-compatible inputs
- Asynchronous or synchronous operation
- Asynchronous master reset
- Outputs source/sink 8 mA
- TRI-STATE outputs
- Full ESD protection
- Input and output pins directly in line for easy board layout
- TRW 1030 work-alike operation

Applications

- High-speed disk or tape controllers
- A/D output buffers
- High-speed graphics pixel buffer
- Video time base correction
- Digital filtering

Ordering Code: See Section 5

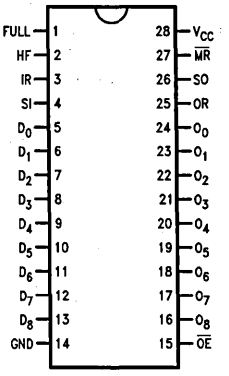
Logic Symbol



TL/F/10144–1

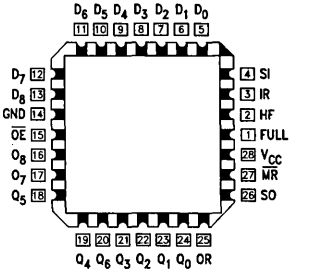
Pin Names	Description
D_0–D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
HF	Half Full Flag
FULL	Full Flag
O_0–O_8	Data Outputs

Pin Assignment for DIP and Flatpak



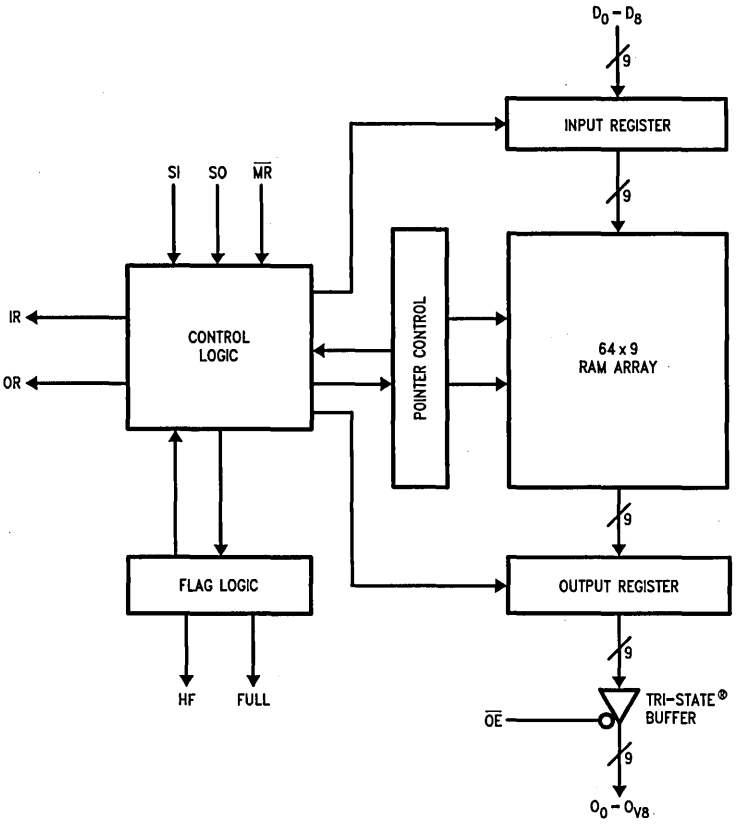
TL/F/10144–2

Pin Assignment for LCC and PCC



TL/F/10144–3

Block Diagram



TL/F/10144–4

Functional Description

INPUTS

Data Inputs (D_0–D_8)

Data inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by trying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)

Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, FH and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)

Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)

Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)

$\overline{OE}$ LOW enables the TRI-STATE output buffers. When $\overline{OE}$ is HIGH, the outputs are in a TRI-STATE mode.

OUTPUTS

Data Outputs (O_0–O_8)

Data outputs are enabled when $\overline{OE}$ is LOW and in the TRI-STATE condition when $\overline{OE}$ is HIGH.

Input Ready (IR)

IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)

OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)

This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)

This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

Status Flags Truth Table

HF	FULL	Status Flag Condition
L	L	Empty
L	H	Full
H	L	<32 Locations Filled
H	H	≥32 Locations Filled

H = HIGH Voltage Level
L = LOW Voltage Level

Reset Truth Table

Inputs			Outputs				
$\overline{MR}$	SI	SO	IR	OR	HF	FULL	O_0–O_8
H	X	X	X	X	X	X	X
L	X	X	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

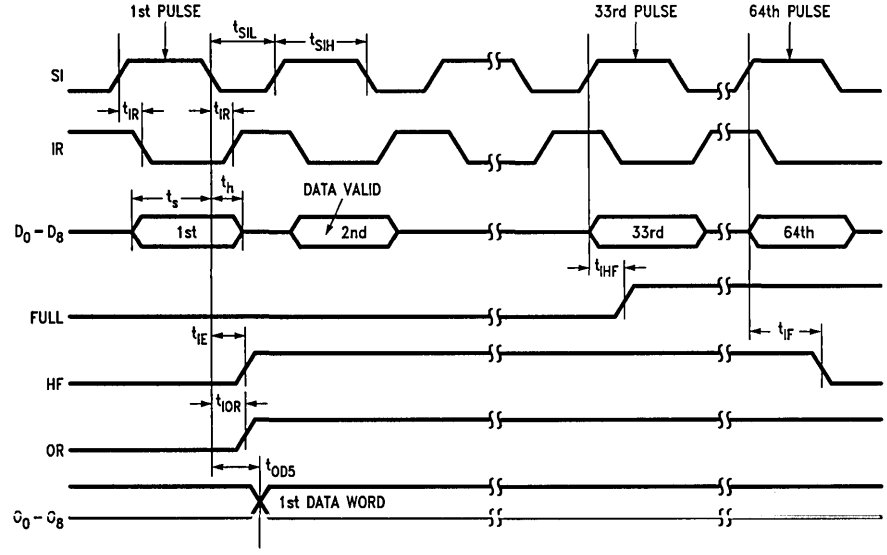
Functional Description (Continued)

MODES OF OPERATION

Mode 1: Shift In Sequence for FIFO Empty to Full

Sequence of Operation

1. Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled t_s before the falling edge of SI and held t_h after.
3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH: input stage is busy.
4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay t_{IE} after SI falls, indicating the FIFO is no longer empty.
5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t_{IHF} after SI, indicating a half-full FIFO. HF goes LOW propagation delay t_{IF} after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.



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Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

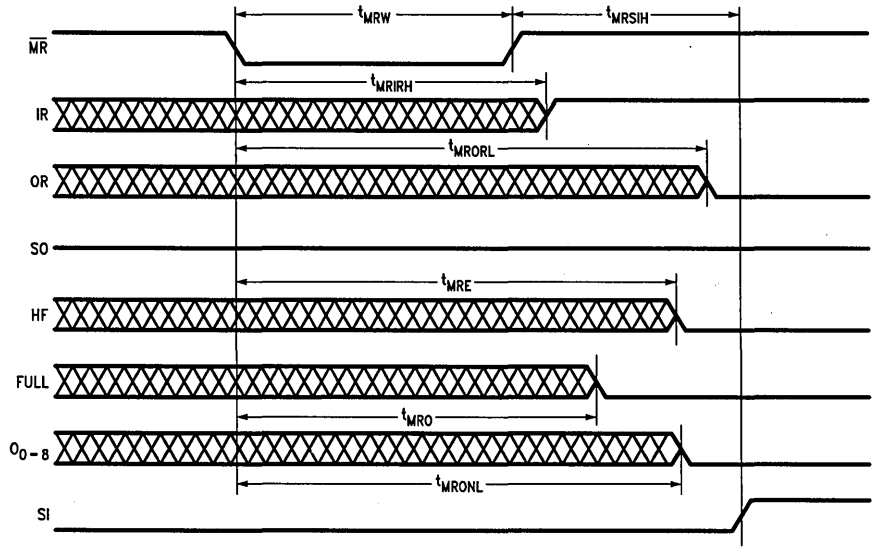
FIGURE 1. Modes of Operation Mode 1

Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.



TL/F/10144–6

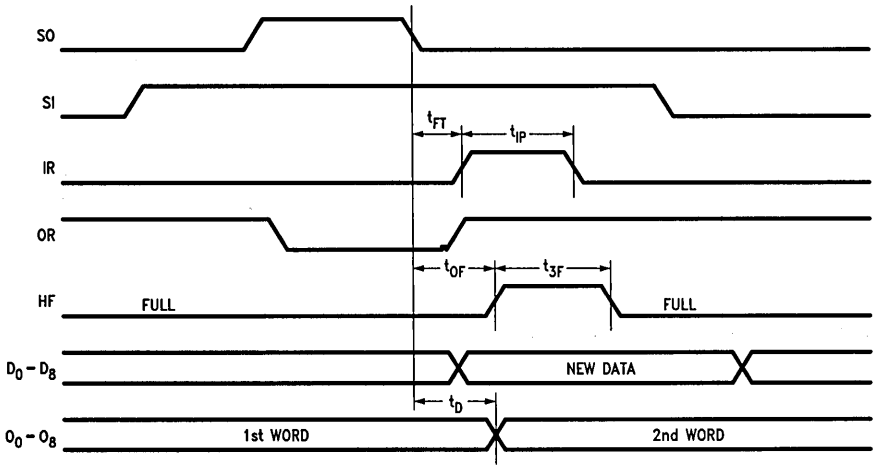
FIGURE 2. Mode of Operation Mode 2

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



TL/F/10144–7

Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

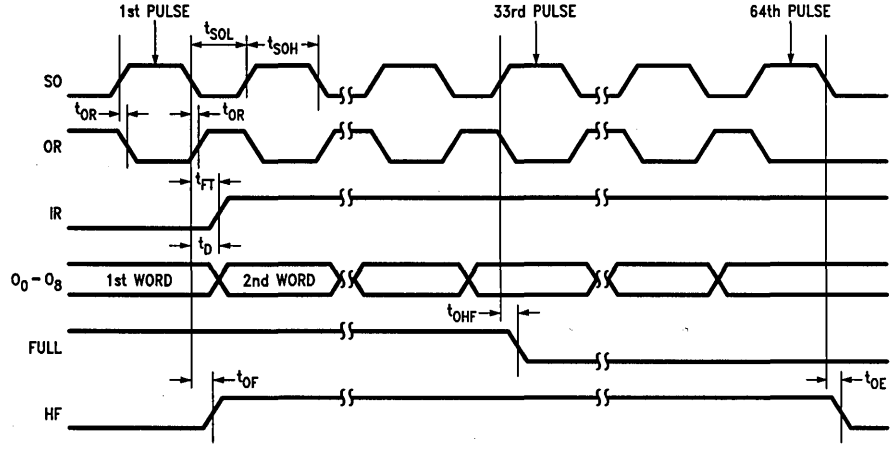
FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



TL/F/10144–8

Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

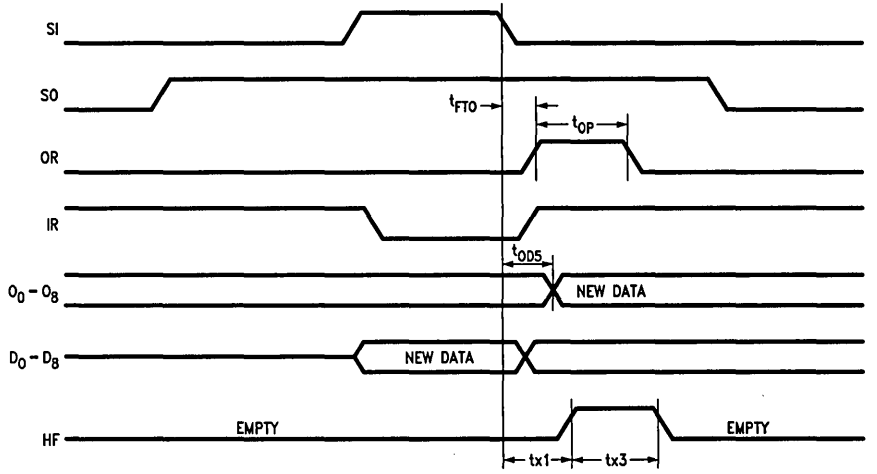
FIGURE 4. Modes of Operation Mode 4

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH In Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



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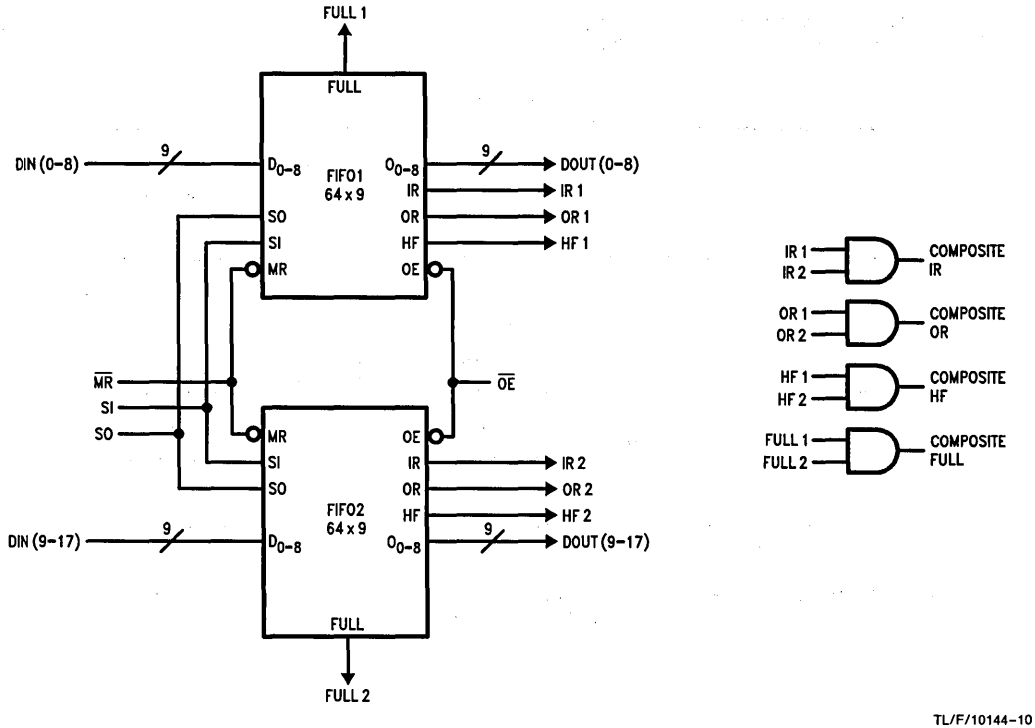
Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5

FIFO Expansion

Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored to obtain a composite signal by ANDing the corresponding flags.



TL/F/10144-10

Note: AND the corresponding flags to obtain a composite signal.

FIGURE 6. Word Width Expansion—64 x 18 FIFO

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±32 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±32 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C
Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V	
V_{CC} @ 4.5V	10 ns/V
V_{CC} @ 5.5V	8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Device

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC} GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0		V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

DC Characteristics for 'AC Family Device (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$ Typ	74AC $T_A = 25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74AC $T_A = -40°$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			32	32	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−32	−32	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{CCD}	Supply Current 20 MHz Loaded	5.5	125	150		150	mA	f = 20 MHz (Note 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

Note 4: Test load 50 pF, 500Ω to ground.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT $T_A = 25°C$ Typ	54ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACT $T_A = -40°$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −8 mA −8 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.32 0.32	0.40 0.40	0.37 0.37	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 8 mA 8 mA
I_{IN}	Maximum Input	5.5		±0.1	+1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.0	1.6	1.5	mA	$V_I = V_{CC}$ −2.1V
I_{OLD}	†Maximum Dynamic	5.5			32	32	mA	V_{OLD} = 1.65V
I_{OHD}	Output Current	5.5			−32	−32	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{CCD}	Supply Current 20 MHz Loaded	5.5	125	150		150	mA	f = 20 MHz (Note 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Notes: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.
When $\overline{MR}$ is low with SO High, I_{CC} > 1.5 mA.

Note 4: Test load 50 pF, 500Ω to ground.

AC Characteristics

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay, t_{IR} SI to IR	3.3 5.0	2.5 1.5	8.5 5.5	16.5 11.5			2.0 1.0	18.5 12.5	ns	2-6
t_{PHL}	Propagation Delay, t_{IR} SI to IR	3.3 5.0	2.5 1.5	7.0 5.0	14.0 10.0			2.0 1.0	16.0 11.0	ns	2-6
t_{PLH}	Propagation Delay, t_{IHF} SI to > HF	3.3 5.0	4.5 3.0	12.0 8.0	23.5 15.5			4.5 3.0	27.0 18.0	ns	2-6
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	3.3 5.0	5.0 3.5	11.5 8.0	22.0 15.0			5.0 3.5	25.0 17.0	ns	2-6
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	3.3 5.0	4.5 3.0	11.5 8.0	23.5 15.5			4.5 3.0	26.5 17.5	ns	2-6
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	3.3 5.0	4.5 3.0	13.5 9.0	30.5 20.0			4.5 3.0	34.5 23.0	ns	2-6
t_{PLH}	Propagation Delay t_{MRIRH} $\overline{MR}$ to IR	3.3 5.0	3.5 2.5	10.5 7.5	21.5 14.5			3.5 2.0	23.5 16.0	ns	2-6
t_{PHL}	Propagation Delay, t_{MRORL} $\overline{MR}$ to OR	3.3 5.0	7.5 6.0	18.5 12.0	35.5 23.0			7.5 6.0	41.0 26.5	ns	2-6
t_{PHL}	Propagation Delay t_{MRO} $\overline{MR}$ to Full Flag	3.3 5.0	4.0 2.5	9.0 6.5	18.0 12.5			4.0 2.0	21.5 15.0	ns	2-6
t_{PHL}	Propagation Delay t_{MRE} $\overline{MR}$ to HF Flag	3.3 5.0	8.5 7.0	20.0 13.5	39.5 26.0			8.5 6.5	44.5 29.5	ns	2-6
t_{PHL}	Propagation Delay, t_{MRONL} $\overline{MR}$ to O_n, LOW	3.3 5.0	3.5 2.0	9.5 7.0	19.5 14.0			3.5 2.0	21.5 15.5	ns	2-6
t_W	IR Pulse Width, t_{IP}	3.3 5.0	17.0 15.0	37.5 22.0	69.0 40.5			17.0 14.5	79.5 48.0	ns	2-6
t_W	HF Pulse Width t_{3F}	3.3 5.0	18.0 16.0	40.0 23.0	71.5 42.0			18.0 15.5	84.0 50.5	ns	2-6
t_{PLH}	Propagation Delay, t_D SO to Data Out	3.3 5.0	7.0 5.5	20.5 13.5	41.5 26.0			7.0 5.0	47.5 31.0	ns	2-6
t_{PHL}	Propagation Delay, t_D SO to Data Out	3.3 5.0	7.0 5.5	22.5 14.5	43.5 28.0			7.0 5.5	50.5 32.5	ns	2-6
t_{PHL}	Propagation Delay, t_{OHF} SO to < HF	3.3 5.0	4.0 2.5	9.0 6.5	17.5 12.0			4.0 2.0	20.5 14.0	ns	2-6
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	3.3 5.0	5.5 4.0	14.5 10.0	29.0 19.0			5.5 4.0	33.0 22.0	ns	2-6
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	3.3 5.0	3.0 2.0	8.5 5.5	17.0 12.0			3.0 1.5	19.5 13.0	ns	2-6

*Voltage Range 3.3 is 3.3V ± 0.3V

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics (Continued)

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, t_{OE} SO to Empty	3.3	4.0	10.5	20.5			3.5	23.5	ns	2-6
		5.0	2.5	7.0	14.0			2.0	16.0		
t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	3.3	7.5	22.5	44.5			7.0	53.5	ns	2-6
		5.0	6.0	15.5	30.0			5.5	35.0		
t_{PHL}	Propagation Delay, t_{OD5} SI to New Data Out	3.3	7.5	21.5	42.0			7.0	48.5	ns	2-6
		5.0	6.0	14.5	28.5			5.5	33.0		
t_{PLH}	Propagation Delay, t_{X1} SI to HF	3.3	4.0	11.5	23.0			3.5	26.0	ns	2-6
		5.0	2.5	8.0	15.5			2.0	17.5		
t_{PLH}	Fall-Thourgh Time, t_{FTO} SI to OR	3.3	4.0	15.5	30.5			4.0	34.5	ns	2-5
		5.0	3.0	10.5	20.0			2.5	23.0		
t_W	OR Pulse Width, t_{OP}	3.3	13.0	23.5	42.0			12.0	48.5	ns	2-6
		5.0	10.0	13.5	25.5			9.0	29.5		
t_W	HF Pulse Width, t_{X3}	3.3	15.0	27.0	49.5			14.0	57.0	ns	2-6
		5.0	12.0	16.0	30.0			11.0	34.5		
t_{PLH}	Fall-Through Time, t_{FT} SO to IR	3.3	6.5	19.0	37.0			6.0	42.5	ns	2-5
		5.0	5.0	12.5	24.0			4.5	27.5		
t_{PZL}	Output Enable $\overline{OE}$ to O_n	3.3	2.5	7.0	14.0			2.0	16.0	ns	2-8
		5.0	1.5	5.0	10.0			1.0	11.0		
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	3.3	2.0	4.5	9.0			1.5	9.5	ns	2-8
		5.0	1.0	3.5	7.0			1.0	7.5		
t_{PZH}	Output Enable $\overline{OE}$ to O_n	3.3	2.5	7.5	16.5			2.0	18.5	ns	2-7
		5.0	1.5	5.5	11.5			1.0	13.0		
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	3.3	2.0	6.5	13.0			1.5	13.5	ns	2-7
		5.0	1.0	5.0	10.0			1.0	11.0		
f_{SI}	Maximum SI Clock Frequency	3.3	35.0					30.0		MHz	2-3
		5.0	60.0					50.0			
f_{SO}	Maximum SO Clock Frequency	3.3	25.0					20.0		MHz	2-3
		5.0	45.0					35.0			

*Voltage Range 3.3 is 3.3V ± 0.3V

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics (Continued)

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0			1.5	12.5	ns	2-6
t_{PHL}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0			1.5	12.0	ns	2-6
t_{PLH}	Propagation Delay, t_{IHF} SI to > HF	5.0	4.0	10.5	17.0			4.0	19.5	ns	2-6
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	5.0	4.5	10.5	16.5			4.5	19.5	ns	2-6
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	5.0	4.0	10.0	15.5			4.0	17.5	ns	2-6
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0	4.0	13.5	16.5			4.0	19.0	ns	2-6
t_{PLH}	Propagation Delay t_{MRIRH} $\overline{MR}$ to IR	5.0	3.0	8.5	13.5			3.0	15.5	ns	2-6
t_{PHL}	Propagation Delay, t_{MRORL} $\overline{MR}$ to OR	5.0	7.0	16.5	25.5			7.0	29.0	ns	2-6
t_{PHL}	Propagation Delay, t_{MRO} $\overline{MR}$ to Full Flag	5.0	3.5	9.0	14.0			3.5	16.0	ns	2-6
t_{PHL}	Propagation Delay, t_{MRE} $\overline{MR}$ to HF Flag	5.0	8.0	17.5	27.5			8.0	30.5	ns	2-6
t_{PHL}	Propagation Delay, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0	3.0	9.0	15.0			3.0	17.0	ns	2-6
t_W	IR Pulse Width, t_{IP}	5.0	16.5	28.0	43.0			16.5	51.5	ns	2-6
t_W	HF Pulse Width, t_{3F}	5.0	17.5	30.0	46.5			17.5	56.0	ns	2-6
t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	27.0			6.5	31.0	ns	2-6
t_{PHL}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	29.5			6.5	34.5	ns	2-6
t_{PHL}	Propagation Delay, t_{OHF} SO to < HF	5.0	3.5	8.5	13.5			3.5	15.5	ns	2-6
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	5.0	5.0	12.5	19.5			5.0	22.0	ns	2-6
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0	2.5	7.0	11.5			2.5	13.5	ns	2-6

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics (Continued)

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, t_{OE} SO to Empty	5.0	3.5	9.5	15.5			3.0	17.5	ns	2-6
t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	30.5			6.0	35.5	ns	2-6
t_{PHL}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	29.5			6.0	34.5	ns	2-6
t_{PLH}	Propagation Delay, t_{X1} SI to HF	5.0	3.5	10.0	16.0			2.5	18.0	ns	2-6
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0	3.5	13.5	21.0			1.5	24.0	ns	2-5
t_W	OR Pulse Width, t_{OP}	5.0	12.5	17.0	26.0			12.5	30.5	ns	2-6
t_W	HF Pulse Width, t_{X3}	5.0	14.5	20.5	30.5			14.5	36.5	ns	2-6
t_{PLH}	Fall-Through Times, t_{FT} SO to IR	5.0	6.0	15.0	23.5			2.5	28.0	ns	2-5
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0			1.5	12.0	ns	2-8
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	5.0	8.5			1.5	9.5	ns	2-8
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	7.0	12.0			1.5	13.0	ns	2-7
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	7.0	12.0			1.5	13.0	ns	2-7
f_{SI}	Maximum SI Clock Frequency	5.0	55	85				45		MHz	2-3
f_{SO}	Maximum SO Clock Frequency	5.0	42	60				35		MHz	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
$t_W(H)$	SI Pulse Width, t_{SIH}	3.3 5.0	9.0 5.5	16.5 10.5		20.5 12.5	ns	2-6
$t_W(L)$	SI Pulse Width, t_{SIL}	3.3 5.0	8.5 6.5	16.0 12.0		19.5 14.5	ns	2-6
t_S	Setup Time, HIGH or LO(W, D_n to SI	3.3 5.0	−2.0 −1.5	1.0 1.0		1.0 1.0	ns	2-9
t_H	Hold Time, HIGH or LOW, D_n to SI	3.3	1.0 1.0	5.5 4.0		6.0 4.5	ns	2-9
t_W	$\overline{MR}$ Pulse Width, t_{MRW}	3.3 5.0	13.0 8.5	26.0 16.0		30.5 20.0	ns	2-6
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	3.3 5.0	4.5 3.0	8.0 6.0		9.5 7.0	ns	2-9
$t_W(H)$	SO Pulse Width, t_{SOH}	3.3 5.0	4.0 2.5	7.5 5.5		8.5 6.5	ns	2-6
$t_W(L)$	SO Pulse Width, t_{SOL}	3.3 5.0	10.0 6.0	18.0 12.0		21.0 14.0	ns	2-6

*Voltage Range 3.3 is 3.3V ± 0.3V
*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
$t_W(H)$	SI Pulse Width, t_{SIH}	5.0	3.5	6.5		7.5	ns	2-6
$t_W(L)$	SI Pulse Width, t_{SIL}	5.0	6.0	10.0		12.0	ns	2-6
t_S	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0	3.5		4.5	ns	2-9
t_H	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5	3.5		4.5	ns	2-9
t_W	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0	20.0		24.5	ns	2-6
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5	7.5		8.5	ns	2-9
$t_W(H)$	SO Pulse Width, t_{SOH}	5.0	7.5	6.5		8.0	ns	2-6
$t_W(L)$	SO Pulse Width, t_{SOL}	5.0	9.0	14.0		17.0	ns	2-6

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54AC/74AC4024
7-Stage Binary Ripple Counter

General Description

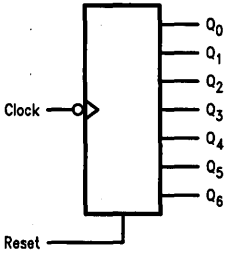
The 'AC4024 consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the 'AC4024 for some designs.

Features

- Outputs directly interface to CMOS, NMOS, and TTL
- Operating voltage range: 2V to 6V
- Low input current: 1 μA
- High noise immunity characteristic of CMOS devices
- Pin and functional compatible to MC1424
- Outputs source/sink 24 mA

Logic Symbol

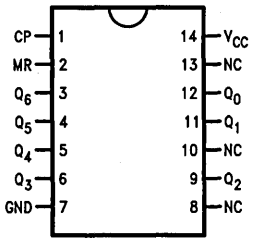


TL/F/10145–1

Pin Names	Description
CP	Clock Pulse Input
MR	Asynchronous Master Reset
Q_0–Q_6	Flip-Flop Outputs

Connection Diagram

Pin Assignment for DIP, Flatpack and SOIC



TL/F/10145–2

NC = No Connection

Section 5

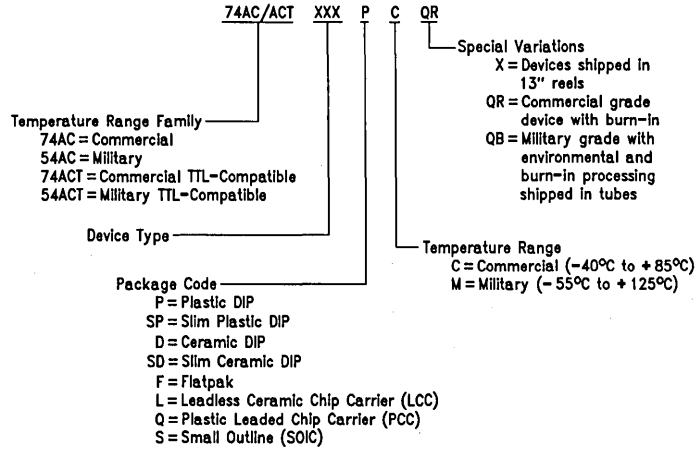
Ordering Information/ Physical Dimensions

Section 5 Contents

National Semiconductor

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



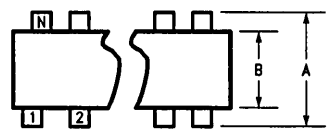
TL/F/10162–1

For most current packaging information, contact Product Marketing.

JEDEC-EIAJ Small Outline Package Comparison

	Dim	14 Pin		16 Pin		20 Pin		24 Pin	
		Min	Max	Min	Max	Min	Max	Min	Max
JEDEC	A	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65)
	B	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
EIAJ	A	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)
	B	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)

Units: Inch (mm)

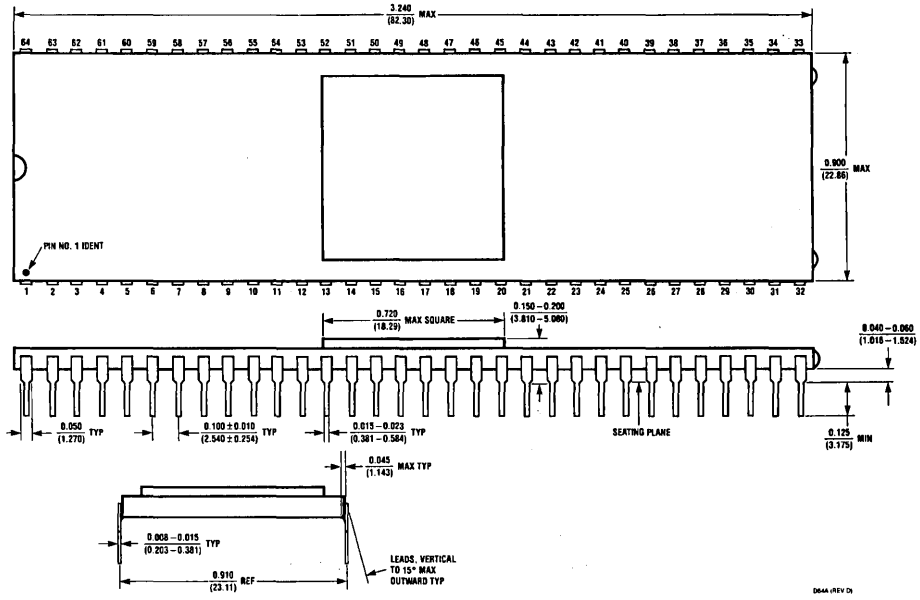


TL/F/10162–2

5

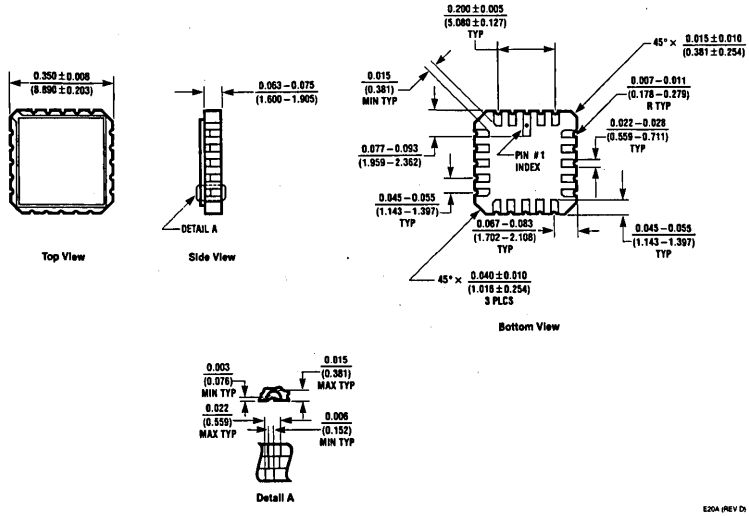
National Semiconductor

64 Lead Side Brazed Ceramic Dual-In-Line Package (D)
NS Package Number D64A

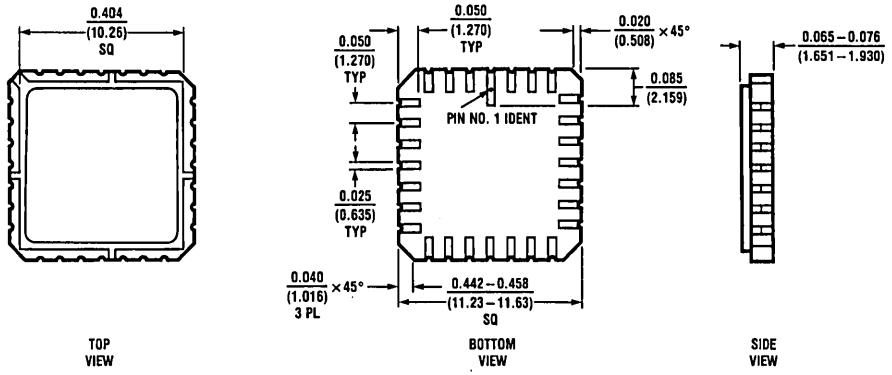


Note: FACT™ Product Shipped WITHOUT Protective Silicon "Bumpers".

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

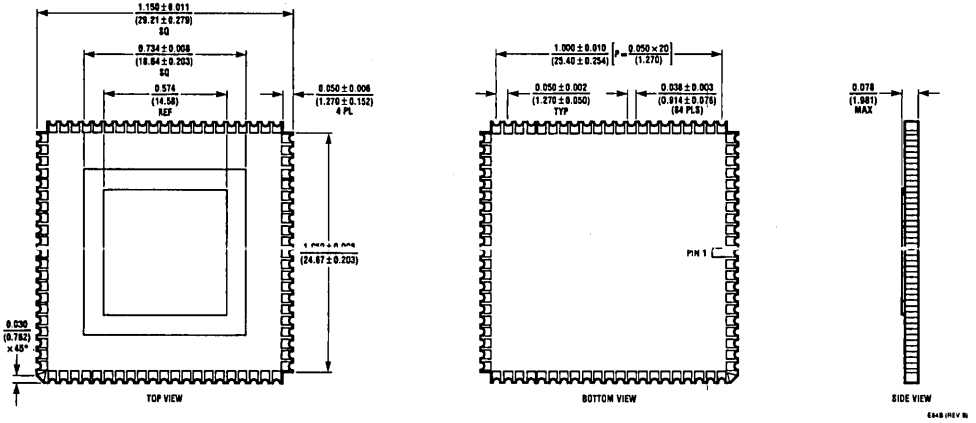


28 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



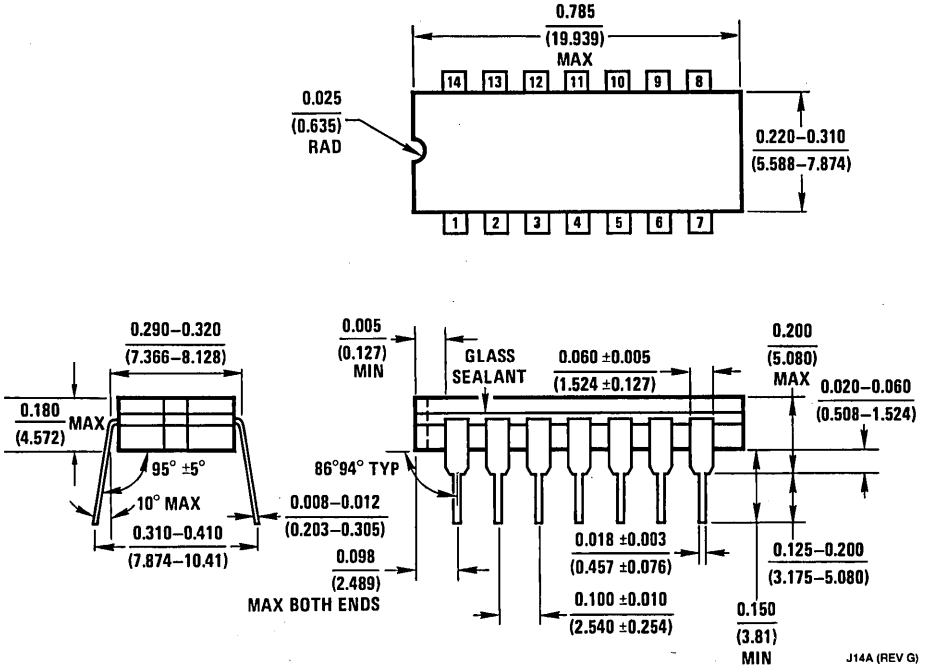
E28A (REV C)

84 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E84B

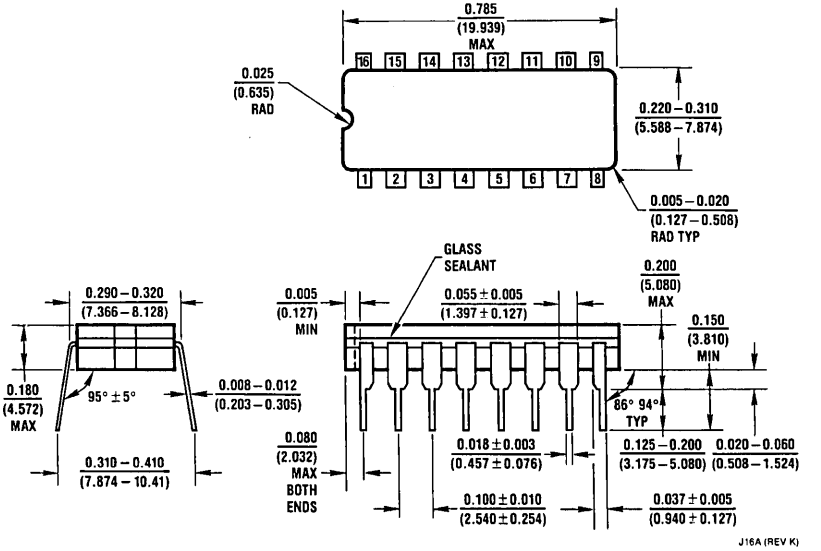


E84B (REV B)

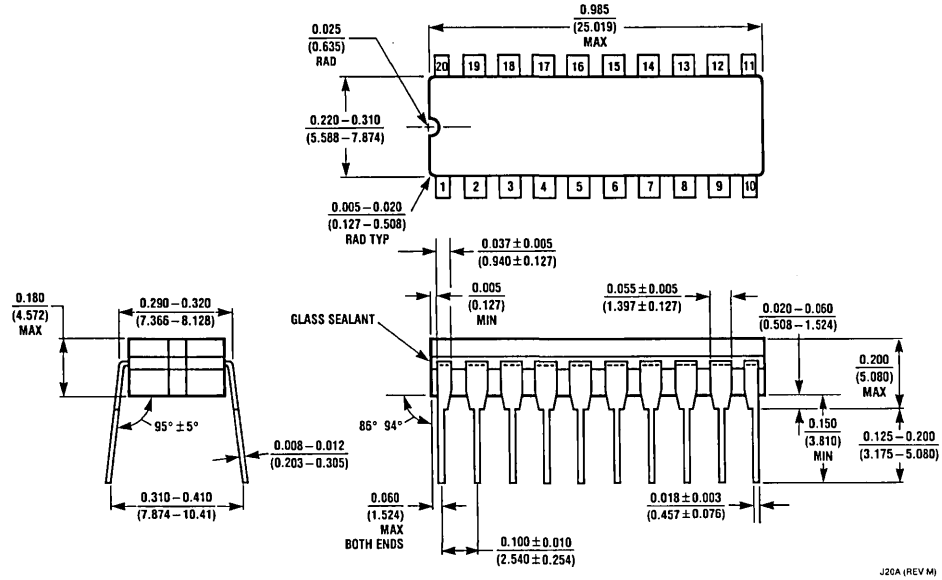
14 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A



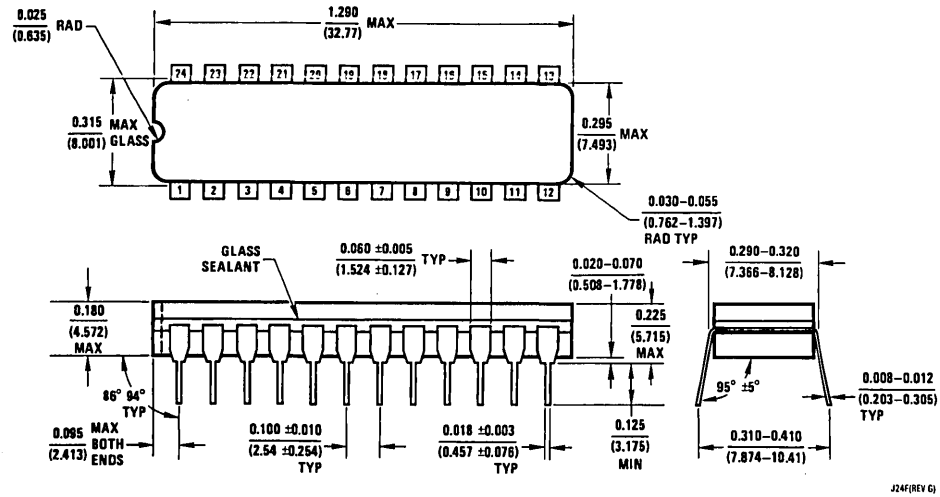
16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



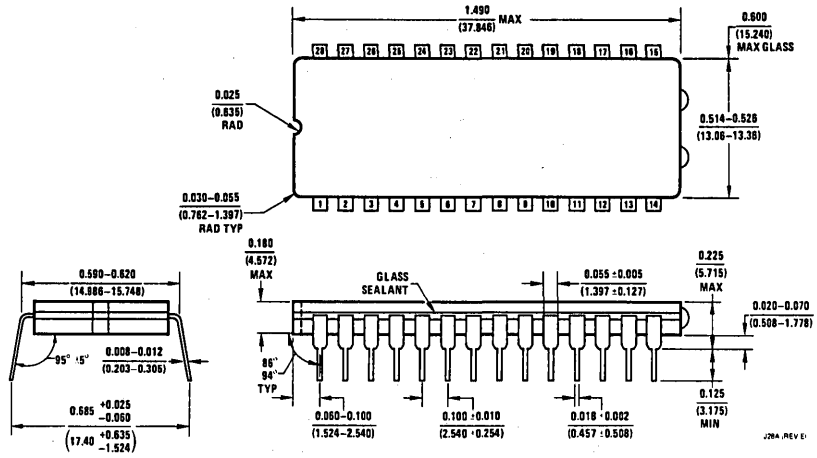
20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

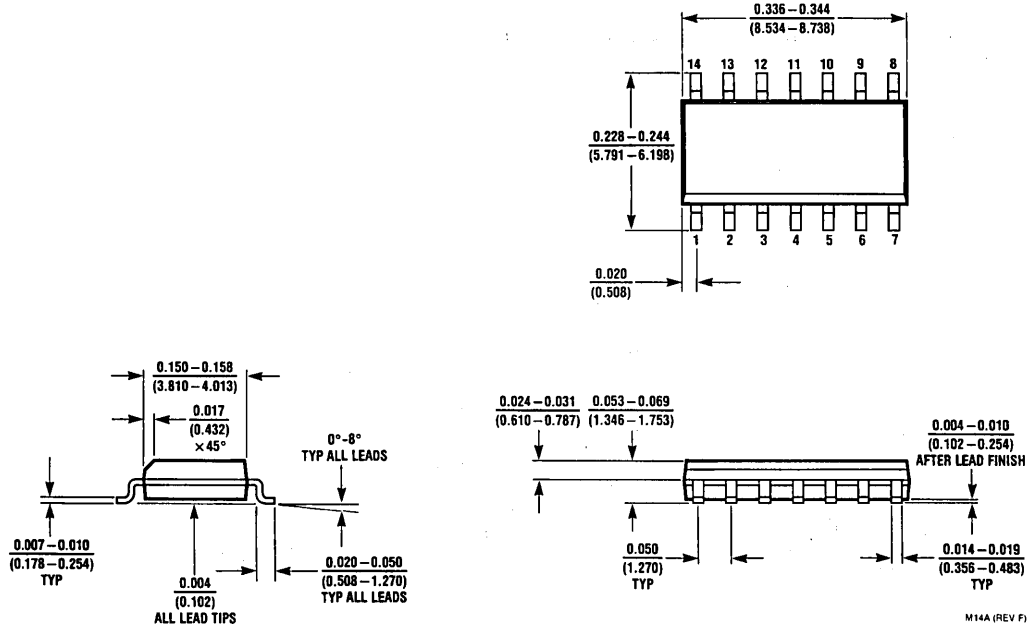


28 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J28A

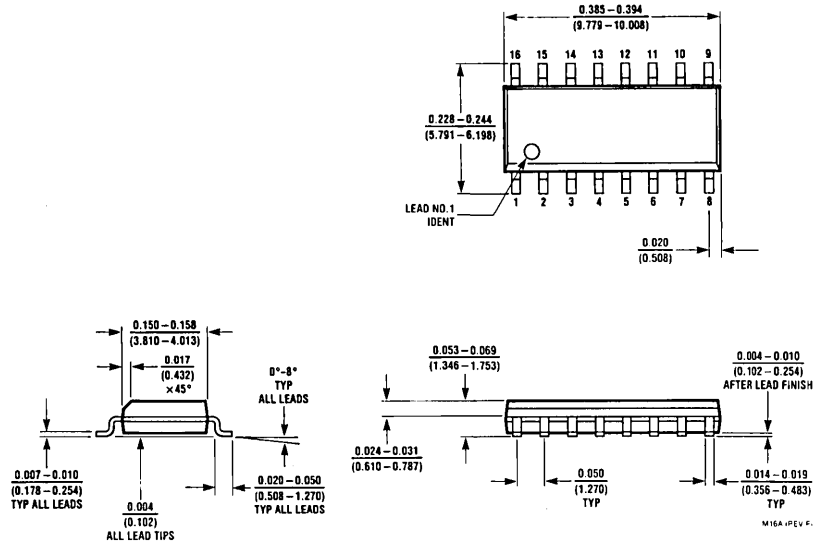


Note: FACT™ Product Shipped WITHOUT Protective Silicon "Bumpers".

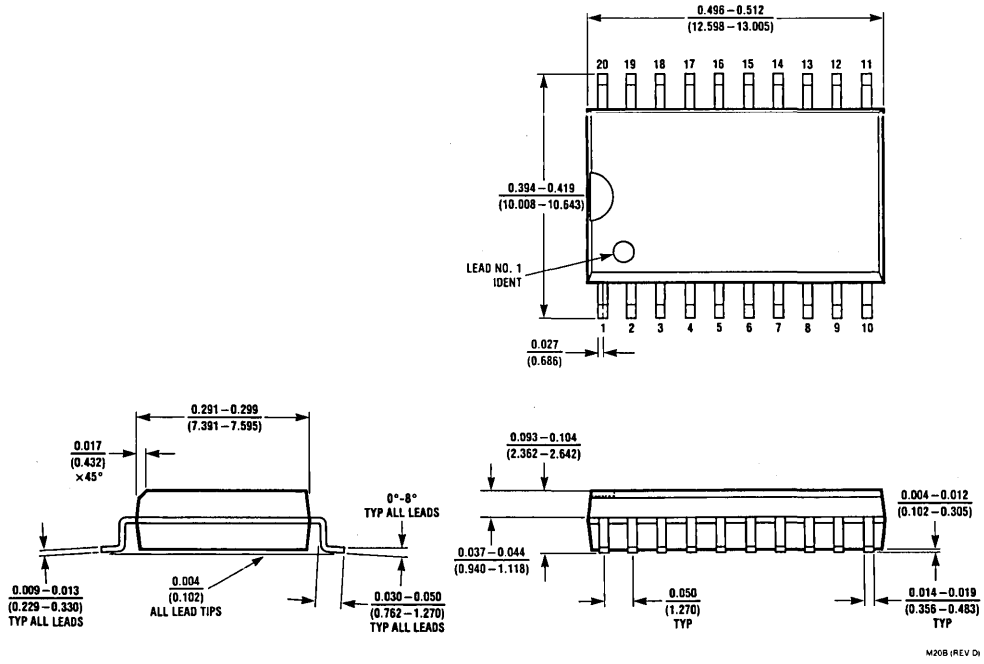
14 Lead Small Outline Integrated Circuit (S)
NS Package Number M14A



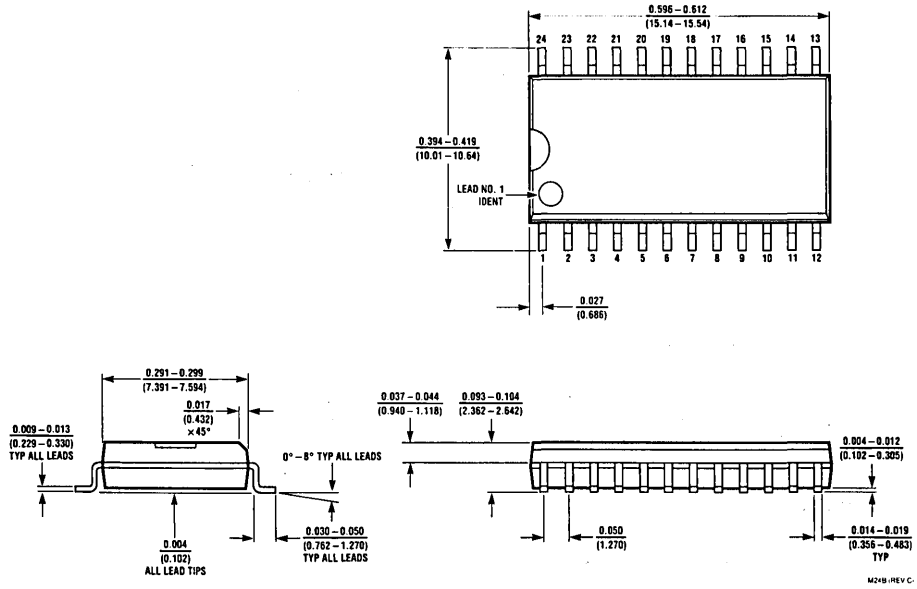
16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



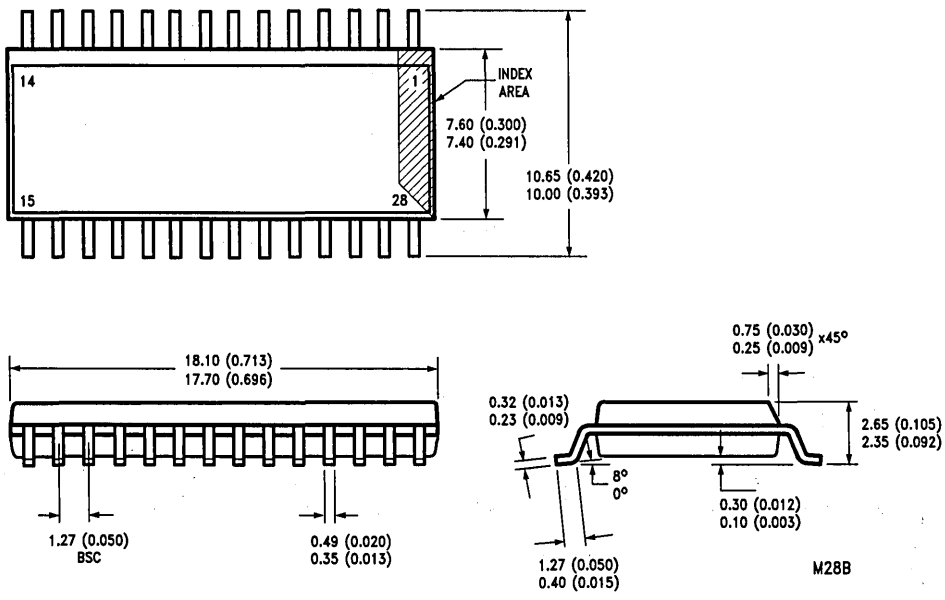
20 Lead Small Outline Integrated Circuit (S)
NS Package Number M20B



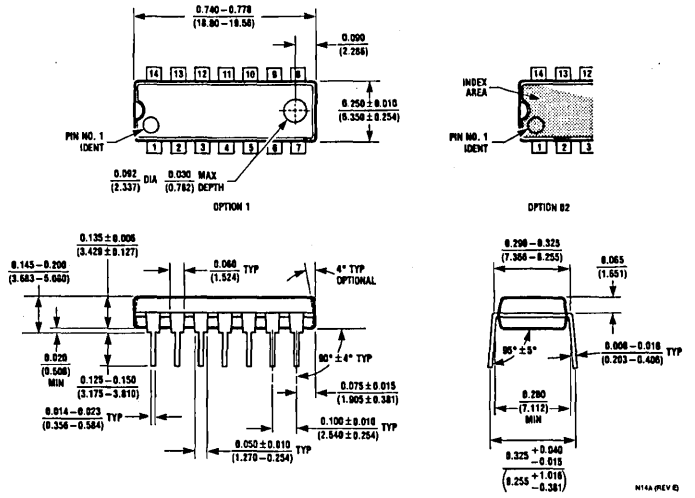
24 Lead Small Outline Integrated Circuit (S)
NS Package Number M24B



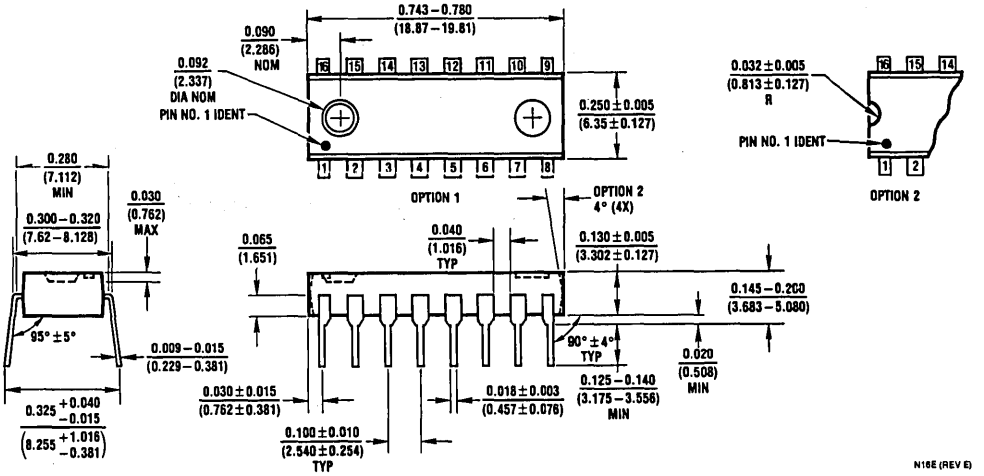
28 Lead Small Outline Integrated Circuit (S)
NS Package Number M28B



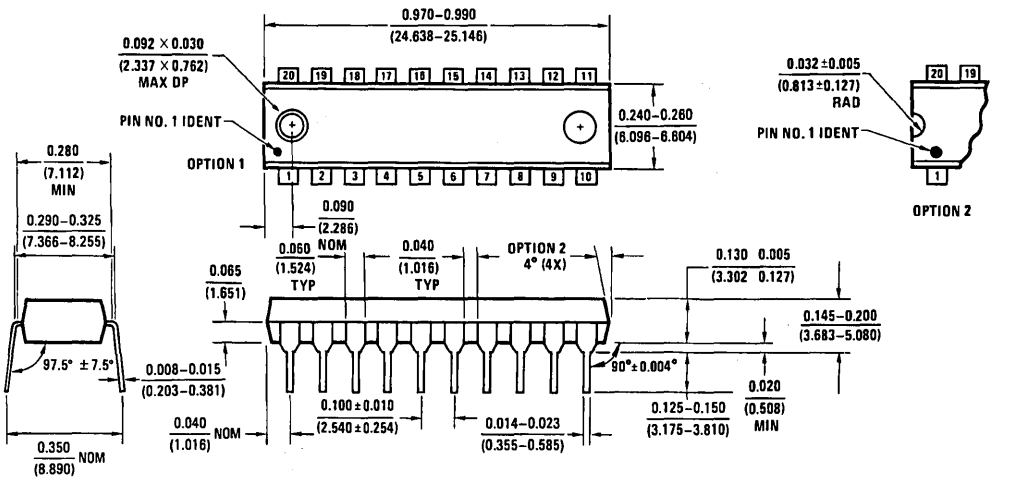
14 Lead Plastic Dual-In-Line Package (P)
NS Package Number N14A



16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

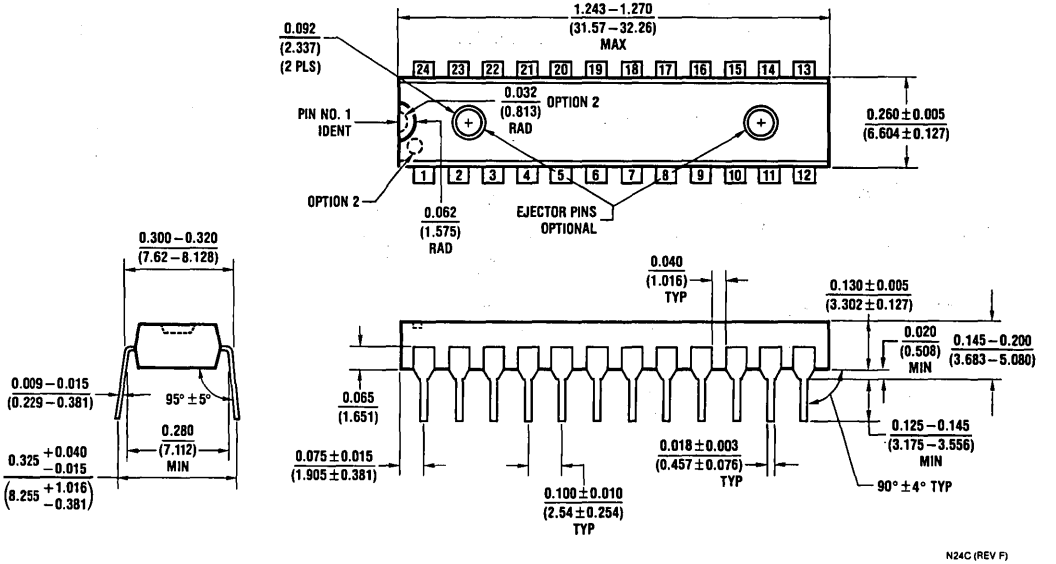


20 Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B



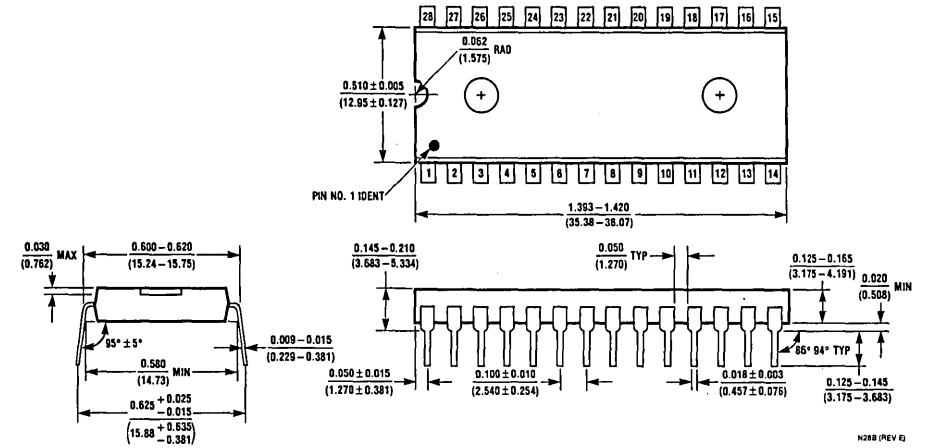
N20B (REV A)

24 Lead Plastic Slim (0.300" Wide) Dual-In-Line Package (SP)
NS Package Number N24C

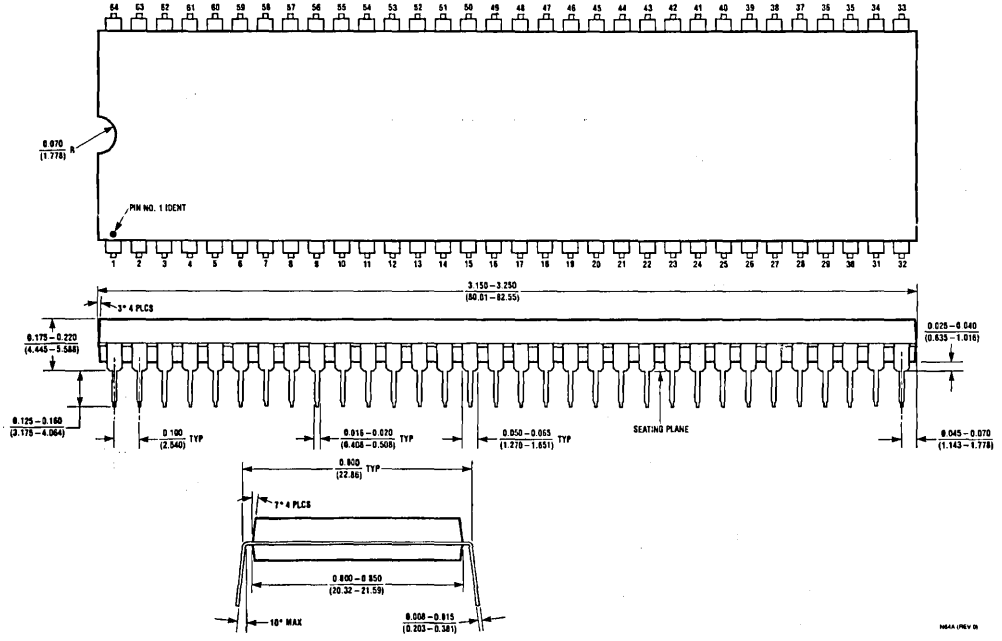


N24C (REV F)

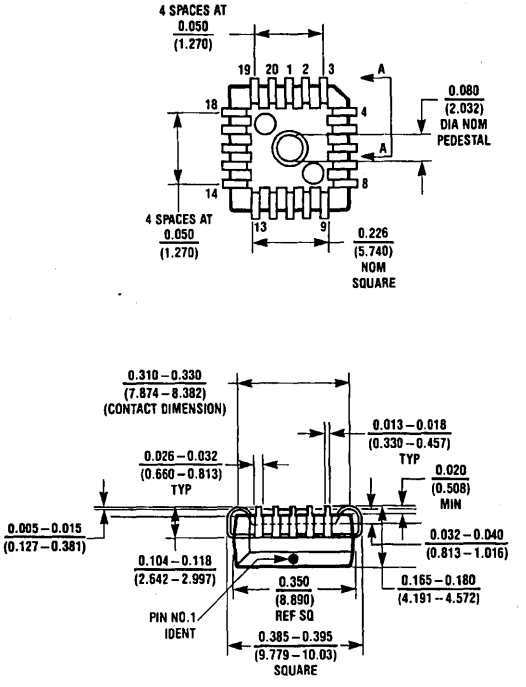
28 Lead Plastic Dual-In-Line Package (P)
NS Package Number N28B



64 Lead Plastic Dual In-Line Package (P)
NS Package Number N64A

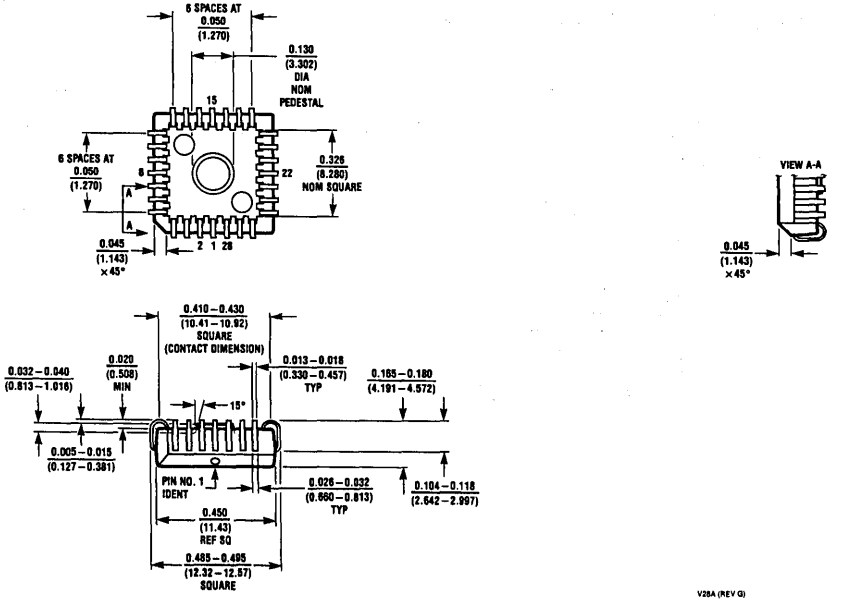


20 Lead Plastic Chip Carrier (Q)
NS Package Number V20A



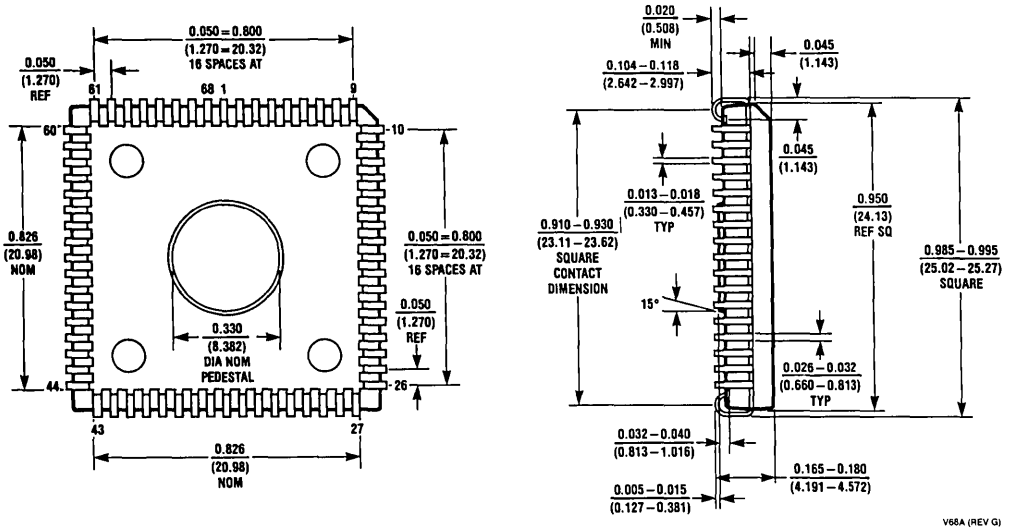
V20A (REV J)

28 Lead Plastic Chip Carrier (Q)
NS Package Number V28A



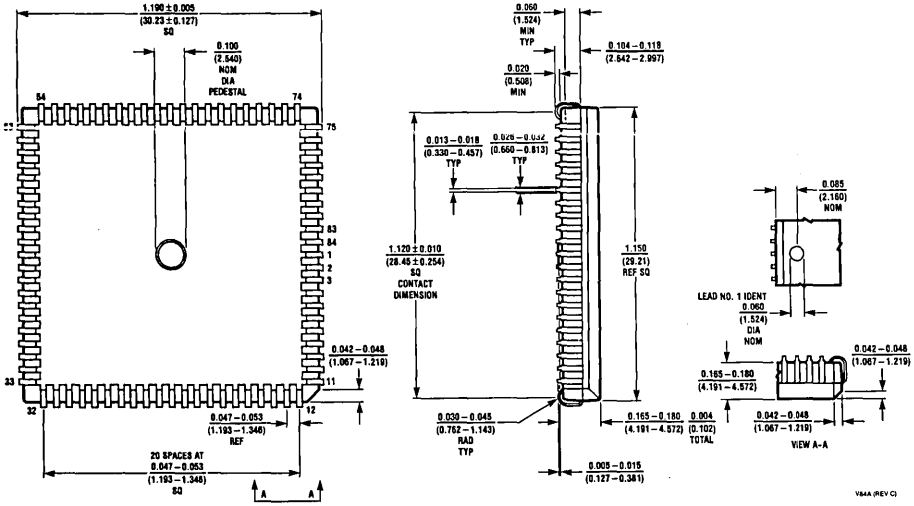
V28A (REV G)

68 Lead Plastic Chip Carrier (Q)
NS Package Number V68A



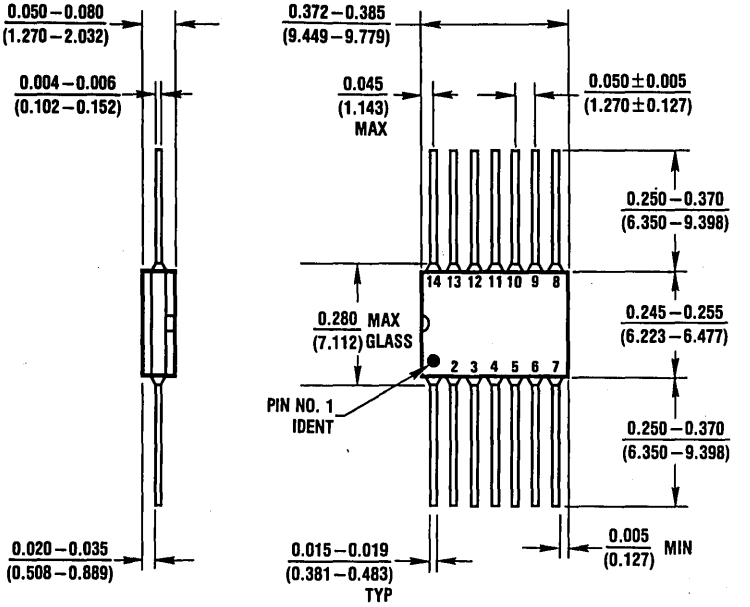
V68A (REV G)

84 Lead Plastic Chip Carrier (Q)
NS Package Number V84A



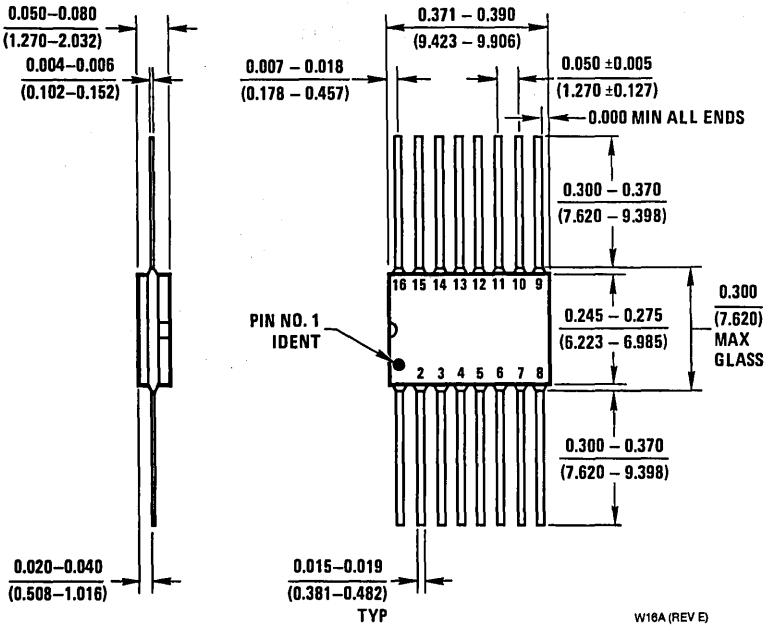
V84A (REV C)

14 Lead Ceramic Flatpak (F)
NS Package Number W14B



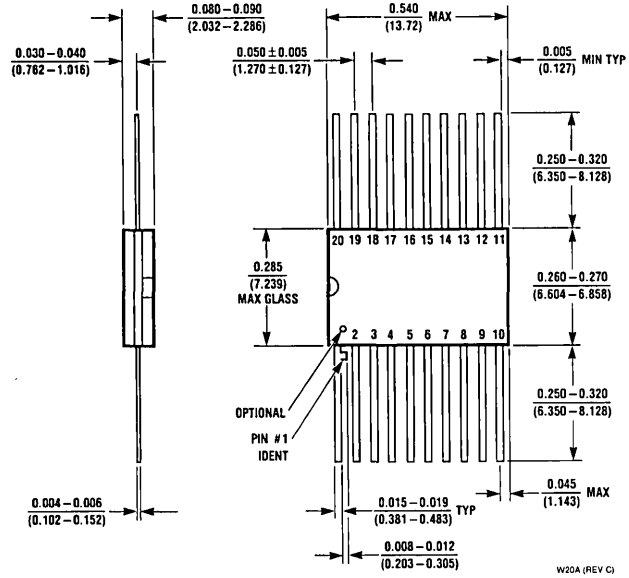
W14B (REV D)

16 Lead Ceramic Flatpak (F)
NS Package Number W16A

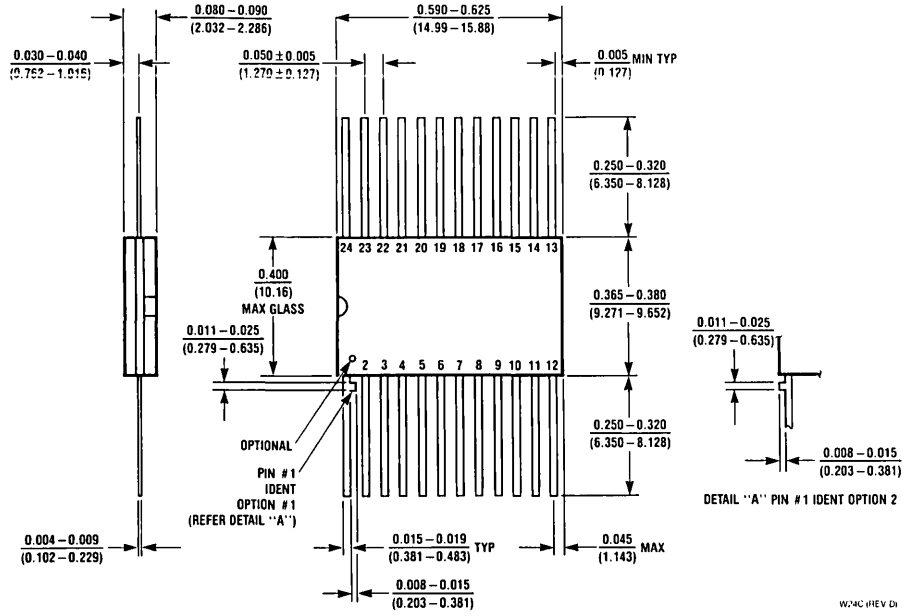


W16A (REV E)

20 Lead Ceramic Flatpak (F)
NS Package Number W20A



24 Lead Ceramic Flatpak (F)
NS Package Number W24C



NOTES

NOTES

National Semiconductor

Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

Please contact your local National sales office for possible complimentary copies. A listing of sales offices follows this bookshelf.

We are interested in your comments on our technical literature and your suggestions for improvement.

Please send them to:

Technical Communications Dept. M/S 16300
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

ALS/AS LOGIC DATABOOK—1987

Introduction to Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

DATA COMMUNICATION/LAN/UART DATABOOK—Rev. 1—1988

LAN IEEE 802.3 • High Speed Serial/IBM Data Communications • ISDN Components • UARTs Modems • Transmission Line Drivers/Receivers

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1988

Dynamic Memory Control • Error Detection and Correction • Microprocessor Applications for the DP8408A/09A/17/18/19/28/29 • Microprocessor Applications for the DP8420A/21A/22A

F100K DATABOOK—1989

Family Overview • F100K Datasheets • 11C Datasheets • 10K and 100K Memory Datasheets Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations Power Distribution and Thermal Considerations • Testing Techniques • Quality Assurance and Reliability

FACT™ ADVANCED CMOS LOGIC DATABOOK—1989

Description and Family Characteristics • Ratings, Specifications and Waveforms Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1988

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—REPRINT

Reprint of 1987 Fairchild FAST Applications Handbook
Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics • Index

GRAPHICS DATABOOK—1988

Advanced Graphics Chipset • Application Notes

INTERFACE DATABOOK—1988

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral Power Drivers • Display Drivers
Memory Support • Microprocessor Support • Level Translators and Buffers • Frequency Synthesis • Hi-Rel Interface

LINEAR APPLICATIONS HANDBOOK—1986

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LINEAR 1 DATABOOK—1988

Voltage Regulators • Operational Amplifiers • Buffers • Voltage Comparators • Instrumentation Amplifiers • Surface Mount

LINEAR 2 DATABOOK—1988

Active Filters • Analog Switches/Multiplexers • Analog-to-Digital • Digital-to-Analog • Sample and Hold
Sensors • Voltage References • Surface Mount

LINEAR 3 DATABOOK—1988

Audio Circuits • Radio Circuits • Video Circuits • Motion Control • Special Functions • Surface Mount

LS/S/TTL DATABOOK—1987

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MASS STORAGE HANDBOOK—1988

Winchester Disk Preamplifiers • Winchester Disk Servo Control • Winchester Disk Pulse Detectors
Winchester Disk Data Separators/Synchronizers and ENDECs • Winchester Disk Data Controller
SCSI Bus Interface Circuits • Floppy Disk Controllers

MEMORY DATABOOK—1988

PROMs, EPROMs, EEPROMs • Flash EPROMs and EEPROMs • TTL I/O SRAMs
ECL I/O SRAMs • ECL I/O Memory Modules

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COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Display/Terminal Management Processor (TMP)
Microcontroller Development Tools

PROGRAMMABLE LOGIC DATABOOK & DESIGN MANUAL—1989

Product Line Overview • Datasheets • Designing with PLDs • PLD Design Methodology • PLD Design Development Tools
Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1989

Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1986

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
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European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETS™ Products • MILS/RETS™ Products • 883/RETS™ Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
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