PACE/blue and green chips...
CPU, support, and
peripheral interface devices

NATIONAL

ERRATA SHEET
PACE DATA BOOK

The September 1975 issue of the PACE Data Book contains the following corrections:

Page 23	The PACE ILE/16 (IPC-168/513J) has been replaced by the PACE ILE/8 (IPC-16A/503J), and this latter part should be used in new designs.
Page 40	The ALE/8 (IPC-16A/508J) has been replaced by the ALE/16 (IPC-16A/518J), and this latter part should be used in new designs.
Pages 45,46	The "J" package in which the Blue/Green Chips are currently supplied is not a hermetic cavity DIP as described. Instead, the package consists of a ceramic substrate to which the chips are fixed. The attached chips are protected by a conformal epoxy coating that provides hermeticity comparable to an Epoxy B package.

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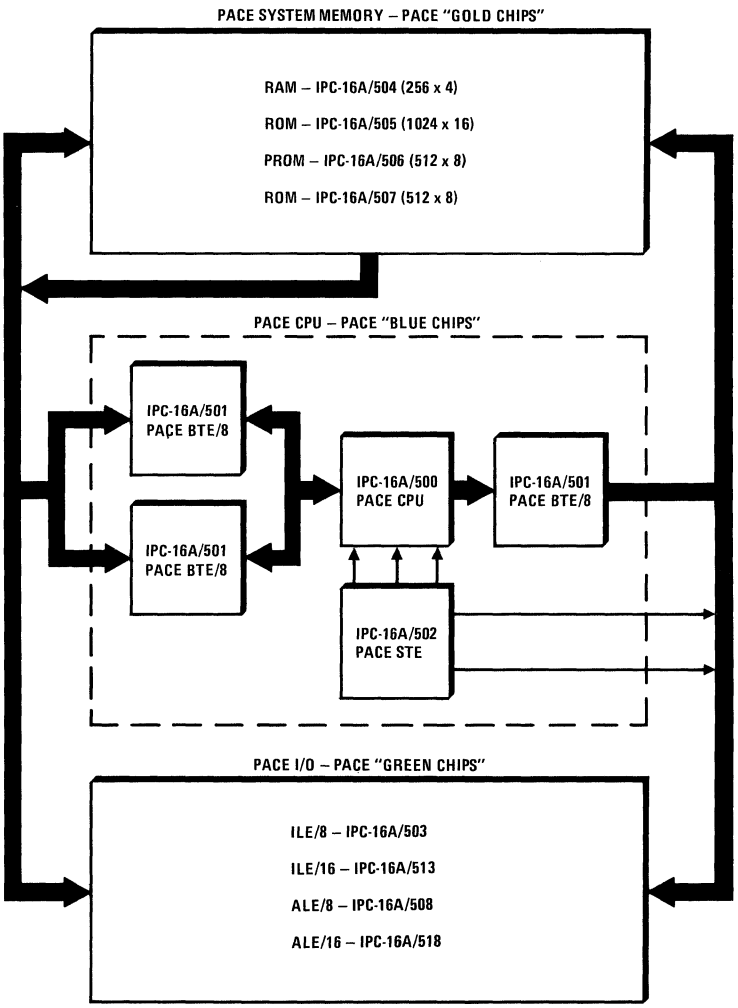
INTRODUCTION

The PACE Data Book contains detailed user information and specifications about the entire PACE family of chips. Included are data related to the PACE CPU, the "Blue Chips" that directly support the microprocessor, the "Green Chips" that provide input/output interfaces to user peripherals and/or memory, and the "Gold Chips" that are specially designed memory devices intended for application in PACE-based systems. Detailed mechanical and packaging information is contained at the back of the PACE Data Book as Physical Dimensions.

In addition to a complete family of PACE chips, PACE APPLICATION CARDS, DEVELOPMENT SYSTEMS, and SOFTWARE DEVELOPMENT AIDS are available to support design and development efforts. Details about these products are given in the PACE Technical Description, available from your local National Semiconductor distributor or sales representative.

The following illustration interrelates the sundry PACE chips.



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IPC-16A/500D MOS/LSI single chip 16-bit microprocessor (PACE)

general description

PACE (Processing And Control Element) is a single-chip, 16-bit microprocessor packaged in a standard, hermetically sealed, 40-pin ceramic dual-in-line package.

Silicon gate, P-channel enhancement mode standard process technology ensures high performance, high reliability and high producibility.

PACE is intended for use in applications where the convenience and efficiency of 16-bit word length is desired while maintaining the low cost inherent in single chip, fixed instruction microprocessors. The basic economics in conjunction with the users' ability to programmatically specify 8 or 16-bit data operations provides the following applications advantages:

(continued on page 3)

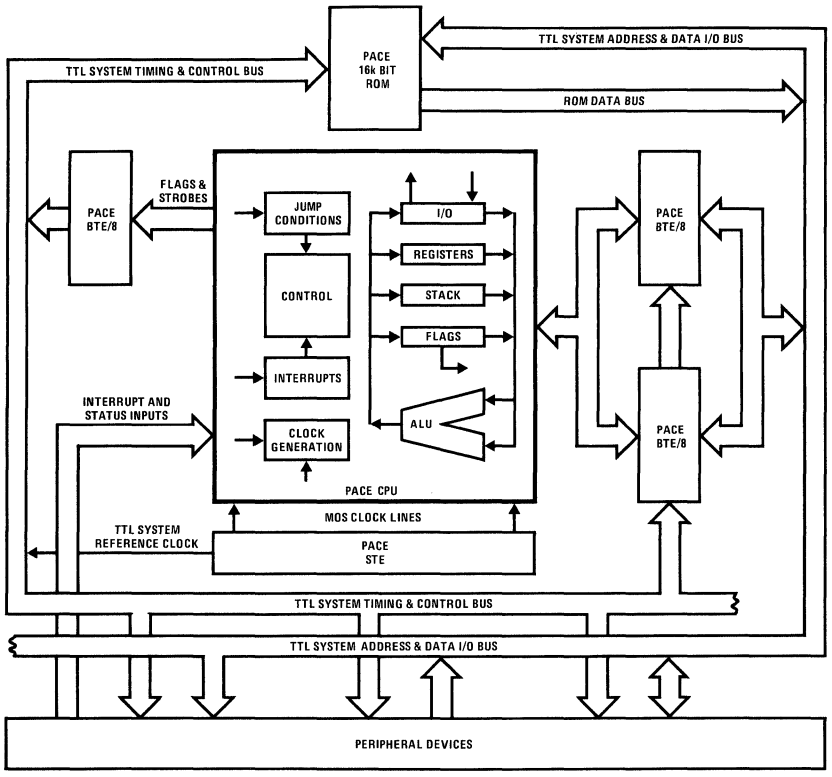
features

■ 16-bit instruction word	Addressing flexibility, speed
■ 8 or 16-bit data word	Wide application
■ Powerful instruction set	Efficient programming
■ Common memory and peripheral addressing	Powerful I/O instructions
■ Shares instructions with National's IMP-16 basic set	Allows software compatibility
■ Four general purpose accumulators	Reduces memory data transfers
■ 10-word stack	Interrupt processing/ data storage
■ Six vectored priority interrupt levels	Simplifies interrupt service and hardware
■ Programmer accessible status register	May be preserved, tested, or modified
■ 2μs microcycle	Fast instruction execution
■ Can utilize IPC-16A/505 1k-by-16 ROM	Single memory package
■ Two clock inputs	Minimum external components

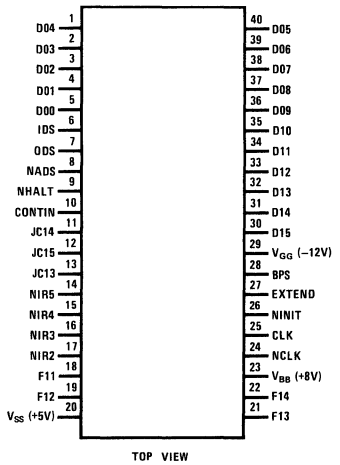
applications

- Test system and instrument control
- Process controllers
- Machine tool control
- Terminal control
- Small business machines
- Traffic controllers
- Word processing systems
- Peripheral device controllers
- Educational systems
- Sophisticated games
- Distributed and multiprocessor systems

block and connection diagrams



Dual-In-Line Package



TOP VIEW

IPC-16A/500D
See Package 2

IPC-16A/500D MOS/LSI single chip 16-bit microprocessor (PACE)

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to Most Positive Supply Voltage (V_{BB}) +0.3V to −20V

Operating Temperature Range 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 300°C

electrical characteristics (T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{BB} = V_{SS} + 3V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SPECIFICATIONS					
D00–D15, F11–F14, ODS, IDS, NADS (These are open drain outputs which may be used to drive DS3608 sense amplifiers, or may be used with pull-down resistors to provide a voltage output.)					
Logic "1" Output Current (Except F11–F14)	V_{OUT} = 2.4V		−2.0		mA
Logic "1" Output Current, F11–F14 (Note 7)	V_{OUT} = 2.0V		−2.0		mA
Logic "0" Output Current	$V_{GG} \leq V_{OUT} \leq V_{SS}$			±10	μA
NHALT, CONTIN (Low Power TTL Output.)					
Logic "1" Output Voltage	I_{OUT} = −650μA		3.0		V
Logic "0" Output Voltage	I_{OUT} = 400μA		−1.0		V
INPUT SPECIFICATIONS					
D00–D15, NIR2–NIR5, EXTEND, JC13–JC15, CONTIN, NINIT, NHALT (These are TTL compatible inputs.) (Note 2)					
Logic "1" Input Voltage		V_{SS}−1		V_{SS}+0.3	V
Logic "0" Input Voltage		V_{SS}−7		V_{SS}−4	V
Pullup Transistor "ON" Resistance (D00–D15) (Note 3)	$V_{IN} = V_{SS} - 1V$		4		kΩ
Pullup Transistor "ON" Resistance (Except D00–D15)	$V_{IN} = V_{SS} - 1V$		2		kΩ
Logic "0" Input Current (D00–D15)	V_{IN} = 0V		−1.0		mA
Logic "0" Input Current (Except D00–D15)	V_{IN} = 0V		−2.0		mA
Input Capacitance	$V_{IN} = V_{SS}$, f_T = 500 kHz		10		pF
BPS (This is a MOS Level Input.) (Note 4)					
Logic "1" Input Voltage		V_{SS}−1		V_{SS}+0.3	V
Logic "0" Input Voltage		V_{GG}		V_{SS}−7	V
Logic "1" Input Current	$V_{IN} = V_{SS} - 1V$		5		μA
CLK, NCLK (These are MOS Clock Inputs)					
Clock "1" Voltage (Note 5)		V_{SS}−1		V_{SS}+0.3	V
Clock "0" Voltage		V_{GG}		V_{GG}+1	V
Input Capacitance (Note 6)			80		pF
Bias Supply Current	$V_{BB} = V_{SS} + 3.0V$		30		μA
Average Power Dissipation	t_p = 0.5μs, T_A = 25°C		700		mW
TIMING SPECIFICATIONS (See *Figures 7 to 10* for additional timing information.)					
CLK, NCLK (See *Figure 1*) (Referenced to 10% and 90% Amplitude)					
Rise and Fall Time (t_r, t_f)		10			ns
Clock Width ($t_{W\,CLK}$, $t_{W\,NCLK}$)		240			ns
Clock Overlap ($t_{OV\,A}$, $t_{OV\,B}$)			−25		ns
Clock Period (t_p)			0.5		μs
EXTEND					
Individual Extend Duration (t_{EX})				2.0	μs
Propagation Delay					
F11–F14 (Note 8)	V_{OUT} = 2.4V		100		ns
NHALT, CONTIN (Note 9)	C_L = 20 pF		100		ns
NADS, IDS, ODS, D00–D15 (Note 8)	V_{OUT} = 2.4V		60		ns
D00–D15 Input Setup Time (Note 10)			75		ns
NINIT Initialization Pulse Width		8			clock cycles
NIR2–NIR5 Input Pulse Width to Set Latch		1			clock cycles

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

Note 2: Pullup transistor provided on chip. (See *Figure 6.)*

Note 3: Pullup transistors on JC13, JC14, JC15 are turned on one out of 8 clock intervals. Pullup transistors on D00–D15 are turned on during last clock period of Input Data Strobe (IDS). Other pullup transistors are on continuously when in data input mode.

Note 4: Pulldown transistor provided on chip.

Note 5: Clamp diodes and series damping resistors may be required to prevent clock overshoot.

Note 6: Capacitance is not constant and varies with clock voltage and internal state of processor.

Note 7: For $V_{SS} \geq V_{OUT} \geq 2.0V$ output current is a linear function of V_{OUT}.

Note 8: Delays measured from valid logic level on clock edge initiating change to valid current output level.

Note 9: Delay measured from valid logic level on clock edge initiating change to valid voltage output level.

Note 10: With respect to end of Input Data Strobe (IDS). See *Figure 7.*

general description (con't)

PACE is particularly efficient when handling both 8 and 16-bit interfaces within the same microprocessor based system. Requirements for external hardware are minimized without sacrificing coding efficiency.

PACE is extremely cost effective in applications dominated by 8-bit data element interfaces. Coding and address generation efficiencies, as well as operating speeds for double precision operations found only in 16-bit microprocessors are extended to the 8-bit system.

The principal resources featured in PACE to minimize system program and read/write storage while increasing throughput include:

FOUR 16-BIT GENERAL PURPOSE WORKING REGISTERS available to the user reduce the number of memory load and store operations associated with saving temporary and intermediate results in system memory. This results in increased throughput with reduced program and data storage requirements.

AN INDEPENDENT 16-BIT STATUS AND CONTROL FLAG REGISTER automatically and continuously preserves system status. The user may operate on its contents as data, allowing masking, testing and modification of several bit fields simultaneously.

A TEN WORD (16-BIT) LAST-IN, FIRST-OUT (LIFO) STACK automatically preserves return addresses during interrupt servicing and sub-routine execution. The presence of a stack inherently decreases response time to interrupts while eliminating both program and read/write system storage overhead associated with storing stack information outside the microprocessor chip. In some applications the 10-word stack plus on-chip registers can totally eliminate the need for off-chip read/write memory.

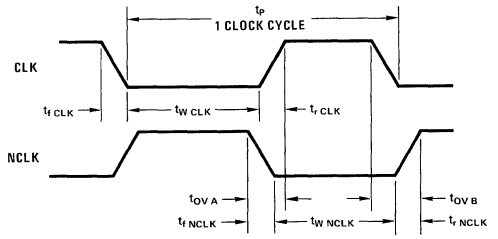
STACK FULL/STACK EMPTY interrupts are provided to facilitate off-chip stack storage in those applications where additional stack capacity is desirable.

A SIX LEVEL, VECTORED PRIORITY INTERRUPT SYSTEM internal to the chip provides automatic interrupt identification, eliminating both program storage overhead and the time normally required to poll peripherals in order to identify the interrupting device. When more than six interrupts are involved, more than one peripheral may be placed on a priority-level by means of a simple open collector connection to the appropriate priority interrupt request line.

FOUR SENSE INPUTS AND FOUR CONTROL FLAG OUTPUTS allow the user to respond directly to specific combinations of status present in the microprocessor based system. This ability to respond directly to system status requires no external hardware and allows appropriate control signal outputs to be generated programmatically, eliminating costly hardware, program overhead and throughput associated with implementing these functions over the system data bus.

Other PACE features which minimize the cost of external support hardware include easily generated clock inputs and I/O cycle extend capability.

The PACE single chip 16-bit microprocessor permits the implementation of a complete microprocessor system with 16,384 bits of read-only program storage and TTL data bus interface in fewer than a dozen standard support packages, as shown in the diagram on the first page.



Note: Clock timing referenced to 10% and 90% amplitude points.

FIGURE 1. Clock Timing

FUNCTIONAL DESCRIPTION

The PACE microprocessor, shown in *Figure 2*, provides 16-bit parallel data processing capability. This word length provides considerable convenience for addressing memory and peripheral devices and provides sufficient accuracy that many applications will not require the use of double precision arithmetic. It also provides increased speed by processing twice as many bits per cycle and reducing time consuming memory accesses. However, for those applications not requiring high accuracy, or for character processing, PACE provides the ability to operate on 8-bit data, while still providing 16-bit instructions and addressing capability.

Data Storage

Seven data registers are provided, four of which are directly available to the programmer (as accumulators AC0 to AC3) for data storage and address formation. AC0 is the principal working register, AC1 is the secondary working register, and AC2 and AC3 are page pointers or auxiliary data registers. The other three registers serve as a program counter and two temporary registers are used by the control section to effect the PACE instruction set.

Additional data storage is provided for up to ten words by a last-in, first-out or push-pull stack. The stack is used primarily for storing the contents of the program counter during subroutine execution and interrupt servicing. The stack may also be used for storing status information or data; in some applications, such as device controllers, the stack plus four accumulators may provide enough storage to eliminate the need for external read-write memory. For applications where the 10-word capacity of the stack is insufficient, external read-write memory may be used as a stack extension. This is facilitated by the provision of stack full and stack empty interrupts, allowing implementation of a simple stack service routine.

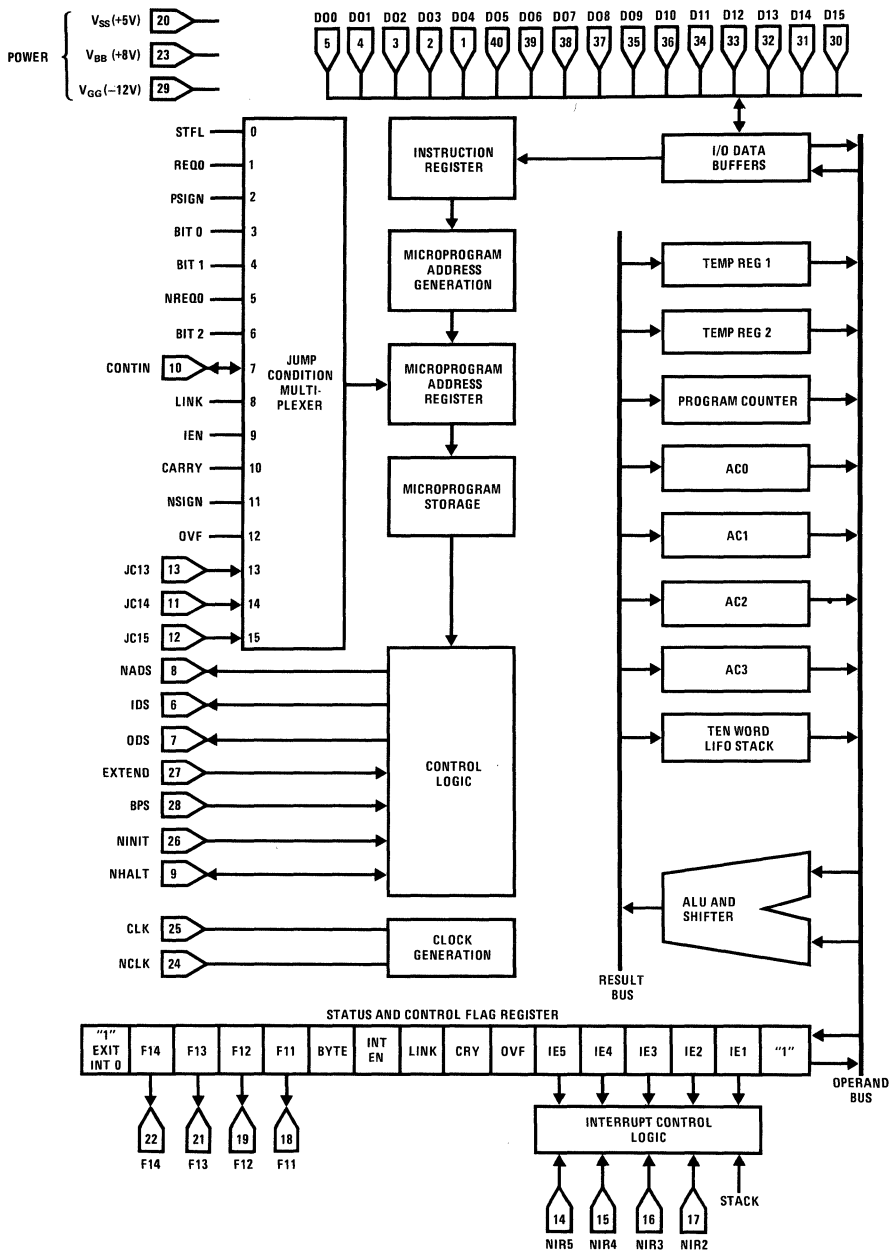


FIGURE 2. PACE Detailed Block Diagram

ALU

The arithmetic and logic unit (ALU) provides the data manipulation capability which is an essential feature of any microprocessor. The operations provided by the ALU include AND, OR, XOR, complement, shift left, shift right, mask byte and sign extend. Both binary and (4-digit per word) binary-coded-decimal (BCD) addition capability are provided, thus eliminating the program storage and execution time required to perform BCD to binary conversion.

A unique feature of the PACE ALU is the ability to operate on either 8 or 16-bit data, as specified by the programmer through the use of a status flag. This feature allows character oriented and other 8-bit applications to be implemented and executed using an 8-bit peripheral data bus and read-write memory, while address formation and instruction storage are implemented in the more effective 16-bit data length.

Status

All status and control bits for PACE are provided in a single status flag register, whose contents may be loaded from or to any accumulator or the stack. This allows convenient testing, masking and storage of status. In addition, a number of status bits may be tested directly by the conditional branch instruction, and any bit may be individually set or reset. The function of each bit in the status flag register is listed in Table I and described

briefly below. The carry flag is set to the state of the carry output resulting from binary and BCD arithmetic instructions, and serves as a carry input for some of these instructions. The overflow flag is set true if an arithmetic overflow results from a binary arithmetic instruction.

TABLE I. Status Flag Register Bit Functions

Register Bit	Flag Name	Function
0	"1"	Not used—always logic 1
1	IE1	Interrupt Enable Level 1
2	IE2	Interrupt Enable Level 2
3	IE3	Interrupt Enable Level 3
4	IE4	Interrupt Enable Level 4
5	IE5	Interrupt Enable Level 5
6	OVF	Overflow
7	CRY	Carry
8	LINK	Link
9	IEN	Master Interrupt Enable
10	BYTE	8-bit data length
11	F11	Flag 11
12	F12	Flag 12
13	F13	Flag 13
14	F14	Flag 14
15	"1"	Always logic 1, addressed for Interrupt 0 exit

The link flag serves as a 1-bit extension for certain shift and rotate instructions. The byte flag is used to specify an 8-bit data length for data processing instructions, while arithmetic operations for address formation remain at the 16-bit data length. In the 8-bit data mode, modifications of the carry, overflow and link flag are based on the eight least significant data bits only.

Four flags (bits 11—14) are provided which may be assigned functions by the programmer. These flags drive output pins and may be used to directly control system functions or as software status flags. Bits 0 and 15 of the status register have not been implemented in hardware and always appear as a logic 1. The interrupt enable flags are explained below.

Control

The operation of the PACE microprocessor consists of repeatedly accessing or fetching instructions from the external program store and executing the operations specified by these instructions. These two steps are carried out under the control of a microprogram (the microprocessor is not designed for user microprogramming). The microprogram is similar to a state table specifying the series of states of system control signals necessary to carry out each instruction. Microprogram storage is provided by a programmable logic array, and microprogram routines are implemented to fetch and execute instructions. The fetch routine causes an instruction address to be transferred from the program counter register to the I/O bus and initiates an input data operation. When the instruction is provided on the data bus, the fetch routine causes it to be loaded into the instruction register. The instruction operation code is transformed into the address of the appropriate instruction-execution routine by the address generation logic. As the last step of the fetch routine, this address is loaded into the microprogram address register, causing a branch to the appropriate instruction execution routine. The execution routine consists of one or more microinstructions to implement the functions required by the instruction. For example, the routine for a register ADD instruction would access the two accumulators to be added over the operand bus, cause the ALU to perform an ADD operation, load the carry and overflow flags from the ALU and store the result in the specified accumulator. The control logic interprets the microinstructions to carry out these operations. The final step of the execution routine is a jump back to the fetch routine to access the next instruction. Each microcycle requires 2μs and 4 or 5 microcycles are typically required to fetch and execute a machine instruction. Other routines implemented by the microprogram include interrupt servicing and system initialization. The microprogram controls the operation of a conditional jump multiplexer which is used to specify 16 conditions for the conditional branch instruction. The conditions which may be tested are indicated in Table II and include four signal inputs to the chip, which may be used to test external system conditions.

TABLE II. Branch Conditions

Number	Mnemonic	Condition
0	STFL	Stack full
1	REQ0	(AC0) equal to zero(1)
2	PSIGN	(AC0) has positive sign(2)
3	BIT 0	Bit 0 of AC0 true
4	BIT 1	Bit 1 of AC0 true
5	NREQ0	(AC0) is non-zero(1)
6	BIT 2	Bit 2 of AC0 is true
7	CONTIN	CONTIN (continue) input is true
8	LINK	LINK is true
9	IEN	IEN is true
10	CARRY	CARRY is true
11	NSIGN	(AC0) has negative sign(2)
12	OVF	OVF is true
13	JC13	JC13 input is true
14	JC14	JC14 input is true
15	JC15	JC15 input is true

Note 1: If the selected data length is 8 bits, only bits 0-7 of AC0 are tested.

Note 2: Bit 7 is the sign bit (instead of bit 15) if the selected data length is 8 bits.

The control circuitry may be initialized at any time by use of the NINIT input signal. This will cause the stack addressing circuitry, all flags and the program counter to be set to zero, and the strobes to go false and level zero interrupt enable to go true. This signal should always be used to initialize the processor after applying power. The first instruction after initialization is accessed from location zero.

Interrupts

The PACE microprocessor provides a six level, vectored, priority interrupt structure. This allows automatic identification of an interrupting device's level and allows all devices on an interrupt level to be enabled or disabled as a group, independent of other interrupt levels. An individual interrupt enable is provided in the status register for each level, as shown in *Figure 3*, and a master

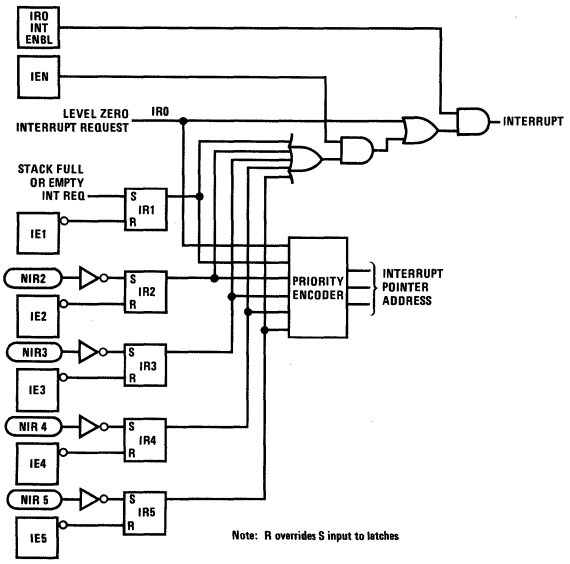


FIGURE 3. Interrupt System

interrupt enable (IEN) is provided for all 5 lower priority levels as a group. Negative true interrupt request inputs are provided to allow several interrupts to be "wire-ORed" on each input. When an interrupt request occurs, it will set the interrupt request latch if the corresponding interrupt enable is true. The latch will be set by any pulse exceeding one clock period in duration, which is useful for capturing narrow timing or control pulses. If the master interrupt enable (IEN) is true, then an interrupt will be generated. During the interrupt sequence an address is provided by the output of the priority encoder and is used to access the pointer for the highest-priority interrupt request (IR0 is highest priority, IR5 is lowest priority). The pointers are stored in locations 2–7 (see Table III) for interrupt requests 1–5 and 0, respectively. The pointer specifies the starting address of the interrupt service routine for that particular interrupt level. Before executing the interrupt service routine, the program counter is pushed on the stack and IEN is set false. The interrupt service routine may set IEN true after turning off the interrupt enable for the level currently being serviced (or resetting the interrupt request). (The interrupt enables may be set and reset using the SFLG and PFLG instructions.)

The non-maskable level zero interrupt (IR0) is an exception to this interrupt procedure. It has a program counter storage location pointer (the program counter is not stored on the stack for this particular interrupt in order to preserve the processor state) which is followed by the level zero interrupt service routine. The IR0 interrupt enable is cleared when a level zero interrupt occurs (IEN is unaffected) and may be set true by addressing (non-existent) status flag 15. This allows execution of one more instruction (typically JMP@) to return from the IR0 interrupt routine before another interrupt will be acknowledged. This interrupt level is typically used by the control panel, which then can always interrupt the application program and does not affect system status. The control panel service routine interprets and executes the functions specified by control panel switches and displays selected data on the panel lights. Level zero interrupts are generated by driving the NHALT signal line low.

TABLE III. Interrupt Pointer Table

8	Int 0 Program
7	Int 0 PC Pointer
6	Int 5 Pointer
5	Int 4 Pointer
4	Int 3 Pointer
3	Int 2 Pointer
2	Int 1 Pointer
1	Not Assigned
Loc 0	Initialization Inst

Data Input and Output

All data transfers between PACE and external memories or peripheral devices take place over the 16 data lines (D00–D15) and are synchronized by the 4 control signals (NADS, IDS, ODS, and EXTEND). Data transfers occur during each instruction access and during the data accesses required by memory reference instructions. This class of instructions could perhaps more properly be called the "I/O reference class" in the case of the PACE microprocessor, since all data transfers, whether with memory or peripheral devices or a central processor data bus, occur through the execution of these instructions. This unified bus architecture is in contrast with many other microprocessors and minicomputers that have one instruction type (I/O class) for communication with peripheral devices and another instruction type (memory reference class) for communication with memories. The advantage of the approach used by PACE is that a wider variety of instructions (the entire memory reference class) is available for communication with peripherals. Thus, the DSZ (decrement and skip if zero) instruction can be used to decrement a peripheral device register, or the SKAZ (skip if AND is zero) instruction can be used to test the contents of a peripheral device status register. The LD (load) and ST (store) instructions are used for simple data transfers.

All I/O transactions consist of an address output interval followed by a data transfer interval. The address specifies a memory location or peripheral device. The allocation is entirely up to the user (within the requirements for interrupt pointers). A straightforward allocation would be to assign all addresses from 0000_{16} to $7FFF_{16}$ as memory addresses and all addresses from 8000_{16} to $FFFF_{16}$ as peripheral device addresses. In this case, the most significant address bit specifies whether the transaction is with memory or a peripheral device. A variety of easily decoded address allocation schemes may be used, depending on the amount of ROM, RAM, peripheral devices and the particular application. Both address and data words are transmitted or received as 16-bit parallel data over the data lines (D00–D15). If 8-bit data is being transferred, the unused bits can be treated as "don't care" bits by the hardware and the 8-bit data length selected by the software.

Data transfer operations are synchronized by the NADS (Address Data Strobe), IDS (Input Data Strobe), ODS (Output Data Strobe) and EXTEND signals as shown in *Figure 4.* Address data is provided on the 16 data lines. An NADS is provided in the center of the address data and may be used to strobe the address into an address latch. A number of memory products provide address

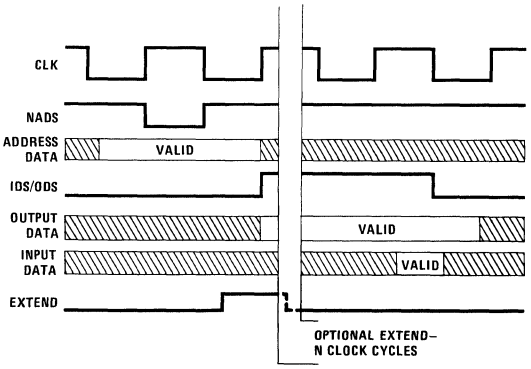


FIGURE 4. PACE I/O Timing

latches on the chip, which avoids the need for implementing this function externally. The input data strobe and output data strobe indicate the type of data transfer and may be used to enable TRI-STATE® I/O buffers and gate data into registers or memories as required by the system design. The EXTEND input allows the I/O cycle time to be extended by multiples of the clock cycle to adapt to a variety of memory and peripheral devices.

INSTRUCTIONS

The PACE microprocessor provides a general-purpose mix of 45 instruction types. The memory reference instructions utilize a flexible memory addressing scheme providing three floating memory pages and one fixed page of 256 words each. The register instructions provide convenient data manipulation without requiring a memory access. The data transfer instructions provide a means of moving data among the functional blocks of the microprocessor system.

Addressing Modes

Instructions which use both direct and indirect memory addressing are included in the PACE instruction set. Three modes of direct memory addressing are available: base page, program counter relative, and index register relative. The mode of addressing is specified by the XR field of the instruction as illustrated in *Figure 5*.

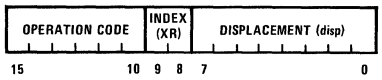


FIGURE 5. Memory Reference Instruction Format

When the XR field is 00, base page (page zero) addressing is used. Two different types of base page addressing are available and may be selected by the base-page-select (BPS) signal input. If BPS = 0, the 16-bit memory address is formed by setting bits 8 through 15 to zero, and using the 8-bit displacement (disp) for bits 0 through 7; this permits addressing of the first 256 words of memory (locations 0–255). If BPS = 1, the 16-bit memory address is formed by setting bits 8 through 15 equal to bit 7 of disp and using disp for bits 0 through 7; this permits addressing the first 128 words (0 through $7F_{16}$) and the last 128 words ($FF80_{16}$ through $FFFF_{16}$) of memory. The latter technique is useful for splitting the base page between read-write and read-only memories or between memory and peripheral devices, so the convenience of base page addressing is available for accessing data or peripherals.

Addressing relative to the program counter (PC) is specified when the XR field is 01. With this mode, the memory address is formed by adding the contents of the program counter to the value of the displacement field interpreted as a signed two's complement number (that is, the 8-bit disp field is interpreted as a 16-bit value with bits 8 through 15 set equal to bit 7; this allows representation of numbers from −128 through +127). When the address is formed, the program counter has already been incremented and contains a value one greater than the location of the current instruction; thus, memory addresses that may be referenced as 127 locations below through 128 above the address of the current instruction.

With the index register relative mode of addressing, any memory location within the 65,536 word address space may be referenced. The disp field is interpreted as a signed value ranging from −128 through 127 as with PC relative addressing. The memory address is formed by adding disp to the contents of either accumulator AC2 (when XR = 10) or accumulator AC3 (when XR = 11).

This type of addressing is very desirable for microprocessor applications which require address computation at execution time, since the use of read-only-memory for program storage prevents address modification within the program storage memory. A summary of the direct addressing modes is presented in Table IV.

TABLE IV. Summary of Addressing Modes

XR Field	Addressing Mode	Effective Address
00	Base Page	EA = disp
01	Program Counter Relative	EA = disp + (PC)
10	AC2 Relative (indexed)	EA = disp + (AC2)
11	AC3 Relative (indexed)	EA = disp + (AC3)

Note 1: For base page addressing, disp is positive and in the range of 000 to 255 if BPS = 0, and is a signed number in the range of −128 to +127 if BPS = 1.
Note 2: For relative addressing, disp has a range of −128 to +127.

Indirect addressing consists of first establishing an address in the same fashion as with direct addressing [by either the base page, relative to PC, or indexed (relative to AC2 or AC3) mode]. The 16-bit contents of the memory location at this address is then used as the address of the operand, allowing any memory location to be addressed.

As noted previously, the memory addressing modes are also used for peripheral I/O operations. The address space must be divided between read-write memory, read-only memory and I/O devices.

Instruction Summary

The instruction set is divided into eight instruction classes as listed in Table V. The branch instructions provide the means to transfer control anywhere in the 16-bit addressing space. Conditional branches are effected using the BOC instruction, which allows testing any one of 16 conditions, including status flags, the contents of AC0, and user inputs to the chip. Additional testing capability is provided by the skip instructions, which provide memory or peripheral to register comparisons

TABLE V. PACE Instruction Summary

Mnemonic	Meaning	Operation	Assembler Format		Instruction Format
1. Branch Instructions					
BOC	Branch On Condition	(PC) ← (PC) + disp if cc true	BOC	cc,disp	0 1 0 0 | cc | disp
JMP	Jump	(PC) ← EA	JMP	disp (xr)	0 0 0 1 1 0 | xr | disp
JMP@	Jump Indirect	(PC) ← (EA)	JMP	@disp (xr)	1 0 0 1 1 0
JSR	Jump To Subroutine	(STK) ← (PC), (PC) ← EA	JSR	disp (xr)	0 0 0 1 0 1
JSR@	Jump To Subroutine Indirect	(STK) ← (PC), (PC) ← (EA)	JSR	@disp (xr)	1 0 0 1 0 1
RTS	Return from Subroutine	(PC) ← (STK) + disp	RTS	disp	1 0 0 0 0 0 0 0 | disp
RTI	Return from Interrupt	(PC) ← (STK) + disp, IEN = 1	RTI	disp	0 1 1 1 1 1
2. Skip Instructions					
SKNE	Skip if Not Equal	If (ACr) ≠ (EA), (PC) ← (PC) + 1	SKNE	r,disp (xr)	1 1 1 1 | r | xr | disp
SKG	Skip if Greater	If (AC0) > (EA), (PC) ← (PC) + 1	SKG	0,disp (xr)	1 0 0 1 1 1
SKAZ	Skip if And is Zero	If [(AC0) ∧ (EA)] = 0, (PC) ← (PC) + 1	SKAZ	0,disp (xr)	1 0 1 1 1 0
ISZ	Increment and Skip if Zero	(EA) ← (EA) + 1, if (EA) = 0, (PC) ← (PC) + 1	ISZ	disp (xr)	1 0 0 0 1 1
DSZ	Decrement and Skip if Zero	(EA) ← (EA) − 1, if (EA) = 0, (PC) ← (PC) + 1	DSZ	disp (xr)	1 0 1 0 1 1
AISZ	Add Immediate, Skip if Zero	(ACr) ← (ACr) + disp, if (ACr) = 0, (PC) ← (PC) + 1	AISZ	r,disp	0 1 1 1 1 0 | r
3. Memory Data Transfer Instructions					
LD	Load	(ACr) ← (EA)	LD	r,disp (xr)	1 1 0 0 | r | xr | disp
LD@	Load Indirect	(AC0) ← ((EA))	LD	0,@disp (xr)	1 0 1 0 0 0
ST	Store	(EA) ← (ACr)	ST	r,disp (xr)	1 1 0 1 | r
ST@	Store Indirect	((EA)) ← (AC0)	ST	0,@disp (xr)	1 0 1 1 0 0
LSEX	Load With Sign Extended	(AC0) ← (EA) bit 7 extended	LSEX	0,disp (xr)	1 0 1 1 1 1
4. Memory Data Operate Instructions					
AND	And	(AC0) ← (AC0) ∧ (EA)	AND	0,disp (xr)	1 0 1 0 1 0 | xr | disp
OR	Or	(AC0) ← (AC0) ∨ (EA)	OR	0,disp (xr)	1 0 1 0 0 1
ADD	Add	(ACr) ← (ACr) + (EA), OV, CY	ADD	r,disp (xr)	1 1 1 0 | r
SUBB	Subtract with Borrow	(AC0) ← (AC0) + ~ (EA) + (CY), OV, CY	SUBB	0,disp (xr)	1 0 0 1 0 0
DECA	Decimal Add	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY	DECA	0,disp (xr)	1 0 0 0 1 0
5. Register Data Transfer Instructions					
LI	Load Immediate	(ACr) ← disp	LI	r,disp	0 1 0 1 0 0 | r | disp
RCPY	Register Copy	(ACdr) ← (ACsr)	RCPY	sr,dr	0 1 0 1 1 1 | dr | sr | not used
RXCH	Register Exchange	(ACdr) ← (ACsr), (ACsr) ← (ACdr)	RXCH	sr,dr	0 1 1 0 1 1
XCHRS	Exchange Register and Stack	(STK) ← (ACr), (ACr) ← (STK)	XCHRS	r	0 0 0 1 1 1 | r | not used
CFR	Copy Flags Into Register	(ACr) ← (FR)	CFR	r	0 0 0 0 0 1
CRF	Copy Register Into Flags	(FR) ← (ACr)	CRF	r	0 0 0 0 1 0
PUSH	Push Register Onto Stack	(STK) ← (ACr)	PUSH	r	0 1 1 0 0 0
PULL	Pull Stack Into Register	(ACr) ← (STK)	PULL	r	0 1 1 0 0 1
PUSHF	Push Flags Onto Stack	(STK) ← (FR)	PUSHF		0 0 0 0 1 1 | not used
PULLF	Pull Stack Into Flags	(FR) ← (STK)	PULLF		0 0 0 1 0 0
6. Register Data Operate Instructions					
RADD	Register Add	(ACdr) ← (ACdr) + (ACsr), OV, CY	RADD	sr,dr	0 1 1 0 1 0 | dr | sr | not used
RADC	Register Add With Carry	(ACdr) ← (ACdr) + (ACsr) + (CY), OV, CY	RADC	sr,dr	0 1 1 1 0 1
RAND	Register And	(ACdr) ← (ACdr) ∧ (ACsr)	RAND	sr,dr	0 1 0 1 0 1
RXOR	Register Exclusive OR	(ACdr) ← (ACdr) ∀ (ACsr)	RXOR	sr,dr	0 1 0 1 1 0
CAI	Complement and Add Immediate	(ACr) ← ~ (ACr) + disp	CAI	r,disp	0 1 1 1 0 0 | r | disp
7. Shift And Rotate Instructions					
SHL	Shift Left	(ACr) ← (ACr) shifted left n places, w/wo link	SHL	r,n,ℓ	0 0 1 0 1 0 | r | n | ℓ
SHR	Shift Right	(ACr) ← (ACr) shifted right n places, w/wo link	SHR	r,n,ℓ	0 0 1 0 1 1
ROL	Rotate Left	(ACr) ← (ACr) rotated left n places, w/wo link	ROL	r,n,ℓ	0 0 1 0 0 0
ROR	Rotate Right	(ACr) ← (ACr) rotated right n places, w/wo link	ROR	r,n,ℓ	0 0 1 0 0 1
8. Miscellaneous Instructions					
HALT	Halt	Halt	HALT		0 0 0 0 0 0 | not used
SFLG	Set Flag	$(FR)_{fc}$ ← 1	SFLG	fc	0 0 1 1 | fc | 1 | not used
PFLG	Pulse Flag	$(FR)_{fc}$ ← 1, $(FR)_{fc}$ ← 0	PFLG	fc	0 0 1 1 | fc | 0

without altering data. The memory data transfer instructions provide data transfers between the accumulators and memory or peripheral devices. The load with sign extended is provided to convert 8-bit, two's complement data to 16-bit data, allowing 16-bit address modification when the 8-bit data length has been selected.

The memory data operate instructions provide operations between the principal working register (AC0) and memory or peripheral data. This includes both binary and BCD arithmetic instructions. The register data transfer instructions provide a very complete set of transfer possibilities between the accumulators, flag register and stack, and include the capability to load immediate data. Register data operate instructions provide logical and arithmetic operations between any two accumulators. They may be used for address and data modification and to reduce the number of (time consuming) memory references in a program. The shift and rotate instructions allow 8 different operations which are useful for multiply, divide, bit scanning and serial input-output operations. The miscellaneous instructions include the capability to set or reset (pulse) any of the 16 bits of the status flag register individually. Instruction execution times are shown in Table VI.

A simple example program is provided by the binary multiply routine shown on page 9. This program multiplies the 16-bit value in AC2 by the 16-bit value in AC0 and provides a 32-bit result in AC0 (high order) and AC1 (low order). Worst case execution time is under one millisecond.

Binary Multiply Routine

```
CONST:  .WORD  X'FFFF      ; CONSTANT FOR DOUBLE PREC. ADD
START:  LI     R1, 0       ; CLEAR RESULT REGISTER
        LI     R3, 16      ; LOOP COUNT TO AC3
        CAI    R0, 0       ; COMPLEMENT MULTIPLIER
LOOP:   RADD   R1, R1      ; SHIFT RESULT LEFT INTO CARRY
        RADC   R0,R0       ; SHIFT CARRY INTO MULTIPLIER
                           ; AND MULTIPLIER INTO CARRY
        BOC CARRY, TEST    ; TEST FOR ADD
        RADD   R2, R1      ; ADD MULTIPLICAND TO RESULT
        SUBB   R0, CONST   ; ADD CARRY TO H.O. RESULT
TEST:   AISZ   R3, -1      ; DECREMENT LOOP COUNT
        JMP LOOP           ; REPEAT LOOP
```

TABLE VI. Instruction Execution Times

Mnemonic	Meaning	Execution Time
1. Branch Instructions		
BOC	Branch On Condition	$5M + E_R + 1M$ if branch
JMP	Jump	$4M + E_R$
JMP@	Jump Indirect	$4M + 2E_R$
JSR	Jump To Subroutine	$5M + E_R$
JSR@	Jump To Subroutine Indirect	$5M + 2E_R$
RTS	Return from Subroutine	$5M + E_R$
RTI	Return from Interrupt	$6M + E_R$
2. Skip Instructions		
SKNE	Skip if Not Equal	$5M + 2E_R + 1M$ if skip
SKG	Skip if Greater	$7M + 2E_R + 1M$ if skip
SKAZ	Skip if And is Zero	$5M + 2E_R + 1M$ if skip
ISZ	Increment and Skip if Zero	$7M + 2E_R + E_W + 1M$ if skip
DSZ	Decrement and Skip if Zero	$7M + 2E_R + E_W + 1M$ if skip
AISZ	Add Immediate, Skip if Zero	$5M + E_R + 1M$ if skip
3. Memory Data Transfer Instructions		
LD	Load	$4M + 2E_R$
LD@	Load Indirect	$5M + 3E_R$
ST	Store	$4M + E_R + E_W$
ST@	Store Indirect	$4M + 2E_R + E_W$
LSEX	Load With Sign Extended	$4M + 2E_R$
4. Memory Data Operate Instructions		
AND	And	$4M + 2E_R$
OR	Or	$4M + 2E_R$
ADD	Add	$4M + 2E_R$
SUBB	Subtract With Borrow	$4M + 2E_R$
DECA	Decimal Add	$7M + 2E_R$
5. Register Data Transfer Instructions		
LI	Load Immediate	$4M + E_R$
RCPY	Register Copy	$4M + E_R$
RXCH	Register Exchange	$6M + E_R$
XCHRS	Exchange Register and Stack	$6M + E_R$
CFR	Copy Flags Into Register	$4M + E_R$
CRF	Copy Register Into Flags	$4M + E_R$
PUSH	Push Register Onto Stack	$4M + E_R$
PULL	Pull Stack Into Register	$4M + E_R$
PUSHF	Push Flags Onto Stack	$4M + E_R$
PULLF	Pull Stack Into Flags	$4M + E_R$
6. Register Data Operate Instructions		
RADD	Register Add	$4M + E_R$
RADC	Register Add With Carry	$4M + E_R$
RAND	Register And	$4M + E_R$
RXOR	Register Exclusive Or	$4M + E_R$
CAI	Complement and Add Immediate	$5M + E_R$
7. Shift And Rotate Instructions		
SHL	Shift Left	$(5 + 3n)\ M + E_R$, n = 1 – 127;
SHR	Shift Right	
ROL	Rotate Left	$6M + E_R$, n = 0
ROR	Rotate Right	
8. Miscellaneous Instructions		
HALT	Halt	
SFLG	Set Flag	$5M + E_R$
PFLG	Pulse Flag	$6M + E_R$

M = Machine cycle time = 4 clock periods
n = number of shifts
E_R = Extend time for read cycle
E_W = Extend time for write cycle
Note: External interrupt response time is $7M + E_R$ plus time to finish current instruction.

While the instruction set is compact at 45 instruction types (or 337 individual instructions), it is powerful enough to allow considerably more efficient program coding than most microprocessors and compares favorably with many minicomputers.

I/O DESCRIPTION

Drivers and Receivers

Equivalent circuits for PACE drivers and receivers are shown in *Figure 6*. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp. These devices should still be handled with care, as the protection circuits can be destroyed by excessive static charge. Pullup transistors on several inputs are turned on during one of the eight internal clock phases. In the case of bidirectional signals, the output driver transistors also serve as input pullup transistors.

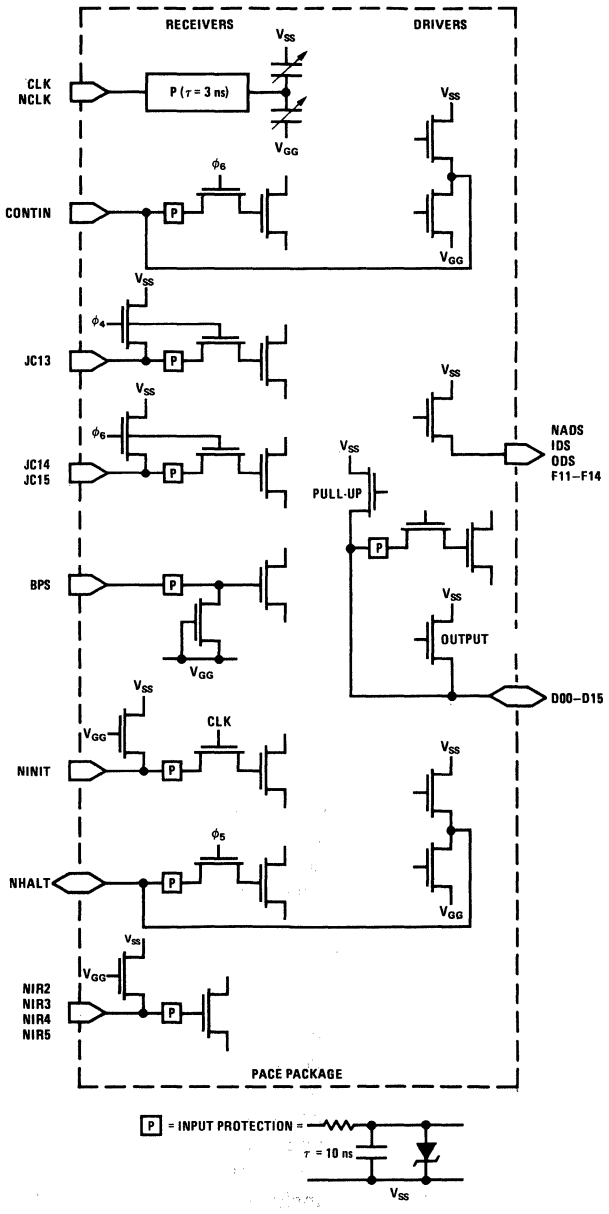


FIGURE 6. PACE Driver and Receiver Equivalent Circuits

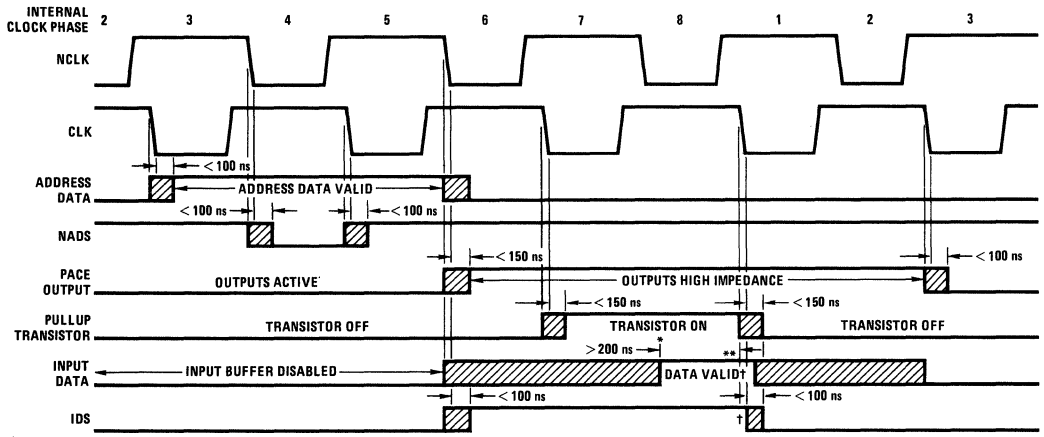
Data I/O Timing

All data transfers between PACE and external memories or peripheral devices take place over the 16 data lines. These transfers are synchronized by the NADS, IDS, ODS and EXTEND signals. Timing for address data output is shown in *Figure 7.* All signal timing is referenced to valid logic "1" or logic "0" clock levels. Cross-hatched areas indicate uncertainty of output transitions or "don't care" (optional) states for data inputs. Address data becomes valid one clock phase prior to the Address Data Strobe and remains valid for one clock phase afterwards. Typically, NADS will be used to strobe the address data into a latch, either internal or external to the memory chips, or to clock decoded peripheral addresses into a flip-flop.

The PACE address output drivers assume a high impedance state during the data input interval as shown in *Figure 7.* The IDS signal may be used to disable the output sense amplifiers and enable TRI-STATE® input buffers. Increased power supply current may occur during the transition period of the TRI-STATE enable signal, when several devices may be simultaneously enabled. Therefore, good power and ground layout and bypass filtering practice should be observed. The data lines must be driven to valid input data logic levels by the end of IDS, and all logic 1 inputs must reach a minimum intermediate level of V_{SS} − 2.35V 200 ns prior to the end of internal clock phase 8. TTL devices will actively drive the input to this minimum intermediate level and the transition will be completed by a combination of the on-chip pullup transistor and the (reduced) TTL output drive current. Typically, this data input timing will allow operation of the microprocessor in a system at maximum speed if the access time of the system memory is less than 700 ns. For memories with longer access times the clock frequency may be reduced or the I/O cycle extend feature may be used, as described below.

Data output timing is shown in *Figure 8.* Output data becomes valid at the leading edge of ODS and remains valid for one clock period following the trailing edge.

The Output Data Strobe is typically used as a read-write signal for memory and an output data latch strobe for peripheral interfaces.



Note: Signals are referenced to valid logic levels on clock inputs. All times in Figures 7 – 10 are typical maximums or minimums. Internal clock phases are shown for reference only, they are not available externally.

*V_{IN} must be > V_{SS} – 2.35V at this time if logic "1" input.

**V_{IN} must be valid level (i.e., V_{SS} – 1) at this time (this timing allows for pull-up transistor time constant).

†Data must be valid until trailing edge of IDS (i.e., data hold time = 0 ns).

FIGURE 7. Address Output and Data Input Timing

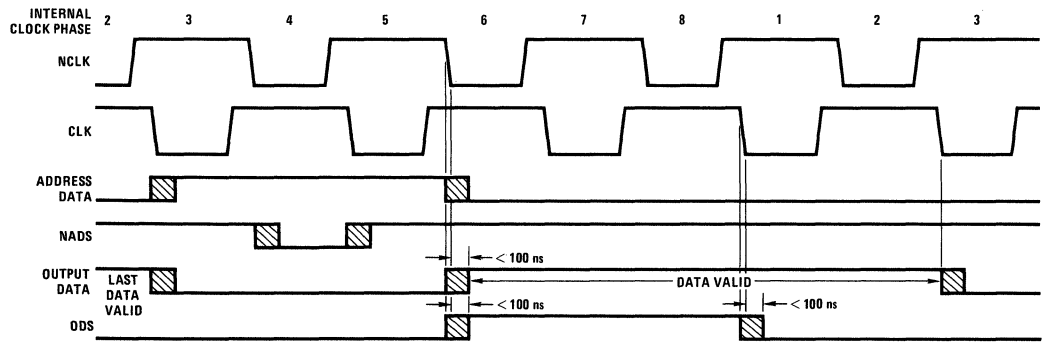


FIGURE 8. Data Output Timing

For systems utilizing memories with access times greater than 700 ns it may be desirable to use the EXTEND input to lengthen the I/O cycle by multiples of the clock period. Timing for this is shown in *Figure 9*. In the case of either input or output operations, the extend should be brought true prior to the end of internal phase 6. The timing shown in *Figure 9* will provide the minimum extend of one clock period. Holding EXTEND true for and additional n clock periods longer will cause an extention of n + 1 clock periods. As indicated in the electrical characteristics, no single extend cycle should exceed t_{EX}. This includes the use of EXTEND for both extending and suspending I/O operations.

In DMA or multiprocessor systems it may be desirable to prevent I/O operations by PACE when the bus is in use by another device. This may be done by using the EXTEND signal immediately following an IDS or ODS as shown in *Figure 10*. Alternatively, the extend timing of *Figure 9* may be used, as the extend function occurs independent of whether there is an I/O operation, that is, whenever the internal clock phase 6 occurs.

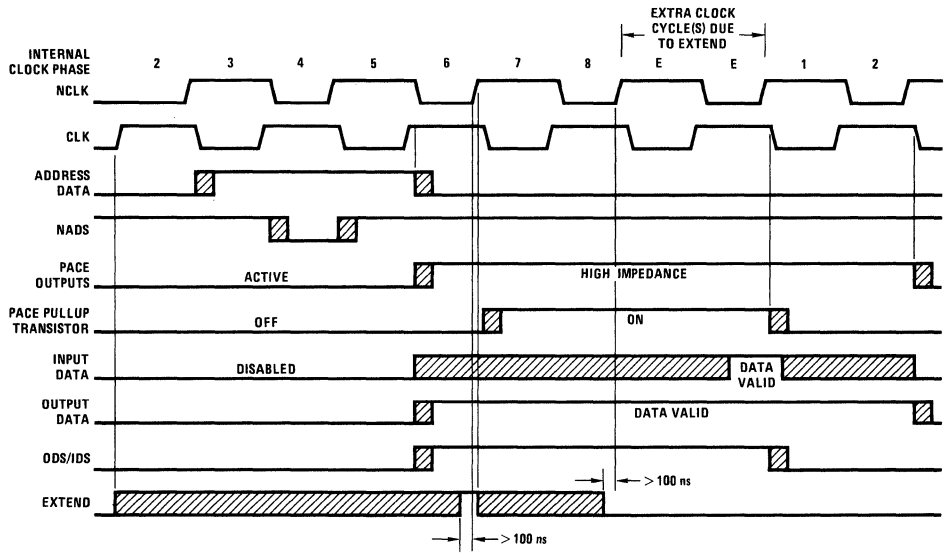


FIGURE 9. Extend I/O Signal Timing

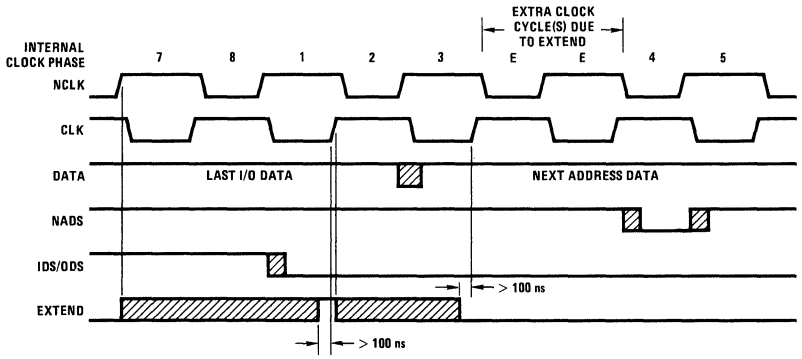
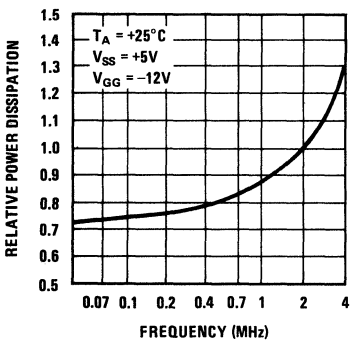


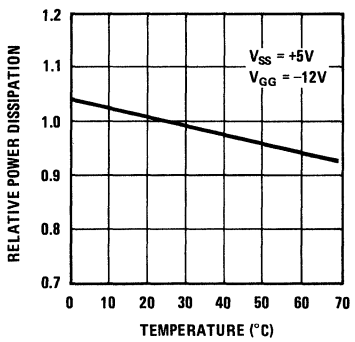
FIGURE 10. Suspend I/O Signal Timing

typical performance characteristics

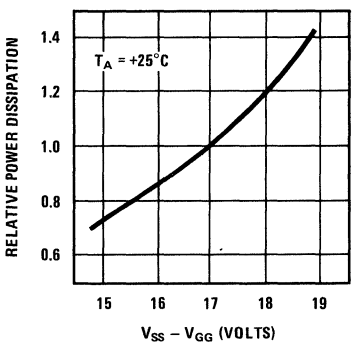
Power Dissipation vs Clock Frequency



Power Dissipation vs Temperature



Power Dissipation vs Supply Voltage



PRELIMINARY DATA: JUNE 1975

NATIONAL

IPC-16A/501J PACE bidirectional transceiver element (PACE BTE/8)

general description

The PACE BTE/8 is an 8-bit TRI-STATE® MOS/TTL bus transceiver Blue Chip element specifically intended for application in PACE microprocessor-based systems. Its electrical characteristics and control flexibility make the BTE/8 attractive in other applications requiring the translation of MOS current outputs to high fan-out TTL levels.

Two BTE/8 devices provide complete system buffering for all 16-bit address and data input/output between the PACE CPU and all system memory and peripheral interfaces.

In the driving mode, the MOS sense amplifiers convert the MOS current outputs of the PACE CPU to a fan-out 30 (50 mA) TTL system bus.[This characteristic makes the BTE/8 an ideal buffer (driving mode only) for the PACE system timing and control bus consisting of the address data strobe (NADS), input data strobe (IDS), output data strobe (ODS) and the four output control flags (F11, F12, F13, F14).]

In the receiving mode the BTE accepts bus data through high impedance input buffers and applies the TTL signals to the PACE I/O pins.

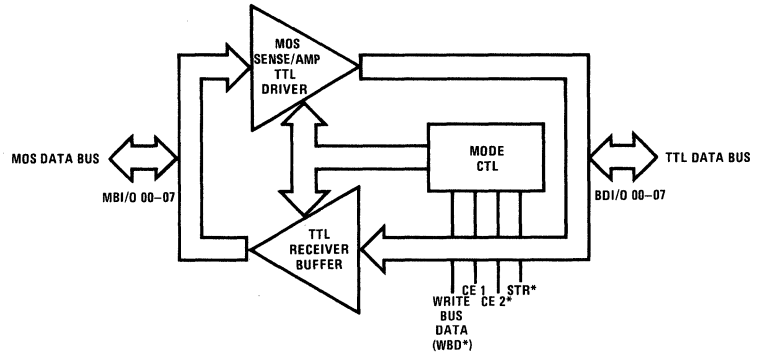
A third mode allows both the MOS and TTL bus to be placed in the TRI-STATE (high impedance) mode. This function facilitates direct memory access (DMA) over the TTL system bus. Furthermore system memory or peripheral data may be accepted directly onto the CPU's MOS bus eliminating output data buffers for on card MOS system memory and MOS peripheral circuits.

A latched chip enable allows the use of multiplexed address/data lines to drive CE and CE*, selecting the BTE/8 for an input cycle. The latching function may be eliminated by connecting the strobe to ground.

features

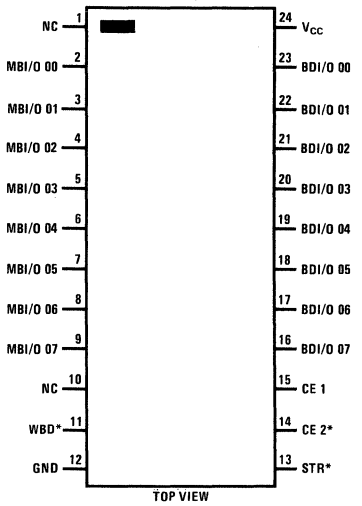
- High TTL fan-out eliminates additional buffering requirements
- Low system data bus loading for minimum input drive
- TRI-STATE data ports and chip enables maximize application flexibility
- 8-Bit parallel data flow reduces system package count
- Pin-outs simplify system interconnections and layout
- Latched chip enable simplifies transmit/receive control

block and connection diagrams



Signal* ≡ N Signal ≡ $\overline{\text{Signal}}$ ≡ Low Active Signal

Dual-In-Line Package



TOP VIEW

IPC-16A/501J (PACE BTE/8)
See Package 3

truth table

t_n			$t_n + 1$	
CE 1	CE 2*	STR*	WBD*	TRANSCEIVER MODE
X	X	X	0	Receiving MOS Bus and Driving TTL Bus
X	X	1	1	Mode t_n: See Note 1
0	0	0	1	TRI-STATE Mode
0	1	0	1	TRI-STATE Mode
1	0	0	1	Receiving TTL Bus and Driving MOS Bus
1	1	0	1	TRI-STATE Mode

Note 1: Latched chip enable is not cleared and transceiver will either be in the TRI-STATE or receiving mode, depending on the previous state of the latched chip enable.

Printed in U.S.A.

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
MOS Bus Input Current	±25 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage	4.75	5.25	V
Temperature	0	+70	°C

dc electrical characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SPECIFICATIONS						
TTL BUS PORT (BDI/O 00–07)						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OH} = −5.0 mA	2.6	3.0		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OL} = 50 mA		0.25	0.4	V
I_{LH}	TRI-STATE Output Current	V_{CC} = Max, WBD* = CE 2* = 1, V_{OUT} = 2.4V			10	μA
I_{LL}		CE 1 = STR* = 0, V_{OUT} = 0.3V			−10	μA
I_{SO}	Output Short Circuit Current	V_{CC} = Max, V_{SO} = 0V, (Note 3)	−20	−50	−90	mA
MOS BUS PORT (MBI/O 00–07)						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OH} = −1.0 mA	2.4	2.8		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OL} = 3.6 mA		0.25	0.4	V
I_{OUT}	TRI-STATE Output Current	V_{CC} = Max, WBD* = CE 2* = 1, V_{OUT} = 2.4V			10	μA
		CE 1 = STR* = 0, V_{OUT} = 0.3V			−10	μA
I_{SO}	Output Short Circuit Current	V_{CC} = Max, V_{SO} = 0V, (Note 3)	−3.0		−15	mA
INPUT SPECIFICATIONS						
TTL BUS PORT (BDI/O 00–07)						
V_{IH}	Logic "1" Input Voltage		2.0			V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IH} = 2.4V		5	10	μA
V_{IL}	Logic "0" Input Voltage				0.7	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.3V		−100	−185	μA
I_{LH}	TRI-STATE Input Current	V_{CC} = Max, WBD* = CE 2* = 1, V_{IN} = 2.4V			10	μA
		CE = 1 = STR* = 0, V_{IN} = 0.3V			−10	μA
INPUT CLAMP VOLTAGE		V_{CC} = Min, I_{IN} = −12 mA		−1.0	−1.5	V
MOS BUS PORT (MBI/O 00–07)						
I_{TH}	Input Threshold Current		450	600	800	μA
I_{IH}	Maximum Input Current	V_{IN} = Max			8	mA
I_{LH}	TRI-STATE Input Current	V_{CC} = Max, WBD* = CE 2* = 1, V_{IN} = 5.0V			40	μA
I_{LL}		CE 1 = STR* = 0, V_{IN} = 0.3V			−40	μA
CONTROL BUS (WBD*, CE 1, CE 2*, STR*)						
V_{IH}	Logic "1" Input Voltage	V_{CC} = Min	2.0			V
I_{IH}	Logic "1" Input Current (WBD*)	V_{IH} = 2.4V		20	80	μA
	(CE 1, CE 2*, STR*)			10	40	μA
V_{IL}	Logic "0" Input Voltage	V_{CC} = Min			0.8	V
I_{IL}	Logic "0" Input Current (WBD*)	V_{IL} = 0.4V			−32	mA
	(CE 1, CE 2*, STR*)				−16	mA
SUPPLY CURRENT		V_{CC} = Max		180	285	mA

ac electrical characteristics (V_{CC} = 5.0V, T_A = +25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DATA TRANSFER SPECIFICATIONS						
RECEIVING MODE (t_{pd} BDI/O 00–07 to MBI/O 00–07)						
t_{pd}	Delay to Logic "0"	C_L = 50 pF		35	75	ns
t_{pd}	Delay to Logic "1"	C_L = 50 pF		30	60	ns
DRIVING MODE (t_{pd} MBI/O 00–07 to BDI/O 00–07)						
t_{pd}	Delay to Logic "0"	C_L = 50 pF		15	25	ns
t_{pd}	Delay to Logic "1"	C_L = 50 pF		15	25	ns

ac electrical characteristics (con't)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TRANSCEIVER MODE SPECIFICATIONS (See timing diagrams)						
SELECT BUS (CE 1, CE 2*)						
t_{DS}	Chip Enable Data Set-Up			20	45	ns
t_{DH}	Chip Enable Data Hold				0	ns
t_{ES}	Chip Enable Set-Up			5	15	ns
TTL DATA BUS (BDI/O 00–07)						
$t_{BD\,OD}$	Bus Data Output Disable		10	40	70	ns
$t_{BD\,IE}$	Bus Data Input Enable			70	120	ns
$t_{BD\,ID}$	Bus Data Input Disable		20	65		ns
$t_{BD\,OE}$	Bus Data Output Enable			70	135	ns
MOS DATA BUS (MBI/O 00–07)						
$t_{MB\,ID}$	MOS Bus Input Disable		10	40	70	ns
$t_{MB\,OE}$	MOS Bus Output Enable			70	120	ns
$t_{MB\,OD}$	MOS Bus Output Disable		20	65		ns
$t_{MB\,IE}$	MOS Bus Input Enable			65	90	ns
TRI-STATE MODE SPECIFICATIONS (See timing diagrams)						
SELECT BUS (CE1, CE2*)						
t_{CLR}	Clear Previous Chip Enable			30	50	ns
TTL DATA BUS (BDI/O 00–07)						
$t_{BD\,OD}$	Bus Data Output Disable		10	40	70	ns
$t_{BD\,OR}$	Bus Data Output Recovery			30	60	ns
MOS DATA BUS (MBI/O 00–07)						
$t_{MB\,ID}$	MOS Bus Input Disable		10	40	70	ns
$t_{MB\,IR}$	MOS Bus Input Recovery			30	60	ns

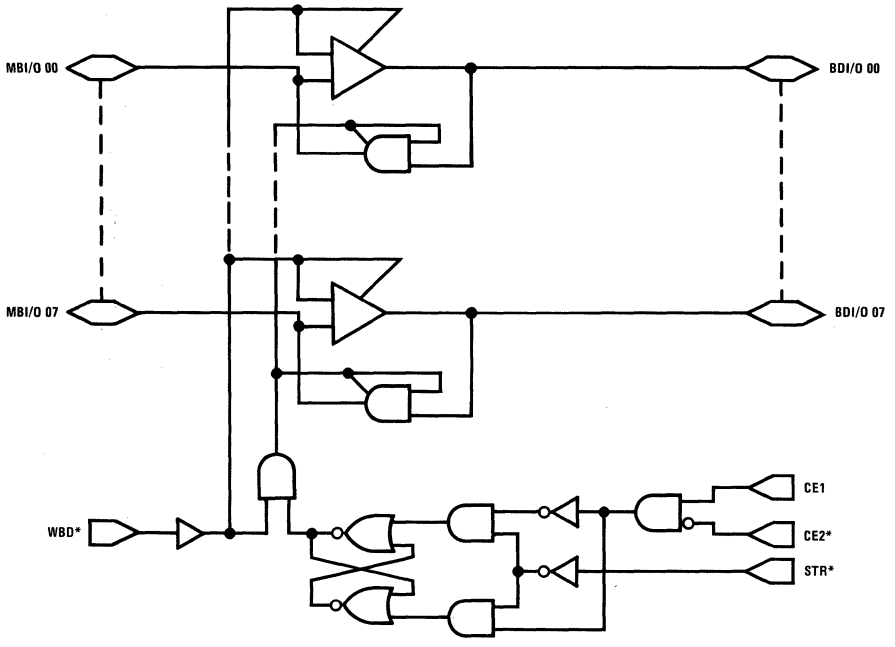
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

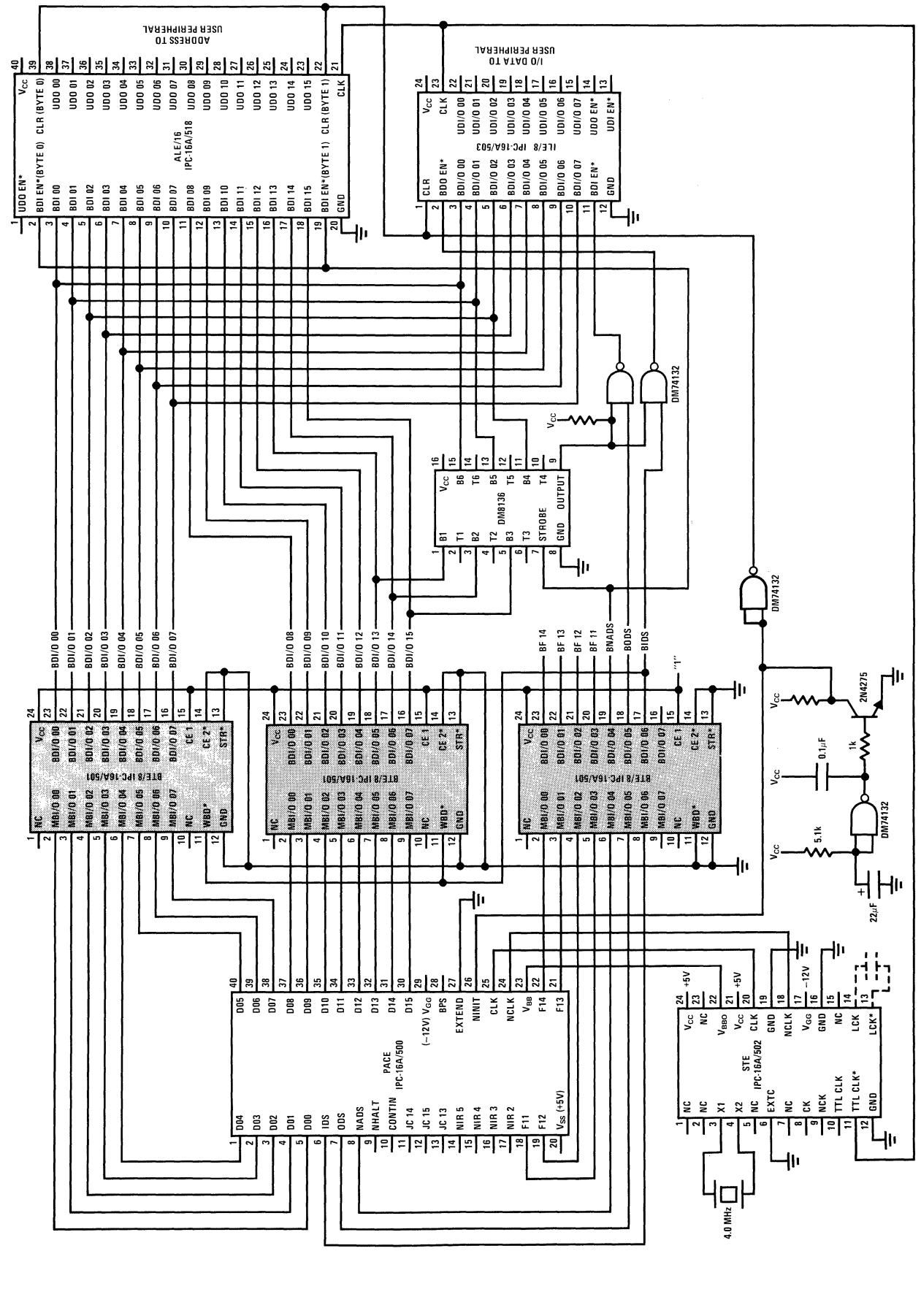
Note 3: Only one output at a time should be shorted.

Note 4: The MOS sense amplifier inputs to the BTE have been optimized for high speed and operate from a constant input reference voltage. Good design practice dictates isolating the sense amplifier inputs from other signal lines carrying high speed signals, particularly the MOS clocks.

logic diagram

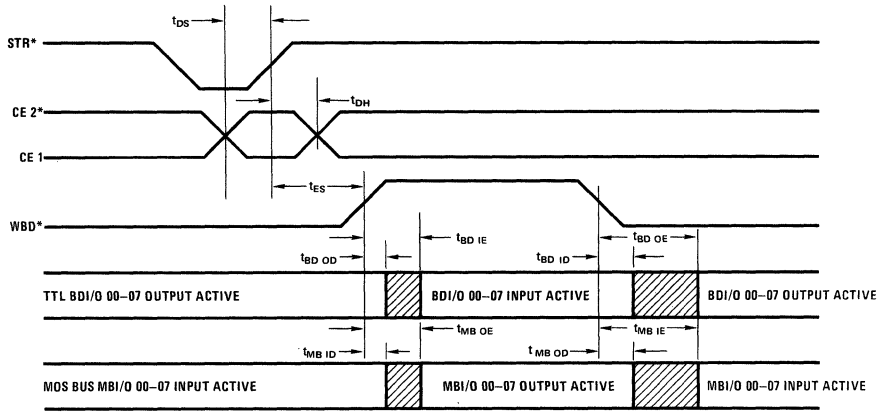


PACE system interconnection diagram

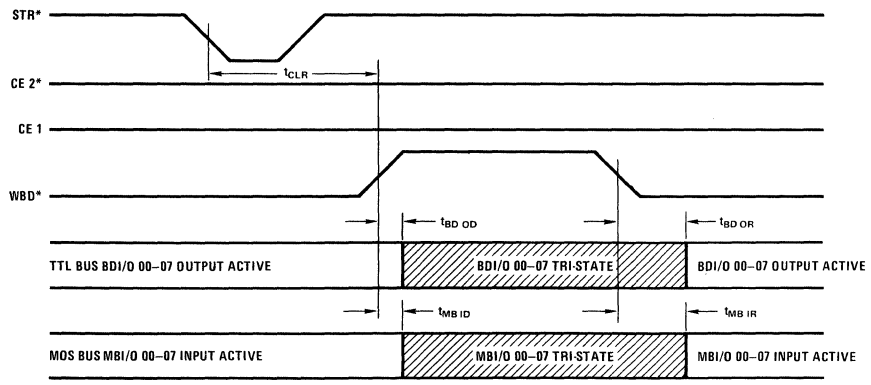


switching time waveforms

Transceiver Mode

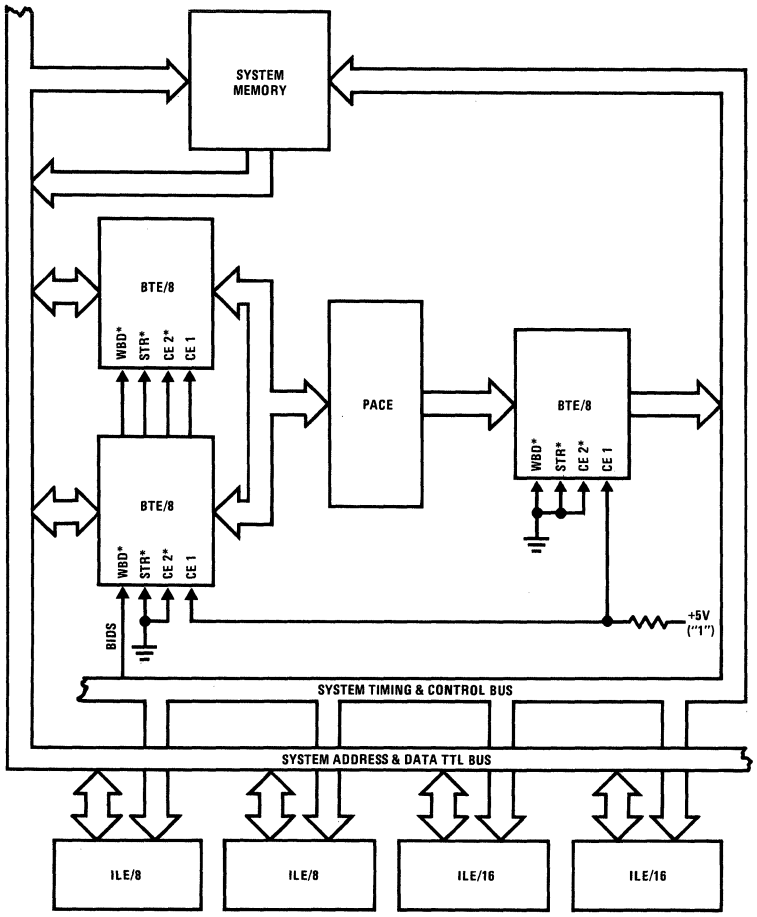


TRI-STATE Mode



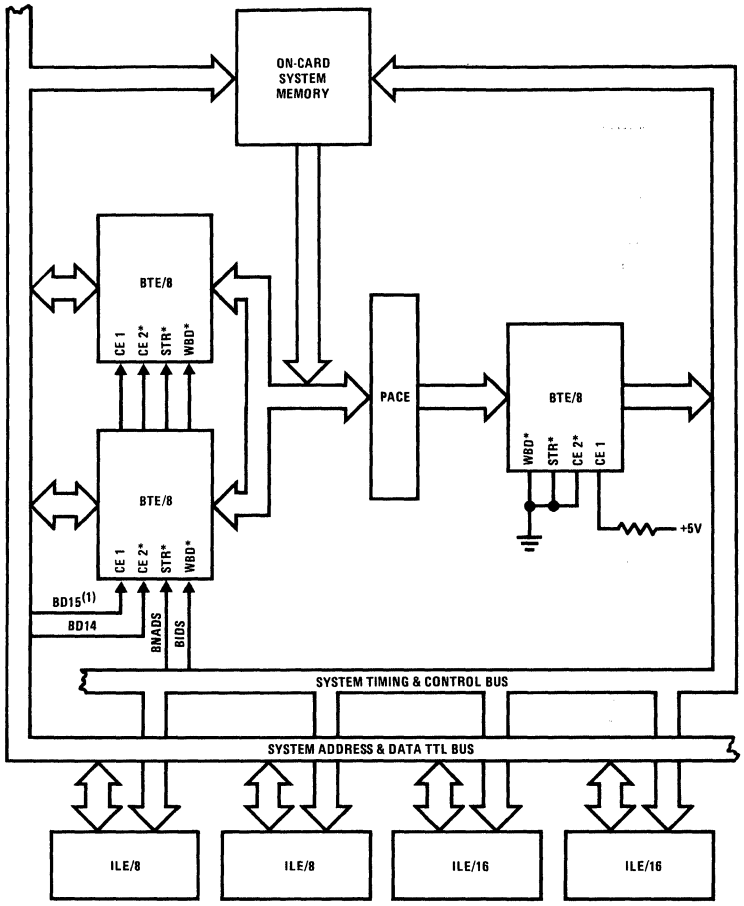
typical applications

Multiplexed TTL System Bus



typical applications (con't)

Multiplexed TTL & MOS Bus



(1)BD14, 15 ARBITRARILY CHOSEN TO DISABLE BTE WHEN MEMORY IS ACCESSED. USER MAY PICK ADDRESS SIGNALS SUITABLE TO HIS APPLICATION AND PROGRAM.

PRELIMINARY DATA: JUNE 1975

NATIONAL

IPC-16A/502J PACE system timing element (PACE STE)

general description

The PACE STE provides an oscillator, CPU clock driver, CPU bias voltage generator and TTL system clocks in a single 24-pin DIP. The STE, Blue Chip, is intended specifically for application in PACE microprocessor-based systems.

An external 4.0 MHz crystal provides frequency control, although an external TTL clock input may be utilized at any frequency up to 4.0 MHz. True and complemented non-overlapping clock outputs are generated at one-half the oscillator frequency. Non-overlap intervals may be controlled with a single external capacitor. Series damping resistors are provided on the MOS (CPU) clock outputs (CLK, NCLK).

TTL level system clock outputs are also provided to facilitate the synchronizing of system operations.

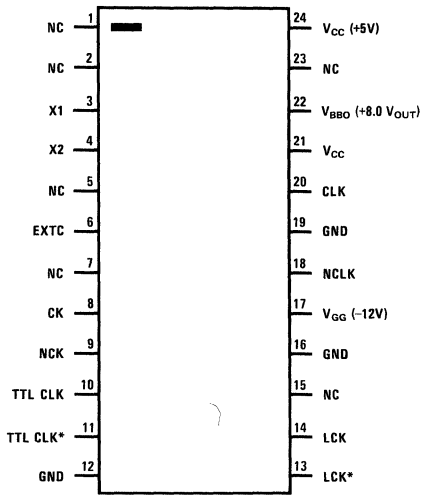
The bias voltage generator supplies a voltage and current level suitable for the V_{BB} supply requirements of the PACE CPU, permitting the entire PACE system to be operated with only +5V and −12V external power supply inputs.

features

- Internal oscillator driven directly from external crystal minimizing package count
- External oscillator input maximizes application flexibility
- MOS clock outputs, no external MOS clock drivers required
- TTL system clocks simplify interfaces and facilitate synchronization of system operations.

connection diagram

Dual-In-Line Package



TOP VIEW

IPC-16A/502J (PACE STE)
See Package 3

Signal* ≡ N Signal ≡ $\overline{\text{Signal}}$ ≡ Low Active Signal

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
$V_{CC}-V_{GG}$	22V
Input Voltage	5.5V
Peak Output Current (MOS)	1.5A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
(V_{GG})	11.4	12.6	V
Temperature	0	+70	°C

dc electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SPECIFICATIONS						
	$V_{BB\,OUT}$	V_{CC} = 5V, I_{OUT} = 30 μA, Freq = 4 MHz T_A = 25°C		8.0		V
TTL CLK, TTL CLK*						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OH} = −400 μA	2.4			V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.4	V
I_{OS}	Output Short Circuit Current	(Note 3), V_{CC} = Max, V_O = 0V	−20		−55	mA
CK, NCK, CLK, NCLK						
V_{OH}	Logical "1" Output Voltage	V_{CC} = 5V, V_{GG} = −12V	4.0	4.3		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = 5V, V_{GG} = −12V		−11.5	11	V
INPUT SPECIFICATIONS						
EXTC						
V_{IH}	Logic "1" Input Voltage		2.0			V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IH} = 2.4V			40	μA
V_{IL}	Logic "0" Input Voltage				0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V			−1.6	mA
INPUT CLAMP VOLTAGE (ALL)		V_{CC} = Min, I_{IL} = −12 mA, T_A = 25°C			−1.5	V
SUPPLY CURRENT						
I_{CC}		V_{CC} = Max, V_{GG} = Max			180	mA
I_{GG}		V_{CC} = Max, V_{GG} = Max			45	mA

ac electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TTL CLOCK LEADING EDGE TO MOS CLOCK LEADING EDGE						
t_{DH}	TTL CLK* to NCLK	C_L = 80 pF, f_{OSC} = 4.0 MHz		20		ns
t_{DL}	TTL CLK* to CLK	C_L = 80 pF, f_{OSC} = 4.0 MHz		42		ns
t_{DH}	TTL CLK to CLK	C_L = 80 pF, f_{OSC} = 4.0 MHz		20		ns
t_{DL}	TTL CLK to NCLK	C_L = 80 pF, f_{OSC} = 4.0 MHz		42		ns
t_{NOV}	Clock Non-Overlap	C_L = 80 pF, f_{OSC} = 4.0 MHz		12		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C temperature range. All typicals are given for V_{CC} = 5.0V, V_{GG} = −12V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

functional description

OSCILLATOR

The oscillator incorporates a low power inverter biased in the linear region utilizing an internal feedback network. An external crystal, series resonant at 4.0 MHz and capable of driving a 10 pF load, is connected between pins X1 and X2 to provide frequency control. EXTC must be grounded for this operating mode. The circuit board traces connecting the crystal to pins X1 and X2 should be as short as possible and physically isolated from all high energy level switching signal traces, particularly the CPU MOS clock lines. Note: While other frequencies may be used, the oscillator feedback network and capacitive loading are optimized for 4.0 MHz operation.

When an external oscillator is to be used in place of the internal crystal oscillator, pin X1 must be grounded and pin X2 must be left open. Then, EXTC may be used as a TTL input for the external oscillator.

DIVIDE AND SQUARING CIRCUIT

A flip-flop is used to provide a square wave clock signal by dividing the buffered oscillator output by two. The outputs of this circuit are buffered to provide TTL system clock signals which lead the MOS level clock outputs.

NON-OVERLAP CIRCUIT

The Divider output drives a cross coupled latch containing a delay in the feedback path which insures non-overlapping MOS clock signals. The delay in the feedback path can be increased by connecting a capacitor between pins LCK and LCK*. The effect of the capacitor on increasing the non-overlap interval is shown in the Typical Characteristics section.

Internal capacitors are used to level shift the output of the non-overlap circuit, providing voltage levels at the input of the MOS clock driver. Note: The value of the level shifting capacitor is optimized for 4.0 MHz operation. Use of a lower frequency external oscillator will result in an increase in the non-overlap interval, but will provide an acceptable clock waveform to the PACE CPU.

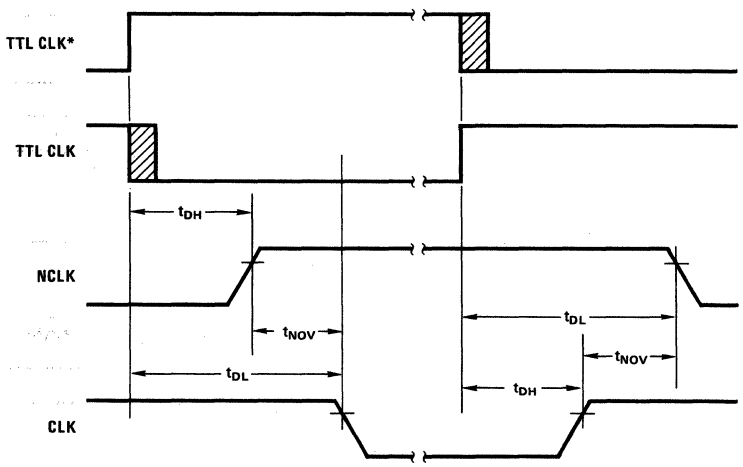
MOS CLOCK DRIVER

The MOS Clock Driver produces output voltage swings from the +5V supply to the −12V supply. CLK and NCLK outputs contain a 43Ω series damping resistor, a typically optimum value for circuit board layouts with clock interconnect lines of less than two inches. The damped clock outputs are adjacent to and separated by power and ground pins so that power traces may be used to shield clock traces from each other and from other signals. Note: These shields should be used for MOS clock interconnects exceeding one inch in order to minimize inductive and capacitive coupling.

Undamped MOS clock outputs, CK and NCK, are also available in the event other values of series damping resistors are desired.

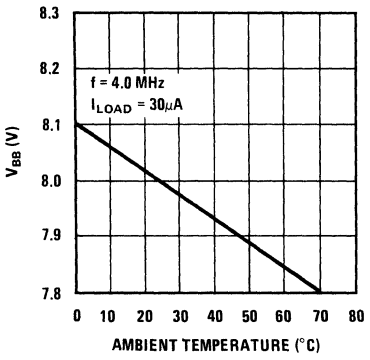
It is recommended that 0.1μF high frequency capacitors be provided from V_{CC} to ground and V_{GG} to ground immediately adjacent to the STE.

timing diagram

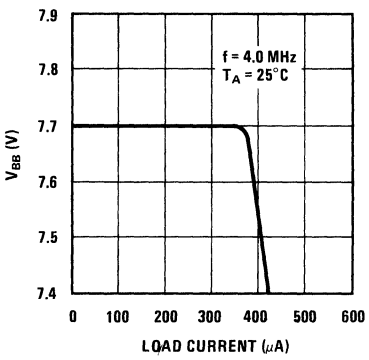


typical performance characteristics

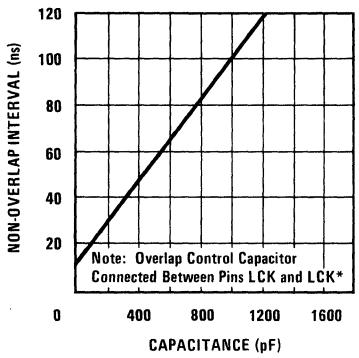
V_{BB} vs Ambient Temperature



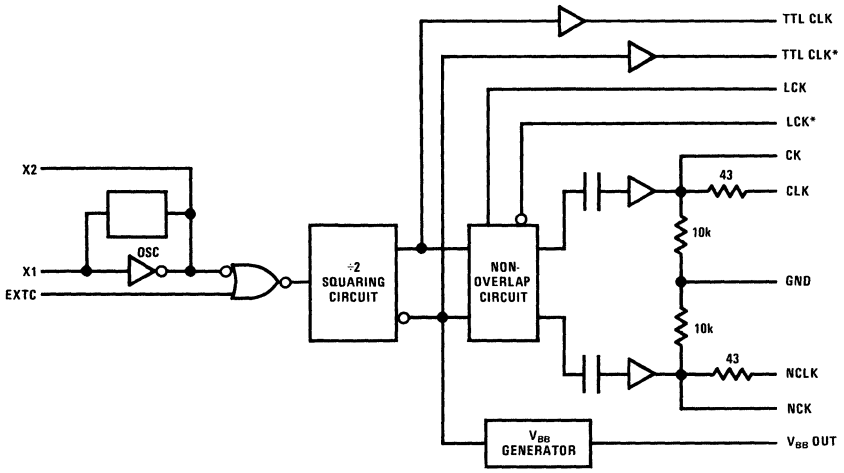
V_{BB} vs Load Current



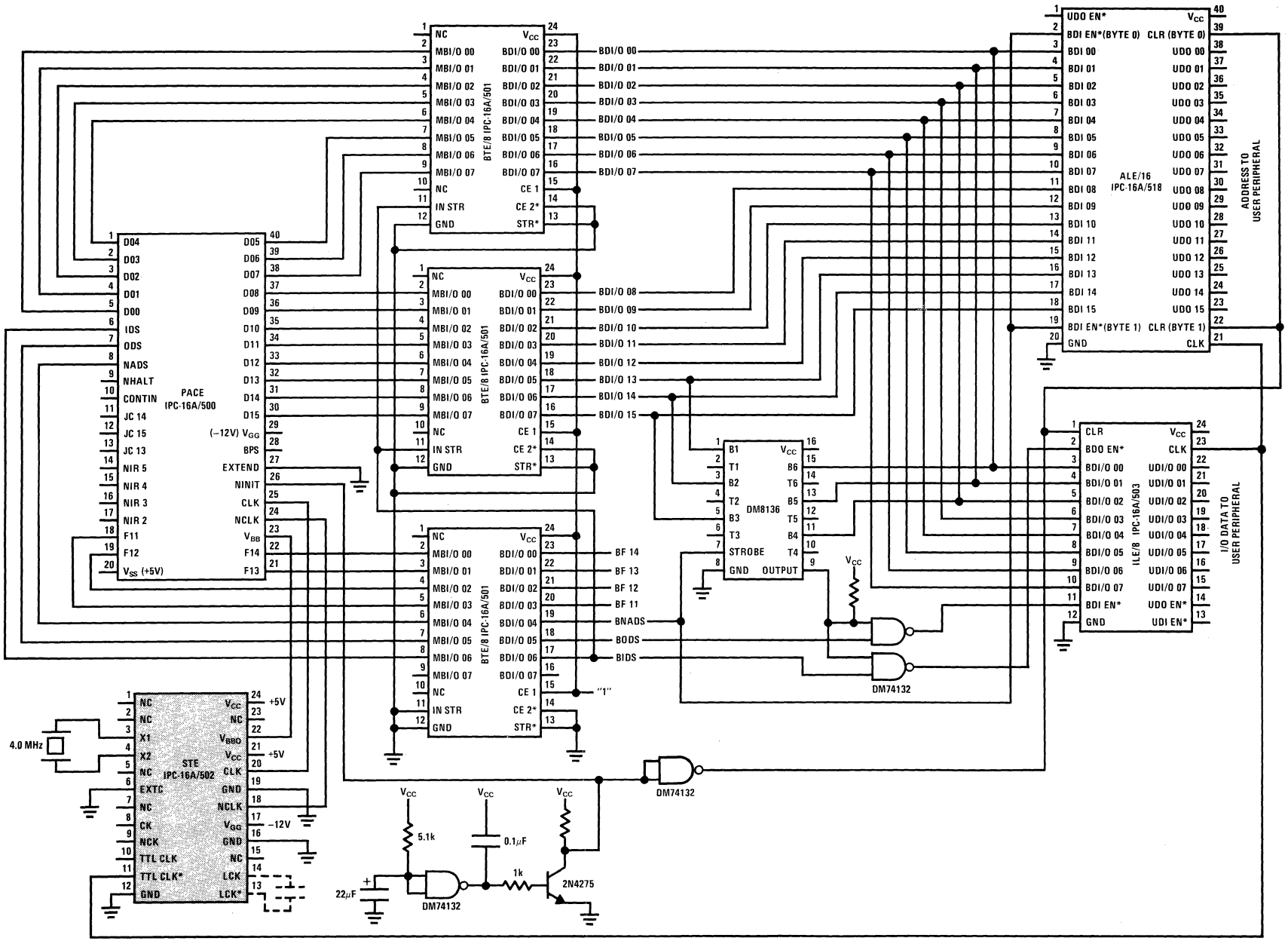
Clock Non-Overlap vs Capacitance



block diagram



Typical Connection Diagram



PRELIMINARY DATA: JUNE 1975

NATIONAL

IPC-16A/503J, IPC-16A/513J
PACE interface latch elements (PACE ILE/8, PACE ILE/16)

general description

The ILE/8 and ILE/16 are positive-edge clocked TRI-STATE® storage elements which provide eight (ILE/8) or sixteen (ILE/16) dual-port flip-flops in a single package. The storage elements operate synchronously from a common clock and may be asynchronously cleared.

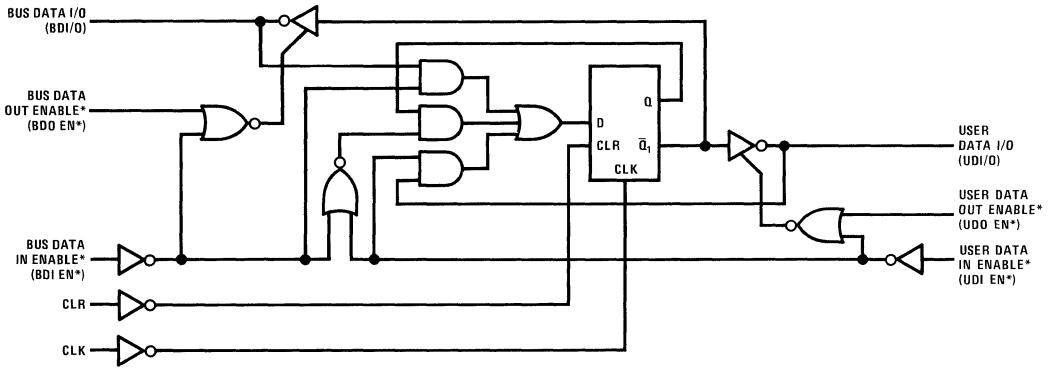
These Green Chip devices are intended specifically for application as bidirectional input/output ports in PACE microprocessor-based systems where minimum package count is desired. User Data Input Enable (UDI EN*) and User Data Output Enable (UDO EN*) control signals are provided for the user to determine whether he inputs data to the microprocessor I/O port or reads data from the microprocessor I/O port during a particular operation. It is possible, therefore, to use the ILE/8 and ILE/16 as either bidirectional I/O ports or as dedicated input and output ports by applying appropriate control signals dynamically (bidirectional mode) or statically (dedicated mode).

TRI-STATE input and output characteristics simplify interface to the system bus and minimize bus loading. The ILE/8 and ILE/16 load the system bus with one TTL load only when they are enabled onto the system bus. All unselected ILE's represent only TRI-STATE loads on the system bus allowing the user to incorporate literally dozens of eight and/or sixteen bit peripheral interfaces without additional buffering of the microprocessor TTL system bus.

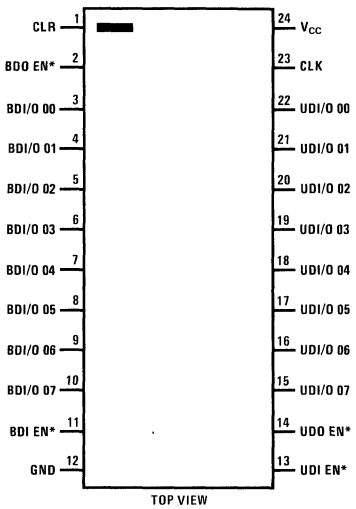
features

- TRI-STATE I/O permits dozens of peripheral interfaces without additional buffering
- Bidirectional dual port storage cuts I/O parts count
- TTL user outputs require no additional buffering
- High speed simplifies interface timing
- Positive-edge clock simplifies data transfer timing

logic diagram



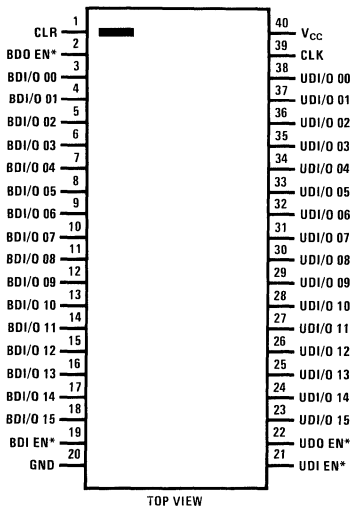
connection diagrams (Dual-In-Line Packages)



TOP VIEW

IPC-16A/503J (PACE ILE/8)

See Package 3



TOP VIEW

IPC-16A/513J (PACE ILE/16)

See Package 4

Signal* ≡ N Signal ≡ $\overline{\text{Signal}}$ ≡ Low Active Signal

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SPECIFICATIONS						
BUS DATA I/O AND USER DATA I/O						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OH} = −800μA	2.4			V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.4	V
I_{LH}	TRI-STATE I/O Current	V_{CC} = Max, V_{OH} = 2.4V			40	μA
I_{LL}	With Inputs and Outputs Disabled	V_{CC} = Max, V_{OH} = 0.4V			−40	μA
(I_{OS})	Output Short Circuit Current	V_{CC} = Max, V_{OL} = 0V (Note 4)	−25		−70	mA
INPUT SPECIFICATIONS						
BUS DATA I/O AND USER DATA I/O						
V_{IH}	Logic "1" Input Voltage		2.0	1.6		V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
V_{IL}	Logic "0" Input Voltage				0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V		−1.0	−1.6	mA
CONTROL, CLR AND CLOCK INPUTS						
V_{iH}	Logic "1" Input Voltage		2.0			V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IH} = 2.4V				
	ILE/8				80	μA
	ILE/16				160	μA
V_{IL}	Logic "0" Input Voltage				0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V				
	ILE/8			−2.0	−3.2	mA
	ILE/16			−4.0	−6.4	mA
INPUT CLAMP VOLTAGE (ALL)		V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
SUPPLY CURRENT						
I_{CC}	ILE/8	V_{CC} = Max			240	mA
	ILE/16				480	mA

ac electrical characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DATA TRANSFER SPECIFICATIONS						
t_{pd0}	Propagation Delay to a Logical "0" From Clear to Output	R_L = 400Ω, C_L = 50 pF		25	40	ns
t_{pd1}	Propagation Delay to a Logical "1" From Clock to Output	R_L = 400Ω, C_L = 50 pF		25	40	ns
t_{S0}	Data to Clock Set-Up Time	R_L = 400Ω, C_L = 50 pF	10	4.5		ns
t_{S1}	Data to Clock Set-Up Time	R_L = 400Ω, C_L = 50 pF	5.0	−4.0		ns
t_{H0}	Data to Clock Hold Time	R_L = 400Ω, C_L = 50 pF	10	4.5		ns
t_{H1}	Data to Clock Hold Time	R_L = 400Ω, C_L = 50 pF	5.0	−4.0		ns

ac electrical characteristics (con't)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL MODE SPECIFICATIONS						
t_{pd0}	Propagation Delay to a Logical "0" From Clear to Output	R_L = 400Ω, C_L = 50 pF		25	40	ns
t_{0H}	Delay From OUT EN* to High Impedance State (From Logical "0" Level)	R_L = 400Ω, C_L = 5.0 pF		15	25	ns
t_{1H}	Delay From OUT EN* to High Impedance State (From Logical "1" Level)	R_L = 400Ω, C_L = 5.0 pF		6.0	15	ns
t_{H0}	Delay From OUT EN* to Logical "0" Level (From High Impedance State)	R_L = 400Ω, C_L = 50 pF		15	25	ns
t_{H1}	Delay From OUT EN* to Logical "1" Level (From High Impedance State)	R_L = 400Ω, C_L = 50 pF		20	30	ns
t_{S0}	Enable to Clock Set-Up Time	R_L = 400Ω, C_L = 50 pF	20	13		ns
t_{S1}	Enable to Clock Set-Up Time	R_L = 400Ω, C_L = 50 pF	20	13		ns
f_{MAX}	Maximum Clock Frequency	R_L = 400Ω, C_L = 50 pF	30	40		MHz
PW_{MIN}	Minimum Clock Pulse Width	R_L = 400Ω, C_L = 50 pF	20			ns
PW_{MIN}	Minimum Clear Pulse Width	R_L = 400Ω, C_L = 50 pF	20			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

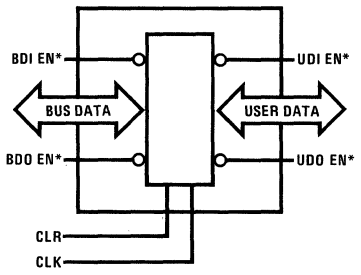
modes of operation (X = Don't Care State)

CLEAR	BDO EN*	UDO EN*	BDI EN*	UDI EN*	BUS DATA	USER DATA	COMMENTS
0	0	1	1	1	Q	Hi-z	Output Data to Bus
0	1	0	1	1	Hi-z	Q	Output Data to User
0	0	0	1	1	Q	Q	Output Data to Both Buses
0	1	1	1	1	Hi-z	Hi-z	"Do-Nothing"—in Hi-z State
0	X	X	0	1	Data	(Note 5)	Enter Data From Bus
0	X	X	1	0	(Note 6)	Data	Enter Data From User
0	X	X	0	0	Data	Data	Enter Data From Both Buses (Logic "1" on Either Will Dominate)
1	X	X	X	X	X	X	Clear

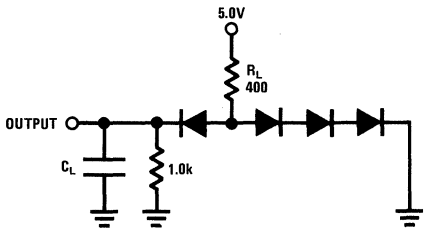
Note 5: Output depends on UDO EN*.

Note 6: Output depends on BDO EN*.

block diagram

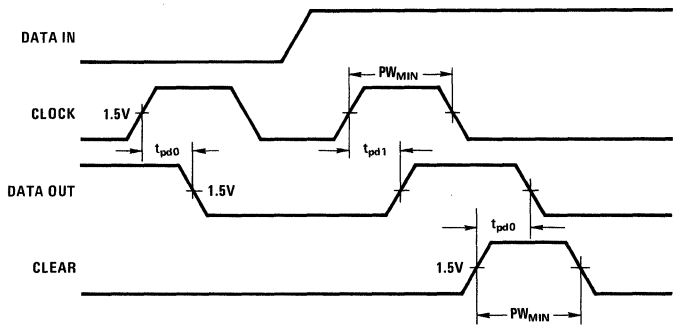


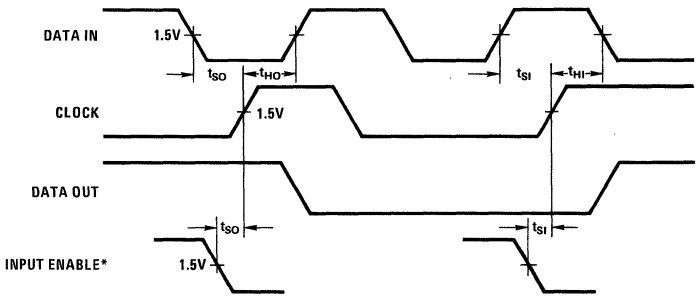
ac test circuit

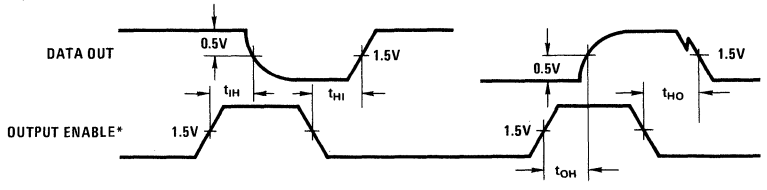


t_{pd0}, t_{pd1}, t_{HI}, t_{HO}: C_L = 50 pF
t_{IH}, t_{OH}: C_L = 5.0 pF

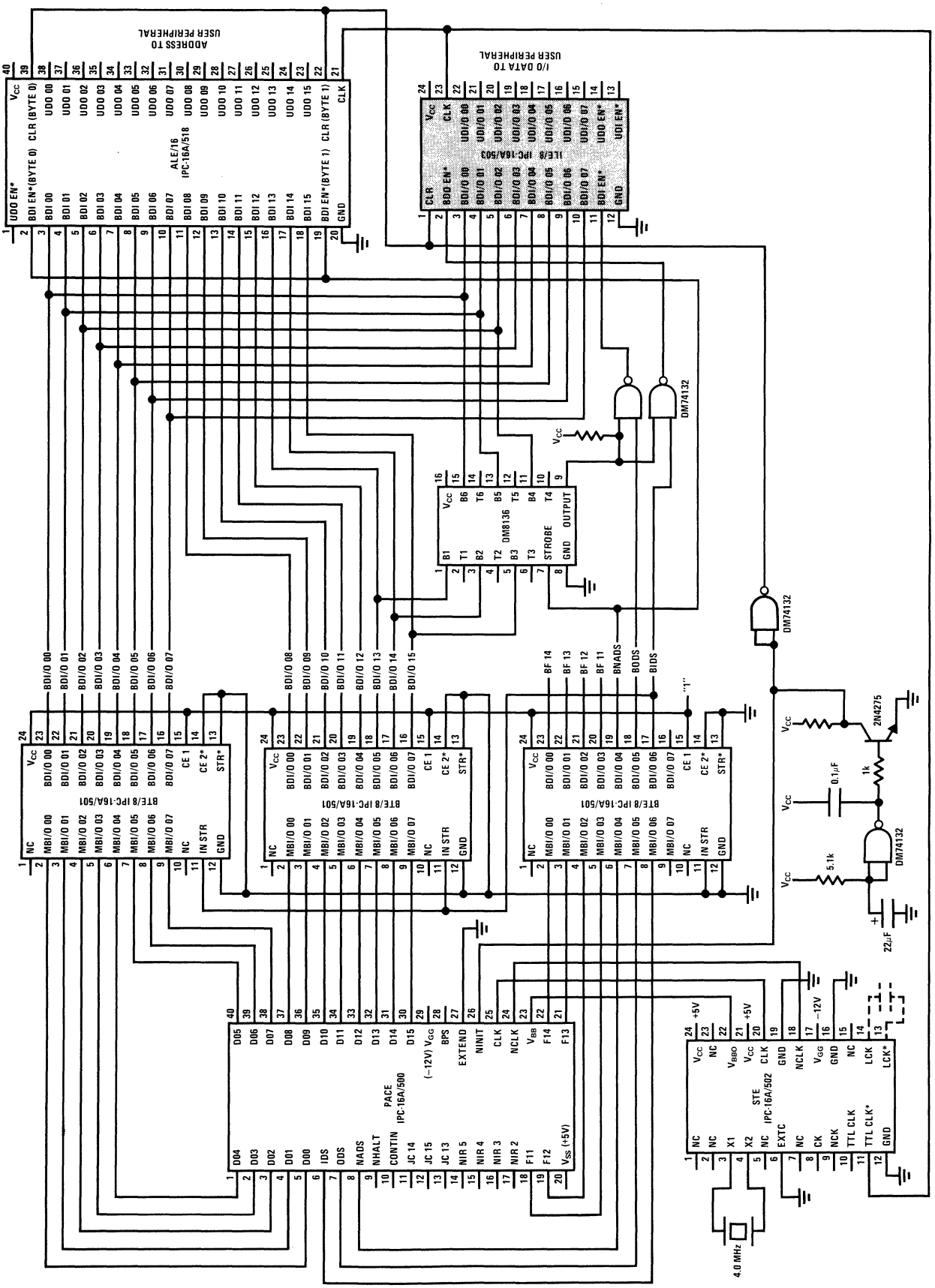
switching time waveforms







PACE system interconnection diagram



NATIONAL

JUNE 1975

IPC-16A/504N 1024-bit (256 × 4) fully decoded static RAM with on chip registers

general description

The National IPC-16A/504N is a 256 word x 4 bit Static Random Access Memory device fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. Data in and data out have the same polarity.

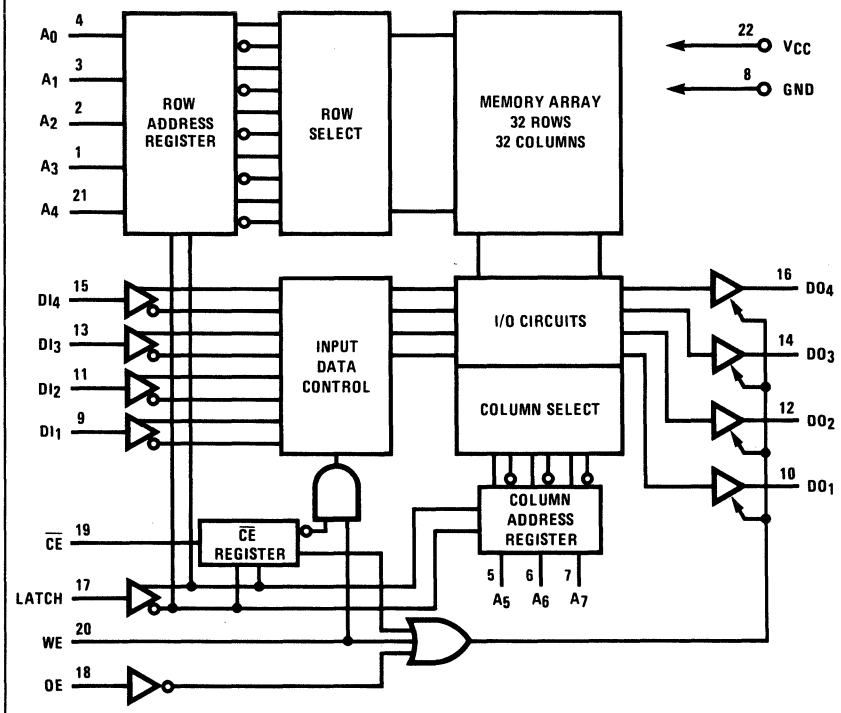
The IPC-16A/504N is fully TTL compatible including inputs, outputs and power supply. The chip enable input allows memory expansion and the address latch feature eliminates the need for external address registers. The output enable is provided for systems which use a common input/output data bus. All of the features of this memory device can be combined to make a low cost, high performance and easy to manufacture memory system. System design costs are also minimized because of the ease-of-use.

National's Silicon Gate process provides protection against contamination and permits the use of low cost Epoxy B packaging.

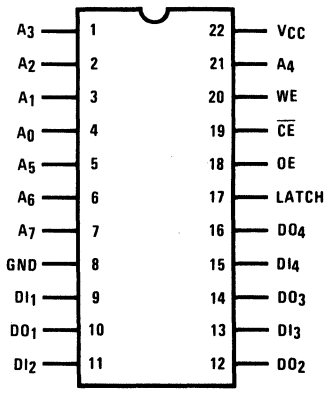
features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs
- On Chip Address and Chip Enable Registers
- Directly TTL Compatible – All Inputs and Outputs
- Single +5 V Power Supply
- TRI-STATE® Output–OR-Tie Capability
- Output Enable for Common Data Bus Systems
- Static Memory – No Refresh Required
- Packaged in a 22 Pin Epoxy B Dual-In-Line

block and connection diagrams



Dual-In-Line Package



IPC-16A/504N (PACE RAM/1k)
See Package 5

absolute maximum ratings

Voltage at Any Pin	-0.5 V to +7.0 V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1 Watt
Lead Temperature (10 s)	300°C

dc electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

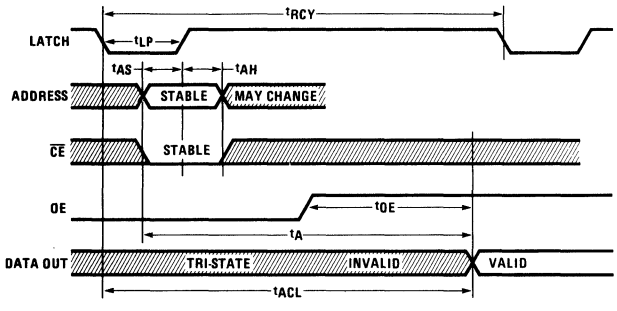
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC}	V	
V_{IL}	Logic "0" Input Voltage	-0.5		0.65	V	
V_{OH}	Logic "1" Output Voltage	2.2			V	I_{OH} = -150 μA
V_{OL}	Logic "0" Output Voltage			0.45	V	I_{OL} = 2.0 mA
I_{LI}	Input Load Current			10	μA	0 V ≤ V_{IN} ≤ 5.0 V
I_{LOH}	Output Leakage Current			15	μA	$\overline{CE}$ = 2.2 V, V_O = 4.0 V
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = 2.2 V, V_O = 0.45 V
I_{CC}	Power Supply Current			70	mA	V_{IN} = 5.25 V, I_O = 0 mA, T_A = 0°C

ac electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

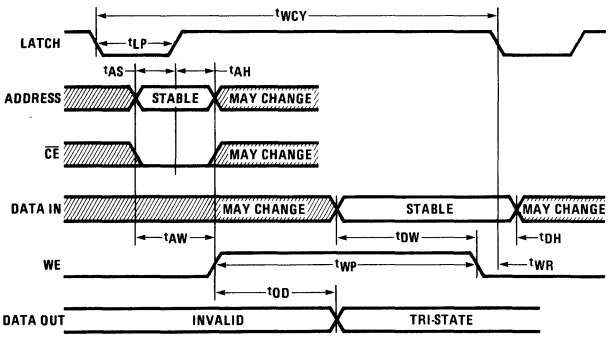
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	
t_A or t_{ACL}	Access Time			1,000	ns	Input Pulse Levels: +0.65 to +2.2 V Input Pulse Rise and Fall Times: 20 ns
t_{OE}	Output Enable to Output Time			500	ns	Timing Measurement Reference Level: 1.5 V
t_{LP}	Latch Pulse Width	200			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{AS}	ADD & $\overline{CE}$ to Latch Setup Time	100			ns	
t_{AH}	ADD & $\overline{CE}$ to Latch Hold Time	100			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	
t_{AW}	Address and CE to Write Setup Time	200			ns	
t_{WP}	Write Pulse Width	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{WR}	Write Recovery Time	50			ns	Input Pulse Rise and Fall Times: 20 ns
t_{OD}	Write to Output Disable Time			400	ns	Timing Measurement Reference Level: 1.5 V
t_{DW}	Data Setup Time	350			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{DH}	Data Hold Time	100			ns	
t_{CW}	Chip Enable to Write	750			ns	
t_{LP}	Latch Pulse Width	200			ns	
t_{AS}	Add & CE to Latch Setup Time	100			ns	
t_{AH}	Add & CE to Latch Hold Time	100			ns	

switching time waveforms

READ CYCLE (WE = "0")



WRITE CYCLE



PRELIMINARY DATA: JUNE 1975

NATIONAL

IPC-16A/505 mask programmable 16,384-bit read only memory (ROM)

general description

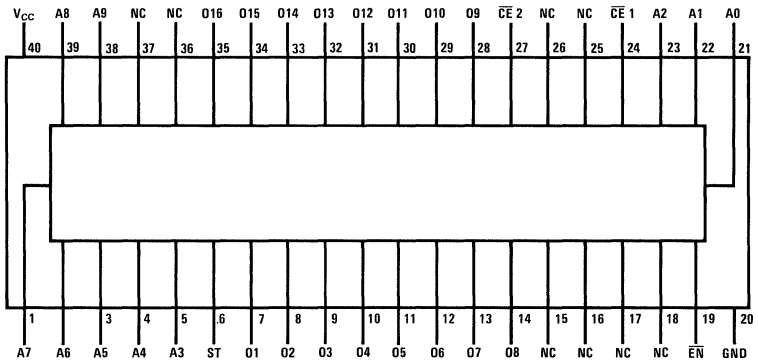
The IPC-16A/505 is 16,384-bit bipolar mask programmable ROM organized as 1024 sixteen-bit words. Ten address inputs select the desired one-of-1024 words. All ten address inputs and two of the three enable inputs have latch feature. The latch function is controlled by the strobe input. The three enable lines are used to either enable or disable the circuit. Truth table and logic diagram for this device are shown below. TRI-STATE® outputs allow for expansion to greater number of words without sacrifice in speed as would be evidenced by open-collector outputs.

features

- On-chip address and enable latches
- Interfaces directly to PACE TTL system bus
- Interfaces directly to PACE TTL control bus
- Fast access eliminates CPU I/O extend
- High density reduces system package count

connection diagram

Dual-In-Line Package



IPC-16A/505D (PACE ROM/16k)
See Package 2

IPC-16A/505N (PACE ROM/16k)
See Package 7

truth table

$\overline{CE\ 1}$ t	$\overline{CE\ 2}$ t	ST t	$\overline{CE\ 1}$ t+1	$\overline{CE\ 2}$ t+1	$\overline{EN}$ t+1	ST t+1	OUTPUT t+1
X	X	X	0	0	0	1	Read stored data for inputs at t+1.
X	X	X	1	X	X	1	Hi - Z
X	X	X	X	1	X	1	Hi - Z
X	X	X	X	X	1	1	Hi - Z
0	0	1	X	X	0	0	Read stored data for add inputs at t.
1	X	1	X	X	X	0	Hi - Z
X	1	1	X	X	X	0	Hi - Z
X	X	X	X	X	1	0	Hi - Z

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC}) IPC-16A/505	4.75	5.25	V
Temperature (T_A) IPC-16A/505	0	70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max,	V_{IN} = 0.4V			−0.8	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min,	V_{IN} = −12 mA	−1.5			V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min,	I_{OUT} = −800μA	2.4			V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)	V_{OUR} = 0V,	−20		−50	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min,	I_{OUT} = 6 mA			0.4	V
I_{CC}	Supply Current	V_{CC} = Max			115		mA
I_O	TRI-STATE Output Current	V_{CC} = Max	V_{OUT} = 0.4V			−40	μA
			V_{OUT} = 2.4V			40	μA

ac electrical characteristics V_{CC} = 5.0V, T_A = 25°C unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Address Inputs to Outputs	V_{CC} = 5.0V, T_A = 25°C		100		ns
t_{pd1}	Propagation Delay to a Logical "1" From Address Inputs to Outputs	V_{CC} = 5.0V, T_A = 25°C		300		ns
t_{1H}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (From Logical "1" Level)	V_{CC} = 5.0V, T_A = 25°C		20		ns
t_{0H}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (From Logical "0" Level)	V_{CC} = 5.0V, T_A = 25°C		40		ns
t_{H1}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to Logical "1" Level (From High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		70		ns
t_{H0}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to Logical "0" Level (From High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		60		ns
	With Respect to Strobe					
t_{S1}	Address Set-Up Time	V_{CC} = 5.0V, T_A = 25°C				
t_{H1}	Address Hold Time	V_{CC} = 5.0V, T_A = 25°C				
t_{S2}	Enable Set-Up Time	V_{CC} = 5.0V, T_A = 25°C				
t_{H2}	Enable Hold Time	V_{CC} = 5.0V, T_A = 25°C				
t_W	Minimum Strobe Pulse Width	V_{CC} = 5.0V, T_A = 25°C		20		ns
t_{ST}	Strobe Access Time	V_{CC} = 5.0V, T_A = 25°C		300		ns

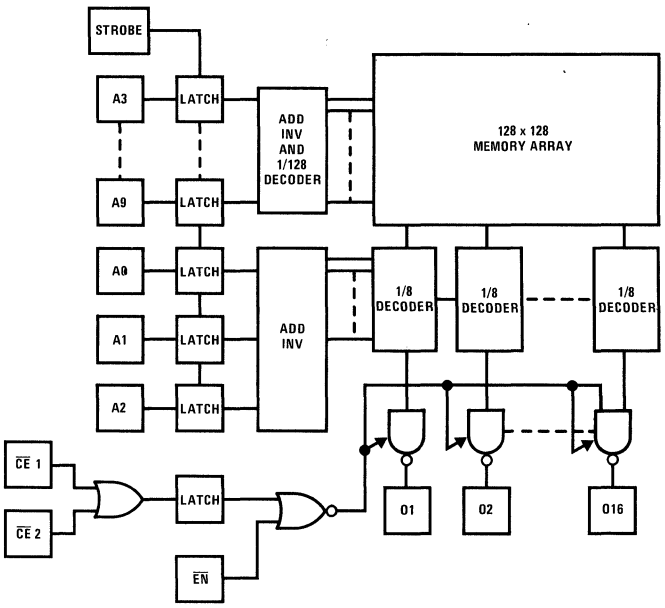
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

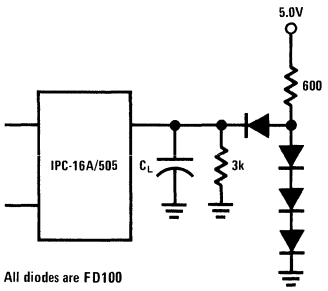
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

logic diagram



ac test circuit



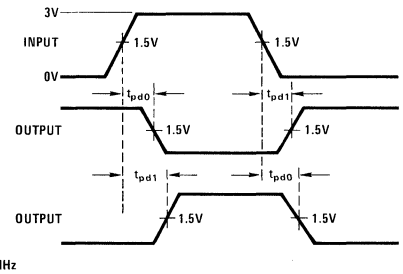
All diodes are FD100

All diodes are FD100

AC TEST	C_L
t_{OH}	5 pF
t_{IH}	5 pF
All others	50 pF

switching time waveforms

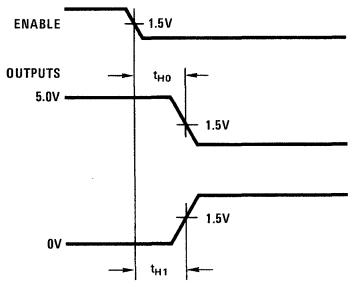
t_{pd1} & t_{pd0}



f = 1 MHz
$t_r = t_f$ 10 ns (10% to 90%)
DUTY CYCLE = 50%

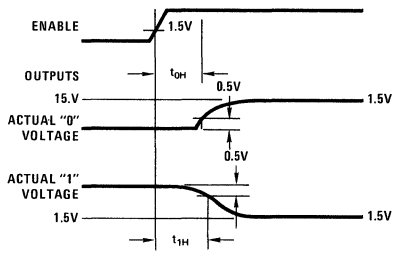
(a)

t_{H0} & t_{H1}

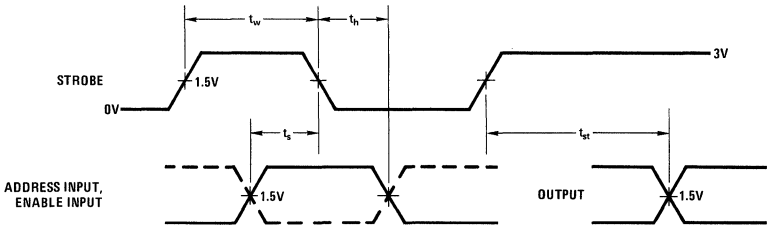


(b)

t_{0H} & t_{1H}



(c)



(d)

PRELIMINARY DATA: MAY 1975

NATIONAL

IPC-16A/506 electrically programmable 4096-bit read only memory (PROM)

general description

The IPC-16A/506 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a 50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

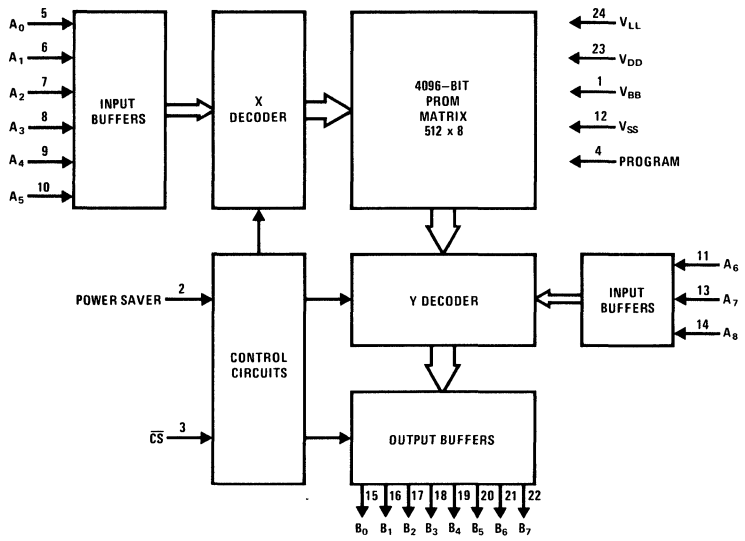
features

- Field programmable
- Fast program time one minute typical for 4096-bits
- Fast access time 750 ns typ
- DTL/TTL compatibility
- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- "Power Saver" control for low power applications
- Pin compatible with IPC-16A/507 (MM5214) mask coded ROM

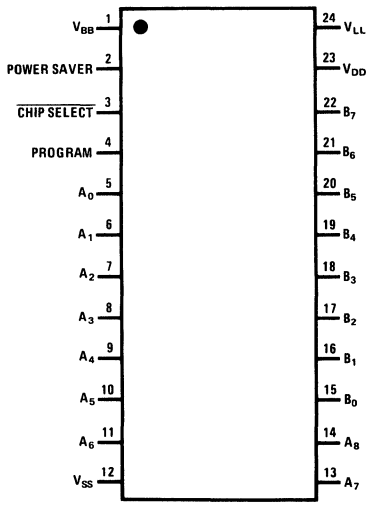
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



TOP VIEW

IPC-16A/506D (PACE PROM/4k)
See Package 1

IPC-16A/506Q (PACE PROM/4k)
See Package 8

Note: For programming information see AN-100.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40	mA
I_{SS}		T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA

ac electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
t_{po}	Power Saver Set-Up Time	*(Figure 1)*			1.8	μs
t_{CO}	Chip Select Delay	*(Figure 1)*			0.5	μs
t_{OH}	Data Hold Time	*(Figure 1)*	30			ns
t_{OD}	Chip Select or Power Saver Deselect Time	*(Figure 1)*	30	300	500	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz (Note 2)		8.0	15	pF

electrical programming characteristics

T_A = 25°C, V_{SS} = CS = 0V, V_{LL} = 0V to −14V, unless otherwise specified, (see *Figure 2*), (Note 5).

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address and Power Saver Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V

electrical programming characteristics (cont.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{ss}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_r, t_f	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 1000 ns + 25 (N-1) where N is the number of devices wire—OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EROM is initially programmed with all "0's." A V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and T_A = 25°C, unless otherwise specified.

erase specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm^2.

programming

The IPC-16A/506Q is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0—A8. Data inputs are B0—B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

programming (cont.)

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP-16P/805
IPC-16P	IPC-16P/805

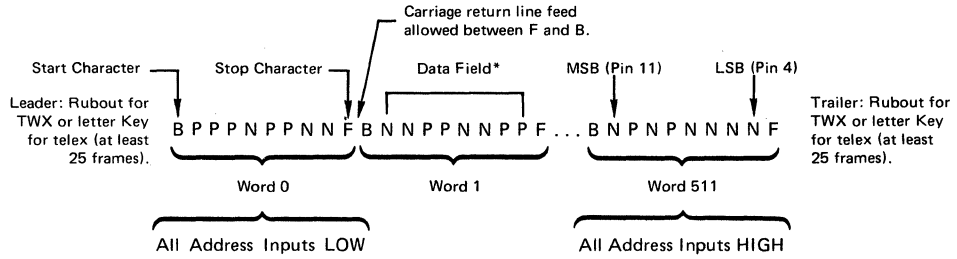
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

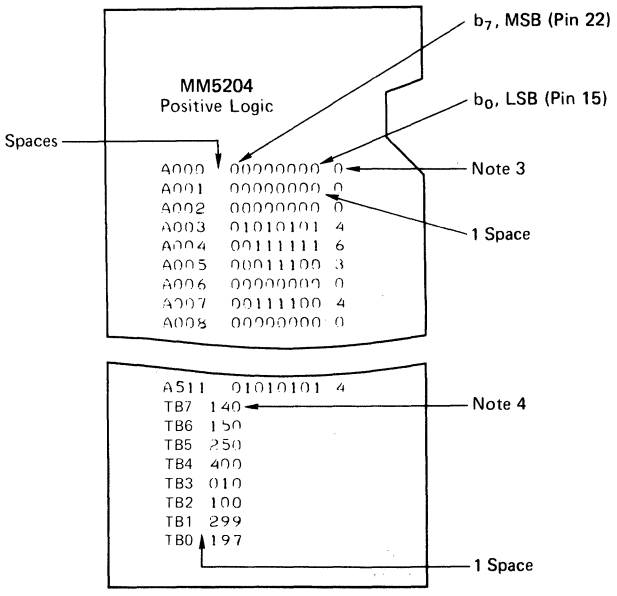
preferred format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

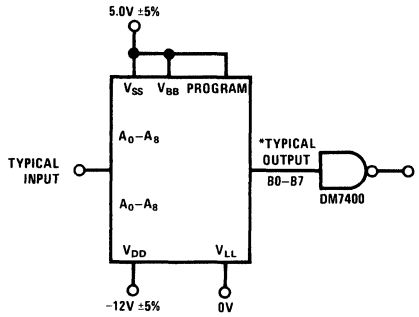
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

erasing procedure

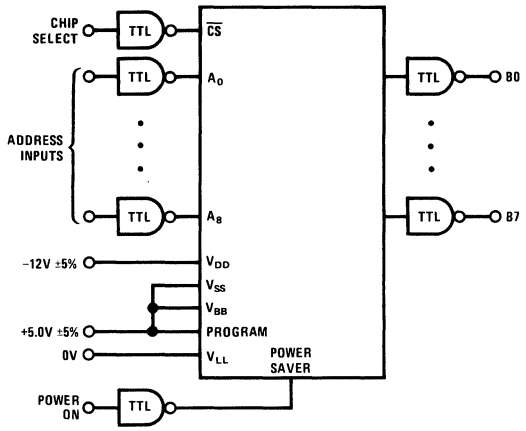
The IPC-16A/506Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2,i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The IPC-16A/506Q should be placed about one inch away from the lamp for about 20—30 minutes.

ac test circuit



*t_{ACC}, t_{OH}, t_{CO}, and t_{OD} measured at output of MM4204/MM5204.

typical application



switching time waveforms

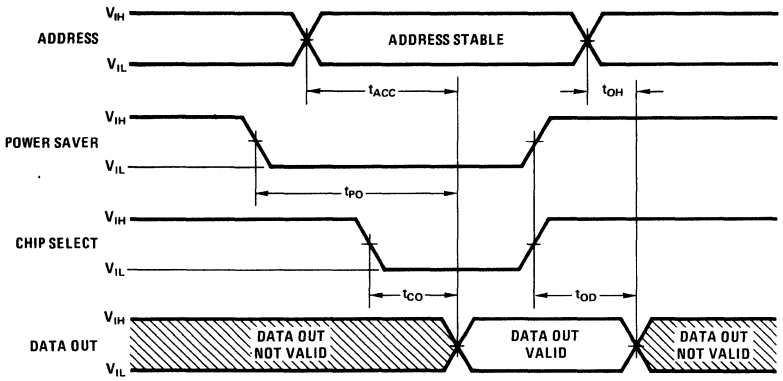


FIGURE 1. Read Operation

programming waveforms

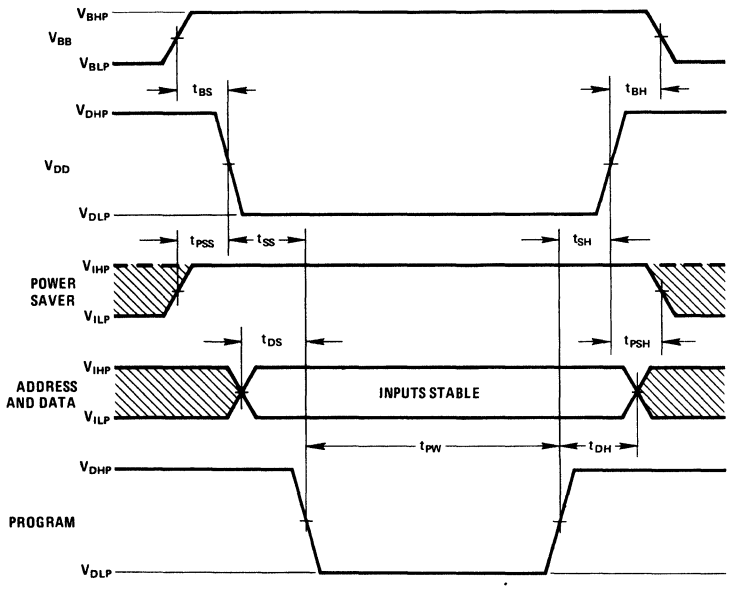


FIGURE 2. Programming Waveforms

JULY 1975

IPC-16A/507 4096-bit static read only memory

general description

The IPC-16A/507 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common date lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

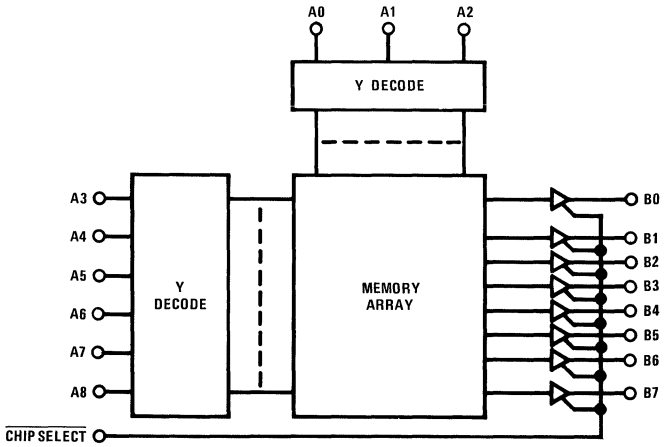
features

- Pin compatible with IPC-16A/506 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

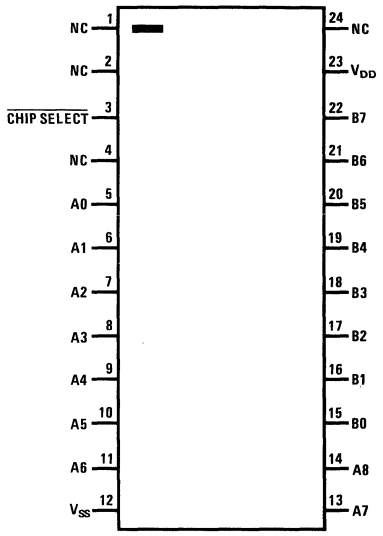
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package

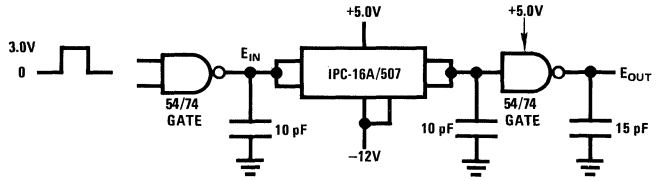


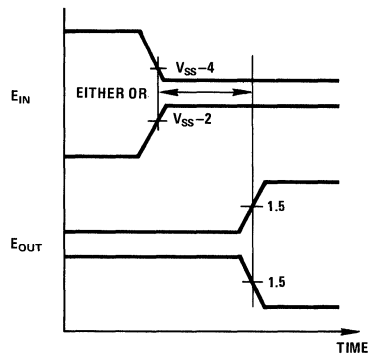
TOP VIEW

IPC-16A/507J
See Package 3

IPC-16A/507N
See Package 6

timing diagram/address time





absolute maximum ratings

V_{DD} Supply Voltage	$V_{SS} - 20V$	Operating Temperature Range	0°C to +70°C
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.03)V$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Logical Low Level Output Voltage	I_L = 1.6 mA, Sink			0.4	V
V_{IH}	Logical High Level Output Voltage	I_L = 100μA, Source	2.4			V
V_L	Logical Low Level Input Voltage				V_{SS}−4.0	V
V_H	Logical High Level Input Voltage		V_{SS}−2.0			V
I_{SS}	Power Supply Current	V_{SS} = 5.0V, V_{DD} = −12V, T_A = 25°C, (Note 4)		23	37	mA
I_{CEX}	Input Leakage	$V_{IN} = V_{SS} - 10V$			1.0	μA
C_{IN}	Input Capacitance	f = 1.0 MHz, V_{IN} = 0V, (Note 2)		5.0	10	pF
C_{OUT}	Output Capacitance	f = 1.0 MHz, V_{IN} = 0V, (Note 2)		4.0	10	pF
T_{ACCESS}	Address Time	V_{DD} = −12V, V_{SS} = 5.0V, T_A = 25°C, (Note 1)	150		1000	ns
	Output AND Connections	(Note 3)			20	

Note 1: Capacitances are measured periodically only.

Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See timing diagram.)

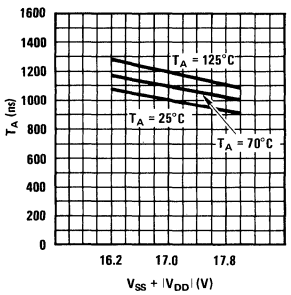
Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N − 1) x 25 ns where N - number of AND connections.

Note 4: Outputs open.

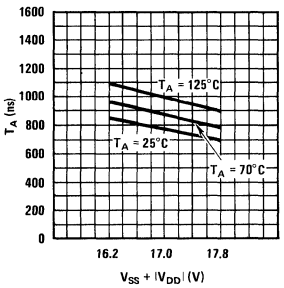
Note 5: Positive true logic notation is used. Logical "1" = most positive voltage level. Logical "0" = most negative voltage level.

typical performance characteristics

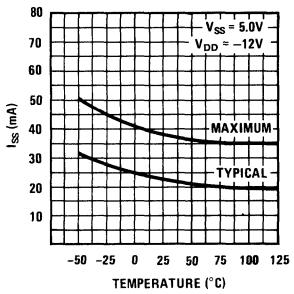
Guaranteed Access Time vs Supply Voltage



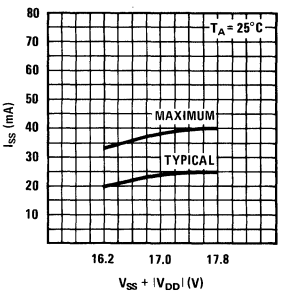
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



PRELIMINARY DATA: JUNE 1975

NATIONAL

IPC-16A/508J, IPC-16A/518J
PACE address latch element (PACE ALE/8, PACE ALE/16)

general description

The ALE/8 and ALE/16 are positive-edge clocked TRI-STATE® storage elements which provide eight (ALE/8) and sixteen (ALE/16) D-type flip-flops in a single package. The storage elements operate synchronously from a common clock. Asynchronous clear inputs are provided.

These Green Chip devices are specifically intended for application as address latches in PACE microprocessor-based systems utilizing time multiplexed address/data buses and incorporating system memory devices without on-chip latched addresses.

Gated input enables allow the user to place the bus data inputs (BDI 00–BDI 15) in a high impedance state minimizing bus loading.

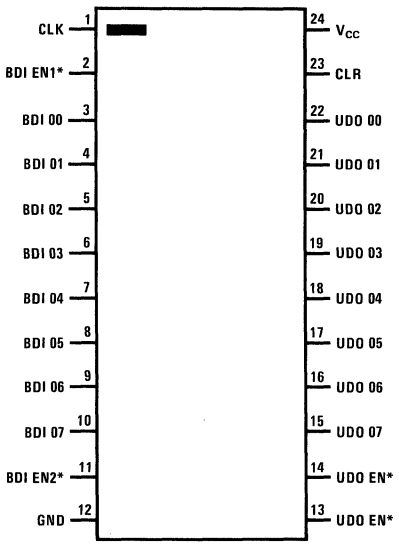
Additionally, the ALE may be used as a dedicated input or output port where its TRI-STATE input and output capability simplifies common bus interfaces by eliminating the need for data port multiplexers and complicated timing and control schemes.

features

- TTL outputs eliminate buffering
- High speed simplifies interface timing
- Positive edge clock simplifies data transfer control
- "Do-nothing" state without gating clock prevents false clocking
- TRI-STATE inputs/outputs minimize bus loading and interface components

connection diagrams

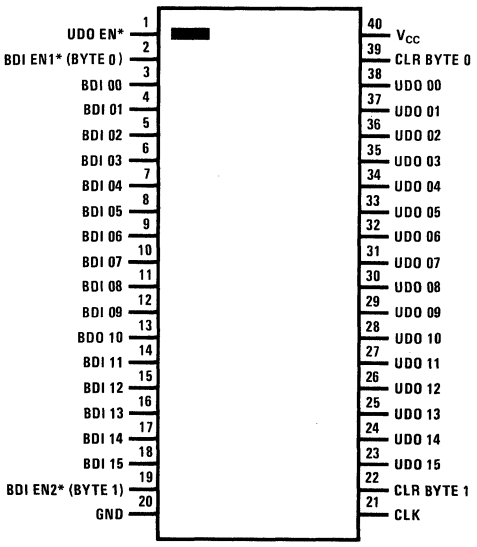
Dual-In-Line Package



TOP VIEW

IPC-16A/508J (PACE ALE/8)
See Package 3

Dual-In-Line Package



TOP VIEW

IPC-16A/518J (PACE ALE/16)
See Package 4

Signal* ≡ N Signal ≡ $\overline{\text{Signal}}$ ≡ Low Active Signal

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage	4.75	5.25	V
Temperature	0	+70	°C

dc electrical characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT SPECIFICATIONS						
USER DATA OUTPUT BUS (UDO 00–15)						
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min, I_{OH} = −5.0 mA	2.6	3.0		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.2	0.4	V
I_{LH}	TRI-STATE Output Current	V_{CC} = Max, UDO EN* = "1", V_O = 0.4V			40	μA
I_{LL}	TRI-STATE Output Current	V_{CC} = Max, UDO EN* = "1", V_O = 2.4V			−40	μA
I_{SO}	Output Short Circuit Current	V_{CC} = Max, V_{OL} = 0V	−30		−70	mA
INPUT SPECIFICATIONS						
BUS DATA INPUTS (BDI φφ–15)						
V_{IH}	Logic "1" Input Voltage	V_{CC} = Min	2.0	1.6		V
I_{IH}	Logic "1" Input Current	V_{CC} = Max, V_{IH} = 2.4V		10	40	μA
		V_{CC} = Max, V_{IH} = 5.5V			1	mA
V_{IL}	Logic "0" Input Voltage	V_{CC} = Min		1.4	0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V		−1.0	−1.6	mA
I_{LH}	TRI-STATE Input Current	V_{CC} = Max, BDI EN* = "1", V_{IH} = 2.4V		10	40	μA
I_{LL}	TRI-STATE Input Current	V_{CC} = Max, BDI EN* = "1", V_{IL} = 0.4V		−10	−40	μA
CONTROL BUS INPUTS						
V_{IH}	Logic "1" Input Voltage	V_{CC} = Min	2.0	1.6		V
I_{IH}	Logic "1" Input Current					
	BDI EN*, CLR, UDO EN*, CLK (ALE/8)	V_{CC} = Max, V_{IH} = 2.4V		15	80	μA
		V_{CC} = Max, V_{IH} = 5.5V			1	mA
	UDO EN*, CLK (ALE/16)	V_{CC} = Max, V_{IH} = 2.4V			120	μA
		V_{CC} = Max, V_{IH} = 5.5V			1	mA
V_{IL}	Logic "0" Input Voltage	V_{CC} = Min		1.4	0.8	V
I_{IL}	Logic "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V				
	BDI EN*, CLR, UDO EN*, CLK (ALE/8)			−2.0	−3.2	mA
	UDO EN*, CLK (ALE/16)			−4.0	−4.8	mA
INPUT CLAMP VOLTAGE (ALL)		V_{CC} = Min, I_{IN} = −12 mA			−1.5	V

ac electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
I_{CC}	(ALE/8)	V_{CC} = Max		100	144	mA
I_{CC}	(ALE/16)	V_{CC} = Max		200	288	mA
DATA TRANSFER SPECIFICATIONS (V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF)						
	Maximum Clock Frequency		25	30		MHz
PW_{MIN}	Minimum Pulse Width		20			ns
t_S	Bus Data Input Set-Up Time			3	10	ns
t_H	Bus Data Input Hold Time			3	10	ns
t_{pd0}	Delay to Logic "0"		10	20	30	ns
t_{pd1}	Delay to Logic "1"		10	20	30	ns
CONTROL MODE SPECIFICATIONS (V_{CC} = 5.0V, T_A = 25°C)						
t_S	BDI EN* Set-Up Time			7	15	ns
t_H	BDI EN* Hold Time			−7	0	ns
UDO EN*						
t_{1H}	Delay to Hi-Z From Active "1"		3	10	30	ns
t_{0H}	Delay to Hi-Z From Active "0"		3	10	30	ns
t_{H1}	Delay to "1" From Hi-Z		5	15	30	ns
t_{H0}	Delay to "0" From Hi-Z		5	15	30	ns
t_{pdR}	Delay to "0" From Clear			20	30	ns

notes

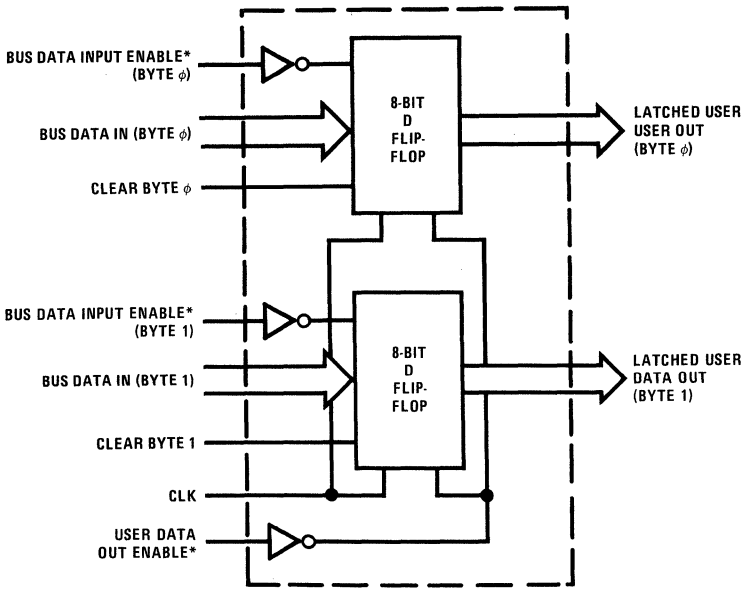
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply operating conditions.

Note 2: Unless otherwise specified the min-max limits across the 0°C to 70°C temperature range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

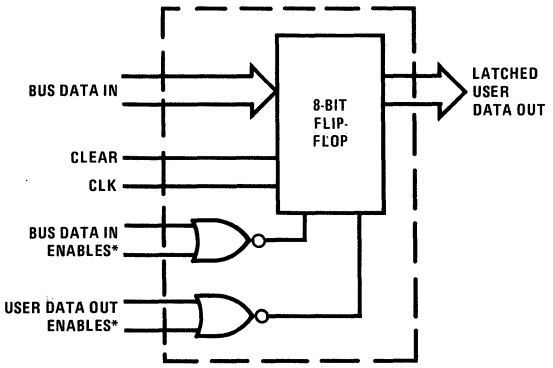
Note 3: Only one output at a time should be shorted.

block diagrams

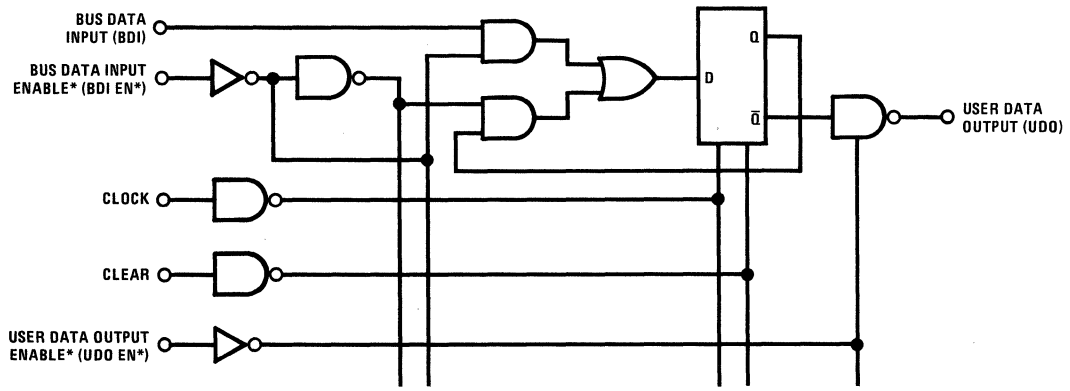
ALE/16



ALE/8



typical circuit diagram

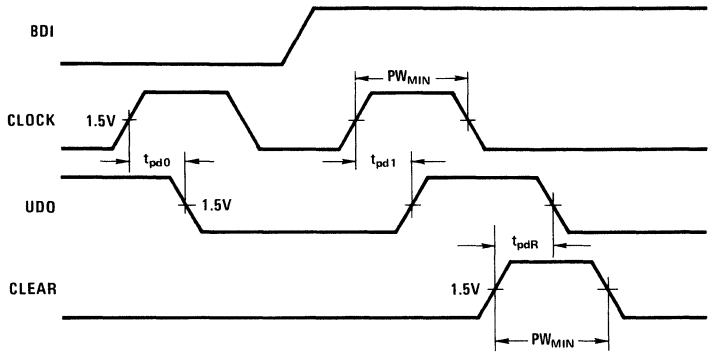


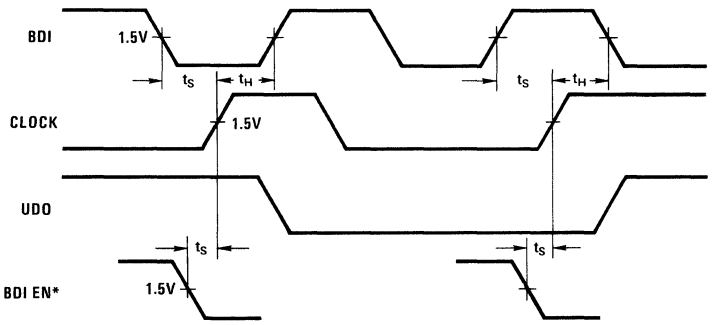
truth table

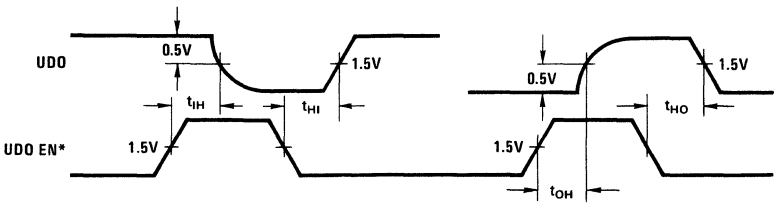
ALE/8 and ALE/16 (UDO EN* = 0)

t_n			t_{n+1}
CLR	BDI EN1* BDI EN2*	BDI	UDO
1	X	X	0
0	1	X	O_n
0	0	1	1
0	0	0	0

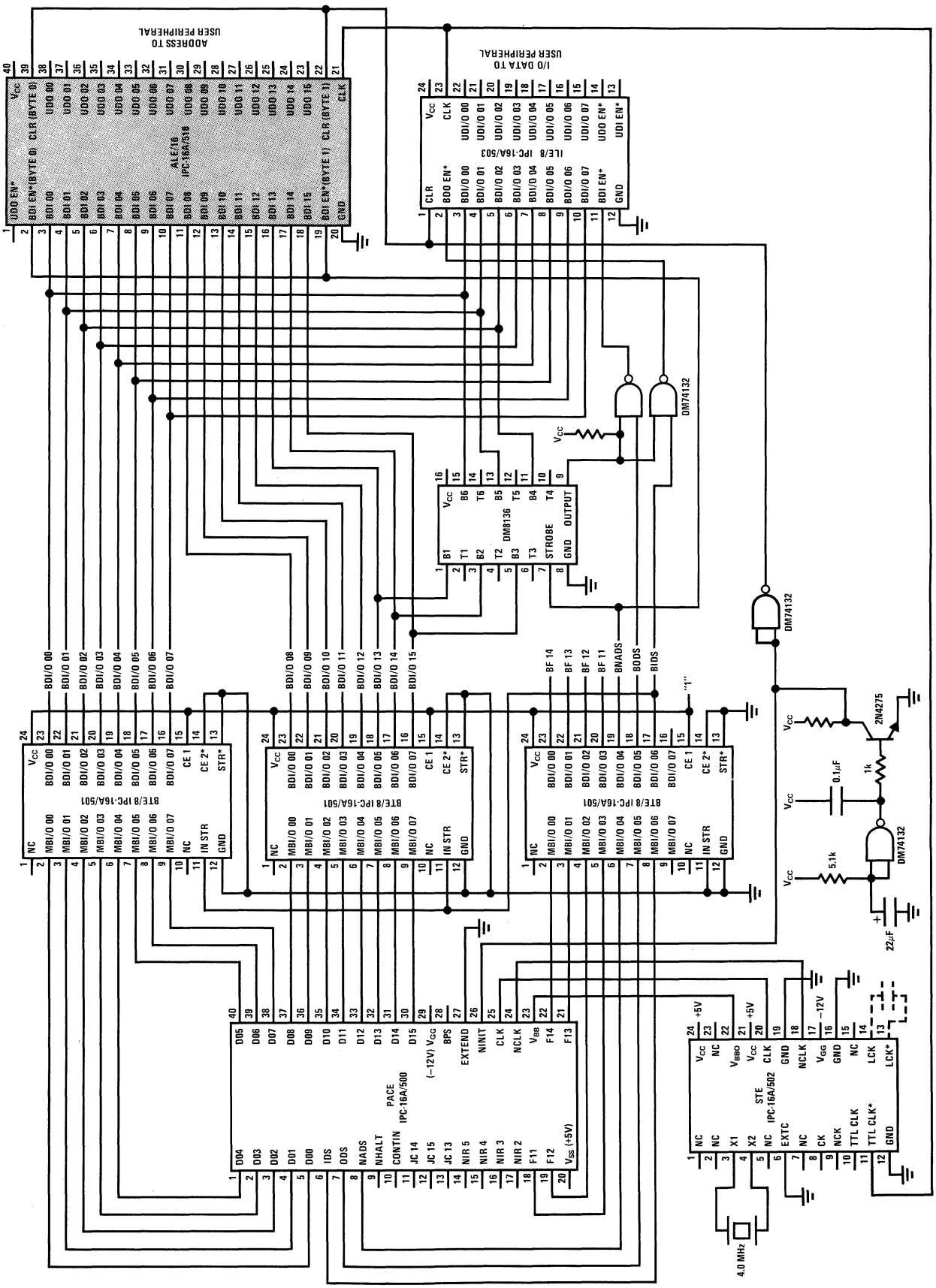
switching time waveforms







PACE system interconnection diagram



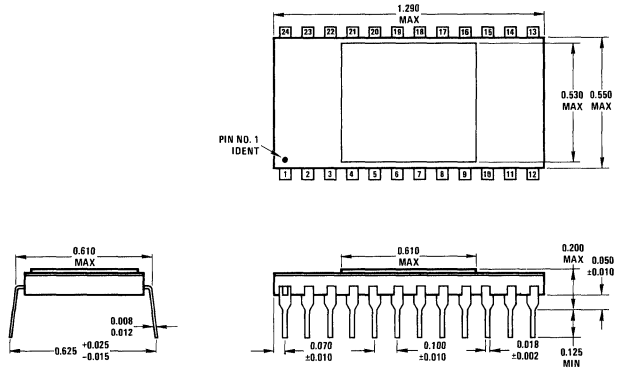
DUAL-IN-LINE PACKAGES

(N) Devices ordered with "N" suffix are supplied in molded dual-in-line package. Molding material is EPOXY B, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot-solder-dipped surface to allow for ease of solderability.

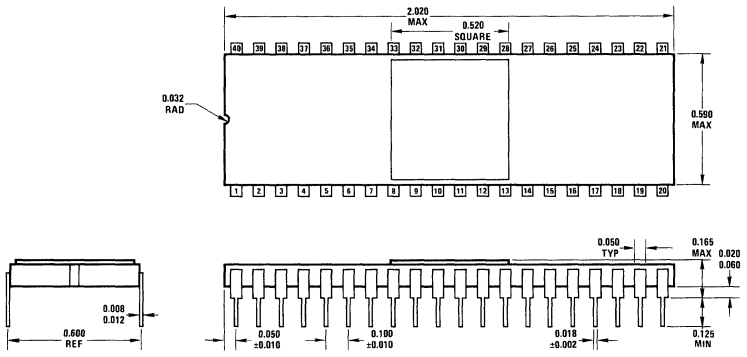
(J) Devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(D) Devices ordered with the "D" suffix are supplied in glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

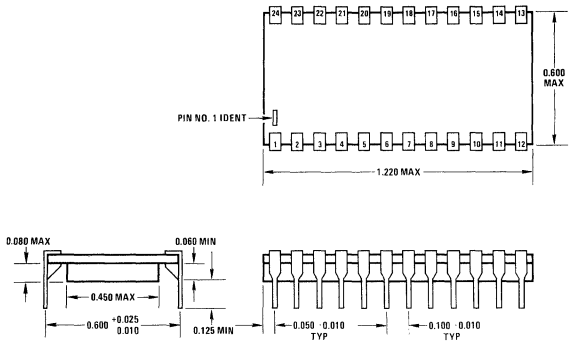
(Q) Devices ordered with the "Q" suffix are supplied in a glass/metal dual-in-line with a quartz cover.



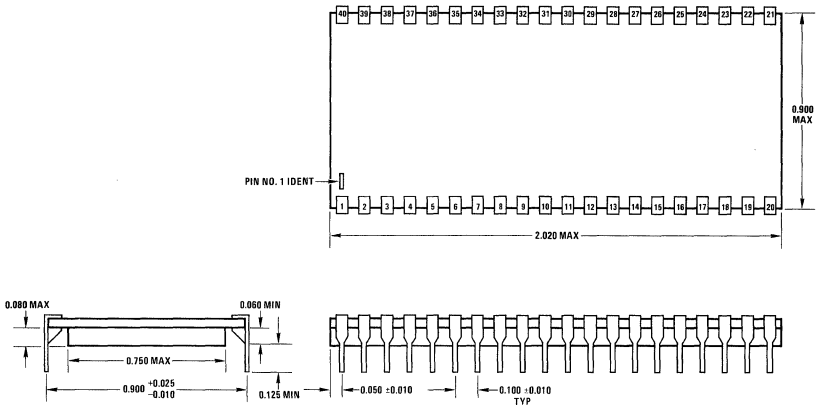
Package 1
24 Lead Cavity DIP (D)



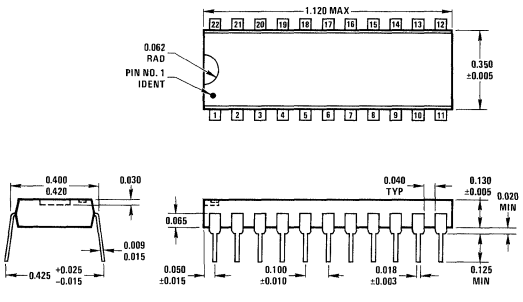
Package 2
40 Lead Cavity DIP (D)



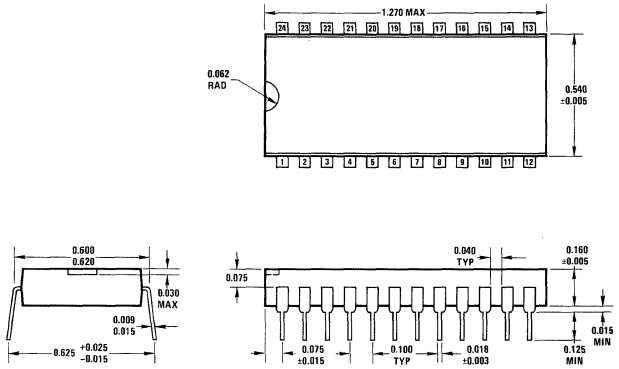
Package 3
24 Lead Cavity DIP (J)



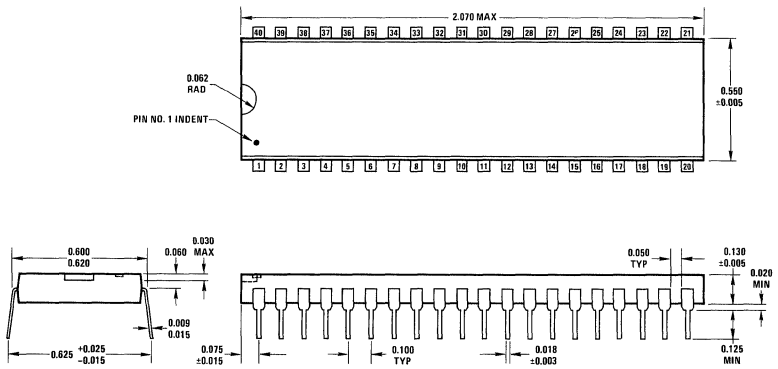
Package 4
40 Lead Cavity DIP (J)



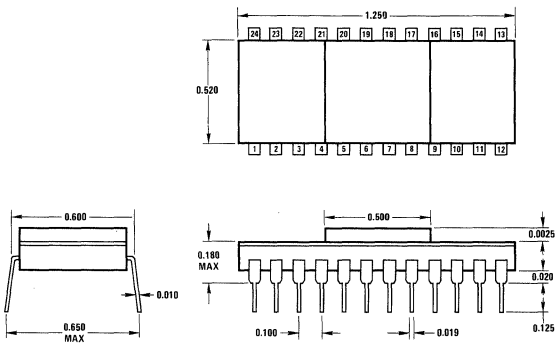
Package 5
22 Lead Molded DIP (N)



Package 6
24 Lead Molded DIP (N)



Package 7
40 Lead Molded DIP (N)



Package 8
24 Lead Cavity DIP (Q)

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