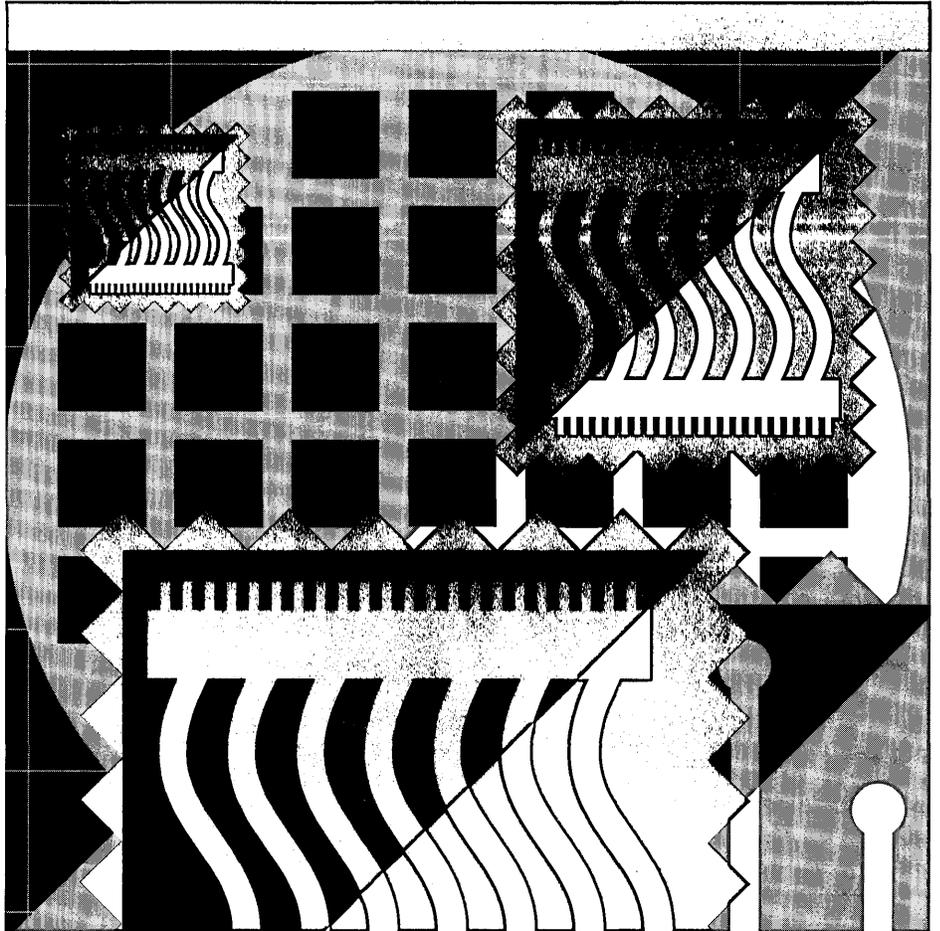
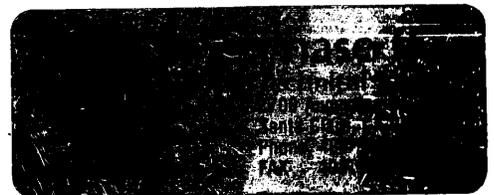


# NCR 53C810 PCI-SCSI I/O Processor

NCR



Data Manual





PRELIMINARY

# NCR 53C810 PCI-SCSI I/O Processor



**Due to changes in the PCI standard, this revision of the 53C810 data manual does not reflect the production version of the 53C810 device. Information in this draft is preliminary. Upcoming changes in the PCI standard will affect the 53C810 chip design. Please contact your NCR sales representative for any current information regarding the 53C810.**

## Data Manual

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# Preface

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## SCSI and PCI Reference Information

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards. For background information, please contact:

### **ANSI**

11 West 42nd Street  
New York, NY 10036  
(212) 642-4900  
Ask for document number X3.131-1986 (SCSI-1)

### **Global Engineering Documents**

2805 McGaw  
Irvine, CA 92714  
(800)-854-7179 or (714) 261-1455  
Ask for document number X3.131-199X (SCSI-2)

### **ENDL Publications**

14426 Black Walnut Court  
Saratoga, CA 95070  
(408) 867-6642  
Document names: *SCSI Bench Reference*, *SCSI Encyclopedia*

### **Prentice Hall**

Englewood Cliffs, NJ 07632  
(201) 767-5937  
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

### **NCR Microelectronic Products Division Electronic Bulletin Board**

(719) 596-1649

### **SCSI Electronic Bulletin Board**

(719) 574-0424

### **PCI Special Interest Group**

C/O Intel Corporation  
52000 NE Elam Young Parkway, HF 3-15  
Hillsboro, OR 97123  
(503) 696-2000

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# Table of Contents

Preface .....	ii
SCSI and PCI Reference Information .....	ii

---

## Chapter One SCSI I/O Processor Description

General Description .....	1-1
NCR TolerANT Technology .....	1-1
53C810 Benefits Summary .....	1-2

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## Chapter Two Functional Description

SCSI Core .....	2-1
DMA Core .....	2-1
SCRIPTS Processor .....	2-1
Executing Instructions With SCSI SCRIPTS .....	2-2
SDMS: The Total SCSI Solution .....	2-2
Loopback Mode.....	2-2
Parity Options .....	2-2
DMA FIFO .....	2-4
Data Paths .....	2-4
SCSI Bus Interface .....	2-5
Terminator Networks .....	2-6
(Re)Select During (Re)Selection .....	2-6
Synchronous Operation .....	2-6

---

## Chapter Three PCI Functional Description

PCI Addressing.....	3-1
PCI Bus Commands and Functions Supported .....	3-2
Configuration Registers .....	3-2

Vendor ID Register .....	3-4
Device ID .....	3-4
Command Register .....	3-4
Revision ID Register .....	3-6
Status Register .....	3-6
Latency Timer Register .....	3-7

**Chapter Four**  
Signal Descriptions

Power and Ground Pins .....	4-2
System Pins .....	4-3
Address and Data .....	4-3
Interface Control .....	4-4
Arbitration .....	4-5
Error Reporting .....	4-5
SCSI Signals .....	4-6
Additional Interface .....	4-7

**Chapter Five**  
Operating Registers

Operating Register Addresses and Descriptions .....	5-1
Register Address Map .....	5-3

**Chapter Six**  
Instruction Set of the I/O Processor

**Chapter Seven**  
Electrical Characteristics

DC Electrical Characteristics .....	6-1
NCR TolerANT Active Negation Technology Electrical Characteristics .....	6-5
AC Electrical Characteristics .....	6-8
53C810 Timings .....	6-19

**Appendix A**  
Register Summary

**Appendix B**  
Mechanical Drawing

## Chapter One

# SCSI I/O Processor Description

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## General Description

The 53C810 PCI-SCSI I/O Processor is based on the NCR 53C7XX I/O Processor architecture with a Peripheral Component Interconnect (PCI) front end. The NCR 53C810 integrates a high-performance SCSI core and a PCI bus master DMA core with a SCSI SCRIPTS processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. The 53C810 solves the protocol overhead problems that have plagued previous intelligent and non-intelligent adapter designs.

The 53C810 has been designed to "gluelessly" connect to the emerging industry standard PCI Bus. An entire SCSI solution, including a SCSI oscillator (40MHz), termination electronics, and an external connector (Figure 1-1), can be implemented on less than four square inches of space on the motherboard. In addition to the required PCI pins, the 53C810 provides two other signals useful in adapter plug-in card designs.

The chip is fully supported by NCR SDMS (SCSI Device Management System) software based on the industry standard Common Access Method (CAM). The 53C810 is packaged in a 100-pin PQFP package, can operate the SCSI bus at 5 MB/s asynchronously or 10 MB/s synchronously, and burst data to the host at full PCI speeds.

The 53C810 is designed to implement a multi-threaded I/O algorithm with a minimum of processor intervention. The 53C810 provides automatic relocation of SCRIPTS, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be

placed in PROM. The 53C810 allows easy firmware upgrades and is supported by advanced SCRIPTS commands.

---

## NCR TolerANT® Technology

The 53C810 features NCR TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI REQ, ACK, Data, and Parity signals to be actively driven high. Active negation is enabled by setting bit 7 in the STEST3 register.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signal to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate the double clocking of data, the single biggest reliability issue with SCSI operations. The filtering period is user-selectable at 30 or 60 ns, with bit 1 in the STEST2 register.

The benefits of TolerANT include increased immunity to noise when the signal is going high, increased performance due to balanced duty cycles, and improved fast SCSI transfer rates. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

---

# 53C810

## Benefits Summary

### Performance

- Supports variable block size and scatter/gather data transfers.
- Supports 32-bit word data bursts with variable burst lengths
- Sustained memory-to-memory DMA transfers in excess of 47 MB/s (@ 33 MHz)
- Zero wait-state bus master with burst transfers in excess of 110 MB/s (@ 33 MHz)
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Unique interrupt status reporting – reduces ISR overhead
- High-speed async/sync single-ended SCSI bus transfers
  - 5 MB/s asynchronous
  - 10 MB/s synchronous
- 64-byte DMA FIFO

### Integration

- Full 32-bit PCI DMA bus master
- Optionally can be used as a third-party PCI bus DMA controller by using the Memory to Memory Move instructions.
- High performance SCSI core
- Integrated SCRIPTS processor

### Ease of Use

- Direct PCI-to-SCSI connection
- First "3-volt friendly" PCI device
- Reduces SCSI development effort
- Easily adapted to the SCSI Common Access Method (CAM)
- Compiler-compatible with existing 53C710 and 53C720 SCRIPTS
- Direct connection to PCI and single-ended SCSI buses.
- Development tools and SCSI SCRIPTS available
- All interrupts are maskable and pollable
- Three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100  $\mu$ s to greater than 1.6 seconds.
- Fully supported by NCR SDMS software for complex PC-based operating system support

### Flexibility

- High level programmer's interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory
- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Low level programmability (register oriented)
- Allows a target to disconnect and later reselect with no interrupt to the system processor

- Allows a multi-threaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching
- Allows relative jumps
- Fetch, Master, and Memory Access control pins.
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Separate SCSI and system clocks
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 25% of pins are power and ground
- Power and ground isolation of I/O pads and internal chip logic
- NCR TolerANT technology provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved fast SCSI transfer rates.
  - Input signal filtering on SCSI receivers; improves data integrity, even in noisy cabling environments.

### Reliability

- 2 K volts ESD protection on SCSI signals
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA

### Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Supports single-step mode operation
- Test mode (AND tree) to check pin continuity to the board

Figure 1-1. SCSI Port Logic

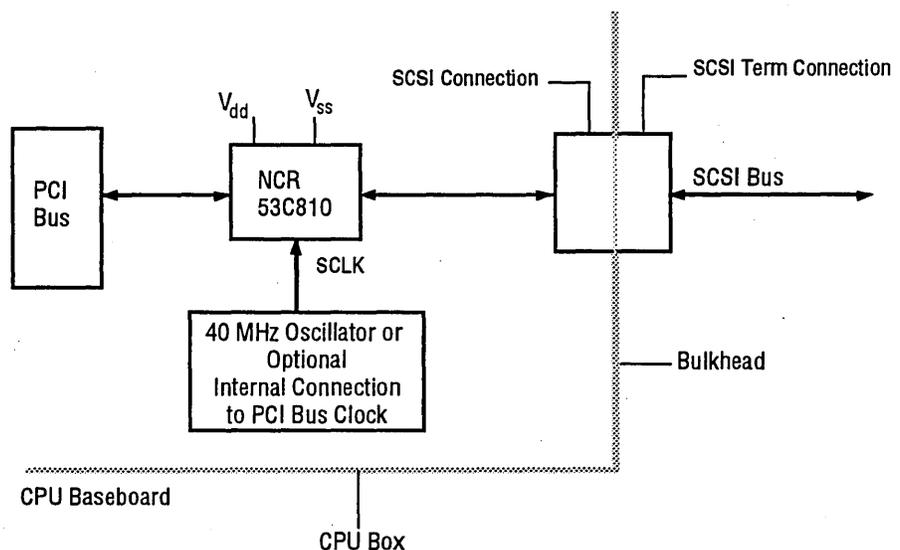
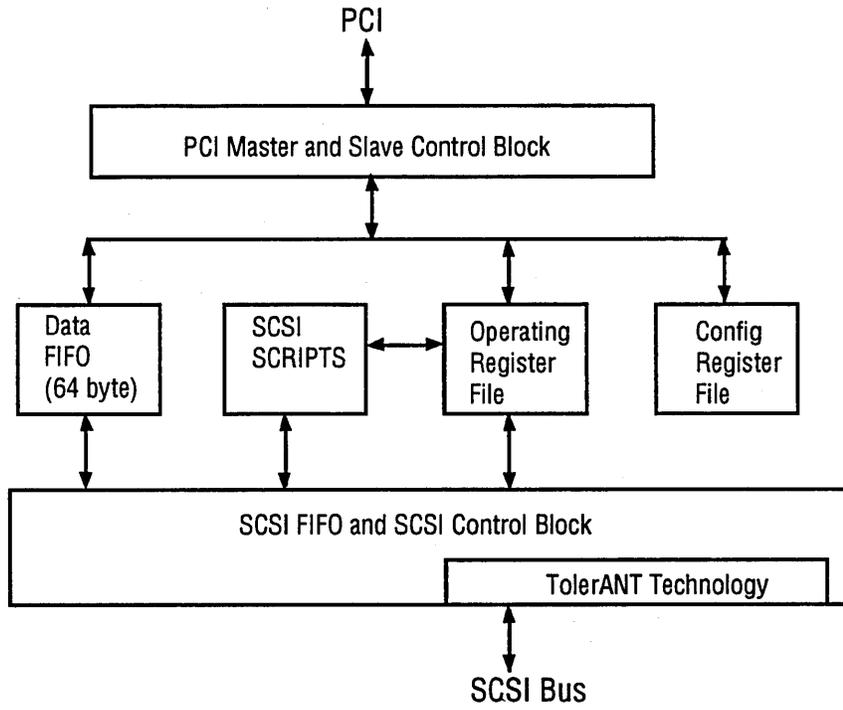


Figure 1-2. 53C810 Block Diagram



---

## Chapter Two

# Functional Description

The 53C810 is composed of three functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor. The 53C810 is fully supported by the SCSI Device Management System (SDMS)<sup>™</sup>, a complete software package that supports the NCR product line of SCSI processors and controllers.

---

## SCSI Core

The SCSI core supports the SCSI-2, 8-bit bus. It supports synchronous transfer rates of up to 10 MB/s, and asynchronous transfer rates up to 5 MB/s. The programmable SCSI interface makes it easy to “fine tune” the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the 53C810 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. The 53C810 can test the SCSI pins for physical connection to the board or the SCSI bus.

The 53C810 SCSI core can be controlled by the integrated DMA core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus

Phases and in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

---

## DMA Core

The DMA core is a bus master DMA device that is made to attach directly to the industry standard PCI Bus. The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

The 53C810 supports 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the 53C810 to support two, four, eight, or sixteen longword bursts across the PCI bus interface.

---

## SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores and are executed from 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This com-

pires with 2-8 ms required for traditional intelligent host adapters. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e., scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2 or SCSI-3 logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are independent of the type of CPU or system bus in use.

The 53C810 can be programmed with SCSI SCRIPTS, including advanced SCSI SCRIPTS capabilities. A complete set of development tools is available for writing custom drivers with SCSI SCRIPTS.

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### Executing SCRIPTS Instructions

After power up and initialization of the 53C810, the chip may be operated in low level (register interface) mode, or in SCSI SCRIPTS mode. To operate in SCSI SCRIPTS mode, the 53C810 requires only a SCRIPTS start address. All SCRIPTS commands are fetched from local or external memory. The 53C810 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an unexpected event causes an interrupt to the external processor. SCSI SCRIPTS operation offloads the microprocessor from servicing the numerous interrupts inherent in I/O operations. Four types of SCRIPTS instructions are available in the 53C810: Block Move, I/O or Read/Write, Transfer Control, and Memory Move. Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, used only by Memory Move instructions, is loaded into the TEMP shadow register.

Block Move instructions allow indirect addressing, table indirect addressing, and chained block moves, depending on bit settings in the DCMD, DBC, and DSPS registers. I/O instructions allow table indirect mode, relative address mode, and options to set or clear the carry bit in the ALU. Read/Write instructions include read-modify-write cycles and moves to and from the SFBR register. Transfer Control instructions include jump, call, return, interrupt (including interrupt-on-the-fly), and relative addressing mode. Memory Move instructions allow the transfer of single or multiple register values to or from system memory, to free the system processor for other tasks and move data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction.

---

## SDMS: The Total SCSI Solution

The 53C810 provides a total SCSI solution in PC environments with the NCR SCSI Device Management System (SDMS). SDMS provides BIOS driver support for hard disk, tape, and removable media peripherals for the DOS, Windows™, OS/2™, and Novell operating environments. The NCR SCSI Evaluation Kit is available to system developers and contains SDMS evaluation software, an evaluation SCSI board, and full documentation for the kit components.

The SDMS includes a SCSI BIOS (CAMcore), resident in the SCSI controller or processor, to manage all SCSI functions related to the device. SDMS also provides a series of SCSI device drivers (CAMpliant modules) that support most major operating systems. SDMS supports multi-threaded I/O application programming interface (API) for user-developed SCSI applications.

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## Loopback Mode

The 53C810 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip communicate with itself. When the Loopback Enable bit is set in the STEST1 register, the 53C810 allows control of all SCSI signals, whether the 53C810 is operating in initiator or target mode.

---

## Parity Options

The 53C810 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

- 1) Assert ATN/ on Parity Errors – Bit 1 in the SCNTL0 register. This bit causes the 53C810 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.
- 2) Enable Parity Checking – Bit 3 in the SCNTL0 register. This bit enables the 53C810 to check for parity errors. The 53C810 checks for odd parity.
- 3) Assert Even SCSI Parity – Bit 2 in the SCNTL1 register. This bit determines the SCSI parity sense checked and generated by the 53C810.
- 4) Disable Halt on ATN/ or a Parity Error (Target Mode Only) – Bit 5 in the SCNTL1 register. This bit causes the 53C810 to halt operations when a parity error is detected in target mode.
- 5) Enable Parity Error Interrupt – Bit 0 in the SIENO register. This bit determines whether the 53C810 will generate an interrupt when it detects a SCSI parity error.
- 6) Parity Error – Bit 0 in the SIST0 register. This status bit is set whenever the 53C810 has detected a parity error on the SCSI bus.
- 7) Status of SCSI Parity Signal – Bit 0 in the SSTAT0 register. This status bit represents the live SCSI Parity Signal (SDP).
- 8) Latched SCSI Parity Signal – Bit 3 in the SSTAT1 register.

Table 2-1. SCSI Parity Control

EPC	ASEP	Description
0	0	Will not check for parity errors. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
0	1	Will not check for parity errors. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.
1	0	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
1	1	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.

**Key:** *EPC = Enable Parity Checking (bit 3 SCNTL0)*  
*ASEP= Assert SCSI Even Parity (bit 2 SCNTL1)*

Table 2-2. SCSI Parity Errors and Interrupts

This table describes the options available when a parity error occurs. This table only applies when the Enable Parity Checking bit is set.

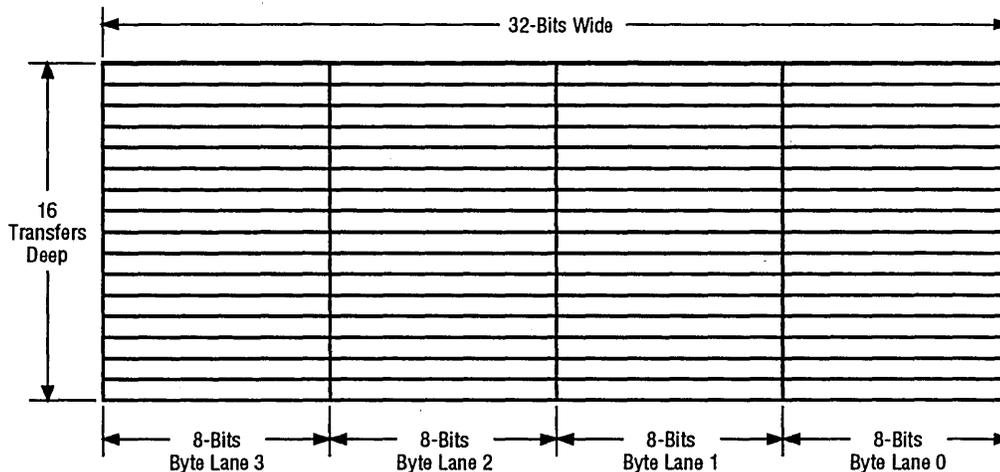
DHP	PAR	Description
0	0	Will halt when a parity error occurs in target or initiator mode and will NOT generate an interrupt.
0	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode.
1	0	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will not be generated.
1	1	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will be generated.

**Key:** *DHP = Disable Halt on ATN/ or Parity Error (bit 5 SCNTL1)*  
*PAR= Parity Error (bit 0 SIEN0)*

## DMA FIFO

The DMA FIFO is 32 bit by 16 transfers deep. It is divided into 4 sections, each 8 bits wide and 16 transfers deep.

Figure 2-1. DMA FIFO Sections



## Data Paths

The data path through the 53C810 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2-2 shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps will determine if any bytes remain in the data path when the chip halts an operation:

### Asynchronous SCSI Send:

- 1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.

- 2) Read bit 5 in the SSTAT0 register to determine if a byte is left in the SODL register. If bit 5 is set in SSTAT0, then the SODL register is full.

### Synchronous SCSI Send:

- 1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 64.
- 2) Read bit 5 in the SSTAT0 register to determine if a byte is left in the SODL register. If bit 5 is set in the SSTAT0, then the SODL register is full.
- 3) Read bit 6 in the SSTAT0 register to determine if any bytes are left in the SODR register. If bit 6 is set in SSTAT0, then the SODR register is full.

**Asynchronous SCSI Receive:**

- 1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.
- 2) Read bit 7 in the SSTAT0 register to determine if a byte is left in the SIDL register. If bit 7 is set in SSTAT0, then the SIDL register is full.

**Synchronous SCSI Receive:**

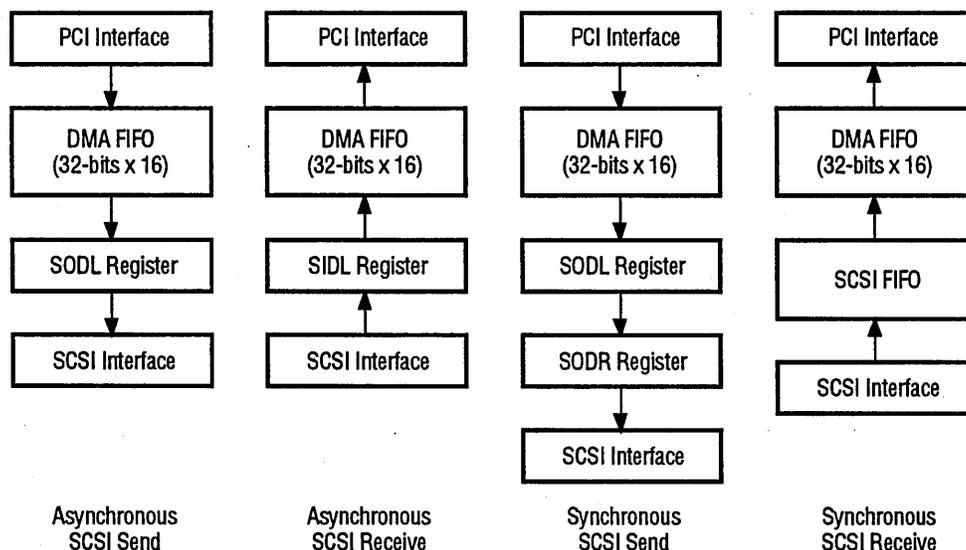
- 1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 64.
- 2) Read the SSTAT1 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

**SCSI Bus Interface**

The 53C810 is intended for use in single-ended applications and has no support for differential operation.

All SCSI signals are active low. The 53C810 contains the output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down 53C810 has no effect on an active SCSI bus (CMOS "voltage feed-through" phenomena). NCR TolerANT technology provides signal filtering at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

Figure 2-2. 53C810 Host Interface Data Paths



## Terminator Networks

The terminator networks provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for single-ended applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed.

Single-ended cables can use a 220  $\Omega$  pullup to the terminator power supply (Term-Power) line and a 330  $\Omega$  pull-down to Ground. Because of the high-performance nature of the 53C810, Alternative Two termination (defined in the ANSI standard) is recommended. This method employs a 2.85 volt regulator and a 110  $\Omega$  pullup resistors (no pull-down). Figure 2-3 shows the schematics for Alternative Two termination. For additional information, refer to the SCSI-2 Specification. Active negation can be used with either termination network.

## (Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select a target and is reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a SET INITIATOR instruction or the target SCRIPTS should start with a SET TARGET instruction. It

should be noted that the selection and reselection enable bits (SCID bits 5 and 6, respectively) should both be asserted so that the 53C810 may respond as an initiator or as a target.

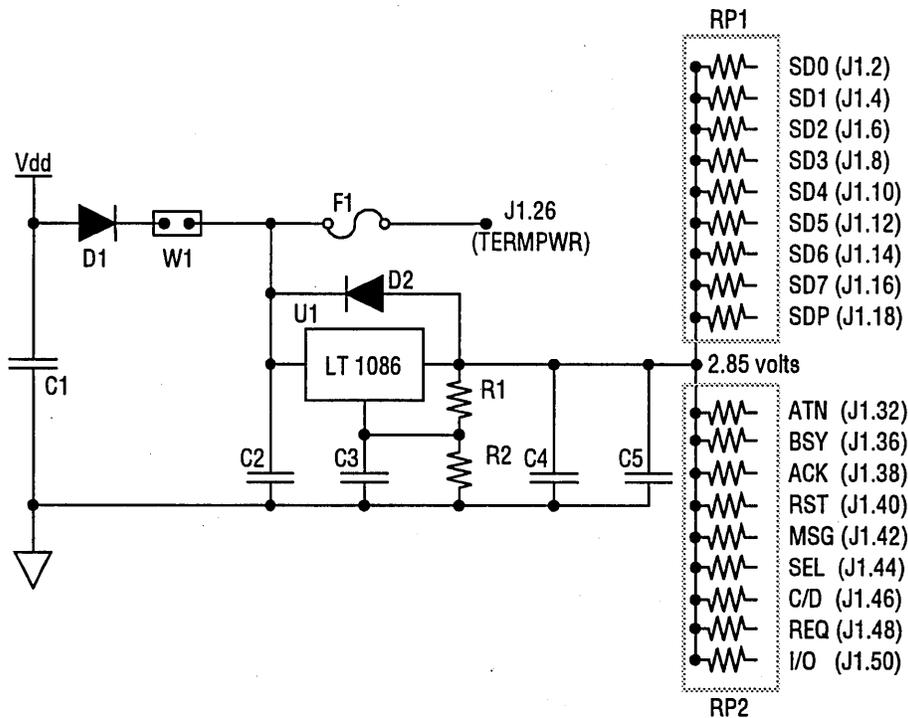
The Selection or Reselection Enable bits allow the 53C810 to respond as either a target or an initiator. For example, if only selection is enabled, the 53C810 cannot be reselected as an initiator. There are also status and interrupt bits in the SIST0 and SIEN0 registers, respectively, indicating if the 53C810 has been selected (bit 5) and reselected (bit 4).

## Synchronous Operation

The 53C810 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPTS execution begins, from within SCRIPTS via a table indirect I/O instruction, or with a read-modify-write instruction.

The 53C810 can receive data from the SCSI bus at a synchronous transfer period as short as 80 ns or 160 ns, regardless of the transfer period used to send data. Depending on the SCLK frequency, and the negotiated transfer period, and the synchronous clock divider, the 53C810 can send synchronous data at intervals as short as 100 ns for fast SCSI and 200 ns for slow SCSI.

Figure 2-3. 53C810 Alternative Two Termination



**Key:**

- |         |   |
|---------|---|
| C1      | 4.7 $\mu$ F tantalum, SMT                   |
| C2, C3  | 1.0 $\mu$ F tantalum, SMT                   |
| C4      | 22 $\mu$ F tantalum, SMT                    |
| C5      | 0.1 $\mu$ F ceramic, SMT                    |
| D1-D2   | Schottkey diode, 1NS817                     |
| F1      | 1.5 Amp fuse, socketed, 2AG                 |
| J1      | 50-pin dual row header, male SCSI connector |
| RP1-RP2 | 110 x 9 (1%) pullups, 1% SIP-10             |
| U1      | Voltage Regulator, LT 1086, TO-39           |
| W1      | 2-position header                           |
| R1      | 121 ohms, 1%                                |
| R2      | 154 ohms, 1%                                |

## Chapter Three

# PCI Functional Description

## PCI Addressing

There are three types of PCI-defined address space:

- Configuration space
- Memory space
- I/O space

Configuration space is a contiguous 256 8-bit set of addresses dedicated to each "slot" or "stub" on the bus. A decode of C\_BE/(3-0) determines if this PCI cycle is intended to access configuration register space. The IDSEL bus signal is a "chip

select" that allows access to the configuration register space only. A configuration read/write cycle without IDSEL will be ignored. The eight lower order addresses are used to select a specific 8-bit register. The host uses this configuration space to initialize the 53C810.

The lower 128 bytes of the 53C810's 256-byte configuration space holds system parameters while the upper 128 bytes maps into the 53C810 operating registers. For all PCI cycles except configuration cycles, the 53C810 registers are located on the 256-byte block boundary defined by the system assigned (through the configured register) base address. The 53C810 operating registers will be available in both the upper and lower 128-byte portions of the 256-byte space selected.

Table 3-1. PCI Bus Commands and Encoding Types

CBE/(3-0)	Command Type	Supported as Master	Supported as Slave
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100	Reserved		n/a
0101	Reserved		n/a
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved		n/a
1001	Reserved		n/a
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	No	Yes*
1101	Reserved		n/a
1110	Memory Read Line	Yes**	Yes*
1111	Memory Write and Invalidate	No	Yes*

\* These cycles will be interpreted as standard memory reads or writes \*\* This operation is selectable by bit 3 in the DMODE register

At initialization time, each PCI device is assigned a base address (in the case of the 53C810, the upper 24 bits of the address are selected) for memory accesses and I/O accesses. On every access, the 53C810 compares its assigned base addresses with the value on the A/D bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the 53C810 and the low order 8 bits define the register to be accessed. A decode of the CBE/ (3-0) determines which registers and what type of access is to be performed.

PCI defines memory space as a contiguous 32-bit memory address that is shared by all system resources including the 53C810. Base Address Register 1 determines which 256-byte memory area this device will occupy.

PCI defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the 53C810. Base Address Register 0 determines which 256-byte I/O area this device will occupy.

---

## PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C<sub>BE</sub>/(3-0) lines during the address phase. (PCI bus command encoding and types are listed in Table 3-1.)

The I/O Read command is used to read data from an agent mapped in I/O address space. All 32 address bits are decoded.

The I/O Write command is used to write data to an agent when mapped in I/O address space. All 32 address bits are decoded.

The Memory Read command is used to read data from an agent mapped in memory address space. All 32 address bits are decoded.

The Memory Write command is used to write data to an agent when mapped in memory address space. All 32 address bits are decoded.

The 53C810 responds to Memory Read Multiple, Memory Read Line, and Memory Write and Invalidate commands by treating them similar to standard Memory Read and Memory Write commands. The 53C810 will not respond to reserved commands, special cycle, or interrupt acknowledge commands.

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## Configuration Registers

Configuration registers are accessible only by PCI configuration cycles. No other cycles, including SCRIPTS, can access these registers.

The lower 128 bytes hold configuration data while the upper 128 bytes hold the 53C810 operating registers, which are described in Chapter Five, *Operating Registers*. These registers can be accessed by SCRIPTS.

Table 3-2 depicts the PCI configuration data implemented by the 53C810. Note that addresses 40h through 7Fh are not defined.

All PCI-compliant devices, such as the 53C810, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional. In the 53C810, registers that are not supported are not writable and will return all zeroes when read. Only those registers and bits that are currently supported by the 53C810 are described in this chapter. For more detailed information on PCI registers, please see the *PCI Specification*.

Table 3-2. Configuration Registers Implemented by the PCI Standard in the 53C810

				Config
31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Reserved	Not Supported	Reserved	Rev ID	08h
Not Supported	Reserved	Latency Timer	Not Supported	0Ch
Base Address 0 (I/O)*				10h
Base Address 1 (Mem)**				14h
Not Supported				18h
Not Supported				1Ch
Not Supported				20h
Not Supported				24h
Reserved				28h
Reserved				2Ch
Not Supported				30h
Not Supported				34h
Reserved				38h
Reserved				3Ch
<i>Addresses 40h through 7Fh are not defined.</i>				

\*I/O Base is supported

\*\*Memory Base is supported

**Note:** Addresses 40h to 7Fh are not defined. All unsupported registers are not writable and will return all zeroes when read. Reserved registers will also return all zeroes when read.

**Vendor ID Register (00h)**  
Read Only

This field identifies the manufacturer of the device. NCR Microelectronic Products Vendor ID is 1000h.

**Device ID (00h)**  
Read Only

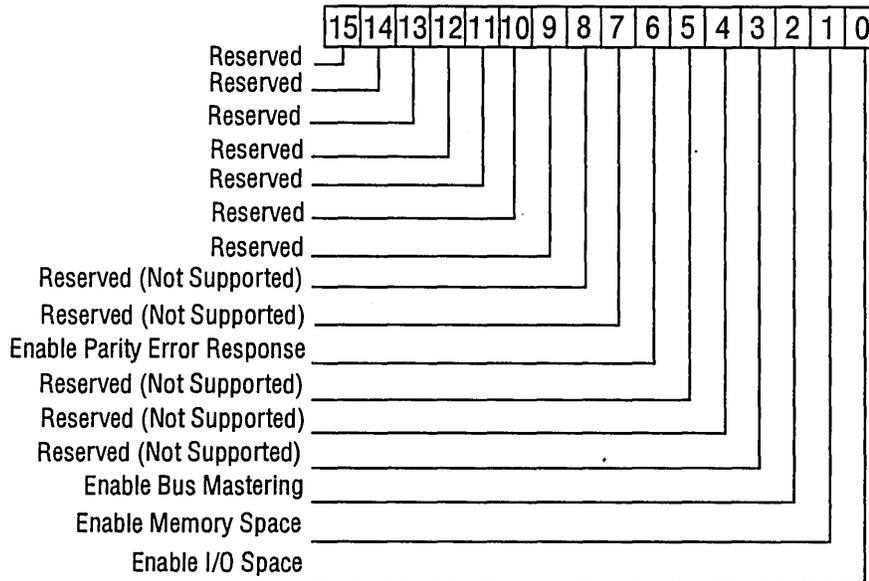
This field identifies the particular device. The 53C810 Device ID is 0001h.

**Command Register (04h)**  
Read/Write

The Command Register (Figure 3-1) provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the 53C810 is logically disconnected from the PCI bus for all accesses except configuration accesses.

In the 53C810 not all the individual bits in the Command Register are implemented. Currently, bits 3 through 5 are not implemented by the 53C810 along with bits 7 through 8. Bits 9 through 15 are reserved. The 53C810 does implement I/O space and thus implements a writable element at bit location (0) of the Command Register.

Figure 3-1. Command Register Layout

**Bits 15-7 Reserved****Bit 6 Enable Parity Error Response**

This bit allows the 53C810 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The 53C810 always generates parity for the PCI bus.

**Bits 5-3 Reserved****Bit 2 Enable Bus Mastering**

This bit controls the 53C810's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI bus master accesses. A value of 1 allows the 53C810 to behave as a bus master.

**Bit 1 Enable Memory Space**

This bit controls the 53C810's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the 53C810 to respond to Memory Space accesses at the address specified by Base Address 1.

**Bit 0 Enable I/O Space**

This bit controls the 53C810's response to I/O space accesses. A value of 0 disables the response. A value of 1 allows the 53C810 to respond to I/O space accesses at the address specified in Base Address 0.

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**Revision ID Register (08h)**  
Read Only

This register specifies a device specific revision identifier. The current value of this register is 00h.

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**Status Register (06h)**  
Read/Write

The Status Register (Figure 3-2) is used to record status information for PCI bus-related events.

In the 53C810, bits 0 through 8 are reserved with bits 11 and 14 not implemented by the 53C810.

Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 8000h to the register.

**Bit 15 Detected Parity Error (from Slave)**

This bit will be set by the device whenever the device detects a data parity error. This bit is disabled when parity error handling is disabled. Devices with a Revision ID register value of 00h do not check or report parity errors if bit 6 is set to 0.

**Bit 14 Reserved**

**Bit 13 Master Abort (from Master)**

This bit should be set by a master device whenever its transaction (except for Special Cycle) is terminated with master-abort. All master devices should implement this bit.

**Bit 12 Received Target Abort (from Master)**

This bit should be set by a master device whenever its transaction is terminated with target-abort. All master devices should implement this bit.

**Bits 10-9 DEVSEL/ Timing**

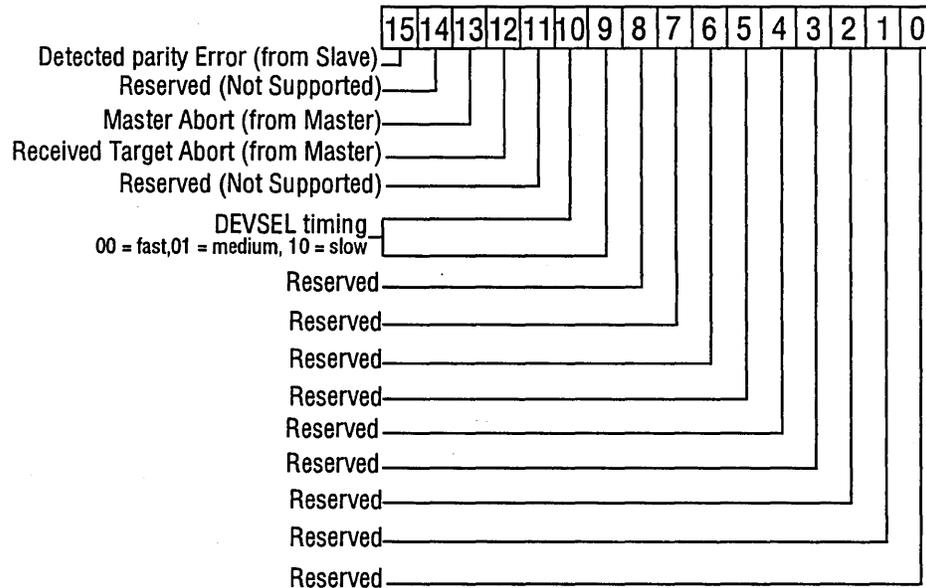
These bits encode the timing of DEVSEL/. These are encoded as 00b for fast, 01b for medium, 10b for slow with 11b reserved. These bits are read-only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. In the 53C810, 01b is supported.

**Bits 8-0 Reserved**

**Latency Timer Register (OCh)**  
Read/Write

The Latency Timer Register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The 53C810 supports this timer. All eight bits are writable, allowing latency values of 0-225 PCI clocks.

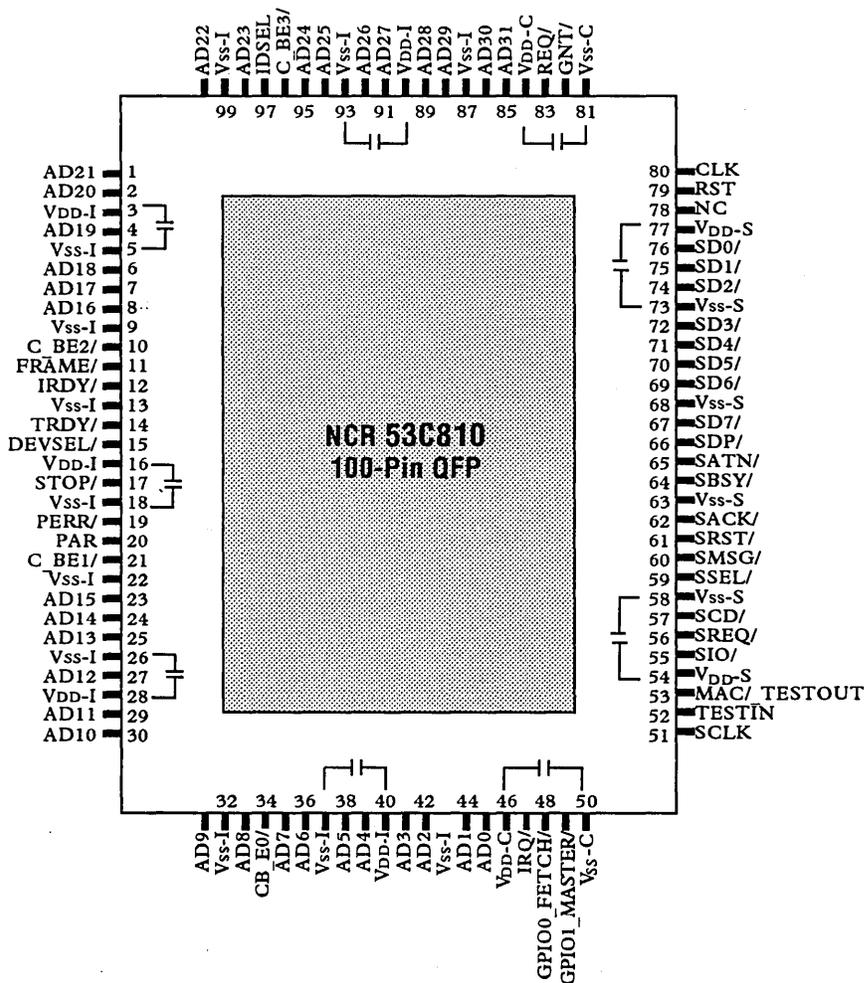
Figure 3-2. Status Register Layout





# Chapter Four Signal Descriptions

Figure 4-1. Pin Diagram



**Note:** The above decoupling capacitor arrangement shown is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 $\mu$ F should provide adequate noise isolation. Because of the number of high current drivers on the 53C810, a multi-layer PC board with power and ground planes is required.

The PCI/SCSI pin definitions are organized into the following functional groups: system, address/data, interface control, arbitration, error reporting, SCSI, and optional interface. A slash (/) at the end of the signal name indicates that the active state occurs when the signal is at a low voltage. When absent, the signal is active at a high voltage.

There are four signal type definitions:

- I        Input, a standard input-only signal
- O        Totem Pole Output, a standard active driver
- T/S     Tri-state, a bi-directional, tri-state input/output pin
- S/T/S   Sustained Tri-state, an active low tri-state signal owned and driven by one and only one agent at a time.

### Power and Ground Pins

Symbol	Pin No	Description
$V_{SS-I}, V_{DD-I}$	3, 5, 9, 13, 16, 18, 22, 26, 28, 32, 37, 40, 43, 87, 90, 93, 99	Power supplies to the PCI I/O pins
$V_{SS-S}, V_{DD-S}$	54, 58, 63, 73, 77	Power supplies to the SCSI bus I/O pins
$V_{SS-C}, V_{DD-C}$	46, 50, 81, 84	Power supplies to the internal logic core

**System Pins**

Symbol	Pin No.	Type	Description
CLK	80	I	Clock provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. This clock can be optionally used as the SCSI core clock; however, fast SCSI transfer rates may not be achieved.
RST	79	I	Reset forces the PCI sequencer of each device to a known state. All <i>t/s</i> and <i>s/t/s</i> signals are forced to a high impedance state, and all internal logic is reset. The RST input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST is active to properly reset the device.

**Address and Data**

Symbol	Pin No.	Type	Description
AD(31-0)	1, 2, 4, 6, 7, 8, 23, 24, 25, 27, 28, 29, 30, 31, 33, 35, 36, 38, 39, 41, 42, 44, 45, 85, 88, 89, 91, 92, 94, 95, 98, 100	T/S	Physical longword address and data are multiplexed on the same PCI pins. During the first clock of a transaction AD (31-0) contain a physical byte address. During subsequent clocks, AD(31-0) contain data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports both read and write bursts. Little Endian byte ordering is used. AD(7-0) define the least significant byte, and AD(31-24) the most significant byte.
C_BE/(3-0)	10, 21, 34, 96	T/S	Bus command and byte enables are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE/(3-0) define the bus command. During the data phase, C_BE/(3-0) are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE/(0) applies to byte 0, and C_BE/(3) to byte 3.
PAR	20	T/S	Parity is the even parity bit that protects the AD(31-0) and C_BE/(3-0) lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

**Interface Control**

Symbol	Pin No.	Type	Description
FRAME/	11	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate a bus transaction is beginning. While FRAME/ is asserted, data transfers continue. When FRAME/ is deasserted, the transaction is in the final data phase or while the bus is idle.
TRDY/	14	S/T/S	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD(31-0). During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
IRDY/	12	S/T/S	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD(31-0). During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	17	S/T/S	Stop indicates the selected target is requesting the master to stop the current transaction.
DEVSEL/	15	S/T/S	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	97	I	Initialization Device Select is used as a chip select in lieu of the upper 24 address lines during configuration read and write transactions.

**Arbitration**

Symbol	Pin No.	Type	Description
REQ/	83	O	Request indicates to the arbiter that this agent desires use of the bus. This is a point-to point signal. Every master has its own REQ/.
GNT/	82	I	Grant indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNT/.

**Error Reporting**

Symbol	Pin No.	Type	Description
PERR/	19	S/T/S	Error may be pulsed active by an agent that detects a parity error. PERR/ can be used by any agent to signal data corruptions. However, on detection of an ERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system will be unable to continue operation once error processing is complete.

**SCSI Signals**

Symbol	Pin No.	Type	Description
SCLK	51	I	SCLK is used to derive all SCSI-related timings. The speed of this clock is determined by the application's requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied low.
SD/ (7-0) SDP	66, 67, 69, 70, 71, 72 74, 75, 76	I/O	SCSI Data includes the following data lines and parity signals: SD7-0 (8-bit SCSI data bus), SDP(SCSI data parity bit).
SCTRL/	55, 56, 57 59, 60, 61 62, 64, 65	I/O	SCSI Control includes the following signals:  CD    SCSI phase line, command/data I_O/    SCSI phase line, input/output MSG/    SCSI phase line, message REQ/    Data handshake signal from target device ACK/    Data handshake signal from initiator device BSY    SCSI bus arbitration signal, busy ATN/    Attention, the initiator is requesting a message-out phase RST/    SCSI bus reset.

**Additional Interface**

Symbol	Pin No.	Type	Description
TESTIN/	52	I	Test In. When this pin is driven low, the 53C810 connects all inputs and outputs to an "AND tree." The SCSI control signals and data lines are not connected to the "AND tree." The output of the "AND tree" is connected to the Test Out pin. This allows manufacturers to verify chip connectivity to the board and to determine exactly which pins are not properly attached. When the TESTIN pin is driven low, internal pullups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be tri-stated, and the MAC/_TESTOUT pin will be enabled. Connectivity can be tested by driving one of the 53C810 pins low. The MAC/_TESTOUT pin should respond by driving low, respectively.
GPIO1_0 FETCH/	48	I/O	General Purpose I/O pin. Optionally, when driven low indicates that the next bus request will be for an Opcode fetch.
GPIO0_1 MASTER/	51	I/O	General purpose I/O pin. Optionally, when driven low indicates that the 53C810 will become bus master.
MAC/ TESTOUT	53	T/S	Memory Access Control. This pin can be programmed to indicate local or system memory accesses (non-PCI applications). It is also used to test the connectivity of the 53C810 signals using an "AND tree" scheme. The MAC/_TESTOUT pin is only driven as the Test Out function when the Test In pin is driven low.
IRQ/	47	0	Interrupt. This signal, when asserted low, indicates that an interrupting condition has occurred and that service is required from the host CPU. The output drive of this pin is programmed as either open drain with an internal weak pullup or optionally as a totem pole driver. Refer to the description of DCNTL Register, Bit 3, for additional information.



## Chapter Five

# Operating Registers

This section contains descriptions of all 53C810 operating registers. Table 5-1 summarizes the 53C810 operating register set. Figure 5-1, the register map, lists registers by operating and configuration addresses. The terms "set" and "assert" are used to refer to bits that are programmed to a binary one. Similarly, the terms "deassert," "clear" and "reset" are used to refer to bits that are programmed to a binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset.

The only register that the host CPU can access while the 53C810 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. However, all operating registers are accessible via SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

Table 5-1. Operating Register Addresses and Descriptions

Memory or I/O	Config Mem/I/O	Read/Write	Label	Description
00	80	R/W	SCNTL0	SCSI Control 0
01	81	R/W	SCNTL1	SCSI Control 1
02	82	R/W	SCNTL2	SCSI Control 2
03	83	R/W	SCNTL3	SCSI Control 3
04	84	R/W	SCID	SCSI Chip ID
05	85	R/W	SXFER	SCSI Transfer
06	86	R/W	SDID	SCSI Destination ID
07	87	R/W	GPREG	General Purpose Bits
08	88	R/W	SFBR	SCSI First Byte Received
09	89	R/W	SOCL	SCSI Output Control Latch
0A	8A	R	SSID	SCSI Selector ID
0B	8B	R/W	SBCL	SCSI Bus Control Lines
0C	8C	R	DSTAT	DMA Status
0D	8D	R	SSTAT0	SCSI Status 0
0E	8E	R	SSTAT1	SCSI Status 1
0F	8F	R	SSTAT2	SCSI Status 2
10-13	90-93	R/W	DSA	Data Structure Address
14	94	R/W	ISTAT	Interrupt Status
18	98	R/W	CTEST0	Chip Test 0
19	99	R	CTEST1	Chip Test 1
1A	9A	R	CTEST2	Chip Test 2
1B	9B	R	CTEST3	Chip Test 3
1C-1F	9C-9F	R/W	TEMP	Temporary Stack

Table 5-1. Operating Register Addresses and Descriptions (Continued)

Memory or I/O	Config Mem/I/O	Read/Write	Label	Description
20	A0	R/W	DFIFO	DMA FIFO
21	A1	R/W	CTEST4	Chip Test 4
22	A2	R/W	CTEST5	Chip Test 5
23	A3	R/W	CTEST6	Chip Test 6
24-26	A4-A6	R/W	DBC	DMA Byte Counter
27	A7	R/W	DCMD	DMA Command
28-2B	A8-AB	R/W	DNAD	DMA Next Address for Data
2C-2F	AC-AF	R/W	DSP	DMA SCRIPTS Pointer
30-33	B0-B3	R/W	DSPS	DMA SCRIPTS Pointer Save
34-37	B4-B7	R/W	SCRATCH A	General Purpose Scratch Pad A
38	B8	R/W	DMODE	DMA Mode
39	B9	R/W	DIEN	DMA Interrupt Enable
3A	BA	R/W	DWT	DMA Watchdog Timer
3B	BB	R/W	DCNTL	DMA Control
3C-3F	BC-BF	R	ADDER	Sum output of internal adder
40	C0	R/W	SIEN0	SCSI Interrupt Enable 0
41	C1	R/W	SIEN1	SCSI Interrupt Enable 1
42	C2	R	SIST0	SCSI Interrupt Status 0
43	C3	R	SIST1	SCSI Interrupt Status 1
44	C4	R/W	SLPAR	SCSI Longitudinal Parity
45	C5		Reserved	
46	C6	R/W	MACNTL	Memory Access Control
47	C7	R/W	GPCNTL	General Purpose Control
48	C8	R/W	STIME0	SCSI Timer 0
49	C9	R/W	STIME1	SCSI Timer 1
4A	CA	R/W	RESPID	Response ID
4B	C7		Reserved	
4C	CC	R	STEST0	SCSI Test 0
4D	CD	R	STEST1	SCSI Test 1
4E	CE	R/W	STEST2	SCSI Test 2
4F	CF	R/W	STEST3	SCSI Test 3
50	D0	R	SIDL	SCSI Input Data Latch
51-53	D1-D3		Reserved	
54	D4	R/W	SODL	SCSI Output Data Latch
55-57	D5-D7		Reserved	
58	D8	R	SBDL	SCSI Bus Data Lines
59-5B	D9-DB		Reserved	
5C-5F	DC-DF	R/W	SCRATCH B	General Purpose Scratch Pad B

Figure 5-1. Register Address Map

				Mem I/O	Config Mem I/O
SCNTL3	SCNTL2	SCNTL1	SCNTL0	00	80
GPREG	SDID	SXFER	SCID	04	84
SBCL	SSID	SOCL	SFBR	08	88
SSTAT2	SSTAT1	SSTAT0	DSTAT	0C	8C
DSA				10	90
RESERVED			ISTAT	14	94
CTEST3	CTEST2	CTEST1	CTEST0	18	98
TEMP				1C	9C
CTEST6	CTEST5	CTEST4	DFIFO	20	A0
DCMD	DBC			24	A4
DNAD				28	A8
DSP				2C	AC
DSPS				30	B0
SCRATCH A				34	B4
DCNTL	DWT	DIEN	DMODE	38	B8
ADDER				3C	BC
SIST1	SIST0	SIEN1	SIEN0	40	C0
GPCNTL	MACNTL	RESERVED	SLPAR	44	C4
RESERVED	RESPID	STIME1	STIME0	48	C8
STEST3	STEST2	STEST1	STEST0	4C	CC
RESERVED			SIDL	50	D0
RESERVED			SODL	54	D4
RESERVED			SBDL	58	D8
SCRATCH B				5C	DC

Register 00 (80)  
SCSI Control Zero (SCNTL0)  
Read/Write

ARB1	ARB0	START	WATN	EPC	RES	AAP	TRG
7	6	5	4	3	2	1	0

Default>>>

1 1 0 0 0 X 0 0

Bit 7 ARB1 (Arbitration mode bit 1)

Bit 6 ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

*Simple Arbitration*

- 1) The 53C810 waits for a bus free condition to occur.
- 2) It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus. If the SEL/ signal is asserted by another SCSI device, the 53C810 will deassert BSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.
- 3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the 53C810 has won arbitration.
- 4) Once the 53C810 has won arbitration, SEL must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 μs) before a low level selection can be performed.

*Full Arbitration, Selection/Reselection*

- 1) The 53C810 waits for a bus free condition.
- 2) It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.
- 3) If the SEL/ signal is asserted by another SCSI device or if the 53C810 detects a higher priority ID, the 53C810 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.
- 4) The 53C810 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.
- 5) The 53C810 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the 53C810's ID (the highest priority ID stored in the SCID register).
- 6) After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.
- 7) If a selection time-out occurs, the Selection Time-out bit is set in the SIST1 register, bit 2.

**Bit 5 START (Start sequence)**

When this bit is set, the 53C810 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected (CON) bit in the SCNTL1 register, bit 4, indicates that 53C810 is already connected to the SCSI bus. This bit is automatically cleared when the

arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the 53C810 did not connect to the SCSI bus.

**Bit 4 WATN (Select with ATN/ on a start sequence)**

When this bit is set and the 53C810 is in initiator mode, the SCSI ATN/ signal will be asserted during 53C810 selection of a target device. This is to inform the target that the 53C810 has a message to send. If a selection time-out occurs while attempting to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted. When this bit is clear, the ATN/ signal will not be asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low level mode.

**Bit 3 EPC (Enable parity checking)**

When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. If a parity error is detected, bit 0 of the SIST0 register is set and an interrupt may be generated.

If the 53C810 is operating in initiator mode and a parity error is detected, ATN/ can optionally be asserted, but the transfer continues until the target changes phase.

When this bit is cleared, parity errors are not reported.

**Bit 2 Reserved**

**Bit 1 AAP (Assert ATN/ on parity error)**

When this bit is set, the 53C810 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the byte

transfer with the parity error. The Enable Parity Checking bit must also be set for the 53C810 to assert ATN/ in this manner. The following parity errors can occur:

- 1) A parity error detected on data received from the SCSI bus.
- 2) A parity error detected on data transferred to the 53C810 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

**Bit 0 TRG (Target mode)**

This bit determines the default operating mode of the 53C810. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target). When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the 53C810 is an initiator device by default.

**CAUTION:** writing this register while not connected may cause the loss of a selection or reselection due to the changing of target or initiator modes.

**Register 01 (81)**  
**SCSI Control One (SCNTL1)**  
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

**Bit 7 EXC (Extra clock cycle of data setup)**

When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time. Setting this bit will only affect SCSI send operations.

**Bit 6 ADB (Assert SCSI data bus)**

When this bit is set, the 53C810 drives the contents of the SCSI Output Data Latch Register (SODL) onto the SCSI data bus. When the 53C810 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the 53C810 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the 53C810 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

**Bit 5 DHP (Disable Halt on Parity Error or ATN) (Target Only)**

The DHP bit is only defined for target mode. When this bit is cleared, the 53C810 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the 53C810 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the

53C810 transfers data until there are no outstanding synchronous offsets. If the 53C810 is receiving data, any data residing in the DMA FIFO is sent to memory before halting.

When this bit is set, the 53C810 does not halt the SCSI transfer when ATN/ or a parity error is received.

**Bit 4 CON (Connected)**

This bit is automatically set any time the 53C810 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C810 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the 53C810 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

**Bit 3 RST (Assert SCSI RST/ signal)**

Setting this bit asserts the SCSI RST/ signal. The RST/ output remains asserted until this bit is cleared. The 25  $\mu$ s minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop.

**Bit 2 AESP (Assert even SCSI parity (force bad parity))**

When this bit is set, the 53C810 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the 53C810. If parity checking is enabled, then the 53C810 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

**Bit 1 IARB (Immediate Arbitration)**

Setting this bit will cause the SCSI core to immediately begin arbitration once a BUS FREE phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration will be re-tried until won. At that point, the 53C810 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2, bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the abort bit in the ISTAT register should be set. Then one of two things will eventually happen:

- 1) The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the 53C810 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.
- 2) The abort will complete because the 53C810 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

**Bit 0 SST (Start SCSI Transfer)**

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

**CAUTION:** Writing to this register while not connected may cause the loss of a selection/reselection by resetting the Connected bit.

**Register 02 (82)**  
**SCSI Control Register Two**  
**(SCNTL2)**  
**Read/Write**

SDU				RESERVED				
7	6	5	4	3	2	1	0	

Default>>>

0 X X X X X X X

**Bit 7 SDU (SCSI Disconnect Unexpected)**

When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2). During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting ACK after receiving a Disconnect command or Command Complete message.

**Bits 6-0 Reserved**

**Register 03 (83)**  
**SCSI Control Three (SCNTL3)**  
**Read/Write**

RES	SCF2-0			RES	CCF2-0		
7	6	5	4	3	2	1	0

Default>>>

X 0 0 0 X 0 0 0

**Bit 7 Reserved**

**Bits 6-4 SCF2-0 (Synchronous Clock Conversion Factor)**

These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. They are encoded as follows. All other combinations are reserved for future expansion and should never be used.

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor Frequency	SCSI Clock (MHz)
0	0	0	SCLK / 3	50.01-75
0	0	1	SCLK / 1	16.67-25
0	1	0	SCLK/1.5	25.01-37.5
0	1	1	SCLK / 2	37.51-50
1	0	0	SCLK / 3	50.01-66
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

**Bit 3 Reserved**

**Bits 2-0 CCF2-0 (Clock Conversion Factor)**

These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as shown in the description of bits 6-4. All other combinations are reserved for future expansion and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above. It is important that these bits be set to the proper values to guarantee that the 53C810 meets the SCSI timings as defined by the ANSI specification.

**Register 04 (84)**  
**SCSI Chip ID (SCID)**  
Read/Write

RES	RRE	SRE	RES	ENC
7	6	5	4	3 2 1 0

Default>>>

X 0 0 X X 0 0 0

**Bit 7 Reserved**

**Bit 6 RRE (Enable Response to Reselection)**

When this bit is set, the 53C810 is enabled to respond to bus-initiated reselection at the chip ID encoded in this register. Note that the 53C810 will not automatically reconfigure itself to initiator mode as a result of being reselected.

**Bit 5 SRE (Enable Response to Selection)**

When this bit is set, the 53C810 is enabled to respond to bus-initiated selection at the chip ID encoded in this register. Note that the 53C810 will not automatically reconfigure itself to target mode as a result of being selected.

**Bits 4-3 Reserved**

**Bits 2-0 Encoded 53C810 Chip SCSI ID, bits 2-0**

These bits are used to store the 53C810 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus, and the ID to which it will respond during bus-initiated selection or reselection. The priority of the eight possible IDs, in descending order is:

---

Highest	Lowest
7 6 5 4 3 2 1 0	

---

**Register 05 (85)**  
**SCSI Transfer (SXFER)**  
Read/Write

	TP2-0		RES		M03-M00		
7	6	5	4	3	2	1	0

Default>>>

0 0 0 X 0 0 0 0

**Note:** When using Table Indirect I/O commands, bits 7-0 of this register will be loaded from the I/O data structure.

**Bits 7-5 TP2-0 (SCSI Synchronous Transfer Period)**

These bits determine the SCSI synchronous transfer period used by the 53C810 when sending synchronous SCSI data in either initiator or target mode.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the 53C810 should use when transferring SCSI data is found as in the following example: The 53C810 is interfaced to a hard disk which can transfer data at 10 MB/s synchronously. The 53C810's SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

$$SXFERP = \text{Period} / \text{SSCP} + \text{ExtCC}$$

$$\text{Period} = 1 \div \text{Frequency} = 1 \div 10 \text{ MB/s} = 100 \text{ ns}$$

$$\text{SSCP} = 1 \div \text{SSCF} = 1 \div 40 \text{ MHz} = 25 \text{ ns}$$

(This SCSI synchronous core clock is determined in SCNTL3 bits 6-4).

ExtCC = 1 if SCNTL1 bit 7 is asserted and the 53C810 is sending data.

(ExtCC = 0 if the 53C810 is receiving data.)

$$SXFERP = 100 \div 25 = 4$$

**Key:** SXFERP = Synchronous transfer period

SSCP = SCSI Synchronous core period

SSCF = SCSI Synchronous core frequency

ExtCC = Extra clock cycle of data setup

**Examples of synchronous transfer periods for SCSI-1 transfer rates.**

CLK (MHz)	SCSI CLK + SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	+3	4	180	5.55
66.67	+3	5	225	4.44
50	+2	4	160	6.25
50	+2	5	200	5
40	+2	4	200	5
37.50	+1.5	4	160	6.25
33.33	+1.5	4	180	5.55
25	+1	4	160	6.25
20	+1	4	200	5
16.67	+1	4	240	4.17

**Example transfer periods for fast SCSI-2 transfer rates.**

CLK (MHz)	SCSI CLK + SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	+1.5	4	90	11.11
66.67	+1.5	5	112.5	8.88
50	+1	4	80	12.5
50	+1	5	100	10.0
40	+1	4	100	10.0
37.50	+1	4	106.67	9.375
33.33	+1	4	120	8.33
25	+1	4	160	6.25
20	+1	4	200	5
16.67	+1	4	240	4.17

**Bit 4 Reserved**

**Bits 3-0 MO3-MO0 (Max SCSI synchronous offset)**

These bits describe the maximum SCSI synchronous offset used by the 53C810 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the 53C810. These bits determine the 53C810's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

M03	M02	M01	M00	Synchronous Offset
0	0	0	0	0 – Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

**Register 06 (86)**  
**SCSI Destination ID (SDID)**  
Read/Write

RESERVED					ENC2-0		
7	6	5	4	3	2	1	0

Default>>>

X X X X X 0 0 0

**Bits 7-3 Reserved**

**Bits 2-0 Encoded destination SCSI ID**

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the eight possible IDs, in descending order, is:

Highest				Lowest			
7	6	5	4	3	2	1	0

**Register 07 (87)**  
General Purpose (GPREG)  
Read/Write

		RESERVED					GPI01	GPI00
7	6	5	4	3	2	1	0	

Default>>>

X X X X X X X X

**Bits 7-2 Reserved**

**Bits 1-0 GPIO1-GPIO0 (General Purpose)**

These bits can be programmed through the GPCNTL Register to become inputs, outputs or special functions. As an output, these pins can be used to drive LEDs or to enable external ROM or RAM. These signals can also be programmed as live inputs and sensed through a SCRIPTS Register to Register Move Instruction. These bits default as inputs and are pulled up internally.

**Register 08 (88)**  
SCSI First Byte Received (SFBR)  
Read/Write

1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

This register contains the first byte received in any asynchronous information transfer phase. For example, when the 53C810 is operating in initiator mode, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C810 register (such as the SCRATCH register), and then to the SFBR.

**Register 09 (89)**  
**SCSI Output Control Latch**  
**(SOCL)**  
 Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>  
 0 0 0 0 0 0 0 0

- Bit 7 REQ (Assert SCSI REQ/ signal)**
- Bit 6 ACK (Assert SCSI ACK/ signal)**
- Bit 5 BSY (Assert SCSI BSY/ signal)**
- Bit 4 SEL (Assert SCSI SEL/ signal)**
- Bit 3 ATN (Assert SCSI ATN/ signal)**
- Bit 2 MSG (Assert SCSI MSG/ signal)**
- Bit 1 C/D (Assert SCSI C/D/ signal)**
- Bit 0 I/O - (Assert SCSI I/O/ signal)**

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the 53C810 starts executing normal SCSI SCRIPTS, as it may cause violation of the SCSI protocol.

**Register 0A (09)**  
**SCSI Selector ID Register (SSID)**  
 Read Only

VAL	RESERVED			ENCID2-0			
7	6	5	4	3	2	1	0

Default>>>  
 0 X X X X 0 0 0

**Bit 7 VAL (SCSI Valid Bit)**

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

**Bits 6-3 Reserved**

**Bits 2-0 Encoded Destination SCSI ID**

Reading the SSID register immediately after the 53C810 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets which are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

**Register 0B (8B)**  
**SCSI Bus Control Lines (SBCL)**  
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>

X X X X X X X X

- Bit 7 REQ (REQ/ status)**
- Bit 6 ACK (ACK/ status)**
- Bit 5 BSY (BSY/ status)**
- Bit 4 SEL (SEL/ status)**
- Bit 3 ATN (ATN/ status)**
- Bit 2 MSG (MSG/ status)**
- Bit 1 C/D (C\_D/ status)**
- Bit 0 I/O (I\_O/ status)**

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. The resulting read data is synchronized before being presented to the PCI bus to prevent parity errors. This register can be used for diagnostics testing or operation in low level mode.

**Register 0C (8C)**  
**DMA Status (DSTAT)**  
Read Only

DFE	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0

Default>>>

1 0 0 0 0 0 X 0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C810 stacks interrupts). The DIP bit in the ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure that the interrupts clear properly. Also, if reading any of the registers when the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

**Bit 7 DFE (DMA FIFO empty)**

This status bit is set when the DMA FIFO is empty. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

**Bit 6 MDPE (Master Data Parity Error)**

This bit is set when the 53C810 as a master detects that a target device has signalled a parity error during a data phase. This bit is completely disabled by Master Parity Error Enable (bit 3 of CTEST4).

**Bit 5 BF (Bus fault)**

This bit is set when a PCI bus fault condition is detected. A PCI bus fault can only occur when the 53C810 is bus master, and is defined as a cycle that ends with a Bad Address or Target Abort Condition.

**Bit 4 ABRT (Aborted)**

This bit is set when an abort condition occurs. An abort condition occurs when a software abort command is issued by setting bit 7 of the ISTAT register.

**Bit 3 SSI (Single step interrupt)**

If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPTS instruction.

**Bit 2 SIR (SCRIPTS interrupt instruction received)**

This status bit is set whenever an Interrupt instruction is evaluated as true.

**Bit 1 Reserved****Bit 0 IID (Illegal instruction detected)**

This status bit will be set any time an illegal instruction is detected, whether the 53C810 is operating in single-step mode or automatically executing SCSI SCRIPTS. This bit will also be set if the 53C810 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

**Register 0D (8D)****SCSI Status Zero (SSTAT0)**

Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST	SDP
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

**Bit 7 ILF (SIDL full)**

This bit is set when the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

**Bit 6 ORF (SODR full)**

This bit is set when the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user (cannot be read or written). This bit can be used to determine how many bytes reside in the chip when an error occurs.

**Bit 5 OLF (SODL full)**

This bit is set when the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

**Bit 4 AIP (Arbitration in progress)**

Arbitration in Progress (AIP = 1) indicates that the 53C810 has detected a bus free condition, asserted BSY and asserted its SCSI ID onto the SCSI bus.

**Bit 3 LOA (Lost arbitration)**

When set, LOA indicates that the 53C810 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

**Bit 2 WOA (Won arbitration)**

When set, WOA indicates that the 53C810 has detected a bus free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

**Bit 1 RST (SCSI reset signal)**

This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the ISTAT register.

**Bit 0 SDP (SCSI parity signal)**

This bit represents the active high current status of the SCSI SDP/ parity signal.

**Register 0E (8E)**

**SCSI Status One (SSTAT1)**

Read Only

FF3	FF2	FF1	FF0	SDPL	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	X	X	X	X
---	---	---	---	---	---	---	---

**Bits 7-4 FF3-FF0 (FIFO flags)**

FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

These four bits define the number of bytes or words that currently reside in the 53C810's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only 9 bytes deep, values over 9 will not occur.

**Bit 3 SDPL (Latched SCSI parity)**

This bit reflects the SCSI parity signal (SDP/), corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register.

This bit is active high, i.e., it is set when the parity signal is active.

**Bit 2 MSG (SCSI MSG/ signal)**

**Bit 1 C/D (SCSI C\_D/ signal)**

**Bit 0 I/O (SCSI I\_O/ signal)**

These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

**Register 0F (8F)**  
**SCSI Status Two (SSTAT2)**  
(Read Only)

RESERVED						LDSC	RES
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	1	X

**Bits 7-2 Reserved**

**Bit 1 LDSC (Last Disconnect)**

Used in conjunction with the Connected (CON) bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects the 53C810. If the CON bit is asserted and the LDSC bit is asserted, a disconnect has occurred.

**Bit 0 Reserved**

**Registers 10-13 (90-93)**  
**Data Structure Address (DSA)**  
Read/Write

This 32-bit register contains the base address used for all table indirect calculations. The DSA register is usually loaded prior to starting an I/O, but it is possible for a SCRIPTS Memory Move to load the DSA during the I/O.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

**Register 14 (94)**  
**Interrupt Status (ISTAT)**  
(Read/Write)

ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the 53C810 is executing SCRIPTS (without interfering in the operation of the 53C810). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

**Bit 7 ABRT (Abort operation)**

Setting this bit aborts the current operation being executed by the 53C810. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

- 1) Set this bit.
- 2) Wait for an interrupt.
- 3) Read the ISTAT register.
- 4) If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2.
- 5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register.
- 6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

**Bit 6 SRST (Software reset)**

Setting this bit resets the 53C810. All operating registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This reset

will not clear the ID Mode bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).

**Bit 5 SIGP (Signal process)**

SIGP is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.

**Bit 4 SEM (Semaphore)**

This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the 53C810 is executing a SCRIPTS. This bit enables the 53C810 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the 53C810 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

**Bit 3 CON (Connected)**

This bit is automatically set any time the 53C810 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C810 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the 53C810 is not connected to the SCSI bus.

**Bit 2 INTF (Interrupt on the Fly)**

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. If this bit is set, when the ISTAT register is read it will not automatically be cleared. To clear this bit, it must be written to a one. The reset operation is self-clearing. **Note:** If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers.

**Bit 1 SIP (SCSI interrupt pending)**

This status bit is set when an interrupt condition is detected in the SCSI portion of the 53C810. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence complete
- A selection or reselection time-out occurs
- The 53C810 was selected
- The 53C810 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- A selection/reselection time-out occurs
- The handshake-to-handshake timer is expired
- The general purpose timer is expired.

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read.

**Bit 0 DIP (DMA interrupt pending)**

This status bit is set when an interrupt condition is detected in the DMA portion of the 53C810. The following conditions will cause a DMA interrupt to occur:

- A PCI parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- An illegal instruction is detected.

To determine exactly which condition(s) caused the interrupt, the DSTAT register should be read.

**Register 18 (98)**  
**Chip Test Zero (CTEST0)**  
Read/Write

CTEST0 is a general purpose, user-definable read/write register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero.

**Register 19 (91)**  
**Chip Test One (CTEST1)**  
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
7	6	5	4	3	2	1	0

Default >>>

1 1 1 1 0 0 0 0

**Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)**

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

**Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)**

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

**Register 1A (9A)****Chip Test Two (CTEST2)**

Read Only

DDIR	SIGP	CIO	CM	RES	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0

Default&gt;&gt;&gt;

0 0 X X 0 0 0 1

**Bit 7 DDIR (Data Transfer Direction)**

This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

**Bit 6 SIGP (Signal process)**

This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS. When this register is read, the SIGP bit in the ISTAT register is cleared.

**Bit 5 CIO (Configured as I/O)**

This bit is defined as the Configuration I/O Enable Status bit. This read-only bit indicates if the chip is currently enabled as I/O space.

**Note:** both bits 4 and 5 may be set if the chip is dual-mapped.

**Bit 4 CM (Configured as Memory)**

This bit is defined as the Configuration Memory enable status bit. This read-only bit indicates if the chip is currently enabled as memory space.

**Note:** both bits 4 and 5 may be set if the chip is dual-mapped.

**Bit 3 Reserved****Bit 2 TEOP (SCSI true end of process)**

This bit indicates the status of the 53C810's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the 53C810. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

**Bit 1 DREQ (Data request status)**

This bit indicates the status of the 53C810's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

**Bit 0 DACK (Data acknowledge status)**

This bit indicates the status of the 53C810's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

**Register 1B (9B)**  
**Chip Test Three (CTEST3)**  
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	RES
7	6	5	4	3	2	1	0

Default>>>

X X X X 0 0 0 X

**Bits 7-4 V3-V0 (Chip revision level)**

These bits identify the chip revision level for software purposes. This data manual applies to devices with revision level 0.

**Bit 3 FLF (Flush DMA FIFO)**

When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the 53C810 has successfully transferred the data, this bit should be reset.

**Note:** Polling of FIFO flags is allowed during flush operations.

**Bit 2 CLF (Clear DMA and SCSI FIFOs)**

When this bit is set, all data pointers for the SCSI and DMA FIFOs are cleared. In addition to the SCSI and DMA FIFO pointers, the SIDL, SODL, and SODR least and most significant byte full bits in the SSTAT0 and SSTAT2 registers are cleared. Any data in either of the FIFOs is lost. This bit automatically resets after the 53C810 has successfully cleared the appropriate FIFO pointers and registers.

**Note:** This bit does not clear the data visible at the bottom of the FIFOs.

**Bit 1 FM (Fetch pin mode)**

When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the opcode portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

**Bit 0 Reserved**

**Registers 1C-1F (9C-9F)**  
**Temporary Stack (TEMP)**  
 Read/Write

This 32-bit register stores the RETURN instruction address pointer from the CALL instruction. The address pointer stored in this register is loaded into the DSP register when a RETURN instruction is executed. This address points to the next instruction to be executed.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

**Register 20 (A0)**  
**DMA FIFO (DFIFO)**  
 Read/Write

RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0

Default>>>

X 0 0 0 0 0 0 0

**Bit 7 Reserved**

**Bits 6-0 BO6-BO0 (Byte offset counter)**

These six bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

- 1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register
- 2) AND the result with 7Fh for a byte count between zero and 64

**Note:** If trying to calculate the total number of bytes in both the DMA FIFO and SCSI logic, see the section on Data Paths in Chapter Two, *Functional Description*.

**Register 21 (A1)**  
**Chip Test Four (CTEST4)**  
Read/Write

BDIS	ZMOD	ZSD	SRTM	MPEE	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

**Bit 7 BDIS (Burst Disable)**

When set, this bit will cause the 53C810 to perform back to back cycles for all transfers. When reset, the 53C810 will perform back to back transfers for opcode fetches and burst transfers for data moves

**Bit 6 ZMOD (High impedance mode)**

Setting this bit causes the 53C810 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the 53C810, this bit must be cleared. This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a crash.

**Bit 5 ZSD (SCSI High Impedance Mode)**

Setting this bit causes the 53C810 to place the SCSI data bus SD and the parity line SDP in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

**Bit 4 SRTM (Shadow Register Test Mode)**

Asserting this bit allows access to the shadow registers used by memory-to-memory Move operations. When this bit is set, register accesses to the TEMP and DSA registers are directed to the shadow copies STEMP and SDSA. This bit is intended for manufacturing diagnostics and therefore should not be set during normal operations.

**Bit 3 MPEE (Master Parity Error Enable)**

Asserting this bit enables parity checking during master address or data phases. When this bit is reset, the 53C810 will not interrupt if a master parity error occurs. This bit is reset at power up.

**Bits 2-0 FBL2-FBL0 (FIFO byte control)**

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits steer the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. When cleared, the byte lane read or written is determined by the current contents of the DNAD and DBC registers. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

**Register 22 (A2)****Chip Test Five (CTEST5)**

Read/Write

ADCK	BBCK	RES	MASR	DDIR	RESERVED		
7	6	5	4	3	2	1	0

Default&gt;&gt;&gt;

0 0 X 0 0 X X X

**Bit 7 ADCK (Clock address incrementor)**

Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

**Bit 6 BBCK (Clock byte counter)**

Setting this bit decrements the byte count contained in the DBC register. The DBC register supports only 24 bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

**Bit 5 Reserved****Bit 4 MASR (Master control for set or reset pulses)**

This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

**Bit 3 DDIR (DMA direction)**

Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

**Bits 2-0 Reserved****Register 23 (A3)****Chip Test Six (CTEST6)**

Read/Write

DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
7	6	5	4	3	2	1	0

Default&gt;&gt;&gt;

0 0 0 0 0 0 0 0

**Bits 7-0 DF7-DF0 (DMA FIFO)**

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS operation. This register should only be written when testing the DMA FIFO using the CTEST4 register. Writes to this register while the test mode is not enabled will have unexpected results.

**Registers 24-26 (A4-A6)**  
**DMA Byte Counter (DBC)**  
Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the 53C810. The DBC counter is decremented each time that data is validly transferred on the PCI bus. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if not a target mode command phase.

The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value. The power-up value of this register is indeterminate.

**Register 27 (A7)**  
**DMA Command (DCMD)**  
Read/Write

DMA Command							
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This 8-bit register determines the instruction for the 53C810 to execute. This register has a different format for each instruction.

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**Registers 28-2B (A8-AB)**  
**DMA Next Data Address (DNAD)**  
Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions. The default value of this register is zero.

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**Registers 2C-2F (AC-AF)**  
**DMA SCRIPTS Pointer (DSP)**  
Read/Write

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPTS must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a single step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPTS. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS. The default value of this register is zero.

---

Registers 30-33 (B0-B3)  
DMA SCRIPTS Pointer Save  
(DSPS)  
Read/Write

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt is fetched, this register holds the interrupt vector. The power-up value of this register is indeterminate.

---

Registers 34-37 (B4-B7)  
Scratch Register A (SCRATCH A)  
Read/Write

This is a general purpose user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The power-up value of this register is indeterminate.

**Register 38 (B8)**  
**DMA Mode (DMODE)**  
 Read/Write

BL1	BL0	SIOM	DIOM	ER	RES		MAN
7	6	5	4	3	2	1	0

Default&gt;&gt;&gt;

0	0	0	0	0	X	X	0
---	---	---	---	---	---	---	---

**Bit 7-6 BL1-BL0 (Burst length)**

BL1	BL0	Burst Length
0	0	2- transfer burst
0	1	4- transfer burst
1	0	8-transfer burst
1	1	16-transfer burst

These bits control the maximum number of bus cycles performed per bus ownership. The 53C810 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. The 53C810 inserts a "fairness delay" of four CLKs between bus ownerships during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

**Bit 5 SIOM (Source I/O-Memory Enable)**

This bit is defined as an I/O Memory Enable bit for the source address of a Memory Move or Block Move Command. If this bit is set, then the source address is in I/O space; and if reset, then the source address is in memory space.

**Bit 4 DIOM (Destination I/O-Memory Enable)**

This bit is defined as a I/O Memory Enable bit for the destination address of a Memory Move or Block Move Command. If this bit is set, then the destination address is in I/O space; and if reset, then the destination address is in memory space.

**Bit 3 Enable Read Line**

This bit is defined to enable a read line command. If this bit is set and the chip is about to execute a read cycle other than an opcode fetch, then the command will be 1110.

**Bits 2-1 Reserved****Bit 0 MAN (Manual Start Mode)**

Setting this bit prevents the 53C810 from automatically fetching and executing SCSI SCRIPTS when the DSP register is written. When this bit is set, the Start DMA bit in the DCNTL register must be set to begin SCRIPT execution. Clearing this bit causes the 53C810 to automatically begin fetching and executing SCSI SCRIPTS when the DSP register is written. This bit is intended for manufacturing diagnosis and should not be set during normal operations.

**Register 39 (B9)**  
**DMA Interrupt Enable (DIEN)**  
Read/Write

RES	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0

Default>>>

X 0 0 0 0 0 X 0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the ISTAT DIP from being set; all DMA interrupts are considered fatal. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt. A masked or non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set. The 53C810 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

- Bit 7 Reserved**
- Bit 6 MDPE (Master Data Parity Error)**
- Bit 5 BF (Bus fault)**
- Bit 4 ABRT (Aborted)**
- Bit 3 SSI (Single step interrupt)**
- Bit 2 SIR (SCRIPTS interrupt instruction received)**
- Bit 1 Reserved**
- Bit 0 IID (Illegal instruction detected)**

**Register 3A (BA)**  
**DMA Watchdog Timer (DWT)**  
Read/Write

This is a general purpose register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero.

**Register 3B (BB)**  
**DMA Control (DCNTL)**  
 Read/Write

RESERVED			SSM	IRQM	STD	SA	COM
7	6	5	4	3	2	1	0
X	X	X	0	0	0	0	0

Default>>>

X X X 0 0 0 0 0

**Bits 7-5 Reserved**

**Bit 4 SSM (Single-step mode)**

Setting this bit causes the 53C810 to stop after executing each SCRIPTS instruction, and generate a single step interrupt. When this bit is clear the 53C810 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the 53C810 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

**Bit 3 IRQM (IRQ Mode)**

When set, this bit will enable a totem pole driver for the IRQ pin. When reset, this bit will enable an open drain driver for the IRQ pin with a internal weak pullup. This bit is reset at power up.

**Bit 2 STD (Start DMA operation)**

The 53C810 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the 53C810 is in one of the following modes:

- 1) *Manual start mode* – Bit 0 in the DMODE register is set
- 2) *Single-step mode* – Bit 4 in the DCNTL register is set

When the 53C810 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the 53C810 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

**Bit 1 SA (Same Agent)**

When set, this bit will not add an extra clock cycle between back-to-back PCI write cycles. When reset, this bit will add an extra clock cycle between back-to-back PCI write cycles. This bit is reset at power up.

**Bit 0 COM (53C700 compatibility)**

When this bit is clear, the 53C810 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten should a selection/reselection occur during a DMA register-to-register operation. The default condition of this bit (clear) causes the 53C810 to act the same as the 53C700, which does not support register-to-register operation.

**Register 3C-3F (BC-BF)**  
Adder Sum Output (ADDER)  
Read Only

This register contains the output of the internal adder, and is used primarily for test purposes. The power-up value for this register is indeterminate.

**Register 40 (C0)**  
SCSI Interrupt Enable Zero (SIEN0)  
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL, RSL, CMP, and ATN/ in target mode). Setting a mask bit un masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP is set.

The 53C810 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the ISTAT SIP bit to clear and allow pending interrupts to fall through (interrupt stacking will be disabled).

**Bit 7 M/A ( SCSI Phase Mismatch - Initiator Mode SCSI ATN Condition - Target Mode )**

In initiator mode, the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by the SCSI transfer SCRIPTS. In target mode, the initiator has asserted ATN/.

See the Disable halt on parity error or ATN condition bit in the SCNTL1 register for more information on when this status is actually raised.

**Bit 6 CMP (Function Complete)**

Full arbitration and selection sequence has completed.

**Bit 5 SEL (Selected)**

The 53C810 has been selected by a SCSI target device. The Enable Response to Selection bit in the SCID register must be set for this to occur.

**Bit 4 RSL (Reselected)**

The 53C810 has been reselected by a SCSI initiator device. The Enable Response to Reselection bit in the SCID register must be set for this to occur.

**Bit 3 SGE (SCSI Gross Error)**

The following conditions are considered SCSI Gross Errors:

- 1) Data underflow: the SCSI FIFO was read when no data was present.
- 2) Data overflow: the SCSI FIFO was written to while full.
- 3) Offset underflow: in target mode, an ACK pulse was received before the corresponding REQ was sent.
- 4) Offset overflow: in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.
- 5) In initiator mode, a phase change occurred with an outstanding REQ/ACK offset.
- 6) Residual data in SCSI FIFO: a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

**Bit 2 UDC (Unexpected Disconnect)**

This condition only occurs in initiator mode. It happens when the target to which the 53C810 is connected disconnects from the

SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

**Bit 1 RST (SCSI Reset Condition)**

The SCSI RST signal has been asserted by the 53C810 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single RST pulse.

**Bit 0 PAR (SCSI Parity Error)**

The 53C810 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

**Register 41 (C1)**  
**SCSI Interrupt Enable One**  
**(SIEN1)**  
Read/Write

RESERVED					STO	GEN	HTH
7	6	5	4	3	2	1	0

Default>>>

X X X X X 0 0 0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST1 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST1 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set. Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT DIP or SIP bit is set.

The 53C810 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the ISTAT SIP bit to clear and allow pending interrupts to fall through (interrupt stacking will be disabled).

**Bits 7-3 Reserved**

**Bit 2 STO (Selection or Reselection Time-out)**

The SCSI device which the 53C810 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register bits 3-0 for more information on the time-out timer.

**Bit 1 GEN (General Purpose Timer Expired)**

The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

**Bit 0 HTH (Handshake to Handshake timer Expired)**

The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

**Register 42 (C2)**  
**SCSI Interrupt Status Zero**  
**(SIST0)**  
**Read Only**

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit asserted indicates that the corresponding condition has occurred. Reading a bit in SIST0 will reset the selected conditions.

Reading this register will clear any bits that are not set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C810 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt.

**Bit 7 M/A (Initiator Mode: Phase Mismatch;  
 Target Mode: ATN/ Active)**

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode.

**Bit 6 CMP (Function Complete)**

This bit is set when an arbitration only or full arbitration sequence has completed.

**Bit 5 SEL (Selected)**

This bit is set when the 53C810 is selected by another SCSI device. The Enable Response to Selection bit must have been set in the SCID register for the 53C810 to respond to selection attempts.

**Bit 4 RSL (Reselected)**

This bit is set when the 53C810 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register for the 53C810 to respond to reselection attempts.

**Bit 3 SGE (SCSI Gross Error)**

This bit is set when the 53C810 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

- 1) Data Underflow - the SCSI FIFO register was read when no data was present.
- 2) Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
- 3) Offset Underflow - the 53C810 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.
- 4) Offset Overflow - the other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.
- 5) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.
- 6) A phase change occurred with an outstanding synchronous offset when the 53C810 was operating as an initiator.

**Bit 2 UDC (Unexpected Disconnect)**

This bit is set when the 53C810 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the 53C810 operates in the initiator mode. When the 53C810 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect. This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt).

**Bit 1 RST (SCSI RST/ Received)**

This bit is set when the 53C810 detects an active RST/ signal, whether the reset was generated external to the chip or caused by the Assert RST/ bit in the SCNTL1 register. This 53C810 SCSI reset detection logic is edge-sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

**Bit 0 PAR (Parity Error)**

This bit is set when the 53C810 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register.

**Register 43 (C3)**

**SCSI Interrupt Status One (SIST1)  
Read Only**

RESERVED					STO	GEN	HTH
7	6	5	4	3	2	1	0

Default>>>

X X X X X 0 0 0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is asserted indicates that the corresponding condition has occurred.

Reading a bit in SIST1 will reset the selected conditions.

**Bits 7-3 Reserved**

**Bit 2 STO (Selection or Reselection Time-out)**

The SCSI device which the 53C810 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register, bits 3-0, for more information on the time-out timer.

**Bit 1 GEN ( General Purpose Timer Expired)**

The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

**Bit 0 HTH (Handshake to Handshake timer Expired)**

The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

### Register 44 (C4) SCSI Longitudinal Parity (SLPAR) Read/Write

This register performs a bitwise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data Bytes	Running SLPAR
—	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3)
	Even Parity >>>10010110
4. 10010110	00000000

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

**Note:** Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances. The default value of this register is zero.

### Register 46 (C6) Memory Access Control (MACNTL) Read/Write

7	6	5	4	3	2	1	0
RES							
DWR							
DRD							
PSCPT							
SCPTS							
Default>>>							
X	X	X	X	0	0	0	0

This register is used to determine if an external access is to local or far memory. When setting bits 3 through 0, the access is considered local.

#### Bits 7-4 Reserved

#### Bit 3 DWR (DataWR)

This bit is used to define if a data write is considered local memory access.

#### Bit 2 DRD (DataRD)

This bit is used to define if a data read or a pointer to a SCRIPTS fetch is considered local memory access.

#### Bit 1 PSCPT (Pointer SCRIPTS)

This bit is used to define if a pointer to a SCRIPTS fetch is considered local memory access.

#### Bit 0 SCPTS (SCRIPTS)

This bit is used to define if a pointer to a SCRIPTS fetch is considered local memory access.

**Register 47 (C7)**  
**General Purpose Pin Control**  
**(GPCNTL)**  
Read/Write

ME	FE		RESERVED			GPIO1	GPIO0
7	6	5	4	3	2	1	0

Default>>>

0 0 X X X X 1 1

This register is used to determine if the pins controlled by the General Purpose register (GPREG) are inputs or outputs. Bits 1-0 in GPCNTL correspond to bits in the GPREG register. When the bits are enabled as inputs, an internal pull-up is also enabled.

**Bit 7 Master Enable**

The internal bus master signal will be presented on GPIO1 if this bit is set, regardless of the state of Bit 1 (GPIO1\_EN).

**Bit 6 Fetch Enable**

The internal Opcode Fetch signal will be presented on GPIO0 if this bit is set, regardless of the state of Bit 0 (GPIO0\_EN).

**Bits 5-2 Reserved**

**Bit 1 GPIO1\_EN (GPIO1 Enable)**

This bit powers up set, causing the GPIO1 to become an input. Resetting this bit causes GPIO1 to become an output.

**Bit 0 GPIO0\_EN (GPIO0 Enable)**

This bit powers up set, causing the GPIO0 to become an input. Resetting this bit causes GPIO0 to become an output.

**Register 48 (C8)**  
**SCSI Timer Register Zero**  
**(STIME0)**  
Read /Write

	HTH				SEL		
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

**Bits 7-4 HTH (Handshake -to-Handshake Timer Period)**

These bits select Handshake-to-Handshake Time-out Period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set, and an interrupt is optionally generated, if bit 0 in the SIEN1 register is set. The following table applies to the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits 3-0), and the General Purpose Timer (STIME1 bits 3-0).

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out
0000	Disabled
0001	100 µs
0010	200 µs
0011	400 µs
0100	800 µs
0101	1.6 ms
0110	3.2 ms
0111	6.4 ms
1000	12.8 ms
1001	25.6 ms
1010	51.2 ms
1011	102.4 ms
1100	204.8 ms
1101	409.6 ms
1110	819.2 ms
1111	1.6+ sec

**Bits 3-0 SEL (Selection Time-Out)**

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200  $\mu$ s selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set.

**Register 49 (C9)**  
**SCSI Timer Register One**  
**(STIME1)**  
Read/Write

RESERVED				GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0

Default>>>

X X X X 0 0 0 0

**Bits 7-4 Reserved**

**Bits 3-0 GEN3-0 (General Purpose Timer Period)**

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set and an interrupt is optionally generated, if bit 1 in the SIEN1 register is set. Refer to the table under STIME0, bits 3-0, for the available time-out periods.

**Note:** to reset a timer before it has expired and obtain repeatable delays, the time value must be written to zero first, and then written back to the desired value. This is also required when changing from one time value to another.

**Register 4A (CA)**  
Response ID Zero (RESPID)  
Read/Write

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

This register contains the selection or reselection IDs. This register contains the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit representing ID 7 and the least significant bit representing ID0. The 53C810 can respond to more than one ID because more than one bit can be set in the RESPID register. However, the 53C810 will arbitrate with only the ID value in the SCID register.

**Register 4C (CC)**  
SCSI Test Register Zero (STEST0)  
Read Only

	RESERVED				SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0	

Default>>>

X X X X 0 X 1 1

**Bits 7-4 Reserved**

**Bit 3 SLT (Selection Response Logic Test)**

This bit is asserted when the 53C810 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

**Bit 2 ART (Arbitration Priority Encoder Test)**

This bit will always be asserted when the 53C810 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the 53C810 has won arbitration.

**Bit 1 SOZ (SCSI Synchronous Offset Zero)**

This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the 53C810, as an initiator, is waiting for the target to request data transfers. If the 53C810 is a target then the initiator has sent the offset number of acknowledges.

**Bit 0 SOM (SCSI Synchronous Offset Maximum)**

This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set the 53C810, as a target, is waiting for the initiator to acknowledge the data transfers. If the 53C810 is an initiator then the target has sent the offset number of requests.

**Register 4D (CD)**  
**SCSI Test Register One (STEST1)**  
 Read Only

SCLK				RESERVED				
7	6	5	4	3	2	1	0	

Default&gt;&gt;&gt;

0 X X X X X X X

**Bit 7 SCLK**

This bit, when set, will disable the external SCLK (SCSI Clock) pin, and the chip will use the DMA clock as the internal SCSI clock. If a transfer rate of 10 MB/s is to be achieved on the SCSI bus, this bit must be reset and at least a 40 MHz external SCLK must be provided.

**Bits 6-0 Reserved**

**Register 4E (CE)**  
**SCSI Test Register Two (STEST2)**  
 Read/Write

SCE	ROF	RES	SLB	SZM	RES	EXT	LOW
7	6	5	4	3	2	1	0

Default&gt;&gt;&gt;

0 0 X 0 0 0 0 0

**Bit 7 SCE (SCSI Control Enable)**

This bit, when set, allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the 53C810 is configured as a target or initiator.

**Note:** This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

**Bit 6 ROF (Reset SCSI Offset)**

Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

**Bit 5 Reserved****Bit 4 SLB (SCSI Loopback Mode)**

Setting this bit allows the 53C810 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

**Bit 3 SZM (SCSI High-Impedance Mode)**

Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

**Bit 2 Reserved**

**Bit 1 EXT (Extend REQ/ACK Filtering)**

The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which will cause glitches on deasserting edges to be disregarded. Asserting this bit will provide additional filtering on the deasserting edge of the REQ/ and ACK/ signals.

**Note:** This bit must never be set during fast SCSI (greater than 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

**Bit 0 LOW (SCSI Low level Mode)**

Setting this bit places the 53C810 in low level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

**Note:** It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers)

**Register 4F (CF)**  
**SCSI Test Register Three**  
**(STEST3)**  
**Read/Write**

EAN	STR	HSC	DSI	RES	TTM	CSF	STW
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 X 0 0 0

**Bit 7 EAN (Enable Active Negation)**

Asserting this bit enables the active negation portion of NCR TolerANT technology. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively deasserted, instead of relying on external pull-ups, when the 53C810 is driving these signals. Active deassertion of these signals will occur only when the 53C810 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active negation should be enabled to improve setup and deassertion times. Active negation is disabled after reset or when this bit is cleared. For more information on NCR TolerANT technology, refer to Chapter One, *Introduction*.

**Bit 6 STR (SCSI FIFO Test Read)**

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the SODL register will cause the FIFO to unload.

**Bit 5 HSC (Halt SCSI Clock)**

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower  $I_{DD}$  during a power down mode.

**Bit 4 DSI (Disable Single Initiator Response)**

If this bit is set, the 53C810 will ignore all bus-initiated selection attempts which employ the single-initiator option from SCSI-1. In order to select the 53C810 while this bit is set, the 53C810's SCSI ID and the initiator's SCSI ID

must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.

**Bit 3 Reserved**

**Bit 2 TTM (Timer Test Mode)**

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the 53C810 will generate interrupts at time-out.

**Bit 1 CSF (Clear SCSI FIFO)**

Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting.

**Bit 0 STW (SCSI FIFO Test Write)**

Setting this bit places the SCSI core FIFO into a test mode in which the SCSI FIFO can easily be written. Writing a byte to the SODL register will load the SCSI FIFO.

**Register 50 (D0)**

**SCSI Input Data Latch (SIDL)**

Read Only

This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the 53C810 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid. The power-up values are indeterminate.

**Register 54 (D4)**  
**SCSI Output Data Latch (SODL)**  
**Read/Write**

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip. The power-up value of this register is indeterminate.

**Registers 58 (D8)**  
**SCSI Bus Data Lines (SBDL)**  
**Read Only**

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode. The power-up value of this register is indeterminate.

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**Registers 5C-5F (DC-DF)**  
**Scratch Register B (SCRATCHB)**  
(Read/Write)

This is a general purpose user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCH register will alter its contents. The power-up values are indeterminate.



## Chapter Six

# Instruction Set of the I/O Processor

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## SCSI SCRIPTS

After power up and initialization of the 53C810, the chip may be operated in one of two modes:

- 1) Low level register interface; or
- 2) SCSI SCRIPTS mode.

In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like an NCR 53C80. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the 53C810 requires only a SCRIPTS start address. All commands are fetched from local or external memory. The 53C810 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the 53C810 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the 53C810 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

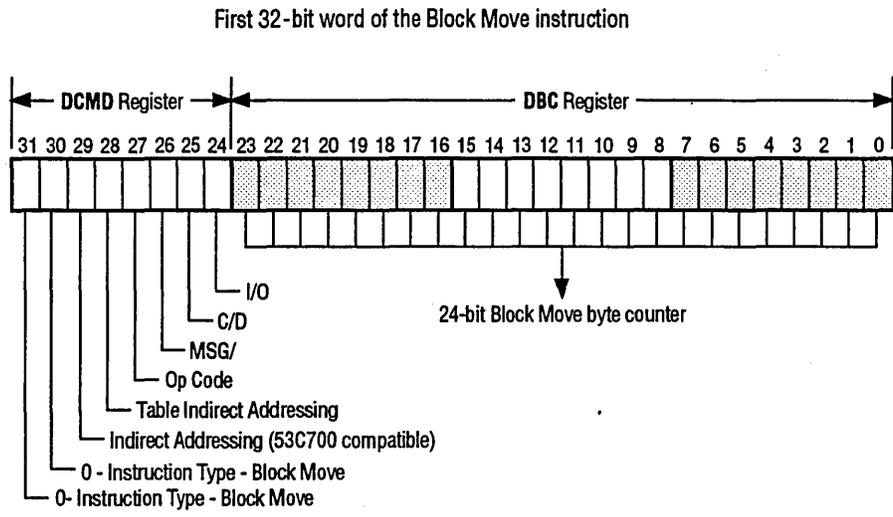
Given the rich set of SCSI oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of instructions are implemented in the 53C810:

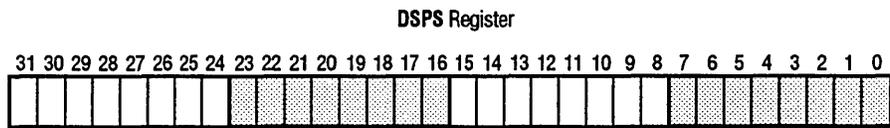
- Block Move
- I/O or Read/Write
- Transfer Control
- Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, only used by Memory Move instructions, is loaded into the TEMP shadow register. In an indirect I/O or Move instruction, the first two 32-bit opcode fetches will be followed by one or two more 32-bit fetch cycles. These cycles are executed with a separate bus ownership request.

Figure 6-1. Block Move Instruction Register



Second 32-bit word of the Block Move instruction



32-bit Start Address of the data to be moved or table entry offset

## Block Move Instructions

For block move commands, bits 5 and 4 (SIOM and DIOM) in the DMODE register determine whether the source/destination address resides in memory or I/O space. When data is being moved onto the SCSI bus, SIOM controls whether that data comes from I/O or memory space. When data is being moved off of the SCSI buss, DIOM controls whether that data goes to I/O or memory space.

### Bits 31-30 Instruction Type-Block Move

#### Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third long word fetch (4-byte transfer across the host computer bus).

**Direct:** The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

**Indirect:** Use the fetched byte count, but fetch the data address from the address in the command.

Command	Byte Count
Address of Pointer	

Once the data pointer address is loaded, it is executed as when the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTS compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

#### Bit 28 Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

**Table Indirect:** Use the signed integer offset in bits 23-0 of the second 4 bytes of the instruction, added to the value in the DSA register, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but bits 31-24 are ignored.

Command	Not Used
Don't Care	Table Offset

Prior to the start of an I/O the Data Structure Base Address register (DSA) should be loaded with the base address of the I/O data structure. The address may be any address on a long word boundary.

After a Table Indirect opcode is fetched, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the 53C810. Execution of the move begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries.

There are two restrictions on the placement of pointer data in system memory: the 8 bytes of data in the MOVE command must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	Byte Count
Physical Data Address	

**Bit 27 Opcode**

This 1-bit field defines the instruction to be executed, either a block move (MOVE) or a chained block move (CHMOV). In the 53C810, the CHMOV instruction is functionally identical to the Move instruction.

**Target Mode**

OPC	Instruction Defined
0	MOVE
1	Reserved

- 1) The 53C810 verifies that it is connected to the SCSI bus as a target before executing this instruction.

- 2) The 53C810 asserts the SCSI phase signals (MSG/, C/D, & I/O) as defined by the Phase Field bits in the instruction.
- 3) If the instruction is for the command phase, the 53C810 receives the first command byte and decodes its SCSI Group Code.
  - a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the 53C810 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
  - b) If any other Group Code is received, the DBC register is not modified and the 53C810 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h an illegal instruction interrupt is generated.
- 4) The 53C810 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register. If the opcode bit is set and a data transfer ends on an odd byte boundary, the 53C810 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 6-2.
- 5) If the SCSI ATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether an interrupt will be generated.

**Initiator Mode**

OPC	Instruction Defined
0	Reserved
1	MOVE

- 1) The 53C810 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
- 2) The 53C810 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the 53C810 has not yet transferred data by responding with an ACK/.
- 3) The 53C810 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when REQ/ is asserted.
- 4) If the SCSI phase bits match the value stored in the SSTAT1 register, the 53C810 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register. If the opcode bit is cleared and a data transfer ends on an odd byte boundary, the 53C810 will store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 6-2.
- 5) If the SCSI phase bits do not match the value stored in the SSTAT1 register, the 53C810 generates a phase mismatch interrupt and the command is not executed.

#### Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the 53C810 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the 53C810 operates in target mode, the 53C810 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

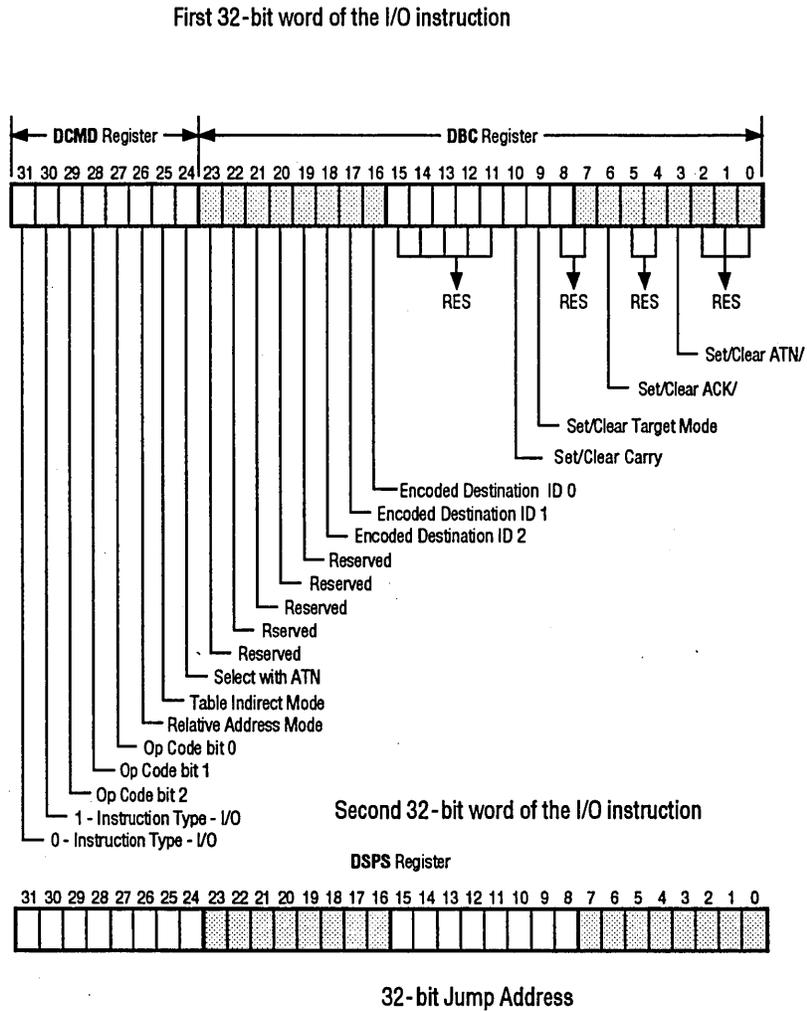
#### Bits 23-0 Transfer Counter

A 24-bit field specifying the number of data bytes to be moved between the 53C810 and system memory. The field is stored in the DBC register. When the 53C810 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the 53C810 fetches the next instruction.

#### Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the 53C810 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

Figure 6-2. I/O Instruction Register



## I/O Instructions

### Bits 31-30 Instruction Type - I/O Instruction

#### Bits 29-27 Opcode

The following Opcode Field bits have different meanings, depending on whether the 53C810 is operating in initiator or target mode. **Note:** Opcode selections 101-111 are considered Read/Write instructions, and are described in that section.

#### Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

#### Reselect Instruction

- 1) The 53C810 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C810 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.
- 2) If the 53C810 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the 53C810 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.

- 3) If the 53C810 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C810 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

#### Disconnect Instruction

The 53C810 disconnects from the SCSI bus by deasserting all SCSI signal outputs.

#### Wait Select Instruction

- 1) If the 53C810 is selected, it fetches the next instruction from the address pointed to by the DSP register.
- 2) If reselected, the 53C810 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C810 should manually be set to initiator mode when reselected.
- 3) If the CPU sets the SIGP bit in the ISTAT register, the 53C810 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

#### Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the ALU is set.

**Note:** None of the signals are set on the SCSI bus in target mode.

### Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

**Note:** None of the signals are reset on the SCSI bus in target mode.

### Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

### Select Instruction

- 1) The 53C810 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C810 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
- 2) If the 53C810 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DSP register.
- 3) If the 53C810 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C810 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.
- 4) If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

### Wait Disconnect Instruction

- 1) The 53C810 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (400 ns), after the 53C810 has received a Disconnect Message or a Command Complete Message.

### Wait Reselect Instruction

- 1) If the 53C810 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C810 should be manually set to target mode when selected.
- 2) If the 53C810 is reselected, it fetches the next instruction from the address pointed to by the DSP register.
- 3) If the CPU sets the SIGP bit in the ISTAT register, the 53C810 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

### Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

### Clear Instruction

When the ACK/or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes.. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

#### Bit 26 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address. This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

#### Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is added to the value in the DSA register, used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, the DSA should be loaded with the base address of the I/O data structure. The address may be any address on a longword boundary. After a Table Indirect opcode is fetched, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries. There are two restrictions on the placement of data in system memory.

- 1) The I/O data structure must lie within the 8 MB above or below the base address.

- 2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

config	ID	offset/period	(00)
--------	----	---------------	------

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

**Direct** – Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

**Table Indirect** – Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

**Relative** – Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
Alternate Jump Offset			

**Table Relative** – Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPT to the data structure base address to form the fetch address.

Command	Table Offset
	Alternate Jump Offset

**Bit 24 Select with ATN/**

This bit specifies whether ATN/ will be asserted during the selection phase when the 53C810 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

**Bit 23-19 Reserved**

**Bits 18-16 Encoded SCSI Destination ID**

This 3-bit field specifies the destination SCSI ID for an I/O instruction.

**Bit 10 Set/Clear Carry**

This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a Set command deasserts the Carry bit in the ALU.

**Bit 9 Set/Clear Target Mode**

This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the 53C810 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear command configures the 53C810 as an initiator device (this clears bit 0 of the SCNTL0 register).

**Bit 6 Set/Clear ACK/**

**Bit 3 Set/Clear ATN/**

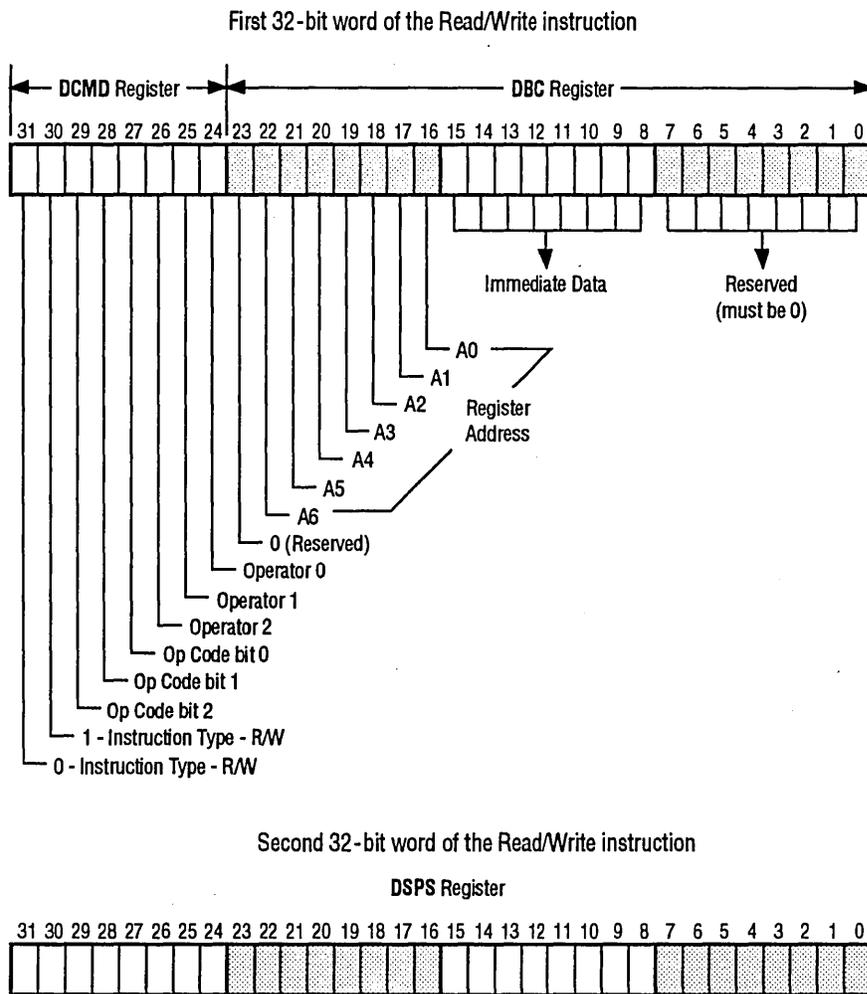
These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the 53C810 is operating as an initiator or the SCSI Loopback Enable bit is set in the STTEST2 register.

The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

Figure 6-4. Read/Write Instruction Register



Not used, must be 0

Table 6-1. Read/Write Instructions

Operator	Opcode 111 Read Modify Write	Opcode 110 Move to SFBR	Opcode 101 Move From SFBR
000	Immediate data to destination register	Immediate data to SFBR	Immediate SFBR to destination register
001*	Immediate data shifted left and placed in destination register	Immediate data shifted left and placed in SFBR	Immediate SFBR shifted left and placed in destination register
010	Immediate data ORed with destination register	Immediate data OR register to SFBR	Immediate data ORed with SFBR to destination register
011	Immediate data XORed with destination register	Immediate data XOR register to SFBR	Immediate data XORed with SFBR to destination register
100	Immediate data ANDed with destination register	Immediate data AND register to SFBR	Immediate data ANDed with SFBR to destination register
101*	Immediate data shifted right and placed in destination register	Immediate data shifted right and placed in SFBR	Immediate SFBR shifted right and placed in destination register
110	Immediate data added to destination register without carry	Immediate data added with register to SFBR without carry	Immediate data added with SFBR to destination register without carry
111	Immediate data added to destination register with carry	Immediate data added with register to SFBR with carry	Immediate data added with SFBR to destination register with carry

- Notes:**
- 1) Substitute the desired register name or address for "RegA" in the syntax examples
  - 2) data8 indicates eight bits of data
- \* Data is shifted through the carry bit and the carry bit is shifted into the data byte.

---

## Read/Write Instructions

### Bits 31-30 Instruction Type - Read/Write Instruction

The Read/Write instruction uses operator bits 26 through 24 in conjunction with the opcode bits to determine which instruction is currently selected. Refer to table 6-1.

### Bits 29-27 Opcode

The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Opcodes 000 through 100 are considered I/O instructions.

### Bits 26-24 Operator

These bits are used in conjunction with the opcode bits to determine which instruction is currently selected.

### Bits 22-16 Register Address - A(6-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the 53C810.

## Read-Modify-Write Cycles

The register is read, the selected operation is performed, and the result is written back to the source register.

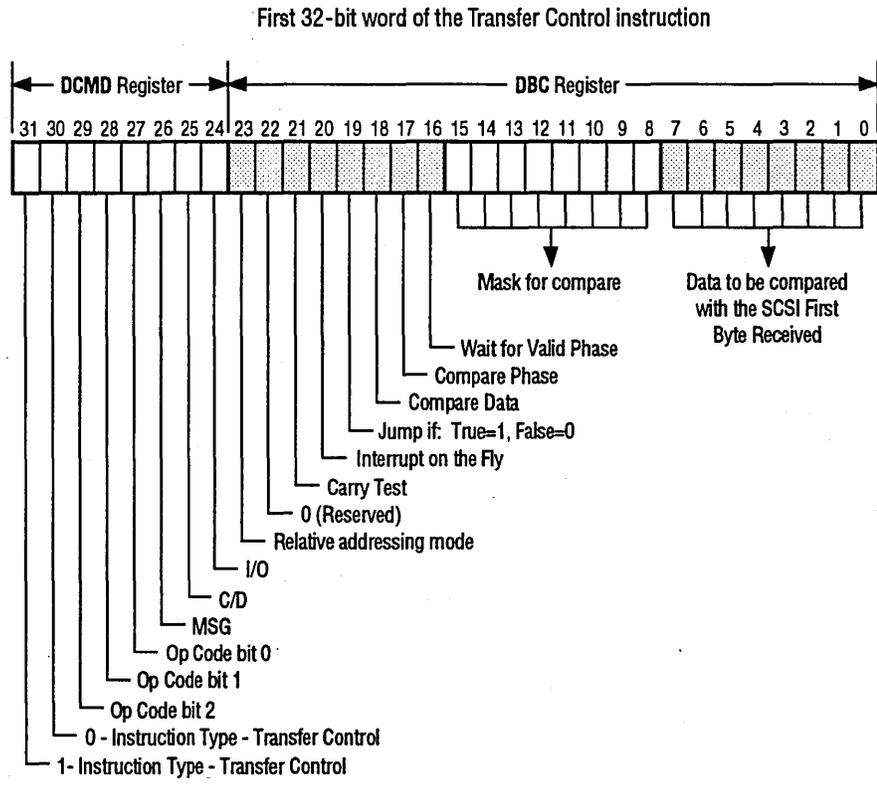
The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

### Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with AND/OR/ADD operators.
- After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

Figure 6-5. Transfer Control Instruction



# Transfer Control Instructions

## Bits 31-30 Instruction Type - Transfer Control Instruction

### Bits 29-27 Opcode

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

### Jump Instruction

- 1) The 53C810 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the 53C810 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.
- 2) If the comparisons are false the 53C810 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

### Call Instruction

- 1) The 53C810 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C810 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

When the 53C810 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

- 2) If the comparisons are false, the 53C810 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

### Return Instruction

- 1) The 53C810 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C810 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register. The 53C810 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

- 2) If the comparisons are false, then the 53C810 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

## Interrupt Instructions

### *Interrupt*

- a) The 53C810 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C810 generates an interrupt by asserting the IRQ/ signal.
- b) The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.
- c) The 53C810 halts and the DSP register must be written to start any further operation.

### *Interrupt on-the-Fly*

- a) The 53C810 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C810 will assert the Interrupt on the fly bit (ISTAT bit 2).

### **Bits 26-24 SCSI Phase**

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the 53C810 is operating in initiator mode; when the 53C810 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

### **Bit 23 Relative Addressing Mode**

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

**Jump/Call an Absolute Address** – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

**Jump/Call a Relative Address** – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
Don't Care	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the 53C810. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos complement), the jump can be forward or backward.

A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

#### Bit 21 Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

#### Bit 20 Interrupt on the Fly

When this bit is asserted, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

#### Bit 19 Jump If True/False

This bit determines whether the 53C810 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Result of Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

#### Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

#### Bit 17 Compare Phase

When the 53C810 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur. When the 53C810 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

#### Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the 53C810 waits for a previously unserved phase before comparing the SCSI phase & data.

If the Wait for Valid Phase bit is clear, then the 53C810 compares the SCSI phase & data immediately.

#### Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored. For instance, a mask of 01111111b and data compare value of

1XXXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

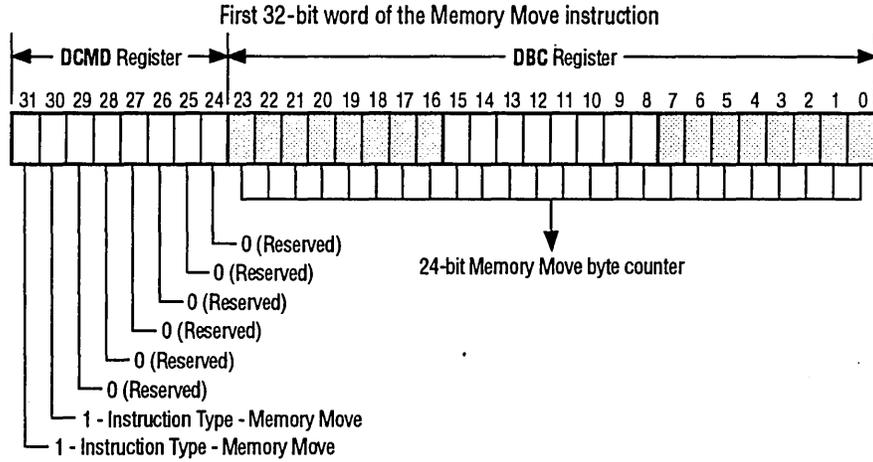
**Bits 7-0 Data Compare Value**

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

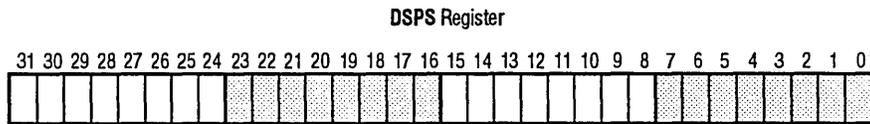
**Bits 31-0 Jump Address**

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the 53C810 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DSP register and becomes the current instruction pointer.

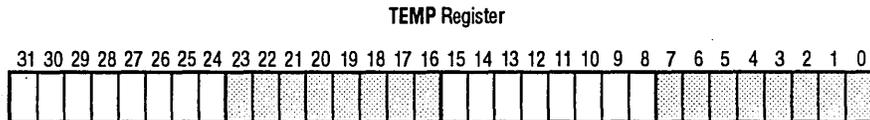
Figure 6-5. Memory Move Instructions



Second 32-bit – source address of the Memory Move instruction



Third 32-bit word – destination address of the Memory Move instruction



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## Memory Move Instructions

For Memory Move commands, bits 5 and 4 (SION and DIOM) in the DMODE register determine whether the source or destination addresses reside in memory or I/O space. By setting these bits appropriately, data may be moved within memory space, within I/O space, or between the two address spaces.

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the 53C810 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

- 1) Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.
- 2) Indirect addresses are not allowed.

A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

The DSPS and DSA registers are additional holding registers used during the Memory Move; however, the contents of the DSA register are preserved.

### Bits 29-24 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

### Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

### Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to/from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower 6 bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C810 register (for example, from a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

## Chapter Seven Electrical Characteristics

### DC Electrical Characteristics

#### Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
$T_{STG}$	Storage temperature	-55	150	°C	-
$V_{DD}$	Supply voltage	-0.5	7.0	V	-
$V_{IN}$	Input Voltage	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V	-
$I_{LP}^*$	Latch-up current	$\pm 200$	-	mA	-
ESD**	Electrostatic discharge	-	2K	V	MIL-STD 883C, Method 3015.7

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the Operating Conditions section of this manual is not implied.

\*  $-2V = VPIN > 8V$

\*\* SCSI pins only

#### Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{DD}$	Supply voltage	4.75	5.25	V	-
$I_{DD}$	Supply current	-	100	mA	-
$T_A$	Operating free air	0	70	°C	-

\* Conditions that exceed the operating limits may cause the device to function incorrectly

**SCSI Signals - SD (7-0)/, SDP/, REQ/, ACK/**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{IH}$	Input high voltage	2.0	$V_{DD} + 0.5$	V	-
$V_{IL}$	Input low voltage	$V_{SS} - 0.5$	0.8	V	-
$V_{OH}^*$	Output high voltage	2.5	3.5	V	2.5 mA
$V_{OL}$	Output low voltage	$V_{SS}$	0.5	V	48 mA
$I_{IN}$	Input leakage	-10	10	$\mu A$	-
$I_{OZ}$	Tristate leakage	-10	10	$\mu A$	-

\* TolerANT active negation enabled

**SCSI Signals - MSG/, I\_O/, C\_D/, ATN/, BSY/, SEL/, RST/**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{IH}$	Input high voltage	2.0	$V_{DD} + 0.5$	V	-
$V_{IL}$	Input low voltage	$V_{SS} - 0.5$	0.8	V	-
$V_{OL}$	Output low voltage	$V_{SS}$	0.5	V	48 mA
$I_{IN}$	Input leakage	-10	10	$\mu A$	-
	SCSI RST/ only	-500	50	$\mu A$	-
$I_{OZ}$	Tristate leakage	-10	10	$\mu A$	-

**Input Signals - CLK, SCLK, GNT/, IDSEL, RST, TESTIN**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{IH}$	Input high voltage	2.0	$V_{DD} + 0.5$	V	-
$V_{IL}$	Input low voltage	$V_{SS} - 0.5$	0.8	V	-
$I_{IN}$	Input leakage	-1.0	1.0	$\mu A$	-
	SCSI RST/ only	-500	50	$\mu A$	-

**Note:** CLK, SCLK, GNT/, and IDSEL have 100  $\mu A$  pull-ups that are enabled when TESTIN is low. TESTIN has a 100  $\mu A$  pull-up that is always enabled.

**Output Signal - MAC/\_TESTOUT**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{OH}$	Output high voltage	2.4	$V_{DD}$	V	-16 mA
$V_{OL}$	Output low voltage	$V_{SS}$	0.4	V	16 mA
$I_{OH}$	Output high current	-8	-	mA	$V_{DD} - .5 V$
$I_{OL}$	Output low current	16	-	mA	0.4 V

**Output Signal - IRQ/**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{OH}$	Output high voltage	2.4	$V_{DD}$	V	-8 mA
$V_{OL}$	Output low voltage	$V_{SS}$	0.4	V	8 mA
$I_{OH}$	Output high current	-4	-	mA	$V_{DD} - .5 V$
$I_{OL}$	Output low current	8	-	mA	0.4 V

**Note:** IRQ/ has a 100  $\mu A$  pull-up that is enabled when TESTIN is low. IRQ/ can be enabled with a register bit as an open drain output with an internal 100  $\mu A$  pull-up.

**Output Signal - REQ/**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{OH}$	Output high voltage	TBD	TBD	V	-
$V_{OL}$	Output low voltage	$V_{SS}$	0.4	V	16 mA
$I_{OH}$	Output high current	-8	-	mA	2.4 V
$I_{OL}$	Output low current	16	-	mA	0.4 V

**Note:** REQ/ has a 100  $\mu A$  pull-up that is enabled when TESTIN is low.

**Bidirectional Signals - AD (31-0), C\_BE (3-0)/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{IH}$	Input high voltage	2.0	$V_{DD} + 0.5$	V	-
$V_{IL}$	Input low voltage	$V_{SS} - 0.5$	0.8	V	-
$V_{OH}$	Output high voltage	TBD	TBD	V	TBD
$V_{OL}$	Output low voltage	$V_{SS}$	0.4	V	16 mA
$I_{OH}$	Output high current	TBD	-	mA	TBD
$I_{OL}$	Output low current	16	-	mA	0.4V
$I_{IN}$	Input leakage	-10	10	$\mu$ A	-
$I_{OZ}$	Tristate leakage	-10	10	$\mu$ A	-

**Note:** All the signals in this table have 100  $\mu$ A pull-ups that are enabled when TESTIN is low.

**Bidirectional Signals - GPIO0\_FETCH/, GPIO1\_MASTER/**

Symbol	Parameter	Min	Max	Unit	Test Conditions
$V_{IH}$	Input high voltage	2.0	$V_{DD} + 0.5$	V	-
$V_{IL}$	Input low voltage	$V_{SS} - 0.5$	0.8	V	-
$V_{OH}$	Output high voltage	2.4	$V_{DD}$	V	-16 mA
$V_{OL}$	Output low voltage	$V_{SS}$	0.4	V	16 mA
$I_{OH}$	Output high current	-8	-	mA	2.4V
$I_{OL}$	Output low current	16	-	mA	0.4V
$I_{IN}$	Input leakage	-10	10	$\mu$ A	-
$I_{OZ}$	Tristate leakage	-10	10	$\mu$ A	-

**Note:** All the signals in this table have 100  $\mu$ A pull-ups that are enabled when TESTIN is low.

# NCR TolerANT Active Negation Technology Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V <sub>oh1</sub>	Output high voltage	I <sub>oh</sub> = 4 mA	2.5	3.1	3.5	V
V <sub>ol</sub>	Output low voltage	I <sub>ol</sub> = 48 mA	0.1	0.2	0.5	V
V <sub>ih</sub>	Input high voltage		2.0		7.0	V
V <sub>il</sub>	Input low voltage	Referenced to V <sub>ss</sub>	-0.5		0.8	V
V <sub>ik</sub>	Input clamp voltage	V <sub>dd</sub> = min;	-0.66	-0.74	-0.77	V
V <sub>th</sub>	Threshold, high to low		1.1	1.2	1.3	V
V <sub>tl</sub>	Threshold, low to high		1.5	1.6	1.7	V
V <sub>th</sub> - V <sub>tl</sub>	Hysteresis		300	350	400	mV
I <sub>oh</sub> <sup>1</sup>	Output high current	V <sub>oh</sub> = 2.4 Volts	5	15	24	mA
I <sub>ol</sub>	Output low current	V <sub>ol</sub> = 0.5 Volts	100	150	200	mA
I <sub>osh</sub>	Short-circuit output high current	Output driving low, pin shorted to V <sub>dd</sub> supply <sup>2</sup>			625	mA
I <sub>osl</sub>	Short-circuit output low current	Output driving high, pin shorted to V <sub>ss</sub> supply			95	mA
I <sub>lh</sub>	Input high leakage	-0.5 < V <sub>dd</sub> < 5.25 V <sub>pin</sub> = 2.7 V		0.05	10	μA
I <sub>ll</sub>	Input low leakage -0.5	< V <sub>dd</sub> < 5.25 V <sub>pin</sub> = 0.5V		-0.05	-10	μA
R <sub>i</sub>	Input resistance	SCSI pins <sup>3</sup>		20		MΩ
C <sub>p</sub>	Capacitance per pin	Quad Flat Pack Pack		6	10	pF
t <sub>r</sub> <sup>1</sup>	Rise time, 10% to 90 %	Figure 6-1	9.7	15.0	18.5	ns
t <sub>f</sub>	Fall time, 90% to 10%	Figure 6-1	5.2	8.1	14.7	ns
dV <sub>h</sub> /dt	Slew rate, low to high	Figure 6-1	0.15	0.23	0.49	V/ns
dV <sub>L</sub> /dt	Slew rate, high to low	Figure 6-1	0.19	0.37	0.67	V/ns

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Electrostatic Discharge	Mil Std 883C; 30125-7			2	KV
	Latch-up		100			mA
	Filter Delay	Figure 6-2	20	25	30	ns
	Extended Filter Delay	Figure 6-2	40	50	60	ns

**Note:** *These values are guaranteed by periodic characterization; they are not 100% tested on every device.*

<sup>1</sup> Active Negation outputs only: Data, Parity, REQ, ACK

<sup>2</sup> Single pin only; irreversible damage may occur if sustained for 1 second

<sup>3</sup> SCSI RESET pin has 10kΩ pull-up resistor

Figure 7-1. Rise and Fall Time Test Conditions

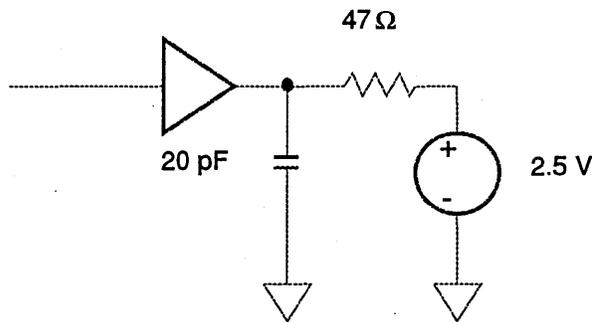


Figure 7-2. SCSI Input Filtering

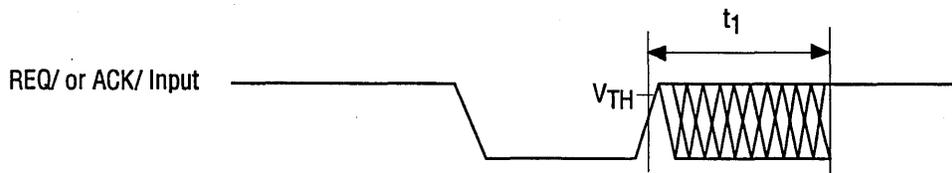


Figure 7-3. Hysteresis of SCSI Receiver

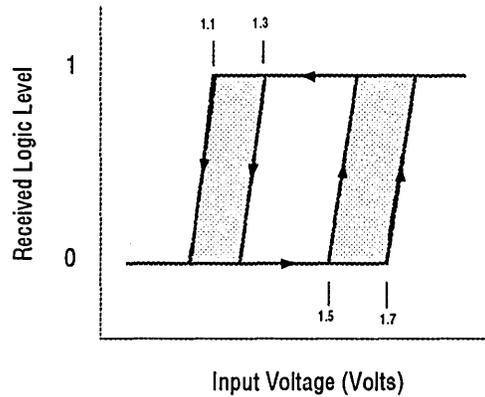


Figure 7-4 Input Current as a Function of Input Voltage

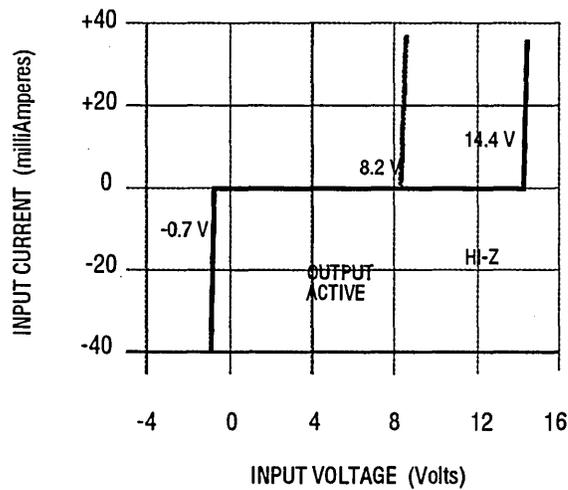
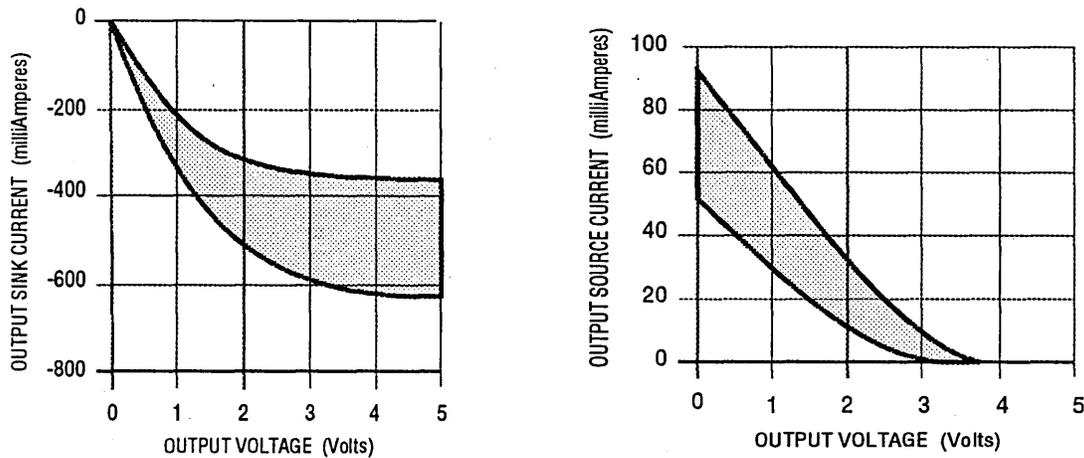


Figure 7-5. Output Current as a Function of Output Voltage



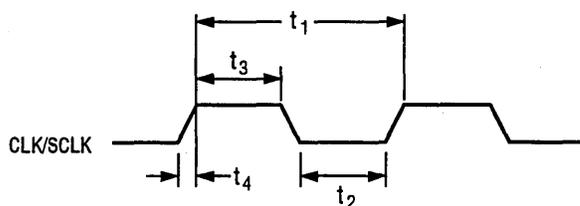
Output Source Current as a Function of Output Voltage ( $I_{OH}$ )

Output Sink Current as a Function of Output Voltage ( $I_{OL}$ )

## AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the *DC Characteristics* section). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Figure 7-6. Clock Timing

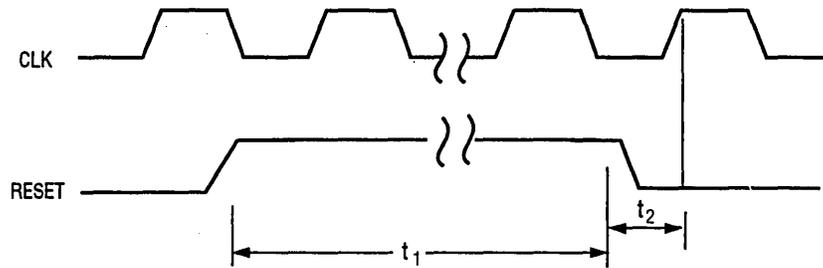


Parameter	Symbol	Min	Max	Units
Bus clock cycle time (CLK)	$t_1$	30	DC	ns
SCSI clock cycle time (SCLK)*		15	60	ns
CLK low time**	$t_2$	14	DC	ns
SCLK low time**		6	33	ns
CLK high time**	$t_3$	14	-	ns
SCLK high time**		6	33	ns
CLK slew rate	$t_4$	1	-	V/ns
SCLK slew rate		1	-	V/ns

\* This parameter must be met to insure SCSI timings are within specification.

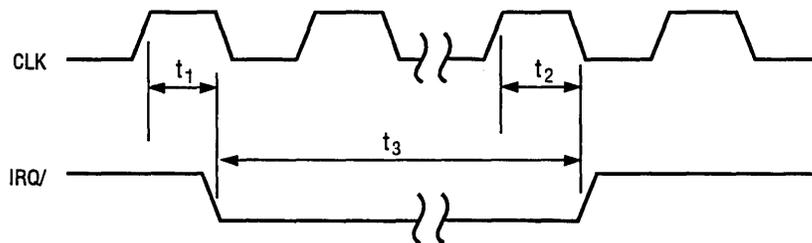
\*\* Duty cycle not to exceed 60/40.

Figure 7-7. Reset Input



Parameter	Symbol	Min	Max	Units
Reset pulse width	$t_1$	10	-	$t_{CLK}$
Reset deasserted setup to CLK high	$t_2$	TBD	-	ns

Figure 7-8. Interrupt Output



Parameter	Symbol	Min	Max	Units
CLK high to IRQ/ low	$t_1$	TBD	-	ns
CLK high to IRQ/ high	$t_2$	TBD	-	ns
IRQ/ deassertion time	$t_3$	TBD	-	CLKS

Figure 7-9. Configuration Register Read

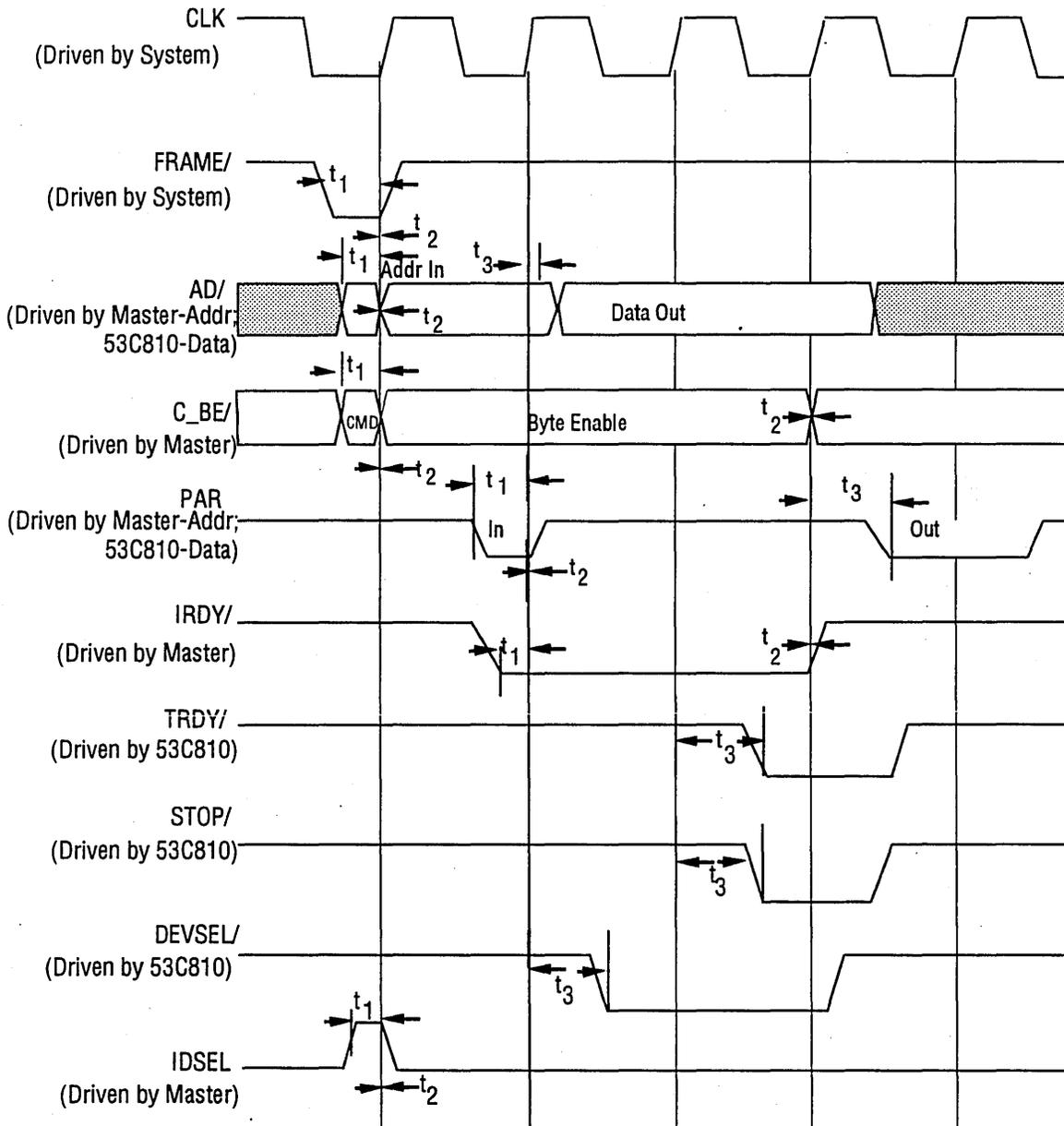


Figure 7-10. Configuration Register Write

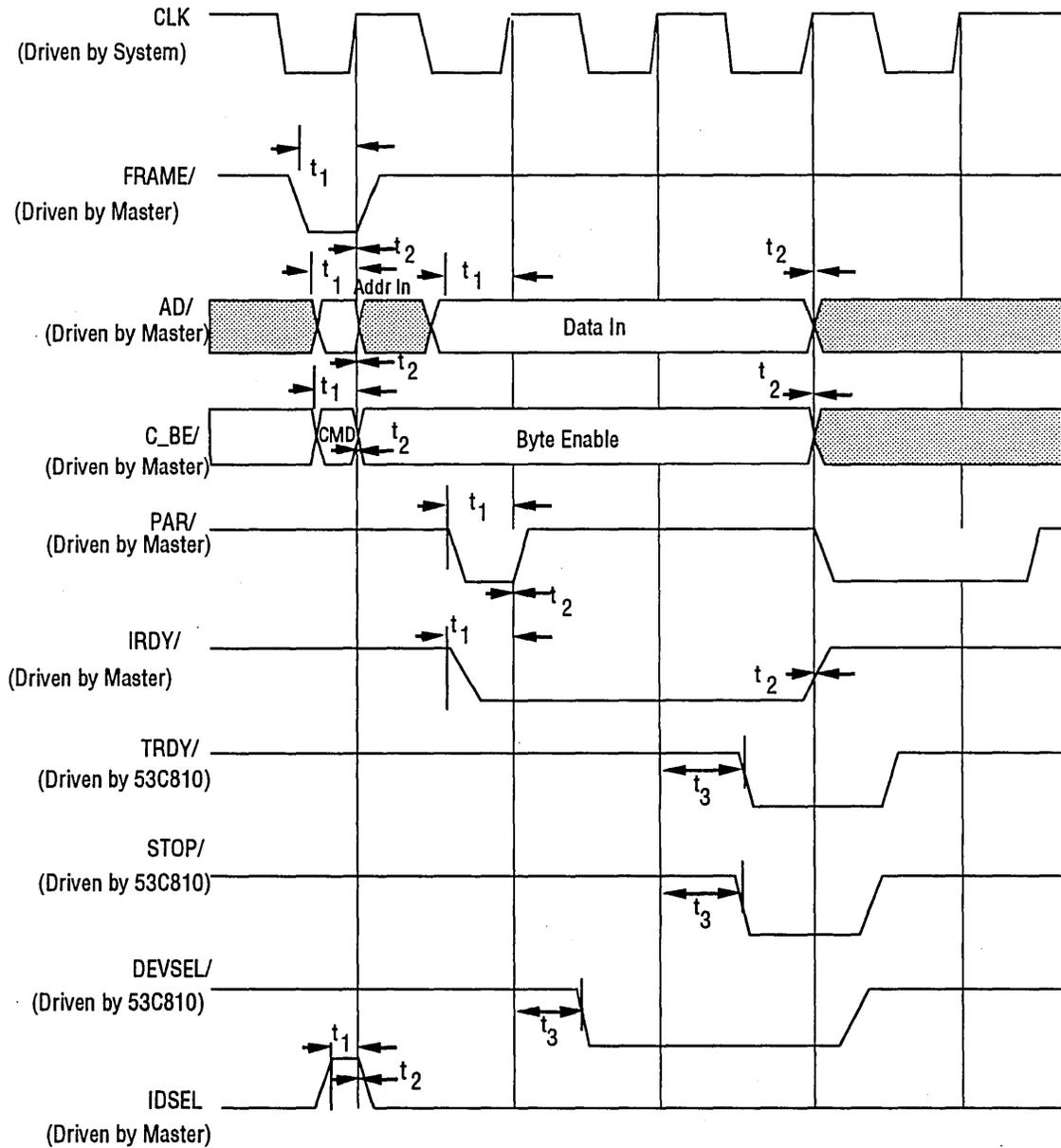


Figure 7-11. Target Read

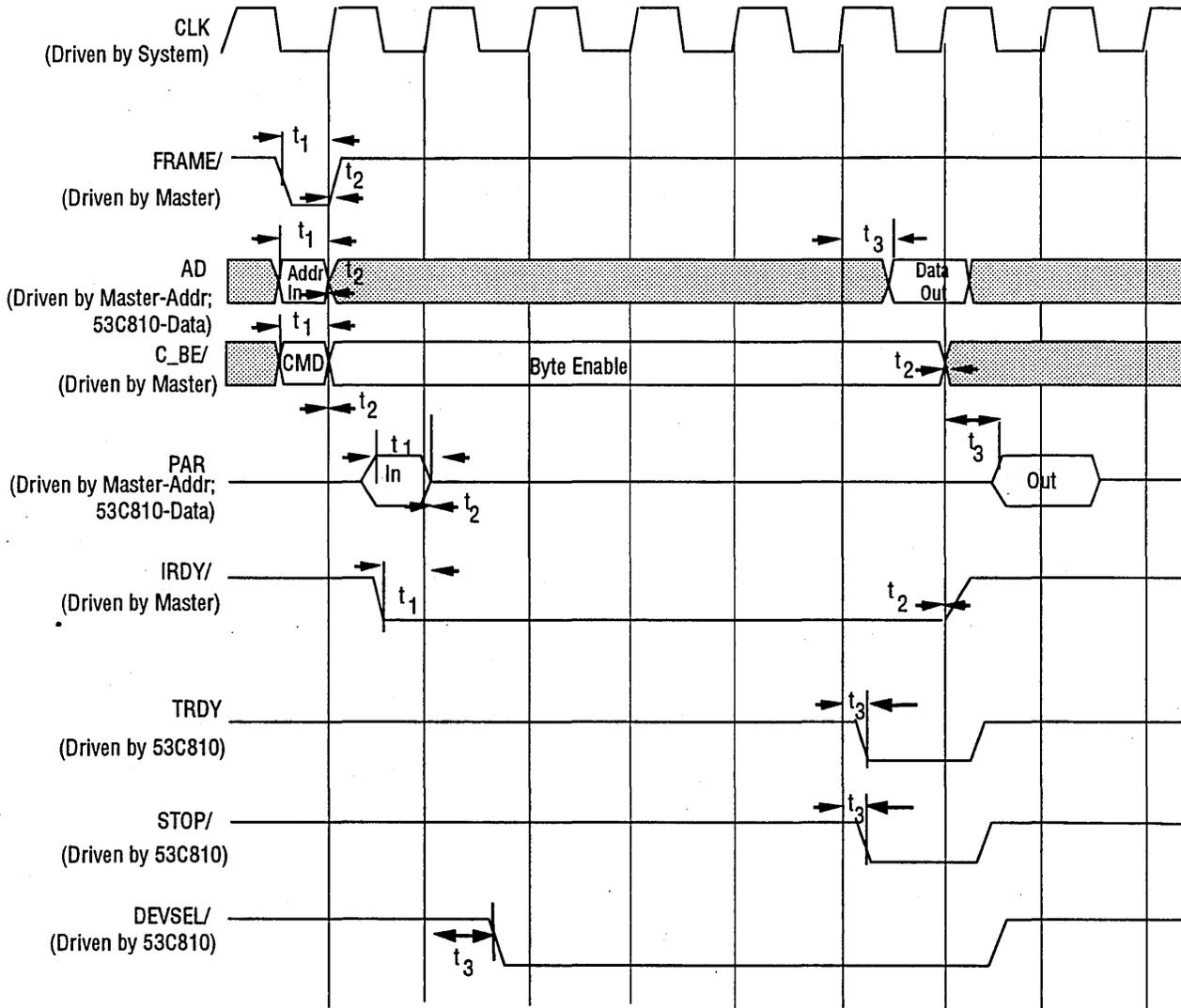


Figure 7-12. Target Write

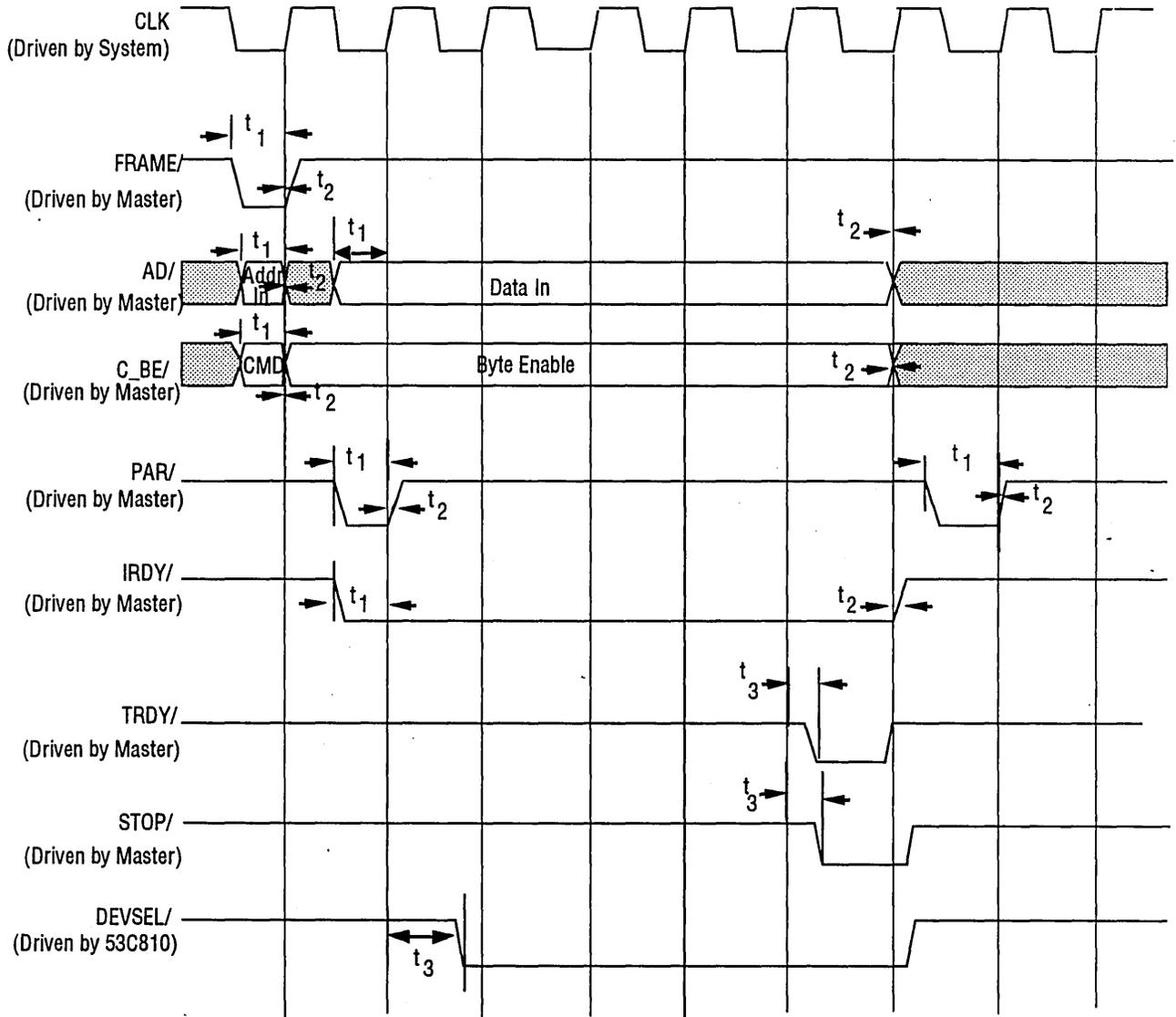
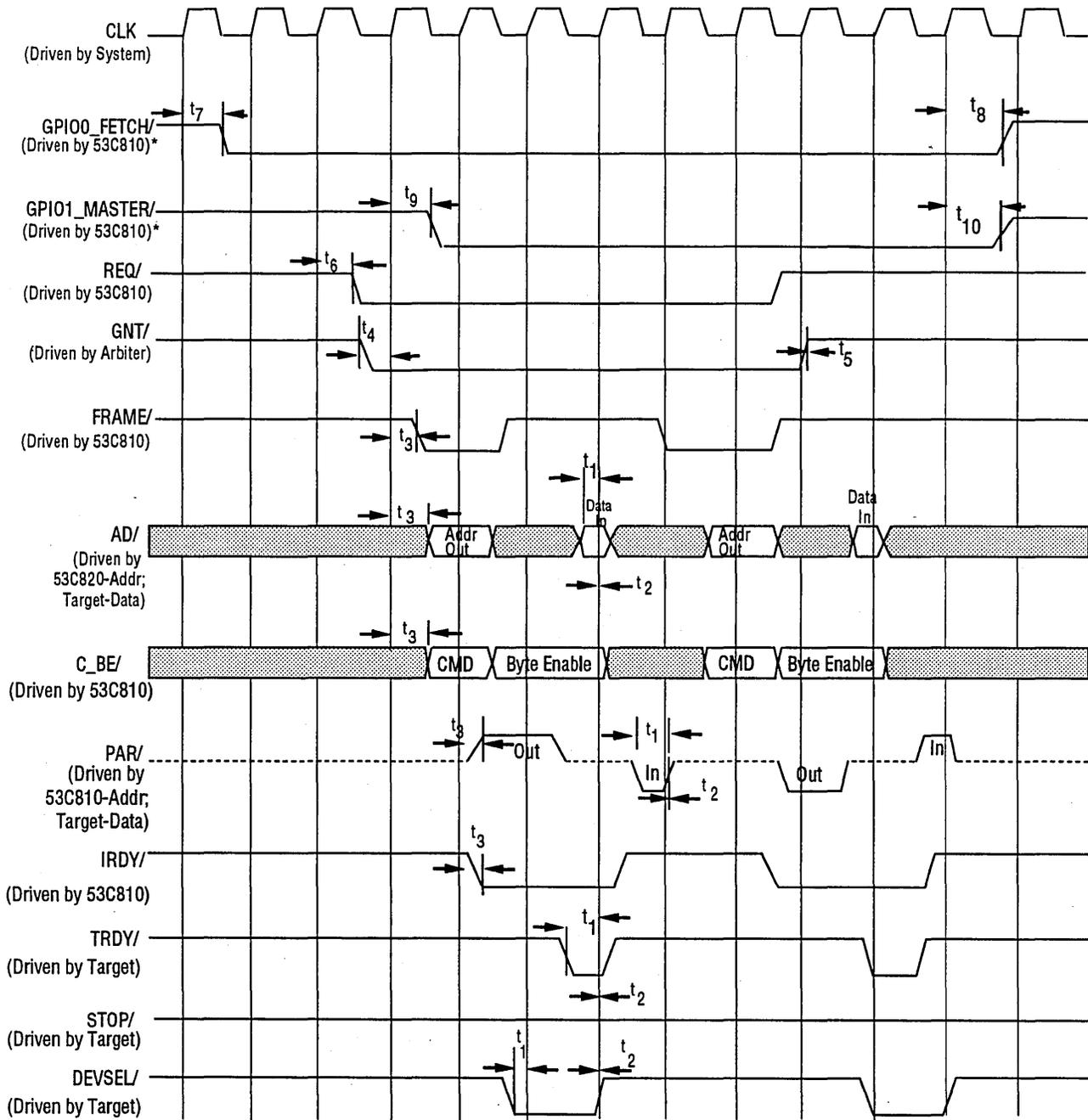
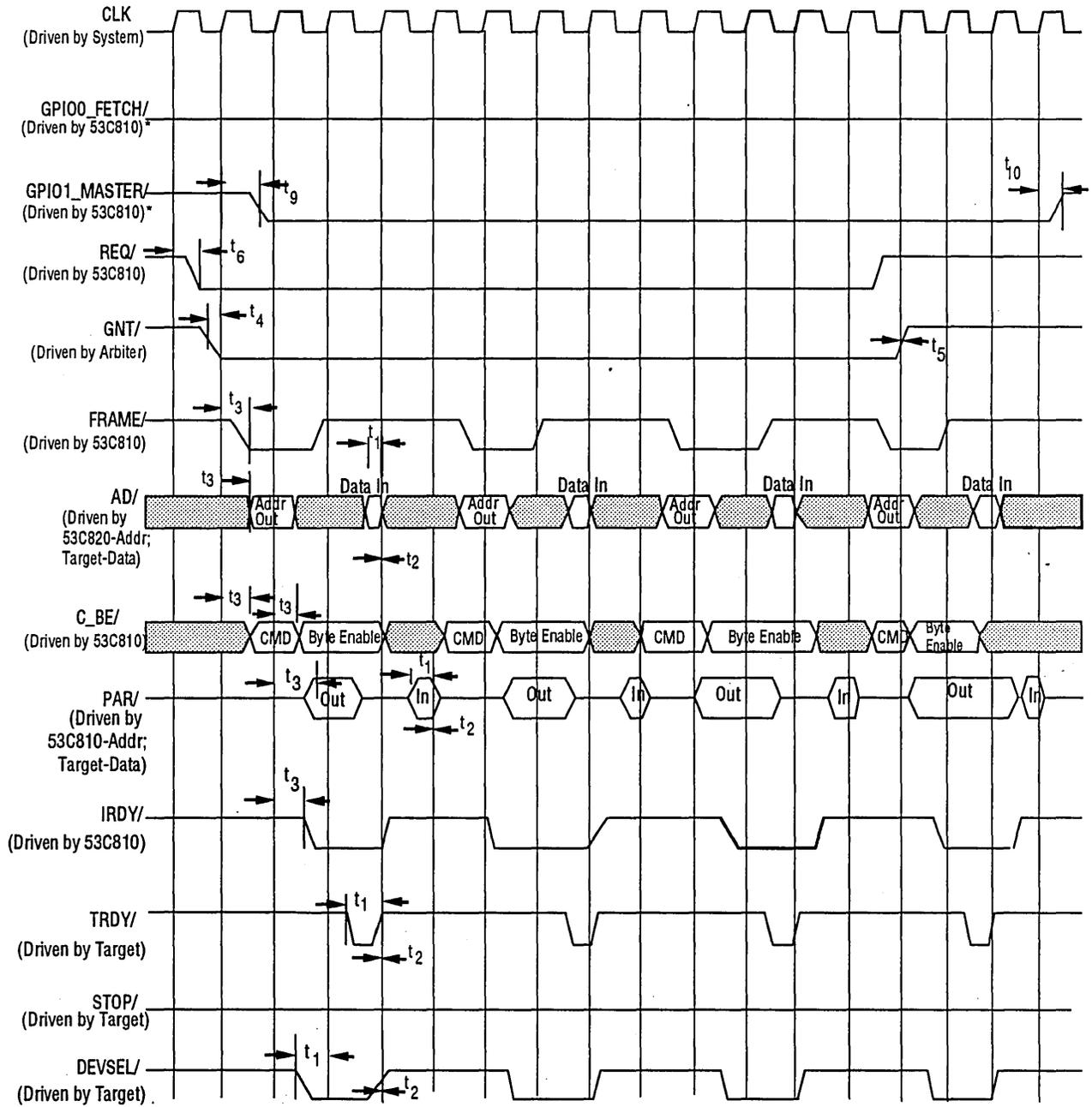


Figure 7-13. Opcode Fetch



\*When enabled

Figure 7-14. Back-to-Back Read



\*When enabled

Figure 7-15. Back-to-Back Write

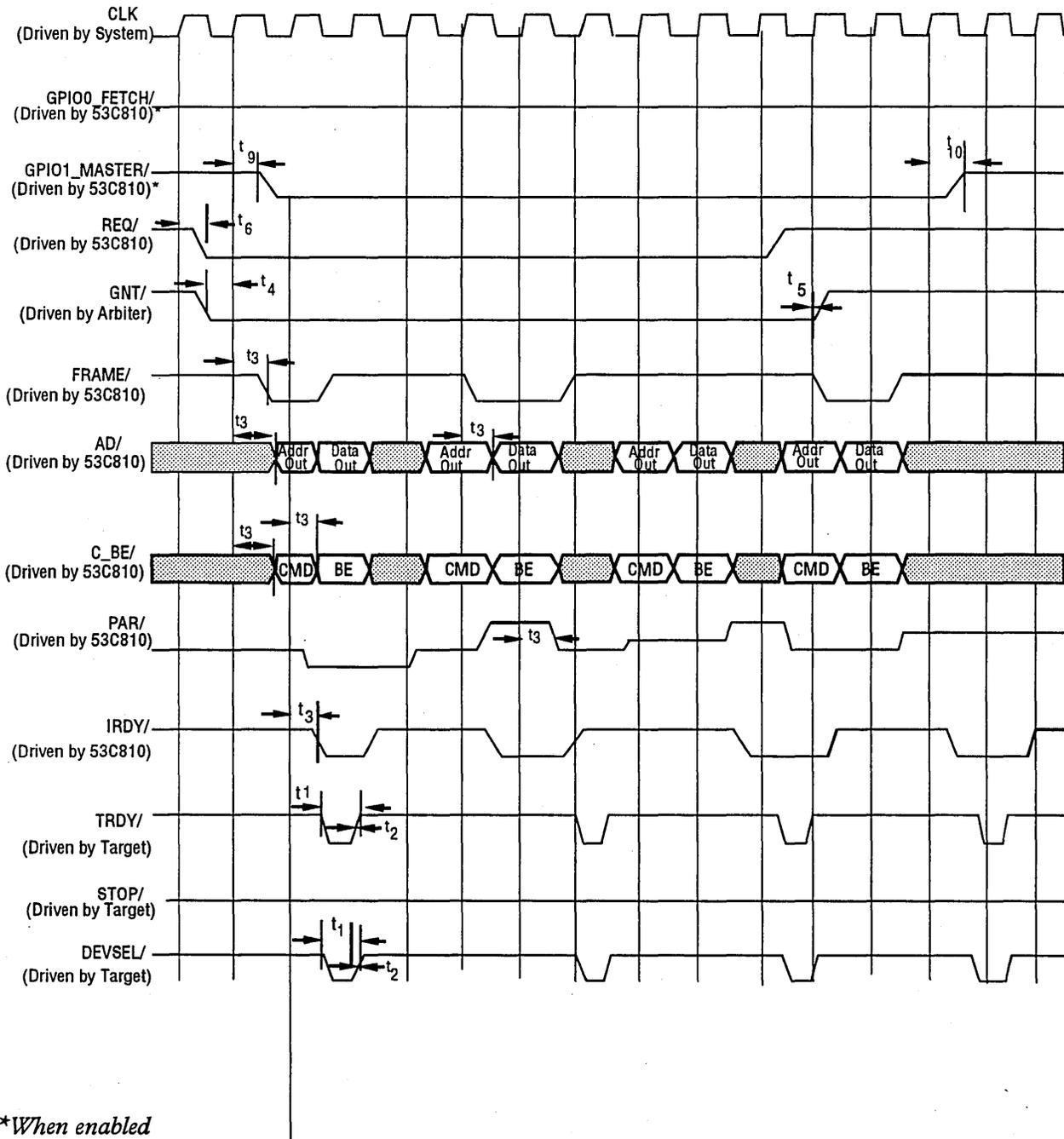


Figure 7-16. Burst Read

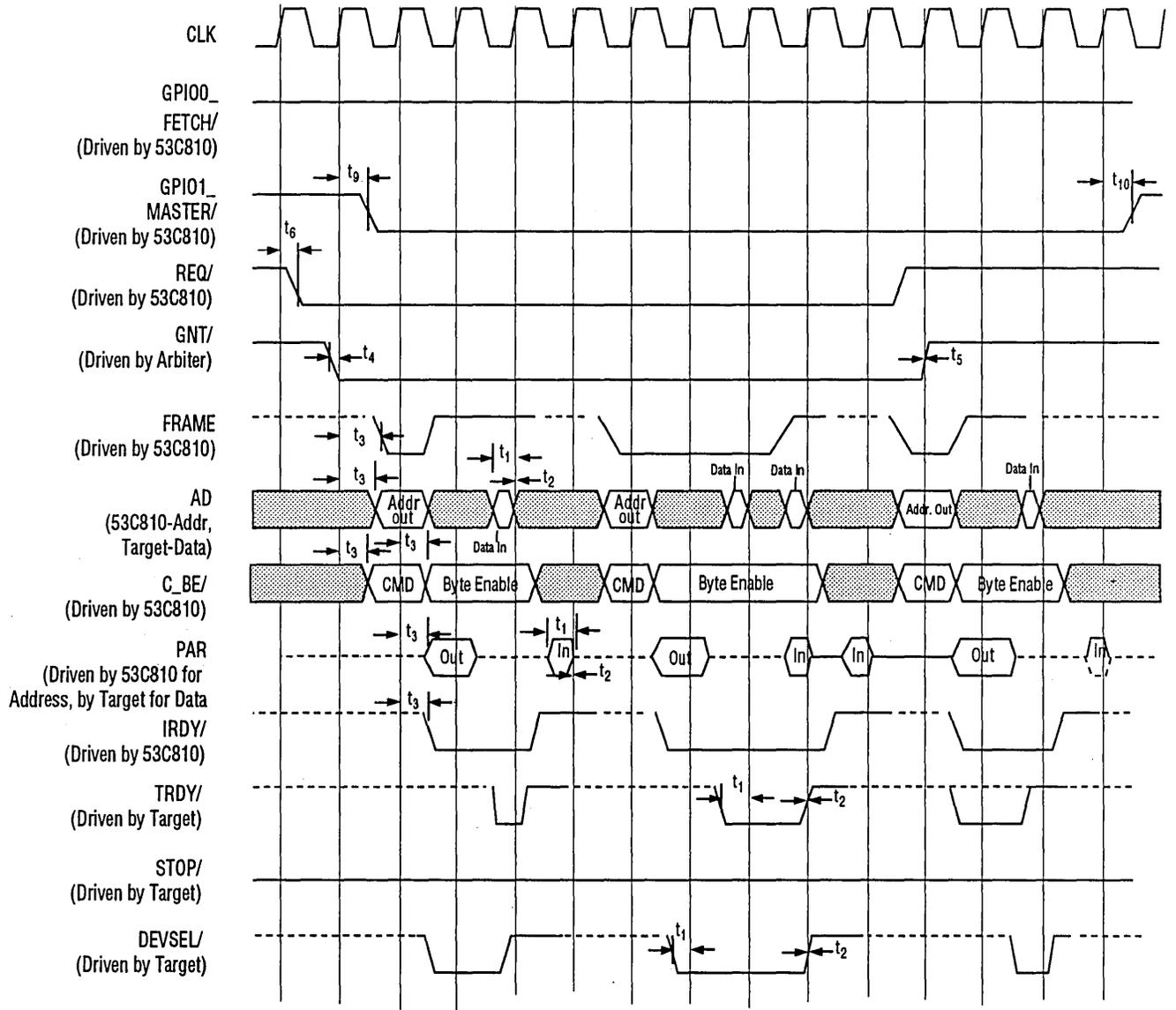
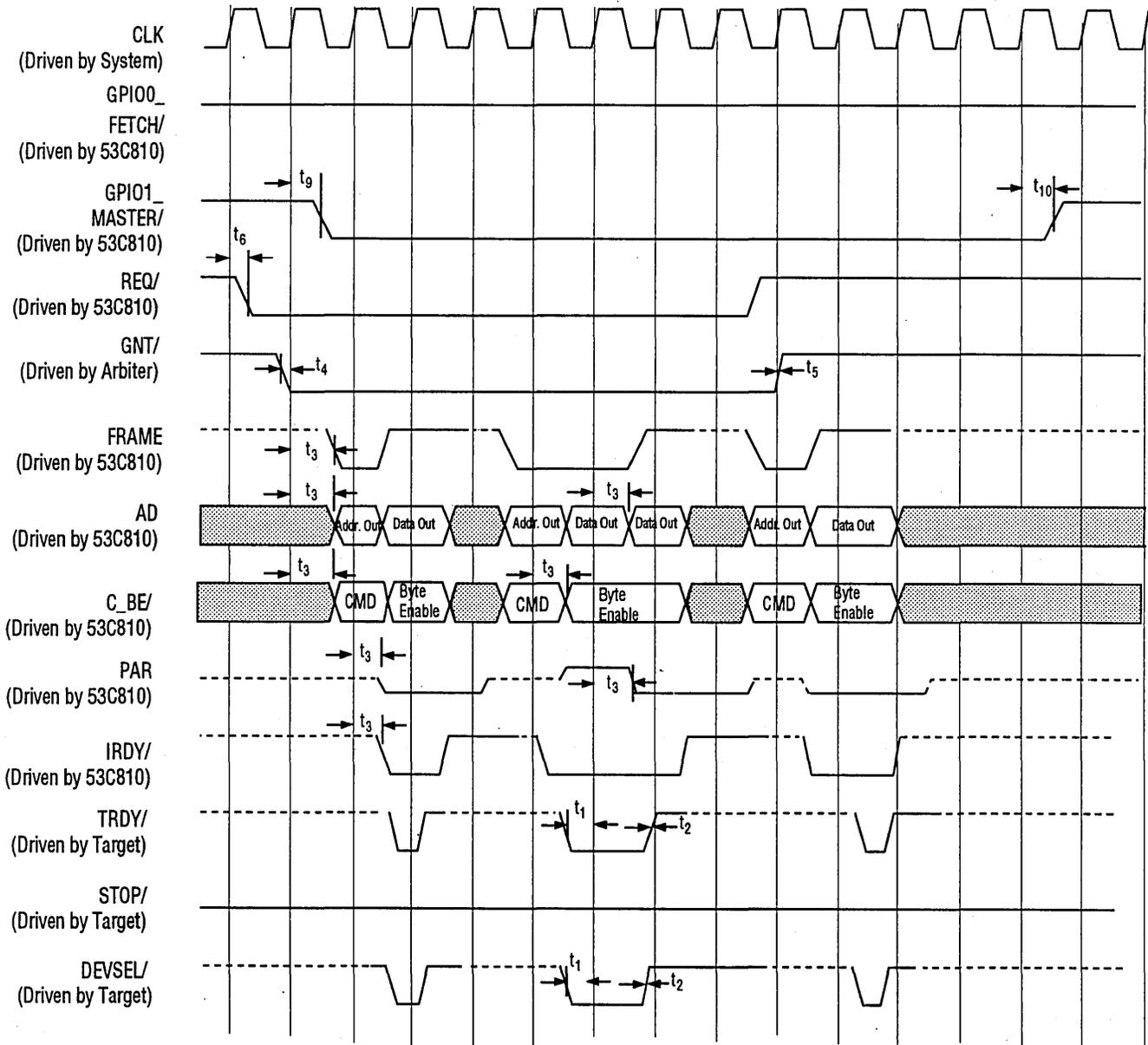


Figure 7-17. Burst Write



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## 53C810 Timings

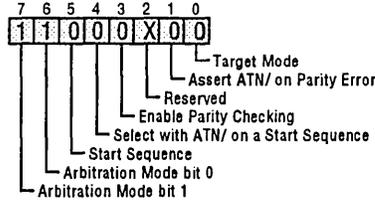
The previous pages illustrate the 53C810 timings. Please note that these are preliminary.

Symbol	Parameter	Min	Max	Units	Conditions
$t_1$	Shared signal input setup time	TBD	-	ns	-
$t_2$	Shared signal input hold time	TBD	-	ns	-
$t_3$	CLK to shared signal output valid	-	TBD	ns	-
$t_4$	Side signal input setup time	TBD	-	ns	-
$t_5$	Side signal input hold time	TBD	-	ns	-
$t_6$	CLK to side signal output valid	-	TBD	ns	-
$t_7$	CLK high to FETCH/ low	-	24	ns	-
$t_8$	CLK high to FETCH/ high	-	24	ns	-
$t_9$	CLK high to MASTER/ low	-	22	ns	-
$t_{10}$	CLK high to MASTER/ high	-	22	ns	-

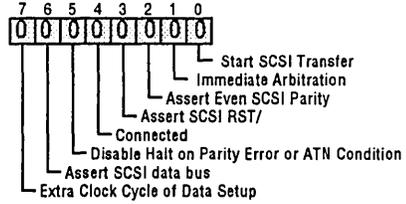


# Appendix A Register Summary

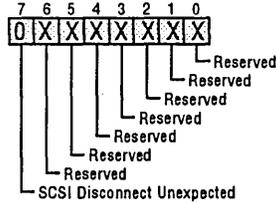
SCNTL0 Register R/W 00h (80h)



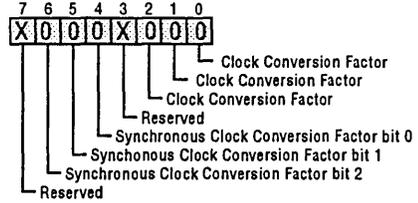
SCNTL1 Register R/W 01h (81h)



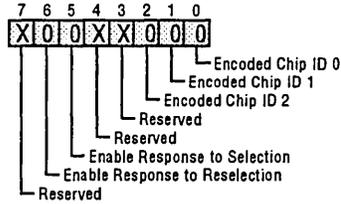
SCNTL2 Register R/W 02h (82h)



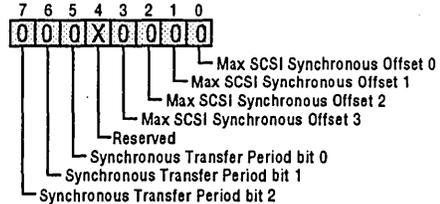
SCNTL3 Register R/W 03h (83h)



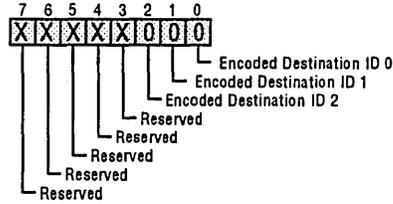
SCID Register R/W 04h (84h)



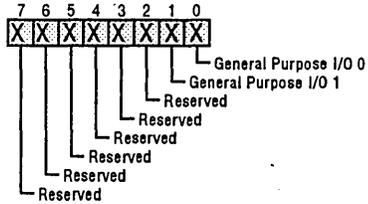
SXFER Register R/W 05h (85h)



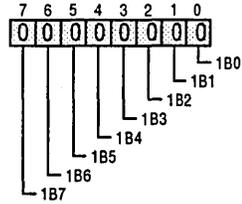
SDID Register R/W 06h (86h)



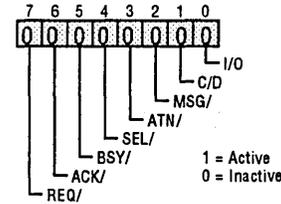
GPREG Register R/W 07h (87h)



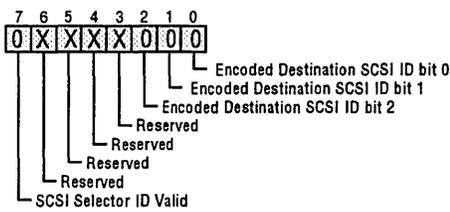
SFBR Register R/W 08h (88h)



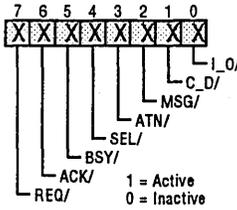
SOCL Register R/W 09h (89h)



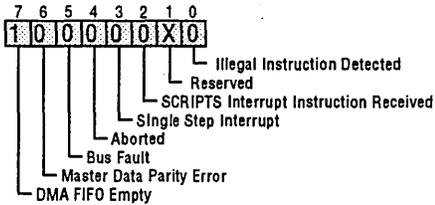
SSID Register R 0Ah (09h)



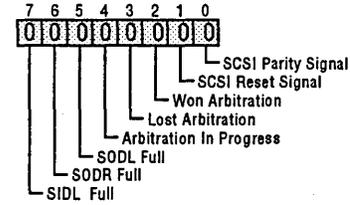
SBCL Register R 0Bh (8Bh)



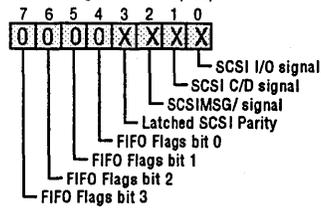
DSTAT Register R 0Ch (8Ch)



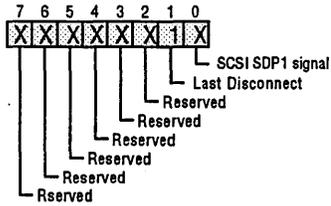
SSTAT0 Register R 0Dh (8Dh)



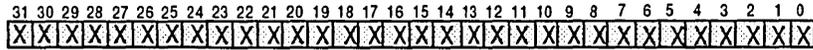
SSTAT1 Register R 0Eh (8Eh)



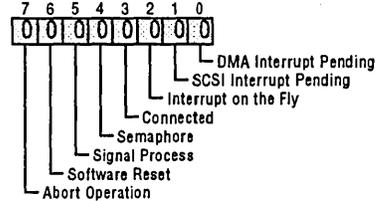
SSTAT2 Register R 0Fh (8Fh)



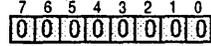
DSA Register R/W 10-13h (90-93h)



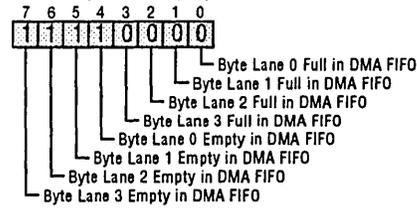
ISTAT Register R/W 14h (94h)



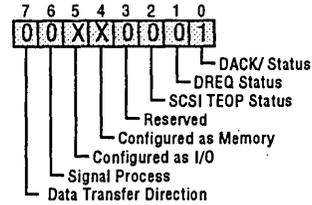
CTEST0 Register R/W 18h (98h)



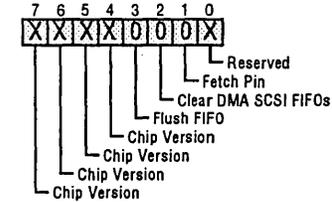
CTEST1 Register R 19h (91h)



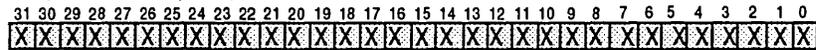
CTEST2 Register R 1Ah (9Ah)



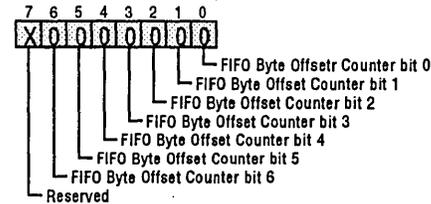
CTEST3 Register R/W 1Bh (9Bh)



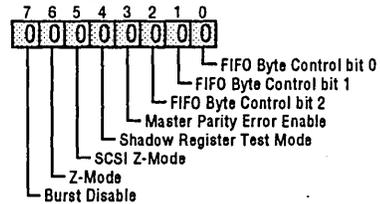
TEMP Register R/W 1C-1Fh (9C-9Fh)



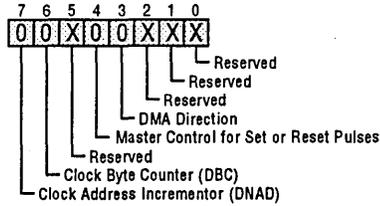
DFIFO Register R/W 20h (A0h)



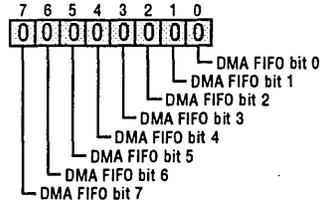
CTEST4 Register R 21h (A1h)



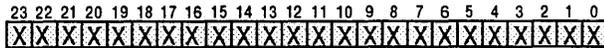
CTEST5 Register R/W 22h (A2h)



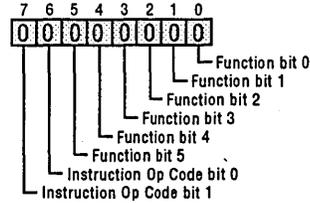
CTEST6 Register R/W 23h (A3h)



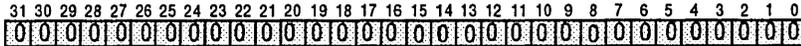
DBC Register R/W 24-26h (A4-A6)



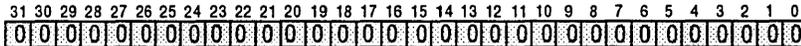
DCMD Register R/W 27h (A7)



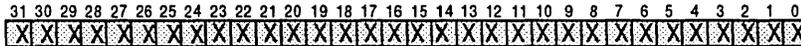
DNAD Register R/W 28-2Bh (A8-ABh)



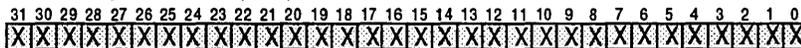
DSP Register R/W 2C-2Fh (AC-AFh)

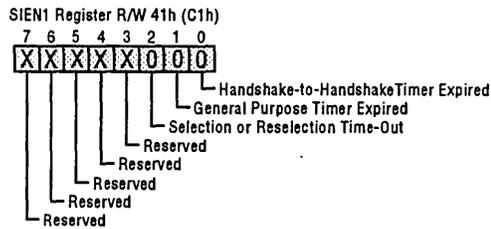
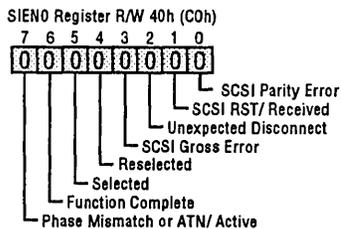
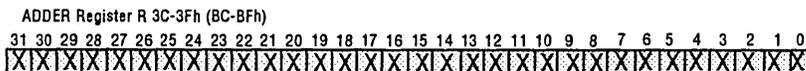
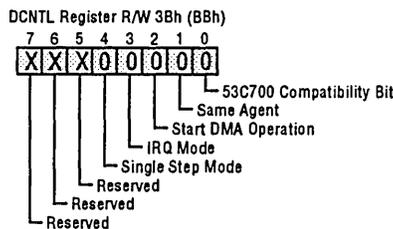
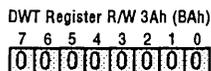
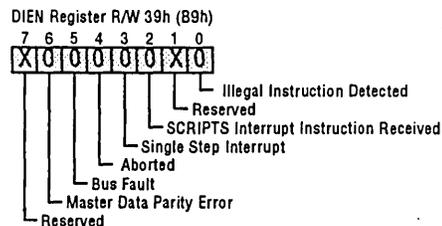
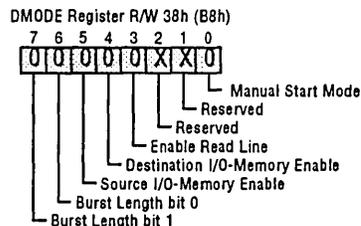


DSPS Register R/W 30-33h (B0-B3h)

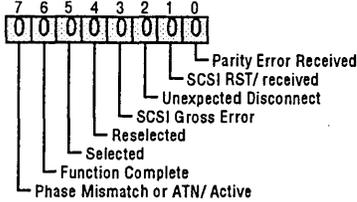


SCRATCHA Register R/W 34-37h (B4-B7)

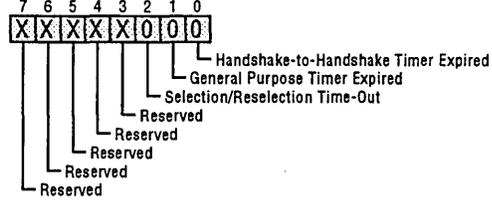




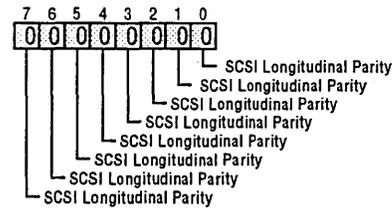
SIST0 Register R 42h (C2h)



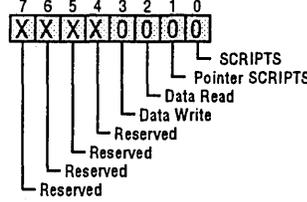
SIST1 Register R 43h (C3h)



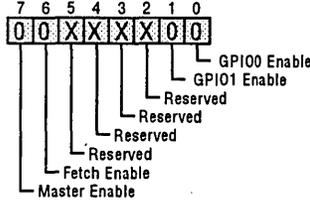
SLPAR Register R/W 44h (C4h)



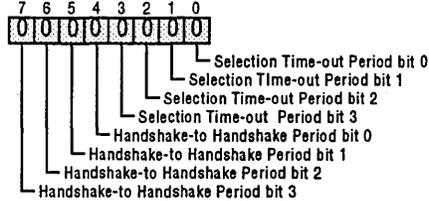
Memory Access Control Register R/W 46h (C6h)



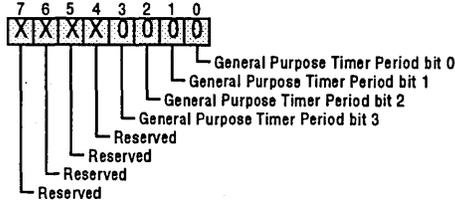
General Purpose Pin Control Register R/W 47h (C7h)



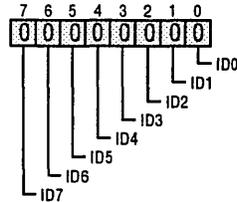
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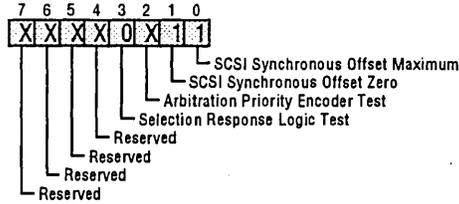
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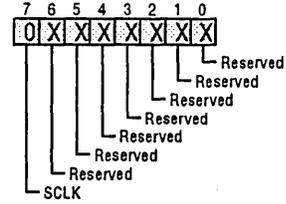
RESPID Register R/W 4Ah (CAh)



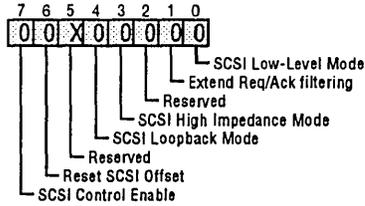
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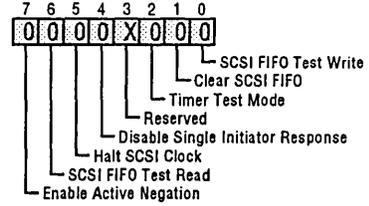
STEST1 Register R 4Dh (CDh)



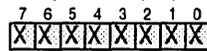
STEST2 Register R/W 4Eh (CEh)



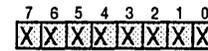
STEST3 Register R/W 4Fh (CFh)



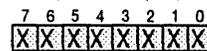
SIDL Register R 50h (D0h)



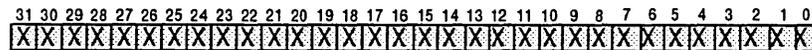
SODL Register R/W 54h (D4h)



SBDL Register R 58h (D8h)

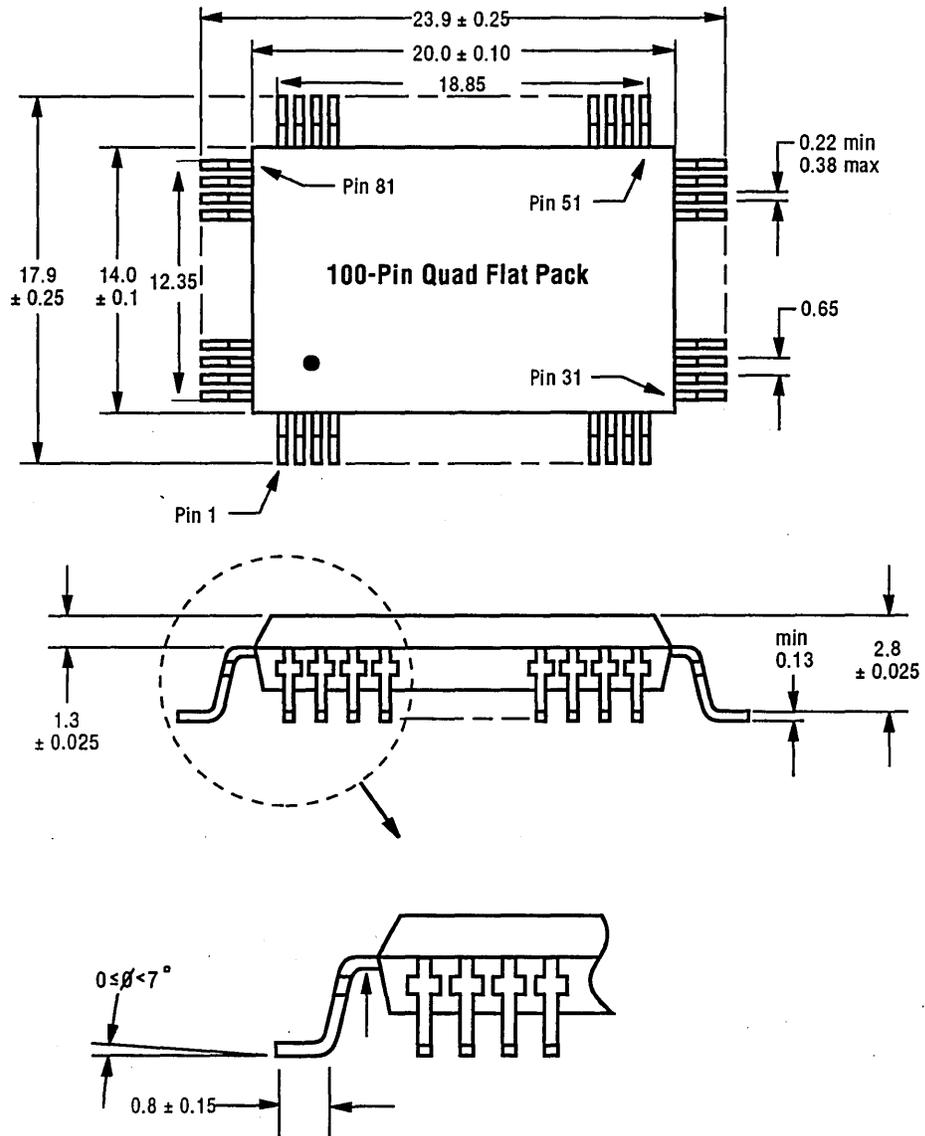


SCRATCHB Register R/W 5C-5Fh (DC-DFh)





Appendix B  
Mechanical Drawing





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# Index

## A

active negation 1-1  
Address and Data 4-3  
Arbitration 4-5

## B

Block Diagram 1-4

## D

Data Paths 2-4  
DC Electrical Characteristics 1-1  
DMA Core 2-1

## E

Error Reporting 4-5

## F

Features Summary 1-2

## I

Interface Control 4-4

## L

Loopback Mode 2-2

## O

Operating Register Addresses and Descriptions 5-1  
Optional Interface 4-7

## P

Parity Options 2-2  
PCI Addressing 3-1  
    Device Identification 3-2  
    PCI Bus Commands and Encoding Types 3-1  
Pin Diagram 4-1  
Power and Ground Pins 4-2

## R

Register Address Map 5-3

## S

SCRIPTS Processor 2-1  
SCSI Bus Interface 2-5  
SCSI Core 2-1  
  
SCSI Signals 4-6  
SDMS  
    SCSI Device Management System 1-1  
System Pins 4-3

## T

Termination 2-6  
TolerANT Technology 1-1



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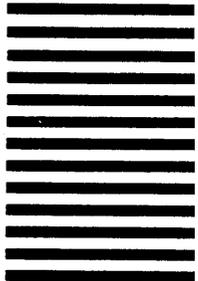
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