MAGNETIC TAPE CASSETTE/CARTRIDGE CONTROLLER

USERS' MANUAL

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NEC MICROCOMPUTERS, INC.

uPD371

MAGNETIC TAPE CASSETTE/CARTRIDGE

USERS' MANUAL

June 9, 1977

The NEC uPD371 is a high performance N-Channel LSI tape cassette/cartridge controller designed to interface between most cassette or cartridge tape drives and most microprocessors or minicomputers.

FEATURES
- Compatible with ANSI, ECMA and ISO standards
- Also compatible with most other standards
- Hardware CRC generation and verification
- Read after write capability
- High speed file search
- Multiple drive capability
- May read or write on one drive while rewinding or file searching on another
- Maximum Data Transfer rate of 375K bits/sec equivalent to 468 IPS at 800 BPI

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INTRODUCTION

The uPD371 uses the ANSI, ECMA and ISO* standard recording technique of "bi-phase-level encoding". The name is usually shortened to "phase encoding".

In phase encoding a logic one is encoded as a positive transition. A logic zero is encoded as a negative transition. These data transitions are made to occur at intervals with a constant period. Halfway between data transitions, a "phase" transition may be required to establish the proper polarity for the succeeding data transition. An example of phase encoded data is shown in Line 1 of Figure 4.

Data is usually recorded on magnetic tape in blocks called "records". Records are separated from each other by regions of erased tape called "inter record gaps" or just "gaps". The lengths of both records and gaps depend on the recording standard used. The uPD371 can adapt to any record or gap length.

ANSI, ECMA and ISO records are made up of 8-bit bytes in which the least significant bit is recorded first. The first byte of a record (the "preamble") is an AA hex. The preamble is followed by 1-256 "data" bytes. The data bytes are followed by two "CRC" (Cyclic Redundancy Character) bytes. The CRC bytes are followed by the last byte of the record (the "postamble") which is also an AA hex. The postamble is followed by an inter record gap. The uPD371 can write records which are completely compatible with the ANSI, ECMA and ISO standard, but it is not limited to this standard. See Other Formats in the SOFTWARE section.

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* ANSI = American National Standards Institute
1430 Broadway, New York, NY 10018
USA
Document Number ANSI X3.48-1977

ECMA = European Computer Manufacturers' Association
114 Rue du Rhone
CH 1204 Geneva, Switzerland
Document Number ECMA 34

ISO = International Organization for Standardization
c/o American National Standards Institute
Document Number ISO 3407-1976

All three documents are identical except for some minor differences in describing physical dimension tolerances.

Most tape drive manuals contain amplified discussions of encoding techniques and recording formats. The interested reader is referred to these sources for further information.

Figure 1 shows a uPD371 based tape controller in block diagram form. The workload of operating the tape drive (or tape drives) is shared between the uPD371 hardware and the processor software. The uPD371 hardware encodes and decodes data for the processor program, calculates the CRC during write operations, verifies the CRC during read operations, informs the processor program when to send data bytes during write operation and when to read bytes during read operations, converts tape drive status signals into register bit levels which may be read by the processor program and converts software commands into signals which may be understood by the tape drive(s).

The software responsibility is usually divided between two sets of programs -- the Drive Handling Routines and the Operating System. The Drive Handling Routines must transfer read or write data when requested to do so by the uPD371, monitor drive performance and issue tape motion commands. The Operating System determines the areas of memory from which write data is taken and into which read data is stored and what use is made of the data.

A discussion of Cassette/Cartridge Operating Systems is beyond the scope of this manual. Drive Handling Routines are described in the SOFTWARE section. Complete listings are included for a uPD8080A microprocessor as an example of typical Drive Handling Routines. The uPD371 hardware is described in the INPUT/OUTPUT SIGNALS and ADDRESSABLE INTERNAL REGISTERS sections. Schematics and discussions of typical controllers are given in the TAPE CASSETTE/CARTRIDGE CONTROLLER EXAMPLES section.

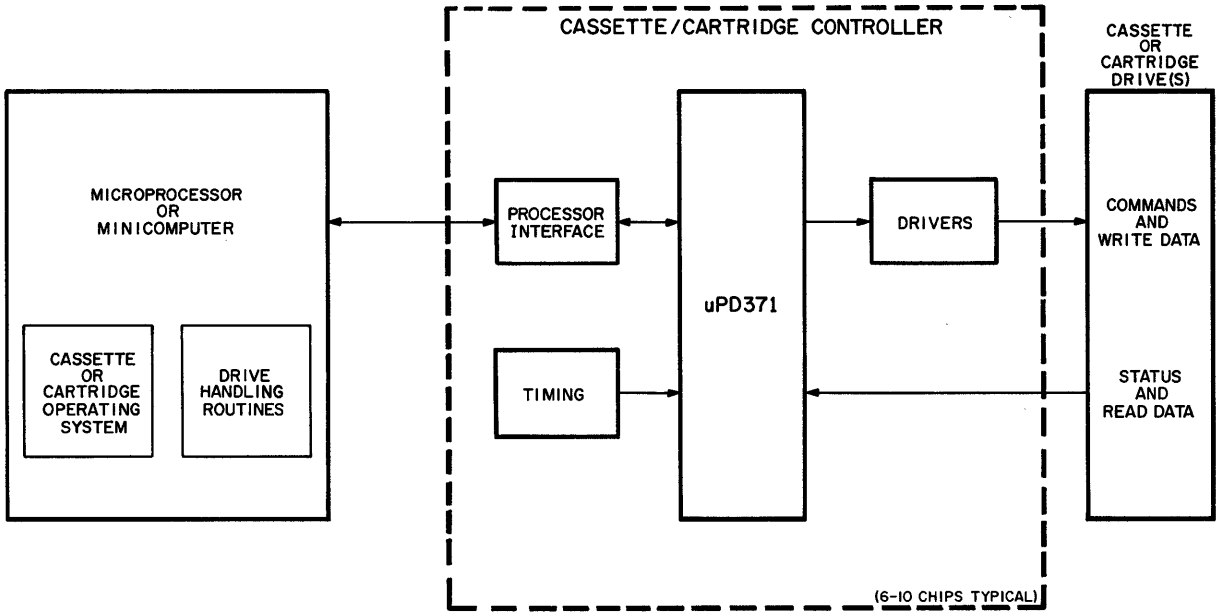


FIGURE 1
uPD371 CASSETTE/CARTRIDGE CONTROLLER

INPUT/OUTPUT SIGNALS

INTRODUCTION

Figure 2 shows the input/output signals of the uPD371 grouped according to function.

These signals are described below in the functional sequence of Figure 2 rather than in numerical sequence.

PROCESSOR INTERFACE

Reset

Pin 40 RST (Reset)

A logic one at pin 40 causes a general reset of the uPD371. The effect is the same as a logic one at RST-bit 7 of Write Register 0 (WR0). For a list of signals and registers affected, see bit 7, WR0 in the ADDRESSABLE INTERNAL REGISTERS section.

Register Select Commands and Data Bus

Pin 11	W/R	(Register Write/Read Select)
Pin 12	DS	(Register Data Strobe)
Pins 13-15	RS0-RS2	(Register Address)
Pins 3-10	DB0-DB7	(Data Bus)

W/R, DS and RS0-RS2 control Data Bus transfers between the uPD371 and the processor as follows:

Writing into a uPD371 register

When W/R is a logic one, information the processor places on DB0-DB7 is written into the uPD371 WRITE REGISTER selected by RS0-RS2. The information is written at the time of the trailing edge of each Ø2 which occurs while DS is a logic one.

Reading from a uPD371 register

When W/R is a logic zero, information from the uPD371 READ REGISTER selected by RS0-RS2 is placed on DB0-DB7 to be read by the processor. The information remains on DB0-DB7 as long as DS is a logic one. See uPD371 SIGNAL TIMING DIAGRAM, Figure 12 for exact timing.

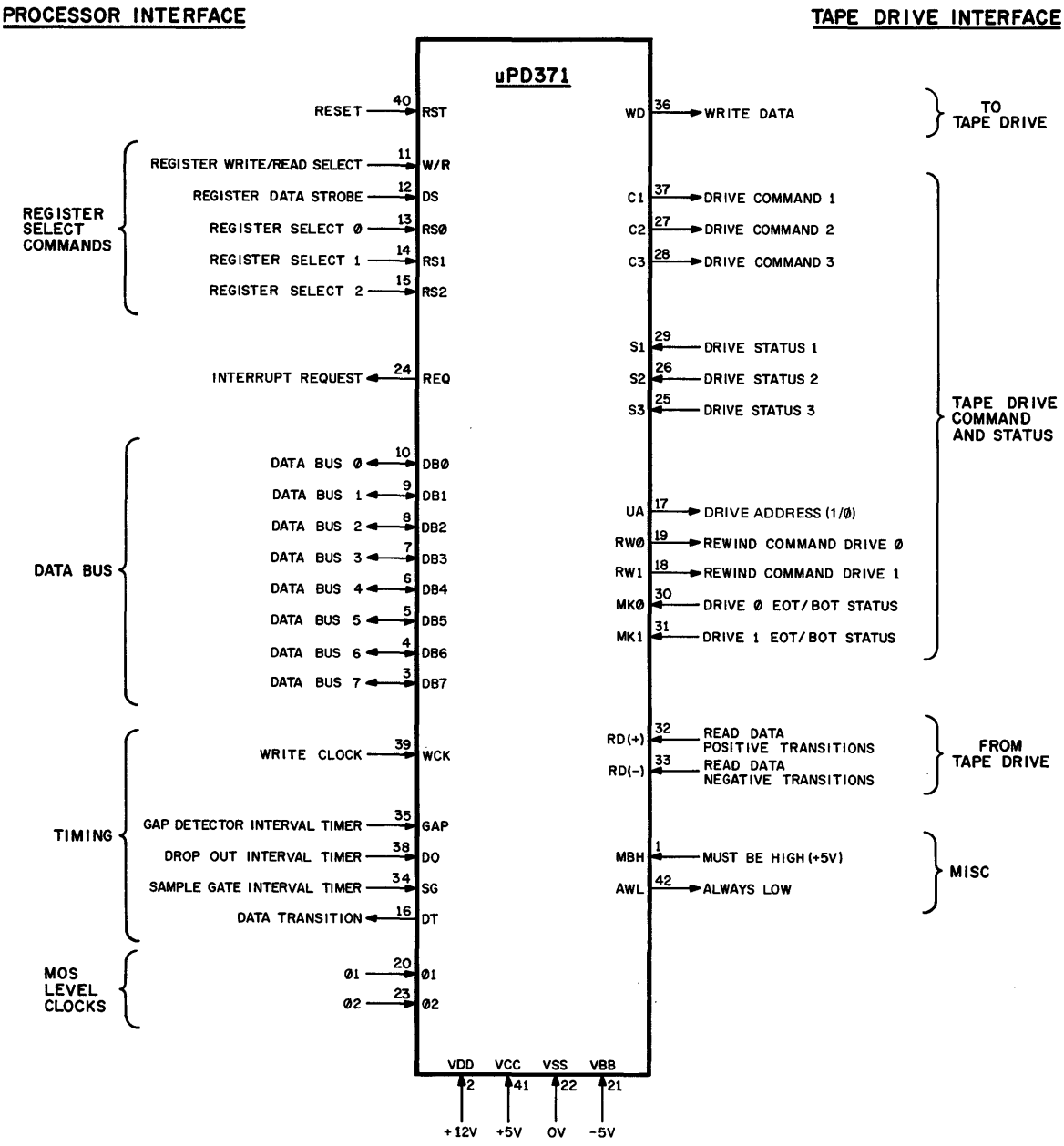


FIGURE 2
INPUT/OUTPUT SIGNALS

Interrupt Request

Pin 24 REQ (Interrupt Request)

The uPD371 may be operated with either interrupt or polling techniques. If the interrupt technique is chosen, REQ should be connected to the interrupt request input of the processor.

As shown in Figure 3, there are three sources of interrupt: READ BUFFER FULL, WRITE BUFFER EMPTY and GAP DETECTION.

READ BUFFER FULL indicates that an 8-bit byte has been read from tape, assembled in the READ SHIFT REGISTER and transferred to the READ BUFFER REGISTER (RR2) where it may be read by the processor program.

WRITE BUFFER EMPTY indicates that the processor program may transmit a new data byte to the WRITE BUFFER REGISTER (WR2) to be written on tape. WRITE BUFFER EMPTY becomes true when the previous data byte has been transferred from the WRITE BUFFER REGISTER to the WRITE SHIFT REGISTER from which the data is removed one bit at a time to be written on tape.

GAP DETECTION (GAP, pin 35) indicates that the beginning of an inter record gap has passed the tape drive read head.

The relationship between the various enabling, resetting, flag and request signals in the interrupt request logic is shown in Figure 3. Each of these signals is either controlled or indicated by a bit in one of the uPD371 ADDRESSABLE INTERNAL REGISTERS and each is described in the ADDRESSABLE INTERNAL REGISTER section.

Timing Signals

The user must provide four timing signals to the uPD371--one for write operations and three for read operations. Each is defined in terms of T, where T is the period between successive data transitions in the phase encoded data written onto or read from the tape drive. For instance, if the tape speed is 10 IPS and the density is 800 BPI, then T=1/8000sec or 125usec.

Pin 39 WCK (Write Clock)

WCK determines the WRITE DATA (WD, pin 36) transfer rate. WCK should have a period of 0.5T. Any duty cycle is allowed as long as WCK remains in each logic state for at least two 01 clock periods.

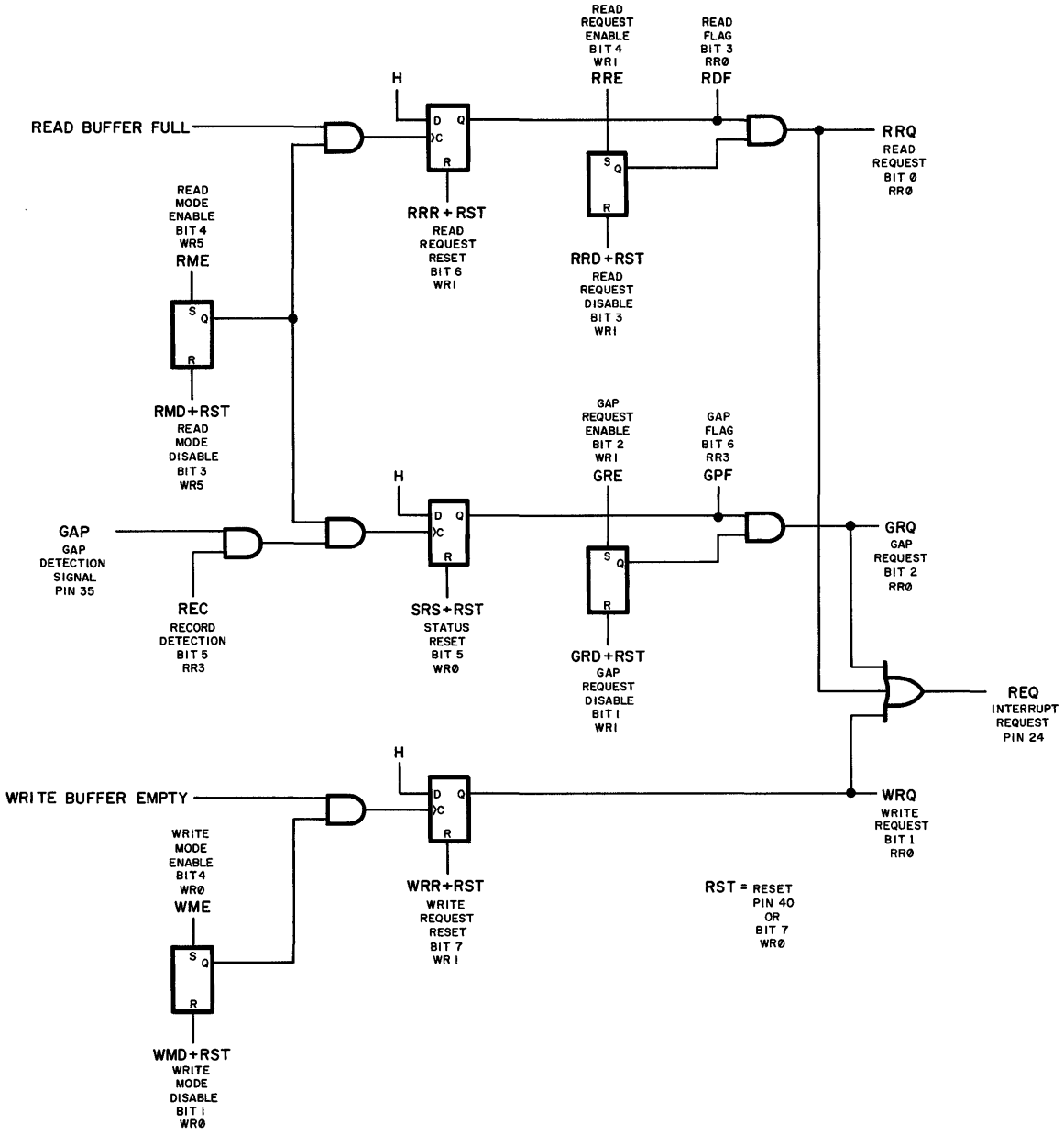


FIGURE 3
uPD371 INTERRUPT REQUEST LOGIC
FUNCTIONAL BLOCK DIAGRAM

Pin 16 DT (Data Transition)

DT is a pulse provided by the uPD371 to be used in the generation of the three read timing signals -- SG, pin 34; DO, pin 38; and GAP, pin 35. DT occurs at each data transition in the data read from tape. DT is not generated at phase transitions, so DT has a period equal to T. DT is one Ø1 cycle in width and occurs during the first Ø1 cycle time following each data transition.

Pin 34 SG (Sample Gate)

Phase encoded data consists of both data and phase transitions. See Line 1 of Figure 4. The phase transitions are artifacts of the encoding process. Only the data transitions contain useful information. The phase transition information is removed from the read data stream by placing a suitable timing signal at the SG (Sample Gate) input, pin 34.

Read data as received by the uPD371 consists of RD(+) pulses at each positive transition (both phase and data transitions) and RD(-) pulses at each negative transition of the phase encoded data from the tape. See Lines 2 and 3 of Figure 4. Note that RD(+) or RD(-) pulses due to phase transitions occur .5Tusec after DT, Line 4 of Figure 4, and data transitions occur Tusec after DT.

The internal sample gate, Line 6 of Figure 4, is "closed" by each DT. As long as the sample gate is closed, all RD(+) or RD(-) pulses are ignored. The internal sample gate is "opened" by a positive transition at the SG input. If SG is made to go positive .75Tusec after DT, the sample gate is closed long enough to gate out a phase (RD(+) or RD(-) pulse at .5T and open in time to receive the next data pulse at T. The gated RD(+) and RD(-) signals are shown in Lines 7 and 8 of Figure 4.

Note that the sample gate is opened by a positive transition at SG. The time of the negative transition is immaterial so long as SG remains in each logic state for at least two Ø1 cycles.

SG may be generated by a one-shot (as in Figure 8), a digital interval timer (as in Figure 9), or in unusually critical applications, by a phase-locked loop.

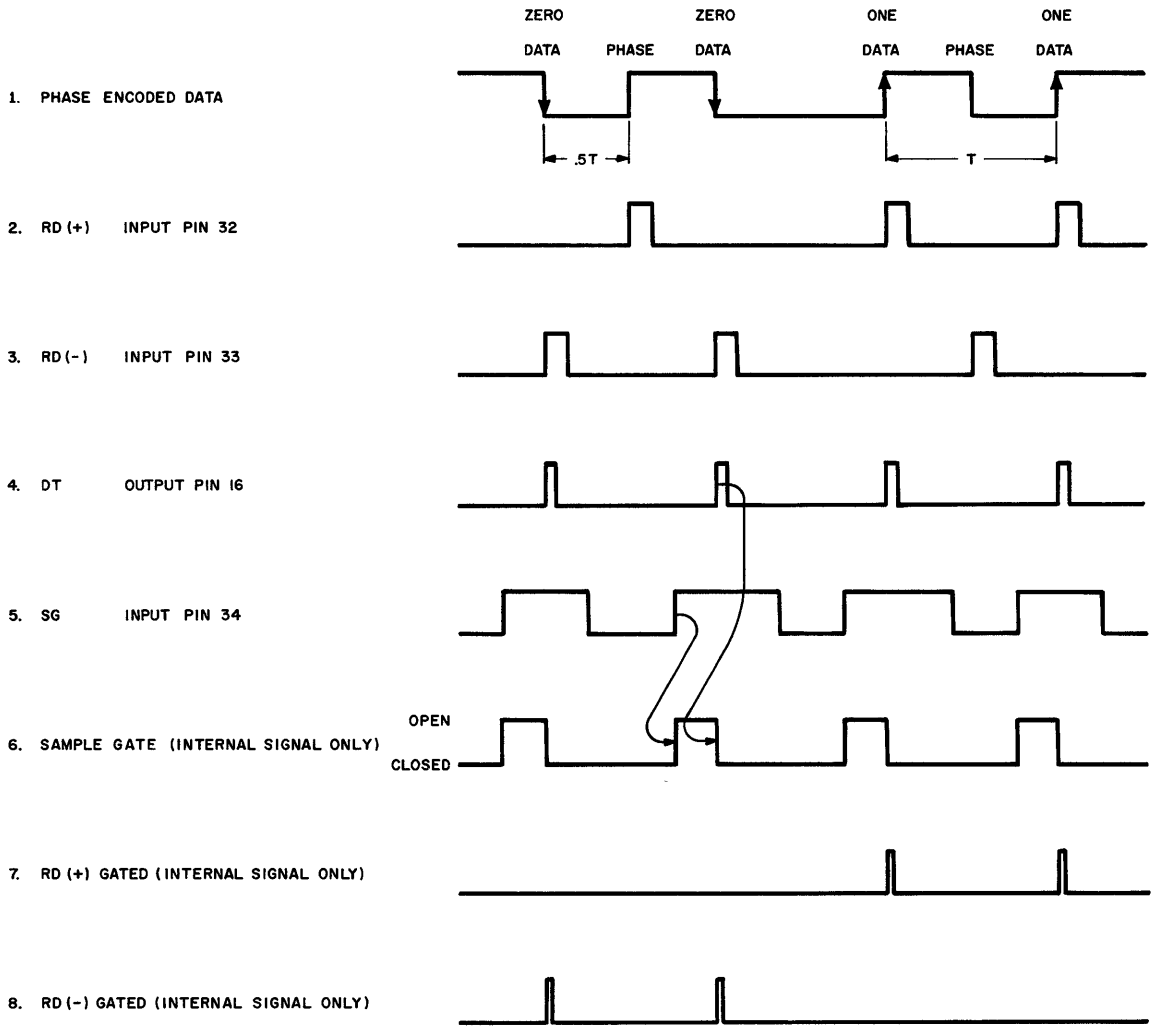


FIGURE 4
SG (SAMPLE GATE) TIMING

Pin 38 DO (Drop Out)

Pin 35 GAP (Gap Detection)

A positive transition should be made at DO whenever a DT pulse stream ceases for a period of 1.5Tusec. A positive transition should be made at GAP whenever a DT pulse stream ceases for a period of 4Tusec.

A positive transition at DO followed by further DT pulses indicates a Drop Out Error (at least one DT missing from the data stream). See DOE, Drop Out Error, bit 3 of RR3.

A positive transition at GAP indicates that the beginning of an inter record gap has passed the tape drive read head. See GPF, Gap Flag, bit 6 of RR3 and GRQ, Gap Request, bit 2 of RRØ.

DO and GAP may be generated by retriggerable one-shots (as in Figure 8) or by their digital analogies (as in Figure 9).

Pin 2Ø Ø1

Pin 23 Ø2

Ø1 and Ø2 are MOS level (12V) clock pulses. The timing of Ø1 and Ø2 is shown in Figure 12. The Ø1 and Ø2 clock pulses of an 8Ø8ØA microprocessor are suitable for the uPD371; and if the 8Ø8ØA and uPD371 are on the same board and located near each other, they may share the Ø1 and Ø2 outputs of an 8224 clock generator chip. If the 8Ø8ØA and uPD371 are located far apart or on separate cards, the 8224 clock outputs should be converted to TTL levels, transmitted to the uPD371 vicinity and reconverted to MOS level by a 75361A or equivalent chip.

Ø1 and Ø2 may be generated by TTL one-shot or digital logic triggered by the clock(s) of other microprocessors such as the 8Ø85, Z8Ø, 68ØØ, etc., and then converted to MOS level. Ø1 and Ø2 need not by synchronized with the processor clock(s), but controller design and debugging are much easier when they are.

TAPE DRIVE INTERFACE

Write Data

Pin 36 WD (Write Data)

Phase encoded data to be written on tape leaves the uPD371 at pin 36.

Tape Drive Commands and Status

Pin 37 C1 (Tape Drive Command 1)

Pin 27 C2 (Tape Drive Command 2)

Pin 28 C3 (Tape Drive Command 3)

C1, C2 and C3 are general purpose tape drive commands. C1, C2 and C3 are set and reset by the software manipulation of bits 5, 6 and 7, respectively, in WR3. Since C1, C2 and C3 are defined by software, they may be configured for any purpose. Typical uses for C1, C2 and C3 are WRITE ENABLE, FORWARD and REVERSE; but the commands required by tape drives differ considerably from manufacturer to manufacturer. An equally typical set of commands might be WRITE ENABLE, FORWARD/REVERSE and GO/STOP. The uPD371 can adapt to any cassette or cartridge drive command set by a slight modification of software. For drives or multiple drive systems requiring more than three commands, see Figure 10.

Pin 29 S1 (Tape Drive Status 1)

Pin 26 S2 (Tape Drive Status 2)

Pin 25 S3 (Tape Drive status 3)

S1, S2 and S3 are general purpose tape drive status inputs. Their logic levels are indicated by bits 3, 4 and 7 of RR1, respectively. Typical tape drive status signals are WRITE PERMIT, CASSETTE IN PLACE and SIDE, but tape drive status signals also vary considerably from manufacturer to manufacturer. The uPD371 can adapt to any tape drive status signal set with a slight change in software. For drives or multiple drive systems requiring more than three status inputs, see Figure 10.

Pin 17 UA (Unit Address) See WR6, bit Ø

Pin 19 RWØ (Rewind Command for Drive Ø) See WR3, bit 3

Pin 18 RWl (Rewind Command for Drive l) See WR3, bit 3

Pin 3Ø MKØ (Drive Ø EOT/BOT Status) See RRl, bits 5,6

Pin 31 MKl (Drive 1 EOT/BOT Status) See RRl, bits 5,6

Read Data

Pin 32 RD(+) Read Data Positive Transitions

Pin 33 RD(-) Read Data Negative Transitions

The read logic of some tape drives completely reconstitutes the phase encoded data read from tape and transmits the read data from a single output. This type of read data signal is similar to that shown in Line 1 of Figure 4.

The read logic of other tape drives, transmits read data from two outputs. These output signals are similar to those labled RD(+) and RD(-), Lines 2 and 3 of Figure 4.

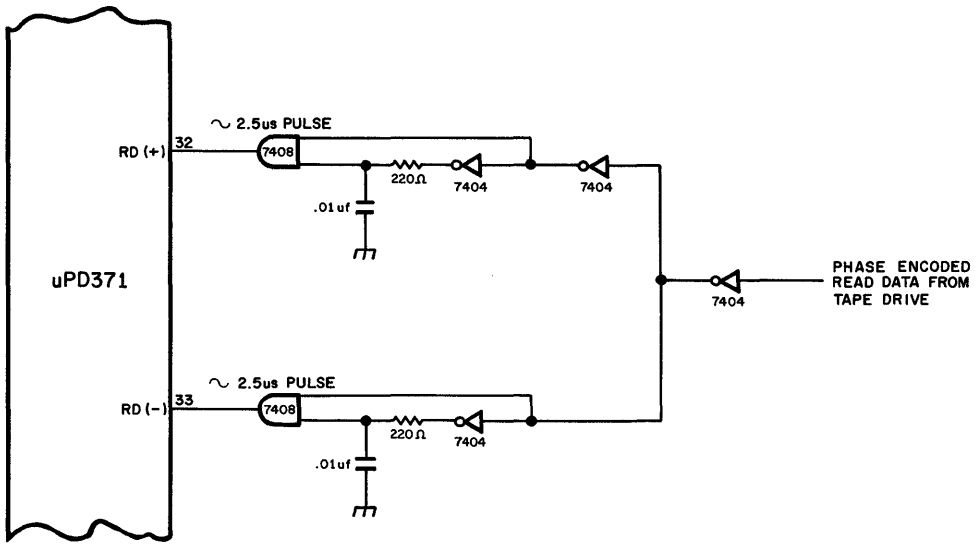
The uPD371 directly accepts the RD(+) and RD(-) type of read data signals at pins 32 and 33. Tape drives with a single phase encoded output signal require a simple conversion circuit such as the one in Figure 5.

Miscellaneous

Pin 1 MBH (Must Be High)

Pin 42 AWL (Always Low)

MBH must be tied to the VCC (+5V) supply. AWL is a logic low output under all normal operating conditions of the uPD371.



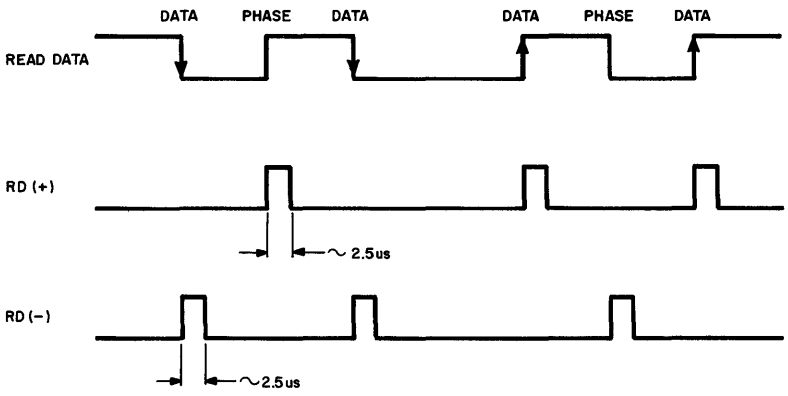


FIGURE 5
CONVERSION OF PHASE ENCODED DATA TO RD(+) AND RD(-)
FOR TAPE DRIVES WITH PHASE ENCODED OUTPUT

ADDRESSABLE INTERNAL REGISTERS

INTRODUCTION

From the point of view of the processor program, the uPD371 makes the tape drive (or multiple drive system) appear as ten addressable registers. The program controls the drive(s) and transmits data to be written on tape by manipulating bits in the six uPD371 Write Registers. The program senses the status of the drive(s) and reads data stored on tape by reading bits from the four uPD371 Read Registers.

Data transfers to and from the uPD371 addressable internal registers are controlled by the signals W/R, DS and RSØ-RS2. These signals are discussed in the INPUT/OUTPUT SIGNALS section.

The address of each register and a mnemonic abbreviation for each register bit are shown in Figure 6. The function initiated, controlled or sensed by each register bit is described below.

WRITE REGISTERS

Write Register Ø (WRØ)

WRØ-Bit Ø GNT (Gap Noise Tolerance)

When GNT is set to a logic one, the uPD371 read logic ignores inter record gap noise bursts less than 8 bits long. When GNT is set to a logic zero, the uPD371 ignores noise bursts less than 16 bits longs.

Gap noise originates during the writing process as follows: After writing the last record of a write operation, the tape is braked to a halt. When tape motion is completely stopped, the write current is turned off. At some later time, the write current may be turned on again and the tape moved forward to write more records. If the tape position shifts forward, even a very small distance, while the write current is off, a noise burst will be left in the gap. Some drives leave noise at the write-current-off position even when no tape position shift occurs.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS2	RS1	RS0		7	6	5	4	3	2	1	0
WRITE REGISTERS												
1	0	0	0	WR0	RST	MBL	SRS	WME	WCR	X	WMD	GNT
1	0	0	1	WR1	WRR	RRR	X	RRE	RRD	GRE	GRD	X
1	0	1	0	WR2	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
1	0	1	1	WR3	C3	C2	C1	RRI	RW	X	X	X
1	1	0	1	WR5	X	X	X	RME	RMD	X	X	X
1	1	1	0	WR6	X	X	X	X	X	X	X	UA
READ REGISTERS												
0	0	0	0	RR0	AWH	AWL	C2	C3	RDF	GRQ	WRQ	RRQ
0	0	0	1	RR1	S3	MK	MKF	S2	S1	RW	C1	UA
0	0	1	0	RR2	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
0	0	1	1	RR3	WD	GPF	REC	CRE	DOE	COR	NBR	NAR

X = NOT USED

FIGURE 6
ADDRESSABLE INTERNAL REGISTERS

It is more difficult to control the write process in such a way as to completely eliminate gap noise than it is to ignore the noise while reading. So, most cassette and cartridge format specifications allow noise to be left in inter record gaps and require that the controller read logic tolerate the noise.

The most common method used to ignore gap noise is to disable the read logic during the time when noise is expected. In many controllers this is the only technique used, but it is effective only if the position of the noise is known.

The uPD371 allows the user to disable the read logic for any desired period; but in addition, counts the number of bits in each group of flux transitions encountered while the read logic is enabled. If the number of bits in the group is less than 8 or 16 (depending on the state of GNT), the group is considered a noise burst and no data is transferred. If the noise occurs in the gap before a record is encountered, NBR (Noise Before Record, bit 1 of RR3) is set to a one. If the noise occurs in the gap after the record is read, NAR (Noise After Record, bit Ø of RR3) is set to a one. When 8 or 16 bits have been counted (depending on the state of GNT), the group of flux transitions is assumed to be a legitimate data record. The uPD371 signals this event by setting REC (Record Detect, bit 5 of RR3) to a one.

WRØ-Bit 1 WMD (Write Mode Disable)

See bit 4 of WRØ (WME-Write Mode Enable)

WRØ-Bit 2 Not used.

WRØ-Bit 3 WCR (Write CRC)

In order to write the two CRC bytes, WCR must be set high while the last data byte of a record is being written. At the completion of that byte, information to be written on tape is taken from the Write CRC Generator rather than from the Write Shift Register. See Figure 7.

Write data will continue to be taken from the Write CRC Generator as long as WCR remains high. So, WCR must be set low again during the writing of the second CRC byte. Then, at the completion of that byte, write data is again taken from the Write Shift Register.

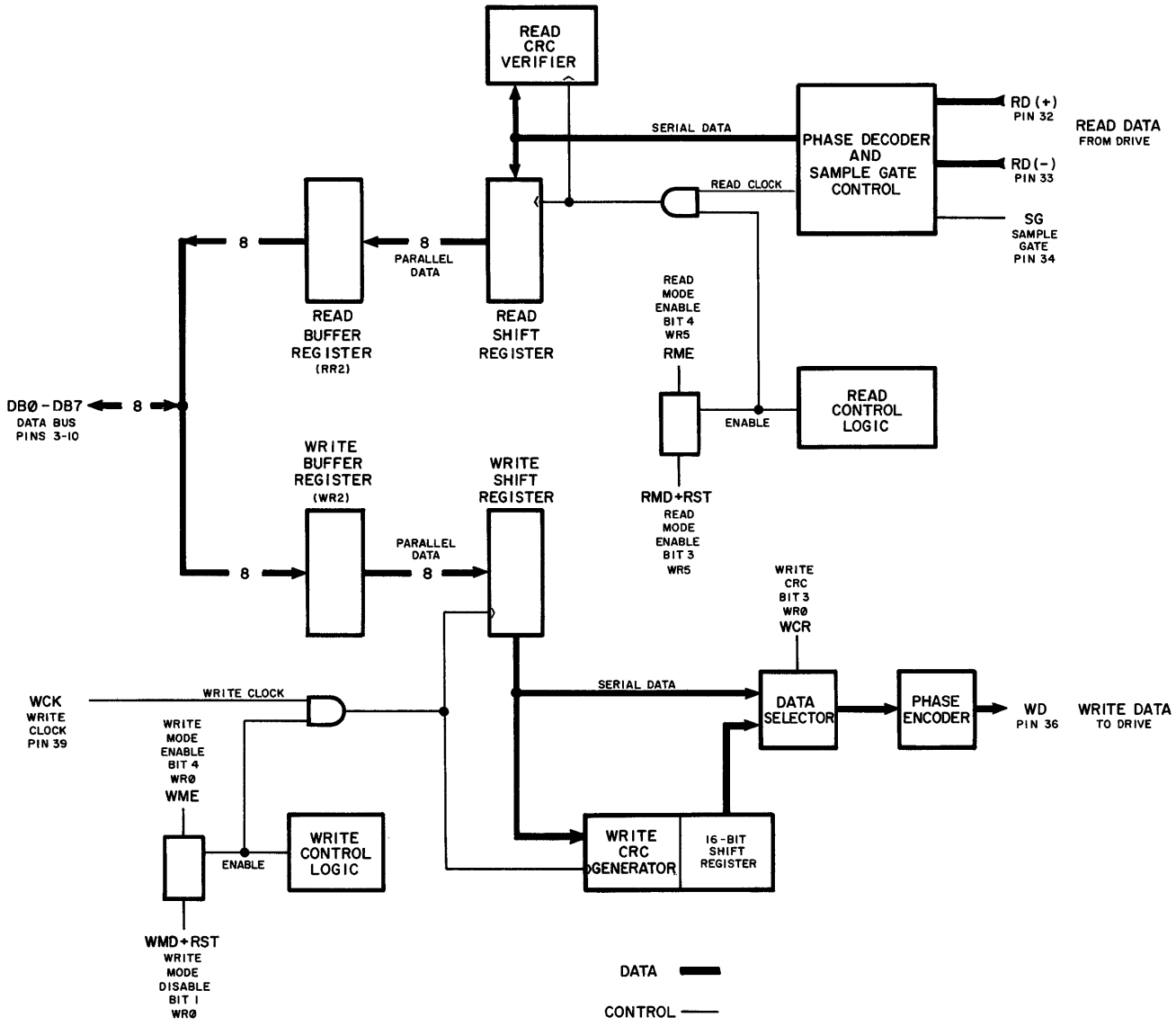


FIGURE 7
uPD371 READ AND WRITE DATA PATHS

WRØ-Bit 4 WME (Write Mode Enable)

WME enables and WMD (bit 1-WRØ) disables the write mode. While the write mode is enabled, the write data path logic (See Figure 7) and the write request logic (see Figure 3) are activated. When the write mode is enabled, the contents of WR2 are transferred into the Write Shift Register and WRQ (Write Request, bit 1 of RRØ) becomes true. The data is shifted one bit at a time from the Write Shift Register, through the Phase Encoder Logic and is written on tape.

When 8 bits have been clocked from the Write Shift Register, the new contents of WR2 are transferred to the Write Shift register and WRQ again becomes true.

This process repeats itself until the write mode is disabled.

WRØ-Bit 5 SRS (Status Reset)

A logic one at SRS resets the following:

The read error status bits -- NAR, NBR, COR, DOE and CRE (bits Ø-4 of RR3);

REC (Record Detection -- bit 5 of RR3);

GPF (Gap Flag -- bit 6 of RR3);

GRQ (Gap Request -- bit 2 of RRØ);

The contents of the Read Shift Register.

SRS may be used to reset the above status signals and data bits while reading or writing "on the fly", that is, without stopping between records. The more powerful General Reset, RST (bit 7 of WRØ) used in the software listings in this manual cannot be used "on the fly", since it would also reset the motion commands.

WRØ-Bit 6 MBL (Must Be Low)

Bit 6 must be low during each transfer into WRØ.

WRØ-Bit 7 RST (Reset)

A logic one at RST, bit 7 of WRØ, causes a general reset of the uPD371. The effect is exactly the same as that of a positive pulse at RST, pin 1.

The following register bits are affected:

WRØ GNT is set to zero (16 bit noise tolerance) the Write Mode is disabled and WCR is reset.

WR1 Gap Request and Read Request are disabled.

WR2 All write data bits are set to zero.

WR3 RW is not changed (see RW-bit 3 of WR3); RRI is reset; C1, C2 and C3 are reset.

WR5 The Read Mode is disabled.

WR6 UA is set to zero.

RRØ All bits, except AWH, are set to zero.

RR1 UA, C1 and MKF are set to zero (RW, S1, S2, MK and S3 are unaffected).

RR2 All Read Data bits are set to zero.

RR3 All bits are set to zero.

The following output signals are set to zero:

WD, pin 36

C1, pin 37

C2, pin 27

C3, pin 28

UA, pin 17

REQ, pin 24

The commands, RWØ and RW1 are unchanged. See RW-bit 3 of WR3.

Write Register 1 (WR1)

WR1-Bit Ø Not used.

WR1-Bit 1 GRD (Gap Request Disable)

WR1-Bit 2 GRE (Gap Request Enable)

GRE enables and GRD disables the gap interrupt request. While the gap interrupt request is enabled, a positive transition at GAP, pin 35 (if a legitimate record has been detected -- see GNT, bit Ø of WRØ), sets both the Gap Request (GRQ, bit 2 of RRØ) and the Interrupt Request (REQ-pin 24) to a true level. See Figure 3.

WR1-Bit 3 RRD (Read Request Disable)

WR1-Bit 4 RRE (Read Request Enable)

RRE enables and RRD disables the read interrupt request. While the read interrupt request is enabled, the Read Request (RRQ, bit Ø of RRØ) and the Interrupt Request (REQ-pin 24) are set true each time a complete byte is read, assembled in the read shift register and transferred to the Read Buffer Register, RR2. See Figures 3 and 7.

WR1-Bit 5 Not used.

WR1-Bit 6 RRR (Read Request Reset)

A logic one at RRR resets the Read Request, RRQ (bit Ø-RRØ). See Figure 3.

WR1-Bit 7 WRR (Write Request Reset)

A logic one at WRR resets the Write Request, WRQ (bit 1-RRØ). See Figure 3.

Write Register 2 (WR2)

WR2-Bits Ø-7 WDØ-WD7 (Write Buffer Register)

A data byte to be written on tape should be transferred into WR2 each time WRQ (Write Request -- bit 1 of RRØ) becomes true. See Figure 7.

The preamble code should be transferred into WR2 before the Write Mode is enabled (WRE-bit 4 of WRØ).

If the processor does not update the data pattern in WR2 while writing, the previously existing data pattern is not cleared, but is repeatedly written on tape.

Write Register 3 (WR3)

WR3-Bit Ø Not used.

WR3-Bit 1 Not used.

WR3-Bit 2 Not used.

WR3-Bit 3 RW (Rewind)

WR3-Bit 4 RRI (Rewind Reset Inhibit)

If UA (Unit Address -- bit Ø of WR6) has previously been set to a logic zero when a logic one is transmitted to RW, the logic level at RWØ, pin 19, goes high and stays high.

If UA has previously been set to a logic one when a logic one is transmitted to RW, the logic level at RW1, pin 18, goes high and stays high.

RWØ and RW1 may be used as rewind commands for two separate tape drives. The drive affected is determined by the setting of UA.

RWØ and RW1 are not reset by transmitting a zero to RW, nor are they reset by RST (Reset -- bit 7 of WRØ) or SRS (Status Reset -- bit 5 of WRØ). In fact, if RRI is set to a logic one, they cannot be reset at all. If RRI is set to a logic zero, RWØ is reset by a positive transition at MKØ (Marker Zero, pin 3Ø), and RW1 is reset by a positive transition at MK1 (Marker One, pin 31). MKØ and MK1 should be connected to the EOT/BOT output of drive zero and drive one respectively.

The intention of this scheme is to allow rewinding to be initiated on either drive under program control; but once initiated, rewinding continues to the load point without program intervention. Consequently, one drive may be rewinding automatically while the other is reading or writing. When RRI is set to a logic one, rewinding proceeds to the hub instead of to the load point.

Of course, this technique requires a drive with a REWIND command input. Drives which require a REVERSE and HIGH SPEED command to rewind must be rewound under program control. Both types of drives are discussed in the TAPE CASSETTE/CARTRIDGE CONTROLLER EXAMPLES section.

WR3-Bit 5 C1 (Command One)

WR3-Bit 6 C2 (Command Two)

WR3-Bit 7 C3 (Command Three)

If C1, bit 5 of WR3, is set to a logic one, the signal level at C1, pin 37, goes high. The signal level at pin 37 remains high until a subsequent data transfer to WR3 resets bit 5 to a logic zero.

Similarly, C2 (bit 6) and C3 (bit 7) control the signal levels at C2 (pin 27) and C3 (pin 28) respectively.

C1, C2 and C3 may be used as tape drive command signals, for instance: FWD/STOP, REV/STOP, FWD/REV, RUN/STOP, HIGH SPEED, DRIVE SELECT and so on.

Write Register 4 Not used.

Write Register 5 (WR5)

WR5-Bit Ø Not used.

WR5-Bit 1 Not used.

WR5-Bit 2 Not used.

WR5-Bit 3 RMD (Read Mode Disable)

WR5-Bit 4 RME (Read Mode Enable)

RME enables and RMD disables the read mode. While the read mode is enabled, data serially read from tape is assembled into 8-bit bytes in the Read Shift Register. See Figure 7.

When a complete 8-bit byte has been assembled, the byte is transferred into the Read Buffer Register, RR2, and RRQ (Read Request -- bit Ø of RRØ) is set true. See Figure 3. The processor program should read RR2 each time that RRQ becomes true.

WR5-Bit 5 Not used.

WR5-Bit 6 Not used.

WR5-Bit 7 Not used.

Write Register 6 (WR6)

WR6-Bit Ø UA (Unit Address)

A logic one transmitted to bit Ø sets UA, pin 17, high. The logic level at pin 17 remains high until a subsequent data transfer to WR6 includes a logic zero in bit Ø.

In a two drive system, the UA signal at pin 17 may be used uninverted, to address drive one and inverted to address drive zero.

The logic level of UA determines which pin issues rewind commands (see RW, bit 3 of WR3) and from which pin, MKØ or MK1, the EOT/BOT signal is read (see MK and MKF, bits 5 and 6 of RR1).

When controlling a single drive or a multiple drive system in which RWØ and RW1 are not used, UA may be used as an additional general purpose command in the same way C1, C2 and C3 are used. In this case, the drive's EOT/BOT signal should be connected to both MKØ and MK1. See Figure 8.

WR6-Bits 1-7 Not used.

READ REGISTERS

Read Register Ø (RRØ)

RRØ-Bit Ø RRQ (Read Request)

RRQ indicates that eight bits of data have been read from the tape, assembled in the READ SHIFT REGISTER and transferred to the READ BUFFER REGISTER (RR2) where they may be read by the processor program. See Figure 7.

RRQ causes an Interrupt Request, REQ, at pin 24. See Figure 3.

In order for RRQ to become true, the Read Mode must be enabled (RME-bit 4, WR5) and the Read Request must be enabled (RRE-bit 4, WR1).

RRQ is reset by RRR (Read Request Reset -- bit 6 of WR1).

RRØ-Bit 1 WRQ (Write Request)

WRQ indicates that the WRITE BUFFER REGISTER (WR2) is empty and that the processor program may transfer into it the next data byte to be written onto the tape. The WRITE BUFFER REGISTER becomes empty when its contents are transferred to the WRITE SHIFT REGISTER. See Figure 7. The data is shifted serially from the WRITE SHIFT REGISTER and phase encoded before leaving the uPD371 at WD, pin 36.

WRQ causes an Interrupt Request, REQ, at pin 24. See Figure 3.

In order for WRQ to become true, the Write Mode must be enabled (WME-bit 4, WRØ).

WRQ is reset by WRR (Write Request Reset -- bit 7 of WR1).

RRØ-Bit 2 GRQ (Gap Request)

GRQ indicates that an inter record gap has been detected. GRQ is set by a positive transition of the gap detection signal, GAP, pin 35. See GAP, pin 35, in the INPUT/OUTPUT SIGNAL section for a discussion of the gap detection signal.

GRQ causes an interrupt request, REQ, at pin 24.

GRQ can become true only if:

1. A legitimate record (not a gap noise burst) preceded the positive transition at GAP. The record is declared to be legitimate when REC, bit 5 of RR3, becomes true. See Gap Noise Tolerance, bit Ø of WRØ.

2. The Read Mode has been enabled by RME, bit 4 of WR5.

3. Gap Request has been enabled by GRE, bit 2 of WR1.

RRØ-Bit 3 RDF (Read Flag)

RDF is equivalent to RRQ, bit Ø of RRØ, as long as the Read Request is enabled (RRE-bit 4, WR1). But, RDF continues to indicate the state of the Read Request flip-flop even when the Read Request is disabled. See Figure 3.

RRØ-Bit 4 C3 (Command 3)

RRØ-Bit 5 C2 (Command 2)

Bits 4 and 5 of RRØ indicate the status of C3 and C2 at pins 28 and 27 and at bits 7 and 6 of WR3. (The status of C1 is indicated by bit 1 of RR1.)

RRØ-Bit 6 AWL (Always Low)

RRØ-Bit 7 AWH (Always High)

AWL is always a logic zero and AWH is always a logic one.

Read Register 1 (RR1)

RR1-Bit Ø UA (Unit Address)

Bit Ø indicates the status of UA at pin 17 and at bit Ø of WR6.

RR1-Bit 1 C1 (Command 1)

Bit 1 indicates the status of C1 at pin 37 and at bit 5 of WR3. (The status of C2 and C3 are indicated by bits 5 and 4 of RRØ.)

RR1-Bit 2 RW (Rewind)

Bit 2 indicates the status of RWØ, pin 19, if UA is zero; or RW1, pin 18, if UA is a one.

RR1-Bit 3 S1 (Status 1)

RR1-Bit 4 S2 (Status 2)

S1 and S2 indicate the logic states at pins 29 and 26 respectively.

RR1-Bit 5 MKF (Marker Flag)

RR1-Bit 6 MK (Marker)

MK indicates the logic state of MKØ, pin 3Ø, if UA is a zero; or MK1, pin 31, if UA is a one.

MKF is the output of a flip-flop which is set by a positive transition at MKØ if UA is zero or by a positive transition at MK1 if UA is a one. MKF is reset by any code transmitted to WR3. MKF is also reset by RST-bit 7 of WRØ or pin 4Ø.

MK is true only while the EOT or BOT marks or the clear leader of the selected drive is adjacent to the sensor. MKF, on the other hand, "remembers" that the EOT or BOT has passed the sensor. MKF may be polled at the convenience of the processor program. The most common action taken by the program after an EOT/BOT mark is sensed, is to stop tape motion. To stop tape motion, the program must modify a motion command which is normally C1, C2 or C3. C1, C2 and C3 are in WR3 and any code transmitted to WR3 resets MKF.

RR1-Bit 7 S3 (Status 3)

S3 indicates the logic state at pin 25.

Read Register 2 (RR2)

RR2-Bits Ø-7 RDØ-RD7 (Read Buffer Register)

Data read serially from tape is assembled into 8-bit bytes in the READ SHIFT REGISTER and then transferred to RR2, the READ BUFFER REGISTER, where it is available to the processor program. See Figure 7.

Read Register 3 (RR3)

RR3-Bit Ø NAR (Noise After Record)

RR3-Bit 1 NBR (Noise Before Record)

Both NAR and NBR are error flags which indicate that noise was encountered in an inter record gap while reading a record. A read operation (data read or read-after-write) begins with the read head in the gap preceding a record and ends with the read head in the gap following the record. If noise is found in the gap before the record, NBR is set. If noise is found in the gap following the record, NAR is set.

Exact definitions of NAR and NBR are given below:

NBR is set if a positive transition occurs at DO (Drop Out-pin 38) after the Read Mode is enabled (RME-bit 4, WR5); but before a record is detected. Record detection is signaled by REC-bit 5, RR3.

NAR is set if the Read Mode is enabled and there is a pulse at either of the read data inputs, RD(+) pin 32 or RD(-) pin 33, after the gap has been detected (i.e., while the Gap Flag -- GPF, bit 6 of RR3 is true).

RR3-Bit 2 COR (Command Overrun)

COR is an error flag which indicates that the processor program did not respond to a Write request or a Read Request in time to prevent a loss of data. The program must service a Read or Write request within the time it takes to read or write 8 bits.

COR is set in the Read Mode if the READ SHIFT REGISTER becomes full and data is transferred to the READ BUFFER REGISTER while the Read Request, RRQ, is still set from the previous byte.

COR is set in the Write Mode if the WRITE SHIFT REGISTER becomes empty and data is transferred from the WRITE BUFFER REGISTER while the Write Request, WRQ, is still set from the previous byte.

RR3-Bit 3 DOE (Drop Out Error)

DOE is an error flag which indicates that at least one byte was missing while reading a record or during read-after-write. DOE is set while the Read Mode is enabled if a positive transition occurs at DO, pin 38, after record detection (REC-bit 5, RR3) if DO is followed by at least one RD(+), pin 32, or RD(-), pin 33 before a positive transition at GAP, pin 35.

RR3-Bit 4 CRE (CRC Error)

CRE is an error flag which indicates that the CRC read at the end of a record does not agree with the CRC calculated from the read data.

RR3-Bit 5 REC (Record Detection)

REC indicates that 8 bits (if GNT, bit Ø of WRØ, is set to a logic one) or 16 bits (if GNT is set to a logic zero) have been counted without a drop out since the beginning of the current record. Having counted that number of bits without a drop out virtually guarantees that the current record is a legitimate data record and not noise left in the inter record gap.

See READ A RECORD routine listing for example of how to use REC.

RR3-Bit 6 GPF (Gap Flag)

GPF is equivalent to the Gap Request (GRQ, bit 2 of RRØ) as long as the Gap Request is enabled (GRE, bit 2 of WR1), but GPF continues to indicate the state of the Gap Request flip-flop even when the Gap Request is disabled. See Figure 3.

RR3-Bit 7 WD (Write Data)

Bit 7 indicates the logic level of the phase encoded Write Data output -- WD, pin 36.

TAPE CASSETTE/CARTRIDGE CONTROLLER EXAMPLE

PROCESSOR INTERFACE

Figure 8 shows a 6 chip tape controller which has hardware CRC generation and checking, read-after-write and high speed file search.

This particular configuration is designed for an 8080A processor. The 8080A addresses the controller with Input/Output instructions in which A3 is true. The drive handling routines in the SOFTWARE section are written for this circuit.

Slight changes in the processor interface logic would allow almost any other microprocessor or minicomputer to drive the controller.

TIMING

The timing logic shown in Figure 8 consists of 5 one-shots on three 74123 chips. One-shot timing is the simplest conceptually and is suitable for many applications. However, objections can be made against the use of one-shots. For instance:

1. The period of 74123's varies with temperature, with VCC and from one chip to another.

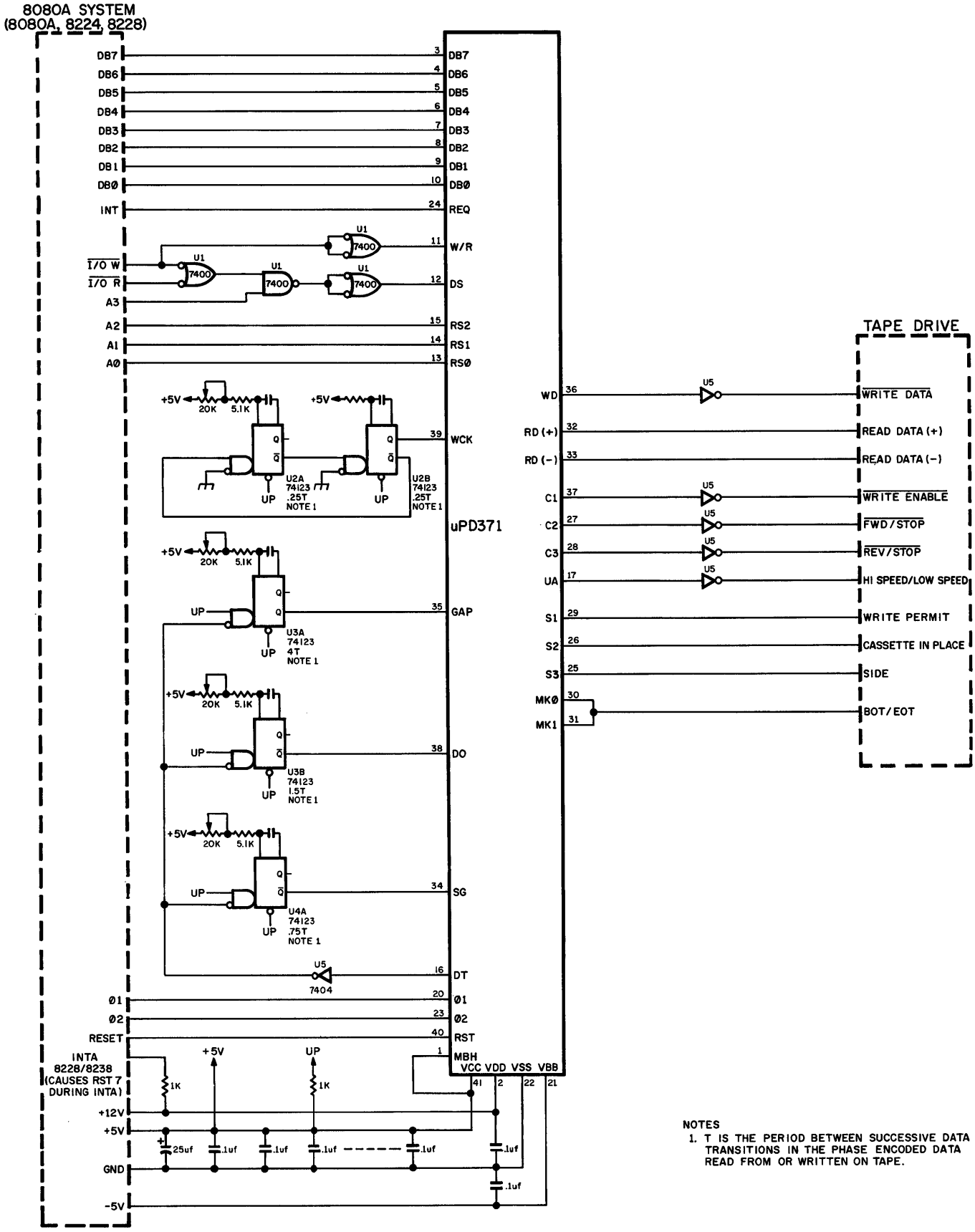
2. This circuit includes 15 discrete components.

3. Four of these discrete components are potentiometers, the most unreliable component of all.

4. The potentiometers require initial adjustment during check out and must be rechecked periodically.

There are a number of digital circuits which may be used in place of the one-shot circuit of Figure 8. All require more chips, but are free from discrete components and from adjustments. They operate with their designed time periods, unless they fail completely. An example is shown in Figure 9.

U1 through U5 in Figure 9 are scalers that count Ø2 (TTL) pulses. Ø2 is normally crystal controlled so its period is stable and accurate. Each of the 8 preset inputs of U1 and U2 and also of U3 and U4 are wired either to ground or through a resistor to +5V. The 8-bit binary number encoded in this manner should be the 2's compliment of the number of Ø2 cycles in .25T. Where T is the period between successive data transitions read from or recorded on tape.



NOTES
1. T IS THE PERIOD BETWEEN SUCCESSIVE DATA TRANSITIONS IN THE PHASE ENCODED DATA READ FROM OR WRITTEN ON TAPE.

FIGURE 8
uPD371 TAPE CASSETTE/CARTRIDGE CONTROLLER EXAMPLE

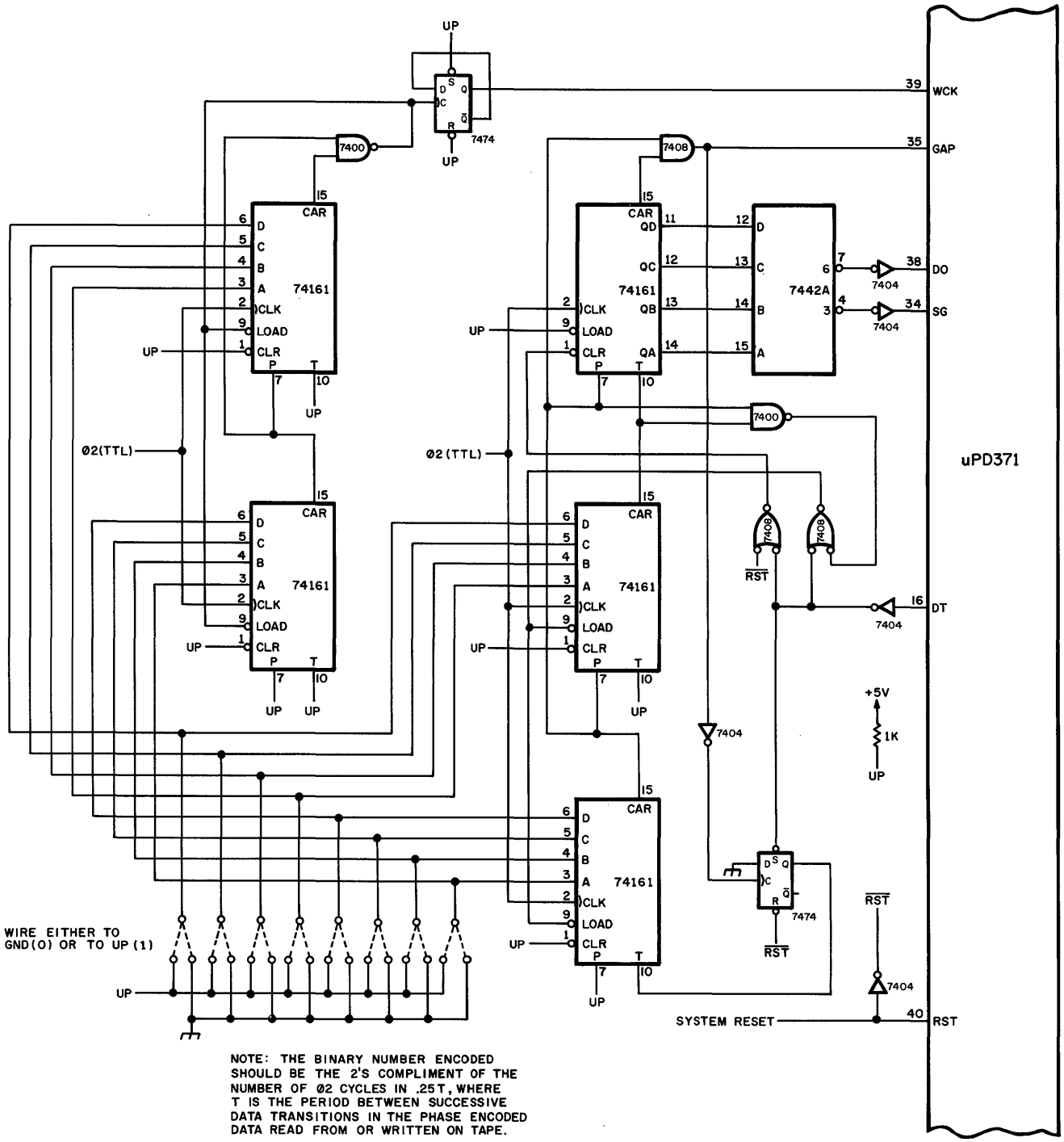


FIGURE 9
DIGITAL TIMING EXAMPLE

U1 and U2 count from the preset code to overflow in .25Tusec. The carry output of U2 reloads the present count so the carry output occurs every .25Tusec as long as power is on. The carry output also toggles a flip-flop, the Q output of which forms a WCK with a period of .5T as required.

U3, U4 and U5 form an interval timer which is reset and started by each DT pulse. The first DT pulse in a record loads the present code into U3 and U4, resets U5 and enables U3, U4 and U5. .25Tusec later U4 overflows. The carry output of U4 reloads the preset code so that the carry output of U4 will occur at every multiple of .25T following DT. The U4 carry output pulses are counted by U5. When 3 carry output pulses have been counted (3 X .25T=.75T), a positive transition is made at SG, as required.

The second DT pulse in a record occurs about Tusec after the first. This DT, and each succeeding DT, resets U5 and reloads the preset code into U3 and U4. So, as long as no bits are missing from the record, the U3, U4 and U5 interval timer is reset and restarted by each DT around the time four U4 carry outputs have been counted. But if one or more bits are missing, U5 continues counting beyond four. When six U4 carry outputs have been counted (6 X .25T=1.5T), a positive transition is made at DO as required.

At the end of a record, U5 counts to 16 (16 X .25T=4T) at which time it overflows. The U5 carry output causes a positive transition at GAP, as required; and disables the U3, U4 and U5 interval timer, ending its operation.

TAPE DRIVE INTERFACE

Single Drive

Since the commands and status signals of tape cassette and cartridge drives vary from manufacturer to manufacturer, nearly all applications will differ in some respects from Figure 8. Adapting to a particular drive is not difficult if the following design practices are followed.

Write Data and the tape drive commands must be buffered since the uPD371 outputs are limited to 1.7mA drive capability.

Some tape drives require Write Data and commands to be inverted, as in Figure 8, while others require them to be uninverted. Unfortunately, many drives mix the two, requiring some signals to be inverted and others not. The uPD371 general reset, RST, sets C1, C2, C3 and UA to the low level. This level should cause commands such as WRITE ENABLE and motion commands to be unasserted whether the drive uses negative or positive logic.

When four commands are needed, UA may be used as the fourth command, as in Figure 8, if the drive EOT/BOT sense signal is connected to both MKØ and MK1. Then regardless of the state of UA, the EOT/BOT sense signal will correctly affect MK and MKF, bits 6 and 5 of RR1. (MK and MKF are described in the ADDRESSABLE INTERNAL REGISTER section under RR1).

If the tape drive status outputs are expressed in negative logic, it is not necessary to invert them to the true state. They may be tied directly to S1, S2 and S3 since the program can easily test for either logic state. The EOT/BOT sense signal, however, must be asserted in the true sense at MKØ or MK1 if MKF is to be affected properly.

If more than four commands and/or four status inputs are required for a single or multiple drive system, they may be added with a simple circuit such as the one shown in Figure 1Ø.

Multiple Drive Systems

Figure 11 shows a particular type of dual drive system for which the uPD371 is especially suited. The drives must each have SELECT and REWIND inputs. UA is used inverted for the SELECT input of drive 1 and uninverted for the SELECT input of drive Ø. RWØ and RW1 are the REWIND inputs of drive Ø and 1 respectively. MKØ and MK1 receive the EOT/BOT sensor output of drives Ø and 1 respectively.

In this configuration, the uPD371 controls part of the rewind operation in hardware which facilitates the rewinding of one drive while reading or writing on the other. For a complete description of this technique, see RW and RRI, bits 4 and 3 of WR3 in the ADDRESSABLE INTERNAL REGISTER section.

Multiple drive systems for other types of drives are easily designed. They generally require additional commands and status signals, as in Figure 1Ø and they may also require multiplexing of commands and status signals.

Cassette/cartridge drive transfer rates are slow enough to allow reading and writing on one drive of a system while rewinding or high speed file searching on other drives. Reading and/or writing simultaneously on more than one drive with a single uPD371 is not possible.

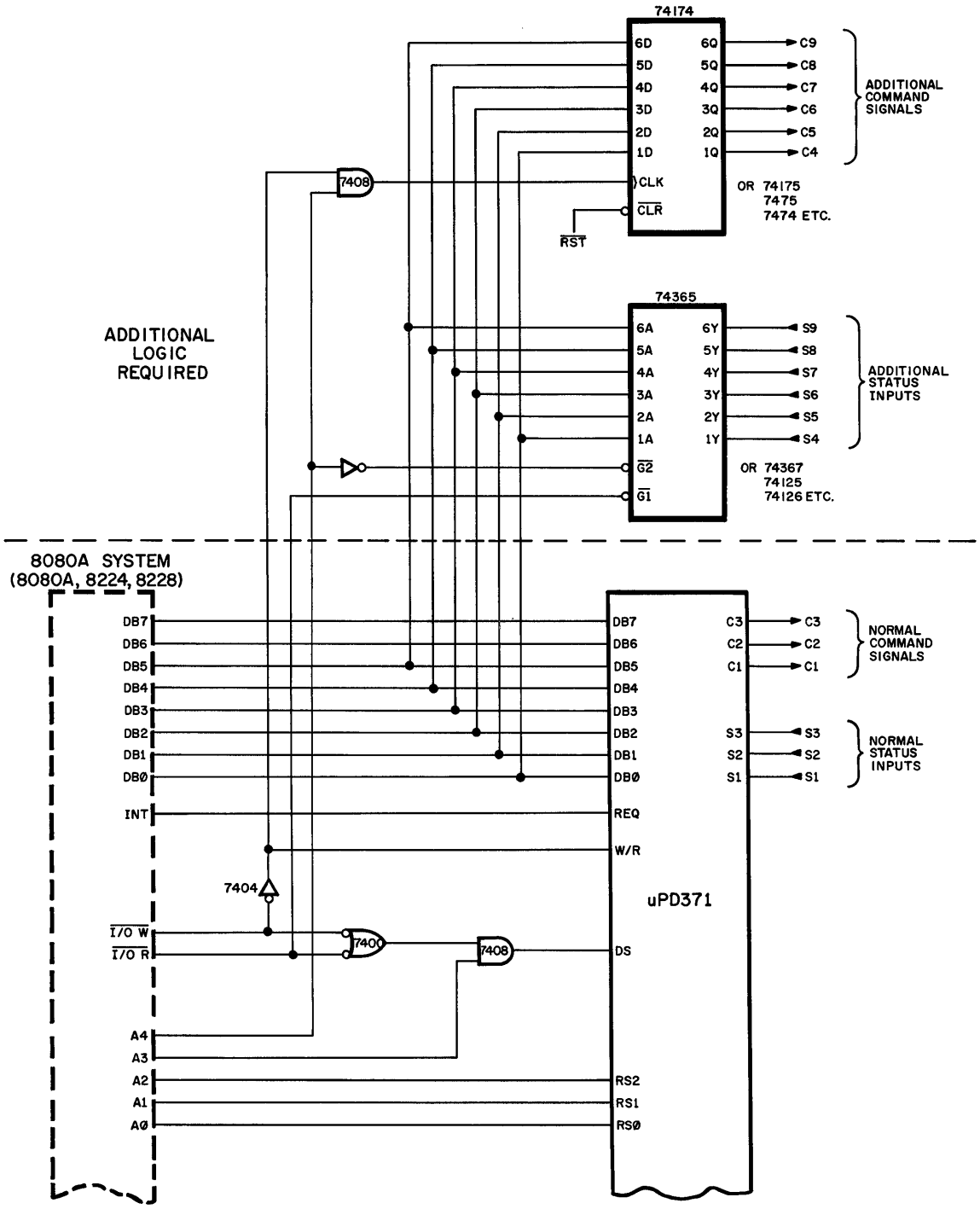
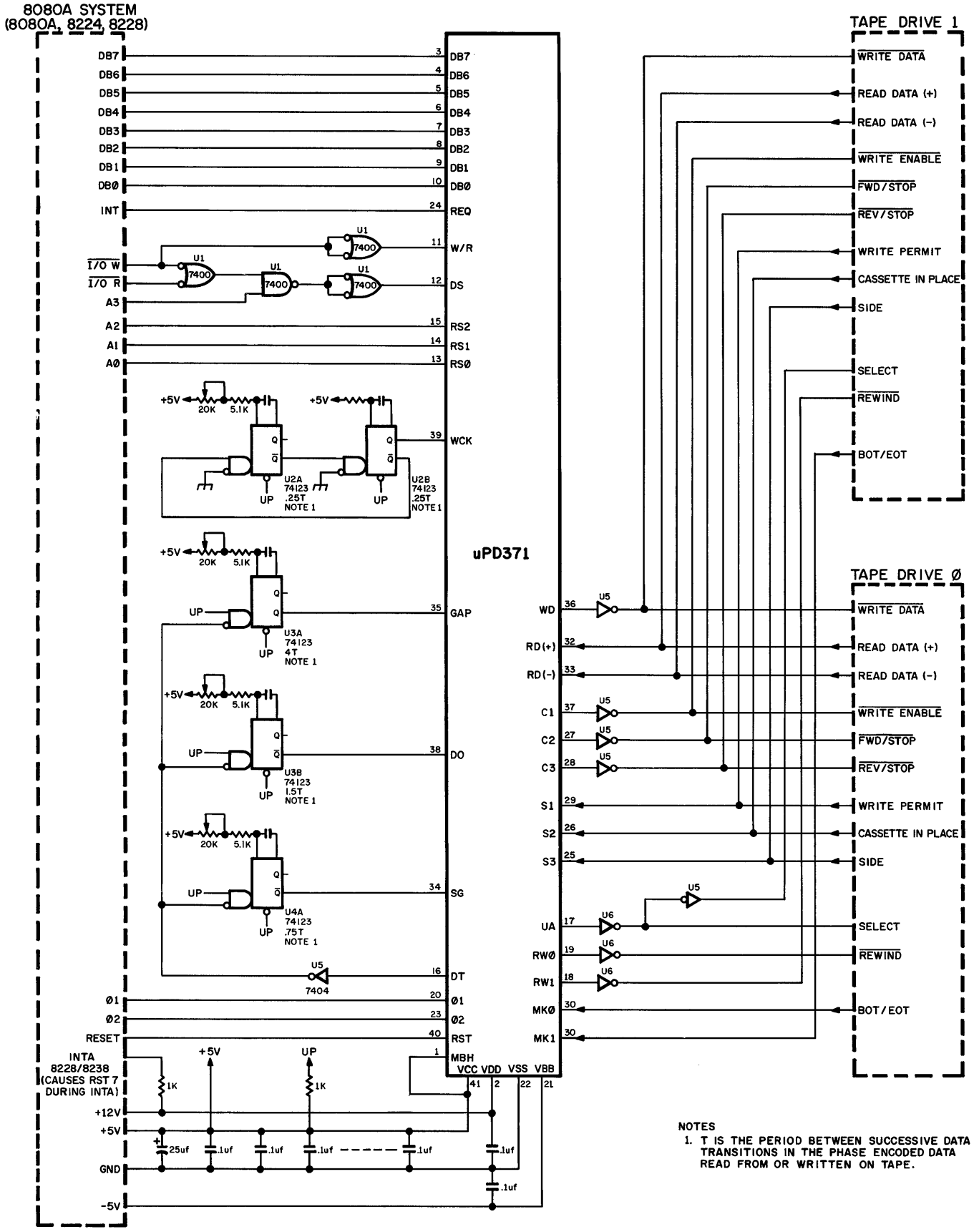


FIGURE 10
ADDITIONAL COMMAND SIGNALS AND STATUS INPUTS
FOR COMPLEX DRIVES OR MULTIPLE DRIVE SYSTEMS



NOTES
1. T IS THE PERIOD BETWEEN SUCCESSIVE DATA TRANSITIONS IN THE PHASE ENCODED DATA READ FROM OR WRITTEN ON TAPE.

FIGURE 11
uPD371 DUAL TAPE CASSETTE/CARTRIDGE CONTROLLER EXAMPLE

SOFTWARE

Introduction

The software listing which follows is written for a uPD8Ø8ØA, but can easily be adapted to run on almost any other processor. These routines will read or write ANSI, ECMA or ISO standard records with the controller shown in Figure 8. A routine to rewind tape to either the load point or to the hub is also included. A high-speed file search routine is not included but the algorithm is described. Although the routines are specifically intended for the controller shown in Figure 8, the command sequence is typical of any cassette/cartridge controller design based on the uPD371.

The routines listed are interrupt driven to allow for multiprogramming. However, no attempt is made here to actually do multiprogramming. Instead, the processor is simply halted after each uPD371 servicing to wait for the next interrupt. In any true multiprogramming application, of course, control would be transferred to the mainline program rather than halting.

If the programmer wishes to use polling rather than interrupt, he may replace the HALT instructions with instruction loops which branch when the expected request flag becomes true.

These routines assume the existence of a 5msec interrupt clock, but timing can be done by other types of system clocks or by software delay routines.

Other Formats

The routines listed produce ANSI, ECMA or ISO standard records with preamble and postamble equal to AA hex and with two CRC bytes generated by the polynomial:

X to the 16th + X to the 15th + X squared + 1.

The uPD371 is not limited to this format, however. The preamble and postamble bytes are completely programmable. The CRC, although always calculated, need not be written on tape (WCR, bit 3 of WRØ causes the CRC to be written), nor does the CRC error flag (CRE, bit 4 of RR3) need to be checked while reading. A CRC generated in software by another polynomial or a check sum or nothing at all may be written on tape in place of the hardware calculated CRC.

High Speed File Search

The ANSI, ECMA or ISO standard EOF "mark" is really a five byte record -- preamble, zero data byte, CRC 1, CRC 2 and postamble. Most data records are much longer -- typically 128 or 256 data bytes. Because of the difference in size between EOF marks and most data records, a search for an EOF mark may be made at high speed, without data transfer, by measuring the time between the first Read Request and the Gap Request of each record. When a record is encountered with a passage time less than a certain amount (calculated below), it should be read at low speed to verify that it is an EOF mark and not an unusually short data record.

The length of time used to distinguish between data records and suspected EOF marks depends on the high tape speed of the drive. The drive used in Figure 8, for example, has a high speed of 80 IPS. At this speed, the time between bits (at 800 BPI) is 15.625usec. The time between the first read request (end of the preamble) and the end of the postamble is 32 x 15.625=500usec. The time between the end of the postamble and the gap request is 4T, where T is the low speed data transfer period -- 10 IPS in this example. 4T = 4 X 125us=500us. So, the total time between the first read request and the gap request is 500usec + 500usec=1msec for an EOF mark read at high speed on the drive used in this example.

Any record encountered in a high speed file search (at 80 IPS) which has a passage time of less than about 2msec (5msec would work) should then be read at low speed to verify that it is, in fact, an EOF mark.

Parameters and Conventions

The tape drive for which these routines are written, Figure 8, has the following parameters:

Low Speed	10 IPS
High Speed	80 IPS
Start Distance at 10 IPS	.5 in.
Start Time at 10 IPS	50msec
Stop Distance at 10 IPS	.15 in.
Stop Time at 10 IPS	30msec
Distance between read and write heads	.15 in.

The controller in Figure 8 causes a RST7 during interrupt acknowledge which vectors the uPD8080A processor to location 38H at each controller interrupt.

The 5ms clock in this 8080A system causes a RST6 during interrupt acknowledge which vectors the uPD8080A to location 30H at each clock interrupt. An OUT 11H instruction starts the 5ms timer and OUT 12H clears the interrupt request.

The uPD371 is addressed as shown in Figure 8. The table below gives the addresses of each uPD371 register.

WR0	OUT 08H
WR1	OUT 09H
WR2	OUT 0AH
WR3	OUT 0BH
WR5	OUT 0DH
WR6	OUT 0EH
RR0	IN 08H
RR1	IN 09H
RR2	IN 0AH
RR3	IN 0BH

C1, C2, C3, UA, S1, S2 and S3 are defined as in Figure 8.

C1 = WRITE ENABLE

C2 = FWD/STOP

C3 = REV/STOP

UA = HI SPEED/LO SPEED

S1 = WRITE PERMIT

S2 = CASSETTE IN PLACE

S3 = SIDE

```
;NEC UPD371 CASSETTE/CARTRIDGE CONTROLLER PROGRAM

            ;READ, REWIND AND WRITE  06/03/77  1600  (AEO)

0000                    ORG     30H

0030 C9     LOC30:      RET                     ;5 MSEC CLOCK INTERRUPT
                                                ;ADDRESS

0031                    ORG     38H

0038 C9     LOC38:      RET                     ;371 INTERRUPT ADDRESS


0039                    ORG     1000H


            ;REWIND TO LOADPOINT ROUTINE


1000 1600   RWLPT:      MVI     D,0             ;INDICATE REWIND TO
1002 C30710             JMP     RW1             ;LOADPOINT


            ;REWIND TO HUB ROUTINE


1005 1601   RWHUB:      MVI     D,01H           ;INDICATE REWIND TO HUB


1007 1E00   RW1:        MVI     E,0             ;INDICATE NONWRITE OPERATION
1009 CD6811             CALL    READY           ;CLEAR FLAGS, RESET 371 AND
                                                ;CHECK FOR CASSETTE IN PLACE

100C AF                 XRA     A               ;RESET EOT
100D 322212             STA     EOT
1010 3E01               MVI     A,01H           ;SET HI SPEED
1012 D30E               OUT     0EH
1014 3E80               MVI     A,80H           ;SET REVERSE
1016 D30B               OUT     0BH
1018 3E96               MVI     A,150           ;DELAY 750 MSEC TO MAKE SURE
101A CD0D12             CALL    DELAY           ;SENSOR IS NOT ON EOT OR
                                                ;EOT CLEAR LEADER


101D CD7C10             CALL    MARK            ;WAIT FOR BOT INDICATION
1020 3E01               MVI     A,1             ;DELAY 5 MSEC TO GUARANTEE
1022 CD0D12             CALL    DELAY           ;THAT NEXT MARK INDICATION
                                                ;IS BOT CLEAR LEADER
1025 CD7C10             CALL    MARK            ;WAIT FOR BOT CLEAR LEADER
1028 AF                 XRA     A               ;RESET REVERSE
1029 D30B               OUT     0BH
102B 3E3C               MVI     A,60            ;WAIT 300 MSEC FOR TAPE
102D CD0D12             CALL    DELAY           ;TO STOP
```

```
1030 7A                MOV     A,D             ;SHOULD TAPE BE REWOUND
1031 B7                ORA     A               ;TO HUB?
1032 CA3F10            JZ      RW2             ;NO: CONTINUE
1035 3E80              MVI     A,80H           ;YES: SET REVERSE
1037 D30B              OUT     0BH
1039 3E64              MVI     A,100           ;DELAY 500 MSEC TO REWIND
103B CD0D12            CALL    DELAY           ;TAPE TO HUB
103E C9                RET                     ;RETURN FROM REWIND TO HUB

103F 3E40      RW2:    MVI     A,40H           ;SET FWD
1041 D30B              OUT     0BH
1043 3E01      RW3:    MVI     A,1             ;DELAY 5 MSEC
1045 CD0D12            CALL    DELAY
1048 DB09              IN      09H             ;HAS TAPE MOVED FWD TO END OF
104A E640              ANI     40H             ;BOT CLEAR LEADER?
104C C24310            JNZ     RW3             ;NO: WAIT 5 MSEC THEN RECHECK

104F 3E1E              MVI     A,30            ;YES: CONTINUE MOVING TAPE
1051 CD0D12            CALL    DELAY           ;FWD AT HI SPEED FOR 150 MSEC
1054 AF                XRA     A               ;RESET FWD TO STOP TAPE
1055 D30B              OUT     0BH
1057 D30E              OUT     0EH             ;RESET HI SPEED
1059 3E28              MVI     A,40            ;WAIT 200 MSEC FOR TAPE
105B CD0D12            CALL    DELAY           ;TO STOP

105E 3E40              MVI     A,40H           ;SET FWD
1060 D30B              OUT     0BH
1062 3E00      MKF:    MVI     A,0             ;DELAY 5 MSEC
1064 CD0D12            CALL    DELAY
1067 DB09              IN      09H             ;HAS TAPE MOVED FWD TO BOT?
1069 E620              ANI     20H
106B CA6210            JZ      MKF             ;NO: WAIT 5 MSEC THEN RECHECK

106E AF                XRA     A               ;YES: RESET FWD TO STOP TAPE
106F D30B              OUT     0BH
1071 3E06              MVI     A,6             ;WAIT 30 MSEC FOR TAPE
1073 CD0D12            CALL    DELAY           ;TO STOP
1076 3E01              MVI     A,01H           ;SET SOFTWARE BOT FLAG
1078 322112            STA     BOT
107B C9                RET                     ;RETURN FROM REWIND TO
                                               ;LOADPOINT

107C DB09      MARK:   IN      09H             ;EOT/BOT?
107E E640              ANI     40H
1080 C0                RNZ                     ;YES: RETURN
1081 3E01              MVI     A,1             ;NO: WAIT 5 MSEC THEN RECHECK
1083 CD0D12            CALL    DELAY
```

```
1086 C37C10          JMP     MARK


             ;WRITE A RECORD ROUTINE

1089 1E01    WRITE:  MVI     E,01H       ;INDICATE WRITE OPERATION
108B CD6811          CALL    READY       ;CLEAR FLAGS,RESET 371,CHECK
                                         ;FOR CASSETTE IN PLACE AND
                                         ;WRITE PERMIT

108E 3A2212          LDA     EOT         ;HAS THE EOT PASSED?
1091 B7              ORA     A
1092 CA9B10          JZ      W1          ;NO: CONTINUE
1095 3E01            MVI     A,01H       ;YES: STORE 01 IN ERF
1097 321912          STA     ERF
109A C9              RET                 ;RETURN

109B CD9611  W1:     CALL    MOVEF       ;SET WRITE ENABLE AND FWD
                                         ;WAIT 50 MSEC FOR TAPE TO
                                         ;REACH FULL SPEED.
                                         ;ENABLE READ TO MAKE READ-
                                         ;AFTER-WRITE CRC CHECK

109E 3A2112          LDA     BOT         ;WAS TAPE AT LOADPOINT?
10A1 B7              ORA     A
10A2 CAB110          JZ      W2          ;NO: USE NORMAL DELAY
10A5 3E3C            MVI     A,60        ;YES: DELAY 300 MSEC TO WRITE
10A7 CD0D12          CALL    DELAY       ;3.3 INCH BOT GAP
10AA AF              XRA     A           ;CLEAR SOFTWARE BOT FLAG
10AB 322112          STA     BOT
10AE C3B610          JMP     W3
10B1 3E06    W2:     MVI     A,6         ;DELAY 30 MSEC TO WRITE 0.8
10B3 CD0D12          CALL    DELAY       ;INCH INTER RECORD GAP


10B6 3EAA    W3:     MVI     A,0AAH      ;LOAD PREAMBLE IN WR2
10B8 D30A            OUT     0AH
10BA 3E10            MVI     A,10H       ;ENABLE WRITE MODE
10BC D308            OUT     08H         ;WRITING BEGINS AT NEXT
                                         ;WCK.  CRC CALCULATION
                                         ;BEGINS AFTER PREAMBLE IS
                                         ;WRITEN.


10BE FB      WLP:    EI
10BF 76              HLT                 ;WAIT FOR WRITE REQUEST
                                         ;INTERRUPT
             ;
             ;
             ;INTERRUPT
             ;
```

```
                ;
10C0 3E80               MVI     A,80H           ;RESET WRITE REQUEST
10C2 D309               OUT     09H
10C4 7E                 MOV     A,M             ;GET NEXT BYTE
10C5 D30A               OUT     0AH             ;PUT IN WR2
10C7 23                 INX     H               ;INCREMENT ADDRESS POINTER
10C8 05                 DCR     B               ;DECREMENT WORDCOUNT
                                                ;IS WORDCOUNT ZERO?
10C9 C2BE10             JNZ     WLP             ;NO: WRITE ANOTHER BYTE


10CC FB                 EI                      ;YES: WAIT FOR LAST DATA
10CD 76                 HLT                     ;BYTE TO BE TRANSFERRED
                                                ;FROM WR2 TO WRITE SHIFT
                                                ;REGISTER
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;LAST DATA BYTE BEING WRITTEN
10CE 3E80               MVI     A,80H           ;RESET WRITE REQUEST
10D0 D309               OUT     09H
10D2 3E08               MVI     A,08H           ;SET WCR - STOPS WRITING DATA
10D4 D308               OUT     08H             ;FROM WR2 AT NEXT WRITE
                                                ;REQUEST AND BEGINS WRITING
                                                ;DATA FROM CRC SHIFT REGISTER
10D6 FB                 EI
10D7 76                 HLT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;1ST CRC BYTE BEING WRITTEN
10D8 3E80               MVI     A,80H           ;RESET WRITE REQUEST
10DA D309               OUT     09H
10DC FB                 EI
10DD 76                 HLT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;2ND CRC BYTE BEING WRITTEN
10DE 3E80               MVI     A,80H           ;RESET WRITE REQUEST
10E0 D309               OUT     09H
10E2 3EAA               MVI     A,0AAH          ;PUT POSTAMBLE CODE IN WR2
10E4 D30A               OUT     0AH
10E6 AF                 XRA     A               ;RESET WCR - STOP WRITING
10E7 D308               OUT     08H             ;DATA FROM CRC SHIFT REGISTER
                                                ;AT NEXT WRITE REQUEST AND
                                                ;RETURN TO WRITING DATA FROM
                                                ;WR2
```

```
10E9 FB                 EI
10EA 76                 HLT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                    ;POSTAMBLE BEING WRITTEN
10EB 3E84               MVI     A,84H               ;RESET WRITE REQUEST AND
10ED D309               OUT     09H                 ;ENABLE GAP REQUEST
10EF 3E02               MVI     A,02H               ;DISABLE WRITE MODE
10F1 D308               OUT     08H
10F3 FB                 EI
10F4 76                 HLT                         ;WAIT FOR GAP DETECTION
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                    ;BEGINING OF GAP HAS PASSED
                                                    ;READ HEAD
10F5 CDB211             CALL    GAP                 ;RESET GAP REQUEST. STOP TAPE
                                                    ;MOTION. CHECK FOR EOF,EOT
                                                    ;AND ERRORS
10F8 AF                 XRA     A
10F9 D30B               OUT     0BH                 ;RESET WRITE ENABLE
10FB C9                 RET                         ;RETURN



                ;READ A RECORD ROUTINE

10FC 1E00       READ:   MVI     E,0                 ;INDICATE NONWRITE OPERATION
10FE CD6811             CALL    READY               ;CLEAR FLAGS, RESET 371 AND
                                                    ;CHECK FOR CASSETTE IN PLACE

1101 3E14               MVI     A,14H               ;ENABLE READ AND GAP
1103 D309               OUT     09H                 ;INTERRUPT REQUESTS
1105 CD9611             CALL    MOVEF               ;SET FWD. WAIT 50 MSEC FOR
                                                    ;TAPE TO REACH FULL SPEED.
                                                    ;ENABLE READ REQUEST

1108 AF                 XRA     A                   ;CLEAR SOFTWARE BOT FLAG
1109 322112             STA     BOT
110C 57                 MOV     D,A                 ;CLEAR INTERRUPT COUNTER
110D FB                 EI                          ;WAIT FOR READ REQUEST
110E 76                 HLT                         ;INTERRUPT
                ;
                ;
                ;INTERRUPT
                ;
                ;
```

```
                                                ;PREAMBLE IN RR2
110F CD5511             CALL    RDINT           ;RESET READ REQUEST AND CHECK
                                                ;FOR GAP
1112 DB0A               IN      0AH             ;READ DATA
1114 D6AA               SUI     0AAH            ;IS IT A PREAMBLE?
1116 321C12             STA     PRERR           ;STORE RESULT IN PRERR
1119 CA2111             JZ      R1              ;YES: CONTINUE
111C 3E01               MVI     A,01H           ;NO: STORE 01 IN ERF
111E 321912             STA     ERF
1121 FB         R1:     EI                      ;WAIT FOR READ REQUEST
1122 76                 HLT                     ;INTERRUPT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;1ST DATA BYTE IN RR2
1123 CD5511             CALL    RDINT           ;RESET READ REQUEST AND CHECK
                                                ;FOR GAP
1126 DB0B               IN      0BH             ;CHECK FOR RECORD DETECTION
1128 E620               ANI     20H
112A D620               SUI     20H             ;WAS A RECORD DETECTED?
112C 321D12             STA     RCERR           ;STORE RESULT IN RCERR
112F CA3711             JZ      R2              ;YES: CONTINUE
1132 3E01               MVI     A,01H           ;NO: STORE 01 IN ERF THEN
1134 321912             STA     ERF             ;CONTINUE
1137 DB0A       R2:     IN      0AH             ;SAVE 1ST DATA BYTE FOR LATER
1139 322612             STA     FSTBY           ;INSPECTION BY EOF DETECTOR
                                                ;DURING GAP ROUTINE


113C DB0A       RLP1:   IN      0AH             ;READ DATA FROM RR2
113E 77                 MOV     M,A             ;STORE IN MEMORY
113F 23                 INX     H               ;INCREMENT ADDRESS POINTER
1140 05                 DCR     B               ;DECREMENT WORDCOUNTER
                                                ;IS IT ZERO?
1141 CA4C11             JZ      RLP2            ;YES: EXIT READ LOOP. NO MORE
                                                ;DATA STORAGE DESIRED
1144 FB                 EI                      ;NO: CONTINUE READING DATA
1145 76                 HLT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;A DATA BYTE IN RR2
1146 CD5511             CALL    RDINT           ;RESET READ REQUEST AND CHECK
                                                ;FOR GAP
1149 C33C11             JMP     RLP1            ;CONTINUE READING DATA


114C FB         RLP2:   EI
114D 76                 HLT
                ;
```

```
                ;
                ;INTERRUPT
                ;
                ;
                                                    ;WORDCOUNT EXCEEDED. NO
                                                    ;STORAGE DESIRED
114E CD5511             CALL    RDINT               ;RESET READ REQUEST AND CHECK
                                                    ;FOR GAP
1151 Ø5                 DCR     B                   ;DECREMENT WORDCOUNTER
1152 C34C11             JMP     RLP2                ;CONTINUE NON DATA STORAGE
                                                    ;LOOP UNTIL GAP DETECTED


1155 DBØ8       RDINT:  IN      Ø8H                 ;READ INTERRUPT FLAGS
1157 E6Ø4               ANI     Ø4H                 ;WAS IT A GAP REQUEST?
1159 C26211             JNZ     ENDRD               ;YES: END OF RECORD
                                                    ;JUMP TO ENDRD
115C 3EØ4               MVI     A,4ØH               ;NO: MUST BE READ REQUEST
115E D3Ø9               OUT     Ø9H                 ;RESET READ REQUEST
116Ø 14                 INR     D                   ;INCREMENT INTERRUPT COUNTER
1161 C9                 RET                         ;RETURN

1162 CDB211     ENDRD:  CALL    GAP                 ;RESET READ REQUEST.STOP TAPE
                                                    ;MOTION.CHECK FOR EOF,EOT
                                                    ;AND ERRORS.
1165 33                 INX     SP
1166 33                 INX     SP
1167 C9                 RET                         ;NORMAL EXIT FROM READ



                ;READY SUBROUTINE



1168 211912     READY:  LXI     H,ERF               ;CLEAR FLAGS
116B Ø6Ø8               MVI     B,8
116D AF                 XRA     A
116E 77         RDYLP:  MOV     M,A
116F 23                 INX     H
117Ø Ø5                 DCR     B
1171 C26E11             JNZ     RDYLP


1174 3E8Ø               MVI     A,8ØH               ;RESET 371
1176 D3Ø8               OUT     Ø8H
1178 7B                 MOV     A,E                 ;READ OR WRITE OPERATION
1179 B7                 ORA     A                   ;CALLING READY?
117A DBØ9               IN      Ø9H                 ;READ RR1
117C C28611             JNZ     RD1                 ;WRITE: GO TO RD1
117F E61Ø               ANI     1ØH                 ;READ: CHECK FOR CASSETTE IN
```

```
1181 D610              SUI     10H             ;PLACE ONLY
1183 C38A11            JMP     RD2
1186 E618      RD1:    ANI     18H             ;WRITE: CHECK FOR CASSETTE IN
1188 D618              SUI     18H             ;PLACE AND WRITE PERMIT

118A 321A12    RD2:    STA     ERR1            ;STORE RESULT IN ERR1
                                               ;WAS THERE AN ERROR?
118D C8                RZ                      ;NO: NORMAL RETURN
118E 3E01              MVI     A,01H           ;YES: STORE 01 IN ERF
1190 321912            STA     ERF
1193 33                INX     SP
1194 33                INX     SP
1195 C9                RET                     ;EXIT FROM ROUTINE WHICH
                                               ;CALLED READY


                ;MOVE SUBROUTINE


1196 7B        MOVEF:  MOV     A,E             ;READ OR WRITE OPERATION
1197 B7                ORA     A               ;CALLING MOVEF?
1198 3E60              MVI     A,60H
119A C29F11            JNZ     MOV1            ;WRITE: SET FWD AND WRITE
                                               ;ENABLE
119D 3E40              MVI     A,40H           ;READ: SET FWD ONLY
119F D30B      MOV1:   OUT     0BH
11A1 3E0A              MVI     A,10            ;WAIT 50 MSEC FOR TAPE TO
11A3 CD0D12            CALL    DELAY           ;REACH FULL SPEED


11A6 3E10              MVI     A,10H           ;ENABLE READ MODE
11A8 D30D      OUT     0DH
11AA 2A2312            LHLD    STADD           ;LOAD START ADDRESS IN HL
11AD 3A2512            LDA     WDCNT           ;LOAD WORDCOUNT IN B
11B0 47                MOV     B,A
11B1 C9                RET


                ;GAP SUBROUTINE


11B2 3E02      GAP:    MVI     A,02H           ;DISABLE GAP REQUEST
11B4 D309              OUT     09H


11B6 7A                MOV     A,D             ;READ INTERRUPT COUNTER
11B7 FE05              CPI     5               ;DID RECORD CONTAIN 5 BYTES?
11B9 C2C811            JNZ     G1              ;NO: CONTINUE
11BC 3A2612            LDA     FSTBY           ;YES: WAS THE DATA BYTE ZERO?
11BF B7                ORA     A
11C0 C2C811            JNZ     G1              ;NO: CONTINUE
11C3 3E01              MVI     A,01H           ;YES SET EOF FLAG
```

```
11C5 321F12            STA     EOF

11C8 78        G1:     MOV     A,B             ;READ WORDCOUNTER FINAL VALUE
11C9 D6FD              SUI     -Ø3             ;IS IT -3?
                                               ;(POSTAMBLE, CRC1 AND CRC2)
11CB 322Ø12            STA     WCDIF           ;STORE RESULT IN WCDIF

11CE 3EØ8              MVI     A,Ø8H           ;DISABLE READ MODE
11DØ D3ØD              OUT     ØDH
11D2 CDØ412            CALL    EOTCK           ;IF EOT WAS PASSED STORE
                                               ;Ø1 IN EOT
11D5 7B                MOV     A,E             ;READ OR WRITE OPERATION
11D6 B7                ORA     A               ;CALLING GAP?
11D7 3E2Ø              MVI     A,2ØH
11D9 C2DD11            JNZ     G2              ;WRITE: RESET FWD LEAVING
                                               ;WRITE ENABLED
11DC AF                XRA     A               ;READ: RESET FWD ONLY
11DD D3ØB      G2:     OUT     ØBH
11DF 3E Ø6             MVI     A,6             ;WAIT 3Ø MSEC FOR TAPE TO STOP
11E1 CDØD12            CALL    DELAY
11E4 CDØ412            CALL    EOTCK           ;IF EOT WAS PASSED STORE
                                               ;Ø1 IN EOT

11E7 DBØB              IN      ØBH             ;STORE ERROR BITS IN ERR2
11E9 E61F              ANI     1FH
11EB 321B12            STA     ERR2            ;WERE THERE ANY ERRORS?
11EE CAF611            JZ      G3              ;NO: CONTINUE
11F1 3EØ1              MVI     A,Ø1H           ;YES: STORE Ø1 IN ERF
11F3 321912            STA     ERF

11F6 DBØA      G3:     IN      ØAH             ;WAS LAST BYTE A POSTAMBLE?
11F8 D6AA              SUI     ØAAH
11FA 321E12            STA     POERR           ;STORE RESULT IN POERR
11FD C8                RZ                      ;YES: RETURN
11FE 3EØ1              MVI     A,Ø1H           ;NO: PUT Ø1 IN ERF AND RETURN
12ØØ 321912            STA     ERF
1203 C9                RET

                ;CHECK FOR EOT SUBROUTINE

1204 DB Ø9     EOTCK:  IN      Ø9H             ;WAS EOT PASSED?
1206 E62Ø              ANI     2ØH
1208 C8                RZ                      ;NO: RETURN - EOT UNMODIFIED
1209 322212            STA     EOT             ;YES: STORE 2ØH IN EOT AND
12ØC C9                RET                     ;RETURN
```

```
                ;DELAY SUBROUTINE

120D 4F         DELAY:  MOV     C,A             ;STORE NUMBER OF 5 MSEC
                                                ;DELAYS DESIRED IN C
120E D313       DELLP:  OUT     13H             ;FIRE 5 MSEC ONE SHOT
1210 FB                 EI                      ;ENABLE INTERRUPTS
1211 76                 HLT                     ;WAIT 5 MSEC FOR INTERRUPT
                ;
                ;
                ;INTERRUPT
                ;
                ;
                                                ;CLOCK INTERRUPT
1212 D312               OUT     12H             ;CLEAR INTERRUPT FLAG
1214 0D                 DCR     C               ;DECREMENT DELAY COUNTER
1215 C20E12             JNZ     DELLP           ;NO: DELAY 5 MSEC MORE
1218 C9                 RET                     ;YES: RETURN



1219 00         ERF:    DB      0               ;MASTER ERROR FLAG


121A 00         ERR1:   DB      0
121B 00         ERR2:   DB      0
121C 00         PRERR:  DB      0
121D 00         RCERR:  DB      0
121E 00         POERR:  DB      0


121F 00         EOF:    DB      0
1220 00         WCDIF:  DB      0


1221 00         BOT:    DB      0
1222 00         EOT:    DB      0


1223 0000       STADD:  DW      0
1225 00         WDCNT:  DB      0


1226 00         FSTBY:  DB      0


0000                    END
```

ABSOLUTE MAXIMUM RATINGS

Ta = 25 C All voltages measured with respect to VSS

Symbol	Parameter	Min	Max	Unit	Conditions
VDD	VDD Supply Voltage	-1	+16	V	VBB=-5V±5%
VCC	VCC Supply Voltage	-1	+8	V	VBB=-5V±5%
VBB	VBB Supply Voltage	-10	0	V	
VI	Input Voltage	-1	+8	V	VBB=-5V±5%
VO	Output Voltage	-1	+8	V	VBB=-5V±5%
VO	Clock Voltage	-1	+16	V	VBB=-5V±5%
Topt	Operating Free-Air Temp.Range	0	+70	C	
Tstg	Storage Temperature	-40	+125	C	

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

Ta = 25 C, VDD = VCC = VSS = 0V, VBB = -5V

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C0	Clock Capacitance			35	pF	fc=1MHz. All pins except measuring pin are grounded
CIN	Input Capacitance			10	pF	
COUT	Output Capacitance			20	pF	

DC CHARACTERISTICS

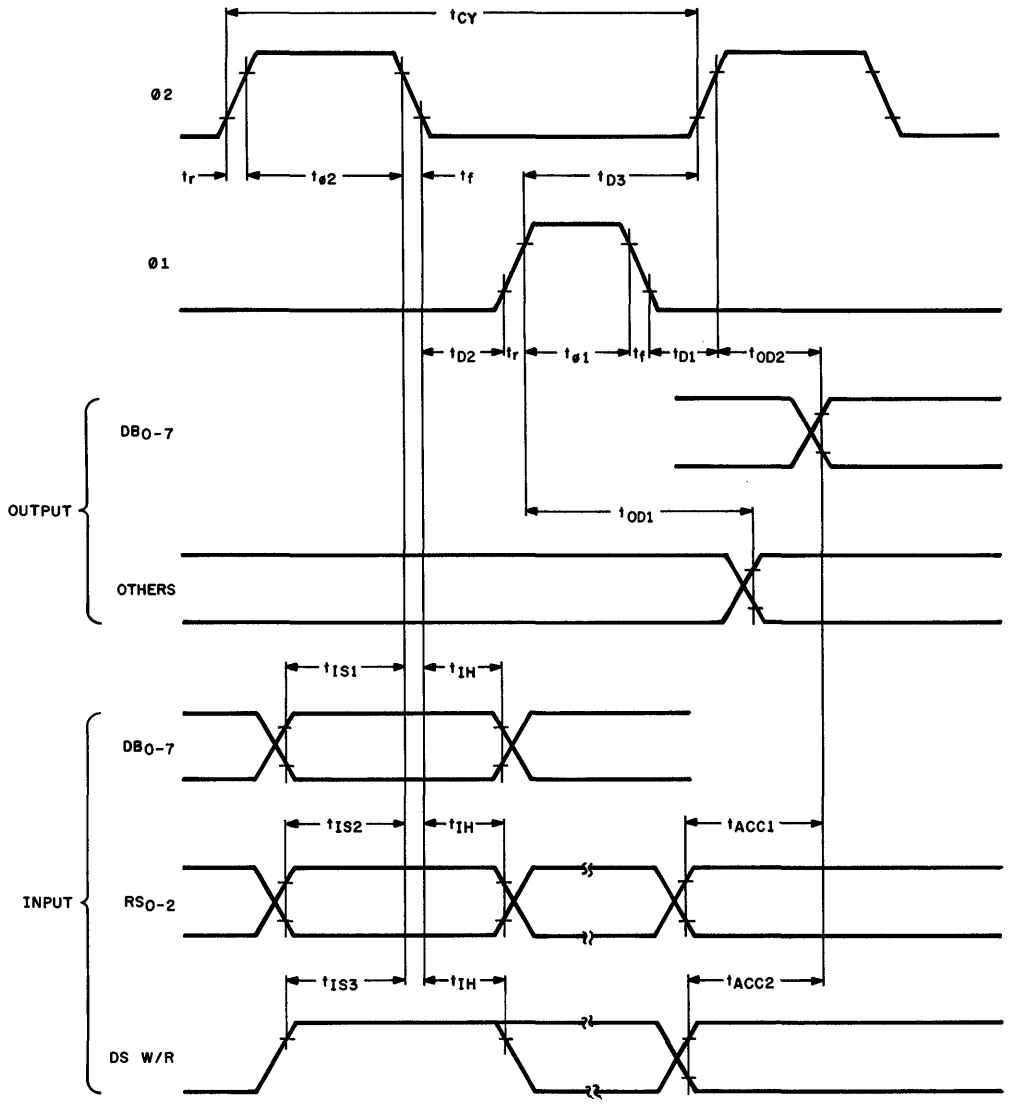
Ta = Ø-7Ø C VDD = +12V±5% VCC = +5V±5% VBB = -5V±5% VSS = ØV

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	Input High Voltage	+3.Ø		VCC	V	
VIL	Input Low Voltage	Ø		+Ø.8	V	
VOH	Output High Voltage	+3.5			V	IOH = -1mA
VOL	Output Low Voltage			+Ø.4	V	IOL = +1.7mA
VØH	Clock Input High Voltage	+9		VDD	V	
VØL	Clock Input Low Voltage	Ø		+Ø.65	V	
ILIH	Input Leakage Current			+1Ø	uA	VI = +3.ØV
ILIL 1	Input Leakage Current DBØ-DB7			-1Ø	uA	VI = +Ø.8V
ILIL 2	Input Leakage Current All Except DBØ-DB7 (~25K Internal Pull-ups)			-1.Ø	mA	VI = +Ø.4V
ILØH	Clock Input Leakage Current			+2Ø	uA	VØ = +9.ØV
ILØL	Clock Input Leakage Current			-2Ø	uA	VØ = +Ø.65V
ILOH	Output Leakage Current			+1Ø	uA	VO = +3.5V
ILOL	Output Leakage Current			-1Ø	uA	VO = +Ø.4V
IDD	Power Supply Current(VDD)		+2Ø		mA	
ICC	Power Supply Current(VCC)		+3Ø		mA	
IBB	Power Supply Current (VBB)			-2	mA	

AC CHARACTERISTICS

Ta = Ø-7Ø C VDD = +12V±5% VCC = +5V±5% VBB = -5V±5% VSS = CU

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
tcy	Clock Period	48Ø		5ØØØ	ns	
tr,tf	Clock Rise & Fall Times	Ø		5Ø	ns	
tØ1	Ø1 Pulse Width	6Ø			ns	
tØ2	Ø2 Pulse Width	22Ø			ns	
tD1	Ø1 to Ø2 Delay	Ø			ns	
tD2	Ø2 to Ø1 Delay	7Ø			ns	
tD3	Delay Ø1 to Ø2 Lead.Edges	8Ø			ns	
tOD1	Data Out Delay from Ø1			48Ø	ns	1TTL & CL=3ØpF
tOD2	Data Out Delay from Ø1			26Ø	ns	1TTL & CL=3ØpF
tACC1	RSØ-RS2 to Output Delay			3ØØ	ns	1TTL & CL=3ØpF
tACC2	DS, W/R to Output Delay			2ØØ	ns	1TTL & CL=3ØpF
tIS1	DBØ-DB7 to Ø2 Setup Time	25Ø			ns	
tIS2	RSØ-RS2 to Ø2 Setup Time	35Ø			ns	
tIS3	DS, W/R to Ø2 Setup Time	15Ø			ns	
tIH	Input Hold Time from Ø2	3Ø			ns	



Note: Timing Measurement Levels:
Clock High / Low Voltage = 9.0V / 0.65V
Input High/ Low Voltage = 3.0V / 0.8V
Output High/Low Voltage = 2.0V / 0.8V

FIGURE 12
uPD371 TIMING DIAGRAM

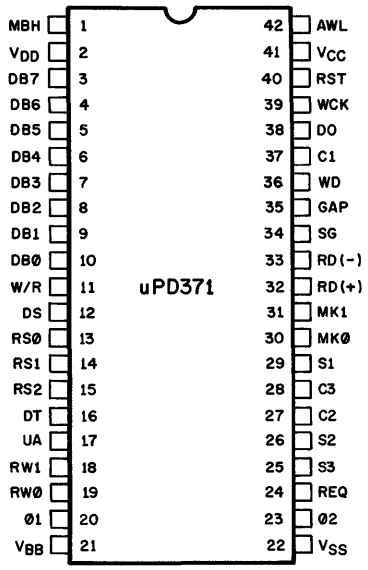
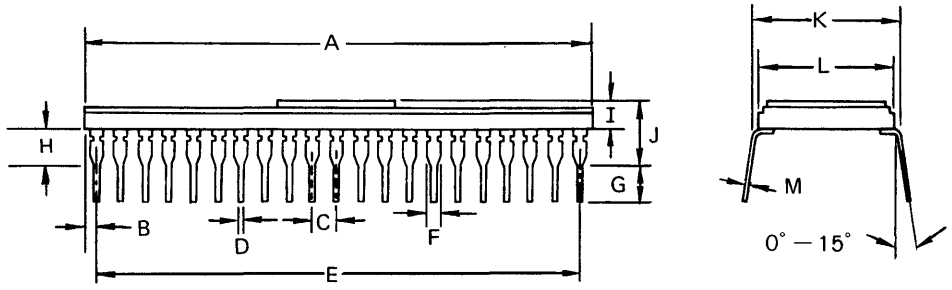


FIGURE 13
PIN CONFIGURATION



ITEM	MILLIMETERS	INCHES
A	53.5 Max.	2.1 Max.
B	1.35	0.05
C	2.54	0.10
D	0.5	0.02
E	50.80	2.0
F	1.27	0.05
G	2.54 Max.	0.10 Min.
H	1.0 Min.	0.04 Min.
I	4.2 Max.	0.17 Max.
J	5.2 Max.	0.21 Max.
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

FIGURE 14
PACKAGE OUTLINE

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PRINTED IN U.S.A.

UM371-7-77-2K

$10