PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD30101

VR4101™

64-BIT MICROPROCESSOR

DESCRIPTION

The μPD30101 (VR4101) is one of NEC's VR series RISC (Reduced Instruction Set Computer) microprocessors and is a high-performance 64-bit microprocessor employing the MIPS RISC architecture.

The VR4101 is ideal for applications in battery-driven, high-performance portable information systems. This microprocessor uses the high-performance, super power-saving VR4100™ as the CPU core, and has many peripheral circuits such as DMA, serial interface, keyboard interface, IrDA interface, touch panel interface, and real-time clock.

The functions of the VR4101 are explained in detail in the following manual. Be sure to refer to this manual when designing your system.

- **VR4101 User's Manual (U12149E)**

FEATURES

- Employs 64-bit MIPS architecture
  - 5-stage pipeline
  - Conforms to MIPS-III instruction set (Floating-point instructions are supported through software emulation.)
- Supports high-speed sum-of-products operation instructions
- Power consumption as low as 250 mW TYP. (at 33 MHz and 3.3 V)
- Supports three types of power control modes
- External clock: 32 kHz, Internal operating frequency: 33 MHz
- Clock generator and PLL (× 1012)
- DRAM interface and ROM interface (Flash memory is also supported.)
- DMA controller (5 channels)
- Peripheral circuits ideal for portable systems
  LCD interface, keyboard interface, and touch panel interface
- IrDA controller
- Supports subset of ISA bus
- Serial interface and debug serial interface
- Supply voltage: 3.0 to 3.6 V
- Package: 160-pin plastic LQFP

APPLICATIONS

- Battery-driven portable information systems
- Embedded controllers, etc.

ORDERING INFORMATION

Part Number	Package
μPD30101GM-33-8ED	160-pin plastic LQFP (fine pitch) (24 × 24 mm)

The information in this document is subject to change without notice.

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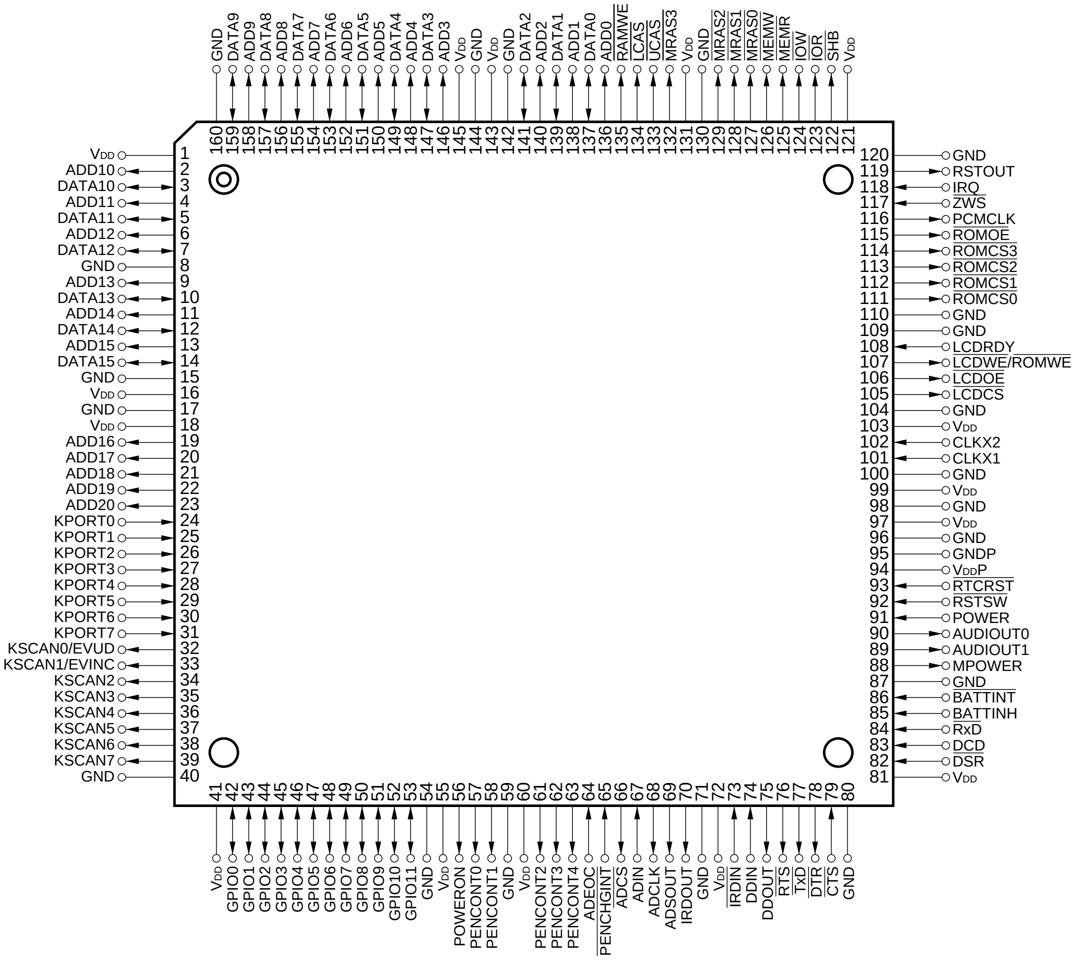
The mark ★ shows major revised points.

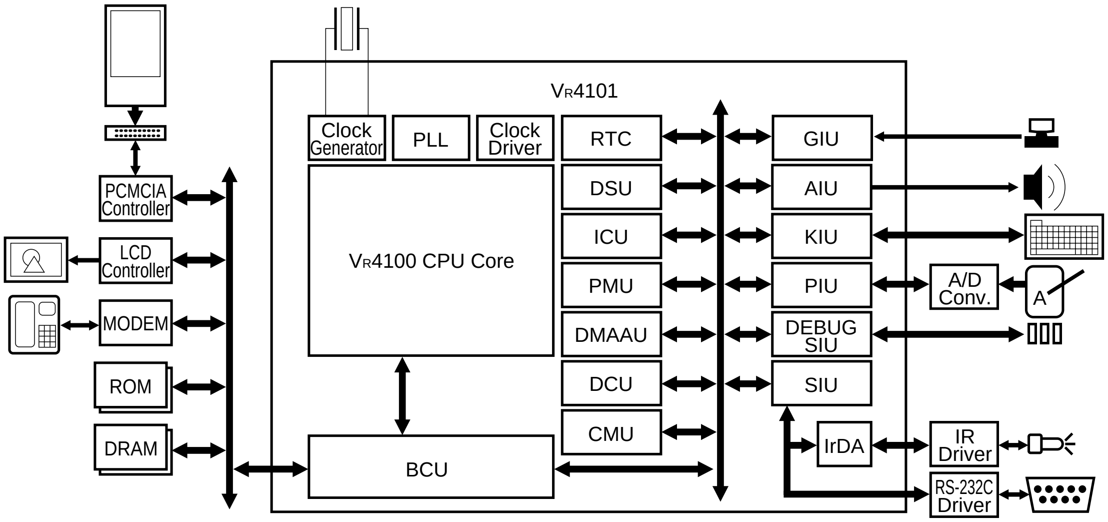
PIN CONFIGURATION



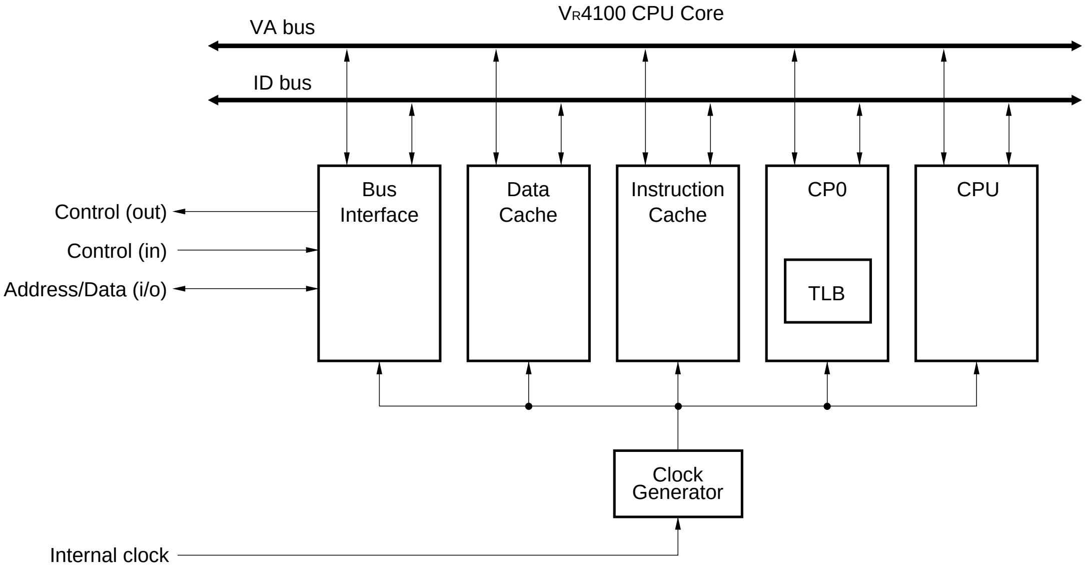
PIN NAME

ADCLK	: A/D Converter Clock
$\overline{\text{ADCS}}$	: A/D Converter Chip Select
ADD (0:20)	: Address Bus
ADEOC	: A/D Converter End of Change
ADIN	: A/D Converter Data In
ADSOUT	: A/D Converter Serial Out
AUDIOUT (0:1)	: Audio Out
$\overline{\text{BATTINH}}$	: Battery Inhibit
$\overline{\text{BATTINT}}$	: Battery Interrupt
CLKX1	: Clock X1
CLKX2	: Clock X2
$\overline{\text{CTS}}$	: Clear to Send
DATA (0:15)	: Data Bus
DCD	: Data Carrier Detection
DDIN	: Debug Serial Data In
DDOUT	: Debug Serial Data Out
$\overline{\text{DSR}}$	: Data Set Ready
$\overline{\text{DTR}}$	: Data Terminal Ready
EVINC	: Electric Volume Input Clock
EVUD	: Electric Volume Up/Down
GND	: Ground
GNDP	: Quiet GND for PLL
GPIO (0:11)	: General Purpose I/O
$\overline{\text{IOR}}$	: I/O Read
$\overline{\text{IOW}}$	: I/O Write
$\overline{\text{IRDIN}}$	: IrDA Data In
IRDOUT	: IrDA Data Out
IRQ	: Interrupt Request
KPORT (0:7)	: Key Scan Data In
KSCAN (0:7)	: Key Scan Data Out
$\overline{\text{LCAS}}$	: Lower Column Address Strobe
$\overline{\text{LCDCS}}$	: LCD Chip Select
$\overline{\text{LCDOE}}$	: LCD Output Enable
LCDRDY	: LCD Ready
$\overline{\text{LCDWE}}$	: LCD Write Enable
$\overline{\text{MEMR}}$	: Memory Read
$\overline{\text{MEMW}}$	: Memory Write
MPOWER	: Main Power On
$\overline{\text{MRAS (0:3)}}$	: DRAM Row Address Strobe
PCMCLK	: PCM Clock
$\overline{\text{PENCHGINT}}$	: Pen Change Interrupt
PENCONT (0:4)	: Touch Panel Control
POWER	: Power On Switch
POWERON	: Power On State
$\overline{\text{RAMWE}}$	: DRAM Write Enable
$\overline{\text{ROMCS (0:3)}}$	: ROM Chip Select
$\overline{\text{ROMOE}}$	: ROM Output Enable
$\overline{\text{ROMWE}}$	: ROM Write Enable
RSTOUT	: PCM Reset
$\overline{\text{RSTSW}}$	: Reset Switch
$\overline{\text{RTCRST}}$	: Real Time Clock Reset
$\overline{\text{RTS}}$	: Request to Send
$\overline{\text{RxD}}$	: Receive Data
$\overline{\text{SHB}}$	: System Bus Hi-Byte Enable
$\overline{\text{TxD}}$	: Transmit Data
$\overline{\text{UCAS}}$	: Upper Column Address Strobe
V_{DD}	: Power Supply Voltage
V_{DD}P	: Quiet V_{DD} for PLL
$\overline{\text{ZWS}}$	: Zero Wait State

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 Pin Functions

(1) System bus interface signals

Signal Name	I/O	Functional Description
ADD (0:20)	Output	21-bit address bus. Used to specify addresses of DRAM, ROM, LCD, or PCMCIA.
DATA (0:15)	I/O	16-bit data bus. Used to transfer data from V$_R$4101 to DRAM, ROM, LCD, or PCMCIA, and vice versa.
$\overline{\text{LCDCS}}$	Output	LCD chip select signal. Asserted active when V$_R$4101 accesses LCD via ADD bus and DATA bus.
$\overline{\text{LCDOE}}$	Output	LCD output enable signal. Asserted active when V$_R$4101 reads data from LCD.
$\overline{\text{LCDWE}}$/$\overline{\text{ROMWE}}$	Output	Multiplexed signal of LCD write enable signal and flash memory write enable signal. This signal functions as LCD write enable signal when $\overline{\text{LCDCS}}$ pin is active, and is asserted active when V$_R$4101 writes data to LCD. When $\overline{\text{LCDCS}}$ pin is inactive, this signal functions as ROM write enable signal, and is asserted active when V$_R$4101 writes data to flash memory.
LCDRDY	Input	LCD ready signal. Assert this signal active when LCD or PCMCIA controller is ready for access by V$_R$4101.
$\overline{\text{ROMCS (0:3)}}$	Output	ROM chip select signals. Used to select ROM to be accessed from up to four ROMs connected to V$_R$4101.
$\overline{\text{ROMOE}}$	Output	ROM output enable signal. Asserted active when V$_R$4101 reads data from ROM.
$\overline{\text{MRAS (0:3)}}$	Output	RAS signals of DRAM. Asserted active when valid row address of RAM to be accessed is output onto ADD bus. Up to four RAMs can be connected to V$_R$4101.
$\overline{\text{UCAS}}$	Output	CAS signal of DRAM. Asserted active when valid column address is output onto ADD bus when high-order byte of DRAM is accessed.
$\overline{\text{LCAS}}$	Output	CAS signal of DRAM. Asserted active when valid column address is output onto ADD bus when low-order byte of DRAM is accessed.
$\overline{\text{RAMWE}}$	Output	DRAM write enable signal. Asserted active when V$_R$4101 writes data to DRAM.
PCMCLK	Output	PCMCIA card clock. Outputs 8-MHz clock to be supplied to PCMCIA controller.
$\overline{\text{SHB}}$	Output	PCMCIA bus high byte enable signal. Asserted active if high-order byte of DATA bus is valid when PCMCIA is accessed.
$\overline{\text{IOR}}$	Output	PCMCIA card I/O read signal. Asserted active when V$_R$4101 reads data from I/O port of PCMCIA.
$\overline{\text{IOW}}$	Output	PCMCIA card I/O write signal. Asserted active when V$_R$4101 writes data to I/O of PCMCIA.
$\overline{\text{MEMR}}$	Output	PCMCIA card memory read signal. Asserted active when V$_R$4101 reads data from memory of PCMCIA.
$\overline{\text{MEMW}}$	Output	PCMCIA card memory write signal. Asserted active when V$_R$4101 writes data to memory of PCMCIA.
$\overline{\text{ZWS}}$	Input	PCMCIA zero wait state signal. Assert this signal active when PCMCIA controller is ready for access by V$_R$4101.
IRQ	Input	PCMCIA card interrupt request signal. PCMCIA controller asserts this pin active to inform V$_R$4101 of interrupt.
RSTOUT	Output	PCMCIA card reset signal. Asserted active when V$_R$4101 resets PCMCIA controller.

(2) Clock interface signals

Signal Name	I/O	Functional Description
CLKX1	Input	32-kHz clock input pin. Connect one end of 32-kHz crystal resonator to this pin.
CLKX2	Input	32-kHz clock input pin. Connect one end of 32-kHz crystal resonator to this pin.

(3) Battery monitor interface signals

Signal Name	I/O	Functional Description
BATTINH	Input	Interrupt signal indicating battery voltage level on power application. External circuit checks battery voltage on power application and, if it judges that battery voltage is sufficient for operation, asserts this pin active.
$\overline{\text{BATTINT}}$	Input	Interrupt signal indicating battery voltage level during normal operation. External circuit checks battery voltage and, if it judges that battery voltage is not sufficient for operation, asserts this pin active.

(4) Initialization interface signals

Signal Name	I/O	Functional Description
MPOWER	Output	Signal to turn ON main power. VR4101 turns ON power supply to external DC/DC converter by asserting this pin active.
POWERON	Output	Signal indicating that VR4101 is to start from Hibernate mode. It is asserted active when start cause is detected, and deasserted inactive after battery check has been completed.
POWER	Input	Signal indicating that power-ON switch has been pressed. When power-ON switch has been pressed, external circuit asserts this pin active.
$\overline{\text{RSTSW}}$	Input	Signal indicating that reset switch has been pressed. When reset switch has been pressed, external circuit asserts this pin active.
$\overline{\text{RTCRST}}$	Input	Signal resetting RTC. When power is supplied to system for first time, external circuit asserts this pin active for 230 ms.

(5) RS-232C interface signals

Signal Name	I/O	Functional Description
$\overline{\text{RxD}}$	Input	Receive data signal. Used to transfer serial data from RS-232C driver/receiver to VR4101.
$\overline{\text{TxD}}$	Output	Transmit data signal. Used to transfer serial data from VR4101 to RS-232C driver/receiver.
$\overline{\text{RTS}}$	Output	Transmit request signal. VR4101 asserts this signal active when it wishes to transmit serial data.
$\overline{\text{CTS}}$	Input	Transmit enable signal. Assert this signal active when RS-232C driver/receiver is ready to receive serial data.
DCD	Input	Carrier detection signal. Assert this signal active while valid serial data is being received. If this signal is asserted active in Hibernate mode and in shutdown state, Fullspeed mode can be restored.
$\overline{\text{DTR}}$	Output	Terminal equipment ready signal. VR4101 asserts this signal active when it is ready to transmit/receive serial data.
$\overline{\text{DSR}}$	Input	Data set ready signal. Assert this signal active when RS-232C driver/receiver and VR4101 are ready to transmit/receive serial data.

(6) IrDA interface signals

Signal Name	I/O	Functional Description
$\overline{\text{IRDIN}}$	Input	IrDA serial data input signal. Used to transfer serial data from VR4101 to IrDA controller.
IRDOUT	Output	IrDA serial data output signal. Used to transfer serial data from IrDA controller to VR4101.

(7) Debug serial interface signals

Signal Name	I/O	Functional Description
DDIN	Input	Debug serial data input signal. Used to transfer serial data from VR4101 to external debug serial controller.
DDOUT	Output	Debug serial data output signal. Used to transfer serial data from external debug serial controller to VR4101.

(8) Keyboard interface signals

Signal Name	I/O	Functional Description
KPORT (0:7)	Input	Keyboard scan data input signals. Used to scan input from keyboard.
KSCAN (2:7)	Output	Keyboard scan data output signals. Assert scan line active when input from keyboard is scanned.
KSCAN1/EVINC	Output	Multiplexed signal of keyboard scan data output signal and electronic volume control clock signal. If EVINC pin is enabled to output by EVVOLREG register, this signal functions as clock output pin to electronic volume controller.
KSCAN0/EVUD	Output	Multiplexed signal of keyboard scan data output signal and electronic volume Up/Down signal. When EVUD pin is enabled to output by EVVOLREG register, this signal functions as volume UP/DOWN pin for electronic volume controller.

(9) Audio interface signals

Signal Name	I/O	Functional Description
AUDIOUT (0, 1)	Output	Audio output signals. Output audio signals when WAVE file is reproduced.

(10) Touch panel interface signals

Signal Name	I/O	Functional Description
$\overline{\text{ADCS}}$	Output	A/D converter chip select signal. This signal is asserted active when data is transferred or received to or from A/D converter.
ADCLK	Output	Clock output signal to supply clock to A/D converter.
ADIN	Input	Input pin to receive output data from A/D converter.
ADSOUT	Output	A/D converter serial data output signal. Used to output serial data to set A/D converter.
ADEOC	Input	A/D converter data conversion end signal. Assert this signal active when A/D conversion by A/D conversion has been completed.
PENCONT (0:4)	Output	Touch panel control signals. Output signals controlling voltage applied to touch panel.
$\overline{\text{PENCHGINT}}$	Input	Touch panel interrupt. External circuit asserts this pin active when touch panel is pressed.

(11) General-purpose I/O signals

Signal Name	I/O	Functional Description
GPIO (0:11)	I/O	General-purpose I/O pins. However, fix function of GPIO9 to battery lid lock detection signal (BATTLOCK).

(12) Other signals

Signal Name	I/O	Functional Description
V_{DD}	—	Positive power supply pin
$V_{DD}P$	—	Power supply for internal PLL
GND	—	Ground pin
GNDP	—	Ground for internal PLL

1.2 Pin Status in Specific Status

(1/2)

Pin Name	At Reset by RTCRST	At Reset by Deadman's SW or RSTSW	In Suspend Mode	In Hibernate Mode or on shutdown by HALTimer
ADD (0:20)	0	×	×	0
DATA (0:15)	0	×	×	0
$\overline{\text{LCDCS}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{LCDOE}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{LCDWE}}$/$\overline{\text{ROMWE}}$	Hi-Z	1	1	Hi-Z
LCDRDY	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{ROMCS (0:3)}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{ROMOE}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{MRAS (0:3)}}$	1	Hi-Z	0	0
$\overline{\text{UCAS}}$	1	Hi-Z	0	0
$\overline{\text{LCAS}}$	1	Hi-Z	0	0
$\overline{\text{RAMWE}}$	1	1	1	1
PCMCLK	0	×	×	0
$\overline{\text{SHB}}$	0	×	×	0
$\overline{\text{IOR}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{IOW}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{MEMR}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{MEMW}}$	Hi-Z	1	1	Hi-Z
$\overline{\text{ZWS}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRQ	Hi-Z	Hi-Z	Hi-Z	Hi-Z
RSTOUT	Hi-Z	0	**Note**	Hi-Z
CLKX1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
CLKX2	Hi-Z	Hi-Z	Hi-Z	Hi-Z
BATTINH	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{BATTINT}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
MPOWER	0	1	1	0
POWERON	0	0	0	0
POWER	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{RSTSW}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{RTCRST}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{RxD}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{TxD}}$	1	1	**Note**	1
$\overline{\text{RTS}}$	1	1	**Note**	1
$\overline{\text{CTS}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DCD	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{DTR}}$	1	1	**Note**	1

Note The status in the Fullspeed mode immediately before is retained.

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance, ×: Undefined

(2/2)

Pin Name	At Reset by RTCRST	At Reset by Deadman's SW or RSTSW	In Suspend Mode	In Hibernate Mode or on shutdown by HALTimer
$\overline{\text{DSR}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$\overline{\text{IRDIN}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDOUT	Hi-Z	Hi-Z	**Note**	Hi-Z
DDIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DDOUT	1	1	**Note**	1
KPORT (0:7)	Hi-Z	Hi-Z	Hi-Z	Hi-Z
KSCAN (2:7)	Hi-Z	Hi-Z	**Note**	Hi-Z
KSCAN1/EVINC	Hi-Z	Hi-Z	**Note**	Hi-Z
KSCAN0/EVUD	Hi-Z	Hi-Z	**Note**	Hi-Z
AUDIOUT (0:1)	0	0	0	0
$\overline{\text{ADCS}}$	Hi-Z	Hi-Z	**Note**	Hi-Z
ADCLK	0	0	**Note**	0
ADIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z
ADSOUT	0	0	**Note**	0
ADEOC	Hi-Z	Hi-Z	Hi-Z	Hi-Z
PENCONT (0:4)	Hi-Z	Hi-Z	**Note**	Hi-Z
$\overline{\text{PENCHGINT}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z
GPIO (0:11)	Hi-Z	Hi-Z	**Note**	Hi-Z

Note The status in the Fullspeed mode immediately before is retained.

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance

2. INTERNAL BLOCKS

2.1 VR4100 CPU Core

(1) CPU

The CPU processes integer instructions and consists of 64-bit register files, a 64-bit integer data bus, and a sum-of-products operation unit.

(2) Coprocessor 0 (CP0)

The CP0 has a memory management unit (MMU) and an exception processing function. The MMU translates addresses and checks whether an access is made between different types (user, supervisor, or kernel) of memory segments. Virtual addresses are translated to physical addresses by TLB (high-speed translation lookaside buffer).

(3) Instruction cache

The instruction cache is of direct mapping, virtual index, and physical tag type.

(4) Data cache

The data cache is of direct mapping, virtual index, physical tag, and write back type.

(5) CPU bus interface

The CPU bus interface controls data transfer between the VR4100 CPU core and BCU, one of the peripheral units. As the bus interface for the VR4100 CPU core, two 32-bit address/data multiplexed buses each for input and output, clock signals, and interrupt control signals are used.

(6) Clock generator

A 32.768-kHz crystal oscillator is oscillated by an internal oscillation circuit and multiplied by 1012 by PLL (phase-locked loop) to generate a pipeline clock (PClock). The system interface clock (SClock) is generated from PClock.

2.2 BCU (Bus Control Unit)

The BCU internally transfers data with the VR4100 CPU core via SysAD bus. It also controls the LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller connected to the system bus, and transfers data with the above devices via ADD and DATA buses.

2.3 RTC (Real-time Clock)

The RTC has a precise counter that operates with a 32.768-kHz clock supplied from the clock generator. It also has several counters and compare registers for various interrupts.

2.4 DSU (Deadman’s Switch Unit)

The DSU is used to check whether the processor is operating normally. If the software does not clear the register of this unit at specific intervals, the system is shut down.

2.5 ICU (Interrupt Control Unit)

The ICU controls interrupt requests generated from the external and internal sources of the VR4101, and reports an interrupt request, if any, to the VR4100 CPU core.

2.6 PMU (Power Management Unit)

The PMU outputs signals necessary for controlling the power of the entire system, including the VR4101. It also controls the PLL of the VR4100 CPU core and the internal clocks (PClock, TClock, and MasterOut) in the power-saving mode.

2.7 DMAAU (Direct Memory Access Address Unit)

The DMAAU controls five types of DMA transfer addresses.

2.8 DCU (Direct Memory Access Control Unit)

The DCU controls arbitration of five types of DMA transfers.

2.9 CMU (Clock Mask Unit)

The CMU controls supply of the clock (TClock or MasterOut) from the VR4100 CPU core to the internal peripheral units.

2.10 GIU (General Purpose I/O Unit)

The GIU controls 12 GPIO pins and the DCD pin. Note, however, that of the 12 GPIO pins, one is reserved for a specific application at present.

2.11 AIU (Audio Interface Unit)

The AIU can be used to generate any frequency by using PWM and outputs audio signals to external devices. It also supplies a buzzer sound.

2.12 KIU (Keyboard Interface Unit)

The KIU has eight scan lines and eight detection lines to detect input of 64 keys. It can also detect roll over of 2 or 3 keys.

2.13 PIU (Touch Panel Interface Unit)

The PIU controls detection of touching on a touch panel. The VR4101 supports two types of A/D converter interfaces: TLC2543C and TLV1543C.

2.14 DebugSIU (Debug Serial Interface Unit)

The DebugSIU is a serial interface for debugging and supports a transfer rate of up to 115 kbps.

2.15 SIU (Serial Interface Unit)

The SIU is a serial interface conforming to the RS-232C Standards, and supports a transfer rate of up to 115 kbps. In addition, a IrDA serial interface that supports a transfer rate of 115 kbps is also included, though this IrDA serial interface is exclusively used with the RS-232C interface.

3. INTERNAL ARCHITECTURE

3.1 Pipeline

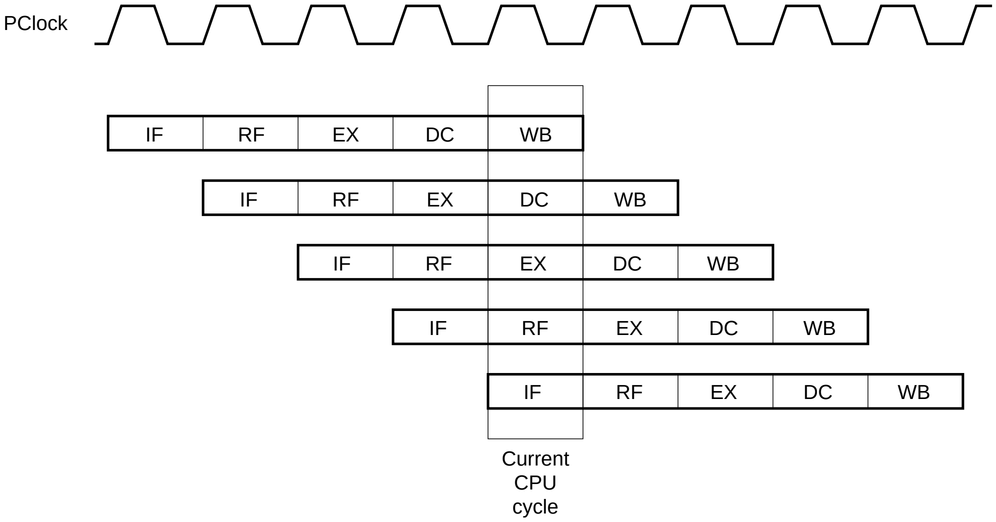
Each instruction is executed in the following five steps:

(1)	IF	Instruction fetch
(2)	RF	Register fetch
(3)	EX	Execution
(4)	DC	Data cache fetch
(5)	WB	Write back

The VR4101 has a five-stage pipeline. It takes five clocks to execute each instruction, but instructions can be executed in parallel. The pipeline clock, PClock, operates at a frequency of 33 MHz.

The following figure outlines the pipeline.

Figure 3-1. Pipeline of VR4101 (5-stage)



3.2 CPU Registers

Figure 3-2 shows the CPU registers of the VR4101. The bit width of these registers is determined by the operation mode of the processor (32 bits in 32-bit mode or 64 bits in 64-bit mode).

Of the 32 general-purpose registers, the following two have a special meaning.

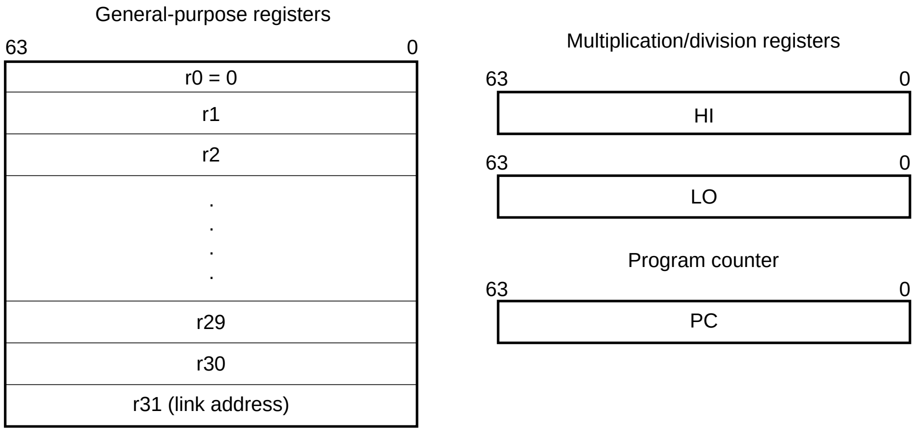
- Register r0 : The contents of this register are always 0. To discard the result of an operation, describe this register as the target of an instruction. When value 0 is necessary, this register can be used as a source register.
- Register r31 : This is a link register for the JAL and JALR instructions. Therefore, do not use this register with any other instructions.

The two multiplication/division registers (HI and LO) store the result of multiplication or sum-of-products operation, or quotient (LO) and remainder (HI) resulting from division.

Because the VR4101 does not support floating-point instructions, it is not provided with the 32 floating-point general-purpose registers (FGR) found in the VR4200™ and VR4400™.

Remark The load link bit (LL bit) used with synchronization instructions (LL and SC) for multi-processor system supported by the VR4200 and VR4400 is not provided in the VR4101 (refer to **3.3 (2) Deletion of multi-processor instructions**).

Figure 3-2. CPU Registers



The VR4101 does not have a program status word (PSW). The function of PSW is substituted by the status registers and cause registers incorporated to the system control coprocessor (CP0).

3.3 Outline of Instruction Set

Basically, the instruction set of the VR4101 conforms to the MIPS-I, -II, and -III instruction sets. However, it is different from those of the other processors in the VR series in the following four points. The difference between the VR4100 and VR4101 is that the VR4101 can manage operations including the peripheral functions by using power mode instructions (refer to **(4)**).

(1) Deletion of floating-point (FPU) instructions

Because the VR4101 does not have a floating-point unit, it does not support FPU instructions. If an FPU instruction is encountered, therefore, a reserved instruction exception occurs. If it is necessary to use an FPU instruction, emulate the instruction in software in an exception handler.

(2) Deletion of multi-processor instructions

The VR4101 does not support a multiple processor operating environment. If a synchronization support instruction (LL or SC instruction) defined by MIPS-II and -III ISA is encountered, a reserved instruction exception occurs. In addition, the load link bit (LL bit) is also unavailable.

The VR4101 executes all load/store instructions in the programmed sequence. Therefore, the SYNC instruction is treated as a NOP instruction.

(3) Addition of sum-of-products instructions

The VR4101 has a dedicated sum-of-products operation core in the CPU and additional integer sum-of-products operation instructions, in order to execute sum-of-products operation at high speeds. Note that these instructions are not correctly executed with any other processors in the VR series.

The operations by the sum-of-products instructions are as follows:

(a) MADD16 (Multiply and Add 16-bit Integer)

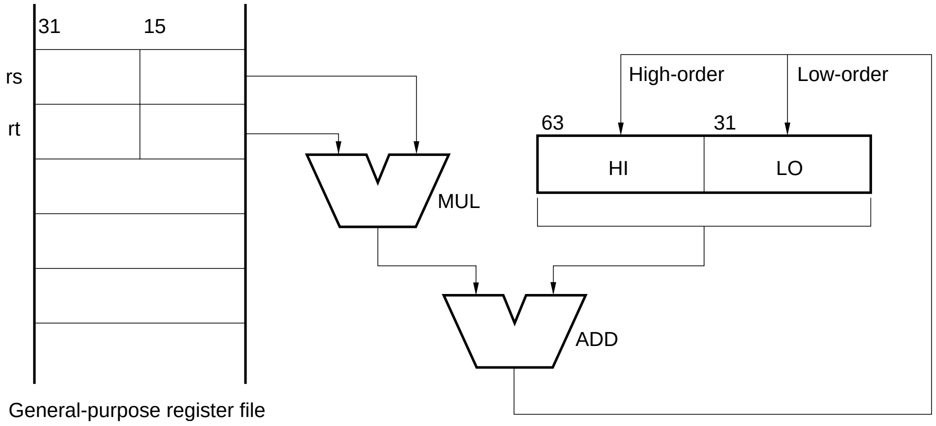
This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to a 64-bit value combining special registers HI and LO. The low-order word (64 bits) of the result is loaded to special register LO, and the high-order word is loaded to HI.

An integer overflow exception does not occur.

Figure 3-3 outline the operation of the MADD16 instruction.

Figure 3-3. Operation of MADD16 Instruction



(b) DMADD16 (Doubleword Multiply and Add 16-bit register)

This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to the value of special register LO. The result of the addition is treated as a signed integer. The 64-bit result is loaded to special register LO.

An integer overflow exception does not occur.

This operation is defined in the 64-bit mode and 32-bit kernel mode. If this instruction is encountered in the 32-bit user/supervisor mode, a reserved instruction exception occurs.

(4) Addition of power mode instructions

The VR4101 supports three power modes to lower the power consumption, and therefore, has dedicated instructions that set these modes. Note that the power mode instructions are not correctly executed by any other processors in the VR series.

The operations of the power mode instructions are as follows:

(a) STANDBY

This instruction places the processor in the Standby mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, the internal clock is fixed to the high level, and the pipeline operation is stopped.

In the Standby mode, the PLL, clocks related to timers/interrupts, and interface clocks to the peripheral function blocks (TClock and MasterOut) operate normally.

When the processor is in the Standby mode it is returned to the Fullspeed mode by any interrupt including an internally generated timer interrupt.

(b) SUSPEND

This instruction places the processor in the Suspend mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, the internal clock and TClock are fixed to the high level, and the pipeline operation and interfacing to the peripheral function blocks are stopped.

In the Suspend mode, the PLL, clocks related to timers/interrupts, and MasterOut operate normally.

The processor remains in the Suspend mode until it accepts an interrupt. When the processor accepts an interrupt, it returns to the Fullspeed mode.

(c) HIBERNATE

This instruction places the processor in the Hibernate mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, all the clocks are fixed to the high level, and the pipeline operation is stopped.

The processor remains in the Hibernate mode until either the POWER pin is asserted active or the WakeUp timer interrupt occurs. The processor returns to the Fullspeed mode when the POWER pin is asserted active, when the WakeUp Timer interrupt occurs, or when the DCD pin is asserted active.

3.4 System Control Coprocessor (CP0)

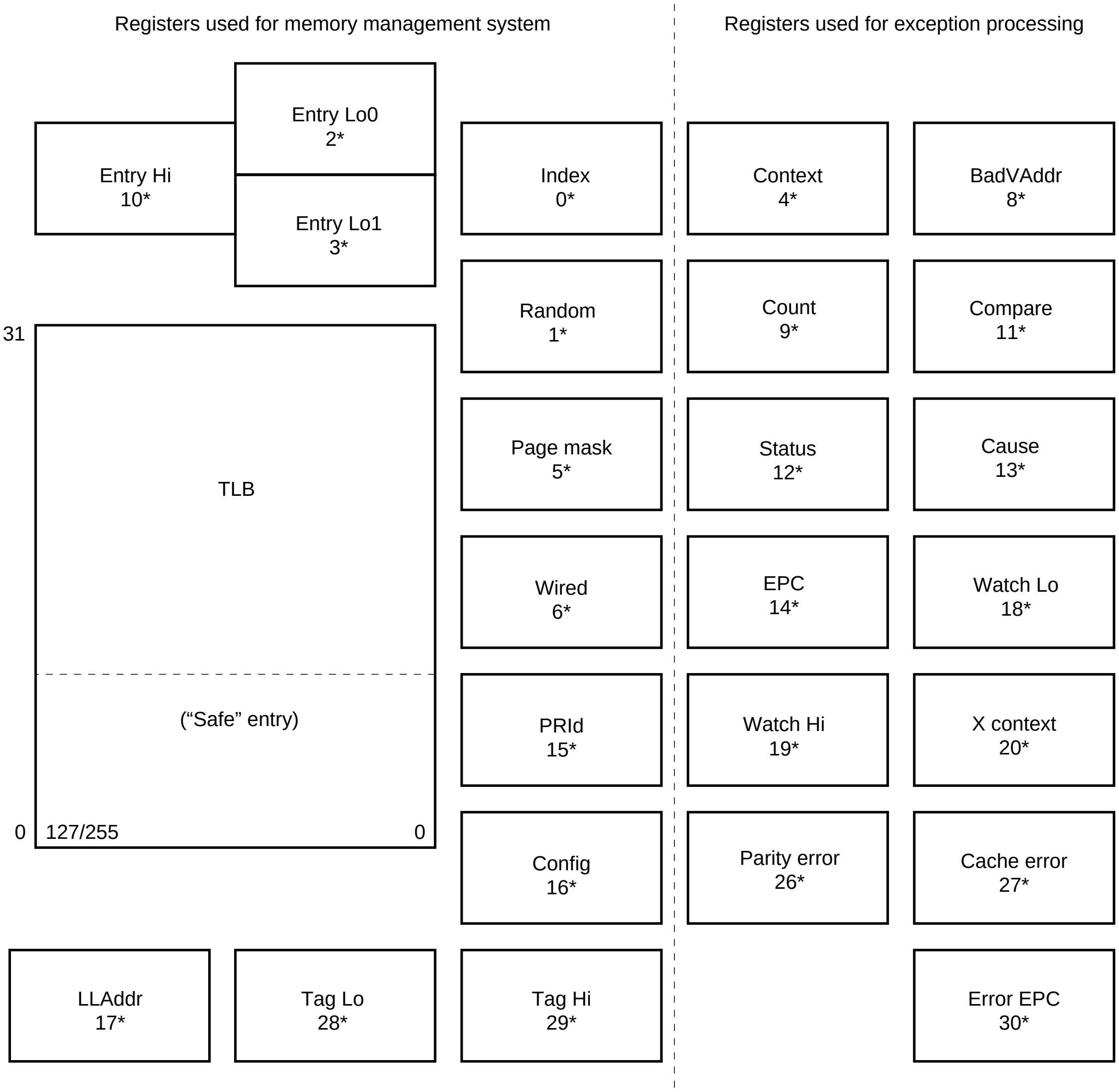
CP0 supports memory management, address translation, exception processing, and privilege operations. CP0 has the registers shown in Table 3-1, and a 32-entry TLB.

The basic configuration of the CP0 registers of the VR4101 is the same as that of the VR4200 and VR4400. However, because the number of entries of TLB, page size, cache size, physical address space, and system interface differ between the VR4101 and VR4200/VR4400, the bit configuration and setting differ. For details, refer to **VR4101 User's Manual**.

3.4.1 CP0 registers

All the CP0 registers that can be used with the VR4101 are listed below. Writing to or reading from an unused register (RFU) is undefined. In the 32-bit mode, the high-order 32 bits of 64-bit registers are masked.

Figure 3-4. CP0 Registers and TLB



Remark "*" indicates a register number.

Table 3-1. CP0 Registers

No.	Register	Description
0	Index	Programmable pointer to TLB array
1	Random	Dummy random pointer to TLB array (read-only)
2	Entry Lo0	Latter half of TLB entry for even-number VPN
3	Entry Lo1	Latter half of TLB entry for odd-number VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page mask	Specifies page size
6	Wired	Number of wired TLB entries
7	—	RFU (Reserved for Future Use)
8	BadVAddr	Indicates virtual address at which error occurs last
9	Count	Timer count
10	Entry Hi	First half of TLB entry (including ASID)
11	Compare	Timer compare value
12	Status	Sets operation status
13	Cause	Indicates cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision ID
16	Config	Sets memory system mode
17	LLAddr	RFU
18	Watch Lo	Low-order bits of memory reference trap address
19	Watch Hi	High-order bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21-25	—	RFU
26	Parity error	Parity bit of cache
27	Cache error	Error and status register of cache
28	Tag Lo	Cache tag register, low
29	Tag Hi	Cache tag register, high (reserved register)
30	Error EPC	Error exception program counter
31	—	RFU

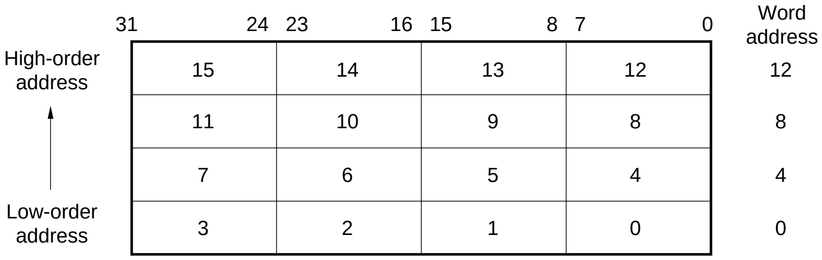
3.5 Data Format and Addressing

The VR4101 uses the following four data formats:

- Double word (64 bits)
- Word (32 bits)
- Half word (16 bits)
- Byte (8 bits)

The byte ordering is set by the BE bit of the config register. With the current VR4101, set little endian.

Figure 3-5. Byte Address in Word: Little Endian

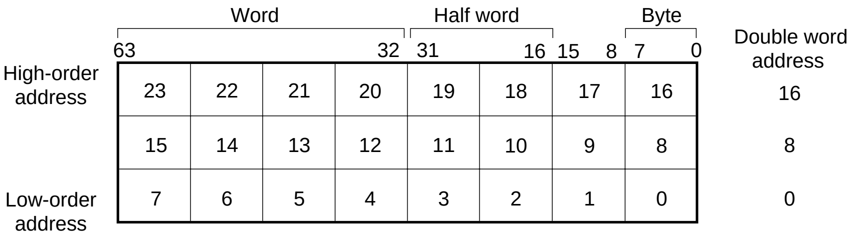


	31 24	23 16	15 8	7 0	Word address
High-order address	15	14	13	12	12
↑	11	10	9	8	8
	7	6	5	4	4
Low-order address	3	2	1	0	0

Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

Figure 3-6. Byte Address in Double Word: Little Endian



	63			32	31	16	15 8	7 0	Double word address
High-order address	23	22	21	20	19	18	17	16	16
	15	14	13	12	11	10	9	8	8
Low-order address	7	6	5	4	3	2	1	0	0

Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

3.6 Virtual Storage

The VR4101 has a virtual storage management mechanism using TLB.

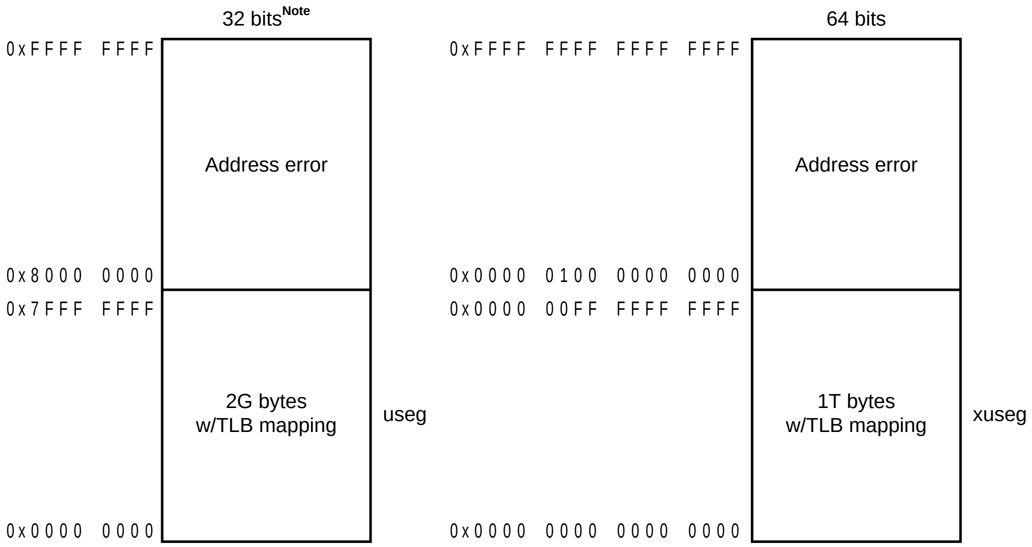
Virtual addresses are used for address management by software or address calculation of the pipeline. To access memories for program fetch and data access, and internal I/O and external I/O, physical addresses translated by TLB are used.

Note that part of the virtual address space is not translated by TLB, but is translated to physical addresses by merely changing specific addresses. If only this part of the address space is used, the VR4101 can be treated in the same manner as a CPU that operates with physical addresses.

3.6.1 Virtual address space

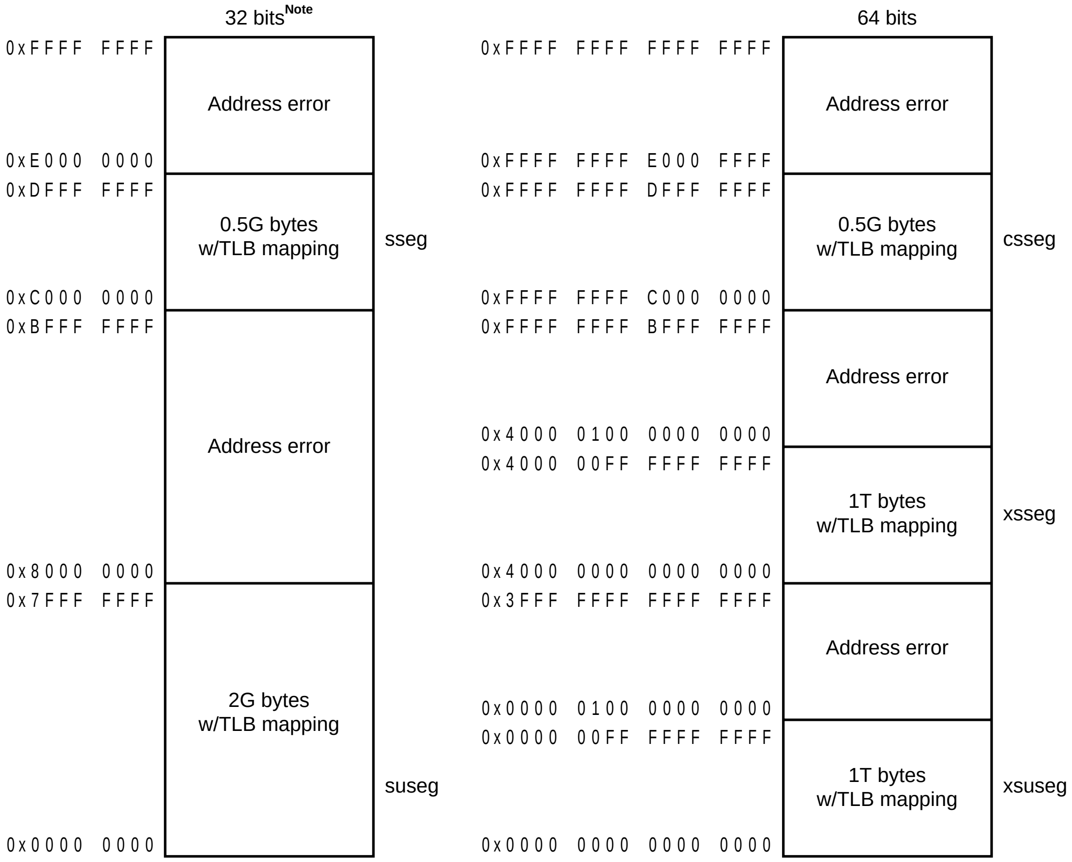
The VR4101 has two operation modes, 32-bit mode and 64-bit mode, and three types of operating modes: user mode, supervisor mode, and kernel mode. The virtual address space in each mode is shown below.

Figure 3-7. User Mode Address Space



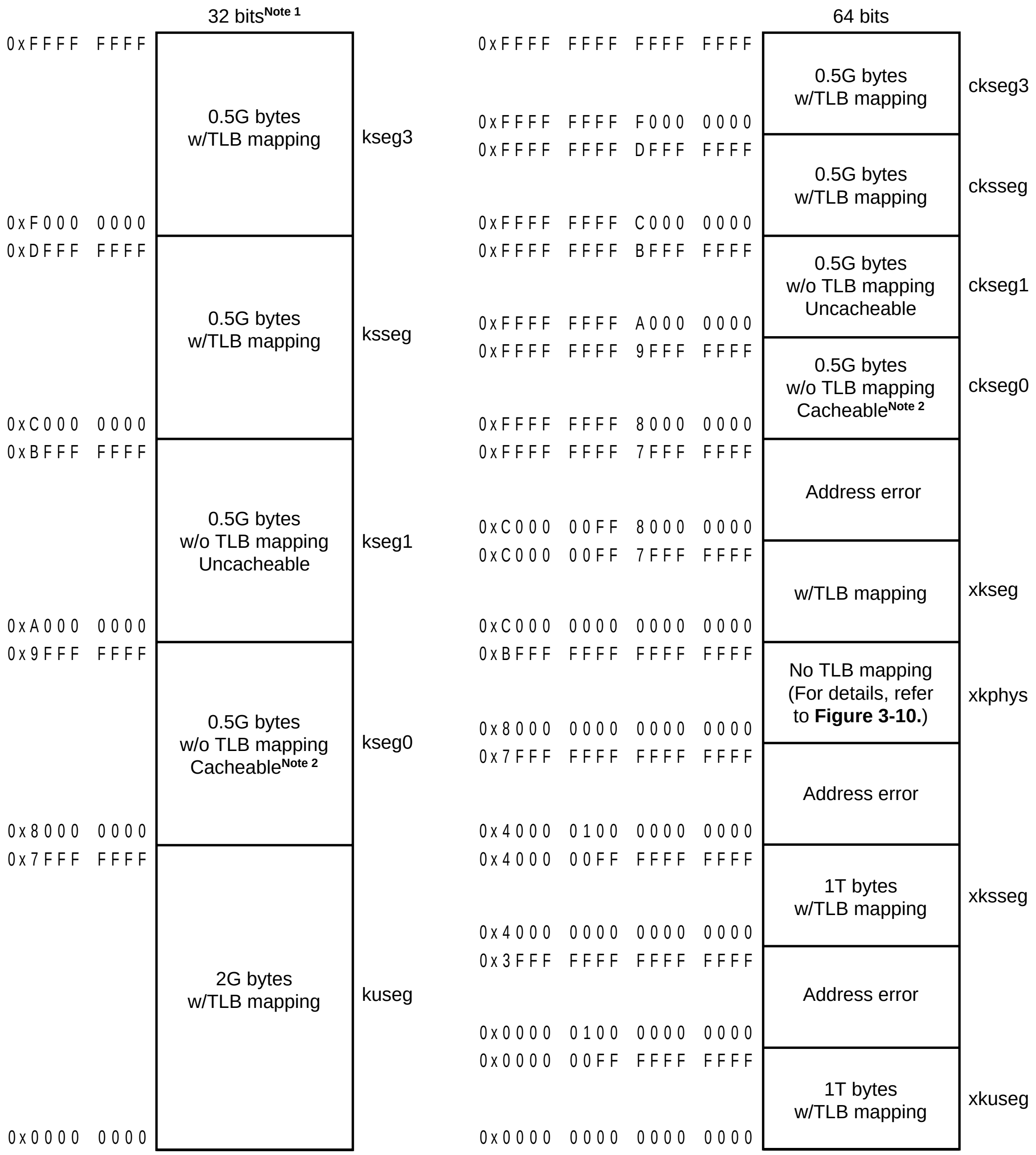
Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4101 User's Manual**.

Figure 3-8. Supervisor Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4101 User's Manual**.

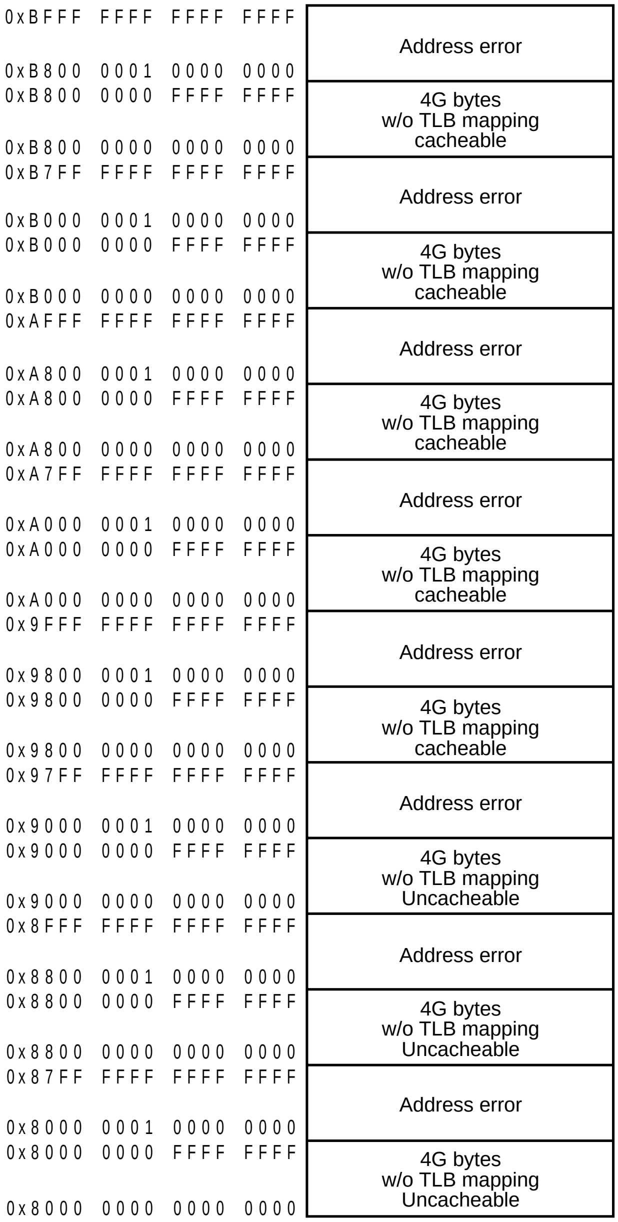
Figure 3-9. Kernel Mode Address Space



Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4101 User's Manual**.

2. Whether this area is used as a cache area is specified by the K0 field of the config register.

Figure 3-10. Details of xkphys Area



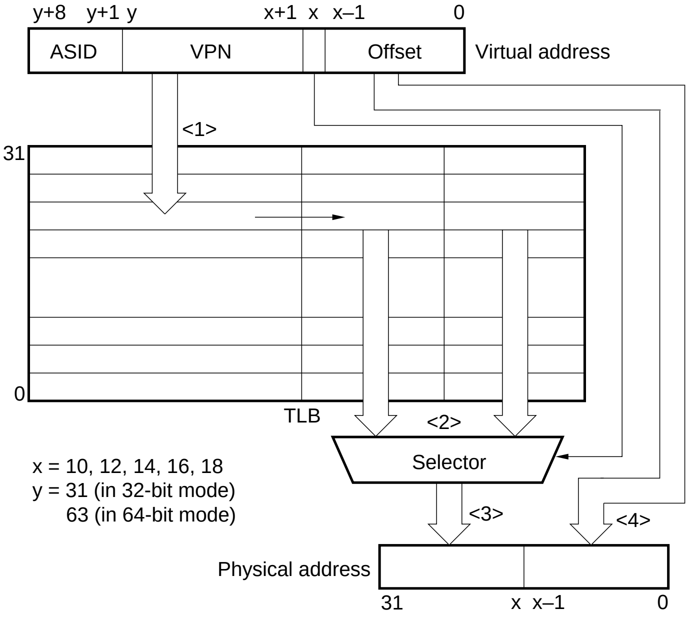
3.6.2 Address translation

Virtual addresses are translated into physical addresses by the internal TLB (Translation Lookaside Buffer) in page units. The TLB has a full-associative configuration and has 64 entries at the virtual address side and 32 entries at the physical address side. The page size is variable from 1K to 256K byte.

If a TLB entry is not found, a TLB non-coincidence exception occurs in the 32-bit mode, and an XTLB non-coincidence exception occurs in the 64-bit mode. Change the contents of the TLB in software.

The following figure outlines address translation.

Figure 3-11. Outline of Address Translation



<1> A virtual address page number (VPN) is compared with VPN in TLB.

<2> If the two VPNs coincide, a page frame number (PFN) indicating the high-order bits of a physical address is output to the selector.

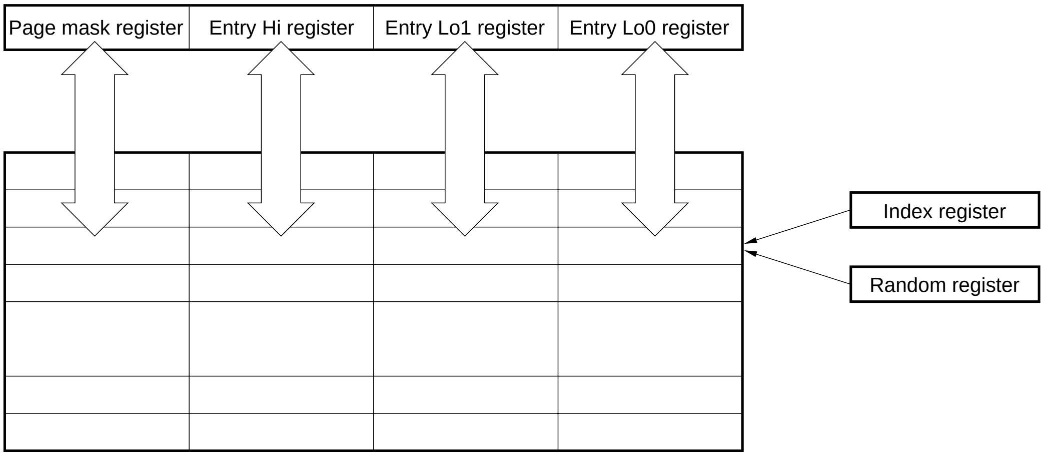
<3> If the low-order 1 bit of VPN is 0, an even page is selected; if it is 1, an odd page is selected. The selected page is output to the high-order bits of the physical address.

<4> The offset is output to the low-order bits of the physical address without going through TLB.

The TLB entry is read or written by loading/storing among the TLB entry indicated by the index register and random register, entry Hi, entry Lo1, entry Lo0, and page mask registers.

How the TLB is manipulated is illustrated below.

Figure 3-12. Outline of TLB Manipulation



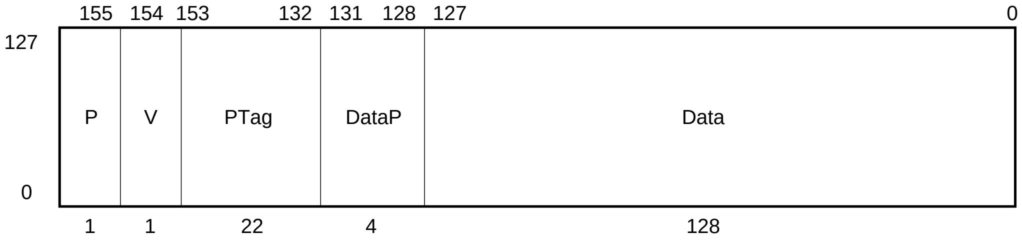
3.7 Cache

(1) Instruction cache

The instruction cache has the following features:

- Internal cache memory
- Capacity: 2K bytes
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-13. Format of Instruction Cache



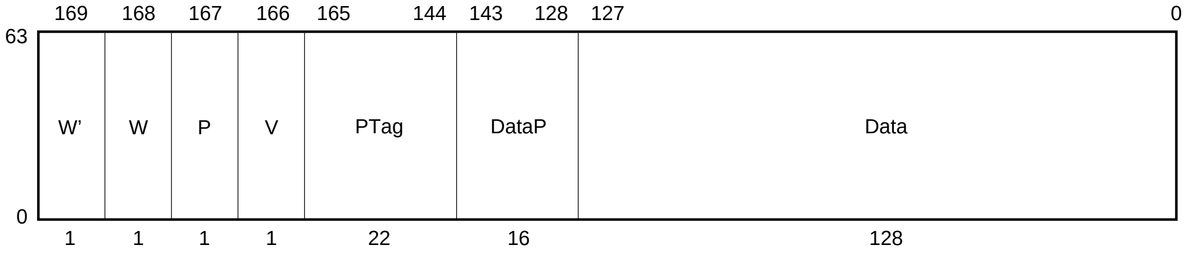
PTag : Physical tag (bits 31-10 of physical address)
V : Valid bit
Data : Cache data
P : Even parity for physical tag and V bit
DataP : Even parity for data (1-bit parity per 4-byte data)

(2) Data cache

The data cache has the following features:

- Internal cache memory
- Capacity: 1K bytes
- Write back
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-14. Format of Data Cache



W' : Even parity for write back bit
W : Write back bit
P : Even parity for physical tag and V bit
V : Valid bit
PTag : Physical tag (bits 31-10 of physical address)
DataP : Even parity for data (1-bit parity per 1-byte data)
Data : Cache data

3.8 Exception Processing

The VR4101 enters the kernel mode in which interrupts are disabled when an exception occurs, and executes an exception handler from a fixed exception vector address. To restore from the exception, the program counter, operating mode, and interrupt enable information must be restored to the original status. Save this information when the interrupt occurs.

When an interrupt occurs, the EPC register holds the address of the instruction that has caused the exception, or the address of the instruction immediately before if the exception has occurred in the branch delay slot. This means that the EPC register stores the address from which execution is to be started after the exception has been processed. At reset and on occurrence of NMI, the EPC register holds a restart address.

Table 3-2. Types of Exceptions

Exception	Symbol	Description
Cold reset	—	This exception occurs if the $\overline{\text{ColdReset}}$ (internal) and $\overline{\text{Reset}}$ (internal) signals are simultaneously asserted active (for details, refer to **Figures 4-1** through **4-5**). As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status, except some bits of the status registers, is undefined.
Soft reset	—	This exception occurs if the $\overline{\text{Reset}}$ (internal) signal is asserted active. As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status before soft reset is retained. However, the current VR4101 does not support soft reset.
NIMI	—	This exception occurs if the NMI (internal) signal is asserted active.
TLB non-coincidence	TLBL/TLBS	This exception occurs if there is no TLB entry that coincides with an address to be referenced in the 32-bit mode.
Extended addressing TLB non-coincidence	TLBL/TLBS	This exception occurs if there is no TLB entry that coincides with an address to be referenced in the 64-bit mode.
TLB invalid	TLBL/TLBS	This exception occurs if the TLB entry that coincides with the virtual address to be referenced is invalid (V bit = 0).
TLB modify	Mod	This exception occurs if the TLB entry that coincides with the virtual address to be referenced is valid but is disabled from being written (D bit = 0) when the store instruction is executed.
Bus error	IBE/DBE	This exception occurs when the external agent indicates an error of data on the SysCmd bus by using an external interrupt to the bus interface (bus time-out, bus parity error, or invalid physical memory address or access type).
Address error	AdEL/AdES	This exception occurs if an attempt is made to execute the LH, SH/LW/SW, LD, or SD instruction to the half word/word/double word not located at the half word/ word/double word boundary, or if an attempt is made to reference the virtual address that cannot be accessed.
Integer overflow	Ov	This exception occurs if a 2's complement overflow occurs as a result of addition or subtraction.
Trap	Tr	This exception occurs if the condition is true as a result of executing the trap instruction.
System call	Sys	This exception occurs if the SYSCALL instruction is executed.
Breakpoint	Bp	This exception occurs if the BREAK instruction is executed.
Reserved instruction	RI	This exception occurs if an instruction with an undefined op code (bits 31-26) or SPECIAL instruction with an undefined op code (bits 5-0) is executed.
Coprocessor non-usable	CpU	This exception occurs if the coprocessor instruction is executed when the corresponding coprocessor enable bit is not set.
Interrupt	Int	This exception occurs if one of the eight interrupt sources becomes active.
Cache error	—	This exception occurs if a parity error is detected in the internal cache or system interface.
Watch	WATCH	This exception occurs if an attempt is made to reference a physical address set by the watch Lo/Hi register with the load/store instruction.

The exception vectors and their offset values in the 64-bit and 32-bit modes are shown below.

Table 3-3. Base Address of Exception Vector in 64-Bit Mode (virtual address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xFFFF FFFF BFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xFFFF FFFF A000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0100
TLB non-coincidence, EXL =0	0xFFFF FFFF 8000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0000
XTLB non-coincidence, EXL = 0		0x0080
Others		0x0180

Table 3-4. Base Address of Exception Vector in 32-Bit Mode (virtual address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xBFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xA000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0100
TLB non-coincidence, EXL =0	0x8000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0000
XTLB non-coincidence, EXL = 0		0x0080
Others		0x0180

4. INITIALIZATION INTERFACE

This section explains the initialization interface and processor mode. Also explained are reset signal description and type, dependency of signals and timing, and initialization sequence in the mode the user can select.

4.1 Reset Function

The VR4101 can be reset in the following five ways. For details, refer to the **VR4101 User's Manual**.

4.1.1 RTC reset

Assert the $\overline{\text{RTCRST}}$ pin active on power application.

RTC reset does not save the status information at all, and completely initializes the internal status of the processor. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RTC reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4101 is reset, completely initialize the processor in software.

4.1.2 RSTSW

Assert the $\overline{\text{RSTSW}}$ pin active.

Reset by RSTSW initializes all the internal statuses except the RTC timer and PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RSTSW reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4101 is reset, completely initialize the processor in software.

4.1.3 Deadman's SW

The VR4101 is reset if Deadman's SW is not cleared within a specific time after Deadman's SW was enabled.

Reset by Deadman's SW initializes all the internal statuses except the RTC timer and PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after Deadman's SW reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4101 is reset, completely initialize the processor in software.

4.1.4 Software shutdown

When the software executes the HIBERNATE instruction, the VR4101 places the DRAM in the self-refresh mode, deasserts the MPOWER pin inactive, and enters the reset status.

Reset by software shutdown initializes all the internal statuses except the RTC timer and PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4101 is reset, completely initialize the processor in software.

4.1.5 HALTimer shutdown

The VR4101 enters the reset status if HALTimer is not cleared by software within 4 seconds after RTC reset has been cleared.

Reset by HALTimer initializes all the internal statuses except the RTC timer and PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4101 is reset, completely initialize the processor in software.

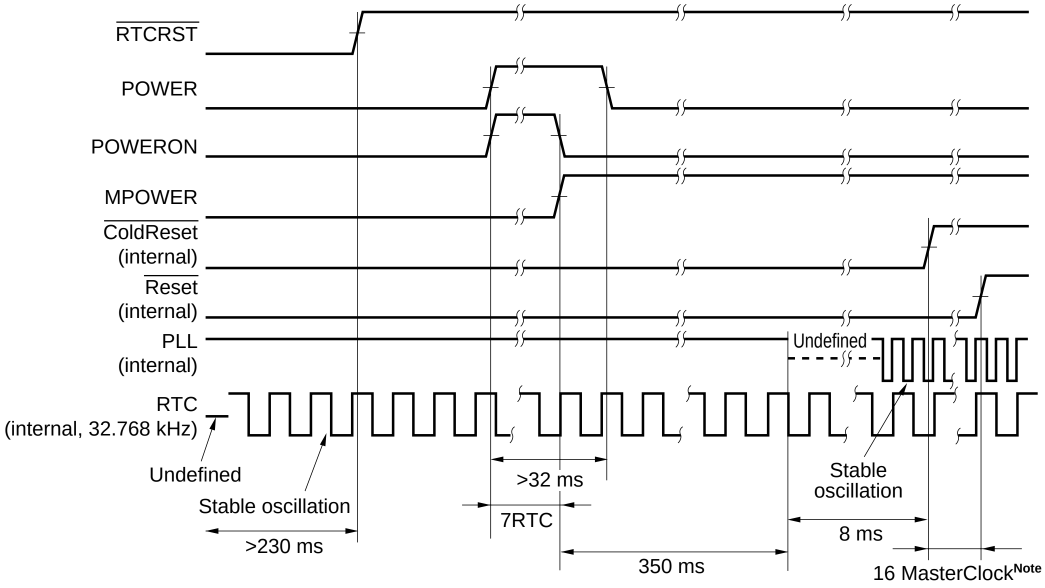
4.2 CPU Core Registers at Reset

Each of the CPU core registers is reset as follows:

- The TS and SR bits of the status register are cleared to 0.
- The ERL and BEV bits of the status register are set to 1.
- The upper-limit value (31) is set to the random register.
- The wired register is initialized to 0.
- Bits 31 through 28 of the config register are cleared to 0, and bits 22 through 3 are set to 0x04800. The other bits are undefined.
- The values of the registers other than above are undefined.

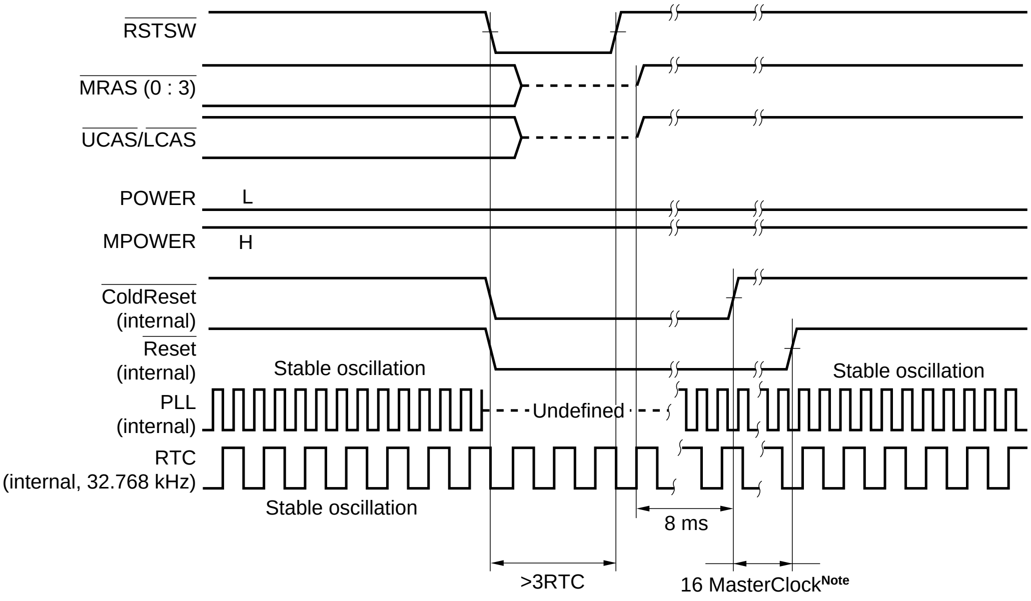
Figures 4-1 through 4-5 show the timing of RTC reset, RSTSW, Deadman's SW, software shutdown, and HALTimer shutdown.

Figure 4-1. RTC Reset



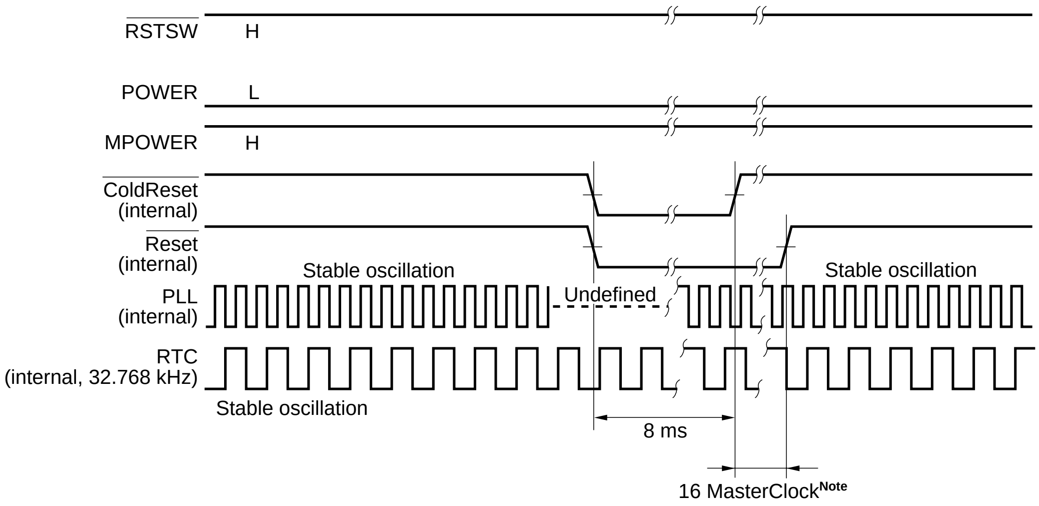
Note MasterClock is the basic clock in the CPU core.

Figure 4-2. RSTSW



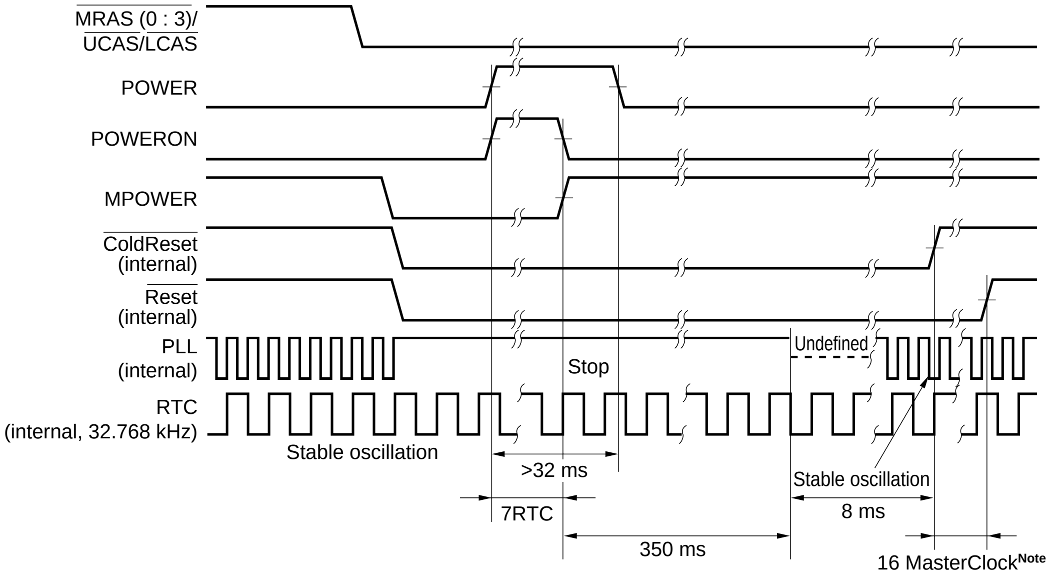
Note MasterClock is the basic clock in the CPU core.

Figure 4-3. Deadman's SW



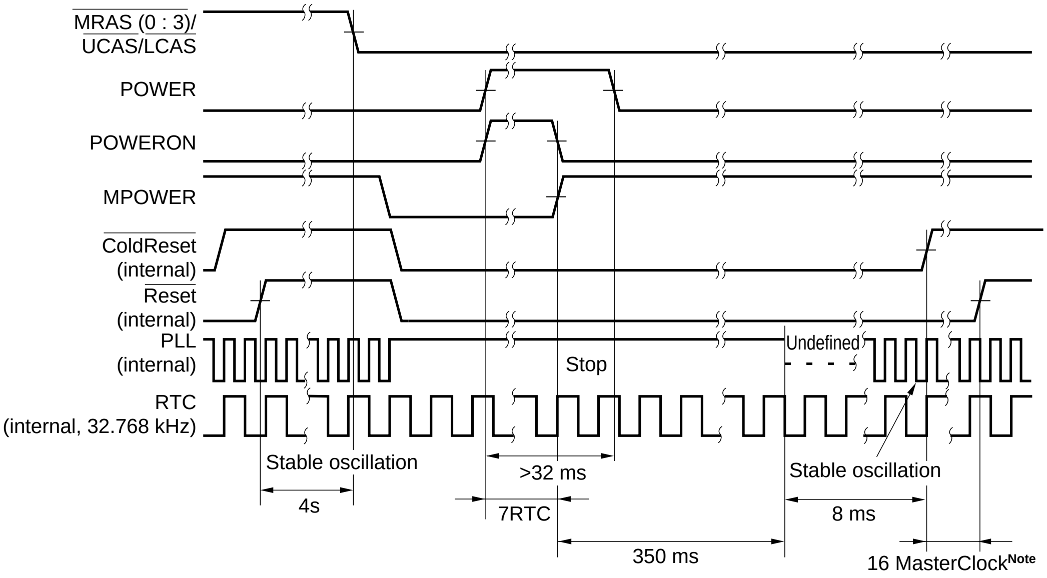
Note MasterClock is the basic clock in the CPU core.

Figure 4-4. Software Shutdown



Note MasterClock is the basic clock in the CPU core.

Figure 4-5. HALTimer Shutdown



Note MasterClock is the basic clock in the CPU core.

4.3 PowerOn Sequence

The causes that change the status of the VR4101 from the Hibernate mode or shutdown status to the Fullspeed mode are called start causes. The start causes include asserting the POWERON pin active, asserting the DCD pin active, and alarm from the WakeUp timer. When a start cause occurs, the VR4101 asserts the POWERON pin active to inform the external circuit that power to the VR4101 is about to be turned ON. Three RTC clocks after the POWERON pin has been asserted active, the VR4101 checks the status of the BATTINH and GPIO9 (BATTLOCK) pins. When the BATTINH or GPIO9 (BATTLOCK) pin is low, the VR4101 deasserts the POWERON pin inactive one RTC clock after checking the BATTINH or GPIO9 pin status, and is not started. If both the BATTINH and GPIO9 (BATTCLOCK) pins are high, the VR4101 deasserts the POWERON pin inactive four RTC clocks after the checking, asserts the MPOWER pin active, and is started.

Figure 4-6 shows the timing chart where the VR4101 is started. Figure 4-7 shows the timing chart where the VR4101 is not started because the BATTINH pin is low.

Figure 4-6. Start Sequence of VR4101 (if started)

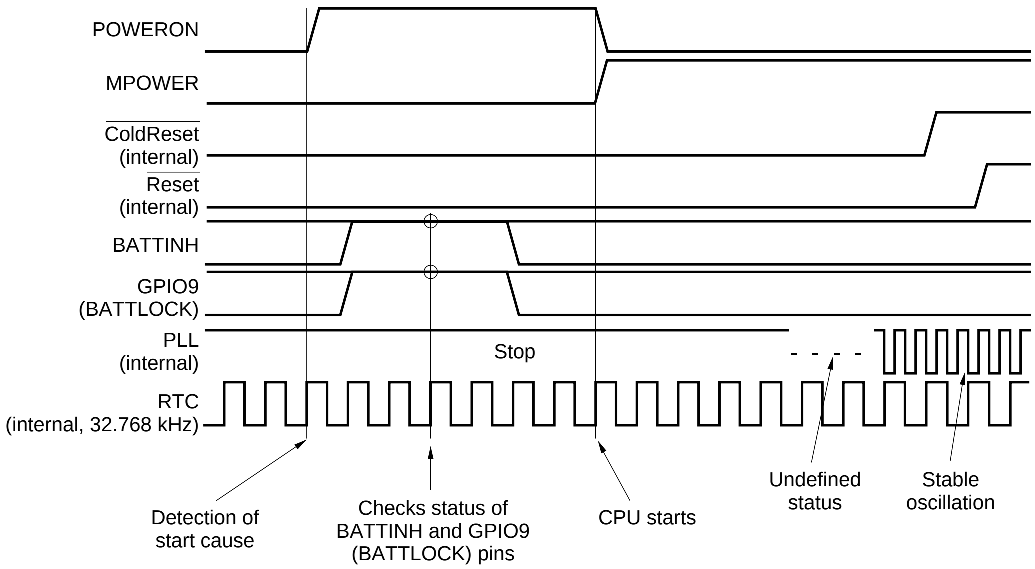
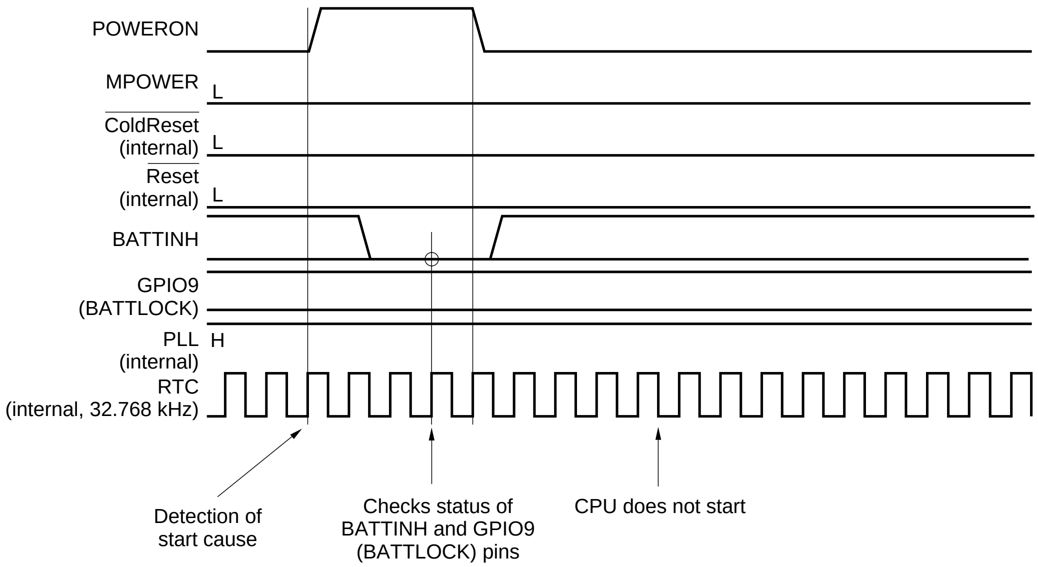


Figure 4-7. Start Sequence of VR4101 (if not started)



4.4 Modes of VR4101

The VR4101 supports various modes which can be selected by the user. The mode of the CPU core is specified by writing data to the status register and config register. The mode of the internal peripheral circuits is specified by writing data to the I/O register.

This section explains the operation modes of the CPU.

4.4.1 Power mode

The VR4101 supports four power modes: Fullspeed, Standby, Suspend, and Hibernate.

(1) Fullspeed mode

Normally, the processor clock (PClock) operates at 33 MHz. The system bus clock operates at the same rate as the PClock.

In the default status, the processor operates in the Fullspeed mode. After reset, it returns to the Fullspeed mode.

(2) Standby mode

The processor can be set in the Standby mode when the STANDBY instruction is executed. In this mode, all the internal clocks of the CPU core, except the timers and interrupts, are kept high. All the peripheral units operate in the same manner as in the Fullspeed mode. Therefore, DMA operation can be executed even in the Standby mode.

When the STANDBY instruction has completed the WB stage, the VR4101 stands by until the SysAD bus (internal) enters the idle status. After that, the internal clock of the CPU core is shut down, and the pipeline stops operating. However, the PLL, timers, interrupt clock, and internal bus clocks (TClock and MasterOut) continue operating.

The processor in the standby mode returns to the Fullspeed mode when an interrupt, including the internally generated timer interrupt, occurs.

(3) Suspend mode

The processor can be set in the Suspend mode when the SUSPEND instruction is executed. In this mode, the processor stalls the pipeline and keeps all the internal clocks, except the PLL and interrupts, high. Supply of TClock to the peripheral units is stopped. Therefore, the peripheral units, except specific interrupt units (such as the one that controls the DCD pin), cannot operate. In this status, the contents of the registers and cache are retained.

When the SUSPEND instruction has completed the WB stage, the VR4101 places the DRAM in the self-refresh mode and stands by until the internal SysAD bus enters the idle status. After that, the internal clock of the CPU core is shut down, and the pipeline continues operating. Supply of TClock to the peripheral units is stopped. However, the PLL, timers, interrupt clock, and internal bus clocks (TClock and MasterOut) continue operating.

The processor remains in the Suspend mode until it accepts an interrupt. When the processor accepts an interrupt, it returns to the Fullspeed mode.

(4) Hibernate mode

The processor can be set in the Hibernate mode when the HIBERNATE instruction is executed. In this mode, the processor stops supply of the clock to all the units. In this status, the contents of the registers and cache are retained, and output of TClock and MasterOut is stopped.

The processor remains in the Hibernate mode until the POWER pin is asserted active or the WakeUp timer interrupt occurs. If the POWER pin is asserted active, if the WakeUp timer interrupt occurs, or if the DCD pin is asserted active, the processor returns to the Fullspeed mode. The power consumption in this mode is almost 0 W (not completely 0 W because a 32.768-kHz oscillator and internal circuits that operate at 32.768 kHz exist).

4.4.2 Privilege mode

The VR4101 supports three system modes: kernel-, supervisor-, and user-extended addressing. These three modes are explained below.

(1) Kernel-extended addressing mode

When the KX bit of the status register is set, extended TLB non-coincidence exception vector is used for TLB non-coincidence of the kernel address. In the kernel mode, the MIPS III op code can be always used, regardless of the KX bit.

(2) Supervisor-extended addressing mode

When the SX bit of the status register is set, the MIPS III op code can be used in the supervisor mode, and extended TLB non-coincidence exception vector is used for TLB non-coincidence of the supervisor address.

(3) User-extended addressing mode

When the UX bit of the status bit is set, the MIPS III op code can be used in the user mode, and the extended TLB non-coincidence exception vector is used for TLB non-coincidence of the user address. When this bit is cleared, the MIPS I and II op codes and 32-bit virtual addresses are used.

4.4.3 Reverse endian

When the RE bit of the status register is set, the endian is reversed in the user mode. However, because the VR4101 always operates in little endian, fix the RX bit to 0 (reversing is prohibited).

4.4.4 Bootstrap exception vector (BEV)

The BEV bit is used to generate an exception while the correct operations of the cache and main memory are tested during self-diagnosis. At reset and on occurrence of the NMI exception, BEV is automatically set to 1.

When the BEV bit of the status register is set, the TLB non-coincidence exception vector is changed to virtual address 0xFFFF FFFF BFC0 0200, and the general exception vector is changed to address 0xFFFF FFFF BFC0 0380.

When the BEV bit is cleared, the TLB non-coincidence exception vector is changed to 0xFFFF FFFF 8000 0000, and the general exception vector is changed to 0xFFFF FFFF 8000 0180.

4.4.5 Cache error check

When the CE bit of the status register is set, the contents of the parity error register are written to the parity bit of the data cache instead of the parity generated by the store instruction when the store instruction is executed. If Fill of the CACHE instruction is executed, the contents of the parity error register are written to the parity bit of the instruction cache instead of the instruction parity.

4.4.6 Inhibiting parity error

When the DE bit of the status register is set, the processor does not generate the cache parity error exception.

4.4.7 Enabling interrupts (IE)

When the IE bit of the status register is cleared, all the interrupts, except reset and non-maskable interrupt, are disabled.

5. BCU (BUS CONTROL UNIT)

5.1 General

The BCU transfers data with the VR4100 CPU core via SysAD bus (internal) inside the VR4101. It also controls an external LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller via system bus, and transfers data with these devices via ADD bus and DATA bus.

The BCU basically operates with internal bus clock TClock.

Table 5-1. BCU Registers

Symbol	Function
BCUCNTREG	BCU control register
BCUBRREG	BCU bus operation interval specification register
BCUBRCNTREG	BCU bus operation interval count register
BCUBCLREG	BCU bus operation interval enable register
BCUBCLCNTREG	BCU bus operation interval enable count register
BCUSPEEDREG	BCU access cycle change register
BCUERRSTREG	BCU bus error status register
BCURFCNTREG	BCU refresh cycle count register
PREVIDREG	Peripheral unit revision ID register

6. DMAAU (DMA ADDRESS UNIT)

6.1 General

The DMAAU controls the addresses for the DMA operations of PIU, SIU (transmission/reception), AIU, and KIU.

The DMA start physical address of each peripheral unit can be specified in a range of 0x0000 0000 to 0x001 FFFE as a half-word address. The DMA space of each peripheral unit is a 2K-block including the DMA start address, and is aligned at a 2K-byte boundary. The DMA operation is not guaranteed if the DMA space overlaps with that of other peripheral unit.

Table 6-1. DMAAU Registers

Symbol	Function
PADDMAADRLREG	DMA channel low-order address register for touch panel
PADDMAADRHREG	DMA channel high-order address register for touch panel
SRXDMAADRLREG	DMA channel low-order address register for SIU reception
SRXDMAADRHREG	DMA channel high-order address register for SIU reception
STXDMAADRLREG	DMA channel low-order address register for SIU transmission
STXDMAADRHREG	DMA channel high-order address register for SIU transmission
AUDDMAADRLREG	DMA channel low-order address register for audio output
AUDDMAADRHREG	DMA channel high-order address register for audio output
KEYDMAADRLREG	DMA channel low-order address register for keyboard input
KEYDMAADRHREG	DMA channel high-order address register for keyboard input

7. DCU (DMA CONTROL UNIT)

7.1 General

The DCU controls the DMA operation. It controls the DMA requests from the peripheral units (SIU, KIU, PIU, and AIU) and the acknowledge signal from the BCU that performs bus arbitration, and enables or disables the DMA operation.

The priorities of the DMA requests from the respective peripheral units are as follows:

AIU > SIU reception > SIU transmission > PIU > KIU

Table 7-1. DCU Registers

Symbol	Function
DMARSTREG	DMA reset register
DMAIDLEREG	DMA status register
DMASENREG	DMA enable register
DMAMSKREG	DMA mask register
DMAREQREG	DMA request register

8. CMU (CLOCK MASK UNIT)

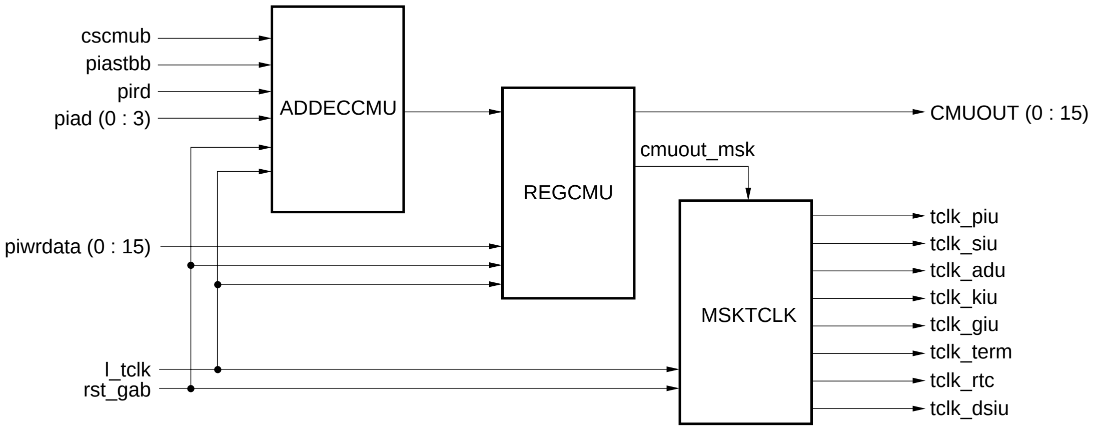
8.1 General

The CMU is used to specify whether the CPU core supplies the clock to each peripheral unit. By supplying the clock only to the necessary peripheral units, the power consumption can be reduced.

Table 8-1. CMU Register

Symbol	Function
CMUCLKMSKREG	CMU clock mask register

8.2 Configuration



9. ICU (INTERRUPT CONTROL UNIT)

9.1 General

The ICU receives an interrupt request signal from each peripheral unit and generates an interrupt request signal (Int0, Int1, or NMI) to the CPU core.

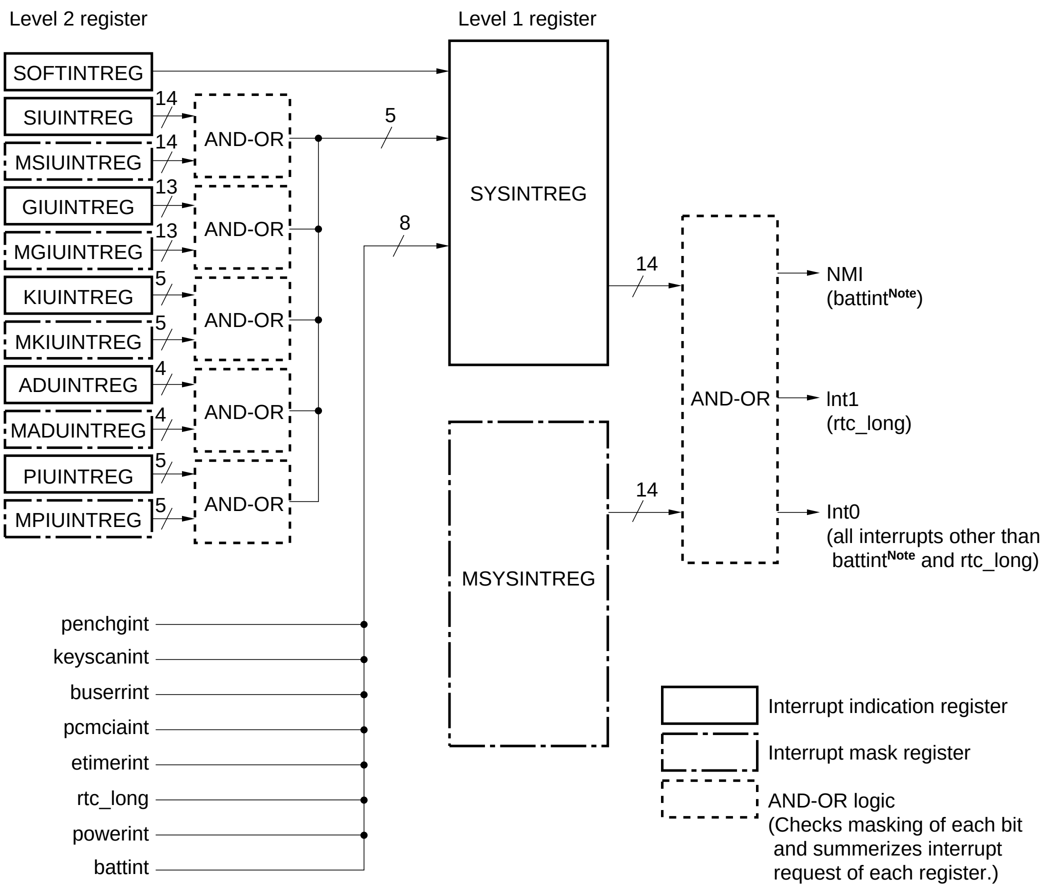
Table 9-1. ICU Registers

Symbol	Function
SYSINTREG	System interrupt register
PIUINTREG	PIU interrupt register
ADUINTREG	AIU interrupt register
KIUINTREG	KIU interrupt register
GIUINTREG	GIU interrupt register
SIUINTREG	SIU interrupt register
MSYSINTREG	System interrupt mask register
MPIUINTREG	PIU interrupt mask register
MADUINTREG	AIU interrupt mask register
MKIUINTREG	KIU interrupt mask register
MGIUINTREG	GIU interrupt mask register
MSIUINTREG	SIU interrupt mask register
NMIREG	Battery interrupt select register
SOFTINTREG	Software interrupt register

Table 9-2. Correspondence of Interrupts of ICU and CPU Core

SYSINTREG Bit Position	Interrupt Source	Interrupt Request Signal
13	PIU (in Suspend mode)	Int0
12	KIU (in Suspend mode)	
11	Software (by SOFTINTREG)	
10	Bus error	
9	SIU	
6	AIU	
8	GIU	
7	KIU	
5	PIU	
4	PCMCIA	
3	Elapsed Time timer	
2	RTClong timer	Int1
1	Power-ON switch	Int0
0	Battery	NMI/Int0 (selected by NMIREG)

9.2 Configuration



Note battint can specify whether NMI or Int0 is used by NMIREG.

10. PMU (POWER MANAGEMENT UNIT)

10.1 General

PMU manages and controls power to the internal and external circuits of the VR4101 as follows:

- Controls shutdown
- Controls reset
- Manages and controls power-ON sequence
- Manages and controls sequence in power mode

Table 10-1. PMU Registers

Symbol	Function
PMUINTREG	PMU interrupt/status register
PMUCNTREG	PMU control register

10.1.1 Power mode

The VR4101 supports the following four power modes:

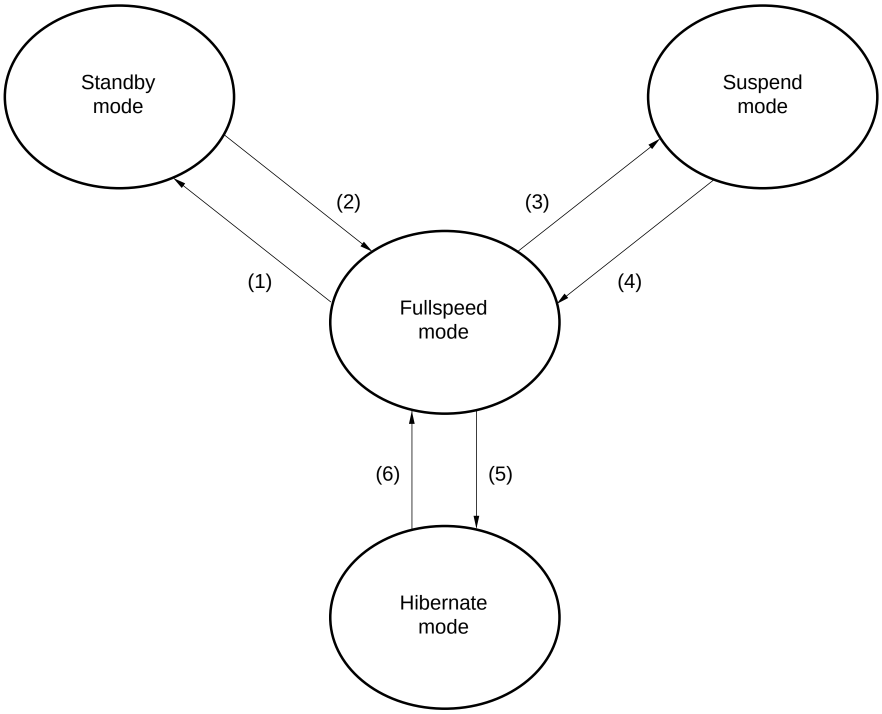
- Fullspeed mode
- Standby mode
- Suspend mode
- Hibernate mode

Figure 10-1 illustrates the transition of the power modes.

To change the mode from Fullspeed to Standby, Suspend, or Hibernate, execute the STANDBY, SUSPEND, or HIBERNATE instruction. To change the mode from Standby, Suspend, or Hibernate to Fullspeed, either generate an interrupt, or execute a reset operation.

Table 10-2 outlines each power mode.

Figure 10-1. Power Mode Transition



(1)	(2)	(3)	(4)	(5)	(6)
STANDBY instruction, pipeline flash, SysAD idle, PClock high level	All interrupts	SUSPEND instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, DRAM self refresh start	BatteryInt POWERSW RTCRST Alarm KeyTouch PenTouch BatteryLock CardLock DCD	HIBERNATE instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, MasterOut high level, DRAM self refresh start	POWERSW Alarm DCD

Table 10-2. Outline of Power Mode

Mode	Internal Peripheral Unit				Power Consumption[Note 1]
	RTC	ICU	DCU	Others	(33 MHz, 3.3 V TYP.)
Fullspeed	On	On	On	Selectable[Note 2]	200 mW
Standby	On	On	On	Selectable[Note 2]	100 mW
Suspend	On	On	Off	Off	13 mW
Hibernate	On	Off	Off	Off	165 μW
Off	Off	Off	Off	Off	0 W

Notes 1. Targeted value

2. Refer to **8. CMU (CLOCK MASK UNIT)**.

11. RTC (REAL-TIME CLOCK UNIT)

11.1 General

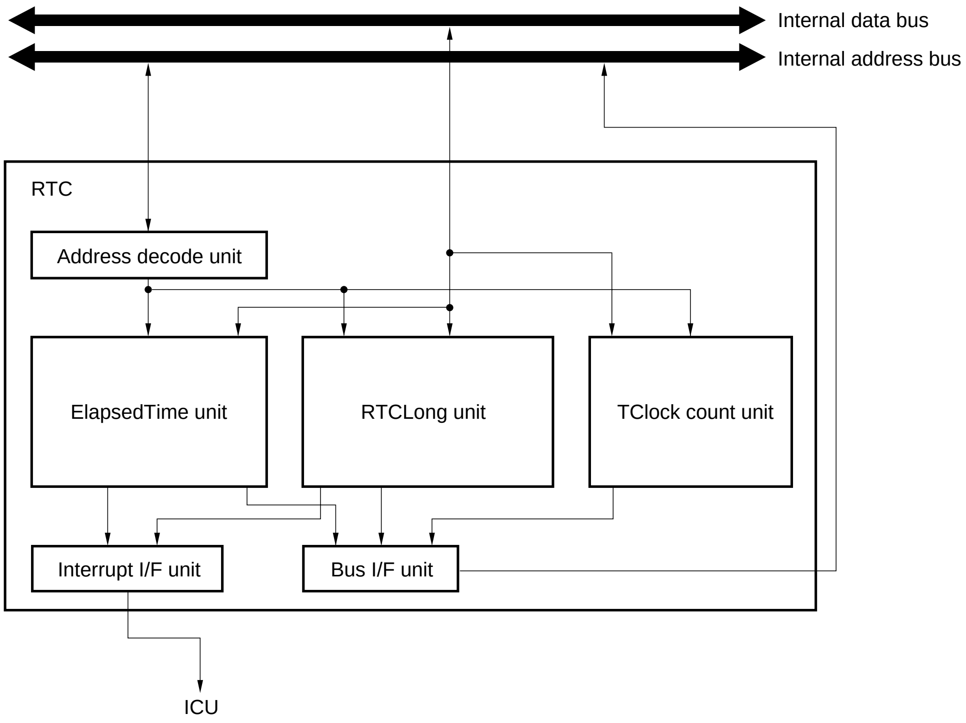
The RTC consists of the following three types of timers.

- RTCLong timer
  This is a 24-bit programmable down counter that counts down at a cycle of 32.768 kHz. It can generate an interrupt request at intervals of up to 512 seconds.
- ElapsedTime timer
  This is a 48-bit up counter that counts up at a cycle of 32.768 kHz. When this counter counts up to about 272 years, it returns to 0. This counter consists of an 48-bit ElapsedTime counter and a 48-bit alarm time register. By comparing these, an interrupt request can be generated at specific time.
- TClock count timer
  This is a 32-bit free-running counter that counts up at a cycle of TClock, and can be used for performance evaluation.

Table 11-1. RTC Registers

Symbol	Function
ETIMELREG	ElapsedTime timer register, low
ETIMEMREG	ElapsedTime timer register, middle
ETIMEHREG	ElapsedTime timer register, high
ECMPHREG	ElapsedTime timer compare register, high
ECMPLREG	ElapsedTime timer compare register, low
ECMPMREG	ElapsedTime timer compare register, middle
RTCLLREG	RTCLong timer register, low
RTCLHREG	RTCLong timer register, high
RTCLCNTLREG	RTCLong timer count register, low
RTCLCNTHREG	RTCLong timer count register, high
TCLKCNTLREG	TCLK count register, low
TCLKCNTHREG	TCLK count register, high
RTCINTREG	RTC interrupt register

11.2 Configuration



12. DSU (Deadman's SW Unit)

12.1 General

The DSU automatically detects a hang-up of the VR4101 and resets the VR4101. By stopping a hang-up at the earliest stage by using the DSU, the destruction of data can be minimized.

The DSU can set for a cycle of up to 15 seconds in units of 1 second. Set the DSWCLR bit of the DSUCLRREG register to 1 within this time in software. If the bit is not set within the time, the CPU is reset (refer to **4. INITIALIZATION INTERFACE**).

Table 12-1. DSU Registers

Symbol	Function
DSUCNTREG	DSU control register
DSUSETREG	Deadman's Switch enable register
DSUCLRREG	Deadman's Switch clear register
DSUTIMREG	Deadman's Switch elapsed time register

13. GIU (GENERAL-PURPOSE I/O UNIT)

13.1 General

The GIU controls the GPIO (0:11) pins and DCD pin. The GPIO (0:11) pins constitute a general-purpose I/O port, but one of the GPIO pins is reserved for a specific application. The other 11 pins and DCD pins can be assigned interrupt requests. As a trigger, the edge of the input level, low level, or high level can be selected.

Table 13-1. GIU Registers

Symbol	Function
GOUTENREG	General-purpose port I/O setting register
GPOTDATREG	General-purpose port data register
GINTSTREG	General-purpose port interrupt register
GINTENREG	General-purpose port interrupt enable register
GCINTSREG	General-purpose port interrupt trigger setting register
GLINTSREG	General-purpose port interrupt level setting register

Table 13-2. Outline of DCD and General-Purpose I/O Pins

Pin	Input Buffer Type	Interrupt Detection Clock (internal)
DCD**Note 1**	—	MasterOut
GPIO11	I/O (Schmitt)	TClock
GPIO10	I/O (Schmitt)	MasterOut
GPIO9**Note 2**	I/O (Schmitt)	MasterOut
GPIO8	I/O	TClock
GPIO7	I/O	TClock
GPIO6	I/O	TClock
GPIO5	I/O	TClock
GPIO4	I/O	TClock
GPIO3	I/O	TClock
GPIO2	I/O	TClock
GPIO1	I/O	TClock
GPIO0	I/O	TClock

Notes 1. The DCD pin (input) is internally connected to bit 13 of the GPIO register. This pin is used only as an input pin with GIU.

2. Fix the GPIO9 pin to a battery lid lock detection signal (BATTLOCK).

Remark All the pins are set in the input mode at reset.

14. PIU (TOUCH PANEL INTERFACE UNIT)

14.1 General

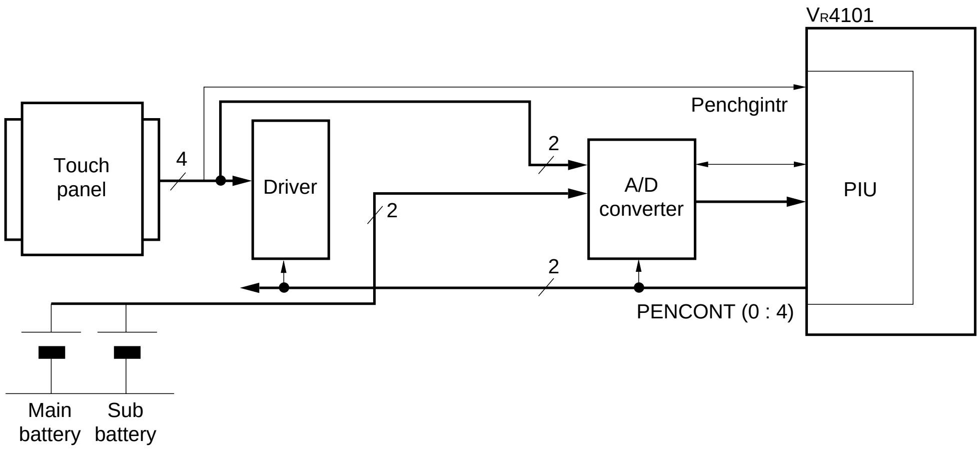
The PIU detects the X and Y coordinates on a panel touched by the pin by using an external A/D converter. It also measures battery voltage.

As the external A/D converter, the TLV1543 (conversion accuracy: 10 bits) and TLC2543C (conversion accuracy: 12 bits) are supported.

Table 14-1. PIU Registers

Symbol	Function
PIUDATAREG	Touch panel data register
PIUCNTREG	PIU control register
PIUINTREG	PIU interrupt register
PIUSIVLREG	Keyboard scan sampling cycle setting register
PIUSTBLREG	A/D converter control register
PIUCMDREG	A/D converter command register
PIUCIVLREG	PIU count register

14.2 Example of External Circuit Configuration



15. SIU (SERIAL INTERFACE UNIT)

15.1 General

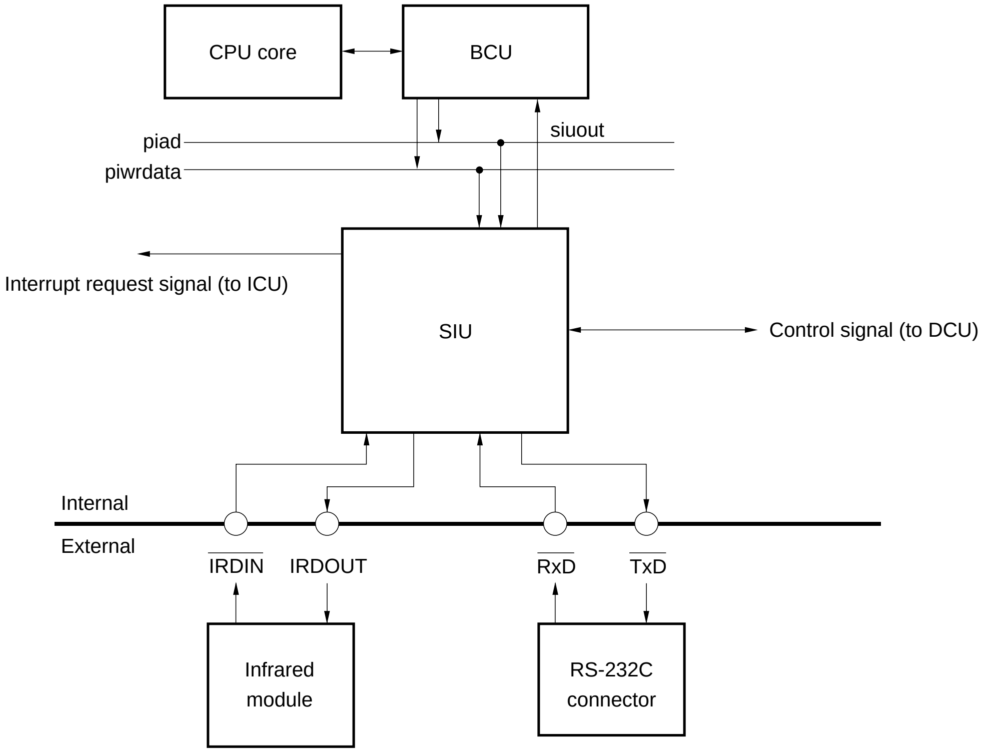
The SIU supports RS-232C communication and IrAD communication and has one channel each for each communication mode. However, RS-232C communication and IrAD communication are mutually exclusive.

This SIU also supports detection of framing errors and detection/transmission of a break, and can also support UART. The parity bit of the transmit/receive data is not automatically processed, but treated as data.

Table 15-1. SIU Registers

Symbol	Function
SIURXDATREG	SIU receive data register
SIUTXDATREG	SIU transmit data register
SIUCNTREG	SIU control register
SIUDLENGTHREG	Serial data length register
SIUINTREG	SIU interrupt register
SIURS232CREG	RS-232C control register
SIUBAUDSELREG	Baud rate setting register

15.2 Configuration



16. AIU (AUDIO INTERFACE UNIT)

16.1 General

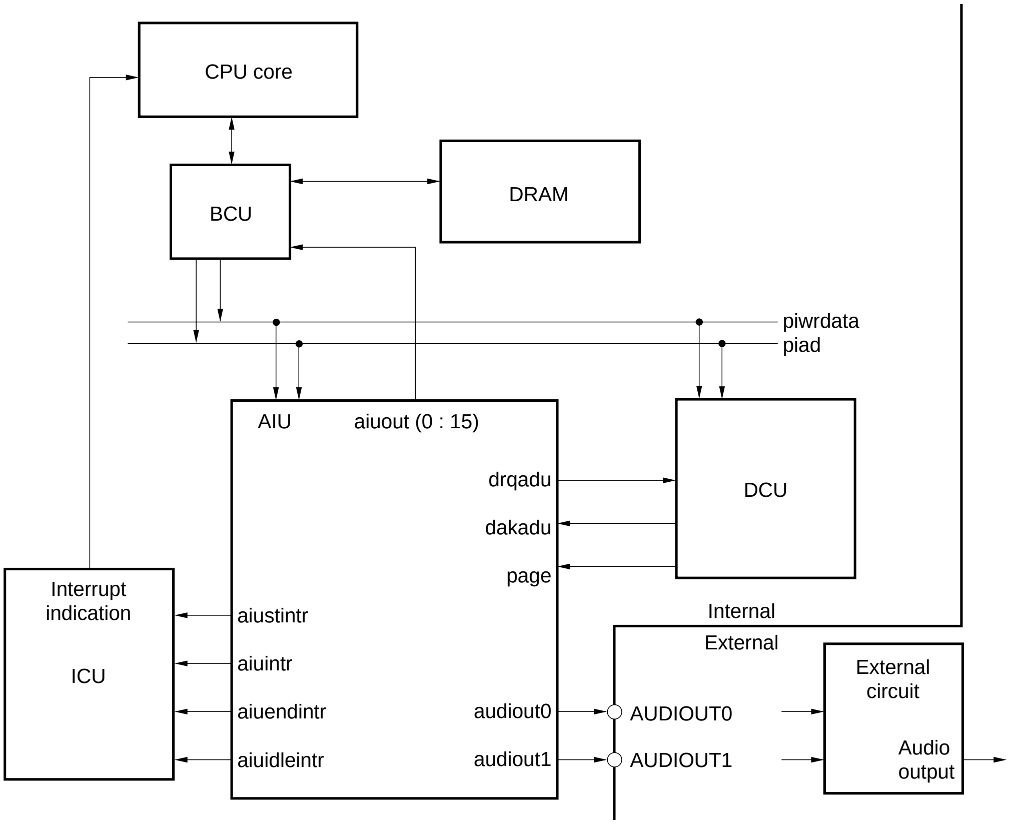
The AIU generates audio signals. It has two preset counters and offers the following two modes:

- Buzz mode
  A signal with a frequency of M and a duty factor of 50% is output for only the duration of N.
- PWM mode
  A high level is output from the output pin for only the duration of M and a low level is output for only the duration of N. By supply data combining M and N at high speeds, PWM of any oversampling is reproduced.

Table 16-1. AIU Registers

Symbol	Function
AIUDATREG	AIU data register
AIURESETREG	AIU reset register
AIUMODEREG	AIU mode register
AIUSEQENREG	AIU sequencer enable register
AIUMUTEREG	AIU output enable register
AIUSTATREG	AIU status register
AIUSTPPAGEREG	Page boundary interrupt enable register
AIUVALIDREG	AIU counter status register
AIUINTREG	AIU interrupt register
AIUCOUNT0REG	AIU counter 0
AIUCOUNT1REG	AIU counter 1
AIUREPNUMREG	Number of PWM repeats setting register
AIUBUSENREG	DMA enable register

16.2 Configuration



Remark The AUDIOUT0 and AUDIOUT1 pins output the same data. Either of these pins can be masked by using the AIUMUTEREG register. The volume of the actual audio output can be controlled by using this register and the external circuit.

17. KIU (KEYBOARD INTERFACE UNIT)

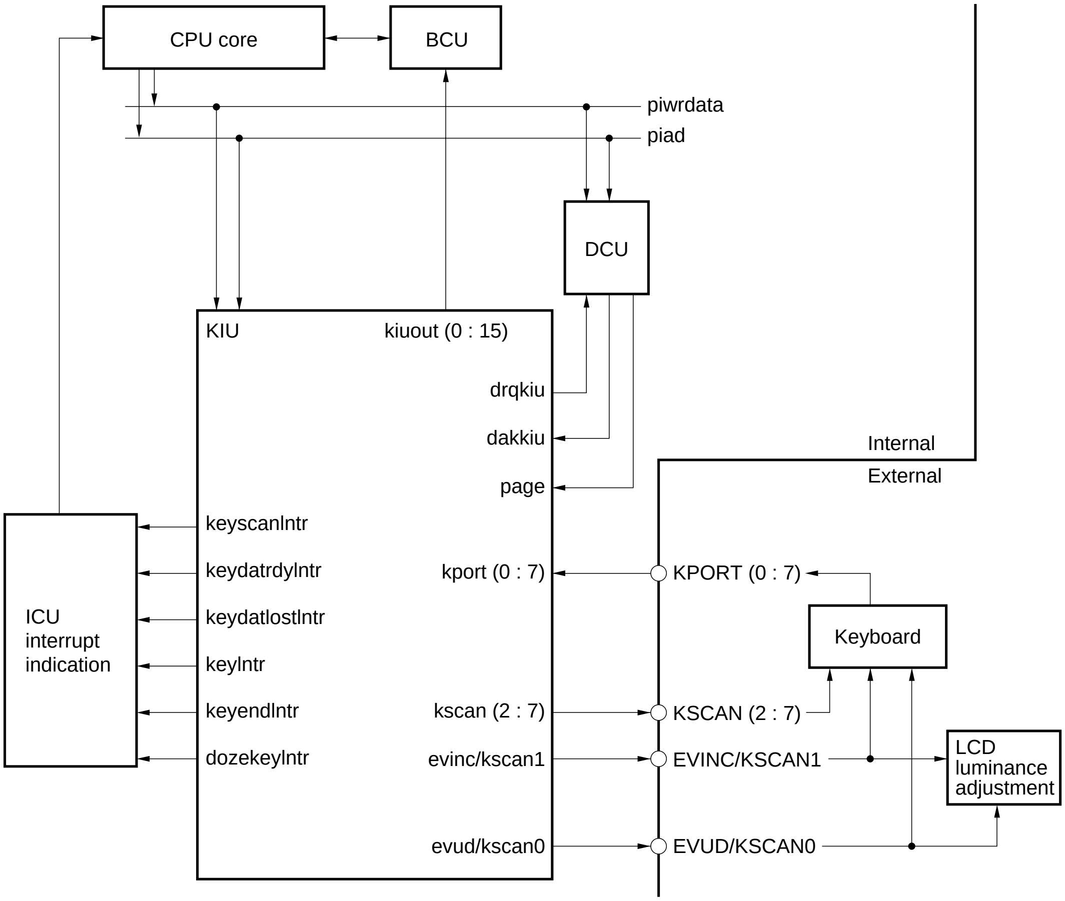
17.1 General

The KIU has eight scan lines and eight detection lines and can detect data input from 64 keys. It can also detect rollover of two or three keys.

Table 17-1. KIU Registers

Symbol	Function
KIUDATREG	Key scan data register
KIUASCANREG	Key auto scan setting register
KIUASTOPREG	Key scan automatic stop register
KIUSCANREG	Key scan start register
KIUSTOPREG	Key scan stop register
KIUSAPREG	Page boundary interrupt enable register
KIUSCANSREG	KIU sequencer enable register
KIUWKSREG	KIU wait time setting register
KIUWKIREG	Key scan interval setting register
KIUSRNREG	KIU sequencer stop setting register
KIUINTREG	KIU interrupt register
KIURSTREG	KIU reset register
KIUENREG	Key scan enable register
DOZEKEYINTREG	Key input detect register
EVVOLREG	Electronic volume control register

17.2 Configuration



18. DebugSIU (DEBUG SERIAL INTERFACE UNIT)

18.1 General

The DebugSIU is a dedicated serial interface unit that is used during debugging. It supports a data transfer rate of up to 115 kbps.

Table 18-1. DebugSIU Registers

Symbol	Function
ASIM00REG	DebugSIU setting register
ASIM01REG	Extended bit enable register
RXB0RREG	DebugSIU reception extended data register
RXB0LREG	DebugSIU receive data register
TXS0RREG	DebugSIU transfer extended data register
TXS0LREG	DebugSIU transfer data register
ASIS0REG	DebugSIU communication status register
INTR0REG	DebugSIU interrupt register
BPRM0REG	Baud rate setting register
DSIURESETREG	DebugSIU reset register

19. INSTRUCTION SET

Each instruction of the VR4101 consists of 1 word (32 bits) located at a word boundary. Three instruction formats are available as shown in Figure 19-1. By employing the three simplified instruction formats, the decoding of instructions is simplified. Complicated operations and addressing modes that are not frequently used are realized by the compiler.

19.1 Instruction Formats

The instruction formats of the VR4101 are shown below.

Figure 19-1. CPU Instruction Format

I-type (immediate format)

31 26	25 21	20 16	15 0
op	rs	rt	immediate

J-type (jump format)

31 26	25 0
op	target

R-type (register format)

31 26	25 21	20 16	15 11	10 6	5 0
op	rs	rt	rd	sa	funct

op	6-bit instruction code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register, or conditional branch
immediate	16-bit immediate value, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register specifier
sa	5-bit shift
funct	6-bit function field

19.2 CPU Instruction Set List

All the CPU instructions of the VR4101 are classified into three sets: instruction set common to all the VR series processors (ISA: Instruction Set Architecture), instruction set executed by the VR4000 series (extended ISA), and system control coprocessor instruction set. Each instruction set is listed below.

Table 19-1. CPU Instruction Set: ISA (1/2)

Instruction	Description	Format	
Load/store instruction	op / base / rt / offset		
LB	Load Byte	LB	rt, offset (base)
LBU	Load Byte Unsigned	LBU	rt, offset (base)
LH	Load Halfword	LH	rt, offset (base)
LHU	Load Halfword Unsigned	LHU	rt, offset (base)
LW	Load Word	LW	rt, offset (base)
LWL	Load Word Left	LWL	rt, offset (base)
LWR	Load Word Right	LWR	rt, offset (base)
SB	Store Byte	SB	rt, offset (base)
SH	Store Halfword	SH	rt, offset (base)
SW	Store Word	SW	rt, offset (base)
SWL	Store Word Left	SWL	rt, offset (base)
SWR	Store Word Right	SWR	rt, offset (base)
AIU immediate instruction	op / rs / rt / offset		
ADDI	Add Immediate	ADDI	rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU	rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI	rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU	rt, rs, immediate
ANDI	And Immediate	ANDI	rt, rs, immediate
ORI	Or Immediate	ORI	rt, rs, immediate
XORI	Exclusive Or Immediate	XORI	rt, rs, immediate
LUI	Load Upper Immediate	LUI	rt, immediate
3-operand type instruction	op / rs / rt / rd / sa / funct		
ADD	Add	ADD	rd, rs, rt
ADDU	Add Unsigned	ADDU	rd, rs, rt
SUB	Subtract	SUB	rd, rs, rt
SUBU	Subtract Unsigned	SUBU	rd, rs, rt
SLT	Set On Less Than	SLT	rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU	rd, rs, rt
AND	And	AND	rd, rs, rt
OR	Or	OR	rd, rs, rt
XOR	Exclusive Or	XOR	rd, rs, rt
NOR	Nor	NOR	rd, rs, rt
Shift instruction	op / rs / rt / rd / sa / funct		
SLL	Shift Left Logical	SLL	rd, rt, sa
SRL	Shift Right Logical	SRL	rd, rt, sa
SRA	Shift Right Arithmetic	SRA	rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV	rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV	rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV	rd, rt, rs

Table 19-1. CPU Instruction Set: ISA (2/2)

Instruction	Description	Format
Multiplication/division instruction	op rs rt rd sa funct	
MULT	Multiply	MULT rs, rt
MULTU	Multiply Unsigned	MULTU rs, rt
DIV	Divide	DIV rs, rt
DIVU	Divide Unsigned	DIVU rs, rt
MFHI	Move From HI	MFHI rd
MFLO	Move From LO	MFLO rd
MTHI	Move To HI	MTHI rs
MTLO	Move To LO	MTLO rs
Jump instruction (1)	op target	
J	Jump	J target
JAL	Jump And Link	JAL target
Jump instruction (2)	op rs rt rd sa funct	
JR	Jump Register	JR rs
JALR	Jump And Link Register	JALR rs, rd
Branch instruction (1)	op rs rt offset	
BEQ	Branch On Equal	BEQ rs, rt, offset
BNE	Branch On Not Equal	BNE rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ rs, offset
Branch instruction (2)	REGIMM rs sub offset	
BLTZ	Branch On Less Than Zero	BLTZ rs, offset
BGEZ	Branch On Greater Than Or Equal to Zero	BGEZ rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL rs, offset
Special instruction	SPECIAL rs rt rd sa funct	
SYNC	Synchronize	SYNC
SYSCALL	System Call	SYSCALL
BREAK	Breakpoint	BREAK
Coprocessor instruction (1)	op base rt offset	
LWCz	Load Word To Coprocessor z	LWCz rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz rt, offset (base)
Coprocessor instruction (2)	COPz sub rt rd 0	
MTCz	Move To Coprocessor z	MTCz rt, rd
MFCz	Move From Coprocessor z	MFCz rt, rd
CTCz	Move Control To Coprocessor z	CTCz rt, rd
CFCz	Move Control From Coprocessor z	CFCz rt, rd
Coprocessor instruction (3)	COPz CO cofun	
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instruction (4)	COPz BC br offset	
BCzT	Branch On Coprocessor z True	BCzT offset
BCzF	Branch On Coprocessor z False	BCzF offset

Table 19-2. CPU Instruction Set: Extended ISA (1/2)

Instruction	Description	Format
Load/store instruction	op base rt offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
AIU immediate instruction	op rs rt immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op rs rt rd sa funct	
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op rs rt rd sa funct	
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shift Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, rs
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, rs
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, rs
DSLL32	Doubleword Shift Left Logical+32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logical+32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic+32	DSRA32 rd, rt, sa
Multiplication/division instruction (1)	op rs rt rd sa funct	
DMULT	Doubleword Multiply	DMULT rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU rs, rt
DDIV	Doubleword Divide	DDIV rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU rs, rt
Multiplication/division instruction (2)	op rs rt rd sa funct	
MADD16	Multiply and Add 16-bit Integer	MADD16 rs, rt
DMADD16	Doubleword Multiply and Add 16-bit Integer	DMADD16 rs, rt
Branch instruction (1)	op rs rt offset	
BEQL	Branch On Equal Likely	BEQL rs, rt, offset
BNEL	Branch On Not Equal Likely	BNEL rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely	BLEZL rs, offset
BGTZL	Branch On Greatrer Than Zero Likely	BGTZL rs, offset

Table 19-2. CPU Instruction Set: Extended ISA (2/2)

Instruction	Description	Format
Branch instruction (2)	REGIMM rs sub offset	
BLTZL	Branch On Less Than Zero Likely	BLTZL rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely	BGEZL rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely	BLTZALL rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely	BGEZALL rs, offset
Exception instruction	SPECIAL rs rt rd sa funct	
TGE	Trap If Greater Than Or Equal	TGE rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned	TGEU rs, rt
TLT	Trap If Less Than	TLT rs, rt
TLTU	Trap If Less Than Unsigned	TLTU rs, rt
TEQ	Trap If Equal	TEQ rs, rt
TNE	Trap If Not Equal	TNE rs, rt
Exception immediate instruction	REGIMM rs sub immediate	
TGEI	Trap If Greater Than Or Equal Immediate	TGEI rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned	TGEIU rs, immediate
TLTI	Trap If Less Than Immediate	TLTI rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned	TLTIU rs, immediate
TEQI	Trap If Equal Immediate	TEQI rs, immediate
TNEI	Trap If Not Equal Immediate	TNEI rs, immediate

Table 19-3. System Control Coprocessor (CP0) Instruction Set

Instruction	Description	Format
System control coprocessor instruction (1)	COP0 sub rt rd 0	
MFC0	Move From Coprocessor 0	MFC0 rt, rd
MTC0	Move To Coprocessor 0	MTC0 rt, rd
DMFC0	Doubleword Move From Coprocessor 0	DMFC0 rt, rd
DMTC0	Doubleword Move To Coprocessor 0	DMTC0 rt, rd
System control coprocessor instruction (2)	COP0 CO funct	
TLBR	Read Indexed TLB Entry	TLBR
TLBWI	Write Indexed TLB Entry	TLBWI
TLBWR	Write Random TLB Entry	TLBWR
TLBP	Probe TLB For Matching Entry	TLBP
ERET	Exception Return	ERET
System control coprocessor instruction (3)	COP0 CO funct	
STANDBY	Standby	STANDBY
SUSPEND	Suspend	SUSPEND
HIBERNATE	Hibernate	HIBERNATE
System control coprocessor instruction (4)	CACHE base sub offset	
CACHE	Cache Operation	CACHE sub, offset (base)

19.3 Instruction Execution Time

In principle, the VR4101 executes one instruction in one cycle, but some instructions take two cycles or more.

(1) The data loaded by a load instruction cannot be used in the delay slot. If an instruction that uses load data is placed in the delay slot, the pipeline stalls.
A store instruction stalls by the delay slot if it is followed by a load instruction or MFC0.
If a branch instruction whose condition is satisfied or a jump instruction is executed, the instruction at the destination address is executed after the delay slot.

Table 19-4. Number of Delay Slot Cycles

Instruction Category	Necessary Number of Cycles (PCycle)
Load	1
Store	1
Jump	1
Branch	1

(2) The number of cycles indicated in the table below is necessary for executing an integer multiplication/division or sum-of-products operation instruction.
These instructions can be executed in parallel with other instructions, except those that access the HI/LO registers that store the result of an operation, and multiplication/division or sum-of-products operation instruction.

Table 19-5. Number of Execution Cycles of Integer Multiplication/Division Instructions

Instruction Category	Necessary Number of Cycles (PCycle)
MULT	1
MULTU	1
DIV	35
DIVU	35
DMULT	4
DMULTU	4
DDIV	67
DDIVU	67
MADD16	1
DMADD16	1

20. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage	V_I	V_{DD} 3.7 V	–0.5 to +4.0	V
		V_{DD} 3.7 V, pulse less than 10 ns	–1.5 to +4.0	V
		V_{DD} < 3.7 V	–0.5 to V_{DD} + 0.3	V
		V_{DD} < 3.7 V, pulse less than 10 ns	–1.5 to V_{DD} + 0.3	V
Operating temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

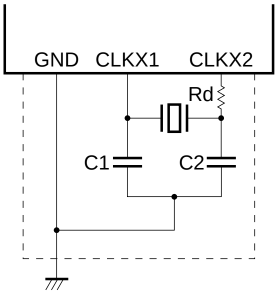
The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHZ Pins other than test pin: 0 V		10	pF
I/O capacitance	C_{IO}			10	pF

Recommended Oscillation Circuit

★ **(a) Crystal resonator connection (T_A = –10 to +70 °C, V_{DD} = 2.5 to 3.6 V)**

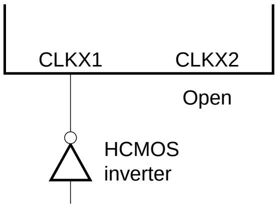


Manufacturer	Product Name	Frequency (kHz)	Recommended Circuit Constant		
			C1 (pF)	C2 (pF)	Rd (kΩ)
Seiko Instruments Inc.	SP-T2A	32.768	20	20	220

Caution When using a system clock oscillation circuit, perform the wiring of the portion enclosed by the dotted line in the above figure to avoid adverse influence due to wiring capacitance, etc.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines. Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Make sure that the ground point of the capacitor of the oscillation circuit is at the same potential as GND. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

(b) External clock input



Caution Do not connect a load such as wiring capacitance to the CLKX2 pin.

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = –2 mA	0.8 V_{DD}			V
		I_{OH} = –20 μA	V_{DD} – 0.1			
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 μA			0.1	
High-level input voltage Note 1	V_{IH1}		2.0		V_{DD} + 0.3	V
Low-level input voltage Note 1	V_{IL1}		–0.3		0.3 V_{DD}	V
		Pulse less than 10 ns	–1.5		0.3 V_{DD}	V
High-level input voltage Note 2	V_{IH2}		0.75 V_{DD}		V_{DD} + 0.3	V
Low-level input voltage Note 2	V_{IL2}		–0.3		0.6	V
		Pulse less than 10 ns	–1.5		0.6	V
Hysteresis voltage Note 3	V_H			0.17 V_{DD}		V
Supply current Note 4	I_{DD}	ADD (0:20) = 120 pF, Other pins = 40 pF, In Fullspeed mode		60	115	mA
		External load: 0 pF, in Standby mode		30	50	
		External load: 0 pF, in Suspend mode		4	7	
		External load: 0 pF, in Hibernate mode		50	100	μA
Input leakage current Note 4	I_{LI}	V_{DD} = 3.6 V, V_I = V_{DD}, 0 V			±5	μA
High-level input leakage current Note 5	I_{LIH}	V_{DD} = 3.6 V, V_I = V_{DD}			36	μA
Output leakage current	I_{LO}	V_{DD} = 3.6 V, V_I = V_{DD}, 0 V			±5	μA

Notes

1. Except CLKX1, POWER, $\overline{\text{RSTSW}}$, $\overline{\text{RTCRST}}$, BATTINH, $\overline{\text{BATTINT}}$, and GPIO (9:10) pins

2. Applied to POWER, $\overline{\text{RSTSW}}$, $\overline{\text{RTCRST}}$, BATTINH, $\overline{\text{BATTINT}}$, and GPIO (9:10) pins

3. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low

4. Except KPORT (0:7) (input pins with pull-down resistor)

5. Applied to KPORT (0:7) (input pins with pull-down resistor)

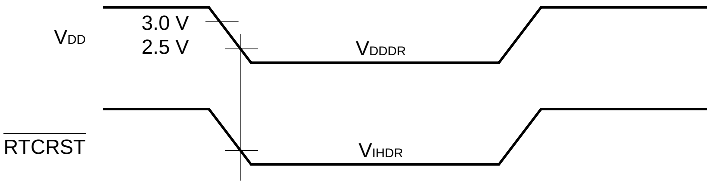
Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data retention voltage[Note 1]	V_{DDDR}	Hibernate mode	Under evaluation (2.5)	3.6	V
Data retention high-level input voltage[Note 2]	V_{IHDR}		Under evaluation (0.9 V_{DDDR})		V

Notes 1. The data retention voltage guarantees retention of the data read from the following registers for the RTC operation, and the data of the compare register (the data in the CPU core cannot be guaranteed). ETIMELREG, ETIMEMREG, ETIMEHREG, ECOMPLREG, ECOMPMREG, ECOMPHREG, RTCLLREG, RTCLHREG, RTCLCNTLREG, RTCLCNTHREG

2. Applied to $\overline{\text{RTCRST}}$ pin

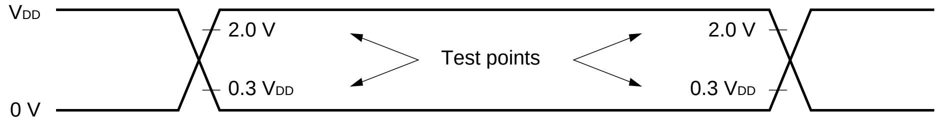
Remark The values in ( ) are the targeted values.



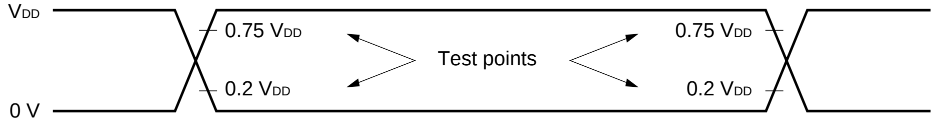
AC Characteristics (T_A = –10 to +70 °C, V_{DD} = 3.0 to 3.6 V)

AC test input waveform

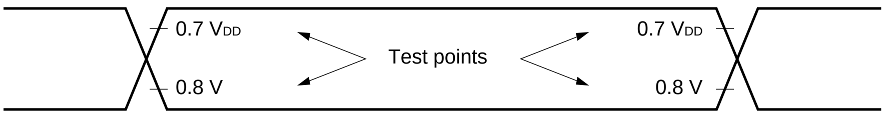
(a) ADEOC, ADIN, $\overline{\text{CTS}}$, DATA (0:15), DCD, DDIN, $\overline{\text{DSR}}$, GPIO (0:8), GPIO11, $\overline{\text{IRDIN}}$, IRQ, KPORT (0:7), LCDRDY, $\overline{\text{PENCHGINT}}$, $\overline{\text{RxD}}$, $\overline{\text{ZWS}}$



(b) BATTINH, $\overline{\text{BATTINT}}$, GPIO (9:10), POWER, $\overline{\text{RSTSW}}$, $\overline{\text{RTCRST}}$

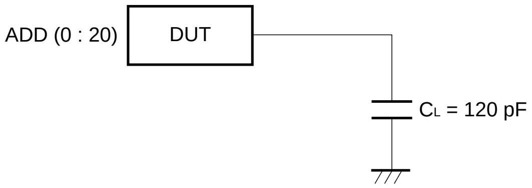


AC test output measuring points

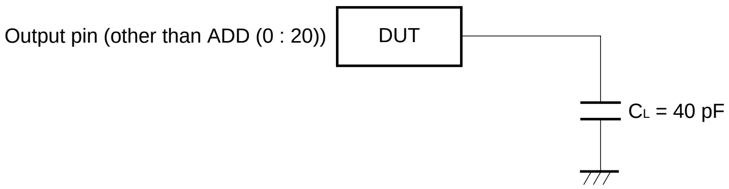


Load condition

(a) ADD (0:20)



(b) Other output pins

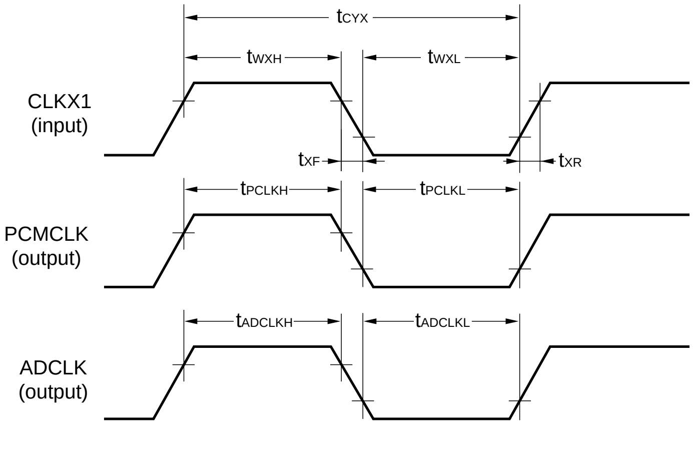


(1) Clock parameter

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLKX1 high-level width	t_{WXH}	With external clock input	15			μs
CLKX1 low-level width	t_{WXL}	With external clock input	15			μs
CLKX1 clock frequency		With external clock input	32	32.768	35	kHz
CLKX1 clock cycle	t_{CYX}	With external clock input	31.250	30.518	28.571	μs
CLKX1 clock rise time	t_{XR}	With external clock input			20	ns
CLKX1 clock fall time	t_{XF}	With external clock input			20	ns
PCMCLK high-level width	t_{PCLKH}		45			ns
PCMCLK low-level width	t_{PCLKL}		45			ns
PCMCLK frequency				8.290		MHz
ADCLK high-level width**Note 1**	t_{ADCLKH}		N – 40			ns
ADCLK low-level width**Note 1**	t_{ADCLKL}		N – 40			ns
ADCLK frequency**Note 2**				M		MHz

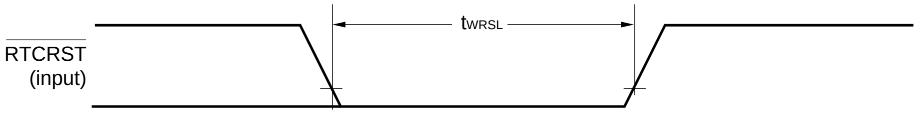
Notes 1. Calculate the value of N from the value of the SELADCLK (0:3) bits of the PIUSTBLREG register by using the following expression:
(SELADCLK × 4 + 2)/33.16

2. Calculate the value of M from the value of the SELADCLK (0:3) bits of the PIUSTBLREG register by using the following expression:
16.58/(SELADCLK × 4 + 2)



(2) Reset parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	Applied to $\overline{\text{RTCRST}}$ pin	305		μs



(3) System interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{INP1}	**Note 1**	91.5		μs
	t_{INP2}	**Note 2**	361.5		ns
	t_{INP3}	**Note 3**	180.6		ns
Output level width	t_{OUTP1}	**Note 4**	29		μs
	t_{OUTP2}	**Note 5**	30		ns
$\overline{\text{MRAS (0:3)}}$/$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ floating delay^{Note 6}	t_{RAMZ}			91.5	μs

Notes 1. Applied to POWER, $\overline{\text{RSTSW}}$, $\overline{\text{RTCRST}}$, BATTINH, $\overline{\text{BATTINT}}$, GPIO9, and DCD pins

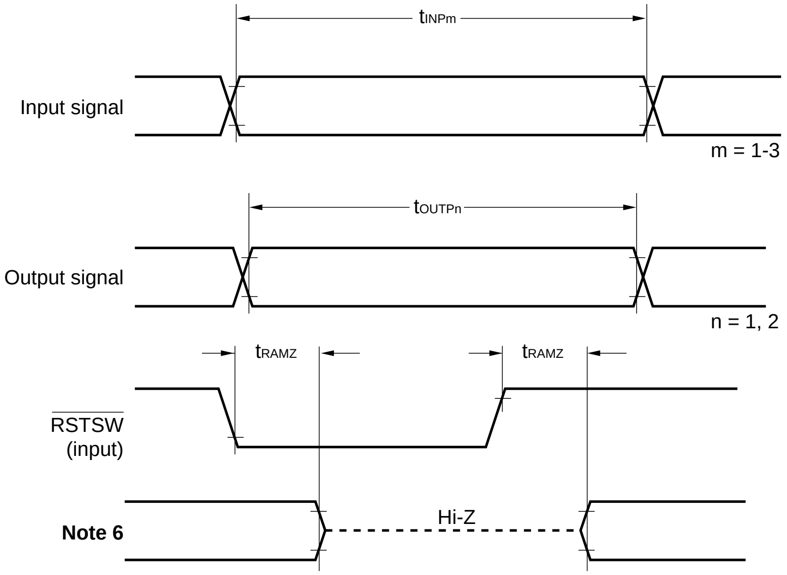
2. Applied to $\overline{\text{DSR}}$, IRQ, $\overline{\text{PENCHGINT}}$, $\overline{\text{CTS}}$, GPIO10, and KPORT (0:7) pins

3. Applied to GPIO11, GPIO (0:8), $\overline{\text{IRDIN}}$, DDIN, LCDRDY, $\overline{\text{ZWS}}$, ADIN, ADEOC, and $\overline{\text{RxD}}$ pins

4. Applied to MPOWER pin

5. Applied to $\overline{\text{ADCS}}$, ADCLK, ADSOUT, PENCNT (0:4), GPIO (0:11), RSTOUT, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, ADD (0:20), DATA (0:15), $\overline{\text{TxD}}$, IRDOUT, DDOUT, KSCAN (0:7), AUDIOUT (0:1), $\overline{\text{LCDCS}}$, $\overline{\text{LCDOE}}$, $\overline{\text{LCDWE}}$/$\overline{\text{ROMWE}}$, $\overline{\text{ROMCS (0:3)}}$, $\overline{\text{ROMOE}}$, PCMCLK, $\overline{\text{SHB}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, and $\overline{\text{MEMW}}$ pins

6. Applied to $\overline{\text{MRAS (0:3)}}$, $\overline{\text{UCAS}}$, and $\overline{\text{LCAS}}$ pins in respect to input of $\overline{\text{RSTSW}}$ pin



(4) EDO type DRAM read parameter (1/2)

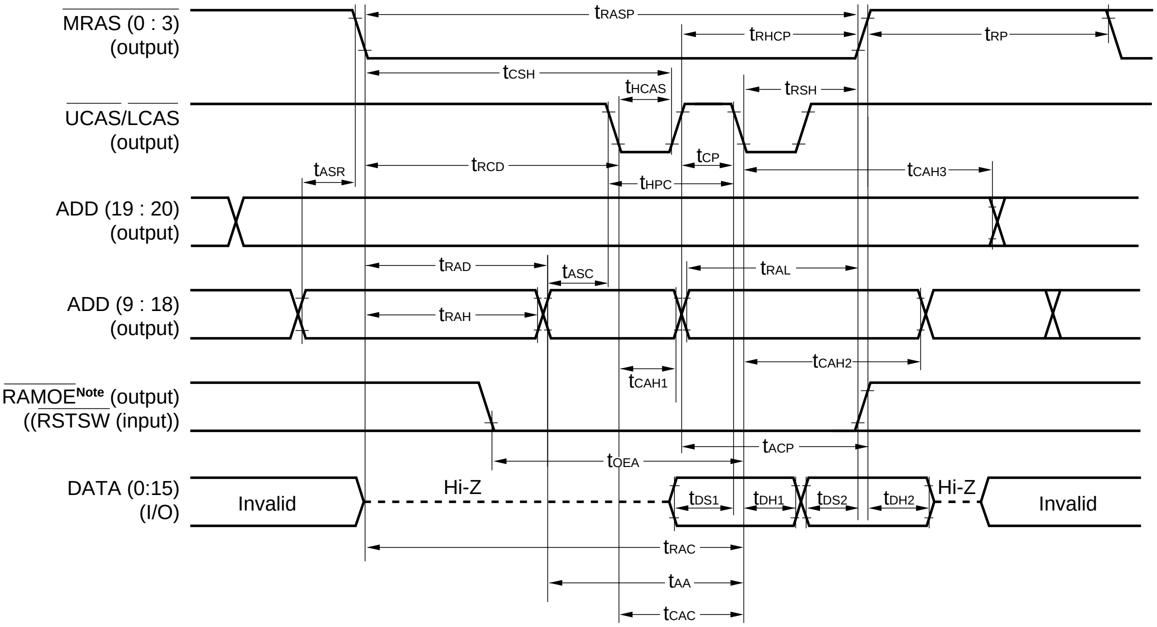
The target DRAM is the μPD42S16165L-A70 or μPD42S18165L-A70.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{MRAS}}$ (0:3) pulse width	t_{RASP}		70		ns
$\overline{\text{MRAS}}$ (0:3) hold time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ precharge)	t_{RHCP}		40		ns
$\overline{\text{MRAS}}$ (0:3) precharge time	t_{RP}		50		ns
$\overline{\text{MRAS}}$ (0:3) hold time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{RSH}		12		ns
$\overline{\text{MRAS}}$ (0:3) ↓ → $\overline{\text{LCAS}}$/$\overline{\text{UCAS}}$ ↓ delay time	t_{RCD}		14		ns
$\overline{\text{MRAS}}$ (0:3) ↓ → $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓ access time	t_{RAC}		95		ns
$\overline{\text{MRAS}}$ (0:3) ↓ → column address delay time	t_{RAD}		12		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ hold time (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{CSH}		50		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ pulse width	t_{HCAS}		12		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ precharge time	t_{CP}		10		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ precharge → $\overline{\text{MRAS}}$ (0:3) ↑ access time	t_{ACP}		60		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓ → $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓ access time	t_{CAC}		43		ns
Read cycle time	t_{HPC}		30		ns
Row address setup time (ADD (9:20)) (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{ASR}		0		ns
Row address hold time (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{RAH}		10		ns
Column address setup time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{ASC}		0		ns
Column address setup time (vs. $\overline{\text{MRAS}}$ (0:3) ↑)	t_{RAL}		35		ns
Column address hold time 1 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH1}	ADD (9:18)[Note 1]	12		ns
Column address hold time 2 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH2}	ADD (9:18)[Note 2]	12		ns
Column address hold time 3 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH3}	ADD (19:20)[Note 2]	12		ns
Column address → $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓ access time	t_{AA}		60		ns
$\overline{\text{RAMOE}}$ ↓ → $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓ access time	t_{OEA}		38		ns
Data input setup time 1 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{DS1}		20		ns
Data input hold time 1 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{DH1}		5		ns
Data input setup time 2 (vs. $\overline{\text{MRAS}}$ (0:3) ↑)	t_{DS2}		20		ns
Data input hold time 2 (vs. $\overline{\text{MRAS}}$ (0:3) ↑)	t_{DH2}		5		ns

Notes 1. Applies to addresses other than the last address during block access

2. Applied to the last address during block access

(4) EDO type DRAM read parameter (2/2)



Note The VR4101 does not have an output enable pin (RAMOE) for DRAM. Create an output enable pin (RAMOE) by using the inverted signal of the RSTSW pin.

(5) EDO type DRAM write parameter (1/2)

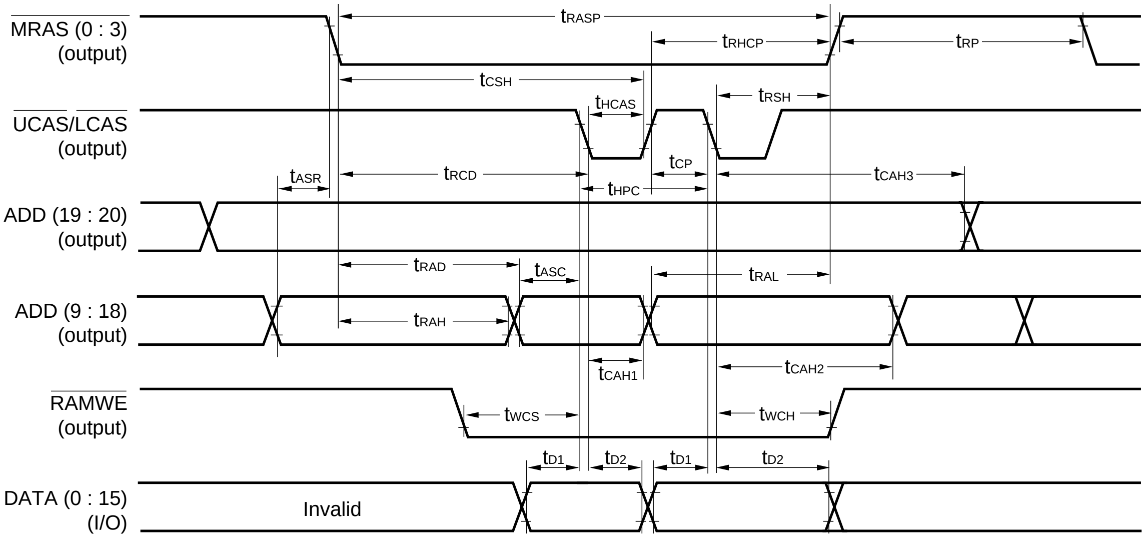
The target DRAM is the μPD42S16165L-A70 or μPD42S18165L-A70.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{MRAS}}$ (0:3) pulse width	t_{RASP}		70		ns
$\overline{\text{MRAS}}$ (0:3) hold time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ precharge)	t_{RHCP}		40		ns
$\overline{\text{MRAS}}$ (0:3) precharge time	t_{RP}		50		ns
$\overline{\text{MRAS}}$ (0:3) hold time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{RSH}		12		ns
$\overline{\text{MRAS}}$ (0:3) ↓ → $\overline{\text{LCAS}}$/$\overline{\text{UCAS}}$ ↓ delay time	t_{RCD}		14		ns
$\overline{\text{MRAS}}$ (0:3) ↓ → column address delay time	t_{RAD}		12		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ hold time (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{CSH}		50		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ pulse width	t_{HCAS}		12		ns
$\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ precharge time	t_{CP}		10		ns
Write cycle time	t_{HPC}		30		ns
Row address setup time (ADD (9:20)) (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{ASR}		0		ns
Row address hold time (vs. $\overline{\text{MRAS}}$ (0:3) ↓)	t_{RAH}		10		ns
Column address setup time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{ASC}		0		ns
Column address setup time (vs. $\overline{\text{MRAS}}$ (0:3) ↑)	t_{RAL}		35		ns
Column address hold time 1 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH1}	ADD (9:18)Note 1	12		ns
Column address hold time 2 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH2}	ADD (9:18)Note 2	12		ns
Column address hold time 3 (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{CAH3}	ADD (19:20)Note 2	12		ns
$\overline{\text{RAMWE}}$ setup time (vs. $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ ↓)	t_{WCS}		0		ns
$\overline{\text{RAMWE}}$ hold time (vs. $\overline{\text{LCAS}}$/$\overline{\text{UCAS}}$ ↓)	t_{WCH}		10		ns
Data output setup time (vs. $\overline{\text{LCAS}}$/$\overline{\text{UCAS}}$ ↓)	t_{D1}		0		ns
Data output hold time (vs. $\overline{\text{LCAS}}$/$\overline{\text{UCAS}}$ ↓)	t_{D2}		10		ns

Notes 1. Applies to addresses other than the last address during block access

2. Applied to the last address during block access

(5) EDO type DRAM write parameter (2/2)

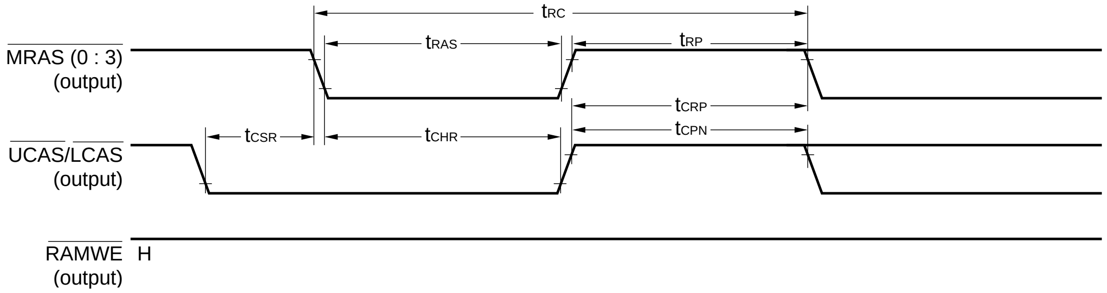


(6) DRAM refresh parameter

The target DRAM is the μPD42S161615L-A70 or μPD42S18165L-A70.

(a) CAS-before-RAS refresh parameter

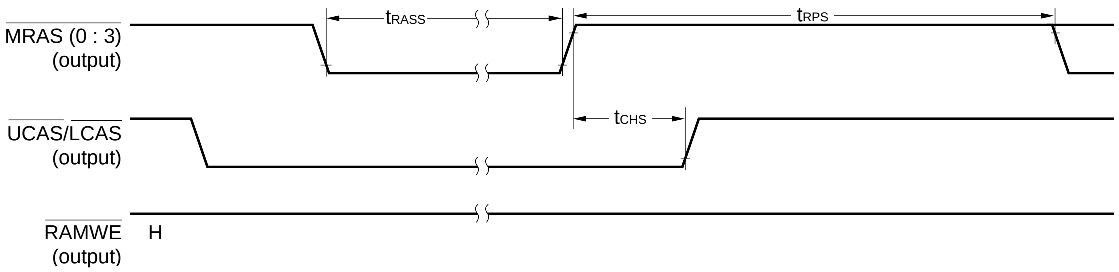
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Read/write cycle time	t_{RC}		130		ns
MRAS (0:3) pulse width	t_{RAS}		70		ns
MRAS (0:3) precharge time	t_{RP}		50		ns
UCAS/LCAS setup time (vs. MRAS (0:3) ↓)	t_{CSR}		5		ns
UCAS/LCAS hold time (vs. MRAS (0:3) ↓)	t_{CHR}		10		ns
UCAS/LCAS ↑ → MRAS (0:3) precharge time	t_{CRP}		5		ns
UCAS/LCAS precharge time	t_{CPN}		10		ns



(b) CAS-before-RAS self-refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3) pulse width[Note]	t_{RASS}		100		μs
MRAS (0:3) precharge time	t_{RPS}		130		ns
UCAS/LCAS hold time (vs. MRAS (0:3) ↑)	t_{CHS}		–50		ns

Note The CAS-before-RAS self-refresh parameter is valid when t_{RASS} exceeds 100 μs.



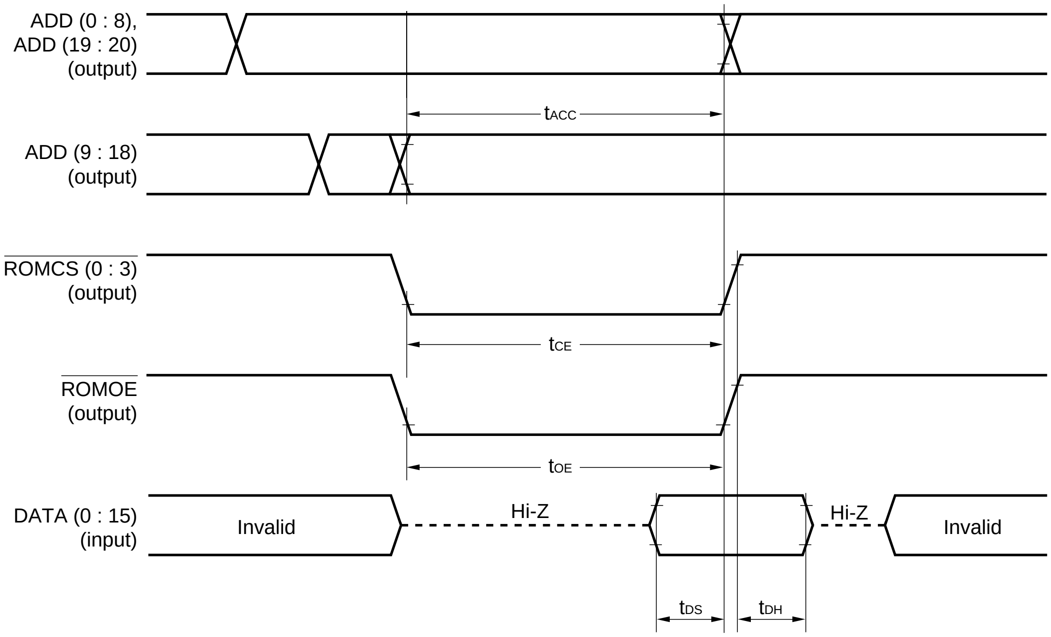
(7) Normal ROM parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Access time width from address (ADD (0:20))Note	t_{ACC}		60N – 28		ns
Access time width from $\overline{\text{ROMCS (0:3)}}$Note	t_{CE}		60N – 28		ns
Access time width from $\overline{\text{ROMOE}}$Note	t_{OE}		60N – 28		ns
Data input setup time (vs. $\overline{\text{ROMCS (0:3)}}$ ↑, $\overline{\text{ROMOE}}$ ↑)	t_{DS}		20		ns
Data input hold time (vs. $\overline{\text{ROMCS (0:3)}}$ ↑, $\overline{\text{ROMOE}}$ ↑)	t_{DH}		5		ns

Note Set the value of N by using the WROMA (0:2) bits of the BCUSPEEDREG register.

WROMA2	WROMA1	WROMA0	N
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

When WROMA (0 : 2) = 111B



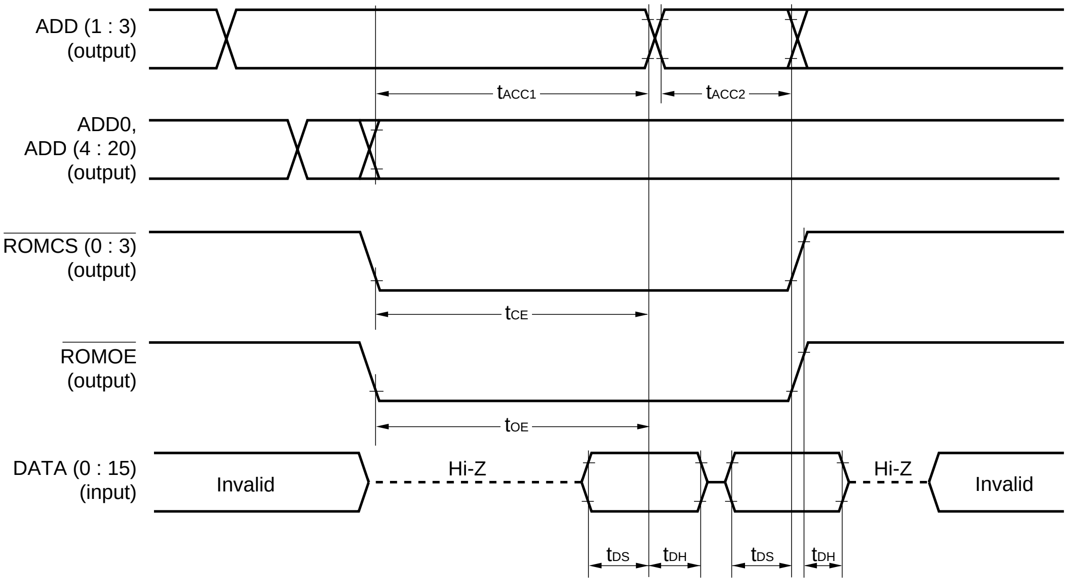
(8) Page ROM parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Access time width 1 from address (ADD (0:20))[Note]	t_{ACC1}		60N – 28		ns
Access time width 2 from address[Note]	t_{ACC2}		60M – 28		ns
Access time width from $\overline{\text{ROMCS (0:3)}}$[Note]	t_{CE}		60N – 28		ns
Access time width from $\overline{\text{ROMOE}}$[Note]	t_{OE}		60N – 28		ns
Data input setup time	t_{DS}		20		ns
Data input hold time	t_{DH}		5		ns

Note Set the values of N and M by using the WROMA (0:2) bits and WPROM (0:1) bits of the BCUSPEEDREG register, respectively.

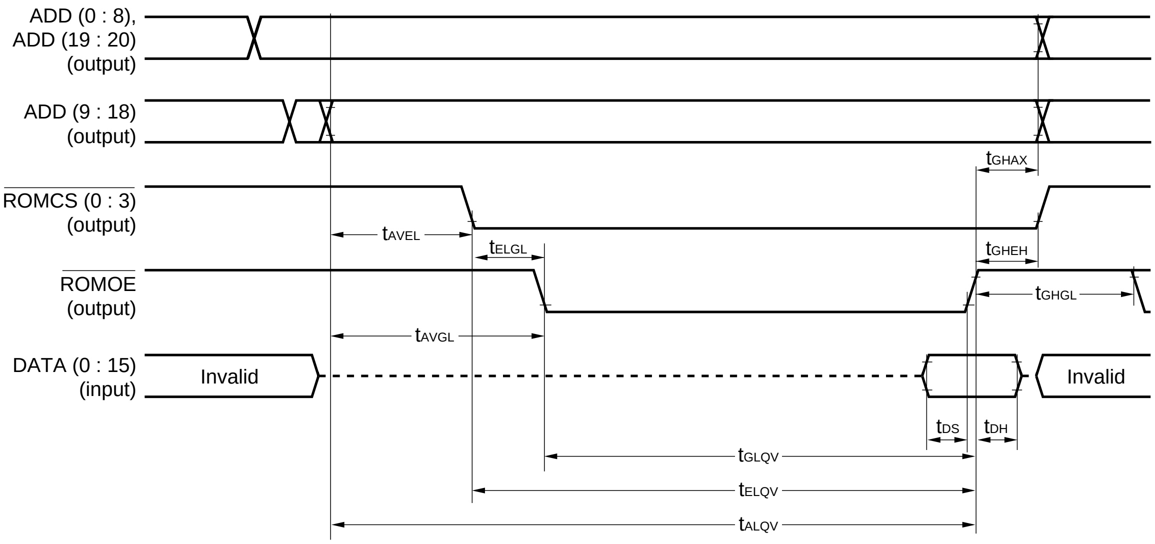
WROMA2	WROMA1	WROMA0	N
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

WPROM1	WPROM0	M
0	0	3
0	1	2
1	0	1
1	1	—



(9) Flash memory mode read parameter

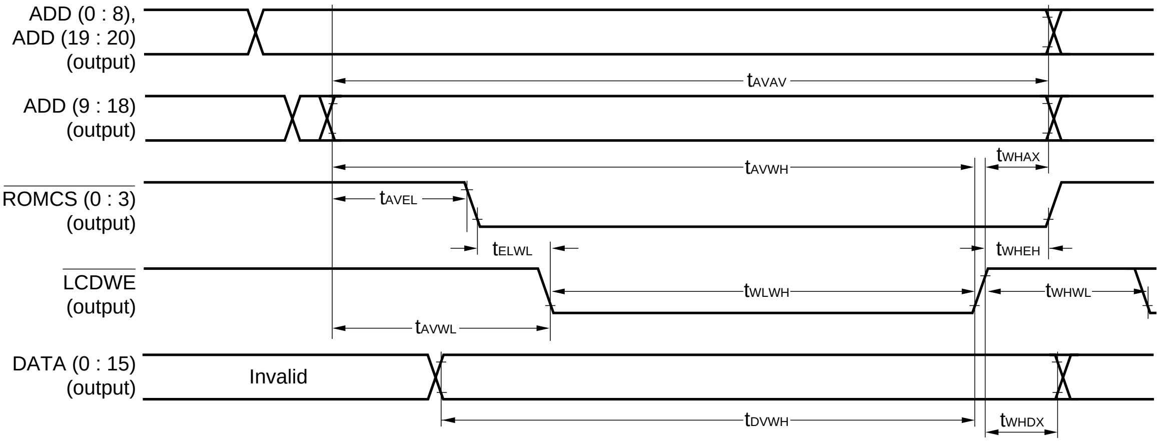
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address (ADD (0:20)) → data output delay time	t_{AVQV}		180		ns
Address (ADD (0:20)) setup time (vs. $\overline{\text{ROMCS (0:3)}}$ ↓)	t_{AVEL}		0		ns
Address hold time (vs. $\overline{\text{ROMOE}}$ ↑)	t_{GHAX}		10		ns
$\overline{\text{ROMCS (0:3)}}$ setup time (vs. $\overline{\text{ROMOE}}$ ↓)	t_{ELGL}		10		ns
$\overline{\text{ROMCS (0:3)}}$ ↓ → data output delay time	t_{ELQV}		180		ns
$\overline{\text{ROMOE}}$ ↓ → data output delay time	t_{GLQV}		80		ns
Address (ADD (0:20)) setup time (vs. $\overline{\text{ROMOE}}$ ↓)	t_{AVGL}		0		ns
$\overline{\text{ROMCS (0:3)}}$ hold time (vs. $\overline{\text{ROMOE}}$ ↑)	t_{GHEH}		10		ns
$\overline{\text{ROMOE}}$ high-level width	t_{GHGL}		75		ns
Data input setup time (vs. $\overline{\text{ROMOE}}$ ↑)	t_{DS}		20		ns
Data input hold time (vs. $\overline{\text{ROMOE}}$ ↑)	t_{DH}		5		ns



Remark The dotted line indicates a high-impedance state.

(10) Flash memory mode write parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write cycle time	t_{AVAV}		150		ns
Address (ADD (0:20)) setup time (vs. $\overline{\text{LCDWE}}$ ↑)	t_{AVWH}		75		ns
Address (ADD (0:20)) setup time (vs. $\overline{\text{ROMCS (0:3)}}$ ↓)	t_{AVEL}		0		ns
Address hold time (vs. $\overline{\text{LCDWE}}$ ↑)	t_{WHAX}		10		ns
Address (ADD (0:20)) setup time (vs. $\overline{\text{LCDWE}}$ ↓)	t_{AVWL}		25		ns
$\overline{\text{ROMCS (0:3)}}$ setup time (vs. $\overline{\text{LCDWE}}$ ↓)	t_{ELWL}		10		ns
$\overline{\text{ROMCS (0:3)}}$ hold time (vs. $\overline{\text{LCDWE}}$ ↑)	t_{WHEH}		10		ns
$\overline{\text{LCDWE}}$ low-level width	t_{WLWH}		75		ns
$\overline{\text{LCDWE}}$ high-level width	t_{WHWL}		75		ns
Data output setup time (vs. $\overline{\text{LCDWE}}$ ↑)	t_{DVWH}		75		ns
Data output hold time (vs. $\overline{\text{LCDWE}}$ ↑)	t_{WHDX}		10		ns



[MEMO]

(11) System bus parameter (LCDRDY) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
PCMCLK low-level pulse width	t_{PCLKL}		45		ns
PCMCLK high-level pulse width	t_{PCLKH}		45		ns
Address (ADD (0:20)) setup time (vs. PCMCLK ↓)	t_{AVCK}		15		ns
Address (ADD (0:20)) setup time (vs. command signal ↓)[Note 1, 2]	t_{AVCL}		60N – 28		ns
Address hold time (vs. command signal ↑)[Note 1]	t_{CHAV}		25		ns
Command signal setup time (vs. PCMCLK ↑)[Note 1]	t_{CLCK}		15		ns
Command signal low-level width[Note 1, 2]	t_{CLCH}		120N – 28		ns
Command signal recovery time[Note 1]	t_{CHCL}		100		ns
LDCRDY sampling time	t_{CLR}		0		ns
Command signal output hold time (vs. CDRDY ↑)[Note 1, 2]	t_{RHCH}		60N	120N + 31	ns
LCDRDY hold time (vs. command signal ↑)[Note 1]	t_{CHRL}		0		ns
Data output setup time (vs. command signal ↓)[Note 1]	t_{DVCL}		0		ns
Data output hold time (vs. command signal ↑)[Note 1]	t_{CHDV}		25		ns
Data input setup time (vs. command signal ↑)[Note 1]	t_{DS}		20		ns
Data input hold time (vs. command signal ↑)[Note 1]	t_{DH}		15		ns

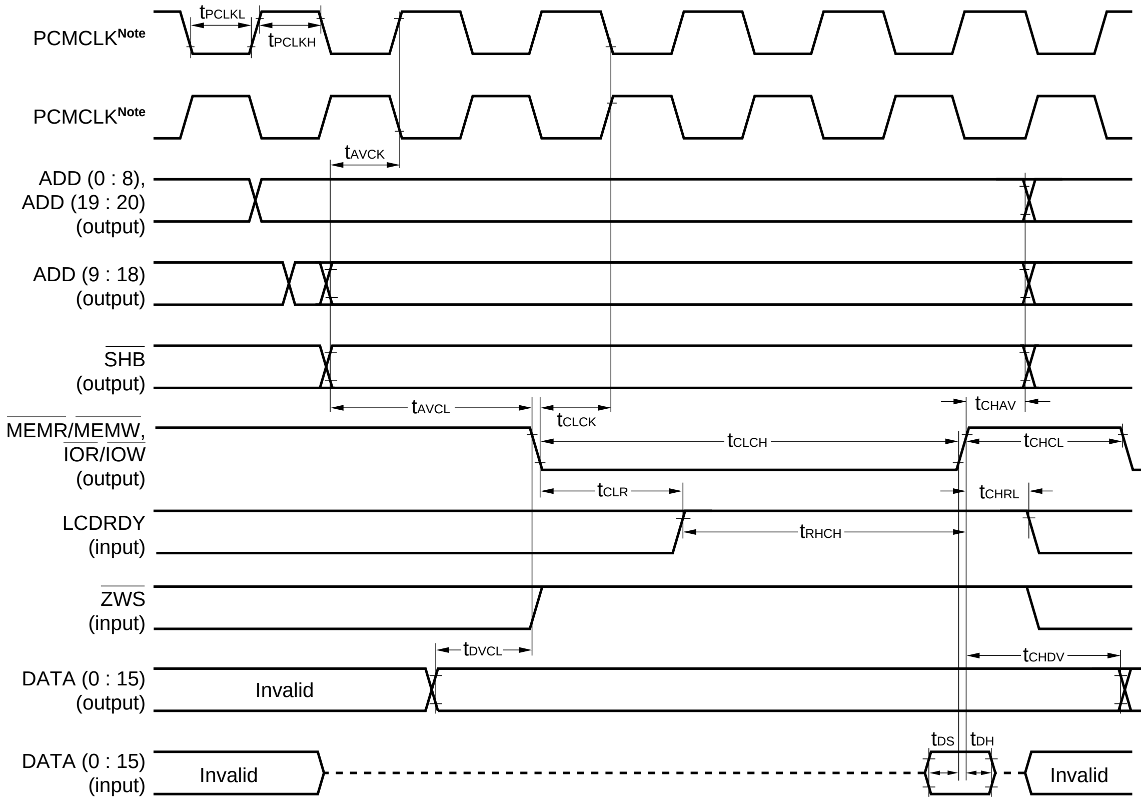
Notes 1. With the V_R4101, the $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$ pins are called the command signals for the system bus interface.

2. Set the value of N by using the WISA (0:2) bits of the BCUSPEEDREG register.

WISA2	WISA1	WISA0	N
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	—
1	1	1	—

(11) System bus parameter (LCDRDY) (2/2)

When WISA (0 : 2) = 101B



Note PCMCLK indicates that there are two possible relationships between PCMCLK and other system bus interface signals.

Remark The dotted line indicates a high-impedance state.

(12) System bus parameter ($\overline{\text{ZWS}}$) (1/2)

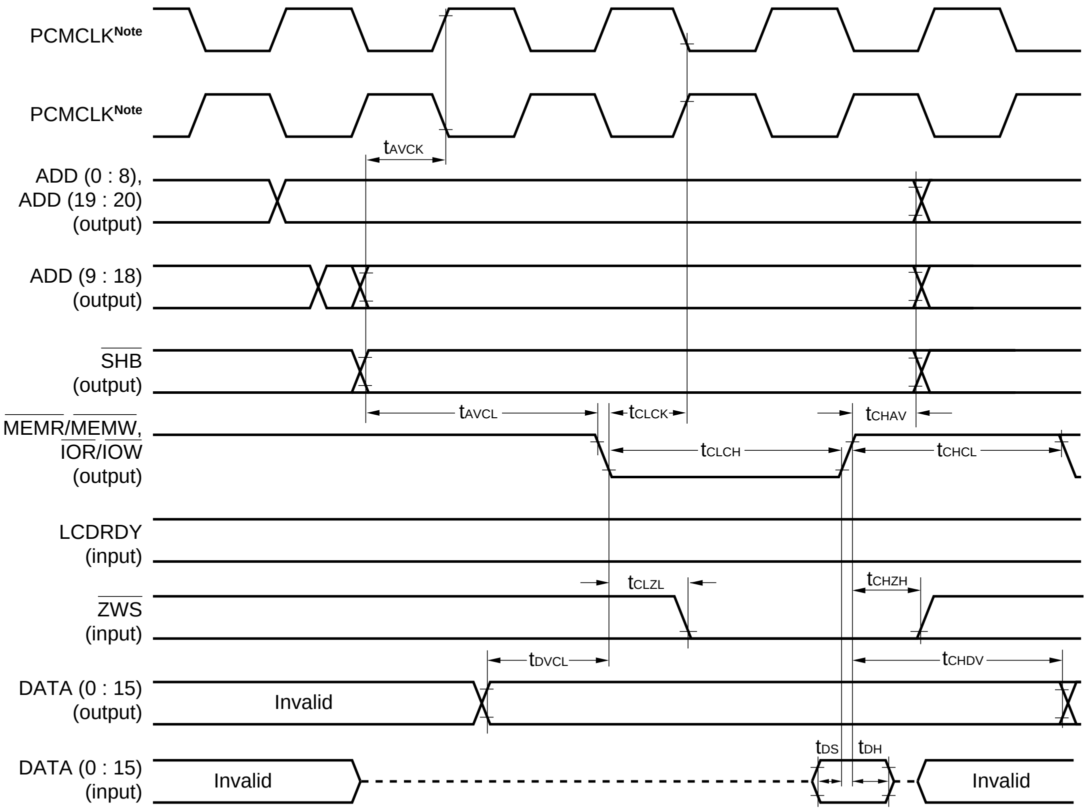
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address (ADD (0:20)) setup time (vs. PCMCLK ↓)	t_{AVCK}		15		ns
Address (ADD (0:20)) setup time (vs. command signal ↓)[Note 1, 2]	t_{AVCL}		60N – 28		ns
Address hold time (vs. command signal ↑)[Note 1]	t_{CHAV}		25		ns
Command signal setup time (vs. PCMCLK ↑)[Note 1]	t_{CLCK}		15		ns
Command signal recovery time[Note 1]	t_{CHCL}		100		ns
Data output setup time (vs. command signal ↓)[Note 1]	t_{DVCL}		0		ns
Data output hold time (vs. command signal ↑)[Note 1]	t_{CHDV}		25		ns
Data input setup time (vs. command signal ↑)[Note 1]	t_{DS}		20		ns
Data input hold time (vs. command signal ↑)[Note 1]	t_{DH}		15		ns
Command signal low-level width[Note 1, 2]	t_{CLCH}		60N – 28		ns
$\overline{\text{ZWS}}$ delay time (vs. command signal ↓)[Note 1, 2]	t_{CLZL}			60N – 111	ns
$\overline{\text{ZWS}}$ hold time (vs. command signal ↑)[Note 1]	t_{CHZH}		0		ns

Notes 1. With the V$_R$4101, the $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$ pins are called the command signals for the system bus interface.

2. Set the value of N by using the WISA (0:2) bits of the BCUSPEEDREG register.

WISA2	WISA1	WISA0	N
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	—
1	1	1	—

(12) System bus parameter ($\overline{\text{ZWS}}$) (2/2)



Note PCMCLK indicates that there are two possible relationships between PCMCLK and other system bus interface signals.

Remark The dotted line indicates a high-impedance state.

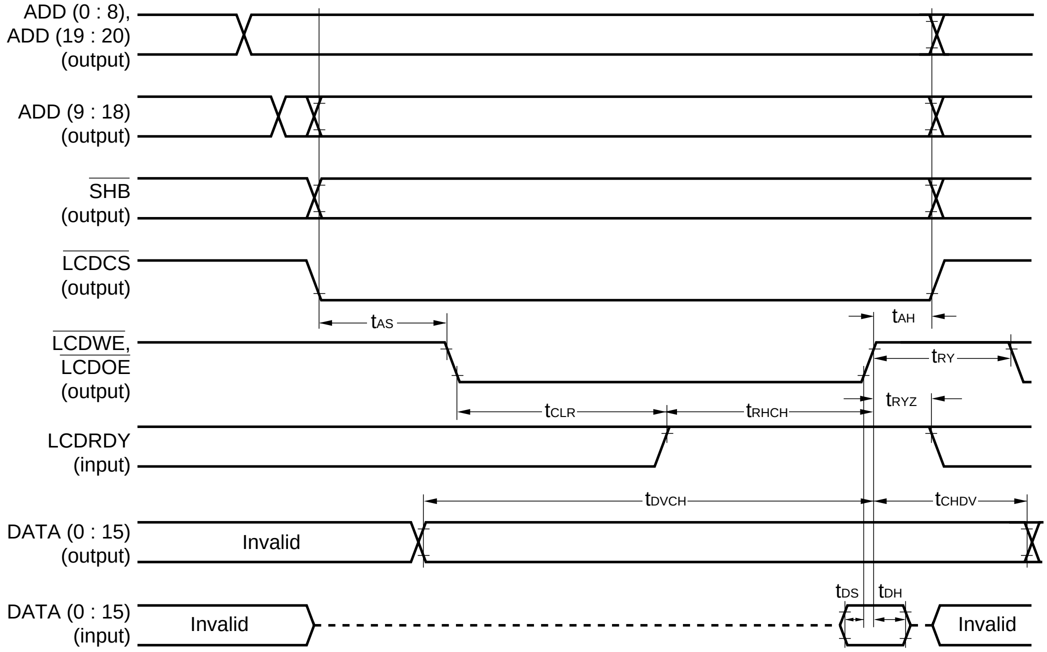
(13) LCD interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (vs. command signal ↓)Note 1	t_{AS}		15		ns
Address hold time (vs. command signal ↑)Note 1	t_{AH}		0		ns
Command signal recovery timeNote 1	t_{RY}		30		ns
LCDRDY sampling time	t_{CLR}		0		ns
Command signal output hold time (vs. LCDRDY ↑)Note 1, 2	t_{RHCH}		60N	60N + 151	ns
LCDRDY hold time (vs. command signal ↑)Note 1	t_{RYZ}		0		ns
Data output setup time (vs. command signal ↑)Note 1, 2	t_{DVCH}		60N + 120		ns
Data output hold time (vs. command signal ↑)Note 1	t_{CHDV}		25		ns
Data input setup time (vs. command signal ↑)Note 1	t_{DS}		20		ns
Data input hold time (vs. command signal ↑)Note 1	t_{DH}		15		ns

Notes 1. With the V_R4101, the $\overline{\text{LCDOE}}$ and $\overline{\text{LCDWE}}$ pin are called the command signals for the LCD interface.

2. Set the value of N by using the WLCDA (0:1) bits of the BCUSPEEDREG register.

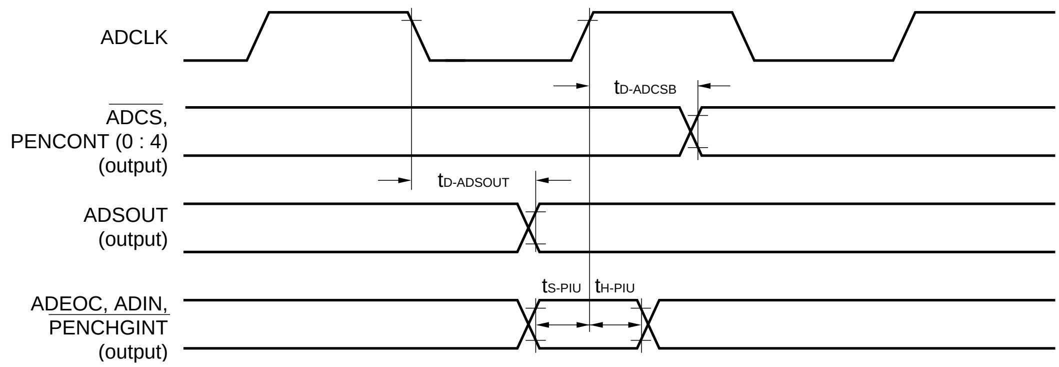
WLCDA1	WLCDA0	N
0	0	8
0	1	6
1	0	4
1	1	2



Remark The dotted line indicates a high-impedance state.

(14) A/D controller interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output delay (vs. ADCLK ↑)	$t_{D\text{-}ADCSB}$			400	ns
Output delay (vs. ADCLK ↓)	$t_{D\text{-}ADSOUT}$			300	ns
Input setup time (vs. ADCLK ↑)	$t_{S\text{-}PIU}$		80		ns
Input hold time (vs. ADCLK ↑)	$t_{H\text{-}PIU}$		200		ns



(15) Audio output interface parameter

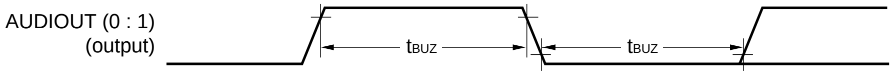
Parameter	Symbol	Condition	MIN.	MAX.	Unit
AUDIOUT (0:1) output pulse width[Note 1]	t_{BUZ}	Buzz mode	30.15L – 1	30.16L + 1	μs
AUDIOUT (0:1) output high-level width[Note 2]	t_{PWMH}	PWM mode	60M – 31	60M + 31	ns
AUDIOUT (0:1) output low level[Note 3]	t_{PWML}	PWM mode	60N – 31	60N + 31	ns

Notes **1.** L is the value set to the AIUCOUNT0REG register in the Buzz mode.

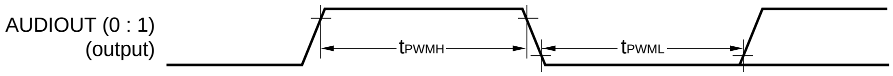
2. M is the value set to the AIUCOUNT0REG register in the PWM mode, or the count data of the high-level pulse (first) prepared for DMA transfer.

3. N is the value set to the AIUCOUNT1REG register in the PWM mode, or the count data of the low-level pulse (second) prepared for DMA transfer.

In Buzz mode



In PWM mode



(16) Keyboard interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-level width[Note 1]	t_{SCAN}		30K – 1	30.16K + 1	μs
Idle time (KSCANn ↓ → KSCAN (n+1) ↑)[Note 2]	t_{KWAIT}		30L – 1	30.16L + 1	μs
Key scan interval time[Note 3]	t_{KI}		30M – 1	30.16M + 1	μs
Key input setup time (vs. KSCANn ↑)[Note 4]	t_{KS}		30N – 1		μs
Key input hold time (vs. KSCANn ↓)	t_{KH}		0		μs

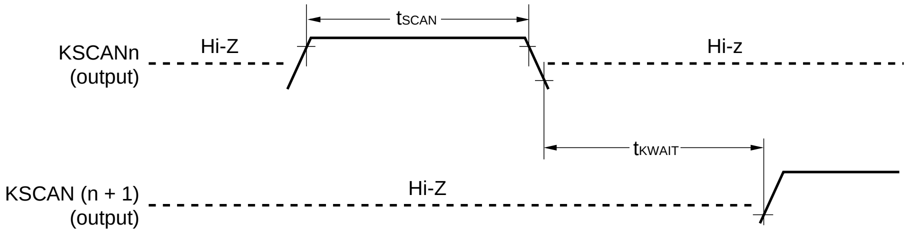
Notes **1.** K: Sum of the values set to the T1COUNT (0:4) bits and T2COUNT (0:4) bits of the KIUWKSREG register

2. L: Value set to the T3COUNT (0:4) bits of the KIUWKSREG register

3. M: Value set to KIUWKIREG register

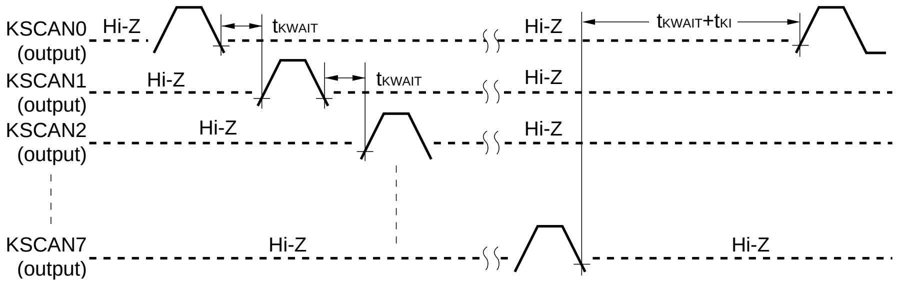
4. N: Value set to the T1COUNT (0:4) bits of the KIUWKSREG register

(a) Keyboard scan parameter 1

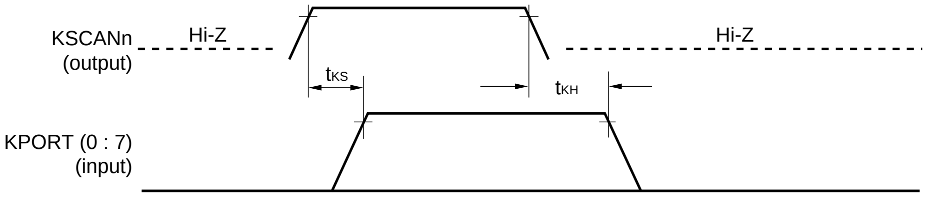


Remark n = 0 to 7

(b) Keyboard scan parameter 2



(c) Keyboard parameter



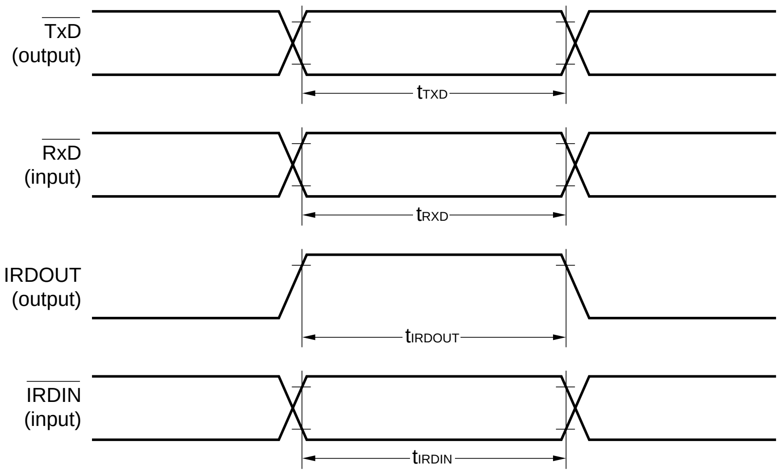
Remark n = 0 to 7

(17) Serial interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{TxD}}$ output pulse width[Note]	t_{TXD}		N – 1	N + 1	μs
$\overline{\text{RxD}}$ input pulse width[Note]	t_{RXD}		(9/16)N		μs
IRDOUT high-level output pulse width[Note]	t_{IRDOUT}		(3/16)N – 1	(3/16)N + 1	μs
$\overline{\text{IRDIN}}$ input pulse width	t_{IRDIN}		1		μs

Note N: Transfer rate of baud rate per bit set to the BPR0 (0:2) bits of the SIUBAUDSELREG register

BPR02	BPR01	BPR00	Baud Rate (bps)	N (μs)
1	1	1	115200	8.68
1	1	0	57600	17.36
1	0	1	38400	26.04
1	0	0	19200	52.03
0	1	1	9600	104.16
0	1	0	4800	208.33
0	0	1	2400	416.66
0	0	0	1200	833.33

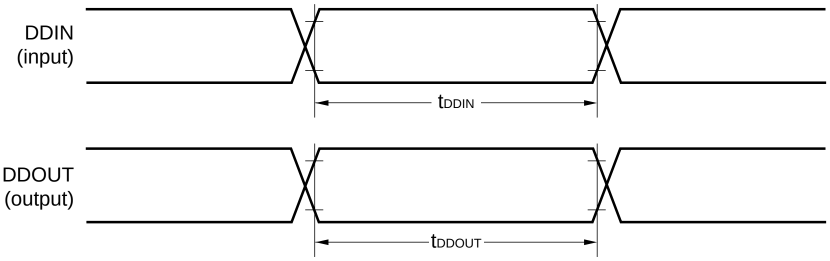


(18) Debug serial interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
DDOUT output pulse width[Note]	t_{DDOUT}		N – 1	N + 1	μs
DDIN input pulse width[Note]	t_{DDIN}		(9/16)N		μs

Note N: Transfer rate of baud rate per bit set to the BPR0 (0:2) bits of the BPRM0REG register

BPR02	BPR01	BPR00	Baud Rate (bps)	N (μs)
1	1	1	115200	8.68
1	1	0	57600	17.36
1	0	1	38400	26.04
1	0	0	19200	52.03
0	1	1	9600	104.16
0	1	0	4800	208.33
0	0	1	2400	416.66
0	0	0	1200	833.33

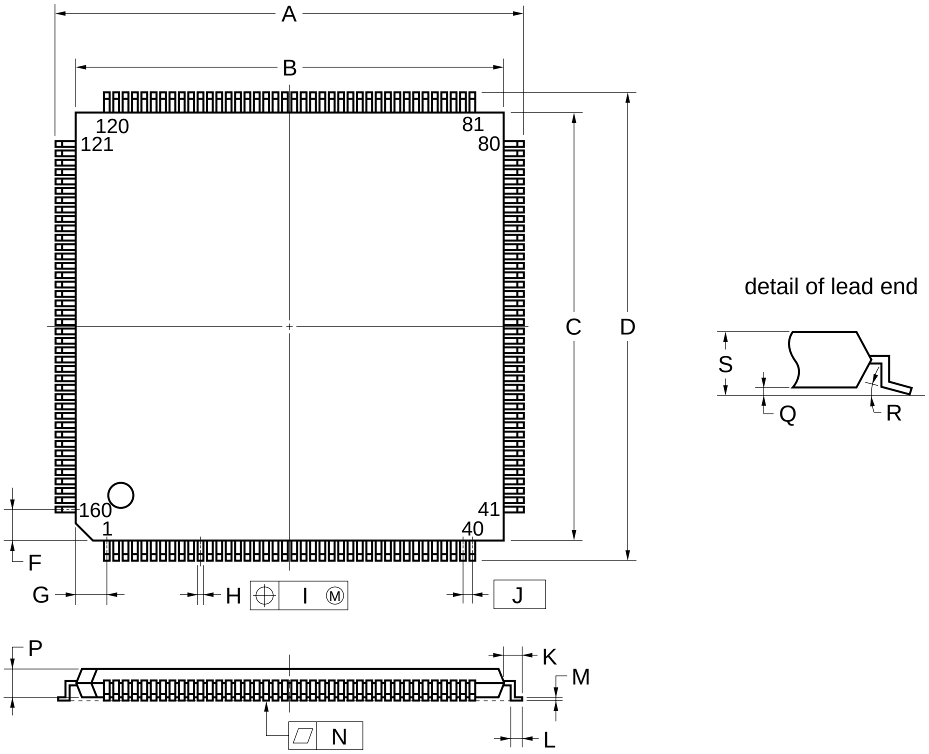


LOAD COEFFICIENT (DELAY TIME PER LOAD CAPACITANCE)

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

21. PACKAGE DRAWING

160 PIN PLASTIC LQFP (FINE PITCH) (□24)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	26.0±0.2	$1.024^{+0.008}_{-0.009}$
B	24.0±0.2	0.945±0.008
C	24.0±0.2	0.945±0.008
D	26.0±0.2	$1.024^{+0.008}_{-0.009}$
F	2.25	0.089
G	2.25	0.089
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.7 MAX.	0.067 MAX.

S160GM-50-8ED-2

★ 22. RECOMMENDED SOLDERING CONDITIONS

This μPD30101 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 22-1. Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Time limit: 3 days[Note] (thereafter 10 to 72 hours prebaking required at 125 °C) **<Precaution>** Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray).	IR35-103-2
VPS	Package peak temperature: 215 °C, Duration: 25 to 40 sec. max. (at 200 °C or above), Number of times: Twice max., Time limit: 3 days[Note] (thereafter 10 to 72 hours prebaking required at 125 °C) **<Precaution>** Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray).	VP15-103-2
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

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