NEC

User's Manual

VRC4171A™ Companion Chip

for VR41xx™ Family MIPS® RISC Microprocessors

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Introduction 1

The VRC4171A™ is a companion chip to NEC's 64-bit VR41xx™ family of MIPS® RISC microprocessors. Together, these two devices form the essential engine for most Windows® CE-based handheld products.

- **Processor Interface**
  - LCD module: *RD, *WR, *LCDCS and LCDRDY signals from the VR41xx
  - Other modules: mini-ISA-like 16-bit bus interface (as defined in the VR41xx)
  - 256 x 18-bit on-chip color palette RAM for STN, DSTN, and TFT color panels
  - On-chip hardware cursor control (32 x 32 x 2)

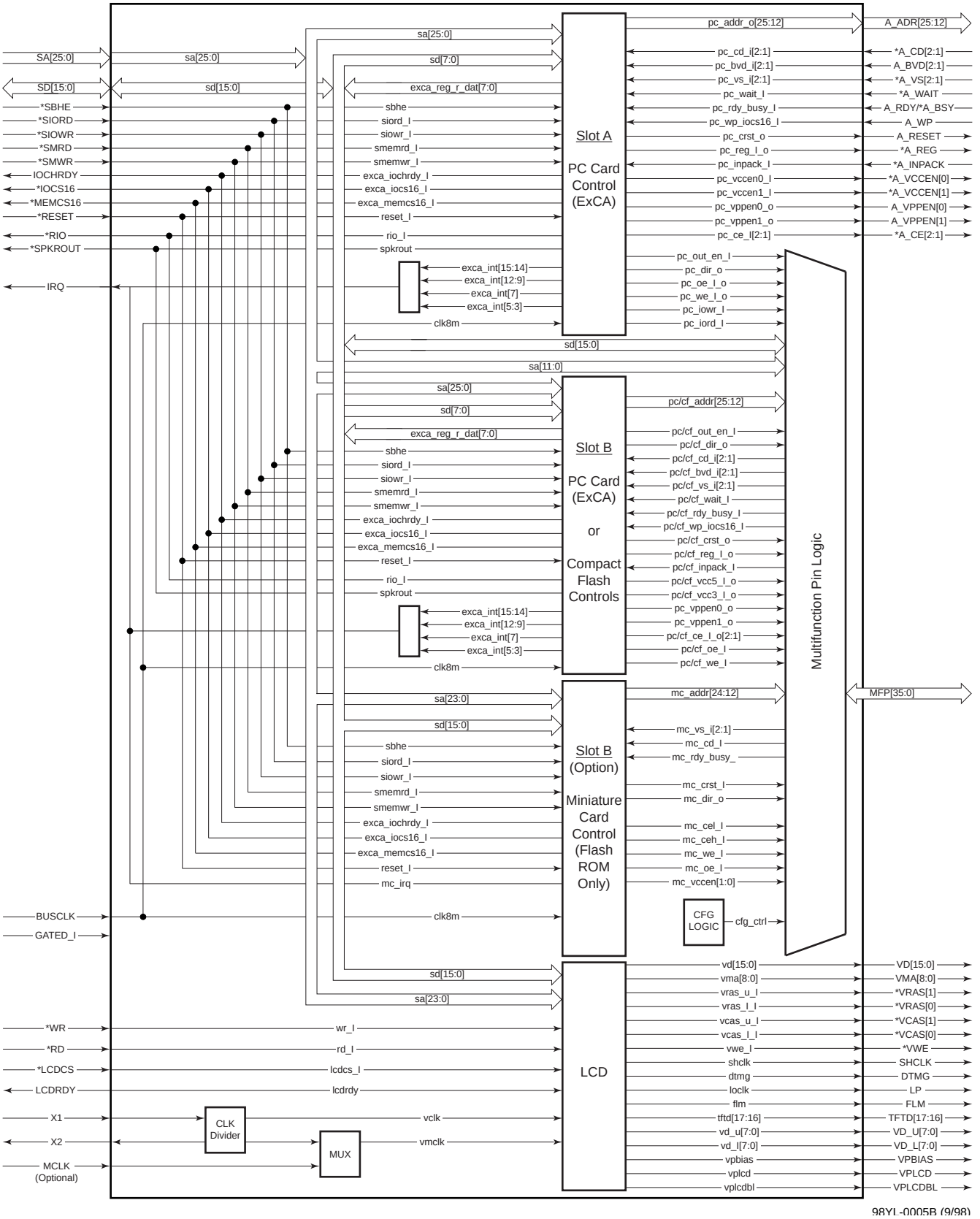
- **LCD Panel Support**
  - 240- and 480-line single scans
  - 480-line dual scans
  - STN, DSTN, and TFT color panels
  - Nonindexed true color (R, G, B): 15-bit (5-5-5) and 16-bit (5-6-5)
  - Controller functions (320 x 240, 480 x 240, 640 x 240, and 640 x 480)
    - Monochrome: up to 16 gray-scale levels (1, 2, or 4 bits/pixel)
    - Color depth: 1, 2, 4, 5, 6, 8, or 16 bits/pixel

- **Frame Buffer Memory**
  - One or two 3.3-volt 256K x 16-bit DRAMs (512K or 1 MB)
  - One 1 MB x 16-bit DRAM (2 MB)

- **PC Card™ Slots (up to two)**
  - PC Card or CompactFlash™ with adapter
  - PC Card or CompactFlash or Miniature Card™
    - PC Card controller: compliant with ExCA and PCMCIA release 2.1
    - CompactFlash controller: compliant with release 1.1
    - Miniature Card controller: compliant with release 1 (flash/ROM only)

- **Other Features**
  - Up to four general-purpose I/O (GPIO) pins *or* up to two GPIO pins and two PCS pins
  - 5-volt tolerance for LCD panel, frame buffer, and PC Card interface signals
  - 208-pin LQFP package
  - 3.3-volt ±5% operation

Figure 1-1. Internal Block Diagram



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Pin Functions 2

The VRC4171A companion chip has 208 total pins (Figure 2-1):

- 188 signal pins
- 20 power/ground pins

Table 2-1. Clock Pins

Name	No.	Type	Drive	Function	Description
X1	55	XTL	–	Crystal input	Frequency operation ranges up to 50 MHz. Lower frequency crystals can be used for lower resolution LCD panels or lower bits/pixel displays to minimize overall power consumption.
X2	54	XTL	–	Crystal output	
CRYL_INH	56	I–S	–	Crystal inhibit input	Normally low; active high signal controls crystal oscillation to save power during suspend mode if a fast resume is not required (Note 2)
BUSCLK	110	CLK	–	ISA bus clock input	Running at 8 MHz; actual operating frequency depends on the bit settings inside the VR41xx
GATED_I	25	I–S	–	Gated_I input	Normally low; active high isolates the device from any access and keeps it in this quiescent state until signal is de-asserted (**Note 2**)
MCLK (VRC4171A)	13	I	–	External clock input	Internal 50 kΩ pulldown (optional MCLK input)
Total pins	**6**				

Notes: **1.** I–S: input buffer; Schmitt trigger

2. Take care when asserting or deasserting gated input signals to ensure proper termination of normal accesses. Gated input signals: SA[25:0], SD[15:0], *SIORD, *SIOWR, *SMRD, *SMWR, *RD, *WR, *LCDCS. *SBHE is gated in the VRC4171A, but not in the VRC4171.

Figure 2-1. Pin Configuration

208-pin LQFP *(28 mm x 28 mm with 0.5 mm pin pitch)*

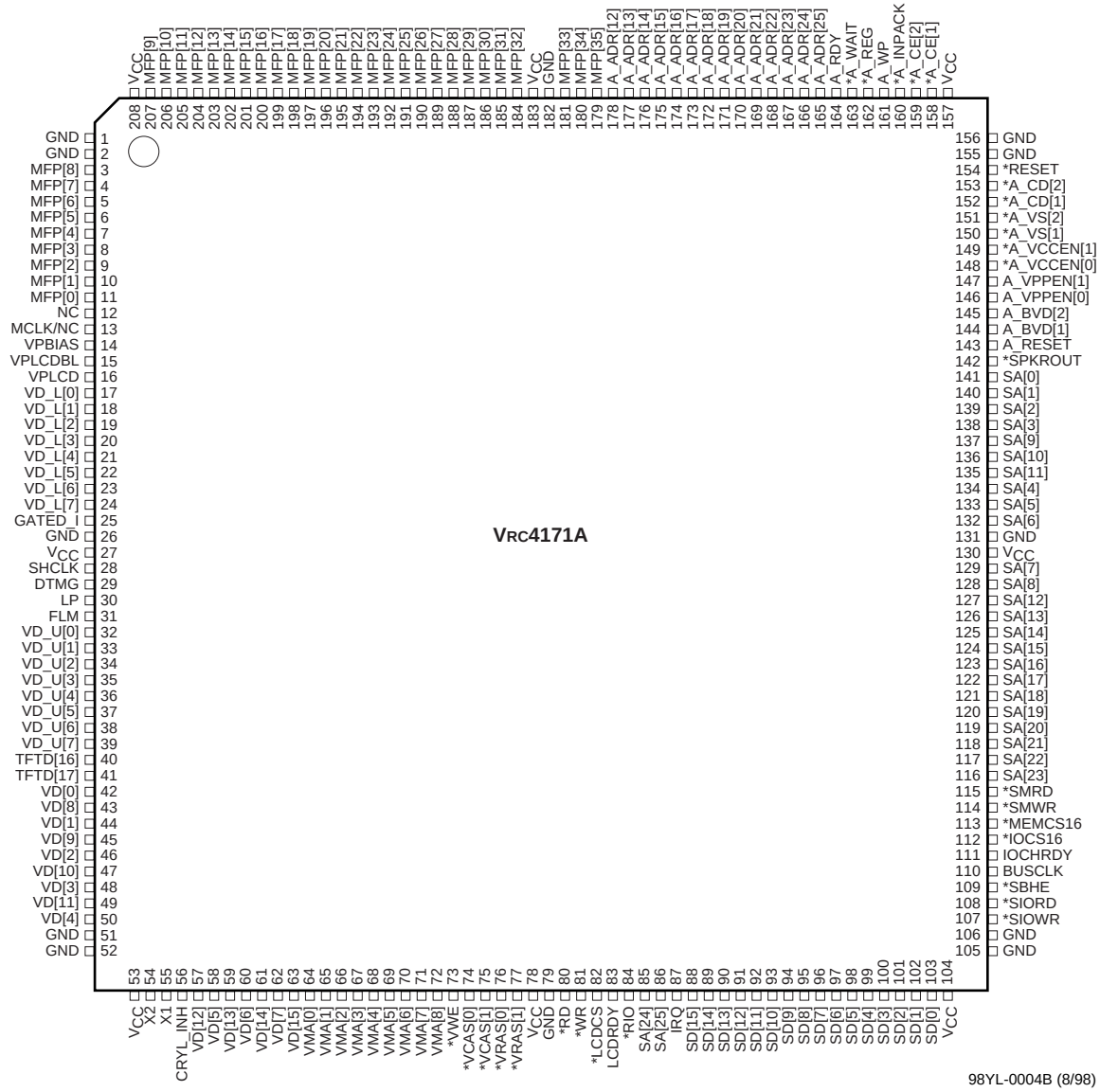

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Table 2-2. System Bus Interface Pins

Name	No.	Type	Drive	Function	Description
SA[25:0]	85–86, 116–129, 132–141	I	–	System address bus inputs	26-bit addresses
SD[15:0]	88–103	I/O	6 mA	System data bus inputs	16-bit data
*SBHE	109	I	–	System byte high enable input	Active low
*SIORD	108	I–S	–	System I/O read command strobe input	Active low
*SIOWR	107	I–S	–	System I/O write command strobe input	Active low
*SMRD	115	I–S	–	System memory read command strobe input	Active low
*SMWR	114	I–S	–	System memory write command strobe input	Active low
IOCHRDY	111	O–T	6 mA	I/O channel ready output	Active high
*IOCS16	112	O–T	6 mA	I/O 16-bit chip select output	Active low; indicates to host that the current cycle is a 16-bit I/O access
*MEMCS16	113	O–T	6 mA	Memory 16-bit chip select output	Active low; indicates to host system that the current cycle is a 16-bit memory access
*RESET	154	I–S	–	Reset input	Active low; should not directly connect to RSTOUT on VR41xx (sometimes tri-stated)
*RIO	84	O	3 mA	Ring indicator output	Active low; passed through *RI from I/O PC Card
*SPKROUT	142	O	3 mA	Digital audio signal output	Active low; provides single amplitude (digital) audio waveform to drive the system speaker; passed through *SPKR from I/O PC Card
IRQ	87	O	3 mA	Interrupt request output	Active high
Total pins	**54**				

Notes: **1.** I: input buffer
2. O: output buffer
3. I/O: bidirectional input/output buffer
4. I–S: input buffer; Schmitt trigger
5. O–T: tri-statable output buffer

Table 2-3. LCD Graphics Controller Pins

Name	No.	Type	Drive	Function	Description
*RD	80	I–S	–	Read command input	Active low; asserted by the VR41xx to indicate a read cycle for RAM, ROM, or video memory
*WR	81	I–S	–	Write command input	Active low; asserted by the VR41xx to indicate a write cycle for RAM, ROM, or video memory
*LCDCS	82	I–S	–	Video memory access chip select input (Note 6)	Active low; indicates a video memory read cycle when *LCDCS and *RD valid *or* video memory write cycle when *LCDCS and *WR are valid (Note 5)
LCDRDY	83	O	6 mA	Video memory data ready output	Active high; indicates that video memory data is valid on the system data bus to VR41xx CPU
VD[15:0]	42–50, 57–63	I/O–5V	3 mA	Video frame buffer memory data bus	16-bit data
VMA[8:0]	64–72	O–5 V	3 mA	Video memory addresses	9 bits for 256K x 16-bit DRAM
VRAS1/ VMA9	77	O–5 V	3 mA	Video memory upper row address strobe control 1 output	Active low signal for second 256K x 16-bit DRAM or 10th address bit of 1M x 16-bit DRAM; configured at power up (Note 7)
VRAS0	76	O-5 V	3 mA	Video memory upper row address strobe control 0 output	Active low
*VCAS[1:0]	74–75	I/O–5 V	3 mA	Video memory upper-byte/lower-byte column address strobe control outputs	Active low
*VWE	73	O–5 V	3 mA	Video memory write command input	Active low
SHCLK	28	O–5 V	6 mA	LCD shift clock output	Shifts data into x-driver of the panel
DTMG	29	O–5 V	6 mA	TFT panels data enable output	
LP	30	O–5 V	6 mA	LCD line pulse output	
FLM	31	O–5 V	6 mA	LCD first line marker	
TFTD[17:16]	40–41	O–5 V	6 mA	TFT panel data output	Uppermost two data bits of TFT panels' 18 bits
VD_U[7:0]	32–39	O–5 V	6 mA	LCD upper-half screen data output	8 bits
VD_L[7:0]	17–24	O–5 V	6 mA	LCD lower-half screen data output	8 bits
VPLCD	16	O–5 V	3 mA	LCD panel driver power control output	Active high
VPLCDBL	15	O–5 V	3 mA	LCD panel back light power control output	Active high
VPBIAS	14	O–5 V	3 mA	LCD panel bias power control output	Active high
Total pins	**59**				

Notes:
1. I–S: input buffer; Schmitt trigger
2. O: output buffer
3. O–5 V: output buffer; 5 V tolerant
4. I/O–5 V; bidirectional input/output buffer; 5 V tolerant
5. A23=0 for video memory access; A23=1 for LCD control register access.
6. See Figure __ for a hardware hookup example.
7. Refer to Video FIFO/Memory Interface Control Register D4-D3.

Table 2-4. PC Card Controller Pins (Partial)

Name	No.	Type	Drive	Function	Description
A_RESET	143	O–T/5V	6 mA	Reset output	Active high
A_ADR[25:12]	165-178	O–T/5V	6 mA	Address bus	
A_BVD[2:1]	145-144	I–S/5V	–	Battery voltage detect inputs	Active high
*A_CD[2:1]	152-153	I–S/5V	–	Card detect inputs	Active low
*A_CE[2:1]	158-159	O–T/5V	6 mA	Chip enable output	Active low
*A_VS[2:1]	150-151	I–S/5V	–	Voltage sense inputs	Active low
*A_REG	162	O–T/5V	6 mA	Attribute memory chip select output	Active low
A_RDY/*A_BSY	164	I–5V	–	Drive ready / busy input	
*A_WAIT	163	I–5V	–	Wait input	Active low
A_WP	161	I–5V	–	Write protect input	Active high
*A_VCCEN [1:0]	148-149	O–5V	3 mA	Vcc enable outputs	Active low
A_VPPEN [1:0]	146-147	O–5V	3 mA	Programming voltage enable outputs	Active high
*A_INPACK	160	I/O–5V	3 mA	Input acknowledge input	Active low data buffer enable signal eliminates external OR gate to minimize system component count (Table 2-6)
Total pins	**32**				

Notes: **1.** O–T/5V: tri-statable output buffer; 5-volt tolerant
2. I–S/5V: input buffer; Schmitt trigger; 5-volt tolerant
3. I–5V: input buffer; 5-volt tolerant
4. O–5V; output buffer; 5-volt tolerant
5. I/O–5V: bidirectional input/output buffer; 5-volt input tolerant

Table 2-5. Memory Card Slot Options

Slot	Type	Condition
A (default)	68-pin PC Card	Without external buffers
	CompactFlash with adapter	
B (optional)	68-pin PC Card	With external buffers (additional option with or without OR gate)
	CompactFlash with adapter	
	50-pin CompactFlash	
	Miniature Card (flash/ROM only)	

Table 2-6. Multifunction Pins

Name	No.	Type	Drive	Single Slot	Dual Slots				
				A: PC Card	A: PC Card B: PC Card		A: PC Card B: CompactFlash		A: PC Card B: Miniature Card
					With External OR	Without External OR	With External OR	Without External OR	With External OR
A_VPPEN[1]	147	O–5V	3 mA	A_VPPEN[1]	A_VPPEN[1]	*A_DBUFEN [1]	A_VPPEN[1]	*A_DBUFEN [1]	A_VPPEN[1]
A_VPPEN[0]	146			A_VPPEN[0]	A_VPPEN[0]		A_VPPEN[0]		A_VPPEN[0]
*A_INPACK	160	I/O–5V		*A_INPACK	*A_INPACK	*A_DBUFEN [0]	*A_INPACK	*A_DBUFEN [0]	*A_INPACK
MFP[35]	179	O–T/5V	6 mA	A_ADR[11]	B_ADR[25]		A_ADR[11]		MC_ADR[24]
MFP[34:24]	184-192 180-181			A_ADR[10:0]	B_ADR[24:14]		A_ADR[10:0]		MC_ADR[23:13]
MFP[23]	193	I/O–5		A_D[15]	B_ADR[13]		CF_OE		MC_ADR[12]
MFP[22]	194			A_D[14]	B_ADR[12]		CF_WE		MC_ADR[11]
MFP[21]	195			A_D[13]	*B_CE[2]		*CF_CE[2]		*MC_OE
MFP[20]	196			A_D[12]	*B_CE[1]		*CF_CE[1]		*MC_WE
MFP[19]	197	I/O–S/5V		A_D[11]	*B_CD[2]		*CF_CD[2]		*MC_CEH
MFP[18]	198			A_D[10]	*B_CD[1]		*CF_CD[1]		*MC_CEL
MFP[17]	199			A_D[9]	B_BVD[2]		CF_BVD[2]		NC
MFP[16]	200			A_D[8]	B_BVD[1]		CF_BVD[1]		NC
MFP[15:14]	201-202			A_D[7:6]	*B_VS[2:1]		*CF_VS[2:1]		*MC_VS[2:1]
MFP[13]	203	I/O–5V		A_D[5]	B_RDY/ *B_BSY		CF_RDY/ *CF_BSY		*MC_BUSY
MFP[12]	204			A_D[4]	*B_WAIT		*CF_WAIT		NC
MFP[11]	205			A_D[3]	B_WP		CF_WP		NC
MFP[10]	206			A_D[2]	*B_INPACK	*B_DBUFEN [0]	*CF_INPACK	*CF_DBUFEN [0]	NC
MFP[9]	207			A_D[1]	B_RESET		CF_RESET		MC_RESET
MFP[8]	3			A_D[0]	*B_REG		*CF_REG		NC
MFP[7]	4	O–T/5V		*A_IOR	*A_ENBUF		*A_ENBUF		A_ENBUF
MFP[6]	5			*A_IOW	A_DBUFDIR		A_DBUFDIR		A_DBUFDIR
MFP[5]	6			*A_OE	*B_ENBUF		*CF_ENBUF		MC_ENBUF
MFP[4]	7			*A_WE	B_DBUFDIR		CF_DBUFDIR		MC_DBUFDIR
MFP[3]	8	I/O–5V		GPIO[3]	*B_VCCEN[1]		*CF_VCCEN[1]		*MC_VCCEN [1]
MFP[2]	9			GPIO[2]	*B_VCCEN[0]		*CF_VCCEN[0]		*MC_VCCEN [0]
MFP[1]	10			GPIO[1]/*PCS[1]	B_VPPEN[1]	*B_DBUFEN [1]	GPIO[1]/*PCS[1]	*CF_DBUFEN[1]	MC_CD
MFP[0]	11			GPIO[0]/*PCS[0]	B_VPPEN[0]		GPIO[0]/*PCS[0]		MC_CINS
Total pins	**36**								

Notes:
1. I: input buffer
2. I–S: input buffer; Schmitt trigger
3. I–5V: input buffer; 5-volt tolerant
4. I–S/5V: input buffer; 5-volt tolerant; Schmitt trigger
5. O: output buffer
6. O–T: tri-statable output buffer
7. O–5 V: output buffer; 5-volt tolerant
8. I/O: bidirectional input/output buffer
9. I/O–S: bidirectional input/output buffer; Schmitt trigger input
10. I/O–5 V: bidirectional input/output buffer; 5-volt input tolerant
11. I/O–S/5 V: bidirectional input/output buffer; 5-volt input tolerant; Schmitt trigger input
12. V_{CC}: Power (3.3 volts)
13. GND: ground

Table 2-7. External Buffer Signals

A: PC Card B: None	A: PC Card B: PC Card	A: PC Card B: CompactFlash	A: PC Card B: Miniature Card
—	A_ADR[11:0]	—	—
	A_D[15:0]	A_D[15:0]	A_D[15:0]
	*A_OE	*A_OE	*A_OE
	*A_WE	*A_WE	*A_WE
	*A_IOR	*A_IOR	*A_IOR
	*A_IOW	*A_IOW	*A_IOW
	B_ADR[11:0]	CF_ADR[10:0]	MC_ADR[10:0]
	B_D[15:0]	CF_D[15:0]	MC_D[15:0]
	*B_OE	—	—
	*B_WE	—	—
	*B_IOR	*CF_IOR	
	*B_IOW	*CF_IOW	

Note: See Section 8 for implementation information.

Table 2-8. Miscellaneous Pins

Pin Name	Pin Numbers	Type	Drive	Description
NC	12–13	–	–	Reserved; no connection
Total pins	**2**			

Table 2-9. Power and Ground Pins

Pin Name	Pin Numbers	Type	Drive	Description
VCC	27, 53, 78, 104, 130, 157, 183, 208	VCC		3.3 volts
Ground	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	GND		0.0 volts
Total pins	**20**			

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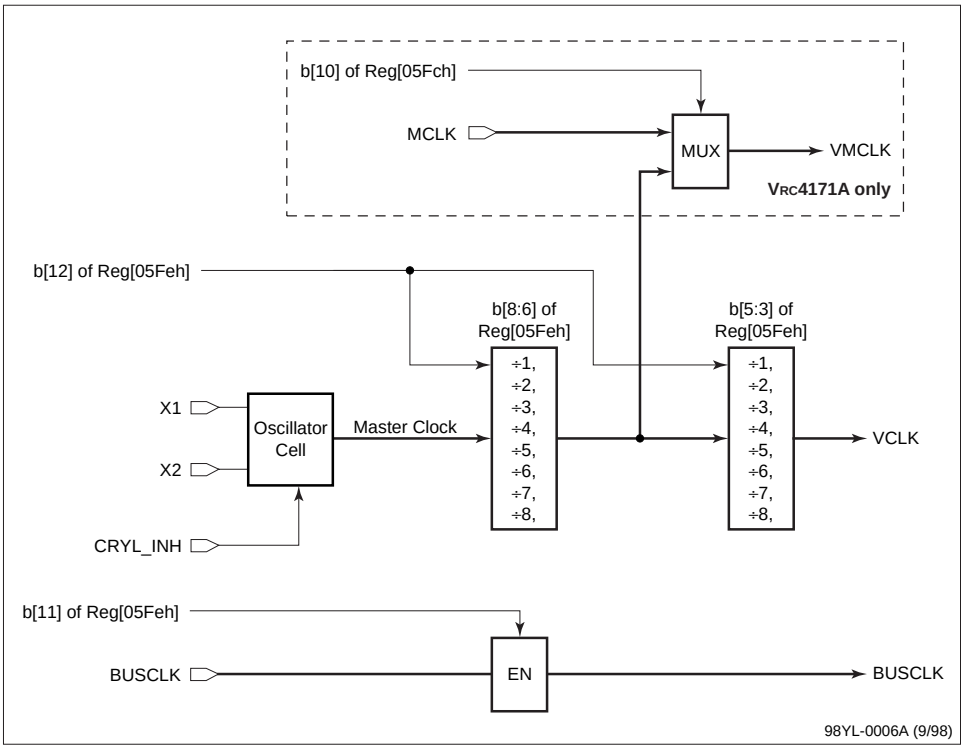
Main Clock Control 3

Figure 3-1. Internal and External Clock Control



Note: The dotted lines show the VRC4171A modification to switch (MUX) the driving source for the VMCLK output pin. This modification selects the original VMCLK signal or the new MCLK signal to output on the VMCLK pin.

Table 3-1. Main Clock Control Specifications

Clock Type	Name	Description
External	X1/X2	Crystal input to generate clocks for the display controller
	CRYL_INH	Crystal oscillation inhibit signal
	MCLK	External clock input for video memory clock
	BUSCLK	8-MHz system bus clock (actual frequency depends on bit setting inside the VR41xx CPU)
Internal	VMCLK	Video memory clock
	VCLK	Video clock

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Card Controllers 4

Two independent card controllers in the VRC4171A are designed to work with a variety of commercially available memory cards:

- 68-pin PC Card (compliant with ExCA or the PCMCIA/JEIDA release 2.1 specification)
- 50-pin CompactFlash card or 68-pin CompactFlash card with PC Card adapter
- 60-pin Miniature Card

The VRC4171A supports one or two independent card slots, depending on the configuration needed (Table 4-1). The single-slot option does not require an external buffer, whereas the dual-slot option does (Table 4-2).

- Slot A supports standard PC Cards or 68-pin CompactFlash cards with a PC Card adapter.
- Slot B supports standard PC Cards, 50-pin CompactFlash cards, or 60-pin Miniature Cards, the latter of which are restricted to flash or ROM types only. There is no support for DRAM or SRAM Miniature Cards.

Table 4-1. Card Options

Slot	Cards Supported	Conditions
A (default)	68-pin PC Card	No external buffers
	CompactFlash card with adapter	
B (optional)	68-pin PC Card	With external buffers (with or without OR gate)
	CompactFlash card with adapter	
	50-pin CompactFlash card	
	Miniature Card (flash/ROM only)	

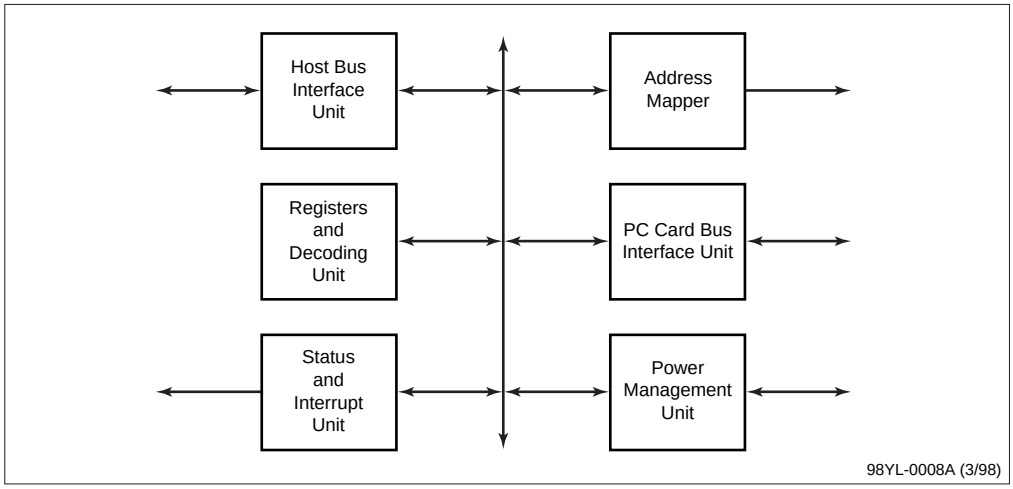
Table 4-2. Slot Requirements

Slot Configuration		
A	**B**	**Requirements**
PC Card	None	No external buffers required (with or without external OR gate)
PC Card	PC Card	Requires four external 16-bit buffers (with or without external OR gate)
PC Card	CompactFlash	Requires three external 16-bit buffers and one-half of external 4-bit buffer
PC Card	Miniature Card	Requires three external 16-bit buffers

Each card controller interfaces directly to either a synchronous or asynchronous ISA-compatible bus or equivalent (Figure 4-1). Card status information, accessible through the interface status register of each slot, includes the following types of information:

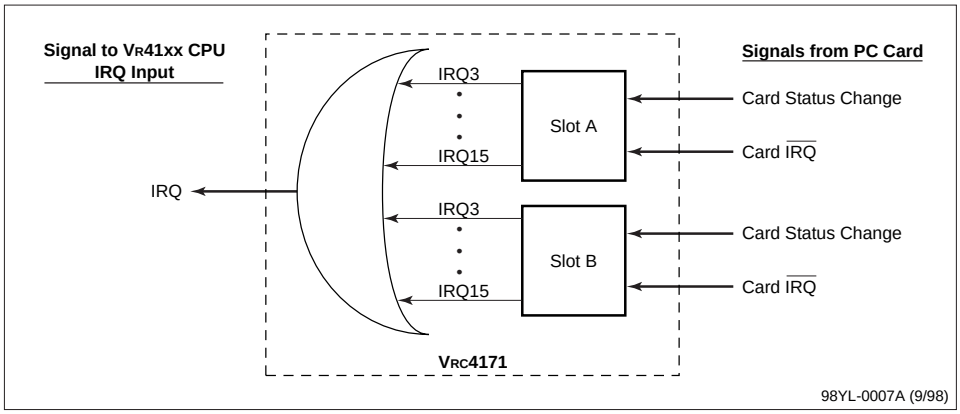
- Detection of card insertion or removal
- Memory write protect status
- Battery voltage warnings
- Power status
- Status of RDY/*BSY signal

Figure 4-1. Controller Block Diagram



A change in status—for example, when a card is inserted or removed—causes a card status change interrupt. Various interrupt sources are enabled separately and independently in each card controller to support the PC's ISA bus software legacy use of interrupts (Figure 4-2). In MIPS design, there is only one interrupt, and a large OR gate collects all of the interrupt sources into one external interrupt output pin. That single VRC4171A external IRQ output drives the system's MIPS VR4111 CPU interrupt. The Interrupt and General Control register's IRQSEL bits steer the I/O card interrupt to an internal chip IRQ line (Table 7-21). The status of these IRQ lines can be checked by reading O5FAh, the Interrupt Status register (Table 7-7).

Figure 4-2. Internal IRQ Routing



Each card controller implements power management for its own card socket via programmed options in the Power/RESETDRV Control register. Power sequencing delays specified by ExCA and PCMCIA release 2.1 are implemented in hardware.

When the memory and I/O windows are disabled and the socket is empty, each card controller automatically enters a lower-power-consuming state, the lowest level of which can be achieved by disabling all I/O and memory windows, tri-stating all output buffers, and removing power to the card socket.

When enabled for PC Card compliance, the controller operates interchangeably with two different types of PC Cards, either memory or I/O. Since the cards have different signal interface requirements, the controller incorporates multiplexers to redirect the appropriate signals (Table 4-3). These signals are configured correctly based on the setting of the CRDTYP bit in the Interrupt and General Control register. Each slot is controlled separately.

Table 4-3. GPIO/*PCS Options

A: PC Card B: None	**A: PC Card B: PC Card**	**A: PC Card B: CompactFlash**	**A: PC Card B: Miniature Card**
Up to four GPIO pins or two GPIO/*PCS pins depending on the selection (Table 2-6)	N/A	Up to two GPIO pins or two *PCS pins depending on the selection (Table 2-6)	N/A

System Memory

Each controller supports five independently enabled and controlled system memory address mapping windows, each of which may map into either the common or attribute memory space of the PC Card independently to control the following:

- Memory data bus width
- System bus wait states
- Software write protection
- Card enable control

Each controller also supports two independently enabled and controlled system I/O address mapping windows. A register provides access to the card information structure and card configuration registers within the PC Card's attribute memory, as described by the PCMCIA/ JEIDA specification.

Caution: Do not overlap memory and I/O windows. When bit IO_UADEC in the top-level Configuration register 1 is set to 0 (Table 7-5), the starting addresses of any memory window should be set to xx0600h or higher (up to 64K boundary xxFFFFh) to avoid conflict with internal register addresses. The ending memory address should not cross the 64K boundary. A good size for a memory window is 32K bytes, from xx8000h-xxFFFFh.

Access of Card Memory

Card memory is accessed if *all* of these conditions are met.

1. The system memory address mapping window is enabled.
2. The system memory address is greater than or equal to the System Memory Address Mapping Start register A[25:12].
3. The system memory address is less than or equal to the System Memory Address Mapping Stop register A[25:12].

Access of Card I/O Addresses

Card I/O addresses are accessed if *all* of these conditions are met.

1. The I/O address mapping window is enabled.
2. The system I/O address is greater than or equal to the System I/O Address Mapping Start register A[15:0]; higher order addresses A[25:16] are set at a fixed value of “0100000000.”
3. The system I/O address is less than or equal to the System I/O Address Mapping Stop register A[15:0]; higher order addresses A[25:16] are set at a fixed value of “0100000000.”
4. The setting of the IO_UADEC bit does not affect control of the I/O Address Mapping window.

System software must account for each I/O address range assigned to a particular card. The reservation of a particular I/O address range for each card can reduce card power consumption since only one card is enabled during each I/O access.

Caution: When bit IO_UADEC in Configuration register 1 is set to 0 (Table 7-5), the I/O address decoder for the top-level registers (Table 7-1) and the PC Card control registers (Table 7-2) does not include upper bits A[25:16]. It is recommended to set bit IO_UADEC to 1 with software, unless the system hardware design interface dictates no fixed decoding of upper address bits A[25:16] for a system I/O address.

CompactFlash Cards

In general, CompactFlash cards are electrically compatible with the PCMCIA ATA Standard, with minor differences that the VRC4171A handles transparently. CompactFlash cards have three modes of operation:

1. PC Card ATA using I/O modes
2. PC Card ATA using memory mode
3. True IDE mode

CompactFlash card configuration is controlled using the standard card configuration registers starting at address 200h in the attribute memory space. The second slot can be configured to support 50-pin CompactFlash cards.

Miniature Cards

The Miniature Card controller supports only the flash and ROM requirements of the Miniature Card release 1.1 specification. Support for DRAM or SRAM Miniature Cards is not provided at this time.

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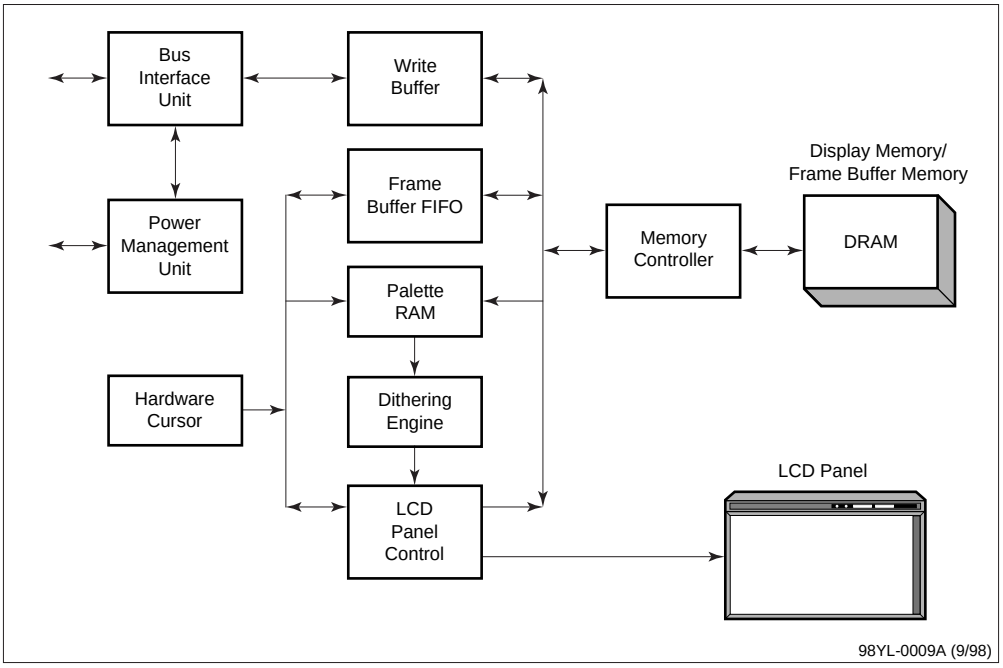
LCD Controller 5

The LCD controller is designed to work with a variety of STN and TFT color or monochrome LCD panels. It consists of the fundamental blocks shown in Figure 5-1.

Figure 5-1. LCD Block Diagram



Functional Description

1. The Bus Interface Unit (BIU) performs all handshaking between the system bus and the internal registers, memory write buffers, and power management unit.

2. The write buffer enables memory write accesses to the frame buffer to occur between the processor system bus and the frame buffer DRAM without large latencies. The write buffer is designed to match the peak bandwidth of both the processor bus and the frame buffer DRAM.

3. The frame buffer FIFO separates the data read from the frame buffer memory during an active scan. The memory controller generates the address and controls the timing and access to the DRAM.

4. The palette RAM contains the color palette used for color display (Table 5-1). It is organized as 256 addresses by 18 bits (6 bits each for red, green, and blue color).

5. The dithering engine is used for color STN panels to provide the appearance of more colors by modulating the data as it is being written to the panel during a frame of refresh.

6. The LCD panel controller functions as the timing generator for the memory read cycles to the frame buffer FIFO and the data write cycles to the LCD panel. It provides the fundamental scanning synchronization timing signals such as frame and line synchronization and retrace timing.

7. The hardware cursor function causes a 32 x 32-pixel by two-color cursor image to appear as an overlay on top of the frame buffer during display time. The hardware cursor interfaces to the memory for the cursor data and to the LCD panel control to switch the data output to the display. The hardware cursor data is stored in off-screen memory in the upper 512 bytes of the frame buffer. When displaying the pixels in the cursor area, the output from the frame buffer data is switched to the output of the cursor data

.

Table 5-1. TFT Panel Connection

Color	Pin Name	Panel Name
RED	VUD_5	RED 5 (MSB)
	VUD_4	RED 4
	VUD_3	RED 3
	VUD_2	RED 2
	VUD_1	RED 1
	VUD_0	RED 0 (LSB)
GREEN	VLD_3	GREEN 5 (MSB)
	VLD_2	GREEN 4
	VLD_1	GREEN 3
	VLD_0	GREEN 2
	VUD_7	GREEN 1
	VUD_6	GREEN 0 (LSB)
BLUE	TFTD_17	BLUE 5 (MSB)
	TFTD_16	BLUE 4
	VLD_7	BLUE 3
	VLD_6	BLUE 2
	VLD_5	BLUE 1
	VLD_4	BLUE 0 (LSB)

The graphics display data is stored in the LCD frame buffer memory and written to the frame buffer memory with a linear address. The display data is read out of the frame buffer by the LCD controller using the starting address and offset registers. This data is then clocked out to the LCD panel using a shift clock with timing based on the value in the horizontal and vertical control registers.

The pixel format used in 8-bit-per-pixel data is an address look-up table (LUT), most commonly referred to as the *color palette*. The 8-bit pixel data is used as an address into the palette RAM. For each address, a specific value of red, green, or blue is read out to the display (6 bits for each color and 18 bits total).

For formats of 5 and 6 bits per pixel, the upper used address bits are available for use as segments that make multiple simultaneous palettes available. This feature allows applications to switch palettes by reloading the on-chip palette, resulting in smoother transitions between applications that may only use a subset of the 256 color address locations available. For 1-, 2-, and 4-bit-per-pixel formats, color registers 0 through 3 are used as a pseudo-palette.

The 16-bit-per-pixel format is a direct color format. Table 5-2 shows 5-6-5 format, but a 5-5-5 format is also supported.

Table 5-2. 16-Bit 5-6-5 Pixel Format

High Byte											Low Byte				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

To map 16-bit pixel data to an 18-bit TFT panel, R0 and B0 must output logic 0 to the panel.

As shown in Table 5-3, the frame buffer origin is in the upper left of the display area.

Table 5-3. Frame Buffer Pixel Organization

Pixel 00, Pixel 01	Pixel 639
Pixel 640	
Pixel 153000	Pixel 153599

Hardware Cursor

The hardware cursor operates in all standard graphic modes and supports a 32 x 32 x 2 user-defined pattern stored in the upper 512 bytes of display memory. The cursor pattern has two bits per pixel; each bit corresponds to a plane. Table 5-4 shows the cursor display state corresponding to the value of the cursor pattern. A single cursor pattern of 32 x 32 x 2 bits occupies 256 bytes of this uppoer 512 bytes of display memory. Two patterns of hardware cursor are supported.

Table 5-4. Cursor Display State

Cursor Plane 0	Cursor Plane 1	Cursor Display State
0	0	Cursor color 0
1	0	Cursor color 1
0	1	Transparent
1	1	Invert video data

The cursor position is defined relative to the cursor offset from the top left of the display screen. Cursor position *X* is in pixels and is specified by register 22. Cursor position *Y* is in scan lines and is specified by register 24.

The cursor pattern data for cursor plane 0 and cursor plane 1 is loaded into display memory one cursor scan line at a time. For each cursor scan line, Cursor Plane 0 data (32 bits or 4 bytes) is loaded first, followed by the Cursor Plane 1 data (32 bits or 4 bytes). This loading sequence continues until all 32 scan lines have been loaded into display memory. The cursor pattern is mapped to the display memory using linear packed-pixel addressing.

NEC

Address Decoding 6

Table 6-1. Address Map

Memory Type	Starting Address	Ending Address
Display memory	0x0A000000	0x0A7FFFFF
LCD control registers	0x0A800000	0x0AFFFFFF
PC Card registers	0x15000000	0x15FFFFFF

Display memory is decoded by the LCD chip select signal. The VR41xx CPU hardware decodes the fixed address for LCD display memory. Your system design may select a different address decoding scheme to drive the VRC4171A's *LCDCS input signal on pin 82.

Access to the 16-bit LCD registers occrs when *LCDCS = 0 and A23 = 1. If the VR41xx's *LCDCS output signal is connected to the VRC4171A's *LCDCS input signal, a 16-bit CPU-style memory access of 0xAA800000-0AA80005E will read or write the 16-bit LCD Controller registers. A CPU-style memory access of 0xAA000000-0xAA1FFFFF will read or write the external 2-MB LCD display memory/.

Table 6-2. Address Decoding

Location	Address	Comment
Internal registers	Either 26 or 16 address bits, depending on the IO_UADEC setting in Configuration register I	A[25:16] set at 0100000000; can't be changed
Two I/O windows (64K range)	A[25:16]	Set at 0100000000; can't be changed (64K range)
Five memory windows (1 MB max. per window)	A[25:20], A[19:12}	Programmable by software driver; used for address decoding (1 MB max.)

NEC

Registers 7

This section contains detailed information about the VRC4171A's registers.

Table 7-1. Top-Level Register Summary (16-Bit Accesses Only)

Register Name	Address	Signal	Description
Configuration register I	05FEh		
Configuration register II	05FCh		
Interrupt Status register	05FAh		
GPIO/*PCS Control/Data register	05EEh		
	05ECh	*PCS[0]	Upper addresses A[25:16] start register
	05EAh	*PCS[0]	Lower addresses A[15:0] start register
	05E8h	*PCS[0]	Upper addresses A[25:16] stop register
	05E6h	*PCS[0]	Lower addresses A[15:0] stop register
	05E4h	*PCS[1]	Upper addresses A[25:16] start register
	05E2h	*PCS[1]	Lower addresses A[15:0] start register
	05DEh	*PCS[1]	Upper addresses A[25:16] stop register
	05DCh	*PCS[1]	Lower addresses A[15:0] stop register

Two of the PC Card Controller registers are located in the I/O address space (Table 7-2). The remaining two PC Card Controller registers are accessed through the PC Card Controller Index registers (Table 7-3).

Table 7-2. 8-Bit PC Card Register I/O Address Space

Register Name	Address
PC Card Controller Index register	03E0h
PC Card Controller Data register	03E1h

Table 7-3. 8-Bit PC Card Controller Index Register

Register Name	Slot A	Slot B
Identification and Revision register	0000h	0040h
Interface Status Register	0001h	0041h
Power and RESETDRV Control register	0002h	0042h
Interrupt and General Control register	0003h	0043h
Card Status Change register	0004h	0044h
Card Status Change Interrupt Configuration register	0005h	0045h
Address Window Enable register	0006h	0046h
I/O Control register	0007h	0047h
I/O Address 0 Start Low-Byte register	0008h	0048h
I/O Address 0 Start High-Byte register	0009h	0049h
I/O Address 0 Stop Low-Byte register	000Ah	004Ah
I/O Address 0 Stop High-Byte register	000Bh	004Bh
I/O Address 1 Start Low-Byte register	000Ch	004Ch
I/O Address 1 Start High-Byte register	000Dh	004Dh
I/O Address 1 Stop Low-Byte register	000Eh	004Eh
I/O Address 1 Stop High-Byte register	000Fh	004Fh
System Memory Address 0 Mapping Start Low-Byte register	0010h	0050h
System Memory Address 0 Mapping Start-High Byte register	0011h	0051h
System Memory Address 0 Mapping Stop Low-Byte register	0012h	0052h
System Memory Address 0 Mapping Stop High-Byte register	0013h	0053h
Card Memory Offset Address 0 Low-Byte register	0014h	0054h
Card Memory Offset Address 0 High-Byte register	0015h	0055h
Card Detect and General Control register	0016h	0056h
System Memory Address 1 Mapping Start Low-Byte register	0018h	0058h
System Memory Address 1 Mapping Start High-Byte register	0019h	0059h
System Memory Address 1 Mapping Stop Low-Byte register	001Ah	005Ah
System Memory Address 1 Mapping Stop High-Byte register	001Bh	005Bh
Card Memory Offset Address 1 Low-Byte register	001Ch	005Ch
Card Memory Offset Address 1 High-Bbyte register	001Dh	005Dh
Global Control register	001Eh	005Eh
Card Voltage Sense register	001Fh	005Fh
System Memory Address 2 Mapping Start Low-Byte register	0020h	0060h
System Memory Address 2 Mapping Start High-Byte register	0021h	0061h
System Memory Address 2 Mapping Stop Low-Byte register	0022h	0062h
System Memory Address 2 Mapping Stop High-Byte register	0023h	0063h
Card Memory Offset Address 2 Low-Byte register	0024h	0064h
Card Memory Offset Address 2 High-Byte register	0025h	0065h
System Memory Address 3 Mapping Start Low-Byte register	0028h	0068h
System Memory Address 3 Mapping Start High-Byte register	0029h	0069h
System Memory Address 3 Mapping Stop Low-Byte register	002Ah	006Ah
System Memory Address 3 Mapping Stop High-Byte register	002Bh	006Bh

Table 7-3. 8-Bit PC Card Controller Index Register (continued)

Register Name	Slot A	Slot B
Card Memory Offset Address 3 Low-Byte register	002Ch	006Ch
Card Memory Offset Address 3 High-Byte register	002Dh	006Dh
Card Voltage Select register	002Fh	006Fh
System Memory Address 4 Mapping Start Low-Byte register	0030h	0070h
System Memory Address 4 Mapping Start High-Byte register	0031h	0071h
System Memory Address 4 Mapping Stop Low-Byte register	0032h	0072h
System Memory Address 4 Mapping Stop High-Byte register	0033h	0073h
Card Memory Offset Address 4 Low-Byte register	0034h	0074h
Card Memory Offset Address 4 High-Byte register	0035h	0075h

To access a register, write the index value listed in Table 7-3 for slot A or slot B into the PC Card Controller Index register at address 03E0h with an 8-bit access only. Read or write the 8-bit PC Controller Data register at byte address 03E1h with an 8-bit access only.

Table 7-4. 16-Bit LCD Register Summary

Register Name	Address
Panel Select register	0000h
LCD Panel Control register	0002h
Power Mode Control register	0004h
MCLK Enable register	0006h
VCLK Enable register	0008h
Video FIFO / Memory Interface Control register	000Ah
Pixel Adjustment / Vertical Half register	000Ch
Reserved	000Eh
Horizontal Display Control register	0010h
Horizontal Retrace Control register	0012h
Vertical Display End Control register	0014h
Vertical Display Control register	0016h
Vertical Retrace Start Control register	0018h
Vertical Retrace End Control register	001Ah
Starting Address register	001Ch
Offset register	001Eh
Hardware Cursor Control register	0020h
Hardware Cursor X Position register	0022h
Hardware Cursor Y Position register	0024h
Hardware Cursor Color 0A register	0026h
Hardware Cursor Color 0B register	0028h
Hardware Cursor Color 1A register	002Ah
Hardware Cursor Color 1B register	002Ch
Hardware Cursor Origin register	002Eh
Reserved	0030h
Reserved	0032h

Table 7-4. 16-Bit LCD Register Summary (continued)

Register Name	Address
Reserved	0034h
Reserved	0036h
Reserved	0038h
Reserved	003Ah
Reserved	003Ch
Reserved	003Eh
RAM Write Address register	0040h
RAM Write Port 0 register	0042h
RAM Write Port 1 register	0044h
RAM Read Address register	0046h
RAM Read Port 0 register	0048h
RAM Read Port 1 register	004Ah
Reserved	004Ch
Reserved	004Eh
Scratch Pad Register 0 register	0050h
Scratch Pad Register 1 register	0052h
Reserved	0054h
Reserved	0056h
Reserved	0058h
Reserved	005Ah
Reserved	005Ch
Reserved	005Eh

Note: The registers' reset status is 0 unless specified differently. Reserved and unused bits internal to a register are left undefined. They might be left floating and not driven to a default level high or low. Do not depend on these bits returning to a repeatable value. It is advisable to mask these bits to zero with software when performing a calculation using the contents of a register containing reserved and unused bits.

Top-Level Registers

Top-level registers [05xxh] are accessed through 16-bit operations; ***byte access is not supported***. All reserved bits are set to zero upon hardware reset and should always be written to zero to ensure proper device operation.

Configuration Register I

Name	Configuration Register I
Type	Read/Write
Register Address	05FEh

Bits

D15–D14	D13	D12	D11	D10	D9	D8–D6	D5–D3	D2–D0
MFP_CONF[1:0]	EN_OR	EN_VCLK	EN_BUSCLK	Reserved	IO_UADEC	VMCLK_DIV{2:0}	VCLK_DIV[2:0]	Reserved

Table 7-5. Configuration Register 1

Bit(s)	Name	Description
D15–D14	MFP_CONF[1:0]	Configure multifunction pin functions
		Default = 0 for all bits
		11 = A: PC Card / B: Miniature Card (flash/ROM only)
		10 = A: PC Card / B: CompactFlash
		01 = A: PC Card / B: PC Card
		00 = A: PC Card / B: none
D13	EN_OR	Default = 0
		1 = Enable external OR gate for PC Card slots
		See Table 2-6 for dual-slot options.
D12	EN_VCLK	Default = 1
		1 = Enable internal VMCLK and VCLK display clocks
D11	EN_BUSCLK	Default = 0
		1 = Enable internal BUSCLK
D10	Reserved	Default = 0
D9	IO_UADEC	Default = 0
		I/O upper address decode
		0 = I/O address decode does not include upper bits A[25:16]
		1 = I/O address decode includes all upper bits A[25:16], where A[25:24] is set to “01” and A[23:16] to “00h”
		This option only affects the top-level registers and PC Card controller index and data registers. Upper addresses A[25:16] for the PC Card I/O windows are always set at “0100000000.” Upper addresses A[25:16] for memory windows are always written by software to the PC Card registers.

Table 7-5. Configuration Register 1 (continued)

D8–D6	VMCLK_DIV[2:0]	Default = 0 for all bits
		Divider from master clock to generate VMCLK
		111 = master clock divide by 8
		110 = master clock divide by 7
		101 = master clock divide by 6
		100 = master clock divide by 5
		011 = master clock divide by 4
		010 = master clock divide by 3
		001 = master clock divide by 2
		000 = master clock divide by 1
D5–D3	VCLK_DIV[2:0]	Divider from VMCLK to generate VCLK
		Default = 0 for all bits
		111 = master clock divide by 8
		110 = master clock divide by 7
		101 = master clock divide by 6
		100 = master clock divide by 5
		011 = master clock divide by 4
		010 = master clock divide by 3
		001 = master clock divide by 2
		000 = master clock divide by 1
D2–D0	Reserved	Default = 0 for all bits

Note: Refer to Figure 3-1 for information about internal and external clock control. Also refer to bit D10 in Configuration Register II.

Configuration Register II

Name	Configuration Register II
Type	Identification and Revision Register
Register Address	05FCh

Bits

D15–D12	D11	D10	D9–D4	D3–D2	D1	D0
SIL_REV	Reserved	MCLK_EN	Reserved	STBCTL[1:0]	IOCH_R1	Reserved

Table 7-6. Configuration Register II

Bits	Name	Description
D15–D12	SIL_REV	Default = 0010 (VRC4171A) and 0001 (VRC4171)
		Silicon revision # = 0010
D11	Reserved	Default = 0
D10 (VRC4171A)	MCLK_EN	Default = 0
		0 = VMCLK is used as frame buffer control clock
		1 = MCLK is used as frame buffer control clock
D9–D4	Reserved	Default = 0 for all bits
D3–D2	STBCTL[1:0]	Default = 0 for all bits
		Read strobe data hold control bits
		The VR41xx demands a 15 ns minimum data hold time. The design cannot guarantee this hold time requirement without risking data contention with next high-speed access, as in LCD cycles. These bits provide flexibility to meet this timing requirement.
		00 = no additional hold time delay for read strobes
		01 = 5–7 ns additional hold time delay for read strobes (composed of two F132 delay cells)
		10 = additional 0.5 to 1.0 LCD X1 clock delay for read strobes (no effect if LCD X1 is OFF)
		11 = 10–14 ns additional hold time delay for read strobes (composed of four F132 delay cells)
D1	IOCH_R1	Default = 0
		I/O channel ready behavior control bit
		Enables IOCHRDY signal to be actively driven to high level before it is tri-stated
		0 = open drain output (external resistor required to pull and keep this signal at high state)
		1 = driven to high level first when released before it is tri-stated. Larger external resistor can be used to maintain the high level and conserve system power during operations.
D0	Reserved	Default = 0

Interrupt Status Register

Name	Interrupt Status Register
Type	Read/Write
Register Address	05Fah

Bits

D15	D14	D13	D12	D11	D10	D9	D8
IRQ[15]	IRQ[14]	Reserved	IRQ[12]	IRQ[11]	IRQ[10]	IRQ[9]	Reserved
D7	D6	D5	D4	D3	D2	D1	D0
IRQ[7]	Reserved	IRQ[5]	IRQ[4]	IRQ[3]	IRQ_A	IRQ_B	Reserved

Table 7-7. Interrupt Status Register

Bit(s)	Name	Description
D15–D14	IRQ[15:14]	Default = 0 for all bits
		Status of interrupt request 15 and 14
		1 = valid
D13	Reserved	Default = 0
D12–D9	IRQ[12:9]	Default = 0 for all bits
		Status of interrupt request 12, 11, 10, and 9
		1 = valid
D8	Reserved	Default = 0
D7	IRQ[7]	Default = 0
		Status of interrupt request 7
		1 = valid
D6	Reserved	Default = 0
D5–D3	IRQ[5:3]	Default = 0 for all bits
		Status of interrupt request 5, 4, and 3
		1 = valid
D2	IRQ_B	Default = 0
		Indication of where interrupt request is generated if any of above D[15:3] bits contain a 1
		1 = from PC Card Slot B
D1	IRQ_A	Default = 0
		Indication of where interrupt request is generated if any of above D[15:3] bits contain a 1
		1 = from PC Card slot A
D0	Reserved	Default = 0

Note: All IRQs are ORed together to produce one IRQ output signal at pin 87. This register is read first to determine which interrupt activated the IRQ line. Refer to Figure 4-2.

*GPIO/*PCS Control/Data Register*

Name	GPIO/*PCS Control/Data Register
Type	Read/Write
Register Address	05EEh

Bits

D15	D14	D13–D12		D11–D10		D9	D8
EN_PCS1	EN_PCS0	PCS1_CTL[1:0]		PCS0_CTL[1:0]		Reserved	Reserved
D7	D6	D5	D4	D3	D2	D1	D0
GPIO_DIR3	GPIO_DIR2	GPIO_DIR1	GPIO_DIR0	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_DAT0

Table 7-8. GPIO/*PCS Control/Data Register

Bit(s)	Name	Description
D15	EN_PCS1	Default = 0
		1 = enable *PCS[1] function
D14	EN_PCS0	Default = 0
		1 = enable *PCS[0] function
D13-D12	PCS1_CTL[1:0]	Default = 0 all bits
		00 = *PCS1 generated when incoming addresses match the defined address range
		01 = *PCS1 generated only at negative BUSCLK edges when incoming addresses match the defined address range
		10 = *PCS1 generated only at positive BUSCLK edges when incoming addresses match the defined address range
		11 = condition not allowed
D11-D10	PCS0_CTL[1:0]	Default = 0 all bits
		00 = *PCS0 generated when incoming addresses match the defined address range
		01 = *PCS0 generated only at negative BUSCLK edges when incoming addresses match the defined address range
		10 = *PCS0 generated only at positive BUSCLK edges when incoming addresses match the defined address range
		11 = condition not allowed
D9-D8	Reserved	Default = 0
D7	GPIO_DIR3	Default = 0
		0 = input mode for GPIO[3] pin
		1 = output mode for GPIO[3] pin
D6	GPIO_DIR2	Default = 0
		0 = input mode for GPIO[2] pin
		1 = output mode for GPIO[2] pin
D5	GPIO_DIR1	Default = 0
		0 = input mode for GPIO[1] pin
		1 = output mode for GPIO[1] pin

*Table 7-8. GPIO/*PCS Control/Data Register (continued)*

D4	GPIO_DIR0	Default = 0
		0 = input mode for GPIO[0] pin
		1 = output mode for GPIO[0] pin
D3	GPIO_DAT3	Default = 0
		Data value for GPIO[3] pin
D2	GPIO_DAT2	Default = 0
		Data value for GPIO[2] pin
D1	GPIO_DAT1	Default = 0
		Data value for GPIO[1] pin
D0	GPIO_DAT0	Default = 0
		Data value for GPIO[0] pin

Programmable Chip Select (PCS) Function

*PCS1 and *PCS0 are independent functions controlled by bits D13–D10 of the GPIO/*PCS control/data register [05EEh]. To enable *PCS:

1. Set b[15:14] of Configuration Register I to either “01” or “10.”
2. Set b[15] of GPIO/*PCS Control/Data Register to “1” to enable *PCS[1].
3. Set b[14] of GPIO/*PCS Control/Data Register to “1” to enable *PCS[0].
4. Define the address ranges to be decoded in each of these registers:
   - Starting/stopping addresses for *PCS[0]: 05ECh, 05EAh, and 05E8h registers
   - Starting/stopping addresses for *PCS[1]: 05E6h, 05E4h, and 05E2h registers

Note: Writing 0s to starting address bits and 1s to stopping address bits indicates that all address values are accepted (effectively a “don't care” situation).

There are three ways to control *PCS signal behavior:

1. Straight address decoding
2. Qualified by positive BUSCLK edge after address decoding
3. Qualified by negative BUSCLK edge after address decoding

Table 7-9. *PCS Options

D13	D12	D11	D10	Description
0	0	0	0	*PCS1 signal is generated whenever an address match corresponds to its window
				*PCS0 signal is generated whenever an address match corresponds to its window
1	0	0	0	*PCS1 signal is generated at positive BUSCLK edge whenever an address match corresponds to its window
				PCS0 signal is generated whenever an address match, regardless of BUSCLK edges, corresponds to its window
0	1	0	0	PCS1 signal is generated at negative BUSCLK edge whenever an address match corresponds to its window
				PCS0 signal is generated whenever an address match, regardless of BUSCLK edges, corresponds to its window
0	0	1	0	PCS1 signal is generated whenever an address match, regardless of BUSCLK edges, corresponds to its window
				PCS0 signal is generated at positive BUSCLK edge whenever an address match corresponds to its window
0	0	0	1	PCS1 signal is generated whenever an address match, regardless of BUSCLK edges, corresponds to its window
				PCS0 signal is generated at negative BUSCLK edge whenever an address match corresponds to its window

*PCS[0] Upper Starting Address A[25:16] Register

Name	*PCS[0] Upper Starting Address A[25:16] Register
Type	Read/Write
Register Address	05ECh

Bits

D15–D10	D9–D8	D7–D0
Reserved	PCS0_STARTA[25:24]	PCS0_STARTA[23:16]

Table 7-10. *PCS[0] Upper Starting Address A[25:16] Register

Bits	Name	Description
D15–D10	Reserved	Default = 0 for all bits
D9–D0	PCS0_STARTA[25:16]	Default = 0 for all bits
		Programmable chip select starting address value

*PCS[0] Lower Starting Address A[15:0] Register

Name	*PCS[0] Lower Starting Address A[15:0] Register
Type	Read/Write
Register Address	05EAh

Bits

D15–D0
PCS0_STARTA[15:0]

*Table 7-11. *PCS[0] Lower Starting Address A[15:0] Register*

Bits	Name	Description
D15–D0	PCS0_STARTA[15:0]	Default = 0 for all bits
		Programmable chip select starting address value

*PCS[0] Upper Stopping Address A[25:16] Register

Name	*PCS[0] Upper Stopping Address A[25:16] Register
Type	Read/Write
Register Address	05E8h

Bits

D15–D10	D9–D8	D7–D0
Reserved	PCS0_STOPA[25:24]	PCS0_STOPA[23:16]

*Table 7-12. *PCS[0] Upper Stopping Address A[25:16] Register*

Bits	Name	Description
D15–D10	Reserved	Default = 0 for all bits
D9–D0	PCS0_STOPA[25:16]	Default = 0 for all bits
		Programmable chip select stopping address value

*PCS[0] Lower Stopping Address A[15:0] Register

Name	*PCS[0] Lower Stopping Address A[15:0] Register
Type	Read/Write
Register Address	05E6h

Bits

D15–D0
PCS0_STOPA[15:0]

*Table 7-13. *PCS[0] Lower Stopping Address A[15:0] Register*

Bits	Name	Description
D15–D0	PCS0_STOPA[15:0]	Default = 0 for all bits
		Programmable chip select stopping address value

*PCS[1] Upper Starting Address A[25:16] Register

Name	*PCS[1] Upper Starting Address A[25:16] Register
Type	Read/Write
Register Address	05E4h

Bits

D15–D10	D9–D8	D7–D0
Reserved	PCS1_STARTA[25:24]	PCS1_STARTA[23:16]

Table 7-14. *PCS[1] Upper Starting Address A[25:16] Register

Bits	Name	Description
D15–D10	Reserved	Default = 0 for all bits
D9–D0	PCS1_STARTA[25:16]	Default = 0 for all bits
		Programmable chip select starting address value

*PCS[1] Lower Starting Address A[15:0] Register

Name	*PCS[1] Lower Starting Address A[15:0] Register
Type	Read/Write
Register Address	05E2h

Bits

D15–D0
PCS1_STARTA[15:0]

Table 7-15. *PCS[1] Lower Starting Address A[15:0] Register

Bits	Name	Description
D15–D0	PCS1_STARTA[15:0]	Default = 0 for all bits
		Programmable chip select starting address value

*PCS[1] Upper Stopping Address A[25:16] Register

Name	*PCS[1] Upper Stopping Address A[25:16] Register
Type	Read/Write
Register Address	05DEh

Bits

D15–D10	D9–D8	D7–D0
Reserved	PCS1_STOPA[25:24]	PCS1_STOPA[23:16]

*Table 7-16. *PCS[1] Upper Stopping Address A[25:16] Register*

Bits	Name	Description
D15–D10	Reserved	Default = 0 for all bits
D9–D0	PCS1_STOPA[25:16]	Default = 0 for all bits
		Programmable chip select stopping address value

*PCS[1] Lower Stopping Address A[15:0] Register

Name	*PCS[1] Lower Stopping Address A[15:0] Register
Type	Read/Write
Register Address	05DCh

Bits

D15–D0
PCS1_STOPA[15:0]

*Table 7-17. *PCS[1] Lower Stopping Address A[15:0] Register*

Bit(s)	Name	Description
D15–D0	PCS1_STOPA [15:0]	Default = 0 for all bits
		Programmable chip select stopping address for A[15:0] bits

PC Card Registers

Identification and Revision Register

Name	Identification and Revision Register
Type	Read only
Register Address (Slot A)	Index Base + 00h
Register Address (Slot B)	Index Base + 40h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
IFTYP1	IFTYP0	Reserved	Reserved	REV3	REV2	REV1	REV0

Table 7-18. Identification and Revision Register

Bit(s)	Name	Description
D7–D6	IFTYP[1:0]	Default = 10
		PC Card controller interface type bits
		Read back as “10” to reflect support for both memory and I/O cards
D5–D4	Reserved	Default = 0 for all bits
		Read back as zero
D3–D0	Revision #	Default = 0011
		These bits identify the revision level of the PC Card controller, where the revision code is 0011.

Interface Status Register

Name	Interface Status Register
Type	Read only
Register Address (Slot A)	Index Base + 01h
Register Address (Slot B)	Index Base + 41h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	PWRON	RDY/*BSY	WP	CD2	CD1	BVD2	BVD1

Table 7-19. Interface Status Register

Bit(s)	Name	Description		
D7	Reserved	Default = 1		
D6	PWRON	Default = 0		
		PC Card power status bit		
		0 = power to the socket is off		
		*VCCEN[1:0] = 11		
		VPPEN{1:0] = 00 (indicating no power applied to the socket)		
		1 = power to socket is on		
		*VCCEN[1:0] and VPPEN{1:0] set to bit D[1:0] of Power and RESET-DRV Control registers [Index 02h for Slot A and 42h for Slot B]		
D5	RDY/*BSY	Default = x		
		Ready/Busy bit		
		0 = PC Card is busy		
		1 = PC Card is ready		
D4	WP	Default = x		
		Memory Write Protect status bit		
		Logic level of the WP signal on the memory PC Card interface		
		0 = PC Card write protect switch is off		
		1 = PC Card write protect switch is on		
D3–D2	CD[2:1]	Default = x for all bits		
		Card Detect status bits		
		Complement of the values of *CD[2:1] on the PC Card interface. Bit is set to “1” if corresponding *CD is active and reset to “0” if inactive.		
D1–D0	BVD[2:1]	Default = x for all bits		
		Battery Voltage Detect status bits		
		For I/O PC Cards, bit D[0] indicates current status of *STSCHG/*RI signal from PC Card. Values of BVD[2:1] for memory PC Cards are:		
		BVD2	**BVD1**	**Condition**
		0	0	Battery Dead
		0	1	Warning
		1	0	Battery Dead
		1	1	Battery Good

Note: In Miniature Card application (slot B only), D[4:0] are reserved (default = 0 for all bits).

Power and RESETDRV Control Register

Name	Power and RESETDRV Control Register
Type	Read/Write
Register Address (Slot A)	Index Base + 02h
Register Address (Slot B)	Index Base + 42h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
OE	Reserved	Reserved	WPREN	Reserved	Reserved	VPPSEL1	VPPSEL0

Table 7-20. Power and RESETDRV Control Register

Bit(s)	Name	Description		
D7	OE	Default = 0		
		Output enable control bit		
		Resets to default every time a card is removed from the socket		
		If bit is cleared to zero, the PC Card outputs from the VRC4171A and CA[25:0], *CE[2;1], *_IOR, *_IOW, *_OE, *_WE, *_REG and _RESET are driven to high impedance.		
		*_ENBUF and *_DBUFEN output signals are driven to 1 if dual-slot mode is selected.		
		Warning: To prevent an unnecessary power surge or potential device latch-up problem while power is applied to the PC Card, OE and PWREN [D4] must not be set at the same time. The delay to set this bit depends on the time it takes for the power to establish a steady state. The recommended minimum delay is >10 ms.		
D6-D5	Reserved	Default = 0		
D4	PWREN	Default = 0		
		PC Card Power Enable bit		
		Resets to default state every time a card is removed from the socket		
		0 = Power to the socket disabled		
		*VCCEN[1:0] output pins are held at 1 to indicate inactive states.		
		VPPEN[1:0] output pins are held at 0 to indicate no connection or grounded.		
		1 = Voltage selected according to Card Voltage Select registers (2Fh or 6Fh). Power to the socket is turned ON when a card is inserted and OFF when a card is removed.		
D3–D2	Reserved	Default = 0 for all bits		
D1–D0	VPPSEL[1:0]	Default = 0 for all bits		
		PC Card VPP Power Control Select bits		
		Resets to default state every time a card is removed from the socket		
		D[1:0]	**Function**	**VPPEN[1:0] Status**
		00	No connect or grounded	00
		01	VPP get VCC	01
		10	VPP get VCC	10
		11	No connect or grounded	00

Note: In Miniature Card application (slot B only), D[3:0] are reserved (default = 0 for all bits).

Interrupt and General Control Register

.

Name	Interrupt and General Control Register
Type	Read/Write
Register Address (Slot A)	Index Base + 03h
Register Address (Slot B)	Index Base + 43h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RI_EN	CRDRST	CRDTYP	Reserved	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0

Table 7-21. Interrupt and General Control Register

Bit(s)	Name	Description			
D7	RI_EN	Default = 0			
		Ring Indicate enable bit			
		Resets to default state every time a card is removed from socket			
		0 = *STSCHG/*RI signal from the I/O PC Card is used as the status change signal *STSCHG. Current status of the signal can be read from the Interface Status register and configured as a source for the card status change interrupt.			
		1 = *STSCHG/*RI signal from the I/O PC Card serves as a ring indicator (RI) signal passed through *RIO to enable system resume if the PC Card RI signal is valid. (No function for memory PC Cards.)			
D6	CRDRST	Default = 0			
		PC Card reset bit (software reset)			
		0 = Activates RESET signal to PC Card; stays active until set to “1”			
		1 = Deactivates RESET signal to PC Card			
D5	CRDTYP	Default = 0			
		PC Card Type bit			
		Resets to default state every time a card is removed from socket			
		0 = configure socket interface to memory type only			
		1 = configure socket interface to I/O and memory types			
D4	Reserved	Default = 0			
D3-D0	IRQSEL	Default = 0011			
		IRQ Level Selection bits (I/O cards only)			
		Resets to default state every time a card is removed from socket			
		IRQSEL[3:0]	**IRQ**	**IRQSEL[3:0]**	**IRQ**
		0000	Not selected	1000	Reserved
		0001	Reserved	1001	IRQ9 enabled
		0010	Reserved	1010	IRQ10 enabled
		0011	IRQ3 enabled	1011	IRQ11 enabled
		0100	IRQ4 enabled	1100	IRQ12 enabled
		0101	IRQ5 enabled	1101	Reserved
		0110	Reserved	1110	IRQ14 enabled
		0111	IRQ7 enabled	1111	IRQ15 enabled

Note: For Miniature Card option (slot B only), D[7] and D[5:0] are reserved (default = 0 for all bits).

Card Status Change Register

.

Name	Card Status Change Register
Type	Read-Only
Register Address (Slot A)	Index Base + 04h
Register Address (Slot B)	Index Base + 44h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	CD_CHG	RDY_CHG	BAT_WARN	BAT_DEAD

Table 7-22. Card Status Change Register

Bit(s)	Name	Description
D7–D4	Reserved	Default = 0 for all bits
D3	CD_CHG	Default = 0
		Card change status bit
		0 = no change detected on either of *CD[2:1]
		1 = change detected on *CD[2:1]
D2	RDY_CHG	Default = 0
		Ready change bit
		0 = no change detected on RDY/*BSY, or I/O PC Card installed
		1 = low-to-high change is detected on RDY/*BSY, indicating that the memory PC Card is ready to accept a new data transfer
D1	BAT_WARN	Default = 0
		Battery Warning bit
		0 = No battery warning condition, or I/O PC Card installed
		1 = A battery warning condition has been detected
D0	BAT_DEAD	Default = 0
		Battery Dead / STSCHG bit
		0 = Battery good condition for memory PC Cards. For I/O PC Cards, the RI enable bit of the Interrupt and General Control Register is set to "1", or *STSCHG/*RI is high.
		1 = Battery dead condition detected for memory PC Cards. For I/O PC Cards, the RI enable bit of the Interrupt and General Control Register is reset to “0” and the *STSCHG/*RI signal from the I/O PC Card pulled low. The system software must then read the PC Card Status Change register to determine the cause of *STSCHG.

Notes:
1. This register provides the source of the card status change interrupt. Each source can be enabled by setting the corresponding bit in the Card Status Change Interrupt Configuration register. The bits in this register are read back as zero if their corresponding enable bits are reset to zero.
2. If EXWRBK in the Global Control register is set to “1,” the acknowledgment of sources for the card status change interrupt is done by writing back a “1” to the appropriate bit in the Card Status Change register. Once acknowledged, that particular bit is read back as zero. If enabled on a system IRQ line, the interrupt signal caused by the card status change is active until all bits in this register are 0.
3. If the EXWRBK bit is set to “0,” the card status change interrupt, when enabled on an IRQ line, will remain active until this register is read. In this mode, reading this register resets to zero all status bits set to “1.”
4. For Miniature Card application (Slot B only), D[1:0] are treated as reserved bits.

Card Status Change Interrupt Configuration Register

Name	Card Status Change Interrupt Configuration Register
Type	Read/Write
Register Address (Slot A)	Index Base + 05h
Register Address (Slot B)	Index Base + 45h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SIRQS3	SIRQS2	SIRQS1	SIRQS0	CD_EN	RDY_EN	BWARN_EN	BDEAD_EN

Table 7-23. Card Status Change Interrupt Configuration Register

Bit(s)	Name	Description			
D7-D4	SIRQ[3:0]	Default = 0 for all bits			
		Interrupt steering selection bits for the card status change interrupt			
		IRQSEL[3:0]	**IRQ**	**IRQSEL[3:0]**	**IRQ**
		0000	Not selected	1000	Reserved
		0001	Reserved	1001	IRQ9 enabled
		0010	Reserved	1010	IRQ10 enabled
		0011	IRQ3 enabled	1011	IRQ11 enabled
		0100	IRQ4 enabled	1100	IRQ12 enabled
		0101	IRQ5 enabled	1101	Reserved
		0110	Reserved	1110	IRQ14 enabled
		0111	IRQ7 enabled	1111	IRQ15 enabled
D3	CD_EN	Default = 0			
		Card Detect Enable bit			
		0 = Disables the card status change interrupt when the card detection signals change state			
		1 = Enables a card status change interrupt when a change is detected on the *CD1/2 signals			
D2	RDY_EN	Default = 0			
		Ready Enable bit			
		0 = Disables the card status change interrupt when a low-to-high transition is detected on the RDY/*BSY signal			
		1 = Enables a card status change interrupt when a low-to-high transition is detected on the RDY/*BSY signal			
D1	BWARN_EN	Default = 0			
		Battery Warning Enable bit (memory PC Cards only)			
		0 = Disables the card status change interrupt when a battery warning condition is detected			
		1 = Enables a card status change interrupt when a battery warning condition is detected			

Table 7-23. Card Status Change Interrupt Configuration Register (continued)

D0	BDEAD_EN	Default = 0
		Battery Dead Enable /*STSCHG bit
		0 = Disables the card status change interrupt when a battery dead condition (memory card) or active *STSCHG (I/O card) is detected
		1 = For memory PC Cards, enables a card status change interrupt when a battery dead condition is detected. For I/O PC Cards, enables a card status change interrupt if *STSCHG/*RI is pulled low by the I/O PC Card (assuming that the RI enable bit of the Interrupt and General Control register is cleared to 0).

Note: For Miniature Card application (Slot B only), D[1:0] are reserved (default = 0 for all bits).

Address Window Enable Register

Name	Address Window Enable Register
Type	Read/Write
Register Address (Slot A)	Index Base + 06h
Register Address (Slot B)	Index Base + 46h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
IOWEN1	IOWEN0	Reserved	MWEN4	MWEN3	MWEN2	MWEN1	MWEN0

Table 7-24. Address Window Enable Register

Bit(s)	Name	Description
D7–D6	IOWEN[1:0]	Default = 0 for all bits
		I/O Window Enable bits
		Automatically resets to default state every time a card is removed from the socket. The start and stop register pairs must all be set to the desired window values before setting these bits to "1."
		0 = Inhibits the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window
		1 = Generates the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card.
D5	Reserved	Default = 0
D4–D0	MWEN[4:0]	Default = 0 for all bits
		Memory Window Enable bits
		Automatically resets to default state every time a card is removed from the socket. The start, stop, and offset register pairs must all be set to the desired window values before setting these bits to "1."
		0 = Inhibits the card enable signals to the PC Card when a memory access occurs within the corresponding memory address window.
		1 = Generates the card enable signals to the PC Card when a memory access occurs within the corresponding memory address window. When the system address is within the window, the computed address is generated to the PC Card.

Note: For Miniature Card application (Slot B only), D[7:6] are reserved (default = 0 for all bits).

I/O Control Register

.

Name	I/O Control Register
Type	Read/Write
Register Address (Slot A)	Index Base + 07h
Register Address (Slot B)	Index Base + 47h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	W1_IOWS	IO1_CS16MD	IO1DSZ	Reserved	W0_IOWS	IO0_CS16MD	IO0DSZ

Table 7-25. I/O Control Register

Bit(s)	Name	Description
D7	Reserved	Default = 0
D6	W1_IOWS	Default = 0
		I/O Window_1 Wait State setting bit
		8-bit cycles: 0 = 3 wait states added to cycles initiated by VR41xx
		1 = 1 additional wait state added (resulting in 4 total wait states)
		16-bit cycles: 0 = no wait states added to cycles initiated by VR41xx
		1 = 1 additional wait state will be added
D5	O1_CS16MD	Default = 0
		I/O Window_1 IOCS16 source bit
		0 = IOCS16 generated based on the value of the data size bit
		1 = IOCS16 generated based on IOCS16 signal returned from PC Card
D4	IO1DSZ	Default = 0
		I/O Window_1 Data Size bit
		0 = 8-bit I/O data path
		1 = 16-bit I/O data path
D3	Reserved	Default = 0
D2	W0_IOWS	Default = 0
		I/O Window_0 Wait State setting bit
		8-bit cycles: 0 = 3 wait states added to cycles initiated by VR41xx
		1 = 1 additional wait state added (resulting in 4 total wait states)
		16-bit cycles: 0 = no wait states added to cycles initiated by VR41xx
		1 = 1 additional wait state added
D1	IO0_CS16MD	Default = 0
		I/O Window_0 *IOCS16 Source bit
		0 = *IOCS16 generated based on the value of the data size bit
		1 = *IOCS16 generated based on *IOIS16 signal returned from PC Card
D0	IO0DSZ	Default = 0
		I/O Window_0 Data Size bit
		0 = 8-bit I/O data path
		1 = 16-bit I/O data path

Note: For Miniature Card application (Slot B only), D[7], D [5:3], and D [1:0] are reserved (default = 0 for all bits).

I/O Address Start Low-Byte Register

Name	I/O Address Start Low-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 08h Window 1: Index Base + 0Ch
Register Address (Slot B)	Window 0: Index Base + 48h Window 1: Index Base + 4Ch

Bits

D7	D6	D5	D4	D3	D2	D1	D0
STARTAL7	STARTAL6	STARTAL5	STARTAL4	STARTAL3	STARTAL2	STARTAL1	STARTAL0

Table 7-26. I/O Address Start Low-Byte Register

Bit(s)	Name	Description
D7–D0	STARTAL[7:0]	Default = 0 for all bits
		I/O Window Start Low Address A[7:0]

Note: For Miniature Card application (Slot B only), D[7:0] are reserved (default = 0 for all bits).

I/O Address Start High-Byte Register

.

Name	I/O Address Start High-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 09h
	Window 1: Index Base + 0Dh
Register Address (Slot B)	Window 0: Index Base + 49h
	Window 1: Index Base + 4Dh

Bits

D7	D6	D5	D4	D3	D2	D1	D0
STARTAH15	STARTAH14	STARTAH13	STARTAH12	STARTAH11	STARTAH10	STARTAH9	STARTAH8

Table 7-27. I/O Address Start High-Byte Register

Bit(s)	Name	Description
D7–D0	STARTAH [15:8]	Default = 0 for all bits
		I/O Window Start High Address A[15:8]

Note: For Miniature Card application (Slot B only), D[7:0] are reserved (default = 0 for all bits).

I/O Address Stop Low-Byte Register

Name	I/O Address Stop Low-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 0Ah
	Window 1: Index Base + 0Eh
Register Address (Slot B)	Window 0: Index Base + 4Ah
	Window 1: Index Base + 4Eh

Bits

D7	D6	D5	D4	D3	D2	D1	D0
STOPAL7	STOPAL6	STOPAL5	STOPAL4	STOPAL3	STOPAL2	STOPAL71	STOPAL0

Table 7-28. I/O Address Stop Low-Byte Register

Bit(s)	Name	Description
D7–D0	STOPAL[7:0]	Default = 0 for all bits
		I/O Window Stop Low Address A[7:0]

Note: For Miniature Card application (Slot B only), D[7:0] are reserved (default = 0 for all bits).

I/O Address Stop High-Byte Register

Name	I/O Address Stop High-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 0Bh
	Window 1: Index Base + 0Fh
Register Address (Slot B)	Window 0: Index Base + 4Bh
	Window 1: Index Base + 4Fh

Bits

D7	D6	D5	D4	D3	D2	D1	D0
STOPAH15	STOPAH14	STOPAH13	STOPAH12	STOPAH11	STOPAH10	STOPAH9	STOPAH8

Table 7-29. I/O Address Stop High-Byte Register

Bit(s)	Name	Description
D7–D0	STOPAH [15:8]	Default = 0 for all bits
		I/O Window Stop High Address A[15:8]

Note: For Miniature Card application (Slot B only): D[7:0] are reserved (default = 0 for all bits).

System Memory Address Mapping Start Low-Byte Register

.

Name	System Memory Address Mapping Start Low-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 10h
	Window 1: Index Base + 18h
	Window 2: Index Base + 20h
	Window 3: Index Base + 28h
	Window 4: Index Base + 30h
Register Address (Slot B)	Window 0: Index Base + 50h
	Window 1: Index Base + 58h
	Window 2: Index Base + 60h
	Window 3: Index Base + 68h
	Window 4: Index Base + 70h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MWSTARTA7	MWSTARTA6	MWSTARTA5	MWSTARTA4	MWSTARTA3	MWSTARTA2	MWSTARTA1	MWSTARTA0

Figure 7-1. Address Map

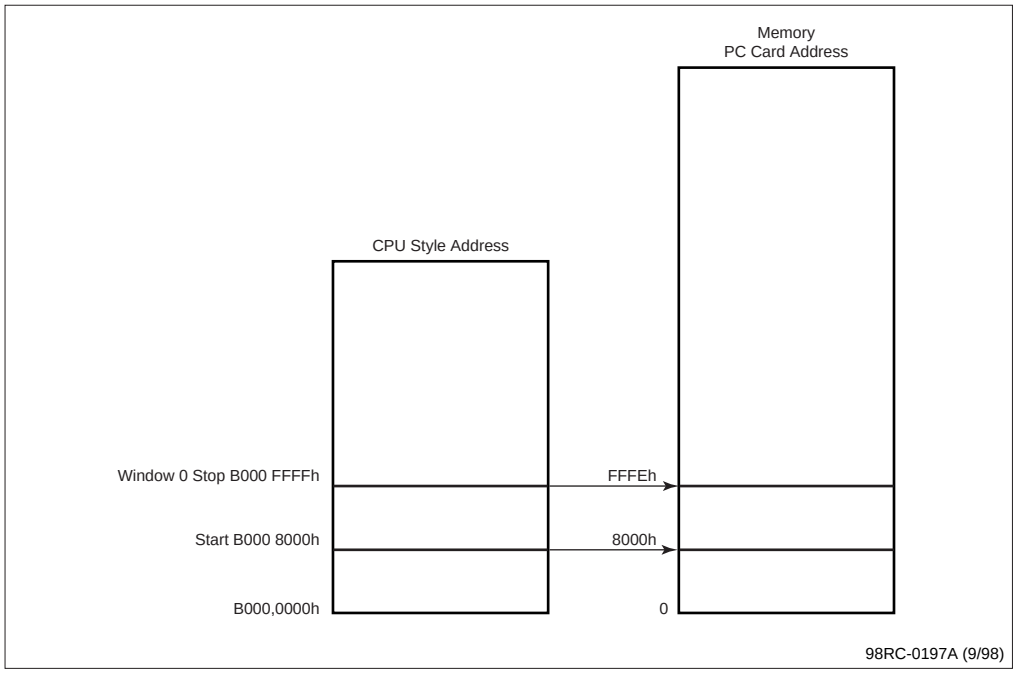


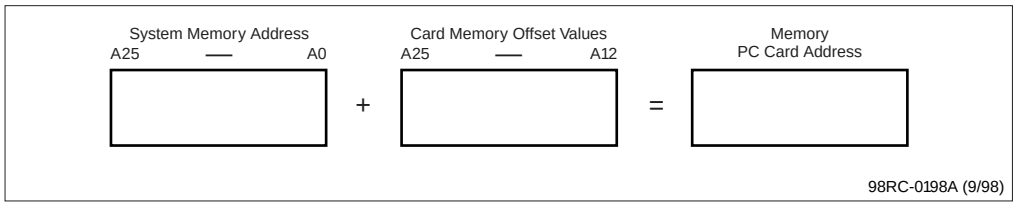
Table 7-30. System Memory Address Mapping Start Low-Byte Register

Bit(s)	Name	Description
D7–D0	MWSTARTA[7:0]	Default = 0 for all bits
		Memory Window Start Address A[19:12] that provides a minimum memory mapping window of 4K

Card memory offset address value 0000h accesses PC Card memory ranging from 32K to 64K.

To access a range from 0 to 32K, set the card memory offset address value to a negative value (offset). For example, A25–A12 = 3FF8h. 3FF800h + 8000h = 4000000. Overflow bit A26 is discarded, resulting in a PC Card address of 0000000. Set a positive value (offset) in the card memory offset address value to achieve positive (higher) PC Card memory access ranges. In other words, the system memory address (A25-A0) + PC Card memory offset values (A25-A12) = the PC Card memory access address.

Figure 7-2.



System Memory Address Mapping Start High-Byte Register

Name	System Memory Address Mapping Start High-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 11H
	Window 1: Index Base + 19H
	Window 2: Index Base + 21H
	Window 3: Index Base + 29H
	Window 4: Index Base + 31H
Register Address (Slot B)	Window 0: Index Base + 51H
	Window 1: Index Base + 59H
	Window 2: Index Base + 61H
	Window 3: Index Base + 69H
	Window 4: Index Base + 71H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
DSIZ	Reserved	MWST_A25	MWST_A24	MWST_A23	MWST_A22	MWST_A21	MWST_A20

Table 7-31. System Memory Address Mapping Start High-Byte Register

Bit(s)	Name	Description
D7	DSIZ	Default = 0
		PC Card Memory Data Width bit
		0 = 8-bit memory data path
		1 = 16-bit memory data path
D6–D0 (rev_1.x)	Reserved	Default = 0 for all bits
D6 (rev_2.0)	Reserved	Default = 0
D5–D0 (rev_2.0)	MWST_A[25:20]	Default = 0 for all bits
		System Memory Window Start Address A[25:20]
		High-order address bits used to determine the start address of the corresponding system memory address mapping window

System Memory Address Mapping Stop Low-Byte Register

Name	System Memory Address Mapping Stop Low-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 12h
	Window 1: Index Base + 1Ah
	Window 2: Index Base + 22h
	Window 3: Index Base + 2Ah
	Window 4: Index Base + 32h
Register Address (Slot B)	Window 0: Index Base + 52h
	Window 1: Index Base + 5Ah
	Window 2: Index Base + 62h
	Window 3: Index Base + 6Ah
	Window 4: Index Base + 72h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MWSTOPA19	MWSTOPA18	MWSTOPA17	MWSTOPA16	MWSTOPA15	MWSTOPA14	MWSTOPA13	MWSTOPA12

Table 7-32. System Memory Address Mapping Stop Low-Byte Register

Bit(s)	Name	Description
D7–D0	MWSTOPA [19:12]	Default = 0 for all bits
		Memory Window Stop Address A[19:12]

System Memory Address Mapping Stop High-Byte Register

Name	System Memory Address Mapping Stop High-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 13h
	Window 1: Index Base + 1Bh
	Window 2: Index Base + 23h
	Window 3: Index Base + 2Bh
	Window 4: Index Base + 33h
Register Address (Slot B)	Window 0: Index Base + 53h
	Window 1: Index Base + 5Bh
	Window 2: Index Base + 63h
	Window 3: Index Base + 6Bh
	Window 4: Index Base + 73h

Bits

D7	D6	D5	D4	D3	D2	D1	D0
M16W1	M16W0	MWSP_A25	MWSP_A24	MWSP_A23	MWSP_A22	MWSP_A21	MWSP_A20

Table 7-33. System Memory Address Mapping Stop High-Byte Register

Bit(s)	Name	Description		
D7–D6	M16W[1:0]	Default = 0 for all bits		
		Wait state select bit for 16-bit memory accesses		
		These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the WAIT signal, wait states are generated by the PC Card asserting the WAIT signal.		
		D[7]	**D[6]**	**16-bit Memory Wait States**
		0	0	Standard 16-bit cycle
		0	1	1 additional wait state
		1	0	2 additional wait states
		1	1	3 additional wait states
D5–D0	MWSP_A[25:20]	Default = 0 for all bits		
		System Memory Window Stop Address A[25:20]		
		High-order address bits used to determine the stop address of the corresponding system memory address mapping window		

Card Memory Offset Address Low-Byte Register

Name	Card Memory Offset Address Low-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 14H
	Window 1: Index Base + 1CH
	Window 2: Index Base + 24H
	Window 3: Index Base + 2CH
	Window 4: Index Base + 34H
Register Address (Slot B)	Window 0: Index Base + 54H
	Window 1: Index Base + 5CH
	Window 2: Index Base + 64H
	Window 3: Index Base + 6CH
	Window 4: Index Base + 74H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
OFFSETA19	OFFSETA18	OFFSETA17	OFFSETA16	OFFSETA15	OFFSETA14	OFFSETA13	OFFSETA12

Table 7-34. Card Memory Offset Address Low-Byte Register

Bit(s)	Name	Description
D7–D0	OFFSETA[19:12]	Default = 0 for all bits
		Low-order address bits added to the system address bits A[19:12] to generate the memory address for the PC Card

Card Memory Offset Address High-Byte Register

Name	Card Memory Offset Address High-Byte Register
Type	Read/Write
Register Address (Slot A)	Window 0: Index Base + 15H
	Window 1: Index Base + 1DH
	Window 2: Index Base + 25H
	Window 3: Index Base + 2DH
	Window 4: Index Base + 35H
Register Address (Slot B)	Window 0: Index Base + 55H
	Window 1: Index Base + 5DH
	Window 2: Index Base + 65H
	Window 3: Index Base + 6DH
	Window 4: Index Base + 75H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
WP	REG	OFFSETA25	OFFSETA24	OFFSETA23	OFFSETA22	OFFSETA21	OFFSETA20

Table 7-35. Card Memory Offset Address High-Byte Register

Bit(s)	Name	Description
D7	WP	Default = 0
		Write Protect bit
		0 = Enables write operation to the PC Card through the corresponding system memory window
		1 = Disables write operation to the PC Card through the corresponding system memory window
D6	REG	Default = 0
		REG Active bit
		0 = Access to the system results in common memory on the PC Card being accessed
		1 = Access to the system results in attribute memory on the PC Card being accessed
D5–D0	OFFSETA[25:20]	Default = 0 for all bits
		Card Memory Offset Address A[25:20] bits
		High-order address bits that are added to the system address bits A[25:20] to generate the memory address for the PC Card

Card Detect and General Control Register

Name	Card Detect and General Control Register
Type	Read/Write
Register Address (Slot A)	Index Base + 16H
Register Address (Slot B)	Index Base + 56H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SWCDINT	CDRSMEN	Reserved	Reserved	CFGRSTEN	DLY16INH

Table 7-36. Card Detect and General Control Register

Bit(s)	Name	Description
D7–D6	Reserved	Default = 0 for all bits
D5	SWCDINT	Default = 0
		Software Card Detect Interrupt bit
		If the Card Detect Enable bit is set to “1” in the Card Status Change Interrupt Configuration register, then writing a “1” to this bit causes a card detect card status change interrupt for the associated slot. The functionality and acknowledgment of this software interrupt works the same way as the hardware-generated interrupt. This bit is always read back as a 0.
		Functionality of the hardware card detect card status change interrupt is not affected. If card detect card status change from the previous state occurs on the *CD[2:1] inputs, a hardware card detect card status change interrupt is generated. If the Card Detect Enable bit is set to zero in the Card Status Change Interrupt Configuration Register, then writing a "1" to this bit has no effect. For Miniature Card applications, *MC_CD and *MC_CINS replace *CD[2:1].
D4	CDRSMEN	Default = 0
		Card Detect Resume Enable bit
		If this bit is set to “1” and a card change is detected on the *CD[2:1] inputs, the internal *RIO signal goes from high to low and the Card Detect Change bit in the Card Status Change register is set to “1.” The internal *RIO output remains low until a “1” is either read or written to the Card Detect Change bit in the Card Status Change register (acknowledge cycle). The Card Detect Change bit then resets to “0” and the internal *RIO signal goes from low to high. The Card Detect Enable bit must be set to “1” in the Card Status Change Interrupt Configuration register to generate *RIO. For Miniature Card applications, *MC_CD and *MC_CINS replace *CD[2:1].
		If the card status change is routed to any of the IRQ signals, the setting of this bit to "1" prevents IRQ from going active as a result of a hardware card detect status change. Once the resume software detects a card detect status change interrupt from *RIO (by reading the Card Status Change register), the software should initiate a software card detect change so that the card detect change condition generates an active interrupt on the IRQ signal.
D3-D2	Reserved	Default = 0 for all bits

Table 7-36. Card Detect and General Control Register (continued)

D1	CFGRSTEN	Default = 0
		Configuration Reset Enable bit
		1 = When this bit is set to “1,” and both the *CD[2:1] inputs go high, a reset pulse is generated to reset the slot configuration registers to their default state. The registers involved are all I/O registers, all memory registers, Interrupt and General Control register, and the Address Window Enable register. For Miniature Card applications, *MC_CD and *MC_CINS replace *CD[2:1].
D0	DLY16INH	Default = 0
		16-bit Memory Delay Inhibit
		0 = When this bit is cleared to “0” and a system memory window is configured for 16-bit access by setting the data size bit to “1” in the System Memory Address Mapping Start High-Byte register, the falling edges of control strobes *WE and *OE are delayed synchronously by BUSCLK.
		1 = Falling edge of the control strobe is not synchronously delayed.

Global Control Register

Name	Global Control Register
Type	Read/Write
Register Address (Slot A)	Index Base + 1EH
Register Address (Slot B	IIndex Base + 5EH

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	CLRPMIRQ	IRQPM_EN	EXWRBK	Reserved	Reserved

Table 7-37. Global Control Register

Bit(s)	Name	Description
D7–D5	Reserved	Default = 0 for all bits
D4	CLRPMIRQ	Default = 0
		Clear Pulse Mode IRQ bit used in conjunction with IRQPM_EN. When IRQPM_EN is set to “0,” this bit is ignored.
		The VR4102 supports level mode only. When the IRQPM_EN bit is set to “1”, the VRC4171A must translate pulse mode behavior to level mode behavior. When an interrupt occurs, the VRC4171A asserts the IRQ line to the VR41xx and keeps it high. Upon completion, the interrupt driver writes this bit to create a short pulse to clear the IRQ line and prepare for the next one. This bit is always read as “0.”
D3	IRQPM_EN	Default = 0
		IRQ Pulse Mode Enable bit
		0 = Indicates that card *IREQ signal is in level mode (default)
		1 = Indicates that the card *IREQ signal is in pulse mode
D2	EXWRBK	Default = 0
		Explicit Write Back Card Status Change Acknowledge bit
		0 = The card status change interrupt is acknowledged by reading the Card Status Change Register and the register bits are cleared upon a read cycle.
		1 = Requires an explicit write of a “1” to the Card Status Change register bit that indicates an interrupting condition.
D1-D0	Reserved	Default = 0 for all bits

Card Voltage Sense Register

Name	Card Voltage Sense Register
Type	Read/Write
Register Address (Slot A)	Index Base + 1FH
Register Address (Slot B)	Index Base + 5FH

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	*VS2	*VS1

Table 7-38. Card Voltage Sense Register

Bit(s)	Name	Description		
D7–D2	Reserved	Default = 0 for all bits		
D1–D0	*VS[2:1]	Default = xx		
		Voltage Sense Status bits from card		
		0	0	3.3v/XV capable
		0	1	X.XV only
		1	0	3.3V capable
		1	1	5V only

Card Voltage Select Register

Name	Card Voltage Select Register
Type	Read/Write
Register Address (Slot A)	Index Base + 2FH
Register Address (Slot B)	Index Base + 6FH

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCCEN1	VCCEN0

Table 7-39. Card Voltage Select Register

Bit(s)	Name	Description			
D7–D2	Reserved	Default = 0 for all bits			
D1–D0	VCCEN[1:0]	Default = 00			
		Voltage Select bits written by software			
		Automatically reset to default state every time a card is removed from the socket; D1–D0 control the V_{CC} value applied to the card when the PC Card Power Enable bit in register 02H is set. The settings below conform to a MICREL 2560-1 without external gates:			
		D1	**D0**	**Voltage Selection**	***VCCEN[1:0] Status**
		0	0	5V	01
		0	1	3.3V	10
		1	0	X.Xv (OFF if X.Xv is not available)	11
		1	1	3.3V	10

Caution: Voltages must switch through 0V when changing from 3.3V to 5V or vice versa.

LCD Registers

Panel Select Register

Name	Panel Select Register
Type	Read/Write
Register Address	0000h

Bits

D15–D7	D6	D5–D4	D3	D2	D1	D0
Reserved	HALF_DUAL	Reserved	8_STN	P_COLOR_SEL	DUAL_PANEL	PANELTYPE

Table 7-40. Panel Select Register

Bit(s)	Name	Description
D15–D7	Reserved	Default = 0 for all bits
D6	HALF_DUAL	Default = 0
		Half Dual Panel Select
		0 = normal dual
		1 = Half dual
D5–D4	Reserved	Default = 0 for all bits
D3	8_STN	Default = 0
		8-Bit Data Output STN Panel Select
		0 = 16-bit
		1 = 8-bit
D2	P_COLOR_SEL	Default = 0
		Panel Color Select
		0 = monochrome
		1 = color
D1	DUAL_PANEL	Default = 0
		Dual Panel Select
		0 = single scan
		1 = dual scan
D0	PANELTYPE	Default = 0
		Panel Type Select
		0 = STN
		1 = TFT

Note: For color TFT panels and CRTs, the value = 05.

Panel Control Register

Name	Panel Control Register
Type	Read/Write
Register Address	0002h

Bits

D15-D13	D11	D10	D9	D8	D7–D3	D2–D0
Reserved	EN_WAVE	FLM_POL	LP_POL	OFF_SHCLK	Reserved	COLOR_DEPTH

Table 7-41. Panel Control Register

Bit(s)	Name	Description	
D15–D12	Reserved	Default = 0	
D11	EN_WAVE	Default = 0	
		1 = enable wave equation (gray level is generated from RGB and output to the G channel)	
D10	FLM_POL	Default = 0	
		First Line Marker Polarity Select	
		0 = active high	
		1 = active low	
D9	LP_POL	Default = 0	
		Line Pulse Polarity Select	
		0 = active high	
		1 = active low	
D8	OFF_SHCLK	Default = 0	
		1 = Turn off SCLK during blanking	
D7–D3	Reserved	Default = 0 for all bits	
D2–D0	COLOR_DEPTH	Default = 0 for all bits	
		Color Depth Select	
		000 = color/mono 1 bpp (default)	Indexed mode
		001 = color/mono 2 bpp	Indexed mode
		010 = color 4 bpp	Indexed mode
		011 = color 5 bpp	Indexed mode
		100 = color 6 bpp	Indexed mode
		101 = color 8 bpp	Indexed mode
		110 = color 16 bpp (5-5-5 format)	Nonindexed mode
		111 = color 16 bpp (5-6-5 format)	Nonindexed mode

Notes: **1.** Indexed mode uses the 18-bit palette RAM to generate the color data output to the LCD. The information in the selected number-of-bits-per-pixel value (1, 2, 4, 5, 6, 8) is used for an index number to address the 18-bit palette RAM. The color data stored in the addressed 18-bit palette RAM is the output to the LCD. Use registers 040h, 042h, and 044h to store or change the color data in the 18-bit palette RAM.

2. The nonindexed modes (both 15 and 16 bpp) generate the color data from the frame buffer memory data directly. No 18-bit palette RAM data is used.

Power Mode Control Register

Name	Power Mode Control Register
Type	Read/Write
Register Address	0004h

Bits

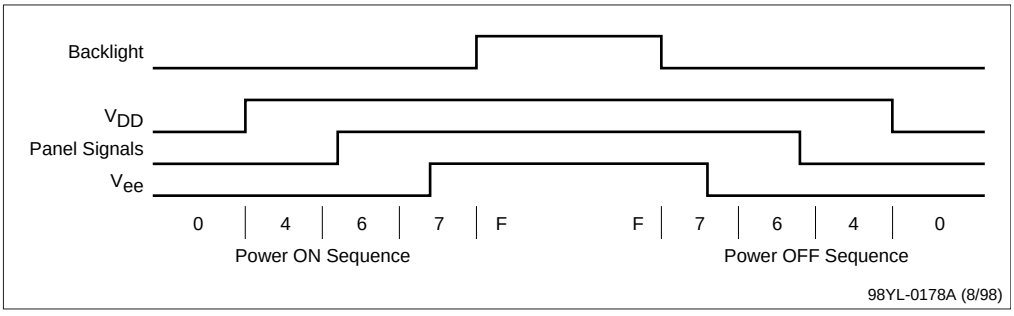
D15–D6	D5	D4	D3	D2	D1	D0
Reserved	SEL_REF	PWR_DWN	BACKLIGHT_ON	EN_VDD	EN_PANEL	EN_VEE

Table 7-42. Power Mode Control Register

Bit(s)	Name	Description
D15–D6	Reserved	Default = 0
D5	SEL_REF	Default = 0
		Self refresh enable
		1 = Enable
D4	PWR_DWN	Default = 0
		Power down enable
		1 = Enable
D3	BACKLIGHT _ ON	Default = 0
		Backlight ON/OFF control
		0 = OFF
		1 = ON (backlight can be turned on only when VEE is enabled)
D2	EN_VDD	Default = 0
		1 = Enable VDD
D1	EN_PANEL	Default = 0
		1 = Enable panel control signals and data output
D0	EN_VEE	Default = 0
		1 = Enable VEE

Note: Check your selected panel for power-on specifications. A suggested power-on sequence is 0xX0, 0xX4, 0xX6, 0xX7, 0xXF. The power-off sequence is the reverse: 0xXF, 0xX7,0xX6, 0xX4, 0xX0.

Figure 7-3. Power On/Off Sequences



VMCLK Enable Register

Name	VMCLK Enable Register
Type	Read/Write
Register Address	0006h

Bits

D15–D1	D0
Reserved	ENABLE_VMCLK

Table 7-43. VMCLK Enable Register

Bit(s)	Name	Description
D15–D1	Reserved	Default = 0
D0	ENABLE_VMCLK	Default = 1
		1 = Enable VMCLK clock in the LCD controller

VCLK Enable Register

Name	VCLK Enable Register
Type	Read/Write
Register Address	0008h

Bits

D15–D1	D0
Reserved	EN_VCLK

Table 7-44. VCLK Enable Register

Bit(s)	Name	Description
D15–D1	Reserved	Default = 0
D0	EN_VCLK	Default = 1
		1 = Enable VCLK clock

Video FIFO/Memory Interface Control Register

Name	Video FIFO/Memory Interface Control Register
Type	Read/Write
Register Address	000Ah

Bits

D15–D13	D12	D11–D10	D9	D8	D7–D5	D4	D3	D2	D0
Reserved	VRAS_CTL	VCAS_CTL (VRC4171A)	SCREEN_OFF	DRAM_OFF	FIFO_THD	MEMSIZE	MEM_CONF	Reserved	FIFO_DEP

Table 7-45. Video FIFO/Memory Interface Control Register

Bit(s)	Name	Description
D15–D13	Reserved	Default = 0
D11	VRAS_CTL	Default = 0
		0 = *VRAS [1:0] low to *VCAS [1:0] low has three MCLK periods
		1 = *VRAS [1:0] low to *VCAS [1:0] low has two MCLK periods
D11–D10 (VRC4171A)	VCAS_CTL	Default = 00
		00 = normal *VCAS[1:0}
		01 = *VCAS[1:0] pulse is lengthened one TD (1.5 ns nominally) *VCAS[1:0] precharge time is decreased one TD (1.5 ns nominally)
		10 = *VCAS[1:0] pulse is lengthened two TD (1.5 ns nominally) *VCAS[1:0] precharge time is decreased two TD (3.0 ns nominally)
		11 = *VCAS[1:0] pulse is lengthened three TD (1.5 ns nominally) *VCAS[1:0] precharge time is decreased three TD (4.5 ns nominally)
D9	SCREEN_ OFF	Default = 0
		1 = turn screen off
D8	DRAM_OFF	Default = 0
		1 = tri-state DRAM interface pins
D7–D5	FIFO_THD	Default = 0
		FIFO threshold select number of empty entries (minus 1) in FIFO before reading from frame buffer
D4–D3	MEM_CONF	Memory Configuration
		Default value on power up or reset is 00.
		00 = 1/2 MB (one 256K x 16 DRAM)
		10 = 1 MB (two 256K x 16 DRAMs)
		01 = 2 MB (one 1M x 16 DRAM)
		11 = invalid
D2	Reserved	Default = 0
D1–D0	FIFO_DEP	Default = 00
		FIFO depth
		00 = 16 level
		01 = 12 level
		10 = 8 level
		11 = 4 level

Note: For a unified board with 3.3-volt, 1M x 16-bit DRAM memory, the register value is 08.

Pixel Adjustment / Vertical Half Register

Name	Pixel Adjustment / Vertical Half Register
Type	Read/Write
Register Address	000Ch

Bits

D15–D13	D12–D11	D10–D0
TFT_ADJ	Reserved	VERT_HALF

Table 7-46. Pixel Adjustment / Vertical Half Register

Bit(s)	Name	Description
D15–D13	TFT_ADJ	Default = 00
		TFT pixel adjustment for starting display
D12–D11	Reserved	Default = 0 for all bits
D10–D0	VERT_HALF	Default = 0
		Vertical Panel Size / 2 for STN panel
		This register must be set to half the vertical panel size.

Table 7-47. Panel Settings

Panel Type	Register Value
TFT LCD screen or 640 x 480 CRT	0x00FO
800 x 600 CRT (Note)	0x012C
320 x 240 TFT panel	0x00FO
320 x 240 monochrome panel	0x0078

Note: To stay within the limits of frame buffer memory bandwidth, do not exceed the maximum bits-per-pixel setting of 8. A smaller bits-per-pixel setting can be used with no problem.

Vert_Half Setting Example for 240 Vertical Pixel Size STN Panel

240/2 = 120 = 0x78
480/2 = 240 = 0xF0
600/2 = 300 = 0x12C

Horizontal Display Register

Name	Horizontal Display Register
Type	Read/Write
Register Address	0010h

Bits

D15-D8	D7-D0
HORIZ_DISP_END	HORIZ_TOTAL

Table 7-48. Horizontal Display Register

Bit(s)	Name	Description
D15-D8	HORIZ_DISP_END	Default = 0 for all bits
		Horizontal Display End (Note)
		Value = (H_{DISP}/8) – 1
D7-D0	HORIZ_TOTAL	Default = 0 for all bits
		Horizontal Total (Note)
		Value = (H_{TOTAL}/8) – 1

Note: All horizontal register values represent characters or 8 pixels. One character clock period represents 8 pixel clocks in the horizontal dimension. For example, 640 pixels (640/8) – 1 = 80 – 1 = 79 = 0x4F.

Horizontal Retrace Control Register

Name	Horizontal Retrace Control Register
Type	Read/Write
Register Address	0012h

Bits

D15–D8	D7–D0
HORIZ_RETEND	HORIZ_RETSRT

Table 7-49. Horizontal Retrace Control Register

Bit(s)	Name	Description
D15–D8	HORIZ_ RETEND	Default = 0
		Horizontal Retrace End (**Note**)
		Value = (H_{DISP} + H_{FRONT}_porch + H_{SYN})/8
D7–D0	HORIZ_ RETSRT	Default = 0
		Horizontal Retrace Start (**Note**)
		Value = (H_{DISP} + H_{FRONT}_porch)/8

Note: All horizontal register values represent characters or 8 pixels. One character clock period represents 8 pixel clocks in the horizontal dimension.

Vertical Display End Register

Name	Vertical Display End Register
Type	Read/Write
Register Address	0014h

Bits

D15–D11	D10–D0
Reserved	VERT_END

Table 7-50. Vertical Display End Register

Bit(s)	Name	Description
D15–D11	Reserved	Default = 0 for all bits
D10–D0	VERT_END	Default = 0 for all bits
		Vertical Display End
		Value = V_{DISP} – 1

Vertical Display Total Register

Name	Vertical Display Total Register
Type	Read/Write
Register Address	0016h

Bits

D15–D11	D10–D0
Reserved	VERT_TOTAL

Table 7-51. Vertical Display Total Register

Bit(s)	Name	Description
D15–D11	Reserved	Default = 0 for all bits
D10–D0	VERT_TOTAL	Default = 0 for all bits
		Vertical Total
		Value = V_{TOTAL} – 1

Vertical Retrace Start Register

Name	Vertical Retrace Start Register
Type	Read/Write
Register Address	0018h

Bits

D15–D11	D10–D0
Reserved	VERT_RETST

Table 7-52. Vertical Retrace Start Register

Bit(s)	Name	Description
D15–D11	Reserved	Default = 0 for all bits
D10–D0	VERT_RETST	Default = 0 for all bits
		Vertical Retrace Start
		Value = V_{DISP} + V_{FRONT}_porch

Note: Different panels require different numbers based on the panel specification. Use at your own risk. For example, 640 x 480 value = 0x01EA and 320 x 240 value = 0x0F1.

Vertical Retrace End Register

Name	Vertical Retrace End Register
Type	Read/Write
Register Address	001Ah

Bits

D15–D10	D9–D7	D6–D4	D3–D0
Reserved	VERT_END_SKIP	VERT_SKIP	VERT_RETEND

Table 7-53. Vertical Retrace End Register

Bit(s)	Name	Description
D15–D10	Reserved	Default = 0 for all bits
D9–D7	VERT_END_ SKIP	Default = 0 for all bits
		Vertical End Skip control; additional LP pulses to be skipped for processing at vertical end (DSTN only)
D6–D4	VERT_SKIP	Default = 0 for all bits
		Vertical Skip control; additional LP pulses to be skipped for processing at vertical half (DSTN only)
D3–D0	VERT_RETEND	Default = 0 for all bits
		Vertical Retrace End
		Value = (VERT_RETST + V_{SYN})mod16

Note: For TFTs and CRTs, 640 x 480 = 0x0008. For STN, 320 x 240 = 0x0385.

Starting Address Register

Name	Starting Address Register
Type	Read/Write
Register Address	001Ch

Bits

D15–D0
START_ADDR

:

Table 7-54. Starting Address Register

Bit(s)	Name	Description
D15–D0	START_ADDR	Address is combined with Offset Register (001Eh) bits [14:12] to form the frame memory starting address for display.
		Frame Memory Starting Address[17:2]; bits [1:0] default to 00

For a 640 x 480 display at 8 bits per pixel, the second page of frame buffer memory would be 307,200 pixels: 640 x 480 = 307200 = 0x4B000. Offset from the beginning of frame buffer memory 307,200 is equal to 0x4B000. Right shift by two bits to drop address bits 1 and 0 (0x4B000 -> 0x12C00): START_ADD = 0x2C00 and OFFSET_REG = 0x1xxx.

Offset Register

Name	Offset Register
Type	Read/Write
Register Address	001Eh

Bits

D15	D14–D12	D11–D10	D9–D0
Reserved	A_OVERFLOW	Reserved	SCREEN_WIDTH

Table 7-55. Offset Register

Bit(s)	Name	Description
D15	Reserved	Default = 0
D14–D12	A_OVERFLOW	Default = 0 for all bits
		Frame Memory Starting Address[20:18]
D11–D10	Reserved	Default = 00
D9–D0	SCREEN_ WIDTH	Default = 0 for all bits
		Logical Line Screen Width
		Value = (H_{DISP} * Byte_per_pixel)/8 (represents character or 8 pixels)

The full offset address is ANDed to select only address bits 20, 19, and 18 using mask 0x1C0000. Shift the result 6 bits to OR these 3 bits into offset register bit positions D14, D13, and D12. For a 640 x 480 display at 8 bits per pixel, the second page of frame buffer memory would be full offset address Ox4B000. In other words, Ox4B000 and Ox1C0000 = Ox040000. Ox040000 right shifted 6 bits = Ox1000. Therefore, Offset Register 1 = Ox1050. With a screen width of 640 pixels and setting of 8 bits per pixel (Table 7-56), the screen width setting value is 0x50.

When changing the bits-per-pixel setting, the Panel Control register [0002] and Offset register [001E] must change (Table 7-41 and Table 7-56).

Table 7-56. Screen Width Setting for 640 x 480 Display

	Panel Control Register	Screen Width	
Bits Per Pixel	**Color Depth**	**640 Pixels**	**320 Pixels**
16	7	0xA0	0x50
8	5	0x50	0x28
4	2	0x28	0x14
2	1	0x14	0x0A
1	0	0x0A	0x05

Hardware Cursor Control Register

Name	Hardware Cursor Control Register
Type	Read/Write
Register Address	0020h

Bits

D15-D3	D2	D1	D0
Reserved	CURSOR	Reserved	EN_CURSOR

Table 7-57. Hardware Cursor Control Register

Bit(s)	Name	Description
D15-D3	Reserved	Default = 0 for all bits
D2	CURSOR	Default = 0
		Hardware Cursor Pattern Select
D1	Reserved	Default = 0
D0	EN_CURSOR	Default = 0
		Hardware Cursor Enable
		0 = disable
		1 = enable

Select a memory area in off-screen memory to display the hardware cursor data pattern, which consists of 32 bits of plane 0 followed by 32 bits of plane 1 for the first hardware cursor scan line, shown in Table 7-58 and Figure 7-7

Table 7-58. Hardware Cursor Function

D2	D0	Harware Cursor	Address in Upper 512 Bytes of Frame Buffer Memory		
0	01	Disabled			
0	1	Pattern 0	... E00	... EFF	256 bytes
1	1	Pattern 1	... F00	... FFF	256 bytes

For a UEB41xx evaluation board reference design using one 1M x 16-bit DRAM, the pattern 0 starting address (CPU style) is OxAA1FFE00. The pattern 1 starting address is OxAA1FFF00, which is the upper 512 bytes of 2-MB LCD frame buffer memory.

Hardware Cursor X Position Register

Name	Hardware Cursor X Position Register
Type	Read/Write
Register Address	0022h

Bits

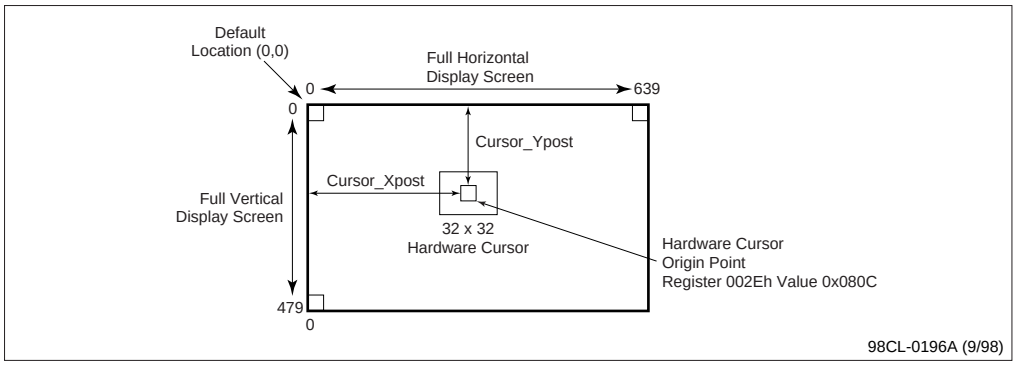
D15–D11	D10–D0
Reserved	CURSOR_XPOST

Table 7-59. Hardware Cursor X Position Register

Bit(s)	Name	Description
D15–D11	Reserved	Default = 0 for all bits
D10–D0	CURSOR_ XPOST	Default = 0
		Cursor X origin position in pixels

The cursor position is defined relative to the hardware cursor pixel point origin from the upper left (0,0) of the full display screen. Cursor position *X* is in pixels and is specified by register 22h. Cursor position *Y* is in scan lines and is specified by register 24h. The cursor origin register 2Eh specifies the origin point inside the hardware cursor as the number x,y pixels from the (0,0) point in the top left of the 32 x 32 hardware cursor image. The default for register 2Eh is 0 for the x-origin and 0 for the y-origin.

Figure 7-4. X and Y Origin Points



Hardware Cursor Y Position Register

Name	Hardware Cursor Y Position Register
Type	Read/Write
Register Address	0024h

Bits

D15–D11	D10–D0
Reserved	CURSOR_YPOST

Table 7-60. Hardware Cursor Y Position Register

Bit(s)	Name	Description
D15–D11	Reserved	Default = 0 for all bits
D10–D0	CURSOR_ YPOST	0 = sets hardware cursor at top line (default)
		Cursor Y origin position in scan lines (the number of vertical pixels downward from the top scan line)

The relative position is measured from the top scan line of the display screen to the hardware cursor pixel point origin, as designated by register [002E].

Hardware Cursor Color 0A Register

Name	Hardware Cursor Color 0A Register
Type	Read/Write
Register Address	0026h

Bits

D15–D14	D13–D8	D7–D6	D5–D0
Reserved	RED_0	Reserved	GREEN_0

Table 7-61. Hardware Cursor Color 0A Register

Bit(s)	Name	Description
D15–D14	Reserved	Default = 0 for all bits
D13–D8	RED_0	Default = 0
		Red
D7–D6	Reserved	Default = 00
D5–D0	GREEN_0	Default = 0
		Green

1. For nonindexed modes (both 16 bpp modes), cursor color 0 is defined directly by the values stored in the 26h and 28h registers.

2. For indexed modes, bits D5–D1 of the Hardware Cursor Color 0B register are the lower five bits (IAD4–IAD0) of the index address to select the 18-bit palette RAM color displayed for cursor color 0. Bits D13-D8 and D5-D3 of the Hardware Cursor Color 0A register are “don’t care” for indexed modes. The upper 3 bits (IAD7–IAD5) of the index address are stored in bits D2–D0 of the Hardware Cursor Color 0A register (in other words, the lower 3 bits of the Green Palette register).

Table 7-62. Example of Bits Conversion

0B	0A	8-Bit Index Address to 18-Bit Palette RAM					
0028	**0026**	**IAD7-IAD0**	**8-Bit Address = 92**				
0x0002	0x0000	01	D7	D5	D4	D0	
0x000A	0x0000	05	100		10010		0
0x003E	0x0000	0x1F	D2	D0	D5	D1	D0
0x0024	0x0004	0x92	Register 26 = 04		Register 28 = 0x24		
0x003E	0x0007	0xFF					

3. The 18-bit palette RAM location designated by the 8-bit index address must be programmed with the color selected to be displayed for Hardware Cursor Color 0. Alternatively, you can use the color already programmed into that location in a previous software setup.

Hardware Cursor Color 0B Register

Name	Hardware Cursor Color 0B Register
Type	Read/Write
Register Address	0028h

Bits

D15–D6	D5–D0
Reserved	BLUE_0

Table 7-63. Hardware Cursor Color 0B Register

Bit(s)	Name	Description
D15–D6	Reserved	Default = 0 for all bits
D5–D0	BLUE_0	Default = 0
		Blue

1. For nonindexed modes, select the value of the blue color for cursor color 0.

2. For indexed modes, bits D5–D1 set the lower 5 bits(IAD4–IAD0) of an 8-bit index address into the 18-bit palette RAM to select cursor color 0.

3. Bit D0 is a “don’t care.”

4. The Hardware Cursor Color 0A register contains the upper 3 bits (IAD7, IAD6, and IAD5) of the 8-bit index address in register bit positions D2, D1, and D0. Combining the 0A register’s 3 bits with the 0B register’s 5 bits makes an 8-bit index address IAD7-IAD0 and selects one of the 256 locations in the 18-bit palette RAM to be displayed for hardware cursor color 0. Hardware cursor color 0 is displayed when the hardware cursor is enabled and when both cursor plane 0 and cursor plane 1 bits equal 0 for this cursor display pixel position.

Hardware Cursor Color 1A Register

Name	Hardware Cursor Color 1A Register
Type	Read/Write
Register Address	002Ah

Bits

D15–D14	D13–D8	D7–D6	D5–D0
Reserved	RED_1	Reserved	GREEN_1

Table 7-64. Hardware Cursor Color 1A Register

Bit(s)	Name	Description
D15–D14	Reserved	Default = 0 for all bits
D13–D8	RED_1	Default = 0 for all bits
D7–D6	Reserved	Default = 00
D5–D0	GREEN_1	Default = 0
		Green

1. For nonindexed modes (both 16 bppp modes), cursor color 1 is defined directly by the values stored in the 2Ah and 2Ch registers.

2. For indexed modes, bits D5–D1 are the lower 5 bits (IAD4–IAD0) of the index address to select the 18-bit palette RAM color displayed for cursor color 1.

3. Bits D13–D8 and D5–D3 of the Hardware Cursor Color 1A register are “don’t care” for indexed modes.

4. The upper 3 bits (IAD7–IAD5) of the index address are stored in bits D2–D0 of the Hardware Cursor Color 1B register (in other words, the lower 3 bits of the Green Palette register).

5. The 18-bit palette RAM location designated by the 8-bit index address must be programmed with the color selected to be displayed for Hardware Cursor Color 1. Alternatively, you can use the color already programmed into that location in a previous software setup.

Hardware Cursor Color 1B Register

Name	Hardware Cursor Color 1B Register
Type	Read/Write
Register Address	002Ch

Bits

D15–D6	D5–D0
Reserved	BLUE_1

Table 7-65. Hardware Cursor Color 1B Register

Bit(s)	Name	Description
D15–D6	Reserved	Default = 0 for all bits
D5–D0	BLUE_1	Default = 0 for all bits
		Blue

1. For nonindexed modes, select the value of the blue color for cursor color 1.

2. For indexed modes, bits D5–D1 set the lower 5 bits (IAD4-IAD0) of an 8-bit index address into the 18-bit palette RAM to select cursor color 1. Bit 0 is “don’t care.”

3. The Hardware Cursor Color 1A register contains the upper 3 bits (IAD7, IAD6, and IAD5) of the 8-bit index address. Combining register 1A’s 3 bits with register 1B’s 5 bits makes an 8-bit index address (IAD7-IAD0) and selects one of the 256 locations in the 18-bit palette RAM to be displaed for hardware cursor color 1. Hardware cursor color 1 is displayed when the hardware cursor is enabled and the cursor plane 0 bit = 1 and the cursor plan 1 bit = 0 for this cursor display pixel bit position.

Hardware Cursor Origin Register

Name	Hardware Cursor Origin Register
Type	Read/Write
Register Address	002Eh

Bits

D15–D14	D13–D8	D7–D6	D5–D0
Reserved	Y_ORIGIN	Reserved	X_ORIGIN

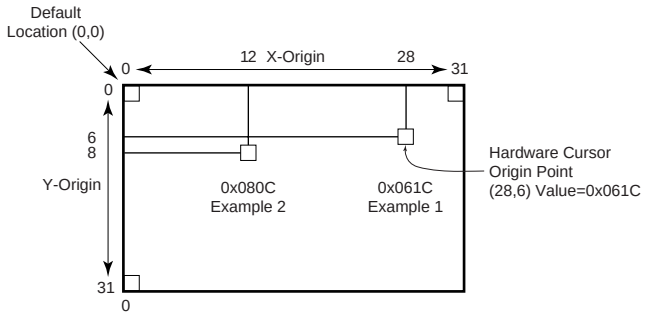
Table 7-66. Hardware Cursor Origin Register

Bit(s)	Name	Description
D15–D14	Reserved	Default = 0 for all bits
D13–D8	Y_ORIGIN	Default = 0 for all bits
D7–D6	Reserved	Default = 0 for all bits
D5–D0	X_ORIGIN	Default = 0 for all bits

In the 32 by 32 matrix for the hardware cursor, select the one pixel to be the hardware cursor origin point. Start from the absolute point of (0,0) in the upper left corner of the cursor image. The cursor origin register 2Eh specifies the origin point for the hardware cursor as the number x pixels from the (0,0) point in the upper left of the 32 x 32 hardware cursor image. The default is 0 for the x-origin and 0 for the y-origin.

Increasing the value of the x-origin register moves the origin point in the horizontal direction to the right. The maximum count of 31 decimal positions would indicate the right edge of the hardware cursor. Increasing the y-origin register moves the origin point down in the vertical direction to the bottom edge of the hardware cursor image. The maximum count of 31 decimal positions would indicate the bottom edge of the hardware cursor.

Figure 7-5. X and Y Origin Points



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RAM Write Address Register

Name	RAM Write Address Register
Type	Write-Only (16-Bit Access Only)
Register Address	0040h

Bits

D15–D8	D7–D0
Reserved	RAM_W_ADDR

Table 7-67. RAM Write Address Register to 18-Bit Palette RAM

Bit(s)	Name	Description
D15–D8	Reserved	Default = 0 for all bits
D7–D0	RAM_W_ADDR	RAM write address

Select an index address (0-FF) before writing to the 18-bit palette RAM color data registers. The next two write cycles to RAM Write Port register 0 (red and green palette) and RAM Write Port register 1 (blue palette) will store the color data into the 18-bit palette RAM data lookup table (LUT) indexed by the address stored in this RAM Write Address register.

RAM Write Port Register 0

Name	RAM Write Port Register 0
Type	Write-Only (16-Bit Access Only)
Register Address	0042h

Bits

D15–D14	D13–D8	D7–D6	D5–D0
Reserved	RED_W_REG	Reserved	GREEN_W_REG

Table 7-68. RAM Write Port Register 0

Bit(s)	Name	Description
D15–D14	Reserved	Default = 0 for all bits
D13–D8	RED_W_REG	Default = 0 for all bits
		Red
D7–D6	Reserved	Default = 0 for all bits
D5–D0	GREEN_W_REG	Default = 0 for all bits
		Green

Write the six red palette RAM data bits (D13–D8) and six green palette RAM data bits (D5–D0) with one single 16-bit write cycle. This is a 16-bit write-only register. You cannot read, AND, or OR data from it. Read cycles are undefined. Use the RAM Read Address registers (46h, 48h, and 4Ah) to read 18-bit palette RAM data.

RAM Write Port Register 1

Name	RAM Write Port Register 1
Type	Write-Only (16-Bit Access Only)
Register Address	0044h

Bits

D15–D6	D5–D0
Reserved	BLUE_W_REG

Table 7-69. RAM Write Port Register 1

Bit(s)	Name	Description
D15–D6	Reserved	Default = 0 for all bits
D5–D0	BLUE_W_REG	Default = 0 for all bits
		Blue

Write the six blue palette RAM data bits (D5–D0) using a 16-bit write command.

RAM Read Address Register

Name	RAM Read Address Register
Type	Write-Only (16-Bit Access Only)
Register Address	0046h

Bits

D15–D8	D7–D0
Reserved	RAM_R_ADDR

Table 7-70. RAM Read Address Register

Bit(s)	Name	Description
D15–D8	Reserved	Default = 0 for all bits
D7–D0	RAM_R_ADDR	Default = 0 for all bits
		RAM read address

To read the contents of a particular index address (0-FF), write to RAM Read Address register (0046h) and then read from RAM Read Port register 0 (0048h) for red and green palettes and RAM Read Port register 1 (004Ah) for the blue palette.

RAM Read Port Register 0

Name	RAM Read Port Register 0
Type	Read-Only
Register Address	0048h

Bits

D15–D14	D13–D8	D7–D6	D5–D0
Reserved	RED_R_REG	Reserved	GREEN_R_REG

Table 7-71. RAM Read Port Register 0

Bit(s)	Name	Description
D15–D14	Reserved	Default = 0 for all bits
D13–D8	RED_R_REG	Default = 0 for all bits
D7–D6	Reserved	Default = 00
D5–D0	GREEN_R_REG	Default = 0 for all bits

Red and green values of 18-bit palette RAM data are returned according to the index address written to RAM Read Address register (0046h).

RAM Read Port Register 1

Name	RAM Read Port Register 1
Type	Read-Only
Register Address	004Ah

Bits

D15–D6	D5–D0
Reserved	BLUE_R_REG

Table 7-72. RAM Read Port Register 1

Bit(s)	Name	Description
D15–D6	Reserved	Default = 0 for all bits
D5–D0	BLUE_R_REG	Default = 0 for all bits
		Blue

The blue palette value of 18-bit palette RAM data is returned according to the index address written to the RAM Read Address register (0046h).

Scratch Pad Register 0

Name	Scratch Pad Register 0
Type	Read/Write
Register Address	0050h

Bits

D15–D0
Reserved

Table 7-73. Scratch Pad Register 0

Bit(s)	Name	Description
D15–D0	Reserved	Default = 0 for all bits

Scratch Pad Register 1

Name	Scratch Pad Register 1
Type	Read/Write
Register Address	0052h

Bits

D15–D0
Reserved

Table 7-74. Scratch Pad Register 1

Bit(s)	Name	Description
D15–D0	Reserved	Default = 0 for all bits

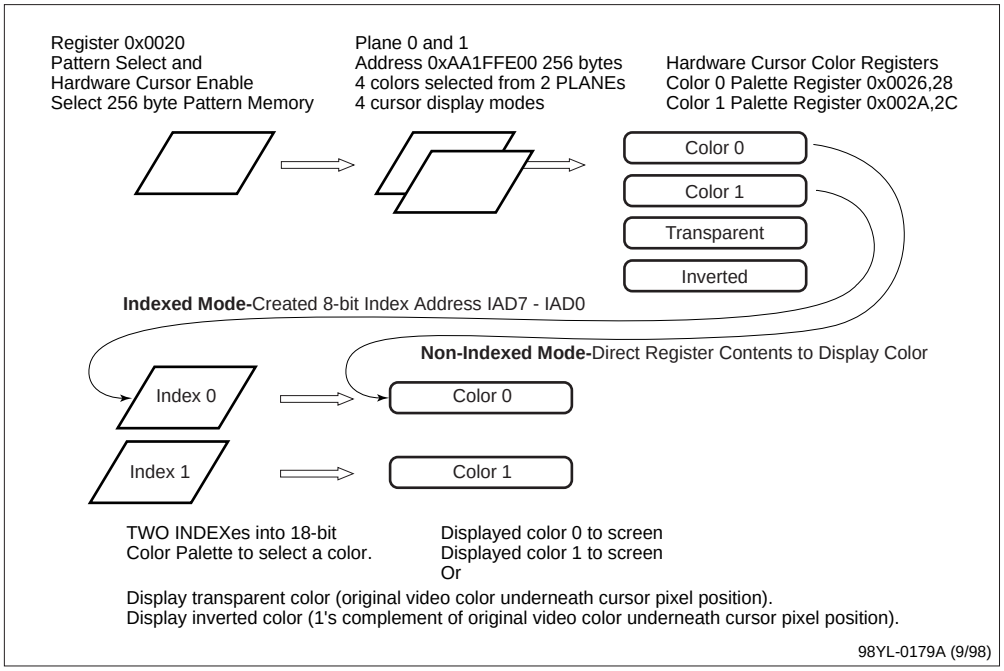
Hardware Cursor

The hardware cursor supports a 32 x 32 x 2 user-defined pattern that is stored in the upper 512 bytes of frame memory. The cursor pattern has two bits to select the display mode of a pixel. Each bit corresponds to a plane. Table 7-75 shows cursor display modes and corresponding cursor pattern values.

Table 7-75. Hardware Cursor Display Modes

Cursor Plane 0	Cursor Plane 1	Cursor Display Mode
0	0	Color 0
1	0	Color 1
0	1	Transparent
1	1	Invert video data

Figure 7-6. Hardware Cursor Color Selection



Nonindexed Modes

Cursor color data would be undefined when read directly from frame buffer memory. Therefore, the VRC4171A includes Cursor Color 0 and Cursor Color 1 registers to define color 0 and color 1. The Color 0 Palette registers 0x0026 and 0x0028 are used as an 18-bit color palette RAM. The Color 1 Palette registers 0x002A and 0x002C are used as secondary 18-bit color palette RAM.

Indexed Modes

The Cursor Color 0 and Cursor Color 1 registers are used as 8-bit address indexes to select a cursor color from one of the color selections programmed into the 18-bit palette RAM. The bits-per-pixel (bpp) setting in Mode register 0002 determines the last index entry able to be accessed. The cursor color registers are used as an index by programming the lower five bits into the blue palette and the upper three bits into the green palette entry. The red palette is a “don’t care” field for indexed modes.

For indexed modes (1, 2, 4, 5, 6 and 8 bpp), the inverted color is the 1's complement of the index number generated from the original video pixel display information. This inverted index number must have a color previously programmed into the 18-bit color RAM palette data. If not previously programmed, color might revert to black (0000) or some odd color. Therefore, color information also must be programmed for the 18-bit palette RAM's complemented index values of the original video pixel display information.

1. For an 8-bpp picture composed of six index values (0, 1, 2, 3, 4, and 5), complemented color data must be programmed into the 18-bit palette RAM index values 0xFF, 0xFE, 0xFD, 0xFC, 0xFB, and 0xFA.

2. For a 4-bpp picture, the complemented color data must be programmed into the 18-bit palette RAM index values 0x0F, 0x0E, 0x0D, 0x0C, 0x0B, and 0x0A.

3. For a 6-bpp picture, the complemented color data must be programmed into the 18-bit palette RAM index values 0x3F, 0x3E, 0x3D, 0x3C, 0x3B, and 0x3A.

As shown in Table 7-76, the pattern continues through address 00-0xFF, for a total of 256 bytes (32 x 32 x 2 bits = 256 bytes).

Table 7-76. Hardware Cursor Pattern Address Mapping

Bytes	Description
0–3	Plane 0 pixel bit for cursor scan line 1
4–7	Plane 1 pixel bit for cursor scan line 1
8–B	Plane 0 pixel bit for cursor scan line 2
C–F	Plane 1 pixel bit for cursor scan line 2

The VRC4171A companion chip uses the little-endian format for the standard bit position within a byte or 32-bit word. Two patterns are available for the hardware cursor (Figure 7-7).

Figure 7-7. Hardware Cursor Pattern

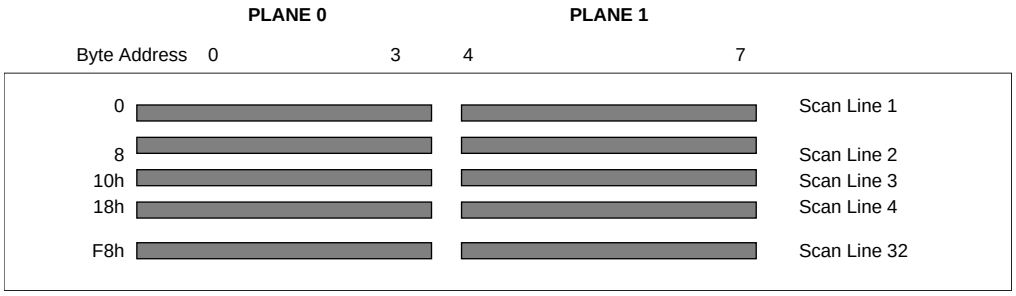


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Table 7-77. Hardware Cursor Display Mode Examples

Line	Cursor Color	Plane	Bytes	Setting
1	0	0	0–3	0
		1	4–7	0
2	1	0	8–B	1
		1	C–F	0
3	Transparent color (original display video data)	0	10h–13h	0
		1	14h–17h	1
4	Inverted display video data	0	18h–1Bh	1
		1	1Ch–1Fh	1

Table 7-78. Hardware Cursor Data Value for Four Display Modes

Horizontal	Scan Line	Byte 1	Address	Byte 2	Address	Byte 3	Address	Byte 4	Address
Plane 0	1	00	0x00	00	0x01	00	0x02	00	0x03
Plane 1	1	00	0x04	00	0x05	00	0x06	00	0x07
Plane 0	2	FF	0x08	FF	0x09	FF	0x0A	FF	0x0B
Plane 1	2	00	0x0C	00	0x0D	00	0x0E	00	0x0F
Plane 0	3	00	0x10	00	0x11	00	0x12	00	0x13
Plane 1	3	FF	0x14	FF	0x15	FF	0x16	FF	0x17
Plane 0	4	FF	0x18	FF	0x19	FF	0x1A	FF	0x1B
Plane 1	4	FF	0x1C	FF	0x1D	FF	0x1E	FF	0x1F

Table 7-79. Maximum Index Number

Bits	Index	Setting
8	255	0xFF
6	64	0x3F
5	31	0x1F
4	15	0x0F
2	3	0x03

Note: The cursor color 0 palettes reside at LCD Control register addresses 0xAA800026 and 0xAA800028. The cursor color 1 palettes reside at addresses 0xAA80002A and 0xAA80002C.

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Table 7-80.

Bits Per Pixel	Maximum Index Size
1	1
2	3
4	15 or 0x0F
5	31 or 0x1F
6	63 or 0x3F
8	255 or 0xFF

For nonindexed modes, the inverted color is the 1's complement of the original video pixels display data read directly from the frame buffer. For 16 bpp, the 5-6-5 format color of rose is 0xEA9C. The 1's complement inverted value to be displayed would be 0x1563, a dark pea green color.

There are two hardware cursor patterns available in register 0xAA800020 (Table 7-81).

Table 7-81. Hardware Cursor Patterns in Register 0xAA800020

0000	00	0 1	(0x01)	0xAA1FFE00 – EFF	Pattern 0
0000	01	0 1	(0x05)	0xAA1FFF00 – FFF	Pattern 1
0000	00	00	(0x00)	Hardware Cursor Disabled	

In indexed modes, the cursor color data is programmed as an 8-bit index pointer into the 18-bit palette RAM for color data selection output to the LCD screen.

For this format, the Blue Palette register holds the lower five index bits (4, 3, 2, 1, 0) in positions D5–D1, allowing 32 indexes in one register location. The Red_Green Palette register holds the upper three index bits (7, 6, 5) in positions D2–D0. To ensure that inverted video color appears in the hardware cursor, program the 1's complement indexes of the original video pixel display values written into frame buffer memory into the unused 18-bit palette RAM indexes. It is problematic if inverted video color in the hardware cursor pattern display memory is used, but the 1's complement indexes are not programmed with inverted video color.

Table 7-82.

Write	Color Register	Index Color
0000	0xAA800026	5
000A	0xAA800028	
0000	0xAA80002A	2
0004	0xAA80002C	

The hardware cursor displays the color 0 pixel when the bit pattern from Planes 0 and 1 together select color 0 (in other words, the Plane 0 bit is 0 and the Plane 1 bit is 0). The Color 1 registers 0x002A and 0x002C select an index number from the 18-bit palette RAM.

Hardware Cursor Inverted Color

For a 4-bpp image containing video data values of 2, 7, and 12, program both the video data values and the 1's complement of these video data values as address index entries into the 18-bit palette RAM. The 1's complements of video data addresses 2, 7 and 12 are 13, 8 and 3, respectively. Program index entries 13, 8, and 3 with the inverted video color to be displayed for the hardware cursor when the hardware cursor pixel is over the top of that image information. Failure to program the 18-bit palette RAM data in index addresses 13, 8, and 3 results in the display of whatever random data is there. If the data is zero, then the color black is displayed for inverted video for that entry. When the hardware cursor pixel selecting inverted video is moved over the part of the picture (image) displaying the index value 12, the V_{RC}4171A companion chip 1 complements that number 12 to 3 and displays to the LCD screen the color previously stored in the 18-bit palette RAM for address index 3.

Programming a Color

Indexed Modes

In indexed modes such as 8-bit-per-pixel mode, the following procedure sets cursor color 0 to display the 18-bit RAM palette color indexed by color 0 registers 0x0026 and 0x0028. When the bits from Plane 1 and Plane 0 are both 0, color 0 is displayed for that hardware mouse cursor pixel position.

1. To program a color for an index between 0 and 255, write the selected index number to address 0xAA800040.

2. Write the RED_GREEN palette values to address 0xAA800042.

3. Write the blue value to address 0xAA800044.

4. The palette values are 6-bit numbers; the upper two unused bits are floating “don't care” values and can be either 1 or 0. Mask them when reading from addresses 0xAA800048 and 0xAA80004A.

5. Write the selected index number to address 0xAA800046 to see the value in the palette RAM.

6. Read the RED_GREEN palette from 0xAA800048.

7. Mask 0x3F3F to the RED_GREEN palette value to zero out the unused upper two bits in each 6-bit field.

8. Read the blue palette from 0xAA80004A and apply mask 0x003F to zero out the unused upper two bits in that blue palette field. These two bits can be either 1 or 0 when read from the Read Register Port 0 (0048h) and Read Register Port 1 (004Ah). Unused bits may be unstable and must be masked off.

9. Once the palette index is programmed with a color, write the Hardware Cursor Color 0 register.

10. Right shift the selected index number by five bits and write the value into 0xAA800026. These are the upper three bits (IAD7–IAD5) of the selected index number written to the three least significant bits (D2–D0) of the green palette.

11. Left shift the selected index number by 1 bit (multiply by 2) and then write the new value into 0xAA800028. These lower five bits (IAD4–IAD0) of the selected index number are stored in bit positions D5-D1 in the blue palette.

12. The hardware cursor to display color 1 pixel when the bit pattern from Plane 0 and Plane 1 together select color 1 (Plane 0 bit is 1 and Plane 1 bit is 0). This pattern uses the color 1 registers 0x002A and 0x002C to select an address index number from the 18-bit palette RAM entries.

Example Programs

Starting Address of Displayed Memory

```
Hardware Starting Address offset from ZERO beginning of frame buffer memory.
//  Set in the Frame buffer memory starting address offset from ZERO
set_start_addr(int buffer_offset)
{
         short reg_upper2, reg_lower16, tmp2, tmp16;
// print("Starting address offset  "); putnum(buffer_offset);
         buffer_offset >>= 2;               // Divide by 4, drop lower 2 bits (address 1,0)
         tmp16 = buffer_offset&0x00FFFF;    // Prepare 16 bits of data (address 17:2)
         *(CC_ptr+0x0E) = tmp16 ;           // Starting address  17-2 bits into Register 001C.
         tmp2=(buffer_offset & 0x01C0000)>>6;//  Separate upper 3 address bits 20,19,18.
         reg_upper2 = (*(CC_ptr+0x0F) & 0x03FF)| tmp2;
         *(CC_ptr+0x0F) = reg_upper2;     // upper bits address bit 20,19,18 & Logical Line Screen
                                          // Width 8 bits like:0x05, 0x0A, 0x14, 0x28, 0x50, 0xA0
// print(" Reg 001C   "); putnum(*(CC_ptr+0x0E));
// print(" Reg 001E   "); putnum(*(CC_ptr+0x0F));  crlf();
}
```

Hardware Cursor Data Pattern for Memory (↗)

```
#define cursorDataLen  256
const unsigned char cursorData[cursorDataLen] = {
         0x00,0x00,0x00,0x00, 0x3f,0xff,0xff,0xff,       //scanline#0
         0x40,0x00,0x00,0x00, 0x1f,0xff,0xff,0xff,       //scanline#1
         0x60,0x00,0x00,0x00, 0x0f,0xff,0xff,0xff,       //scanline#2
         0x70,0x00,0x00,0x00, 0x07,0xff,0xff,0xff,       //scanline#3
         0x78,0x00,0x00,0x00, 0x03,0xff,0xff,0xff,       //scanline#4
         0x7c,0x00,0x00,0x00, 0x01,0xff,0xff,0xff,       //scanline#5
         0x7e,0x00,0x00,0x00, 0x00,0xff,0xff,0xff,       //scanline#6
         0x7f,0x00,0x00,0x00, 0x00,0x7f,0xff,0xff,       //scanline#7

         0x7f,0x80,0x00,0x00, 0x00,0x3f,0xff,0xff,       //scanline#8
         0x7f,0xc0,0x00,0x00, 0x00,0x1f,0xff,0xff,       //scanline#9
         0x7f,0xe0,0x00,0x00, 0x00,0x0f,0xff,0xff,       //scanline#10
         0x7f,0xf0,0x00,0x00, 0x00,0x07,0xff,0xff,       //scanline#11
         0x7f,0x80,0x00,0x00, 0x00,0x03,0xff,0xff,       //scanline#12
         0x7f,0x00,0x00,0x00, 0x00,0x3f,0xff,0xff,       //scanline#13
         0x7f,0x00,0x00,0x00, 0x00,0x7f,0xff,0xff,       //scanline#14
         0x43,0x80,0x00,0x00, 0x00,0x3f,0xff,0xff,       //scanline#15

         0x03,0x80,0x00,0x00, 0x18,0x3f,0xff,0xff,       //scanline#16
         0x03,0xc0,0x00,0x00, 0x78,0x1f,0xff,0xff,       //scanline#17
         0x01,0xc0,0x00,0x00, 0xfc,0x1f,0xff,0xff,       //scanline#18
         0x01,0xc0,0x00,0x00, 0xfc,0x1f,0xff,0xff,       //scanline#19
         0x01,0xe0,0x00,0x00, 0xfc,0x0f,0xff,0xff,       //scanline#20
         0x00,0xe0,0x00,0x00, 0xfe,0x0f,0xff,0xff,       //scanline#21
         0x00,0xf0,0x00,0x00, 0xfe,0x07,0xff,0xff,       //scanline#22
         0x00,0x70,0x00,0x00, 0xff,0x07,0xff,0xff,       //scanline#23

         0x00,0x60,0x00,0x00, 0xff,0x07,0xff,0xff,       //scanline#24
         0x00,0x00,0x00,0x00, 0xff,0x1f,0xff,0xff,       //scanline#25
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#26
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#27
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#28
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#29
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#30
         0x00,0x00,0x00,0x00, 0xff,0xff,0xff,0xff,       //scanline#31
};
```

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8 System Implementation

This section contains detailed diagrams for system configuration.

Figure 8-1. Single Slot: PC Card or CompactFlash with 68-Pin Adapter

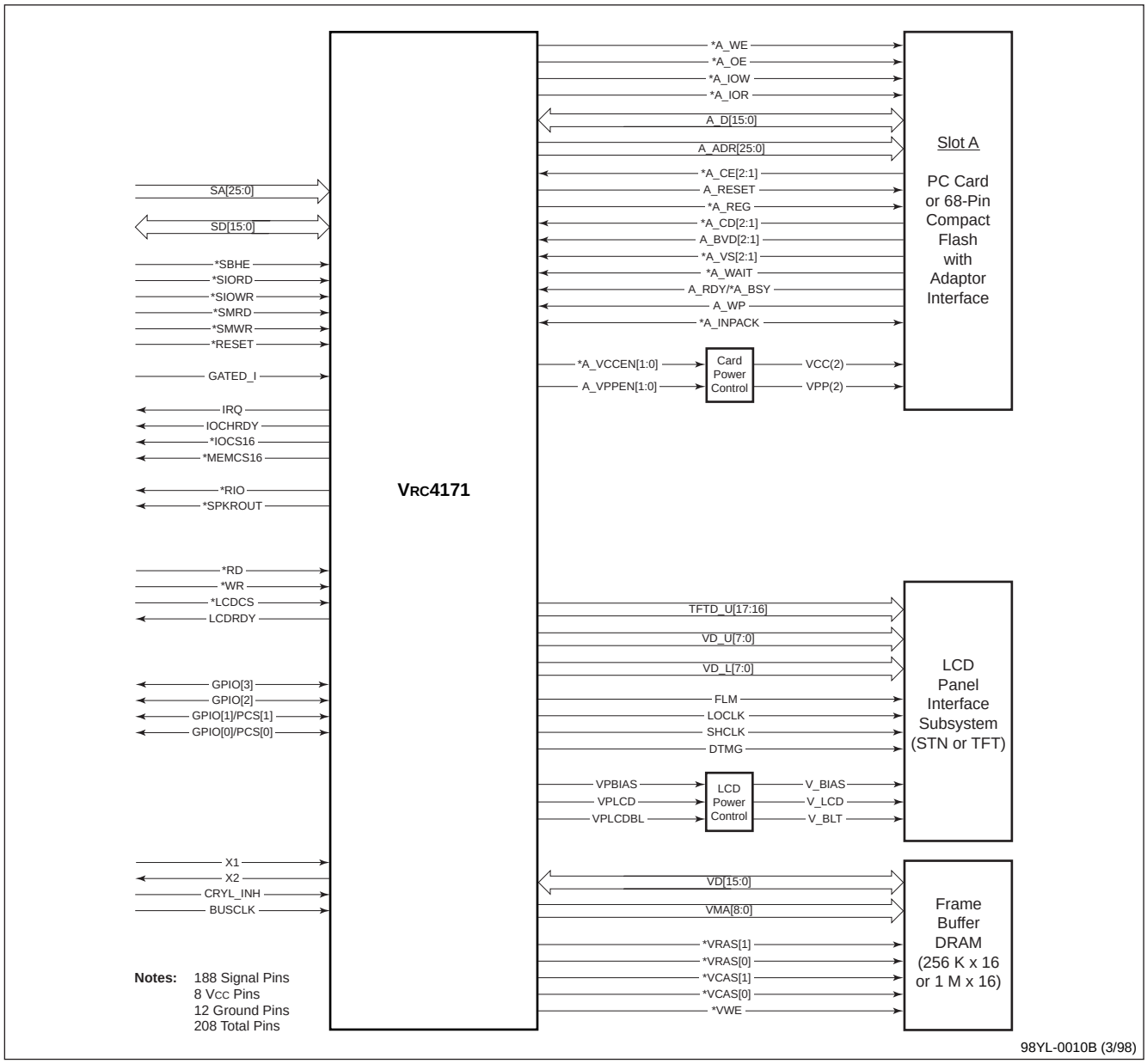


Figure 8-2. Single Slot with 50-Pin CompactFlash

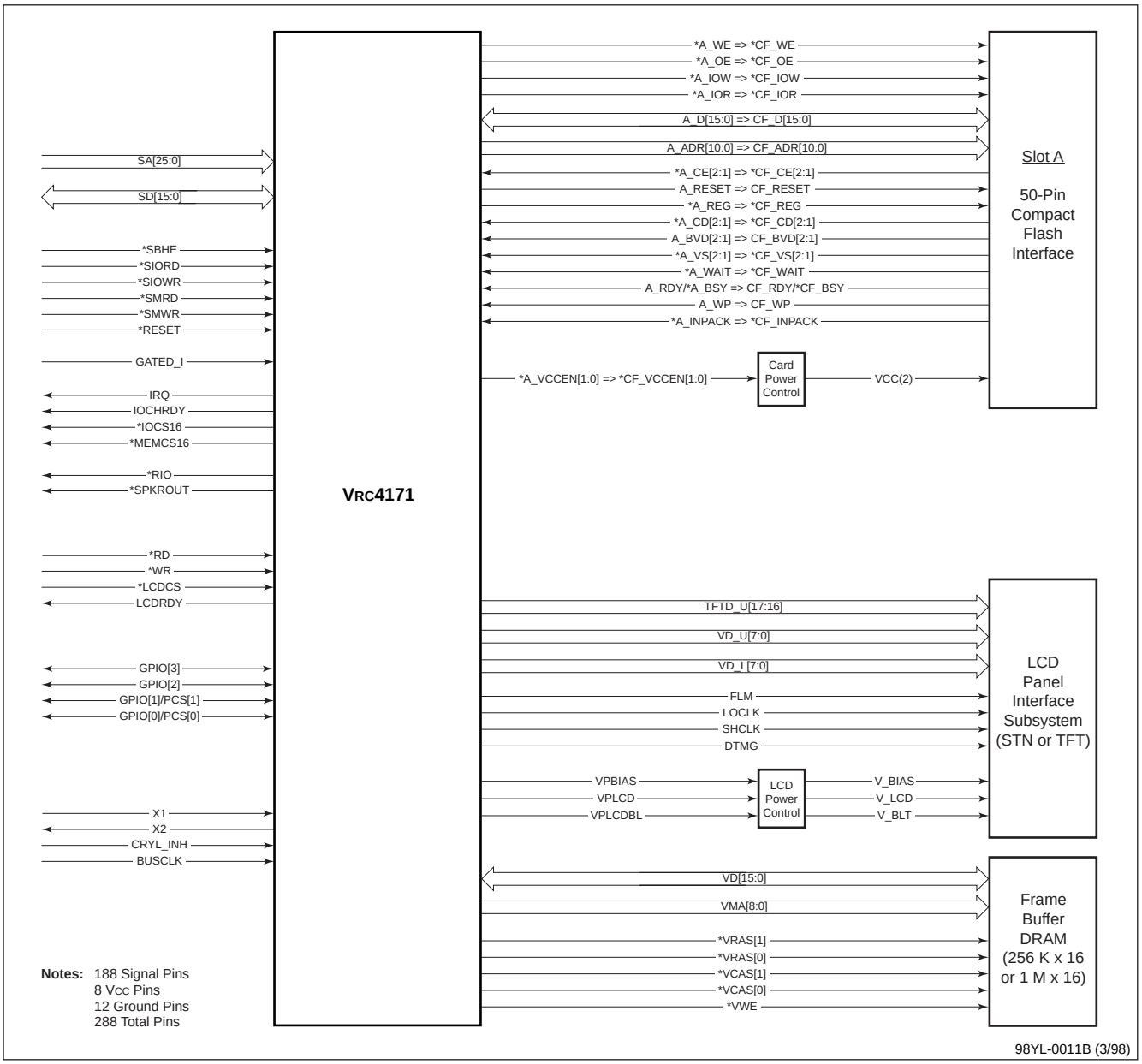


Figure 8-3. Dual Slots with Two PC Cards without External OR Gate

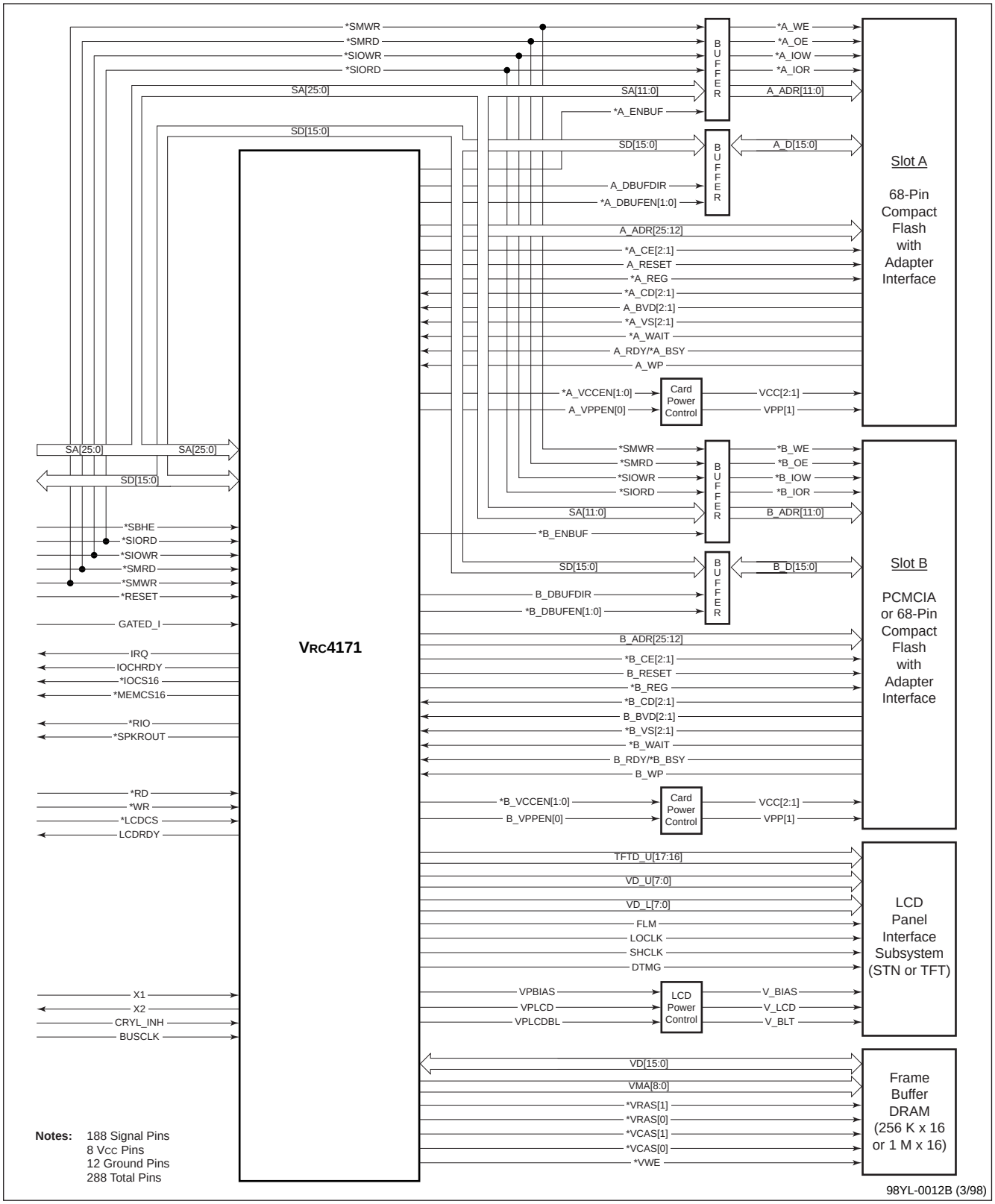
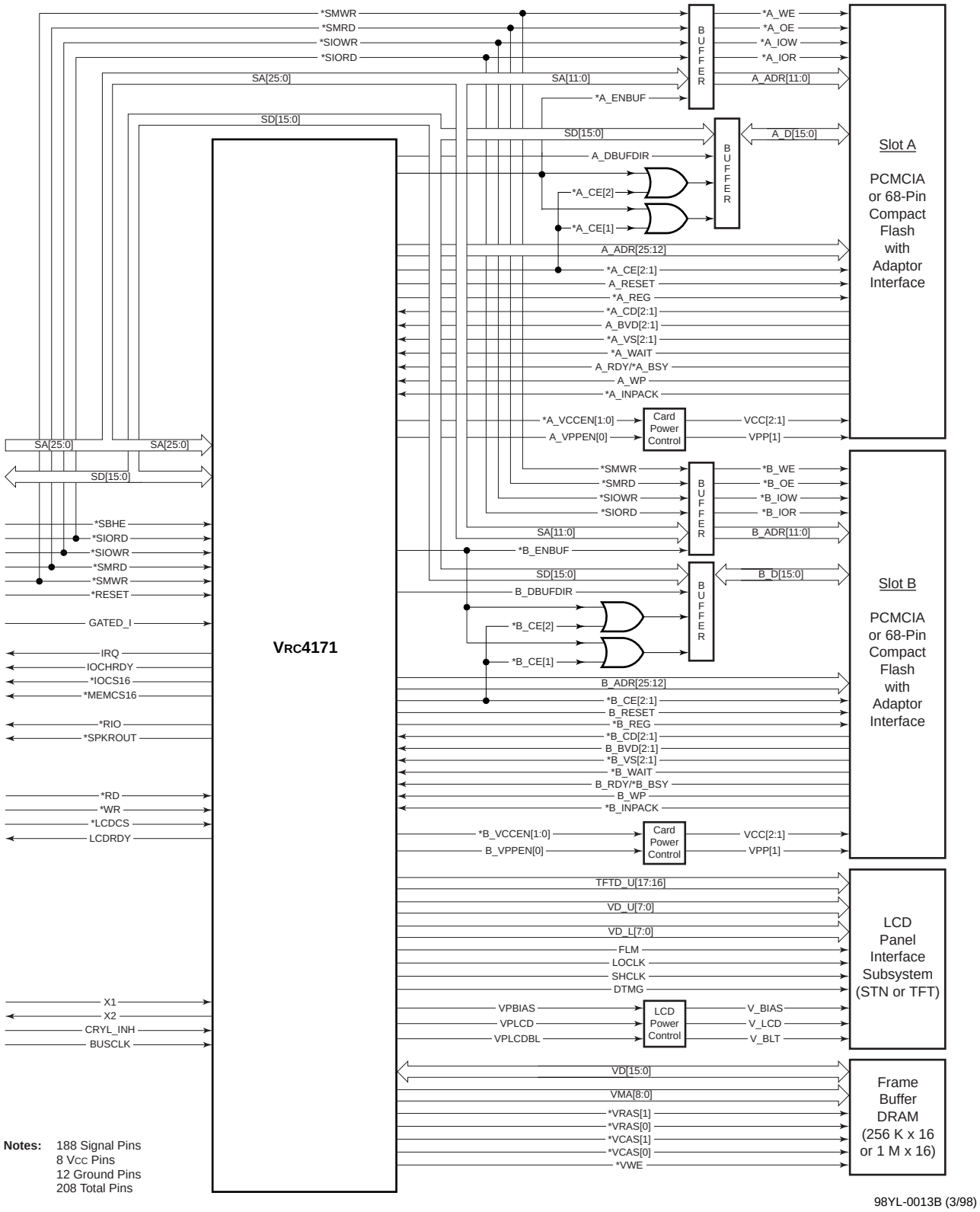


Figure 8-4. Dual Slots with Two PC Cards and External OR Gate



Notes: 188 Signal Pins
8 V_{CC} Pins
12 Ground Pins
208 Total Pins

98YL-0013B (3/98)

Figure 8-5. Dual Slots: PC Card or 50-Pin CompactFlash without External OR Gate

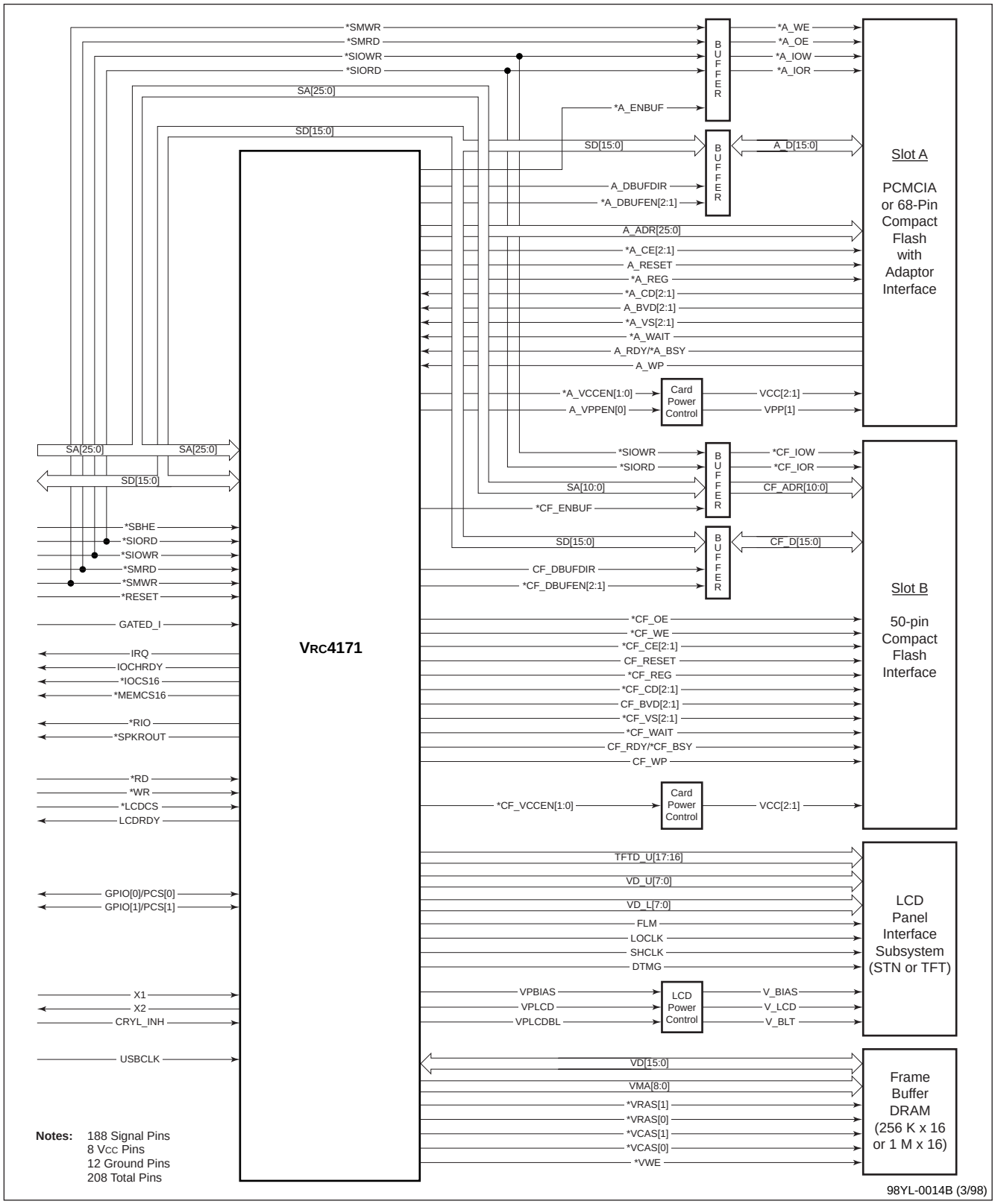


Figure 8-6. Dual Slots: PC Card and 50-Pin CompactFlash with External OR Gate

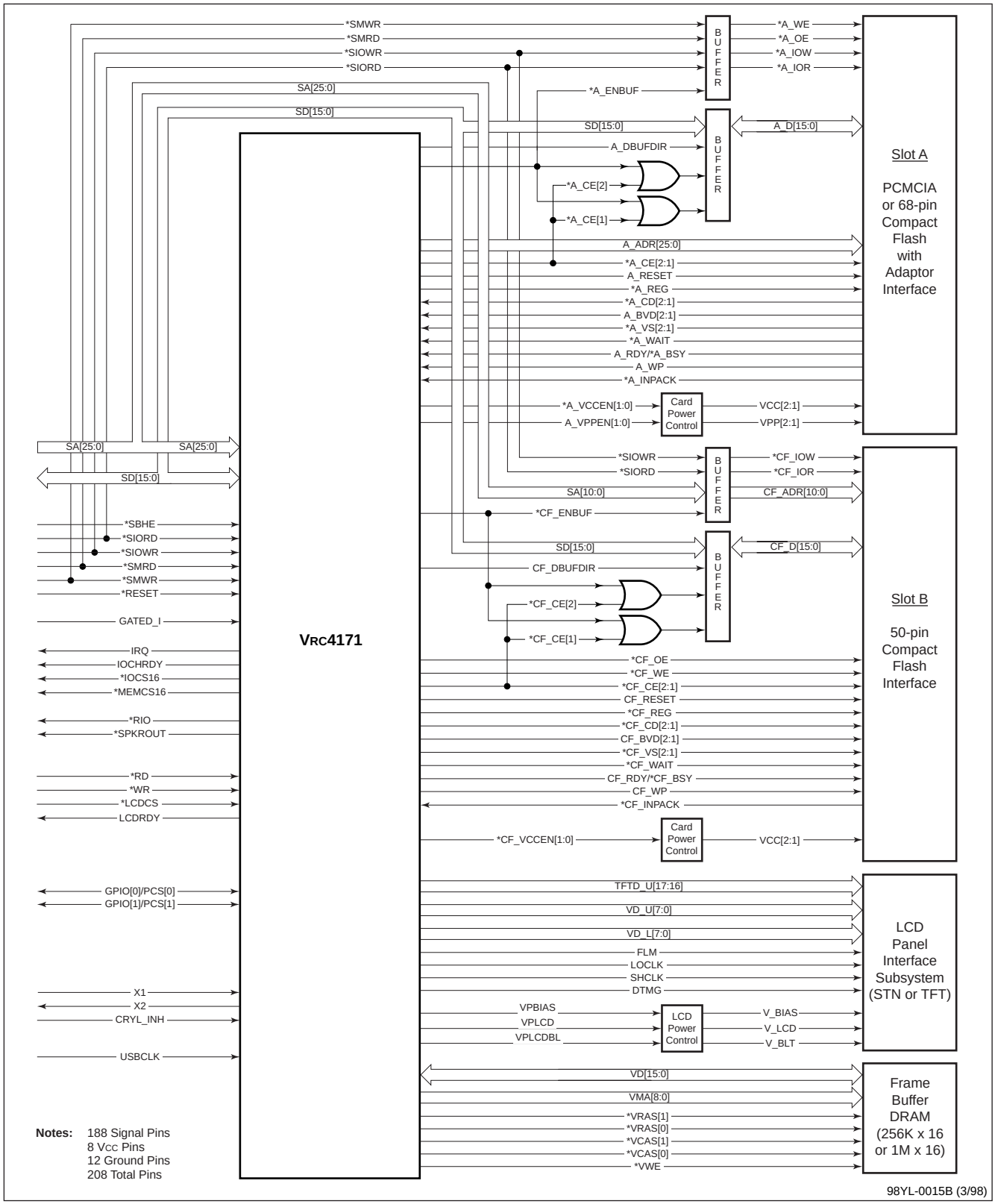
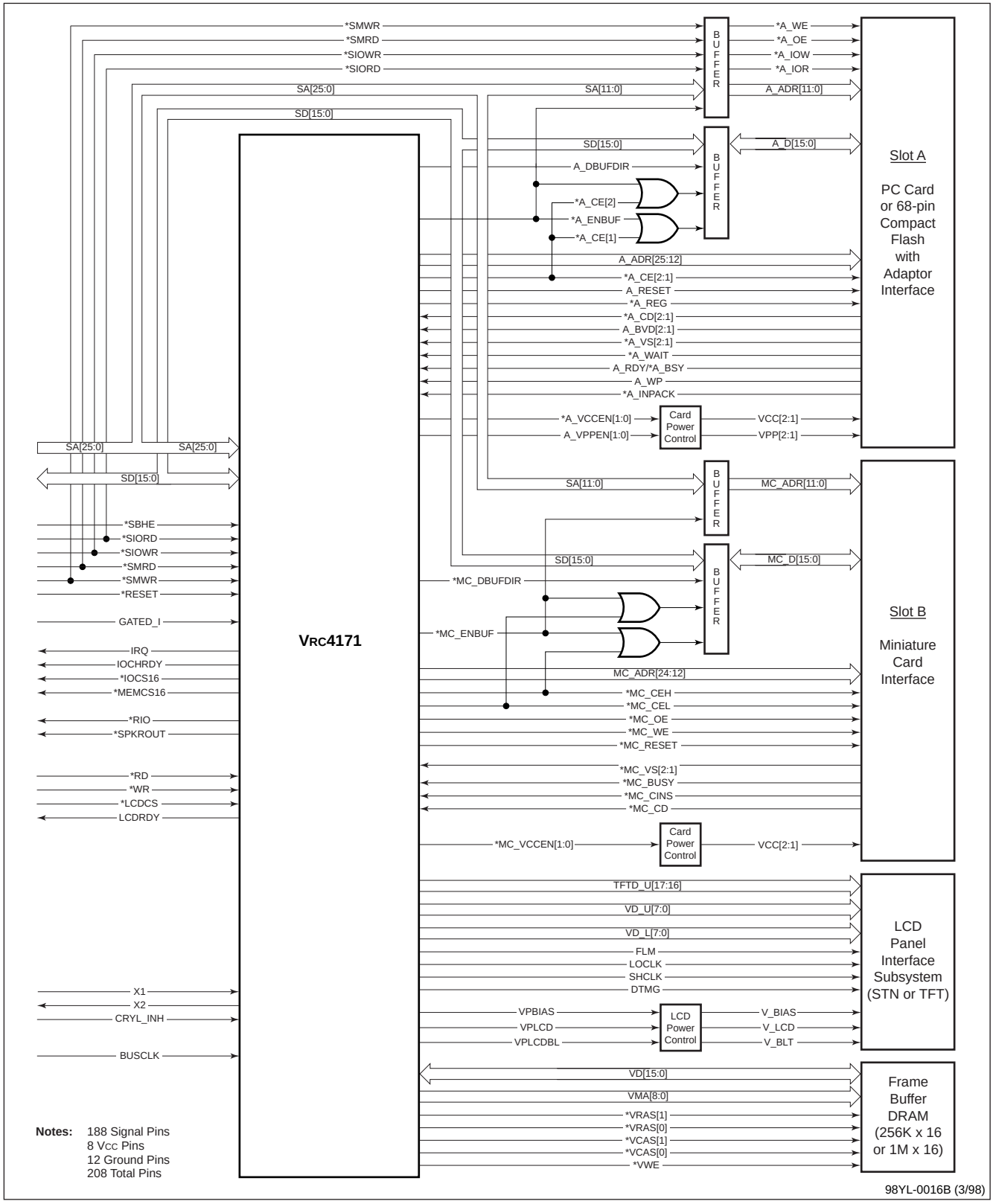


Figure 8-7. Dual Slots: PC Card and 60-Pin Miniature Card



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Design Considerations 9

At power-up, all signals to PC Card slots are tri-stated. To enable operation, the system must first write to Configuration Registers I and II to set up this device for system implementation. During Suspend mode or when the PC Card is not present, the PC Card slot is powered down and card V_{CC} is at 0 volts. External pull-ups are required for some control signals to minimize power consumption. Other signals to the PC Card slots will be tri-stated and will not be driven until a card is inserted while the system is active. If the system is not active when a card is inserted, the system does not wake up automatically; some other event has to wake up the system first.

Single Slot With One 68-Pin PC Card

Table 9-1. Pin Assignments for Slot A

Pin Name	I/O Type	Function	Functional Description	Connect to Card Slot	Pull-Up to Card VCC	Pull-Up to SYS VCC
A_RESET	O–T/5V	PC Card reset output signal	Provides a hard reset to PC Card and clears Card Configuration Option register, placing card into a default state (defined by the PCMCIA 2.1 specification); asserted when PC Card is first inserted into slot, under software control, or when slot is powered up	√	–	–
A_ADR [25:12]	O–T/5V	PC Card address bus	High-order address bus to PC Card; controlled either by enabling memory or I/O windows in ExCA controller	√	–	–
A_BVD[2] (*SPKR)	I–S/5V	PC Card battery voltage detect pin	When A_BVD[2] is negated while A_BVD[1] is still asserted, the PC Card battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, A_BVD[2] may be used to provide a single amplitude digital audio waveform intended to be passed through to the system's speaker without signal conditioning.	√	√	–
A_BVD[1] (*STSCHG / *RI)	I–S/5V	PC Card battery voltage detect pin	If A_BVD[1] is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal can be used to indicate a card status change or as Ring Indicator and is passed through to the *RIO pin.	√	√	–
*A_CD[2:1]	I–S/5V	PC Card detect inputs	Detects proper card insertion	√	–	÷
*A_CE[2:1]	O–T/5V	PC Card chip enable outputs	Active low card enable signals: *A_CE[1] enables even bytes and *A_CE[2] enables odd bytes	√	–	÷
*A_VS[2:1]	I–S/5V	PC Card voltage sense inputs	Used to determine the operating voltage of the PC Card	√	–	÷
*A_REG	O–T/5V	PC Card attribute memory chip select output	Set low to access PC Card attribute memory	√	√	–
A_RDY / *A_BSY (*IREQ)	I–S/5V	PC Card Ready / Busy signal	Memory cards drive this signal low when busy processing a previous write command. I/O PC Cards use this pin as an interrupt request.	√	√	–
*A_WAIT	I–5V	PC Card wait input	Driven by PC Card to delay completion of memory or I/O cycle	√	√	–
A_WP (*IOCS16)	I– 5V	PC Card write protect input	Reflects the status of the PC Card write protect switch. I/O PC Cards assert this signal to indicate that the addressed I/O port is capable of 16-bit access.	√	√	–
*A_VCCEN [1:0]	O–5V	PC Card VCC enable outputs	Power control signals for card VCC	√ (to power switch)	–	–
A_VPPEN [1:0]	O–5V	PC Card programming voltage enable outputs	Power control signals for card VPP	√ (to power switch)	–	–
*A_INPACK	I/O–5V	PC Card input acknowledge signal	Used by some PC Cards during I/O read cycles	√	√	–

Table 9-2. Multifunction Pin Assignments for Slot A

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card Vcc	Pull-Up to SYS Vcc
MFP[35:24]	A_ADR[11:0]	O–T/5 V	PC Card address bus	Lower order address bus to PC Card; internally buffered system address bus	√	–	–
MFP[23:8]	A_D[15:0]	I/O–5V	PC Card data bus	Data bus to the PC Card; internally buffered system data bus	√	–	–
MFP[7]	*A_IOR	O–T/5V	PC Card I/O read strobe	Driven active to read data from the PC Card's I/O space	√	–	–
MFP[6]	*A_IOW	O–T/5V	PC Card I/O write strobe	Driven active to write data to the PC Card's I/O space	√	–	–
MFP[5]	*A_OE	O–T/5V	PC Card output enable	Active low signal used to gate memory reads from memory PC Cards	√	–	–
MFP[4]	*A_WE	O–T/5V	PC Card write enable	Active low signal used to gate memory writes to memory PC Cards	√	–	–
MFP[3:0]	GPIO[3:0] or GPIO[3:2] / *PCS[1:0]	I/O–5V		General-purpose I/O pins or programmable chip select pins depending on system selections	–	–	–

Certain pins defined for PCMCIA compliance can be converted for compliance with a 50-pin CompactFlash socket.

Table 9-3. Pin Assignments for Slot A with 50-Pin CompactFlash

PCMCIA-Specified Signal Names	CompactFlash Equivalent
*A_WE	*CF_WE
*A_OE	*CF_OE
*A_IOW	*CF_IOW
*A_IOR	*CF_IOR
A_D[15:0]	CF_D[15:0]
A_ADR[10:0]	CF_ADR[10:0]
A_ADR[25:11]	No connection
*A_CE[2:1]	*CF_CE[2:1]
A_RESET	CF_RESET
*A_REG	*CF_REG
*A_CD[2:1]	*CF_CD[2:1]
A_BVD[2:1]	CF_BVD[2:1]
*A_VS[2:1]	*CF_VS[2:1]
*A_WAIT	*CF_WAIT
A_RDY/*A_BSY	CF_RDY/*CF_BSY
A_WP	CF_WP
*A_INPACK	*CF_INPACK
*A_VCCEN[1:0]	*CF_VCCEN[1:0]
*A_VPPEN[1:0]	No connection

Dual Slots With Two 68-Pin PC Cards

Pin assignments for slot A are the same as those described in Tables 9-1 through 9-3. Pin assignments for slot B are described in Table 9-4.

Table 9-4. Multifunction Pin Assignments for Slot B (with External OR Gates)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card Vcc	Pull-Up to SYS Vcc
MFP[35:22]	B_ADR [25:12]	O–T/5V	Slot B PC Card address bus	High-order address bus to the PC Card; controlled either by enabling memory or I/O windows in the ExCA controller	√	–	–
MFP[21:20]	*B_CE[2:1]	O–T/5V	Slot B PC Card chip enable outputs	Active low card enable signals: *B_CE[1] enables even bytes and *B_CE[2] enables odd bytes	√	–	√
MFP[19:18]	*B_CD[2:1]	I–S/5V	Slot B PC Card detect inputs	Detects proper card insertion	√	–	√
MFP[17]	B_BVD[2] (*SPKR)	I–S/5V	Slot B PC Card battery voltage detect pin	When B_BVD[2] is negated while B_BVD[1] is still asserted, the PC Card battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, B_BVD[2] may be used to provide a single amplitude digital audio waveform intended to be passed through to the system's speaker without signal conditioning.	√	√	–
MFP[16]	B_BVD[1] (*STSCHG/ *RI)	I–S/5V	Slot B PC Card battery voltage detect pin	If B_BVD[1] is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal can be used to indicate a card status change or as Ring Indicate and is passed through to the *RIO pin.	√	√	–
MFP[15:14]	*B_VS[2:1]	I–S/5V	Slot B PC Card voltage sense input	Used to determine the operating voltage of the PC Card	√	–	√
MFP[13]	B_RDY / *B_BSY (*IREQ)	I–5V	Slot B PC Card Ready / Busy signal	Memory cards drive this signal low when busy processing a previous write command. I/O PC Cards use this pin as an interrupt request.	√	√	–
MFP[12]	*B_WAIT	I – 5 V	Slot B PC Card wait input	Driven by PC Card to delay completion of memory or I/O cycle	√	√	–
MFP[11]	B_WP (*IOCS16)	I–5V	Slot B PC Card write protect input	Reflects the status of the PC Card write protect switch. I/O PC Cards assert this signal to indicate that the addressed I/O port is capable of 16-bit access.	√	√	–
MFP[10]	*B_INPACK	I–5V	Slot B PC Card input acknowledge signal	Used by some PC Cards during I/O read cycles	√	√	–
MFP[9]	B_RESET	O–T/5V	Slot B PC Card reset output signal	Provides hard reset to PC Card and clears Card Configuration Option register, placing card in default state; asserted when PC Card is first inserted into slot, under software control or when slot is powered up	√	–	–
MFP[8]	*B_REG	O–T/5V	Slot B PC Card attribute memory chip select output	Set low to access PC Card attribute memory	√	√	–
MFP[7]	*A_ENBUF	O–5V	Slot A PC Card address and data buffer enable	Active low signal controls external address and data buffer logic; externally ORed with *A_CE[2:1] before connecting to EN pin of data buffer	Directlyt o EN pin of address buffer	–	–
MFP[6]	A_DBUFDIR	O–5V	Slot A PC Card direction control	Set high during a read from the PC Card slot and low during a write to the PC Card slot	Directly to DIR pin of data buffer	–	–

Table 9-4. Multifunction Pin Assignments for Slot B (with External OR Gates) (continued)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card V_{CC}	Pull-Up to SYS V_{CC}
MFP[5]	*B_ENBUF	O–5V	Slot B PC Card address and data buffer enable.	Active low signal controls external address and data buffer logic; externally ORed with *B_CE[2:1] before connecting to EN pin of data buffer	Directly to EN pin of address buffer	–	–
MFP[4]	B_DBUFDIR	O–5V	Slot B PC Card direction control	High during a read from the PC Card slot and low during a write to the PC Card slot	Directly to DIR pin of data buffer	–	–
MFP[3:2]	*B_VCCEN [1:0]	O–5V	Slot B PC Card V_{CC} enable outputs	Power control signals for card V_{CC}	√ (to power switch)	–	–
MFP[1]	B_VPPEN[1]	O–5V	Slot B PC Card programming voltage enable output 1	One of two power control signals for card V_{PP}	√ (to power switch)	–	–
MFP[0]	B_VPPEN[0]	O–5V	Slot B PC Card programming voltage enable output 0	One of two power control signals for card V_{PP}	√ (to power switch)	–	–

Table 9-5. Alternate Pin Assignments (without External OR Gates)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card V_{CC}	Pull-Up to SYS V_{CC}
A_VPPEN[1]	*A_DBUFEN[1]	O–5V	Slot A Data Buffer high byte enable	Internally qualified with *A_ENBUF; low true signal used to enable data buffer on A_D[15:8] during 16-bit PC Card accesses	Directly to EN pin of high-byte data buffer	–	–
*A_INPACK	*A_DBUFEN[0]	O–5V	Slot A data buffer low byte enable	Internally qualified with *A_ENBUF; low true signal used to enable the data buffer on A_D[7:0] during 8- or 16-bit PC Card accesses	Directly to EN pin of low-byte data buffer	–	–
MFP[1]	*B_DBUFEN[1]	O–5V	Slot B data buffer high byte enable	Internally qualified with *B_ENBUF; low true signal used to enable the data buffer on B_D[15:8] during 16-bit PC Card accesses	Directly to EN pin of high-byte data buffer	–	–
MFP[10]	*B_DBUFEN[0]	O–5V	Slot B data buffer low byte enable	Internally qualified with *B_ENBUF; low true signal used to enable the data buffer on B_D[7:0] during 8- or 16-bit PC Card accesses	Directly to EN pin of low-byte data buffer	–	–

Dual Slots
(A: 68-Pin PC Card / B: 50-Pin CompactFlash)

Table 9-6. Multifunction Pin Assignments for Slot B (with External OR Gates)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card Vcc	Pull-Up to SYS Vcc
MFP[35:24]	A_A[11:0]	O–T/5V	Slot A PC Card address bus	Lower order address bus to PC Card; internally buffered system address bus	√	–	–
MFP[23]	*CF_OE	O–T/5V	Slot B CompactFlash card output enable	Active low signal used to read data from the CompactFlash Card in memory mode and to read the CIS and configuration registers. In PC Card I/O mode, this signal is used to read the CIS and configuration registers.	√	–	–
MFP[22]	*CF_WE	O–T/5V	Slot B CompactFlash card write enable	Active low signal used to write data to the CompactFlash card. In PC Card I/O mode it is used to write the configuration registers.	√	–	–
MFP[21:20]	*CF_CE[2:1]	O–T/5V	Slot B CompactFlash card enable	Active low signals used to select the CompactFlash card and to indicate to the card whether a byte or word operation is being performed. *CF_CE[2] accesses the odd byte of the word. *CF_CE[1] accesses the even byte or the odd byte of the word depending on A0 and *CF_CE[2] (16-bit / 8-bit accesses).	√	–	÷
MFP[19:18]	*CF_CD[2:1]	I –S/5V	Slot B CompactFlash card detect inputs	Detects proper card insertion	√	–	÷
MFP[17]	CF_BVD[2] *SPKR	I – S/5 V	Slot B CompactFlash card battery voltage detect input	Driven to high state by the CompactFlash card in both memory and I/O modes. CompactFlash cards do not require a battery and do not support audio function.	√	√	–
MFP[16]	CF_BVD[1] *STSCHG	I – S/5 V	Slot B CompactFlash card battery voltage detect input	Driven to a high state by the Compact Flash card in memory mode since a battery is not required. Signal is asserted low by CompactFlash in I/O mode to alert the host to card status changes.	√	√	–
MFP[15:14]	*CF_VS[2:1]	I –S/5V	Slot B CompactFlash Card Voltage Sense inputs	Compact Flash cards pull *CF_VS[1] to ground so CIS can be read at +3.3V in all modes	√	√	–
MFP[13]	CF_RDY / *CF_BSY (*IREQ)	I –5V	Slot B CompactFlash Card Ready / *Busy low signal	In memory mode, cards drive this signal low when busy processing a previous write command. In I/O mode, cards use this pin as an interrupt request.	√	√	–
MFP[12]	*CF_WAIT	I –5V	Slot B CompactFlash card wait input	Driven by CompactFlash card to delay completion of memory or I/O cycle	√	√	–
MFP[11]	CF_WP (*IOCS16)	I –5V	Slot B CompactFlash card write protect input	CompactFlash cards drive *CF_WP low after completion of reset initialization sequence in memory mode. For I/O operation, used as *IOCS16 to indicate a 16-bit access at the addressed port.	√	√	–
MFP[10]	*CF_INPACK	I –5V	Slot B CompactFlash card input acknowledge signal	Not used in memory mode. In I/O mode, asserted by CompactFlash card when the card is selected and responding to an I/O read cycle at the addressed port.	√	√	–
MFP[9]	CF_RESET	O–T/5V	Slot B CompactFlash card reset signal	Active high signal used to reset the CompactFlash card	√	-	-
MFP[8]	*CF_REG	O–T/5V	Slot B CompactFlash card attribute memory chip select output	Signal is set low to access Compact Flash card attribute memory	√	√	–
MFP[7]	*A_ENBUF	O–T/5V	Slot A PC Card address and data buffer enable	Active low signal controls external data buffer logic; externally ORed with *A_CE[2:1] before connecting to EN pin of data buffer	Directly to EN pin of address buffer	–	–

Table 9-6. Multifunction Pin Assignments for Slot B (with External OR Gates) (continued)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card V_{CC}	Pull-Up to SYS V_{CC}
MFP[6]	A_DBUFDIR	O–5V	Slot A PC Card direction control	High during a read from the PC Card slot and low during a write to the PC Card slot.	**Note 1**	–	–
MFP[5]	*CF_ENBUF	O–5V	Slot B CompactFlash card address and data buffer enable	Active low signal controls external address and data buffer logic; externally ORed with *CF_CE[2:1] before connecting to EN pin of data buffer		–	–
MFP[4]	CF_DBUFDIR	O–5V	Slot B CompactFlash card direction control	High during a read from the CompactFlash card slot and low during a write to the CompactFlash card slot	**Note 1**	–	–
MFP[3:2]	*CF_VCCEN [1:0]	O–5V	Slot B CompactFlash card V_{CC} enable outputs	Power control signals for card V_{CC}	√ (to power switch)	–	–
MFP[1]	GPIO[1] / *PCS[1]	I/O–5V	Variable	General-purpose I/O pin or programmable chip select pin	–	–	–
MFP[0]	GPIO[0] / *PCS[0]	I/O–5V	Variable	General-purpose I/O pin or programmable chip select pin	–	–	–

Notes: **1.** Connects directly to DIR pin of data buffer.
2. Connects directly to EN pin of address buffer.

Table 9-7. Alternate Pin Assignments (without External OR Gates)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card V_{CC}	Pull-Up to SYS V_{CC}
A_VPPEN[1]	*A_DBUFEN[1]	O–5V	Slot A data buffer high byte enable	Internally qualified with *A_ENBUF; low true signal used to enable the data buffer on A_D[15:8] during 16-bit PC Card accesses	**Note 1**	–	–
*A_INPACK	*A_DBUFEN[0]	I/O–5V	Slot A data buffer low byte enable	Internally qualified with *A_ENBUF; low true signal used to enable the data buffer on A_D[7:0] during 8- or 16-bit PC Card accesses	**Note 2**	–	–
MFP[1]	*CF_DBUFEN[1]	O–5V	Slot B data buffer high byte enable	Internally qualified with *B_ENBUF; low true signal used to enable the data buffer on CF_D[15:8] during 16-bit PC Card accesses	**Note 1**	–	–
MFP[10]	*CF_DBUFEN[0]	I/O–5V	Slot B data buffer low byte enable	Internally qualified with *CF_ENBUF; low true signal used to enable the data buffer on CF_D[7:0] during 8- or 16-bit PC Card accesses	**Note 2**	–	–

Notes: **1.** Connects directly to EN pin of the high-byte data buffer.
2. Connects directly to EN pin of the low-byte data buffer.

Dual Slots (A: 68-Pin PC Card / B: 60-Pin Miniature Card)

For Miniature Card applications, only ROM and flash ROM are supported for DRAMs and SRAMs.

Table 9-8. Multifunction Pin Assignments for Slot B (With External OR Gates)

Pin Name	Signal Name	I/O Type	Function	Description	Connect to Card Slot	Pull-Up to Card Vcc	Pull-Up to SYS Vcc
MFP[35:22]	MC_ADR [24:11]	O–T/5V	Miniature Card address bus	.	√	–	–
MFP[21]	*MC_OE	O–T/5V	Slot B Miniature Card output enable	Active low signal	√	–	–
MFP[20]	*MC_WE	O–T/5V	Slot B Miniature Card write enable	Active low signal	√	–	–
MFP[19]	*MC_CEH	O–T/5V	Slot B Miniature Card high byte enable	Active low signal	√	–	–
MFP[18]	*MC_CEL	O–T/5V	Slot B Miniature Card low byte enable	Active low signal	√	–	–
MFP[17]	NC	–		–	–	–	–
MFP[16]	NC	–		–	–	–	–
MFP[15:14]	*MC_VS[2:1]	I –S/5V	Slot B Miniature Card voltage sense inputs		√	-	–
MFP[13]	*MC_BUSY	I –5V	Slot B Miniature Card Ready/*Busy signal		√	√	–
MFP[12]	NC	–		–	–	–	–
MFP[11]	NC	–		-	–	–	–
MFP[10]	NC	–		-	–	–	–
MFP[9]	*MC_RESET	O–T/5V	Slot B Miniature Card reset signal	Active low signal	√	–	–
MFP[8]	NC	–		–	–	–	–
MFP[7]	*A_ENBUF	O–T/5V	Slot A PC Card address and data buffer enable	Active low signal controls external data buffer logic; externally ORed with *A_CE[2:1] before connecting to EN pin of data buffer	Directly to EN pin of address buffer	–	–
MFP[6]	A_DBUFDIR	O–5V	Slot A PC Card direction control	High during a read from the PC Card slot and low during a write to the PC Card slot	Directly to DIR pin of data buffer	–	–
MFP[5]	*MC_ENBUF	O–5V	Slot B Miniature Card address and data buffer enable	Active low signal controls external address and data buffer logic; externally ORed with *MC_CEH and *MC_CEL before connecting to EN pin of data buffer	Directly to EN pin of address buffer	–	–
MFP[4]	MC_ DBUFDIR	O–5V	Slot B Miniature Card direction control	High during a read from the Miniature Card slot and low during a write to the Miniature Card slot	Directly to DIR pin of data buffer	–	–
MFP[3:2]	*MC_VCCEN [1:0]	O–5V	Slot B Miniature Card Vcc enable outputs	Power control signals for card Vcc	√ (to power switch)	–	–
MFP[1]	*MC_CD	I –5V	Slot B Miniature Card card detection input	Active low signal	–	–	–
MFP[0]	*MC_CINS	I –5V	Slot B Miniature Card card insertion input	Active low signal	–	–	–

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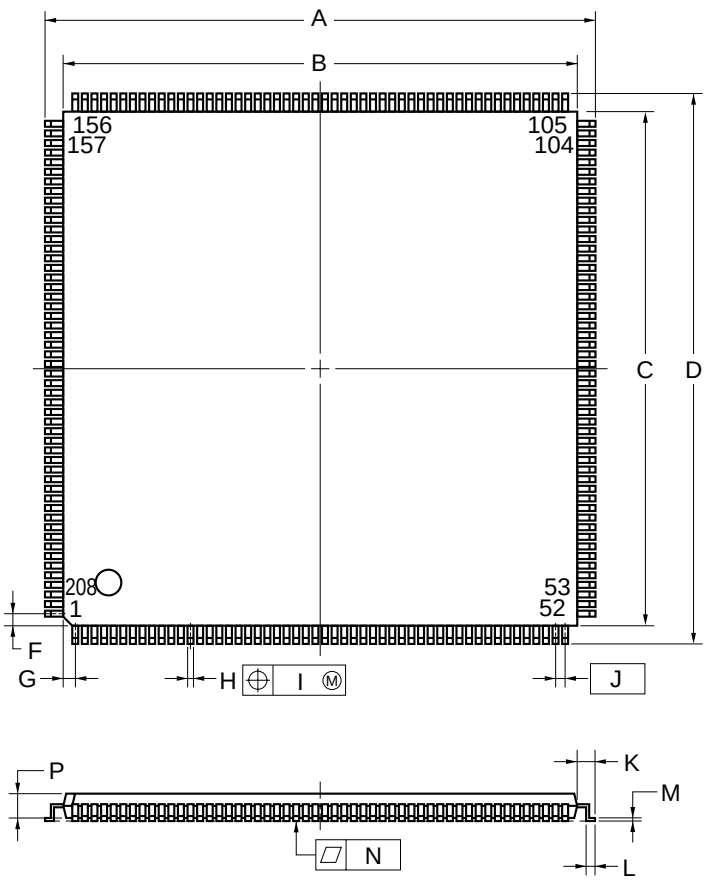
Package Specifications 10

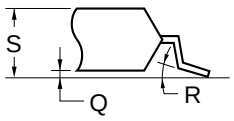
Figure 10-1. 208-Pin LQFP



ITEM	MILLIMETERS	INCHES
A	30.0±0.2	1.181±0.008
B	28.0±0.2	$1.102^{+0.009}_{-0.008}$
C	28.0±0.2	$1.102^{+0.009}_{-0.008}$
D	30.0±0.2	1.181±0.008
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S208GD-50-8EU-2

detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

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- **Device availability**
- **Ordering information**
- **Product release schedule**
- **Availability of related technical literature**
- **Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)**
- **Network requirements**

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