OPTi Inc.
2525 Walsh Avenue
Santa Clara, CA 95051
(408) 980-8178
Fax: (408) 980-8860

Errata

Product Name: 82C264 GUI Accelerator
Document: 82C264 Data Book
(PN: 912-3000-030 Revision 1.0)
Date: July 24, 1995

Page 12
The power and signal ground interface table on page twelve incorrectly lists the pin numbers for AGNDM and AGNDV. The correct numbers should be as shown:

3.1.5 Power and Signal Ground Interface

Pin Name	Pin	Type	Description
AGNDM	45	GND	Analog ground for the memory clock Phase Lock Loop (PLL).
AGNDV	111	GND	Analog ground for the video clock PLL.
AVDDV	113	PWR	Analog power for the video clock PLL.
GND	5, 19, 35, 62, 76, 85, 99, 106, 110, 120, 136, 154	GND	Ground pins.
RVDD	117	PWR	Power for RAMDAC RAM.
VAA	121	PWR	Power supply for the internal DAC of the RAMDAC. The voltage is 5V + 10%.
VGNDA	125	GND	Analog ground for the DAC.

9004196 0000821 423

Powered by ICminer.com Electronic-Library Service CopyRight 2003

OPTi Inc.
2525 Walsh Avenue
Santa Clara, CA 95051
(408) 980-8178
Fax: (408) 980-8860

Addendum

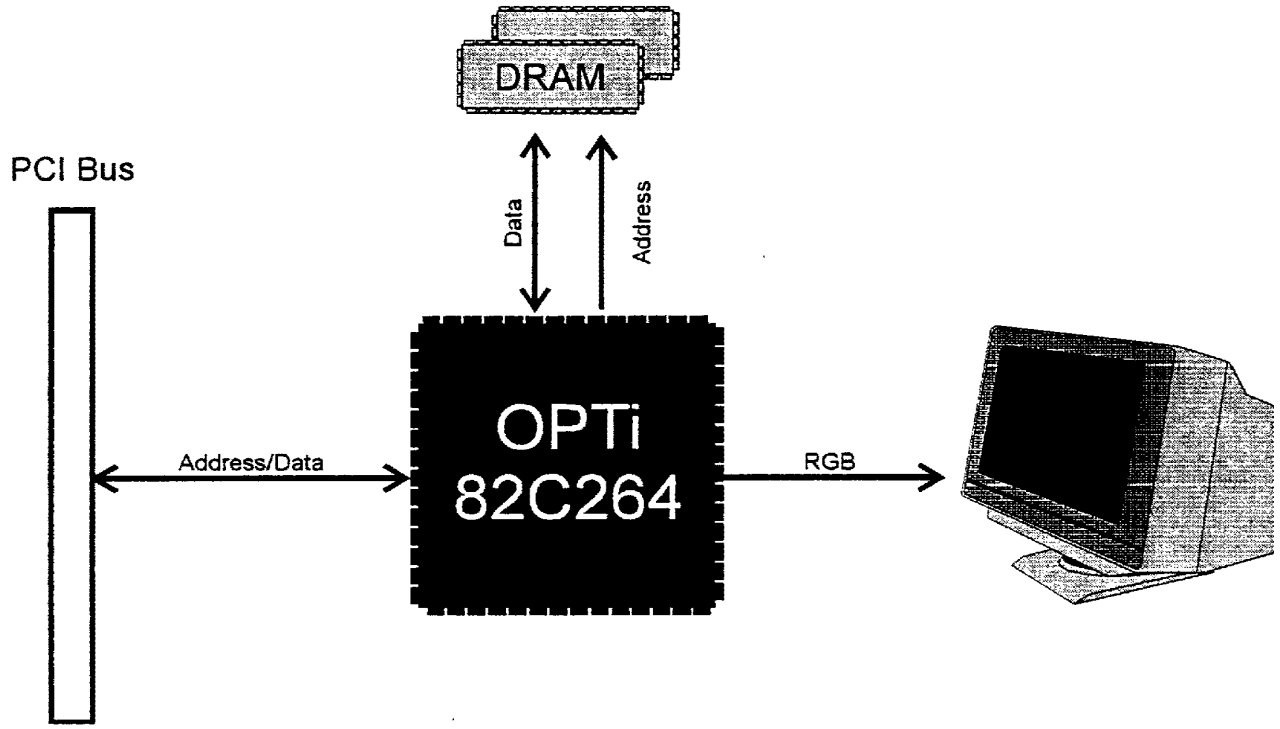
Product Name: 82C264 GUI Controller
Document: Design Reference Manual (PN: 912-6000-002, Rev. 1.0)
Date: June, 1995

The following changes should be made to the 82C264 GUI Controller Reference Design Manual, dated March, 1995.

Page 1

The System Block Diagram should be shown as follows:

Figure 1-1 OPTi 82C264 System Block Diagram

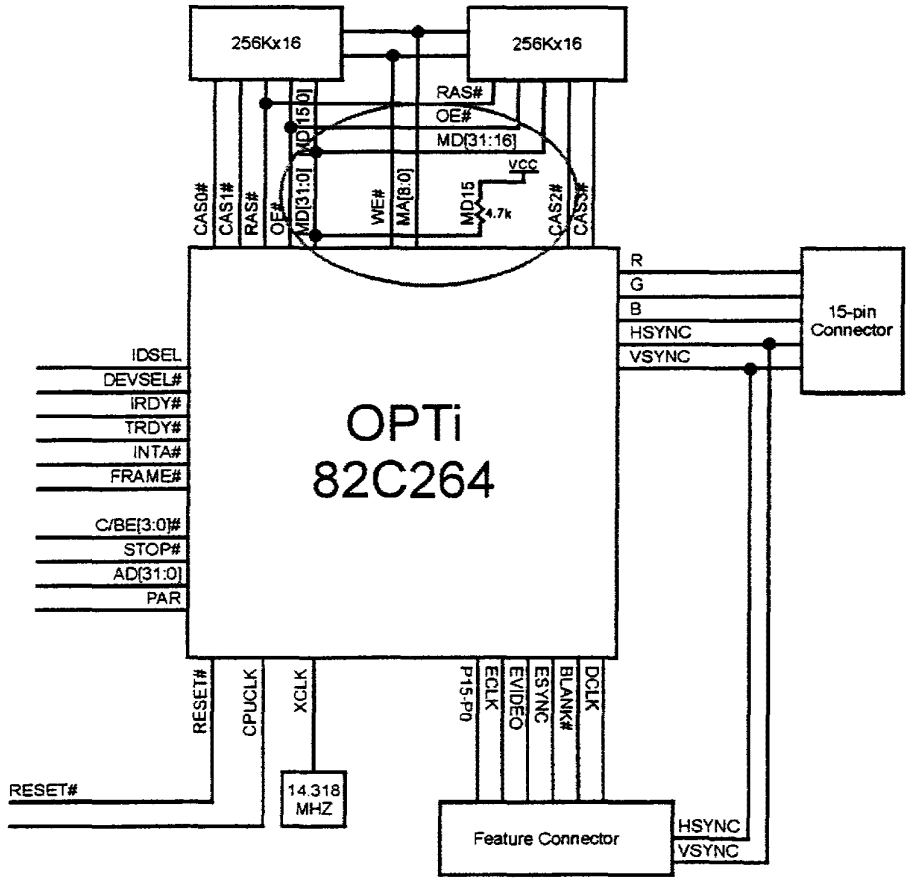


9004196 0000822 36T

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Page 4

The PCI-Bus example controller block diagram should be shown as follows (changes are shown in circle):



Page 5

Table 2-1 has the logical values for MD15 reversed. They should be listed as:

Table 2-1 MD31-MD0 Definitions at Reset

MD	Logical Level	Definition
MD15	0	Select dual WE# DRAM
	1	Select dual CAS# DRAM

Page 10

The description of CAS# in the Memory Interface section (3.1.2) should refer to signal MD15, not RAMCNF, being pulled low to change the function of this pin to WE# for display memory.

9004196 0000823 2T6

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Page 11

The description of WE3#-WE0# in the Memory Interface section (3.1.2) should be changed to the following:

Pin Name	Pin	Type	Description
WE3#-WE0#	93, 82, 72, 59	O	DRAM Write Enables. When MD15 signal is pulled low, these pins are write enable signals for the display memory (for 256Kx4 or 256Kx16 dual WE DRAM). When MD15 signal is pulled high, these pins function as CAS# signals for display memory (for 256Kx16 dual CAS DRAM).

Page 18

Change the values for 800x600, 16M (24) to Yes in Table 4-2, CRT Display Resolutions.

9004196 0000824 132

Powered by ICminer.com Electronic-Library Service CopyRight 2003

OPTi

82C264

GUI Accelerator

Data Book

Revision 1.0
912-3000-030
March, 1995

9004196 0000825 079

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Copyright

Copyright © 1994, OPTi Inc. All rights reserved. No part of this publication may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual, or otherwise, without the prior written permission of OPTi Incorporated, 2525 Walsh Avenue, Santa Clara, CA 95051.

Disclaimer

OPTi Inc. makes no representations or warranties with respect to the design and documentation herein described and especially disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, OPTi Inc. reserves the right to revise the design and associated documentation and to make changes from time to time in the content without obligation of OPTi Inc. to notify any person of such revisions or changes.

Trademarks

OPTi and OPTi Inc. are registered trademarks of OPTi Incorporated.

VESA is a trademark of the Video Electronic Standards Association (VESA).
All other trademarks and copyrights are the property of their respective holders.

OPTi Inc.
2525 Walsh Avenue
Santa Clara, CA 95051
Tel: (408) 980-8178
Fax: (408) 980-8860
BBS: (408) 980-9774

9004196 0000826 T05

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table of Contents

9004196 0000827 941

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table of Contents

9004196 0000828 888

Powered by ICminer.com Electronic-Library Service CopyRight 2003

9004196 0000829 714

Powered by ICminer.com Electronic-Library Service CopyRight 2003

List of Figures

9004196 0000830 436

Powered by ICminer.com Electronic-Library Service CopyRight 2003

List of Tables

9004196 0000831 372

Powered by ICminer.com Electronic-Library Service CopyRight 2003

1.0 Introduction

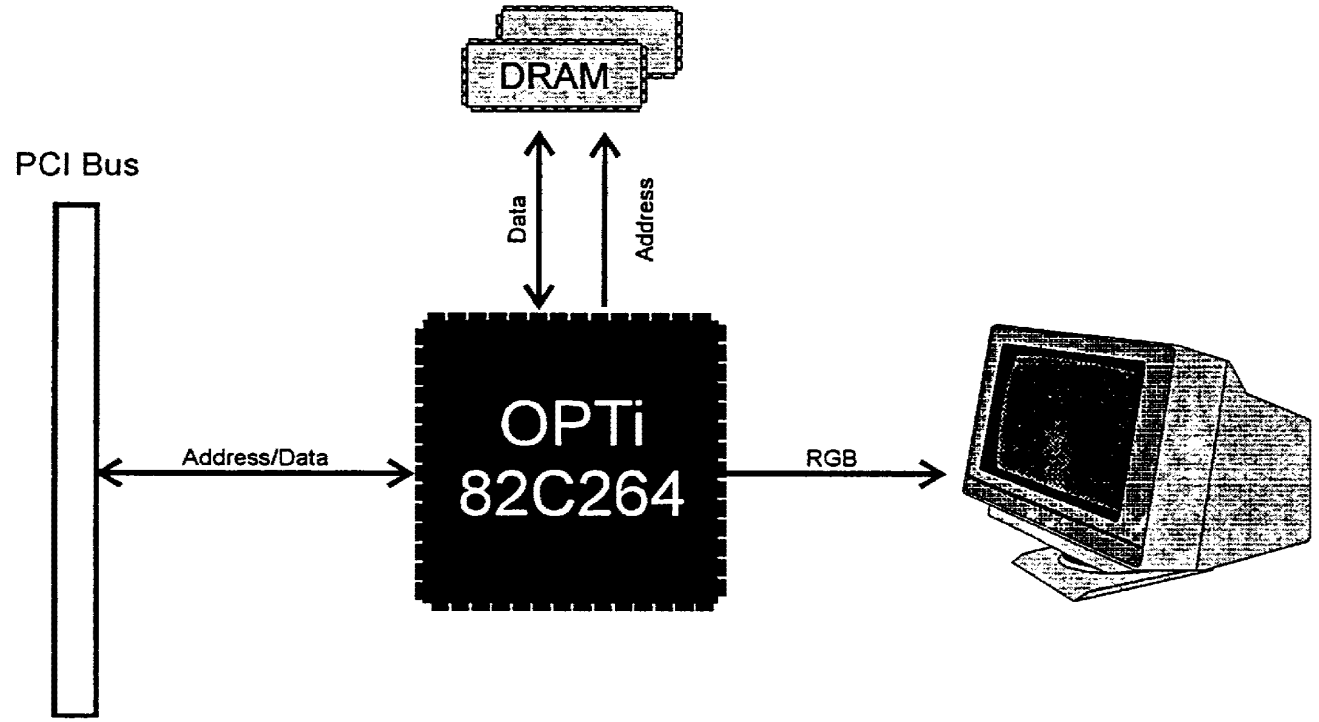
The OPTi 82C264 provides an unmatched price/performance VGA solution for personal computers. The 82C264 offers high performance and full integration as part of a highly integrated PCI graphics subsystem.

High performance is made possible by a built-in fixed function graphics accelerator. The accelerator supports BitBlt, polygon fill, line draw, color expansion, and clipping. Acceleration is supported for pixel depths of 8, 15, 16, and 24 bits/pixel. Hardware cursor support further enhances performance in GUI environments by removing software cursor overhead.

The RAMDAC and clock synthesizer are built into the 82C264. No external logic is required to connect to the PCI bus. A complete VGA video subsystem can be implemented with two 256Kx16 DRAM chips. CRT display resolutions up to 1280x1024-256 colors are supported.

The OPTi 82C264 is 100% register level compatible with the IBM VGA standard. OPTi supplies a fully compatible VGA/VESA BIOS, drivers for common applications and operating systems, such as Windows, Windows95 and OS/2, as well as OEM and end-user level utility software.

Figure 1-1 OPTi 82C264 System Block Diagram



9004196 0000832 209

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2.0 Features

2.1 Features	2.2 Benefits
Integrated true color RAMDAC and clock.	Full integration. One chip solution.
Built-in graphics accelerator. Supports: • Polygon fill • Line draw • Color expansion • Clipping	Superior performance.
32-bit direct interface with PCI bus.	No external glue logic. Reduced footprint design. Cost savings.
Flexible DRAM configurations: • Two or four 256Kx16 DRAMs • Eight or sixteen 256Kx4 DRAMs.	Design flexibility for 1MB or 2MB implementations. Facilitates cost-effective graphics frame buffer solutions.
Hardware cursor (32x32x2 and 64x64x2 cursor sizes supported).	No distracting cursor flicker. Improved performance.
Supports up to 16.8 million colors.	Superior color display quality.
Programmable linear addressing.	Eliminates bank switching.
100% hardware/BIOS compatible with IBM VGA standard.	Allows use of any VGA compatible software with the video subsystem.
Multimedia Features • VAFC compatible feature connector • Overlay • Genlock	Multimedia ready.
VESA Display Data Channel support.	Plug and play ready.
DPMS support.	Green PC compatible.

2.3 Architecture

The OPTi 82C264 contains the following major functional modules:

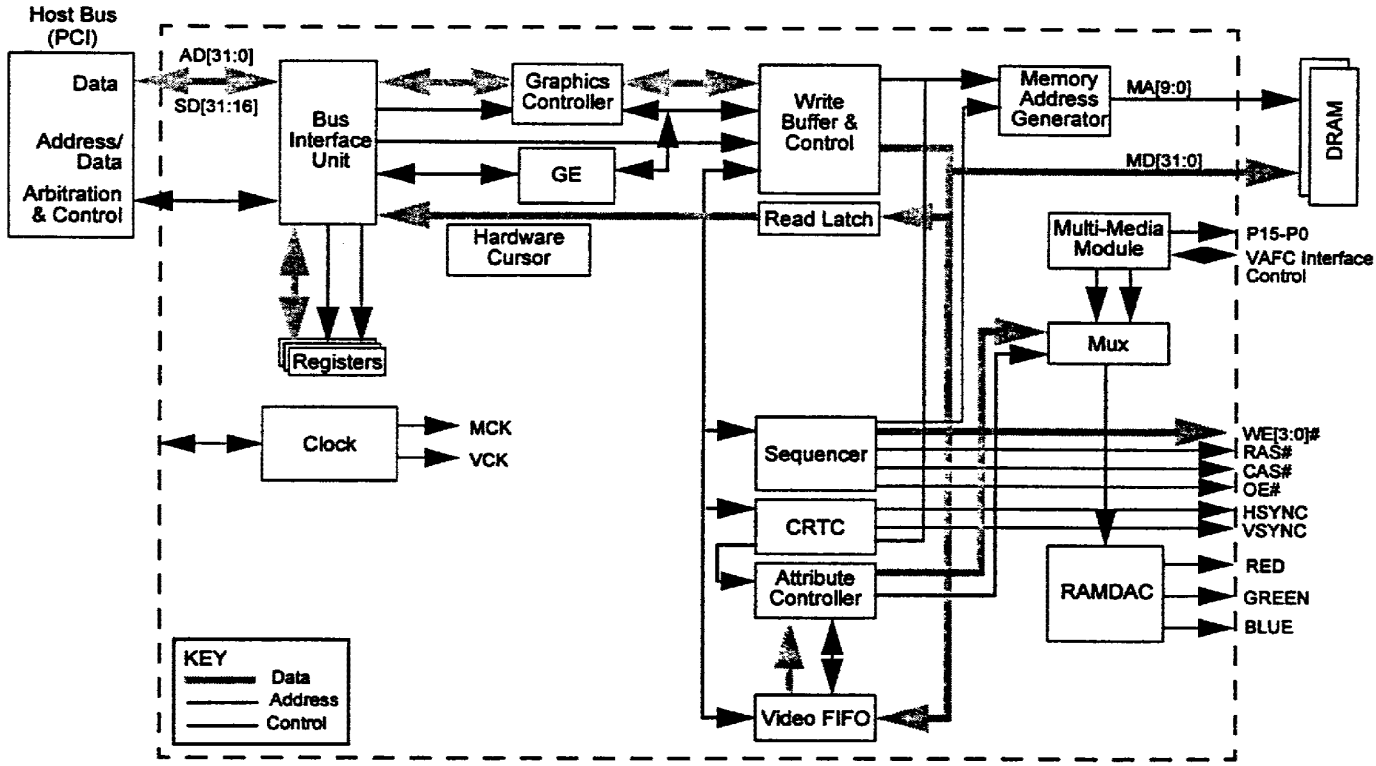
- Bus Interface Unit
- Write Buffer Control Unit
- Graphic Controller
- Memory Sequencer
- Video FIFO
- CRT Controller
- Attribute Controller
- GUI Engine
- Hardware Cursor
- Pop-up Icon
- RAMDAC
- DPMS
- Clock Synthesizer
- Multi-media Module

The function of each module is described in Section 4.0, *Bus Interface Unit*.

9004196 0000833 145

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 2-1 OPTi 82C264 Functional Block Diagram

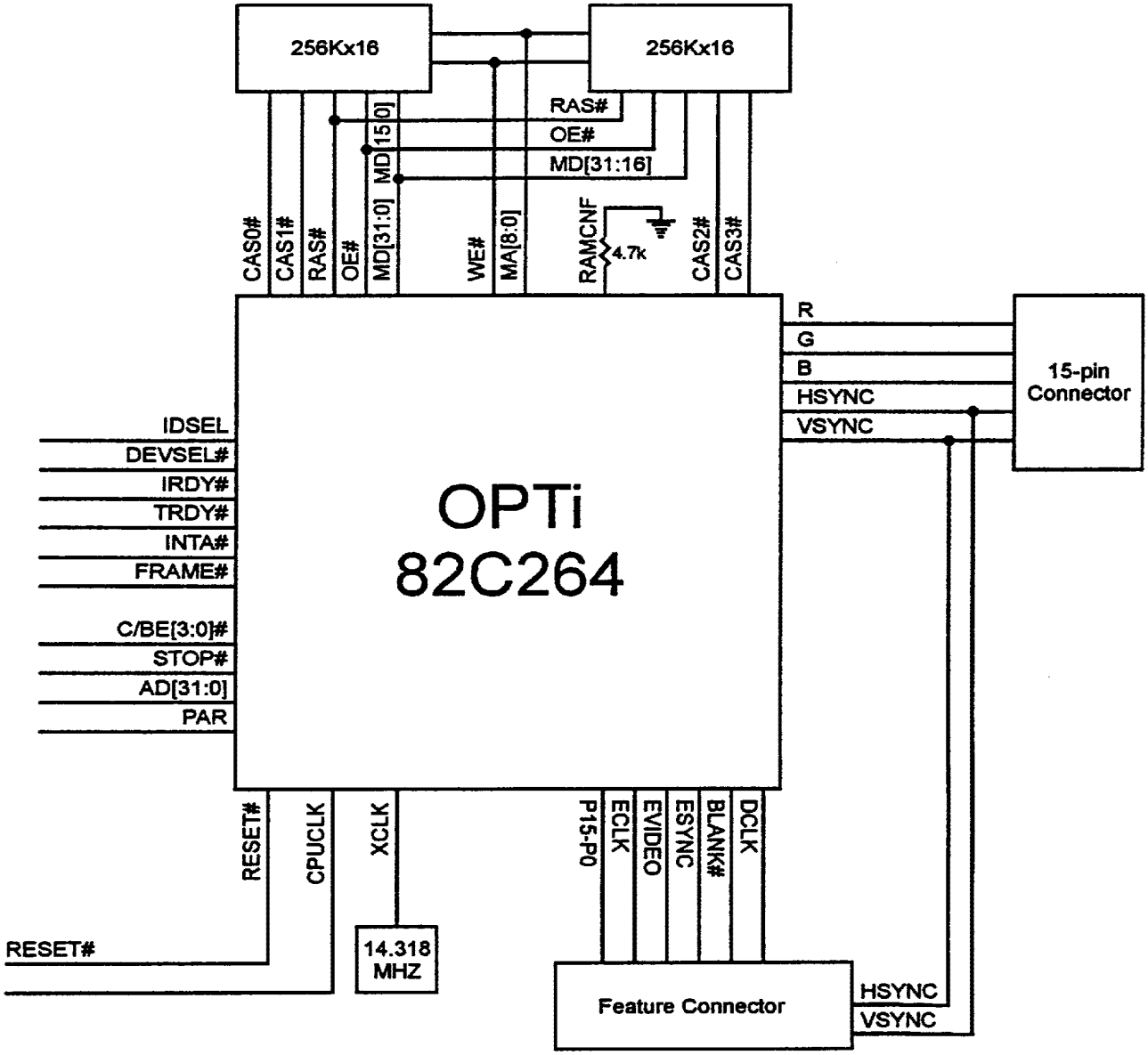


9004196 0000834 081

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2.4 Example Controller Block Diagram

Figure 2-2 PCI-Bus Solution with 16-bit Feature Connector



9004196 0000835 T18

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2.4.1 Definitions of MD31-MD0 at System Reset

Table 2-1 lists the definitions of MD31-MD0 at system reset. To set the given MD bit to a logical 1, pull high through a 4.7Kohm resistor. To set the given bit to a logical 0, pull low through a 4.7KΩ resistor.

NOTE MD31-MD16 do not directly set any register bits in the chip. The OPTi BIOS reads MD31-MD16 and then sets the 82C264 register bits appropriately.

Table 2-1 MD31-MD0 Definitions at Reset

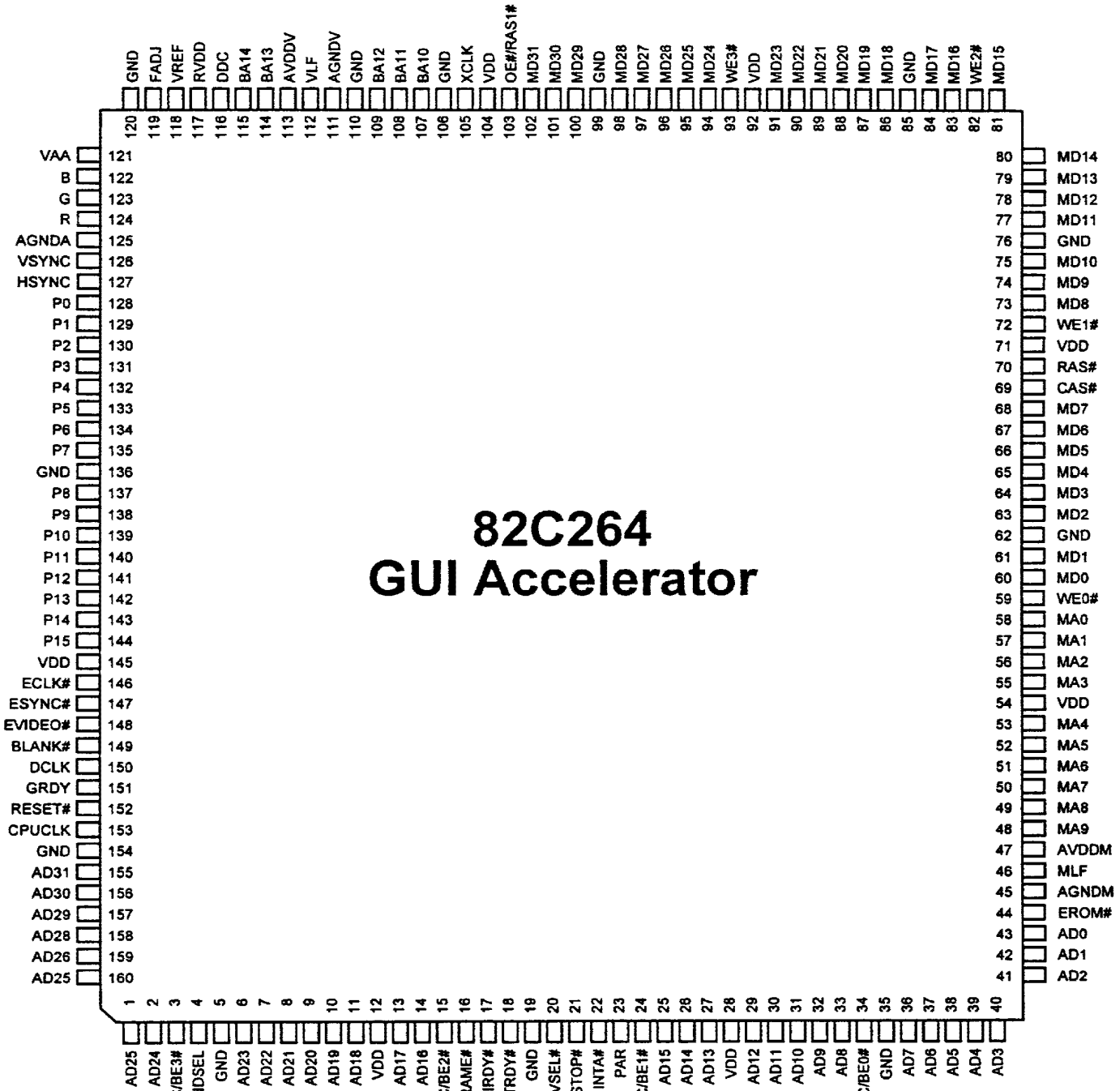
MD	Logical Level	Definition
MD31	1	Enables Feature Connector.
	0	Disables Feature Connector.
MD30	1	Enable PCI BIOS interface.
	0	Disable PCI BIOS interface.
MD29-16	–	Reserved
MD15	1	Select dual WE# DRAM
	0	Select dual CAS# DRAM
MD14	1	46E8 is the VGA enable port
	0	3C3 is the VGA enable port
MD13-0	–	Reserved

9004196 0000836 954

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.0 Signal Descriptions

Figure 3-1 Pin Diagram



9004196 0000837 890

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table 3-1 Numerical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD25	41	AD2	81	MD15	121	VAA
2	AD24	42	AD1	82	WE2#	122	B
3	C/BE3#	43	AD0	83	MD16	123	G
4	IDSEL	44	EROM#	84	MD17	124	R
5	GND	45	AGNDM	85	GND	125	AGNDA
6	AD23	46	MLF	86	MD18	126	VSYNC
7	AD22	47	AVDDM	87	MD19	127	HSYNC
8	AD21	48	MA9	88	MD20	128	P0
9	AD20	49	MA8	89	MD21	129	P1
10	AD19	50	MA7	90	MD22	130	P2
11	AD18	51	MA6	91	MD23	131	P3
12	VDD	52	MA5	92	VDD	132	P4
13	AD17	53	MA4	93	WE3#	133	P5
14	AD16	54	VDD	94	MD24	134	P6
15	C/BE2#	55	MA3	95	MD25	135	P7
16	FRAME#	56	MA2	96	MD26	136	GND
17	IRDY#	57	MA1	97	MD27	137	P8
18	TRDY#	58	MA0	98	MD28	138	P9
19	GND	59	WE0#	99	GND	139	P10
20	DEVSEL#	60	MD0	100	MD29	140	P11
21	STOP#	61	MD1	101	MD30	141	P12
22	INTA#	62	GND	102	MD31	142	P13
23	PAR	63	MD2	103	OE#/RAS1#	143	P14
24	C/BE1#	64	MD3	104	VDD	144	P15
25	AD15	65	MD4	105	XCLK	145	VDD
26	AD14	66	MD5	106	GND	146	ECLK#
27	AD13	67	MD6	107	BA10	147	ESYNC#
28	VDD	68	MD7	108	BA11	148	EVIDEO#
29	AD12	69	CAS#	109	BA12	149	BLANK#
30	AD11	70	RAS#	110	GND	150	DCLK
31	AD10	71	VDD	111	AGNDV	151	GRDY
32	AD9	72	WE1#	112	VLF	152	RESET#
33	AD8	73	MD8	113	AVDDV	153	CPUCLK
34	C/BE0#	74	MD9	114	BA13	154	GND
35	GND	75	MD10	115	BA14	155	AD31
36	AD7	76	GND	116	DDC	156	AD30
37	AD6	77	MD11	117	RVDD	157	AD29
38	AD5	78	MD12	118	VREF	158	AD28
39	AD4	79	MD13	119	FADJ	159	AD27
40	AD3	80	MD14	120	GND	160	AD26

9004196 0000838 727

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table 3-2 Alphabetical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
43	AD0	109	BA12	55	MA3	103	OE#/RAS1#
42	AD1	114	BA13	53	MA4	128	P0
41	AD2	115	BA14	52	MA5	129	P1
40	AD3	149	BLANK#	51	MA6	130	P2
39	AD4	34	C/BE0#	50	MA7	131	P3
38	AD5	24	C/BE1#	49	MA8	132	P4
37	AD6	15	C/BE2#	48	MA9	133	P5
36	AD7	3	C/BE3#	60	MD0	134	P6
33	AD8	69	CAS#	61	MD1	135	P7
32	AD9	153	CPUCLK	63	MD2	137	P8
31	AD10	150	DCLK	64	MD3	138	P9
30	AD11	116	DDC	65	MD4	139	P10
29	AD12	20	DEVSEL#	66	MD5	140	P11
27	AD13	146	ECLK#	67	MD6	141	P12
26	AD14	44	EROM#	68	MD7	142	P13
25	AD15	147	ESYNC#	73	MD8	143	P14
14	AD16	148	EVIDEO#	74	MD9	144	P15
13	AD17	119	FADJ	75	MD10	23	PAR
11	AD18	16	FRAME#	77	MD11	124	R
10	AD19	123	G	78	MD12	70	RAS#
9	AD20	5	GND	79	MD13	152	RESET#
8	AD21	19	GND	80	MD14	117	RVDD
7	AD22	35	GND	81	MD15	21	STOP#
6	AD23	62	GND	83	MD16	18	TRDY#
2	AD24	76	GND	84	MD17	121	VAA
1	AD25	85	GND	86	MD18	12	VDD
160	AD26	99	GND	87	MD19	28	VDD
159	AD27	106	GND	88	MD20	54	VDD
158	AD28	110	GND	89	MD21	71	VDD
157	AD29	120	GND	90	MD22	92	VDD
156	AD30	136	GND	91	MD23	104	VDD
155	AD31	154	GND	94	MD24	145	VDD
125	AGNDA	151	GRDY	95	MD25	112	VLF
45	AGNDM	127	HSYNC	96	MD26	118	VREF
111	AGNDV	4	IDSEL	97	MD27	126	VSYNC
47	AVDDM	22	INTA#	98	MD28	59	WE0#
113	AVDDV	17	IRDY#	100	MD29	72	WE1#
122	B	58	MA0	101	MD30	82	WE2#
107	BA10	57	MA1	102	MD31	93	WE3#
108	BA11	56	MA2	46	MLF	105	XCLK

9004196 0000839 663

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.1 Interface Signals

3.1.1 Host Interface-PCI Bus

Pin Name	Pin	Type	Description
AD31-AD0	155-160, 1, 2, 6-11, 13, 14, 25-27, 29-33, 36-43	I/O	Multiplexed Address and Data Lines, bits 31 through 0: These pins are the multiplexed PCI address and data lines. During the address phase, these pins are inputs. During the data phase, these pins are inputs for write cycles or outputs for read cycles.
C/BE3-C/BE0#	3, 15, 24, 34	I	Bus Command and Byte Enables, bits 3 through 0: These pins are the multiplexed PCI command and byte enable lines.
CPUCLK	153	I	CPU Clock: Timing reference clock for PCI Bus. Connect directly to the PCI Bus Clock.
DEVSEL#	20	O	Device Select: This signal is driven low when the 82C264 decodes its address as the target of the current access.
FRAME#	16	I	Cycle Frame: This pin is driven by the PCI bus master to indicate the beginning and duration of an access.
IDSEL	4	I	ID Select. This signal is used as a chip select for PCI configuration space accesses.
INTA#	22	O	Interrupt Request. Interrupt generation is enabled by bit 5 of the Vertical Sync End register (3D5.11). Interrupt requests are generated at the Vertical Display Enable End time.
IRDY#	17	I	Initiator Ready: This signal is asserted by the PCI bus master to indicate the ability to complete the current data phase of the transaction.
PAR	23	I/O	Parity: This signal is used to provide even parity across AD31-AD0 and C/BE3#-C/BE0#. This signal is sampled as an input during write cycles and provides correct parity as an output for read cycles.
STOP#	21	O	Stop: This signal is used by the target to request the master to stop the current transaction.
TRDY#	18	O	Target Ready: This pin is asserted by the 82C264 to indicate the ability to complete the current data phase of the transaction.
BA14-BA10*	115, 114, 109-107	O	BIOS Address bits 14-10. NOTE BA9-BA0 for the ROM BIOS interface are multiplexed with MA9-MA0.
BD7-BD0* (MD7-MD0)	68-63, 61, 60	I	ROM BIOS data bits 7-0. These bits are multiplexed with memory data bits MD7-MD0.
EROM#	44	O	Enable BIOS ROM. This signal is activated for memory read cycles which fall in the address range of the video BIOS (C000:0-C7FF:F).

* To enable BA14-BA0 and BD7-BD0 pin definitions, pull MD30 to logical 1 at power-on. Pull MD30 high through a 4.7kΩ resistor.

3.1.2 Memory Interface

Pin Name	Pin	Type	Description
CAS#	69	O	DRAM column address strobe. When signal RAMCNF is pulled low, this pin functions as WE# for display memory (for 256Kx16 dual CAS DRAM).

9004196 0000840 385

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.1.2 Memory Interface (cont.)

Pin Name	Pin	Type	Description
MA9-MA0 (BA9-BA0)	48-53, 55-58	O	Memory address bus pins 9-0. MA8-MA0 are used for standard 256Kx4 and 256Kx16 DRAM. MA9 is used for asymmetric 256Kx16 DRAM. NOTE When PCI BIOS ROM is enabled, BA9-BA0 are multiplexed with MA9-MA0.
MD31-MD0	102-100, 98-94, 91-86, 84, 83, 81-77, 75-73, 68-63, 61, 60	I/O	Memory data bus pins 31-0. NOTE MD7-MD0 have a multiplexed definition and are used as BD7-BD0 when the ROM BIOS interface is enabled. (MD30 enables/disables the ROM BIOS interface. A logical 1 enables the interface.)
OE#/RAS1#	103	O	DRAM output enable signal for 1MB configurations. For 2MB configurations, this pin is used as RAS1#. For the 2MB case, the OE# of the DRAM should just be tied to GND.
RAS#	70	O	DRAM row address strobe.
WE3#-WE0#	93, 82, 72, 59	O	DRAM Write Enables. When signal is pulled high, these pins are write enable signals for the display memory (for 256Kx4 or 256Kx16 dual WE DRAM). When signal is pulled low, these pins function as CAS# signals for display memory (for 256Kx16 dual CAS DRAM).

3.1.3 CRT Interface

Pin Name	Pin	Type	Description
B	122	O	Blue DAC output. Blue CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
DDC	116	I	Display Data Channel Input. Supplies a serial data stream from a DDC compliant monitor to the 82C264. This serial data stream is clocked from VSYNC.
FADJ	119	I	Full Scale Current. This pin is connected to GND through a resister to set the full scale current of the DAC. The full scale current is determined by the following equation: *IFULLSCALE = 7.7273 * (VREF/R)* Recommended value for the resistor is 690Ωs.
G	123	O	Green DAC output. Green CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
HSYNC	127	I/TS/O	Horizontal Sync. This signal provides horizontal sync to the CRT or the feature connector. This signal may be tristated when sync from the feature connector is being used to drive the CRT. The polarity of HSYNC is set by bit 6 of Miscellaneous Output Register (3C2). When configured as an input, the sync signal may be used to genlock the 82C264 to an external video source. When configured as an output, HSYNC may be used to support DPMS.
R	124	O	Red DAC output. Red CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
VREF	118	I	Voltage Reference. This pin is the voltage reference input for the internal RAMDAC. The voltage level requirement is 1.22V

9004196 0000841 211

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.1.3 CRT Interface (cont.)

Pin Name	Pin	Type	Description
VSYNC	126	I/TS/ O	Vertical Sync. This signal provides vertical sync to the CRT or the feature connector. This signal may be tristated when sync from the feature connector is being used to drive the CRT. The polarity of VSYNC is set by bit 7 of the Miscellaneous Output Register (3C2). When configured as an input, the sync signal may be used to genlock the 82C264 to an external video source. When configured as an output, VSYNC may be used to support DPMS and to provide a clock to DDC compliant monitors.

3.1.4 Clock Interface

Pin Name	Pin	Type	Description
MLF	46	–	Memory clock loop filter.
VLF	112	–	Video clock loop filter.
XCLK	105	I	14.318MHz crystal clock input.

3.1.5 Power and Signal Ground Interface

Pin Name	Pin	Type	Description
AGNDM	51	GND	Analog ground for the memory clock Phase Lock Loop (PLL).
AGNDV	136	GND	Analog ground for the video clock PLL.
AVDDV	113	PWR	Analog power for the video clock PLL.
GND	5, 19, 35, 62, 76, 85, 99, 106, 110, 120, 136, 154	GND	Ground pins.
RVDD	117	PWR	Power for RAMDAC RAM.
VAA	121	PWR	Power supply for the internal DAC of the RAMDAC. The voltage is 5V + 10%.
VGNDA	125	GND	Analog ground for the DAC.

3.1.6 Feature Connector Interface

NOTE MD31 must be set to a logical 1 at power-on in order to enable the feature connector interface.

Pin Name	Pin	Type	Description
BLANK#	149	I/O	Blank signal when the feature connector interface is enabled. BLANK# is an output when ESYNC# is a logical 1. BLANK# is an input when ESYNC# is a logical 0.
DCLK	150	I/O	Pixel clock signal when the feature connector interface is enabled. DCLK is an output when ECLK# is a logical 1. DCLK is an input when ECLK# is a logical 0.
ECLK#	146	I	Enable Clock signal when the feature connector interface is enabled. This signal controls the direction of DCLK. When ECLK# is a logical 1, DCLK is an output. When DCLK is a logical 0, DCLK is an input from the feature connector.

9004196 0000842 158

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.1.6 Feature Connector Interface (cont.)

NOTE MD31 must be set to a logical 1 at power-on in order to enable the feature connector interface.

Pin Name	Pin	Type	Description
ESYNC#	147	I	Enable Sync signal when the feature connector interface is enabled. This signal controls the direction of VSYNC, HYSNC, and BLANK#. When ESYNC# is a logical 1, VSYNC, HSYNC, and BLANK# are outputs. When ESYNC# is a logical 0, BLANK# is an input from the feature connector. VSYNC and HSYNC will be tristated if genlock is disabled, or inputs if genlock is enabled.
EVIDEO#	148	I/O	Enable Video signal when the feature connector interface is enabled. This signal controls the buffer direction of P15 - P0. When ECLK is a logical 1, P15-P0 are outputs. When EVIDEO# is a logical 0, P15-P0 are inputs from the feature connector. EVIDEO# is defined as an output when the Color Key overlay function is enabled. EVIDEO# is defined as an input for all other cases.
GRDY	151	O	Graphics Ready Output Signal when the 16-bit feature connector interface is enabled. The GRDY signal indicates the graphics subsystem is ready to latch pixel data on P15-P0. This pin can also function as the Color Key Window signal when connected to signal EVIDEO (EVIDEO functions as an input in this case). NOTE An external invertor must be used for GRDY in this Color Key Window case because of the definition of EVIDEO# (logical 0 indicates the overlay window area).
HSYNC	127	I/TS/ O	Horizontal Sync. HSYNC is defined as an output when the feature connector interface is disabled. HSYNC may be an output, tristated, or an input when the feature connector interface is enabled. Signal ESYNC and the genlock state determine the direction of HSYNC. HSYNC is an output when signal ESYNC is a logical 1. HSYNC will tristate when ESYNC is a logical 0, and the sync from the feature connector will be used to drive the CRT. If genlock is enabled and ESYNC is a logical 0, HSYNC can be configured as an input and used to genlock the 82C264 to an external video source.
P15-P0	144-137, 135-128	I/O	Pixel data bits 15-0.
VSYNC	126	I/TS/ O	Vertical Sync. VSYNC is defined as an output when the feature connector interface is disabled. VSYNC may be an output, tristated, or an input when the feature connector interface is enabled. Signal ESYNC and the genlock state determine the direction of VSYNC. VSYNC is an output when signal ESYNC is a logical 1. VSYNC will tristate when ESYNC is a logical 0, and the sync from the feature connector will be used to drive the CRT. If genlock is enabled and ESYNC is a logical 0, VSYNC can be configured as an input and used to genlock the 82C264 to an external video source.

9004196 0000843 094

Powered by ICminer.com Electronic-Library Service CopyRight 2003

4.0 Bus Interface Unit

The OPTi 82C264 allows connection directly to the 32-bit PCI Bus. No external bus logic is required.

The Bus Interface Unit provides decoding logic for both I/O, configuration and memory accesses. The proper handshaking signals are provided to handle PCI bus protocols. The Bus Interface Unit also provides the necessary decoding logic and control signal EROM# to allow BIOS ROM accesses when the 82C264 is implemented as a plug-in peripheral.

For CPU read/writes of video memory, Segment Offset Register A (3CF.20) and Segment Offset Register B (3CF.21) can be used as Source and Destination respectively to speed CPU access to display memory. Linear addressing may also be implemented to eliminate bank switching overhead.

4.1 Write Buffer and Control

The Write Buffer queues CPU memory write commands which cannot be executed immediately because of memory bandwidth arbitration. The commands queued in the Write Buffer are executed as soon as display memory bandwidth is available. Once the address and the data of the CPU command is in the write buffer, the 82C264 immediately releases the CPU for ensuing cycles. The end result is maximized CPU bandwidth.

The Write Buffer data path is 32-bits wide. The depth can be programmed to zero, two, or four levels (bits 1, 0 of 3C5.14). The default value is four levels deep. The Write Buffer control logic allows packing of consecutive byte and word commands if the address of the commands are within a double word boundary.

4.2 Graphic Controller

The Graphic Controller manipulates the CPU data before it is sent to the display memory. The data path is 32-bits wide. For a write operation, the Graphic Controller performs data rotation, masking, and set/reset of the CPU data. Logical operations may also be performed using the CPU data and the data in the read latch. For a read operation, the Graphic Controller takes DRAM data from the read latch and either feeds the data directly back to the CPU, or performs a color compare operation before feeding the data back to CPU.

4.3 Memory Sequencer

The Memory Sequencer generates the timing for the display DRAM. The timing generated includes that for RAS, CAS, WE, OE, and multiplexed address. The memory clock which drives this logic is optimized for the speed of the DRAM used. The Memory Sequencer generates CAS- before-RAS refresh cycles, Random Read and Random Early Write cycles, Fast Page Read and Fast Page Early Write cycles. Multiple CAS or WEs are generated depending on the setting of MD15 (pin 81). A logical zero on this pin selects multiple CAS, while a logical one selects multiple WEs.

The Memory Sequencer allocates video memory bandwidth for the GUI engine, CPU access, screen refresh, DRAM refresh and hardware cursor access (if enabled), as follows:

- The allocation between the GUI engine or CPU access and screen refresh is based on the status of the video FIFO. Priority is given to the screen refresh function.
- DRAM refresh is allocated at the end of each scan line. At this allocated period, the 82C264 will generate CAS-before-RAS refresh cycles to ensure that the DRAM refresh timing requirement is meet. The number of CAS-before-RAS refresh cycles is selectable by bit 6 of the Vertical Sync End Register (3D5.11).
- The hardware cursor accesses are allocated at the beginning of any scan line in which the hardware cursor appears. Depending on the size of the cursor, the 82C264 will generate two (32X32X2) or four (64X64X2) page mode CAS cycles to fetch the cursor pattern from the off screen area of the display RAM.

4.4 Video FIFO

The Video FIFO allows the Memory Sequencer to allocate cycles more efficiently and therefore to optimize CPU bandwidth. The Memory Sequencer fetches data from the display DRAM with fast page mode read cycles and loads the data to the Video FIFO. The data in the Video FIFO is then delivered to the Attribute Controller. The Video FIFO can be set to 4, 8, 12 or 16 levels by programming bits 5,4 of the Extended FIFO Control Register (3C5.13). A threshold value can be set as well by programming bits 2-0 of 3C5.13. The threshold can be from one level of empty to eight levels of empty. If the data in the Video FIFO is below the programmed threshold, then the screen refresh cycle takes priority over CPU access.

4.5 CRT Controller (CRTC)

The CRT Controller generates the horizontal sync and vertical sync for the CRT display monitor and provides a BLANK# signal to the integrated RAMDAC and to the feature connector. The CRT registers provides the flexibility to configure the horizontal and vertical timing, the text cursor position, the starting display address, split screen, screen horizontal panning, and other display related functions.

4.6 Attribute Controller

The Attribute Controller takes video memory data from the Video FIFO and serializes it in accordance with the display

9004196 0000844 T20

Powered by ICminer.com Electronic-Library Service CopyRight 2003

mode structure (e.g. text, 4-bit/pixel, 8-bit/pixel, etc.). The video data, along with hardware cursor data, is merged together and then routed to the RAMDAC. The Attribute Controller controls blinking and underline for text modes, and pixel panning for both graphic and text modes.

4.7 GUI Engine

The 32-bit GUI Engine provides acceleration of those functions which most greatly enhance graphics performance in GUI environments, such as Microsoft Windows. Acceleration is supported for 8-bit, 15-bit, 16-bit, and 24-bit/pixel modes. Any graphics resolution up to 1280x1024 may be accelerated. A summary of the available GUI functions follows:

- BitBLT
- Color Expansion
- Fast Polygon Fill
- Area Fill
- Line Draw
- Short Stroke Vector Draw
- Rectangular Clipping
- Raster Operations

Programming the GUI Engine register set is facilitated by a one level deep Register Queue and Memory Mapped I/O registers. The Register Queue allows the complete set of GUI registers to be programmed for the next GUI operation without having to wait for the completion the current GUI operation. A status bit (bit 1 of the GUI Accelerator Status/Start Register - memory map location BF800h) indicates the state of the Register Queue. Memory Mapping the GUI Engine's I/O registers allows for faster programming of the 82C264's GUI Engine register set, since memory read/write operations can be used to access the registers instead of slower I/O read/write operations. Memory Mapped I/O is enabled by programming bit 7 of the Extended Mode Control Register (3CF.22) to a logical 1. Bits 3 and 2 of the Miscellaneous Register (3CF.06) must also be programmed to a logical 1 and a logical 0 respectively.

A short discussion of each of the GUI Engine functions follows:

4.7.1 BitBLT

Bit-Block transfer, or BitBLT, is among the most important of the GUI Engine functions. The BitBLT function is used to move blocks of graphics data from a source location in video memory or system memory to a specified destination in video memory or system memory. The direction of data transfer is determined by bits 7 (source) and 6 (destination) of the BitBLT Mode Register - memory map location BF801h. A logical 1 for the given bit selects system memory. A logical 0 selects video memory. Raster operations between the source and destination data are supported.

A standard BitBLT function and an 8x8 Pattern BitBLT function are supported. Bit 2 of the BitBLT Mode Register controls the BitBLT function type. A logical 1 selects 8x8 Pattern BitBLT. Color data, Monochrome data, or a fixed color may be selected for each function. Bits 1 and 0 of the BitBLT Mode Register control this selection.

In Windows, BitBLT is most often used to perform SRCCOPY and PATCOPY. The direction of data transfer is typically from video memory to video memory, or from system memory to video memory.

4.7.2 Color Expansion

The Color Expansion function is used in cases where only a foreground color and a background color (for instance, black text on a white background) are required to fill a given display area. For these cases (e.g. BitBLTing from a monochrome source pattern), a single bit of data can be used to represent a given pixel on the screen. The bit is used as a lookup to a Foreground Color Register and a Background Color Register in the GUI Engine register set. The Foreground Color Register contains the 8, 16, or 24-bit foreground color to be filled. The Background Color Register contains the background color to be filled. If the given bit is a logical 1, the foreground color will be filled. If the given bit is a logical 0, the background color will be filled.

Transparency for Color Expansion is also supported. Bit 4 of the BitBLT mode register enables/disables the transparency effect. A logical 1 enables transparency. When transparency is enabled, the original background color of the destination is retained.

In Windows, Color Expansion is most often used to perform TextOut operations, where font data is transferred from system memory to video memory.

4.7.3 Fast Polygon Fill

Fast Polygon Fill is used to fill geometric shapes such as trapezoids, triangles, etc. This function makes use of a specialized scan line fill technique to fill the geometric shapes. The shapes may be filled with a solid color or a pattern (monochrome or color source pattern is supported). Source color selection is via bits 1 and 0 of the BitBLT mode register. Raster Operations between the source and destination data are supported.

4.7.4 Area Fill

The Area Fill function is used to fill an area in display memory (usually on the screen) with a fixed color. The color to be filled is programmed into the Foreground Color register. Raster Operations between the source and destination data are supported.

9004196 0000845 967

Powered by ICminer.com Electronic-Library Service CopyRight 2003

4.7.5 Line Draw

The Line Draw function is based on the Bresenham algorithm. This function may be used to draw a solid line (or lines) of any length/direction within the defined bitmap. The color to be used is programmed into the Foreground Color register. This function is especially useful in CAD programs (e.g. AutoCAD) where drawings are constructed using large numbers of vectors.

4.7.6 Short Stroke Vector Draw

The Short Stroke Vector Draw function is a specialized line draw function. This function may be used to draw solid lines of up to 16-pixels in length in one of eight directions (0, 45, 90, 135, 180, 225, 270, 315 degrees). Up to two Short Stroke Vectors may be drawn at once. The color to be used is programmed into the Foreground Color register.

In Windows, this function is useful for drawing the borders of geometric shapes (e.g. ellipses). This function is also very useful in MCAD applications, where large numbers of short, solid lines are often required to represent a given mechanical shape.

4.7.7 Rectangular Clipping

The Rectangular Clipping function is most easily described as a rectangular mask function. The rectangular area is defined by four registers; the Clip Left Register, Clip Right Register, Clip Top Register, and Clip Bottom Register. In Windows, Clipping is most useful for TextOut operations.

4.7.8 Raster Operations

The Raster Operations function facilitates the logical mixing of source and destination graphics data. The 82C264 supports 2ROPs, or 16 raster operations. Reference the Raster Operation Code Register - memory map location B8F02 for additional detail on available raster operations.

4.8 Hardware Cursor

The Hardware Cursor supports a 32X32X2 or a 64X64X2 user defined pattern. The cursor pattern is stored in the upper 1K or 2K of display memory. The Hardware Cursor operates for all standard VGA graphic and text modes, 4 bit per pixel extended graphics planar modes, and 8/16/24-bit per pixel packed-pixel modes.

The cursor pattern has 2-bits to represent a pixel. Each bit corresponds to a plane. Table 4-1 shows the cursor display state corresponding to the value of the cursor pattern.

Table 4-1 Cursor Display State

Cursor Plane 0	Cursor Plane 1	Cursor Display State
0	0	Cursor color 0
1	0	Cursor color 1
0	1	Transparent
1	1	Invert video data

The cursor position is defined relative to the cursor offset from the top-left corner of the display screen. The cursor position X is in pixels and it is specified by 3CF.23 for the lower eight bits and 3CF.24 for the remaining three higher order bits. The cursor position Y is in scan lines and it is specified by 3CF.25 for the lower eight bits and 3CF.26 for the remaining three higher order bits. The cursor offset is specified by the Hardware Cursor Y Origin Register (3CF.2E) and the Hardware Cursor X Origin Register (3CF.2F). The cursor position is changed only on VSYNC following a write to the cursor Y position registers.

For 32X32 cursor size, each cursor pattern requires 256 bytes. The cursor pattern is stored in the top 1K of display memory. Up to four cursor patterns may be loaded. The active cursor pattern is selected by programming the bits 3 and 2 of the Hardware Cursor Pattern Address Offset register (3CF.2D).

For 64X64 cursor size, each cursor pattern requires 1024 bytes. The cursor pattern is stored in the top 2K of display memory. Up to two cursor patterns may be loaded. The active cursor pattern is selected by programming bit 2 of 3CF.2D.

The cursor pattern data for cursor plane 0 and cursor plane 1 is loaded into display memory one cursor scan line at a time. For each cursor scan line, cursor plane 0 data is loaded first, followed by the cursor plane 1 data. This loading sequence continues until all 32/64 scanlines have been loaded into display memory. The cursor pattern is mapped to the display memory using linear packed-pixel addressing.

4.9 RAMDAC

The internal true color RAMDAC has a 24-bit wide pixel data port. This means that HiColor™ (5-5-5 format and 5-6-5 format) and true color modes (8-8-8 format) can be supported without having to double or triple the pixel clock rate. Three 8-bit D/A converters generate RS-343A compatible red, green, and blue video signals. The signal outputs can drive a doubly-terminated 75 ohm coax cable directly without the need for external buffers.

The RAMDAC has a VGA compatible triple 6-bit color lookup table (CLUT). The RAMDAC supports 4-bit/pixel modes, 8-bit pseudo color (256 colors) modes, and CLUT bypass versions of HiColor and true color modes. The palette DAC register I/O

9004196 0000846 8T3

Powered by ICminer.com Electronic-Library Service CopyRight 2003

addresses and functionality are 100% compatible with the VGA standard.

Two external pins are used to control current in the RAMDAC. VREF (pin 118) connects to an external band-gap reference circuit which generates 1.22V to the RAMDAC. This voltage reference is used along with the resistor value on pin FADJ (pin 155) to set the full scale current output of the red, green, and blue Digital to Analog Converters (DACs). The desired resistor value may be determined by the following equation.

$$R = 7.7273 \times ((VREF) \div (IFULLSCALE))$$

To achieve a full scale reference current of 14mA, which will deliver 0.7V peak to peak on the RGB outputs, a 690ohm resistor is recommended.

Table 4-2 shows the resolutions and color depths supported by the internal RAMDAC.

Table 4-2 CRT Display Resolutions

Resolution	Text Mode	Number of Colors (Number of bits)				
		16 (4)	256 (8)	32K (16)	64K (16)	16M (24)
640 x 480		Yes	Yes	Yes	Yes	Yes
800 x 600		Yes	Yes	Yes	Yes	
1024 x 768		Yes	Yes	Yes	Yes	
1280x1024		Yes	Yes			
	132 col	Yes				

4.10 Clock Synthesizer

The clock synthesizer module provides video clock and a memory clock. The video clock may be selected from one of four programmable video clock groups. Each group is individually programmable from 25MHz to 100MHz. The memory clock is programmable from 30MHz to 80MHz. All frequencies are derived from a 14.318MHz input (XCLK-pin 105).

4.11 Multimedia Module

The Multimedia Module provides Feature Connector support, Genlock to an external video source, Overlay capabilities, and a mode switching RAMDAC.

4.11.1 Feature Connector

The 82C264 provides support for a 16-bit feature connector interface. The 16-bit feature connector offers VAFC baseline function compatibility as well as additional overlay options (Section 4.11.3, Overlay). To enable the 16-bit feature connector solution strap MD31 to a logical 1 at power-on.

4.11.2 Genlock

To support video overlay on a pixel by pixel basis, the video data from the feature connector must be synchronized with the graphics data from the 82C264. This synchronization is defined as "Genlock". To accomplish this, the 82C264 can be configured to input VSYNC, HSYNC, or both VSYNC and HSYNC from the feature connector. The sync information is then used to synchronize the graphics data frame with the incoming video data frame. This method for synchronizing the two data frames is intended for configurations where the pixel clock from the remote video source is the same as the pixel clock from the graphics controller.

The Genlock function is controlled by the Genlock Control register (3CF.4B). Bit 7 enables/disables VSYNC Genlock. Bit 6 enables/disables HSYNC Genlock. In both cases, a logical 1 enables Genlock for the given sync signal.

4.11.3 Overlay

Three types of overlay are supported:

1. **Pass-Through Overlay**
   The entire display frame is replaced with video data from the feature connector. To accomplish this, the ESYNC#, EVIDEO#, and ECLK# inputs are pulled low and remain low. The graphics data from display memory is ignored. Genlock is not required for Pass-Through Overlay.
2. **Overlay using EVIDEO#**
   The video source from the feature connector controls overlay on a pixel by pixel basis. When given pixel(s) from display memory are to be overlaid with video data from the feature connector, EVIDEO# is pulled low by the remote video source. The pixel in display memory is then replaced with the video pixel from the feature connector. EVIDEO# can be toggled on a pixel by pixel basis. This function is selected by programming bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 0 and a logical 1 respectively.

9004196 0000847 73T

Powered by ICminer.com Electronic-Library Service CopyRight 2003

3. Overlay with Color Key:

   a. **Full Screen Overlay with Color Key**
   The 82C264 controls overlay on a pixel by pixel basis. For this case, EVIDEO# is configured as an output. When the color key condition is met (e.g. pixel data = color key value), the 82C264 drives EVIDEO# low. The pixel in display memory is then replaced with the video pixel from the feature connector. EVIDEO# can be toggled on a pixel by pixel basis. This function is selected by programming both bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 1.

   b. **Overlay with Color Key in a Window**
   This overlay function operates in the same manner as Full Screen Overlay with Color Key, except that the Color Key is used only within a localized window. The window is defined by six overlay window registers within the 82C264, which define the horizontal start and end and the vertical start and end of the window. If the display update location is within the defined window and if the color key condition is met, output signal GRDY is driven high. GRDY should be connected to EVIDEO# through an inverter, so EVIDEO# will be driven low. The pixel in display memory is then replaced with the video pixel from the feature connector. GRDY can be toggled on a pixel by pixel basis. This function is selected by programming bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 1 and a logical 0 respectively.

For all overlay types, the video data stream must be applied at all times, even when video data from the feature connector is being ignored. Some form of genlock is required (e.g., external video device genlocks video and graphics data or 82C264 genlocks video and graphics data) for Overlay using EVIDEO# and Overlay with a Color Key.

4.11.4 RAMDAC

The internal RAMDAC of the 82C264 allows mode switching between the overlay window and the surrounding graphics screen. This means that the overlay window color depth can be set independently of the color depth of the surrounding graphics. For instance, the overlay window could be at 16-bits/pixel while the surrounding graphics is at 8-bits/pixel. To invoke DAC mode switching, program bit 5 of the Overlay Control Register (3CF.40) to a logical 1, then use bits 4-2 of the same register to indicate the color mode of the feature connector input data.

9004196 0000848 676

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.0 Register Description

This section describes the OPTi 82C264 register set. The standard VGA core registers are listed in table format. For detailed bit level information on the VGA core registers, please reference one of the many available VGA programmer's reference guides. A recommended VGA programming reference book is the Programmer's Guide to the EGA and VGA Cards (Second Edition) by Richard M. Ferraro. The book is published by Addison-Wesley.

A table listing and bit level detail are provided for the 82C264's GUI Engine, Extended, Clock Synthesizer, Overlay Control and PCI Configuration register sets.

5.1 VGA Register Port Map

Table 5-1 VGA Register Port Map

Address	Port
3C0h	Attribute Controller Write
3C1h	Attribute Controller Read
3C2h	Miscellaneous Output (Write)/Input Status Register 0 (Read)
3C3h	Video Subsystem Enable
3C4h	Sequencer Index
3C5h	Sequencer Data
3C6h	DAC Pixel Mask
3C7h	Pixel Address Read Mode (Write)/DAC State (Read)
3C8h	Pixel Mask Write
3C9h	Pixel Data
3CEh	Graphics Controller Index
3CFh	Graphics Controller Data
3x4h[1]	CRT Controller Address
3x5h[1]	CRT Controller Data
3xAh[1]	Feature Control (Write)/Input Status Register 1 (Read)
46E8h	Video Subsystem Enable

1. "x" = D for color modes and B for monochrome modes.

5.2 Standard VGA Register Tables

Table 5-2 VGA General Registers

Register Name	Address	Index
Miscellaneous Output	3CCh = read port 3C2h = write port	--
Input Status Register 0	3C2h = read port	--
Input Status Register 1	3xAh = read port	--
Feature Control Register	3CAh = read port 3xAh = write port	--
Video Subsystem Enable	3C3h	--
Video Subsystem Enable	46E8h	--

Table 5-3 VGA Sequencer Registers

Register Name	Address	Index
Sequencer Index	3C4h	--
Reset	3C5h	00h
Clocking Mode	3C5h	01h
Plane Mask	3C5h	02h
Character Map Select	3C5h	03h
Memory Mode	3C5h	04h

Table 5-4 CRTC Registers

Register Name	Address	Index
CRTC Index	3x4h	--
Horizontal Total	3x5h	00h
Horizontal Display End	3x5h	01h
Horizontal Blanking Start	3x5h	02h
Horizontal Blanking End	3x5h	03h
Horizontal Sync Start	3x5h	04h
Horizontal Sync End	3x5h	05h
Vertical Total	3x5h	06h
Overflow	3x5h	07h
Screen Preset Row Scan	3x5h	08h
Maximum Scan Line	3x5h	09h
Cursor Start	3x5h	0Ah
Cursor End	3x5h	0Bh
Start Address High	3x5h	0Ch
Start Address Low	3x5h	0Dh
Cursor Location High	3x5h	0Eh
Cursor Location Low	3x5h	0Fh

9004196 0000849 502

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table 5-4 CRTC Registers (cont.)

Register Name	Address	Index
Vertical Sync Start	3x5h	10h
Vertical Sync End	3x5h	11h
Vertical Display End	3x5h	12h
Offset	3x5h	13h
Underline Location	3x5h	14h
Vertical Blanking Start	3x5h	15h
Vertical Blanking End	3x5h	16h
Mode Control	3x5h	17h
Line Compare	3x5h	18h

Table 5-5 Graphics Controller Registers

Register Name	Address	Index
Graphics Controller Index	3CEh	--
Set/Reset	3CFh	00h
Set/Reset Enable	3CFh	01h
Color Compare	3CFh	02h
Data Rotate	3CFh	03h
Read Map Select	3CFh	04h
Mode	3CFh	05h
Miscellaneous	3CFh	06h
Color Don't Care	3CFh	07h
Bit Mask	3CFh	08h

Table 5-6 Attribute Controller Registers

Register Name	Address	Index
Attribute Controller Index	3C0h write/ 3C1h read	--
Color Palette Registers	3C0h write/ 3C1h read	00h -Fh
Mode Control	3C0h write/ 3C1h read	10h
Overscan Color	3C0h write/ 3C1h read	11h
Color Plane Enable	3C0h write/ 3C1h read	12h
Horizontal Pixel Panning	3C0h write/ 3C1h read	13h
Color Select	3C0h write/ 3C1h read	14h

Table 5-7 Internal RAMDAC Registers

Register Name	Address	Index
Pixel Mask	3C6h	--
Pixel Address Read Mode	3C7h (for write)	--
DAC State	3C7h (for read)	--
Pixel Address Write Mode	3C8h	--
Pixel Data	3C9h	--

5.3 OPTi Register Tables

Table 5-8 OPTi GUI Engine Registers

Register Name	Address	Index
Status/Start Register	X3C4h	00h
BitBLT Mode	X3C4h	01h
BitBLT Raster Operation	X3C4h	02h
Display Configuration	X3C4h	03h
Source Start X/Diagonal Step Constant	X3C4h	04h
Source Start Y/Axial Step Constant	X3C4h	06h
Destination Start X	X3C4h	08h
Destination Start Y	X3C4h	0Ah
BitBLT Width/Short Stroke	X3C4h	0Ch
BitBLT Height	X3C4h	0Eh
Error Term/Short Pitch	X3C4h	12h
Foreground Color	X3C4h	18h
Background Color	X3C4h	1Ch
Clip Left	X3C4h	20h
Clip Right	X3C4h	22h
Clip Top	X3C4h	24h
Clip Bottom	X3C4h	26h

Table 5-9 82C264 Extended Registers

Register Name	Address	Index
Unlock Extended Registers	3C5h	10h
Mode Control	3C5h	11h
Clock Select	3C5h	12h
Video FIFO Control	3C5h	13h
Write Buffer Control	3C5h	14h
Miscellaneous Control 1	3C5h	15h
Miscellaneous Control 2	3C5h	17h

9004196 0000850 224

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Table 5-9 82C264 Extended Registers (cont.)

Register Name	Address	Index
DDC/DPMS	3C5h	18h
Configuration 2	3C5h	1Fh
Configuration 3	3C5h	2Eh
OffsetA	3CFh	20h
OffsetB	3CFh	21h
Extended Mode Control	3CFh	22h
Hardware Cursor X Position Low	3CFh	23h
Hardware Cursor X Position High	3CFh	24h
Hardware Cursor Y Position Low	3CFh	25h
Hardware Cursor Y Position High	3CFh	26h
Hardware Cursor Color 0 L/M/H	3CFh	27h-29h
Hardware Cursor Color 1 L/M/H	3CFh	2Ah-2Ch
Hardware Cursor Pattern Offset	3CFh	
Hardware Cursor Y Origin	3CFh	2Eh
Hardware Cursor X Origin	3CFh	2Fh
Scratch Pad Register	3x5h	1Ch
Extended Overflow	3x5h	30h
Starting Address Overflow	3x5h	31h
Interlaced Odd Frame Horizontal Retrace End	3x5h	32h
Extended CRT Control	3x5h	33h
External RAMDAC Control	3x5h	36h

Table 5-10 Clock Synthesizer Registers

Register Name	Address	Index
Video Clock Group 0 (VCK0) Input Frequency Divider	3C4h	20h
Video Clock Group 0 (VCK0) VCO Frequency Divider	3C4h	21h
Video Clock 1 (VCK1) Input Frequency Divider	3C4h	22h
Video Clock Group 1 (VCK1) VCO Frequency Divider	3C4h	23h
Video Clock 2 (VCK2) Input Frequency Divider	3C4h	24h
Video Clock Group 2 (VCK2) VCO Frequency Divider	3C4h	25h
Video Clock 3 (VCK3) Input Frequency Divider	3C4h	26h
Video Clock Group 3 (VCK3) VCO Frequency Divider	3C4h	27h

Table 5-10 Clock Synthesizer Registers (cont.)

Register Name	Address	Index
Memory Clock Input Frequency Divider	3C4h	28h
Memory Clock VCO Frequency Divider	3C4h	29h

Table 5-11 Overlay Control Registers

Register Name	Address	Index
Overlay Control	3CFh	40h
Color Key	3CFh	41h
Color Key Mask	3CFh	43h
Overlay Window Horizontal Start	3CFh	45h
Overlay Window Horizontal End	3CFh	46h
Overly Window Horizontal Pixel Alignment	3CFh	47h
Overlay Window Vertical Start	3CFh	48h
Overlay Window Vertical End	3CFh	49h
Overlay Window Vertical Overflow	3CFh	4Ah
Genlock Control	3CFh	4Bh

Table 5-12 PCI Configuration Space Registers

Register Name	Byte Location in Configuration Space Header
Vendor ID	00h - 01h
Device ID	02h - 03h
Command	04h - 05h
Status	06h - 07h
Revision	08h
Class Code	09h - 0Bh
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address	10h - 27h
Expansion ROM Base Address	30h - 33h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_Gnt	3Eh
Max_Lat	3Fh

9004196 0000851 160

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.4 82C264 GUI Engine Register Set

The 82C264 GUI engine register set may be accessed via the standard I/O port method or as a memory mapped I/O block. To access the GUI register set via the standard I/O method, use X3C0h as the 16-bit index port and X3C4 as the 32-bit data port. "X" may be any value for PCI configurations.

To access the GUI register set as a memory mapped I/O block, set bit 7 of the Extended Mode Control Register (3CF.22) to a logical 1 and bits 3, 2 of the Miscellaneous Register (3CF.06) to 0, 1 respectively.

The memory map location for the GUI registers is B8F00h - B8F24h. 8-bit, 16-bit and 32-bit write cycles are supported.

Table 5-13 is a diagram of the memory mapped I/O register structure.

Table 5-13 Memory Mapped I/O Register Structure

Port	31:24	23:16	15:8	7:0
B8F00	Display Configuration	BitBLT Raster	BitBLT Mode	GUI Engine Status Start
B8F04	Source Start Y/Axial Step Constant		Source Start X/Diagonal Step Constant	
B8F08	Destination Start Y		Destination Start X	
B8F0C	BitBLT Height		BitBLT Width/Short Stroke Vector	
B8F10	Error Term/Source Pitch			
B8F14				
B8F18		Foreground Color		
B8F1C		Background Color		
B8F20	Clip Right		Clip Left	
B8F24	Clip Bottom		Clip Top	

5.4.1 Status/Start Register

I/O Port: X3C4h

Index: Write value 00h to index port location X3C0h

Memory Map Location: B8F00h

Bits	Function
7-5	Function Select
4	X Direction Select
3	Y Direction Select
2	CPU Write Enable Status
1	GUI Engine Register Queue Status
0	GUI Engine Busy

Bit 7 - 5: GUI Engine Function Select. The operation will start when the given function is selected. Be sure all applicable registers are programmed before selecting the GUI function type. Bits 7-5 select GUI engine functions as follows:

7	6	5	Function Selected
1	1	1	No operation
0	0	1	BitBLT
0	1	0	Fast Polygon Fill
0	1	1	Short Stroke Vector Draw
1	0	0	Line Draw (Bresenham algorithm)

For standard programming, a write to these register bits engages the engine to perform the selected function. A Quick Start feature is also available. This feature is enabled by programming bit 7 of the Display Configuration Register. With the Quick Start feature enabled, a write to the BitBLT Width Register will engage the engine to perform the function currently selected by bits 7-5 of this register. The Quick Start feature is most useful for Fast Polygon Fill operations.

Bit 4: X Direction Select. This bit selects the horizontal direction of the selected BitBLT operation.
Logical 1: Selects bottom to top.
Logical 0: Selects top to bottom (default).

9004196 0000852 0T7

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 3: Y Direction Select. This bit selects the vertical direction of the selected BitBLT operation.
Logical 1: Selects bottom to top.
Logical 0: Selects top to bottom (default).
Note BitBLT directions other than the default are useful for cases of overlapping Source and Destination.

Bit 2: CPU Write Enable Status. This bit is intended to provide CPU write status for memory to screen operations, particularly color expansion. This bit is read only.
Logical 1: Indicates the CPU will need to wait before the next write command to display memory.
Logical 0: Indicates 82C264 is ready to accept a host write.

Bit 1: GUI Engine Register Queue Status. All GUI Engine registers may be queued with the exception of this register. This bit is read only.
Logical 1: Indicates the GUI Engine Register Queue is empty.
Logical 0: Indicates the GUI Engine Register Queue is full.

Bit 0: GUI Engine Busy. This bit is read only.
Logical 1: Indicates GUI engine is busy.
Logical 0: Indicates GUI engine is idle.

5.4.2 BitBLT Mode Register

I/O Port: X3C4h

Index: Write value 01h to index port location X3C0h

Memory Map Location: B8F01h

Bits	Function
7	BitBLT Source Select
6	BitBLT Destination Select
5	Enable Clipping
4	Enable Monochrome Transparency
3	Enable Source Pitch
2	Enable 8x8 Pattern BitBLT
1,0	Source Map Color Selection

Bit 7: BitBLT Source Select.
Logical 1: Selects system memory as the source for the BitBLT operation.
Logical 0: Selects display memory as the source for the BitBLT operation.

Bit 6: BitBLT Destination Select.
Logical 1: Selects system memory as the destination for the BitBLT operation.
Logical 0: Selects display memory as the destination for the BitBLT operation.
Note Screen to Screen and Memory to Screen operations are fully supported. Screen to Memory operations are supported for SRCOPY only. Memory to Memory operations are not supported.

Bit 5: Enable Clipping.
Logical 1: Enables the Rectangular Clipping function. Registers X3C4.20 (Clip Left Register), X3C4.22 (Clip Right Register), X3C4.24 (Clip Top Register), X3C4.26 (Clip Bottom Register) determine the boundary area for clipping.
Logical 0: Disables the Rectangular Clipping function.

Bit 4: Enable Monochrome Transparency.
Logical 1: Enables monochrome transparency. This feature is intended for use with a monochrome source. When monochrome transparency is enabled, only the foreground color of the monochrome source is filled at the destination. The original destination background color is maintained.
Logical 0: Disables monochrome transparency.

Bit 3: Enable Source Pitch.
Logical 1: Enables source pitch. The source pitch is defined as the number of pixels locations from a pixel on a given row to the same pixel location in the next row. Enable this bit to address the BitBLT area in a linear fashion. Bits 14-3 of X3C4.12 set the source pitch. This selection is intended for TextOut functions which involve font caching.
Logical 0: Disables source pitch. Use X/Y addressing.

Bit 2: Enable 8x8 Pattern BLT.
Logical 1: Enables 8x8 pattern BLT. At the start of a BLT operation, an 8x8 color or monochrome source pattern is read from display memory. This pattern is repeatedly filled to the selected destination.
Logical 0: Disables 8x8 pattern BLT. Use pixel by pixel BLT operation.

9004196 0000853 T33

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits 1,0: Source Map Color Selection for BitBLT and Fast Polygon Fill Operations.

1	0	Source Map
0	0	Color
0	1	Monochrome (e.g. for Color Expansion). Color is determined by the Foreground and Background Color Registers.
1	0	Fixed Color (e.g. for Area Fill). Color is determined by the Foreground Color Register.
1	1	Reserved

5.4.3 BitBLT Raster Operation Register

I/O Port: X3C4h

Index: Write value 02h to index port location X3C0h

Memory Map Location: B8F02h

Bits	Function
7	Clipping Type
6	Reserved
5	Last Pixel Off
4	Major Axis
3-0	Raster Operation Select

Bit 7: Clipping Type. Selects whether the clipping function is performed inside or outside the clipping rectangle.
Logical 1: The clipping function is performed outside the clipping rectangle (standard clipping).
Logical 0: The clipping function is performed inside the clipping rectangle.

Bit 6: Reserved.

Bit 5: Last Pixel Off.
Logical 1: Selects last pixel off for line draw operations. Set this bit for Polyline applications.
Logical 0: Selects last pixel on for line draw operations. Use this setting for stand-alone lines.

Bit 4: Major Axis Select.
Logical 1: Indicates the Y-axis is the major axis for line draw.
Logical 0: Indicates the X-axis is the major axis for line draw.

Bits 3-0: Raster Operation Select. Sixteen two-operand raster operations are supported.

Bit 3	2	1	0	Raster Operation (Microsoft Designation)	Boolean Equation
0	0	0	0	Blackness	0
0	0	0	1	NOTSRCERASE	~(S+D)
0	0	1	0	--	~S*D
0	0	1	1	NOTSRCCOPY	~S
0	1	0	0	SRCERASE	~D*S
0	1	0	1	DSTINVERT	~D
0	1	1	0	SRCINVERT	~(S+D)
0	1	1	1	--	~(S*D)
1	0	0	0	SRCAND	S+D
1	0	0	1	--	S=D
1	0	1	0	--	D
1	0	1	1	MERGEPAINT	~S+D
1	1	0	0	SRCCOPY	S
1	1	0	1	--	S+~D
1	1	1	0	SRCPAINT	S+D
1	1	1	1	Whiteness	1

5.4.4 Display Configuration Register

I/O Port: X3C4h

Index: Write value 03h to index port location X3C0h. This register is used when the Source Pitch bit (bit 3) in the BitBLT Mode Register is disabled.

Memory Map Location: B8F03h

Bits	Function
7	Enable Quick Start
6, 5	Data Width Write to GUI Engine
4-2	X Resolution
1,0	Pixel Depth

Bit 7: Enable Quick Start.
Logical 1: Enables Quick Start feature.
Logical 0: Disables Quick Start feature.

9004196 0000854 97T

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits 6,5: Data Width Write to GUI Engine. These bits are typically used for color expansion operations.

7	6	Data Width for GUI Engine Write
0	0	1 Byte
0	1	2 Bytes
1	0	4 Bytes
1	1	Reserved

Bits 4-2: X Resolution. Indicates X resolution of the current graphics display mode. The value is used to convert X/Y pixel addressing to linear pixel addressing.

4	3	2	X Resolution
0	0	0	640 pixels
0	0	1	800 pixels
0	1	0	1024 pixels
0	1	1	1280 pixels
1	0	0	1600 pixels
1	0	1	2048 pixels
1	1	0	Reserved
1	1	1	Reserved

Bits 1,0: Pixel Depth. Indicates pixel depth of current graphics display mode. The value is used to convert X/Y pixel addressing to linear pixel addressing.

1	0	Pixel Depth (bits/pixel)
0	0	Reserved
0	1	8
1	0	16
1	1	24

5.4.5 Source Start X/Diagonal Step Constant Register

I/O Port: X3C4h

Index: Write value 04h to index port location X3C0h

Memory Map Location: B8F04h

Bits	Function
15-(12)	Reserved
(14) 11-0	Source Start X Coordinate

Bits 15-(12): Reserved. Bit 15 is reserved when source is monochrome. Bits 15-12 are reserved when source is color

Bits (14)11-0: Source Start X Coordinate. Source start X coordinate for X/Y pixel addressing. Bits 14-0 are used when the source is monochrome. Bits 11-0 are used when the source is color.

Note If the Source Pitch bit (X3C4.01h bit 3) is set, bits 15-12 are reserved. Bits 11-3 are the lower nine bits of the source start linear address within the 2MB display memory space. Bits 2-0 represent the pixel position within one byte of the linear address.

When performing line draws which use the Bresenham algorithm, this register is defined as the Diagonal Step Constant Register. For the line draw case, bits 15 and 14 are reserved, and bits 13-0 contain the diagonal step constant value K2. The value K2 is determined in software by the following equation:

$$K2 = 2 * (\min(|dx|, |dy|) - \max(|dx|, |dy|))$$

5.4.6 Source Start Y/Axial Step Constant Register

I/O Port: X3C4h

Index: Write value 06h to index port location X3C0h

Memory Map Location: B8F06h

Bits	Function
15-(12)	Reserved
(14) 11-0	Source Start Y Coordinate/K1

Bits 15-(12): Reserved. Bit 15 is reserved when source is monochrome. Bits 15-12 are reserved when source is color.

9004196 0000855 806

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits (14)11-0: Source Start Y Coordinate. Source start Y coordinate for X/Y pixel addressing. Bits 14-0 are used when the source is monochrome. Bits 11-0 are used when the source is color.

Note If the Source Pitch bit (X3C4.01h bit 3) is set, bits 11-0 are the upper 12 bits of the source start linear address.

When performing line draw using the Bresenham algorithm, this register is defined as the Axial Step Constant Register. For the line draw case, bits 15 and 14 are reserved, and bits 13-0 contain the axial step constant value K1. The value K1 is determined in software by the following equation:
K1 = 2 * (min (|dx| , | dy|))

5.4.7 Destination Start X Register

I/O Port: X3C4h

Index: Write value 08h to index port location X3C0h

Memory Map Location: B8F08h

Bits	Function
15-12	Reserved
11-0	Destination Start X Coordinate

Bits 15-12: Reserved.

Bits 11-0: Destination Start X Coordinate. Specifies destination X coordinate for a BitBLT or Fast Polygon Fill operation.

5.4.8 Destination Start Y Register

I/O Port: X3C4h

Index: Write value 0Ah to index port location X3C0h

Memory Map Location: B8F0Ah

Bits	Function
15-12	Reserved
11-0	Destination Start Y Coordinate

Bits 15-12: Reserved.

Bits 11-0: Destination Start Y Coordinate. Specifies destination Y coordinate for a BitBLT or Fast Polygon Fill operation.

5.4.9 BitBLT Width/Short Stroke Register

I/O Port: X3C4h

Index: Write value 0Ch to index port location X3C0h.

Memory Map Location: B8F0Ch

BitBLT Width Case

Bits	Function
15-12	Reserved
11-0	BitBLT Width

Bits 15-12: Reserved.

Bits 11-0: BitBLT Width. Value programmed is width of BitBLT operation - 1.
When the Quick Start feature is enabled, a write to this register will engage the GUI engine to perform the function currently programmed into bit 7-5 of the GUI Engine Status/Start Register.

Short Stroke Vector Case

Bits	Function
15-13	Drawing Direction for Short Stroke Vector 0
12	Draw or Move for Short Stroke Vector 0
11-8	Pixel Length of Short Stroke Vector 0
7-5	Drawing Direction for Short Stroke Vector 1
4	Draw or Move for Short Stroke Vector 1
3-0	Pixel Length of Short Stroke Vector 1

Bits 15-13: Drawing Direction for Short Stroke Vector 0. Selects one of eight octants as follows:

Bit 15	14	13	Drawing Direction (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

9004196 0000856 742

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 12: Draw or Move for Short Stroke Vector 0. This bit may be used to draw a patterned short stroke vector.
Logical 1: Draw pixel. The color is determined by the value in the Foreground Color Register.
Logical 0: Move to next pixel location but do not draw pixel.

Bits 11-8: Pixel Length of Short Stroke Vector 0. The value programed equals the pixel length of the vector - 1.

Bits 7-5: Drawing Direction for Short Stroke Vector 1. Selects one of eight octants as follows:

Bit 7	6	5	Drawing Direction (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

Bit 4: Draw or Move for Short Stroke Vector 1. This bit may be used to draw a patterned short stroke vector.
Logical 1: Draw pixel. The color is determined by the value in the Foreground Color Register.
Logical 0: Move to next pixel location but do not draw pixel.

Bits 3-0: Pixel Length of Short Stroke Vector 1. The value programed equals the pixel length of the vector - 1.
Short Stroke Vector 0 is always drawn first.

5.4.10 BitBLT Height Register

I/O Port: X3C4h

Index: Write value 0Eh to index port location X3C0h

Memory Map Location: B8F0Eh

Bits	Function
15-12	Reserved
11-0	BitBLT Height

Bits 15-12: Reserved.

Bits 11-0: BitBLT Height. Value programmed is height of BitBLT operation - 1.

5.4.11 Error Term/Source Pitch Register

I/O Port: X3C4h

Index: Write value 12h to index port location X3C0h

Memory Map Location: B8F12h

Error Term Case (for Bresenham Line Draw)

Bits	Function
15, 14	Reserved
13-0	Error Term

Bits 15, 14: Reserved.

Bits 13-0: Error Term. The value programmed specifies the error term for a Bressenham Line Draw operation. The equation for determining the value follows:
For starting X location of the line < ending X location of the line -
Error Term=2 * min (|dx| , | dy |) - max (| dx | , | dy |) - 1
For starting X location of the line >= ending X location of the line -
Error Term=2 * min (|dx| , | dy |) - max (| dx | , | dy |)

Source Pitch Case (for BitBLT operations)

Bits	Function
15	Reserved
14-3	Source Pitch
2-0	Reserved

Bit 15: Reserved.

Bits 14-3: Source Pitch. Specifies the number of pixel locations from any pixel in a given row to the same pixel location in the next row. This value is used when Source Pitch operation is enabled. Bit 3 of X3C4.01 (BitBLT Mode Register) enables Source Pitch operation.

Bits 2-0: Reserved.

5.4.12 Foreground Color Register

I/O Port: X3C4h

Index: Write value 18h to index port location X3C0h

Memory Map Location: B8F18h

9004196 0000857 689

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits	Function
31-24	Reserved
23-0	Foreground Color

Bits 31-24: Reserved.

Bits 23-0: Foreground Color. The color value may be up to 24-bits. This color value may be used for Color Expansion, Area Fill, or Line Draw functions. For the color expansion case, a logical 1 from the monochrome source bitmap selects a foreground color fill. For Area Fill, the foreground color value is used to fill the given area. For Line Draw functions (Bressenham and Short Stroke), the foreground color value determines the color of the line.

5.4.13 Background Color Register

I/O Port: X3C4h

Index: Write value 1Ch to index port location X3C0h

Memory Map Location: B8F1Ch

Bits	Function
31-24	Reserved
23-0	Background Color

Bits 31-24: Reserved.

Bits 23-0: Background Color. The color value may be up to 24-bits. This color value is used for Color Expansion. A logical 0 from the monochrome source bitmap selects a background color fill.

5.4.14 Clip Left Register

I/O Port: X3C4h

Index: Write value 20h to index port location X3C0h

Memory Map Location: B8F20h

Bits	Function
15-12	Reserved
11-0	Clip Left Location

Bits 15-12: Reserved.

Bits 11-0: Clip Left Location. The value programmed specifies the left edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation beyond the left edge of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.4.15 Clip Right Register

I/O Port: X3C4h

Index: Write value 22h to index port location X3C0h

Memory Map Location: B8F22h

Bits	Function
15-12	Reserved
11-0	Clip Right Location

Bits 15-12: Reserved.

Bits 11-0: Clip Right Location. The value programmed specifies the right edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation beyond the right edge of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.4.16 Clip Top Register

I/O Port: X3C4h

Index: Write value 24h to index port location X3C0h

Memory Map Location: B8F24h

Bits	Function
15-12	Reserved
11-0	Clip Top Location

Bits 15-12: Reserved.

9004196 0000858 515

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits 11-0: Clip Top Location. The value programmed specifies the top edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation above the top of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.4.17 Clip Bottom Register

I/O Port: X3C4h

Index: Write value 26h to index port location X3C0h

Memory Map Location: B8F26h

Bits	Function
15-12	Reserved
11-0	Clip Bottom Location

Bits 15-12: Reserved.

Bits 11-0: Clip Top Location. The value programmed specifies the bottom edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation below the bottom of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.5 82C264 Extended Registers

The following is a detailed description of the 82C264's extended register set. The power-on default for all extended registers (with the exception of the Device ID Registers, 3D5.28 and 3D5.29) is 0h.

5.5.1 Unlock Extended Registers Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 10h to Sequencer Address Register location 3C4.

Bits	Function
7-0	Lock/Unlock the Extended Registers

Bits 7-0: Lock/Unlock Extended Registers. A value of XXXX1010 written to this register will unlock all OPTi 82C264 extended registers. Any other value written to this register will lock the extended registers. When the extended registers are locked, the value read back from this register is always 0Fh.

5.5.2 Mode Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 11h to Sequencer Address Register location 3C4.

Bits	Function
7, 6	Reserved
5	Divide INVCK by 3
4	Divide INVCK by 2
3	Select 32K or 64K Color Mode
2	Select True Color Mode
1	Select 15/16-Bit Per Pixel Mode
0	Select Extended 256-Color Mode

Bits 7, 6: Reserved.

Bit 5: Divide VCK by 3. Set to a logical 1 for true color modes. The Sequencer divides VCK by 3. The divided clock is then sent to the internal RAMDAC as the pixel clock.

9004196 0000859 451

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 4: Divide VCK by 2. Set to a logical 1 for 15/16-bit per pixel modes. The Sequencer divides VCK by 2. The divided clock is then sent to the internal RAMDAC as the pixel clock.

Bit 3: Select 32K or 64K Color Mode.
Logical 1: Selects 5-6-5 version of HiColor mode.
Logical 0: Selects 5-5-5 version of HiColor mode.

Bit 2: Select True Color Mode. Set this bit to a logical 1 to select true color mode.

Bit 1: Select 15/16-Bit Per Pixel Mode. Set this bit to a logical 1 to select HiColor mode.

Bit 0: Select Extended 256-Color Mode. Set this bit to a logical 1 to select and extended 256 color mode (e.g. 640x480, 800x600, 1024x768).

5.5.3 Clock Select Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 12h to Sequencer Address Register location 3C4.

Bits	Function
7	Enable Interlaced Mode
6, 5	Reserved
4	Do Not Allow Divide by 2 for INVCK
3	Divide INMCK by 2
2	Divide INVCK by 2
1	Select Internal/External Clock
0	IOVCK1 and IOVCK2 Direction Select

Bit 7: Enable Interlaced Mode
Logical 1: Enables interlaced mode.
Logical 0: Enables non-interlaced mode.

Bits 6, 5: Reserved

Bit 4: Do not allow divide by two for INVCK.
Logical 1: Do not allow INVCK to be divided by 2. This bit overrides bit 3 of the Clocking Mode Register (3C5.01).
Logical 0: Allow division of INVCK by two. Bit 3 of register 3C5.01 can be used to divide INVCK by two.
The setting of this bit has no effect on bit 2 of this register.

Bit 3: Divide INMCK by two.
Logical 1: Divide INMCK by two.
Logical 0: Do not divide INMCK by two.

Bit 2: Divide INVCK by two.
Logical 1: Divide INVCK by two.
Logical 0: Do not divide INVCK by two.

Bit 1: Select Internal/External Clock.
Logical 1: Selects Internal Clock. All other bits in this register are not used of the internal clock is selected.
Logical 2: Selects External Clock.

Bit 0: IOVCK1 and IOVCK2 Direction Select.
Logical 1: Defines IOVCK1 and IOVCK2 as clock select output pins 2 and 3 to the external clock chip. The logical level output for these signals is programmed by setting bits 6 and 5 respectively of this register.
Logical 0: Defines IOVCK1 and IOVCK2 as video clock inputs 2 and 3 to the 82C264. Video clock input 1 is IOVCK0. For this case, video clock selection is determined by bits 3 and 2 of the Miscellaneous Output Register (3C2).

5.5.4 Video FIFO Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 13h to Sequencer Address Register location 3C4.

Bits	Function
7, 6	Reserved
5, 4	Video FIFO Depth Select
3	Reserved
2-0	Video FIFO Threshold

Bits 7, 6: Reserved.

Bits 5, 4: Video FIFO Depth Select. Video FIFO depth is dependent upon mode selection.

5	4	Levels
0	0	16
0	1	12
1	0	8
1	1	4

Bit 3: Reserved.

9004196 0000860 173

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits 2-0 Video FIFO Threshold Select. When the number of empty levels in the Video FIFO is greater than or equal to the programmed threshold value, then the Video FIFO must be filled above the threshold before CPU access requests from the Write Buffer can be processed.

5.5.5 Write Buffer Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 14h to Sequencer Address Register location 3C4.

Bits	Function
7-5	Reserved
4	Tristate Control for DRAM Interface Pins
3	Screen Refresh Bandwidth Select
2	Reserved
1, 0	Select Write Buffer Depth

Bits 7-5: Reserved. Bits 7 and 6 are logical 0. Bit 5 is a logical 1.

Bit 4: Tristate Control for DRAM Interface Pins. This bit can be used for board testing.
Logical 1: Tristate RAS#, CAS#, WE#, OE#, and MA9-MA0.
Logical 0: Standard DRAM interface signal operations.

Bit 3: Screen Refresh Bandwidth Select.
Logical 1: Enables a video FIFO operation request to terminate a CPU access cycle.
Logical 0: Standard bandwidth allocation operations.

Bit 2: Reserved.

Bits 1, 0: Select Write Buffer Depth.

1	0	Levels
0	0	4
0	1	Reserved
1	0	2
1	1	0

5.5.6 Miscellaneous Control Register 1

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 15h to Sequencer Address Register location 3C4.

Bits	Function
7, 6	Reserved
5	DRAM Interface
4	Wrap-Around
3	Reserved
2	2MB DRAM
1	Select Asymmetric DRAM
0	INMCK Frequency Greater than 45MHz

Bits 7, 6: Reserved.

Bit 5: DRAM Interface. Set this bit to a logical 1 to support a 32-bit DRAM interface (eight 256Kx4 or two 256Kx16 DRAMs).
Set this bit to a logical 0 to support a 16-bit DRAM interface.

Bit 4: Wrap-Around.
Logical 1: Use this setting for modes that require more than 256K of memory.
Logical 0: Wrap around to start of display memory after 256K.

Bit 3: Reserved.

Bit 2: 2MB DRAM. Set this bit to a logical 1 to support 2MB of DRAM.

Bit 1: Select Asymmetric DRAM.
Logical 1: Selects asymmetric DRAM support. MA9-MA0 used to address the DRAM.
Logical 0: Selects standard DRAM support. MA8-MA0 used to address the DRAM.

Bit 0: INMCK Frequency Greater than 45MHz. Set this bit to a logical 1 when the frequency of INMCK is greater than 45MHz.

5.5.7 Miscellaneous Control Register 2

Read/Write Port: 3C5h

Index: This register is accessed by writing a value of 17h to Sequencer Address location 3C4h.

9004196 0000861 00T

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits	Function
7	Reserved
6	Feature Connector Enable
5	GRDY Enable
4	Reserved
3	Enable DPMS
2	CAS Precharge Adjust
1,0	CPU Bus Cycle Adjustment

Bit 7: Reserved.

Bit 6: Feature Connector Enable.
Logical 1: Enables Feature Connector.
Logical 0: Disables Feature Connector.
Feature Connector pin definitions backward compatible to the 92C168.

Bit 5: GRDY Enable.
Logical 1: Enables GRDY output (pin 151). This signal is used to define an overlay window area for 8-bit feature connector and as VAFC signal GRDY for 16-bit feature connector.
Logical 0: Disables GRDY output (pin 151)

Bit 4: Reserved.

Bit 3: Enable DPMS (Display Power Management Signaling).
Logical 1: Enables DPMS.
Logical 0: Disables DPMS.

Bit 2: CAS Precharge Adjust.
Logical 1: Set CAS precharge pulse to two MCLK cycles.
Logical 0: Set CAS precharge pulse to one MCLK cycle.

Bits 1.0: CPU Bus Cycle Adjustment.

1	0	MCLK Cycles
0	0	Standard I/O and Memory Cycles (default).
0	1	Reduce I/O and Memory Cycles by the value of 1MCLK
1	0	Reduce I/O and Memory Cycles by the value 2 MCLKs
1	1	Reduce I/O and Memory Cycles by the value 3 MCLKs

5.5.8 DDC/DPMS Register

Read Port: 3C5

Index: This register is accessed by writing a value of 18h to Sequencer Address Register location 3C4.

Bits	Function
7	VSYNC State
6	HSYNC State
5, 4	DPMS Control
3	Reserved
2	VSYNC Speed for DDC
1	DDC Pin Status (read only)
0	VSYNC Output Pin Status (read only)

Bit 7: VSYNC State. Sets VSYNC polarity when VSYNC is in its off state.
Logical 1: Polarity is high.
Logical 0: Polarity is low (default).

Bit 6: HSYNC State. Sets HSYNC polarity when HSYNC is in its off state.
Logical 1: Polarity is high.
Logical 0: Polarity is low (default).

Bits 5, 4: DPMS Control.

5	4	DPMS State
0	0	On
0	1	Standby (minimum power savings for monitor)
1	0	Suspend (substantial power savings for monitor)
1	1	Off (maximum power savings for monitor)

Bit 3: Reserved.

Bit 2: VSYNC Speed for DDC. BIOS sets this bit in accordance with the state of bits 1,0 of this register.
Logical 1: Sets VSYNC output to DDC requirements.
Logical 0: Standard VSYNC output (default)

Bit 1: DDC Input Pin Status (pin 116). This is a read-only bit for use by BIOS. BIOS can use this bit to monitor the state of signal DDC. If BIOS sees this bit and bit 0 are toggling, then BIOS will set bit 2 of this register for DDC requirements.

Bit 0: VSYNC Output Pin Status (pin 126). This is a read-only bit for use by BIOS. BIOS can use this bit to monitor the state of signal VSYNC. If BIOS sees this bit and bit 1 are toggling, then BIOS will set bit 2 of this register for DDC requirements.

9004196 0000862 T46

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.5.9 Configuration Register 0 (read only)

Read Port: 3C5

Index: This register is accessed by writing a value of 1Fh to Sequencer Address Register location 3C4. Bits 7-6 of this register correspond to MD31-MD30 respectively at power-up. BIOS reads these values at power-up and configures the appropriate extended registers.

Bits	Function
7	Enable/Disable Feature Connector
6	Enable/Disable PCI ROM Interface
5-0	Reserved

Bit 7 Enable/Disable Feature Connector.
Logical 1: Enable feature connector.
Logical 0: Disable feature connector

Bit 6 Enable/Disable PCI ROM Interface.
Logical 1: Enables PCI ROM interface.
Logical 0: Disables PCI ROM interface.

Bits 5-0: Reserved.

5.5.10 Configuration Register 1 (read only)

Read Port: 3C5h

Index: This register is accessed by writing a value of 2Eh to Sequencer Address location 3C4h. Bits 7-6 of this register correspond to MD15-MD14 respectively at power-up.

Bits	Function
7	Dual CAS# or Dual WE# DRAM Configuration
6	VGA Enable Port
5-0	Reserved

Bits 7: Dual CAS# or Dual WE# DRAM Configuration. When the Feature Connector is enabled, this bit reflects the value of MD15 at power-on.
Logical 1: Selects dual WE# DRAM configuration.
Logical 0: Selects dual CAS# DRAM configuration.

Bit 6: VGA Enable Port. When the Feature Connector is enabled, this bit reflects the value of MD14 at power-on.
Logical 1: Selects 46E8 as VGA enable port.
Logical 0: Selects 3C3 as VGA enable port.

Bits 5-0: Reserved.

5.5.11 OffsetA Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 20h to Graphics Controller Address Register location 3CE. This register is not used when linear addressing is enabled.

Bits	Function
7-5	Reserved
4-0 or [6-0]	Graphics Frame Buffer Offset for CPU Access

Bits 7-5: Reserved.

Bits 4-0: [6 -0] Graphics Frame Buffer Offset for CPU Access.
These frame buffer offset bits specify which 64K video memory segment is addressable through the standard VGA graphics mode memory access window (A0000-AFFFF). This register can programmed to function for CPU reads from display memory only, or for CPU read/writes from/to display memory. The register can also be programmed to use 64K (bits 4-0 of OffsetA select memory segment) or 16K (bits 6-0 of OffsetA select memory segment) offsets into the display memory. Bits 3, 1 and 0 of the Extended Mode Control Register (3CF.22) control the programming. Reference 3CF.22 for details.

5.5.12 OffsetB Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 21h to Graphics Controller Address Register location 3CE. This register is not used when linear addressing is enabled.

9004196 0000863 982

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits	Function
7-5	Reserved
4-0 or [6-0]	Graphics Frame Buffer Offset for CPU Access

Bits 7-5: Reserved.

Bits 4-0: [6 -0] Graphics Frame Buffer Offset for CPU Access.
These frame buffer offset bits specify which 64K video memory segment is addressable through the standard VGA graphics mode memory access window (A0000-AFFFF). This register can programmed to function for CPU writes to display memory only, or for CPU read/ writes from/to display memory. The register can also be programmed to used 64K (bits 4-0 of OffsetA select memory segment) or 16K (bits 6-0 of OffsetA select memory segment) offsets into display memory. Bits 3, 1 and 0 of the Extended Mode Control Register (3CF.22) control the programming. Reference 3CF.22 for details.

5.5.13 Extended Mode Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 22h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Memory Mapped I/O
6	Enable 16-bit Feature Connector Support
5	Enable 132-Column Text Mode
4	Enable 64K BIOS Decode
3	Offset Register Control Bit 2
2	PCI Burst Mode Enable
1	Offset Register Control Bit 1
0	Offset Register Control Bit 0

Bit 7: Enables/disables Memory Mapped I/O for the GUI Engine Register Set.
Logical 1: Enables Memory Mapped I/O at B8F00-B8F24. Bits 3, 2 of 3CF.06 must also be set to 0, 1 respectively to allow proper access to the GUI Engine Register Set.
Logical 0: Disables Memory Mapped I/O. Use I/O addresses to access the GUI Engine Register Set.

Bit 6: Enable 16-bit Feature Connector Support (PCI only)
Logical 1: Enables 16-bit feature connector support.
Logical 0: Disables 16-bit feature connector support.

Bit 5: Enable 132-Column Text Mode.
Logical 1: Enables 132-column text mode.
Logical 0: Standard 80 column text display.

Bit 4: Enable 64K BIOS decode.
Logical 1: Enables 64K video BIOS decode. Decode area is C0000-CFFFF.
Logical 0: Standard 32K video BIOS decode space. Decode area is C0000-C7FFF.

Bit 3: Offset Register Control Bit 2.
Logical 1: Enables register OffsetA as the display memory read segment register and enables register OffsetB as display memory write segment register.
Logical 0: Read/Write operations for register OffsetA and register OffsetB. Register OffsetB must be activated by bit 0 of this register before register OffsetB can be defined as a write only segment register or a read/write segment register.

Bit 2: PCI Burst Mode Enable.
Logical 1: Enables PCI Burst Mode for memory writes.
Logical 2: Disables PCI Burst Mode.

Bit 1: Offset Register Control Bit 1.
Logical 1: Configures OffsetA and OffsetB for 16KB offsets into display memory (bits 6-0 of the offset registers are used to program the address offset).
Logical 0: Configures OffsetA and OffsetB for 64KB offsets into display memory (bits 4-0 of the offset registers are used to program the address offset. Bits 5, 4 are reserved).

9004196 0000864 819

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 0: Offset Register Control Bit 0:
Logical 1: Activates register OffsetB.
Logical 0: Deactivates register OffsetB.

5.5.14 Hardware Cursor X Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 23h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor X Position

Bits 7-0: Hardware Cursor X Position.
Lower 8 bits of the Hardware Cursor X position. Writing this register activates the Cursor X position change. Bits 2-0 are used to set the inter-character position.

5.5.15 Hardware Cursor X Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 24h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Extended Inter-Character Position
6-3	Reserved
2-0	Hardware Cursor X Position

Bit 7: Extended Inter-Character Position. This bit is used along with bits 2-0 of the Hardware Cursor X Position Low Register to set the inter-character position of the hardware cursor.

Bits 6-3: Reserved.

Bits 2-0: Hardware Cursor X Position.
Upper 3 bits of the Hardware Cursor X position. Write this register first and then write the Hardware Cursor X Position Low Register to activate the X position change.

5.5.16 Hardware Cursor Y Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 25h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Y Position

Bits 7-0: Hardware Cursor Y Position.
Lower 8 bits of the Hardware Cursor Y position. Writing this register activates the Cursor Y position change.

5.5.17 Hardware Cursor Y Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 26h to Graphics Controller Address Register location 3CE.

Bits	Function
7-3	Reserved
2-0	Hardware Cursor Y Position

Bits 7-3: Reserved.

Bits 2-0: Hardware Cursor Y Position.
Upper 3 bits of the Hardware Cursor Y position. Write this register first and then write the Hardware Cursor Y Position Low Register to activate the Y position change.

5.5.18 Hardware Cursor Color 0 Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 27h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 0

Bits 7-0: Hardware Cursor Color 0.
Low byte of Hardware Cursor Color 0.

9004196 0000865 755

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.5.19 Hardware Cursor Color 0 Mid Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 28h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 0

Bits 7-0: Hardware Cursor Color 0.
2nd byte of Hardware Cursor Color 0.

5.5.20 Hardware Cursor Color 0 High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 29h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 0

Bits 7-0: Hardware Cursor Color 0.
High byte of Hardware Cursor Color 0.
Please note the following when programming color at particular color depths:
Pseudo-color: Load the color value to the Hardware Cursor Color 0 Low Register. Activate color by writing any value to the Hardware Cursor Color 0 High Register.
HiColor: Load the color value to the Hardware Cursor Color 0 Mid Register and Hardware Cursor Color 0 High Register. The high byte should be the last value written.
True color: Load the color value to all three cursor color 0 registers. The high byte should be the last value written.

5.5.21 Hardware Cursor Color 1 Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Ah to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 1

Bits 7-0: Hardware Cursor Color 1.
Low byte of Hardware Cursor Color 1.

5.5.22 Hardware Cursor Color 1 Mid Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Bh to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 1

Bits 7-0: Hardware Cursor Color 1.
2nd byte of Hardware Cursor Color 1.

5.5.23 Hardware Cursor Color 1 High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Ch to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Color 1

Bits 7-0: Hardware Cursor Color 1.
High byte of Hardware Cursor Color 1.
Please note the following when programming the Hardware Cursor color at particular color depths:
Pseudo-color: Load the color value to the Hardware Cursor Color 1 Low Register. Activate color by writing any value to the Hardware Cursor Color 1 High Register.
HiColor: Load the color value to the Hardware Cursor Color 1 Mid Register and Hardware Cursor Color 1 High Register. The high byte should be the last value written.
True color: Load the color value to all three cursor color 1 registers. The high byte should be the last value written.

9004196 0000866 691
Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.5.24 Hardware Cursor Pattern Offset Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Dh to Graphics Controller Address Register location 3CE.

Bits	Function
7-4	Reserved
3, 2	Select Hardware Cursor Pattern
1	Select Hardware Cursor Size
0	Enable Hardware Cursor

Bit 7-4: Reserved.

Bits 3, 2: Select Hardware Cursor Pattern. For a 32x32x2 Hardware Cursor off, bits 3 and 2 may be used to select one of four available patterns.

3	2	Pattern Location
0	0	F:FC00h
0	1	F:FD00h
1	0	F:FE00h
1	1	F:FF00h

For a 64x64x2 Hardware Cursor off, bit 2 may be used to select one of two available patterns. A logical 0 selects the pattern at F800h. A logical 1 selects the pattern at FC00h. Bit 3 should be set to a logical 0.

Bit 1: Select Hardware Cursor Size.
Logical 1: Selects 32x32x2 cursor.
Logical 0: Selects 64x64x2 cursor.

Bit 0: Enable Hardware Cursor.
Logical 1: Enables Hardware Cursor.
Logical 0: Disables Hardware Cursor.
The hardware cursor is always in the highest available bank of display memory.

5.5.25 Hardware Cursor Y Origin Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Eh to Graphics Controller Address Register location 3CE.

Bits	Function
7-6	Reserved
5-0	Hardware Cursor Y Origin

Bits 7, 6: Reserved.

Bits 5-0: Hardware Cursor Y Origin.
Specifies Y offset from the top-left corner of the cursor pattern. Used for case when part of the Hardware Cursor is off the screen edge. Bit 5 not used for 32x32x2 cursor.

5.5.26 Hardware Cursor X Origin Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Fh to Graphics Controller Address Register location 3CE.

Bits	Function
7	Extended Inter-Character Position
6	Reserved
5-0	Hardware Cursor X Origin

Bit 7: Extended Inter-Character Position. This bit is used with bits 2-0 to set the inter-character origin position.

Bit 6: Reserved.

Bits 5-0: Hardware Cursor X Origin.
Specifies X offset from the top-left corner of the cursor pattern. Used for case when part of the Hardware Cursor is off the screen edge. Bit 5 not used for 32x32x2 cursor. Bits 2-0 set inter-character origin position.

5.5.27 Scratch Pad Register 0

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 1Ch to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Scratch Pad Bits

Bits 7-0: Scratch Pad Bits.
Scratch pad bits 7-0.

9004196 0000867 528

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.5.28 Extended Overflow Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 30h to CRT Controller Address Register location 3D4. Bit 5 of the CRT Extended Control Register (3D5.33) must be a logical 0 in order to access this register.

Bits	Function
7	Reserved
6, 5	Offset Bits 9, 8
4	Line Compare Bit 10
3	Vertical Total Bit 10
2	Vertical Display Enable End Bit 10
1	Vertical Blank Start Bit 10
0	Vertical Retrace Start Bit 10

Bit 7: Reserved.

Bits 6,5: Offset Bits 9, 8.
The lower eight bits of the offset value are located in the CRTC Offset Register (3D5.13). The ten bit value specifies the address width of the display. The value corresponds to the difference between the addresses of two vertically neighboring pixels.

Bit 4: Line Compare Bit 10.
Bit 9 is located in the Maximum Scan Line Register (3D5.09). Bit 8 is located in the Vertical Overflow Register (3D5.07). Bits 7-0 are located in the Line Compare Register (3D5.18). The 11-bit value is used for split screen display.

Bit 3: Vertical Total Bit 10.
Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Total Register (3D5.06). The 11-bit value specifies the total number of displayed and undisplayed scan lines for a given mode.

Bit 2: Vertical Display Enable Bit 10.
Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Display Enable End Register. The 11-bit value specifies the last horizontal scan line to be displayed on the screen.

Bit 1: Vertical Blank Start Bit 10.
Bit 9 is located in the Maximum Scan Line Register (3D5.09). Bit 8 is located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Display Enable End Register (3D5.12). The 11-bit value specifies the horizontal scan line at which the data stream to the display is stopped during the vertical retrace period.

Bit 0: Vertical Retrace Start Bit 10.
Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Retrace Start Register (3D5.10). The 11-bit value specifies the horizontal scan line count at which the vertical sync pulse is generated.

5.5.29 Starting Address Overflow Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 31h to CRT Controller Address Register location 3D4.

Bits	Function
7	Reserved
6	Enable Interlaced Mode
5-3	Reserved
2-0	Starting Address Overflow Bits 18-16

Bit 7: Reserved.

Bit 6: Enable Interlaced Mode. Set this bit along with bit 7 of 3C5.12 (Clock Select Register) to a logical 1 to enable interlaced Mode.

Bits 5-3: Reserved.

Bits 2, 0: Starting Address Overflow Bits 18-16.
Bit 15-8 are located in the Start Address High Register (3D5.0C). Bits 7-0 are located in the Start Address Low Register (3D5.0D). The 19-bit value specifies the address in display memory which corresponds to the upper left corner of the screen.

9004196 0000868 464

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.5.30 Interlaced Odd Frame Horizontal Retrace End Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 32h to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Interlaced Odd Frame Horizontal Retrace End

Bit 7-0: Interlaced Odd Frame Horizontal Retrace End.
Specifies the horizontal sync pulse width for the odd frame of an interlaced mode (e.g. 1024x768).

5.5.31 Extended CRT Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 33h to CRT Controller Address Register location 3D4.

Bits	Function
7-3	Reserved
2	BLANK# Select
1	Enable Starting Address Double Buffering
0	Reserved

Bits 7-3: Reserved.

Bit 2: BLANK# Select.
Logical 1: Blanking is enabled at Display Enable End. This setting will eliminate screen borders.
Logical 0: Standard Blanking signal.

Bit 1: Enable Starting Address Double Buffering.
Logical 1: Enables double buffering for the Starting Address High Register (3D5.0C) and Starting Address Low Register (3C5.0D). This setting is useful for applications which need to continually change the starting address (e.g. switching between two images in display memory to create animation effects).
Logical 0: Standard access for 3D5.0C and 3D5.0D.

Bit 0: Reserved.

5.5.32 External RAMDAC Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 36h to CRT Controller Address Register location 3D4.

Bits	Function
7-5	Reserved
4	Select External RAMDAC
3-0	Reserved

Bits 7-5: Reserved.

Bit 4: Select External RAMDAC.
Logical 1: Selects external RAMDAC.
Logical 0: Selects internal RAMDAC (default).

Bits 3-0: Reserved.

9004196 0000869 3T0

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.6 Clock Synthesizer Register Descriptions

The clock synthesizers registers are accessed by sending a register index value to port 3C4h, followed by data.

5.6.1 Video Clock Group 0 (VCK0) Input Frequency Divider

Write Port: 3C4h

Index: 20h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 1Fh.

5.6.2 Video Clock Group 0 (VCK0) VCO Frequency Divider

Write Port: 3C4h

Index: 21h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 6Dh.

5.6.3 Video Clock Group 1 (VCK1) Input Frequency Divider

Write Port: 3C4h

Index: 22h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 17h.

5.6.4 Video Clock Group 1 (VCK1) VCO Frequency Divider

Write Port: 3C4h

Index: 23h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 5Bh.

5.6.5 Video Clock Group 2 (VCK2) Input Frequency Divider

Write Port: 3C4h

Index: 24h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

9004196 0000870 012

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default.)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 23h.

5.6.6 Video Clock Group 2 (VCK2) VCO Frequency Divider

Write Port: 3C4h

Index: 25h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 58h.

5.6.7 Video Clock Group 3 (VCK3) Input Frequency Divider

Write Port: 3C4h

Index: 26h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default.)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 18h.

5.6.8 Video Clock Group 3 (VCK3) VCO Frequency Divider

Write Port: 3C4h

Index: 27h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 45h.

5.6.9 Memory Clock Input Frequency Divider

Write Port: 3C4h

Index: 28h

Bit	Definition
7, 6	Reserved.
5-0	Frequency Divider Value (D).

Bits 7,6: Reserved

Bits 5-0: Frequency Divider Value. This value is designated "D". Default value after power-up is 10h.

5.6.10 Memory Clock VCO Frequency Divider

Write Port: 3C4h

Index: 29h

Bit	Definition
7	Reserved.
6-0	VCO Frequency Divider Value (N).

Bit 7: Reserved.

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 2Ah.

9004196 0000871 T59

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.6.11 Programming Video Clock and Memory Clock Frequencies

The video clock group is selected by setting bits 3,2 (see table) of the Miscellaneous Function Control Register (3C2).

Bit 3	Bit 2	VCK Clock Group
0	0	Video Clock Group 0
0	1	Video Clock Group 1
1	0	Video Clock Group 2
1	1	Video Clock Group 3

Equations for VCK and MCK frequency selection follow.

5.6.11.1 Equations for VCK and MCK Frequency Selection

The output frequency of the selected video clock group is determined by the following equation:

$$Fv = \frac{(14.318MHz \times N/D)}{(P+1)}$$

Where:

- Fv is the video clock output for the given video clock group
- N is the video clock VCO divider value
- D is the video clock input clock divider value
- P is the post scale

The output frequency of the selected video clock group is determined by the following equation:

$$Fm = \frac{14.318MHz \times N}{(int(D/4) \times 4)}$$

Where:

- Fv is the memory clock output
- N is the memory clock VCO divider value
- D is the memory clock input clock divider value.

Note In order to reduce frequency error, D for the memory clock should be divisible by four.

5.7 Overlay Control Registers

5.7.1 Overlay Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 40h to Graphics Controller Address Register location 3CE.

Bits	Function
7, 6	Color Key Control
5	DAC Color Mode Control
4 - 2	Input Data Color Mode
1, 0	Overlay Select

Bit 7, 6: Color Key Comparison Select. Bits 1 and 0 determine the Color Key equation when overlay with color key selected.

1 0 Color Key Equation
0 0 Overlay will occur when pixel data = color key
0 1 Overlay will occur when pixel data < color key
1 0 Overlay will occur when pixel data > color key
1 1 Reserved

Bit 5: DAC Color Mode Control.
Logical 1: When the overlay condition is true, the DAC will switch to the same color mode as the incoming data from the feature connector. When the overlay condition is false, the DAC will remain in the currently selected graphics mode.
Note: The color mode for the incoming feature connector data is defined by bits 4-2 of this register.
Logical 0: The DAC color mode will not switch for a true overlay condition.

Bit 4-2: Input Data Color Mode.

2	1	0	Color Mode
0	0	0	8-bit/pixel using CLUT
0	0	1	8-bit/pixel grayscale
0	1	0	8-bit RGB (3:3:2 format)
0	1	1	Reserved
1	0	0	15-bit RGB (5:5:5 format)
1	0	1	16-bit RGB (5:6:5 format)
1	1	0	Reserved
1	1	1	Reserved

9004196 0000872 995
Powered by ICminer.com Electronic-Library Service CopyRight 2003

Note For RGB (3:3:2) format, R=P7-P5, G=P4-P2, B=P1-P0.
For RGB (5:5:5) format, R=P14-P10, G=P9-P5, B=P4-P0.
For RGB (5:6:5) format, R=P15-P10, G=P9-P5, B=P4-P0.
Where P[x] is a given pixel data signal on the feature connector.

Note 8-bit feature connector option: For 15 and 16-bit RGB modes, data is clocked in at the rising and falling edge of DCLK. For all other modes, data is clocked in at the rising edge of DCLK.

Bits 1,0: Overlay Select. Selects overlay mode type.

1	0	Overlay Mode
0	0	Overlay disabled
0	1	Overlay using EVIDEO#
1	0	Overlay with Color Key and EVIDEO#
1	1	Overlay with Color Key

5.7.2 Color Key Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 41h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	8-bits of Color Key

Bits 7-0: 8-bits of Color Key. 8-bits of the color key value.

5.7.3 Color Key Mask Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 42h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	8-bits of Color Key Mask

Bits 7-0: 8-bits of Color Key. 8-bits of the color key mask. Each bit corresponds to a pixel on the screen. Pixel display is from Most Significant Bit to Least Significant Bit. A logical 1 causes the given pixel to be masked. Please note the following when programming the color key mask at particular color depths:
Pseudo-color: Load the color key mask to Color Key Mask Register 0.

5.7.4 Overlay Window Horizontal Start Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 45h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Horizontal Start

Bits 7-0: Overlay Window Horizontal Start. Bits 10-3 of the overlay window horizontal start value. Bits 2-0 located in the Overlay Window Horizontal Pixel Alignment Register.

5.7.5 Overlay Window Horizontal End Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 46h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Horizontal End

Bits 7-0: Overlay Window Horizontal Start. Bits10-3 of the overlay window horizontal start value. Bits 2-0 located in the Overlay Window Horizontal Pixel Alignment Register.

5.7.6 Overlay Window Horizontal Pixel Alignment Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 47h to Graphics Controller Address Register location 3CE.

9004196 0000873 821

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits	Function
7	Reserved
6-4	Bits 2-0 of Overlay Window Horizontal End
3	Reserved
2-0	Bits 2-0 of Overlay Window Horizontal Start

Bit 7: Reserved.

Bits 6-4: Bits 2-0 of Overlay Window Horizontal End

Bit 3: Reserved.

Bits 2-0: Bits 2-0 of Overlay Window Horizontal Start

5.7.7 Overlay Window Vertical Start Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 48h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Vertical Start

Bits 7-0: Overlay Window Vertical Start. Lower 8-bits of the overlay window vertical start value. Bits 8 and 9 are located in the Overlay Window Vertical Overflow Register.

5.7.8 Overlay Window Vertical End Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 49h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Vertical End

Bits 7-0: Overlay Window Vertical End. Lower 8-bits of the overlay window vertical end value. Bits 8 and 9 are located in the Overlay Window Vertical Overflow Register.

5.7.9 Overlay Window Vertical Overflow Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 4Ah to Graphics Controller Address Register location 3CE.

Bits	Function
7-4	Reserved
3, 2	Bits 8 and 9 of Overlay Vertical Window End
1, 0	Bits 8 and 9 of Overlay Vertical Window Start

Bits 7-4: Reserved.

Bits 3, 2: Overlay Window Vertical End. Upper two bits of overlay window vertical end value.

Bits 1, 0: Overlay Window Vertical Start. Upper two bits of overlay window vertical end value.

5.7.10 Genlock Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 4Bh to Graphics Controller Address Register location 3CE.

Bits	Function
7	Enable VSYNC Genlock
6	Enable HSYNC Genlock
5-3	Horizontal Total Adjust for HSYNC Genlock
2-0	Horizontal Sync Adjust for HSYNC Genlock

Bit 7: Enable VSYNC Genlock.
Logical 1: Enables VSYNC Genlock. VSYNC becomes an input to the 82C264 and is used to genlock the 82C264 to an external video source.
Logical 0: Disables VSYNC genlock.

Bit 6: Enable HSYNC Genlock.
Logical 1: Enables HSYNC genlock. HSYNC becomes an input to the 82C264 and is used to genlock the 82C264 to an external video source.
Logical 0: Disables HSYNC genlock.
To activate HSYNC genlock and VSYNC genlock at the same time, program bits 7,6 to a logical 1.

9004196 0000874 768

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bits 5-3: Horizontal Total Adjust for HSYNC Genlock. Allows adjustment of the Horizontal Total as follows:

5	4	3	Adjustment (VCLK)
0	0	0	No adjustment
0	0	1	-4
0	1	0	-3
0	1	1	-2
1	0	0	-1
1	0	1	+1
1	1	0	+2
1	1	1	+3

Bits 2-0: Horizontal Sync Adjust for HSYNC Genlock. Allows adjustment of Horizontal Sync Start (relative to BLANK#) as follows:

2	1	0	Adjustment (VCLK delay)
0	0	0	No adjustment
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.8 PCI Configuration Space Description

Table 5-14 shows the header region of the 82C264's PCI configuration space. An explanation of each of the registers within the header follows the table.

Table 5-14 Configuration Space Layout

Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision	08h
BIST	Header Type	Latency Timer	Cache Line Size	0h
Base Address Registers				10h 14h 18h 1Ch 20h 24h
Reserved				28h
Reserved				2Ch
Expansion ROM Base Address				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

A description of each of the PCI Configuration Space Registers follows. For clarity, the registers have been grouped by function type. Five categories are listed: Device Identification, Device Control, Device Status, Other Functions, and Base Address.

9004196 0000875 6T4

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.8.1 Device Identification

5.8.1.1 Vendor ID Register (read only)

Byte location within the Configuration Space Header: 00h-01h

Bits	Function
15-0	Vendor ID Code

Bits 15-0: Vendor ID Code. The Vendor ID code identifies OPTi as the manufacturer of the 82C264. This code is assigned by the PCI SIG. The assigned Vendor ID code for OPTi is 1045h.

5.8.1.2 Device ID Register (read only)

Byte location within the Configuration Space Header: 02h-03h

Bits	Function
15-0	Device ID Code

Bits 15-0: Device ID Code. The Device ID code identifies the 82C264. This code is assigned by OPTi. The Device ID code for OPTi is C101h.

5.8.1.3 Revision ID Register (read only)

Byte location within the Configuration Space Header: 08h

Bits	Function
7-0	Revision ID Code

Bits 7-0: Revision ID Code. The Revision ID code indicates the revision number of the 82C264.

5.8.1.4 Class Code Register (read only)

Byte location within the Configuration Space Header: 09h - 11h

Bits	Function
23-16	Base Class Code
15-8	Sub-Class Code
7-0	Programming Interface Identifier

Bits 23-16: Base Class Code. Defines type of function the 82C264 performs. The Base Class Code Value is 03h, which identifies the 82C264 as a Display Controller.

Bits 15-8: Sub-Class Code. Defines the Display Controller type for 82C264. The Sub-Class Code value is 00h, which identifies the 82C264 as a VGA Compatible Controller or 8514 Compatible Controller.

Bits 7-0: Programming Interface Identifier. Defines the programming interface for the 82C264. The Programming Interface Identifier value is 00h, which identifies the programming interface as that of a VGA Compatible Controller.

5.8.1.5 Header Type Register (read only)

Byte location within the Configuration Space Header: 0Eh

Bits	Function
7	Single/Multi-function Device
6-0	Configuration Space Layout

Bit 7: Single/Multi-function Device. This bit is set to a logical 0 which indicates a single function device.

Bits 6-0: Configuration Space Layout. Defines layout for bytes 10h and up of the PCI configuration space header. The 82C264 supports a 00h Header Type.

5.8.2 Device Control

5.8.2.1 Command Register

Byte location within the Configuration Space Header: 04h - 05h

Bits	Function
15-7	Reserved
6	Parity Error Response
5	VGA Palette Snoop
4	Reserved
3	Special Cycles
2	Bus Master
1	Memory Space
0	I/O Space

When a value of 0h is written to this register, the 82C264 will not respond to any PCI bus accesses except for Configuration Space accesses. Definitions of the individual bits within the Command Register follow:

Bits 15-7: Reserved. Returns a logical 0 when read.

9004196 0000876 530

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 6: Parity Error Response. This bit is set to a logical 0. A logical 0 means the 82C264 will ignore any parity errors it detects and continue normal operations.

Bit 5: VGA Palette Snoop. Enables/Disables palette snooping.
Logical 1: Enables palette snooping.
Logical 0: Disables palette snooping.

Bit 4: Reserved. Returns a logical 0 when read.

Bit 3: Special Cycles. Special Cycle control. This bit is set to a logical 0. A logical 0 means the 82C264 will ignore all Special Cycle operations.

Bit 2: Bus Master. Since the 82C264 is not a bus master, this bit is set to a logical 0. A logical 0 disables the 82C264 from generating PCI accesses.

Bit 1: Memory Space. Enables/Disables the 82C264's response to memory accesses.
Logical 1: Enables response to memory accesses.
Logical 0: Disables response to memory accesses (default after RESET#).

Bit 0: I/O Space. Enables/Disables the 82C264's response to I/O accesses.
Logical 1: Enables response to I/O accesses.
Logical 0: Disables response to I/O accesses (default after RESET#).

5.8.3 Device Status

5.8.3.1 Command Register

Byte location within the Configuration Space Header: 06h - 07h

Bits	Function
15-11	Reserved
10-9	DEVSEL# Timing
8	Reserved
7	Fast Back-to-Back Capable
6-0	Reserved

Bit 15-11: Reserved. Returns a logical 0 when read.

Bit 10-9: DEVSEL# Timing. These bits are set to 01b and are read only. The value indicates that DEVSEL# will be asserted a maximum of two clock cycles after the address phase.

Bit 8: Reserved. Returns a logical 0 when read.

Bit 7: Fast Back-to-Back Capable. This bit is set to a logical 0. A logical 0 indicates the 82C264 does not support Fast Back-to-Back transactions which are not to the same agent.

Bit 6-0: Reserved. Returns a logical 0 when read.

5.8.4 Other Functions

The following registers in this functional group are reserved:

- Cache Line Size Register - byte location 0Ch in the Configuration Space Header
- Latency Timer Register - byte location 0Dh in the Configuration Space Header
- BIST Register - byte location 0Fh in the Configuration Space Header
- MIN_GNT Register - byte location 3Eh in the Configuration Space Header
- MAX_LAT Register - byte location 3Fh in the Configuration Space Header

All of the above registers return 00h when read.

The following interrupt registers are also in this functional group.

5.8.4.1 Interrupt Line Register

Byte location within the Configuration Space Header: 3Ch

Bits	Function
7-0	Interrupt Line Routing Information

Bits 7-0: Interrupt Line Routing Information. Value in this register indicates which system interrupt pin the 82C264's interrupt pin is connected to. POST software will write the routing information to the Interrupt Line Register as the system is initialized and configured. The value in this register depends on the system architecture.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

5.8.4.2 Interrupt Pin Register (read only)

Byte location within the Configuration Space Header: 3Dh

Bits	Function
7-0	Interrupt Pin Information

Bits 7-0: Interrupt Pin Information. The value in this register indicates which interrupt pin the 82C264 uses. For 82C264, the value in this register is 01h, which corresponds to INTA#.

5.8.5 Base Address Registers

The following Base Address Register locations are reserved:

- Base Address Location 18h - Reserved
- Base Address Location 1Ch - Reserved
- Base Address Location 20h - Reserved
- Base Address Location 24h - Reserved

Definitions of the remaining Base Address Register locations follow:

5.8.5.1 Base Address Register Location 10h

Bits	Function
31-2	I/O Space Base Address
1	Reserved
0	I/O Space Indicator

Bits 31-16: hardwired to logical 0.

Bits 15-12: These bits are writable. Gives 4K address space.

Bits 11-2: Hardwired to logical 0.

Bit 1: Reserved. Returns a logical 0 when read.

Bit 0: I/O Space Indicator. This bit is hardwired to a logical 1. A logical 1 indicates this is the base address for an I/O space.

5.8.5.2 Base Address Register Location 14h

Bits	Function
31-4	Memory Space Base Address
3	Prefetchable
2-1	Type
0	Memory Space Indicator

Bits 31-22: Bits 31-22: These bits are writable. Gives 4M address space.

Bits 21-4: Hardwired to logical 0.

Bit 3: Prefetchable. This bit is a logical 0 for the 82C264. A logical 0 indicates the video memory space is not prefetchable.

Bits 2-1: Type. These bits are set to 00b for the 82C264. This value indicates the defined 4M memory space may be located anywhere within the 32-bit address space.

Bit 0: Memory Space Indicator. This bit is hardwired to a logical 0. A logical 0 indicates this is the base address for an memory space.

5.8.5.3 Expansion ROM Base Address Register

Byte location within the Configuration Space Header: 30h - 33h

Bits	Function
31-11	Expansion ROM Base Address
10-1	Reserved
0	Address Decode Enable

Bits 31-22: These bits are writable. Gives 4M address space.

Bits 21-11: Logical 0.

Bits 10-1: Reserved. These bits will return a logical 0 value when read.

Bit 0: Address Decode Enable. A logical 1 enables access to the expansion ROM base address. Note: Bit 1 in the Command Register must also be set to a logical 1 to enable access to the expansion ROM base address.

9004196 0000878 303

Powered by ICminer.com Electronic-Library Service CopyRight 2003

6.0 Electrical Specification

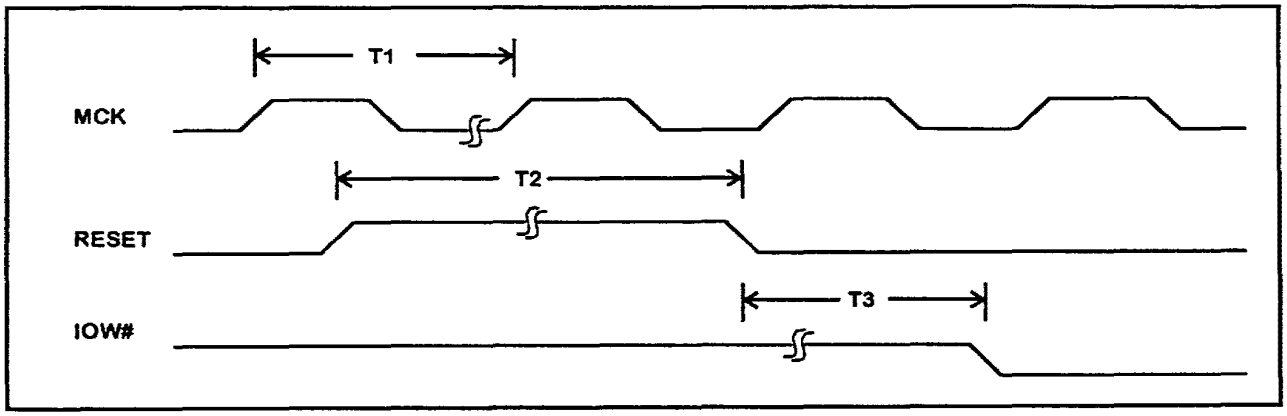
6.1 Internal DAC Specifications

Table 6-1 Internal DAC Specifications

Symbol	Parameter	Min.	Typical	Max.	Units	Notes
	DAC Resolution	8	8	8	bits	
IL	Integral Linearity Error	--	--	1/2	LSB	
DL	Differential Linearity Error	--	--	1/2	LSB	
	White Level Relative to Black	--	14.0	--	mA	VREF = 1.22V RSET = 690Ωs
	LSB Size	--	55	--	µA	VREF = 1.22V RSET = 690Ωs
RSET	FADJ Resistor Value	--	690	--	ohms	50Ω load
RL	Output Load	--	50	--	ohms	
VREF	Voltage Reference	--	1.22	--	volts	

6.2 AC Timing Characteristics

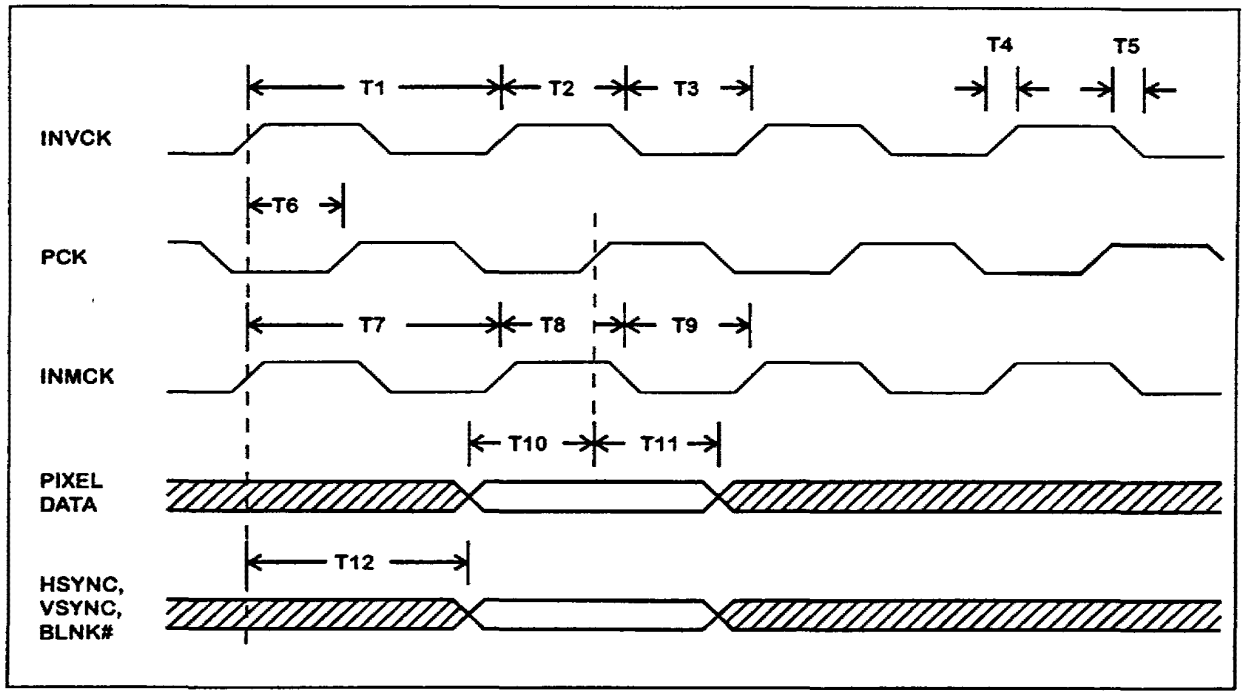
Figure 6-1 Clock and Reset Timing



Symbol	Description
T1	50MHz
T2	16Ti
T3	16Ti

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-2 Clock and Video Timing

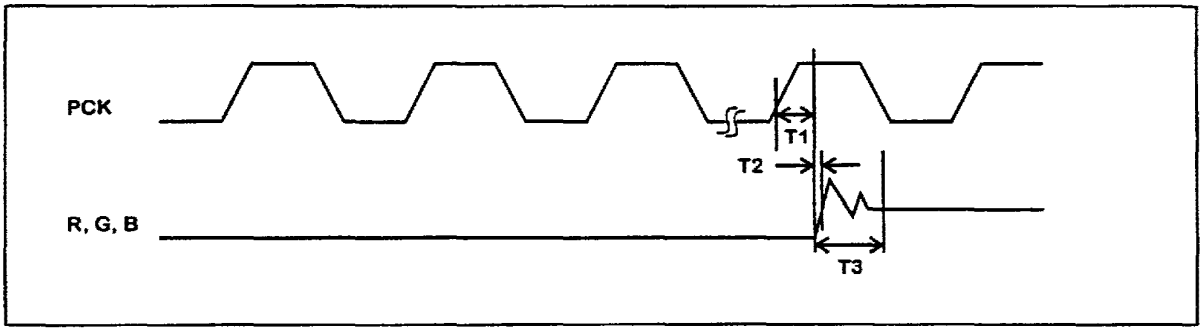


Symbol	Description	Min (ns)	Max (ns)
T1	INVCK Period	14	
T2	INVCK High	5	
T3	INVCK Low	5	
T4	INVCK Rise Time		2
T5	INVCK Fall Time		2
T6	PCK to INVCK Delay	7	
T7	INMCK Period	20	
T8	INMCK High	9	
T9	INMCK Low	9	
T10	Pixel Data Setup to PCK	4	
T11	Pixel Data Hold from PCK	8	
T12	HSYNC, VSYNC to INVCK Delay		

9004196 0000880 T61

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-3 RAMDAC Timing (Analog Outputs)



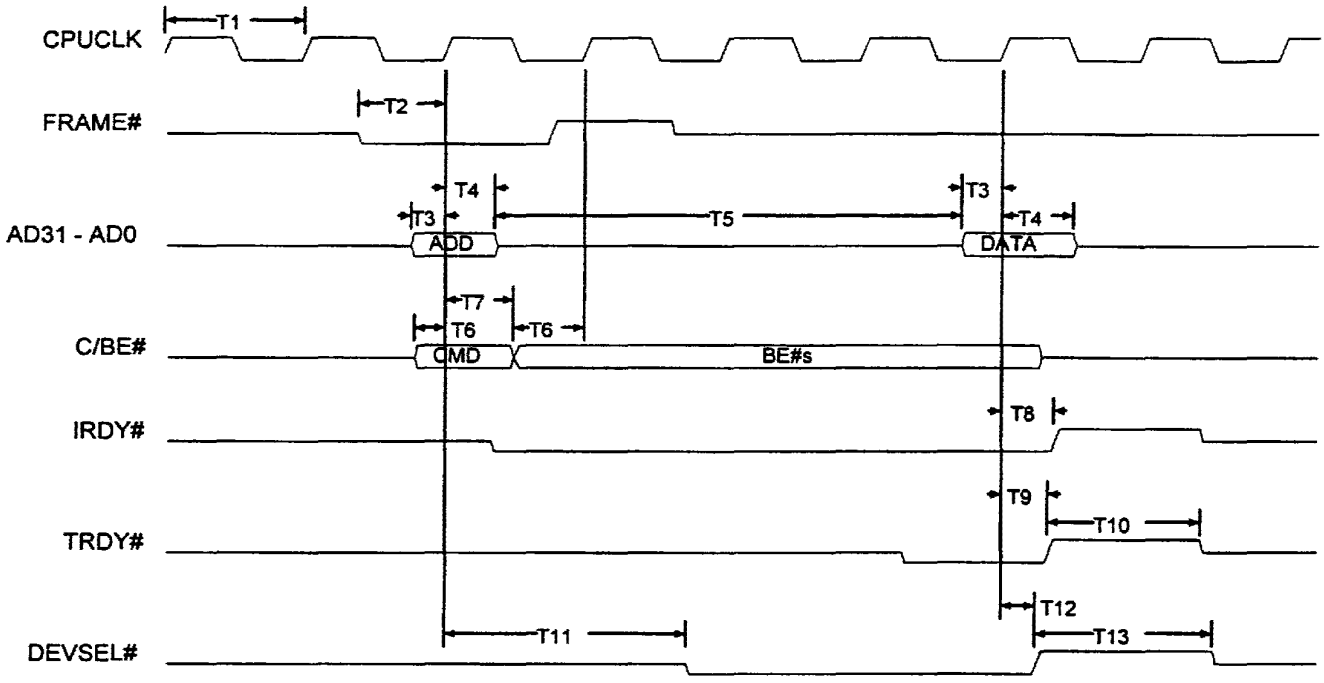
Symbol	Description	Min (ns)	Typ (ns)	Max (ns)
T1	Analog Output Delay	--	6	
T2	Analog Output Rise/Fall Time[1]	--	3/8	
T3	INVCK Low	--	12	

1. Defined as 10% to 90% of final value.

9004196 0000881 9T8

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-4 Basic Read/Write Operation (PCI)

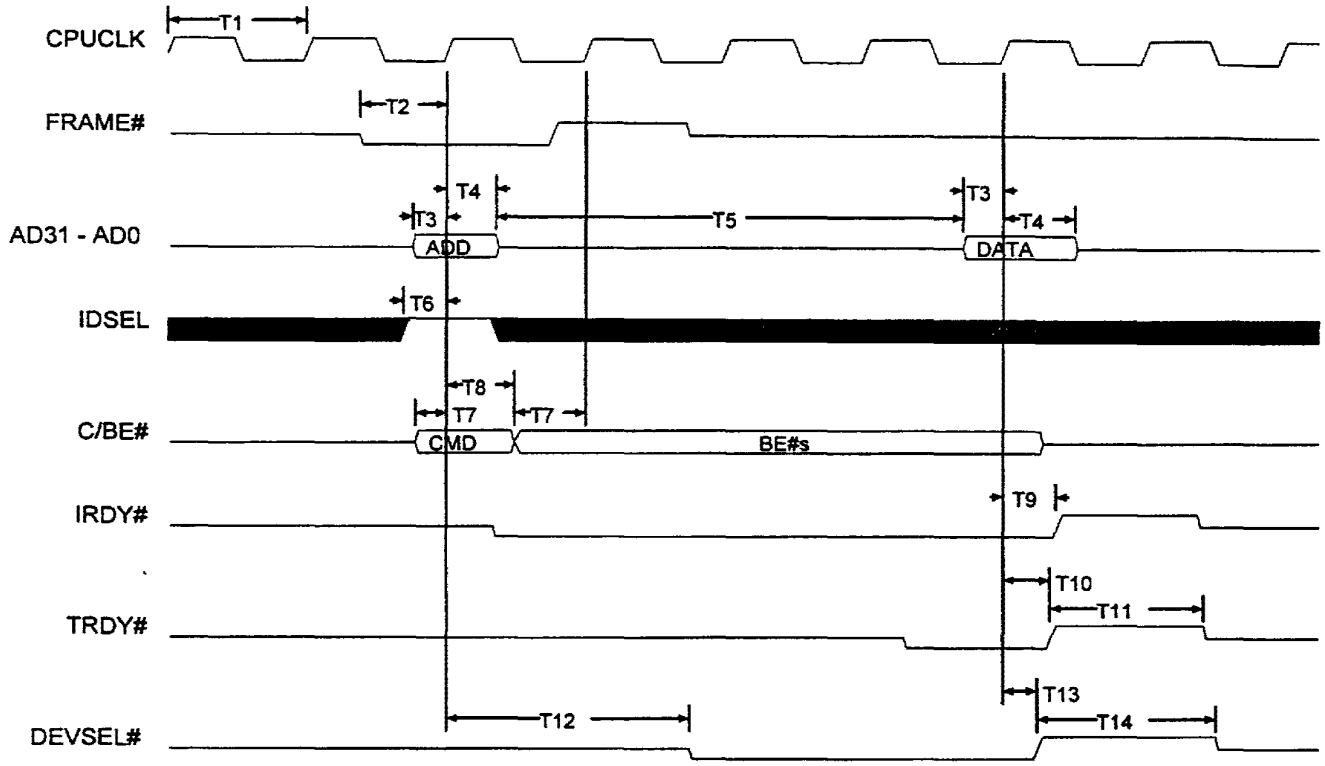


Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	FRAME# setup to CPUCLK	7	
T3	Address/Data setup to CPUCLK	7	
T4	Address/Data hold from CPUCLK	0	
T5	Address Phase to Data Phase		4T
T6	Bus Command setup to CPUCLK	7	
T7	Bus Command hold from CPUCLK	0	
T8	IRDY# hold from CPUCLK	0	
T9	TRDY# delay from CPUCLK	2	
T10	TRDY# high before HI-Z	1T	
T11	Address Phase to DEVSEL#		2T
T12	DEVSEL# delay from CPUCLK	2	
T13	DEVSEL# delay from CPUCLK	1T	

9004196 0000882 834

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-5 Configuration Read/Write Operation (PCI)

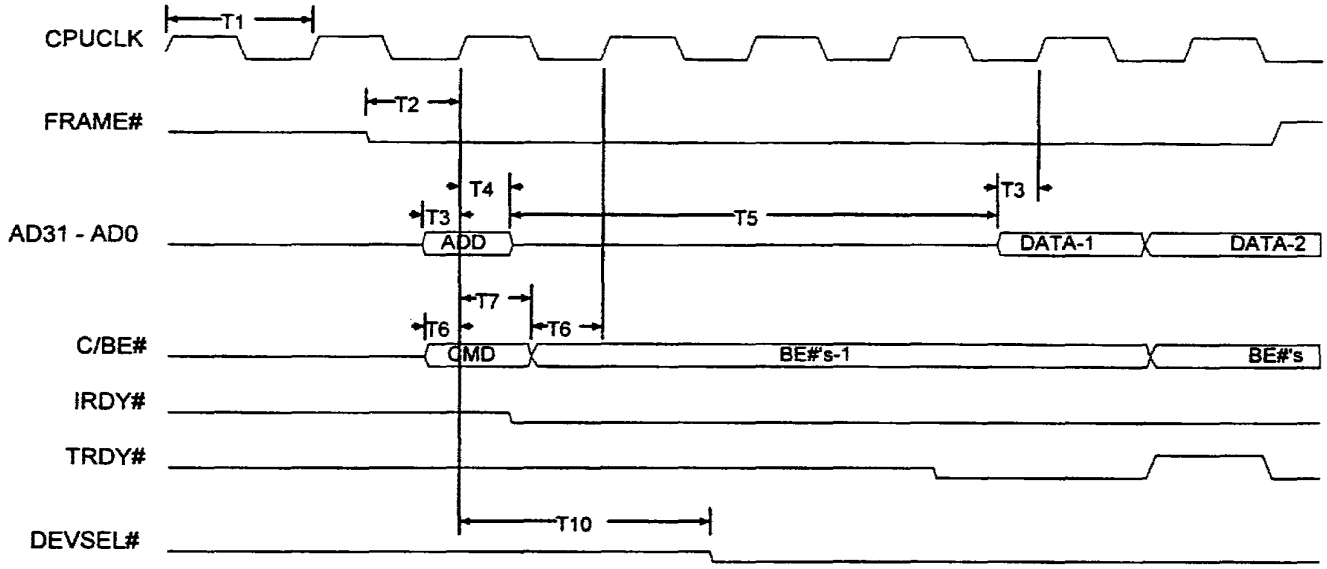


Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	FRAME# setup to CPUCLK	7	
T3	Address/Data setup to CPUCLK	7	
T4	Address/Data hold from CPUCLK	0	
T5	Address Phase to Data Phase		4T
T6	IDSEL setup to CPUCLK	7	
T7	Bus Command setup to CPUCLK	7	
T8	Bus Command hold from CPUCLK	0	
T9	IRDY# hold from CPUCLK	0	
T10	TRDY# delay from CPUCLK	2	
T11	TRDY# high before HI-Z	1T	
T12	Address Phase to DEVSEL#		2T
T13	DEVSEL# delay from CPUCLK	2	
T14	DEVSEL# high before HI-Z	1T	

9004196 0000883 770

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-6 Burst Write Operation (PCI)

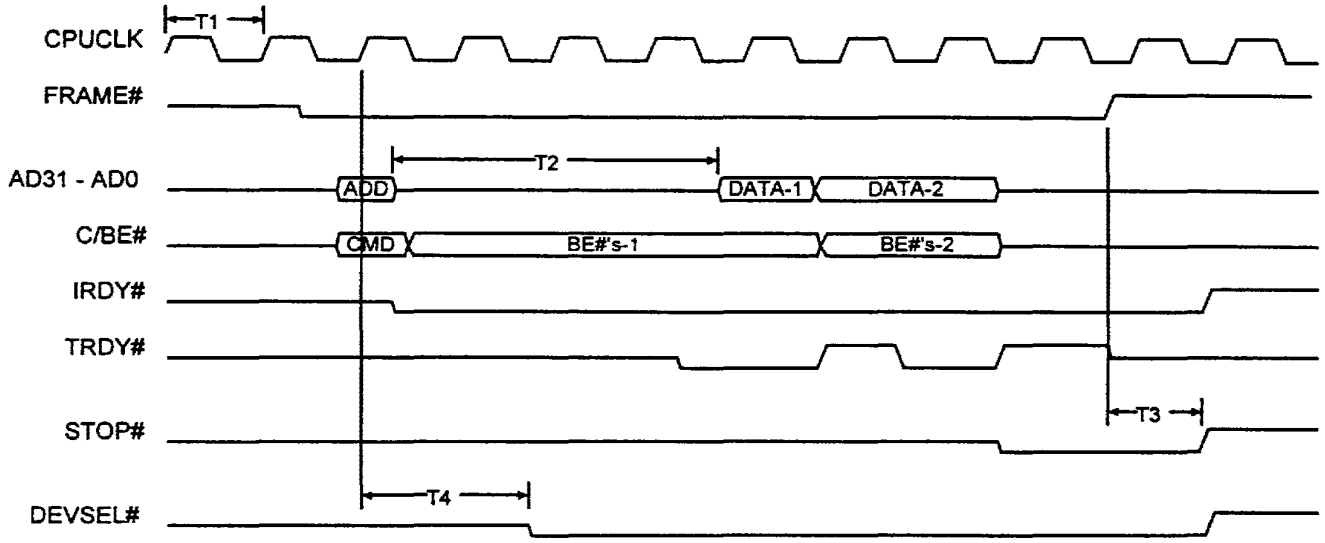


Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	FRAME# setup to CPUCLK	7	
T3	Address/Data setup to CPUCLK	7	
T4	Address/Data hold from CPUCLK	0	
T5	Address Phase to 1st Data Phase		4T
T6	Bus Command setup to CPUCLK	7	
T7	Bus Command hold from CPUCLK	0	
T8	IRDY# hold from CPUCLK	0	
T9	TRDY# delay from CPUCLK	2	
T10	Address Phase to DEVSEL#		2T
T11	DEVSEL# delay from CPUCLK	2	

9004196 0000884 607

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-7 Burst Write Operation with STOP# (PCI)

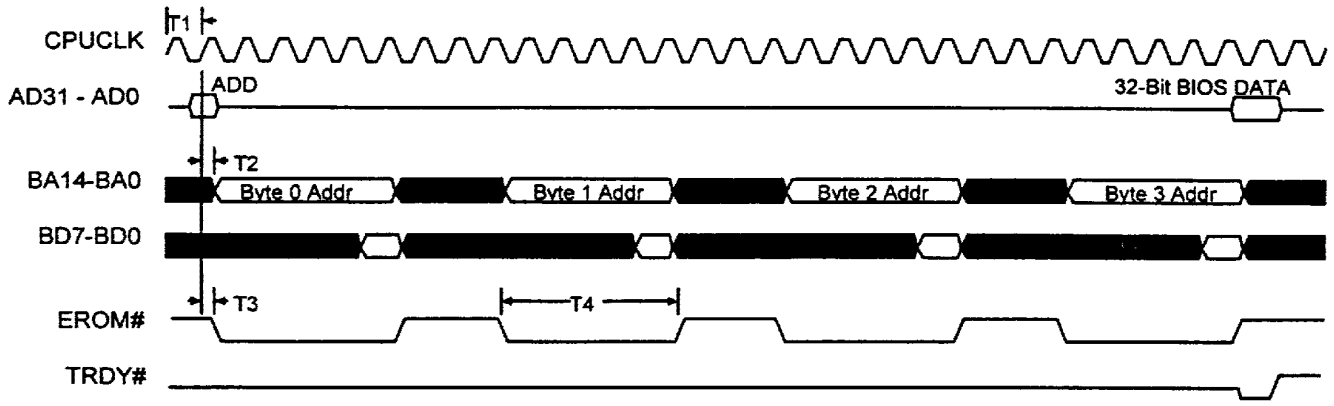


Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	Address Phase to 1st Data Phase		4T
T3	FRAME# inactive to STOP# inactive		1T

9004196 0000885 543

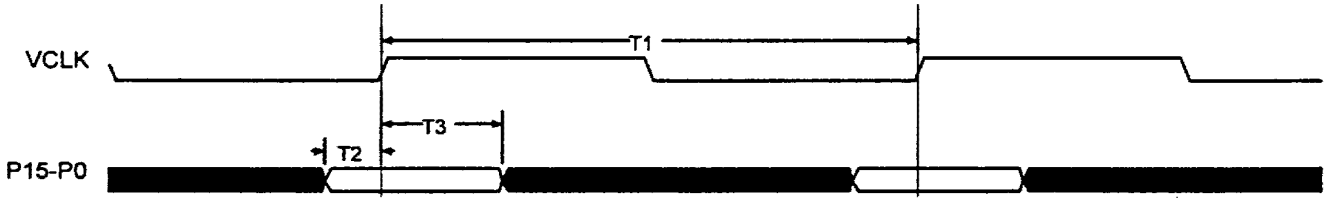
Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-8 BIOS Access Operation (PCI)



Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	Byte Address delay from CPUCLK		6T
T3	EROM# delay from CPUCLK		6T
T4	EROM# active	160	

Figure 6-9 Pixel Data In Timing

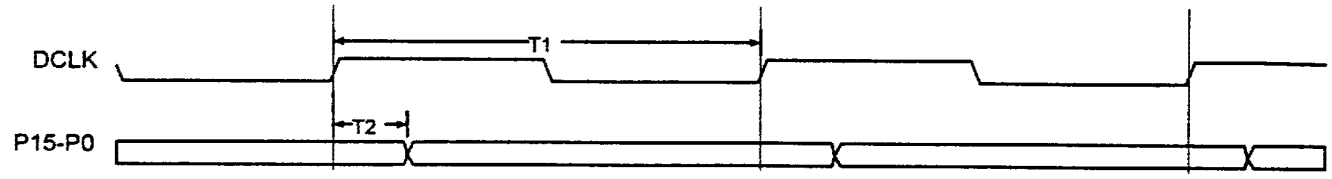


Symbol	Description	Min (ns)	Max (ns)
T1	VCLK Period	26.6	
T2	Pixel Data setup to VCLK	8	
T3	Pixel Data hold from VCLK	1.2	

9004196 0000886 48T

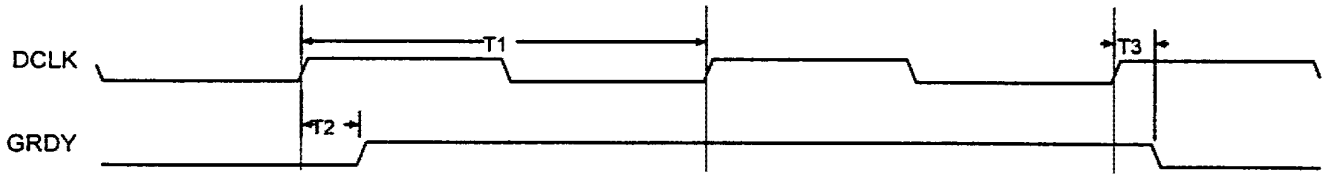
Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-10 Pixel Data Out Timing



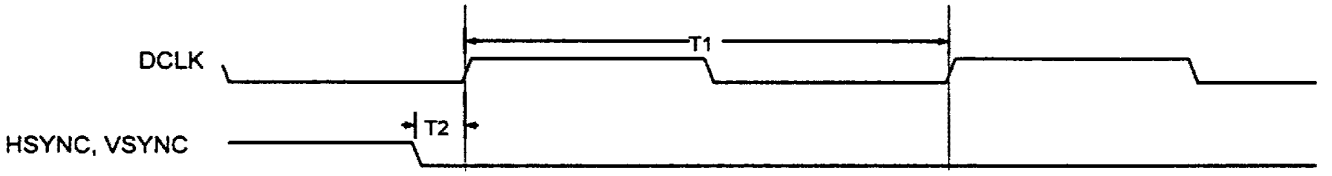
Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	Pixel data delay from DCLK	5	

Figure 6-11 GRDY Timing



Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	GRDY delay from DCLK	5	
T3	GRDY inactive from DCLK	5	

Figure 6-12 Genlock Timing

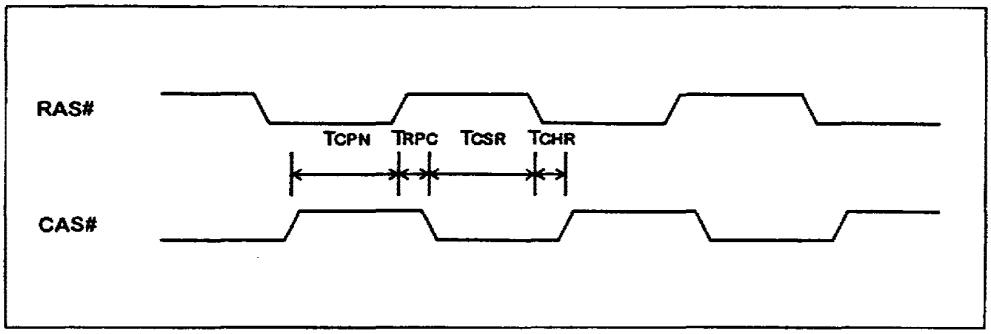


Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	Sync setup to DCLK	5	

9004196 0000887 316

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-13 CAS Before RAS DRAM Timing

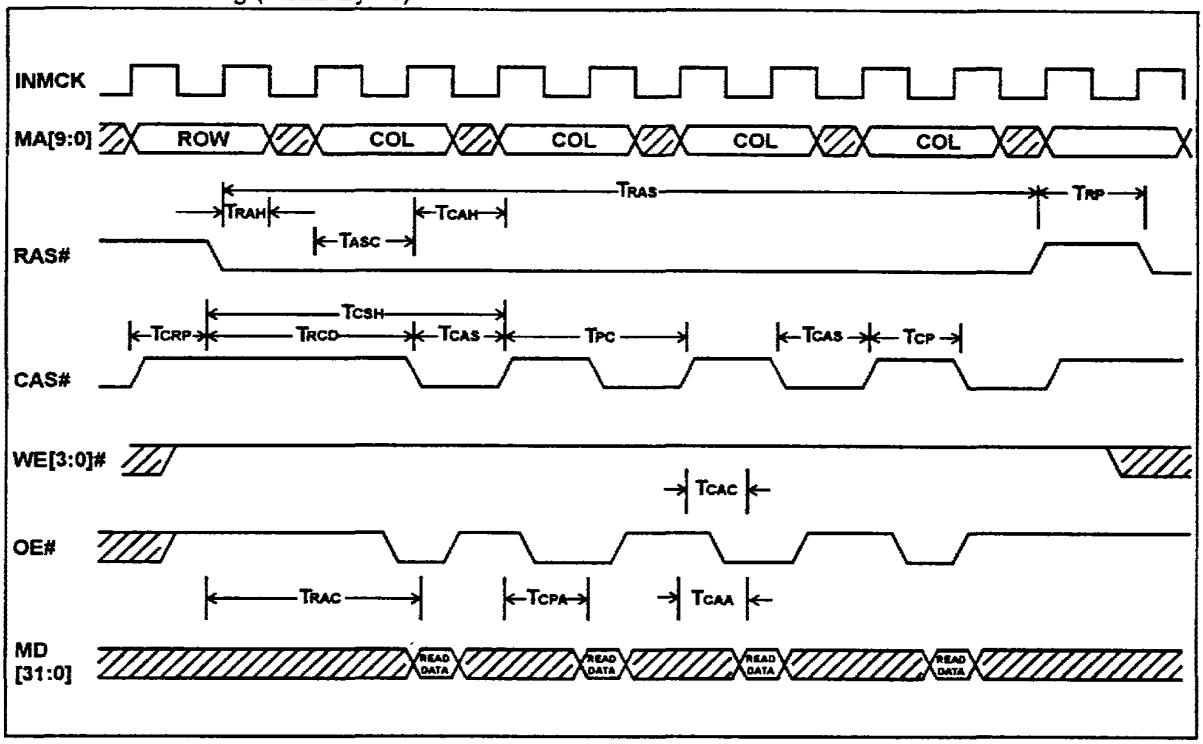


Symbol	Description	Min (ns)
INMCK	1/T	
TCPN	CAS# Precharge Time	T + 3.5
TRPC	RAS# High to CAS High Precharge	T + 4
TCSR	CAS# before RAS Setup Time	2T - 1.5
TCHR	CAS# before RAS Hold Time	3T + 6

9004196 0000888 252

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-14 DRAM Timing (Read Cycle)



NOTE Display Memory Fast Page Mode Parameters

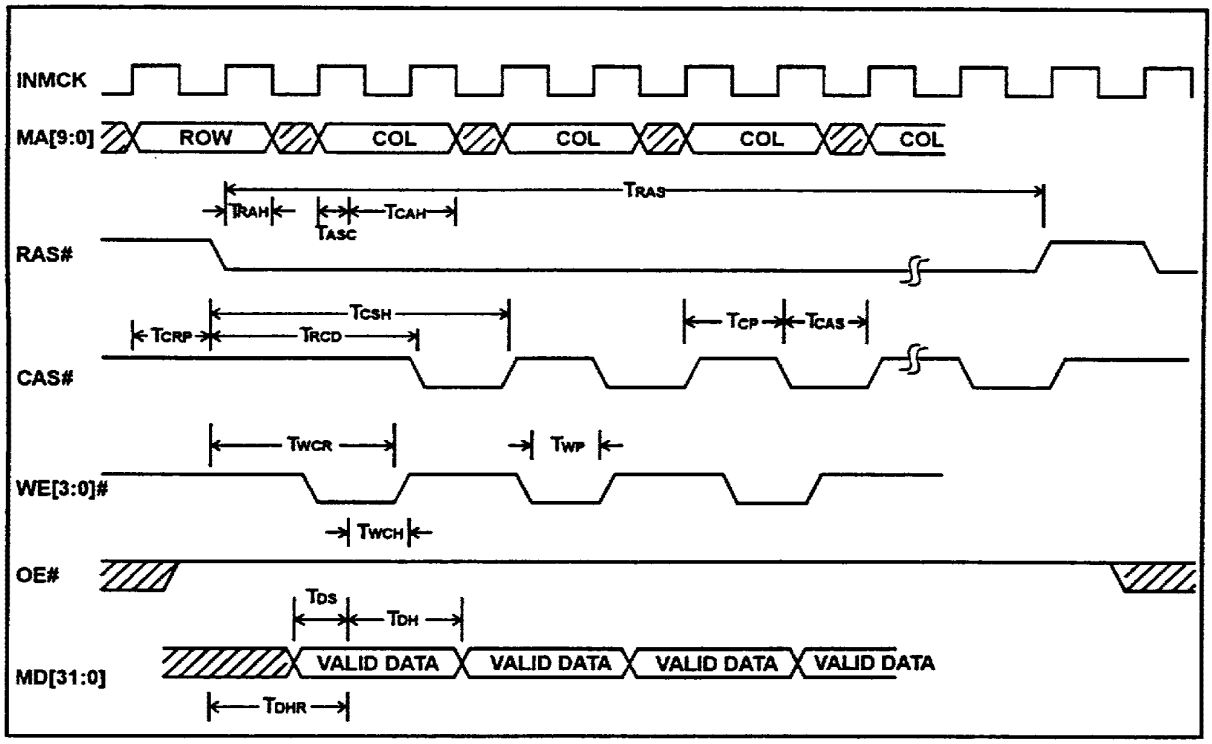
Symbol	Description	Min (ns)	Max (ns)
TRAH	Row Address Hold Time	T-4.5	
TASC	Column Address Setup	T-1	
TCAH	Column Address Hold Time	T-1	
TRAS	RAS# Pulse Width	5T-8	
TRP	RAS# Precharge Time	4T+1	
TCRP	CAS# to RAS# Precharge Time	4T+1	
TRCD	RAS# to CAS# Delay Time	2T-1.5	
TCSH	CAS# Hold Time	3T+2	
TCAS	CAS# Pulse Width	T+3.5	
TPC	CAS# Cycle Time	2T+3	
TCP	CAS# Precharge Time	T-4.5	
TRAC	Data Access Time from RAS#		3.5T
TCAC	Data Access Time from CAS#		T
TCPA	Data Access Time from CAS# Precharge		2T
TCAA	Data Access Time from Column Address		2T

NOTE INMCK = 1/T MHz.

9004196 0000889 199

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure 6-15 DRAM Timing (Write Cycle)



Symbol	Description	Min (ns)	Max (ns)
TRAH	Row Address Hold Time	T-4.5	
TASC	Column Address Setup	T-1	
TCAH	Column Address Hold Time	T-1	
TRAS	RAS# Pulse Width	3T+1.9	
TCRP	CAS# to RAS# Precharge Time	3T+2	
TCSH	CAS# Hold Time from RAS#	3T+2	
TRCD	RAS# to CAS# Delay Time	2T-1.5	
TCP	CAS# Precharge Time	T-4.5	
TCAS	CAS# Pulse Width	T+3.5	
TWP	Write Pulse Width	2T+1	
TWCH	Write Pulse Hold Time from CAS#	T+7.5	
TDS	Data Setup Time to CAS#	T+3.5	
TDH	Data Hold Time to CAS#	T-1	
TDHR	Data Hold Time to RAS#	T-1	
TWCR	Write Pulse Hold Time from RAS#	5T+5	

NOTE INMCK = 1/T MHz.

9004196 0000890 900

Powered by ICminer.com Electronic-Library Service CopyRight 2003

7.0 Video BIOS Extended Modes

7.1 Standard VGA Modes

Mode	Resolution (pixels)	Colors	Col x Row	Char Size	Type	Segment
0+h, 1+h	360x400	16	40x25	9x16	Text	B800h
2+h, 3+h	720x400	16	80x25	9x16	Text	B800h
4h, 5h	320x200	4	40x25	8x8	Graphics	A000h
6h	640x200	2	80x25	8x8	Graphics	A000h
7+h	720x400	Mono	80x25	9x16	Text	B800h
Dh	320x200	16	40x25	8x8	Graphics	A000h
Eh	640x200	16	80x25	8x8	Graphics	A000h
Fh	640x350	Mono	80x25	8x14	Graphics	A000h
10h	640x350	16	80x25	8x14	Graphics	A000h
11h	640x480	2	80x30	8x16	Graphics	A000h
12h	640x480	16	80x30	8x16	Graphics	A000h
13h	320x200	256	40x25	8x8	Graphics	A000h
0+h, 1+h	360x400	16	40x25	9x16	Text	B800h
2+h, 3+h	720x400	16	80x25	9x16	Text	B800h
4h, 5h	320x200	4	40x25	8x8	Graphics	A000h
6h	640x200	2	80x25	8x8	Graphics	A000h
7+h	720x400	Mono	80x25	9x16	Text	B800h
Dh	320x200	16	40x25	8x8	Graphics	A000h
Eh	640x200	16	80x25	8x8	Graphics	A000h
Fh	640x350	Mono	80x25	8x14	Graphics	A000h
10h	640x350	16	80x25	8x14	Graphics	A000h
11h	640x480	2	80x30	8x16	Graphics	A000h

9004196 0000891 847

Powered by ICminer.com Electronic-Library Service CopyRight 2003

7.2 Extended VGA Modes

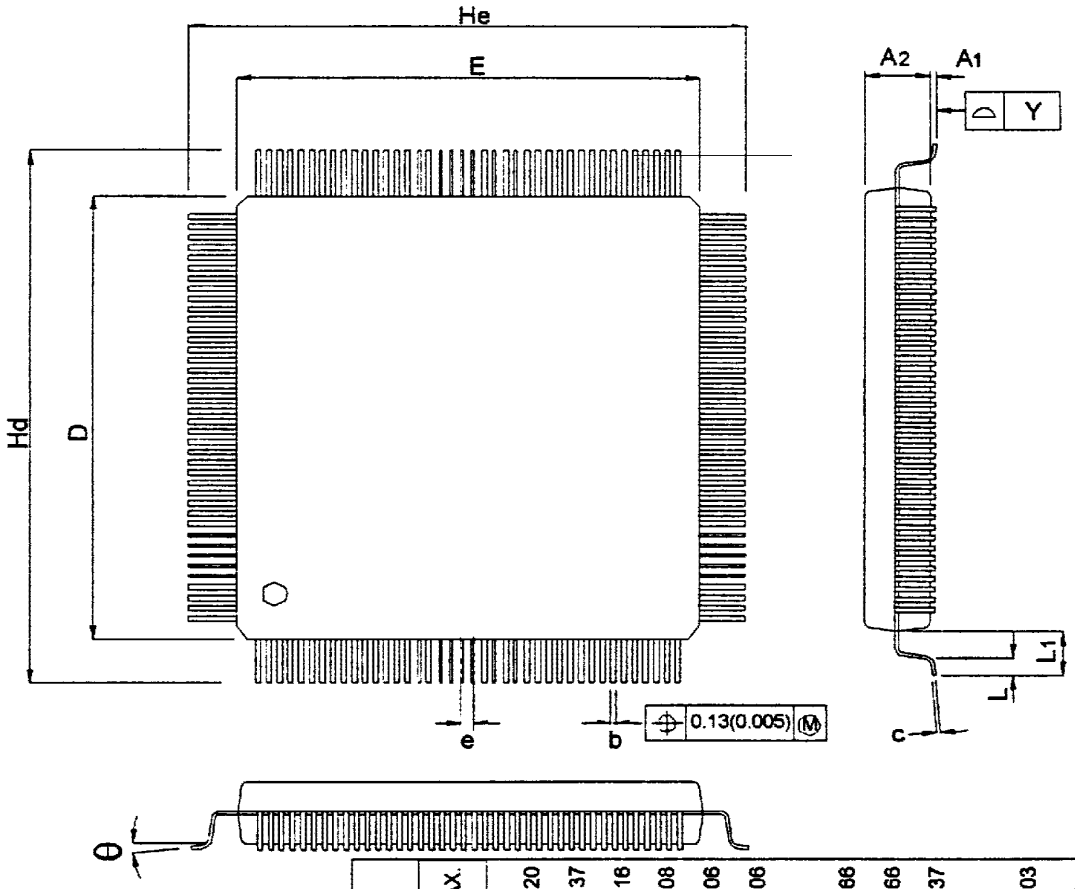
Mode	VESA Mode	Resolution	Colors	Col x Row	Char Size	Type	Segment
20h	--	720x476	16	80x34	8x14	Text	B800h
21h	--	640x350	16	80x43	8x8	Text	B800h
22h	108h	640x480	16	80x60	8x8	Text	B800h
23h	109h	1056x400	16	132x25	8x16	Text	B800h
24h	10Ah	1056x350	16	132x43	8x8	Text	B800h
25h	10Bh	1056x400	16	132x50	8x8	Text	B800h
26h	10Ch	1056x480	16	132x60	8x8	Text	B800h
30h	102h	800x600	16	100x75	8x8	Graphics	A000h
31h	104h	1024x768	16	128x48	8x16	Graphics	A000h
32h	106h	1280x1024	16			Graphics	A000h
33h		1600x1200	16			Graphics	A000h
38h	100h	640x400	256	80x25	8x16	Graphics	A000h
39h	101h	640x480	256	80x30	8x16	Graphics	A000h
3Ah	103h	800x600	256	100x75	8x8	Graphics	A000h
3Bh	105h	1024x768	256	128x48	8x16	Graphics	A000h
3Ch	107h	1280x1024	256			Graphics	A000h
3Dh		1600x1200	256			Graphics	A000h
40h		640x400	32K			Graphics	A000h
41h	110h	640x480	32K			Graphics	A000h
42h	113h	800x600	32K			Graphics	A000h
43h	116h	1024x768	32K			Graphics	A000h
48h		640x400	64K			Graphics	A000h
49h	111h	640x480	64K			Graphics	A000h
4Ah	114h	800x600	64K			Graphics	A000h
4Bh	117h	1024x768	64K			Graphics	A000h
50h		640x400	16M			Graphics	A000h
51h	112h	640x480	16M			Graphics	A000h
52h	115h	800x600	16M			Graphics	A000h

9004196 0000892 783

Powered by ICminer.com Electronic-Library Service CopyRight 2003

8.0 Mechanical Package

Figure 8-1 160-Pin Plastic Quad Flat Pack (PQFP)



SYMBOL	MILLIMETER MIN.	MILLIMETER NOM.	MILLIMETER MAX.	INCH MIN.	INCH NOM.	INCH MAX.
A_1	0.05	0.25	0.50	0.002	0.010	0.020
A_2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
Hd	31.65	31.90	32.15	1.246	1.256	1.266
He	31.65	31.90	32.15	1.246	1.256	1.266
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1		1.95			0.077	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.: AS160PQFP-001
Dwg. Rev.: A0 Unit: MM / INCH

9004196 0000893 61T

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Appendix A. Accessing the BBS

The OPTi BBS offers a wide range of useful files and utilities to our customers, from Evaluation PCB Schematics to HPGL/ PostScript format Databooks that you can copy directly to your laser printer. The only requirements for accessing and using the BBS is a modem and an honest response to our questionnaire.

A.1 Paging the SYSOP

Currently, Paging the SYSOP is not a valid choice for the OPTi BBS. Once a full-time SYSOP is created, then there will be hours available for paging the SYSOP and getting immediate help.

For now, you must send [C] Comments to the SYSOP with any questions or problems you are experiencing. They will be answered promptly.

NOTE Each conference has its own Co-SYSOP (the application engineer responsible for that product line), so specific conference questions can be addressed that way, but general, BBS-wide, questions should be sent to the SYSOP from the [0] - Private E-Mail conference.

A.2 System Requirements

The OPTi BBS will support any PC modem up to 14,400 baud, with 8 bits, no parity, and 1 stop bit protocol. The baud rate, handshaking, and system type will automatically be detected by the OPTi BBS.

A.3 Calling In/Hours of Operation

The OPTi BBS phone number is (408) 980-9774. The BBS is on-line 24 hours a day, seven days a week. Currently there is only one line, but as traffic requires additional lines will be installed.

A.4 Logging On for the First Time

To log on to the BBS for the first time,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Select a password (write it down).
6. Reenter the password to verify spelling.
7. You must then answer the questionnaire that follows.

After you have answered the questionnaire, you are given Customer rights. To change your profile (security level, password, etc.), you must send a [C]omment to the SYSOP explaining why.

After you have logged on for the first time, each subsequent log on will bypass the questionnaire and put you directly at the bulletin request prompt. As bulletins will be added on a regular basis in the future, it is recommended that you read the new bulletins on a regular basis.

A.5 Log On Rules and Regulations

- As a FULLUSER you can download from any conference.
- You will be limited to 45 minutes per day of access time (note that once a download has started, it will finish, even if the daily time limit is exceeded). If you have not entered any keystrokes after 5 minutes, you will automatically be logged off.
- You can upload to the Customer Upload Conference[1] only. This area is used for our customers/contacts to send data to OPTi. You will not be able to download any files from this area.

A.6 Using the BBS

This section will describe how to use the BBS on a daily basis.

The BBS is divided into Conferences that are specific to a product (for example, the Viper Desktop Chipset), or an application group (for example, the Field Application Conference is used by OPTi Field Application Engineers to send data to their contacts in the field). As a general rule, the files in the application specific areas will be for specific application and may contain a password. If a file is password protected, and you know you need that file, you must contact your OPTi sales representative for the password.

The files in the Product Conferences are released data that can be used for evaluating the OPTi product line.

To access a feature of the BBS, you should type the letter in brackets that precedes each menu item. This document places the appropriate letter in brackets whenever you are told to access a feature.

1. See Section A.6.5 for more information on uploading.

9004196 0000894 556

Powered by ICminer.com Electronic-Library Service CopyRight 2003

A.6.1 Reading Bulletins

The OPTi BBS will present you with a set of bulletins each time you log on that are global bulletins applying to OPTi in general. In addition to these, each Product Conference will have its own set of bulletins that apply to that product. These bulletins will announce new product information, documentation updates, and bug fixes and product alerts.

It is recommended that you read any new bulletins on a regular basis to keep up to date on the OPTi product line.

A.6.2 Sending/Receiving Messages

The Message Menu can be used to send and receive messages from OPTi employees, or other BBS users. The Message menu can also be used to attach files for the receiver to download after they read the message. This method will be used often to send customer specific files to OPTi customers.

Messages to the SYSOP depend upon the conference you are in. Each Product Conference sends Comments and Messages to the SYSOP to the Application Engineer responsible for that conference.

A.6.3 Finding Information

To find information on the OPTi BBS, you must use the [J] Join a Conference option and then list all of the conferences available. They are arranged by product number and name.

Once you are in the correct conference, you should read all applicable bulletins and messages. Then you can [L] List all the files that are available from the File Menu.

A.6.4 Downloading Files From OPTi

The easiest way to download files from OPTi, is to [L] List the files from the File Menu, the [M] Mark and files you want from the list. After you have marked all the files you need, you can [D] Download all the marked files and then logoff automatically.

A.6.5 Uploading Files To OPTi

There are two ways to upload a file to OPTi. The first is similar to the download option. You should [J] Join the Customer Upload Conference (this is the only conference that allows uploads from users) and [U] Upload the file to this conference.

If you are sending the file to a specific person, you should use the Message Menu to [E] Enter a new message to that person and then [A] Attach the file to the message. This way, the person receiving the message can download the file to his or her system without leaving behind a file that will not be used by anyone else on the BBS.

A.6.6 Logging Off

Once you have completed your visit to the OPTi BBS, you must say [G] Goodbye.

A.6.7 Logging Back on Again

To log back on to the BBS,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Enter your password.

You will not have to answer the questionnaire after the initial log-on. You will also be in the conference you were in when you last logged-on.

A.7 The Menus

There are four major menus that OPTi customers will use, the Main Menu, the File Menu, the Bulletin Menu and the Message Menu.

NOTE The following menus are for the Customer Profile (FULLUSER) only, if your user profile has been changed, you may see slightly different menus.

Figure A-1 The Main Menu

```
MAIN MENU:
[ J ] Join a conference              [ F ] File menu
[ M ] Message menu                   [ B ] Bulletin menu
[ C ] Comments to the sysop          [ U ] Userlog list
[ Y ] Your settings                  [ G ] Goodbye & logoff

Conf: "[0] - Private E-Mail", time on 0, with 45 remaining.
MAIN MENU: [J F M B C P U Y G] ?
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

Figure A-2 The Bulletin Menu

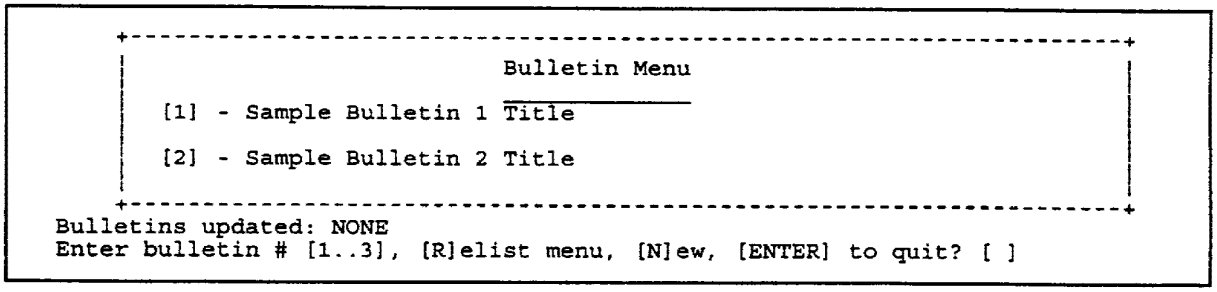


Figure A-3 The File Menu

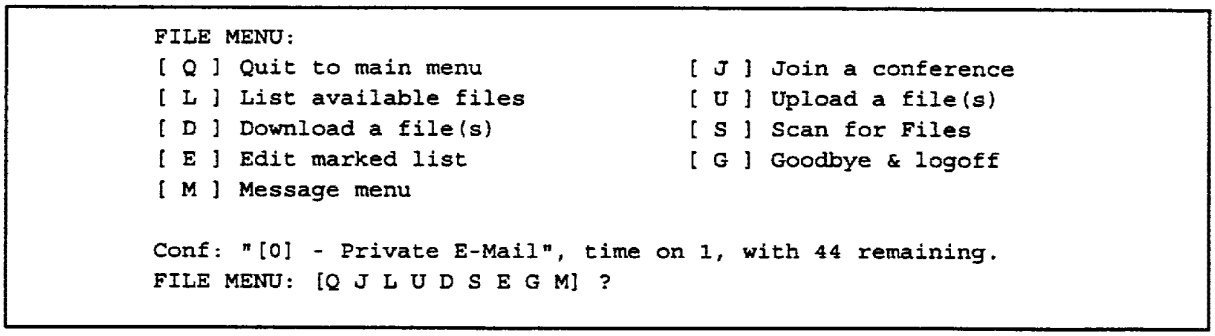
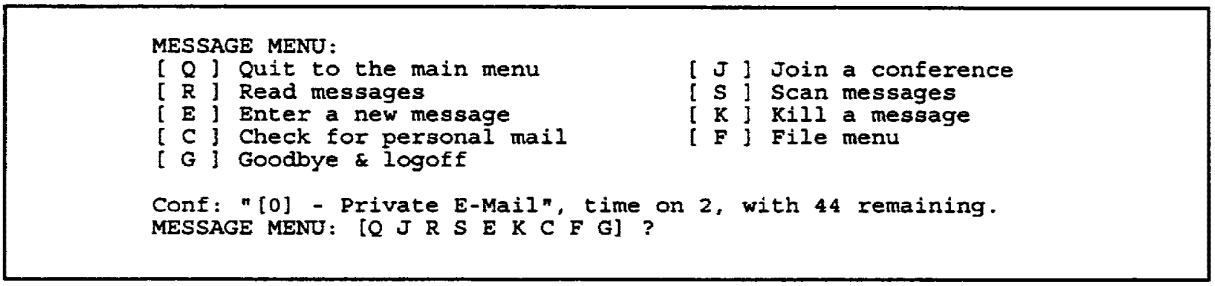


Figure A-4 The Message Menu



A.7.1 Menu Selections

- [B] Bulletin MenuMenu(s): main
  Access the Bulletin Menu.
- [C] Check for personal mailMenu(s): message
  See if you have any mail.
- [C] Comments to the sysopMenu(s): main
  Leave a private comment for the SYSOP.
- [D] Download a file(s)Menu(s): file
  Download a file from the BBS to your computer. If you have marked files it will display these files. If you have not marked any files, it will ask you for a file name. The file must be present in the current conference for you to be able to enter its name.
- [E] Edit Marked ListMenu(s): file
  Change the entries that you have selected as Marked for downloading.
- [E] Enter a new messageMenu(s): message
  Send a new message to someone on the BBS.
- [F] File MenuMenu(s): main, message
  Access the File Menu.
- [G] Goodbye and logoffMenu(s): main, message, file
  Logoff the system.
- [J] Join a ConferenceMenu(s): main, message, file
  Change conferences (product areas).
- [K] Kill a messageMenu(s): message

9004196 0000896 329

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Delete a message.

- [L] List available filesMenu(s): file
  List the files in the current conference. Note that most conferences have sub-categories of files (Schematics, JOB, etc.) that you will be asked for (or you can press enter the list all of the categories).
- [M] Message MenuMenu(s): main, file
  Access the Message Menu.
- [Q] Quit to Main MenuMenu(s): message, file
  Leave current menu and return to the Main Menu.
- [R] Read MessagesMenu(s): message
  Read messages in the current conference or all conferences.
- [S] Scan for FilesMenu(s): file
  Scan for particular files (by name, or extension, etc.).
- [S] Scan messagesMenu(s): message
  Search for message by specific qualifier (date, sender etc.).
- [U] Upload a file(s)Menu(s): file
  Send a file from your computer to OPTi. This can only be done in the Customer Upload Conference.
- [U] Userlog ListMenu(s): main
  Lists the user database, in order of logon. This is useful if you are sending a message and are looking for the spelling of a persons name.
- [Y] Your settingsMenu(s): main
  Show you settings and allow you to make changes. These include password, name, address, etc.

9004196 0000897 265

Powered by ICminer.com Electronic-Library Service CopyRight 2003