

82C465MVB
32-Bit 486/586
Mobile Chipset
with PCMCIA

82C465MVB
System Controller

82C852
100-Pin PCMCIA
Controller

82C602A
Data Buffer

The OPTi 82C465MVB chipset is a highly integrated device that supports 32-bit 486 and 586 architectures. It implements ISA-compatible core logic, along with power management and CPU thermal management hardware, in a single device. Its feature set provides an array of control and status monitoring options, all accessed through a simple and straightforward interface. All major BIOS vendors provide power management modules that are optimized for the OPTi power management unit and provide extensive software "hooks" that allow system designers to integrate their own special features with minimal effort.

The 82C465MVB requires very little board space, implemented as a single 208-pin PQFP package in 0.8 micron CMOS technology. When used with the 82C602A RTC/Buffer companion chip, the chipset provides necessary interfaces with a minimal amount of support logic.

CPU/VL-Bus

- Supports Cyrix 586-type 32-bit CPUs (M1sc)
- Supports AMD, Cyrix, Intel, and IBM 32-bit 486-type CPUs, in 3.3V or 5V, including clock-tripled technology
- Provides a fail-safe thermal management scheme (cool-down clocking)
- Provides fast emulation of keyboard controller CPU reset and gate A20 control; supports port 092h as well
- Fully supports local bus implementations, including VL-bus masters
- Offers complete Microsoft APM operability, with CPU stop-clock support
- Internal resistors eliminate external pull up/pull down resistors on CPU address, data, and control lines
- Supports hybrid CPU interfaces; supports all 32-bit data interfaces
- Provides SMBASE relocation
- Up to 50MHz bus speeds
- ATHOLD function is included for ISA docking station support



INNOVATIVE
CHIPSET
SOLUTIONS



DRAM/Cache Controller

- Supports fast page mode and EDO DRAM
- Provides L1 cache support for CPUs with an integrated write-back and write-through cache
- Provides power-managed L2 cache support with a high-performance, write-back external cache
- Supports combined tag/dirty RAM
- Supports five banks of DRAM; bank skipping for automatic BIOS-based disabling of defective DRAM
- Uses simplified memory programming scheme; symmetrical and asymmetrical types can be mixed
- Allows any bank to use 256KB, 512KB, 1MB, 2MB, 4MB, 8MB, or 16MB DRAM devices
- Supports 3-2-2-2, 4-3-3-3, and 5-4-4-4 burst read memory cycles, 0- or 1-wait state DRAM write cycles
- Supports two programmable non-cacheable regions
- Offers fully programmable shadowing of ROM using DRAM in the C0000-FFFFFh region
- Allows normal or slow refresh, CAS-before-RAS refresh, and self-refresh DRAM support

ISA Bus

- Supports Type F DMA
- Implements Compact ISA (CISA) specification, which supports Windows 95 features of programmable IRQ and DMA channels
- The internal 82C206 IPC offers a true single-chip notebook implementation
- Implements a complete AT-compatible system with only one extra device, the 82C602A, which contains:
 - RTC with 256 bytes of non-volatile RAM, and
 - the equivalent of seven discrete TTL devices
- Integrates an enhanced IDE interface running at local-bus speeds
- IDE support uses one external TTL device to control the IDE, with a second optional device for complete power-down isolation of the IDE drive
- Prevents ISA-bus device incompatibility with IDE command scheme that shares no ISA-bus command lines
- Supports four IDE drives
- Four programmable chip selects

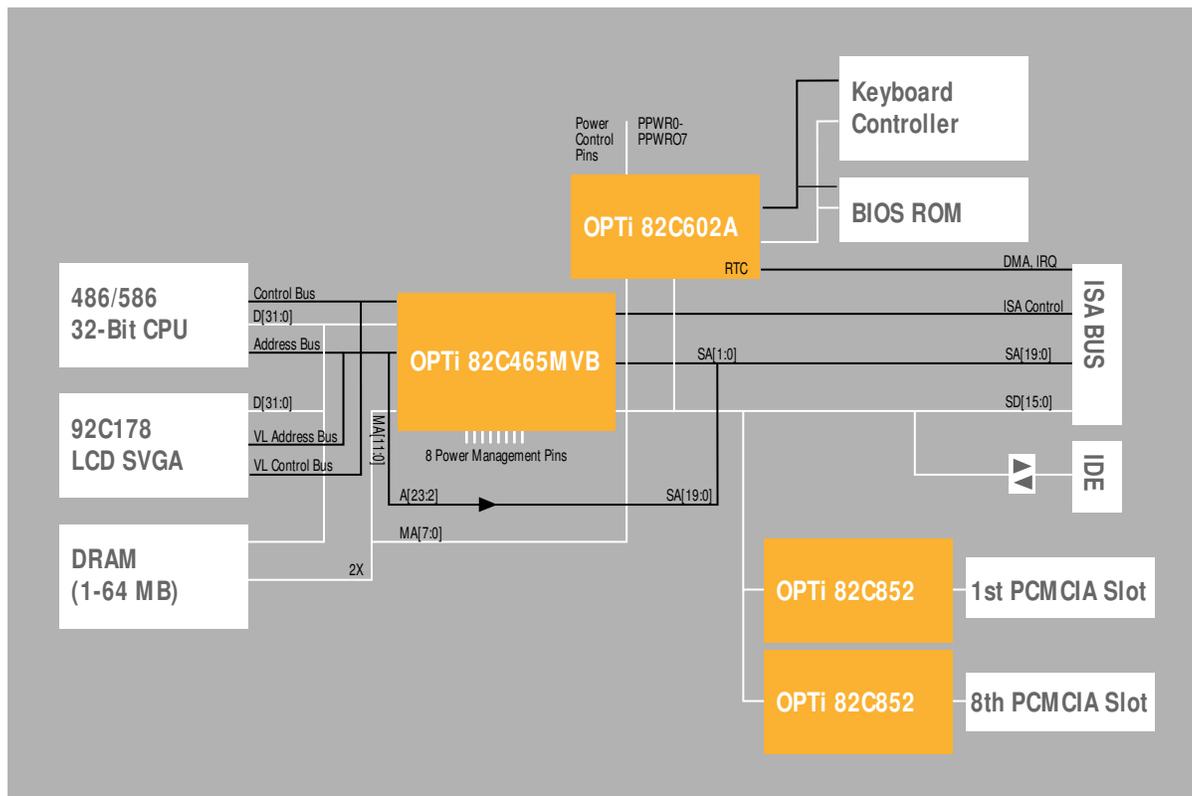
Power Management

- Recognizes 28 separate PMI events
 - 11 of the PMI events have individual timers to indicate inactivity timeout situations.
- Eight external inputs are available for monitoring asynchronous system events
- Allows polling for I/O activity via activity tracking register of eight events for SMI and non-SMI applications
- Memory watchdog monitoring allows accesses to memory ranges to cause an SMI
- Supports system-level low-power suspend, low-power suspend with zero-volt CPU suspend, or total system zero-volt suspend
- 12 peripheral power control pins plus four user-definable I/O pins provide exceptional flexibility in peripheral device control
- RTC alarm or modem ring can wake up the system from low-power suspend mode
- Local bus device can reset doze mode
- Dual doze timers
- DMA state can be fully saved and restored when suspending
- Suspend current leakage control ensures that negligible power will be consumed in suspend mode without additional external buffering

82C852 Features

- Compliant with 16-bit PC Card 95 specification
- Based on Intel 82365SL core
- Can be programmed to use any DMA channel and any interrupt channel to support Windows 95
- 100-pin 16mm by 16mm TQFP significantly reduces board space requirements
- Use up to eight 82C852 chips to support multiple independent PCMCIA slots
- Supports 3.3V PCMCIA cards
- For card reader applications, requires single IDE-type cable for any number of slots
- Automatically enters power-down mode during CPU APM stop clock mode
- Core operates at 5V or 3.3V, independent of PCMCIA card
- No external logic required to combine SPKROUT pins

System Block Diagram



About OPTi

Founded in 1989, OPTi is a leading supplier of core logic and multimedia chipsets to manufacturers of desktop and mobile computer products worldwide. OPTi's innovative chipset solutions enable our customers to get to market quickly with quality, state of the art products. In 1994, we shipped

more than nine million chipsets to leading personal computer and board manufacturers worldwide.

Our headquarters are located in Milpitas, California and our stock is traded on NASDAQ under the symbol OPTi.

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