82C941

Advanced Sound Synthesizer

Data Book

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OPTi Inc.
888 Tasman Drive
Milpitas, CA 95035
Tel: (408) 486-8000
Fax: (408) 486-8001
Web Site: http://www.opti.com/

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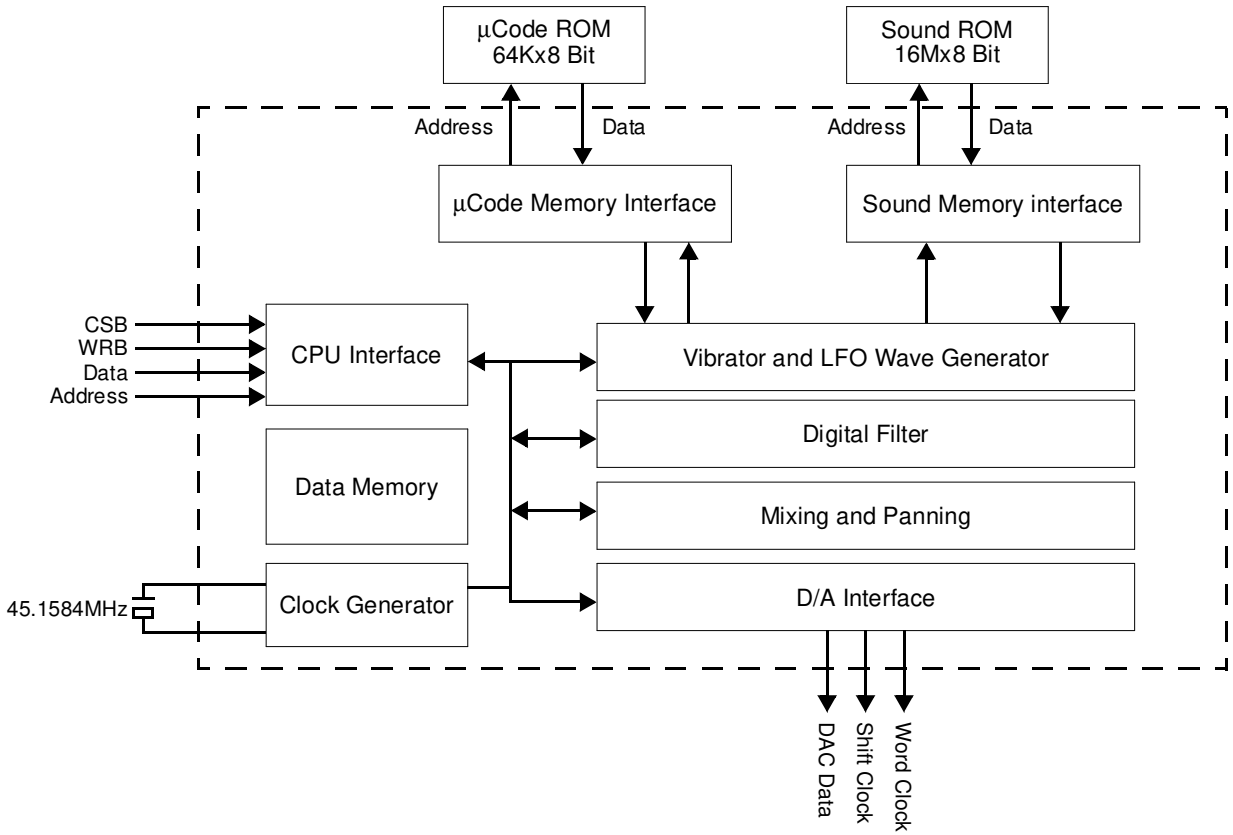
1.0 Overview

The 82C941 Advanced Sound Synthesizer creates high-quality, accurate, realistic musical sound. All the music synthesis algorithms are preset to generate the most realistic acoustic sound, or many of the control parameters can be customized during the creation of the music according to General MIDI specifications. Also, the built-in OPTi proprietary decompression algorithm, along with Advanced Time-variable Filter and Amplitude (ATFA) control technique, provides compressed sound memory without degrading quality. The 82C941 is an ideal device to make musical instruments, Karaoke machines, MIDI modules, and PC sound cards.

2.0 Features

- 32 polyphonic playback at 44.1KHz
- Advance Time-variable Filter and Amplitude (ATFA) control
- Subtractive sound synthesis
- Built-in power management
- Built-in CPU data memory and interface TTL
- Dynamic voice assignment
- Supports up to 16Mx8 sampling memory
- 100 pin CMOS QFP package

Figure 2-1 Functional Block Diagram



3.0 Signal Definitions

Figure 3-1 Pin Diagram

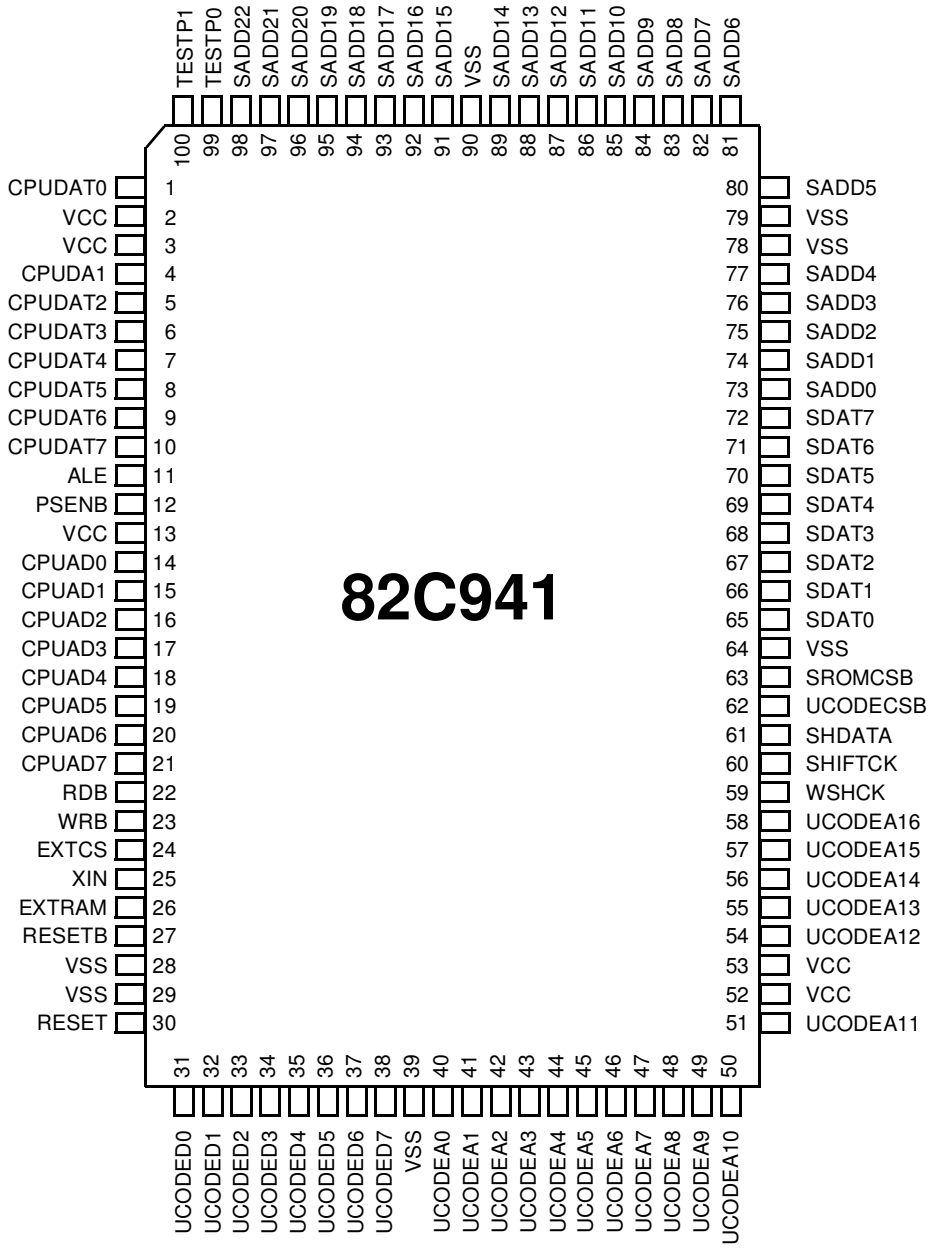


Table 3-1 Numerical Pin Cross-Reference

Pin#	Name	Pin Type	Pin#	Name	Pin Type	Pin#	Name	Pin Type	Pin#	Name	Pin Type
1	CPUDAT0	I/O	26	EXTRAM	I	51	UCODEA11	O	76	SADD3	O
2	VCC		27	RESETB	I	52	VCC		77	SADD4	O
3	VCC		28	VSS		53	VCC		78	VSS	
4	CPUDAT1	I/O	29	VSS		54	UCODEA12	O	79	VSS	
5	CPUDAT2	I/O	30	RESET	O	55	UCODEA13	O	80	SADD5	O
6	CPUDAT3	I/O	31	UCODED0	I	56	UCODEA14	O	81	SADD6	O
7	CPUDAT4	I/O	32	UCODED1	I	57	UCODEA15	O	82	SADD7	O
8	CPUDAT5	I/O	33	UCODED2	I	58	UCODEA16	O	83	SADD8	O
9	CPUDAT6	I/O	34	UCODED3	I	59	WSHCK	O	84	SADD9	O
10	CPUDAT7	I/O	35	UCODED4	I	60	SHIFTCK	O	85	SADD10	O
11	ALE	I	36	UCODED5	I	61	SHDATA	O	86	SADD11	O
12	PSENB	I	37	UCODED6	I	62	UCODECSB	O	87	SADD12	O
13	VCC		38	UCODED7	I	63	SROMCSB	I	88	SADD13	O
14	CPUAD0	O	39	VSS		64	VSS		89	SADD14	O
15	CPUAD1	O	40	UCODEA0	O	65	SDAT0	I	90	VSS	
16	CPUAD2	O	41	UCODEA1	O	66	SDAT1	I	91	SADD15	O
17	CPUAD3	O	42	UCODEA2	O	67	SDAT2	I	92	SADD16	O
18	CPUAD4	O	43	UCODEA3	O	68	SDAT3	I	93	SADD17	O
19	CPUAD5	O	44	UCODEA4	O	69	SDAT4	I	94	SADD18	O
20	CPUAD6	O	45	UCODEA5	O	70	SDAT5	I	95	SADD19	O
21	CPUAD7	O	46	UCODEA6	O	71	SDAT6	I	96	SADD20	O
22	RDB	I	47	UCODEA7	O	72	SDAT7	I	97	SADD21	O
23	WRB	I	48	UCODEA8	O	73	SADD0	O	98	SADD22	O
24	EXTCS	I	49	UCODEA9	O	74	SADD1	O	99	TESTP0	I
25	XIN	I	50	UCODEA10	O	75	SADD2	O	100	TESTP1	I

Table 3-2 Alphabetical Pin Cross-Reference

Name	Pin#	Pin Type	Name	Pin#	Pin Type	Name	Pin#	Pin Type	Name	Pin#	Pin Type
ALE	11	I	SADD2	75	O	SDAT4	69	I	UCODEA16	58	O
CPUDAT0	1	I/O	SADD3	76	O	SDAT5	70	I	UCODECSB	62	O
CPUDAT1	4	I/O	SADD4	77	O	SDAT6	71	I	UCODED0	31	I
CPUDAT2	5	I/O	SADD5	80	O	SDAT7	72	I	UCODED1	32	I
CPUDAT3	6	I/O	SADD6	81	O	SHDATA	61	O	UCODED2	33	I
CPUDAT4	7	I/O	SADD7	82	O	SHIFTCK	60	O	UCODED3	34	I
CPUDAT5	8	I/O	SADD8	83	O	SROMCSB	63	I	UCODED4	35	I
CPUDAT6	9	I/O	SADD9	84	O	TESTP0	99	I	UCODED5	36	I
CPUDAT7	10	I/O	SADD10	85	O	TESTP1	100	I	UCODED6	37	I
CPUAD0	14	O	SADD11	86	O	UCODEA0	40	O	UCODED7	38	I
CPUAD1	15	O	SADD12	87	O	UCODEA1	41	O	VCC	2	
CPUAD2	16	O	SADD13	88	O	UCODEA2	42	O	VCC	3	
CPUAD3	17	O	SADD14	89	O	UCODEA3	43	O	VCC	13	
CPUAD4	18	O	SADD15	91	O	UCODEA4	44	O	VCC	52	
CPUAD5	19	O	SADD16	92	O	UCODEA5	45	O	VCC	53	
CPUAD6	20	O	SADD17	93	O	UCODEA6	46	O	VSS	28	
CPUAD7	21	O	SADD18	94	O	UCODEA7	47	O	VSS	29	
EXTCS	24	I	SADD19	95	O	UCODEA8	48	O	VSS	39	
EXTRAM	26	I	SADD20	96	O	UCODEA9	49	O	VSS	64	
PSENB	12	I	SADD21	97	O	UCODEA10	50	O	VSS	78	
RDB	22	I	SADD22	98	O	UCODEA11	51	O	VSS	79	
RESET	30	O	SDAT0	65	I	UCODEA12	54	O	VSS	90	
RESETB	27	I	SDAT1	66	I	UCODEA13	55	O	WRB	23	I
SADD0	73	O	SDAT2	67	I	UCODEA14	56	O	WSHCK	59	O
SADD1	74	O	SDAT3	68	I	UCODEA15	57	O	XIN	25	I

3.1 Signal Descriptions

Pin No	Signal Name	Signal Type	Signal Description
1, 4-10	CPUDAT0-CPUDAT7	I/O	CPU Data Bus. CPUDAT7 (MSB) through CPUDAT0 (LSB).
11	ALE	I	CPU Address Latch Enable signal for latching the low byte of the address.
12	PSENB	I	CPU Program Store Enable is the read strobe to external program.
21-14	CPUAD7-CPUAD0	O	CPU Address lower byte address.
22	RDB	I	Internal CPU Data RAM Read enable signal.
23	WRB	I	Internal CPU Data RAM and DSP Register Write enable signal.
24	EXTCS	I	External DSP Chip Select active high enable signal.
25	XIN	I	45.1584 MHz master clock input.
26	EXTRAM	I	Internal CPU Data RAM disable signal.
27	RESETB	I	DSP Master Reset active low input signal.
30	RESET	O	DSP Master Reset signal output.
31-38	UCODED0-UCODED7	I	µcode memory data bus. UCODED7 (MSB) through UCODED0 (LSB).
40-51, 54-58	UCODEA0-UCODEA16	O	µcode memory address bus. UCODEA16 (MSB) through UCODEA0 (LSB).
59	WSHCK	O	DAC Word Clock signal.
60	SHIFTCK	O	DAC Data Shift Clock signal.
61	SHDATA	O	DAC Serial Data signal.
62	UCODECSB	O	µcode Memory Chip Select active low enable signal.
63	SROMCSB	I	Sound Memory Chip Select active low signal.
65-72	SDAT0-SDAT7	I	Sound Memory Data Bus. SDAT7 (MSB) through SDAT0 (LSB).
73-77, 80-88, 90-98	SADD0-SADD22	O	Sound Memory Address Bus. SADD22 (MSB) through SADD0 (LSB).
99-100	TESTP0-TESTP1	I	Chip Test Mode select pins. For normal chip operation test pins must be connected to ground.
2-3, 13, 52-53	VCC		5V supply pins.
28-29, 39, 64, 78-79, 90	VSS		Ground pins.

4.0 Functional Overview

The 82C941 is a specialized digital signal processor (QDSP) designed to generate high quality and realistic sound. The 82C941 musical synthesizer contains all the necessary modules to create acoustic sound; and each module of parameters can be modified for each individual voice during the creation of sound. To make the best and simple MIDI interpreter interface, the 82C941 has an advanced parameter self-extracting module. The υcode memory and CPU interface module allows true playback of the 32 polyphonic voices of music at 44.1KHz without any frequency degradation or loss of quality of sound. The OPTi Advanced Time-variable Filter and Amplitude (ATFA), along with the subtractive sound generation synthesis method, are highly balanced to create accurate acoustic sound between each functional module. All the functional module parameters are automatically extracted and modified without CPU command access during each voice of music generation. The low frequency oscillator with vibrator module creates a deeper sensation of timbre which makes a better effect of sound. The high performance of the internal multi-stage filter with 32 different cut-off frequency levels, along with two-dimensional envelop generator, makes it possible to recreate very accurate acoustic sound.

The 82C941 automatic power management module is an advanced control unit that achieves maximum power saving during creation of sound and stand-by operation of the DSP, υcode, and sound memory access operations. With this module, the device reliability of operation is expanded beyond industrial specification and operational environment for all of the 82C941 application fields.

Using OPTi Q_PCM technology, the 16 bit-sound sampling data is compressed at a 4:1 rate to accomplish a low cost requirement for sound memory with no sound degradation. The inside of the 82C941 decompression module reconverts original true 16-bit sampled sound data using compressed sound data. The internal 16 bit Q_PCM data produces the best quality of sound at 44.1 KHz playback by using an internal 32-bit data path for each module, along with an auto-looping sequencer, which is capable of handling 1 to 1 million auto-reload looping or non-looping sequences or one short looping sequence.

The 82C941 digital Q_filter is implemented to support variable frequency for each voice from 12 dB to 96 dB to achieve optimized sound characteristics. With this Q_filter, each sound can be produced more clearly and naturally with a small amount of sound data, also, musical effects can be obtained by time varying filter control. Due to the high performance of the Q_filter, a more realistic patch split effect, an after-touch effect, and a breath effect can be achieved by cross-mapping the Q_filter either by note or by velocity with the MIDI parameter.

The 82C941 CPU interface module contains all the necessary interface logic and CPU data memory to minimize overall system integration cost and to utilize slow speed 8-bit microprocessors without degradation of playback sound quality. To achieve minimum CPU handshaking during operation, all the generation and recreation of sound parameters is done by self-control hardware inside the module instead of depending on the CPU handshaking to receive internal synthesizer parameters to continue sound generation operation. Also, EXTCSB and EXTRAM can be used for multilevel connection of synthesis devices and record memory connection for high performance sound module or instrument applications.

5.0 Electrical Specification

Parameter	Symbol	Min	Typ	Max	Units
Absolute Maximum Ratings					
Ambient Temperature	-	-40		+85	°C
Storage Temperature	-	-65		+150	°C
Voltage on any Pin to VSS	-	-0.5		VCC + 0.5	V
Supply Voltage	VCC	-0.5		6.5	V
Maximum IOL per I/O Pin	-			15	mA
Recommended Operating Conditions					
Supply Voltage	VCC	4.75		5.25	V
Supply Voltage	VSS		0		V
Operating Free-Air Temperature	TA	0		70	°C
DC Characteristics (Over Operating Conditions)					
Input low voltage @ VCC = 5.0V	VIL	-0.5		1.5	V
Input high voltage @ VCC = 5.0V	VIH	3.5		VCC + 0.5	V
Output low voltage @ IOL = 3.2mA, Vcc = 5.0V	VOL			0.45	V
Output high voltage @ IOH = 0.8mA, Vcc = 5.0V	VOH	2.4			V
Logical 0 input current @ VIN = 0.45V	IIL			-50	µA
Input leakage current @ 0.45 < VIN < VCC	ILI			±10	µA
Power supply current @ Vcc = 5.0V	ICC		5	10	mA
External Clock Characteristics					
Oscillator frequency	1/TCLCL		45.1585		MHz
High Time	TCHCX		9		ns
Low Time	TCLCX		9		ns
Rise Time	TCLCH		5		ns
Fall Time	TCHCL		5		ns
AC Characteristics (Over Operating Conditions)					
ALE Signal Width	TLHL	127			ns
Address Valid Time to ALE Low	TAVLL	28			ns
Address Hold Time after ALE Low	TLLAX	48			ns
ALE Low to RDB for WRB Low	TLLWL	200			ns
ALE Low to Valid Time Data Out	TLLDV			517	ns
Address Valid Time to RDB WRB Low	TAVWL	203			ns
Address to Valid Data Out Time	TAVDV			585	ns
RDB Low to Address Hold Time	TRLAZ			0	ns
ALE High to Address Latch Out	TALDL		20		ns

Parameter	Symbol	Min	Typ	Max	Units
RDB Signal Width	TRLRH	400			ns
RDB Low to Valid Data Out	TRLDV			252	ns
Data Hold Time after RDB	TRHDX	0			ns
Data Hold Time after RDB	TRHDZ			97	ns
WRB to RDB High to ALE High	TWHLH	43		123	ns
Data Valid Time to WRB Transition	TQVWX	23			ns
Data Hold Time after WRB	TWHQX	33			ns
Memory Chip Select Pulse Width	TCSPW	850			ns
Memory Address Valid after CSB Low	TCSLAV		20		ns
Memory Data Value Time after CSB Low	TAVDO			150	ns

5.1 Timing Diagrams

Figure 5-1 Format of DAC Output Waveforms

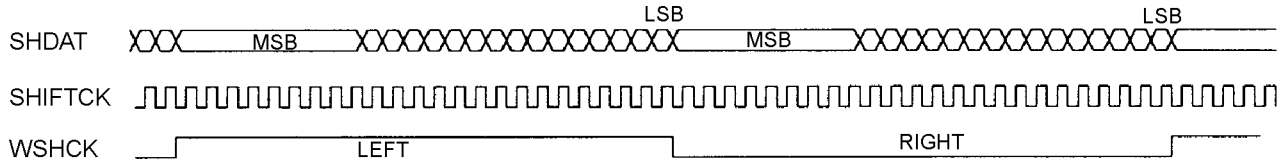


Figure 5-2 External Clock Waveform

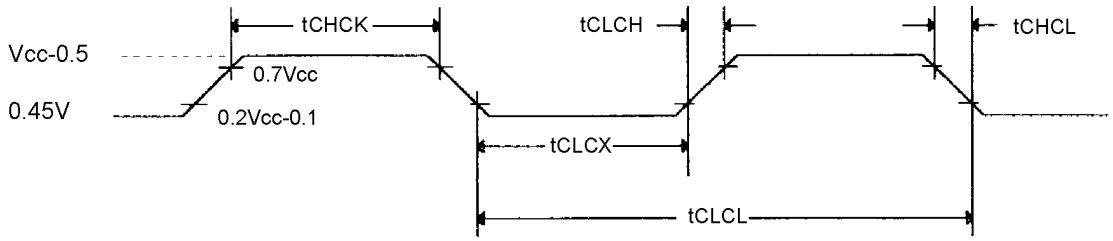


Figure 5-3 Data Memory Read Waveform

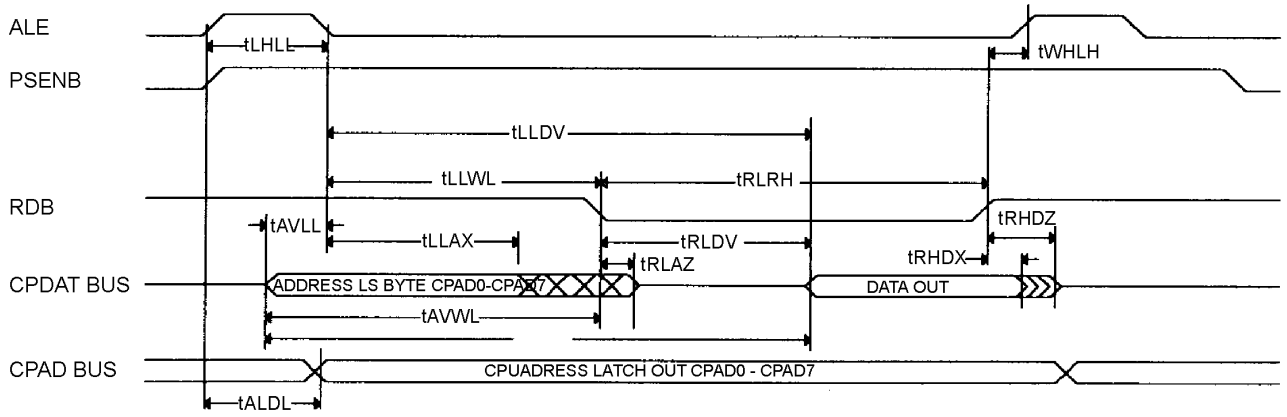


Figure 5-4 Data Memory and DSP Write Waveform

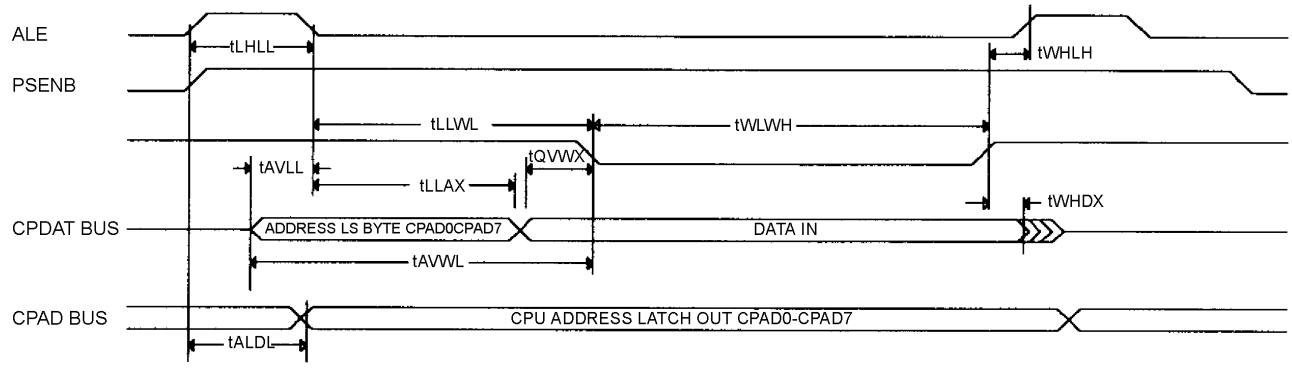
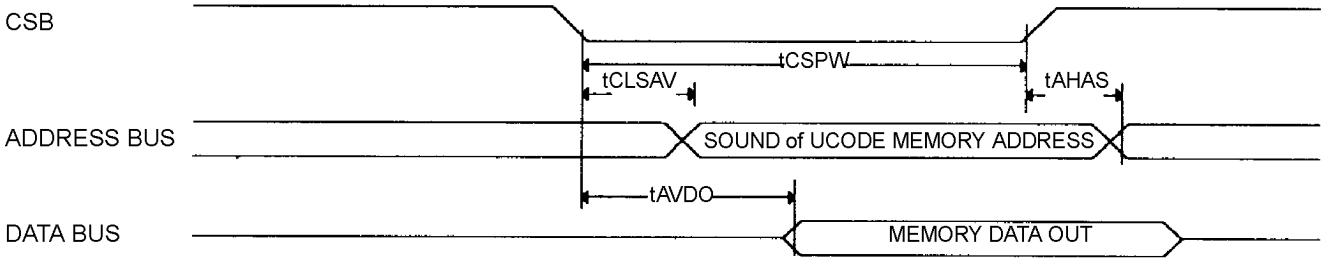
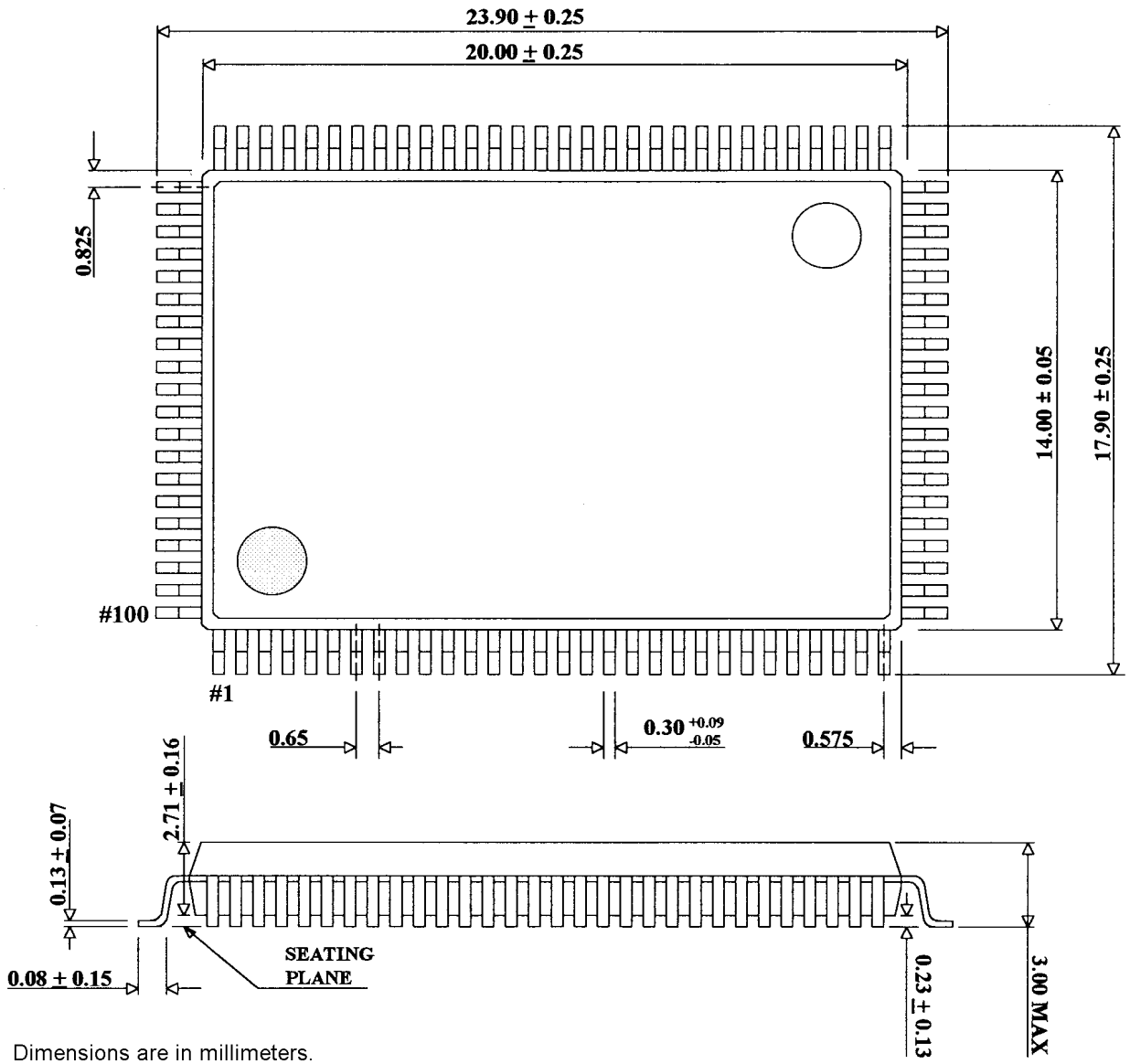


Figure 5-5 Sound and µcode Memory Read Waveform



6.0 Mechanical Package Dimensions

Figure 6-1 Mechanical Package Dimensions



Dimensions are in millimeters.