AN8212K

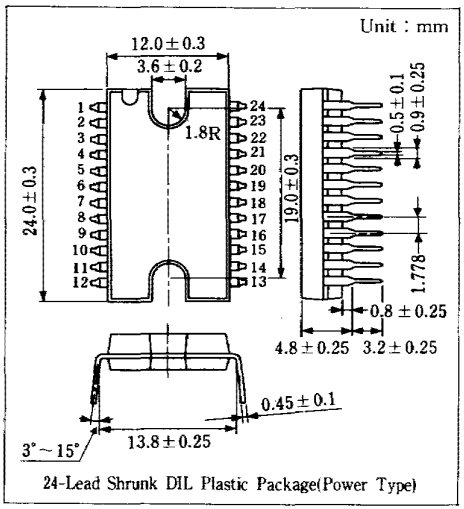
IC for FDD Spindle Motor Control

■ Outline

The AN8212K is an integrated circuit in which 300/360 rpm speed change-over function is added to the AN8210NK for FDD spindle motor.

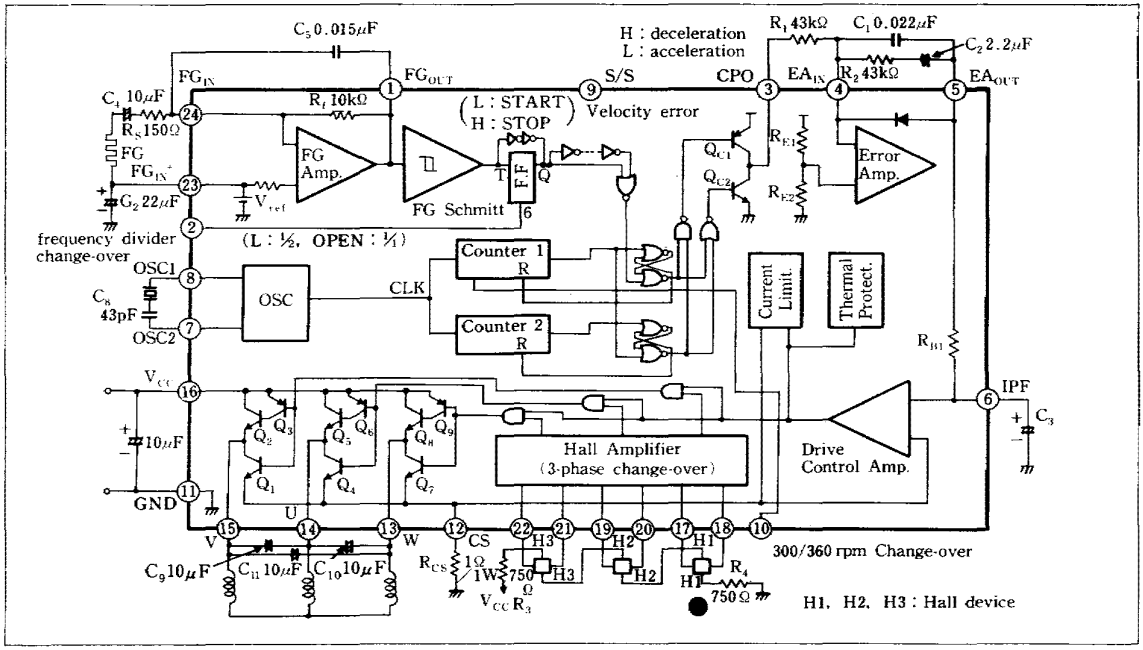
■ Features

- Speed change-over built-in (300/360rpm)
- FG divider change-over built-in (1/½)
- Speed control by digital velocity detector
- 3-phase full wave current drive
- Motor current limit built-in
- Thermal protect built-in
- Start/stop switch



24-Lead Shrunk DIL Plastic Package(Power Type)

■ Block Diagram and Application Circuit



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	FG Amp. Output	13	Motor Drive Output W
2	FG Divider	14	Motor Drive Output U
3	Verocity Error Output	15	Motor Drive Output V
4	Error Amp. Inversion Input	16	V_{CC}
5	Error Amp. Output	17	Hall Amp. 1+Input
6	Low-Pass Filter	18	Hall Amp. 1−Input
7	Oscillation Circuit 2	19	Hall Amp. 2+Input
8	Oscillaton Circuit 1	20	Hall Amp. 2−Input
9	Start/Stop Switching	21	Hall Amp. 3−Input
10	300/360 rpm Switching	22	Hall Amp. 3+Input
11	GND	23	FG Amp.+Input
12	Current Sensing	24	FG Amp.+Input

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
Motor Drive Pin Voltage	V_{13},V_{14},V_{15}	20	V
Pin Applied Voltage 1	V_1~V_9,V_{24}	−0.3~+5.5	V
Pin Applied Voltage 2	V_{17}~V_{22}	0~V_{CC}	V
Pin Applied Voltage 3	V_{10}	−0.3~0.9	V
Supply Current	I_{CC}	900	mA
Pin Current 1	I_{12}	−900~0	mA
Motor Drive Pin Current	I_{13},I_{14},I_{15}	−900~+900	mA
Pin Current 2	I_{23}	−20~+1	mA
Power Dissipation	P_D	2.5	W
Operating Ambient Temperature	T_{opr}	−20~+75	℃
Storage Temperature	T_{stg}	−55~+150	℃

■ Electrical Characteristics (V_{CC}=12V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Standby Quiescent Current	I_{QS}	1	$V_{S/S}$=2V		0.3	0.5	mA
No-load Quiescent Current	I_{QN}	1	$V_{S/S}$=0V		18	25	mA
Reference Voltage Part							
Reference Voltage	V_{OR}	2	I_{OR}=0mA	2.3		2.8	V
Output Sink Current	I_{OR}^+	2		0.5			mA
Output Source Current	I_{OR}^-	2			−15	−10	mA
Output Impedance	Z_{OR}	2	I_{OR}=0~−10mA		5	10	Ω
FG Amp./Schmitt Part							
Offset Voltage	V_{OSF}	3		−15		15	mV
Feedback Resistance	R_{FF}			6.2	8.7	11.2	kΩ
Output Sink Current	I_{OF}^+	4	V_S=0V, V_R=3V	3			mA
Output Source Current	I_{OF}^-	4	V_S=0V, V_R=2V			−3	mA
Speed Error Detect Part(Logic)							
Count Switch-Over Voltage	V_{CT}	5		1.0	1.8	2.5	V
Count No. 1	N_{CT1}	5	V_{CT}=L		1006		Time
Count No. 2	N_{CT2}	5	V_{CT}=H		838		Time

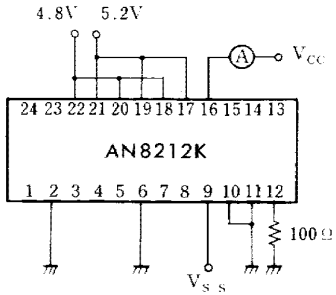
■ Electrical Characteristics (Cont'd) (V_{CC}=12V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Speed Error Output Part							
Output Low Voltage	V_{OLC}	6			0.1	0.3	V
Output High Voltage	V_{OHC}	6		4.4		5.2	V
Output Sink Current	I_{OC}^+	6		300			μA
Output Source Current	I_{OC}^-	6				−150	μA
Error Amp. Part							
Output Sink Current	I_{OE}^+	8		2			mA
Output Source Current	I_{OE}^+	8				−2	mA
Gain Bandwidth Product	f_{GBE}	8			500		kHz
FG Divider Change-Over			V_{FG}=0V		600/720		rpm
300/360 rpm Change-Over			V_{FG}=2.5V		300/360		rpm
Drive Control Amp. Part							
Threshold Voltage	V_{THD}	9		2.3	2.55	2.8	V
Drive Gain	A_{CD}	9		1.6	1.8	2.0	Time
Limiter Voltage	V_{LD}	9		0.59	0.66	0.72	V
Open Loop Drive Gain	A_{OD}				30	30	dB
Hall Amp. Part							
Phase Input Voltage Range	V_{ICH}			2		V_{CC}−2	V
Error Input Voltage Range	V_{IDH}					400	mV
Hall Input Sensitivity	V_{ISH}				10		mV
Hall Offset Voltage	V_{OSH}	10				20	mV
Input Bias Current	I_{BH}	11			1.0	5.0	μA
Drive Output Part							
Saturation Voltage(on V_{CC})	V_{SU}	12				1.4	V
Saturation Voltage (on ground)	V_{SL}	12				1.1	V
OFF Leak Current	I_{LO}	12		−20		20	μA
Start/Stop Control Part							
Input Low Voltage	V_{IL}		$V_{S/S}$=0V			0.7	V
Input High Voltage	V_{IH}		$V_{S/S}$=2V	2			V
Input Low Current	I_{IL}	13		−100	−50		μA
Input High Current	I_{IH}	13			10	100	μA
Speed Error Output Part							
Output Leak Current	I_{LC}*	6				0.1	μA
Input Bias Current	I_{BE}*	7				0.1	μA
Quienscent Breakdown Level	V_S*		Applied between GND and each pin (C=100pF, No R)	300			V

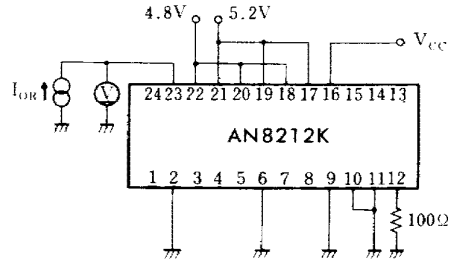
Note) Operating Supply Voltage Range : $V_{CC(opr)}$=9~16V

* These values are of reference values but not guaranteed values.

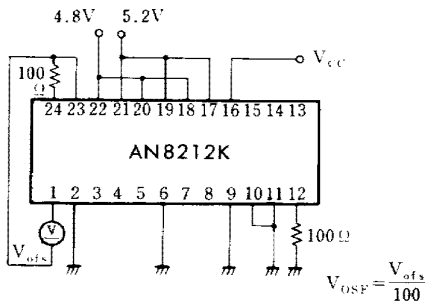
Test Circuit 1 (I_{QS}, I_{QN})



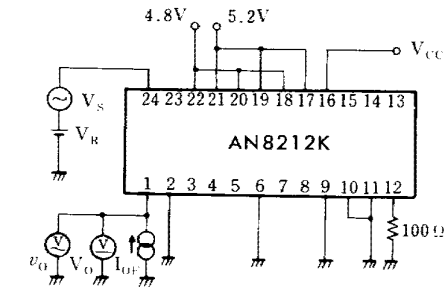
Test Circuit 2 (V_{OR}, I_{OR}^+, I_{OR}^-, Z_{OR})



Test Circuit 3 (V_{OSF})

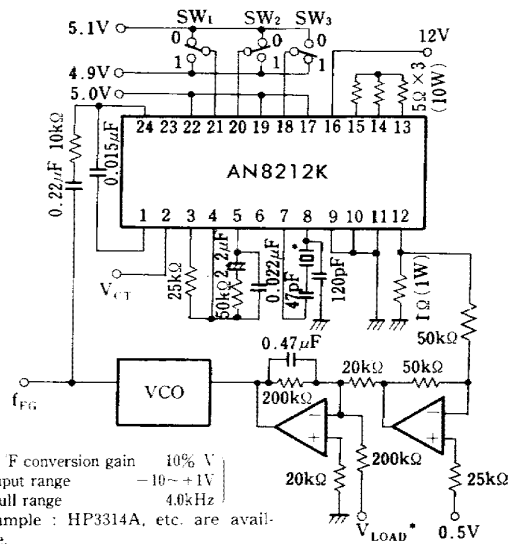


Test Circuit 4 (I_{OF}^+, I_{OF}^-)



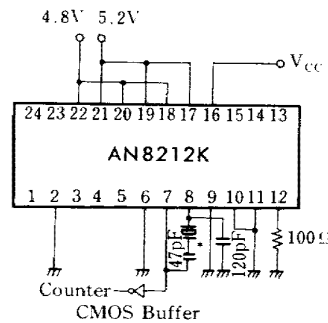
When output sink current $I_{OF}=3mA$, $V_O<1.7V$ ($V_R=3V$, $V_S=0V$)
When output source current $I_{OF}=-3mA$, $V_O>3.2V$, ($V_R=2V$, $V_S=0V$)
Open loop gain $A_{VF}=20\log(v_O/V_S)$

Test Circuit 5 (V_{CT}, N_{CT1}, N_{CT2})



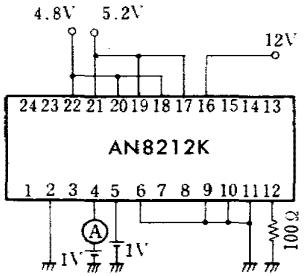
V F conversion gain 10% V
Input range −10~+1V
Full range 4.0kHz
Example : HP3314A, etc. are available.
*Ceramic resonator (512kHz)

Test Circuit 6 (V_{OLC}, V_{OHC}, I_{OC}^+, I_{OC}^-, I_{BE})

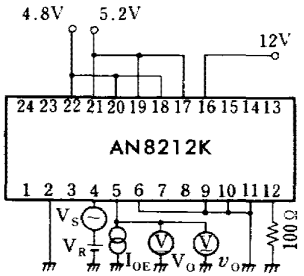


*Ceramic resonator is used (512kHz)

Test Circuit 7 (I_{BE})

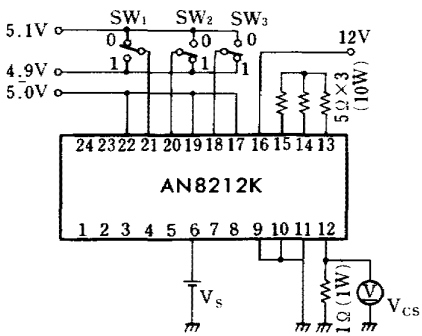


Test Circuit 8 (I_{OE}^+, I_{OE}^-, f_{GBE})

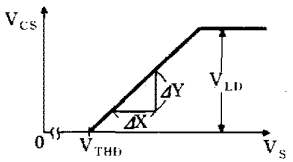


When output sink current I_{OF}=2mA, V_O<1.6V (V_R=3V, V_S=0V)
When output source current I_{OF}=−2mA, V_O>1.8V, (VR=2V, V_S=0V)
Open loop gain A_{VF}=20log (v_O/V_S)

Test Circuit 9 (V_{THD}, A_{CD}, V_{LD})



$V_S - V_{CS}$ Input Characteristics



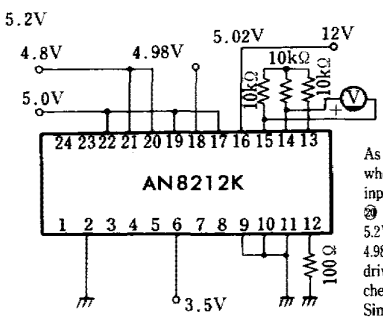
Drive gain $A_{CD}=\Delta Y/\Delta X$ (ΔX=0.2V)

Measure each point (V_{THD}, A_{CD}, V_{LD}) shown in the figure left.

Test	SW_1	SW_2	SW_3
1	1	0	1
2	1	1	0
3	0	1	1

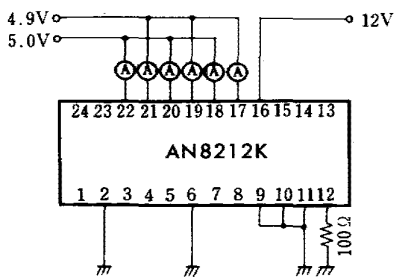
At the same time, change over SW_1 to SW_3 as shown in the figure left and measure each point every item above.

Test Circuit 10 (V_{OSH})

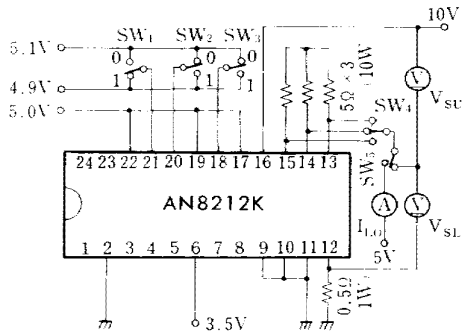


As shown in the figure left, when all polarity of hall amp. input is reversed such as Pin ⑳ and ㉑ are reversed from 5.2V to 4.8V and Pin ⑱ from 4.98V to 5.02V, polarity of drive output is reversed, checking offset voltage Pin ⑯. Similarly, measurement is made for each phase.

Test Circuit 11 (I_{BH})



Test Circuit 12 (V_{ST}, V_{SL}, I_{LO})

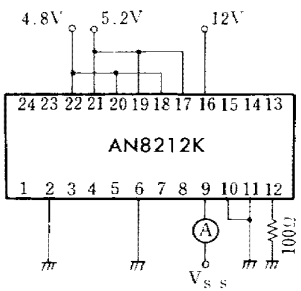


Logical Table of Phase Change-over · Hall Input-Drive Output Logic

No.	SW_1	SW_2	SW_3	13(W)	14(U)	15(V)
1	1	1	1	off	off	off
2	1	1	0	off	H	L
3	1	0	1	H	L	off
4	0	1	1	L	off	H
5	1	0	0	H	off	L
6	0	1	0	L	H	off
7	0	0	1	off	L	H
8	0	0	0	off	off	off

According to the logic table above, determine the states of output Pins ⑬ to ⑮ and select SW_4 or SW_5 appropriately.

Test Circuit 13 (I_{IL}, I_{IH})



P_D Ta