

Components and materials

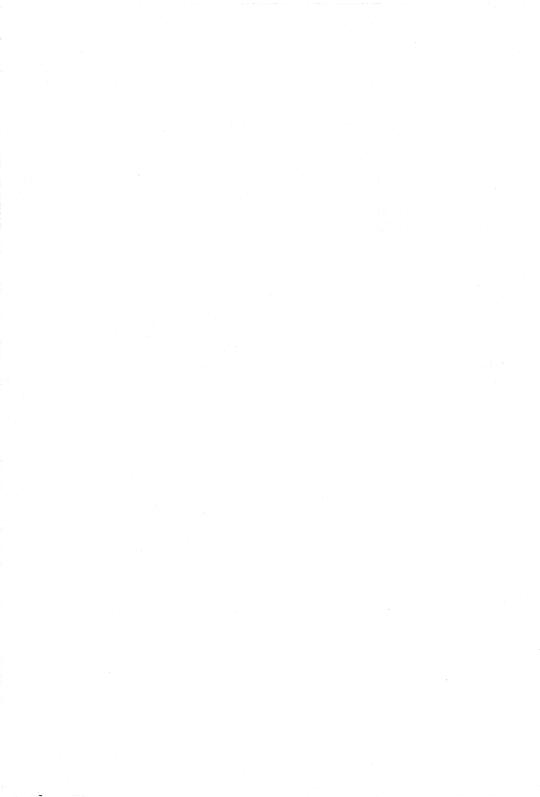
Book C1

1985

PLC modules PC20 modules

PROGRAMMABLE CONTROLLER MODULES

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES

BLUE

SEMICONDUCTORS

RED

INTEGRATED CIRCUITS

PURPLE

COMPONENTS AND MATERIALS

GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

- T1 Tubes for r.f. heating
- T2a Transmitting tubes for communications, glass types
- T2b Transmitting tubes for communications, ceramic types
- T3 Klystrons, travelling-wave tubes, microwave diodes
- ET3 Special Quality tubes, miscellaneous devices (will not be reprinted)
- T4 Magnetrons for microwave heating
- T5 Cathode-ray tubes
 Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6 Geiger-Müller tubes
- T7 Gas-filled tubes

Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 Picture tubes and components

Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 Photo and electron multipliers

Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

- T10 Camera tubes and accessories
- T11 Microwave semiconductors and components
- T12 Vidicons and Newvicons
- T13 Image intensifiers
- T14 Infrared detectors
- T15 Dry reed switches
- T16 Monochrome tubes and deflection units

 Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

Data collations on these subjects are available now. Data Handbooks will be published in 1985.

November 1984

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1	$\label{eq:continuous} \begin{tabular}{ll} \textbf{Diodes} \\ Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes ($<$ 1,5$ W), voltage reference diodes, tuner diodes, rectifier diodes ($<$ 1,5$ W), voltage reference diodes, tuner diodes, rectifier diodes ($<$ 1,5$ W), voltage reference diodes, tuner diodes, rectifier diodes ($<$ 1,5$ W), voltage results ($<$ 1,5$ W), voltage reference diodes, tuner diodes, rectifier diodes ($<$ 1,5$ W), voltage results ($<$ 1,5$ W), voltage results$
S2a	Power diodes
S2b	Thyristors and triacs
S3	Small-signal transistors
S4a	Low-frequency power transistors and hybrid modules
S4b	High-voltage and switching power transistors
S 5	Field-effect transistors
S6	R.F. power transistors and modules
S7	Surface mounted semiconductors
S8	Devices for optoelectronics Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
S9	Power MOS transistors
S10	Wideband transistors and wideband hybrid IC modules
S11	Microwave semiconductors (to be published in this series in 1985) All present available in Handbook T11
S12	Surface acoustic wave devices

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1	Bipolar ICs for radio and audio equipment
IC2	Bipolar ICs for video equipment
IC3	ICs for digital systems in radio, audio and video equipment
IC4	Digital integrated circuits CMOS HE4000B family
IC5	Digital integrated circuits — ECL ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
IC6	Professional analogue integrated circuits
IC7	Signetics bipolar memories
IC8	Signetics analogue circuits
IC9	Signetics TTL logic
IC10	Signetics Integrated Fuse Logic (IFL)

Microprocessors, microcomputers and peripheral circuitry

IC11

NEW SERIES

IC01N	Radio, audio and associated systems Bipolar, MOS	
IC02N	Video and associated systems Bipolar, MOS	
IC03N	Telephony equipment Bipolar, MOS	
IC04N	HE4000B logic family CMOS	
IC05N	HE4000B logic family uncased integrated circuits CMOS	(published 1984)
IC06N	PC54/74HC/HCU/HCT logic families HCMOS	
IC07N	PC54/74HC/HCU/HCT uncased integrated circuits HCMOS	
IC08N	10K and 100K logic family ECL	(published 1984)
IC09N	Logic series TTL	(published 1984)
IC10N	Memories MOS, TTL, ECL	
IC11N	Analogue - industrial	
IC12N	Semi-custom gate arrays & cell libraries ISL, ECL, CMOS	
IC13N	Semi-custom integrated fuse logic IFL series 20/24/28	
IC14N	Microprocessors, microcontrollers & peripherals Bipolar, MOS	
IC15N	Logic series FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 -	Programmable controller modules
	PLC modules PC20 modules

- C2 Television tuners, video modulators, surface acoustic wave filters
- C3 Loudspeakers
- C4 Ferroxcube potcores, square cores and cross cores
- C5 Ferroxcube for power, audio/video and accelerators
- C6 Synchronous motors and gearboxes
- C7 Variable capacitors
- C8 Variable mains transformers
- C9 Piezoelectric quartz devices

Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

- C10 Connectors
- C11 Non-linear resistors

Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

- C12 Variable resistors and test switches
- C13 Fixed resistors
- C14 Electrolytic and solid capacitors
- C15 Ceramic capacitors*
- C16 Permanent magnet materials
- C17 Stepping motors and associated electronics
- C18 D.C. motors
- C19 Piezoelectric ceramics
- C20 Wire-wound components for TVs and monitors
- C21 Assemblies for industrial use
 HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

October 1984

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^{*} Film capacitors are included in Data Handbook C22 which will be published in 1985. The September 1982 edition of C15 should be retained until C22 is issued.

PLC MODULES



MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

INTRODUCTION

The programmable logic controller (PLC) is used for the controlling of machines or processes. It can be easily programmed and re-programmed as required.

The modular design of the PLC enables a user to build a PLC which is 'tailor-made' for his control task. By specifying the number and the types of PLC modules that he requires, he avoids purchasing more of the expensive electronic capability than he needs.

The PLC modules are formed on standard double Eurocards. Optically coupled interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ease compatibility headaches.

Besides the PLC modules, the PLC comprises back panels, a frame (19 in rack) and a standard power supply. The frame must conform to IEC297 or DIN41494 (for racks) and IEC130-14 or DIN41612 (for connectors). The adoption of these standards means that the frame and the power supply should be easily obtainable.

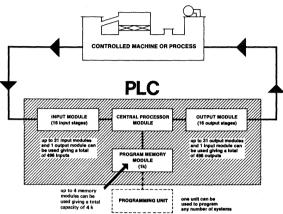
The following PLC modules are available.

type	description	catalogue no.	page
CP10	central processor, 32 registers	4322 027 90420	7
CP11	central processor, without registers	4322 027 90390	7
IM10	input module, 16 inputs, 24 V d.c.	4322 027 90434	17
IM11	input module, 16 inputs, 24 V a.c.	4322 027 90403	17
LX10	load external interface module	4322 027 91600	23
MM10	program memory module, 1 k, non-volatile core RAM	4322 027 91400	31
MM11	program memory module, non-volatile, UV-erasable PROMs. 1 k 13 or 2 k 13 capacity; for program copying or read-out	4322 027 91630	37
MM12	program memory module, non-volatile. UV-erasable PROMs, 1 k 13 or 2 k 13 capacity; for read-out only	4322 027 91640	45
OM10	output module, 16 outputs, max. 0,1 A each, 24 V d.c.	4322 027 90440	51
OM12	output module, 8 outputs max. 2 A each, 24 V d.c.	9360 011 50112	57
PI10*	punch and teletype interface module	8222 412 41572	63
PU10	programming unit	4322 027 90410	71
BP11 to BP16	back panels	9390 269 .0112	79

^{*} Obsolescent type.

MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

The diagram shows, in a simplified form, the function of each of the PLC modules. In operation the PLC cycles continuously through a data input/output cycle and a data processing cycle.



The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is portable and thus one may be used to serve any number of PLCs. It is also sufficiently inexpensive to make the permanent location of one in each PLC for monitoring or test purposes, a realistic and useful proposition.

PLC

MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

GENERAL CHARACTERISTICS

Operating temperature range

0 to +60 °C

Storage temperature range

-40 to +70 °C

Dimensions

160 mm x 233 mm (double Eurocard) according to IEC297 or DIN41494

Supply voltage (d.c.)

 $V_P = 5 \text{ V } \pm 5\%; \frac{dV_P}{dt} \le 5 \text{ V/ms}$

Maximum number of input + output signals

512

Maximum program length

4 x 1024 words

Cycle time

0,029 $(n_{IM} + n_{OM}) + 1$,85 n_{MM} ms

$$\begin{split} &n_{IM} = number \ of \ input \ modules \\ &n_{OM} = number \ of \ output \ modules \\ &n_{MM} = number \ of \ memory \ modules \end{split}$$

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC68-2, test method Fc: 5 to 55 Hz, amplitude 1,5 mm or 5 g (whichever is less).

Shock test

IEC68-2, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50 g.

Rapid change of temperature test

IEC68-2, test method Na: 5 cycles of 2 h at -40 $^{\rm o}$ C and 2 h at +70 $^{\rm o}$ C.

Damp heat test

IEC68-2, test method Ca: 21 days at 40 $^{\circ}$ C, R.H. 90 to 95%.



CENTRAL PROCESSORS

DESCRIPTION

These central processors are modules intended for use in combination with the input module IM10 (or IM11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The central processor is the heart of the logic controller; it asks the input modules for data and the program memory for instructions, processes the data according to these instructions, and applies the result to the output modules. It also generates the internal timing of the controller.

The processor actions take place in two distinct cycles: an input/output cycle and a data processing cycle.

During the input/output cycle the processor addresses each input stage in turn (counter/buffer register) and transfers the present data to the corresponding scratch-pad memory location, see Fig. 1. In the same cycle the processed data of the previous data processing cycle are clocked out from the scratch-pad memory into the latch flip-flops of the output modules. As the scratch-pad memory can hold up 512 bits of data the central processor can handle a maximum combination of 512 inputs, outputs, and intermediate results. Provision is made to prevent loss of information of the scratch-pad memory in the case of power failure.

During the data processing cycle the processor applies an address and a cycle initiate signal to the program memory, which in turn then apply a program word to the processor. The program word contains an instruction and an address, which comprise 13 data bits. An instruction consists of 4 bits of data; these are applied to the logic processing unit and the register processing unit. \(^1\) The other 9 bits of data form the scratch-pad memory address and are used to select the data bit at this memory location, and also one of the 32 8-bit registers. \(^1\) The logic processing unit only processes data from the scratch-pad memory. The register processing unit processes the data stored in one of the 8-bits registers, in conjunction with a working register (A-register). Due to the fact that a register is always selected when a scratch-pad memory address is selected, the results of register processing will be stored in the corresponding scratch-pad memory location (condition register). Data for the registers can be supplied by the program memory or by an external source. These data are stored in the registers during the data processing cycle.

¹⁾ Only present in the CP10.

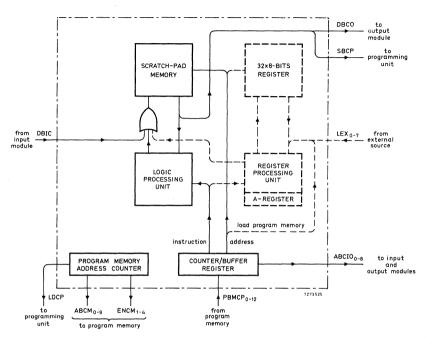


Fig. 1. Simplified block diagram of the central processor. Blocks drawn with broken lines are only extant in the CP10.

The central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) 1). The board has a metal screen at the components side, which is connected to the 0 V line.

¹⁾ For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Battery back-up requirements to save contents of the scratch-pad memory in case of power failure.

Battery current
$$(V_p = 0 V)$$

Trickle charge current $(V_P = 5 V)$

$$I_{B}$$

I_B typ. 3,5 mA at
$$V_B = 5 V$$

typ. 2 mA at $V_B = 5 V$

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
PBMCP0 PBMCP1 PBMCP2 PBMCP3 PBMCP4 PBMCP5 PBMCP6 PBMCP7 PBMCP8 PBMCP9 PBMCP10 PBMCP11	Program word bits from program memory.	1 TTL 1 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7 a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13
MICC	Memory identification signal; this signal is connected to one of the four ENCM-outputs of the central processor.	1 TTL 2 TTL	a5	a14, c14
SCPC	Store command from programming unit; initiates SCCM (see output data) when the central processor is in a data processing cycle.	2 TTL		a15, c15
DBIC	Data bit from input stage; data is stored in scratch-pad memory during input/output cycle.	3 TTL	c20	
CLCP	Clear signal from external source. When CLCP is LOW the central processor is kept in the start position of an input/output cycle; when CLCP is HIGH the central processor is running (see also SPCE).	2 TTL	a20	

input	function	load	terminations (Fig. 4)		
			connector 1	connector 2	
SPCE	Scratch-pad clear enable line from external source. When SPCE is HIGH and CLCP goes from LOW to HIGH all scratch-pad places (except those which are addressed as an input) are set to zero in the first input/output cycle; when SPCE is LOW and CLCP goes from LOW to HIGH the central processor starts with a normal input/output cycle.	2 TTL	a22		
IDIC	Identification signal from input module; prepares central processor for data on DBIC to be written in the scratch-pad memory.	3 TTL	c24		
IDLC	Identification signal from last input or output module; indicates that the last input or output module has been selected.	2 TTL	c26		
LEX ₀ LEX ₁ LEX ₂ LEX ₃ LEX ₄ LEX ₅ LEX ₆ LEX ₇	Data inputs from an external source; eight data bits from an external source can be loaded into the A-register.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a6 a7 a8 a9 a10 a11 a12 a13		

Output data

All outputs meet the standard TTL specifications.

output	function	loada - bility	terminations (Fig. 4)	
			connector 1	connector 2
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits to input and output modules. ABCIO $_{0-3}$ select the input or output stage, ABCIO $_{4-8}$ select the input or output modules.	32 TTL 32 TTL 32 TTL 32 TTL 32 TTL 32 TTL 32 TTL 32 TTL 32 TTL 32 TTL	c2 c4 c6 c8 c10 c12 c14 c16	

output	function	loada - bility	terminations (Fig. 4)		
			connector 1	connector 2	
ABCM ₀ ABCM ₁ ABCM ₂ ABCM ₃ ABCM ₄ ABCM ₅ ABCM ₆ ABCM ₇ ABCM ₈ ABCM ₉	Address bits to program memory, initiated by program address counter.	10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL		a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28 a29, c29	
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4 k	8 TTL 8 TTL 8 TTL 8 TTL	a1, c1 a2 a3 a4		
SCCM	Store command to program memory; level determines whether a program word is read out from program memory to central processor (LOW) or a new program word is written into the program memory (HIGH). SCCM = SCPC.	10 TTL		al7, cl7	
CICM CICM	Cycle initiate signal to program memory; depending on the level of SCCM, CICM starts read/restore or clear/write cycle (bipolar to reduce noise sensitivity).	9 TTL		a19, c19 a18, c18	
$\overline{\text{CL}}_{23}$	Inverted clock signal to programming unit.	10 TTL	a 15		
CLCO	Clock signal to output module, stores data on DBCO into output stage during input/output cycle.	32 x OM10	a28		
DBCO	Data bit to output module; data is stored in output stage by CLCO.	31 TTL	c22		
SBCP	Status bit to programming unit; clocked by ϕ_{57} it indicates "1" or "0" at selected scratch-pad memory address.	1 TTL	a16		
LDCP	Synchronization signal to programming unit, synchronizes auxiliary address counter in programming unit with address counter in central processor.	10 TTL	a 14		
^Ф 57	Clock signal for state indication on programming unit; occurs only during data processing cycle.	10 TTL		a16, c16	

Alarm output (a26 of connector 1): open collector output, which indicates a LOW level when Vp< 4,75 V. $V_{\hbox{\tt alarm}},$ LOW level < 0,4 V at I_{C} = 3 mA.

Time data

Scan time per input or output module Read time per 1 k memory module

Total cycle time

0,029 ms 1,85 ms

 $0,029 (n_{IM} + n_{OM}) + 1,85 n_{MM} ms$

 $\begin{array}{ll} n_{IM} & = number \ of \ input \ modules \\ n_{OM} & = number \ of \ output \ modules \\ n_{MM} & = number \ of \ memory \ modules \end{array}$

Note - By removing a wire jump, marked "A", on the central processor board the scan time per input or output module is set to 7,4 ms.

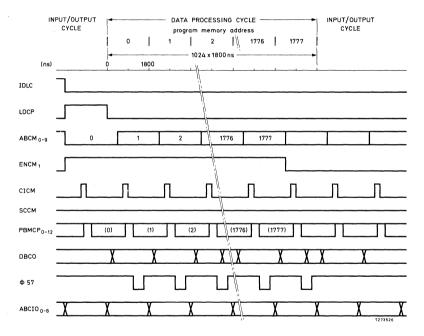


Fig. 2. Timing diagram of data processing cycle.

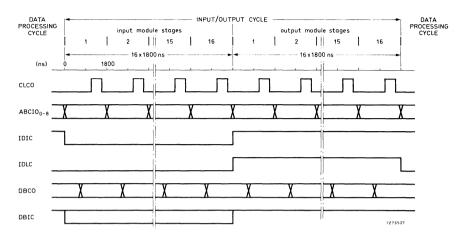
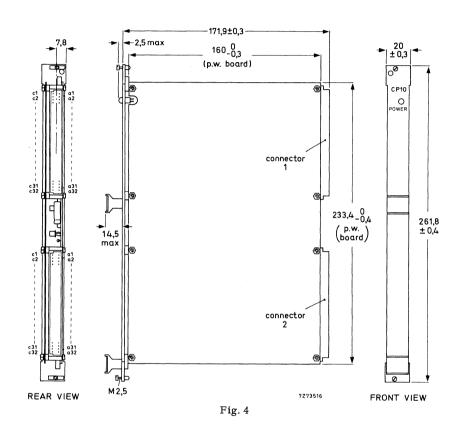


Fig. 3. Timing diagram of input/output cycle.

MECHANICAL DATA

Dimensions in mm

Outlines



Mass

400 g

Terminal location

co	onnector	1	co	nnector	2
row c		row a	row c		row a
ENCM ₁	1	ENCM ₁	i.c.	1	i.c.
$ABCIO_0$	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀
n.c.	3	ENCM3	PBMCP ₁	3	PBMCP ₁
ABCIO ₁	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂
n.c.	5	MICC	PBMCP3	5	PBMCP ₃
ABCIO ₂	6	LEX_0	PBMCP 4	6	PBMCP ₄
n.c.	7	LEX ₁	PBMCP5	7	PBMCP5
ABCIO ₃	8	LEX ₂	PBMCP ₆	8	PBMCP6
n.c.	9	LEX3	PBMCP7	9	PBMCP7
ABCIO 4	10	LEX ₄	PBMCP ₈	10	PBMCP ₈
n.c.	11	LEX5	PBMCP9	11	PBMCP ₉
ABCIO5	12	LEX ₆	PBMCP ₁₀	12	PBMCP ₁₀
n.c.	13	LEX ₇	PBMCP ₁₁	13	PBMCP ₁₁
ABCIO ₆	14	LDCP	PBMCP ₁₂	14	PBMCP ₁₂
n.c.	15	$\overline{\mathrm{CL}}_{23}$	SCPC	15	SCPC
ABCIO ₇	16	SBCP	ϕ 57	16	φ57
n.c.	17	n.c.	SCCM	17	SCCM
ABCIO8	18	n.c.	CICM	18	CICM
n.c.	19	n.c.	CICM	19	CICM
DBIC	20	CLCP	$ABCM_0$	20	$ABCM_0$
n.c.	21	n.c.	ABCM ₁	21	ABCM ₁
DBCO	22	SPCE	$ABCM_2$	22	ABCM ₂
n.c.	23	n.c.	ABCM ₃	23	ABCM3
IDIC	24	n.c.	ABCM ₄	24	ABCM ₄
n.c.	25	n.c.	ABCM5	25	ABCM ₅
IDLC	26	alarm	ABCM ₆	26	ABCM ₆
n.c.	27	n.c.	ABCM ₇	27	ABCM ₇
0 V ¹)	28	CLCO	ABCM ₈	28	ABCM ₈
n.c.	29	n.c.	ABCM9	29	ABCM9
n.c.	30	n.c.	v_{B}	30	$\mathbf{v_B}$
$V_{\mathbf{P}}$	31	$V_{\mathbf{P}}$	$V_{\mathbf{P}}^{\mathbf{D}}$	31	$V_{\mathbf{p}}^{\mathbf{D}}$
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

i.c. = internal connection.

 $^{^{1}\!\!}$) No supply line; only to be used as a ground connection for CLCO.



INPUT MODULES

DESCRIPTION

These input modules are intended for use in combination with the central processor CP10 (or CP11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The IM10 and IM11 are identical in many respects, but the IM10 is designed for d.c. inputs, whereas the IM11 is designed for a.c. and unsmoothed rectified inputs. Each input module contains 16 addressable input stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage of the IM10, to increase the noise immunity. The delay time can be increased by adding extra capacitance (approx. 0,068 μ F/ms). A rectifying and smoothing circuit is incorporated in each input stage of the IM11.

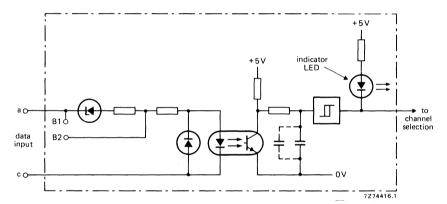


Fig. 1a Circuit diagram of an input stage (IM10).

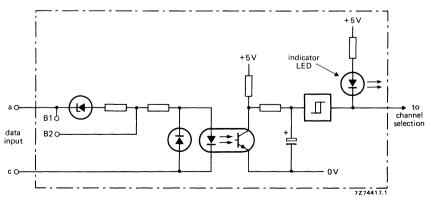


Fig. 1b Circuit diagram of an input stage (IM11).

4322 027 90434 4322 027 90403

Each input module has nine address inputs (ABCIO_{0.8}) and five module identification inputs (MID_{0.4}), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-1 connectors (board parts); the corresponding rack parts are available on the back panels BP11 to BP16 or separately under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags).*

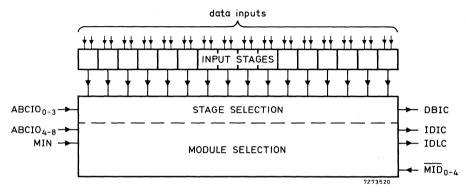


Fig. 2 Block diagram of the input modules.

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

current

٧p lp

5 V ± 5%

max. 0,5 A typ. 0,45 A

Input data

The data inputs are DIXY0 to DIXY7 and DIXZ0 to DIXZ7. They are accessible on connector 2, see "Terminal location".

Active voltage (Va-c)*

5 V level** 3.5 to 6 V▲

24 V level 17 to 30 V▲

Non-active voltage (Va-c)*

0 to 0,8 V or floating 0 to 7 V or floating 4 tvp. 10 mA

typ. 10 mA

The inputs mentioned below meet the standard TTL specifications.

Input current, active at $V_{a-c} = 5 \text{ V}$ or 24 V resp.

input	function	load	terminations of connector 1 (Fig. 3)
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits from central processor; ABCIO ₀₋₃ select the input stage, ABCIO ₄₋₈ selection the input module.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a2, c2 a4, c4 a6, c6 a8, c8 a10 a12 a14 a16 a18
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBIC to be stored in the scratch-pad memory of the central processor.	2 TTL	c26
MID ₀ MID ₁ MID ₂ MID ₃ MID ₄	Module identification inputs; provide module with individual identity.	2 TTL 2 TTL 2 TTL 2 TTL 2 TTL	c10 c12 c14 c16 c18

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

^{**} By short-circuiting terminals B1 and B2 (see Figs 1a and 1b).

[▲] D.C. (for IM10) or a.c. values (for IM11).

4322 027 90434 4322 027 90403

Output data

All outputs (open collector) meet the standard TTL specifications.

output	function	loadability	terminations of connector 1 (Fig. 3)
DBIC	Data bit to central processor; data is stored in scratch-pad memory of central processor.	10 TTL	a20
IDIC	Identification signal to central processor (active LOW); prepares central processor for data on DBIC to be written in the scratch-pad memory.	10 TTL	с24
IDLC	Identification signal from last input module to central processor (active HIGH); only the IDLC output of the last input module has to be connected with the IDLC input of the central processor.	2 TTL	a26

MECHANICAL DATA

Dimensions in mm

Outlines

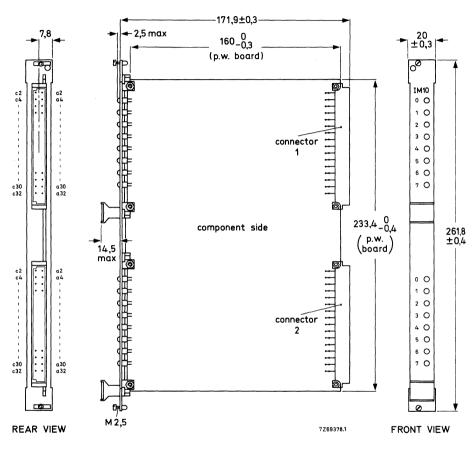


Fig. 3.

Mass 250 g

Terminal location

C	onnector '	1	C	onnector 2	
row c		row a	row c		row a
ABCIO ₀	2	ABCIO ₀	DIXY0	2	DIXY0
ABCIO ₁	4	ABCIO ₁	DI _{XY1}	4	DIXY1
ABCIO ₂	6	ABCIO ₂	DIXY2	6	DIXY2
ABCIO3	8	ABCIO3	DIXY3	8	DIXY3
\overline{MID}_{0}	10	ABCIO ₄	DIXY4	10	DIXY4
$\overline{\text{MID}}_1$	12	ABCIO ₅	DI _{XY5}	12	DIXY5
\overline{MID}_2	14	ABCIO ₆	DIXY6	14	DIXY6
MID ₃	16	ABCIO ₇	DIXY7	16	DIXY7
MID ₄	18	ABCIO ₈	DIXZ0	18	DIXZ0
0 V*	20	DBIC	DI _{XZ1}	20	DIXZ1
0 V*	22	n.c.	DI_{XZ2}	22	DIXZ2
IDIC	24	n.c.	DI _{XZ3}	24	DIXZ3
MIN	26	IDLC	DI _{XZ4}	26	DIXZ4
n.c.	28	n.c.	DI _{XZ5}	28	DI _{XZ5}
V_P	30	V _P	DIXZ6	30	DIXZ6
0 V	32	0 V	DI _{XZ7}	32	DIXZ7

n.c. = not connected.

^{*} No supply line; only to be used for coding of the $\overline{\text{MID}}_{0\text{--}4}$ lines.

LOAD EXTERNAL INTERFACE

DESCRIPTION

This load external interface is intended for use in combination with the central processor CP10, input module IM10 or IM11, output module OM10 or OM12, memory module MM10, MM11 or MM12 and programming unit PU10 to assemble a programmable logic controller (PLC). The module can be used as an interface between the load external inputs LEX₀ to LEX₇ on the CP10 and a number of 8-bit data sources. The data outputs of the different data sources have to be connected to one 8-bit data bus. The LX10 has 16 enable outputs $\overline{\text{EN}}_0$ to $\overline{\text{EN}}_{17}$, which are to enable the different data sources. The 8-bit data bus has to be connected to the data inputs DB0 to DB7. The data applied to the data inputs can be inverted on the LX10 by activating the data bit invert input DBI (see the truth table on the next page). The applied data can have a 5 V or a 24 V level. A block diagram is given in Fig. 1. The data inputs and enable outputs are electrically isolated from the 5 V logic circuitry by means of photocouplers. All data inputs are floating with respect to each other. Reading data from the data sources will only occur during the input/output cycle. The data are then stored in a 16 x 8 randomaccess memory (RAM) on the LX10. The data can be read out of the RAM during the data processing cycle. Storing data into the RAM can be inhibited by applying a 0 V level to the module inhibit input (MIN). Reading data out of the RAM cannot be inhibited. The module has 6 address inputs ABCIO3 to ABCIOs. This means that a total number of 64 data sources of 8-bits can be connected to the PLC system via 4 LX10 modules. Therefore the module is provided with 2 module identification inputs (MID₃, MID₄) which are accessible on the connector. Irrespective of the number of LX10 modules used, a complete input/output cycle of 0.924 ms will occur.

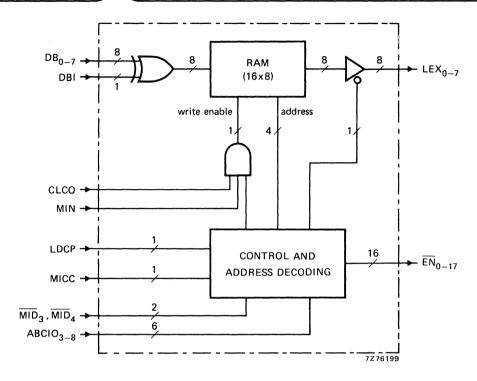


Fig. 1.

Truth	Table	e

data inputs DB ₀ to DB ₇	data input DBI	data ouput LEX ₀ to LEX ₇
active	active	0
non-active	active	1
active	non-active	. 1
non-active	non-active	0

ELECTRICAL DATA

Supply

Logic suppl	y voltage	(d.c.)
-------------	-----------	--------

Logic supply current (d.c.)

Supply voltage (d.c.) to drive enable outputs

Supply current (d.c.) to drive enable outputs

V۵	5\	/ +	5%

_ max. 0,7 A

typ. 0,6 A

5 V ± 5% 24 V ± 25%

max. 3 mA

max. 3 mA typ. 2,5 mA

Input data

The data inputs are DB_0 to DB_7 and DBI. They are accessible on connector 2 (see "Terminal location" and Fig. 2 for connection).

Active voltage (V _{a-c})*
Non-active voltage (V _{a-c}) *

Input current, active at $V_{a-c} = 5 \text{ V or } 24 \text{ V resp.}$

5 V level	24 V level
3,5 to 6 V	18 to 30 V
0 to 0,8 V	0 to 0,8 V
typ. 10 mA	typ. 10 mA

Connector 2

row a, terminals 1, 3, 5, 7, 9, 11, 13, 15, 17

row a, terminals 2, 4, 6, 8, 10, 12, 14, 16, 18

row c, terminals (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), (15,16), (17,18)

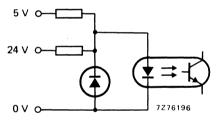


Fig. 2 Input circuit DB₀ to DB₇ and DBI.

All other inputs are connected to the CP10 and meet the standard TTL specification except the CLCO-input.

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

· 1	terminations (Fig. 4)	
load	connector 1	connector 2
1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a8 a10 a12 a14 a16 a18	
2 TTL	c15	
1 TTL	с5	
o 2 TTL	c26	
2 TTL 2 TTL	c16 c18	
*	a28	
	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 2 TTL 2 TTL 2 TTL 2 TTL 2 TTL	load connector 1 1 TTL

^{*} Input with relatively high input resistance (typ. 40 k Ω). CLCO-input, LOW level: max. 1 V; HIGH level: min. 2,4 V.

Output data

The enable outputs are $\overline{\text{EN}}_0$ to $\overline{\text{EN}}_{17}$; they are open-collector outputs.

Output voltage LOW, with respect to COMMON

at $\overline{IEN} = 80 \text{ mA}$

≤ 0,5 V

Output voltage HIGH

≤30 V

output	function	loada-	terminations (Fig. 4)	
		bility	connector 1	connector 2
LEX ₀ LEX ₁ LEX ₂ LEX ₃ LEX ₄ LEX ₅ LEX ₆ LEX ₇	Data outputs to be connected to LEX ₀ to LEX ₇ inputs of CP10.	10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL	a7 c7 a9 c9 a11 c11 a13 c13	
IDLC	Identification signal from the LX10 to the CP10. This connection forces a complete input/output cycle. This terminal is direct connected to 0 V on the LX10.		a25	

Time data

Time that a data source is enabled

when CP10 is used with non-extended

input/output cycle

t_{en} 58 μs

when CP10 is used with extended input/output cycle

t_{en} 14,8 ms

Time that data have to be present on DB₀ to DB₇

before end of enable signal

with non-extended input/output cycle with extended input/output cycle

t_{ds} 12 μs

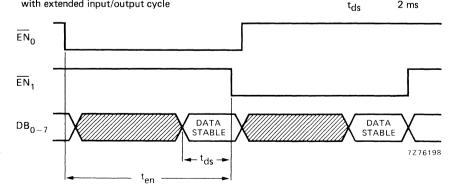


Fig. 3.

MECHANICAL DATA Outlines

Dimensions in mm

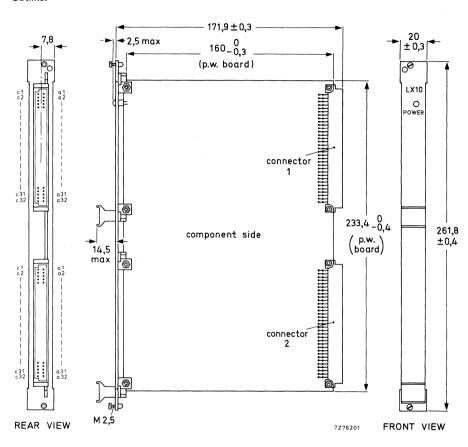


Fig. 4.

Mass

270 g

Terminal location

	connector 1			connector 2			
ro	ow c		row a	row c			row a
n.	.c.	1	n.c.	, , n (DBO	1	DB ₀ (5 V)
n.	.c.	2	n.c.	(note 4)	DB_0	2	DB ₀ (24 V)
n.	.c.	3	n.c.		DB ₁	3	DB ₁ !
n.	.c.	4	n.c.	(note 4)	DB ₁	4	DB ₁
M	IICC	5	n.c.	, . a j	DB ₂	5	DB ₂
n.	.c.	6	n.c.	(note 4)	DB_2	6	DB ₂
L	EX ₁	7	LEX ₀		DB3	7	DB ₃
		8	ABCIO ₃	(note 4)	DB_3	8	DB ₃
L	EX ₃	9	LEX ₂	(note 4) { } { } { } { } { } { } { } { } { } { }	DB₄	9	DB ₄
		10	ABCĨO₄		DB₄	10	DB ₄
L	EX ₅	11	LEX4	(DB ₅	11	DB ₅
		12	ABCIO ₅	(note 4)	DB5	12	DB ₅
L	EX ₇	13	LEX ₆	1 . 1	DB ₆	13	DB ₆
		14	ABCĬO ₆	(note 4)	DB ₆ DB ₆	14	DB ₆
L	DCP	15	n.c.	1	DB ₇	15	DB ₇
M	\overline{IID}_3	16	ABCIO ₇	(note 4)	DB ₇	16	DB ₇
n.	.c.	17	n.c.	(note 4) {	DBÍ	17	DBÍ (5 V)
M	IID ₄	18	ABCIO ₈	(note 4)	DBI	18	DBI (24 V)
n.	.c.	19	n.c.		n.c.	19	n.c.
0	V (note 1)	20	n.c.		ĒN _O	20	EN ₁
n.	.c.	21	n.c.		EN ₂	21	EN ₃
0	V (note 1)	22	n.c.		EN ₄	22	EN ₅
n.	.c.	23	n.c.		EN ₆	23	EN ₇
n.	.c.	24	n.c.		EN ₁₀	24	EN ₁₁
n.	.c.	25	IDLC		EN ₁₂	25	EN ₁₃
M	IIN :	26	n.c.		EN ₁₄	26	EN ₁₅
n.	.c.	27	n.c.		EN ₁₆	27	EN ₁₇
0	V (note 2)	28	CLCO		n.c.	28	n.c.
n.	.c.	29	n.c.		n.c.	29	n.c.
n.		30	n.c.	ſ	24 V	30	24 V
		31	5 V (note 3)	(note 5)	5 V	31	5 V (note 5)
(110te 3) (0	V	32	0 V \ (Hote 3)	l	COMMON	32	COMMON

n.c. = not connected

- 1. No supply line; only to be used for coding of the $\overline{\text{MID}}_{3,4}$ lines. 2. No supply line; only to be used as a ground connection for CLCO.
- 3. Logic supply.
- 4. Interconnected.
- 5. Enable output drive.



MEMORY MODULE

DESCRIPTION

This memory module is intended for use in combination with the central processor CP10 (or CP11), input module IM10,output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The control program is stored in the memory module.

The memory module is a random access magnetic core memory system with a basic capacity of 1024 words of 13 bits (1 k l3) and a cycle time of 1 μ s. The memory is complete in itself; it consists of a 3 D, 3-wire stack, timing selecting and inhibit circuitry, address and data registers, and a memory retention circuit including the 5 V sensing.

The memory module is built on three epoxy-glass printed-wiring boards. The module is provided with two F068-I connectors (board parts, Euro-card system); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) 1).

ELECTRICAL DATA

Supply

Supply voltage (d.c.) $V_P = 5 \ V \pm 5\%$ current (cycle time 1, 8 $\mu s)$ $I_P = 0$ operating max. 5, 1 A $typ. \quad 4 \ A$ standby max. 3, 6 A $typ. \quad 3, 3 \ A$

Note: The memory is in standby position when ENCM is LOW.

Cooling

An air velocity of 0,2 m/s is required.

For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminatio	ons (Fig. 3) connector 2
CICM	Cycle initiate signal from central processor	1 TTL		a19, c19
CICM	to program memory (bipolar to reduce noise sensitivity).	1 TTL		a18, c18
SCCM	Store command from central processor; determines read/restore and clear/write cycle.	2 TTL		a17, c17
ABCM ₀ ABCM ₁ ABCM ₂ ABCM ₃ ABCM ₄ ABCM ₅ ABCM ₆ ABCM ₆ ABCM ₇ ABCM ₈ ABCM ₉	Address bits from central processor.	2 TTL 2 TTL		a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28 a29, c29
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable signal from central processor to select one out of four memory modules.	3 TTL 3 TTL 3 TTL 3 TTL	a1 a2 a3 a4	
PBPM ₀ PBPM ₁ PBPM ₂ PBPM ₃ PBPM ₄ PBPM ₅ PBPM ₆ PBPM ₇ PBPM ₈ PBPM ₉ PBPM ₁₀ PBPM ₁₁ PBPM ₁₁	Program word bits from programming unit.	1 TTL 1 TTL	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12	
ENPB	Enables outputs are enabled, when HIGH these outputs are disabled.	2 TTL	a6	

Output data

All outputs meet the standard TTL specifications.

output	function	loada-	terminatio	ns (Fig. 3)
output	Tunction	bility	connector 1	connector 2
PBMCP ₀ PBMCP ₁ PBMCP ₂ PBMCP ₃ PBMCP ₄ PBMCP ₅ PBMCP ₆ PBMCP ₇ PBMCP ₈ PBMCP ₉ PBMCP ₁₀ PBMCP ₁₁ PBMCP ₁₁	Program word bits from program memory to central processor and programming unit. Open collector output with pull-up resistor (3, 9 k Ω).	9 TTL 9 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7 a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13 a14, c14
PBMCP ₀ PBMCP ₁ PBMCP ₂ PBMCP ₃ PBMCP ₄ PBMCP ₅ PBMCP ₆ PBMCP ₇ PBMCP ₉ PBMCP ₁₀ PBMCP ₁₁	Inverted PBMCP ₀₋₁₂ enabled by ENPB (three-state outputs).	10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL 10TTL	c17 c18 c19 c20 c21 c22 c23 c24 c25 c26 c27 c28	
DA	Data available signal. This signal becomes LOW max. 150 ns after CICM (or $\overline{\text{CICM}}$), and goes HIGH as soon as the data become available at the outputs (max. 500 ns after CICM or $\overline{\text{CICM}}$). Open collector output with pull-up resistor (3,9 k Ω).	9 TTL		a16, c16

March 1977

Time data

The relationship between the different input and output signals are given when the memory module is operating in a programmable logic controller system.

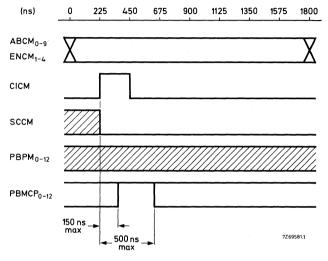


Fig. 1. Timing of read/restore mode.

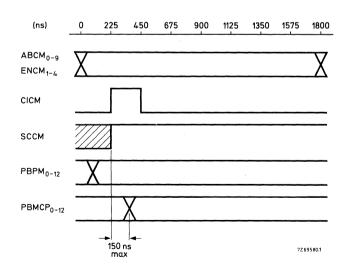


Fig. 2. Timing of clear/write mode.

MM10

MECHANICAL DATA

Dimensions in mm

Outlines

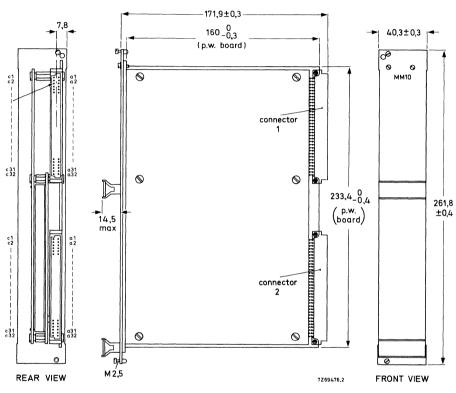


Fig. 3

Mass

780 g

Terminal location

connector 1

row c		row a
$PBPM_0$	1	ENCM ₁
PBPM ₁	2	$ENCM_2$
PBPM ₂	3	ENCM ₃
PBPM3	4	$ENCM_4$
PBPM ₄	5	n.c.
PBPM ₅	6	ENPB
PBPM ₆	7	n.c.
PBPM ₇	8	n.c.
PBPM ₈	9	n.c.
PBPM ₉	10	n.c.
$PBPM_{10}$	11	n.c.
PBPM ₁₁	12	n.c.
PBPM ₁₂	13	n.c.
n.c.	14	n.c.
n.c.	15	n.c.
n.c.	16	n.c.
$PBMCP_0$	17	n.c.
PBMCP ₁	18	n.c.
PBMCP ₂	19	n.c.
PBMCP ₃	20	n.c.
$PBMCP_4$	21	n.c.
PBMCP ₅	22	n.c.
PBMCP ₆	23	n.c.
PBMCP ₇	24	n.c.
PBMCP ₈	25	n.c.
PBMCP ₉	26	n.c.
\underline{PBMCP}_{10}	27	n.c.
PBMCP ₁₁	28	n.c.
\overline{PBMCP}_{12}	29	n.c.
n.c.	30	n.c.
v_P	31	v_P
0 V	32	0 V

n.c. = not connected.

i.c. = internal connection.

connector 2

row c		row a
n.c.	1	n.c.
$PBMCP_0$	2	PBMCP0
PBMCP ₁	3	PBMCP ₁
PBMCP ₂	4	PBMCP ₂
PBMCP3	5	$PBMCP_3$
PBMCP ₄	6	PBMCP ₄
PBMCP ₅	7	PBMCP ₅
PBM€P ₆	8	PBMCP ₆
PBMCP ₇	9	PBMCP ₇
PBMCP ₈	10	PBMCP ₈
PBMCP9	11	PBMCP ₉
PBMCP ₁₀	12	$PBMCP_{10}$
PBMCP ₁₁	13	$PBMCP_{11}$
PBMCP ₁₂	14	PBMCP ₁₂
i.c.	15	i.c.
DA	16	DA
SCCM	17	SCCM
CICM	18	CICM
CICM	19	CICM
$ABCM_0$	20	$ABCM_0$
$ABCM_1$	21	$ABCM_1$
ABCM ₂	22	$ABCM_2$
ABCM ₃	23	ABCM3
ABCM ₄	24	$ABCM_4$
$ABCM_5$	25	ABCM ₅
ABCM ₆	26	ABCM ₆
ABCM ₇	27	ABCM ₇
ABCM ₈	28	ABCM ₈
ABCM ₉	29	ABCM9
i.c.	30	i.c.
v_P	31	v_P
0 V	32	0 V

MEMORY MODULE

DESCRIPTION

The memory module MM11 is intended for use in the PLC system as a program memory or as an auxiliary unit for programming EPROMs (2708); see also Remark below. It contains 4 IC sockets in which 4 UV-erasable EPROMs can be plugged. The MM11 also contains an address buffer, output buffers, and 3 d.c./d.c. converters (5 V to 12 V, 5 V to -5 V and 5 V to 27 V).

The MM11 has three operation modes which can be selected by two mode-selection inputs MSI₁ and MSI₂ (see also truth table under "Input data"):

- Read mode (RD): the module can be used as a read only memory (ROM), that is the situation when the module is used in an operating PLC system.
- Write into master mode (WIM): data from MM10, MM11 or MM12* can program the EPROMs in the IC sockets.
- Write into RAM mode (WIR): the contents of the EPROMs on the MM11 can be written into an MM10*.

The last two modes will be started after pressing a push button, to be connected between terminal 24a of connector 1 and 0 V, or by applying a LOW level to that terminal.

When the MM11 is in the WIM mode the data flow will be as follows:

- the MM11 sends an address (ABCM₀ to ABCM₉), an enable signal (ENCM₁ or ENCM₂) and a cycle initiate signal (CICM/CICM) to the data source which may be an MM10, MM11 or MM12 (the MM12 does not need a CICM signal);
- the data source will send the data to be programmed into the EPROMs on the MM11.

When the MM11 is in the WIR mode the data flow will be:

- the MM11 sends an address (ABCM₀ to ABCM₉), an enable signal (ENCM₁ or ENCM₂), a cycle initiate signal (CICM/CICM) and a store command to the MM10;
- data from MM11 will go via PBPM0 to PBPM12 to the MM10 and be stored into the MM10.

The MM11 has a capacity of 1k13 or 2k13 depending on whether there are 2 or 4 EPROMs on the module.

The enable input ENCM₁ or ENCM₃ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input ENCM₂ or ENCM₄ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

The MM11 is supplied with two empty EPROMs 2708.

Remark

Correct programming of EPROMs is only guaranteed, when completely erased EPROMs are used; for the correct erase procedure consult the relevant data sheet of the 2708 EPROMs.

* The connections between these modules have to be done in a separate module set-up, outside the system. No special programming apparatus is required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

V_P 5 V ± 5%

____ max. 2,4 A

Supply current

lp max. 2,4 A typ. 2 A

Remark

There are several terminals on the connectors which act as inputs or outputs depending on the mode in which the MM11 is operating (see below). These terminals are described under "Input data" and "Output data".

-	operation mode				
terminal	WIM	WIR	RD		
CICM/CICM	output	output	input		
ENCM ₁ to ENCM ₄	output	output	input		
ABCM ₀ to ABCM ₉	output	output	input		
PBMCP ₀ to PBMCP ₁₂	input	output	output		

Input data

All inputs meet the standard TTL specifications.

innut	function	lood	terminations (Fig.1)		
input	lunction	load	connector 1	connector 2	
ABCM0 ABCM1 ABCM2 ABCM3 ABCM4 ABCM5 ABCM6 ABCM7 ABCM8 ABCM9	Address inputs (RD mode).	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL		a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28 a29, c29	
CICM	Cycle initiate signal; bipolar to reduce noise sensitivity (RD mode).	2 TTL 2 TTL		a19, c19 a18, c18	
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable inputs; memory is enabled when ENCM is HIGH (RD mode).	2 TTL 2 TTL 2 TTL 2 TTL	a1 a2 a3 a4		
PBMCP ₀ PBMCP ₁ PBMCP ₂ PBMCP ₃ PBMCP ₄ PBMCP ₅	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7	

input	function	load	terminations (Fig.1)		
put	Tunction	load	connector 1	connector 2	
РВМСР6		1 TTL		a8, c8	
PBMCP ₇		1 TTL		a9, c9	
PBMCP8	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL		a10, c10	
PBMCP9		1 TTL		a11, c11	
PBMCP ₁₀		1 TTL		a12, c12	
PBMCP ₁₁		1TTL		a13, c13	
PBMCP ₁₂		1 TTL		a14, c14	
START	Input to start the WIM or the WIR mode (active LOW).	2 TTL	a24		
REST	Input to restart the stopped WIM or WIR mode (active LOW)	1 TTL	a19		
INH	Inhibit and stop input; when LOW the start input is inoperative.	2 TTL	a 2 5		
MSI ₁ MSI ₂	Mode selection inputs.	6 TTL 6 TTL	a26 a27		

Operation mode truth table

mode	mode selection inputs				
	MSI ₁	MSI ₂			
RD	HIGH	HIGH			
	(floating)	(floating)			
WIM	active LOW	arbitrary level			
WIR	HIGH	active LOW			
WIL	(floating)	active LOW			

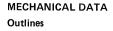
Output data

All outputs meet the standard TTL specifications.

Output	function	loada-	terminations (Fig.1)		
output	lunction	bility	connector 1	connector 2	
PBMCP ₀		10 TTL		a2, c2	
PBMCP ₁		10 TTL		a3, c3	
PBMCP2		10 TTL		a4, c4	
PBMCP3		10 TTL		a5, c5	
PBMCP4		10 TTL		a6, c6	
PBMCP ₅	Drogram word hits to control avecage	10 TTL		a7, c7	
PBMCP6	Program word bits to central processor (RD mode) or MM10 (WIR mode).	10 TTL		a8, c8	
PBMCP ₇	(ND mode) of wild to (with mode).	10 TTL	·	a9, c9	
PBMCP ₈		10 TTL		a10, c10	
PBMCPg		10 TTL		a11, c11	
PBMCP ₁₀		10 TTL		a12, c12	
PBMCP11		10 TTL		a13, c13	
PBMCP ₁₂	·	10 TTL		a14, c14	
ABCMo		10 TTL		a20, c20	
ABCM ₁		10 TTL		a21, c21	
ABCM ₂	·	10 TTL		a22, c22	
ABCM ₃		10 TTL		a23, c23	
ABCM₄	Address bits to MM10, MM11 or MM12	10 TTL		a24, c24	
ABCM5	(WIM mode) or to MM10 (WIR mode).	10 TTL		a25, c25	
ABCM ₆	(10 TTL		a26, c26	
ABCM ₇		10 TTL		a27, c27	
ABCMg		10 TTL		a28, c28	
ABCMg		10 TTL		a29, c29	
CICM	Cycle initiate signal to MM10 or MM11	9 TTL		a19, c19	
CICM	(WIM mode) or to MM10 (WIR mode).	9 TTL		a18, c18	
SCCM	Read-write output (three-state) to MM10. The output is LOW in the WIM mode, HIGH in the WIR mode, floating in the RD mode.	10 TTL		a17, c17	
ENCM ₁		9 TTL	a1		
ENCM ₂	Enable signal to MM10, MM11 or	9 TTL	a2		
ENCM3	MM12 (WIM mode) or to MM10 (WIR mode).	9 TTL	a3		
ENCM ₄	,	9 TTL	a 4		
PRB	Program busy output signal to external equipment. When LOW it indicates that WIM mode or WIR mode is active and becomes HIGH as soon as these actions are finished.	10 TTL	a23		

output	function	loada-	terminations (Fig.1)		
output	Tunction	bility	connector 1	connector 2	
PBPM _O		10 TTL	c1		
PBPM ₁		10 TTL	c2		
PBPM ₂		10 TTL	c3		
PBPM3		10 TTL	c4		
PBPM ₄		10 TTL	c5		
PBPM ₅		10 TTL	c6		
PBPM ₆	Program word bits to MM10 (WIR mode).	10 TTL	c7		
PBPM ₇	These three-state outputs are only	10 TTL	c8		
PBPM ₈	active in the WIR mode.	10 TTL	c9		
PBPM ₉		10 TTL	c10		
PBPM ₁₀		10 TTL	c11		
PBPM11		10 TTL	c12		
PBPM ₁₂		10 TTL	c13		

PBPM ₁₂	10 TTL	c13		
Time data				
RD mode				
Time between leading edges of CICM/CICM and data valid \mbox{PBMCP}_o to \mbox{PBMCP}_{12}			max.	550 ns
Time between address changes on ABCM0 to ABCM9 and leading edges of CICM/ $\overline{\text{CICM}}$			min.	0 ns
WIM mode				
Time to program 1k or 2k EPROM memory			max. typ.	18 min 15 min
WIR mode				
Time to read-out MM11 and store into MM10			max. typ.	4,2 s 3,5 s



Dimensions in mm

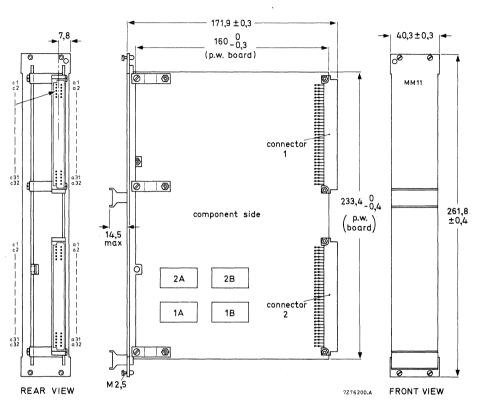


Fig.1.

Mass

350 g

Terminal location

Co	onnector 1		со	nnector 2	
row c		row a	row c		row a
PBPM _O	1	ENCM ₁	n.c.	1	n.c.
PBPM ₁	2	ENCM ₂	PBMCPO	2	PBMCP ₀ (O _{5A} *)
PBPM2	3	ENCM3	PBMCP ₁	3	PBMCP ₁ (O _{6A})
PBPM3	4	ENCM ₄	PBMCP2	4	PBMCP ₂ (O _{7A})
PBPM ₄	5	n.c.	PBMCP3	5	PBMCP3 (O8A)
PBPM ₅	6	n.c.	PBMCP ₄	6	PBMCP ₄ (O _{1B})
PBPM ₆	7	n.c.	PBMCP ₅	7	PBMCP ₅ (O _{2B})
PBPM ₇	8	n.c.	PBMCP6	8	PBMCP ₆ (O_{3B})
PBPM ₈	9	n.c.	PBMCP ₇	9	PBMCP ₇ (O _{5B})
PBPM ₉	10	n.c.	PBMCP8	10	PBMCP8 (O6B)
PBPM ₁₀	11	n.c.	PBMCP9	11	PBMCP ₉ (O _{7B})
PBPM ₁₁	12	n.c.	PBMCP ₁₀	12	PBMCP ₁₀ (O _{1A})
PBPM ₁₂	13	n.c.	PBMCP ₁₁	13	PBMCP ₁₁ (O _{2A})
n.c.	14	n.c.	PBMCP ₁₂	14	PBMCP ₁₂ (O _{3A})
n.c.	15	n.c.	n.c.	15	n.c.
n.c.	16	n.c.	n.c.	16	n.c.
n.c.	17	n.c.	SCCM	17	SCCM
n.c.	18	n.c.	CICM	18	CICM
n.c.	19	REST	CICM	19	CICM
n.c.	20	n.c.	ABCM ₀	20	ABCM ₀
n.c.	21	n.c.	ABCM ₁	21	ABCM ₁
n.c.	22	n.c.	ABCM ₂	22	ABCM ₂
n.c.	23	PRB	ABCM ₃	23	ABCM ₃
n.c.	24	START	ABCM ₄	24	ABCM ₄
n.c.	25	INH	ABCM ₅	25	ABCM ₅
n.c.	26	MSI ₁	ABCM ₆	26	ABCM ₆
n.c.	27	MSI ₂	ABCM ₇	27	ABCM ₇
n.c.	28	n.c.	ABCM ₈	28	ABCM ₈
n.c.	29	n.c.	ABCM ₉	29	ABCM ₉
n.c.	30	n.c.	n.c.	30	n.c.
VP	31	VP	Vp	31	V _P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

^{*} Corresponding output number of EPROM.

MEMORY MODULE

DESCRIPTION

The memory module MM12 is intended for use in the PLC system as a program memory. It contains 4 IC sockets in which 4 UV-erasable PROMs (2708) can be plugged. The MM12 also contains 10 buffered address inputs, 4 enable inputs, 16 buffered outputs and 2 d.c./d.c. converters (5 V to 12 V and 5 V to -5 V).

The MM12 has a capacity of 2k16. Although the PLC system operates with program words of 13 bits, the remaining 3 bits are also brought out (Q_{4A}, Q_{4B}, Q_{8B}) , so that the module can be used in other applications which require 16 bits.

The enable input ENCM₁ or ENCM₃ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input ENCM₂ or ENCM₄ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

Programming of the EPROMs cannot be done on the MM12: this has to be done on the MM11or by existing programming equipment.

The MM12 is supplied with two empty EPROMs 2708.

ELECTRICAL DATA

Supply

Supply current

Supply voltage (d.c.)

 V_P 5 V \pm 5%

max. 1,2 A

typ. 1 A

Input data

All inputs meet the standard TTL specifications.

input	out function		terminations	(Fig. 2)
		-	connector 1	connector 2
ABCM ₀ ABCM ₁ ABCM ₂ ABCM ₃ ABCM ₄ ABCM ₅ ABCM ₆ ABCM ₇ ABCM ₈ ABCM ₉	Address bits from central processor	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL		a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28 a29, c29
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable inputs from central processor	1 TTL 1 TTL 1 TTL 1 TTL	a1 a2 a3 a4	

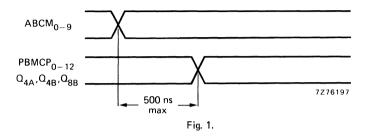
Output data

All outputs are three-state outputs and meet the standard TTL specifications.

output	function	loada-	terminations	s (Fig. 2)
		bility	connector 1	connector 2
PBMCP0 PBMCP1 PBMCP2 PBMCP3 PBMCP4 PBMCP5 PBMCP6 PBMCP7 PBMCP8 PBMCP9 PBMCP10 PBMCP11 PBMCP12	Program word bits from memory module to central processor	10 TTL 10 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7 a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13 a14, c14
0 _{4A}	Buffered output from output O4 of EPROM A.	10 TTL		a1, c1
Q _{4B}	Buffered output from output O4 of EPROM B.	10 TTL		a15, c15
Q _{8B}	Buffered output from output O8 of EPROM B.	10 TTL		a16, c16

Time data

The relationship between the different input and output signals are given when the memory module is operating in the PLC system.



MECHANICAL DATA Outlines

Dimensions in mm

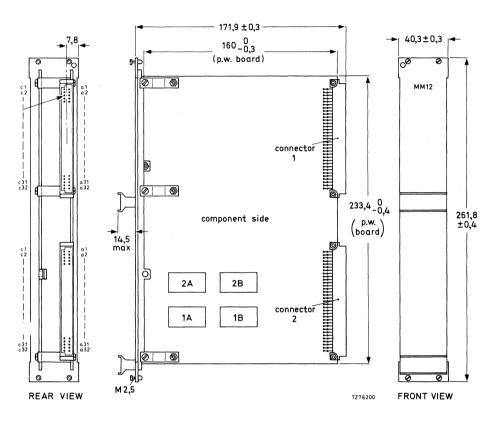


Fig. 2.

Mass

290 g

Terminal location

cor	nector 1		cor	nnector 2	
row c		row a	row c		row a
n.c.	1	ENCM ₁	Q _{4A}	1	Q _{4A} (O _{4A} *)
n.c.	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀ (O _{5A})
n.c.	3	ENCM3	PBMCP ₁	3	PBMCP ₁ (O _{6A})
n.c.	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂ (O _{7A})
n.c.	5	n.c.	PBMCP ₃	5	PBMCP3(O8A)
n.c.	6	n.c.	PBMCP ₄	6	PBMCP ₄ (O _{1B})
n.c.	7	n.c.	PBMCP ₅	7	PBMCP ₅ (O _{2B})
n.c.	8	n.c.	PBMCP ₆	8	PBMCP ₆ (O _{3B})
n.c.	9	n.c.	PBMCP ₇	9	PBMCP ₇ (O _{5B})
n.c.	10	n.c.	PBMCP8	10	PBMCP8(O6B)
n.c.	11	n.c.	PBMCP ₉	11	PBMCP ₉ (O _{7B})
n.c.	12	n.c.	PBMCP ₁₀	12	PBMCP ₁₀ (O _{1A})
n.c.	13	n.c.	PBMCP ₁₁	13	PBMCP ₁₁ (O _{2A})
n.c.	14	n.c.	PBMCP ₁₂	14	PBMCP ₁₂ (O _{3A})
n.c.	15	n.c.	0 _{4B}	15	$Q_{4B}(Q_{4B})$
n.c.	16	n.c.	Ω _{8B}	16	O _{8B} (O _{8B})
n.c.	17	n.c.	n.c.	17	n.c.
n.c.	18	n.c.	n.c.	18	n.c.
n.c.	19	n.c.	n.c.	19	n.c.
n.c.	20	n.c.	ABCM ₀	20	ABCM ₀
n.c.	21	n.c.	ABCM ₁	21	ABCM ₁
n.c.	22	n.c.	ABCM ₂	22	ABCM ₂
n.c.	23	n.c.	ABCM ₃	23	ABCM ₃
n.c.	24	n.c.	ABCM ₄	24	ABCM ₄
n.c.	25	n.c.	ABCM ₅	25	ABCM ₅
n.c.	26	n.c.	ABCM ₆	26	ABCM ₆
n.c.	27	n.c.	ABCM ₇	27	ABCM ₇
n.c.	28	n.c.	ABCM ₈	28	ABCM ₈
n.c.	29	n.c.	ABCM ₉	29	ABCM ₉
n.c.	30	n.c.	n.c.	30	n.c.
V_{P}	31	V_{P}	V _P	31	V _P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

^{*} Corresponding output number of EPROM.



OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 16 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other.

Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

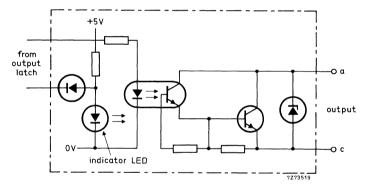


Fig. 1. Circuit diagram of an output stage.

The output module has nine address inputs (ABCIO $_{0-8}$) and five module identification inputs ($\overline{\mathrm{MID}}_{0-4}$), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card sytem). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89291 (pins for wire wrap), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags) 1).

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¹⁾ For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.

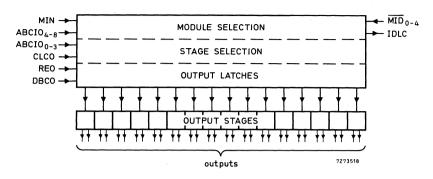


Fig. 2. Block diagram of the output module.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

 v_{P}

5 V ± 5%

current

ΙP

max. 1 A (all stages "ON")

typ. 0,75 A (8 stages "ON", 8 stages "OFF")

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig. 3)
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits from central processor; ABCIO ₀₋₃ select the output stage, ABCIO ₄₋₈ select the output module.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a2, c2 a4, c4 a6, c6 a8, c8 a10 a12 a14 a16 a18
DBCO	Data bit from central processor; data is stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\frac{\overline{\text{MID}_0}}{\overline{\text{MID}_1}}$ $\frac{\overline{\text{MID}_2}}{\overline{\text{MID}_3}}$ $\overline{\text{MID}_4}$	Module identification inputs; provide module with individual identity.	2 TTL 2 TTL 2 TTL 2 TTL 2 TTL 2 TTL	c10 c12 c14 c16 c18
CLCO*	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

^{*)} Input with relatively high input resistance (typ. 40 kΩ). CLCO-input, LOW level:max. 1 V:

HIGH level: min. 2,4 V.

Output data

The data outputs are DOXY0 to DOXY7 and DOXZ0 to DOXZ7. They are accessible on connector 2, see "Terminal location".

Output transistor conducting : output current = max. 100 mA at V_{a-c}^{-1}) = max. 1,5 V Output transistor non-conducting: output current = max. 10 μ A at V_{a-c}^{-1}) = max. 30 V

Each data output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H.

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¹⁾ Voltage between terminal of row a and terminal of row c of connector 2.

The output (open collector) below meets the standard TTL specifications.

output	function	loada- bility	terminations of connector 1 (Fig. 3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

MECHANICAL DATA

Dimensions in mm

Outlines

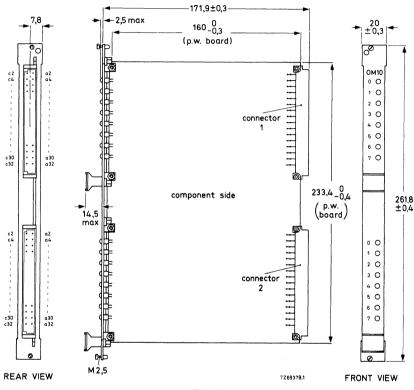


Fig. 3

Mass

230 g

Terminal location

					-
С	:on	ıne	CI	or	1

connector 1		r l		con	nector	2
row c		row a		row c		row a
ABCIO ₀	2	ABCIO ₀		DO_{XY0}	2	DO_{XY0}
ABCIO ₁	4	ABCIO ₁		DO_{XY1}	4	DO_{XY1}
ABCIO ₂	6	ABCIO ₂		DO_{XY2}	6	DO_{XY2}
ABCIO3	8	$ABCIO_3$		DO_{XY3}	8	DO_{XY3}^{X12}
$\overline{\mathrm{MID}_0}$	10	ABCIO ₄		DO_{XY4}	10	DO_{XY4}^{X10}
$\overline{\mathrm{MID}_1}$	12	ABCIO5		DO_{XY5}	12	DO_{XY5}
$\overline{\mathrm{MID}_2}$	14	ABCIO ₆		DOXY6	14	DO_{XY6}
$\overline{\mathrm{MID_3}}$	16	ABCIO ₇		DO_{XY7}	16	DOXY7
$\overline{\mathrm{MID_4}}$	18	ABCIO ₈		DO_{XZ0}	18	DO_{XZ0}
$0V^{1}$	20	n.c.		DO_{XZ1}	20	DO_{XZ1}^{XZ0}
$0V^{1}$)	22	DBCO		DO_{XZ2}	22	DO _{XZ2}
n.c.	24	REO		DO_{XZ3}	24	DO_{XZ3}
MIN	26	IDLC		DO_{XZ4}	26	DOXZ4
0V ²)	28	CLCO		DO_{XZ5}	28	DO_{XZ5}
v_p	30	v_p		DO_{XZ6}	30	DO _{XZ6}
0V	32	0 V		DO_{XZ7}	32	DO _{XZ7}

n.c. = not connected.

 $[\]overline{}^{1}$) No supply line; only to be used for coding of the $\overline{\text{MID}}_{0\text{-}4}$ lines.

 $^{^{2}}$) No supply line; only to be used as a ground connection for CLCO.

OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 8 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are open-collector outputs. Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages feature electronic short-circuit protection which can only be de-activated by resetting the input signal. Short-circuit indication is provided by the lower row of LEDs on the front panel. If the status indicator LED and the short-circuit indicator LED with the same number are both lit, these output stages are working correctly. If the former LED is lit and the latter extinguished, this will indicate a short-circuit condition.

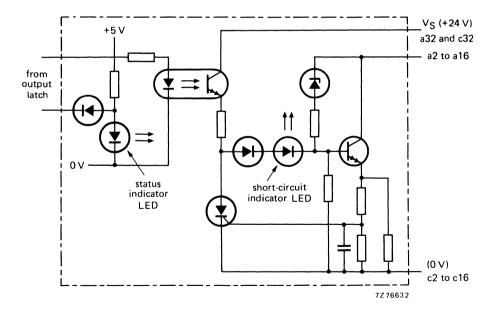


Fig. 1 Circuit diagram of an output stage.

The output module has 9 address inputs (ABCIO₀₋₈) and 5 module identification inputs ($\overline{\text{MID}}_{0-4}$) at the rear, for selecting 16 addresses. Because 8 are used as output stages (with even second digit e.g. 162), the remaining 8 addresses can be used as internal places (with odd second digit e.g. 172),

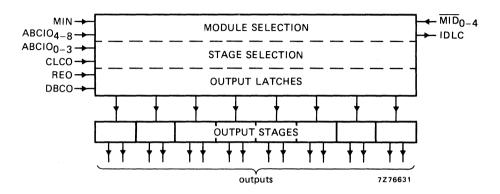


Fig.2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts), the corresponding panel parts are available too, but should be ordered additionally: 2422 025 89291 (with wire-wrap pins), 2422 025 89299 (with dip-solder pins), or 2422 025 89327 (with solder tags). For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

typ 0,1 A

Is

ELECTRICAL DATA

load current)

Supply

ombb.)			
Supply voltage (d.c.)		V_{P}	5 V ± 5 %
Supply current	logic	Iр	typ 0,75 A
Supply voltage (d.c.)	for	٧s	24 V ± 25%
Supply current (excluding	Cutnut		

circuitry

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig.3)
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	address bits from central processor; ABCIO ₀₋₃ select the output stage, ABCIO ₄₋₈ select the output module.	1TTL 1TTL 1TTL 1TTL 1TTL 1TTL 1TTL 1TTL	a2, c2 a4, c4 a6, c6 a8, c8 a10 a12 a14 a16 a18
DBCO	Data bit from central processor; data are stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\frac{\overline{\text{MID}}_0}{\overline{\text{MID}}_1}$ $\overline{\overline{\text{MID}}_2}$ $\overline{\overline{\text{MID}}_3}$ $\overline{\overline{\text{MID}}_4}$	Module identification inputs; provide module with individual identity.	2 TTL 2 TTL 2 TTL 2 TTL 2 TTL 2 TTL	c10 c12 c14 c16 c18
CLCO *	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

^{*} Input with relatively high input resistance (typical 40 k Ω). CLCO-input: LOW level, maximum 1 V; HIGH level, minimum 2,4 V.

Output data

Table 1

The data outputs are DO_{XY0} to DO_{XY7} (Y is always even). They are accessible on connector 2, see terminal location.

Output transistor conducting: V_{a-c} * = max.2,53 V at output current (I_O) is 2 A.

Output transistor non-conducting: $I_O = \text{max. } 10 \,\mu\text{A}$ at V_{a-C} * is 30 V.

Maximum load inductance (Lmax)

see Table 1

Maximum switching frequency at maximum

see Table 2

output current (I_{Omax})

Table 2

I _O	L _{max} mH
2,0	50
1,8	60
1,6	80
1,4	100
1,2	140
1,0	200
0,8	310
0,6	560
0,4	1300
0,2	5000
0,1	20000

max. switching frequency Hz
3
2
1
0,5

Output current at operation with forced air cooling of 1 m/s, for all stages

max. 2 A per stage

Output current at operation without forced air cooling

for all stages

max. 0,915 A per stage max. 2 A per stage

for maximum 4 stages

Short-circuit protection trip level

2,16 A

The output (open collector) meets the standard TTL specifications

output	function	loadability	terminations of connector 1 (Fig.3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Dimensions in mm

Outlines

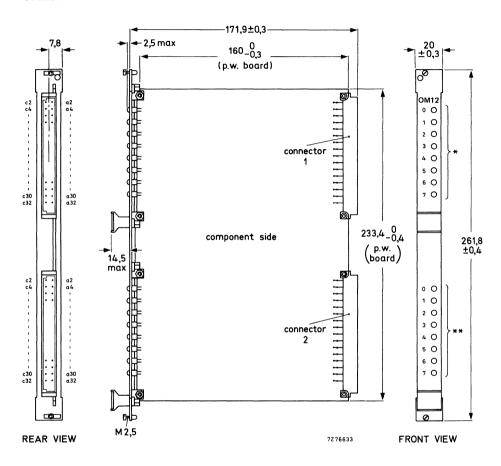


Fig.3 The LEDs identified with * are for status indication, those identified with ** are for short-circuit indication.

Mass

260 g

Terminal location

connector 1			connector 2			
row c		row a	row c		row a	
ABCIO ₀	2	ABCIO ₀	0 V)	2	DO _{XY0}	
ABCIO ₁	4	ABCIO ₁	0 V	4	DOXY1	
ABCIO ₂	6	ABCIO ₂	0 V	6	DOXY2	
ABCIO3	8	ABCIO3	0 / / / / / / / / / / / / / / / / / / /	_{40.3} / ₈	DOXY3	
\overline{MID}_{O}	10	ABCIO ₄	0 V (''''	te 3) 10	DO_{XY4}	
\overline{MID}_1	12	ABCIO ₅	0 V	12	DO_{XY5}	
MID ₂	14	ABCIO ₆	0 V	14	DOXY6	
$\overline{\text{MID}}_3$	16	ABCIO ₇	0 V	16	DOXY7	
MID ₄	18	ABCIO ₈	i.c.	18	i.c.	
0 V (note 1)	20	n.c.	i.c.	20	i.c.	
0 V (note 1)	22	DBCO	i.c.	22	i.c.	
n.c.	24	REO	n.c.	24	n.c.	
MIN	26	IDLC	i.c.	26	n.c.	
0 V (note 2)	28	CLCO	n.c.	28	n.c.	
V _p	30	V_p	n.c.	30	n.c.	
0 V	32	0 آ	v_S	32	v_S	

n.c. = not connected.

i.c. = internally connected.

Notes

- No supply line; only to be used for coding of the MID₀₋₄ lines.
 No supply line; only to be used as a ground connection for CLCO.
- 3. 0-line of Vs.

PUNCH AND TELETYPE INTERFACE MODULE

DESCRIPTION

This punch and teletype interface module is intended for use in a PLC system to enable the user to make a hard copy of the program.

For this purpose, the CP10 or CP11 central processor module must be replaced by the PI10 in the operating PLC system. Connections to the hard copy equipment can de done via two F161 connectors in the front panel. The upper (connector 4, female, 25 pins) is for the TTY which supplies data in a serial form including start and stop bits according to standard RS232C. The lower (connector 3, female, 15 pins) is for the punch which supplies data in a parallel form (TTL-level). Both data are in ASCII code including parity-bit. The module is also provided with "start" and "reset" pushbuttons and a "ready" indication. The latter is ON as soon as the power supply is switched-on. When "start" is pushed it extinguishes and relights as soon as the read-out has been completed or when "reset" is pushed.

Data output is approx. 9 characters per second, adjusted for normal TTY operation. If higher speeds are required, e.g. for a fast punch, a resistor Rp can be inserted between two solder-pins on the board, marked "a" and "b" (see Fig. 3; maximum 29 characters/s possible).

The punch and teletype interface module is built on an epoxy glass printed-wiring board of 233,4 mm x 160 mm (Eurocard system). The board is provided with two F068-I connectors (board parts) to fit in the place of a CP10 or CP11.

ELECTRICAL DATA

Supply

Voltage (d.c.) Current V_P 5 V ± 5% I_P typ. 1,5 A

Input data

All inputs meet the standard TTL-specifications.

input	function	load	terminations (Fig. 5)		
			connector 1	connector 2	
PBMCP0 PBMCP1 PBMCP2 PBMCP3 PBMCP4 PBMCP5 PBMCP6 PBMCP7 PBMCP8 PBMCP9 PBMCP10 PBMCP11 PBMCP11	Program word bits from program memory.	1 TTL 1 TTL 1 TTL 2 TTL 1 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7 a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13 a14, c14	
MICC	Memory identification signal; this signal is connected to one of the four ENCM-outputs of the central processor.	1 TTL	a5		

Output data

Outputs to PLC system (rear side).

All outputs meet the standard TTL specifications.

auitaut.	function	loada-	terminations (Fig. 5)		
output		bility	connector 1	connector 2	
ABCM ₀ ABCM ₁ ABCM ₂ ABCM ₃ ABCM ₄	Address bits to program memory.	9 TTL 9 TTL 9 TTL 9 TTL 9 TTL		a20, c20 a21, c21 a22, c22 a23, c23 a24, c24	
ABCM ₅ ABCM ₆ ABCM ₇ ABCM ₈ ABCM ₉		9 TTL 9 TTL 9 TTL 9 TTL 9 TTL		a25, c25 a26, c26 a27, c27 a28, c28 a29, c29	
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4k.	10 TTL 10 TTL 10 TTL 10 TTL	a1 a2 a3 a4		
SCCM	Store command to program memory. This terminal is directly connected to 0 V on punch/teletype interface, forcing the program memory into "read" operation.			a17, c17	
CICM	Cycle initiate signal to program memory (bipolar to reduce noise sensitivity).	10 TTL 9 TTL		a19, c19 a18, c18	

Output data (continued)

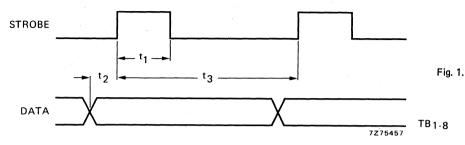
Outputs to hard copy equipment (front panel).

All outputs of connector 3 meet the standard TTL specifications. The output of connector 4 meets the standard RS232C specification.

		loada-	termination (Fig. 5)	
output	function	bility	connector 3	connector 4
TB ₁	Tape bits performing ASCII code.	10 TTL	1	
TB ₂		10 TTL	2	
TB3		10 TTL	3	
TB4		10 TTL	4	
TB ₅		10 TTL	5	
тв6		10 TTL	6	
TB ₇	Directly connected to 0 V.		7	
TB ₈	Parity bit *.	10 TTL	8	
STROBE	Chart simple to make (date on TD amodul)	10 TTL	9	
STROBE	Start signal to punch (data on TB ₁₋₈ ready).	10 TTL	10	
HIGH	Constant HIGH level (directly connected to Vp).		12	
0 V	Signal ground (directly connected to 0 V).		15	
DO	Data output (RS232C).			3
0 V	Signal ground (directly connected to 0 V).			7

^{*} When points "c" and "d" on the PC board are not interconnected (see Fig. 5), the module supplies an even parity. With a short-circuit bridge across these points an odd parity occurs.

TIME DATA Parallel output



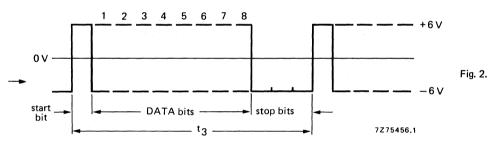
t₁ STROBE pulse duration

t₂ DATA valid before STROBE pulse

t₃ depending on R_P

2 ms \pm 20% min. 10 μ s 9 characters/s (Rp = ∞) 29 characters/s (Rp = $8 \text{ k}\Omega$)

Serial output



→ t₃ depending on R_P

approx. 9 characters/s ($R_P = \infty$)

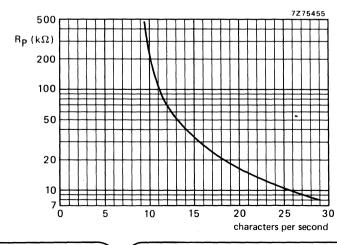


Fig. 3 Required R_p as a function of print/punch speed (number of characters per second).

APPLICATION INFORMATION

If the user wants to have only a part of the program dumped, he can preset the starting point by means of three switches on the PC board; see Figs 4 and 5. Termination of the read-out can be achieved by pressing the "reset" button.

start with	pre	set sv	vitch
line number	4	2	1
0000	L	L	L
1000	Ĺ	L	н
2000	L	Н	L
3000	L	Н	н
4000	Н	L	L
5000	Н	L	н
6000	Н	Н	L
7000	Н	Н	Н

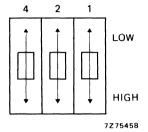


Fig. 4.

Punch format

After pressing the "start" button, the module will generate "tape feed" 56 times. Hereafter, the line number followed by "space", the program word, "enter", "step", "carriage return" and "line feed" will be punched. This cycle, consisting of 14 characters, is repeated, starting with the next line number. After the addresses 1777, 3777, 5777 and 7777, other sections of 56 times "tape-feed" will be inserted.

Teletype format

The same characters as mentioned above are sent to the TTY, producing the following print out:

	(line)	(space)	(program word)	(enter)	(step
e.g.	3271		1.401	>	<
	3272		*2.130	>	<
	3273		*0.740	>	<

MECHANICAL DATA
Outlines

Dimensions in mm

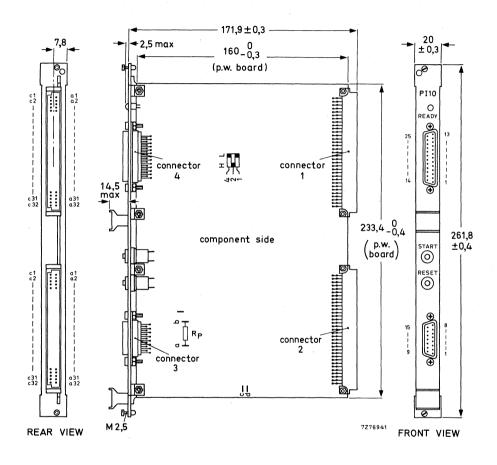


Fig. 5.

Mass

310 g

Terminal location

connector 1				
row c		row a		
n.c.	1	ENCM ₁		
n.c.		ENCM ₂		
n.c.	2 3	ENCM3		
n.c.	4	ENCM ₄		
n.c.	5	MICC		
n.c.	6	n.c.		
n.c.	7	n.c.		
n.c.	8	n.c.		
n.c.	9	n.c.		
n.c.	10	n.c.		
n.c.	11	n.c.		
n.c.	12	n.c.		
n.c.	13	n.c.		
n.c.	14	n.c.		
n.c.	15	n.c.		
n.c.	16	n.c.		
n.c.	17	n.c.		
n.c.	18	n.c.		
n.c.	19	n.c.		
n.c.	20	n.c.		
n.c.	21	n.c.		
n.c.	22	n.c.		
n.c.	23	n.c.		
n.c.	24	n.c.		
n.c.	25	n.c.		
n.c.	26	n.c.		
n.c.	27	n.c.		
n.c.	28	n.c.		
n.c.	29	n.c.		
n.c.	30	n.c.		
VP	31	VP		
0 V	32	0 V		

n.c. = not connected

connector 2

row c		row a
n.c.	1	n.c.
PBMCPo	2	PBMCPO
PBMCP ₁	3	PBMCP ₁
PBMCP ₂	4	PBMCP ₂
PBMCP3	5	PBMCP3
PBMCP ₄	6	PBMCP ₄
PBMCP ₅	7	PBMCP ₅
PBMCP6	8	PBMCP ₆
PBMCP ₇	9	PBMCP ₇
PBMCP8	10	PBMCP8
PBMCPg	11	PBMCPg
PBMCP ₁₀	12	PBMCP ₁₀
PBMCP ₁₁	13	PBMCP ₁₁
PBMCP ₁₂	14	PBMCP ₁₂
n.c.	15	n.c.
n.c.	16	n.c.
SCCM	17	SCCM
CICM	18	CICM
CICM	19	CICM
ABCMo	20	ABCMo
ABCM ₁	21	ABCM ₁
ABCM ₂	22	ABCM ₂
ABCM ₃	23	ABCM ₃
ABCM ₄	24	ABCM ₄
ABCM5	25	ABCM5
ABCM6	26	ABCM ₆
ABCM ₇	27	ABCM ₇
ABCM8	28	ABCMa
ABCM ₉	29	ABCMg
n.c.	30	n.c.
VP	31	V _P
ον	32	0 V

Terminal location (continued)

connector 3	connector 4
V * 15 • 8 TB8 c. 14 • 7 TB7 c. 13 • 6 TB6 IGH ** 12 • 5 TB5 c. 11 • 4 TB4 TROBE 10 • 2 TB2 TROBE 9 • 1 TB1	n.c. 25 • 13 n.c. n.c. 24 • 12 n.c. n.c. 23 • 11 n.c. n.c. 22 • 9 n.c. n.c. 21 • 9 n.c. n.c. 20 • 7 0 V n.c. 19 • 6 n.c. n.c. 17 • 5 n.c. n.c. 16 • 3 DO n.c. 15 • 2 n.c. n.c. 14 • 2 n.c.

n.c. = not connected

^{*} No supply line, only to be used as signal ground.

** No supply line, only to be used as fixed HIGH level.

PROGRAMMING UNIT

DESCRIPTION

The programming unit is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and output module OM10 (or OM12) to assemble a programmable logic controller (PLC). The control program is written into the program memory with the aid of this unit, by means of the built-in keyboard, or from a punched tape.

The unit can also be used to read the contents of the program memory: eight seven-segments LED displays show the program line number (memory address) and the program word belonging to it. Each program word contains a scratch-pad memory address; the content of this address (1 or 0) is indicated by the status indicator LED.

Programming a system by means of the keyboard (or a punched tape) is only possible when the key switch of the programming unit is set to the on position. The key switch determines the authority of the unit: with a key the user has the complete command of the PLC, without a key he can only monitor its actions.

The keyboard comprises 13 keys (Fig. 3):

- 9 keys, marked 0 to 7 and *, with which the program word is typed in;
- 1 key, marked ENTER; by pressing this key the displayed program word is transferred to the program memory. As soon as the key is released the program memory is set to the read mode; the programming unit reads the contents of the program memory and the program word is again displayed as a check that it is written correctly into the program memory.
- 1 key marked STEP; by pressing this key the next memory address is selected. Each time this key is pressed the line number is incremented by one.
- 1 key, marked CIRC, a repetitive STEP key; by pressing this key the line number is incremented continuously with a frequency of approx. 50 Hz.
- 1 key, marked DECR; by pressing this key simultaneously with either the STEP or CIRC keys, the line number is decremented by one or continuously respectively.

When the key switch is in the off position only the STEP, CIRC and DECR keys are operative. When selecting a particular address by means of these keys, the program word is displayed and the status of the scratch-pad memory address specified in the program word is indicated. In this way the PLC can be monitored without disrupting the working system.

If a punched tape is used, it must be coded according to the ASCII code. The characters to be used for the ENTER and the STEP commands are > and < respectively.

The unit is so constructed that it can be plugged into the PLC; after loading the program into the memory module the PU10 can be removed to be used in another PLC system.

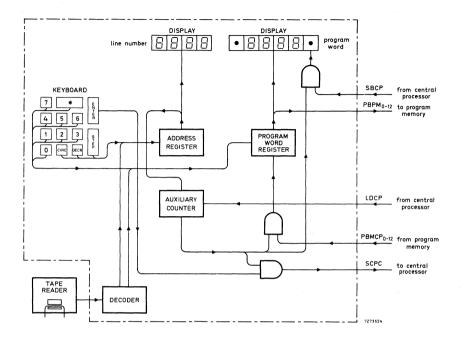


Fig. 1. Simplified block diagram of the programming unit.

The circuit is built on two epoxy-glass printed-wiring boards, mounted in a metal housing, which fits into the Euro-card system. The unit is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 242202589291 (pins for wire wrap), 242202589299 (pins for dip soldering) or 242202589327 (solder tags) $\frac{1}{2}$).

¹⁾ For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.) current

 $V_{
m p}$ 5 V ± 5% $I_{
m p}$ max. 2 A typ. 1,8 A

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminatio	terminations (Fig. 2)	
			connector 1	connector 2	
PBMCP0 PBMCP1 PBMCP2 PBMCP3 PBMCP4 PBMCP5 PBMCP6 PBMCP7 PBMCP8 PBMCP9 PBMCP10 PBMCP11 PBMCP12	Program word bits from program memory.	1 TTL 1 TTL		c2 a2 c4 a4 c6 a6 c8 a8 c10 a10 c12 a12 c14	
LDCP	Synchronization input from central processor; synchronizes auxiliary address counter in programming unit with address counter in central processor.	1 TTL	a14		
$\overline{\text{CL}}_{23}$	Inverted clock input from central processor.	1 TTL	c16		
φ57	Clock signal for status indication from central processor.	1 TTL		c16	
SBCP	Status bit from central processor; clocked by ϕ_{57} it indicates state 1 or 0 at selected scratch-pad memory address.	1 TTL	a16		
TB ₁ TB ₂ TB ₃ TB ₄ TB ₅ TB ₆ TB ₇	Tape bits (ASCII code) from tape reader	2 TTL	c18 a18 c20 a20 c22 a22 c24		

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
STROBE	Signal from tape-reader sprocket.	2 TTL	a24	
SLTP	Selection signal from tape reader or external switch; if tape reader is used the input must be connected to the logic LOW level.	2 TTL	c28	

Output data

PU10

All outputs meet the standard TTL specifications.

output	function	loada-	terminations (Fig. 2)		
		bility	connector 1	connector 2	
PBPM0 PBPM1 PBPM2 PBPM3 PBPM4 PBPM5 PBPM6 PBPM7 PBPM7 PBPM8 PBPM9 PBPM10 PBPM11 PBPM11 PBPM12	Program word bits to program memory.	9 TTL 9 TTL	c2 a2 c4 a4 c6 a6 c8 a8 c10 a10 c12 a12 c14	Connector 2	
ABP 0 ABP 1 ABP 2 ABP 3 ABP 4 ABP 5 ABP 6 ABP 7 ABP 8 ABP 9 ABP 10 ABP 11	Inverted address bits (line number bits to external printer).	10 TTL 10 TTL		c18 a18 c20 a20 c22 a22 c24 a24 c26 a26 c28	
READY	Signal indicating that contents of program memory address counter agrees with line number.	10 TTL		a16	

output	function	loada-	terminations (Fig. 2)		
		bility	connector 1	connector 2	
SCPC	Store command to central processor.	10 TTL		a14	
BSP	Busy signal to external tape reader; the output becomes LOW when a correct code has been recognized, and becomes HIGH when this code has been stored.	10 TTL	c26		
BSP	Inverted BSP.	10 TTL	a26		

Time data

If a tape reader is used for loading the control program into the program memory the following considerations have to be taken in account.

Delay time between the level changes on TB1-7 and strobe signal $$t_1$$ min. 0 ns Delay time between leading edge of strobe pulse and code recognition on BSP $$t_2$$ max. 500 ns Strobe pulse duration $$t_8$$ min. 2 μs max. 10 ms

BSP becomes LOW when a correct code has been recognized and HIGH when this code has been stored. At this moment the tape reader can be started to give the next code.

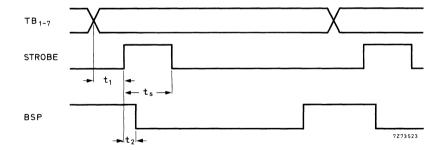


Fig. 2

PROGRAMMING UNIT

4322 027 90410

76

October 1976

1140 g

Mass

Terminal location connector 1 connector 2

	incecor	-	001	IIICCCCCI	-
row c		row a	row c		row a
$PBPM_0$	2	PBPM ₁	PBMCP ₀	2	PBMCP ₁
PBPM ₂	4	PBPM ₃	PBMCP ₂	4	PBMCP ₃
PBPM ₄	6	PBPM 5	PBMCP ₄	6	PBMCP ₅
PBPM ₆	8	PBPM ₇	PBMCP ₆	8	PBMCP ₇
PBPM8	10	PBPM9	PBMCP ₈	10	PBMCP ₉
PBPM ₁₀	12	PBPM ₁₁	PBMCP $_{10}$	12	PBMCP ₁₁
<u>PBPM 12</u>	14	LDCP	PBMCP ₁₂	14	SCPC
CL23	16	SBCP	$\frac{\phi}{57}$	16	READY
$^{\mathrm{TB}}1$	18	${ m TB_2}$	$\overline{\text{ABP}}_0$	18	$\overline{ ext{ABP}}_1$
TB_3	20	TB_4	\overline{ABP}_2	20	$\overline{\text{ABP}}_3$
TB_5	22	TB ₆	$\overline{\text{ABP}}_4$	22	$\overline{\text{ABP}}_5$
TB_7	24	STROBE	$\overline{\text{ABP}}_{6}$	24	ABP ₇
BSP	26	BSP	ABP ₈	26	ABP9
SLTP	28	n.c.	$\overline{ ext{ABP}}_{10}$	28	$\overline{\mathrm{ABP}}_{11}$
Vp	30	Vp	$\nabla \mathbf{p}$	30	Vp
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.



BACK PANELS

APPLICATION

Back panels BP11 to BP16 are designed for use as mother boards in 19-inch racks in the PLC system. Use of these panels removes the work of wiring separate connectors to receive the modules. The range avoids system redundancy and allows the rack space to be fully utilized.

DESCRIPTION

The back panels are equipped with female connectors, matching the male counterparts of the PLC modules. They have solder bridges for determining the addresses of an input/output/LX10 module (MID), the addresses of the MM modules (ENCM), the last IM/OM module or cycle time (IDLC), the last MM module (MICC), and connecting blocks for external connections.

Types BP11 to BP14 each consist of two back panels. The upper panel provides the required interconnections for connector 1 of each PLC module. The lower panel provides the interconnections for connector 2 of each MM, PU and CP module (see Figs 1 to 4). External connections are made to the lower connectors of the IM, OM and LX10 modules; these must be received by the separately mounted female connectors.

As the layout of the panels depends on the number of MM modules used, four different types have been developed. Table 1 surveys the various back panels and the type and number of each module which can be placed in the rack. Since a greater number of MM modules generally requires a greater number of IM/OM modules, need will be felt for an extension rack to accommodate these extra modules. Two back panel types are available for this purpose: the BP15 is for 15 IM/OM modules; the BP16 is for 21. These, of course, are only upper back panels.

Table 1 Back panels

no. of MM modules	no. of IM/OM/LX* modules	no, of CP modules	no. of PU modules	type of back panel	catalogue number 9390 269
1	13	1	1	BP11	30112
2	11	1	1	BP12	40112
3	9	1	1	BP13	50112
4	7	1	. 1	BP14	60112
-	15**	_	-	BP15	70112
_	21**		_	BP16	80112

The back panels are screwed to the rack by M2,5 screws, using threaded rails and isolation strips.

- * A maximum of 4 LX modules can be inserted at positions IM/OM1 to IM/OM4. If an extension rack is used, one place in each rack must be reserved for data bus cable, thus the number of modules is one less than the number stated in this column.
- ** Back panels type BP15 and BP16 are extension panels for use in a second rack to accommodate additional IM/OM modules.

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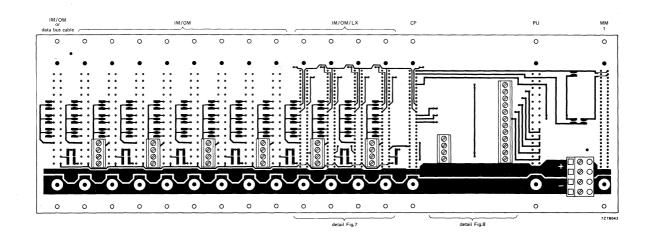


Fig. 1 Back panel BP11.

= input module

OM = output module

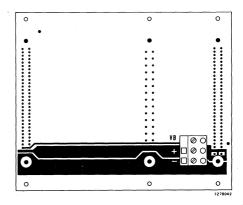
= load external interface module

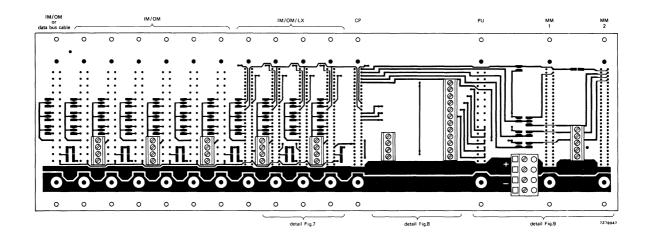
= central processor

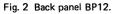
= programming unit MM = program memory module

supply voltage

 $V_B = +4,5 \text{ V to } +7,5 \text{ V (battery voltage)}$







IM = input module

OM = output module

LX = load external interface module

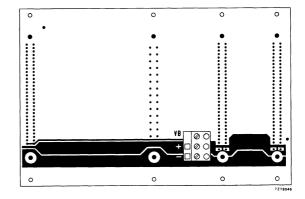
CP = central processor

PU = programming unit

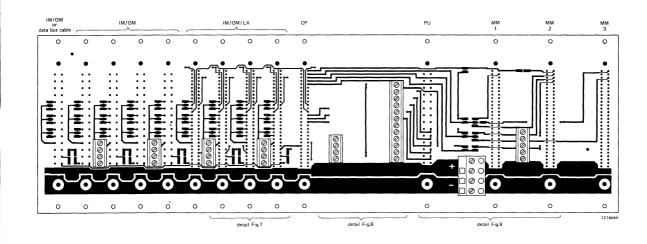
MM = program memory module

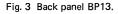
+ = +5 V ± 5% supply voltage

 $V_B = +4,5 \text{ V to } +7,5 \text{ V (battery voltage)}$



October 1978





IM = input module

OM = output module

LX = load external interface module

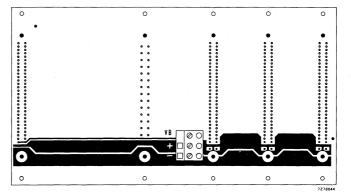
CP = central processor

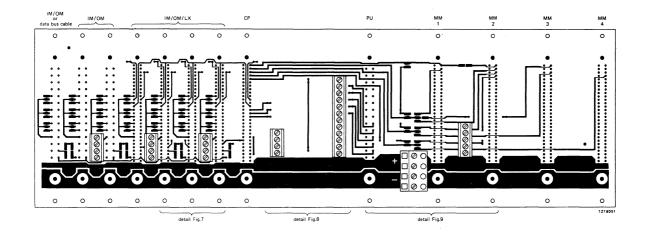
PU = programming unit

MM = program memory module

 $\begin{array}{ccc} + & = +5 \text{ V} \pm 5\% \\ - & = 0 \end{array}$ supply voltage

 $V_B = +4.5 \text{ V to } +7.5 \text{ V (battery voltage)}$





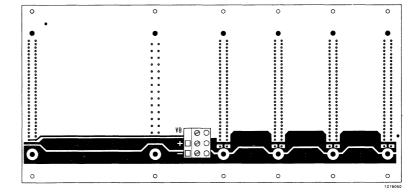


Fig. 4 Back panel BP14.

IM = input module

OM = output module

LX = load external interface module

CP = central processor

PU = programming unit

MM = program memory module

 $\begin{array}{ccc} + & = +5 \text{ V} \pm 5\% \\ - & = 0 \text{ V} \end{array}$ supply voltage

 $V_B = +4.5 \text{ V to } +7.5 \text{ V (battery voltage)}$

Fig. 5 Back panel BP15. IM = input module OM = output module ifi ifi ifi 0 فههه أبا أبا أبا 0 0 0 0 0 0 7278048 0 0 0 0 0 0 0 ifi ifi ifi MO/M 0 0 0 0 ابا ابا ابا 🔊 🔊 0 الم الم الم الم 0 0 0 فههه إذا أبا أبا 0 هههها ابا ابا ó 0 0 أبا أبا أبا أي 0 ابا ابا ابا 0 0 data bus cable 0 işi işi işi)

Fig. 6 Back panel BP16.

OM = output module

IM = input module

Each of the IM and OM modules has a discrete address so that the central processor can address each in turn during an input/output cycle. This address is formed by bridging the appropriate MID pad (MID_{0.4}) and the adjacent 0 V pad (connected to connector 1, pin c22). Table 2 gives the address codes for the IM and OM modules. The MID₅ pad is not used.

If no LX modules are used, it is important to assign the MID addresses to the IM and OM modules, so that the spare addresses, if any, are of a higher order than the used addresses. If this is not done, the input/output cycle will take longer than necessary. If no LX modules are inserted, the IDLC pad of the last IM/OM module (the one with the highest address) must be bridged to the adjacent r or n-shaped pad. If output modules are inserted at places IM/OM/LX2 and IM/OM/LX3, for instance, a logic LOW level applied via wires, connected to REO₂ and REO₃ of the connector block between places IM/OM/LX2 and IM/OM/LX1, will reset all the output latches in the relevant modules. Consequently the output transistors are driven in the non-conductive state. A logic LOW (inhibit) applied via wires connected to MIN₁ or MIN₂ of the same connector block, causes data from input modules (IM/LX) inserted at places IM/OM/LX1 or IM/OM/LX2 respectively, to be ignored by the central processor. It also prevents data stored during the preceding input/output cycle in output modules, inserted in the same places, from changing. If one or more LX modules are inserted, pin a25 automatically connects the IDLC line of the central processor to zero (maximum cycle time of 0,924 ms). Removal of all LX modules will affect the 0,924 ms cycle time. As the maximum number of LX modules in any one PLC system is 4, only two MID pads are used for addressing (see Table 3).

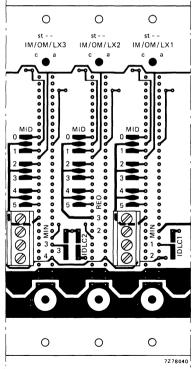


Fig. 7 Detail of back panels BP11 to BP16. Note: $\overline{\text{MID}}_5$ is normally not used.

Table 2 IM and OM module address codes

MID ₀	MID ₁	$\overline{\text{MID}}_2$	MID ₃	$\overline{\text{MID}}_4$	input/output stage address $-$ scratch-pad locations
_		_	_	_	000 to 017
0 V	_		_	_	020 to 037
_	0 V		_	· -	040 to 057
0 V	0 V		_	_	060 to 077
		0 V	_	_	100 to 117
0 V	_	0 V		_	120 to 137
_	0 V	0 V	_	_	140 to 157
0 V	0 V	0 V	_	_	160 to 177
	_	_	0 V	_	200 to 217
0 V	_		0 V	_	220 to 237
	0 V	_	0 V		240 to 257
0 V	0 V	_	0 V	_	260 to 277
_		0 V	0 V	_	300 to 317
0 V	_	0 V	0 V	_	320 to 337
_	0 V	0 V	0 V	_	340 to 357
0 V	0 V	0 V	0 V	_	360 to 377
_	_	_		0 V	400 to 417
0 V	_		_	0 V	420 to 437
_	0 V		_	0 V	440 to 457
0 V	0 V	_		0 V	460 to 477
_		0 V	-	0 V	500 to 517
0 V		0 V		0 V	520 to 537
-	0 V	0 V	-	0 V	540 to 557
0 V	0 V	0 V		0 V	560 to 577
			0 V	0 V	600 to 617
0 V	-		0 V	0 V	620 to 637
_	0 V	_	0 V	0 V	640 to 657
0 V	0 V		0 V	0 V	660 to 677
	-	0 V	0 V	0 V	700 to 717
0 V		0 V	0 V	0 V	720 to 737
_	0 V	0 V	0 V	0 V	740 to 757
0 V	0 V	0 V	0 V	0 V	760 to 777

Table 3 LX module address codes

MID ₃	MID ₄	address of eight-bit data source
_	_	00o to 17o
0 V	_	20o to 37o
	0 V	40o to 57o
0 V	0 V	60o to 77o

Notes to Tables 2 and 3.

- 1. 0 V indicates that the $\overline{\text{MID}}$ terminal is connected to connector 1, pin c22 (0 V).
- 2. indicates that the MID terminal is floating.
- 3. The least significant digit of each LX address is always 0, e.g. 000 to 170 in the table signifies addresses 000, 010, 020, 030 etc., up to 170.

Fig. 8 shows the connector blocks on the back panels BP11 to BP14. The left-hand block contains connections for the REO₁ wire and the MIN wire with the number of the highest IM/OM place (13, 11, 9 or 7). A CLCP wire can be connected to the upper terminal, carrying a disable signal from external source (switch) to central processor (active LOW). The operation of this signal in combination with the SPCE signal, carried by a wire connected to the lower terminal, is given in Table 4.

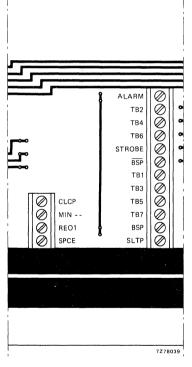
The right-hand connector block contains the output connection ALARM, which will become LOW when the supply voltage drops below 4,75 V. The tape reader connections TB₁ to TB₇ and STROBE can be connected to the corresponding tape bit outputs of a tape reader. Connection BSP or BSP must then be connected to the start/stop input of the tape reader. Connection SLTP must be switched to 0 V during tape reader programming and left floating during keyboard programming.

Fig. 8 Detail of back panels BP11 to BP14.

Table 4 Operation of CLCP and SPCE

CLCP	SPCE	operation
0	X*	The central processor is held at the beginning of an input/output cycle.
1	X*	The central processor is running.
0 → 1	1	The central processor starts running at the beginning of an input/output cycle. All scratch-pad locations, except those corresponding to inputs are reset to '0' during the first input/output cycle. All outputs from the PLC output modules are passive after the first input/output cycle.
0 → 1	0	The central processor starts running at the beginning of an input/output cycle. Any data existing in the scratch-pad locations corresponding to outputs determine the state of the output stages in the output modules during the first input/output cycle.

^{*} X indicates either 0 or 1.



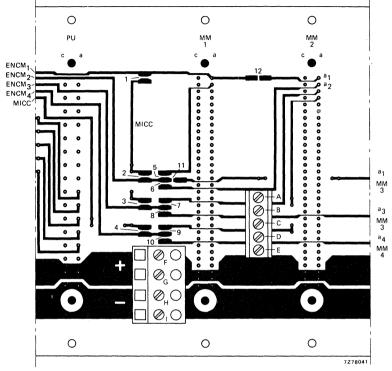


Fig. 9 Detail of back panels BP12 to BP14.

A = PRB; B = START; C = INH; D = MSI_1 ; E = MSI_2 ; F = +5 V, \pm 5%; G = +5 V, \pm 5%; H = 0 V; I = 0 V.

Pads 11 and 12 and connections A to E are used for program copying with the MM11 module.

ENCM₁₋₄ = enable signal from central processor to program memory;

MICC = memory identification signal derived from MM module in highest position;

PRB = program busy output signal to external equipment;

INH = inhibit input, when LOW the start input is inoperative;

MSI = mode selection inputs (see data sheets MM11).

Table 5 MM module address codes

total byte content	number and type of MM	MM module position			ו	pad pairs to be bridged		module position in which a ₁ must be
	modules	1	2	3	4		ENCM	connected with a ₂
1k	1 MM10					1		
	1 MM12					1		
2k	2 MM10					2	6	
	2 MM12					2	6	1 2
	1 MM12					2	5	
3k	3 MM10					3	6 8	
	3 MM12					3	6 8	1 2 3
	2 MM12					3	5 7 9	
4k	4 MM10					4	6 8 10	
	4 MM12					4	6 8 10	1 2 3 4
	2 MM12					4	5 7 9	

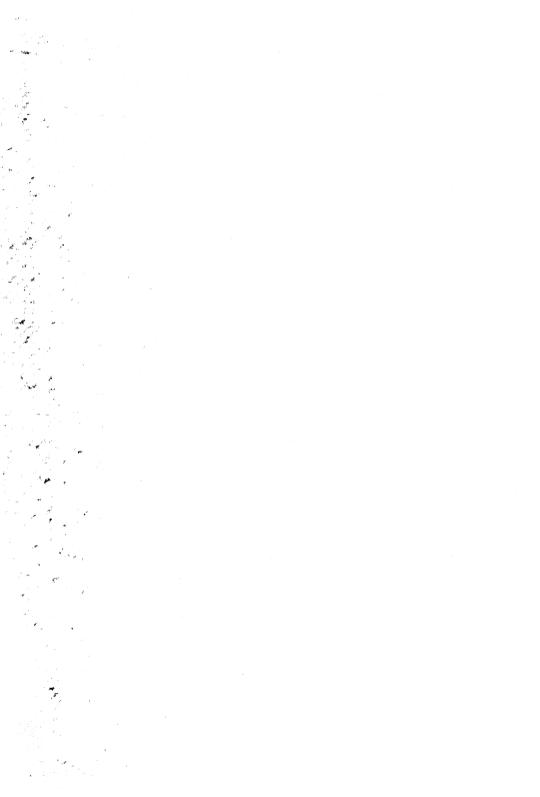
Note

= MM12 equipped with 1 k only (PROMs in position 1A and 1B).

= MM12 equipped with 2 k.



PC20 MODULES



MODULES FOR PROGRAMMABLE CONTROLLERS

GENERAL

The programmable controller PC20 is used for controlling machines and/or processes. It can be easily programmed and re-programmed.

The modular design of the PC20 enables a user to build a programmable controller which is 'tailor-made' for his control task. By specifying the number and the types of PC20 modules that he requires he only has to purchase the electronic capability he needs.

The PC20 modules are on standard double Eurocards.* Optically isolated interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ensures good compatibility.

Besides these modules, the PC20 comprises back panels, frames (19 in racks), input and output cables, and a standard power supply. The frames and modules conform to IEC 297 or DIN 41494 (for racks) and IEC 130-14 or DIN 41612 (for connectors). For smaller controllers the special frame SC20 and power supply SO20 are available.

The microcontroller MC20 is suited for controlling small systems. This controller is based on the same principles as the PC20 system, however it is built on a single printed board** with sufficient inputs and outputs for the general run of machine tool and process controls.

Software modules are available e.g. for communication in hierarchical systems.

Tables 1 to 5 give a survey of the available modules, accessories and cables.

^{*} Except programming unit PU20, which is a desk-top apparatus.

^{**} Different from standard Eurocards.

PROGRAMMABLE CONTROLLERS

Table 1 Modules

type	description	catalogue number	page
AD20	analogue to digital module	4322 027 94200	153
C120*	computer interface	4322 027 94630	
CP20	central processor with program memory (2 k (E) PROM)	4322 027 92040	99
CP21**	central processor with program memory (1 k RAM)	4322 027 92050	109
CP22	central processor without program memory	4322 027 92060	119
CP24	central processor with program memory (2 k RAM)	4322 027 94140	129
DA20	digital to analogue module	4322 027 94210	197
IM20	input module (16 inputs, 24 V)	4322 027 92000	139
IM22	input module (32 inputs, 24 V)	4322 027 94660	147
IM23	input module (16 inputs, 48 V)	4322 027 94610	139
MM20	program memory module (8 k (E) PROM)	4322 027 92070	161
MM21	program memory module (8 k RAM)	4322 027 92080	167
MM22	program memory module (4 k RAM)	4322 027 94160	167
OM20	output module (16 x 0,5 A; 24 V)	4322 027 92010	173
OM21	output module (8 x 2 A; 24 V)	4322 027 92020	179
OM22	output module (32 x 0,1 A; 24 V)	4322 027 94100	185
OM23*	output module (16 x 0,5 A; 24/48 V)	4322 027 94700	
RP20	bidirectional parallel interface	4322 027 92170	205
RS20	bidirectional serial interface	4322 027 92180	215
SO20	supply and output module (8 x 0,5 A)	4322 027 92030	191
V120	bidirectional serial interface	4322 027 92200	223
MC20	microcontroller	4322 027 23000	233

Table 2 Programming aids

type	description	catalogue number	page
M120	microcontroller interface for MC20	4322 027 94190	241
PU20/2	programming unit for PC20 and MC20	4322 027 92090	247
PU23	programming unit interface for PC20 and MC20	4322 027 94180	253

^{*} Under development.

^{**} Obsolescent type.

Table 3 Accessories

type	description	catalogue number	page
BP22	terminal strip for inputs/outputs in controller cabinet SC20	4322 027 92140	267
BP23	back panel for main Eurorack	4322 027 94010	261
BP25	back panel for half extension rack	4322 027 94030	261
BP26	back panel for full extension rack	4322 027 94040	261
BP27	terminal strip for output module OM22 in controller		
	cabinet SC20	4322 027 93950	267
FP20	front plate, 15 mm width, in controller cabinet SC20	4322 027 92150	269
FP21	front plate, 20 mm width (standard module width)	4322 027 92160	269
MB20	mounting clip for microcontroller MC20	4322 027 23080	238
RA23	main rack assembly	9390 294 10000	
RA25	half extension rack assembly (for 15 I/O modules)	9390 294 20000	
RA26	full extension rack assembly (for 21 I/O modules)	9390 294 30000	
SC20	small controller cabinet	4322 027 92110	267
	CP front panel kit (one LED hole)	4322 027 91440	
	IM/OM front panel kit (16 LED holes)	4322 027 91450	
	front panel kit, double width (no holes)	4322 027 91460	
SM20*	supply module		

Table 4 Cables

type	description	catalogue number	page
BI21	bus extension cable for one I/O extension rack	4322 027 37910	266
B122	bus extension cable with bus interface for two		
	I/O extension racks	4322 027 37920	266
B123	bus extension cable with bus interface for three		
	I/O extension racks	4322 027 37930	266
CC20	connecting cable for module OM21	9390 293 50000	
CC21	connecting cable for module SO20	9390 293 60000	
CC22	connecting cable for modules IM20/IM23	9390 293 70000	
CC23	connecting cable for modules IM20/IM23 and OM20/OM23	9390 293 80000	

Table 5 Software modules

type	description	catalogue number	page
PVI1	message program	4322 027 99011	230
PVI2	data terminal program	4322 027 99021	230
PVI3	mass memory program	4322 027 99031	
PVI4	communication program A	4322 027 99041	230
PVI5	communication program B	4322 027 99051	230
PV17	communication program C	4322 027 99071	230
PVI8	PID control loop	4322 027 99081	230
PDS2	program development system n	4322 027 99921	

^{*} Under development.

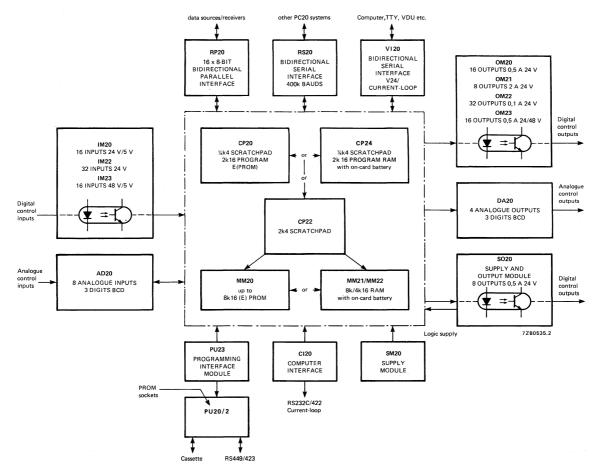


Fig. 1 Diagram of PC20 system.

Figure 1 shows, in a simplified form, the function of each of the PC20 modules. In operation the PC20 cycles continuously through a data input/output cycle and a data processing cycle.

The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit PU20/2 is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is a portable desk-top apparatus so that only one is required to serve any number of PC20 systems. It is connected to the PC20 system via the programming unit interface PU23, which is not too expensive to leave in the PC20 system.

For programming and monitoring the MC20 system, the same programming unit (PU20/2) as for the PC20 system is used, however this unit has to be used in conjunction with microcontroller interface MI20 and programming unit interface PU23, see Fig. 2.

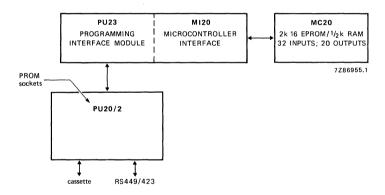


Fig. 2 Diagram of MC20 system.

PROGRAMMABLE CONTROLLERS

GENERAL CHARACTERISTICS

Operating temperature range

Storage temperature range

Dimensions

Supply voltage (d.c.)

Number of input + output signals

Maximum program length

Cycle time

0 to + 60 °C (0 to + 45 °C*)

 $-40 \text{ to} + 70 ^{\circ}\text{C}$

160 mm x 233 mm (double Eurocard) according to IEC 297 or DIN 41494**

 $V_P = 10 \text{ V} \pm 10\%$; 24 V $\pm 25\%$ **

2000

8 k instructions

1 ms for a typical program of 1 k instructions

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC 68-2-6, test method Fc; 10 to 55 Hz, amplitude 0,75 mm (0,35 mm*) or 5g (whichever is less).

Shock test

IEC 68-2-27, test method Ea; 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50g (30g*).

Rapid change of temperature test

IEC 68-2-14, test method Na: 5 cycles of 2 h at -40 °C and 2 h at + 85 °C.

Damp heat test

IEC 68-2-3, test method Ca: 21 days at 40 °C, R.H. 90 to 95%.

Note

For detailed information refer to the PC20 User Manual, catalogue number 9398 609 60011.

Valid for PU20/2.

^{**} For PU20/2 and MC20 see the relevant data sheet.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP20 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The program memory consists of 2 EPROMs 2716 (2k), for which 2 sockets (A and B, Fig. 5) are provided. The CP20 is supplied with 2 empty EPROMs, which can be programmed on the programming unit PU20/2.

The capacity of the *scratchpad memory* is ½k4. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case the address notation is, for example, 147.2 or 076.0. The CP20 has no on-board battery back-up; provisions for an external battery for data retention in the scratchpad memory are present.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

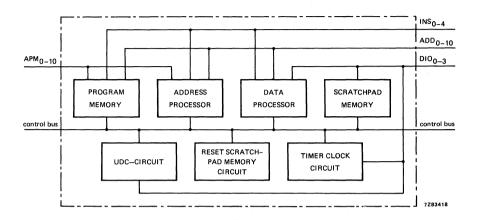
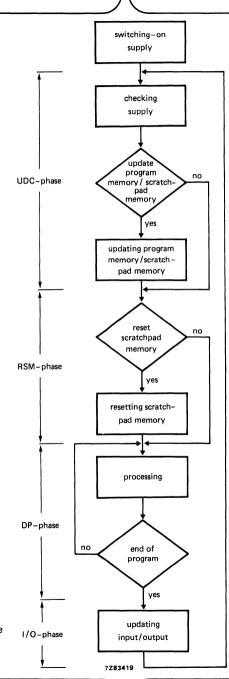


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1 , are:

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.



ELECTRICAL DATA

Supply

Supply voltage (d.c.)

٧p 10 V ± 10% lρ max. 270 mA

current

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage

 V_{B}

3 to 4.5 V

2 mA

Battery current (Vp = 0 V)

Trickle charge current (Vp = 10 V)

l_B max.

-6 mA typ.

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (ons (Fig.	(Fig. 5)	
	Turiction			connector		
BI-DIRECT	TIONAL BUSSES					
ADD0 ADD1 ADD2 ADD3 ADD4 ADD5 ADD6 ADD7 ADD8 ADD9 ADD10	Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15, a16,	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15			
APMO APM1 APM2 APM3 APM4 APM6 APM7 APM8 APM9 APM10	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).			a16, a17, a18, a19, a20, a21, a22, a23, a24, a25, a26,	c10 c11 c15 c20 c2 c2 c22 c22 c22 c22	
APM ₁₁ APM ₁₂	Pseudo address bits connected via resistor to 0 V.			a27, a28,	c2	
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scratchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM.	a19, a20, a21, a22,	c19 c20 c21 c22			

	function	te	terminati		ons (Fig. 5)	
	Idioton	conne	ctor 1	conne	ector 2	
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU23; commanded by PDBE	a1, a2, a3, a4, a5,	c1 c2 c3 c4 c5		•	
INPUTS		- Navara				
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29,	c29			
CPSD	Central processor slow down; input commanded by PU23.			a3,	c3	
CPSI	Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH).			a4,	c4	
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25				
HOLD	Command from PU23 to stop central processor in DP-phase (active LOW).			а6,	с6	
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.			a1,	c1	
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.			a2,	c2	
PRF	Preparation input/output modules finished.	a24				
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.			a12,	c12	
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.			a10,	c10	

	function	terminati	ons (Fig	, 5)
	Tunction	connector 1	conne	ector 2
R/WSM	Read-write level from input and output modules; only effective during I/O-phase.	c24		
WEPC	Write enable signal from PU23; prepares central processor to store data from PU23 into scratch-pad memory.	c28		
WPSM	Write pulse for scratchpad memory; signal from PU23 to store data on DIO ₀₋₃ into scratchpad memory.		a13,	c13
OUTPUTS				
APF	Address processing for input and output modules finished; address stable.	a26		
CLOCK	Clock output to PU23.		а7,	с7
CPSC	Central processor stop completed; command (HIGH) to PU23 indicating that central processor has been stopped in UDC-phase.		а5,	с5
PB ₀ PB ₁	Page bits, connected to 0 V.	a17 c17		
PHC ₀ PHC ₁	Phase control to PU23 and input and output modules.	c23 a23		
RCO	Reset output to output modules; becomes LOW during switch-on of the system, or if \overline{RCP} is LOW. When a wire jump has been inserted between the \overline{RCO} points on the module (Fig. 3), \overline{RCO} output will also become LOW if $V_P < 9$ V or > 11 V.	c27		
RR	Result Register.	a18, c18		
SBI	Storage command to store data on data bus into output modules and PU23.	c26		
SRI + SRI	System run indication; Darlington transistor output, galvanically isolated by means of opto-coupler. SRI += collector, SRI — = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30 c30		

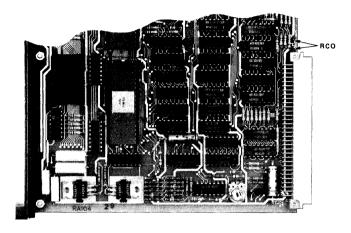


Fig. 3 Location of RCO points.

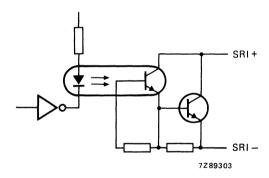


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I $_{\rm Q}$ = max. 100 mA, V $_{\rm CE}$ < 1,5 V; transistor non-conducting: I $_{\rm Q}$ = max. 10 μ A; V $_{\rm CE}$ \leq 30 V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Fixed scratchpad memory addresses

address	description
0.000	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \le 17,5 \text{ V}$).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA Outlines

Dimensions in mm

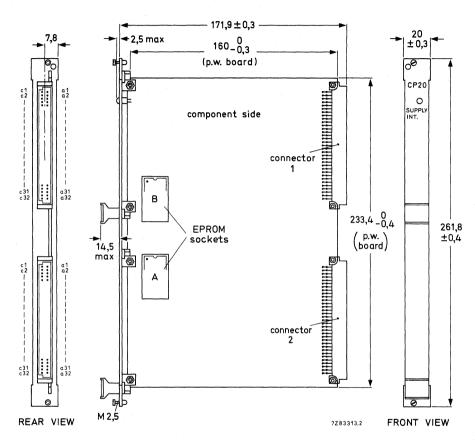


Fig. 5.

Mass

approx. 270 g

Terminal location

	connector 1			connector 2	
row c		row a	row c		row a
INSO	1	INS ₀	PABE	1	PABE
INS ₁	2	INS ₁	PDBE	2	PDBE
INS ₂	3	INS ₂	CPSD	3	CPSD
INS3	4	INS3	CPSI	4	CPSI
INS ₄	5	INS ₄	CPSC	5	CPSC
ADD_0	6	ADD_0	HOLD	6	HOLD
ADD ₁	7	ADD_1	CLOCK	7	CLOCK
ADD ₂	8	ADD_2	n.c.	8	n.c.
ADD_3	9	ADD_3^-	n.c.	9	n.c.
ADD ₄	10	ADD_4	RSME	10	RSME
ADD ₅	11	ADD ₅	n.c.	11	n.c.
ADD_6	12	ADD ₆	RCP	12	RCP
ADD_7	13	ADD_7	WPSM	13	WPSM
ADD ₈	14	ADD ₈	n.c.	14	n.c.
ADD9	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	ADD ₁₀	APM_O	16	APM_O
PB ₁	17	PB _O	APM ₁	17	APM ₁
RR	18	RR	APM ₂	18	APM ₂
DIO_0	19	DIO ₀	APM3	19	APM_3
DIO ₁	20	DIO ₁	APM ₄	20	APM ₄
DIO ₂	21	DiO ₂	APM ₅	21	APM ₅
DIO_3^-	22	DIO3	APM ₆	22	APM ₆
PHC0	23	PHC ₁	APM ₇	23	APM ₇
R/WSM	24	PRF	APM ₈	24	APM ₈
0 V *	25	DEF	APM ₉	25	APMg
SBI	26	APF	APM ₁₀	26	APM ₁₀
RCO	27	n.c.	APM ₁₁	27	APM ₁₁
WEPC	28	n.c.	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
SRI —	30	SRI +	VB	30	VB
Vp	31	V_{p}	V _p	31	V_p
0 ν	32	0 V	0 V	32	0 V

n.c. = not connected.

^{*} No supply line; is used as return line for control signals.



CENTRAL PROCESSOR

DESCRIPTION

The central processor CP21 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* is a C-MOS RAM (1k16). The CP21 has on-board battery back-up and a provision to connect an external battery for longer memory retention.

The capacity of the *scratchpad memory* is ¼k4. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case, the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

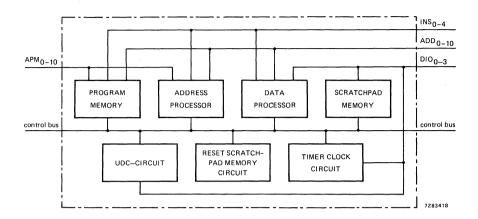


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC₀ and PHC₁, are:

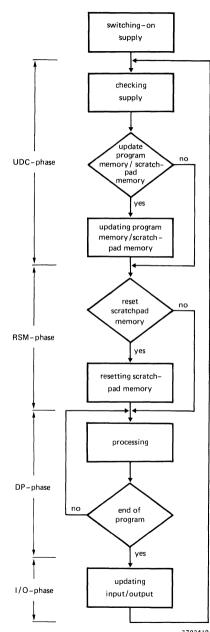
- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;

- reset scratchpad memory (RSM): PHC₀ = 1, PHC₁ = 0.

data processing (DP):
 up-date input/output (I/O):
 PHC₀ = 0, PHC₁ = 1.
 PHC₀ = 1, PHC₁ = 1.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130—14 or DIN 41612 for connectors.



7Z83419

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

current

V_P 10 V ± 10% I_P max. 160 mA

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.

Battery voltage

...

V_B 3 to 4,5 V

Battery current $(V_P = 0 V)$

I_B max. 2 mA typ. -6 mA

Trickle charge current (V_P = 10 V)

Data retention with on-board battery at 40 °C

typ. 40 h, provided the module is in operation for at least

20 h

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	termination connector 1		s (Fig. 4)	
	Tunction			conne	ctor 2
BI-DIRECTI	ONAL BUSSES				
ADD0 ADD1 ADD2 ADD3 ADD4 ADD5 ADD6 ADD7 ADD8 ADD9 ADD10	Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15,	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15		
APM0 APM1 APM2 APM3 APM4 APM5 APM6 APM7 APM8 APM9 APM10	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).			a16, a17, a18, a19, a20, a21, a22, a23, a24, a25, a26,	c16 c17 c18 c19 c20 c21 c22 c23 c24 c25 c26
APM ₁₁ APM ₁₂	Pseudo address bits connected via resistor to 0 V.			a27, a28,	c27 c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scratchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM.	a19, a20, a21, a22,	c19 c20 c21 c22		

		termina	ations (F	ig. 4)
	function	connector 1	conne	ector 2
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU23; commanded by PDBE,	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5		
INPUTS				
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29		
CPSD	Central processor slow down; input commanded by PU 23.		аЗ,	с3
CPSI	Central processor stop initiate; command from PU23 stops central processor in UCD-phase (active HIGH).		a4,	c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25		
HOLD	Command from PU23 to stop central processor in DP-phase (active LOW).		а6,	c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1,	c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2,	c2
PRF	Preparation input/output modules finished.	a24		
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.		a12,	c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10,	c10
R/WPM	Write signal from PU23 to CP21, to store data in program memory (active HIGH).		a14,	c14

•	· ·	t	terminations (Fig.		
	function	conne	ector 1	conne	ector 2
R/WSM	Read-write level from input and output modules; only effective during I/O-phase.		c24		
WEPC	Write enable signal from PU23; prepares central processor to store data from PU23 into scratch-pad memory.		c28		
WPSM	Write pulse for scratchpad memory; signal from PU23 to store data on DIO ₀₋₃ into scratchpad memory.			a13,	c13
OUTPUTS					
APF	Address processing for input and output modules finished; address stable.	a26			
CLOCK	Clock output to PU23.			a7,	с7
CPSC	Central processor stop completed; command (HIGH) to PU23 indicating that central processor has been stopped in UDC-phase.			a5,	с5
PB ₀ PB ₁	Page bits, connected to 0 V.	a17	c17		
PHC ₀ PHC ₁	Phase control to PU23 and input and output modules.	a23	c23		
RCO	Reset output to output modules; becomes LOW during switch-on of the system, or if \overline{RCP} is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), \overline{RCO} output will also become LOW if $V_P < 9$ V or > 11 V.		c27		
RR	Result Register	a18,	c18		
SBI	Storage command to store data on data bus into output modules and PU23.		c26		

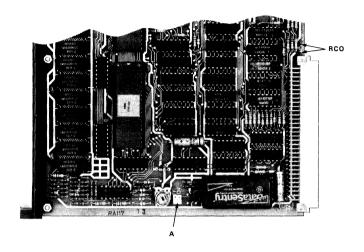


Fig. 3 Location of RCO points and switch (jumper A) of on-board battery.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \le 17,5 \text{ V}$).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA Outlines

Dimensions in mm

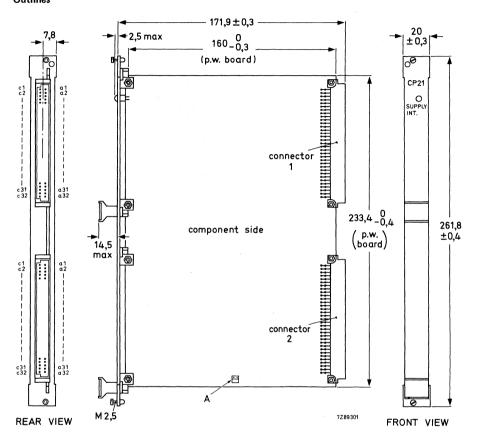


Fig. 4.

Mass

approx. 270 g

Notes

- At delivery of the central processor the on-board battery is switched off (jumper A, Figs 3 and 4, in off-position).
- If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

	connector 1		,	connector 2	
row c		row a	row c		row a
INS ₀	1	INS ₀	PABE	1	PABE
INS ₁	2	INS ₁	PDBE	2	PDBE
INS ₂	3	INS ₂	CPSD	3	CPSD
INS3	4	INS3	CPSI	4	CPSI
INS ₄	5	INS ₄	CPSC	5	CPSC
ADD_0	6	ADD ₀	HOLD	б	HOLD
ADD_1	7	ADD ₁	CLOCK	7	CLOCK
ADD ₂	8	ADD_2	n.c.	8	n.c.
ADD_3	9	ADD_3^-	n.c.	9	n.c.
ADD ₄	10	ADD ₄	RSME	10	RSME
ADD ₅	11	ADD ₅	n.c.	11	n.c.
ADD ₆	12	ADD ₆	RCP	12	RCP
ADD ₇	13	ADD ₇	WPSM	13	WPSM
ADD8	14	ADD ₈	R/WPM	14	₹/WPM
ADD9	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	ADD ₁₀	APM ₀	16	APM ₀
PB ₁	17	PB _O	APM ₁	17	APM ₁
RR	18	RR	APM ₂	18	APM ₂
DIO ₀	19	DIO ₀	APM ₃	19	APM3
DIO ₁	20	DIO ₁	APM ₄	20	APM ₄
DIO_2	21	DIO ₂	APM ₅	21	APM ₅
DIO_3	22	DIO3	APM ₆	22	APM ₆
PHC0	23	PHC ₁	APM ₇	23	APM ₇
R/WSM	24	PRF	APM ₈	24	APM ₈
0 V*	25	DEF	APM ₉	25	APM ₉
SBI	26	APF	APM ₁₀	26	APM ₁₀
RCO	27	n.c.	APM ₁₁	27	APM ₁₁
WEPC	28	n.c.	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V _p 0 V	31	v_p	v_p	31	V_{p}
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

^{*} No supply line; is used as return line for control signals.



CENTRAL PROCESSOR

DESCRIPTION

The central processor CP22 is for use with other PC20 modules, to assemble a programmable controller,

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates the clock pulses for the controller.

The central processor block diagram is given in Fig. 1.

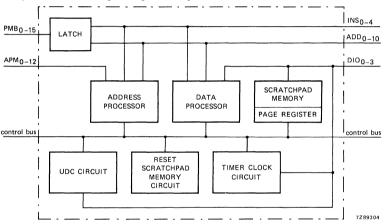


Fig. 1 Block diagram.

The data processor performs the control of the system and the complete timing. It includes the instruction decoder, the logic processor, the arithmetic processor and the control of the internal data traffic.

The address processor generates addresses for the program memory. It also generates addresses for the input and output modules. It has an address range for an 8 k program memory.

In the scratchpad memory the data from the inputs are stored as are the processed data for transfer to the outputs; for this purpose the inputs and outputs each have their own, individual place in the scratchpad. The capacity of the scratchpad memory, including the page register, is 2k4, divided in 4 pages of 512 words each; for details see para. "Organization of scratchpad memory and page register". The CP22 has provisions for an external battery for data retention in the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system about power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* provides the central processor with the possibility to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after the switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC₀ and PHC₁, are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$.

- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$.

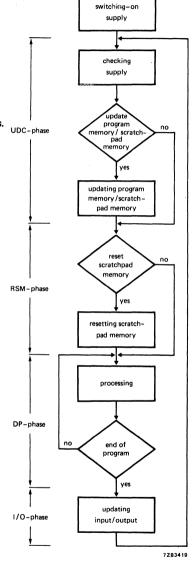
— data processing (DP):

 $PHC_0 = 0, PHC_1 = 1.$

- up-date input/output (I/O):

 $PHC_0 = 1, PHC_1 = 1.$

Each central processor is built on an epoxy-glass printedwiring board of 233,4 mm x 160 mm (double Euro-card*). The board is provided with two F068-I connectors (male parts); the corresponding female parts are on the back panels.



For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

current

V_P 10 V ± 10%

lp typ. 90 mA max. 110 mA

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage

Battery current (V_P = 0 V)

Trickle charge current (V_P = 10 V)

V_B 3 to 4,5 V

lΒ

typ. 1,5 mA typ. -5 mA

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications

	function	terminatio	ns (Fig. 7)
	Tunction	connector 1	connector 2
BI-DIRECTI	ONAL BUSSES		
ADD0 ADD1 ADD2 ADD3 ADD4 ADD5 ADD6 ADD7 ADD8 ADD9 ADD10	Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15, a16,	
APM0 APM1 APM2 APM3 APM4 APM5 APM6 APM7 APM8 APM9 APM10 APM11 APM12	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scartchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM.	a19, c19 a20, c20 a21, c21 a22, c22	

	function	termination	ons (Fig.	7)
	function	connector 1	conn	ector
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU23; commanded by PDBE.	a1 a2 a3 a4 a5		
INPUTS				
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29		
CPSI	Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH).		a4,	c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25		
HOLD	Command from PU23 to stop central processor in DP-phase (active LOW).		a6,	c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus is in high-impedance state.		a1,	c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, ADD-bus function as input, and INS-bus is in high-impedance state.		a2,	c2
PMB ₀ PMB ₁ PMB ₂ PMB ₃ PMB ₄ PMB ₅ PMB ₆ PMB ₇ PMB ₈ PMB ₉ PMB ₁₀ PMB ₁₁ PMB ₁₂ PMB ₁₃ PMB ₁₃ PMB ₁₄ PMB ₁₅	Program memory bits from memory module.	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15		

**************************************		terminatio	ons (Fig. 7)
	function	connector 1	connector 2
PRF	Preparation input/output module finished.	a24	
PRFP	Preparation memory module finished.	a27	
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory locations 002.2 and 002.3.		a10, c10
R/WSM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU23; prepares central processor to store data from PU23 into scratch-pad memory.	c28	•
WPSM	Write pulse for scratchpad memory; signal from PU23 to store data on DIO ₀₋₃ into scartchpad memory		a13, c13
OUTPUTS			
APF	Address processing for input and output modules finished.	a26	
APFP	Address processing for memory modules finished.	a28	
CLOCK	Clock output to PU23.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU23 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB ₀ PB ₁	Page bits, contents of page register, interconnected with PU23.	a17 c17	
PHC ₀ PHC ₁	Phase control to PU23, memory module and input and output modules.	c23 a23	
RCO	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{\text{RCP}}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{\text{RCO}}$ output will also become LOW if $V_P < 9 \text{ V or } > 11 \text{ V}$.	c27	

	function	terminations (Fig. 7)			
		conne	ector 1	connector 2	
RR	Result Register, interconnected with PU23.	a18,	c18		
SBI	Storage command to store data on data bus into output modules and PU23.		c26		
SRI + SRI	System run indication; Darlington transistor output, galvanically isolated by means of opto coupler. SRI + = collector, SRI — = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30	c30		

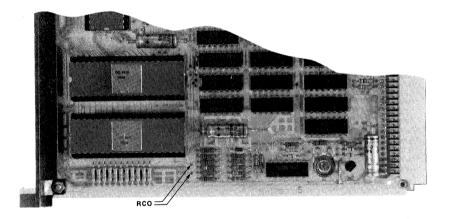


Fig. 3 Location of RCO points.

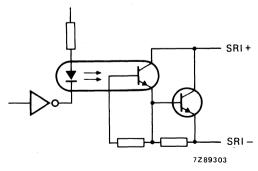


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I $_{\rm Q}$ = max. 100 mA, V $_{\rm CE}$ < 1,5 V; transistor non-conducting: I $_{\rm Q}$ = max. 10 μ A; V $_{\rm CE}$ \leqslant 30 V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Organization of scratchpad memory and page register

The capacity of the scratchpad memory is 2k4, divided into 4 pages of 512 words each, see Fig. 5. Depending on the instruction the scratchpad memory is addressed word by word or bit by bit. The page numbers run from 0 to 3 and the addresses within a page from 000 to 511. When addressing word by word the address notation is 0000 to 0511, 1000 to 1511, 2000 to 2511 or 3000 to 3511. When addressing bit by bit the addresser run from 000.0 to 511.3. This bit by bit addressing can, basically, only be done on page 0; addressing on other pages is possible by using the page register. This register, which has the fixed address 0002, is connected in parallel with the scratchpad memory and is enabled by inserting a wire jump between points PBE on the module, see Fig. 6. When a number 1, 2 or 3 has been stored in this register, the succeeding bit by bit addressing is then carried out on the page indicated by the contents of the page register.

At the end of a DP-phase the contents of the page register is always set to zero, independent of whether the wire jump PBE has been inserted or not.

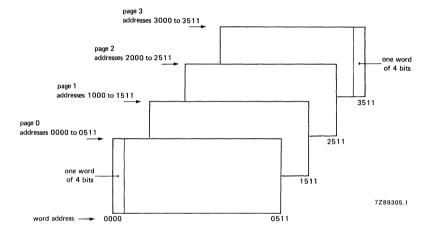


Fig. 5 Schematic presentation of the scratchpad memory.

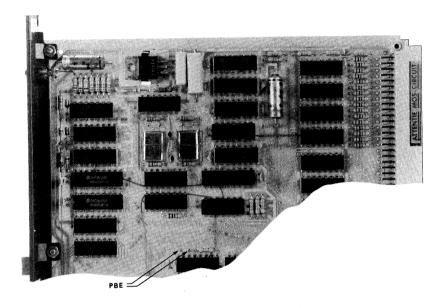


Fig. 6 Location of PBE points.

Fixed scratchpad memory addresses

address	description
0.000	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if V _S ≤ 17,5 V).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.
002.0	Page register.
002.1	1 age register.

MECHANICAL DATA Outlines

Dimensions in mm

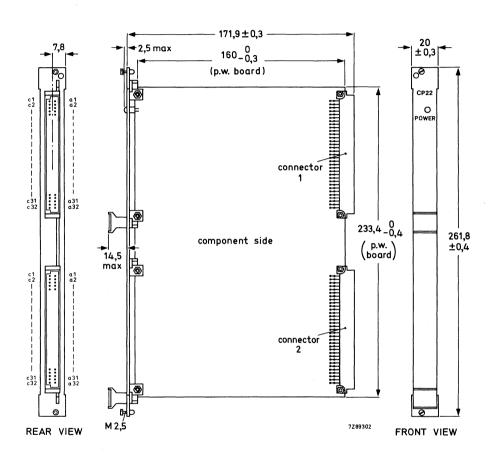


Fig. 7.

Mass

approx. 270 g

Terminal location

	connector 1			connector 2	
row c		row a	row c		row a
PMB ₀	1	INS ₀	PABE	1	PABE
PMB ₁	2	INS ₁	PDBE	2	PDBE
PMB ₂	3	INS ₂	n.c.	3	n.c.
PMB3	4	INS3	CPSI	4	CPSI
PMB ₄	5	INS ₄	CPSC	5	CPSC
PMB ₅	6	ADD_0	HOLD	6	HOLD
PMB ₆	7	ADD ₁	CLOCK	7	CLOCK
PMB ₇	8	ADD_2	n.c.	8	n.c.
PMB ₈	9	ADD_3	n.c.	9	n.c.
PMB ₉	10	ADD_4	RSME	10	RSME
PMB ₁₀	11	ADD ₅	n.c.	11	n.c.
PMB ₁₁	12	ADD ₆	RCP	12	RCP
PMB ₁₂	13	ADD ₇	WPSM	13	WPSM
PMB ₁₃	14	ADD ₈	n.c.	. 14	n.c.
PMB ₁₄	15	ADD_9	n.c.	15	n.c.
PMB ₁₅	16	ADD ₁₀	APM_0	16	APM_0
PB ₁	17	PB _O	APM ₁	.17	APM ₁
RR [.]	18	RŘ	APM ₂	18	APM ₂
DIO ₀	19	DIO ₀	APM_3	19	APM3
DIO ₁	20	DIO ₁	APM4	20	APM ₄
	21	DIO2	APM5	21	APM ₅
DIO_3	22	DIO_3	APM6	22	APM6
PHCO	23	PHC ₁	APM ₇	23	APM ₇
R/WSM	24	PRF.	APM ₈	24	APM ₈
0 V*	25	DEF	APMg	25	APMg
SBI	26	APF	APM ₁₀	26	APM ₁₀
RCO	27	PRFP	APM ₁₁	27	APM ₁₁
WECP	28	APFP	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
SRI	30	SRI+	VB	30	VB
V _n	31	Vn		31	
ν _ρ 0 ν	32	V _р 0 V	V _p 0 V	32	V _р 0 V

n.c. = not connected

^{*} No supply line; is used as return line for control signals.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP24 is for use with other PC20 modules, to assemble a programmable controller. The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The program memory is a C-MOS RAM (2k16). The CP24 has on-board battery back-up and a provision to connect an external battery for longer memory retention.

The capacity of the *scratchpad memory* is ¼k4. Depending on the instruction the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The timer clock circuit provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

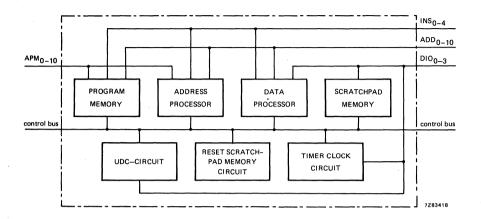


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1 , are:

up-date and check phase (UDC): PHC₀ = 0, PHC₁ = 0;
 reset scratchpad memory (RSM): PHC₀ = 1, PHC₁ = 0;

- data processing (DP): $PHC_0 = 0$, $PHC_1 = 1$;

- data processing (DP): PHC₀ = 0, PHC₁ = 1; - up-date input/output (I/O): PHC₀ = 1, PHC₁ = 1.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

^{*} For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC130-14 or DIN41612 for connectors.

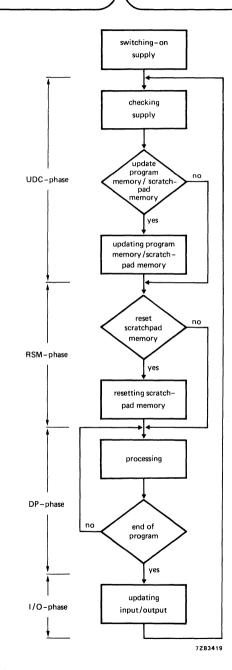


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

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ELECTRICAL DATA

Supply

Supply voltage (d.c.)

current

V_P 10 V ± 10%

Ip max. 250 mA

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.

Battery voltage

Battery current (Vp = 0 V)

Trickle charge current (Vp = 10 V)

Data retention with on-board battery at 40 °C

V_B 3 to 4,5 V

I_B typ. 1,5 mA

typ. $-5 \, \text{mA}$

typ. 30 h, provided the module is in operation for

terminations (Fig. 5)

at least 20 h

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function			(g	- ,
	tunction	connec	tor 1	conne	ctor 2
BI-DIR	ECTIONAL BUSSES				
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁	Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15,	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15		
APM0 APM1 APM2 APM3 APM4 APM5 APM7 APM8 APM8 APM9 APM1	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).			a16, a17, a18, a19, a20, a21, a22, a23, a24, a25, a26,	c16 c17 c18 c19 c20 c21 c22 c23 c24 c25 c26
APM ₁				a27, a28,	c27 c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scratchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM.	a19, a20, a21, a22,	c19 c20 c21 c22		:

	function	terminations (Fig. 5)			
	Tunction	connector 1	conne	ctor 2	
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU23; commanded by PDBE.	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5			
INPUTS					
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29			
CPSD	Central processor slow down; input commanded by PU23.		аЗ,	сЗ	
CPSI	Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH).		a4,	c4	
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored (input current = -5 mA).	a25			
HOLD	Command from PU23 to stop central processor in DP-phase (active LOW).		а6,	c6	
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1,	c1	
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2,	c2	
PRF	Preparation input/output modules finished.	a24			
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 4 mA.		a12,	c12	
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10,	c10	
R/WPM	Write signal from PU23 to central processor, to store data in program memory (active HIGH).		a14,	c14	

	function	terminations (Fig. 5)			
	Tunction	connector 1	conne	ector :	
R/WSM	Read-write level from input and output modules; only effective during I/O-phase.	c24			
WEPC	Write enable signal from PU23; prepares central processor to store data from PU23 into scratchpad memory.	c28			
WPSM	Write pulse for scratchpad memory; signal from PU23 to store data on DIO $_{0-3}$ into scratchpad memory.		a13,	c13	
OUTPUTS	3				
APF	Address processing for input and output modules finished; address stable.	a26			
CLOCK	Clock output to PU23.		а7,	с7	
CPSC	Central processor stop completed; command (HIGH) to PU23 indicating that central processor has been stopped in UDC-phase.		a5,	с5	
PB ₀ PB ₁	Page bits, connected to 0 V.	a17 c17			
PHC ₀ PHC ₁	Phase control to PU23 and input and output modules.	c23 a23			
RCO	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{\text{RCP}}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{\text{RCO}}$ output will also become LOW if $\text{Vp} < 9 \text{ V or} > 11 \text{ V}$.	c27			
RR	Result Register, interconnected with PU23.	a18, c18			
SBI	Storage command to store data on data bus into output modules and PU23.	c26			
SRI + SRI –	System run indication; Darlington transistor output, galvanically isolated by means of opto-coupler. SRI += collector, SRI — = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30 c30			

ints ard

Fig. 3 Location of RCO points and jumper A of the on-board battery.

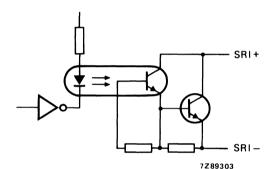


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I_Q = max. 100 mA, $V_{CE} <$ 1,5 V; transistor non-conducting: I_Q = max. 10 μ A; $V_{CE} \leqslant$ 30 V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Fixed scratchpad memory addresses

address	description
0.000	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \le 17,5 \text{ V}$).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA Outlines

Dimensions in mm

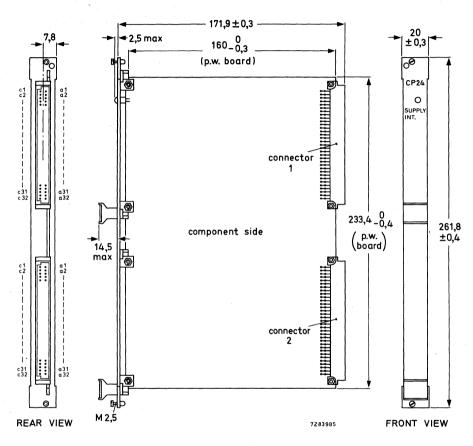


Fig. 5.

Mass

approx. 270 g

Notes

- 1. At delivery of the central processor the on-board battery is switched off (jumper A, Fig. 3, in off-position).
- If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

	connector 1	1		connector 2	?
row c		row a	row c		row a
INS ₀	1	INS ₀	PABE	1	PABE
INS ₁	2	INS ₁	PDBE	2	PDBE
INS ₂	3	INS ₂	CPSD	3	CPSD
INS3	4	INS3	CPSI	4	CPSI
INS4	5	INS4	CPSC	5	CPSC
ADD ₀	6	ADD ₀	HOLD	6	HOLD
ADD ₁	7	ADD_1^{v}	CLOCK	7	CLOCK
ADD_2	8	ADD_2	n.c.	8	n.c.
ADD_3	9	ADD_3^-	n.c.	9	n.c.
ADD4	10	ADD ₄	RSME	10	RSME
ADD ₅	11	ADD ₅	n.c.	11	n.c.
ADD ₆	12	ADD ₆	RCP	12	RCP
ADD ₇	13	ADD ₇	WPSM	13	WPSM
ADD_8	14	ADD ₈	\overline{R}/WPM	14	\overline{R}/WPM
ADD9	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	ADD ₁₀	APM ₀	16	APM ₀
PB ₁	17	PB _O	APM ₁	17	APM ₁
RR	18	RR	APM ₂	18	APM ₂
DIO_0	19	DIO ₀	APM ₃	19	APM_3^-
DIO ₁	20	DIO ₁	APM ₄	20	APM ₄
DIO_2	21	DIO_2	APM ₅	21	APM ₅
$D(O_3^-)$	22	$DIO_3^{\overline{2}}$	APM ₆	22	APM ₆
PHC_0	23	PHC ₁	APM ₇	23	APM ₇
R/WSM	24	PRF	APM ₈	24	APM ₈
0 V*	25	DEF	APM ₉	25	APMg
SBI	26	APF	APM ₁₀	26	APM ₁₀
RCO	27	n.c.	APM ₁₁	27	APM ₁₁
WEPC	28	n.c.	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
SRI-	30	SRI+	VB	30	VB
ν _p 0 ν	-31	V _p	V_{p}	31	V _р 0 V
oν	32	٥٧	0 آ	32	0 ν

n.c. = not connected.

^{*} No supply line; is used as return line for control signals.



INPUT MODULES

DESCRIPTION

These input modules are used with the other PC20 modules to assemble a programmable controller. The IM20 and IM23 are for 24 V and 48 V input levels resp.; both modules can be adapted to drive from 5 V input levels.

The modules contain 16 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. Furthermore, to limit power consumption, these LEDs can be switched-off. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage to increase the noise immunity. The delay time can be increased by adding extra capacitance.

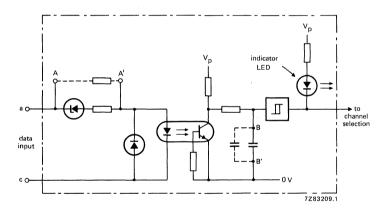


Fig. 1 Circuit diagram of an input stage.

Each input module has 11 address inputs (ADD₀₋₁₀) and 9 module identification inputs (MID₂₋₁₀), which are accessible on the connectors at the rear (Fig. 2).

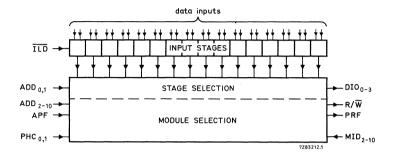


Fig. 2 Block diagram of the input module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip-soldering) or 2422 025 89327 (solder tags).*

For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_{P}	10 V ± 10%
current	lρ	typ. 45 mA (all inputs inactive) typ. 175 mA (all inputs active) max. 200 mA (all inputs active)

Input data

The data inputs are DIW.0 to DIW.3, DIX.0 to DIX.3, DIY.0 to DIY.3 and DIZ.0 to DIZ.3. They are accessible on connector 2, see "Terminal location".

	IM20	IM23	5 V level (note 2)
Active voltage (V _{a-c}) note 1	17 to 30 V	35 to 60 V	3,5 to 6 V
Non-active voltage (V _{a-c})			0 to 0,8 V or floating
Input current, active	typ. 10 mA (at $V_{a-c} = 24 V$)	typ. 5,5 mA (at V _{a-c} = 48 V)	typ. 10 mA (at V _{a-c} = 5 V)

The delay time of the delay circuit can be increased by inserting capacitors (approx. 0,015 μ F/ms) between connecting points B and B' (Fig. 3).

Notes

- 1. V_{a-c} is the voltage between terminal of row a and terminal of row c of connector 2.
- 2. For 5 V-level operation a resistor of 360 Ω ± 5%, style CR25, has to be connected to each input stage between connecting points A and A' (Fig. 3).

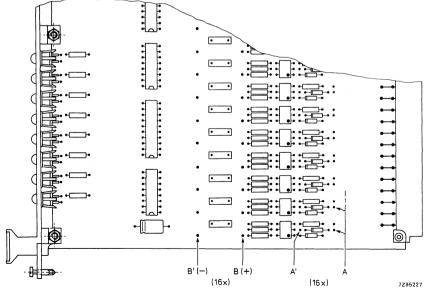


Fig. 3 Part of the printed-wiring board, showing the connecting points for the additional delay capacitors and the resistors for 5 V-level operation.

4322 027 92000 4322 027 94610

The inputs mentioned below meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 4)	
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bits from central processor: ADD ₀₋₁ select a group of 4 input stages, ADD ₂₋₁₀ select the input module.	c11 a11 c12 a12 c13 a13 c14 a14 c15	
APF	Handshake signal; input/output address correct.	a26	
ĪLD	Indication LED disable; input current LOW: 0,1 mA	c28	
MID2 MID3 MID4 MID5 MID6 MID7 MID8 MID9 MID10	Module identification inputs; provide module with individual identity.	c2 c3 c4 c5 c6 c7 c8 c9	
PHC ₀ PHC ₁	Phase control signals.	c23	

Output data

All outputs meet the standard LOCMOS specifications, except the R/\overline{W} and PRF outputs.

output	function	terminations of connector 1 (Fig. 4)	
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits to central processor; data is stored in scratchpad memory of central processor.	c21 a21 c22 a22	
PRF	Preparation of input module finished (open collector output).	a24	
R/W	Signal to central processor (active LOW); prepares central processor for data on DIO ₀₋₃ to be written in the scratchpad memory (open collector output).	c24	

MECHANICAL DATA
Outlines

Dimensions in mm

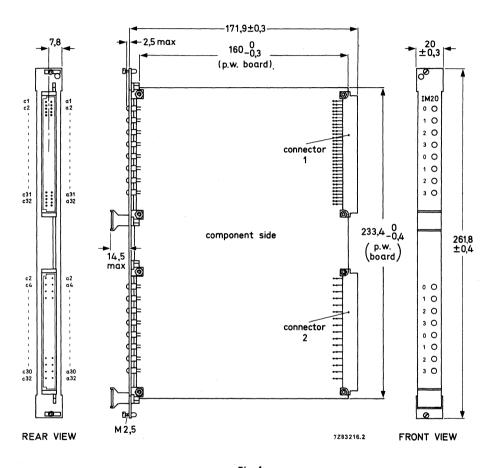


Fig. 4.

Mass

250 g

row a

DI_{W.0}

DIW.1 DIW.2

DIW.3

DIW.3 DIX.0 DIX.1 DIX.2 DIX.3 DIY.0 DIY.1 DIY.2

DIY.3 DIZ.0 DIZ.1 DIZ.2 DIZ.3

connector 2

2

4

6

8

10

Terminal location

	connector 1		
row c		row a	row
n.c.	1	HIGH level	DIW
MID2	2	HIGH level	DΙγ
MID3	3	HIGH level	DΙγ
MID4	4	HIGH level	DIW
MID5	5	HIGH level **	DIX
MID6	6	HIGH level	DI_X
MID7	7	HIGH level	DIX
MID8	8	HIGH level	DIX
MID9	9	HIGH level	DI_Y
MID10	10	HIGH level	DΙγ
ADD_0	11	ADD ₁	DIY
ADD_2	12	ADD_3	DΙγ
ADD ₄	13	ADD ₅	DI_Z
ADD_6	14	ADD ₇	DI_Z
ADD8	15	ADD ₉	DI_Z
ADD ₁₀	16	n.c.	DI_Z
n.c.	17	n.c.	
n.c.	18	n.c.	
n.c.	19	n.c.	
n.c.	20	n.c.	
DIO0	21	DIO ₁	
DIO ₂	22	DIO ₃	
PHC ₀	23	PHC ₁	
R/W	24	PRF	
0 V *	25	n.c.	
n.c.	26	APF	
n.c.	27	n.c.	
ILD	28	n.c.	
n.c.	29	n.c.	
n.c.	30	n.c.	
VP	31	Vp	
0 V	32	0 V	

n.c. = not connected.

^{*} No supply line; is used as return line for control signals.

^{**} For coding MID lines.



INPUT MODULE

DESCRIPTION

This input module is used with the other PC20 modules to assemble a programmable controller.

The input module contains 32 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. The module has 16 LEDs for status indication; with the switch on the front panel they can be connected whether to the 16 inputs with the lowest addresses or to the 16 inputs with the highest addresses. The LEDs are lit when the input stage is active. When the switch is in its middle position all LEDs are switched-off.

A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage to increase the noise immunity.

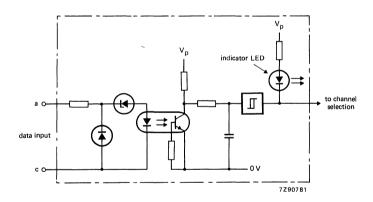


Fig. 1 Circuit diagram of an input stage.

The input module has 11 address inputs (ADD_{0.10}) and 8 module identification inputs (MID₃₋₁₀), which are accessible on the connectors at the rear (Fig. 2).

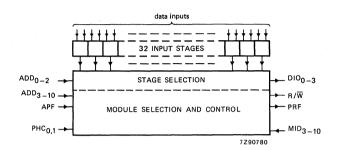


Fig. 2 Block diagram of the input module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm \times 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

supply

Supply voltage (d.c.)	VР	10 V ± 10%
Supply current	lp	typ. 3 mA (all inputs inactive) typ. 140 mA (all inputs active) max.175 mA (all inputs active)

Input data

The data inputs are DIS.0 to DIS.3, DIT.0 to DIT.3, DIU.0 to DIU.3, DIV.0 to DIV.3, DIW.0 to DIW.3, DIX.0 to DIX.3, DIY.0 to DIY.3 and DIZ.0 to DIZ.3. They are accessible on connector 2, see "Terminal location".

Active voltage (V _{a-c})	17 to 30 V
Non-active voltage (V _{a-c})	0 to 7 V or floating
Input current, active at V _{a-c} = 24 V	typ. 10 mA

- * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
- ** V_{a-c} is the voltage between terminal of row a and terminal of row c of connector 2.

The inputs mentioned below meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)	
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄	Address bits from central processor; ADD ₀₋₂	c1' a11 c12 a12	
ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉	select a group of 4 input stages, ADD ₃₋₁₀ select the input module.	a13 c' a14 c' a15	
ADD ₁₀ APF	Handshake signal; input/output address correct.	a26	
MID3 MID4 MID5 MID6 MID7 MID8 MID9 MID10	Module identification inputs; provide module with individual identity.	c3 c4 c5 c6 c7 c8 c9	
PHC ₀ PHC ₁	Phase control signals.	a23	

Output data

All outputs meet the standard LOCMOS specifications, except the R/\overline{W} and PRF outputs.

output	function	terminations of connector 1 (Fig. 3)		
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits to central processor; data is stored in scratchpad memory of central processor.	a21	c21	
PRF	Preparation of input module finished (open collector output).	a24		
R/W	Signal to central processor (active LOW); prepares central processor for data on DIO ₀₋₃ to be written in the scratchpad memory (open collector output).		c24	

MECHANICAL DATA Outlines

Dimensions in mm

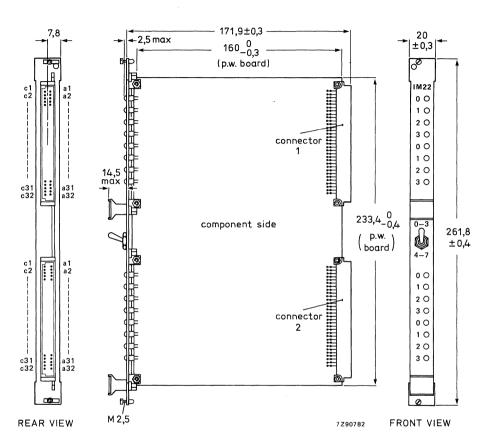


Fig. 3.

Mass

250 g

Terminal location

	connector 1				connector	2
row c		row a		row c		row a
n.c.	1	n.c.		DI _{S.0}	1	DI _{S.0}
n.c.	2	n.c.		DIS.1	2	DIS.1
MID_3	3	HIGH level		DI _{S.2}	3	$DI_{S,2}$
MID_4	4	HIGH level		DI _{S.3}	4	DIS.3
MID_5	5	HIGH level		DIT.0	5	DIT.0
MID ₆	6	HIGH level	> * *	DIT.1	6	DIT.1
MID ₇	7	HIGH level		DIT.2	7	$DI_{T.2}$
MID ₈	8	HIGH level		DIT.3	8	DIT.3
MIDg	9	HIGH level		DIU.0	9	DIU.0
MID ₁₀	10	HIGH level		$DI_{U,1}$	10	DIU.1
ADD_0	11	ADD ₁		DI _{U.2}	11	DI _{U.2}
ADD_2	12	ADD_3		DIU.3	12	DI _{U.3}
ADD_4	13	ADD ₅		DIVO	13	DIV.0
ADD ₆	14	ADD ₇		$DIV_{.1}$	14	DI _{V.1}
ADD8	15	ADD_9		$DIV_{.2}$	15	DI _{V.2}
ADD ₁₀	16	n.c.		DIV.3	16	DI _{V.3}
n.c.	17	n.c.		DIW_{O}	17	DIW_{O}
n.c.	18	n.c.		DIW.1	18	DIW.1
n.c.	19	n.c.		DIW.2	19	DIW.2
n.c.	20	n.c.		DIW_3	20	DI _{W.3}
DIO_0	21	DIO ₁		DIX.0	21	DIX.0
DIO_2	22	DIO3		DIX.1	22	DIX.1
PHC0	23	PHC ₁		DIX.2	23	DIX.2
R/W	24	PRF		DIX.3	24	DIX.3
0 V*	25	n.c.		DIY.0	25	DIY.0
n.c.	26	APF		DIY.1	26	DIY.1
n.c.	27	n.c.		DIY.2	27	DIY.2
n.c.	28	n.c.		DIY.3	28	DIY.3
n.c.	29	n.c.		$DI_{Z,O}$	29	DIZ_{0}
n.c.	30	n.c.		DIZ.1	30	DIZ.1
V_{P}	31	V_{P}		$DI_{Z,2}$	31	$DI_{Z,2}$
0 V	32	0 V		$DI_{Z,3}$	32	$DI_{Z,3}$

n.c. = not connected.

No supply line; is used as return line for control signals.For coding MID lines.

ANALOGUE TO DIGITAL MODULE

DESCRIPTION

This analogue input module is for use with other PC20 modules to assemble a programmable controller. With this module 8 analogue input signals can be processed in a PC20 system.

Analogue to digital conversion is achieved by a 10-bit A/D converter, using the successive approximation technique.

The module converts analogue voltages from 0 to 10 V and currents from 0 to 20 mA or 4 to 20 mA into 3½-digit BCD values from 0000 to 1000, representing 0 to 1000% of the input range. The most significant digit of the values is represented by 1 bit (13th bit). To store these values into the scratch-pad memory of the central processor 4 addresses per input channel have to be reserved (see Fig. 1), that means an address area of max. 32 addresses for 8 inputs. The module has 3 channel select inputs (CHS_{0, 1, 2}) with which the number of analogue inputs to be scanned can be selected. See Table 1 for connection of the CHS inputs and the influence on the address range of the module.

	m	m + 1	m + 2	m + 3	
3					
2					
1					
0	MSB				
		MSD		LSD	

Fig. 1.

m = multiple of 4

 $m_0 = MSB (13th bit)$

 $m_1 = 0$ no assignment

 $m_2 = 1$ if analogue voltage < 10 mV (out of range indication)

 $m_3 = 1$ if analogue voltage > 10.2 V (out of range indication)

Table 1

channel to be scanned	CHS ₀ (SCIO ₀)*	CHS ₁ (SCIO ₁)*	CHS ₂ (SCIO ₂)*		nge of AD20 . (see below)
0 to 7	0	0	0	0 to 31)
1 to 7	1	0	0	4 to 31	
2 to 7	0	1	0	8 to 31	
3 to 7	1	1	0	12 to 31	n = 1 to 7 for CP20, CP21, CP24;
4 to 7	0	0	1	16 to 31	n = 1 to 63 for CP22
5 to 7	1	0	1	20 to 31	
6 and 7	0	1	1	24 to 31	
7	1	1	1	28 to 31	J

^{* 1} if SCIO pads on back panel are bridged;

0 if SCIO pads on back panel are not bridged.

The address range is determined by the coding on the module identification inputs MID₅₋₁₀. If less then 8 analogue input channels are used, the module must be regarded as a complete module for the MID-coding; the addresses which are not used may be occupied by other input/output modules.

The analogue input circuit contains a double-pole multiplexer with 8 inputs, an operational amplifier with 3 gain settings (1, 10 and 12,5), a –2,5 V reference voltage, and an A/D converter, see Fig. 2.

Resistors (50 Ω) are provided for each input to be connected in parallel with the input terminals (terminals Al₀₋₇ + to be connected to terminals R₀₋₇), to obtain both input ranges 0 to 20 mA and 4 to 20 mA. Jumpers are provided for adjustment of the module to the required range; see ADJUSTMENTS FOR OPERATION.

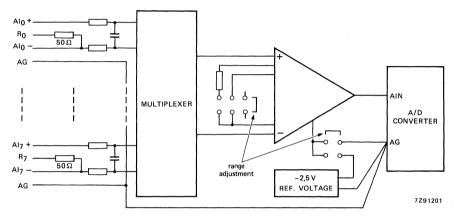


Fig. 2.

The operational amplifier needs a return path for the bias currents, which can be established by connecting terminal AG of the module to the common or earth terminal of the voltage/current input source. An example is shown in Fig. 3.

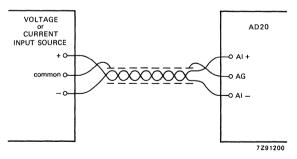


Fig. 3.

The analogue part is electrically isolated from the logic part by means of optocouplers. A d.c./d.c. converter with electrical isolation is provided on the module to generate the required supply voltages for the analogue part, providing complete isolation of the analogue part from both input circuit supply (Vs) and logic supply (Vp).

After the AD20 (in a PC20 system) has been switched on the module starts scanning the analogue input with the lowest number, dependent on the selection made on the CHS inputs, and stores the value in a buffer memory. The module continues scanning the other channels, and after channel 7 has been scanned it switches over to data exchange with the scratchpad memory of the central processor. When the data exchange has been finished a new scanning of the analogue inputs starts.

The scanning time per channel is 100 µs. When the time between end of scanning and data exchange exceeds 100 ms the module automatically starts a new scanning.

The module has a 3-digit display that enables monitoring of the inputs; channel selection is done with the thumbwheel switch. The display gives a 3-digit number without a decimal point. As the AD20 handles analogue input voltages up to 10,23 V (3½-digit) the ½ digit is represented by 3 decimal points, so values greater than 999 are displayed as x.x.x.

The whole circuitry is built on an epoxy printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 5) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply voltage (d.c.) Supply current for input circuitry	V _S I _S	24 V ± 25% max. 90 mA
Supply voltage (d.c.) Supply current logic	V _P I _P	10 V \pm 10% max. 120 mA
Current input (input impedance 50 Ω ± 0,1%)	0 to 20 mA o	or 4 to 20 mA
Voltage input (input impedance \geq 10 M Ω)	0 to 10 V	
	max. error	max, temp, coefficient
Accuracy	max. ciroi	mara comp. coomoione
O to 10 mV range	± 0,1%	+ 30 × 10 ⁻⁶ /K
•		
0 to 10 mV range	± 0,1%	+ 30 × 10 ⁻⁶ /K
0 to 10 mV range 0 to 20 mA range	± 0,1% ± 0,4%	+ 30 × 10 ⁻⁶ /K + 60 × 10 ⁻⁶ /K
0 to 10 mV range 0 to 20 mA range 4 to 20 mA range	± 0,1% ± 0,4% ± 0,4%	+ 30 × 10 ⁻⁶ /K + 60 × 10 ⁻⁶ /K

For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input and output data

All inputs and outputs, except the PRF and $R/\overline{W}SM$ outputs meet the standard LOCMOS specifications.

	function	terminations of connector 1 (Fig. 5)				
INPUTS						
ADD ₀ ADD ₁		c11 a11				
ADD ₂ ADD ₃		c12 a12				
ADD ₅	Address bits from central processor.	c13 a13				
ADD ₆ ADD ₇ ADD ₈		c14 a14 c15				
ADD8 ADD ₉ ADD ₁₀		a15 c16				
APF	Handshake signal, indicates that addresses are correct.	a26				
CHS ₀ CHS ₁ CHS ₂	Channel select inputs.	c17 c18 c19				
MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	c5 c6 c7 c8 c9 c10				
PHC ₀ PHC ₁	Phase control signals.	c23 a23				
RCO	Reset from central processor	c27				
OUTPUTS						
DIO ₀ DIO ₁	Data hita ta agatual avaganay	c21 a21				
DIO ₂ DIO ₃	Data bits to central processor.	c22 a22				
PRF	Preparation of addressing AD20 finished (open collector output).	a24				
R/WSM	Read-write level for central processor (open collector output).	a26				

	function	tion terminations connector 2	
ANALOGUE	E INPUTS		
AI ₀ + AI ₀ - R ₀ AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a10 a9	c10 c8/c9
AI ₁ + AI ₁ - R1 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a12 a11	c12 c11
Al ₂ + Al ₂ – R2 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a14 a13	c14 c13
Al ₃ + Al ₃ – R3 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a16 a15	c16 c15
Al ₄ + Al ₄ R4 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a18 a17	c18 c17
Al ₅ + Al ₅ – R5 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a20 a19	c20 c19
Al ₆ + Al ₆ – R6 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a22 a21	c22 c21
Al ₇ + Al ₇ – R7 AG	Positive terminal Negative terminal 50 Ω input resistor terminal Analogue ground	a24 a23	c24 c23/c26

ADJUSTMENTS FOR OPERATION

The input range can be selected by positioning the jumpers A and B (Fig. 4) as shown below.

input range	position of jumpers A	position of jumper B	relation between measured value and data (D) stored in scratchpad memory
0 to 10 V	0 0 0 0 0	0 0	D = 100 Vi
0 to 20 mA	0 0 0 0 0	0 0 0	D = 50 Ii
4 to 20 mA	0 0 0 0 0 0	0 0 0	D = 62,5 (Ii – 4)

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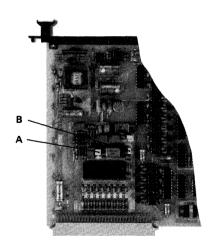


Fig. 4 Location of jumpers for adjustment of input range.

MECHANICAL DATA Outlines

Dimensions in mm

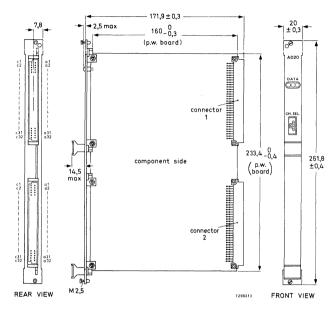


Fig. 5.

Mass

approx. 270 g

Terminal location

	connector	1			connector 2	
row c		row a		row c		row a
n.c.	1	n.c.		n.c.	1	n.c.
n.c.	2	n.c.		n.c.	2	n.c.
n.c.	3	n.c.		n.c.	3	n.c.
n.c.	4	n.c.		n.c.	4	n.c.
MID ₅	5	HIGH level)	n.c.	5	n.c.
MID ₆	6	HIGH level		n.c.	6	n.c.
MID ₇	7	HIGH level	**	n.c.	7	n.c.
MID ₈	8	HIGH level		AG	8	n.c.
MID ₉	9	HIGH level		AG	9	R_0
MID ₁₀	10	HIGH level	,	AI ₀ —	10	AI ₀ +
ADD_0	11	ADD ₁		AG	11	R ₁
ADD ₂	12	ADD3		Al ₁ –	12	Al ₁ +
ADD ₄	13	ADD ₅		AG	13	R ₂
ADD ₆	14	ADD ₇		Al ₂ –	14	Al ₂ +
ADD8	15	ADD ₉		AG	15	R ₃
ADD ₁₀	16	n.c.		Al3 -	16	Alg+
CHS ₀	17	HIGH level)	AG	17	R_4
CHS ₁	18	HIGH level	A	AI4	18	Al ₄ +
CHS ₂	19	HIGH level	J	AG	19	R ₅
n.c.	20	n.c.		AI ₅ —	20	Al ₅ +
DIO ₀	21	DIO ₁		AG	21	R ₆
DIO ₂	22	DIO3		AI ₆ —	22	AI ₆ +
PHC ₀	23	PHC ₁		AG	23	R ₇
R/WSM	24	PRF		AI7 —	24	Al7 +
0 V*	25	n.c.		n.c.	. 25	n.c.
n.c.	26	APF		AG	26	n.c.
RCO	27	n.c.		n.c.	27	n.c.
n.c.	28	n.c.		n.c.	28	n.c.
n.c.	29	n.c.		n.c.	29	n.c.
n.c.	30	n.c.		n.c.	30	n.c.
V_{P}	31	V _P		0 V	31	v_S
0 V	32	0 V		n.c.	32	n.c.

n.c. = not connected.

^{*} No supply line, is used as return line for control signals.

^{**} For coding MID lines.

[▲] For coding CHS lines.

PROGRAM MEMORY MODULE

DESCRIPTION

This memory module is for use with central processor CP22 and other PC20 modules to assemble a programmable controller.

The MM20 is an 8 k 16 EPROM memory. It is supplied with 8 empty EPROMs, type 2716, which can be programmed on the programming unit PU20.

The 8 IC-sockets for the EPROMs are marked 0-1, 2-3, 4-5, or 6-7, for A and B type EPROMs, indicating the address range of the socket.

EPROMs should be inserted into the sockets as follows:

EPROMs (A and B) with addresses 0000 to 2047 into sockets 0-1 (A and B):

EPROMs (A and B) with addresses 2048 to 4095 into sockets 2-3 (A and B):

EPROMs (A and B) with addresses 4096 to 6143 into sockets 4-5 (A and B);

EPROMs (A and B) with addresses 6144 to 8191 into sockets 6-7 (A and B).

The memory module is built on a glass-epoxy double Euro-card* (233,4 mm x 160 mm) with two F068-1 connectors (male parts); the corresponding female parts are on the back panels.

ELECTRICAL DATA

Supply

Supply voltage (d.c.) current

V_P 10 V ± 10% I_P max. 550 mA (module filled with 8 EPROMs)

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 2)		
	Tunction	connector 1	connector 2	
INPUTS				
APFP	Address processing finished; when LOW addresses may change.	a28		
APM0 APM1 APM2 APM3 APM4 APM5 APM6 APM7 APM8 APM9 APM10 APM11 APM11	Address bits for program memory.		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28	
PHC ₀	Phase control line.	c23		
OUTPUTS				
PMB0 PMB1 PMB2 PMB3 PMB4 PMB5 PMB6 PMB7 PMB8 PMB9 PMB10 PMB10 PMB11 PMB12 PMB13 PMB14 PMB15	03 EPROM A 04 EPROM A 05 EPROM A 06 EPROM A 07 EPROM B 01 EPROM B 02 EPROM B 03 EPROM B 04 EPROM B 05 EPROM B 06 EPROM B 07 EPROM B 07 EPROM B 00 EPROM A 01 EPROM A 01 EPROM A 02 EPROM A	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15		
PRFP	Output indicating that preparation for reading data has been finished and data is available on outputs PMB $_{0-15}$ (active when PHC $_{0}$ is LOW).	a27		

Time data

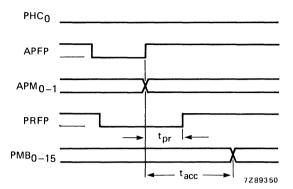
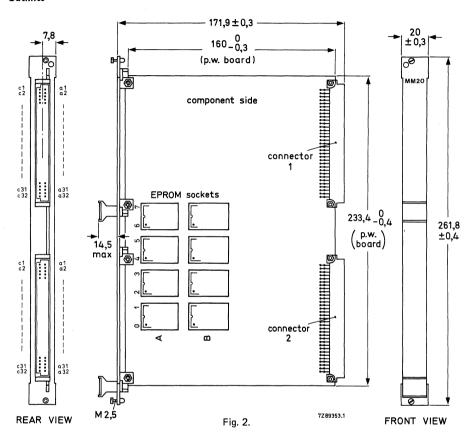


Fig. 1 Read-out of program memory during DP-phase.

Preparation time	^t pr	max.	350 ns
Access time	tacc	max.	525 ns

MECHANICAL DATA
Outlines

Dimensions in mm



Mass

approx. 310 g

Terminal location

	connector 1			connector 2	2
row c		row a	row c		row a
PMB ₀	1	n.c.	n.c.	1	n.c.
PMB ₁	2	n.c.	n.c.	2	n.c.
PMB ₂	3	n.c.	n.c.	3	n.c.
PMB_3^-	4	n.c.	n.c.	4	n.c.
PMB ₄	5	n.c.	n.c.	5	n.c.
PMB ₅	6	n.c.	n.c.	6	n.c.
PMB ₆	7	n.c.	n.c.	7	n.c.
PMB ₇	8	n.c.	n.c.	8	n.c.
PMB ₈	9	n.c.	n.c.	9	n.c.
PMB ₉	10	n.c.	n.c.	10	n.c.
PMB ₁₀	11	n.c.	n.c.	11	n.c.
PMB ₁₁	12	n.c.	n.c.	12	n.c.
PMB ₁₂	13	n.c.	n.c.	13	n.c.
PMB ₁₃	14	n.c.	n.c.	14	n.c.
PMB ₁₄	15	n.c.	n.c.	15	n.c.
PMB ₁₅	16	n.c.	APM _O	16	APM_{O}
n.c.	17	n.c.	APM ₁	17	APM ₁
n.c.	18	n.c.	APM ₂	18	APM ₂
n.c.	19	n.c.	APM ₃	19	APM ₃
n.c.	20	n.c.	APM ₄	20	APM ₄
n.c.	21	n.c.	APM ₅	21	APM ₅
n.c.	22	n.c.	APM ₆	22	APM ₆
PHC ₀	23	n.c.	APM ₇	23	APM ₇
n.c.	24	n.c.	APM ₈	24	APM ₈
n.c.	25	n.c.	APM ₉	25	APM ₉
n.c.	26	n.c.	APM ₁₀	26	APM ₁₀
n.c.	27	PRFP	APM ₁₁	27	APM ₁₁
n.c.	28	APFP	APM ₁₂	28	APM ₁₂
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V _р 0 V	31	V_{p}	V _p 0 V	31	V _р 0 V
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

PROGRAM MEMORY MODULES

DESCRIPTION

These memory modules are for use with central processor CP22 and other PC20 modules to assemble a programmable controller.

The two modules are identical, except for the program memory capacity: 8 k 16 C-MOS RAM for the MM21, 4 k 16 C-MOS RAM for the MM22. The modules have an on-board battery for data retention (30 h) in case the supply voltage is switched off. An external battery can be connected for longer memory retention.

Each module is built on a glass-epoxy double Euro-card* (233,4 mm x 160 mm) with two F068-I connectors (male parts); the corresponding female parts are on the back panels.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V _P	10 V ± 10%
current	l _n	typ. 110 mA
carrent	ίP	max. 150 mA

Requirements of the back-up battery

Battery voltage V_B 3 to 4,5 V Battery current (Vp = 0 V) I_B typ. 1,5 mA Trickle charge current (Vp = 10 V) typ. -5 mA Data retention with on-board battery at 40 °C typ. 30 h, pp

typ. 30 h, provided the module has been in operation for at least 20 h.

Note

When the supply voltage drops below 7 V the C-MOS RAM memory is automatically switched to the stand-by position, so that the battery can take over the supply of the memory as soon as V_P falls below V_B .

^{*} For a general description of the Euro-card system see IEC 127 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

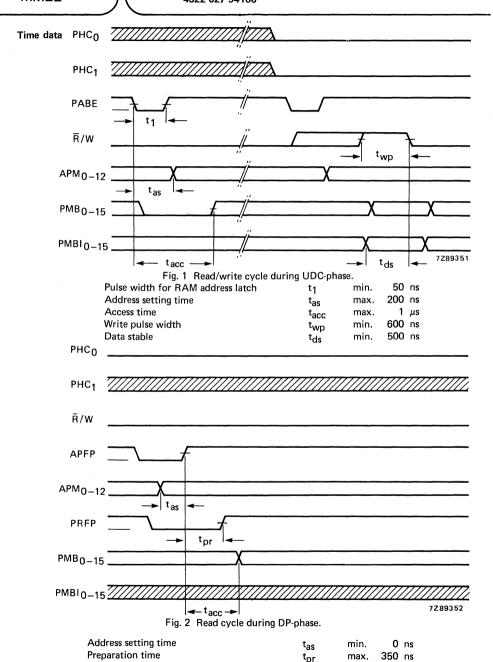
4322 027 92080 4322 027 94160

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations	terminations (Fig. 3)		
	lunction	connector 1	connector 2		
INPUTS					
APFP	Address processing finished; when LOW addresses may change, when goes HIGH address on APM ₀₋₁₂ is clocked into the address latch in the RAM (active when PHC ₀ is LOW).	a28			
APM0 APM1 APM2 APM3 APM4 APM5 APM6 APM7 APM8 APM9 APM10 APM11 APM12	Address bits for program memory.		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28		
PABE	Input to clock address on APM ₀₋₁₂ into the address latch in the RAM.		a1, c1		
PHC ₀ PHC ₁	Phase control lines	c23 a23			
PMBIO PMBI1 PMBI2 PMBI3 PMBI4 PMBI5 PMBI6 PMBI7 PMBI8 PMBI9 PMBI10 PMBI11 PMBI11 PMBI12 PMBI13 PMBI14 PMBI15	Data inputs for program memory bits.	a1 a2 a3 a4 a5 a6 a7 a8 a9 a10 a11 a12 a13 a14 a15 a16			
R/W	Read/write input. When HIGH data on PMBI ₀₋₁₅ is written into the RAM only when PHC ₀ and PHC ₁ are LOW.		a14, c14		

	function	termination	ıs (Fig. 3)
	function	connector 1	connector 2
OUTPUTS	·		
PMB0 PMB1 PMB2 PMB3 PMB4 PMB5 PMB6 PMB7 PMB8 PMB9 PMB10 PMB11 PMB12 PMB13 PMB13 PMB14 PMB15	Data output of program memory. The output stage is built-up with transistor drive circuit with pull-up resistor (2,2 k Ω). The sink capability is max. 3 mA.	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15	
PRFP	Output indicating that preparation for reading data has been finished and data is available on outputs PMB ₀₋₁₅ (active when PHC ₀ is LOW).	a27	

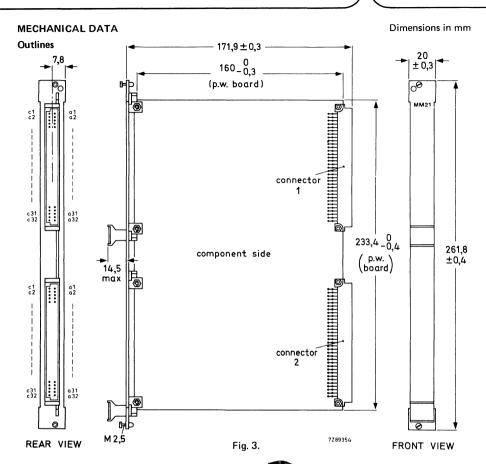


600 ns

max.

tacc

Access time



Mass

approx. 270 g

Notes

- When the program memory module is delivered, the on-board battery is switched off (jumper A, Fig. 4).
- If the program memory module is removed from the rack, ensure that it is placed on an insulated surface to prevent short-circuiting of the on-board battery.

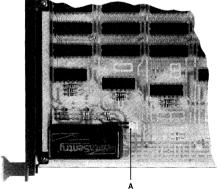


Fig. 4.

Terminal location

	connector 1			connector 2	
row c		row a	row c		row a
PMB _O	1	PMBI ₀	PABE	1	PABE
PMB ₁	2	PMBI ₁	n.c.	2	n.c.
PMB ₂	3 .	PMBI ₂	n.c.	3	n.c.
PMB3	4	PMBI3	n.c.	4	n.c.
PMB ₄	5	PMBI ₄	n.c.	- 5	n.c.
PMB ₅	6	PMBI ₅	n.c.	6	n.c.
PMB ₆	7	PMBI6	n.c.	7	n.c.
PMB ₇	8	PMB17	n.c.	8	n.c.
PMB ₈	9	PMBI ₈	n.c.	9	n.c.
PMB ₉	10	PMBIg	n.c.	10	n.c.
PMB ₁₀	11	PMBI ₁₀	n.c.	11	n.c.
PMB ₁₁	12	PMBI ₁₁	n.c.	12	n.c.
PMB ₁₂	13	PMBI ₁₂	n.c.	13	n.c.
PMB ₁₃	14	PMBI ₁₃	R∕W	14	R/W
PMB ₁₄	15	PMBI ₁₄	n.c.	15	n.c.
PMB ₁₅	16	PMBI ₁₅	APM ₀	16	APM_{O}
n.c.	17	n.c.	APM ₁	17	APM ₁
n.c.	. 18	n.c.	APM ₂	18	APM ₂
n.c.	19	n.c.	APM_3^-	19	APM_3^-
n.c.	20	n.c.	APM ₄	20	APM_4
n.c.	21	n.c.	APM ₅	21	APM ₅
n.c.	22	n.c.	APM ₆	22	APM ₆
PHC ₀	23	PHC ₁	APM ₇	23	APM_7
n.c.	24	n.c.	APM ₈	24	APM ₈
n.c.	25	n.c.	APMg	25	APM ₉
n.c.	26	n.c.	APM ₁₀	26	APM ₁₀
n.c.	27	PRFP	APM ₁₁	27	APM ₁₁
n.c.	28	APFP	APM ₁₂	28	APM ₁₂
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V_p	31	Vp	V_p	31	V_{p}
oν	32	ο ν	oν	32	0 V

n.c. = not connected.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 16 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs have grounded loads. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

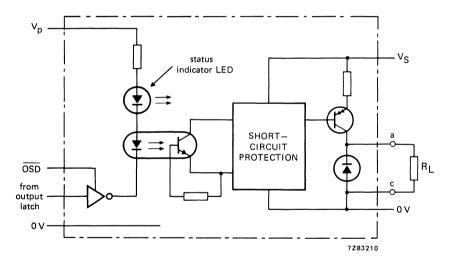


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs (ADD₀₋₁₀) and 9 module identification inputs (MID₂₋₁₀), which are accessible on the connectors at the rear (Fig. 2).

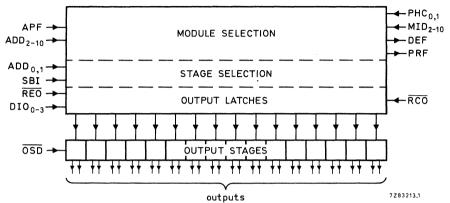


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.) Supply current	logic	V _P I _P	10 V ± 10% typ. 120 mA (all stages ON) max. 150 mA (all stages ON) typ. 25 mA (all stages OF F)
Supply voltage (d.c.) Supply current (excluding load current)	for output circuitry	V _S I _S	24 ± 25%** typ. 75 mA (all stages ON) max. 110 mA (all stages ON) typ. 50 mA (all stages OFF)

- * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
- ** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)
ADD ₀ ADD ₁		c11 a11
ADD ₂ ADD ₃		c12 a12
ADD ₄ ADD ₅	Address bits from central processor; ADD ₀₋₁ select a group of four output stages,	c13
ADD ₆ ADD ₇	ADD ₂₋₁₀ select the output module.	c14 a14
ADD ₈ ADD ₉		c15
ADD ₁₀		c16
DIO ₀ DIO ₁	Data bits from central processor; data are stored in output stages by SBI.	c21 a21
DIO ₂ DIO ₃	stored in output stages by opi.	a22
REO	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA.	a27
RCO	Reset from central processor (low level) during switch-on.	c27
MID2 MID3 MID4 MID5 MID6 MID7 MID8 MID9 MID10	Module identification inputs; provide module with individual identity.	c2 c3 c4 c5 c6 c7 c8 c9
SBI	Clock signal from central processor to output module, stores data on DIO _{0.3} into output stages during input/output cycle.	c26
PHC ₀ PHC ₁	Phase control signals.	c23 a23
APF	Handshake signal; input/output address correct.	a26
OSD	Output stage disable for all stages; input current LOW: 10 mA.	a28

Output data

The data outputs are DO $_{W.0}$ to DO $_{W.3}$, DO $_{X.0}$ to DO $_{X.3}$, DO $_{Y.0}$ to DO $_{Y.3}$ and DO $_{Z.0}$ to DO $_{Z.3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_1 = 48 \Omega$.

Output transistor conducting: R $_L$ = 48 $\Omega;$ V $_{a\text{-}c}{}^*$ = min. V $_{S}{}^-$ 1,5 V. Output transistor non-conducting: I $_{0}$ = max. 2 mA at V $_{S}$ = 30 V.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 6A per module)

for all stages

for maximum 12 stages

max. 0,375 A per stage max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA Outlines

Dimensions in mm

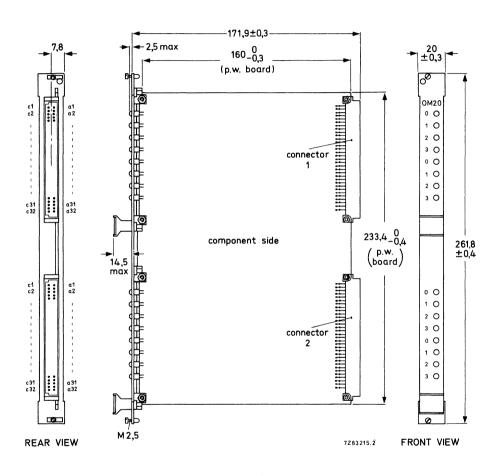


Fig. 3.

Mass

230 g

Terminal location

	connector 1				connector :	2
row c		row a		row c		row a
n.c.	1	HIGH level	1	0 V	1	٧s
MID ₂	2	HIGH level		0 V	2	DÖ _{W.0}
MID3	3	HIGH level		0 V	3	v_S
MID4	4	HIGH level		0 V	4	DO _{W.1}
MID5	5	HIGH level	**	0 V	5	v_{s}
MID6	6	HIGH level		0 V	6	DO _{W.2}
MID7	7	HIGH level		0 V	7	٧s
MIDg	8	HIGH level	j	0 V	8	DOW.3
MID9	9	HIGH level		0 V	9	٧s
MID 10	10	HIGH level)	0 V	10	DOX.0
ADD ₀	11	ADD ₁		0 V	11	٧s
ADD ₂	12	ADD3		0 V	12	$DO_{X.1}$
ADD ₄	13	ADD ₅		0 V	13	٧s
ADD ₆	14	ADD ₇		0 V	14	DO _{X.2}
ADD8	15	ADD ₉		0 V	15	V_{S}
ADD ₁₀	16	n.c.		0 V	16	DOX.3
n.c.	17	n.c.		0 V	17	v_S
n.c.	18	n.c.		. 0 V	18	DOY.0
n.c.	19	n.c.		0 V	19	v_S
n.c.	20	n.c.		0 V	20	DOY.1
DIO	21	DIO ₁		0 V	21	v_S
DIO ₂	22	DIO3		0 V	22	DOY.2
PHC _O	23	PHC ₁		0 V	23	V_S
n.c.	24	PRF		0 V	24	DOY.3
0 V *	25	DEF		0 V	25	v_S
SBI	26	APF		0 V	26	$DO_{Z,0}$
RCO	27	REO		0 V	27	VS
n.c.	28	OSD		0 V	28	DOZ.1
n.c.	29	n.c.		0 V	29	v_S
n.c.	30	n.c.		0 V	30	$DO_{Z,2}$
VP	31	V_{P}		0 V	31	v_S
0 V	32	0 V		0 V	32	$DO_{Z,3}$

n.c. = not connected.

Note

Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

No supply line; is used as return line for control signals.
 For coding MID lines.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 8 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are grounded load outputs. Each output stage has a voltage regulator diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages feature electronic short-circuit protection, i.e. when a short circuit occurs the relevant output stage is switched off automatically, and is indicated via the short-circuit indication output (SCI). After removing the short circuit the output stage can be reactivated via the REO input.

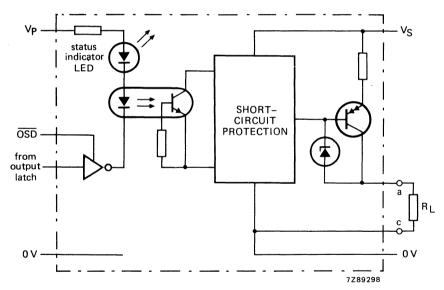


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs (ADD $_{0.10}$) and 10 module identification inputs (MID $_{1.10}$) which are accessible on the connectors at the rear (Fig. 2).

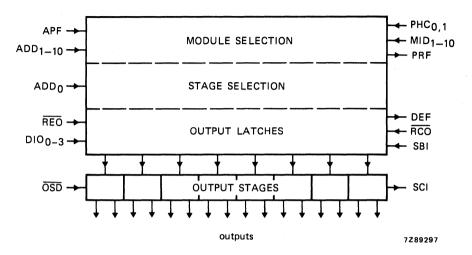


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.) Supply current	logic	V _P I _P	10 V ± 10% typ. 65 mA (all stages ON) max. 75 mA (all stages ON) typ. 5 mA (all stages OFF)
Supply voltage (d.c.) Supply current (excluding load current)	for output circuitry	V _S I _S	24 ± 25%** typ. 115 mA (all stages ON) max. 160 mA (all stages ON) typ. 35 mA (all stages OFF)

^{*} For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

^{**} If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations connector 1	
ADD ₀		a11	c11
ADD ₂ ADD ₃		a12	CIZ
ADD ₄	Address bits from central processor; ADD ₀ select	4.2	c13
ADD ₅	a group of four output stages, ADD ₁₋₁₀ select	a13	
ADD ₆	the output module.		c14
ADD ₇		a14	-15
ADD ₈ ADD ₉		a15	c15
ADDg ADD ₁₀		10	с16
DIO		p	c21
DIO ₁	Data bits from central processor; data are	a21	OL.
DIO ₂	stored in output stages by SBI.	1	c22
DIO3		a22	
REO	Reset output module input; a low level on this input will reset all output latches and the short-circuit protection circuitry (output transistor non-conducting; input current LOW: 10 mA).	a27	
RCO	Reset from central processor (low level) during switch-on.		c27
MID ₁			c1
MID ₂		1	c2
MID ₃		•	с3
MID4		:	c4
MID ₅	Module identification inputs; provide module		с5
MID ₆	with individual identity.		c6
MID ₇	,		c7 c8
MID ₈ MID ₉	·	1	c9
MID ₁₀		:	c10
SBI	Clock signal from central processor to output module, stores data on DIO ₀₋₃ into output stages during input/output cycle.	1	c26
PHC ₀ PHC ₁	Phase control signals.	a23	c23
APF	Handshake signal; input/output address correct.	a26	
ŌSD	Output stage disable for all stages; input current LOW: 10 mA.	a28	

Output data

The data outputs are DO_{Y.0} to DO_{Y.3} and DO_{Z.0} to DO_{Z.3}. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_1 = 12 \Omega$.

Output transistor conducting: R $_L$ = 12 $\Omega;$ V $_{a\text{-}c}{}^*$ = min. V $_S$ –1,5 V. Output transistor non-conducting: I $_0$ = max. 2 mA at V $_S$ = 30 V.

For load inductance, see Fig. 3.

Output current (limited to 8 A per module)

for all stages

for maximum 4 stages

max. 1 A per stage max. 2 A per stage

Output SCI is an open-collector output; drive capability max. 20 mA. In case of a short circuit in one of the output stages, the output transistor is conducting: $V_{SCI} = \text{max. } 0.5 \text{ V}$ (with respect to 0 V - line); transistor non-conducting: $V_{SCI} = 30 \text{ V}$.

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 4)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25

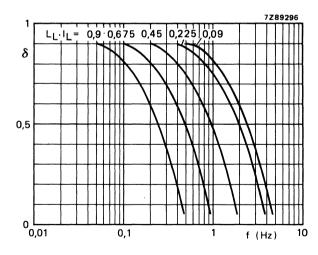


Fig. 3 Maximum duty factor (δ) as a function of switching frequency at different L_LI_L - products (L_L = load inductance; I_L = load current).

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA Outlines

Dimensions in mm

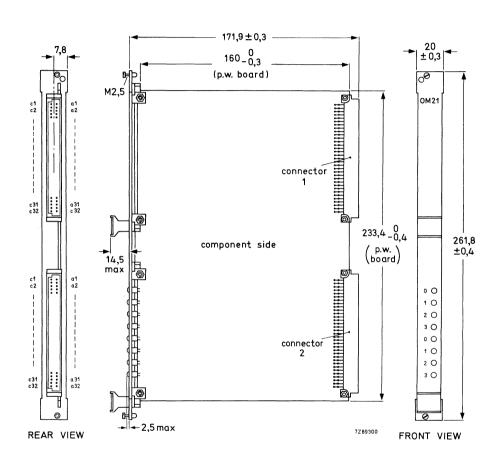


Fig. 4.

Mass

230 g

Terminal location

connecto	r 1		C	connector 2	2
row c	row a		row c		row a
MID ₁ 1	HIGH level)	0 V	1	V_S
MID_2 2	HIGH level		0 V	2	SČI
MID_3 3	HIGH level		0 V	3	v_S
MID ₄ 4	HIGH level		0 V	4	DOY.0
MID ₅ 5	HIGH level	**	0 V	5	٧s
MID_6 6	HIGH level		0 V	6	DŎ _{Y.1}
MID_7 7	HIGH level		0 V	7	٧ _S
MID ₈ 8	HIGH level		0 V	8	DÖ _{Y.1}
MID ₉ 9	HIGH level		0 V	9	V_S
MID ₁₀ 10	HIGH level)	0 V	10	DO _{Y.2}
ADD ₀ 11	ADD ₁		0 V	11	v_{S}
ADD ₂ 12	ADD ₃		0 V	12	DÖ _{Y.2}
ADD ₄ 13	ADD ₅		0 V	13	v_S
ADD ₆ 14	ADD ₇		0 V	14	DOY.3
ADD ₈ 15	ADD ₉		0 V	15	v_{S}
ADD ₁₀ 16	n.c.		0 V	16	$DO_{Y.3}$
n.c. 17	n.c.		0 V	17	$V_{\mathbf{S}}$
n.c. 18	n.c.		0 V	18	DÖ _{Z.0}
n.c. 19	n.c.		0 V	19	v_{s}
n.c. 20	n.c.		0 V	20	$DO_{Z,0}$
DIO ₀ 21	DIO ₁		0 V	21	v_{S}
DIO_2 22	DIO3		0 V	22	DÖZ.1
PHC_0 23	PHC ₁		0 V	23	v_S
n.c. 24	PRF		0 V	24	DÖZ.1
0 V * 25	DEF		0 V	25	v_S
SBI 26	APF		0 V	26	$DO_{Z,2}$
RCO 27	REO		0 V	27	٧ _S
n.c. 28	OSD		0 V	28	DO _{Z.2}
n.c. 29	n.c.		0 V	29	VS
n.c. 30	n.c.		0 V	30	DO _{Z.3}
V _P 31	V _P		0 V	31	٧s
0 V 32	0 V		0 V	32	DÖ _{Z.3}

n.c. = not connected.

Supply-voltage lines (V_S) have to be connected to each output.

^{*} No supply line; is used as return line for control signals.

^{**} For coding MID lines.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 32 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other. Each output stage has a suppressor diode, to allow it to switch inductive loads.

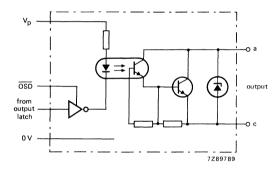


Fig. 1 Circuit diagram of an output stage.

To obtain a pull-down facility for the first 16 output stages, e.g. to drive TTL circuitry, the module has two 16-pin sockets (S₃ and S₄, Fig. 5), to provide insertion of adapter headers to which pull-down resistors are soldered. (See also Output Data.)

The output module has 11 address inputs (ADD₀₋₁₀) and 8 module identification inputs (MID₃₋₁₀), which are accessible on the connectors at the rear (Fig. 2).

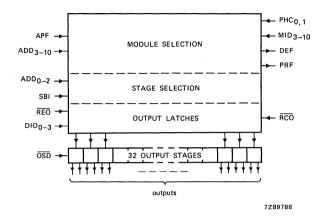


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under

catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.) ۷p 10 V ± 10% logic Supply current lρ typ. 340 mA (all stages ON) max. 400 mA (all stages ON) typ. 1 mA (all stages OFF)

^{*} For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 5)
ADD ₀ ADD ₁ ADD ₂		c11 a11 c12 a12
ADD ₃ ADD ₄ ADD ₅	Address bits from central processor; ADD ₀₋₂ select a group of four output stages,	c13 a13
ADD ₆ ADD ₇ ADD ₈	ADD ₃₋₁₀ select the output module.	c14 a14 c15
ADD ₉ ADD ₁₀		a15 c16
APF	Handshake signal; input/output address correct.	a26
DIO ₀	Data bits from central processor; data are	c21
DIO ₂	stored in output stages by SBI.	c22 a22
MID ₃ MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	c3 c4 c5 c6 c7 c8 c9 c10
OSD	Output stage disable for all stages; input current LOW: 10 mA.	a28
PHC ₀ PHC ₁	Phase control signals.	c23 a23
RCO	Reset from central processor (low level) during switch-on.	c27
REO	Reset output module input; a low level on this input will reset all outputs latches (output transistor non-conducting); input current LOW: 10 mA.	a27
SBI	Clock signal from central processor to output module, stores data in DIO ₀₋₃ into output stages during input/output cycle.	c26

Output data

The data outputs are DOS.0 to DOS.3, DOT.0 to DOT.3, DOU.0 to DOU.3, DOV.0 to DOV.3, DOW.0 to DOW.3, DOX.0 to DOX.3, DOY.0 to DOY.3 and DOZ.0 to DOZ.3. They are accessible on connector 2, see Terminal location.

Output transistor conducting: output current = max. 100 mA at V_{a-c}^* = max. 1,5 V. Output transistor non-conducting: output current = max. 10 μ A at V_{a-c}^* = max. 30 V.

Each output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H.

Note: If a supply voltage of 5 V is required, e.g. to drive TTL circuitry, pull-down resistors (R, Figs 3 and 4) must be used. These resistors can be soldered to adapter headers, which have to be inserted into sockets S_3 and S_4 (Figs 3 and 5). The emitter-output on terminal c31 of connector 2 must be connected to the 0 V-line of the external supply voltage V_S (Fig. 4); this output can then only be used in common emitter configuration.

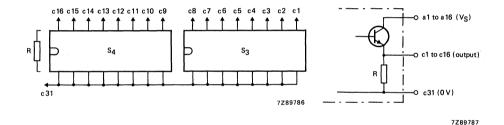


Fig. 3.

Fig. 4.

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 5)
DEF	Data exchange finished.	a25
PRF	Preparation of output module finished.	a24

MECHANICAL DATA Outlines

Dimensions in mm

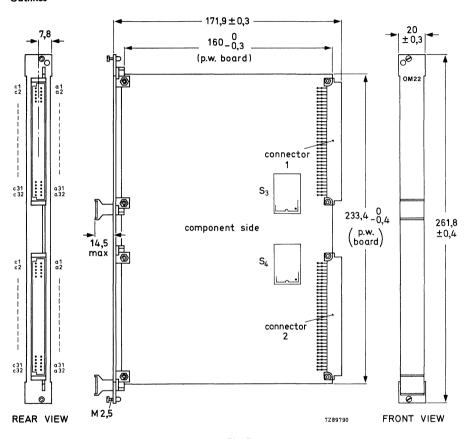


Fig. 5.

Mass

approx. 230 g

Terminal location

	connector 1			connector 2	
row c	19. 19. 19. 19. 19. 19. 19. 19. 19. 19. 19.	row a	row c		row a
n.c.	1	HIGH level	DO _{S.0}	1	DO _{S.0}
n.c.	2	HIGH level	DO _{S 1}	2	DO _{S 1}
MID ₃	3	HIGH level	DOs 2	3	DOc 2
MID_4	4	HIGH level	DO _{S.3}	4	DOc 3
MID ₅	5	HIGH level **	DO _{T 0}	5	DOT n
MID ₆	6	HIGH level	DO _{T.1}	6	DOT 1
MID_7	7	HIGH level	$DO_{T,2}$	7	DOT 2
MIDA	8	HIGH level	$DO_{T.3}$	8	DOT 3
MID9	9	HIGH level	$DO_{U,0}$	9	DOU.0
MID ₁₀	10	HIGH level	DO _{U.1}	10	DOU.1
ADD_0	11	ADD ₁	DO _{U.2}	11	$DO_{U,2}$
ADD_2	12	ADD3	DO _{U.3}	12	DOU.3
ADD_4	13	ADD ₅	$DO_{V,O}$	13	$DO_{V,0}$
ADD ₆	14	ADD ₇	$DO_{V,1}$	14	$DO_{V,1}$
ADD8	15	ADD ₉	$DO_{V,2}$	15	$DO_{V,2}$
ADD ₁₀	16	n.c.	$DO_{V.3}$	16	DO _{V 3}
n.c.	17	n.c.	DO_{W} O	17	$DO_{W,0}$
n.c.	18	n.c.	DO _{W.1}	18	DOW.1
n.c.	19	n.c.	DO _{W.2}	19	DOw.2
n.c.	20	n.c.	$DO_{W,3}$	20	DO _{W 3}
DIO ₀	21	DIO ₁	$DO_{X,0}$	21	DOXU
DIO ₂	22	DIO3	DO _{X.1}	22	$DO_{X,1}$
PHC ₀	23	PHC ₁	DO _{X.2}	23	DO _{X 2}
n.c.	24	PRF	$DO_{X.3}$	24	$DO_{X,3}$
0 V*	25	DEF	DOY.0	25	DOV 0
SBI	26	APF	DO _{Y.1}	26	DO _{Y 1}
RCO	27	REO	$DO_{Y,2}$	27	DOY 2
n.c.	28	OSD	$DO_{Y,3}$	28	DO _{Y 3}
n.c.	29	n.c.	$DO_{Z,0}$	29	DO ₇ 0
n.c.	30	n.c.	DOZ.1	30	DO ₇ 1
V _P	31	VP	DO _{Z 2} (0 V)▲	31	DO _{7 2}
0 V	32	0 V	DOZ.3	32	DO _{Z.3}

n.c. = not connected.

^{*} No supply line; is used as return line for control signals.

^{**} For coding MID lines.

^{▲ 0-}line of V_S when pull-down resistors are used.

SUPPLY AND OUTPUT MODULE

DESCRIPTION

This supply and output module is used with the other PC20 modules to assemble a programmable controller.

The module contains 8 addressable output stages, a 24 V/10 V d.c.-d.c. converter and an alarm circuit for the 24 V supply. The output stages have photo-isolators between external and internal circuitry (Fig. 1). All outputs have a grounded load. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

The 24 V/10 V d.c.-d.c. converter provides the logic supply voltage for a small controller system with galvanic isolation from the external 24 V supply. Furthermore, it is short-circuit protected and two or more of these modules may be connected in parallel for higher current demands in larger systems.

The alarm circuit monitors the 24 V supply (V_{ic}) , providing two alarm outputs. One of these is accessible for external use (hardware); the other can be used internally for processing (software). Furthermore, a LED on the front panel indicates that V_{ic} is above its minimum specified level.

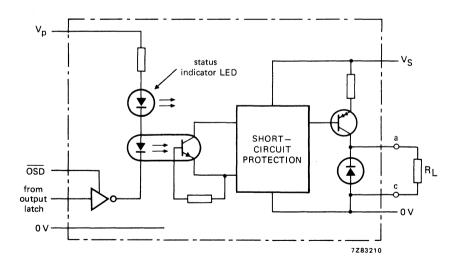


Fig. 1 Circuit diagram of an output stage.

The output part has 11 address inputs (ADD₀₋₁₀) and 10 module identification inputs (MID₁₋₁₀), which are accessible on the connectors at the rear (Fig. 2).

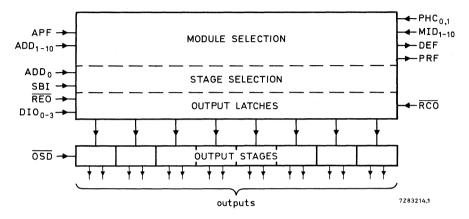


Fig. 2 Block diagram of the output part.

The circuits are built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	for	V_S	24 V ± 25%**
Supply current (excluding load current)	output circuitry		typ. 50 mA (all stages (ON) max. 60 mA (all stages ON) typ. 30 mA (all stages OFF)
Supply voltage (d.c.)	for	V_{ic}	24 V ± 25%
Supply current, at $V_{ic} = 24 \text{ V}$ and output current $I_p = 1,7$		l _{ic}	typ. 1,1 A

^{*} For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

^{**} If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	termination connector	
ADD ₀ ADD ₁		a11	c11
ADD ₂ ADD ₃		a12	c12
ADD ₅	Address bits from central processor; ADD ₀ selects a group of four output stages,	a13	c13
ADD6	ADD ₁₋₁₀ select the (output) module.		c14
ADD ₇ ADD ₈		a14	c15
ADD ₉ ADD ₁₀		a15	c16
DIO			c21
DIO ₁	Data bits from central processor; data are stored in output stages by SBI.	a21	c22
DIO3	stored in output stages by 3b1.	a22	022
REO	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA.	a27	
RCO	Reset from central processor (low level) during switch-on.		c27
MID1 MID2 MID3 MID4 MID5 MID6 MID7 MID8 MID9 MID10	Module identification inputs; provide module with individual identity.		c1 c2 c3 c4 c5 c6 c7 c8 c9
SBI	Clock signal from central processor to output module, stores data on DIO ₀₋₃ into output stages during input/output cycle.		c26
PHC ₀ PHC ₁	Phase control signals.	a23	c23
APF	Handshake signal; input/output address correct.	a26	
ŌŚŌ	Output stage disable for all stages; input current LOW: 0,1 mA.	a28	

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Output data

The data outputs are $DO_{Y,0}$ to $DO_{Y,3}$ and $DO_{Z,0}$ to $DO_{Z,3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_1 = 48 \Omega$.

Output transistor conducting: $R_L = 48 \Omega$; $V_{a-c}^* = min. V_{S}-1,5 V$.

Output transistor non-conducting: $I_0 = \text{max. 2 mA}$ at $V_S = 30 \text{ V}$.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 3 A per module)

for all stages

for maximum 6 stages

max. 0,375 A per stage max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25
ALI	Alarm internal; active LOW as long as V _{ic} is above 17,5 V; with opto-coupler isolation between internal and external supply.	a29 c29

The external alarm output ALE (connector 2, a2) has a similar function as ALI. It is an open collector output and can sink a current of 10 mA ($V_{ALE\ LOW}$ = 1,3 V).

Converter output

Output voltage

 V_{P}

10 V ± 10%

Output current

ĺρ

max. 1,7 A; short-

circuit proof **

Vp: on terminals a31, c31 of connector 10 V: on terminals a32, c32 of connector 1

^{*} Voltage between terminal of row a and terminal of row c of connector 2.

^{**} If two or more modules are connected in parallel the output current per module is max. 1,5 A.

MECHANICAL DATA Outlines

Dimensions in mm

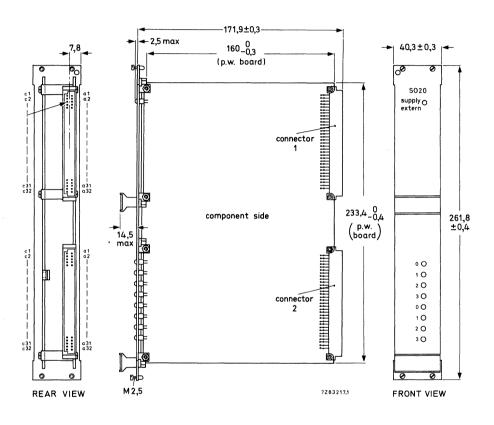


Fig. 3.

Mass

400 g

Terminal location

	connector '				connector 2	
row c		row a		row c		row a
MID ₁	1	HIGH level)	n.c.	1	n.c.
MID ₂	2	HIGH level		0 V *	2	ALE
MID3	3	HIGH level	1	n.c.	3	n.c.
MID ₄	4	HIGH level		0 V *	4	Vic
MID ₅	5	HIGH level	! **	n.c.	5	n.c.
MID6	6	HIGH level		0 V *	6	V _{ic}
MID7	7	HIGH level		n.c.	7	n.c.
MID8	8	HIGH level		0 V *	8	Vic
MID9	9	HIGH level	į	0 V	9	٧s
MID ₁₀	10	HIGH level	J	0 V	10	n.c.
ADD_0	11	ADD ₁		0 V	11	v_S
ADD ₂	12	ADD3		0 V	12	n.c.
ADD_4	13	ADD ₅		0 V	13	V_S
ADD ₆	14	ADD ₇		0 V	14	n.c.
ADD ₈	15	ADD ₉		0 V	15	٧s
ADD ₁₀	16	n.c.		0 V	16	n.c.
n.c.	17	n.c.		0 V	17	VS
n.c.	18	n.c.		0 V	· 18	DOY.0
n.c.	19	n.c.		0 V	19	V_{S}
n.c.	20	n.c.		0 V	20	DÖ _{Y.1}
DIO ₀	21	DIO ₁		0 V	21	v_S
DIO ₂	22	DIO3		0 V	22	DOY.2
PHC ₀	23	PHC ₁		0 V	23	v_S
n.c.	24	PRF		0 V	24	DOY.3
0 V ***	25	DEF		0 V	25	v_s
SBI	26	<u>APF</u>		0 V	26	DÖZ.0
RCO	27	REO		0 V	27	٧s
n.c.	28	OSD		0 V	28	$DO_{Z,1}$
ALI	29	ALI		0 V	29	٧s
n.c.	30	n.c.		0 V	30	$DO_{Z,2}$
V _P	31	V_{P}		0 V	31	v_s
0 V	32	0 V		0 V	32	DO _{Z.3}

n.c. = not connected.

Note

Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

- 0 V for V_{ic.} For coding MID-lines.
- No supply line; is used as return line for control signals.

DIGITAL TO ANALOGUE MODULE

This output module is for use in PC20 programmable controllers if an analogue voltage or current output level is required. The module contains four 3-decade D/A converters, which accept 3-digit BCD data from the scratchpad memory of the central processor in the PC20 system. Each converter has a voltage output (0 to 9,99 V) and a current output (0 to 20 mA or 4 to 20 mA) in a grounded load configuration (0 to 500 Ω). The output current range is selected by means of jumper connectors on the module.

Four addresses in the scratchpad memory are reserved for each output (Fig. 1), that means an address area of 16 addresses for 4 outputs. The address range is determined by the coding on the module identification inputs MID₄₋₁₀.

When the module is switched on in the PC20 system all data latches on the DA20 are set to 0.

The module has a 3-digit display that enables monitoring of the outputs; channel selection is done with the thumbwheel switch.

	m	m + 1	m + 2	m + 3	
3					
2					
1					
0					
	MSD		LSD		

Fig. 1 Address arrangement in the scratchpad memory.

The addresses m+3 are not used.

m = multiple of 4.

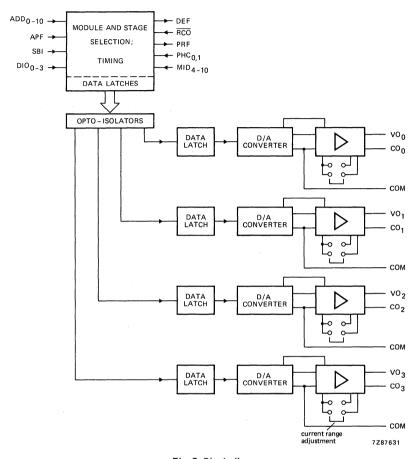


Fig. 2 Block diagram.

The whole circuitry is built on an epoxy printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dipsoldering) or 2422 025 89326 (solder tags).*

^{*} For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply voltage (d.c.) for input circuitry	V _S I _S	24 V ± 25% max. 250 mA
Supply voltage (d.c.) logic	V _P I _P	10 V ± 10% max. 60 mA
Output current ranges		0 to 20 mA selectable 4 to 20 mA by jumper
Maximum output impedance of current output		500 Ω
Output voltage range		0 to 9,99 V
Minimum output impedance of voltage output		2 kΩ
Non-linearity of D/A converters		± 1 LSB
Accuracy of voltage to current conversion (current output is derived from voltage output)		± 0.25%

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Input and output data

All inputs meet the standard LOCMOS specifications.

	function	terminatio connector	
INPUTS			
ADD ₀ ADD ₁ ADD ₂ ADD ₃		a11	c11 c12
ADD ₄ ADD ₅ ADD ₆ ADD ₇	Address bits from central processor.	a13	c13 c14
ADD ₈ ADD ₉ ADD ₁₀		a15	c15 c16
APF	Handshake signal, indicates that addresses are correct.	a26	
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits from central processor.	a21	c21
MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	-	c4 c5 c6 c7 c8 c9
PHC ₀ PHC ₁	Phase control signals.	a23	c23
RCO	Reset signal from central processor, to reset all data latches.		c27
SBI	Clock signal from central processor to clock data into latches.		c26

	function	terminati connecto	ons of r 1 (Fig. 4)
OUTPUT	s		
DEF	Data exchange finished (open collector output).	a25	
PRF	Preparation of addressing DA20 finished (open collector output).	a24	
	function	terminati connecto	ons of r 2 (Fig. 4)
ANALOG	EUE OUTPUTS		
vo ₀	Voltage output of channel 0	a4	
COM	Current output of channel 0 Common	a2	c2/c4
vo ₁	Voltage output of channel 1	a8	
CO ₁	Current output of channel 1 Common	a6	c6/c8
VO ₂	Voltage output of channel 2	a12	
CO ₂	Current output of channel 2 Common	a10	c10/c12
VO ₃	Voltage output of channel 3	a16	
COM	Current output of channel 3 Common	a14	c14/c16

ADJUSTMENTS FOR OPERATION

For the 4 channels the output current range can be selected by positioning the jumpers 0, 1, 2 and 3 (Fig. 3) as shown below.

output current range	position of the relative jumper*
0 to 20 mA	0 0
4 to 20 mA	0 0

^{*} Module in position as shown in Fig. 3.

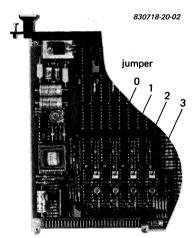


Fig. 3 Location of jumpers for adjustment of output current range.

MECHANICAL DATA Outlines

Dimensions in mm

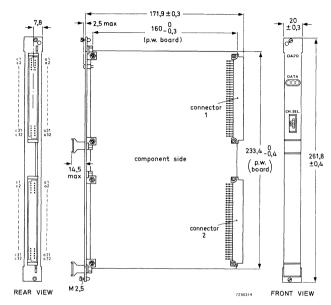


Fig. 4.

Mass

approx. 270 g

Terminal location

	connector 1			connector 2	
row c		row a	row c		row a
n.c.	1	n.c.	n.c.	1	n.c.
n.c.	2	n.c.	COM	2	co _o
n.c.	3	n.c.	n.c.	3	n.c.
MID ₄	4	HIGH level	COM	4	vo_0
MID ₅	5	HIGH level	n.c.	5	n.c.
MID ₆	6	HIGH level	COM	6	CO ₁
MID ₇	7	HIGH level \ **	n.c.	7	n.c.
MID ₈	8	HIGH level	COM	8	vo ₁
MIDg	9	HIGH level	n.c.	9	n.c.
MID ₁₀	10	HIGH level J	COM	10	CO ₂
ADD_0	11	ADD ₁	n.c.	11	n.c.
ADD_2	12	ADD3	COM	12	V02
ADD_4	13	ADD ₅	n.c.	13	n.c.
ADD ₆	14	ADD ₇	COM	14	CO3
ADD8	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	n.c.	COM	16	V03
n.c.	17	n.c.	n.c.	17	n.c.
n.c.	18	n.c.	n.c.	18	n.c.
n.c.	19	n.c.	n.c.	19	n.c.
n.c.	20	n.c.	n.c.	20	n.c.
DIO ₀	21	DIO ₁	n.c.	21	n.c.
DIO ₂	22	DIO ₃	n.c.	22	n.c.
PHC ₀	23	PHC ₁	n.c.	23	n.c.
n.c.	24	PRF	n.c.	24	n.c.
0 V*	25	DEF	n.c.	25	n.c.
SBI	26	APF	n.c.	26	n.c.
RCO	27	n.c.	n.c.	27	n.c.
n.c.	28	n.c.	n.c.	28	n.c.
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V_P	31	V _P	0 V	31	v_S
0 V	32	0 V	n.c.	32	n.c.

n.c. = not connected.

No supply line, is used as return line for control signals.For coding MID lines.

BIDIRECTIONAL PARALLEL INTERFACE

DESCRIPTION

The RP20 is intended for use as an interface between a PC20-system and data input and output devices, e.g. thumbwheel switches, seven-segment displays, etc.

The module has 16 enable outputs, each of which can select an eight-bit input or output device, so it has a capacity of 16 x 8 bits and therefore it occupies 32 four-bit places in the input/output field. When an enable output selects an input device, this device will put 8 bits of information on the data lines. This data information is stored in the buffer memory of the RP20. When an output device is selected, data is transferred from the buffer memory to this device. The lower enable lines always select outputs; inputs are selected by the remaining lines. Separation between these two groups is done by means of the SCIO inputs, which determine the number of outputs that are scanned.

Enabling always starts at EN_0 and finishes at EN_{15} . The scanning rate can be chosen by means of switches on the module.

After having activated successively all enable outputs the RP20 stops scanning, activates its READY output and enables the central processor to get access to the buffer memory. Data exchange between central processor and RP20 takes place during the I/O-phase in which the RP20 is scanned. As soon as the central processor finishes this I/O-phase, the RP20 disables the central processor access to its memory and starts scanning the inputs and outputs, provided the START input is at the high level. If the START input is at the low level, scanning is postponed until this level is high again. During scanning the RP20 ignores the addressing of the central processor; this does not influence the cycle time of the PC20-system.

The start procedure is initiated by a low level on the RCO input. First all buffer memory locations of the RP20 are set to 0, then there will be a data exchange between the scratchpad memory of the central processor and the buffer memory of the RP20. At the moment central processor finishes the I/O-phase, the RP20 starts scanning the input and output devices.

Data lines, enable lines, READY output and START input are electrically isolated from the PC20 circuitry by means of photocouplers.

Although the system is designed for use in combination with input and output devices requiring 24 V supply, the RP20 can be adapted for use with devices for 5 V supply by means of a jumper on the printed-wiring board.

The RP20 is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply			
Supply voltage (d.c.)		V_{P}	10 V ± 10%
Supply current		Ι _Ρ	max. 150 mA ($V_P = 10 \text{ V}$, all outputs used, all data 0)
Supply voltage (d.c.)	for	Vs*	24 V ± 25%
Supply current	output	IS	max. 250 mA (all data lines at low level) min. 20 mA (all data lines at high level)
Supply voltage (d.c.)	for	V_S^*	5 V ± 5%**
Supply current	output	IS	max. 250 mA (all data lines and inverting inputs at low level, 4 enable lines inverted) min. 20 mA (all data lines at high level)

^{*} The value of V_S depends on the supply voltage and signal levels required for the input and output devices.

^{**} To be adjusted by means of a jumper; see 'ADJUSTMENTS'.

Input and output data

The inputs at connector 1 meet the standard LOCMOS specifications; the inputs and outputs at connector 2 are electrically isolated from the logic part by means of photocouplers.

	function	ter	terminations (Fig. 7)			
	tanotion	conne	ctor 1	connec	ctor 2	
INPUTS						
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bits from central processor; ADD ₀₋₄ select the memory position on the module, ADD ₅₋₁₀ select the module.	a11 a12 a13 a14 a15	c11 c12 c13 c14 c15 c16			
APF	Handshake signal, indicates that addresses are correct.	a26				
INVI	Input that inverts input information; input current LOW: 10 mA.			a24		
ĪNVO	Input that inverts output information; input current LOW: 10 mA.				c24	
MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.		c5 c6 c7 c8 c9 c10			
PHC ₀ PHC ₁	Phase control signals from central processor.	a23	c23			
RCO	Reset from central processor (low level) during switch-on.		c27			
SCIO ₀ SCIO ₁ SCIO ₂ SCIO ₃	Input/output separation code inputs, control the R/\overline{W} line to central processor, and determine whether data is received or sent on DB ₀₋₇ .		c17 c18 c19 c20		,	
START	A high level (24 V) starts a scanning cycle of the RP20; if this input is kept HIGH permanently, scanning starts immediately after the I/O cycle during which data was exchanged; input current high: 10 mA. For 5 V-level operation, see 'ADJUSTMENTS'.				c20	

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		terminations (Fig. 7)			
	function	connecto	r 1	conne	ctor :
BI-DIREC	CTIONAL BUSES				
010 ₀ 010 ₁ 010 ₂ 010 ₃	Data bits to and from central processor.	a21	21		
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	These external data bus terminals form outputs when the enable outputs of the first group are activated, and inputs during activation of the second group. A "1" in the scratchpad memory of the central processor will be represented as a high level at these outputs, provided INVO input is at high level (or floating). If INVO input is at low level a "1" will be represented as a low level. A high level at these inputs will be represented in the scratchpad memory as a "0" when the INVI input is at the high level (or floating). A low level of the INVI input causes a high level to become a "1". DB ₀₋₇ occupy two four-bit places in the scratchpad memory; DB ₀₋₃ occupy the lower place, DB ₄₋₇ occupy the higher place. Input current low (I _{iI}): 10 mA; output current low (I _{OI}): max. 15 mA; see Fig. 1.			a26 a28 a30 a32	c26 c28 c30 c32
OUTPUTS ENO EN1 EN2 EN3 EN4 EN5 EN6 EN7 EN8 EN10 EN11 EN11 EN12 EN113 EN14 EN15	Enable outputs (open collector); select an input or output device. During the scanning period of the RP20, these outputs go successively to the low level, enabling an input device to put its information on DB ₀₋₇ , or an output device to store the information from this bus. For devices requiring a high level for enabling, see 'ADJUSTMENTS'. Each enable output corresponds with two four-bit places; the lower enable lines refer to the lower scratchpad places. Output current: max. 120 mA at 0,5 V.			a2 a4 a6 a8 a10 a12 a14 a16	c2 c4 c6 c8 c10 c12 c14 c16

	function	termination	ns (Fig. 7)
	Tunction	connector 1	connector 2
DEF	Data exchange finished (open collector output)	a25	
PRF	Preparation of RP20 finished (open collector output)	a24	
READY	A low level indicates that RP20 finished I/O scanning (open collector output); output current low: max. 20 mA at 0,5 V.		a20
R/W	A low level indicates that the central processor has to receive data (open collector output).	c24	

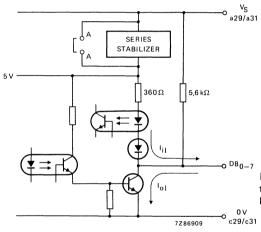


Fig. 1 External data bus circuit. Points A to be bridged for 5 V supply, see "ADJUST-MENTS".

Time data (see also Figs 2 and 3)

Scanning time for one input or output
Time that scanning pulse is active
Time that input information must become stable

Time between two scanning pulses

Time between enable output active and output data valid

Time that output data remains valid

Total scanning time

 t_{O} $t_{SC} = 0.8 t_{O}$

 $t_{v} = \text{max. } 0.7 \ t_{0} - 50 \ \mu \text{s}$

 $t_1 = 0.2 t_0$

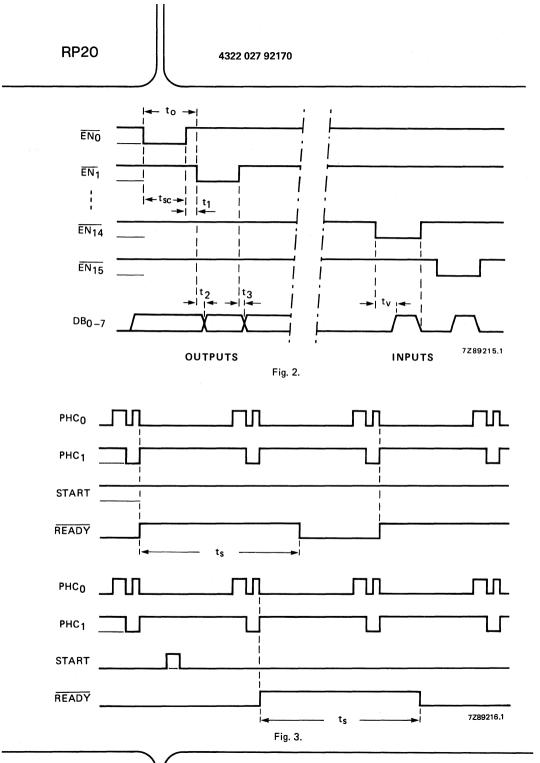
 $t_2 = max. 40 \mu s$

 $t_3 = 0.1 t_0$

 $t_s = 16 t_O$

To be adjusted with switches on the module, see 'ADJUSTMENTS'.

t_s	to
ms	μs
5,12	320
10,24	640
20,48	1280
40,96	2560



ADJUSTMENTS

Adjustment for use with devices requiring 5 V supply

If the input and output devices require 5 V levels, the supply voltage (V_S) should be 5 V. By bridging the points A (Figs 1 and 5) with a jumper, the module is adapted for 5 V supply.

Adjustment for 5 V level operation on START input

For 5 V level operation on the START input, a resistor of 360 Ω should be connected between the points B (Figs. 4 and 5).

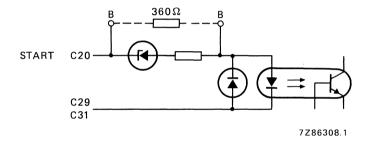


Fig. 4.

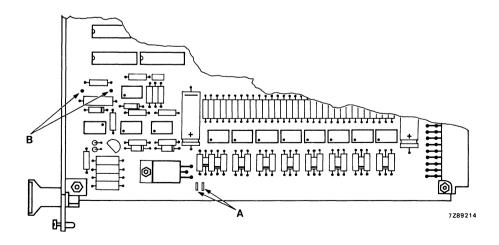


Fig. 5.

Adjustment for use with devices requiring a high level for enabling

For devices which require a high level for enabling, it is necessary to invert the outputs \overline{EN}_0 , \overline{EN}_1 , \overline{EN}_{14} and \overline{EN}_{15} by means of switches on the printed-wiring board (Fig. 6). The following points have to be connected:

```
point 1 to point 16: EN<sub>14</sub> is inverted;
point 2 to point 15: EN<sub>1</sub> is inverted;
point 3 to point 14: EN<sub>15</sub> is inverted;
point 4 to point 13: EN<sub>0</sub> is inverted.
Proper functioning is only possible if the 5 V-jumper is used (Fig. 5).
```

For inverting purposes a transistor BC337 with common emitter and a resistor of 4700 Ω between base and emitter have been added; the collector has been connected to output CT (termination c18, connector 2), the base to input BT (termination a18, connector 2).

Adjustment of scanning time

The total scanning time (t_s, Fig. 3) can be adjusted with switches on the printed-wiring board (Fig. 6). A choice can be made of the following connections:

```
point 5 to point 12: t_s = 40.96 ms;
point 6 to point 11: t_s = 10.24 ms;
point 7 to point 10: t_s = 20.48 ms;
point 8 to point 9: t_s = 5.12 ms.
```

Note: Only one connection should be made.

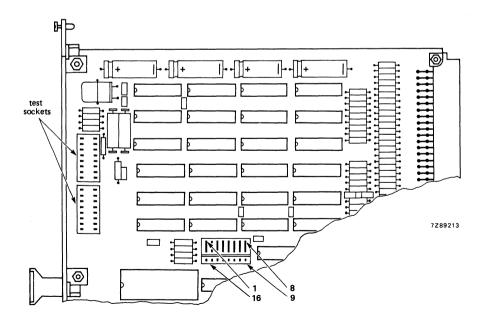


Fig. 6.

MECHANICAL DATA Outlines

Dimensions in mm

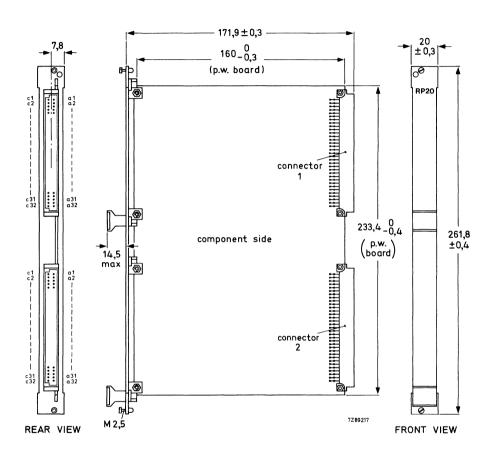


Fig. 7.

Mass approx. 270 g

Terminal location

c	onnector 1			connector 2	?
row c		row a	row c		row a
n.c.	1	n.c.	n.c.	1	n.c.
n.c.	2	n.c.	EN ₁	2	EN ₀
n.c.		n.c.	n.c.	3	n.c.
n.c.	4	n.c.	EN ₃	4	EN ₂
MID ₅	5	HIGH level	n.c.	5	n.c.
MID ₆	6	HIGH level	ĒN ₅	6	EN ₄
MID ₇	7	HIGH level	n.c.	7	n.c.
MID8	8	HIGH level	EN ₇	8	EN ₆
MIDg	9	HIGH level	n.c.	9	n.c.
MID ₁₀	10	HIGH level	ĒNg	10	EN ₈
ADD_0	11	ADD ₁	n.c.	11	n.c.
ADD_2	12	ADD3	EN ₁₁	12	EN ₁₀
ADD4	13	ADD ₅	n.c.	13	n.c.
ADD ₆	14	ADD ₇	EN ₁₃	14	EN ₁₂
ADD8	15	ADD_{9}	n.c.	15	n.c.
ADD ₁₀	16	n.c.	EN ₁₅	16	EN ₁₄
SCIO	17	HIGH level	n.c.	17	n.c.
SCIO ₁	18	HIGH level	СТ	18	BT
SCIO	19	HIGH level	n.c.	19	n.c.
SCIO ₃	20	HIGH level	START	20	READY
DIO	21	DIO ₁	n.c.	21	n.c.
DIO ₂	22	DIO3	n.c.	22	n.c.
PHCO	23	PHC ₁	n.c.	23	n.c.
R/W	24	PRF	ĪNVO	24	INVI
0 V	25	DEF	n.c.	25	n.c.
SBI	26	APF	DB ₁	26	DB_0
RCO	27	n.c.	n.c.	27	n.c.
n.c.	28	n.c.	DB ₃	28	DB ₂
n.c.	29	n.c.	0V	29	∨ _S *¯
n.c.	30	n.c.	DB ₅	30	DB ₄
V_{P}	31	V_{P}	0V	31	V _S *
ον	32	0 V	DB ₇	32	DB ₆

^{*} $V_S = 24 \ V$: points A (Fig. 5) **not** bridged; $V_S = 5 \ V$: points A to be bridged with a jumper.

BIDIRECTIONAL SERIAL INTERFACE

The RS20 is for remote control of input and output modules of a PC20-system (passive slave). Furthermore it allows two PC20-systems to be connected to each other in a master/slave configuration, for data exchange between the systems (active slave); see Fig. 1.

Both master and slave station must have an RS20 module and they must be connected to each other via a coaxial cable or a shielded twisted pair of wires.

The RS20 performs three modes of operation, which are selected by the levels on inputs BMS and CMS, as shown in Table INPUTS, paragraph ELECTRICAL DATA.

Mode A (master mode): when used in the master PC20-system for communication with one slave station.

Mode B (active slave mode): when used in the slave PC20-system with a central processor.

Mode C (passive slave mode): when used in the slave PC20-system, which includes only input and output modules, to transfer data without further processing.

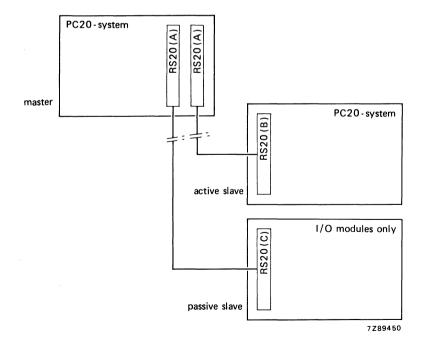


Fig. 1.

Master/slave communication takes place via the 256-bit RAM buffer memories of the RS20 modules. The data transfer rate is 256 bits in 0,75 ms. Within this time all control and data is transferred and checked.

Whether data are handled as inputs or outputs is established by the setting of the SCIO coding inputs. Error detection is accomplished by Cyclic Redundancy Checking. The ERROR output is set to 0 if an error has been detected on received data at either or both ends of the external data line. This output is also set to 0 during the first 120 ms after switching on the supply voltage, and after 60 ms if no communication has taken place. During this period continuous testing takes place to restore communication. If the ERROR output is set to 0, the LED at the front of the module is lit.

After data exchange between the PC20-systems, the $\overline{\text{READY}}$ output is set to 0, and the RS20 is ready for internal data exchange between its buffer memory and the scratchpad memory of the PC20-system of which it forms part, or the connected input and output modules. This internal data exchange takes place during the I/O phase in which the RS20 is scanned. The sequence of the various data flows is shown in Fig. 2.

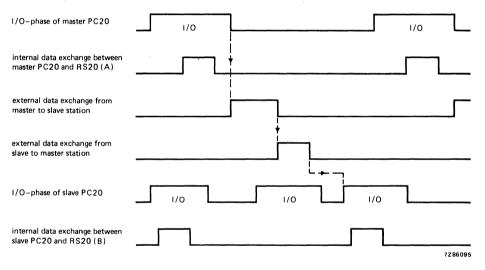


Fig. 2.

The RS20 is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

^{*} For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply voltage (d.c.)) tania	V_P	10 V :	± 10%	
Supply current	logic	lр	typ.	160	mA
Supply voltage (d.c.)	for input/output	v_S	24 V :	± 25%	
Supply current	circuitry	IS	typ.	5	mΑ
Output voltage between TR ₁	and TR3*	$V_{o(p-p)}$	min.	5,66	V
Input voltage between TR ₁ a	and TR ₃ *	$V_{i(p-p)}$	min.	4,24	٧
Input impedance between Ti	R ₁ and TR ₃ *	z _i	approx.	75	Ω
Data transfer rate				400	kbaud

Connection between master and slave station

For distances up to 250 m a shielded twisted pair of wires, max. loop resistance 50Ω , with polythene insulation can be used (Fig. 4). For larger distances a coaxial cable has to be used (Fig. 3), e.g. COAX-12** for max. 750 m, or BAMB00-SIX** for max. 2000 m.

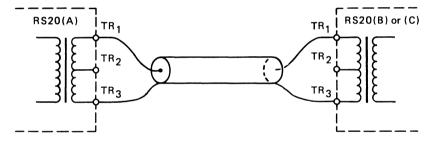


Fig. 3 Connection of bidirectional busses via a coaxial cable.

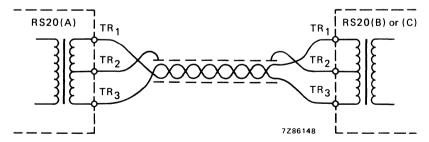


Fig. 4 Connection of bidirectional busses, via a shielded twisted pair of wires.

- * Bidirectional busses for the external data line.
- ** Trade name of NKF (Nederlandse Kabel Fabrieken).

Input and output data

All inputs and outputs meet the standard LOCMOS specifications, unless otherwise specified.

	C	terminatio	ons (Fig. 7)			
	function	connector 1	connector 2			
BI-DIRECT	BI-DIRECTIONAL DATA BUSSES					
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₈ ADD ₉ ADD ₁₀	Address bits. Inputs in A and B modes, outputs in C mode.	c11 a11 c12 a12 c13 a13 c14 a14 c15 a15				
APF	Handshake signal, indicates that addresses are correct. Input in A and B modes, output in C mode.	a26				
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data exchange between RS20 and PC20 system.	c21 a21 c22 a22				
PHC ₀ PHC ₁	Phase control. Inputs in A and B modes, outputs in C mode.	c23 a23				
SBI	Store command; Stores data in buffer memory during I/O cycle. Input in A and B modes, output in C mode.	c26				
TR ₁ TR ₂ TR ₃	Transmit/receive terminals for connection of external data line (TR ₂ common); via transformer coupled to the inner circuitry of the RS20, (Figs 3 and 4).		c26 c28 c30			

		terminat	ions (Fig. 7)
	function	connector 1	connector 2
INPUTS			
BMS CMS	Mode select inputs. Mode A: BMS and CMS are LOW. Mode B: BMS is HIGH, CMS is LOW. Mode C: BMS is HIGH or LOW, CMS is HIGH.	c1 c2	
MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	c6 c7 c8 c9	
SCIO ₀ SCIO ₁ SCIO ₂ SCIO ₃	Input/output separation coding inputs. Numbers smaller than code are outputs (seen from PC20 master system); other numbers are inputs.	c17 c18 c19 c20	
START	Enables external data exchange. Input is isolated from the internal circuitry with photo-isolator (Fig. 5), to be connected to an OM20 output. LOW input level: 0 to 7 V; HIGH input level: 18 to 30 V.		c20

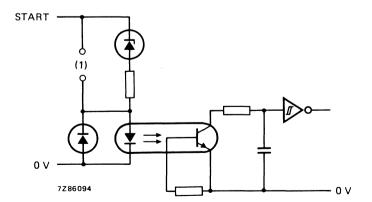


Fig. 5 Circuit diagram of START input.

(1) For 5 V-level operation a resistor of 360 Ω \pm 5%, style CR25, has to be connected.

		terminations (Fig. 7)		
	function	connector 1	connector 2	
OUTPUTS				
DEF	Signal to central processor, indicating that data from central processor has been stored.	a25		
DER *	Detected error output, indicating an error has been detected on data received from the other RS20 module.		c14	
ERROR *	Error output, indicating data exchange along the external data line did not happen errorless or did not happen at all		c16	
PRF	Preparation of RS20 finished (open collector output)	a24		
READY *	Output, indicating RS20 has finished external data exchange.		a20	
R/W	Read-write level PC20-system. Only active during I/O-phase.	c24		
TER*	Transmitted error output, indicating the RS-20 at the other side of the external data line has detected an error on the received data.		c12	

^{*} Open-collector output; isolated from the internal circuitry with photo-isolator (Fig. 6). To be connected to IM20 inputs.

Maximum sink current: 25 mA; maximum collector voltage in off-position: 30 V.

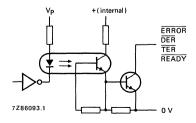


Fig. 6 Circuit diagram of ERROR, DER, TER and READY outputs.

MECHANICAL DATA Outlines

Dimensions in mm

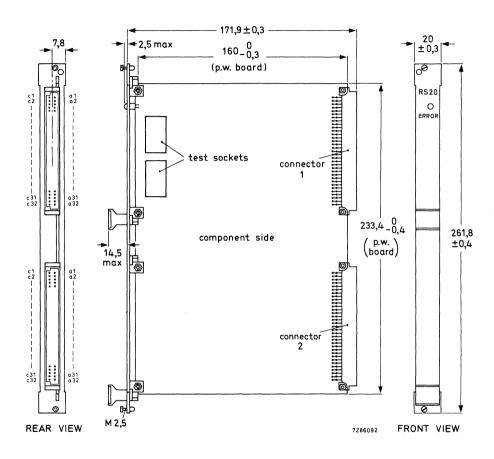


Fig. 7.

Mass approx. 270 g

Terminal location

connector 1

connector 2

row c		row a	row c		row a
BMS	1	HIGH level	n.c.	1	n.c.
CMS	2	HIGH level	n.c.	2	n.c.
n.c.	3	n.c.	n.c.	3	n.c.
n.c.	4	n.c.	n.c.	4	n.c.
n.c.	5	n.c.	n.c.	5	n.c.
MID ₆	6	HIGH level	n.c.	6	n.c.
MID ₇	7	HIGH level	n.c.	7	n.c.
MID ₈	8	HIGH level	n.c.	8	n.c.
MID ₉	9	HIGH level	n.c.	9	n.c.
MID ₁₀	10	HIGH level	n.c.	10	n.c.
ADD_0	11	ADD ₁	n.c.	11	n.c.
ADD ₂	12	ADD3	TER	12	n.c.
ADD ₄	13	ADD ₅	n.c.	13	n.c.
ADD ₆	14	ADD ₇	DER	14	n.c.
ADD8	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	n.c.	ERROR	16	n.c.
SCIO ₀	17	HIGH level	n.c.	17	n.c.
SCIO ₁	18	HIGH level	n.c.	18	n.c.
SCIO2	19	HIGH level	n.c.	19	n.c.
SCIO3	20	HIGH level	START	20	READY
DIO ₀	21	DIO ₁	n.c.	21	n.c.
DIO ₂	22	DIO3	n.c.	22	n.c.
PHC_0^-	23	PHC ₁	n.c.	23	n.c.
R/W	24	PRF	0 V	24	n.c.
0 V*	25	DEF	n.c.	25	n.c.
SBI	26	APF	TR ₁	26	n.c.
n.c.	27	n.c.	n.c.	27	n.c.
n.c.	28	n.c.	TR ₂	28	n.c.
n.c.	29	n.c.	0 V	29	Vs
n.c.	30	n.c.	TR ₃	30	n.c.
V_{p}	31	V_p	0 V	31	Vs
0 V	32	ον	0 V	32	n.c.

n.c. = not connected

^{*} No supply line; is used as return line for control signals.

BIDIRECTIONAL SERIAL INTERFACE

The VI20 bidirectional serial interface is used in PC20 systems to communicate with TTYs, VDUs, minicomputers and other equipment handling serial data. It has V24/RS232C/RS423 and current-loop inputs and outputs for this purpose. Furthermore, the VI20 can be used to advantage as a satellite processor for handling complex and time-consuming operations thus maintaining rapidity of system response. Its address and data processors are identical to those used in the PC20 central processor modules. Having a 2k16 EPROM program memory* and a ¼k4 data memory it resembles most the CP20 central processor; see Fig. 1. Figure 8 shows the location of the two type 2716 EPROMs (sockets A and B). As with all other I/O modules the VI20 uses photo-isolators between its logic circuitry and the outside world.

For communication with the PC20, the VI20 has a 16-bit (4 x 4 bits) control register to exchange control data, and a 128-bit (32 x 4 bits) buffer register (part of data memory) to transfer process data. The control register is identified in the PC20 scratchpad memory using the MID_{2-9} code on the back panel: hardware addressing. The buffer register is identified by six bits, A_{5-10} , generated in the PC20 program and accumulated in the control register: software addressing. Utmost flexibility is achieved through free selection of the software addressing code allowing the entire area of a 2k4 scratchpad memory to be covered for storing and retrieving the process data.

In contrast to the PC20 system, the VI20 is intermittent in operation. When started by the PC20 it completes one data processing phase (active state) then stops and waits until the next start signal (idle state). During the processing phase the VI20 inputs and outputs are directly accessible.

Basically, there are three PC20 I/O operations (Fig. 2):

- for communication between the PC20 and its process (marked '1' in Fig. 2);
- for communication between the PC20 and the VI20 via the control register (marked '2');
- for transfer of process data between PC20 scratchpad memory and buffer register (hatched). Transfer of process data occurs upon request; the VI20 must be in the idle state to allow this.

The VI20 instruction set is identical to that of the PC20 system. Intermittent operation of the VI20 is clear from the flow chart, Fig. 3. Upon switch-on or reset the CONDITION is set to '1' level. Also, in the first cycle after switch-on or reset, all 4-bit data memory locations are set to 1001.

The VI20 has been built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts). The corresponding rack part of connector 1 (Fig. 8) is available on the back panel. That of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags). **

- Standard programs are available, see paragraph "Software modules".
- ** For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-inch racks and IEC 130-14 or DIN 41612 for connectors.

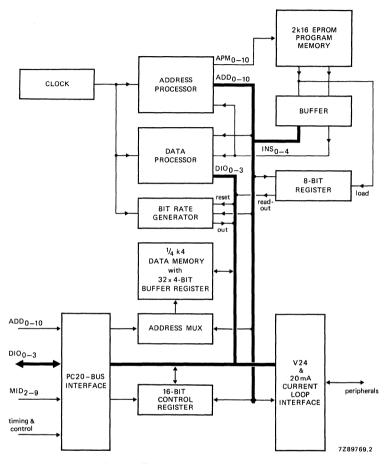


Fig. 1 Block diagram.

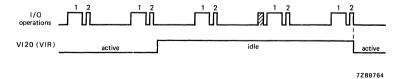


Fig. 2 Basic PC20 I/O operations and VI20 states.

Bidirectional serial interface VI20

The 4 x 4-bit *control register*, Fig. 4, contains four outputs (one-bit places) to and ten inputs (one-bit places) from the PC20 scratchpad memory. Addressing of the control register can only occur on pages 0 and 1 of the CP22 scratchpad (MID $_{10}$ internally connected to 0 V).

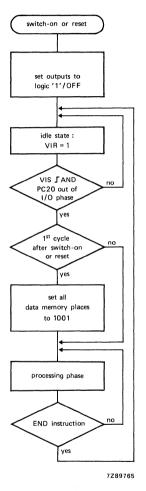


Fig. 3 Flow chart.

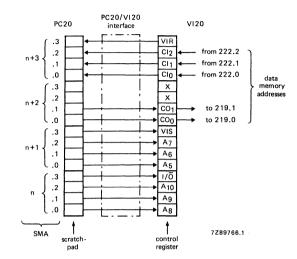


Fig. 4 Control Register.

The control register bit functions are:

VIR VIR = 1: VI20 in idle state;

VIR = 0: VI20 in active state.

Cl_{0, 1, 2} General-purpose control bits originating in

VI20 program.

XX No assignment.

 $CO_{0.1}$ General-purpose control bits originating in

PC20 program.

VIS Provided VIR = 1 (VI20 idle) a positive change of this bit will cause the VI20 to become active

and start with line 0000 of its program; V120 will not become active before the end of the PC20 I/O phase in which the positive transition

of VIS has been detected.

I/O

I/O = 0: data transfer from scratchpad memory to buffer register;

I/O = 1: data transfer from buffer register to scratchpad memory.

A₅₋₁₀ Software addressing bits originating in the PC20 program (A_5 = least significant bit; A_{10} = most significant bit).

In the table below the occupation of the *data memory* is specified. Locations 0 to 215 are free for storing data generated in the VI20 program. Locations 216 and 217 form the eight-bit register that can be loaded by the LSTI0 instruction only. The highest locations, 224 to 255, form the *buffer register*.

The bit-rate generator is used in asynchronous data transmission. It can be adjusted to a variety of bit rates by means of jumpers (S, Fig. 5) on the printed-wiring board; see table below.

Mark/space ratio is 1 : 1 (50% duty factor). Reset to start of LOW phase is done using the 'STRD 221' execute instruction.

Bit-rate selection. Upper jumper position = 1, lower jumper position = 0. Jumper positioning shown in Fig. 5 for 300 bits/s.

Assignment of data memory addresses.

address	function	bits/s	jumper positions
0 to 215	no assignment		S ₃ S ₂ S ₁ S ₀
216, 217	read-only eight-bit register	50	
218.0/.1/.2/.3	V24 inputs	75	
219.0/.1	CO _{0. 1} control bits	110	
219.2	arithmetic overflow	150	
219.3	bit-rate generator output	300	ōō□ō
220 . 0/ . 1/ . 2/ . 3	V24 outputs	600	
221	reset bit-rate generator	1200	
222.0/.1/.2	Cl _{0. 1. 2} control bits	2400	
223	no assignment	4800	_□□0 <u>0</u>
224 to 255	buffer register	9600	<u>0</u>
ELECTRICAL DATA			
Supply			
Supply voltage (d.c.)	logic	V _P	10 V ± 10%

Supply voltage (d.c.) Supply current	logic	V _P	10 V ± 10% typ, 160 mA
			max. 170 mA
Supply voltage (d.c.)	d.cd.c.	v_S	24 V ± 25%
Supply current	converter*	ls	max. 110 mA

Inputs

Data inputs. The data inputs I_0 (218.0), I_1 (218.1), I_2 (218.2) and I_3 (218.3) are zener-diode protected and meet V24 standards. The bit level is '1' when input voltage $V_i \leqslant -1$ V and '0' when $V_i \geqslant +1$ V. They are accessible via connector 2; see 'Terminal location'. The inputs are commoned through V_c .

Input resistance R_i see Fig. 6 Max. permissible input voltage (positive or negative) $V_{i \, max}$ 30 V

The first input (corresponding to address 218.0) can be made to act as a 20 mA current loop by changing the position of two jumpers (A, Fig. 5) on the printed-wiring board. Current flow is from CLI₀ to CLI₁, see Fig. 6. The bit level is '1' when input current $I_i \le 0.1$ mA and '0' when $I_i \ge 10$ mA.

Max. permissible input current I_{i max} 20 mA

^{*} Used to supply V24 interface circuitry.

Individual reset. The VI20 can either be reset via \overline{RCO} together with the PC20 system using the \overline{RCP} input to the central processor or it can be individually reset using input \overline{RVI} (table below). Individual reset.

RVI	voltage	typ current
active	0 V to + 1 V	0,5 mA
not active	+ 10 V or floating	-

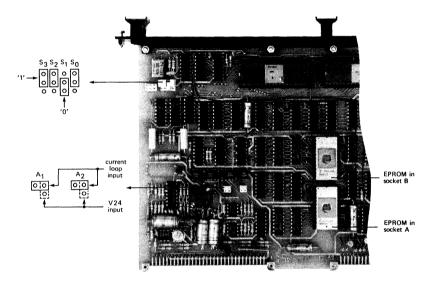


Fig. 5 VÎ20 adjustments.

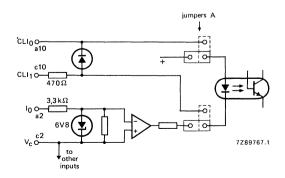


Fig. 6 Circuit diagram for input 218.0; for jumpers A see Fig. 5.

input	function	termination of connector 1 (Fig. 8)	
ADD0 ADD1 ADD2 ADD3 ADD4 ADD5 ADD6 ADD7 ADD8 ADD9 ADD10	Address bits from central processor. Control register ADD _{0.1} select a group of four bits in the control register. ADD _{2.9} select the control register. Buffer register ADD _{0.4} address both the buffer register and its address field in the scratchpad memory. ADD _{5.10} select the buffer register.	a11 a12 a13 a14 a15	c11 c12 c13 c14 c15
APF	Handshake signal indicating that address for VI20 is stable.	a26	
DIO ₀ * DIO ₁ * DIO ₂ * DIO ₃ *	Data bits from and to central processor.	a21	c21
MID ₂ MID ₃ MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉	Control register identification inputs; provide control register with individual identity.		c2 c3 c4 c5 c6 c7 c8 c9
PHC ₀ PHC ₁	Phase control signals from central processor.	a23	c23
RCO	Reset from central processor during switch-on (active LOW)		c27
RVI	Individual VI20 reset (active LOW)	a27	
SBI	Store command to store data from central processor in control register or buffer register.		c26

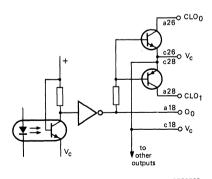


Fig. 7 Circuit diagram for output 220.0.

^{*} Either input or output.

Outputs

Data outputs. The data outputs O_0 (220.0), O_1 (220.1), O_2 (220.2) and O_3 (220.3) conform to V24 standards. The bit level is '1' when output voltage V_0 is -4 to -6 V and '0' when V_0 is + 4 to + 6 V. Access is via connector 2; see 'Terminal location'. All outputs are commoned through V_0 .

Min. permissible load resistance

 $R_{1 min}$ 450 Ω

Output O_0 (address 220.0) drives 20 mA current-loop outputs CLO_0 and CLO_1 for two-line and four-line transmission (open collector outputs): see Fig. 7. Current flow is from CLO_0 to V_c (NPN transistor) and from V_c to CLO_1 (PNP transistor) respectively.

Specifications of current-loop outputs CLO₀ and CLO₁.

bit level in data	NPN transistor	PNP transistor
memory address	between	between
220.0	CLO ₀ and V _C	V _C and CLO ₁
'1' '0'	not conducting conducting	conducting not conducting

Collector-emitter leakage current VCEmax VCE

Reference outputs. Reference outputs V_+ and V_- are available (+ 12 V and -12 V) to bias any one of the inputs. These outputs are commoned via V_c .

Minimum permissible load resistance is 1 k Ω for each output.

output	function	termination of connector 1 (Fig. 8)
DEF	Data exchange — scratchpad memory to buffer register — finished (open collector output).	a25
PRF	Preparation of VI20-addressing finished (open collector output).	a24
R/W	Signal to central processor (active LOW); prepares central processor for data on DIO ₀₋₃ to be written in scratchpad memory (open collector output).	c24

Note: All V24 inputs and outputs as well as V_+ and V_- are commoned to V_c and floating with respect to V_P and V_S .

Software modules

Standard programs are available, which come as software modules, each consisting of two pre-programmed type 2716 EPROMs. These modules have to be ordered separately. The following software modules are available:

- PVII message program: provides a framework to assemble messages of any nature; catalogue number 4322 027 99011.
- PVI2 data terminal program: a TTY or VDU with keyboard is used to write data in or read data from the central processor scratchpad memory; catalogue number 4322 027 99021.
- PVI4 communication program A: for communication between a master station and slave stations (VI20 modules); the four-bit data are embedded in seven-bit ASCII characters; catalogue number 4322 027 99041.
- PVI5 communication program B: for communication between a master station and a PC20 system via a VI20 module (slave); eight bits of data are transferred as asynchronous eight-bit characters; catalogue number 4322 027 99051.
- PVI7 communication program C: for communication between a master station and slave stations (VI20 modules); the slave stations can take initiative for communication. The four-bit data are embedded in seven-bit ASCII characters; catalogue number 4322 027 99071.
- PVI8 twelve channel PID controller, to be used in conjunction with analogue input and output modules AD20 and DA20; catalogue number 4322 027 99081.

MECHANICAL DATA

Outlines

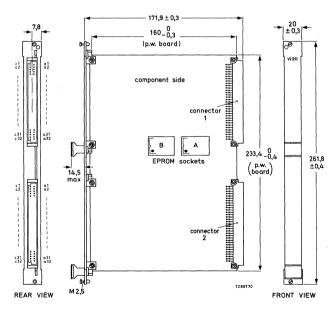


Fig. 8.

Mass

approx, 300 g

Terminal location

	connector 1			connector 2	
row c		row a	row c		row a
n.c.	1	n.c.	n.c.	1	n.c.
MID_2	2	HIGH level	$V_{\mathbf{c}}$	2	10
MID_3	3	HIGH level	n.c.	3	n.c.
MID_4	4	HIGH level	V_c	4	11
MID ₅	5	HIGH level *	n.c.	5	n.c.
MID ₆	6	HIGH level	$V_{\mathbf{c}}$	6	12
MID_7	7	HIGH level	n.c.	7	n.c.
MID ₈	8	HIGH level	V_c	8	l ₃
MID ₉	9	HIGH level	n.c.	9	n.c.
n.c.	10	n.c.	CLI ₁	10	CLI ₀
ADD_0	11	ADD ₁	n.c.	11	n.c.
ADD_2	12	ADD3	n.c.	12	n.c.
ADD_4	13	ADD ₅	n.c.	13	n.c.
ADD_6	14	ADD ₇	٧+	14	n.c.
ADD8	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	n.c.	V_	16	n.c.
n.c.	17	n.c.	n.c.	17	n.c.
n.c.	18	n.c.	V_c	18	o_0
n.c.	19	n.c.	n.c.	19	n.c.
n.c.	20	n.c.	V_c	20	O_1
DIO_0	21	DIO ₁	n.c.	21	n.c.
DIO_2	22	DIO3	V_c	22	0_2
PHC_0	23	PHC ₁	n.c.	23	n.c.
R/W¯	24	PRF	V_c	24	03
0 V**	25	DEF	0 V	25	٧S
SBI	26	APF	V_c	26	CLO ₀
RCO	27	RVI	0 V	27	V_S
n.c.	28	n.c.	V_c	28	CLO ₁
n.c.	29	n.c.	0 V	29	٧ _S ·
n.c.	30	n.c.	n.c.	30	n.c.
V_P	31	V_{P}	0 V	31	V_S
ο̈ν	32	0 V	n.c.	32	n.c.

n.c. = not connected.

^{*} For coding MID lines only.

^{**} No supply line; is used as return line for control signals.



MICROCONTROLLER

The MC20 is a programmable controller for small systems. It uses the same address and data processors as the PC20 system.

The controller is on one printed-wiring board, and contains the following functions:

- 32 inputs:
- 20 outputs;
- 2k16 EPROM program memory;
- ½k4 scratchpad memory:
- 8 adjustments for software timers/counters:
- 5 internal clock references;
- 24 V/5 V d.c.-d.c. converter;
 automatic reset when power switched-on.

The microcontroller is protected by a plastic cover. External connections are made via screw terminals.

The controller can be mounted to a panel by means of screws, or to Euro-rails (DIN 46277, Blatt 3) by means of mounting clips (see "Accessories").

Inputs

The 32 inputs are arranged in 8 groups of 4, each input being galvanically isolated by photo-isolators (Fig. 1). A delay circuit (delay time typ. 1 ms) is incorporated in each input to increase noise immunity.

Active voltage ('1' level) 16 to 30 V Non-active voltage ('0' level) 0 to 7 V Input current, active at 24 V typ. 10 mA

The input terminals are marked 8.0 to 15.3, in accordance with their fixed addresses in the scratchpad memory.

Outputs

The 20 outputs are arranged according to Fig. 2.

Supply voltage, V $_{\rm S2}$ \$18 to 30 V Minimum load resistance, R $_{\rm L}$ $$120~\Omega$ Maximum output current at 24 V \$200 mA

The output terminals are marked 3.0 to 7.3, in accordance with their fixed addresses in the scratchpad memory.

NOTE

Since the inputs and outputs have fixed addresses 3 to 15 in the scratchpad memory, the relevant I/O-phase should only be specified within this field (to be programmed as LSTI015, END3).

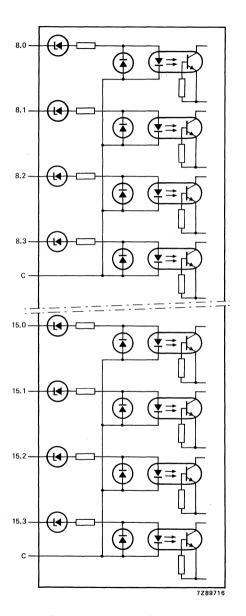


Fig. 1 Configuration of input stages.

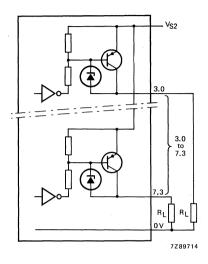


Fig. 2 Configuration of output stages.

Program memory

Two empty EPROMs (2716) are supplied with the MC20 (inside the cover) having a capacity of 2048 instructions. For programming instructions, see "Programming and monitoring".

The programmed EPROMs (A and B) should be inserted into the sockets as shown in Fig. 3.

Scratchpad memory

The scratchpad memory has a capacity of 1/2k4 (512 words of 4 bits).

Fixed scratchpad memory addresses are:

- 0.0 overflow bit
- 0.1 constant '1' level
- 0.2 alarm supply voltage (V_{S1} < 18 V)
- 0.3 timer clock 10 ms
- 1.0 timer clock 100 ms
- 1.1 timer clock 1 s
- 1.2 timer clock 10 s
- 1.3 timer clock 1 ms
- 3.0 to 7.3 outputs
- 8.0 to 15.3 inputs
- 240 to 255 potentiometer settings

No battery back-up is provided for the scratchpad memory.

Adjustments of software timers

Eight potentiometers (P, Fig. 3) provide adjustment of software timers. The potentiometer setting is converted into a two-decade BCD-value (0 to 99), and stored in the scratchpad memory at two consecutive addresses when the system is in the UDC-phase. The potentiometer settings are scanned sequentially and each time a conversion is completed and the system is in the UDC-phase the scratchpad memory is updated. The conversion of one potentiometer setting takes a maximum of 0,5 ms.

The results of the conversions are stored at the scratchpad memory addresses 240 to 255; the setting of potentiometer 1 being stored at the two lowest number addresses 240 and 241 (LSD).

Internal clock periods

The MC20 has 5 crystal-controlled timer clocks, which are accessible at fixed scratchpad memory addresses 0.3 to 1.3.

24 V/5 V d.c.-d.c. converter

The logic part of the controller has a supply voltage of 5 V. To allow the controller to be directly operated in a machine control system with a supply of 24 V, the MC20 has a 24 V/5 V d.c.-d.c. converter. If the supply voltage to the converter, V_{S1} (24 V), falls below 18 V the alarm input (scratchpad memory address 0.2) becomes '1'.

Automatic reset

When the supply voltage is switched on, the control system generates an automatic reset. This resets the whole system, including setting all locations in the scratchpad memory to '0'. A system reset also occurs if the supply voltage (V_{S1}) falls below 16 V.

The system has a pushbutton (R, Fig. 3) for manual reset (cover to be removed).

System speed

The system execute time depends on the types of instructions used. The execute time of read instructions and all conditional instructions of which the condition is false is 2,5 μ s/instruction. For an average program of 1k instructions the cycle time is typically 3 ms.

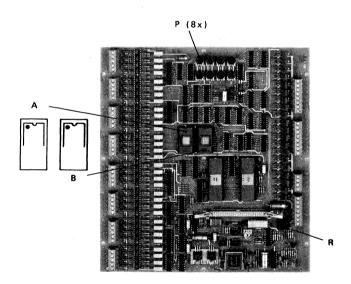


Fig. 3 Microcontroller; cover removed.

Supply			
Supply voltage	for 24 V/5 V d.cd.c. converter	v_{S1}	24 V ± 25%
Supply current	for 24 V/5 V a.ca.c. converter	I _{S1}	typ. 100 mA max. 130 mA
Supply voltage Supply current	for output circuitry, exclusive load current	V_{S2}	24 V ± 25%
Supply current	for output circuitry, exclusive load current	I _{S2}	max. 250 mA

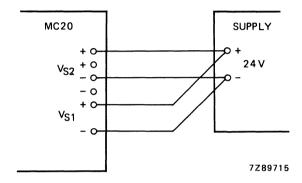


Fig. 4 Connection of supply voltages.

Programming and monitoring

Programming unit PU20, in conjunction with microcontroller interface MI20, can be used to program and monitor the MC20. The MI20 contains an RI20 module (2k16 CMOS RAM + interface) and a PU23* module. The MC20 can be connected to the RI20 with a 50-core flat cable.

The program can also be developed with a PC20-system.

Note that an MC20-program in the EPROMs cannot be monitored when the PU20 is in the EDIT-mode, or in the MONITOR CONT-mode when the UDC-key is operated.

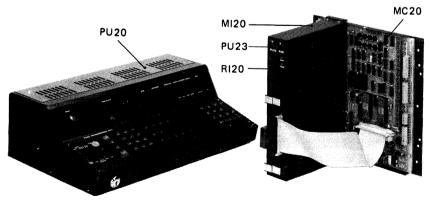


Fig. 5 Programming/monitoring MC20.

^{*} To be ordered separately.

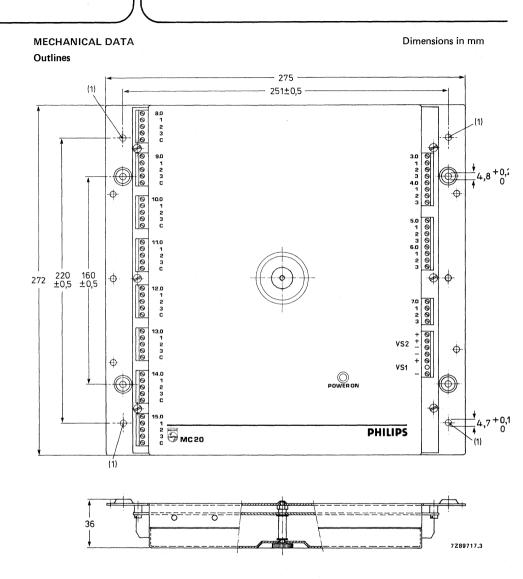


Fig. 6 The holes marked⁽¹⁾ are for mounting clips MB20, see 'Accessories'.

ACCESSORIES

For mounting the microcontroller to Euro-rails, snap-on mounting clips MB20 can be supplied; catalogue number of set of 4 clips: 4322 027 23080.

ENVIRONMENTAL DATA

Operating temperature range Storage temperature range

0 to + 60 °C -40 to + 70 °C

TESTS AND REQUIREMENTS

The MC20 is designed to meet the tests below.

Vibration test

IEC 68-2-6, test method Fc: 10 to 55 Hz, amplitude 0,75 mm or 5g (whichever is less).

Shock test

IEC 68-2-27, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50g.

Rapid change of temperature test

IEC 68-2-14, test method Na: 5 cycles of 2 h at -40 °C and 2 h at +85 °C.

Damp heat test

IEC 68-2-3, test method Ca: 21 days at 40 °C, R.H. 90 to 95%.



MICROCONTROLLER INTERFACE

This microcontroller interface is used between an MC20 system and the programming unit PU20. Via this interface the PU20 obtains access to the system for programming and monitoring.

The MI20 is a metal housing, containing a RAM/interface unit RI20 and a programming unit interface PU23; the PU23 has to be ordered separately under catalogue number 4322 027 94180. The RI20 forms an interface between the PU23 and the MC20; it has a 2k16 C-MOS RAM program memory for programming the MC20 system.

The metal housing MI20 can be fitted to the MC20 by means of a quick-coupling system. A 50-pole male header F303 at the front of the RI20 provides electrical connection to the MC20 via a 50-core flat cable, which is supplied with the MI20.

The MI20 performs two modes of operation for programming and monitoring the MC20 system, which are indicated by LEDs at the front panel of the RI20.

PROM mode (PROM LED is on): for the MC20 system, operating on a program that is stored in its EPROM memory. The MI20 is automatically set to this mode when the system is switched on.

RAM mode (RAM LED in on): for the MC20 system, operating on a program that is stored in the program memory of the RI20. The MI20 is set to this mode by pushing the button at the front of the RI20; the actual setting takes place when the MC20 comes in the UDC phase.

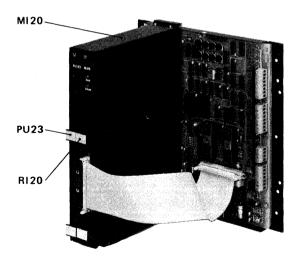


Fig. 1.

In the PROM mode an MC20 program cannot be monitored when the PU20 is in the EDIT mode, or in the MONITOR CONT n • de when the UDC key is operated. In the latter case the END instruction also cannot be monitored.

When the EPROM sockets on the MC20 are empty and a program has to be written into the RAMs of the MI20 the following procedure has to be followed.

- Switch on the PU20, select EDIT mode and line number 0, and push ENTER key.
- Switch on the MC20/MI20 system; the PROM LED on the front plate of the RI20 lights and the PU20 displays 27 0000.
- Push the button on the front plate of the RI20; the RAM LED lights and the system is ready for RAM programming.

ELECTRICAL DATA

Supply voltage Supply current from MC20 via flat cable	V _P I _P	5 V + 5% typ. 80 mA
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Data retention with on-board battery min. 7 days, provided the module is in operation for at least 10 h.

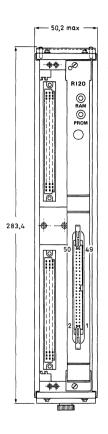
Input and output data

	function	terminations of male header at the front of RI20
BI-DIRECTIONA	L BUSSES	
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉	Scratchpad memory address bus.	21 22 29 30 31 32 33 20 19
ADD ₁₀ APM ₀ APM ₁ APM ₂ APM ₃ APM ₄ APM ₅ APM ₆ APM ₇ APM ₈ APM ₉ APM ₉	Program memory address bus.	34 36 37 38 39 40 41 42 43 44 45 46

	function	terminations of male header at the front of RI20
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Scratchpad memory data bus.	9 8 10 11
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus	14 13 12 16 17
INPUTS		
APF	Timing signal from MC20 to PU23	1
CLOCK	Clock signal to PU23	48
CPSI	Signal from PU23 to stop MC20 in UDC phase	4
PHC ₀ PHC ₁	Phase control outputs from MC20	7 6
RESET	Reset output from MC20 (active low).	23
RR	Output Result Register from MC20.	35
SBI	Clock signal from MC20 to RI20 and PU23.	15
OUTPUTS		
CPDC	Timing pulse to clock data in program memory data latch on MC20 during UDC phase.	2
CPSC	Signal from MC20 to PU23 indicating that MC20 has been stopped.	50
HOLD	Signal from PU23 to hold MC20.	5
PDLE	Program memory data latch enable.	49
WDSM	Signal from PU23 to write data on DIO bus into scratchpad memory.	47

MECHANICAL DATA





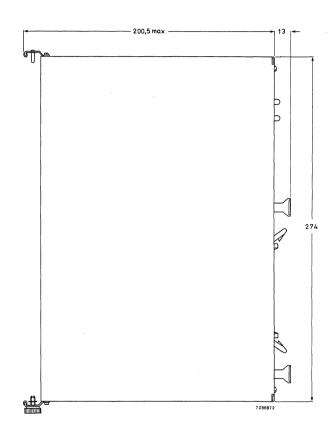


Fig. 2.

Mass: 1,5 kg

MI20

TERMINAL LOCATION

Termina	Terminations of male header at the front of R120				
APF	1	2	CPDC		
n.c.	3	4	CPSI		
HOLD	5	6	PHC ₁		
PHC_0	7	8	DIO ₁		
D10 ₀	9	10	DIO_2		
DIO_3	11	12	INS ₂		
INS ₁	13	14	INS ₀		
SBI	15	16	INS ₃		
INS ₄	17	18	ADD ₉		
ADD ₈	19	20	ADD ₇		
ADD_0	21	22	ADD ₁		
RESET	23	24	n.c.		
0V	25	26	0V		
V_P	27	28	V_{P}		
ADD ₂	29	30	ADD_3		
ADD ₄	31	32	ADD ₅		
ADD_6	33	34	ADD ₁₀		
RR	35	36	APM_0		
APM ₁	37	38	APM ₂		
APM_3	39	40	APM ₄		
APM ₅	41	42	APM ₆		
APM ₇	43	44	APM ₈		

APM₁₀

CLOCK

CPSC

46

48

50

n.c. = not connected.

APM₉

WDSM

PDLE

45

47

49



PROGRAMMING UNIT

DESCRIPTION

This mains-powered programming unit is for loading, checking, dumping and monitoring the control program of the PC20-system. It provides access to the program memory and the scratchpad memory. The programming unit is a desk-top apparatus. The program is written into the program memory via the keyboard (Fig. 1) or other sources e.g. tape readers, cassette recorders, program developing systems. The program is monitored by the display or, for example, by an external VDU.

The programming unit must be used in conjunction with the programming unit interface PU21/PU23 (placed in the PC rack), to which it is connected via an 8-core cable. The circuits of the PU20/2 and the PU21/PU23 are galvanically isolated from each other by means of photo-isolators. The data transport via the data-in and data-out lines is serial.

After loading the program into the program memory, the programming unit can be removed to be used in another PC-system. If necessary, for monitoring purposes for example, it is very easy to connect the PU20/2 to the system again.

The programming unit is provided with two sockets for EPROMs, type 2716 (2k bytes). Programming of the EPROMs is done in such a way that each program word is distributed over two EPROMs, A and B (Fig. 1). EPROM A contains the instruction and the most significant digit of the address and EPROM B contains the remaining digits. The programmed EPROMs can be used in central processor CP20, program memory module MM20 and microcontroller MC20.

The programming unit has the following 10 modes of operation.

- 1. EDIT: creating a new program or changing an existing program.
- 2. MONITOR CONT: continuous monitoring the PC20-system in operation; on-line change facilities.
- 3. MONITOR CYCLE: monitoring the PC20-system, which operates on command for one cycle.
- 4. MONITOR STEP: monitoring the PC20-system, which executes on command one program line.
- 5. PROM PROG: dumping the program from the PC20-system into the EPROMs in the sockets of the programming unit.
- 6. DUMP CASS: dumping the program from the PC20-system onto cassette tape.
- 7. DUMP RS449/423: dumping the program from the PC20-system into peripheral equipment with EIA-standard specification RS449/423.
- 8. LOAD PROM SOCK: loading the program from the EPROMs in the sockets of the programming unit into the PC20-system.
- 9. LOAD CASS: loading the program from cassette tape into the PC20-system.
- LOAD RS449/423: loading the program from peripheral equipment with EIA-standard specification RS449/423 into the PC20-system.

A keyswitch is provided. Without the key a user can only monitor system operation and check the states of scratchpad memory locations; a user with a key has full command over all functions.

PU20/2

MECHANICAL DATA

Dimensions

see Fig. 2

Mass

approx. 6,3 kg

ENVIRONMENTAL DATA

Operating temperature range Storage temperature range 0 to 45 °C

 $-40 \text{ to} + 70 ^{\circ}\text{C}$

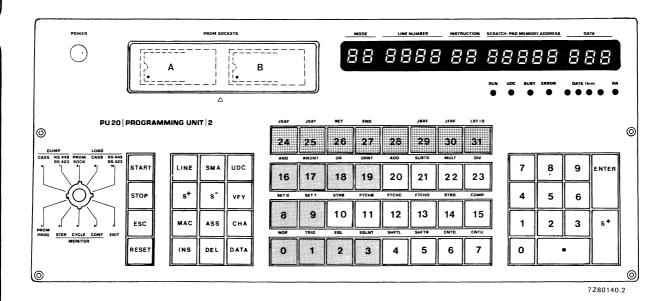
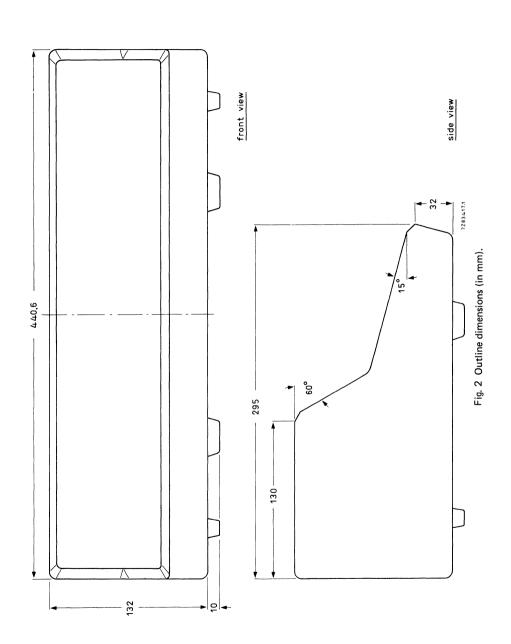


Fig. 1 Keyboard and display lay-out.



FLECTRICAL DATA

Mains voltage

110, 127, 220 or 240 V; tolerance + 10%, -15%

Mains frequency 46 to 65 Hz

Fusing

for 110 or 127 V mains 200 mA (delayed action fuse) for 220 or 240 V mains 100 mA (delayed action fuse)

20 VA Power consumption

On delivery the programming unit is adjusted to 220 V mains voltage. If the local voltage is different, the switch at the rear must be set to the required position and the fuse must be replaced.

CONNECTING FACILITIES (see Fig. 4)

- Fixed mains cable (1) with plug with side earth-contact; length 2,4 m.
- Fixed 8-core cable (2) with 9-pole female plug F161, for connection to programming unit interface PU21/PU23: length 2.5 m. For terminal location see Table 1.
- EIA-standard interface connector plug (3), according to RS449/423, for connecting data terminal equipment (DTE), like CRT terminals, punchers, printers, readers. The pins 4, 6, 9, and 19 are operational. For detailed information Table 2 should be consulted.

Note: The programming unit is data communication equipment (DCE).

- DIN-socket (4) for connecting a normal audio cassette recorder (see also Fig. 3). To avoid drop-outs it is recommended that C60 Super Quality Ferrochromium cassette tape be used.
- Two sockets for EPROMs, type 2716 (2k bytes) or 2758 (1k bytes).

Note: At the rear of the programming unit provisions (5) are made for stowage of the mains cable and the 8-core cable during transport.

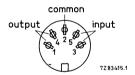


Fig. 3 DIN audio socket.

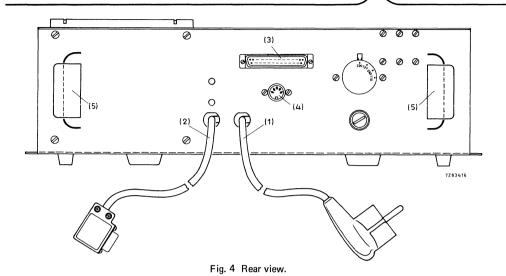


Table 1 Terminal location of connecting cable to PU21/PU23

terminal	function
1	connected to terminal 6
2. CLDT	clock signal for data transfer between PU20/2 and PU21/PU23
3. TRANSFER	data transfer required by PU20/2
4. SSE	system stop enable
5.	+ 5 V *
6.	connected to terminal 1
7. DPI	data from PU20/2 to PU21/PU23
8. DIP	data from PU21/PU23 to PU20/2
9. READY	ready signal to PU20/2, indicating that PU21/PU23 is available for data transfer

^{*} No supply line; is used as a common line for the control signals.

Table 2 Terminal location of RS449/423 plug

terminal	function	operational	dummy ON	dummy OFF	jumper 1	jumper 2
2	SI — signalling route indicator		х			
4	SD — send data	X				
6	RD - receive data	Х				
9	CS — clear to send	X*				X**
11	DM — data mode					Х
12	TR — terminal ready					Х
13	RR — receiver ready	-				Х
15	IC — incoming call			×		
18	TM — test mode			×		
19	SG — signal ground	Х			Х	
20	RC - receive common				×	
33	SQ — signal quality		Х			
36	SB — stand-by indicator			Х		
37	SC — send common				×	

^{*} Not applicable to the former type PU20.

The PU20/2 has an input (pin 9 of connector plug (3), Fig. 4) which enables interruption of the data transfer from the PU20/2 to peripheral equipment with RS449/423 or RS232 input specification. When this input goes to the 'OFF' condition (-5 V) the data transfer is stopped. When this input goes to the 'ON' condition (+5 V) or is left floating, the data transfer is started again.

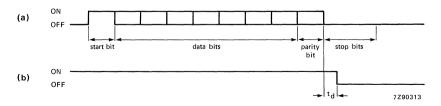


Fig. 5 Time relation between data stream (a) and stop signal (b); $t_d = min. 0$; max. $\frac{2}{bit rate}$ s.

^{**} Only applicable to the former type PU20.

PU23

PROGRAMMING UNIT INTERFACES

DESCRIPTION

The programming unit interface can be used between a PC20-system or MC20-system (in conjunction with microcontroller interface MI20) and the programming unit PU20/2 which obtains access to the system via this interface*. The programming unit interface does not form an essentail part of an operating system which can function normally without it.

Figure 1 is a block diagram of the programming unit interface which has direct access to the data, address and control lines of the PC20/MC20-system. Furthermore it is connected to the PU20/2 via an 8-core cable, which contains a data-in, transfer, clock, ready, system stop enable and a common line. These lines are galvanically isolated from the PU21/PU23 circuitry by photo-isolators. The data transport via the data-in and data-out lines is serial. All actions to be executed are commanded by the PU20/2 through a 4-bit function mode code. This code is transmitted, with the other data to the programming unit interface, in both normal and inverted form so that correct reception can be verified.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card**). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels. At the front of the unit a 9-pole male connector F161 allows connection of the cable from the programming unit.

The PU21 can only be used with a PC20-system.

For a general description of the Euro-card system see IEC 297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.

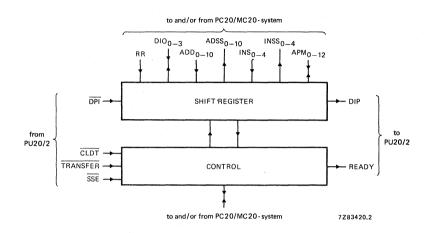


Fig. 1 Simplified block diagram.

ELECTRICAL DATA

Supply

Supply voltage (d.c.) current

	PU21	PU23
V_p	10 V ± 10%	5 or 10 V ± 10%
lp	max. 20 mA	max. 20 mA

Input and output data

All inputs and outputs meet the standard LOCMOS specifications.

	function	terminati	ons (Fig.	2)
	, and the same same same same same same same sam	connector 1	conn	ector 2
BI-DIRECT	TIONAL DATA BUSSES			
APM0 APM1 APM2 APM3 APM4 APM5 APM6 APM7 APM8 APM9 APM10 APM11 APM12	Program memory address bus; APM ₀₋₁₂ act as outputs when PABE is LOW (only during UDC-phase).		a16, a17, a18, a19, a20, a21, a22, a23, a24, a25, a26, a27, a28,	c16 c17 c18 c19 c20 c21 c22 c23 c24 c25 c26 c27
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data to or from scratchpad memory, controlled by WEPC.	a19, c19 a20, c20 a21, c21 a22, c22		
INPUTS				
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Program memory data bits from central processor (address bus).	a6 a7 a8 a9 a10 a11 a12 a13 a14 a15 a16		
CLOCK	Clock input from central processor for timing purposes.		а7,	с7
CPSC	Input that indicates that the central processor has been stopped (HIGH) in the UDC-phase.		a5,	с5
INS ₀ INS ₁ !NS ₂ INS ₃ INS ₄	Program memory data bits from central processor (instruction bus).	a1 a2 a3 a4 a5		

4322 027 92100 4322 027 94180

	function	ter	minatio	ns (Fig.	2)
	Taneton	connect	or 1	conn	ector :
PB ₀ PB ₁	Page bits.	a17,	c17		
PHC ₀ PHC ₁	Phase control from central processor.	a23,	c23		
RR	Result register.	a18,	c18		
SBI	Store command.		c26		
OUTPUTS					
ADDS ₀ ADDS ₁ ADDS ₂ ADDS ₃ ADDS ₄ ADDS ₅ ADDS ₆ ADDS ₇ ADDS ₈ ADDS ₉ ADDS ₁₀	Program memory data bits (address bus) to be stored in the program memory on CP21/CP24, MM21/MM22 or RI20*, or address bits for scratch-pad memory to read data from or to write data in the scratchpad memory. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).		c6 c7 c8 c9 c10 c11 c12 c13 c14 c15		
CPSD	Central processor slow down; command to central processor is only effective when the PU20/2 has been connected to the PU21/PU23.			аЗ,	сЗ
CPSI	Central processor stop initiate; command to central processor (active HIGH) to stop in UDC-phase.			a4,	c4
HOLD	Command to stop the central processor during the DP-phase (active LOW).			a6,	c6
INSS ₀ INSS ₁ INSS ₂ INSS ₃ INSS ₄	Program memory data bits (instruction bus) to be stored in the program memory of CP21/CP24, MM21/MM22 or RI20*. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).		c1 c2 c3 c4 c5		
PABE	Program memory address bus enable to central processor; APM ₀₋₁₂ terminals of PU21/PU23 act as outputs when PABE is LOW (only during UDC-phase).			a1,	c1
PDBE	Program memory data bus enable. INSS ₀₋₄ and ADDS ₀₋₁₀ act as outputs when PDBE is LOW (only during UDC-phase).			a2,	c2

^{*} Not for PU21.

	function	terminatio	ns (Fig.	2)
	Idiotoli	connector 1	connector 2	
R/WPM	Write signal to CP21/CP24, M21/M22 or RI20* to store data in program memory (active HIGH).		a14,	c14
WEPC	Write enable signal to central processor; prepares central processor to store data on DIO ₀₋₃ in scratchpad memory (active LOW, only during UDC-phase).	c28		
WPSM	Write pulse for scratchpad memory; signal to store data on DIO _{0.3} into scratchpad memory.		a13,	c13

Connection to programming unit PU20

line	function	terminations (Fig. 2) connector 3
CLDT	clock signal for data transfer between PU20/2 and PU21/PU23.	2
DIP	data from PU21/PU23 to PU20/2.	8
DPI	data from PU20/2 to PU21/PU23.	7
READY	ready signal to PU20/2, indicating that PU21/PU23 is available for data transfer.	9
SSE	system stop enable.	4
TRANSFER	data transfer required by PU20/2.	3

^{*} Not for PU21.

MECHANICAL DATA
Outlines

Dimensions in mm

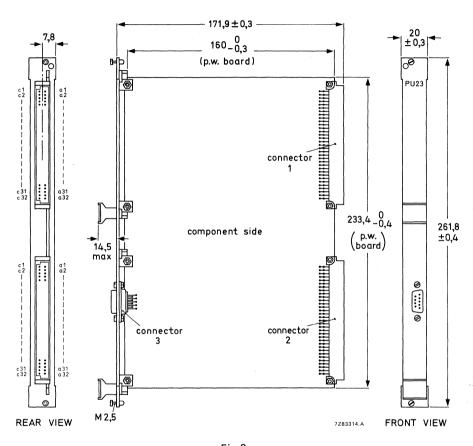


Fig. 2.

Mass

approx. 270 g

Terminal location

connector 1				connector 2	
row c		row a	row c		row a
INSS ₀	1	INS ₀	PABE	1	PABE
INSS ₁	2	INS ₁	PDBE	2	PDBE
INSS ₂	3	INS ₂	CPSD	3	CPSD
INSS ₃	4	INS ₃	CPSI	4	CPSI
INSS ₄	5	INS ₄	<u>CPSC</u>	5	CPSC
ADDS ₀	6	ADD_0	HOLD	6	HOLD
ADDS ₁	7	ADD ₁	CLOCK	7	CLOC
ADDS ₂	8	ADD ₂	n.c.	8	n.c.
ADDS3	9	ADD ₃	n.c.	9	n.c.
ADDS ₄	10	ADD ₄	n.c.	10	n.c.
ADDS ₅	11	ADD ₅	n.c.	11	n.c.
ADDS ₆	12	ADD ₆	n.c.	12	n.c.
ADDS ₇	13	ADD ₇	WPSM	13	WPSM
ADDS ₈	14	ADD ₈	\overline{R} /WPM	14	R/WPI
ADDS ₉	15	ADD ₉	n.c.	15	n.c.
ADDS ₁₀	16	ADD ₁₀	APM_{O}	16	APM _O
PB ₁	17	PB _O	APM ₁	17	APM ₁
RR [°]	18	RR	APM ₂	18	APM ₂
DIO ₀	19	DIO ₀	APM3	19	APM3
DIO ₁	20	DIO ₁	APM4	20	APM ₄
DIO2	21	DIO_2	APM ₅	21	APM ₅
DIO3	22	DIO_3^2	APM6	22	APM ₆
PHC_0	23	PHC ₁	APM ₇	23	APM ₇
n.c.	24	n.c.	APM ₈	24	APM8
n.c.	25	n.c.	APMg	25	APMg
SBI	26	n.c.	APM ₁₀	26	APM ₁
n.c.	27	n.c.	APM11	27	APM ₁
WEPC	28	n.c.	APM 12	28	APM ₁
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V _p	31	V _p	V_p	31	V_p
οV	32	οV	οV	32	οV

Connector 3 (front panel)

1	i.c.
2	CLDT
3	TRANSFER
4	SSE
5	+ 5 V*
6	i.c.
7	DPI
8	DIP
9	READY

n.c. = not connected i.c. = internal connected

^{*} No supply line; is used as a common line for the control signals.



BACK PANELS

APPLICATION

These back panels are for use in 19 inch racks, to accommodate the modules of the PC20 system. Use of these panels eliminates the need to wire separate connectors to receive the modules.

DESCRIPTION

The back panels incorporate female connectors which mate with the male counterparts of the PC20 modules. Type BP23 consists of two back panels. The upper panel (BP23A) provides the required interconnections for connector 1 of a PU21/PU23, MM module, CP module and of eighteen input/output modules. It has solder pads for allocation of the addresses of the input/output modules. The lower panel (BP23B) provides the interconnections for connector 2 of a PU21/PU23, MM module and CP module. External connections to the lower connectors of the input/output modules must be made individually; for this purpose connecting cables are available, see Table 1. Back panels BP25 and BP26 are used in extension racks to accommodate additional input/output modules. Type BP25 is for 15 input/output modules, type BP26 for 21. These types, of course, are only upper back panels.

The back panels carry a four-terminal block for external connection of the 10 V supply. Interconnection between the panels can be made via a ribbon cable (see Table 2); for this purpose, the panels incorporate an F303 male header.

The back panels are fixed to the rack with M2,5 x 10 screws, using threaded rails and isolation strips.

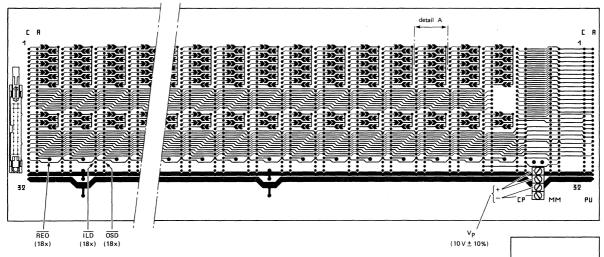
Table 1 Connecting cables

type	description	catalogue number
CC20	connecting cable for module OM21	9390 293 50000
CC21	connecting cable for module SO20	9390 293 60000
CC22	connecting cable for module IM20	9390 293 70000
CC23	connecting cable for modules IM20 and OM20	9390 293 80000

Table 2 Bus extension cables (see also Fig. 5)

type	description	catalogue number
BI21	bus extension cable for one I/O extension rack	4322 027 37910
B122	bus extension cable with bus interface for two I/O extension racks	4322 027 37920
B123	bus extension cable with bus interface for three I/O extension racks	4322 027 37930

BP23 BP25 BP26



detail A

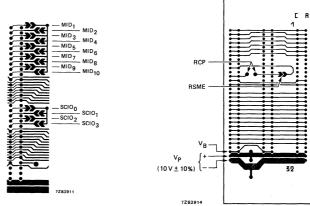
Fig. 1 Back panels BP23A (upper) and BP23B (lower), seen from rear of rack.

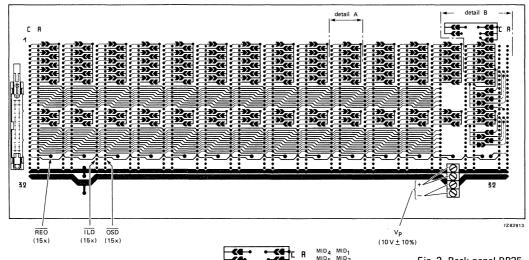
CP = central processor;

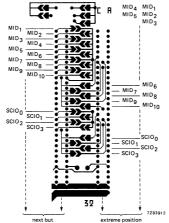
MM = memory module;

PU = programming unit interface (PU21/PU23).

For terminal location of the male header, see last page of this data sheet.







extreme position

Fig. 2 Back panel BP25, see from rear of rack.

For terminal location of the male header, see last page of this data sheet.

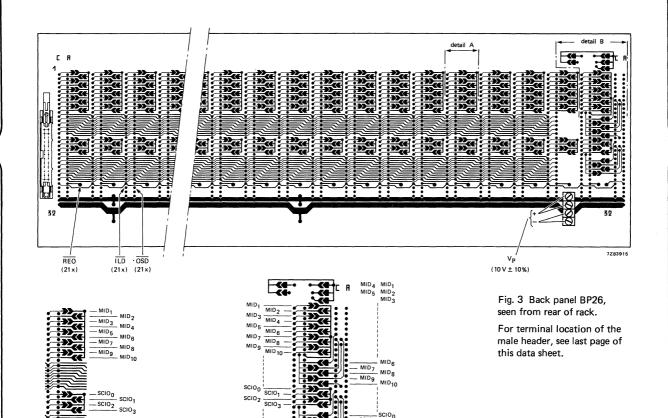
detail B

- MID3 _ MID4

detail A

BP23 BP25 BP26

BP23 BP25 BP26



next but extreme position

detail A

detail B

7Z83912

extreme position

Connection of control signals and external battery

Control signals can be connected to the connecting points on the rear side of the back panels (see Figs 1, 2 and 3. The functions of the control signals are indicated in the table below. RCP and RSME signals are only applicable to panel BP23A.

connecting points	function
ĪLD	Indication LED disable; input current low: 0,1 mA.
REO	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 0,1 mA.
OSD	Output stage disable for all stages; input current low: 10 mA.
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current = 2 mA.
RSME	Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current is 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.
V _B	External battery connection for saving the contents of the program memory and/or the scratchpad memory, in case of power failure. If central processor CP21/CP24 or memory module MM21/MM22 is used, this battery is parallel to the on-board battery and the retention time is lengthened.

Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratchpad memory of the central processor. This address is allocated by bridging the appropriate MID-pads (MID₁ to MID₁₀) on the back panels.

Separation of inputs and outputs of modules RP20 and RS20

Inputs and outputs are separated by bridging the appropriate SCIO-pads (SCIO $_{0}$ to SCIO $_{3}$) on the back panels.

Connection for logic supply voltage

The logic voltage (V_p) is 10 V \pm 10%. It can be connected to the four-terminal connecting block on the back panels. This connection is only applicable if there is no SO20 module provided.

Note: For full information see PC20 user manual.

Terminal location of F303 male header

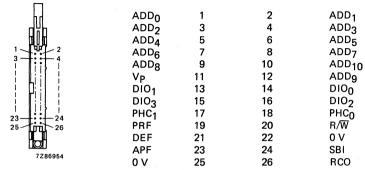
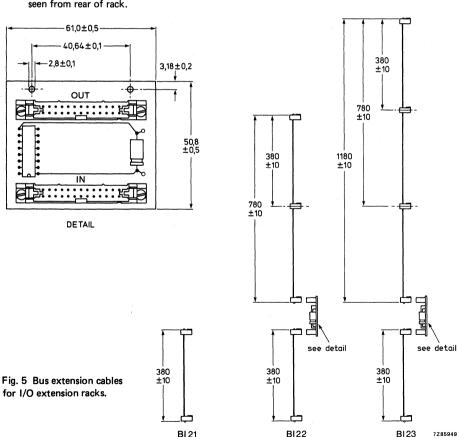


Fig. 4 Male header, seen from rear of rack.



SMALL CONTROLLER CABINET

APPLICATION

This cabinet is designed for accommodating PC20 modules, for easy assembling of small controller systems.

DESCRIPTION

This metal cabinet houses a programming unit interface PU21/PU23, a central processor CP20 or CP21/CP24, a supply and output module SO20 and six input/output modules.

The cabinet has back panels, so the work of wiring separate connectors to receive the male connectors of the modules is eliminated.

The upper panel BP20 provides the required interconnections for connector 1 of a PU21/PU23, CP20 or CP21/CP24 and an SO20 module, and of six input/output modules. It has solder bridges for allocating the addresses of the input/output modules.

The lower panel BP21 provides the interconnections for connector 2 of a PU21/PU23, CP20 or CP21/CP24 and an SO20 module; type BP22 provides for connector 2 of an input/output module, type BP27 provides for connector 2 of output module OM22 or input module IM22. These panels have connecting blocks with screw terminals for connection of supply voltages and input and output circuits. Furthermore, panel BP21 has connecting points for the control signals.

The cabinet is supplied with one panel BP22 but space is provided for another five BP22 or BP27 panels, which must be ordered separately.

The connections to the outside world are protected by the sloping cover on the lower part of the cabinet. Openings in the underside provide entry of the input/output cables. The cabinet is intended for wall mounting.

Note: For larger controller systems, back panels BP23, BP25 and BP26 are available, to be used in 19 inch racks; see the relevant data sheet.

MECHANICAL DATA Outlines

Dimensions in mm

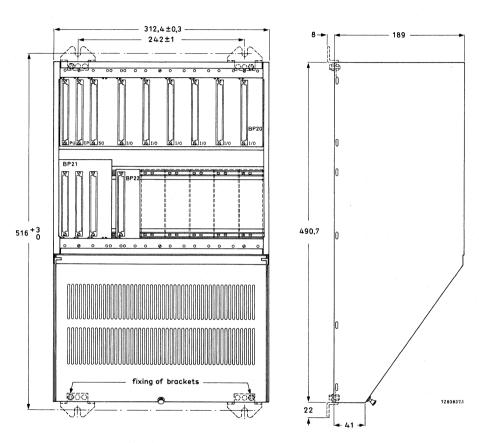


Fig. 1 Small controller cabinet.

Cabinet, material colour

steel black

Mass

5,2 kg

Small controller cabinet SC20

ENVIRONMENTAL DATA

Maximum permissible temperature, measured 5 cm above the cabinet

60 °C

MOUNTING OF THE CABINET

Four mounting brackets can be fitted to the cabinet (Fig. 1). They are supplied with bolts and washers with the cabinet.

The cabinet can be fixed to a wall with M6 bolts. In some cases, e.g. if the wall is not flat, it is sufficient to use three mounting brackets (one at the top and two at the bottom of the cabinet).

The cabinet must be positioned so that air has free access.

MOUNTING OF ADDITIONAL BACK PANELS BP22 AND BP27

The back panel BP22 or BP27 has to be positioned through the openings in the bottom of the cabinet, to avoid bending of the panel. It is fitted to the mounting strip in the cabinet by means of the four $M2.5 \times 10$ screws, which are supplied with the cabinet. Two of these screws also secure the female connector. Before tightening the screws, the panel has to be aligned. To this end an input/output module has to be slid carefully into the cabinet, so that its connectors are fully mated with their counterparts on the back panel. The lower two screws can then be tightened and, after removing the module, the fixing screws of the connector can be tightened.

Catalogue number of back panel BP22: 4322 027 92140. Catalogue number of back panel BP27: 4322 027 93950.

ACCESSORIES

To give sufficient space for connection of the input/output cables to the connecting blocks on back panels BP22 and BP27, the various input/output modules in the cabinet are 15 mm apart. To cover these spaces front plates FP20 are available.

Unused module spaces, can be covered with a front plate FP21.

Catalogue number of front plate FP20 (15 mm width): 4322 027 92150. Catalogue number of front plate FP21 (20 mm width): 4322 027 92160.

INSTALLATION

Connection of control signals and external battery

Control signals can be connected to the connecting points on the lower end of back panel BP21 (see Fig. 2). The functions of the control signals are indicated in the table below.

Note: Use of control signals ILD, REO and OSD requires interconnections between back panels BP20 and BP21 (see Fig. 2).

connecting points	function
ĪLD	Indication LED disable; input current low: 0,1 mA.
REO	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 10 mA.
OSD	Output stage disable for all stages; input current low: 10 mA.
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current = 2 mA.
RSME	Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.
± BATT	External battery connection for saving the contents of the program/scratchpad memories, in case of power failure. If central processor CP21/CP24 is used, this battery is parallel to the on-board battery and the retention time is lengthened.
ALE	Alarm external; active low as long as V _{ic} is above 17,5 V; with photo-isolator between internal and external supply.

SC20

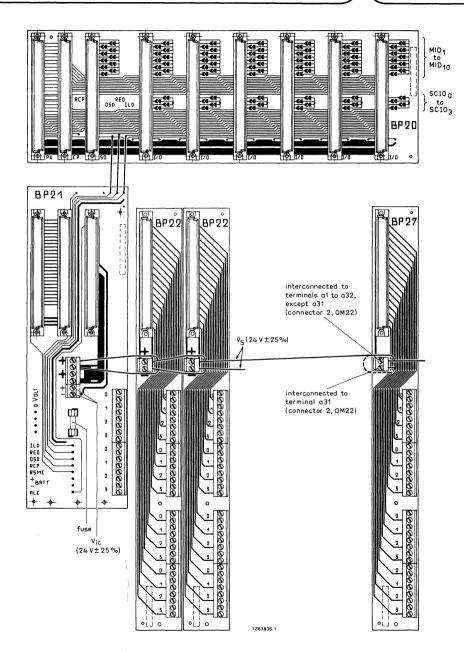


Fig. 2 Back panel arrangement. See also note at the top of the next page.

Note to Fig. 2 on the preceding page: If all outputs of the OM22 are used in grounded load configuration, an interconnection between the two connecting points of the small connecting block of back panel BP27 has to be used (indicated with a dashed line). This interconnection has not to be made if the first 16 output stages of the OM22 are used with pull-down resistors, e.g. to drive TTL circuitry. See also data sheet OM22.

Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratchpad memory of the central processor. This address is allocated by bridging the appropriate MID-pads (MID₁ to MID₁₀) on back panel BP20, see Fig. 2.

Coding of inputs and outputs on modules RP20 and RS20

The coding of inputs and outputs is done by bridging the appropriate SCIO-pads (SCIO₀ to SCIO₃) on back panel BP20, see Fig. 2.

Connection of input and output circuits

The input circuits of the input modules and the output circuits of the output modules should be connected to the large connecting blocks on back panel(s) BP22, with the exception of the modules IM22, OM22, SO20:

- the input circuits of IM22 and output circuits of OM22 to be connected to the large connecting blocks on back panel(s) BP27,
- the output circuits of SO20 to be connected to the large connecting block on back panel BP21, see Fig. 2.

Connection of supply voltage for 24 V/10 V d.c.-d.c. converter of module SO20

The supply voltage for the converter (V_{ic}) is 24 V \pm 25%. It should be connected to the terminals of the small connecting block on back panel BP21, see Fig. 2. A fuse (I_n = 1,6 A, delayed action) protects the supply against short-circuit in the converter.

Connection of supply voltage for output modules

The supply voltage for the output modules (V_S) is 24 V \pm 25%. It should be connected to the double connecting block on back panel BP21 and the small connecting block on the panel(s) BP22 and BP27 (only + connection), see Fig. 2.

Note: For full information see PC20 Manual.

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