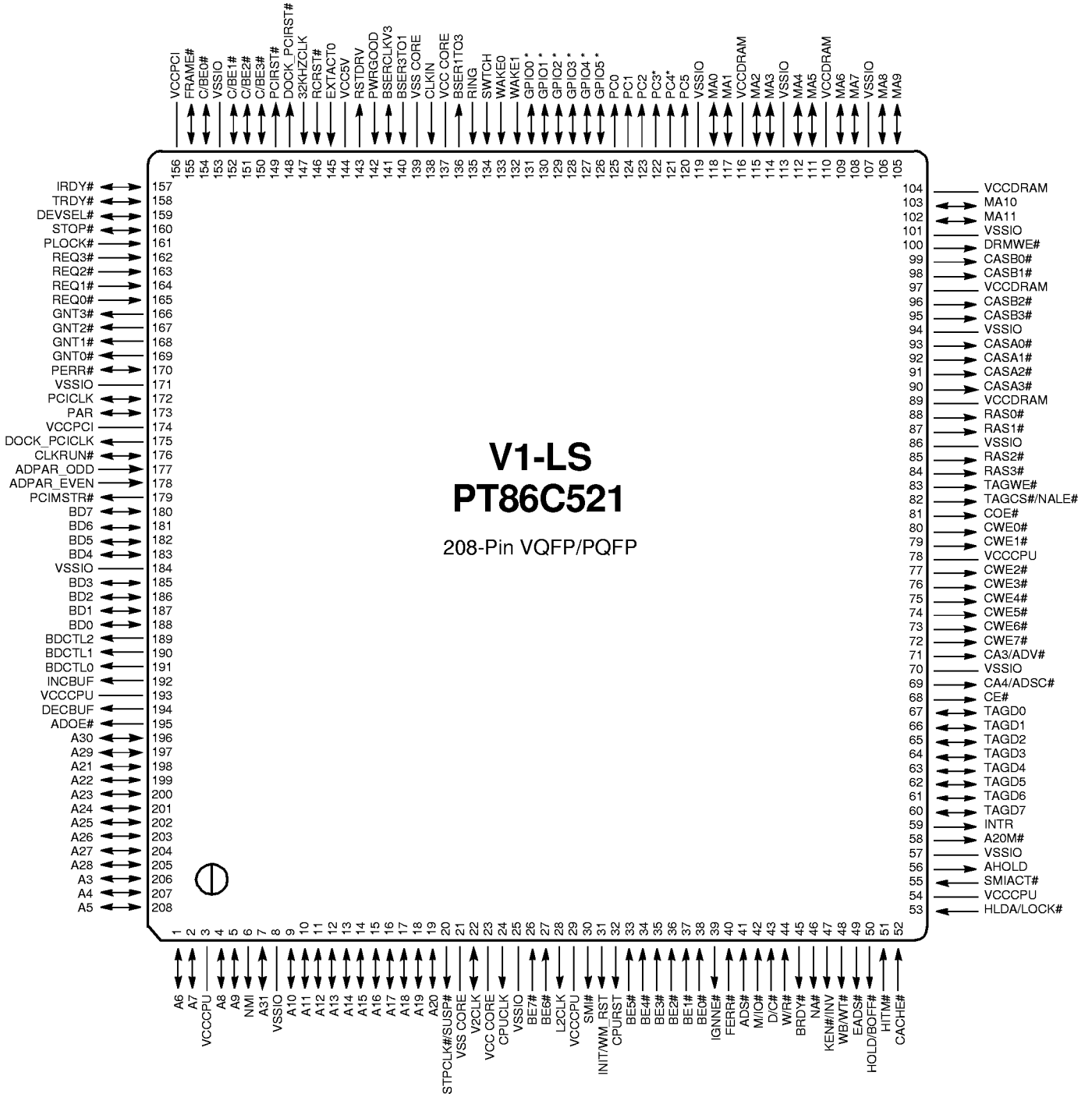
1. V1-LS PIN INFORMATION

1.1 Pin Diagram



NOTE: Multiplexed GPIO and PC signals are shown with an asterisk (*). Refer to Section 4.4.60 on page 1-193 for additional details on the multiplexing scheme.

1.2 Pin Cross Reference by Pin Numbe r

Table 1-1. Pin Assignment T able (Arranged by Pin Number)

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
1	A6	I/O	T	3.3-V	VCCCPU	CPU
2	A7	I/O	T	3.3-V	VCCCPU	CPU
3	VCCCPU	PWR		3.3-V	VCCCPU	POWER
4	A8	I/O	T	3.3-V	VCCCPU	CPU
5	A9	I/O	T	3.3-V	VCCCPU	CPU
6	NMI	O		3.3-V	VCCCPU	CPU
7	A31	I/O	T	3.3-V	VCCCPU	CPU
8	VSSIO	GND			VSSIO	GROUND
9	A10	I/O	T	3.3-V	VCCCPU	CPU
10	A11	I/O	T	3.3-V	VCCCPU	CPU
11	A12	I/O	T	3.3-V	VCCCPU	CPU
12	A13	I/O	T	3.3-V	VCCCPU	CPU
13	A14	I/O	T	3.3-V	VCCCPU	CPU
14	A15	I/O	T	3.3-V	VCCCPU	CPU
15	A16	I/O	T	3.3-V	VCCCPU	CPU
16	A17	I/O	T	3.3-V	VCCCPU	CPU
17	A18	I/O	T	3.3-V	VCCCPU	CPU
18	A19	I/O	T	3.3-V	VCCCPU	CPU
19	A20	I/O	T	3.3-V	VCCCPU	CPU
20	STPCLK#/SUSP#	O		3.3-V	VCCCPU	CPU
21	VSS CORE	GND			VSSC	GROUND
22	V2CLK	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
23	VCC CORE	PWR		3.3-V	VCC CORE	POWER
24	CPUCLK	O		3.3-V	VCCCPU	CPU
25	VSSIO	GND			VSSIO	GROUND
26	BE7#	I	T	3.3-V	VCCCPU	CPU
27	BE6#	I	T	3.3-V	VCCCPU	CPU
28	L2CLK	O		3.3-V	VCCCPU	L2 CACHE
29	VCCCPU	PWR		3.3-V	VCCCPU	POWER

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
30	SMI#	O		3.3-V	VCCCPU	CPU
31	INIT/WM_RST	O		3.3-V	VCCCPU	CPU
32	CPURST	O		3.3-V	VCCCPU	CPU
33	BE5#	I	T	3.3-V	VCCCPU	CPU
34	BE4#	I	T	3.3-V	VCCCPU	CPU
35	BE3#	I	T	3.3-V	VCCCPU	CPU
36	BE2#	I	T	3.3-V	VCCCPU	CPU
37	BE1#	I	T	3.3-V	VCCCPU	CPU
38	BE0#	I	T	3.3-V	VCCCPU	CPU
39	IGNNE#	O		3.3-V	VCCCPU	CPU
40	FERR#	I	T	3.3-V	VCCCPU	CPU
41	ADS#	I	T	3.3-V	VCCCPU	CPU
42	M/IO#	I	T	3.3-V	VCCCPU	CPU
43	D/C#	I	T	3.3-V	VCCCPU	CPU
44	W/R#	I	T	3.3-V	VCCCPU	CPU
45	BRDY#	O		3.3-V	VCCCPU	CPU
46	NA#	O		3.3-V	VCCCPU	CPU
47	KEN#/INV	O		3.3-V	VCCCPU	CPU
48	WB/WT#	O		3.3-V	VCCCPU	CPU
49	EADS#	O		3.3-V	VCCCPU	CPU
50	HOLD/BOFF#	O		3.3-V	VCCCPU	CPU
51	HITM#	I	T	3.3-V	VCCCPU	CPU
52	CACHE#	I	T	3.3-V	VCCCPU	CPU
53	HLDA/LOCK#	I	T	3.3-V	VCCCPU	CPU
54	VCCCPU	PWR		3.3-V	VCCCPU	POWER
55	SMIACT#	I	T	3.3-V	VCCCPU	CPU
56	AHOLD	O		3.3-V	VCCCPU	CPU
57	VSSIO	GND			VSSIO	GROUND
58	A20M#	O		3.3-V	VCCCPU	CPU
59	INTR	O		3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
60	TAGD7	I/O	T	3.3-V	VCCCPU	L2 CACHE
61	TAGD6	I/O	T	3.3-V	VCCCPU	L2 CACHE
62	TAGD5	I/O	T	3.3-V	VCCCPU	L2 CACHE
63	TAGD4	I/O	T	3.3-V	VCCCPU	L2 CACHE
64	TAGD3	I/O	T	3.3-V	VCCCPU	L2 CACHE
65	TAGD2	I/O	T	3.3-V	VCCCPU	L2 CACHE
66	TAGD1	I/O	T	3.3-V	VCCCPU	L2 CACHE
67	TAGD0	I/O	T	3.3-V	VCCCPU	L2 CACHE
68	CE#	O		3.3-V	VCCCPU	L2 CACHE
69	CA4/ADSC#	O		3.3-V	VCCCPU	L2 CACHE
70	VSSIO	GND			VSSIO	GROUND
71	CA3/ADV#	O		3.3-V	VCCCPU	L2 CACHE
72	CWE7#	O		3.3-V	VCCCPU	L2 CACHE
73	CWE6#	O		3.3-V	VCCCPU	L2 CACHE
74	CWE5#	O		3.3-V	VCCCPU	L2 CACHE
75	CWE4#	O		3.3-V	VCCCPU	L2 CACHE
76	CWE3#	O		3.3-V	VCCCPU	L2 CACHE
77	CWE2#	O		3.3-V	VCCCPU	L2 CACHE
78	VCCCPU	PWR		3.3-V	VCCCPU	POWER
79	CWE1#	O		3.3-V	VCCCPU	L2 CACHE
80	CWE0#	O		3.3-V	VCCCPU	L2 CACHE
81	COE#	O		3.3-V	VCCCPU	L2 CACHE
82	TAGCS#/NALE#	O		3.3-V	VCCCPU	L2 CACHE
83	TAGWE#	O		3.3-V	VCCCPU	L2 CACHE
84	RAS3#	O		3.3-V/5-V	VCCDRAM	DRAM
85	RAS2#	O		3.3-V/5-V	VCCDRAM	DRAM
86	VSSIO	GND			VSSIO	GROUND
87	RAS1#	O		3.3-V/5-V	VCCDRAM	DRAM
88	RAS0#	O		3.3-V/5-V	VCCDRAM	DRAM
89	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
90	CASA3#	O		3.3-V/5-V	VCCDRAM	DRAM
91	CASA2#	O		3.3-V/5-V	VCCDRAM	DRAM
92	CASA1#	O		3.3-V/5-V	VCCDRAM	DRAM
93	CASA0#	O		3.3-V/5-V	VCCDRAM	DRAM
94	VSSIO	GND			VSSIO	GROUND
95	CASB3#	O		3.3-V/5-V	VCCDRAM	DRAM
96	CASB2#	O		3.3-V/5-V	VCCDRAM	DRAM
97	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
98	CASB1#	O		3.3-V/5-V	VCCDRAM	DRAM
99	CASB0#	O		3.3-V/5-V	VCCDRAM	DRAM
100	DRMWE#	O		3.3-V/5-V	VCCDRAM	DRAM
101	VSSIO	GND			VSSIO	GROUND
102	MA11	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
103	MA10	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
104	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
105	MA9	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
106	MA8	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
107	VSSIO	GND			VSSIO	GROUND
108	MA7	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
109	MA6	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
110	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
111	MA5	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
112	MA4	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
113	VSSIO	GND			VSSIO	GROUND
114	MA3	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
115	MA2	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
116	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
117	MA1	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
118	MA0	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
119	VSSIO	GND			VSSIO	GROUND

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
120	PC5	O		5-V	VCC-5V	PMC
121	PC4*	O		5-V	VCC-5V	PMC
122	PC3*	O		5-V	VCC-5V	PMC
123	PC2	O		5-V	VCC-5V	PMC
124	PC1	O		5-V	VCC-5V	PMC
125	PC0	O		5-V	VCC-5V	PMC
126	GPIO5*	I/O	T	5-V	VCC-5V	PMC
127	GPIO4*	I/O	T	5-V	VCC-5V	PMC
128	GPIO3*	I/O	T	5-V	VCC-5V	PMC
129	GPIO2*	I/O	T	5-V	VCC-5V	PMC
130	GPIO1*	I/O	T	5-V	VCC-5V	PMC
131	GPIO0*	I/O	T	5-V	VCC-5V	PMC
132	WAKE1	I	T	5-V	VCC-5V	PMC
133	WAKE0	I	T	5-V	VCC-5V	PMC
134	SWTCH	I	T	5-V	VCC-5V	PMC
135	RING	I	T	5-V	VCC-5V	PMC
136	BSER1TO3	O		5-V	VCC-5V	V1-LS/V3-LS
137	VCC CORE	PWR		3.3-V	VCC CORE	POWER
138	CLKIN	I	C	5-V	VCC-5V	CLOCK
139	VSS CORE	GND			VSSC	GROUND
140	BSER3TO1	I	T	5-V	VCC-5V	V1-LS/V3-LS
141	BSERCLKV3	I/O	T	5-V	VCC-5V	V1-LS/V3-LS
142	PWRGOOD	I	T	5-V	VCC-5V	RESET
143	RSTDRV	O		5-V	VCC-5V	RESET
144	VCC5V	PWR		5-V	VCC-5V	POWER
145	EXTACT0	I	T	5-V	VCC-5V	PMC
146	RCRST#	I	T	5-V	VCC-5V	RESET
147	32KHZCLK	I	S	5-V	VCC-5V	CLOCK
148	DOCK_PCIRST#	O		3.3-V/5-V	VCCPCI	PCI
149	PCIRST#	O		3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
150	C/BE3#	I/O	T	3.3-V/5-V	VCCPCI	PCI
151	C/BE2#	I/O	T	3.3-V/5-V	VCCPCI	PCI
152	C/BE1#	I/O	T	3.3-V/5-V	VCCPCI	PCI
153	VSSIO	GND			VSSIO	GROUND
154	C/BE0#	I/O	T	3.3-V/5-V	VCCPCI	PCI
155	FRAME#	I/O	T	3.3-V/5-V	VCCPCI	PCI
156	VCCPCI	PWR			VCCPCI	POWER
157	IRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
158	TRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
159	DEVSEL#	I/O	T	3.3-V/5-V	VCCPCI	PCI
160	STOP#	I/O	T	3.3-V/5-V	VCCPCI	PCI
161	PLOCK#	I	T	3.3-V/5-V	VCCPCI	PCI
162	REQ3#	I	T	3.3-V/5-V	VCCPCI	PCI
163	REQ2#	I	T	3.3-V/5-V	VCCPCI	PCI
164	REQ1#	I	T	3.3-V/5-V	VCCPCI	PCI
165	REQ0#	I	T	3.3-V/5-V	VCCPCI	PCI
166	GNT3#	O		3.3-V/5-V	VCCPCI	PCI
167	GNT2#	O		3.3-V/5-V	VCCPCI	PCI
168	GNT1#	O		3.3-V/5-V	VCCPCI	PCI
169	GNT0#	O		3.3-V/5-V	VCCPCI	PCI
170	PERR#	I/O	T	3.3-V/5-V	VCCPCI	PCI
171	VSSIO	GND			VSSIO	GROUND
172	PCICLK	I/O	T	3.3-V/5-V	VCCPCI	PCI
173	PAR	I/O	T	3.3-V/5-V	VCCPCI	PCI
174	VCCPCI	PWR			VCCPCI	POWER
175	DOCK_PCICLK	O		3.3-V/5-V	VCCPCI	PCI
176	CLKRUN#	I/O	T	3.3-V/5-V	VCCPCI	PCI
177	ADPAR_ODD	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
178	ADPAR_EVEN	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
179	PCIMSTR#	O		3.3-V	VCCCPU	V1-LS/V2-LS

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
180	BD7	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
181	BD6	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
182	BD5	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
183	BD4	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
184	VSSIO	GND			VSSIO	GROUND
185	BD3	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
186	BD2	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
187	BD1	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
188	BD0	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
189	BDCTL2	O		3.3-V	VCCCPU	V1-LS/V2-LS
190	BDCTL1	O		3.3-V	VCCCPU	V1-LS/V2-LS
191	BDCTL0	O		3.3-V	VCCCPU	V1-LS/V2-LS
192	INCBUF	O		3.3-V	VCCCPU	V1-LS/V2-LS
193	VCCCPU	PWR		3.3-V	VCCCPU	POWER
194	DECBUF	O		3.3-V	VCCCPU	V1-LS/V2-LS
195	ADOE#	O		3.3-V	VCCCPU	V1-LS/V2-LS
196	A30	I/O	T	3.3-V	VCCCPU	CPU
197	A29	I/O	T	3.3-V	VCCCPU	CPU
198	A21	I/O	T	3.3-V	VCCCPU	CPU
199	A22	I/O	T	3.3-V	VCCCPU	CPU
200	A23	I/O	T	3.3-V	VCCCPU	CPU
201	A24	I/O	T	3.3-V	VCCCPU	CPU
202	A25	I/O	T	3.3-V	VCCCPU	CPU
203	A26	I/O	T	3.3-V	VCCCPU	CPU
204	A27	I/O	T	3.3-V	VCCCPU	CPU
205	A28	I/O	T	3.3-V	VCCCPU	CPU
206	A3	I/O	T	3.3-V	VCCCPU	CPU
207	A4	I/O	T	3.3-V	VCCCPU	CPU
208	A5	I/O	T	3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

1.3 Pin Cross Reference by Pin Name

Table 1-2. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
32KHZCLK	147	A30	196	BSER3TO1	140
A3	206	A31	7	C/BE0#	154
A4	207	ADOE#	195	C/BE1#	152
A5	208	ADPAR_EVEN	178	C/BE2#	151
A6	1	ADPAR_ODD	177	C/BE3#	150
A7	2	ADS#	41	CA3/ADV#	71
A8	4	AHOLD	56	CA4/ADSC#	69
A9	5	BD0	188	CACHE#	52
A10	9	BD1	187	CASA0#	93
A11	10	BD2	186	CASA1#	92
A12	11	BD3	185	CASA2#	91
A13	12	BD4	183	CASA3#	90
A14	13	BD5	182	CASB0#	99
A15	14	BD6	181	CASB1#	98
A16	15	BD7	180	CASB2#	96
A17	16	BDCTL0	191	CASB3#	95
A18	17	BDCTL1	190	CE#	68
A19	18	BDCTL2	189	CLKIN	138
A20	19	BE0#	38	CLKRUN#	176
A20M#	58	BE1#	37	COE#	81
A21	198	BE2#	36	CPUCLK	24
A22	199	BE3#	35	CPURST	32
A23	200	BE4#	34	CWE0#	80
A24	201	BE5#	33	CWE1#	79
A25	202	BE6#	27	CWE2#	77
A26	203	BE7#	26	CWE3#	76
A27	204	BRDY#	45	CWE4#	75
A28	205	BSERCLKV3	141	CWE5#	74
A29	197	BSER1TO3	136	CWE6#	73

Table 1-2. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
CWE7#	72	M/IO#	42	RAS3#	84
D/C#	43	MA0	118	RCRST#	146
DECBUF	194	MA1	117	REQ0#	165
DEVSEL	159	MA2	115	REQ1#	164
DOCK_PCICLK	175	MA3	114	REQ2#	163
DOCK_PCIRST#	148	MA4	112	REQ3#	162
DRMWE#	100	MA5	111	RING	135
EADS#	49	MA6	109	RSTDRV	143
EXTACT0	145	MA7	108	SMI#	30
FERR#	40	MA8	106	SMIACT#	55
FRAME#	155	MA9	105	STOP#	160
GNT0#	169	MA10	103	STPCLK#/SUSP#	20
GNT1#	168	MA11	102	SWTCH	134
GNT2#	167	NA#	46	TAGCS#/NALE#	82
GNT3#	166	NMI	6	TAGD0	67
GPIO0*	131	PAR	173	TAGD1	66
GPIO1*	130	PC0	125	TAGD2	65
GPIO2*	129	PC1	124	TAGD3	64
GPIO3*	128	PC2	123	TAGD4	63
GPIO4*	127	PC3*	122	TAGD5	62
GPIO5*	126	PC4*	121	TAGD6	61
HITM#	51	PC5	120	TAGD7	60
HLDA/LOCK#	53	PCICLK	172	TAGWE#	83
HOLD/BOFF#	50	PCIMSTR#	179	TRDY#	158
IGNNE#	39	PCIRST#	149	V2CLK	22
INCBUF	192	PERR#	170	VCC5-V	144
INIT/WM_RST	31	PLOCK#	161	VCC CORE	23
INTR	59	PWRGOOD	142	VCC CORE	137
IRDY#	157	RAS0#	88	VCCCPU	3
KEN#/INV	47	RAS1#	87	VCCCPU	29
L2CLK	28	RAS2#	85	VCCCPU	54

Table 1-2. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
VCCCPU	78	VSS CORE	139	VSSIO	113
VCCCPU	193	VSSIO	8	VSSIO	119
VCCDRAM	89	VSSIO	25	VSSIO	153
VCCDRAM	97	VSSIO	57	VSSIO	171
VCCDRAM	104	VSSIO	70	VSSIO	184
VCCDRAM	110	VSSIO	86	W/R#	44
VCCDRAM	116	VSSIO	94	WAKE0	133
VCCPCI	156	VSSIO	101	WAKE1	132
VCCPCI	174	VSSIO	107	WB/WT#	48
VSS CORE	21				

2. V1-LS DETAILED PIN DESCRIPTIONS

This chapter contains a detailed functional description of the pins on PT86C521. For ease of reference, the pins are arranged alphabetically within each of the following functional interface groups:

- CPU Interface (CPU)
- DRAM Interface (DRAM)
- L2 Cache Interface (L2 CACHE)
- PCI Interface (PCI)
- Power Management Interface (PMC)
- PT86C521 / V2-LS Interface (V1-LS / V2-LS)
- V1-LS / V3-LS Interface (V1-LS / V3-LS)
- Reset and Clock Interface (RESET / CLOCK)
- Power and Ground (POWER / GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the '#' symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed or have dual functionality and use the same pin for all functions.

The following conventions have been used to describe the pin type: 'I' = input-only pins; 'O' = output-only pins; 'I/O' = bi-directional pins; 'PWR' = power pins, and 'GND' = ground pins. The pin type is defined relative to the V1-LS device.

For a list of pins arranged by pin number, refer to Section 1.2 on page 1-15. For a list of pins arranged by pin name, refer to Section 1.3 on page 1-22.

2.1 CPU Interface

Pin Name	Type	Description
A20M#	O	**ADDRESS BIT 20 MASK#** : This output to the CPU indicates that the CPU should mask A20 in order to emulate the 8086 address wrap-around.
A[31:3]	I/O	**CPU ADDRESS LINES [31:3]** : These are address lines that together with the byte enable signals (BE[7:0]#) make the address bus and define the physical area of memory or I/O accessed; they are driven as outputs during bus master cycles.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
ADS#	I	**ADDRESS STROBE#** : This input indicates the presence of a new valid bus cycle currently being driven by the CPU. ADS# is driven active in the first clock of a bus cycle and is driven inactive in the second or subsequent clocks of the cycle. ADS# is driven inactive when the bus is idle.
AHOLD	O	**ADDRESS HOLD** : This output is used in conjunction with EADS# for write-protecting a cacheable ROM region.
BE[7:0]#	I	**CPU BYTE ENABLE [7:0]** : The byte enable pins are used to determine which bytes must be written to memory, or which bytes were requested by the processor for the current cycle. They help define the physical area of the memory or I/O accessed. Byte enable pins are driven in the same clock as ADS#. They are driven with the same timing as the address lines A[31:3].
BRDY#	O	**BURST READY#:** This output to the Pentium processor indicates completion of the current cycle. BRDY# indicates that the V2-LS has presented valid data in response to a read, or that it has accepted the data from the Pentium processor in response to a write request.
CACHE#	I	**CACHE#:** This input from the Pentium processor indicates a CPU cacheable/burstable operation.
CPUCLK	O	**CPU CLOCK OUTPUT:** This will be the clock output from V1-LS to the CPU.
CPURST	O	**CPU RESET:** This output resets the CPU.
D/C#	I	**DATA_CODE#:** This cycle-definition input from the Pentium processor indicates whether the current cycle is a data or a code/special access. The D/C# pin is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after the earlier of NA# or the last BRDY#.
EADS#	O	**EXTERNAL ADDRESS STROBE#:** This output to the Pentium processor indicates that a valid address has been driven onto the CPU address bus for internal cache snoop cycle.
FERR#	I	**FLOATING-POINT ERROR#:** This output pin from the Pentium processor is used for floating-point error reporting.
HITM#	I	**HITM#:** This input indicates that the snoop cycle hit a modified line in the level-1 cache inside the CPU such that V1-LS should suspend the master operation, allow the CPU to evict the modified line, and then restart the master cycle.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
HLDA/LOCK#	I	**HOLD ACKNOWLEDGE:** This input from the Pentium processor indicates a Hold Acknowledge state. **LOCK#:** Indicates to the system that the current sequence of bus cycles should not be interrupted.**Note:** This pin applies to Revision CC only.
HOLD/BOFF#	O	**HOLD REQUEST:** This output to the Pentium processor indicates a Hold Request state. **BACK OFF#:** The back off input is used to force the Pentium processor off the bus in the next clock.**Note:** This pin applies to Revision CC only.
IGNNE#	O	**IGNORE NUMERIC ERROR#:** This pin indicates that a floating-point error should be ignored.
INIT/WM_RST	O	**INIT:** This Pentium processor initialization input forces the Pentium processor to begin execution in a known state. The INIT/WM_RST will typically be asserted when software reset commands are written to either Port 64 or 92, or a shutdown cycle is detected. **WM_RST:** Cyrix 6x86 processor initialization input forces the processor to begin execution in a known state.
INTR	O	**MASKABLE INTERRUPT:** This pin indicates a maskable interrupt request to the Pentium processor.
INV	O	See KEN#.
KEN#/INV	O	**CACHE ENABLE# :** This output to the Pentium processor indicates that the current cycle is cacheable. **INV:** This output pin indicates a request to invalidate the processor cache line during snoop cycles. If this function is not used, CPU's INV pin should either be pulled high or connected to W/R#.
M/IO#	I	**MEMORY_INPUT & OUTPUT#:** This cycle-definition signal is one of the main pins that define the bus cycle. It distinguishes a memory access from an I/O access. This signal is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
NA#	O	**NEXT ADDRESS #:** NA# indicates to the Pentium processor that V1-LS is ready to accept a new bus cycle. This signal is used for CPU's pipelining feature.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
NMI	O	**NON-MASKABLE INTERRUPT:** This pin indicates that an external non-maskable interrupt has been generated.
SMI#	O	**SYSTEM MANAGEMENT INTERRUPT#:** This output triggers a system management interrupt and is used to invoke the SMM (system management mode).
SMIACT#	I	**SYSTEM MANAGEMENT INTERRUPT ACTIVE#:** This input from the Pentium processor indicates that the CPU is operating in SMM. Assertion of SMIACT# enables remapping of SMRAM to physical DRAM at 000A0000-000BFFFF region.
STPCLK#/SUSP#	O	**STOP CLOCK#:** This output indicates a stop clock request to Intel's Pentium and AMD's K5 processor. **SUSP#:** This output indicates a suspend request to Cyrix® 6x86 CPU.
SUSP#	O	See STPCLK#.
W/R#	I	**WRITE_READ#:** This is a cycle-definition input from the processor indicating whether the current cycle is a write or a read cycle. It is one of the primary bus cycle-definition pins. W/R# is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
WB/WT#	O	**WRITE-BACK_WRITE-THROUGH#:** This output to the processor allows a data cache line to be defined as write-back or write-through on a line-by-line basis.
WM_RST	O	See INIT.

2.2 DRAM Interface

Pin Name	Type	Description
CASA[3:0]# CASB[3:0]#	O	**COLUMN ADDRESS STROBES [3:0] GROUPS A AND B# :** In 64-bit bank mode, CASA[3:0]# corresponds to BE[3:0]# and CASB[3:0]# corresponds to BE[7:4]#. In 32-bit bank mode CASA[3:0]# outputs drive the CAS# inputs on DRAM bytes 3 to 0 in even banks (banks 0, 2, 4, 6) and CASB[3:0]# for odd banks (banks 1, 3, 5, 7).

2.2 DRAM Interface *(cont.)*

Pin Name	Type	Description
DRMWE#	O	**DRAM WRITE ENABLE# :** This output drives write-enable for all DRAM.
MA[11:0]	I/O	**MEMORY ADDRESSES [11:0] :** These outputs drive the MA lines for all DRAM. They are also used as RC-RESET configuration inputs during power up (on RCRST# rising edge).
RAS[3:0]#	O	**ROW ADDRESS STROBES [3:0]# :** These outputs drive the RAS# inputs on DRAM bank pairs 7/6, 5/4, 3/2, and 1/0 respectively.

2.3 L2 Cache Interface

Pin Name	Type	Description
ADSC#	O	See CA4.
ADV#	O	See CA3.
CA3/ADV#	O	**CACHE ADDRESS 3 :** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. **ADVANCE# :** This active-low output is used with synchronous SRAM to advance the internal SRAM burst counter, controlling burst accesses after the address is loaded.
CA4/ADSC#	O	**CACHE ADDRESS 4 :** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. **ADDRESS STATUS CONTROLLER# :** This active-low output is used with synchronous SRAM and interrupts any ongoing SRAM burst, causing a new address to be registered.
CE#	O	**CHIP ENABLE# :** Cache data RAM chip enable.
COE#	O	**CACHE OUTPUT ENABLE# :** Cache Data RAM output enable.
CWE[7:0]#	O	**CACHE WRITE ENABLE [7:0]# :** Cache data RAM byte write enables.
L2CLK	O	**L2 CLOCK:** This pin is a clock output to synchronous cache data RAM.
NALE#	O	See TAGCS#.

2.3 L2 Cache Interface *(cont.)*

Pin Name	Type	Description
TAGCS#/NALE#	O	**TAG RAM CHIP SELECT# :** TAG Data RAM chip select. **NEXT ADDRESS LATCH ENABLE# :** When using asynchronous SRAM, this output controls an external latch for the cache addresses necessary for pipelining.
TAGD[7:0]	I/O	**TAG RAM DATA BIT [7:0]:** These pins are used to compare addresses from the Pentium processor to determine L2 Cache cycles.
TAGWE#	O	**TAG RAM WRITE ENABLE# :** TAG Data RAM write enable.

2.4 PCI Interface

Pin Name	Type	Description
C/BE[3:0]#	I/O	**BUS COMMAND AND BYTE ENABLES [3:0]# :** Both command and byte enables are multiplexed on the same PCI pins. These pins define the Bus Command during the address phase and are used as Byte Enables during the data phase.
CLKRUN#	I/O	**CLOCK RUN#:** Used in the PCI mobile environment, this is a sustained tristate signal used by the central resource to request permission to stop or slow CLK.
DEVSEL#	I/O	**DEVICE SELECT#:** As an output it indicates whether V1-LS system memory is the target of the current address. As an input, V1-LS sees whether or not a PCI target exists.
DOCK_PCICLK	O	**PCI CLOCK FOR DOCKING STATION:** This signal is the PCI clock for the docking station. It provides timing for all transactions on the PCI bus in the docking station and is synchronous to PCICLK.
DOCK_PCIRST#	O	**PCI RESET FOR DOCKING STATION#:** This signal is the PCI reset for the docking station. When asserted, it resets all PCI devices in the docking station.
FRAME#	I/O	**FRAME#:** FRAME# is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addressed target.

2.4 PCI Interface *(cont.)*

Pin Name	Type	Description
GNT[3:0]#	O	**PCI GRANT [3:0]# :** When the bus arbiter has granted access to the master requesting the ownership of the PCI bus, the master is notified using this point-to-point signal. Each PCI bus master has its own GNT#.
IRDY#	I/O	**INITIATOR READY# :** This indicates the bus master's state of readiness to complete the current data phase. During a write, IRDY# shows that valid data is present. During a read, it indicates the bus master's readiness to accept data. IRDY# is used in conjunction with TRDY#.
PAR	I/O	**PARITY :** This indicates that all PCI agents require parity generation.
PCICLK	I/O	**PCI CLOCK:** This pin provides timing for all transactions on the PCI bus.
PCIRST#	O	**PCI RESET:** When asserted, this pin resets all PCI devices.
PERR#	I/O	**PARITY ERROR#:** This signal indicates a data parity error. It may be pulsed active by any agent that detects an error condition.
PLOCK#	I	**PLOCK#:** This signal allows the master to lock the PCI bus and the arbiter does not grant the PCI bus to a new master until this signal has been deasserted.
REQ[3:0]#	I	**PCI REQUEST [3:0]#:** This signal indicates to the arbiter that this agent requests use of the bus. This is a point-to-point signal. Every PCI bus master has its own REQ#.
STOP#	I/O	**STOP#:** This signal facilitates either master-abort or target-abort cycles.
TRDY#	I/O	**TARGET READY#:** This indicates the ability of the target device to complete the current data phase of the bus transaction. During a read phase, TRDY# indicates that the valid data is present. During a write phase, it indicates that the device is ready to accept data.

2.5 Power Management Controller Interface

Pin Name	Type	Description
EXTACT0	I	**EXTERNAL ACTIVITY 0:** This pin indicates that there is a current external activity. This input can be unmasked to trigger a primary (P/A) or secondary activity (S/A). Refer to Registers PAM2 and SAM for more information. **NOTE:** EXTACT0 cannot be unmasked to wakeup from Suspend mode. Refer to Register WMC for more information.
GPIO0/ LED0	I/O	**GENERAL PURPOSE I/O 0:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [1:0]. **LED 0:** LED indicator output 0.
GPIO1/ LED1	I/O	**GENERAL PURPOSE I/O 1:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bits [3:2]. Refer toSection 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **LED 1:** LED indicator output 1.
GPIO2/ DDMARETRY/ DPSLP_IRQPA	I/O	**GENERAL PURPOSE I/O 2:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [5:4]. Refer toSection 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **DDMARETRY:** During normal operation this input to V1-LS is used to define the Distributed DMA function between V1-LS and V3-LS devices. When high, it indicates that the V3-LS device is requesting V1-LS for ownership of the PCI bus. **DEEP SLEEP IRQ PRIMARY ACTIVITY:** Before entering Deep Sleep mode, the software will set this signal to DPSLP_IRQPA. During Deep Sleep mode, this pin acts as a wake-up source due to P/A on IRQs from V3-LS.
GPIO3/ SUPRESS_RESUME	I/O	**GENERAL PURPOSE I/O 3:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [7:6]. Refer toSection 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **SUPRESS RESUME:** This pin prevents a wake-up from Suspend mode regardless of the wake-up source. For example, when the system battery is running low, this pin will prevent the battery from further drain by not resuming from Suspend mode.

2.5 Power Management Controller Interface *(cont.)*

Pin Name	Type	Description
GPIO4 SUSPA#	I/O	**GENERAL PURPOSE I/O 4:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [9:8]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **SUSPEND ACKNOWLEDGE#:** This input from the Cyrix® 6x86 CPU indicates a suspend acknowledge state.
GPIO5 /THERM	I/O	**GENERAL PURPOSE I/O 5:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [11:10]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **THERMAL SENSOR INPUT:** This input allows an external thermal sensor to feed thermal information back to the thermal throttler to regulate the control of heat generated by the CPU.
LED0	O	See GPIO0 and PC3.
LED1	O	See GPIO1 and PC4.
PC[2:0]	O	**POWER CONTROL [2:0]:** This output provides individual power control for any system component. PC[2:0] will default to high on power-up reset.
PC3/ LED0	O	**POWER CONTROL 3:** This output provides individual power control for any system component. PC3 will default to low on power-up reset. Refer to Section 4.4.60 on page 1-193 for additional details on the PC multiplexing scheme. **LED 0:** LED indicator output 0.
PC4/ LED1	O	**POWER CONTROL 4:** This output provides individual power control for any system component. PC4 will default to low on power-up reset. Refer to Section 4.4.60 on page 1-193 for additional details on the PC multiplexing scheme. **LED 1:** LED indicator output 1.
PC5	O	**POWER CONTROL 5:** This output provides individual power control for any system component. PC5 will default to low on power-up reset.
RING	I	**RING:** This input provides for a 'wake-up' call from a modem. RING can be unmasked to trigger a P/A (see Register PAM2). The number of RING to wake up from the Suspend mode is programmable in Register RCC. **Note:** RING cannot be unmasked to trigger a SMI.

2.5 Power Management Controller Interface *(cont.)*

Pin Name	Type	Description
SUSPA#	I	See GPIO1.
SWTCH	I	**SWITCH:** This input is used for power management functions and can be unmasked to trigger a P/A or a SMI. The wake mask of SWTCH is default-enabled. See Section 3.2.9.10 on page 1-76 for more details.
THERM	I	See GPIO5.
WAKE[1:0]	I	**WAKE [1:0]:** These pins request V1-LS to wake up or "resume" operation if the system was previously in Suspend mode. See Section 3.2.9.10 on page 1-76 for more details.

2.6 V1-LS / V2-LS Interface

Pin Name	Type	Description
ADOE#	O	**AD BUS OUTPUT ENABLE#:** When this signal is active V2-LS drives the PCI AD bus AD[31:0].
ADPAR_ODD	I	**ODD AD BUS PARITY:** This pin is an input from V2-LS to indicate odd PCI AD Bus parity.
ADPAR_EVEN	I	**EVEN AD BUS PARITY:** This pin is an input from V2-LS to indicate even PCI AD Bus parity.
BD[7:0]	I/O	**BURST DATA BUS [7:0]:** This 8-bit bus carries different information during various phases between V1-LS and V2-LS.
BDCTL[2:0]	O	**BUFFER DATA CONTROL [2:0]:** This pin indicates a data path control signal to V2-LS.
DECBUF	O	**DECREMENT WRITE BUFFER COUNTER:** This output is used to decrease the pointer on the eight-level write buffer.
INCBUF	O	**INCREMENT WRITE BUFFER COUNTER:** This output is used to increase the pointer on the eight-level write buffer.
PCIMSTR#	O	**PCI MASTER#:** This pin indicates to V2-LS that V1-LS is responding to a PCI master cycle.
V2CLK	I/O	**V2 CLOCK:** This pin is a clock for the interface between V1-LS and V2-LS.

2.7 V1-LS / V3-LS Interface

Pin Name	Type	Description
BSER1TO3	O	**SERIAL BUS:** This pin is the serial bus interface from V1-LS to V3-LS.
BSER3TO1	I	**SERIAL BUS:** This pin is the serial bus interface from V3-LS to V1-LS.
BSERCLKV3	O	**CLOCK:** This pin indicates a clock for the serial interface between V1-LS and V3-LS.
DDMARETRY		See Section 2.5 on page 1-32.

2.8 Reset and Clock Interface

Pin Name	Type	Description
32KHZCK	I	**CLOCK:** This pin indicates the clock source used for DRAM Refresh Controller and power management functions.
CLKIN	I	**CLOCK:** This pin indicates an input clock source to the CPU clock. CMOS level 50/50 duty cycle is recommended.
PWRGOOD	I	**POWER GOOD INPUT:** This input causes a complete system reset. It is driven by the PWRGOOD signal from the power supply or a reset switch. When transitioning from low to high on power-up, PWR-GOOD indicates that the external VCC is stable.
RCRST#	I	**RC RESET#:** This input is used to reset V1-LS' power management controller upon initial system power-up. It should have a pull-up resistor tied to the same power source as V1-LS' VCC-5V.
RSTDRV	O	**AT BUS RESET OUTPUT:** This output provides a system reset.

2.9 Power and Ground

Pin Name	Type	Description
VCC5-V	PWR	**VCC5-V:** These are I/O power pins for VCC-5V power plane.
VCC CORE	PWR	**VCC CORE:** These are I/O power pins for VCC CORE power plane.
VCCCPU	PWR	**VCCCPU:** These are I/O power pins for VCCCPU power plane.
VCCDRAM	PWR	**VCCDRAM:** These are I/O power pins for VCCDRAM power plane.
VCCPCI	PWR	**VCCPCI:** These are I/O power pins for VCCPCI power plane.
VSS CORE	GND	**VSSC:** These are I/O ground pins.
VSSIO	GND	**VSSIO:** These are I/O ground pins.

3. V1-LS FUNCTIONAL DESCRIPTION

This chapter provides functional information and design guidelines on chip resources and interfaces of the V1-LS device. To fully understand the functionality of the V1-LS device, it is important to become familiar with the programming model of the VESUVIUS-LS platform. The BIOS will access the V1-LS device through a 16-bit access on Port 24H (index port) and Port 26H (data port). While the V3-LS device has its own register set, it is accessed through an 8-bit access on Port 24H and 26H. Registers discussed in this chapter are referred to by their abbreviated name. For a complete list of register names and their abbreviated names, refer toSection 4.1 on page 1-78.

3.1 Power Plane Structure

The VESUVIUS-LS platform offers a flexible power plane structure to support a wide variety of system configurations. The V1-LS device has five independent power planes:

- VCC CORE
- VCCCPU
- VCCDRAM
- VCCPCI
- VCC-5V

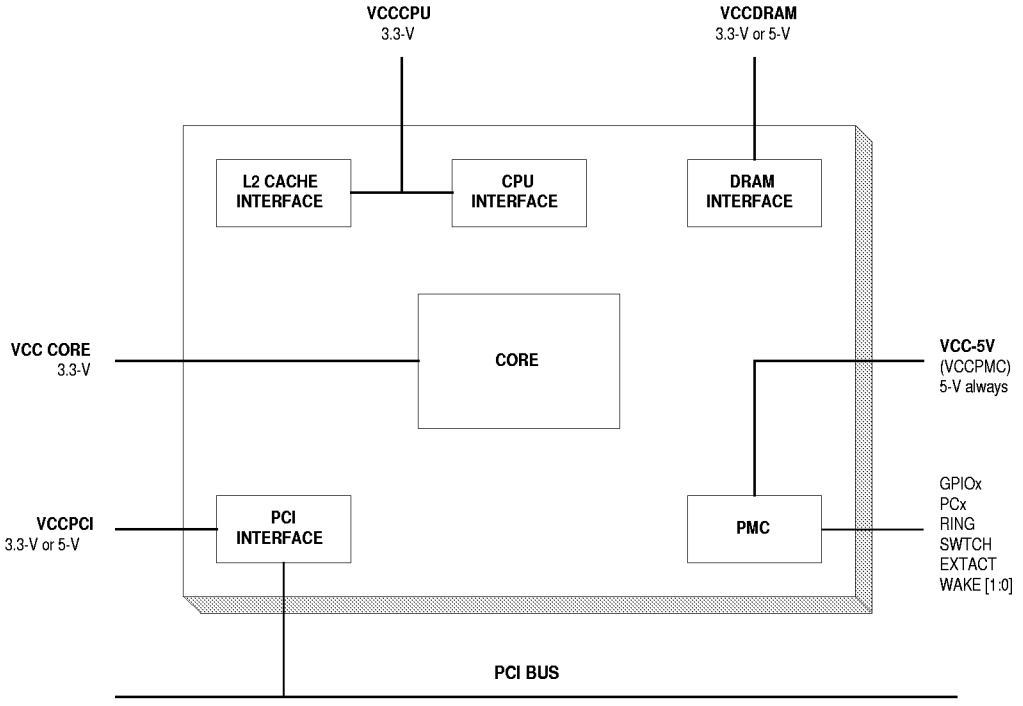


Figure 3-1. Power Plane Block Diagram

The V2-LS device has four power planes:

- VCC CORE
- VCCCPU
- VCCDRAM
- VCCPCI

Table 3-1 outlines the typical power plane usage for V1-LS and V2-LS**Power On Sequence:** If the I/O power plane is 5-V, then the 5-V power plane should be turned on first, followed by the 3.3-V planes. **Power Down Sequence:** 3.3-V planes should be turned off first, followed by the 5-V planes.

Table 3-1. Typical Power Plane Usage

Power Plane	V1-LS[1]	V2-LS
VCC CORE	always set to 3.3-V	always set to 3.3-V
VCCCPU	always set to 3.3-V	always set to 3.3-V
VCCDRAM	can be selected as 3.3-V or 5-V[2]	can be selected as 3.3-V or 5-V[1]
VCCPCI	can be selected as 3.3-V or 5-V[2]	can be selected as 3.3-V or 5-V[1]
VCC-5V	always set to 5-V	not applicable

1) During 5-V Suspend (STR) mode, though all V1-LS power planes must be kept on, all signals will be properly 'leakage-controlled.' Peripherals can be independently powered off during STR.

2) Example: Support for either 3.3-V or 5-V DRAM can be enabled simply by changing the setting for VCCDRAM.

3.1.1 Suspend-to-Disk (STD) or 0-V Suspend Mode

Figure 3-2 shows the typical design of a STD-capable portable system which can be woken up by a modem ring or RTC alarm (IRQ8). During STD all power planes of V1-LS, V2-LS, and V3-LS devices are powered off. Therefore, the RS232_RI# output from the PCMCIA controller and RS232 port or the IRQ8 from RTC are connected to an external microcontroller—typically H8 or 8051SL— through glue logic.

Figure 3-2 assumes that rising edge signals (IRQ8 and RI) are used so that the microcontroller can stay in a low-power state (around 1 µA) and wake up through its 'edge detect wakeup' feature. Both 3V_SUSP and 5V_SUSP are off, implying that RCRST# and PWRGOOD should be low. Refer to Section 3.2.9.4 on page 1-65 for a detailed discussion of the STD mode.

3.1.2 Suspend-To-RAM (STR) or 5-V/3.3-V-Suspend Mode

In the STR mode all V1-LS power planes must be kept on. It is important to note that while PC and GPIO signals are also driven, all other signals are properly leakage-controlled and devices like PCI VGA and PCI CardBus/PCMCIA controller can still be kept alive. Therefore, PCIRST# input of these PCI devices should not be asserted. This can be done by gating PCIRST# with a GPIO pin (set to high during Suspend mode) through an OR gate. On resume, the BIOS will toggle the GPIO pin back to low for normal operation. Refer to Section 3.2.9.4 on page 1-65for a detailed discussion of the STR mode.

NOTE: If used for GPIO functions, all GPIO signals should have an external pull-up or pull-down resistor. During the STR mode, RCRST# and PWRGOOD must be kept high.

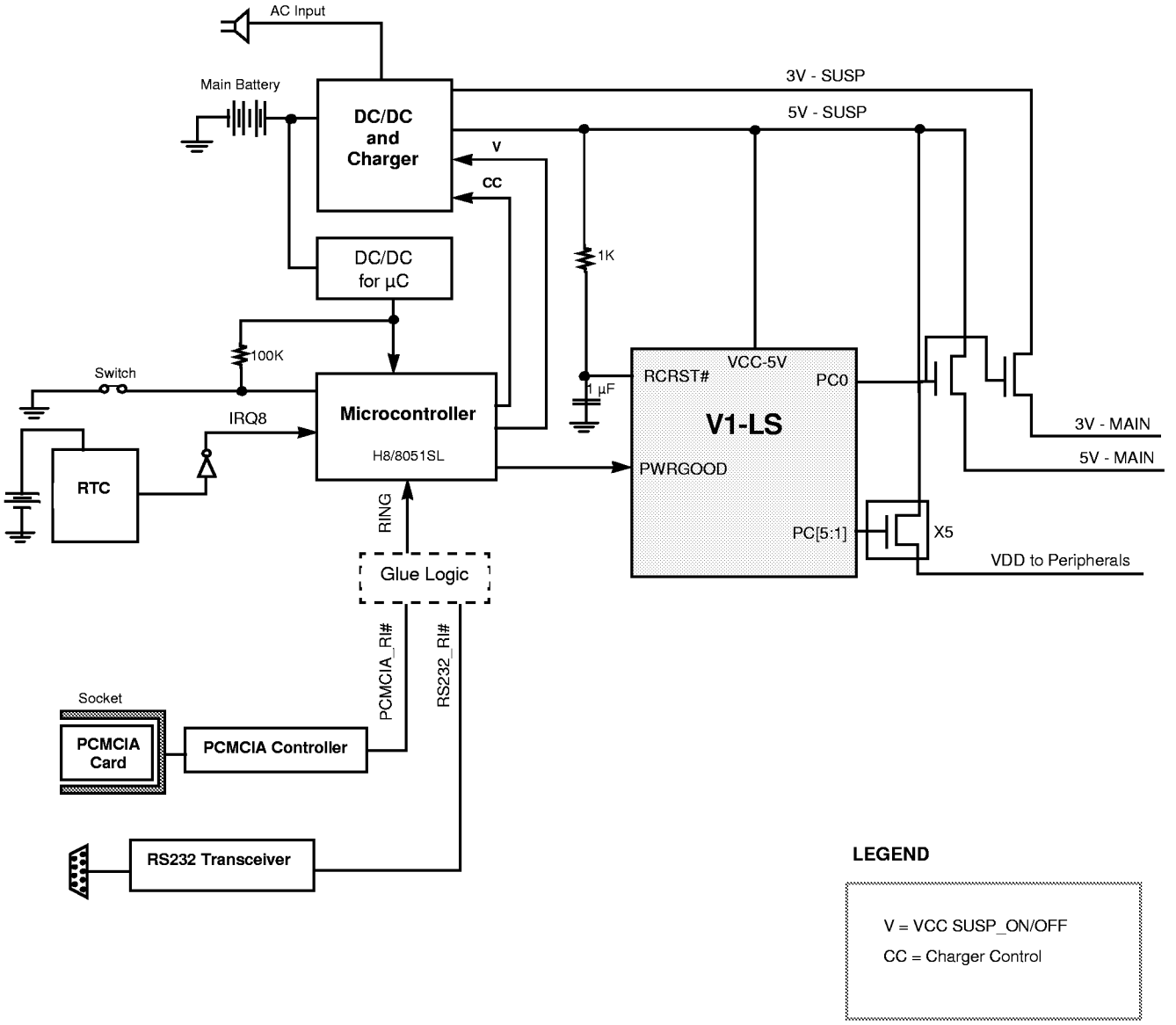


Figure 3-2. A Typical Portable Computer Design (With Zero-Volt Suspend)

3.2 Functional Blocks

The following functional blocks have been integrated into the V1-LS device. Refer to Figure 3-3 for a functional block diagram of the V1-LS device. This diagram also includes an alphabetical listing of pins in each functional group.

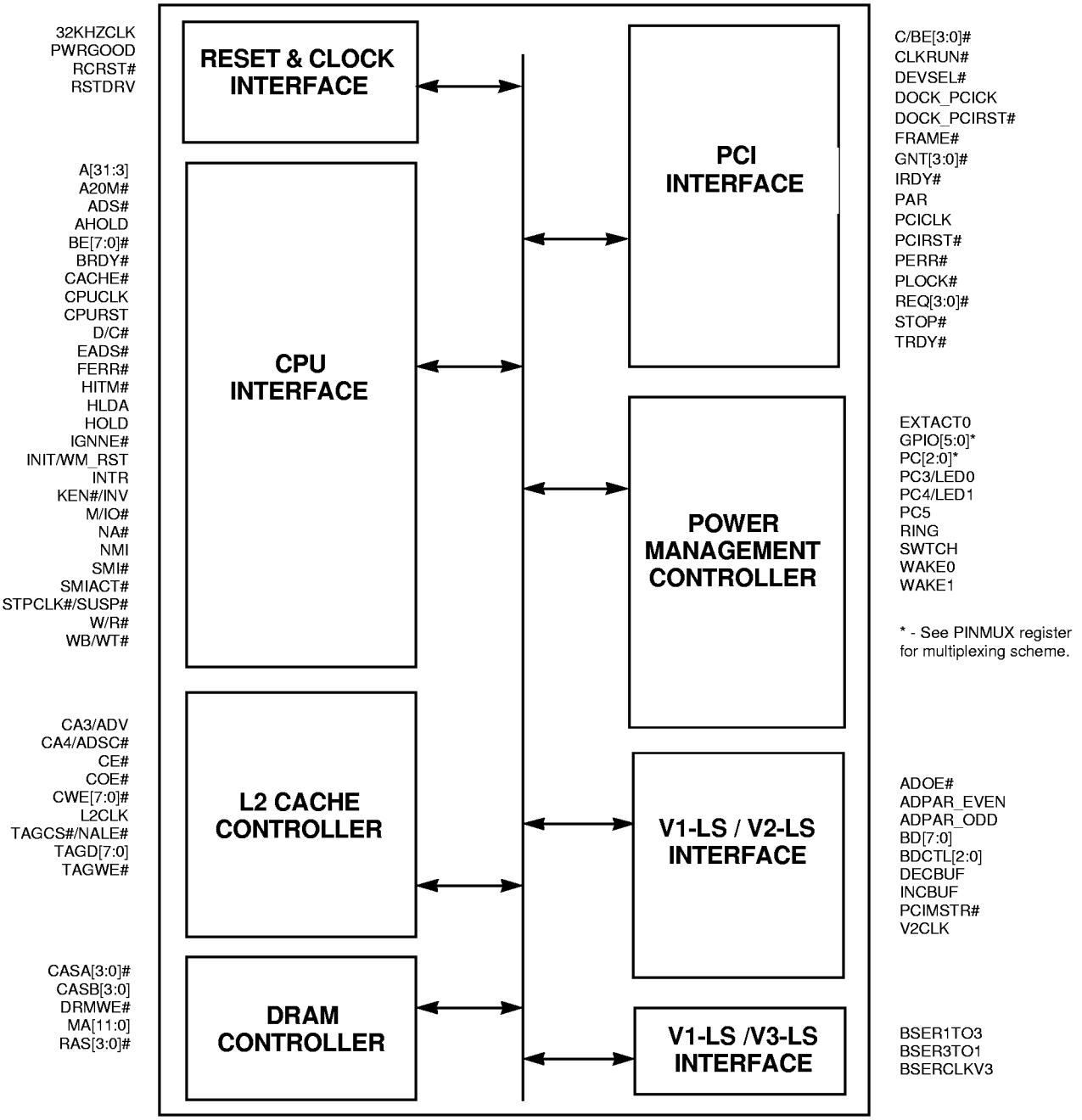


Figure 3-3. V1-LS Functional Block Diagram

3.2.1 Clock Interface

Refer to Figure 3-4 for a distribution of clocks in the V1-LS device. The CLKIN signal, an input to the V1-LS, is the clock source for the CPU/L2/DRAM/PCI subsystem. Since the CLKIN signal is a part of the VCC-5V plane, the PMC and power control interface voltage has a direct correlation with the choice of clock synthesizer or oscillator. Since the system logic of V1-LS and V2-LS uses both the rising and falling edges of the clock (derived from CLKIN), it is important to keep the CLKIN as close as possible to the 50/50 duty cycle. Therefore, CLKIN should use CMOS-level input with the threshold at VCC-5V and the synthesizer should generate an output with a worst case of 45/55 to 55/45 duty cycle, CMOS-level clock output.

The V1-LS also requires a 32-KHz input which is typically referred to as the power management clock. The 32KHZCLK is used as a debouncing clock for power management input signals like SWTCH, WAKE [1:0], EXTACT0, and RING. It is also used as a DRAM refresh clock source and as power management timers clock sources for Device Timers [5:0], Doze/Sleep/Suspend mode timers etc. Note that, the 32KHZCLK is usually connected to various devices like PCI VGA and RTC that can be independently powered on or off. Consequently, leakage could result if the 32KHz clock is not properly isolated between these devices. Since the 32KHz clock is used for power management functions, it also belongs to the VCC-5V plane and is typically set at 5-V.

Derived from CLKIN, the CPUCLK, L2CLK, and V2CLK are synchronous signals that are running at the same frequency. These signals can be stopped or restarted under certain conditions. The CPUCLK can be stopped in the Sleep, MoreStop, or Deep-Sleep mode and restarted when a primary activity (P/A) is detected. The L2CLK will stop when L2 is idle or when STPCLK# is asserted and there is no PCI Master cycle (snooping). All three clocks belong to the VCCCPU plane to minimize any potential clock skew which may otherwise result from the differences in the voltage of output buffers.

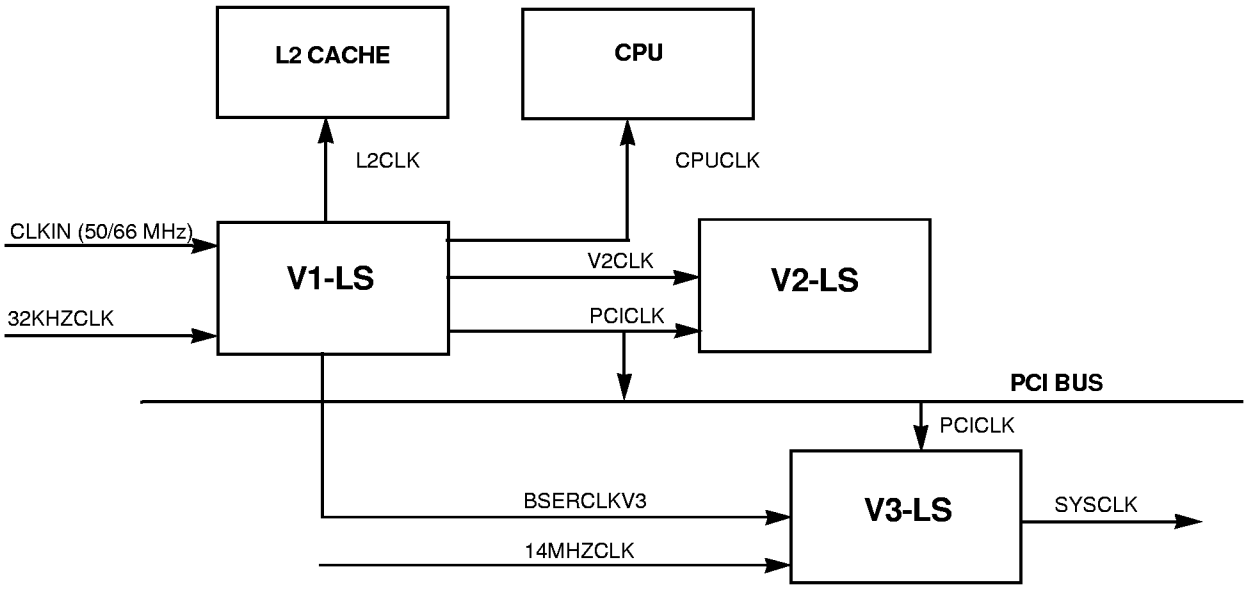


Figure 3-4. VESUVIUS-LS Clock Distribution

To ensure short rise and fall time, all three clocks use 24-mA output drivers. When laying out the printed circuit board, care must be taken to balance the trace length and loading to minimize the clock skew and clock distortion.

The PCICLK is also derived from CLKIN and runs at half the frequency of the CPUCLK. Therefore, both CPU/L2 and PCI subsystems are also running synchronously. The PCICLK belongs to the VCCPCI plane and is programmable as 3.3-V or 5-V. Clock buffering can be added if the buffer chip has a worst-case delay of 2 ns and a maximum difference of 0.5 ns among all buffered outputs. The VESUVIUS-LS also offers a proprietary PCI power management feature: If PCI idle cycles are detected for a predefined period of time, the PCICLK will be scaled (up to divided by 256) and substantially reduce the power of an idle PCI bus.

The BSERCLKV3 is the clock for BSER1TO3 and BSER3TO1 operation. The BSER3TO1 is a serialized signalling pin from V3-LS to V1-LS, indicating activities detected in V3-LS. The activities include, SMI events, P/A, secondary activities (S/A) resulting from IRQx, and V3-LS REQ#. The BSER1TO3 carries other system information from V1-LS to V3-LS, including V3-LS GNT# and IRQ13. The IRQ13 signal is also embedded because the coprocessor interface is located in V1-LS while the 8259s are located in V3-LS. All three burst signalling pins belong to the VCC-5V plane and are typically 5-V interface. In the Fully-On, Doze and Sleep mode, BSERCLKV3 will be running at the same frequency as the PCICLK to ensure minimal latency on SMI and IRQ events. However, during the Deep-Sleep mode, all clock sources (except 32KHz) are powered off and BSERCLKV3 will also stop. V3-LS will trigger V1-LS to restart the clock with a special protocol on the GPIO2 signal.

3.2.2 Reset Interface

The V1-LS device has two separate reset inputs: RCRST# and PWRGOOD. The RCRST# is the master reset of V1-LS and will reset all registers in V1-LS, V2-LS and V3-LS devices. Figure 3-5 illustrates the distribution of reset signals on VESUVIUS-LS. In a typical notebook design, the RCRST# signal should be connected to a resistor pulled up to the VCC-5V plane and a capacitor connected to ground. The time constant should be between 50 ms and 150 ms (typical value is 22 K to 68 K and 2.2 µF). If the system requires a hardware reset input, the RCRST# signal should be used.

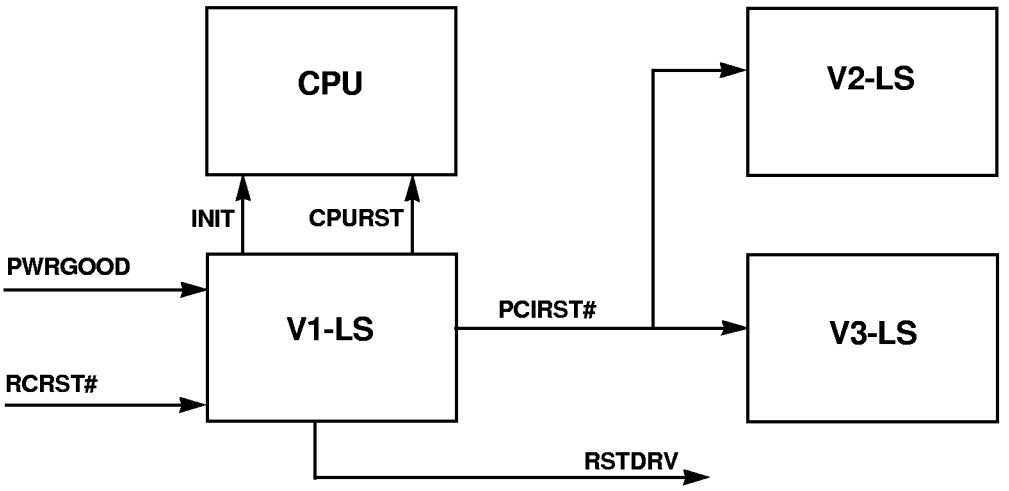


Figure 3-5. Distribution of Reset Signals

The PWRGOOD signal indicates that at least the VCC CORE and VCC-5V planes to V1-LS are powered on and in a stable condition. A low state on the PWRGOOD while the RCRST# is high and vice-versa, will trigger a reset pulse on CPURST, PCIRST#, and RSTDRV signals with a minimum pulse-width of 128 ms. For PC/AT compatibility, it is recommended that on power up, PWRGOOD should be asserted within 150 ms to 500 ms after all VCC planes have reached their regulation range. Depending on the power supply and DC/DC converter design, it may need some R, C time constant to delay the assertion of the PWRGOOD signal.

The INIT/WM_RST signal is generated under the following circumstances:

- A CPU shutdown special cycle is detected
- Keyboard reset command is written to Port 64H
- Fast reset command is written to Port 92H

3.2.3 Power-On Configuration

The VESUVIUS-LS platform incorporates a V1_POC register (V1 Power-On Register) to define any fundamental system configuration variables that must be set by hardware options. Bit [2:0] are defined as miscellaneous configuration bits (MISC_CFG [2:0]) that may be used in conjunction with the BIOS to control system variables or to detect system configurations (e.g. CPU type, CPUCLK clock speed, SRAM type, etc.) and are design-specific. Bit [5:3] are defined as Clock Skew Adjust [2:0] control bits. These bits allow the fine-tuning of internal-to-external clock skew to compensate for clock skews introduced by system design.

Register V1_POC is loaded by sampling the present value of MA[11:0] on RCRST# rising edge. In order to select the desired options for a particular system, each MA[11:0] pin should have either a pull-up or pull-down resistor connected. From the point of powering up the VESUVIUS-LS until the RCRST# rising edge, all MA lines will be tristated, therefore a weak pull-up or pull-down can easily set each MA pin to the intended high or low value. 100-K resistors are recommended. Once set, this register becomes read-only and will be sampled again only on the next RCRST# rising edge.

NOTE: Every MA pin must have either a pull-up or pull-down resistor. Any unused or reserved MA pins should be pulled-up or down according to the suggested default shown in the V1_POC register description. Since bit [11:6] are reserved, MA[11:6] should be pulled-down by 100-K resistors. Any unused MISC_CFG [2:0] should also be pulled down by a 100-K resistor.

3.2.4 CPU Interface

The VESUVIUS-LS fully supports Pentium®, K5 and 6x86 processors. It incorporates high-performance features including full pipelining support, eight-level deep write-buffers for both DRAM and PCI cycles, and read reordering on DRAM and PCI cycles.

3.2.4.1 Pentium Processor Toggle Burst Sequence and AMD/Cyrix Linear Burst Sequence

The VESUVIUS-LS supports both toggle burst sequence (Pentium processor) and linear burst sequence (K5 and 6x86 processors). This allows maximum performance for each processor in its corresponding operating frequency. The burst sequence is programmable by Register PROC bit 3, LINEARBURST.

3.2.4.2 Full CPU Address Pipelining Support (NA#)

The VESUVIUS-LS provides full address pipelining support. The pipelining option is programmable by Register PROC bit 2, PIPELINEEN.

If asynchronous data SRAM is used for L2, an external 16-bit address latch is required to latch the CPU address. Refer to Figure 3-6, and Figure 3-9 for more details.

Table 3-2. Toggle and Linear Burst Sequence

Burst Cycle First Address A[4:3]	Pentium Toggle Burst Sequence A[4:3]	K5 or 6x86 Linear Burst Sequence A[4:3]
00	00-01-10-11	00-01-10-11
01	01-00-11-10	01-10-11-00
10	10-11-00-01	10-11-00-01
11	11-10-01-00	11-00-01-10

3.2.4.3 High-Performance Eight-level Deep Write-Buffers With Read Reordering Support

The VESUVIUS-LS supports eight-level memory write-buffers. The write-buffers support (2-1-1-1) burst writes for CPU-to-DRAM and zero wait state CPU-to-PCI cycle at bus frequencies up to 66 MHz, vastly enhancing L2 write-miss and CPU-to-PCI performance. Since the write-buffers are deep enough to hold two back-to-back burst-write cycles, most L2 write-miss cycles complete in (2-1-1-1). Multiple CPU burst writes occurring in a short period of time are unlikely in a system with level-1 write-back CPU.

The VESUVIUS-LS also supports read reordering. Read reordering ensures that the CPU will not unnecessarily wait for the write-buffer to flush its content to the DRAM or PCI bus, resulting in loss of performance. In the VESUVIUS-LS platform, memory-reads (while the write-buffer is not empty) take priority and can interrupt the buffer dump to process the memory-read first. However, read reordering does not occur if the address read is still outstanding within the write buffer.

3.2.4.4 Cacheable Regions

The VESUVIUS-LS allows caching system memory which is directly controlled by the V1-LS DRAM controller into level-1 and level-2 cache. The DRAM banks and sizes programmed into the DRAM control registers imply the Top-of-Memory.

NOTE: For Revision AA and earlier revisions of VESUVIUS-LS silicon, the cacheability for L1 was limited by the memory size of the L2 cache. This limitation has been removed for silicon revision BB and beyond. By default, all memory accesses directed to on-board memory are cacheable by L1 cache.

The memory will be non-cacheable in the L1 cache:

- If the address is not within the local DRAM area: 00000000H to Top-Of-Memory.
- If the address is within one of the four programmable regions, PR [3:0], which is marked non-cacheable.
- If Register PROC bit 0, KENEN, is set to '0'.
- If during SMM, the address is within SMRAM and Register SMMC bit 1, KDISSMMRAM is set to '1.' The SMRAM address is programmable in 32-Kbyte granularity from 000D0000H-000EFFFFH by Register SMMC bit [11:4].

The VESUVIUS-LS system controller will always mark the lowest 4-Kbyte (00000000H-00000FFFH) region as non-cacheable for future proprietary features. Therefore, the lowest 64-Kbyte segment should not be used for L2 cache initialization.

The memory will be non-cacheable in the L2 cache:

- If the address is not within the local DRAM area: 00000000H to Top-Of-Memory.
- If the address is within one of the four programmable regions, PR [3:0], which is marked non-cacheable.
- If Register PROC (index 119H) bit 0, KENEN, is set to '0'.
- If any SMRAM within 000D0000H-000EFFFFH will not be cached in L2. During SMM, and if the address is within SMRAM, L2 will not respond to the cycle if it is L2 read-hit or miss. However, any write to L2 will be invalidated.
- If Register L2C (index 400H) bit 0, L2EN is set to '0'.

The memory address will be marked as write-through in L1 cache:

- If the address is within one of the four programmable regions, PR [3:0], which is marked write-through.
- If Register PROC bit 1, WTALWAYS# is set to '0'.
- If during SMM mode, i.e. SMIACT# is set to '0'.
- If the address is in the shadowed ROM range 000C0000H-000FFFFFH.

3.2.4.5 Special Programmable Regions

To allow greater system flexibility, the VESUVIUS-LS has four programmable regions: Register PR [3:0], that can be individually programmed as non-cacheable or treated as L1 write-through. The mode of each region is programmable in Register PRC. In a typical system configuration, these regions are not required since standard non-cacheable regions — non-shadowed ROM regions between 000C0000H-000FFFFFH — are automatically non-cached. The region sizes are programmable to 32 Kbytes, 64 Kbytes, 128 Kbytes, 256 Kbytes, 512 Kbytes, or 1 Mbyte.

3.2.4.6 Invalidate Write-Protected, Shadowed ROM Region in L1 Cache

When there is a write to a write-protected, shadowed ROM region (Register SHADWC, LMEMWRENn bit is set to '0') which has been cached in L1, that particular cache line must be invalidated in L1. To preserve coherency, the cached ROM region must be marked as write-through in L1 so that any write to it will become a CPU write cycle on the CPU bus. The VESUVIUS-LS will then invalidate the cached ROM line by asserting AHOLD (the VESUVIUS-LS drives out the same address) and then EADS# to the CPU.

To ensure L2 cache coherency, the L2 cache controller will not respond to any write to a write-protected, shadowed ROM region. For flash updating or flash disk operation, the corresponding LMEMWRENn bits in Register SHADWC should be set to '1' to enable a write to that region.

Snoop Filtering to Increase PCI Master Performance With L1 Cache

The VESUVIUS-LS provides a snoop filter (also known as snoop-line comparator) to compare the current memory address with the previous memory address, which will increase performance on PCI Master (V3-LS is also treated as PCI Master since it will generate REQ# for DMA/ISA Master cycle) operation with L1 cache. If the current memory address is in the same line as the previous one, snooping will be disabled and the DRAM cycle can be started earlier. Snooping is done only if the address is in the cacheable region.

3.2.4.7 STPCLK# and SUSP#/SUSPA# Support

The VESUVIUS-LS supports both Pentium/K5-style STPCLK# protocol and 6x86-style SUSP#/SUSPA# protocol. While operating in the STPCLK# protocol, the VESUVIUS-LS will look for the Stop Grant Bus Cycle (SGBC) to determine when the CPU has entered Stop Grant or Stop Clock state and decide

whether to keep the CPUCLK running or stop it to enter Stop Clock state. While operating in SUSP#/SUSPA# protocol, the VESUVIUS-LS will wait for SUSPA# from 6x86 to indicate that the CPU has entered a low-power state and the CPUCLK can then be kept running or stopped.

Since STPCLK# and SUSP# perform the same function, they share the same pin and do not require any multiplexing control. SUSPA# is multiplexed with GPIO1/LED1 pin functions and is selected by setting Register PINMUX bit [2:1] to '10'.

3.2.4.8 System Memory Map

Table 3-3. System Memory Map

Address Space	Address Range	Remarks
System DRAM	0 Mbyte – Top-of-Memory (max. 256 Mbyte)	
PCI Memory Space	Top-of-Memory – 256 Mbyte	
PCI Memory Space	256 – 479 Mbyte	10000000H – 1DF00000H
SMBASE	000D0000H–000EFFFFH (below 1 Mbyte)	See section on SMM
Upper ROM	(4 Gbytes – 32 Mbytes) to 4 Gbytes	

3.2.4.9 CPU Special Cycle

The V1-LS will always generate BRDY# to the processor when a special cycle is generated. However, for Shutdown and Halt special cycles, the V1-LS will broadcast these special cycles to the PCI bus and then generate a master-abort cycle to terminate the cycle.

3.2.5 Cache Controller

The V1-LS has an integrated L2 cache controller. It supports a direct-mapped, write-through scheme and can use 3.3-V asynchronous, synchronous burst or pipelined burst SRAM. Since V1-LS has an eight-level deep write-buffer, most L2 write-miss cycles will be completed in (2-1-1-1) up to 66 MHz, which provides the advantage of L2 write-back cache without the read-miss Dirty (castout) penalty. For systems that can only provide (3-1-1-1) L2 read-hit or write-hit at 60- or 66-Mhz with synchronous burst SRAM, the write-buffers will easily outperform them as long as the write-buffers are not full.

The L2 cache controller fully supports both non-pipelined and pipelined operations. For the pipelined mode, however, an external 16-bit latch is required when using asynchronous SRAM to latch the CPU address bus by NALE# signal from the V1-LS. Note that NALE# is multiplexed with TAGCS# signal.

3.2.5.1 L2 Cache Configurations

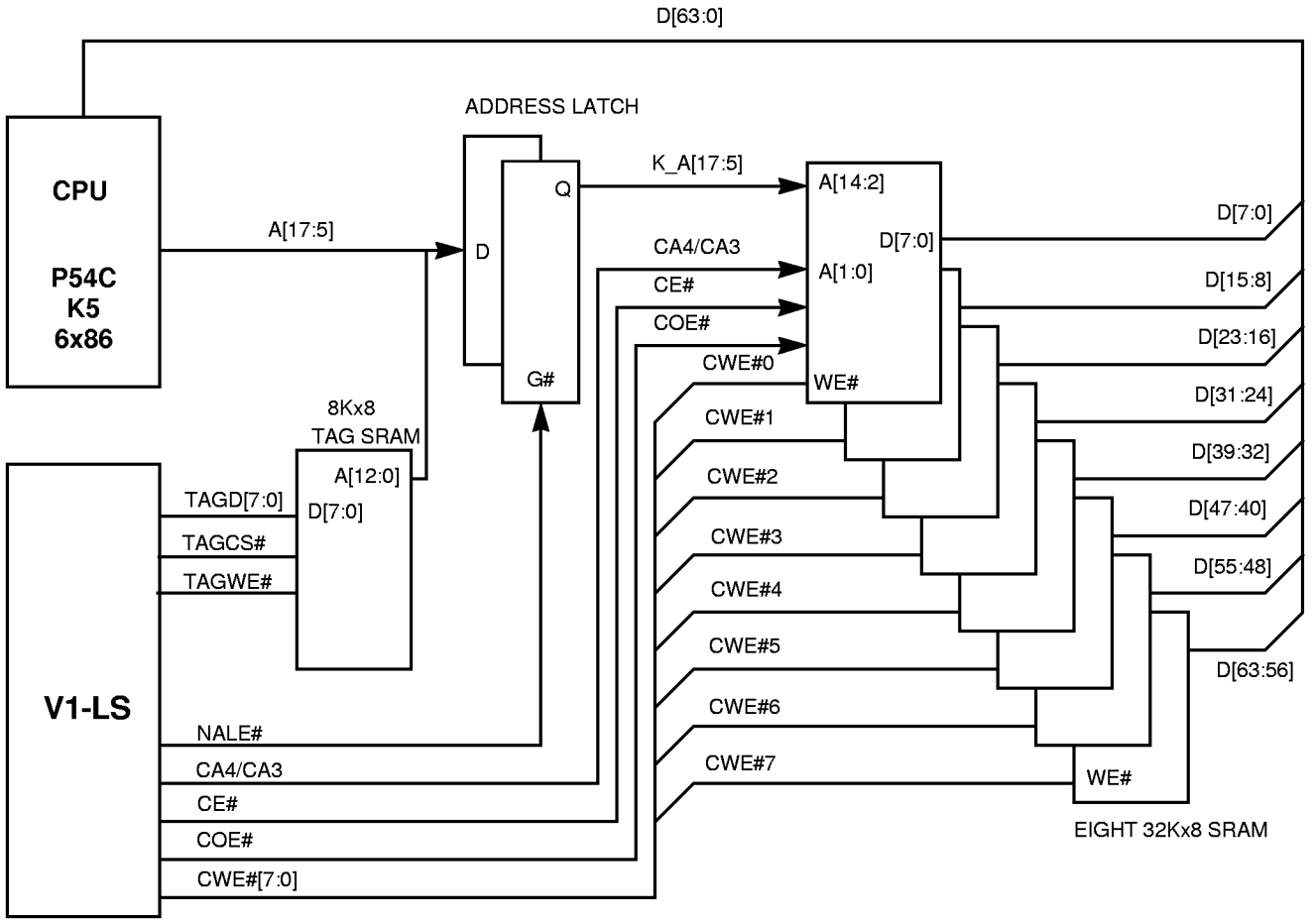
The VESUVIUS-LS supports both asynchronous and synchronous SRAM from 256 Kbyte, 512 Kbyte to 1 MByte size with 32-byte line size. All configurations are single-bank — with the exception of 512 Kbytes configuration — using two banks of 32 K x 36 synchronous SRAM (synchronous burst or pipelined burst). Refer to Table 3-4 for the cache configurations supported by V1-LS.

Table 3-4. Cache Configurations Supported

SRAM Size	SRAM Type[1]	# of Chips A-Bus Loading	D-Bus Loading	Address Latch Required for Pipeline	L2CLK Loading	L2 Cache Size	Figure
32K x 8	Async.	9	1	Yes	N.A.	256 Kbytes	Figure 3-6
32K x 16	Async.	5	1	Yes	N.A.	256 Kbytes	
32K x 36	Sync.	3	1	No	2	256 Kbytes	Figure 3-7
64K x 18	Sync.	5	1	No	4	512 Kbytes	
32K x 36	Sync.	5	2	No	4	512 Kbytes	Figure 3-8
128K x 8	Async.	9	1	Yes	N.A.	1 Mbyte	Figure 3-9

1 Sync. implies either synchronous burst or pipelined burst SRAM.

Note that for a robust system operation, there should be no more than two loads on CPU D-Bus data and five loads on CPU A-bus from the TAG SRAM and Data SRAM. If there are more than five address loads, an external buffer or latch will be required.



NOTE: TAGCS# and NALE# are multiplexed on a single pin. If NALE# function is used with asynchronous SRAM, the CS# of TAG SRAM should be connected to ground.

Figure 3-6. 256 Kbyte L2 Cache Using Eight 32 X 8 Asynchronous SRAM

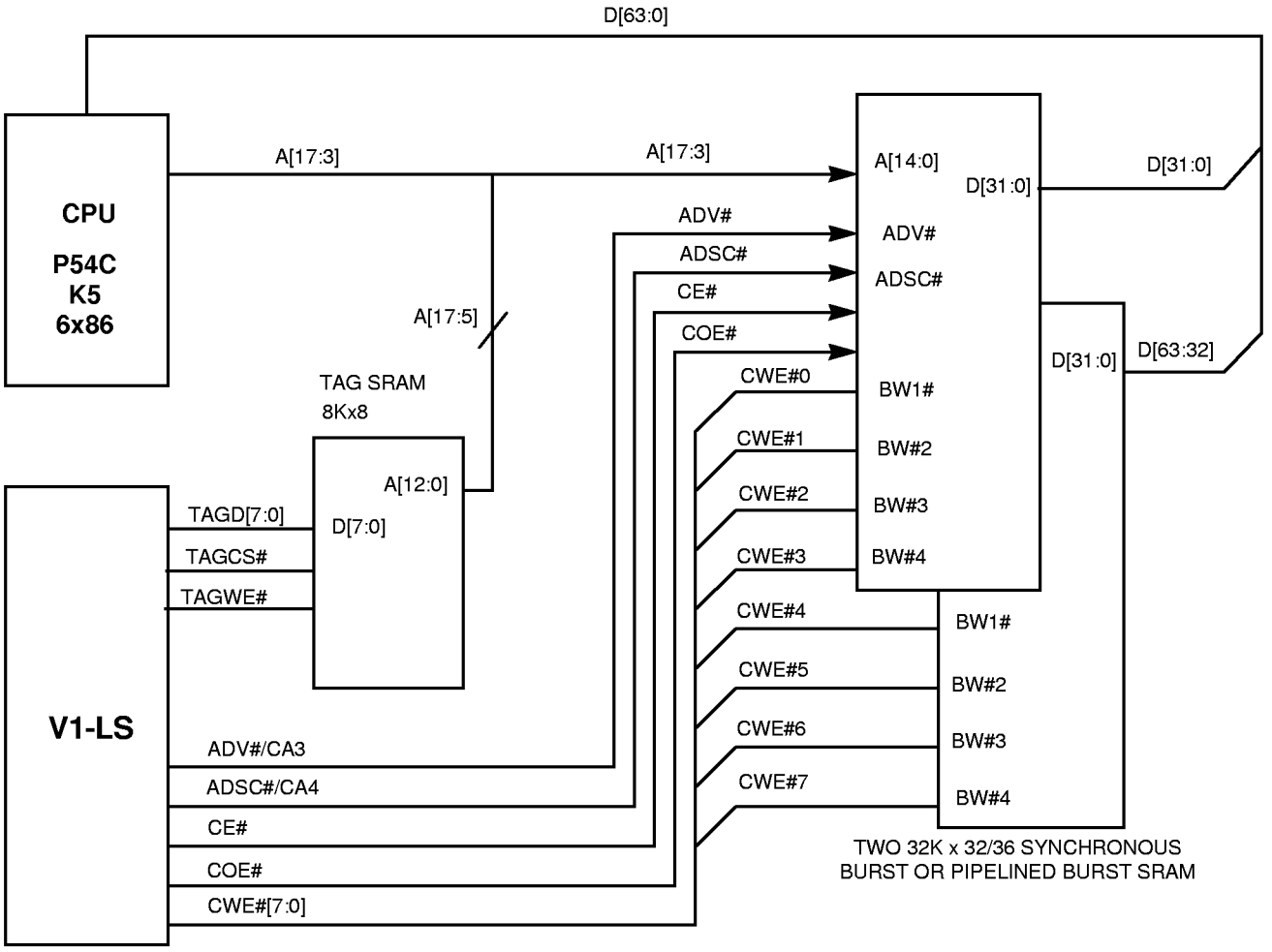


Figure 3-7. 256 Kbyte L2 Cache Using Two 32K X 32/36 Synchronous or Pipelined Burst SRAM

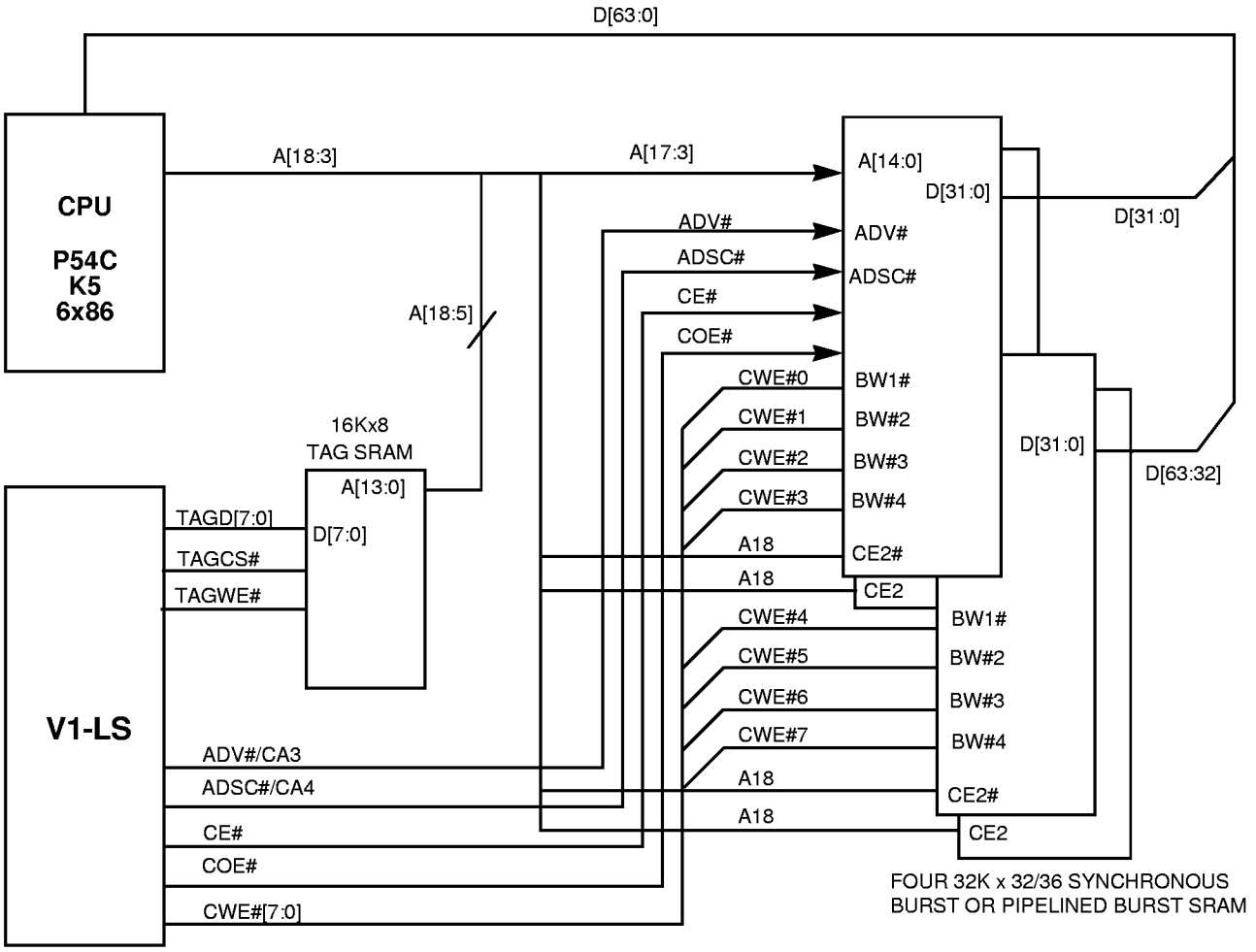
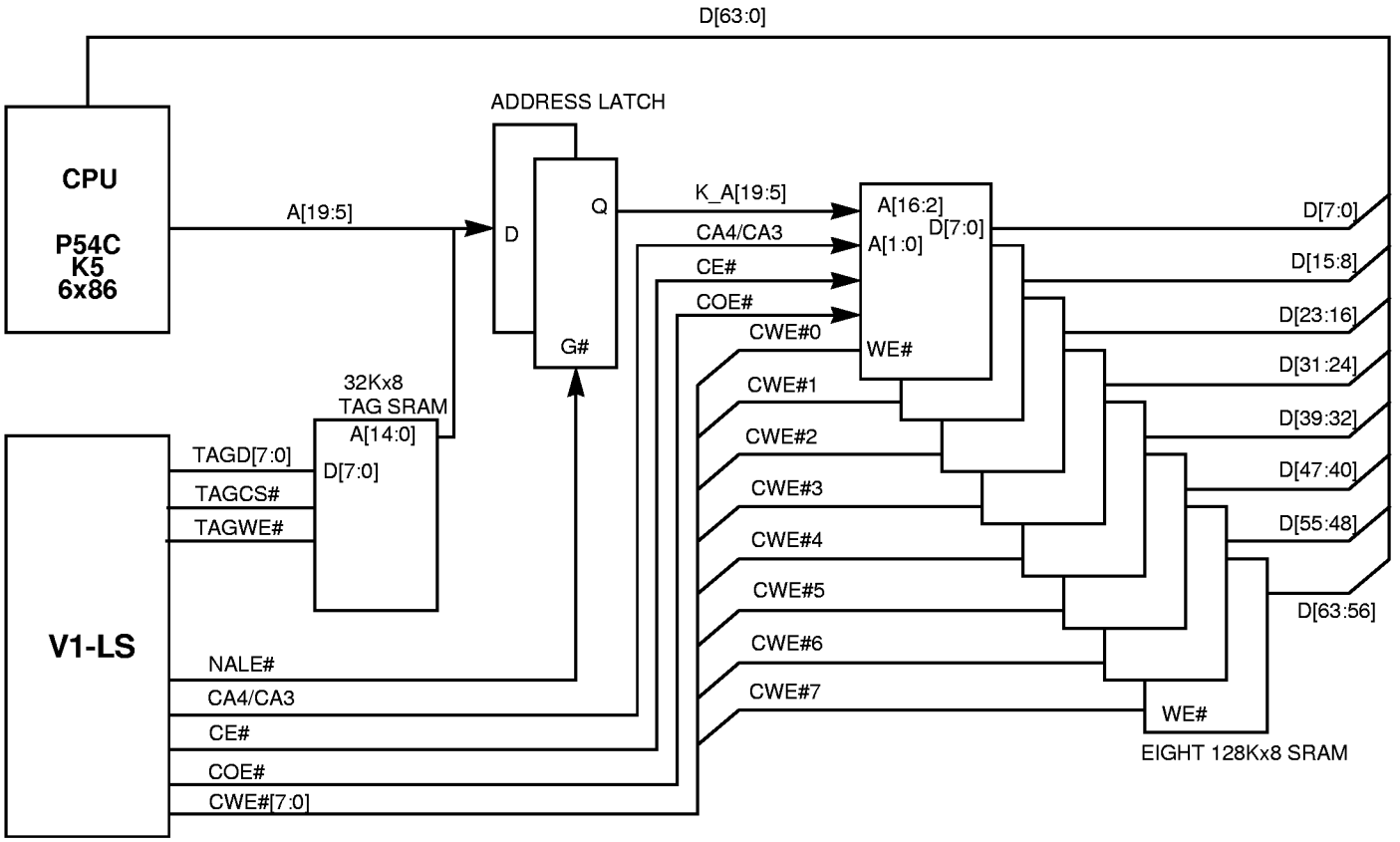


Figure 3-8. 512 Kbyte L2 Cache Using Four 32K X 32/36 Synchronous or Pipelined Burst SRAM



NOTE: TAGCS# and NALE# are multiplexed on a single pin. If NALE# function is used with asynchronous SRAM, the CS# of TAG SRAM should be connected to ground.

Figure 3-9. 1 Mbyte L2 Cache Using Eight 128K x 8 Asynchronous SRAM

3.2.5.2 TAG SRAM Size and Maximum Cacheable Region

The V1-LS has a a built-in TAG comparator which enables system designers to use low-cost Data SRAM as TAG RAM. This scheme enables 2-1-1-1 burst read or write up to 50 MHz. At 60- or 66-Mhz, 3-1-1-1 are supported.

Table 3-5. TAG SRAM Size and Maximum Cacheable Region

TAG RAM Size	L2 Cache Size	TAG SRAM Address Bus	TAG SRAM Data Bus	Maximum Cache-able Memory
8K x 8 or 32K x 8	256 Kbyte	A[17:5]	A[25:18]	64 Mbytes
16K x 8 or 32K x 8	512 Kbyte	A[18:5]	A[26:19]	128 Mbytes
32K x 8	1 Mbyte	A[19:5]	A[27:20]	256 Mbytes

3.2.5.3 TAG SRAM Speed Requirements and Hit/Miss Detection

Table 3-6 shows the TAG SRAM speed requirement for 2-x-x-x and 3-x-x-x burst cycles. It also shows the corresponding hit/miss detection point inside the VESUVIUS-LS to determine whether it is a L2 cache hit or miss cycle. The table is applicable to systems using either synchronous or asynchronous L2 data SRAM.

Table 3-6. TAG SRAM Speed Requirement and Hit/Miss Detection

Burst Performance (Lead Off Cycle)	Hit/Miss Detection Point	t_{AA} 50 MHz	t_{AA} 60 MHz	t_{AA} 66 MHz
(2-x-x-x)	t_{AA} + 9 ns	12 ns	5 ns	4 ns
(3-x-x-x)	t_{AA} + 9 ns	30 ns	15 ns	15 ns
(4-x-x-x)	t_{AA} + 9 ns	45 ns	30 ns	30 ns

3.2.5.4 Asynchronous Data SRAM Speed Requirements

Refer to Table 3-7 for the speed requirements of asynchronous data SRAM.

Table 3-7. Asynchronous Data SRAM Speed Requirement

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(3-2-2-2)	t_{AA} = Address access time	25 ns	15 ns	15 ns
	t_{OE} = OE# access time	8 ns	7 ns	7 ns
	t_{WP} = WE# pulse width	15 ns	12 ns	12 ns

NOTE: t_{AA} = TAG SRAM address access Time

3.2.5.5 Synchronous Burst Data SRAM Speed Requirements

Refer to Table 3-8 for the speed requirements of synchronous burst Data SRAM.

Table 3-8. Synchronous Burst Data SRAM Speed Requirements

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(x- 1-1-1)	t_{KQ} = Clock to output valid	10 ns	8 ns	7 ns
	t_{KC} = Clock cycle time	20 ns	16.7 ns	15 ns

3.2.5.6 Pipelined Burst Data SRAM Speed Requirement

Refer to Table 3-9 for the speed requirements of pipelined burst data SRAM.

Table 3-9. Pipelined Burst Data SRAM Speed Requirements

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(x- 1-1-1)	t_{KQ} = Clock to output valid	10 ns	8 ns	7 ns
	t_{KC} = Clock cycle time	20 ns	16.7 ns	15 ns

Pipelined SRAM supports zero wait-state writes (2-1-1-1). Thus the TAG speed must comply with this parameter.

3.2.5.7 TAGD[7:0] Mapping to CPU Address

Refer to Table 3-10 for the mapping of TAGD[7:0] to the CPU address. This information, though not required for typical system design, is provided for system debugging purposes.

Table 3-10. TAGD[7:0] Mapping to CPU Address

L2 Size	TAGD7	TAGD6	TAGD5	TAGD4	TAGD3	TAGD2	TAGD1	TAGD0
256 Kbytes	A25	A24	A23	A22	A21	A20	A19	A18
512 Kbytes	A26	A25	A24	A23	A22	A21	A20	A19
1 Mbyte	A27	A26	A25	A24	A23	A22	A21	A20

3.2.5.8 Invalidate or Write-Protect ROM Shadowed Region in L2 Cache

To ensure L2 cache coherency, the L2 cache controller will not:

- respond to any write to write-protected, shadowed ROM region.
- generate L2 cache hit cycle for reading shadowed ROM region by a non-CPU master .

In the above situations, the L2 cache controller will invalidate the cache line in L2.

For flash updating or flash disk operation, the corresponding LMEMWRENn bits in Register SHADWC should be set to '1' to enable a write to that region.

3.2.5.9 L2 Cache Coherency With SMM

While in SMM, the L2 cache controller will monitor the SMIACT# pin and disable normal L2 activity. All read cycles from the CPU, while in SMM, will be marked write-through and will be fetched from the DRAM. All write cycles from the CPU will be passed to the DRAM and the corresponding index (for example, as defined by A[17:5]) to the TAG will be invalidated. Note that read misses will NOT be updated in the L2 during SMM.

3.2.5.10 L2 Cache Timing Options

To optimize system performance with specific SRAM speed grade, the cache read and write timings may be different. Thus, VESUVIUS-LS provides two independent sets of programmable timing options for read and write cycles. The read/write lead-off cycle timing is programmable to 2, 3, or 4 clocks. The read/write follow-on (subsequent burst) cycle timing is programmable to 1, 2, or 3 clocks. For details, refer to Register L2T.

Note that if Register PROC bit 2, PIPELINEEN is set to '1', the lead-off becomes follow-through time on a back-to-back L2 read or write hit cycle. Example: 4-2-2-2 back-to-back burst-read will become 2-2-2-2.

3.2.5.11 L1, L2, DRAM Cache Coherency Policy on CPU and PCI Master Cycles

Refer to Table 3-11 and Table 3-12 for more information.

Table 3-11. CPU-Initiated Cycles to Non-SMRAM Region

CPU Read/Write Cycle	L2 Hit/Miss	Description
Read	Miss	Read data from DRAM and write it to L2 cache
Read	Hit	Read data from L2 cache
Write	Miss	Write data to DRAM
Write	Hit	Write data to DRAM and L2 cache

Table 3-12. PCI Master Cycles

PCI Master Cycles	L1 Cache Line	L2 Cache Line	L1 Cache Operation	L2 Cache Operation	DRAM Operations
Read	Hit, Clean	Miss	Invalidate		PCI Master read from DRAM
Read	Hit, Clean	Hit	Invalidate	Invalidate	PCI Master read from DRAM
Read	Hit, Dirty	Miss	Castout, Invalidate		PCI Master read from DRAM
Read	Hit, Dirty	Hit	Castout, Invalidate	Invalidate	PCI Master read from DRAM
Read	Miss	Miss			PCI Master read from DRAM
Read	Miss	Hit		Invalidate	PCI Master read from DRAM
Write	Hit, Clean	Miss	Invalidate		PCI Master write data to DRAM
Write	Hit, Clean	Hit	Invalidate	Invalidate	PCI Master write data to DRAM
Write	Hit, Dirty	Miss	Castout, Invalidate		PCI Master write data to DRAM

Table 3-12. PCI Master Cycles *(cont.)*

PCI Master Cycles	L1 Cache Line	L2 Cache Line	L1 Cache Operation	L2 Cache Operation	DRAM Operations
Write	Hit, Dirty	Hit	Castout, Invalidate	Invalidate	PCI Master write data to DRAM
Write	Miss	Miss			PCI Master write data to DRAM
Write	Miss	Hit		Invalidate	PCI Master write data to DRAM

3.2.5.12 L2 Cache Auto-Sizing Procedure

Refer to Appendix C. for an example pseudo-code sequence of an algorithm for auto-sizing the L2 cache.

3.2.5.13 Power Management for L2 Cache

L2CLK will be stopped on all bus idle cycles.

For TAG SRAM, the TAGCS# will be deasserted in the following instances to save power, regardless of whether the data SRAM is synchronous or asynchronous:

- During non-L2 CPU memory cycles
- STPCLK# asserted while HOLD not asserted
- Deep-Sleep mode

3.2.6 DRAM Controller

The V1-LS incorporates a flexible DRAM controller that supports up to four 64-bit DRAM banks or eight 32-bit banks. Each 64-bit DRAM bank can be split into two 32-bit banks for finer granularity system upgrade, allowing memory expansion through a standard JEDEC 88-pin 32-bit DRAM memory card.

Additionally, the DRAM controller supports mixed 64- and 32-bit DRAM operation, thus providing unsurpassed flexibility to support virtually all possible DRAM configurations:

- 4 x 64-bit banks
- 3 x 64-bit banks and 2 x 32-bit banks
- 2 x 64-bit banks and 4 x 32-bit banks
- 1 x 64-bit bank and 6 x 32-bit banks
- 8 x 32-bit banks

Refer to Figure 3-10 for a typical 32-bit/64-bit DRAM configuration in the VESUVIUS-LS. RAS[3:0]# are connected to RAS# of the corresponding 64-bit bank, or 32-bit bank pair. In a 64-bit bank operation, CASA[3:0]# should be connected to the CAS[3:0]# (which corresponds to MD[31:0]) while CASB[3:0]# to CAS[7:4]# (corresponds to MD[63:32]). In a 32-bit bank operation, CASA[3:0]# should be connected to the CAS[3:0]# of the *even* banks (banks 0, 2, 4, 6) and CASB[3:0]# to CAS[7:4]# of the *odd* banks (banks 1, 3, 5, 7).

In addition to mixed 32/64-bit, the DRAM controller also supports mixed EDO, Burst EDO, FPM DRAM, and mixed asymmetric or symmetric DRAM without any limitation.

3.2.6.1 Programming Model for 64-bit and 32-bit DRAM Bank Configuration

Register DCONF2 (index 20FH) controls how a particular DRAM bank is configured. Bit [11:8] individually controls whether Bank 0/1, Bank 2/3, Bank 4/5 and Bank 6/7 will operate as one 64-bit bank or two 32-bit banks. Bit [7:0] individually enables/disables bank 7 to 0 as 32-bit bank. However, whenever bit [11:8] are set to enable 64-bit bank operation, the corresponding bit-pair in bit [7:0] will be overridden and ignored. For example, if DCONF2 bit 8 is set to '1', then bit [1:0] will be ignored and Bank 0/1 will operate as one 64-bit bank.

Additionally, if a bank is selected as a 64-bit bank, only the information programmed into the corresponding *even* bank registers (Registers B0C, B2C, B4C or B6C) is used and the corresponding *odd* bank information (Registers B1C, B3C, B5C or B7C) will be ignored and the DRAM bank SIZE will automatically *double* the programmed value in the even bank register. For example, if DCONF2 bit 8 is set to '1', Bank 0/1 will operate as one 64-bit bank, if B0C bit [11:0] are programmed as '100' or 16 Mbyte, the 64-bit bank size will be 32 Mbyte and the DRAM type will be 4 M (deep) x 64-bit (wide).

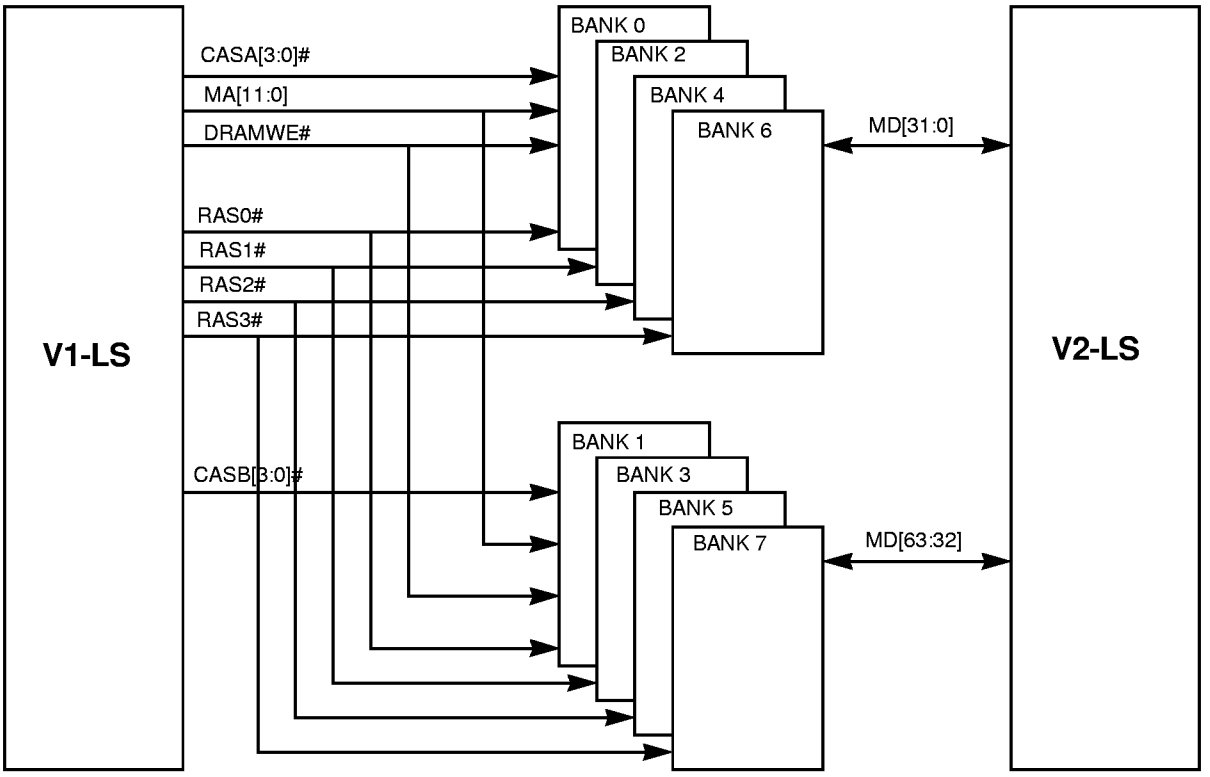


Figure 3-10. Typical 32-bit or 64-bit DRAM Configuration

3.2.6.2 Independently Programmable DRAM Timing Per 64-bit Bank or 32-bit Bank Pair

The V1-LS has a sophisticated programming model for DRAM timing control; it has an independent set of programmable DRAM timings per 64-bit bank or 32-bit bank pair (Registers B01TC, B23TC, B45TC and B67TC).

Programming the timing of a DRAM bank is an easy task; the BIOS simply needs to setup the RAS precharge time, RAS Address Hold time, CAS Address setup time, CAS precharge time, CAS Read pulse-width and CAS Write pulse-width of the DRAM used in 0.5T granularity and the DRAM controller will automatically generate optimized timing to meet the target DRAM specifications. Note, if external MA, RAS and CAS buffering is required, it should be considered when setting the timing parameters. Due to the advanced optimization of the DRAM controller to maximize system performance, the resulting waveform and burst sequence timing may not always be predictable from the programmed parameters.

3.2.6.3 Mixed FPM, EDO and Burst EDO DRAM Bank Support

The DRAM controller supports standard Fast Page Mode (FPM) DRAM, Extended Data Output (EDO) DRAM, and Burst EDO DRAM. An important use of this feature is that it allows the base system memory to use EDO to maximize performance while it can accept standard FPM memory expansion card or module, in either portable or desktop system. Register DCONF3 selects the DRAM type of each bank.

3.2.6.4 Mixed Symmetric and Asymmetric DRAM Bank Support

The DRAM controller also supports mixed symmetric and asymmetric DRAM banks with depths ranging from 256K, 512K, 1M, 2M, 4M, 8M to 16M. The MA mapping of the VESUVIUS-LS is arranged such that it will work with any available symmetric and asymmetric DRAM on the market. With the proper algorithm, the BIOS can determine the number of CAS address lines in the DRAM. The BIOS can then program the Column Address bits, or COLADRx[2:0] of the corresponding Register B0C to B7C, with the proper bank size, 32-bit/64-bit configuration information. The VESUVIUS-LS will then generate the proper MA for the DRAM cycle addressed to that particular bank. Note that symmetric and asymmetric DRAM can be mixed within the same 32-bit bank pair.

3.2.6.5 DRAM Memory Map

Refer to Table 3-13 and Table 3-14 for more information.

Table 3-13. 64-Bit DRAM Bank CPU A-Bus to MA Mapping

MA	8-bit Column Address		9-bit Column Address		10-bit Column Address		11-bit Column Address		12-bit Column Address	
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS
11	22	14	23	14	24	14	25	14	25	14
10	21	24	22	24	23	24	23	13	23	13
9	20	22	21	22	21	12	21	12	21	12
8	19	20	19	11	19	11	19	11	19	11
7	18	10	18	10	18	10	18	10	18	10
6	17	9	17	9	17	9	17	9	17	9
5	16	8	16	8	16	8	16	8	16	8
4	15	7	15	7	15	7	15	7	15	7
3	14	6	14	6	14	6	14	6	26	6
2	13	5	13	5	13	5	24	5	24	5
1	12	4	12	4	22	4	22	4	22	4
0	11	3	20	3	20	3	20	3	20	3

Table 3-14. 32-Bit DRAM Bank CPU A-Bus to MA Mapping

MA	8-bit Column Address		9-bit Column Address		10-bit Column Address		11-bit Column Address		12-bit Column Address	
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS
11	21	13	22	13	23	13	24	13	25	13
10	20	23	21	23	22	23	23	12	23	12
9	10	21	20	21	21	11	21	11	21	11
8	19	10	19	10	19	10	19	10	19	10
7	18	4	18	4	18	4	18	4	18	4
6	17	9	17	9	17	9	17	9	17	9
5	16	8	16	8	16	8	16	8	16	8
4	15	7	15	7	15	7	15	7	15	7
3	14	6	14	6	14	6	14	6	14	6
2	13	5	13	5	13	5	13	5	24	5
1	12	3	12	3	12	3	22	3	22	3
0	11	2	11	2	20	2	20	2	20	2

3.2.6.6 Shadow RAM Control

Register SHADRC controls the shadow RAM readability from 000C0000-000FFFFF in 16-Kbyte granularity while Register SHADWC controls the shadow RAM writability. The 16-Kbyte granularity supports the Plug and Play BIOS specification as recommended by various BIOS vendors. In the VESUVIUS-LS, Shadow RAM readability is tied to cacheability. It means that if Register SHADRC bit [1:0] are both set to '1', then 000C0000-000C7FFF will become a cacheable region.

3.2.6.7 Advanced DRAM Refresh Support

To support all possible DRAM types, the VESUVIUS-LS also provides versatile DRAM refresh support. Register DRFSHC controls the refresh scheme, RAS pulse-width and precharge time for refresh cycles and refresh period. The DRAM refresh clock source is based on 32KHz input clock which generates an internal refresh request once every 15 µs. However, some new DRAM require to be refreshed every 3.75 µs or 7.5 µs. If such options are selected through Register DRFSHC bit [7:5], the VESUVIUS-LS will generate a burst of 4 or 2 refreshes respectively every 15 µs.

3.2.7 System Management Mode (SMM)

The VESUVIUS-LS provides a flexible SMM interface for both software and hardware. It can generate SMI by up to 52 possible sources: external pins, power management events, timer time-out, and software-triggered events. To simplify polling of SMI events, the SMI trigger sources (and masks) are grouped. Refer to Section 3.2.9.6 on page 1-71for details on SMM as it relates to power management functions. The discussion on SMM in this section is limited to SMM as it relates to the CPU interface.

3.2.7.1 SMM Base and Remapping of SMRAM

The SMM base address in the VESUVIUS-LS is defined as 000D0000H-000EFFFFH. The physical memory space used for SMM memory is at 000A0000H-000BFFFFH in DRAM. The SMBASE and remapping options are programmable by Register SMMC bit [11:4].

It is suggested to use 000D0000H-000EFFFFH as the SMBASE and set SMRAM as non-cacheable; this not only eliminates the overhead on flushing L1 cache, it also eliminates potentially high overhead for eviction of all dirty lines on flushing L1 if it is operating in the write-back mode (even though WB/WT# pin is always low during SMIACT# low).

3.2.7.2 Relocating SMBASE and Initializing SMRAM

To simplify loading SMM handler and relocating SMBASE, the V1-LS device also supports remapping 0002000H-0003FFFFH to the SMRAM (at 000A0000H-000BFFFFH). The BIOS can set Register SMMC bit 2, EN23RMAB to '0' and set SMMC bit 14, LDSMIHLDER to '1'. It can then load the SMM handler by simply writing to 00020000H-0003FFFFH, thereby initialing the SMRAM at 000A0000H-000BFFFFH. Note that L1 and L2 cache must be disabled when remapping 2-3FFFF to A0000-BFFFF.

3.2.7.3 Other SMM Characteristics

- SMRAM accesses will always be marked as L1 WT, as specified by CPU specification.
- SMRAM will not be accessible by PCI masters. If a PCI master cycle access hit the memory range of SMRAM, V1-LS will not remap the address but will access the regular DRAM, even SMIACT# is still asserted low.

3.2.8 PCI Bus Interface and Arbiter

3.2.8.1 PCI configuration Address and Data Registers

The VESUVIUS-LS supports configuration type 1 with 64 bytes of configuration space (offset 00H-3FH). The PCI configuration address and data registers are located at the standard 0CF8H and 0CFCH respectively. Since some registers within these 64 bytes are reserved, any write to these areas is to be ignored and any read from these areas is to be returned with '0's, as recommended by *PCI Bus Specifications*.

3.2.8.2 PCI Master Arbitration Scheme

The V1-LS supports up to five PCI masters, one dedicated to the V3-LS PCI-ISA bridge, and remaining four REQ[3:0]# and GNT[3:0]# pairs for PCI masters. Since V3-LS represents ISA DMA and ISA Masters which do not support preempt mechanism, therefore, V3-LS has the highest priority in the arbitration. The VESUVIUS-LS supports rotating priority scheme for the other PCI masters since they have the same priority. Note that the arbiter will only grant to the requesting master after the write buffer has been emptied.

Since V3-LS REQ#/GNT# protocol is embedded into BSER1TO3 and BSER3TO1 protocol, there are only four pairs of REQ[3:0]# and GNT[3:0]# signals.

3.2.8.3 CPU-initiated PCI Bus Cycle Types

Refer to Table 3-15 for more information on CPU-initiated PCI bus cycles types.

Table 3-15. CPU-Initiated PCI Bus Cycle Types

M/IO#	D/C#	W/R#	CPU Bus Definition	C/BE[3:0]#	PCI Bus Definition
'0'	'0'	'0'	Interrupt Acknowledge	'0000'	Interrupt Acknowledge
'0'	'0'	'1'	Special Cycle*	'0001'	Special Cycle
'0'	'1'	'0'	I/O Read	'0010'	I/O Read
'0'	'1'	'1'	I/O Write	'0011'	I/O Write
'0'	'1'	'0'	I/O Read to CF8H or CFCH	'1010'	Configuration Write
'0'	'1'	'1'	I/O Write to CF8H or CFCH	'1011'	Configuration Write
'1'	X	'0'	Memory Read	'0110'	Memory Read
'1'	'1'	'1'	Memory Write	'0111'	Memory Write

* Only Shutdown and Halt special cycles are translated into PCI cycles; V1-LS will return BRDY# to CPU for other special cycles.

3.2.8.4 PCI interrupt Acknowledge Cycle

For PC AT compatibility, the processor will generate two INTA# cycles for each INTR assertion. The PCI interface only requires one PCI interrupt acknowledge cycle for each interrupt, thus, V1-LS will generate PCI interrupt acknowledge cycle only on the second CPU INTA# cycle.

3.2.8.5 Early AD[31:0] Assertion for PCI Configuration Access

As recommended by the*PCI Bus Specification 2.1*, during PCI configuration access, AD[31:0] (in address phrase) will be driven out one PCICLK before FRAME# is asserted. This provides enough precharge time for devices that resistively connect their IDSEL signals to the AD bus.

3.2.9 Power Management Controller (PMC)

The VESUVIUS-LS power management registers have evolved from the REDWOOD/FIR family and are engineered to be more programmer-friendly, while maintaining full flexibility and versatility. The key features of the VESUVIUS-LS PMC are:

- Advanced primary and secondary activity monitors.
- Support of Fully-On, Conserve, Doze, Sleep, Deep-Sleep and 0V-Suspend or Suspend-to-Disk modes.
- Three independently programmable power control registers for On/Doze, Sleep/Deep-Sleep and Suspend mode.
- Sophisticated CPU clock management by STPCLK# (or SUSP#/SUSPA#) throttling; independent throttler control for Conserve mode; Doze/Sleep/Deep-Sleep mode and THERM input.
- Generation of PMI from 14 different groups and up to 52 events.
- I/O trap and restart support.
- Six programmable range monitors, PRM[5:0], that can monitor any I/O or memory device on read, write or read/write accesses.

- Five external power management inputs, including SWTCH, RING, WAKE0/1, and EXTACT0. Each is independently selectable to be debounced or not, and triggers on either rising, falling or both rising and falling edges.
- Three mode (Doze, Sleep, Suspend) timers and six independent device timers .
- Device timers can be linked to any monitored device, PRM0/1 or EXTACT0 input.
- Flexible and easy-to-program BCD-encoded timer and prescalar select on all timers.
- Six GPIOs and six power control outputs.
- Two programmable LED indicator outputs.
- Effective PCI clock power management .

The VESUVIUS-LS PMC provides high flexibility and programmability to meet the system power management demands in an advanced portable system. The PMC employs both passive and active power management techniques to achieve power management in both Fully-On and power saving modes. The following discussion defines the usage of each power-saving mode and feature. It assumes that the reader is familiar with SMI# and STPCLK# operations of the CPU.

3.2.9.1 Activity Monitors

The concept of National Semiconductor's Power Management Controller deals with monitoring system activities in order to determine whether the system is idle or not. Various timers, including Doze Mode Timer (DZMT), Sleep Mode Timer (SLPMT), and Suspend Mode Timer (SPNDMT) are setup to determine the amount of time the system is idle in order to trigger mode timer time-out SMI to enter a progressively lower power state. To understand how activity monitors work, first we need to define primary and secondary activity.

3.2.9.2 Primary Activity (P/A)

A primary activity is defined as an 'important' system activity which indicates that the system is active and that the system resources are being accessed. If a primary activity is unmasked, it will trigger the activity monitor. If the system is already in either Doze, Sleep or Deep-Sleep mode, P/A brings the system back to Fully-On/Conserve mode. Also, P/A will reset all mode timers, i.e., DZMT, SLPMT and SPNDMT.

The V1-LS can monitor any of the following as primary activities. Each of these activities can be enabled/disabled by the corresponding mask bits in Register PAM1 and PAM2:

Primary Activity Mask 1 (Register PAM1)

P/A can be individually masked or triggered by accesses to VGA, primary or secondary IDE, FDD, KBC, Serial I/O 1 and 2, and parallel I/O. P/A can also be individually masked or triggered by any read, write, or both read and write accesses to PRM[5:0].

NOTE: HOLD can also be enabled as a primary activity because HOLD will represent any PCI Master, including ISA DMA or ISA Master requests, which will access system resources and requires the system to be in Fully-On / Conserve mode.

Primary Activity Mask 2 (Register PAM2)

P/A can be individually masked or triggered by a 'toggling' edge (triggered by either rising, falling or both rising and falling edges). See Register EDC, Edge Detect Control on EXTACT0, RING, SWTCH, WAKE0 or WAKE1.

Primary Activity Option Control (Register PAOC)

Any unmasked P/A can optionally be flagged in the activity flag Registers, AFR1 and AFR2. To enable flagging, Register PAOC bit 0, PAFLGEN, must be set to '1'. Registers PAM1 and PAM2 correspond — bit by bit — to AFR1 and AFR2 for easy BIOS implementation.

P/A also has an option to trigger SMI and is enabled by setting Register PAOC bit 1, SMI_MSK_PA to '0'. This is useful in SMI-driven mode change environment. Example: SMI_MSK_PA should not be masked if there is any BIOS housecleaning required when switching from Sleep mode back to Fully-On mode. Register PAOC bit 3, DISPACTVON should also be set to '1' to prevent automatic transition to On mode by hardware due to primary activity.

Register PAOC, bit 2, ENLTCH_PA_SMM, when set to '1' causes any primary activity detected within SMM to latch P/A until deassertion of SMIACT#. This primary activity will keep the timers reset and the system in On mode.

Register PAOC, bit 4, MSKSMI_PA, when set to '0' allows any unmasked SMI (except for an SMI caused by primary activity to prevent a recursive generation of SMI and P/A) to trigger primary activity. This is particularly useful when a SLPTO SMI causes a transition to Deep Sleep mode and a SPNDTO SMI is generated. Even if secondary activity is unmasked for SMI, it cannot revive clocks out of Deep Sleep mode. This bit allows SPNDTO SMI to trigger a P/A which will then cause a transition from Deep Sleep back to the Fully On mode.

Primary Activity Triggered by V3-LS (Register PAIRQM-1, PAIRQM-2 of V3-LS)

The VESUVIUS-LS platform allows any unmasked IRQs to trigger P/A. This enables 'any-key wakeup' from Deep-Sleep mode or 'Network-compliant Deep-Sleep mode', among other functions. The V3-LS Registers PAIRQM-1 and PAIRQM-2 are used to mask or unmask IRQ[15:3], IRQ1 and NMI to trigger a P/A.

P/A, S/A, SMI, and other power management information is passed through the BSER1TO3 from V1-LS to V3-LS and through BSER3TO1 from V3-LS to V1-LS. Therefore, V3-LS register PMCR (20H), bit 0 (BSEREN) must be set to'1' to enable communication between BSER1TO3 and BSER3TO1.

IMPORTANT: To trigger an SMI due to a PAIRQ, set Register PMCR bit 2, PMIPAENB to '1' in V3-LS device. This will allow the generation of both P/A and SMI due to an IRQ and the SMI source will only indicate V3-LS activity as the source (not primary activity as well). The BIOS should then reference Registers PMIIRQS-1 and PMIIRQ-2 in V3-LS device to find the particular source. Note that even if Register PAOC bit 1, SMI_MSK_PA in V1-LS is set to '0', it does not generate an SMI due to PAIRQs.

3.2.9.3 Secondary Activity (S/A)

A secondary activity or S/A is one that only requires a short service time during either Doze or Sleep modes. Refer to Figure 3-12 on page 1-69, where the system will temporarily go back to full speed (or conserve throttling speed if Conserve mode is enabled) to service the S/A while remaining in the state when S/A occurs, either Doze or Sleep mode. For example, the system should typically service IRQ0 in order to keep the system timer and to ensure any chained interrupt service routine (ISR) to IRQ0 to be serviced, e.g. scheduled faxing or tape backup. If the system doesn't require such a feature, it can mask IRQ0 from S/A. Another example: During Doze mode the 'lid-switch' toggles from open to close, triggering an SMI to power-off the LCD backlight in order to maximize battery life. Note that switching to and returning from "revive state" is not a mode change and will not trigger any PC[5:0] toggling.

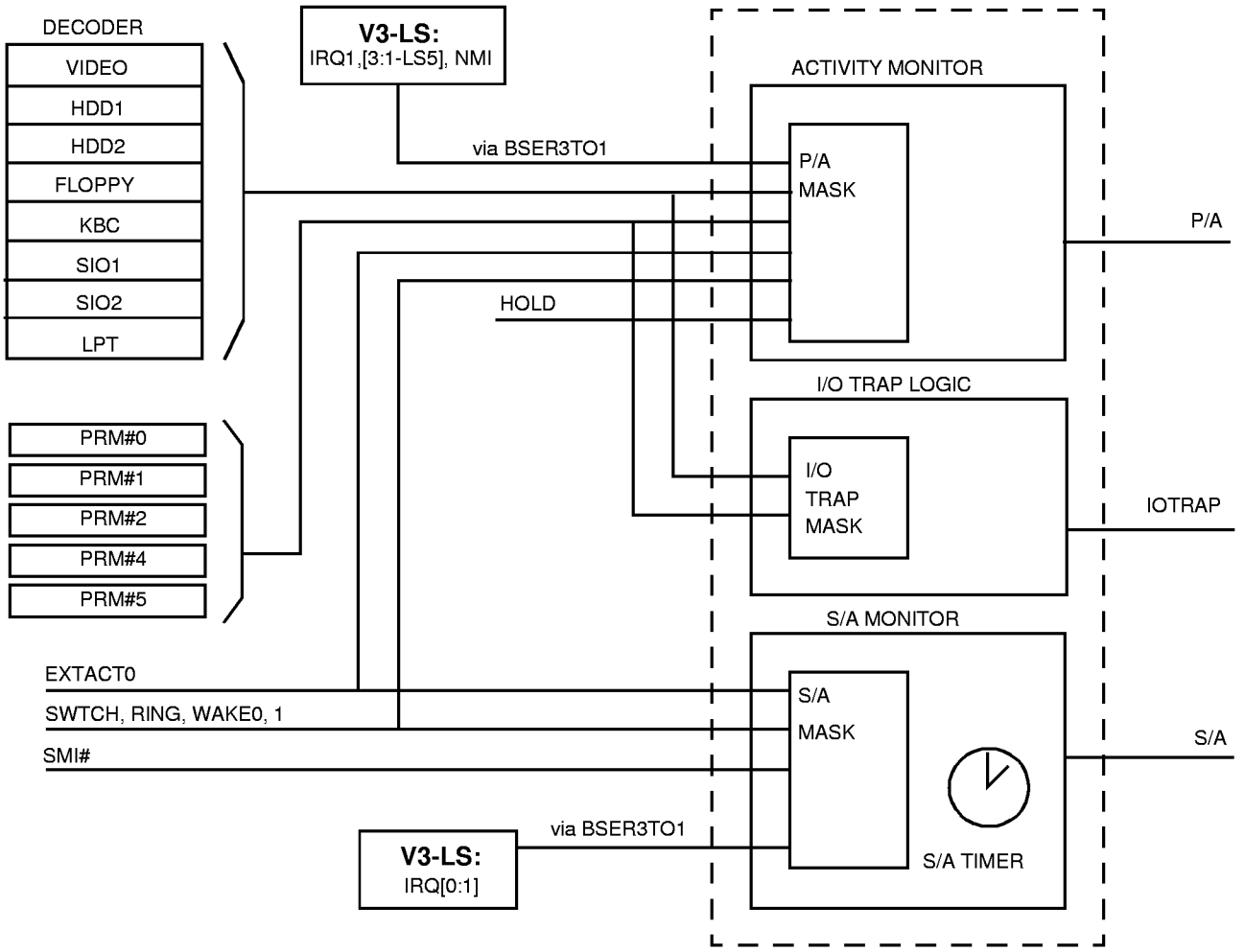


Figure 3-11. Generation of P/A, S/A, and I/O Trap

S/A cannot revive clocks from Deep Sleep mode. Since IRQ0 is not serviced, when the system wakes up from Deep-Sleep mode, a 'timing-correction' should be performed to read from RTC and update the DOS or operating system timer.

The V1-LS can monitor various secondary activities. They can be enabled/disabled by the corresponding mask bits in Register SAM :

Secondary Activity Mask (Register SAM)

S/A can be individually masked or triggered by a 'toggling' edge (triggered by either rising, falling or both rising and falling edges. See Register EDC, Edge Detect Control) on EXTACT0.

NOTE: SMI or HOLD assertion can also be unmasked to trigger S/A because SMI interrupt and PCI Master activity may only require a short period of service. This provides flexibility to different system environments. The decision to enable HOLD as P/A or S/A and SMI as S/A is system-specific and is up to the system designer.

Secondary Activity Triggered by V3-LS (Register PMCR of V3-LS)

The VESUVIUS-LS platform allows unmasked IRQ0 or IRQ1 to trigger a secondary activity. This offers a flexible option to update the system timer (IRQ0) and to service a keystroke (IRQ1) without returning to Fully-On/Conserve mode. The system designer has the choice of selecting whether a keystroke will wakeup the system (IRQ1 as P/A) or if it will only perform a screen update (IRQ1 as S/A) and wait until the key sequences to wake up the system by other P/A. Example `DIR C:<CR>` will access hard disk.

Secondary Activity Timer (Register SAT)

S/A will not reset any mode timers. However, S/A has its own timer, programmable by Register SAT. S/A timer determines the time to stay in 'revive state' before returning to either Doze or Sleep mode. The S/A timer provides a range from 100 µs to 79 ms and can be enabled or disabled. The S/A timer can be considered an 'additional time' timer.

Although typical S/A requires only a short service time, in some real-time or multitasking operating system environments, the service time may be extended due to the priority of other real-time events. The V1-LS provides various options to correctly time the S/A events.

S/A Triggered by SMI

If S/A is triggered by SMI events, SMIACT# deassertion (low-to-high edge) can be used to determine the end of the S/A event. Example: If the S/A timer is programmed to be 1 ms, the system will stay in 'revive state' until 1 ms after SMIACT# is deasserted.

For BIOS implementations that prefer to go to a power management mode which causes LessStop or MoreStop such as Sleep mode within SMM, it is recommended that Register SAT, bit 8, RST_SA_ON_SMI be used. Writing this bit high allows a one-time reset pulse to the SA on SMI latch. This terminates the secondary activity before the deassertion of SMIACT#, thus allowing STPCLK# to go low. Using this bit prevents unnecessary overhead in disabling and then enabling Register SAM, bit 0, SA_MSK_SMI.

S/A Triggered by HOLD

If a S/A is triggered by HOLD (PCI Master events), HLDA deassertion will be used to determine the end of the S/A event. Example: If the S/A timer is programmed to be 1 ms, the system will stay in 'revive state' until 1 ms after HLDA is deasserted.

S/A Triggered by IRQ0/1

If S/A is triggered by IRQ0/1, the corresponding ISR and IRR bits can be used to determine the end of S/A event. If S/A timer is programmed to be, e.g., 1 ms, the system will stay in 'revive state' until 1 ms after ISR and IRR are both cleared. Note that, since the interrupt service routine can execute EOI to clear ISR bit long before it executes IRET instruction, ISR and IRR bits can only be used as reference and S/A timer should be set to long enough time to complete the service routine, otherwise, undesirable nested interrupts may occur.

S/A Triggered by EXTACT0

If S/A is triggered by EXTACT0, the value programmed in the S/A timer will directly determine the amount of time the system will stay in 'revive state' before returning to either Doze or Sleep mode.

3.2.9.4 Power Management (PM) Modes

This section discusses the power management modes found in the VESUVIUS-LS system controller. Refer to Figure 3-12 on page 1-69 for a conceptual visualization of the VESUVIUS-LS power management modes.

Fully-On Mode

During the Fully-On mode the system is running at full-speed and all devices (except those powered-down by device timer time-out events) are powered-on.

Conserve Mode

This is a logical equivalent to the Fully-On mode. It is used in situations where prolonging the battery life is more critical than the need for full system performance. Example: running a word processing application on a portable computer during air travel. Once enabled, Conserve mode will logically replace the Fully-On mode. Register CON-CTRC enables and selects clock throttling ratio (see Section 3.2.9.5 on page 1-68 for additional details) during the Conserve mode.

Doze Mode

The first level of power conservation, this mode is typically entered when the system is idle. System idle is defined as the absence of P/A for a predefined time-out value (in range of seconds). Register DZMT selects the idle time before entering Doze mode. Register DS-CTRC is bit [4:0] enables and controls the clock throttling ratio during Doze mode. In VESUVIUS-LS, there are two ways to enter Doze mode. Each method can be selected by Register ISTM bit 6, SMI_MSK_DOZE_TO:

1) If SMI_MSK_DOZE_TO is set to '1', Doze mode can be entered automatically on DZMT time-out, without triggering SMI. This is used in situations where no PC[5:0] toggling is required. This allows entering Doze mode between keystrokes and returning to Fully-On / Conserve mode when keystroke or other P/A is detected.
2) If SMI_MSK_DOZE_TO is set to '0', then DZMT time-out will trigger a SMI. If PC[5:0] toggling is required, SMM handler should first write the new PC[5:0] state to Register ONDZ-PC, then write to Register PMM bit [2:0] to switch to Doze mode.

Note that both Fully-On and Doze modes share the same ONDZ-PC register. If Conserve mode is enabled and Doze mode is entered from Conserve, P/A will return the system to Conserve mode (or Conserve mode throttling for S/A) since it will logically replace Fully-On mode until it is disabled.

Sleep Mode

The second-level of power conservation, the Sleep mode is entered when the system is idle for a prolonged duration (defined as a range of minutes). Register SLPMT selects the idle time before entering Sleep mode. In VESUVIUS-LS, Sleep mode can be entered through SLPMT time-out SMI. Sleep mode can be entered through hardware time-out if SMI_MSK_SLPTO is set to '1. If PC[5:0] toggling is required, SMM handler should first write the new PC[5:0] state to Register SLP-PC, then write to Register PMM bit [2:0] to switch to Sleep mode.

The VESUVIUS-LS provides a high degree of programming flexibility to achieve different levels of power-savings in the Sleep mode. Also, there is a sub-mode called Deep-Sleep which provides the highest level of power-saving when compared with modes other than the Suspend mode. Refer to Table 3-16 on page 1-66 to find out about the options selected by Register DS-CTRC bit [7:5].

As shown in Figure 3-13, any unmasked S/A will temporarily put the system into 'revive state', overriding the MoreStop or LessStop and revive from Sleep mode until the S/A event or timer has expired.

Deep-Sleep Mode

This mode is entered the same way as the Sleep mode. On entering this sub-mode, STPCLK# is asserted continuously, PMC waits for Stop Grant bus cycle, stops the CPUCLK (CPU enters Stop Clock state) and then a clock-gate blocks the CLKIN from the internal logic. Register SPND_PC can be programmed to toggle PC output to either power-off or power-down CLKIN and other high speed clocks except 32 kHz (to keep the PMC running). On waking up from Deep-Sleep mode, the PC output (set high in Register ONMD_PC) will toggle to power-on CLKIN and other high speed clocks, wait for 20-30 ms stabilization time, and then the clock-gate will cleanly pass CLKIN to the internal logic. CPUCLK is then restarted, waits for the 'STPCLK Release Latency' (defined in DS-CTRC bit [10:8]), and then STPCLK# will be deasserted so that the CPU can service the P/A or SMI events. Refer to Register PAOC regarding the use of MSKSMI_PA bit to trigger a P/A due to an SMI to return to On mode from Deep Sleep mode.

Table 3-16. Register DS_CTRC bit[7:5] Selectable Options

DS-CTRC Bit [7:5]	Function
'000'	**Disable clock throttling in Sleep mode** .
'001'	**Enable clock throttling in Sleep mode:** The ratio is selected by DS-CRTC bit [2:0]
'010'	**Enable LessStop state (CPU in Stop Grant state) in Sleep mode:** STPCLK# will be asserted continuously, with CPUCLK running, until the system returns to Fully-On / Conserve mode by P/A.
'011'	**Enable MoreStop (CPU in Stop Clock state) in Sleep mode:** In this case, STPCLK# will be asserted continuously, with CPUCLK stopped, until the system returns to Fully-On / Conserve mode by P/A. DS-CTRC bit [10:8], STPCLK Release Latency, controls the time from CPUCLK restarted to STPCLK# deasserted to meet various CPU PLL stabilization specifications (1 µs to 2 ms).
'100'	**Enable Deep-Sleep mode:** Deep- Sleep mode is defined to provide a very low power state with very fast wakeup time.

If using the DISPACTVON bit (Register PAOC), make sure that it is low before entering Deep-Sleep mode; otherwise a P/A source cannot wakeup the system. The VESUVIUS-LS provides the capability to wakeup from Deep-Sleep mode by pressing any key since an IRQ is communicated through BSER3TO1 pin toggling. Any unmasked IRQs can trigger P/A to wake up from Deep-Sleep mode. Similarly, 'Network-compliance' is achieved due to the fast wakeup time possible from the network polling interrupt (around 30 ms).

As mentioned earlier, an S/A cannot revive the system out of Deep-Sleep mode. This is to maximize the power-savings since most devices are already in a static state (high frequency clock is stopped).

Suspend Mode

This mode offers the highest level of power saving. Suspend mode is activated (always through software) if the system is idle for an extended period after having entered the Sleep mode. Register SPNDMT selects the idle time before entering Suspend mode. There are two different implementations of the Suspend mode:

0V-Suspend or Suspend-to-Disk (STD)

The system and video memory, status, register dump, and shadowed register values are stored in the hard disk. A flag is setup in CMOS SRAM to indicate that a 0V-Suspend has previously occurred. Then the system (except the RTC and optionally, a microcontroller that monitors the keyboard and switch but-

ton activity) is totally shut-off. This mode does not require leakage control because all system devices, including V1-LS, are powered-off.

If the modem RING or RTC alarm IRQ8# is allowed to wake up a system in 0V-Suspend, an external microcontroller can be used to monitor the toggling of RI# from RS232 or PCMCIA and the assertion of IRQ8# since the V1-LS is powered off. The microcontroller will then resume the system by powering the DC/DC converter; the BIOS will check the CMOS SRAM flag to determine if a 0V-Suspend has occurred and perform the proper resume sequence. Refer to Figure 3-2 on page 1-39 for details.

Since the V1-LS is off, the 0V-Suspend and resume process relies on the external microcontroller. Therefore:

- Register WSS bit [10:8] will not indicate any wake source on resume from STD
- Register WMC bit [3:0] is not applicable to STD
- Register RCC bit [4:0] is not applicable to STD
- Register SPND-PC is not applicable to STD
- Register LC is not applicable to STD

5V-Suspend or Suspend-to-RAM (STR)

In this mode most devices (except V1-LS, VGA, RTC and optionally, the external microcontroller or PCMCIA controller) are powered off. Leakage control is required for all devices that are powered on during STR. V1-LS will keep the system DRAM refreshed while the VGA will keep the video memory refreshed. Register settings of devices that will be powered-off should be saved. For read-only registers, particularly for important ISA resources, the V3-LS provides an extensive set of shadow registers to enable the read-back process.

A flag is setup in CMOS SRAM to indicate that a STR has previously occurred. The BIOS will then write to Register SPND-PC to power-off the appropriate devices. In this mode, the system can wakeup directly from external PM inputs including SWTCH, RING, WAKE0 and WAKE1. If the RTC alarm IRQ8# will be allowed to wake up a system in STR state, one can utilize any unused wake sources or an external microcontroller to monitor the assertion of IRQ8#, then the microcontroller will assert any external wakeup source to resume the system. On resume, the BIOS will perform the proper resume sequence if the CMOS SRAM flag determines that a STR has occurred. In this mode, RCRST# and PWRGOOD must be kept high.

On resume, the BIOS should:

- Read Register WSS bit [10:8] to determine the wake source. If the wake source is an external microcontroller, the BIOS should interrogate the microcontroller on the source.
- Clear the wake source by writing Register WSS bit [10:8] to '111'.
- Execute resume sequence.

NOTE: All power planes of V1-LS must be kept on during the STR mode.

The following registers are reset during 5-V Suspend mode:

Table 3-17. Registers Reset During 5-V Suspend Mode

Index	Register Type	Registers Reset During 5-V Suspend
1XXH	Miscellaneous	110H-114H; 118H-119H, 11BH-11FH
2XXH	DRAM	None
3XXH	PMC	300H-304H; 310H (bit[4:0]); 311H; 314H-31DH; 320H-32DH; 335H-338H; 344H-34DH;
4XXH	L2 Cache	400H-402H
n.a.	PCI	All

3.2.9.5 CPU Clock Management (Using Clock Throttling)

Clock throttling, a technique that periodically modulates STPCLK# without stopping or scaling the clock to the CPU, has been used extensively in VESUVIUS-LS. This is because the minimum CPU bus frequency is 33 MHz and even if the CPU is allowed to run at that frequency continuously, it will still consume substantial power (and generate heat). In VESUVIUS-LS, the system designer can select both the clock throttling period (CTP) and clock throttling ratio or duty cycle (CTR) to fit various hardware and operating system requirements. For example, you may not want to select a CTP longer than the time slot in a multitasking operating system. CPU speed emulation — a by-product of clock throttling — is possible because the CPU performance will be scaled during STPCLK# throttling. Also, clock throttling can achieve substantial power-saving without the PLL stabilization penalty associated with Stop Clock state.

The VESUVIUS-LS has an independent CTR control during the following modes:

- Conserve mode, through Register CON-CTRC
- THERM input indicating overheat condition, through Register HR-CTRC
- Doze/Sleep mode, through Register DS-CTRC

Register CTPC selects the CTP from 800T to 409600T (where T=CPU bus frequency period) and the CTP is applicable to all CTRs. Example: If the CPU bus frequency is 66 MHz or T=15 ns, setting Register CTPC bit [2:0] to '100' or 12800T will enable STPCLK# to throttle with the duty cycle programmed in the 192-µs period when triggered.

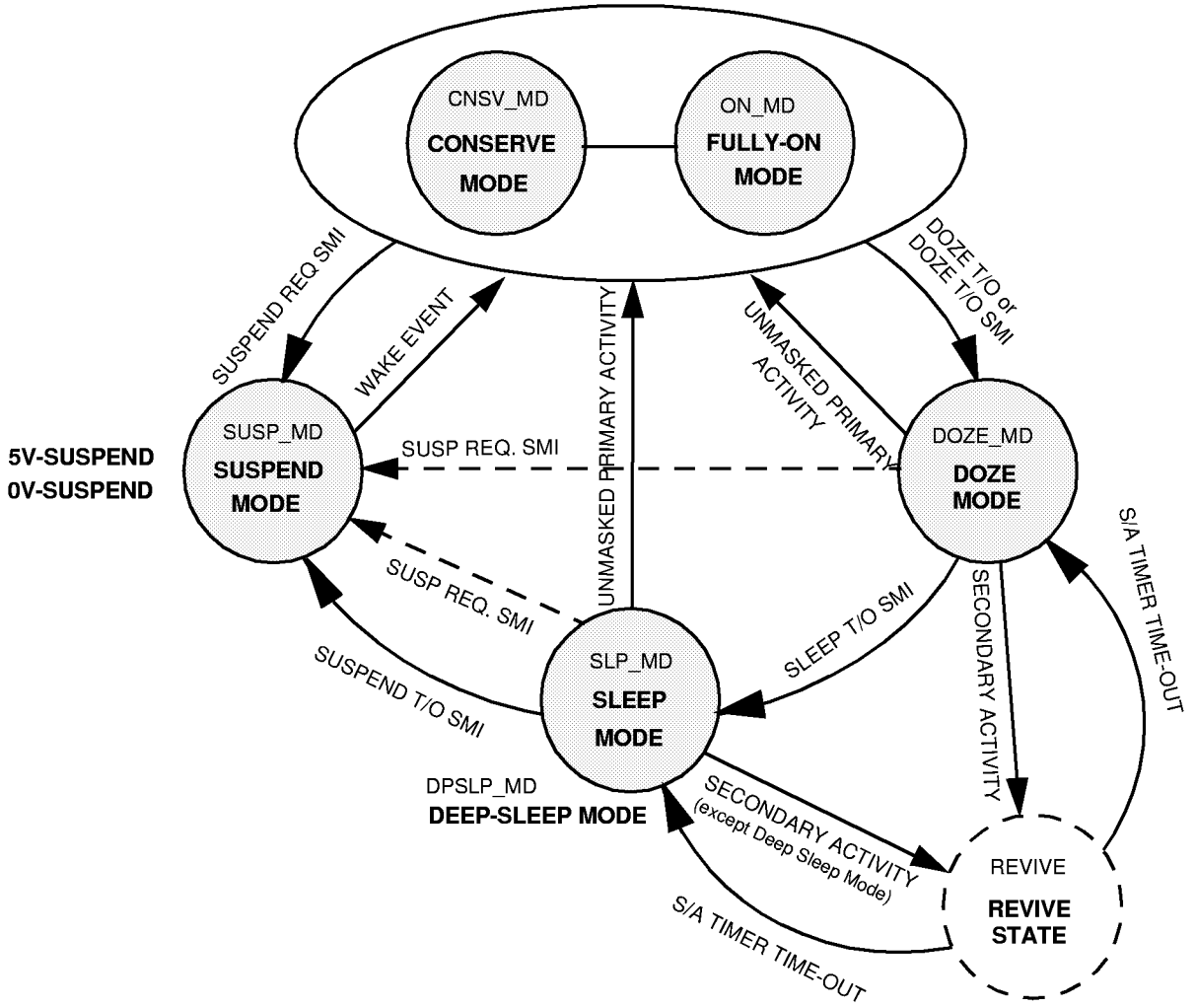


Figure 3-12. Conceptual Visualization of Power Management Mode s

Refer to Figure 3-13 for additional information. Each CTR is selectable as 5 percent or 10 to 90 percent in 10 percent steps. The percentage is defined as the time when the CPU is operating, or STPCLK# is deasserted. This gives independent and automatic control when switching between different modes. For example, if a user selects CON-CTRC=50%, HR-CTRC=5% and DS-CTRC=20%, once Conserve mode is enabled, STPCLK# will start throttling with 192 µs period and STPCLK# will be deasserted 50 percent of the time. If THERM — programmable as active-high or active-low in Register PINMUX bit [7:6] — is asserted indicating a CPU overheat condition, STPCLK# will change the throttling ratio to only 5 percent of the time deasserted.

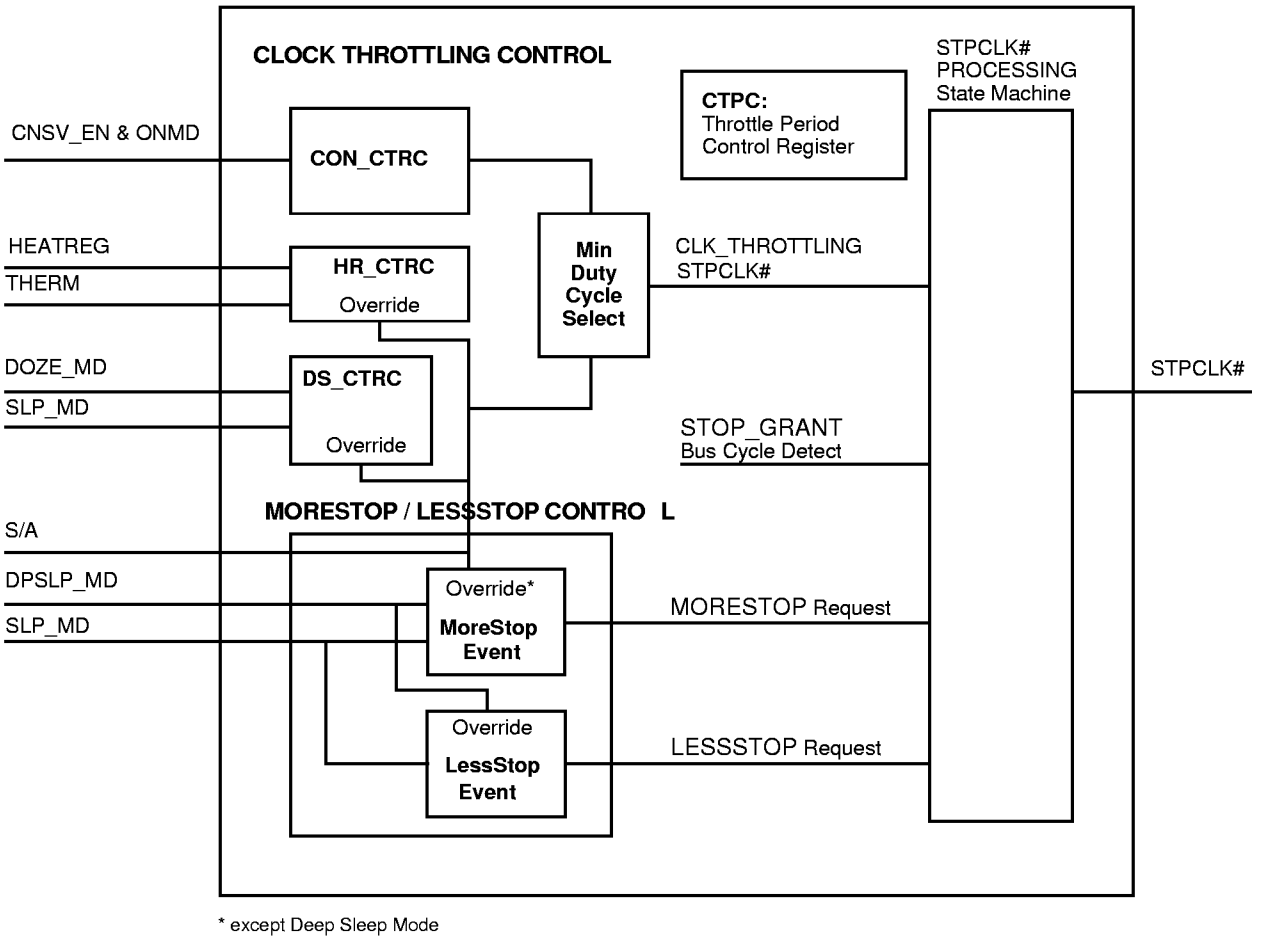


Figure 3-13. STPCLK# Generation in VESUVIUS-LS

On entering the Doze mode (with THERM input deasserted), the V1-LS will change the STPCLK# throttling ratio to 20 percent. To prevent the CPU from overheating due to incorrect parameters, the V1-LS is equipped with a "Minimum Duty Cycle Selector." Therefore, if CON-CTRC=20%, and HR-CTRC=50%, asserting THERM will not change throttling ratio to 50 percent; the minimum duty cycle selector will choose 20 percent instead.

Note that S/A will override MoreStop, LessStop, HR-CTRC and DS-CTRC's STPCLK# assertion. This means that if the Conserve mode is not enabled, S/A will immediately deassert STPCLK# to process the S/A event. In the case of MORESTOP, STPCLK# will be deasserted after the PLL Restart Latency. However, if Conserve mode is enabled, S/A will revert to the throttling ratio defined in Register CON-CTRC.

Both Doze and Sleep mode enable throttling ratios defined by Register DS-CTRC bit [3:0]. Sleep mode provides options other than clock throttling, like LessStop, MoreStop or Deep-Sleep mode. Refer to Section 3.2.9.4 on page 1-65for details.

3.2.9.6 SMI Sources

The V1-LS can generate PMI, which triggers SMI#, from 14 different groups and up to 52 individual events. Table 3-18 shows the SMI sources defined in Register WSS bit [4:0] and the corresponding actions in the SMM handler. Refer toFigure 3-14 on page 1-72for a diagrammatic presentation of all the SMI sources. Due to the nature of different SMI groups, they are masked or unmasked through different mechanism.

Table 3-18. SMI Sources

Bit[4:0]	Source Group	Action in SMM Handler
00H	None	
01H	Primary Activity	Read AFR1, AFR2 to determine activity source, execute P/A handler, and then clear activity flag.
02H	I/O Trap	Read AFR1 to determine activity source, execute I/O Trap handler, and then clear activity flag.
03H	Device Timers time-out	Read AFR2 bit[13:8] to determine time-out source, execute device time-out handler, and then clear activity flag.
04H, 05H,- 06H	Doze, Sleep, or Suspend time-out	Read Register PMTS to confirm, execute PM mode switching handler, and then clears corresponding time-out status bit.
07H 08H	GP Timer Compare SWTCH Input Toggling	Execute GP Timer Time-out handler Execute SWTCH handler.
0AH, 0BH	WAKE0, 1 Input Toggling	Execute WAKE0, 1 handler.
0CH,	EXTACT0 Input Toggling	Execute EXTACT0 handler.
0EH	Rescheduled PMI	Recall SMI that has been previously rescheduled, and then execute appropriate SMM handler.
0FH	Software SMI	Execute APM-related handler (typical).
10H	V3-LS INT SMI	Read V3-LS Register PMIIRQS-1 and PMIIRQS-2 to determine IRQ source, execute SMM, and then clear activity flag.

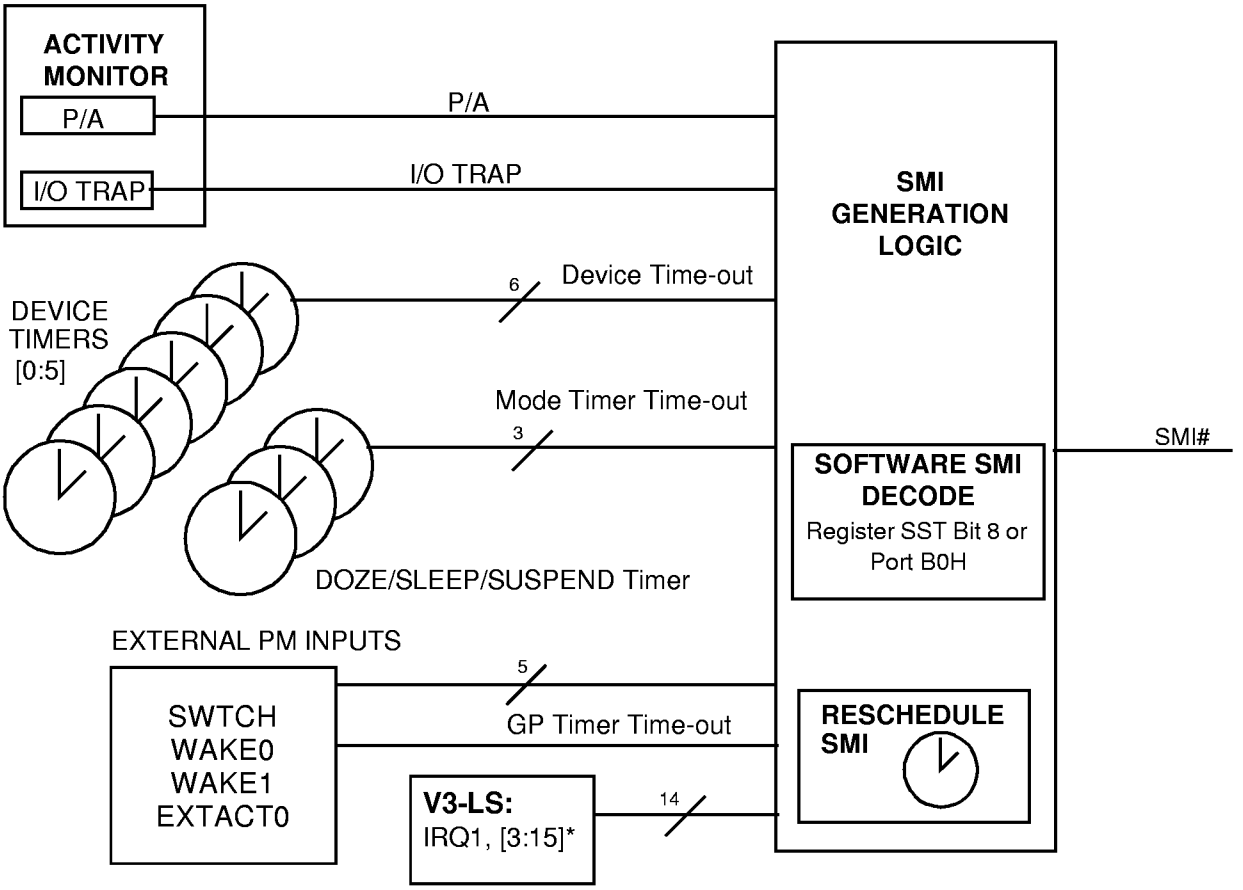


Figure 3-14. SMI# Generation in VESUVIUS-LS

SMI Triggered by P/A

P/A will trigger SMI if Register PAOC bit 1, SMI_MSK_PA is set to '0' and any unmasked P/A occurs. Individual P/A can be unmasked by Register PAM1, PAM2, and V3-LS Register PAIRQM-1 or PAIRQM-2.

SMI Triggered by I/O Trap

There is no group mask for an I/O Trap event. SMI will always be generated if the corresponding bit in Register IOTM is set to '0' and an access to that device occurs. Refer to Section 3.2.9.8 on page 1-74 for I/O Trap and Restart support in V1-LS.

SMI Triggered by Device Timers Time-out

Time-out of device Timer [5:0] will trigger SMI if the corresponding bit in Register ISTM bit [5:0] is unmasked. Refer to Section 3.2.9.4 on page 1-65 for using Device Timers in I/O Trap operation in V1-LS.

SMI Triggered by Doze, Sleep or Suspend Time-out

Doze, Sleep or Suspend time-out will trigger SMI if the corresponding bit in Register ISTM bit [6:8] is unmasked. See Section 3.2.9.4 on page 1-65 for power management modes.

SMI Triggered by SWTCH, WAKE0, WAKE1, and EXTACT0 Toggling

Toggling of SWTCH, WAKE0/1, and EXTACT0 will trigger SMI if the appropriate bits in Register ESTM bit [4:0] are unmasked. Programmable in Register EDC (Edge Detection Control), power management input "toggling" can be selected to trigger either on rising, falling or both rising and falling edges. See Section 3.2.9.10 on page 1-76 for more information on PM inputs.

Rescheduled SMI

If a SMI is triggered during a critical system operation, especially if it requires the system resources currently in use, that SMI should be rescheduled. Example: The system is updating the HDD while a 0V-Suspend request is issued. In this instance, the SMI should be rescheduled until all HDD operations are done. Typically, a flag will be setup to tell which SMI source is being rescheduled so that on Rescheduled SMI, the SMM handler can read the flag and determine the original SMI event. The rescheduling can range from 10 ms to 900 ms, selectable by Register SST bit [4:0]. In some situations, the same event may need to be rescheduled more than once.

Software SMI

Software SMI is mainly triggered by APM-idle call. V1-LS has two options for the APM BIOS to trigger a software SMI:

1) If a value of '1' is written to Register SST bit 8, this will trigger a software SMI.
2) If Register SST bit 9 is set to '1', a write to I/O port 0B0H will trigger a SMI.

When APM issues a call for low or very low power operation, the SMM handler then has a choice of putting the system into Doze, Sleep or Deep- Sleep mode with appropriate CTRs setup.

Nested SMI

The VESUVIUS-LS fully supports nested SMI. It is recommended that the SMM handler should check if there is any pending SMI before exiting SMM; this will save tremendous overhead on entering and exiting SMM. Multiple SMIs that occur simultaneously will be latched. To ensure that pending SMI will not be lost at the end of the current SMM handler, it should clear the SMI source by writing 1Fh to Register WSS bit [4:0], and then clear the corresponding activity flag in Register AFR1 or AFR2. The SMM handler can then detect any pending SMI by reading Register WSS bit [4:0]. The presence of a non-zero value indicates that a pending SMI exists and the SMM handler can then jump directly to the proper SMM handler to process it.

There are two simple rules for nested SMI:

1) On polling for nested SMI, the next SMI that pops up will be based on priority, but will not be in a chronological order.
2) SMI can be generated and nested in any sequence, except that the same SMI source cannot be nested itself before the SMM handler clears the SMI source and its activity flag.

3.2.9.7 Device Timer Time-out

The V1-LS has six device timers with time-out values ranging from 1 sec. to 90 min. in either 1 sec., 10 sec., 1 min., 10 min. steps. These device timers are independently programmable by Registers DDT0 to

DDT5. All monitored devices, including VGA, primary IDE, secondary IDE, FDD, KBC, serial I/O 1 and 2, parallel port, PRM0/1 and EXTACT0 can be linked to the device timers. Each timer can be linked to one or more devices, but each device can be linked to only one timer. The devices and timers are linked through the Registers DDTS1 to DDTS4 (Device Timer time-out Source). Note that EXTACT0 is used to monitor devices that are equipped with an output that indicates access to that device.

The VESUVIUS-LS also has a special device timer feature: the BIOS can setup a device timer without linking any device to it, which will then become a generic timer to trigger SMI. In the VESUVIUS-LS, the designer has up to seven generic timers, including six device timers and a doze timer (DZMT). If bit 8 of DZMT is set to '0' it will prevent a P/A from resetting the doze timer.

3.2.9.8 I/O Trap and Restart Support

I/O Trap and Restart, a special CPU feature, is usually used to trap an I/O access to a powered-off device. If the CPU accesses a device which has been powered-off, the V1-LS can generate an SMI to initiate an I/O Trap event if SMI# is asserted at least three CPUCLK before BRDY# is asserted (guaranteed by V1-LS). The SMM handler will power-on the device and instruct the CPU to restart the I/O cycle by writing a value 0FFH to offset 7F00H in SMRAM.

Devices that are powered-off during Fully-On, Doze or Sleep modes can result from either PC toggling during mode-switching or time-out of any of the six device timers triggering SMI to power-off the idle device(s). A device timer can be linked to one or more monitored devices and any access to the device(s) will reset the linked device timer if there is no activity on the linked device(s) for the preprogrammed period. A device timer time-out SMI (seeSection 3.2.9.6 on page 1-71) will be triggered and the SMM handler will then power-off or power-down the device(s).

Note that the I/O trapping address range can be different from the P/A monitoring range for the same device. Refer to Table 3-19 for the address ranges.

Table 3-19. I/O Trap and Primary Activity Address Ranges

Device	Primary Activity Address Range	I/O Trap Address Range
Hard Disk 1	1F0H-1F7H, 3F6H	1F0H-1F7H, 3F6-3F7H
Hard Disk 2	170H-177H, 376H	170H-177H, 376-377H
Floppy Disk Drive	3F2H, 3F4H, 3F5H	3F2H, 3F4H, 3F5H, 3F7H

Programming Example 1

Primary IDE, or Hard Disk 1 is linked to Device Timer 3. On device timer 3 time-out, SMI# is asserted, and the SMM handler will:

- Read Register WSS (Wake/SMI Source) to determine the SMI source. In this example, WSS bit [4:0], or SMISRC, will indicate 03H, or device timers time-out event. Then clear SMI source by writing 1FH to WSS bit [4:0].
- Read Register AFR2 to determine which Device Timer time-out. In this example, Register AFR2 bit 11, DEVTMRTO3, will be set indicating HD1 is timed out by Device Timer 3. Then clear Device Timer [3] time-out flag in Register AFR2.
- Set Register PAM1 bit 1 to mask PAM1 from triggering P/A.
- Clear Register IOTM bit 1 to enable I/O Trapping for HD1 address range (1F0-1F7, 3F6-3F7).

- Power-off HD1 through the appropriate PCx or GPIOx.
- If there is no other pending SMI request, then exit SMM.

Programming Example 2

On CPU accesses to HD1 which is powered-off when device timer 3 times out. The V1-LS will trigger SMI# to initiate the I/O Trap, and the SMM handler will:

- Read Register WSS to determine the SMI source. In this example, WSS bit [4:0] will indicate 02H, or I/O trap event. Then clear SMI source by writing 1FH to WSS bit [4:0].
- Read Register AFR1 to determine what device access triggers the I/O trapping. In this example, Register AFR1 bit 1, HD1_ACTV will be set indicating HD1 is accessed. Then clear HD1_ACTV flag in Register AFR1.
- Clear Register PAM1 bit 1 to enable PAM1 to trigger P/A.
- Set Register IOTM bit 1 to mask I/O Trapping for HD1 access.
- Power on HD1 through the appropriate PCx or GPIOx.
- Optionally, wait for 3 seconds for HD1 to spin-up to accept commands.
- If there is no other pending SMI request, then exit SMM.

3.2.9.9 Programmable Range Monitors (PRM)

The V1-LS has six PRMs, namely PRM[5:0]. PRM is defined primarily for activity detection and can be used to monitor any user-defined I/O or memory address ranges. It can also detect either read, write or both read and write access to trigger an event. The following describes how the PRM is programmed. PRM[5:0] are independently programmable:

Register PRM_CTRL1 bit [5:0] controls PRM[5:0] to monitor either memory or I/O.

Register PRM_CTRL1 bit[13:8] enables PRM[5:0].

Register PRM_CTRL2 bit [5:0] enables 'write access' to trigger PRM[5:0] event.

Register PRM_CTRL2 bit [13:8] enables 'read access' to trigger PRM[5:0] event.

The PRM address compare logic works like this: A 'base address' Register defines the base I/O or memory address range of the device. For an I/O device, PRMAx[15:0] will correspond to A[15:0]. For a memory device, PRMAx[14:0] corresponds to A[28:14] and PRMAx15 will be ignored. A 'compare mask' register is a bit mask defining which PRMAx[15:0] will be compared against the equivalent CPU address in the decoder.

Programming Example 1

If PRM0 is used to decode and monitor write-access to an audio device with address 0220-022F, then:

PRM_CTRL1 bit 0 = '0', bit 8 = '1'

PRM_CTRL2 bit 0 = '1', bit 8 = '0'

PRMA0 should be set to 0220h

PRMC0 should be set to FFF0h

Programming Example 2

If PRM1 is used to decode and monitor read/write access to two memory address blocks, one at 128 Mbyte and another at 129 Mbyte boundary, then:

PRM_CTRL1 bit 1 = '1', bit 9 = '1'

PRM_CTRL2 bit 1 = '1', bit 9 = '1'

PRMA1 should be set to 2000H

PRMC1 should be set to FF80H

3.2.9.10 Power Management (PM) Inputs

Power management inputs are defined as inputs involved with power management functions like triggering a P/A, S/A, SMI or wakeup event. The following five PM inputs are available in V1-LS: SWTCH, WAKE0, WAKE1, EXTACT0, and RING. The PM inputs have the following characteristics:

- All inputs can be unmasked to trigger P/A (see Register PAM2).
- Activities on unmasked inputs can be read through Register AFR2.
- All input pin status can be read through Register PMPS.
- All inputs can be unmasked to trigger SMI, except RING input (see Register ESTM).
- All inputs can be unmasked to wake up from suspend, except EXTACT0 (see Register WMC).
- All inputs have independent debounce control through Register DBC.
- All inputs have independent edge detect control through Register EDC.

Other Characteristics

- EXTACT0 can be unmasked to trigger S/A (see Register SAM).
- EXTACT0 can be linked to reset device timers (see Register DTTS4).
- The number of RING to wake up from suspend is programmable in Register RCC.
- The wake mask of SWTCH is default-disabled, all other wake masks are default-enabled.

THERM, dedicated for external thermal sensor input to trigger clock throttling with ratio defined in HRCTRC, is also a PM input although it doesn't perform any function other than preventing prolonged CPU overheat condition. Refer to Register PINMUXfor more information.

Reading PM Input Pin Status

The V1-LS provides Register PMPS for SMM handler to read the pin status (except THERM) of all the PM inputs. This is necessary for any PM inputs programmed to trigger on both rising and falling edges. The BIOS needs to read the pin status to determine the proper action. Example: A lid switch is connected to EXTACT0 which generates a falling edge on closing the lid and a rising edge on opening it, and both will trigger SMI. The SMM handler will read the EXTACT0 status from Register PMPS. If it is '0', then it will turn off the LCD backlight and vice versa.

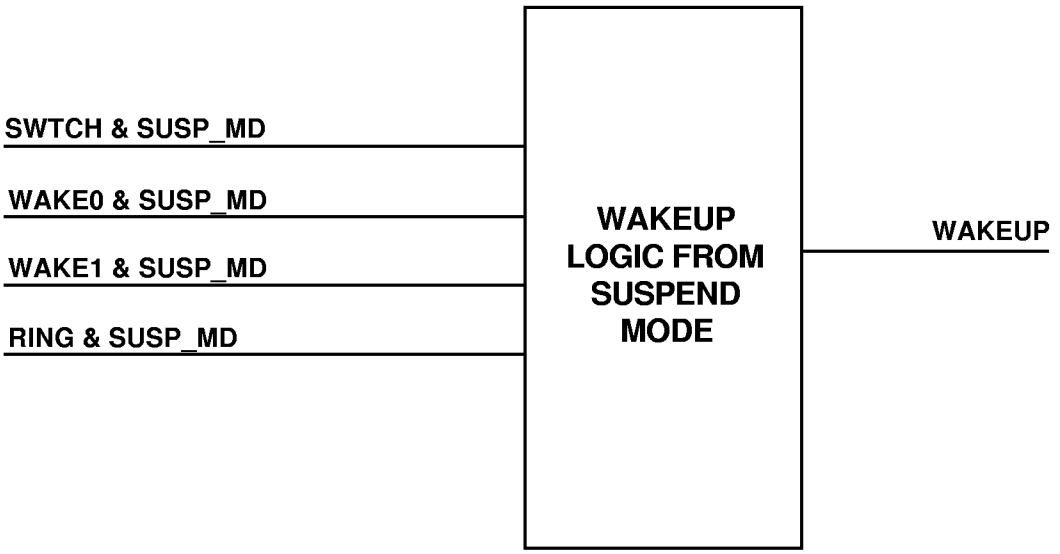


Figure 3-15. WAKE Sources in VESUVIUS-LS

3.2.9.11 PCICLK Power Management

The V1-LS has proprietary PCICLK power management control. Register PCIC bit [5:4] selects the number of PCICLKs that the PCI bus has idled (FRAME# and IRDY# deasserted). The idle count ranges from 0 (immediate) to 256 PCICLKs. When the idle condition is met, PCICLK will be divided down by the PCICLK divisor programmed in Register PCIC bit [1:0].

On CPU-initiated PCI bus cycle, PCICLK is returned to full speed immediately before FRAME# is being asserted and there is no performance loss. On PCI master cycle, V1-LS will detect REQ# assertion to return PCICLK to full speed. Slowing down the PCICLK will increase the latency in recognizing REQ# but does not cause a performance loss.

4. V1-LS REGISTER INFORMATION

This chapter describes the registers contained in the V1-LS device. The registers are divided into the following groups:

- Reset Sampling and Miscellaneous Registers
- DRAM Registers
- PMC Registers
- Level-2 Cache Registers
- PCI Configuration Registers

NOTE: Some registers discussed here may not be consecutively numbered ; registers reserved for future expansion are not shown in this chapter. Note that 16-bit access to Port 24H and 26H will be directed to V1-LS and not passed to the PCI bus. Access to V3-LS registers must be executed as an 8-bit access to Port 24H and 26H.

4.1 Register Summary Table

This table shows the index numbers and page cross-references to detailed register descriptions.

Index	Register Name	Abbreviation	Page
Reset Sampling and Miscellaneous Registers			
100H	Revision ID Register	V1_ID	1-81
101H	V1 Power On Register	V1_POC	1-82
110H	Programmable Region 1 Register	PR1	1-84
111H	Programmable Region 2 Register	PR2	1-85
112H	Programmable Region 3 Register	PR3	1-86
113H	Programmable Region 4 Register	PR4	1-87
114H	Programmable Region Control Register	PRC	1-88
118H	SMM Control Register	SMMC	1-90
119H	Processor Control Register	PROC	1-93
11AH	Write FIFO Control Register	WFIFOC	1-95
11BH	PCI Control Register	PCIC	1-96
11CH	Clock Skew Adjust Register	CSA	1-97
11DH	Bus Master and Snooping Control Register	SNOOPCTRL	1-98
11EH	Arbiter Control Register	ARBCTRL	1-99
11FH	Docking Control Register	DOCKC	1-100
DRAM Registers			
200H	Shadow RAM Read Enable Control Register	SHADRC	1-101
201H	Shadow RAM Write Enable Control Register	SHADWC	1-103
202H	Bank 0 Control Register	B0C	1-105
203H	Bank 1 Control Register	B1C	1-106
204H	Bank 0/1 Timing Control Register	B01TC	1-107
205H	Bank 2 Control Register	B2C	1-109
206H	Bank 3 Control Register	B3C	1-110
207H	Bank 2/3 Timing Control Register	B23TC	1-111
208H	Bank 4 Control Register	B4C	1-113
209H	Bank 5 Control Register	B5C	1-114
20AH	Bank 4/5 Control Register	B45TC	1-115
20BH	Bank 6 Control Register	B6C	1-117
20CH	Bank 7 Control Register	B7C	1-118
20DH	Bank 6/7 Timing Control Register	B67TC	1-119
20EH	DRAM Configuration Register 1	DCONF1	1-121
20FH	DRAM Configuration Register 2	DCONF2	1-122

4.2 Reset Sampling and Miscellaneous Registers

4.2.1 Revision ID Register (V1_ID)

Index: 100H

Bit	Description	Name	Reset State
0	V1-LS Mask ID [0]	V1LS_MSK_ID0	'0'
1	V1-LS Mask ID [1]	V1LS_MSK_ID1	'0'
2	V1-LS Mask ID [2]	V1LS_MSK_ID2	'0'
3	V1-LS Mask ID [3]	V1LS_MSK_ID3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**V1-LS Mask ID [3:0]:** These bits indicate the metal-mask version of the V1-LS device. 3H = Revision AA 4H = Revision BB 5H = Revision CC
15:4	Reserved

4.2.2 V1 Power On Register (V1_POC)

Index: 101H

Bit	Description	Name	Default State
0	Miscellaneous Configuration Bit [0]	MISC_CFG0	PU/PD strap
1	Miscellaneous Configuration Bit [1]	MISC_CFG1	PU/PD strap
2	Miscellaneous Configuration Bit [2]	MISC_CFG2	PU/PD strap
3	Clock Skew Adjust [0]	CLK_SKW0	PU/PD strap
4	Clock Skew Adjust [1]	CLK_SKW1	PU/PD strap
5	Clock Skew Adjust [2]	CLK_SKW2	PU/PD strap
6	DRAM Power Plane Voltage	DRAM_VCC	PU/PD strap
7	PCI Power Plane Voltage	PCI_VCC	PU/PD strap
8	Snooping Scheme	SNOOP_CFG	PU/PD strap
9	Reserved		PU/PD strap
10	Tristate All Outputs	TRSTATE	PU/PD strap
11	Internal Clocks for Simulation	INT_CLK	PU/PD strap
12	Reserved		PD strap
13	Reserved		PD strap
14	Reserved		PD strap
15	Reserved		PD strap

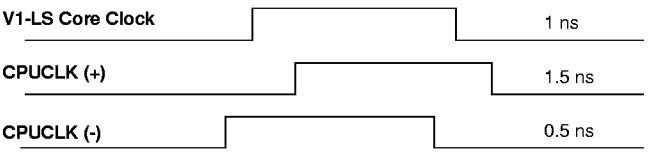
The V1 Power On register is loaded on the leading edge of the RCRESET pulse. This pulse should be triggered by power first being applied to the V1-LS device. At this time the present value of MA[11:0] will be loaded into the corresponding register bits. Once set, this register becomes read only. To select the desired options for a particular system, each MA pin should have either a pull-up or pull-down connected. From the point of powering up the V1-LS until slightly past the leading edge of RCRESET pulse, all MA pins will be floating. Therefore, the pull-up or pull-down will easily set each MA pin to the appropriate high or low value. It is recommended that 100 K resistors be used. Since MA pins do not have internal pull-downs, every MA pin should have either a pull-up or pull-down connected externally to ensure Power-On sampling.

NOTE: All reserved bits in this register must be pulled-down to ensure future compatibility.

IMPORTANT: Refer to Appendix F for special information related to silicon revision BB.

Bit	Description
2:0	**Miscellaneous Configuration Bit [2:0]:** These signals can be strapped to indicate miscellaneous system configuration. Example: In the case of Intel's Pentium or Cyrix's M1 processors, the user can define the bus-to-core frequency ratio to simplify the BIOS detection algorithm.

Bit	Description *(cont.)*
5:3	**Clock Skew Adjust:** These bits can be used to adjust the clock skew of CPUCLK, relative to V1-LS core clock. The following illustration shows how to interpret '+' and '-' delay.



Bit [2:0]	Delay (relative to V1 core clock)
'000'	0.0 ns (recommended default)
'001'	+0.55 ns
'010'	+1.10 ns
'011'	+1.65 ns
'100'	-2.20 ns
'101'	-1.65 ns
'110'	-1.10 ns
'111'	-0.55 ns

6	**DRAM Power Plane Voltage:** '0' = 3.3-V; '1' = 5-V. **NOTE:** This bit applies to Revision BB and later silicon revisions.
7	**PCI Power Plane Voltage:** '0' = 3.3-V; '1' = 5-V. **NOTE:** This bit applies to Revision BB and later silicon revisions.
8	**Snooping Scheme:** '0' = HOLD/HLDA; '1' = BOFF#/LOCK#. **NOTE:** This bit applies to Revision CC and later silicon revisions.
9	Reserved
10	**Tristate All Outputs:** When this bit is set to '0', it indicates a 'no tristate' condition; when set to '1', it indicates a 'tristate' condition.
11	**Use Internal Clocks for Simulation Purposes:** When this bit is set to '0', it disables the internal clock speedup. Setting this bit to '1' enables the internal clock speedup.
15:12	Reserved

4.2.3 Programmable Region 1 Register (PR1)

Index: 110H

Bit	Description	Name	Reset State
0	Programmable Region 1 Block Size [0]	PREG1S0	'0'
1	Programmable Region 1 Block Size [1]	PREG1S1	'0'
2	Programmable Region 1 Block Size [2]	PREG1S2	'0'
3	Programmable Region 1 Starting Address [15]	PREG1A15	'0'
4	Programmable Region 1 Starting Address [16]	PREG1A16	'0'
5	Programmable Region 1 Starting Address [17]	PREG1A17	'0'
6	Programmable Region 1 Starting Address [18]	PREG1A18	'0'
7	Programmable Region 1 Starting Address [19]	PREG1A19	'0'
8	Programmable Region 1 Starting Address [20]	PREG1A20	'0'
9	Programmable Region 1 Starting Address [21]	PREG1A21	'0'
10	Programmable Region 1 Starting Address [22]	PREG1A22	'0'
11	Programmable Region 1 Starting Address [23]	PREG1A23	'0'
12	Programmable Region 1 Starting Address [24]	PREG1A24	'0'
13	Programmable Region 1 Starting Address [25]	PREG1A25	'0'
14	Programmable Region 1 Starting Address [26]	PREG1A26	'0'
15	Programmable Region 1 Starting Address [27]	PREG1A27	'0'

Bit **Description**

2:0 **Programmable Region 1 Block Size [2:0]:** These bits indicate the block size of programmable region 1. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 1 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 1 Starting Address [27:15]:** The programmable region 1 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 010**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.4 Programmable Region 2 Register (PR2)

Index: 111H

Bit	Description	Name	Reset State
0	Programmable Region 2 Block Size [0]	PREG2S0	'0'
1	Programmable Region 2 Block Size [1]	PREG2S1	'0'
2	Programmable Region 2 Block Size [2]	PREG2S2	'0'
3	Programmable Region 2 Starting Address [15]	PREG2A15	'0'
4	Programmable Region 2 Starting Address [16]	PREG2A16	'0'
5	Programmable Region 2 Starting Address [17]	PREG2A17	'0'
6	Programmable Region 2 Starting Address [18]	PREG2A18	'0'
7	Programmable Region 2 Starting Address [19]	PREG2A19	'0'
8	Programmable Region 2 Starting Address [20]	PREG2A20	'0'
9	Programmable Region 2 Starting Address [21]	PREG2A21	'0'
10	Programmable Region 2 Starting Address [22]	PREG2A22	'0'
11	Programmable Region 2 Starting Address [23]	PREG2A23	'0'
12	Programmable Region 2 Starting Address [24]	PREG2A24	'0'
13	Programmable Region 2 Starting Address [25]	PREG2A25	'0'
14	Programmable Region 2 Starting Address [26]	PREG2A26	'0'
15	Programmable Region 2 Starting Address [27]	PREG2A27	'0'

Bit **Description**

2:0 **Programmable Region 2 Block Size [2:0]:** These bits indicate the block size of programmable region 2. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 2 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 2 Starting Address [27:15]:** The programmable region 2 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 010**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.5 Programmable Region 3 Register (PR3)

Index: 112H

Bit	Description	Name	Reset State
0	Programmable Region 3 Block Size [0]	PREG3S0	'0'
1	Programmable Region 3 Block Size [1]	PREG3S1	'0'
2	Programmable Region 3 Block Size [2]	PREG3S2	'0'
3	Programmable Region 3 Starting Address [15]	PREG3A15	'0'
4	Programmable Region 3 Starting Address [16]	PREG3A16	'0'
5	Programmable Region 3 Starting Address [17]	PREG3A17	'0'
6	Programmable Region 3 Starting Address [18]	PREG3A18	'0'
7	Programmable Region 3 Starting Address [19]	PREG3A19	'0'
8	Programmable Region 3 Starting Address [20]	PREG3A20	'0'
9	Programmable Region 3 Starting Address [21]	PREG3A21	'0'
10	Programmable Region 3 Starting Address [22]	PREG3A22	'0'
11	Programmable Region 3 Starting Address [23]	PREG3A23	'0'
12	Programmable Region 3 Starting Address [24]	PREG3A24	'0'
13	Programmable Region 3 Starting Address [25]	PREG3A25	'0'
14	Programmable Region 3 Starting Address [26]	PREG3A26	'0'
15	Programmable Region 3 Starting Address [27]	PREG3A27	'0'

Bit **Description**

2:0 **Programmable Region 3 Block Size [2:0]:** These bits indicate the block size of programmable region 3. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 3 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 3 Starting Address [27:15]:** The programmable region 3 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 01**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.6 Programmable Region 4 Register (PR4)

Index: 113H

Bit	Description	Name	Reset State
0	Programmable Region 4 Block Size [0]	PREG4S0	'0'
1	Programmable Region 4 Block Size [1]	PREG4S1	'0'
2	Programmable Region 4 Block Size [2]	PREG4S2	'0'
3	Programmable Region 4 Starting Address [15]	PREG4A15	'0'
4	Programmable Region 4 Starting Address [16]	PREG4A16	'0'
5	Programmable Region 4 Starting Address [17]	PREG4A17	'0'
6	Programmable Region 4 Starting Address [18]	PREG4A18	'0'
7	Programmable Region 4 Starting Address [19]	PREG4A19	'0'
8	Programmable Region 4 Starting Address [20]	PREG4A20	'0'
9	Programmable Region 4 Starting Address [21]	PREG4A21	'0'
10	Programmable Region 4 Starting Address [22]	PREG4A22	'0'
11	Programmable Region 4 Starting Address [23]	PREG4A23	'0'
12	Programmable Region 4 Starting Address [24]	PREG4A24	'0'
13	Programmable Region 4 Starting Address [25]	PREG4A25	'0'
14	Programmable Region 4 Starting Address [26]	PREG4A26	'0'
15	Programmable Region 4 Starting Address [27]	PREG4A27	'0'

Bit **Description**

2:0 **Programmable Region 4 Block Size [2:0]:** These bits indicate the block size of programmable region 4. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 4 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 4 Starting Address [27:15]:** The programmable region 4 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 01**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.7 Programmable Region Control Register (PRC)

Index: 114H

Bit	Description	Name	Reset State
0	Programmable Region 1 Select [0]	PRGREG1_SEL0	'0'
1	Programmable Region 1 Select [1]	PRGREG1_SEL1	'0'
2	Programmable Region 2 Select [0]	PRGREG2_SEL0	'0'
3	Programmable Region 2 Select [1]	PRGREG2_SEL1	'0'
4	Programmable Region 3 Select [0]	PRGREG3_SEL0	'0'
5	Programmable Region 3 Select [1]	PRGREG3_SEL1	'0'
6	Programmable Region 4 Select [0]	PRGREG4_SEL0	'0'
7	Programmable Region 4 Select [1]	PRGREG4_SEL1	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

1:0 **Programmable Region 1 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

3:2 **Programmable Region 2 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

5:4 **Programmable Region 3 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

Bit	Description *(cont.)*
7:6	**Programmable Region 4 Select [1:0]:** **Bit [1:0]** — **Function** '00' — Disable '01' — Write-through '10' — Non-cacheable '11' — Reserved
15:8	Reserved

4.2.8 SMM Control Register (SMMC)

Index: 118H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	SMRAM KEN Disable	KDISSMMRAM	'0'
2	Enable 0G+20000H	EN23RMAB	'0'
3	Reserved		'0'
4	SMM D0000H-D7FFFH Select [0]	SMM_DL_SEL0	'0'
5	SMM D0000H-D7FFFH Select [1]	SMM_DL_SEL1	'0'
6	SMM D8000H-DFFFFH Select [0]	SMM_DH_SEL0	'0'
7	SMM D8000H-DFFFFH Select [1]	SMM_DH_SEL1	'0'
8	SMM E0000H-E7FFFH Select [0]	SMM_EL_SEL0	'0'
9	SMM E0000H-E7FFFH Select [1]	SMM_EL_SEL1	'0'
10	SMM E8000H-EFFFFH Select [0]	SMM_EH_SEL0	'0'
11	SMM E8000H-EFFFFH Select [1]	SMM_EH_SEL1	'0'
12	Swap SMM 2/3 Mapping	SWAP_23_MAP	'0'
13	Swap SMM D/E Mapping	SWAP_DE_MAP	'0'
14	Load SMI Handler into SMM RAM	LDSMIHLDER	'0'
15	Lock SMRAM Access in Normal Mode	SMIHLDERLOCK	'0'

Bit | **Description**

0 — Reserved

1 — **SMRAM KEN Disable:** '1'= KEN# will be held inactive (high) when SMI is active.

2 — **Enable 20000H-3FFFFH Remapped to A0000H-BFFFFH Physical Memory in SMM Mode:** '0' = enable, '1' = disable. This bit can be used to simplify the loading of SMI handler. BIOS must set this bit to '1' after the SMI handler is loaded. Refer to Section 3.2.7.2 on page 1-59 for more information.

NOTE: This bit can only be used if both L1 and L2 are disabled.

3 — Reserved

5:4 — **SMM D0000H-D7FFFH Select [1:0]:**

Bit [1:0]	Function
'00'	000D0000H-000D7FFFH is used as normal memory space.
'01'	Reserved
'10'	000D0000H-000D7FFFH is used as SMM space. (Remap to 000A0000H-000A7FFFH in physical DRAM space.)
'11'	Reserved

NOTE: When programmed to '10', 000D0000H-000D7FFFH will be automatically set to non-cacheable.

Bit	Description *(cont.)*
7:6	**SMM D8000H-DFFFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000D8000H-000DFFFFH is used as normal memory space. '01' — Reserved '10' — 000D8000H-000DFFFFH is used as SMM space. (Remap to 000A8000H-000AFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000D8000H-000DFFFFH will be automatically set to non-cacheable.
9:8	**SMM E0000H-E7FFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000E0000H-000E7FFFH is used as normal memory space. '01' — Reserved '10' — 000E0000H-000E7FFFH is used as SMM space. (Remap to 000B8000H-000BFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000E0000H-000E7FFFH will be automatically set to non-cacheable.
11:10	**SMM E8000H-EFFFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000E8000H-000EFFFFH is used as normal memory space. '01' — Reserved '10' — 000E8000H-000EFFFFH is used as SMM space. (Remap to 000B8000H-000BFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000E8000H-000EFFFFH will be automatically set to non-cacheable.
12	**Swap SMM 2/3 Mapping:** When set to '0', 00020000H–0002FFFFH region will be mapped to 000A0000H–000AFFFFH and 00030000H–0003FFFFH region will be mapped to 000B0000H–000BFFFFH. When set to '1', 00020000H–0002FFFFH region will be mapped to 000B0000H–000BFFFFH and 00030000H–0003FFFFH region will be mapped to 000A0000H–000AFFFFH. **NOTE:** This bit applies to Revision BB and later silicon revisions.
13	**Swap SMM D/E Mapping:** When set to '0', 000D0000H–000DFFFFH region will be mapped to 000A0000H–000AFFFFH and 000E0000H–000EFFFFH region will be mapped to 000B0000H–000BFFFFH. When set to '1', 000D0000H–000DFFFFH region will be mapped to 000B0000H–000BFFFFH and 000E0000H–000EFFFFH region will be mapped to 000A0000H–000AFFFFH. **NOTE:** This bit applies to Revision BB and later silicon revisions.

Bit	Description *(cont.)*
14	**Load SMI Handler into SMM RAM:** '1' = enable access to SMM RAM during normal cycle; '0' = disable access to SMM RAM during normal cycle. **NOTE:** SMI handler loading is directly achieved through A0000-BFFFF range.
15	**SMM RAM Access in Normal Mode Lock:** This bit provides an option to lock bit 14 in a disabled state, thereby prohibiting any further access to SMM RAM from normal mode. This bit can only be written once. Reading a '0' from this bit indicates that bit 14 is not locked. Reading a '1' from this bit indicates that bit 14 is locked to a disabled state.

4.2.9 Processor Control Register (PROC)

Index: 119H

Bit	Description	Name	Reset State
0	Cache Enable	KENEN	'0'
1	L1 Write-Back Enable	WB_ENABLE	'0'
2	Enable Processor Pipeline Mode	PIPELINEEN	'0'
3	Enable Linear Burst	LINEARBURST	'0'
4	Enable Combine of KEN# and INV Pins	EN_KEN_INV	'0'
5	Enable Write FIFO	WRFIFO_EN	'0'
6	INV is Asserted for Write Cycle Only	INV_ON_WR	'0'
7	Reserved		'0'
8	Disable FPU Error Clearing by F0H	DIS_FPUCLR_F0	'0'
9	Disable FPU Error Clearing by F1H	DIS_FPUCLR_F1	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**CACHE Enable:** When low, KEN# will be forced to an inactive state for all cycles. When high, KEN# will be asserted for all local memory cycles.
1	**L1 Write-Back Enable:** When low, WB_WT# will always be in write-through state. When high, WB_WT# will be in write-back state whenever it is possible.
2	**Enable Processor Pipeline Mode:** '0' = disable; '1' = enable.
3	**Enable Linear Burst:** '0' = toggle burst; '1' = linear burst. This bit should be set to the correct value before L1 and L2 cache is turned on.
4	**Enable Combination of KEN# and INV Pins:** When low, KEN# will only indicate cacheability of the cycle and CPU's INV input should be either pulled high or connected to W_R#. When high, KEN# and INV functionality will be combined into a single pin and KEN# should also be connected to CPU's INV pin.
5	**Enable Write FIFO:** '0' = disable; '1' = enable. When disabled, the write FIFO is forced to one level. When enabled, the write FIFO is forced to eight level.
6	**INV is Asserted for Write Cycle Only:** When '0', INV be asserted for both read and write cycles; when '1', INV will be asserted for write cycle only.
7	Reserved

Bit	Description *(cont.)*
8	**Disable FPU Error Clearing by Writing to I/O Port F0H:** Setting this bit to '0' will enable the clearing of FPU error by writing to I/O port F0H; setting it to '1' will disable it.
9	**Disable FPU Error Clearing by Writing to I/O Port F1H:** Setting this bit to '0' will enable the clearing of FPU error by writing to I/O port F1H; setting it to '1' will disable it.
15:10	Reserved

4.2.10 Write FIFO Control Register (WFIFOC)

Index: 11AH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	DRAM Read Reordering Enable	DRMRDREODEREN	'0'
4	PCI Read Reordering Enable	PCIRDREODEREN	'0'
5	PCI Write Buffering Select [0]	PCIWRBUFSEL0	'0'
6	PCI Write Buffering Select [1]	PCIWRBUFSEL1	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'1'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	Reserved
3	**DRAM Read Reordering Enable:** '0' = disable; '1' = enable. When this bit is set and there is a pending DRAM write cycle, a DRAM read operation will be preceded by a DRAM write operation. **NOTE:** This bit applies to Revision BB and later silicon.
4	**PCI Read Reordering Enable:** '0' = disable; '1' = enable. When this bit is set and there is a pending DRAM write cycle, a PCI read operation will be preceded by a DRAM write operation. **NOTE:** A PCI read operation will never get reordered around a pending PCI write cycle. This bit applies to Revision BB and later silicon.
6:5	**PCI Write Buffering Select[1:0]:** **Bit [1:0]** — **Function** 00 — Disable 01 — Post-write PCI IO Write Cycle Only 10 — Post-write PCI Memory Write Cycle Only 11 — Post-write All PCI Write Cycles
15:7	Reserved

4.2.11 PCI Control Register (PCIC)

Index: 11BH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	PCI Master-to-DRAM Burst Enable	PCI2DRM_BRST_EN	'0'
2	Reserved		'0'
3	Enable Optimized Address Transfer	ENOPT_ADDR_XFR	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	Reserved
1	**PCI Master-to-DRAM Burst Enable:** When this bit is set to '0', V1-LS will conduct a single PCI transfer only when the PCI Master is accessing the DRAM. When set to '1', V1-LS will attempt a burst to DRAM when PCI Master is accessing.
2	Reserved
3	**Enable Optimized Address Transfer Between V1-LS and V2-LS:** '0' = disable; '1' = enable. When enabled, the upper 24 bits of address are the same as the previous PCI address. By only allowing the transfer of the lower eight bits of address, a saving of at least one PCI clock is achieved.
15:4	Reserved

4.2.12 Clock Skew Adjust Register (CSA)

Index: 11CH

Bit	Description	Name	Reset State
0	L2CLK Skew Adjust [0]	L2CK_SKW_ADJ0	'0'
1	L2CLK Skew Adjust [1]	L2CK_SKW_ADJ1	'0'
2	L2CLK Skew Adjust [2]	L2CK_SKW_ADJ2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**L2CLK Skew Adjust [2:0]:** These bits are used to adjust the clock skew of L2CLK relative to the V1-LS core clock

Bit [2:0]	Delay
'000'	0.0 ns
'001'	+0.55 ns
'010'	+1.10 ns
'011'	+1.65 ns
'100'	-2.20 ns
'101'	-1.65 ns
'110'	-1.10 ns
'111'	-0.55 ns

15:3	Reserved

4.2.13 Bus Master and Snooping Control Register (SNOOPCTRL)

Index: 11DH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Early DRAM Cycle When PCI Master is Accessing DRAM	DISPCIM_ELY_DRM_CY	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
12:0	Reserved
13	**Early DRAM Cycle When PCI Master is Accessing DRAM:** '0' = enable; '1' = disable.
15:14	Reserved

4.2.14 Arbiter Control Register (ARBCTRL)

Index: 11EH

Bit	Description	Name	Reset State
0	Disable Preemptability of PCI Request/Grant [0]	DIS_REQGNT0	'0'
1	Disable Preemptability of PCI Request/Grant [1]	DIS_REQGNT1	'0'
2	Disable Preemptability of PCI Request/Grant [2]	DIS_REQGNT2	'0'
3	Disable Preemptability of PCI Request/Grant [3]	DIS_REQGNT3	'0'
4	SIO Request/Grant Source [0]	SIOREQGNT0	'0'
5	SIO Request/Grant Source [1]	SIOREQGNT1	'0'
6	Enable REQ2# as FLOAT_REQ# and GNT2# as FLOAT_GNT#	FLOAT_REQ_GNT	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Disable Preemptability of PCI Request/Grant 0:** '0' = preemptable; '1' = non-preemptable.
1	**Disable Preemptability of PCI Request/Grant 1:** '0' = preemptable; '1' = non-preemptable.
2	**Disable Preemptability of PCI Request/Grant 2:** '0' = preemptable; '1' = non-preemptable.
3	**Disable Preemptability of PCI Request/Grant 3:** '0' = preemptable; '1' = non-preemptable.
5:4	**SIO Request/Grant Source [1:0]:** These bits must be set to '01' for normal operation. **Bit [1:0]** — **SIO Request/Grant Source** '00' — None '01' — From BSER interface '10' — Reserved '11' — Reserved
6	**Enable REQ2# as FLOAT_REQ# and GNT2# as FLOAT_GNT#:** '0' = disable; '1' = enable.
15:7	Reserved

4.2.15 Docking Control Register (DOCKC)

Index: 11FH

Bit	Description	Name	Reset State
0	Tristate DOCK_PCIRST# and DOCK_PCICLK	TS_DOCK_SIGS	'0'
1	Reserved		'0'
2	Deassert DOCK_PCIRST#	DOCKRST_DASRT	'0'
3	Enable DOCK_PCICLK to Toggle	DOCK_CLK_EN	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	System Docked Indication	DOCKED	'0'

Bit	Description
0	**Tristate DOCK_PCIRST# and DOCK_PCICLK in Normal Operating Mode:** '0' = drive out DOCK_PCIRST# and DOCK_PCICLK; '1' = tristate DOCK_PCIRST# and DOCK_PCICLK.
1	Reserved
2	**Deassert DOCK_PCIRST#:** '0' = assert DOCK_PCIRST# in a low state; '1' = DOCK_PCIRST# will follow the state of PCIRST#.
3	**Enable DOCK_PCICLK to Toggle:** '0' = force DOCK_PCICLK low; '1' = DOCK_PCICLK will follow the state of PCICLK.
14:4	Reserved
15	**System Docked Indication:** This bit is used when the PCI floating method is used; it is set to '1' by SMI handler when the system is docked. This bit will be reset to '0' when it is previously set to '1' and FLOAT_REQ# is deasserted to indicate the completion of the undock procedure.

4.3 DRAM Registers

4.3.1 Shadow RAM Read Enable Control Register (SHADRC)

Index: 200H

Bit	Description	Name	Reset State
0	Local Memory Read Enable [0]	LMEMRDEN0	'0'
1	Local Memory Read Enable [1]	LMEMRDEN1	'0'
2	Local Memory Read Enable [2]	LMEMRDEN2	'0'
3	Local Memory Read Enable [3]	LMEMRDEN3	'0'
4	Local Memory Read Enable [4]	LMEMRDEN4	'0'
5	Local Memory Read Enable [5]	LMEMRDEN5	'0'
6	Local Memory Read Enable [6]	LMEMRDEN6	'0'
7	Local Memory Read Enable [7]	LMEMRDEN7	'0'
8	Local Memory Read Enable [8]	LMEMRDEN8	'0'
9	Local Memory Read Enable [9]	LMEMRDEN9	'0'
10	Local Memory Read Enable [10]	LMEMRDEN10	'0'
11	Local Memory Read Enable [11]	LMEMRDEN11	'0'
12	Local Memory Read Enable [12]	LMEMRDEN12	'0'
13	Local Memory Read Enable [13]	LMEMRDEN13	'0'
14	Local Memory Read Enable [14]	LMEMRDEN14	'0'
15	Local Memory Read Enable [15]	LMEMRDEN15	'0'

Bit	Description
0	**Local Memory C0000H-C3FFFH Read Enable:** '0' = disable; '1' = enable.
1	**Local Memory C4000H-C7FFFH Read Enable:** '0' = disable; '1' = enable.
2	**Local Memory C8000H-CBFFFH Read Enable:** '0' = disable; '1' = enable.
3	**Local Memory CC000H-CFFFFH Read Enable: '** 0' = disable; '1' = enable.
4	**Local Memory D0000H-D3FFFH Read Enable:** '0' = disable; '1' = enable.
5	**Local Memory D4000H-D7FFFH Read Enable:** '0' = disable; '1' = enable.
6	**Local Memory D8000H-DBFFFH Read Enable:** '0' = disable; '1' = enable.
7	**Local Memory DC000H-DFFFFH Read Enable:** '0' = disable; '1' = enable.
8	**Local Memory E0000H-E3FFFH Read Enable:** '0' = disable; '1' = enable.
9	**Local Memory E4000H-E7FFFH Read Enable:** '0' = disable; '1' = enable.
10	**Local Memory E8000H-EBFFFH Read Enable:** '0' = disable; '1' = enable.
11	**Local Memory EC000H-EFFFFH Read Enable:** '0' = disable; '1' = enable.

Bit	Description *(cont.)*
12	**Local Memory F0000H-F3FFFH Read Enable:** '0' = disable; '1' = enable.
13	**Local Memory F4000H-F7FFFH Read Enable:** '0' = disable; '1' = enable.
14	**Local Memory F8000H-FBFFFH Read Enable:** '0' = disable; '1' = enable.
15	**Local Memory FC000H-FFFFFH Read Enable:** '0' = disable; '1' = enable.

4.3.2 Shadow RAM Write Enable Control Register (SHADWC)

Index: 201H

Bit	Description	Name	Reset State
0	Local Memory Write Enable [0]	LMEMWREN0	'0'
1	Local Memory Write Enable [1]	LMEMWREN1	'0'
2	Local Memory Write Enable [2]	LMEMWREN2	'0'
3	Local Memory Write Enable [3]	LMEMWREN3	'0'
4	Local Memory Write Enable [4]	LMEMWREN4	'0'
5	Local Memory Write Enable [5]	LMEMWREN5	'0'
6	Local Memory Write Enable [6]	LMEMWREN6	'0'
7	Local Memory Write Enable [7]	LMEMWREN7	'0'
8	Local Memory Write Enable [8]	LMEMWREN8	'0'
9	Local Memory Write Enable [9]	LMEMWREN9	'0'
10	Local Memory Write Enable [10]	LMEMWREN10	'0'
11	Local Memory Write Enable [11]	LMEMWREN11	'0'
12	Local Memory Write Enable [12]	LMEMWREN12	'0'
13	Local Memory Write Enable [13]	LMEMWREN13	'0'
14	Local Memory Write Enable [14]	LMEMWREN14	'0'
15	Local Memory Write Enable [15]	LMEMWREN15	'0'

Bit	Description
0	**Local Memory C0000H-C3FFFH Write Enable:** '0' = disable; '1' = enable.
1	**Local Memory C4000H-C7FFFH Write Enable:** '0' = disable; '1' = enable.
2	**Local Memory C8000H-CBFFFH Write Enable:** '0' = disable; '1' = enable.
3	**Local Memory CC000H-CFFFFH Write Enable:** '0' = disable; '1' = enable.
4	**Local Memory D0000H-D3FFFH Write Enable:** '0' = disable; '1' = enable.
5	**Local Memory D4000H-D7FFFH Write Enable: '** 0' = disable; '1' = enable.
6	**Local Memory D8000H-DBFFFH Write Enable:** '0' = disable; '1' = enable.
7	**Local Memory DC000H-DFFFFH Write Enable:** '0' = disable; '1' = enable.
8	**Local Memory E0000H-E3FFFH Write Enable:** '0' = disable; '1' = enable.
9	**Local Memory E4000H-E7FFFH Write Enable:** '0' = disable; '1' = enable.
10	**Local Memory E8000H-EBFFFH Write Enable:** '0' = disable; '1' = enable.
11	**Local Memory EC000H-EFFFFH Write Enable:** '0' = disable; '1' = enable.
12	**Local Memory F0000H-F3FFFH Write Enable:** '0' = disable; '1' = enable.

Bit	Description *(cont.)*
13	**Local Memory F4000H-F7FFFH Write Enable:** '0' = disable; '1' = enable.
14	**Local Memory F8000H-FBFFFH Write Enable:** '0' = disable; '1' = enable.
15	**Local Memory FC000H-FFFFFH Write Enable:** '0' = disable; '1' = enable.

4.3.3 Bank 0 Control Register (B0C)

Index: 202H

Bit	Description	Name	Reset State
0	Bank 0 Starting Address [20]	B0A20	'0'
1	Bank 0 Starting Address [21]	B0A21	'0'
2	Bank 0 Starting Address [22]	B0A22	'0'
3	Bank 0 Starting Address [23]	B0A23	'0'
4	Bank 0 Starting Address [24]	B0A24	'0'
5	Bank 0 Starting Address [25]	B0A25	'0'
6	Bank 0 Starting Address [26]	B0A26	'0'
7	Bank 0 Starting Address [27]	B0A27	'0'
8	Reserved		'0'
9	Bank 0 DRAM Size [0]	B0S0	'0'
10	Bank 0 DRAM Size [1]	B0S1	'0'
11	Bank 0 DRAM Size [2]	B0S2	'0'
12	Column Address Bits for Bank 0 [0]	COLADR00	'0'
13	Column Address Bits for Bank 0 [1]	COLADR01	'0'
14	Column Address Bits for Bank 0 [2]	COLADR02	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 0 Starting Address [27:20]:** Starting address of bank 0.
8	Reserved
11:9	**Bank 0 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 0 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.4 Bank 1 Control Register (B1C)

Index: 203H

Bit	Description	Name	Reset State
0	Bank 1 Starting Address [20]	B1A20	'0'
1	Bank 1 Starting Address [21]	B1A21	'0'
2	Bank 1 Starting Address [22]	B1A22	'0'
3	Bank 1 Starting Address [23]	B1A23	'0'
4	Bank 1 Starting Address [24]	B1A24	'0'
5	Bank 1 Starting Address [25]	B1A25	'0'
6	Bank 1 Starting Address [26]	B1A26	'0'
7	Bank 1 Starting Address [27]	B1A27	'0'
8	Reserved		'0'
9	Bank 1 DRAM Size [0]	B1S0	'0'
10	Bank 1 DRAM Size [1]	B1S1	'0'
11	Bank 1 DRAM Size [2]	B1S2	'0'
12	Column Address Bits for Bank 1 [0]	COLADR10	'0'
13	Column Address Bits for Bank 1 [1]	COLADR11	'0'
14	Column Address Bits for Bank 1 [2]	COLADR12	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 1 Starting Address [27:20]:** Starting address of bank 1.
8	Reserved
11:9	**Bank 1 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 1 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.5 Bank 0/1 Timing Control Register (B01TC)

Index: 204H

Bit	Description	Name	Reset State
0	Bank 0 and Bank 1 RAS Precharge Time [0]	B01_TRP0	'1'
1	Bank 0 and Bank 1 RAS Precharge Time [1]	B01_TRP1	'1'
2	Bank 0 and Bank 1 RAS Precharge Time [2]	B01_TRP2	'1'
3	Bank 0 and Bank 1 RAS Address Hold Time [0]	B01_TRAH0	'1'
4	Bank 0 and Bank 1 RAS Address Hold Time [1]	B01_TRAH1	'1'
5	Bank 0 and Bank 1 CAS Address Setup Time [0]	B01_TASC0	'1'
6	Bank 0 and Bank 1 CAS Address Setup Time [1]	B01_TASC1	'1'
7	Bank 0 and Bank 1 CAS Address Hold Time	B01_TCAH	'1'
8	Bank 0 and Bank 1 CAS Precharge Time	B01_TCP	'1'
9	Bank 0 and Bank 1 CAS Read Pulse Width [0]	B01_TCAS_RD0	'1'
10	Bank 0 and Bank 1 CAS Read Pulse Width [1]	B01_TCAS_RD1	'1'
11	Bank 0 and Bank 1 CAS Read Pulse Width [2]	B01_TCAS_RD2	'1'
12	Bank 0 and Bank 1 CAS Write Pulse Width [0]	B01_TCAS_WR0	'1'
13	Bank 0 and Bank 1 CAS Write Pulse Width [1]	B01_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 0 and Bank 1 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 0 and Bank 1 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 0 and Bank 1 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 0 and Bank 1 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 0 and Bank 1 CAS Precharge** : '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 0 and Bank 1 CAS Read Pulse Width [2:0]:** **Bit [2:0]** — **Read Pulse Width** '000' — 0.5T (EDO or Burst EDO only) '001' — 1.0T '010' — 1.5T '011' — 2.0T '100' — 2.5T '101' — 3.0T '110' — 3.5T '111' — 4.0T
13:12	**Bank 0 and Bank 1 CAS Write Pulse Width [1:0]:** **Bit [1:0]** — **Write Pulse Width** '00' — 0.5T (EDO or Burst EDO only) '01' — 1.0T '10' — 1.5T '11' — 2.0T
15:14	Reserved

4.3.6 Bank 2 Control Register (B2C)

Index: 205H

Bit	Description	Name	Reset State
0	Bank 2 Starting Address [20]	B2A20	'0'
1	Bank 2 Starting Address [21]	B2A21	'0'
2	Bank 2 Starting Address [22]	B2A22	'0'
3	Bank 2 Starting Address [23]	B2A23	'0'
4	Bank 2 Starting Address [24]	B2A24	'0'
5	Bank 2 Starting Address [25]	B2A25	'0'
6	Bank 2 Starting Address [26]	B2A26	'0'
7	Bank 2 Starting Address [27]	B2A27	'0'
8	Reserved		'0'
9	Bank 2 DRAM Size [0]	B2S0	'0'
10	Bank 2 DRAM Size [1]	B2S1	'0'
11	Bank 2 DRAM Size [2]	B2S2	'0'
12	Column Address Bits for Bank 2 [0]	COLADR20	'0'
13	Column Address Bits for Bank 2 [1]	COLADR21	'0'
14	Column Address Bits for Bank 2 [2]	COLADR22	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 2 Starting Address [27:20]:** Starting address of bank 2.
8	Reserved
11:9	**Bank 2 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 2 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.7 Bank 3 Control Register (B3C)

Index: 206H

Bit	Description	Name	Reset State
0	Bank 3 Starting Address [20]	B3A20	'0'
1	Bank 3 Starting Address [21]	B3A21	'0'
2	Bank 3 Starting Address [22]	B3A22	'0'
3	Bank 3 Starting Address [23]	B3A23	'0'
4	Bank 3 Starting Address [24]	B3A24	'0'
5	Bank 3 Starting Address [25]	B3A25	'0'
6	Bank 3 Starting Address [26]	B3A26	'0'
7	Bank 3 Starting Address [27]	B3A27	'0'
8	Reserved		'0'
9	Bank 3 DRAM Size [0]	B3S0	'0'
10	Bank 3 DRAM Size [1]	B3S1	'0'
11	Bank 3 DRAM Size [2]	B3S2	'0'
12	Column Address Bits for Bank 3 [0]	COLADR30	'0'
13	Column Address Bits for Bank 3 [1]	COLADR31	'0'
14	Column Address Bits for Bank 3 [2]	COLADR32	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 3 Starting Address [27:20]:** Starting address of bank 3.
8	Reserved
11:9	**Bank 3 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 3 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.8 Bank 2/3 Timing Control Register (B23TC)

Index: 207H

Bit	Description	Name	Reset State
0	Bank 2 and Bank 3 RAS Precharge Time [0]	B23_TRP0	'1'
1	Bank 2 and Bank 3 RAS Precharge Time [1]	B23_TRP1	'1'
2	Bank 2 and Bank 3 RAS Precharge Time [2]	B23_TRP2	'1'
3	Bank 2 and Bank 3 RAS Address Hold Time [0]	B23_TRAH0	'1'
4	Bank 2 and Bank 3 RAS Address Hold Time [1]	B23_TRAH1	'1'
5	Bank 2 and Bank 3 CAS Address Setup Time [0]	B23_TASC0	'1'
6	Bank 2 and Bank 3 CAS Address Setup Time [1]	B23_TASC1	'1'
7	Bank 2 and Bank 3 CAS Address Hold Time	B23_TCAH	'1'
8	Bank 2 and Bank 3 CAS Precharge Time	B23_TCP	'1'
9	Bank 2 and Bank 3 CAS Read Pulse Width [0]	B23_TCAS_RD0	'1'
10	Bank 2 and Bank 3 CAS Read Pulse Width [1]	B23_TCAS_RD1	'1'
11	Bank 2 and Bank 3 CAS Read Pulse Width [2]	B23_TCAS_RD2	'1'
12	Bank 2 and Bank 3 CAS Write Pulse Width [0]	B23_TCAS_WR0	'1'
13	Bank 2 and Bank 3 CAS Write Pulse Width [1]	B23_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 2 and Bank 3 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 2 and Bank 3 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 2 and Bank 3 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 2 and Bank 3 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 2 and Bank 3 CAS Precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 2 and Bank 3 CAS Read Pulse Width [2:0]:**

Bit [2:0]	Read Pulse Width
'000'	0.5T (EDO or Burst EDO only)
'001'	1.0T
'010'	1.5T
'011'	2.0T
'100'	2.5T
'101'	3.0T
'110'	3.5T
'111'	4.0T

13:12	**Bank 2 and Bank 3 CAS Write Pulse Width [1:0]:**

Bit [1:0]	Write Pulse Width
'00'	0.5T (EDO or Burst EDO only)
'01'	1.0T
'10'	1.5T
'11'	2.0T

15:14	Reserved

4.3.9 Bank 4 Control Register (B4C)

Index: 208H

Bit	Description	Name	Reset State
0	Bank 4 Starting Address [20]	B4A20	'0'
1	Bank 4 Starting Address [21]	B4A21	'0'
2	Bank 4 Starting Address [22]	B4A22	'0'
3	Bank 4 Starting Address [23]	B4A23	'0'
4	Bank 4 Starting Address [24]	B4A24	'0'
5	Bank 4 Starting Address [25]	B4A25	'0'
6	Bank 4 Starting Address [26]	B4A26	'0'
7	Bank 4 Starting Address [27]	B4A27	'0'
8	Reserved		'0'
9	Bank 4 DRAM Size [0]	B4S0	'0'
10	Bank 4 DRAM Size [1]	B4S1	'0'
11	Bank 4 DRAM Size [2]	B4S2	'0'
12	Column Address Bits for Bank 4 [0]	COLADR40	'0'
13	Column Address Bits for Bank 4 [1]	COLADR41	'0'
14	Column Address Bits for Bank 4 [2]	COLADR42	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 4 Starting Address [27:20]:** Starting address of bank 4.
8	Reserved
11:9	**Bank 4 DRAM Size [2:0]:** **Bit [2:0]** — **DRAM Bank Size** '000' — 1 Mbyte '001' — 2 Mbyte '010' — 4 Mbyte '011' — 8 Mbyte '100' — 16 Mbyte '101' — 32 Mbyte '110' — 64 Mbyte '111' — Reserved
14:12	**Number of Column Address Bits for Bank 4 [2:0]:** **Bit [2:0]** — **Column Address** '000' — 8 bits '001' — 9 bits '010' — 10 bits '011' — 11 bits '100' — 12 bits All others — Reserved
15	Reserved

4.3.10 Bank 5 Control Register (B5C)

Index: 209H

Bit	Description	Name	Reset State
0	Bank 5 Starting Address [20]	B5A20	'0'
1	Bank 5 Starting Address [21]	B5A21	'0'
2	Bank 5 Starting Address [22]	B5A22	'0'
3	Bank 5 Starting Address [23]	B5A23	'0'
4	Bank 5 Starting Address [24]	B5A24	'0'
5	Bank 5 Starting Address [25]	B5A25	'0'
6	Bank 5 Starting Address [26]	B5A26	'0'
7	Bank 5 Starting Address [27]	B5A27	'0'
8	Reserved		'0'
9	Bank 5 DRAM Size [0]	B5S0	'0'
10	Bank 5 DRAM Size [1]	B5S1	'0'
11	Bank 5 DRAM Size [2]	B5S2	'0'
12	Column Address Bits for Bank 5 [0]	COLADR50	'0'
13	Column Address Bits for Bank 5 [1]	COLADR51	'0'
14	Column Address Bits for Bank 5 [2]	COLADR52	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 5 Starting Address [27:20]:** Starting address of bank 5.
8	Reserved
11:9	**Bank 5 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 5 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.11 Bank 4/5 Control Register (B45TC)

Index: 20AH

Bit	Description	Name	Reset State
0	Bank 4 and Bank 5 RAS Precharge Time [0]	B45_TRP0	'1'
1	Bank 4 and Bank 5 RAS Precharge Time [1]	B45_TRP1	'1'
2	Bank 4 and Bank 5 RAS Precharge Time [2]	B45_TRP2	'1'
3	Bank 4 and Bank 5 RAS Address Hold Time [0]	B45_TRAH0	'1'
4	Bank 4 and Bank 5 RAS Address Hold Time [1]	B45_TRAH1	'1'
5	Bank 4 and Bank 5 CAS Address Setup Time [0]	B45_TASC0	'1'
6	Bank 4 and Bank 5 CAS Address Setup Time [1]	B45_TASC1	'1'
7	Bank 4 and Bank 5 CAS Address Hold Time	B45_TCAH	'1'
8	Bank 4 and Bank 5 CAS Precharge Time	B45_TCP	'1'
9	Bank 4 and Bank 5 CAS Read Pulse Width [0]	B45_TCAS_RD0	'1'
10	Bank 4 and Bank 5 CAS Read Pulse Width [1]	B45_TCAS_RD1	'1'
11	Bank 4 and Bank 5 CAS Read Pulse Width [2]	B45_TCAS_RD2	'1'
12	Bank 4 and Bank 5 CAS Write Pulse Width [0]	B45_TCAS_WR0	'1'
13	Bank 4 and Bank 5 CAS Write Pulse Width [1]	B45_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 4 and Bank 5 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 4 and Bank 5 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 4 and Bank 5 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 4 and Bank 5 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 4 and Bank 5 CAS precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 4 and Bank 5 CAS Read Pulse Width [2:0]:** **Bit [2:0]** — **Read Pulse Width** '000' — 0.5T (EDO or Burst EDO only) '001' — 1.0T '010' — 1.5T '011' — 2.0T '100' — 2.5T '101' — 3.0T '110' — 3.5T '111' — 4.0T
13:12	**Bank 4 and Bank 5 CAS Write Pulse Width [1:0]:** **Bit [1:0]** — **Write Pulse Width** '00' — 0.5T (EDO or Burst EDO only) '01' — 1.0T '10' — 1.5T '11' — 2.0T
15:14	Reserved

4.3.12 Bank 6 Control Register (B6C)

Index: 20BH

Bit	Description	Name	Reset State
0	Bank 6 Starting Address [20]	B6A20	'0'
1	Bank 6 Starting Address [21]	B6A21	'0'
2	Bank 6 Starting Address [22]	B6A22	'0'
3	Bank 6 Starting Address [23]	B6A23	'0'
4	Bank 6 Starting Address [24]	B6A24	'0'
5	Bank 6 Starting Address [25]	B6A25	'0'
6	Bank 6 Starting Address [26]	B6A26	'0'
7	Bank 6 Starting Address [27]	B6A27	'0'
8	Reserved		'0'
9	Bank 6 DRAM Size [0]	B6S0	'0'
10	Bank 6 DRAM Size [1]	B6S1	'0'
11	Bank 6 DRAM Size [2]	B6S2	'0'
12	Column Address Bits for Bank 6 [0]	COLADR60	'0'
13	Column Address Bits for Bank 6 [1]	COLADR61	'0'
14	Column Address Bits for Bank 6 [2]	COLADR62	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 6 Starting Address [27:20]:** Starting address of bank 6.
8	Reserved
11:9	**Bank 6 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 6 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.13 Bank 7 Control Register (B7C)

Index: 20CH

Bit	Description	Name	Reset State
0	Bank 7 Starting Address [20]	B7A20	'0'
1	Bank 7 Starting Address [21]	B7A21	'0'
2	Bank 7 Starting Address [22]	B7A22	'0'
3	Bank 7 Starting Address [23]	B7A23	'0'
4	Bank 7 Starting Address [24]	B7A24	'0'
5	Bank 7 Starting Address [25]	B7A25	'0'
6	Bank 7 Starting Address [26]	B7A26	'0'
7	Bank 7 Starting Address [27]	B7A27	'0'
8	Reserved		'0'
9	Bank 7 DRAM Size [0]	B7S0	'0'
10	Bank 7 DRAM Size [1]	B7S1	'0'
11	Bank 7 DRAM Size [2]	B7S2	'0'
12	Column Address Bits for Bank 7 [0]	COLADR70	'0'
13	Column Address Bits for Bank 7 [1]	COLADR71	'0'
14	Column Address Bits for Bank 7 [2]	COLADR72	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 7 Starting Address [27:20]:** Starting address of bank 7.
8	Reserved
11:9	**Bank 7 DRAM Size [2:0]:** **Bit [2:0]** — **DRAM Bank Size** '000' — 1 Mbyte '001' — 2 Mbyte '010' — 4 Mbyte '011' — 8 Mbyte '100' — 16 Mbyte '101' — 32 Mbyte '110' — 64 Mbyte '111' — Reserved
14:12	**Number of Column Address Bits for Bank 7 [2:0]:** **Bit [2:0]** — **Column Address** '000' — 8 bits '001' — 9 bits '010' — 10 bits '011' — 11 bits '100' — 12 bits All others — Reserved
15	Reserved

4.3.14 Bank 6/7 Timing Control Register (B67TC)

Index: 20DH

Bit	Description	Name	Reset State
0	Bank 6 and Bank 7 RAS Precharge Time [0]	B67_TRP0	'1'
1	Bank 6 and Bank 7 RAS Precharge Time [1]	B67_TRP1	'1'
2	Bank 6 and Bank 7 RAS Precharge Time [2]	B67_TRP2	'1'
3	Bank 6 and Bank 7 RAS Address Hold Time [0]	B67_TRAH0	'1'
4	Bank 6 and Bank 7 RAS Address Hold Time [1]	B67_TRAH1	'1'
5	Bank 6 and Bank 7 CAS Address Setup Time [0]	B67_TASC0	'1'
6	Bank 6 and Bank 7 CAS Address Setup Time [1]	B67_TASC1	'1'
7	Bank 6 and Bank 7 CAS Address Hold Time	B67_TCAH	'1'
8	Bank 6 and Bank 7 CAS Precharge Time	B67_TCP	'1'
9	Bank 6 and Bank 7 CAS Read Pulse Width [0]	B67_TCAS_RD0	'1'
10	Bank 6 and Bank 7 CAS Read Pulse Width [1]	B67_TCAS_RD1	'1'
11	Bank 6 and Bank 7 CAS Read Pulse Width [2]	B67_TCAS_RD2	'1'
12	Bank 6 and Bank 7 CAS Write Pulse Width [0]	B67_TCAS_WR0	'1'
13	Bank 6 and Bank 7 CAS Write Pulse Width [1]	B67_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 6 and Bank 7 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 6 and Bank 7 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 6 and Bank 7 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 6 and Bank 7 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 6 and Bank 7 CAS Precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 6 and Bank 7 CAS Read Pulse Width [2:0]:** **Bit [2:0]** — **Read Pulse Width** '000' — 0.5T (EDO or Burst EDOt only) '001' — 1.0T '010' — 1.5T '011' — 2.0T '100' — 2.5T '101' — 3.0T '110' — 3.5T '111' — 4.0T
13:12	**Bank 6 and Bank 7 CAS Write Pulse Width [1:0]:** **Bit [1:0]** — **Write Pulse Width** '00' — 0.5T (EDO or Burst EDO only) '01' — 1.0T '10' — 1.5T '11' — 2.0T
15:14	Reserved

4.3.15 DRAM Configuration Register 1(DCONF1)

Index: 20EH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	DRAM Inactive Time-out [0]	DRAM_INAT_TO0	'0'
4	DRAM Inactive Time-out [1]	DRAM_INAT_TO1	'0'
5	DRAM Inactive Time-out [2]	DRAM_INAT_TO2	'0'
6	DRAM Auto-Detect Mode [0]	DRAM_AUTODET0	'0'
7	DRAM Auto-Detect Mode [1]	DRAM_AUTODET1	'0'
8	Fast Cacheless Read Enable	FSTL2DISRDEN	'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	Reserved
5:3	**DRAM Inactive Time-out [2:0]:** **Bit [2:0]** — **Duration (T = CPU Bus Clock Frequency)** '000' — Never '001' — 8 T '010' — 32 T '011' — 128 T '100' — 512 T '101' — Reserved '110' — Reserved '111' — Immediate
7:6	**DRAM Auto-Detect Mode [1:0]:** **Bit [1:0]** — **Function** '00' — Normal mode '01' — Setup for Auto-Detect. Set before auto-detect algorithm. '10' — Reserved '11' — Auto-Detect read mode
8	**Fast Cacheless Read Enable:** '0' = fast cacheless read is disabled; '1' = fast cacheless read feature is enabled. **NOTE:** L2 cache must be disabled and L2 read lead-off must be set to 2T.
15:9	Reserved

4.3.16 DRAM Configuration Register 2 (DCONF2)

Index: 20FH

Bit	Description	Name	Reset State
0	Bank 0 Enable	BANK0_32EN	'1'
1	Bank 1 Enable	BANK1_32EN	'0'
2	Bank 2 Enable	BANK2_32EN	'0'
3	Bank 3 Enable	BANK3_32EN	'0'
4	Bank 4 Enable	BANK4_32EN	'0'
5	Bank 5 Enable	BANK5_32EN	'0'
6	Bank 6 Enable	BANK6_32EN	'0'
7	Bank 7 Enable	BANK7_32EN	'0'
8	Bank 0 and Bank 1 as a 64-bit Bank	BANK01_64EN	'0'
9	Bank 2 and Bank 3 as a 64-bit Bank	BANK23_64EN	'0'
10	Bank 4 and Bank 5 as a 64-bit Bank	BANK45_64EN	'0'
11	Bank 6 and Bank 7 as a 64-bit Bank	BANK67_64EN	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Bank 0 Enable:** '0' = disable; '1' = enable. When enabled, bank 0 will operate as a 32-bit bank.
1	**Bank 1 Enable:** '0' = disable; '1' = enable. When enabled, bank 1 will operate as a 32-bit bank.
2	**Bank 2 Enable:** '0' = disable; '1' = enable. When enabled, bank 2 will operate as a 32-bit bank.
3	**Bank 3 Enable:** '0' = disable; '1' = enable. When enabled, bank 3 will operate as a 32-bit bank.
4	**Bank 4 Enable:** '0' = disable; '1' = enable . When enabled, bank 4 will operate as a 32-bit bank.
5	**Bank 5 Enable:** '0' = disable; '1' = enable . When enabled, bank 5 will operate as a 32-bit bank.
6	**Bank 6 Enable:** 0 = disable; '1' = enable. When enabled, bank 6 will operate as a 32-bit bank.
7	**Bank 7 Enable:** '0' = disable; '1' = enable. When enabled, bank 7 will operate as a 32-bit bank.

Bit	Description *(cont.)*
8	**Bank 0 and Bank 1 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 0 and bank 1 will be used as a single 64-bit bank, (b) bit [1:0] above will be ignored, (c) all DRAM parameters will be from bank 0, and (d) the DRAM bank size programmed in bank 0 will be doubled.
9	**Bank 2 and Bank 3 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 2 and bank 3 will be used as a single 64-bit bank, (b) bit [3:2] above will be ignored, (c) all DRAM parameters will be from bank 2, and (d) the DRAM bank size programmed in bank 2 will be doubled.
10	**Bank 4 and Bank 5 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 4 and bank 5 will be used as a single 64-bit bank, (b) bit [5:4] above will be ignored, (c) all DRAM parameters will be from bank 4, and (d) the DRAM bank size programmed in bank 4 will be doubled.
11	**Bank 6 and Bank 7 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 6 and bank 7 will be used as a single 64-bit bank, (b) bit [7:6] above will be ignored, (c) all DRAM parameters will be from bank 6, and (d) the DRAM bank size programmed in bank 6 will be doubled.
15:12	Reserved

4.3.17 DRAM Configuration Register 3 (DCONF3)

Index: 210H

Bit	Description	Name	Reset State
0	Bank 0 DRAM Type [0]	B0DRMTYPE0	'0'
1	Bank 0 DRAM Type [1]	B0DRMTYPE1	'0'
2	Bank 1 DRAM Type [0]	B1DRMTYPE0	'0'
3	Bank 1 DRAM Type [1]	B1DRMTYPE1	'0'
4	Bank 2 DRAM Type [0]	B2DRMTYPE0	'0'
5	Bank 2 DRAM Type [1]	B2DRMTYPE1	'0'
6	Bank 3 DRAM Type [0]	B3DRMTYPE0	'0'
7	Bank 3 DRAM Type [1]	B3DRMTYPE1	'0'
8	Bank 4 DRAM Type [0]	B4DRMTYPE0	'0'
9	Bank 4 DRAM Type [1]	B4DRMTYPE1	'0'
10	Bank 5 DRAM Type [0]	B5DRMTYPE0	'0'
11	Bank 5 DRAM Type [1]	B5DRMTYPE1	'0'
12	Bank 6 DRAM Type [0]	B6DRMTYPE0	'0'
13	Bank 6 DRAM Type [1]	B6DRMTYPE1	'0'
14	Bank 7 DRAM Type [0]	B7DRMTYPE0	'0'
15	Bank 7 DRAM Type [1]	B7DRMTYPE1	'0'

Bit	Description
1:0	**Bank 0 DRAM Type [1:0]:**

Bit [1:0]	DRAM Type
'00'	Standard
'01'	EDO
'10'	Burst EDO
'11'	Reserved

Bit	Description
3:2	**Bank 1 DRAM Type [1:0]:**

Bit [1:0]	DRAM Type
'00'	Standard
'01'	EDO
'10'	Burst EDO
'11'	Reserved

Bit	Description
5:4	**Bank 2 DRAM Type [1:0]:**

Bit [1:0]	DRAM Type
'00'	Standard
'01'	EDO
'10'	Burst EDO
'11'	Reserved

Bit	Description *(cont.)*	
7:6	**Bank 3 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
9:8	**Bank 4 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
11:10	**Bank 5 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
13:12	**Bank 6 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
15:14	**Bank 7 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved

4.3.18 DRAM Refresh Control Register (DRFSHC)

Index: 211H

Bit	Description	Name	Reset State
0	DRAM Refresh Scheme	DRAM_RF_NLYRF	'0'
1	RAS Precharge Time for Refresh Cycles [0]	RFRPRE0	'0'
2	RAS Precharge Time for Refresh Cycles [1]	RFRPRE1	'0'
3	RAS Pulse Width for Refresh Cycles [0]	RFRPW0	'0'
4	RAS Pulse Width for Refresh Cycles [1]	RFRPW1	'0'
5	Refresh Period [0]	REFRPRD0	'1'
6	Refresh Period [1]	REFRPRD1	'0'
7	Refresh Period [2]	REFRPRD2	'1'
8	Reserved		'0'
9	Reserved		'0'
10	Self-Refresh Enable	SLFREFEN	'0'
11	Reserved		'0'
12	Refresh Stagger Select [0]	REF_STAG_SEL0	'1'
13	Refresh Stagger Select [1]	REF_STAG_SEL1	'1'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**DRAM Refresh Scheme:** '0' = CAS-before-RAS refresh; '1' = RAS-only refresh.
2:1	**RAS Precharge Time for Refresh Cycles [1:0]:**

Bit [1:0]	RAS Precharge Time
'00'	5T
'01'	4T
'10'	3T
'11'	2T

Bit	Description
4:3	**RAS Pulse Width for Refresh Cycles [1:0]:**

Bit [1:0]	RAS Pulse Width Time
'00'	6T
'01'	5T
'10'	4T
'11'	3T

Bit	Description *(cont.)*
7:5	**Refresh Period:** These bits determine the refresh period for local DRAM. **Bit [2:0]** — **Refresh Period** '000' — 3.75 µs '001' — 7.5 µs '010' — 15 µs '011' — 30 µs '100' — 120 µs '101' — Stopped All Others — Reserved
9:8	Reserved
10	**Self-Refresh Enable:** When high, this bit enables self-refresh mode during Suspend Mode.
11	Reserved
13:12	**Refresh Stagger Select [1:0]:** **Bit [1:0]** — **Function** '00' — No staggering '01' — Reserved '10' — Stagger the active edge of RAS '11' — Stagger both edges of RAS
15:14	Reserved

4.3.19 Burst EDO Control Register (BEDOC)

Index: 212H

Bit	Description	Name	Reset State
0	Enable Burst EDO WCBR Configuration Cycle	ENWCBR_CONFIG	'0'
1	DRAM Bank Configuration Select [0]	BANK_CONGIG0	'0'
2	DRAM Bank Configuration Select [1]	BANK_CONGIG1	'0'
3	Trigger WCBR Configuration Cycle	TRIG_WCBR	
4	MA Setting During WCBR Cycle [0]	WCBR_MA0	'1'
5	MA Setting During WCBR Cycle [1]	WCBR_MA1	'0'
6	MA Setting During WCBR Cycle [2]	WCBR_MA2	'0'
7	MA Setting During WCBR Cycle [3]	WCBR_MA3	'0'
8	MA Setting During WCBR Cycle [4]	WCBR_MA4	'0'
9	MA Setting During WCBR Cycle [5]	WCBR_MA5	'1'
10	MA Setting During WCBR Cycle [6]	WCBR_MA6	'0'
11	MA Setting During WCBR Cycle [7]	WCBR_MA7	'0'
12	MA Setting During WCBR Cycle [8]	WCBR_MA8	'0'
13	MA Setting During WCBR Cycle [9]	WCBR_MA9	'0'
14	MA Setting During WCBR Cycle [10]	WCBR_MA10	'0'
15	MA Setting During WCBR Cycle [11]	WCBR_MA11	'0'

Bit — **Description**

0 — **Enable Burst EDO Write CAS-Before-RAS (WCBR) Configuration Cycle:** '0' = disable; '1' = enable.

2:1 — **DRAM Bank Configuration Select [1:0]:**

Bit [1:0]	DRAM Bank
'00'	Bank 0/1
'01'	Bank 2/3
'10'	Bank 4/5
'11'	Bank 6/7

NOTE: CASA[3:0]# and CASB[3:0]# are enabled, depending on the settings in Registers DCONF2 and DCONF3. Only banks set to burst EDO DRAM type will have CAS asserted.

3 — **Trigger WCBR Configuration Cycle:** A '0' to '1' transition generates a WCBR/refresh cycle. If bit 0 (ENWCBR_CONFIG) is set to '1', MA[11:0] is driven to the value programmed in bit [15:4] of this register and WE# is asserted during a CAS-before-RAS cycle. If bit 0 (ENWCBR_CONFIG) is set to '0', a normal refresh cycle is generated.

Bit	Description *(cont.)*
15:4	**MA Setting During WCBR Cycle [11:0]:** MA[0] and MA[11] are mapped to bits 4 and 15 respectively. DRAM vendors currently define MA[0] as selecting toggle mode (Pentium processor) versus linear burst mode. MA[11:1] must be 00000010000. Thus, for linear burst mode, the setting is 020H and for toggle mode, the setting is 021H.

4.4 Power Management Control Registers

4.4.1 Clock Control Register

Index: 300H

Bit	Description	Name	Reset State
0	PCI Clock Divisor During Idle [0]	PCI_IDLE_DIV0	'0'
1	PCI Clock Divisor During Idle [1]	PCI_IDLE_DIV1	'0'
2	Reserved		'0'
3	Reserved		'0'
4	PCI Idle Count [0]	PCI_IDLE_CNT0	'0'
5	PCI Idle Count [1]	PCI_IDLE_CNT1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Enable PCI Clock to Full Speed When PCI Request or Grant is Detected	MSTR_FULLSPD	'0'
9	Enable PCI Clock to Full Speed When PCI LOCK# is Detected	CKFUL_LOCKEN	'0'
10	Reserved		'0'
11	Enable CLKRUN# Method for PCI Clock Control	EN_CLKRUN	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Enable Modular Clocking on V2 Clock	EN_MODCLKV2	'0'

Bit **Description**

1:0 **PCI Clock Divisor During Idle [1:0]:** When PCI is detected to be idle, the PCI clock will be divided by the value programmed in this register.

Bit [1:0]	Divisor
'00'	1
'01'	2
'10'	32
'11'	256

3:2 Reserved

5:4 **PCI Idle Count [1:0]:** When PCI is idle, the PCI idle counter will start counting from zero.

Bit [1:0]	Idle Count (PCI Clocks)
'00'	Immediate
'01'	8
'10'	32
'11'	256

7:6 Reserved

Bit	Description *(cont.)*
8	**Enable PCI Clock to go Back to Full Speed When PCI Request or Grant is Detected:** '0' = disable; '1' = enable.
9	**Enable PCI Clock to go Back to Full Speed When PCI LOCK# is Detected:** '0' = disable; '1' = enable.
10	Reserved
11	**Enable CLKRUN# Method for PCI Clock Control:** '0' = use PicoPower's proprietary PCI clock control method; '1' = use PCI Mobile Design Guide's CLKRUN# pin method.
14:12	Reserved
15	**Enable Modular Clocking on V2 Clock:** '0' = disable; '1' = enable. When enabled, modular clocking for V2 clock will take effect every time the processor is in STOP GRANT state. Upon detection of DRAM refresh, PCI master request, etc. during STOP GRANT state, V2 clock will be restarted.

4.4.2 Clock Throttling Period Control Register (CTPC)

Index: 301H

Bit	Description	Name	Reset State
0	Clock Throttling Period Select [0]	CT_PERIOD0	'0'
1	Clock Throttling Period Select [1]	CT_PERIOD1	'0'
2	Clock Throttling Period Select [2]	CT_PERIOD2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**Clock Throttling Period Select [2:0]:** Modulation period = CPU clock period× divisor. Modulation period is the period within which STPCLK# will throttle. **NOTE:** T = CPU bus frequency period.

Bit [2:0]	Modulation Period
'000'	800T
'001'	1600T
'010'	3200T
'011'	6400T
'100'	12800T
'101'	25600T
'110'	102400T
'111'	409600T

15:3	Reserved

4.4.3 Conserve Clock Throttling Ratio/Control Register (CON-CTRC)

Index: 302H

Bit	Description	Name	Reset State
0	Conserve Clock Throttling Ratio [0]	CONSERVE_CTR0	'0'
1	Conserve Clock Throttling Ratio [1]	CONSERVE_CTR1	'0'
2	Conserve Clock Throttling Ratio [2]	CONSERVE_CTR2	'0'
3	Conserve Clock Throttling Ratio [3]	CONSERVE_CTR3	'0'
4	Conserve Clock Throttling Enable	CONSERVE_ CTR_EN	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

3:0 — **Conserve Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU. The accuracy of the duty cycle is within ±1.25%.

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

4 — **Conserve Clock Throttling Enable:** '0' = disable; '1' = enable.

15:5 — Reserved

4.4.4 Heat Regulator Clock Throttling Ratio / Control Register (HR-CTRC)

Index: 303H

Bit	Description	Name	Reset State
0	Heat Regulator Clock Throttling Ratio [0]	HR_CTR0	'0'
1	Heat Regulator Clock Throttling Ratio [1]	HR_CTR1	'0'
2	Heat Regulator Clock Throttling Ratio [2]	HR_CTR2	'0'
3	Heat Regulator Clock Throttling Ratio [3]	HR_CTR3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	THERM Input Enable	THERM_EN	'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Heat Regulator Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU. The accuracy of the duty cycle is within ±1.25%

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

11:4 Reserved

12 **THERM Input Enable:** This bit uses the THERM input to indicate asystem or CPU overheat condition. When this bit is set high, an active level on the THERM input pin will force STPCLK# to throttle according to the setting of HR_CTRC Bit [3:0].

15:13 Reserved

4.4.5 Doze/Sleep Mode Clock Throttling Ratio/Control Register (DS-CTRC)

Index: 304H

Bit	Description	Name	Reset State
0	Doze/Sleep Clock Throttling Ratio [0]	DS_CTR0	'0'
1	Doze/Sleep Clock Throttling Ratio [1]	DS_CTR1	'0'
2	Doze/Sleep Clock Throttling Ratio [2]	DS_CTR2	'0'
3	Doze/Sleep Clock Throttling Ratio [3]	DS_CTR3	'0'
4	Doze Mode Clock Throttling Enable	DOZE_CTR_EN	'0'
5	Sleep Mode Clock Throttling Enable [0]	SLP_CTR_EN0	'0'
6	Sleep Mode Clock Throttling Enable [1]	SLP_CTR_EN1	'0'
7	Sleep Mode Clock Throttling Enable [2]	SLP_CTR_EN2	'0'
8	STPCLK Release Latency [0]	STPCLK_LAT0	'0'
9	STPCLK Release Latency [1]	STPCLK_LAT1	'0'
10	STPCLK Release Latency [2]	STPCLK_LAT2	'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Doze/Sleep Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

4 **Doze Mode Clock Throttling Enable:** When set to '0', Doze mode will not enable clock throttling. When set to '1', Doze mode will enable clock throttling in the ratio set in DS_CTRC Bit [3:0]

Bit	Description *(cont.)*
7:5	**Sleep Mode Clock Throttling Enable [2:0] :** **Bit [2:0]** — **Function** '000' — Disable clock throttling in Sleep mode '001' — Enable clock throttling in ratio set in DS_CTRC Bit [3:0] in Sleep mode '010' — Enable LessStop mode (CPU Stop Grant state) in Sleep mode '011' — Enable MoreStop mode (CPU Stop Clock state) in Sleep mode '100' — Enable Deep_Sleep mode (MoreStop and high speed oscillator off; only 32 kHz is running.) **NOTE:** For Deep Sleep mode, if high speed oscillator is off, make sure that all devices can tolerate unstable oscillation when the clock oscillator is restarted. It is recommended that the power-down pin of the clock synthesizer chip be used to enable or disable the clock output so that its output clocks will always restart with stable frequency.
10:8	**STPCLK Release Latency (PLL Stabilization Delay) [2:0]:** This parameter defines the delay between restarting the CPU clock and deasserting STPCLK. This parameter applies only during Sleep mode when MoreStop is enabled, or when resuming from Deep Sleep mode. **Bit [2:0]** — **Delay** '000' — 0 s '001' — 1 µs '010' — 45 µs '011' — 1 ms '100' — 2 ms All Others — Reserved
15:11	Reserved

4.4.6 Wake/SMI Source Register (WSS)

Index: 310H

Bit	Description	Name	Reset State
0	System Management Interrupt Source [0]	SMISRC0	'0'
1	System Management Interrupt Source [1]	SMISRC1	'0'
2	System Management Interrupt Source [2]	SMISRC2	'0'
3	System Management Interrupt Source [3]	SMISRC3	'0'
4	System Management Interrupt Source [4]	SMISRC4	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Wake-Up Source [0]	WAKEUP_SRC0	'0'
9	Wake-Up Source [1]	WAKEUP_SRC1	'0'
10	Wake-Up Source [2]	WAKEUP_SRC2	'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

4:0 **System Management Interrupt Source [4:0]:**

Bit [4:0]	Source
00H	None
01H	Primary Activity
02H	I/O trap
03H	Device Timers Time-out
04H	Doze Time-out
05H	Sleep Time-out
06H	Suspend Time-out
07H	GP Timer Compare
08H	SWTCH input toggling
09H	Reserved
0AH	WAKE0 input toggling
0BH	WAKE1 input toggling
0CH	EXTACT0 toggling
0DH	Reserved
0EH	Rescheduled SMI
0FH	Software SMI
10H	V3-LS INT SMI
1FH	Clear SMI source
All Others	Reserved

NOTE: These bits are read only; they should be cleared by writing a 1FH to bit [4:0]. To avoid losing any nested SMIs, the SMM handler should always clear the SMI group by writing a 1FH to bit [4:0] of WSS, then clear the corresponding flag in the Activity Registers (AFR1 and AFR2).

7:5 Reserved

Bit	Description *(cont.)*
10:8	**Wake-Up Source [2:0]:** **Bit [2:0]** — **Source** 0H — None 1H — RING 2H — SWTCH 3H — GP Timer Compare 4H — WAKE0 5H — WAKE1 6H — Reserved 7H — Clear Wake Source **NOTE:** These bits are read only; they should be cleared after reading by a write of 7H to bit [10:8].
15:11	Reserved

4.4.7 Power Management Timer Status Register (PMTS)

Index: 311H

Bit	Description	Name	Reset State
0	Doze Time-out Status	DOZE_TO	'0'
1	Sleep Time-out Status	SLEEP_TO	'0'
2	Suspend Time-out Status	SUSPEND_TO	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Doze Time-out Status:** When high, this bit indicates that a doze Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
1	**Sleep Time-out Status:** When high, this bit indicates that a sleep Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
2	**Suspend Time-out Status:** When high, this bit indicates that a suspend Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
15:3	Reserved

4.4.8 Power Management Pin Status Register (PMPS)

Index: 312H

Bit	Description	Name	Reset State
0	WAKE0 Pin Status	WAKE0_ST	X
1	WAKE1 Pin Status	WAKE1_ST	X
2	EXTACT0 Pin Status	EXTACT0_ST	X
3	Reserved		'0'
4	RING Pin Status	RING_ST	X
5	SWTCH Pin Status	SWTCH_ST	X
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**WAKE0 Pin Status:** This bit reflects the status of WAKE0 input pin. This bit is read only.
1	**WAKE1 Pin Status:** This bit reflects the status of WAKE1 input pin. This bit is read only.
2	**EXTACT0 Pin Status:** This bit reflects the current status of EXTACT0 input pin. This bit is read only.
3	Reserved
4	**RING Pin Status:** This bit reflects the current status of RING input pin. This bit is read only.
5	**SWTCH Pin Status:** This bit reflects the current status of SWTCH input pin. This bit is read only.
15:6	Reserved

4.4.9 Wake Mask Control Register (WMC)

Index: 313H

Bit	Description	Name	Reset State
0	Mask WAKE0 From Resume	WMSK_WAKE0	'1'
1	Mask WAKE1 From Resume	WMSK_WAKE1	'1'
2	Mask SWTCH From Resume	WMSK_SWTCH	'0'
3	Mask RING From Resume	WMSK_RING	'1'
4	Mask GP Timer Compare From Resume	WMSK_GPTMR	'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask WAKE0 from Resume:** When high, the WAKE0 input toggling will not trigger a wake-up from suspend mode; when low it will.
1	**Mask WAKE1 from Resume:** When high, the WAKE1 input toggling will not trigger a wake-up from suspend mode; when low it will.
2	**Mask SWTCH from Resume:** When high, the SWTCH input toggling will not trigger a wake-up from suspend mode; when low it will.
3	**Mask RING from Resume:** When high, the RING input toggling will not trigger a wake-up from suspend mode; when low it will.
4	**Mask GP Timer Compare from Resume:** When high, a compare on the GP Timer will not trigger a wake-up from suspend mode; when low it will.
15:5	Reserved

NOTE: WAKE0/1, SWTCH, and RNG toggling can be selected through EDC Register (index 354H).

4.4.10 Activity Flag Register 1 (AFR1)

Index: 314H

Bit	Description	Name	Reset State
0	Video Active	VID_ACTV	'0'
1	Hard Disk 1 Active	HD1_ACTV	'0'
2	Hard Disk 2 Active	HD2_ACTV	'0'
3	Floppy Disk Active	FLP_ACTV	'0'
4	Keyboard Active	KB_ACTV	'0'
5	Serial I/O 1 Active	SIO1_ACTV	'0'
6	Serial I/O 2 Active	SIO2_ACTV	'0'
7	Parallel I/O Active	PIO_ACTV	'0'
8	HOLD Active	HOLD_ACTV	'0'
9	Reserved		'0'
10	Programmable Range Monitor Active [0]	PROG_ACTV0	'0'
11	Programmable Range Monitor Active [1]	PROG_ACTV1	'0'
12	Programmable Range Monitor Active [2]	PROG_ACTV2	'0'
13	Programmable Range Monitor Active [3]	PROG_ACTV3	'0'
14	Programmable Range Monitor Active [4]	PROG_ACTV4	'0'
15	Programmable Range Monitor Active [5]	PROG_ACTV5	'0'

Bit	Description
0	**Video Active:** When video access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect
1	**Hard Disk 1 Active:** When hard disk 1 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
2	**Hard Disk 2 Active:** When hard disk 2 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
3	**Floppy Disk Active:** When floppy disk access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
4	**Keyboard Active:** When keyboard access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
5	**Serial I/O 1 Active:** When serial I/O 1 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
6	**Serial I/O 2 Active:** When serial I/O 2 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
7	**Parallel I/O Active:** When parallel I/O access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.

Bit	Description *(cont.)*
8	**HOLD Active:** When HOLD is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
9	Reserved
15:10	**Programmable Range Monitor Active [5:0]:** When programmable range [5:0] access is detected, the corresponding bits will be set high. Writing '0' to these bits will clear it; writing '1' will have no effect.

4.4.11 Activity Flag Register 2 (AFR2)

Index: 315H

Bit	Description	Name	Reset State
0	V3-LS Active	V3-LS_ACTV	'0'
1	Reserved		'0'
2	RING Active	RING_ACTV	'0'
3	SWTCH Active	SWTCH_ACTV	'0'
4	WAKE0 Active	WAKE0_ACTV	'0'
5	WAKE1 Active	WAKE1_ACTV	'0'
6	EXTACT0 Active	EXT0_ACTV	'0'
7	FLOAT_REQ# Active	FLOAT_REQ_ACTV	'0'
8	Device Timer [0] Time-out	DEV_TMRTO0	'0'
9	Device Timer [1] Time-out	DEV_TMRTO1	'0'
10	Device Timer [2] Time-out	DEV_TMRTO2	'0'
11	Device Timer [3] Time-out	DEV_TMRTO3	'0'
12	Device Timer [4] Time-out	DEV_TMRTO4	'0'
13	Device Timer [5] Time-out	DEV_TMRTO5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**V3-LS Active:** When unmasked PAIRQ from V3-LS is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
1	Reserved
2	**RING Active:** When RING toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
3	**SWTCH Active:** When SWTCH toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
4	**WAKE0 Active:** When WAKE0 toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
5	**WAKE1 Active:** When WAKE1 toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
6	**EXTACT0 Active:** When EXTACT0 toggling is detected, this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
7	**FLOAT_REQ# Active:** When FLOAT_REQ# is detected, this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.

Bit	Description *(cont.)*
13:8	**Device Timer [5:0] Time-out:** When the device timer [5:0] time-out occurs, these bits will be set high. These bits remain high until a reset of timer occurs or until it is written low. Writing this bit high has no effect.
15:14	Reserved

NOTE: EXTACT0, WAKE0/1, SWTCH, and RING toggling is selectable by EDC Register.

4.4.12 I/O Trap SMI Mask Register (IOTM)

Index: 316H

Bit	Description	Name	Reset State
0	Video On	VID_ON	'1'
1	Hard Disk 1 On	HD1 _ON	'1'
2	Hard Disk 2 On	HD2_ON	'1'
3	Floppy On	FLP _ON	'1'
4	Keyboard On	KBD_ON	'1'
5	Serial I/O 1 On	SIO1 _ON	'1'
6	Serial I/O 2 On	SIO2_ON	'1'
7	Parallel I/O On	PIO _ON	'1'
8	Reserved		'1'
9	Reserved		'1'
10	Programmable Range Device On [0]	PROG_ON0	'1'
11	Programmable Range Device On [1]	PROG_ON1	'1'
12	Programmable Range Device On [2]	PROG_ON2	'1'
13	Programmable Range Device On [3]	PROG_ON3	'1'
14	Programmable Range Device On [4]	PROG_ON4	'1'
15	Programmable Range Device On [5]	PROG_ON5	'1'

Bit	Description
0	**Video On:** When high, no SMI will be generated upon video access. When low, video is assumed to be off and SMI will be generated upon video access (A0000H-BFFFFH)
1	**Hard Disk 1 On:** When high, no SMI will be generated upon hard disk 1 access. When low, hard disk 1 is assumed to be off and SMI will be generated upon hard disk 1 access (1F0H-1F7H, 3F6H-3F7H).
2	**Hard Disk 2 On:** When high, no SMI will be generated upon hard disk 2 access. When low, hard disk 2 is assumed to be off and SMI will be generated upon hard disk 2 access(170H-177H, 376H-377H).
3	**Floppy On:** When high, no SMI will be generated upon floppy disk access. When low, floppy is assumed to be off and SMI will be generated upon floppy disk access (3F2H, 3F4H, 3F5H, 3F7H).
4	**Keyboard On:** When high, no SMI will be generated upon keyboard access. When low, keyboard is assumed to be off and SMI will be generated upon keyboard access (60H, 64H).
5	**Serial I/O 1 On:** When high, no SMI will be generated upon serial I/O 1 access. When low, serial I/O 1 is assumed to be off and SMI will be generated upon serial I/O 1 access (3F8H-3FFH, 3E8H-3EFH).

Bit	Description *(cont.)*
6	**Serial I/O 2 On:** When high, no SMI will be generated upon serial I/O 2 access. When low, serial I/O 2 is assumed to be off and SMI will be generated upon serial I/O 2 access (2F8H-2FFH, 2E8H-2EFH).
7	**Parallel I/O On:** When high, no SMI will be generated upon parallel I/O access. When low, parallel I/O is assumed to be off and SMI will be generated upon parallel I/O access (3BCH-3BFH, 378H-37FH, 278H-27FH).
9:8	Reserved
15:10	**Programmable Range Device On [5:0]:** When high, programmable range [5:0] device is on and no SMI will be generated. When low, programmable range [5:0] device is off and SMI will be generated when there is any access to the programmable range [5:0] device.

NOTE: There is no group mask for I/O trap event; SMI will always be generated if the corresponding bit is set to '0' and an access to that device occurs.

4.4.13 External SMI Trigger Mask Register (ESTM)

Index: 317H

Bit	Description	Name	Reset State
0	Mask WAKE0 From SMI	SMI_MSK_WAKE0	'1'
1	Mask WAKE1 From SMI	SMI_MSK_WAKE1	'1'
2	Mask SWTCH From SMI	SMI_MSK_SWTCH	'1'
3	Mask EXTACT0 From SMI	SMI_MSK_EXTACT0	'1'
4	Reserved		'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask WAKE0 From SMI:** When high, the programmed edge of WAKE0 toggling will not trigger a SMI; when low, it will.
1	**Mask WAKE1 From SMI:** When high, the programmed edge of WAKE1 toggling will not trigger a SMI; when low, it will.
2	**Mask SWTCH From SMI:** When high, the programmed edge of SWTCH toggling will not trigger a SMI but put the system into Standby mode.
3	**Mask EXTACT0 From SMI:** When high, the programmed edge of EXTACT0 toggling will not trigger a SMI; when low, it will.
15:4	Reserved

NOTE: WAKE0, WAKE1, SWTCH, EXTACT0 toggling is selectable by EDC Register.

4.4.14 Internal SMI Trigger Mask Register (ISTM)

Index: 318H

Bit	Description	Name	Reset State
0	Mask Device Timer 0 Time-out from SMI	SMI_MSK_DEVTMR0TO	'1'
1	Mask Device Timer 1 Time-out from SMI	SMI_MSK_DEVTMR1TO	'1'
2	Mask Device Timer 2 Time-out from SMI	SMI_MSK_DEVTMR2TO	'1'
3	Mask Device Timer 3 Time-out from SMI	SMI_MSK_DEVTMR3TO	'1'
4	Mask Device Timer 4 Time-out from SMI	SMI_MSK_DEVTMR4TO	'1'
5	Mask Device Timer 5 Time-out from SMI	SMI_MSK_DEVTMR5TO	'1'
6	Mask Doze Time-out from SMI	SMI_MSK_DOZE_TO	'1'
7	Mask Sleep Time-out from SMI	SMI_MSK_SLEEP_TO	'1'
8	Mask Suspend Time-out From SMI	SMI_MSK_SPND_TO	'1'
9	Mask GP Timer Compare From SMI	SMI_MSK_GPTMR	'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask Device Timer 0 Time-out from SMI:** When high, device timer 0 time-out will not trigger a SMI; when low, it will.
1	**Mask Device Timer 1 Time-out from SMI:** When high, device timer 1 time-out will not trigger a SMI; when low, it will.
2	**Mask Device Timer 2 Time-out from SMI:** When high, device timer 2 time-out will not trigger a SMI; when low, it will.
3	**Mask Device Timer 3 Time-out from SMI:** When high, device timer 3 time-out will not trigger a SMI; when low, it will.
4	**Mask Device Timer 4 Time-out from SMI:** When high, device timer 4 time-out will not trigger a SMI; when low, it will.
5	**Mask Device Timer 5 Time-out from SMI:** When high, device timer 5 time-out will not trigger a SMI; when low, it will.
6	**Mask Doze Time-out from SMI:** When high, Doze time-out will not trigger a SMI. Instead the power management controller will change state directly from fully-on to Doze mode. When low, Doze time-out will trigger a SMI and no automatic mode transition.

Bit	Description *(cont.)*
7	**Mask Sleep Time-out from SMI:** When high, sleep time-out will not trigger a SMI; when low, it will. When high, the power management controller will change the state directly from Doze to Sleep mode. When low, sleep time-out will trigger a SMI and no automatic mode transition will occur.
8	**Mask Suspend Time-out from SMI:** When high, Suspend mode time-out will not trigger a SMI; when low, it will.
9	**Mask GP Timer Compare from SMI:** When high, a compare on the GP Timer/Counter will not trigger a SMI; when low, it will.
15:10	Reserved

NOTE: Primary Activity can also trigger SMM and its mask bit is located at Register PAOC bit 1.

4.4.15 Software SMI Trigger Register (SST)

Index: 319H

Bit	Description	Name	Reset State
0	Reschedule SMI Select [0]	RSMI_SEL0	'0'
1	Reschedule SMI Select [1]	RSMI_SEL1	'0'
2	Reschedule SMI Select [2]	RSMI_SEL2	'0'
3	Reschedule SMI Select [3]	RSMI_SEL3	'0'
4	Reschedule SMI Prescalar	RSMI_PRESCALAR	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Soft SMI Immediate	SFTSMI_TRIG	'0'
9	Enable Soft SMI on I/O Write to B0H	SFTSMI_B0	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Reschedule SMI Select [3:0]:** **Bit [3:0]** — **Value** 0H — Disable 1H — 1 2H — 2 3H — 3 4H — 4 5H — 5 6H — 6 7H — 7 8H — 8 9H — 9 All Others — Reserved
4	**Reschedule SMI Prescalar:** '0' = 10 ms; '1' = 100 ms.
7:5	Reserved
8	**Soft SMI Immediate:** Setting this bit to '1' will trigger a SMI. The value read from this bit has no meaning.
9	**Enable Soft SMI on I/O Write to B0H:** When high, a write to port B0H will trigger a SMI; when low, a write to port B0H will not trigger a SMI.
15:10	Reserved

4.4.16 Primary Activity Option Control register (PAOC)

Index: 31AH

Bit	Description	Name	Reset State
0	Primary Activity Flag Enable	PAFLGEN	'0'
1	Mask Primary Activity From SMI	SMI_MSK_PA	'1'
2	Enable P/A to be Latched in SMM Mode	ENLTCH_PA_SMM	'0'
3	Disable Primary Activity On	DISPACTVON	'0'
4	Mask SMI From Primary Activity	MSKSMI_PA	'1'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Primary Activity Flag Enable:** '0' = disable; '1' = enable. When enabled, primary activity will be flagged (Refer to register AFR1 and AFR2 for additional information) during Doze or Sleep mode. When disabled, no flagging occurs. If SMI is used, this bit should be enabled to specify exact P/A source.
1	**Mask Primary Activity From SMI:** When high, primary activity will not trigger a SMI; when low, it will.
2	**Enable Primary Activity to be Latched in SMM Mode:** '0' = disable; '1' = enable. This bit enables latching primary activity that occurs in SMM. The P/A is active until deassertion of SMIACT# and will keep in a reset state and the system in On/Conserve mode while active.
3	**Disable Primary Activity On:** This bit disables the power management controller from switching to 'on' mode upon detection of any unmasked condition of the primary idle detector.
4	**Mask SMI from Primary Activity:** When set low, this bit allows any unmasked SMI (except for SMI caused by a primary activity) to trigger a primary activity. **NOTE:** This primary activity does not reset timers. This bit applies to Revision BB and later silicon revisions.
15:5	Reserved

4.4.17 Primary Activity Mask Register 1 (PAM1)

Index: 31BH

Bit	Description	Name	Reset State
0	Primary Activity Mask Video Accesses	PAMSK_VID	'1'
1	Primary Activity Mask Hard Disk 1 Accesses	PAMSK_HD1	'1'
2	Primary Activity Mask Hard Disk 2 Accesses	PAMSK_HD2	'1'
3	Primary Activity Mask Floppy Accesses	PAMSK_FLP	'1'
4	Primary Activity Mask Keyboard Accesses	PAMSK_KBD	'1'
5	Primary Activity Mask Serial I/O 1 Accesses	PAMSK_SIO1	'1'
6	Primary Activity Mask Serial I/O 2 Accesses	PAMSK_SIO2	'1'
7	Primary Activity Mask Parallel I/O Accesses	PAMSK_PIO	'1'
8	Primary Activity Mask HOLD	PAMSK_HOLD	'1'
9	Reserved		'1'
10	Primary Activity Mask Programmable Range Accesses [0]	PAMSK_PROG0	'1'
11	Primary Activity Mask Programmable Range Accesses [1]	PAMSK_PROG1	'1'
12	Primary Activity Mask Programmable Range Accesses [2]	PAMSK_PROG2	'1'
13	Primary Activity Mask Programmable Range Accesses [3]	PAMSK_PROG3	'1'
14	Primary Activity Mask Programmable Range Access [4]	PAMSK_PROG4	'1'
15	Primary Activity Mask Programmable Range Accesses [5]	PAMSK_PROG5	'1'

Bit	Description
0	**Primary Activity Mask Video Accesses:** When high, video accesses will not trigger the primary idle detector. (A0000H-BFFFFH)
1	**Primary Activity Mask Hard Disk 1 Accesses:** When high, hard disk 1 accesses will not trigger the primary idle detector. (1F0H-1F7H, 3F6H)
2	**Primary Activity Mask Hard Disk 2 Accesses:** When high, hard disk 2 accesses will not trigger the primary idle detector. (170H-177H, 376H)
3	**Primary Activity Mask Floppy Accesses:** When high, floppy accesses will not trigger the primary idle detector. (3F2H, 3F4H, 3F5H)
4	**Primary Activity Mask Keyboard Accesses:** When high, keyboard accesses will not trigger the primary idle detector. (60H, 64H)
5	**Primary Activity Mask Serial I/O 1 Accesses:** When high, serial I/O 1 accesses will not trigger the primary idle detector. (3F8H-3FFH, 3E8H-3EFH)

Bit	Description *(cont.)*
6	**Primary Activity Mask Serial I/O 2 Accesses:** When high, serial I/O 2 accesses will not trigger the primary idle detector (2F8H-2FFH, 2E8H-2EFH).
7	**Primary Activity Mask Parallel I/O Accesses:** When high, parallel I/O accesses will not trigger the primary idle detector (3BCH-3BFH, 378H-37FH, 278H-27FH).
8	**Primary Activity Mask HOLD:** When high, HOLD active will not trigger the primary idle detector.
9	Reserved
15:10	**Primary Activity Mask Programmable Range [5:0] Accesses:** When high, programmable range [5:0] accesses will not trigger the primary idle detector.

4.4.18 Primary Activity Mask Register 2 (PAM2)

Index: 31CH

Bit	Description	Name	Reset State
0	Reserved		'1'
1	Reserved		'1'
2	Reserved		'1'
3	Reserved		'1'
4	Reserved		'1'
5	Reserved		'1'
6	Primary Activity Mask EXTACT0	PAMSK_EXT0	'1'
7	Reserved		'1'
8	Primary Activity Mask RING	PAMSK_RING	'1'
9	Primary Activity Mask WAKE0	PAMSK_WAKE0	'1'
10	Primary Activity Mask WAKE1	PAMSK_WAKE1	'1'
11	Primary Activity Mask SWTCH	PAMSK_SWTCH	'1'
12	Primary Activity Mask FLOAT_REQ#	PAMSK_FLOTREQ#	'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
5:0	Reserved
6	**Primary Activity Mask EXTACT0:** When high, the programmed edge of EXTACT0 toggling will not trigger the primary idle detector; when low, it will.
7	Reserved
8	**Primary Activity Mask RING:** When high, the programmed edge of RING will not trigger the primary idle detector; when low, it will. **NOTE:** The ring counter does not apply in generating primary activity.
9	**Primary Activity Mask WAKE0:** When high, the programmed edge of WAKE0 will not trigger the primary idle detector. When low, it will.
10	**Primary Activity Mask WAKE1:** When high, the programmed edge of WAKE1 will not trigger the primary idle detector; when low, it will.
11	**Primary Activity Mask SWTCH:** When high, the programmed edge of SWTCH will not trigger the primary idle detector; when low, it will.
12	**Primary Activity Mask FLOAT_REQ#:** When high, FLOAT_REQ# active will not trigger the primary idle detector.
15:13	Reserved

4.4.19 Secondary Activity Mask Register (SAM)

Index: 31DH

Bit	Description	Name	Reset State
0	Mask SMI From Secondary Activity (S/A)	SA_MSK_SMI	'1'
1	Mask HOLD From Secondary Activity	SA_MSK_HOLD	'1'
2	Reserved		'1'
3	Reserved		'1'
4	Reserved		'1'
5	Reserved		'1'
6	Mask EXTACT0 From Secondary Activity	SA_MSK_EXT0	'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask SMI From Secondary Activity:** When high, SMI will not trigger the secondary activity. When low, SMI will trigger the secondary activity and the duration of this activity will be determined by SMIACT#. **NOTE:** S/A can only revive out of Doze or Sleep mode.
1	**Mask HOLD From Secondary Activity:** When high, HOLD will not trigger the secondary activity. When low, HOLD will trigger the secondary activity and the SA duration will be determined by HLDA.
5:2	Reserved
6	**Mask EXTACT0 From Secondary Activity:** When high, EXTACT0 toggling will not trigger the secondary activity; when low, it will. **NOTE:** S/A can only revive out of Doze or Sleep mode.
15:7	Reserved

NOTE: EXTACT0 toggling is selectable by EDC Register for more information. Refer to SAT Register for more information.

4.4.20 RING Count Control Register (RCC)

Index: 31EH

Bit	Description	Name	Reset State
0	RINGS One's Digit [0]	RINGS1SEL0	'0'
1	RINGS One's Digit [1]	RINGS1SEL1	'0'
2	RINGS One's Digit [2]	RINGS1SEL2	'0'
3	RINGS One's Digit [3]	RINGS1SEL3	'0'
4	RINGS Ten's Digit	RINGS10SEL	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**RINGS One's Digit [3:0]:** When these bits are set to 0H and bit 4, RINGS10SEL is set to '0', the ring counter will be reset:

Bit [3:0]	Value
0H	Disabled (Ring counter reset to '0')
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

4	**RINGS Ten's Digit:** '0' = 0; '1' = 1.
15:5	Reserved

4.4.21 Programmable Range Monitor Control Register 1 (PRM_CTRL1)

Index: 320H

Bit	Description	Name	Reset State
0	Programmable Range Monitor [0]	PRMMIO0	'0'
1	Programmable Range Monitor [1]	PRMMIO1	'0'
2	Programmable Range Monitor [2]	PRMMIO2	'0'
3	Programmable Range Monitor [3]	PRMMIO3	'0'
4	Programmable Range Monitor [4]	PRMMIO4	'0'
5	Programmable Range Monitor [5]	PRMMIO5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Programmable Range Monitor Enable [0]	PRMEN0	'0'
9	Programmable Range Monitor Enable [1]	PRMEN1	'0'
10	Programmable Range Monitor Enable [2]	PRMEN2	'0'
11	Programmable Range Monitor Enable [3]	PRMEN3	'0'
12	Programmable Range Monitor Enable [4]	PRMEN4	'0'
13	Programmable Range Monitor Enable [5]	PRMEN5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Programmable Range Monitor [5:0] Memory or I/O Compare Enable:** When high, the monitor will select memory addresses, and when low, the monitor will select I/O addresses.
7:6	Reserved
13:8	**Programmable Range Monitor Enable [5:0]:** When high, the programmable range monitor will be enabled.
15:14	Reserved

4.4.22 Programmable Range Monitor Control Register 2 (PRM_CTRL2)

Index: 321H

Bit	Description	Name	Reset State
0	Programmable Range Monitor Write Enable [0]	PRMWREN0	'0'
1	Programmable Range Monitor Write Enable [1]	PRMWREN1	'0'
2	Programmable Range Monitor Write Enable [2]	PRMWREN2	'0'
3	Programmable Range Monitor Write Enable [3]	PRMWREN3	'0'
4	Programmable Range Monitor Write Enable [4]	PRMWREN4	'0'
5	Programmable Range Monitor Write Enable [5]	PRMWREN5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Programmable Range Monitor Read Enable [0]	PRMRDEN0	'0'
9	Programmable Range Monitor Read Enable [1]	PRMRDEN1	'0'
10	Programmable Range Monitor Read Enable [2]	PRMRDEN2	'0'
11	Programmable Range Monitor Read Enable [3]	PRMRDEN3	'0'
12	Programmable Range Monitor Read Enable [4]	PRMRDEN4	'0'
13	Programmable Range Monitor Read Enable [5]	PRMRDEN5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Programmable Range Monitor [5:0] Write Enable:** When high, the monitor will select write cycles.
7:6	Reserved
13:8	**Programmable Range Monitor Read Enable [5:0]:** When high, the monitor will select read cycles.
15:14	Reserved

4.4.23 Programmable Range Monitor 0 Address Register (PRMA0)

Index: 322H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 0 Addresses [0]	PRMA00	'0'
1	Programmable Range Monitor 0 Addresses [1]	PRMA01	'0'
2	Programmable Range Monitor 0 Addresses [2]	PRMA02	'0'
3	Programmable Range Monitor 0 Addresses [3]	PRMA03	'0'
4	Programmable Range Monitor 0 Addresses [4]	PRMA04	'0'
5	Programmable Range Monitor 0 Addresses [5]	PRMA05	'0'
6	Programmable Range Monitor 0 Addresses [6]	PRMA06	'0'
7	Programmable Range Monitor 0 Addresses [7]	PRMA07	'0'
8	Programmable Range Monitor 0 Addresses [8]	PRMA08	'0'
9	Programmable Range Monitor 0 Addresses [9]	PRMA09	'0'
10	Programmable Range Monitor 0 Addresses [10]	PRMA010	'0'
11	Programmable Range Monitor 0 Addresses [11]	PRMA011	'0'
12	Programmable Range Monitor 0 Addresses [12]	PRMA012	'0'
13	Programmable Range Monitor 0 Addresses [13]	PRMA013	'0'
14	Programmable Range Monitor 0 Addresses [14]	PRMA014	'0'
15	Programmable Range Monitor 0 Addresses [15]	PRMA015	'0'

Bit	Description
15:0	**Programmable Range Monitor 0 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.24 Programmable Range Monitor 0 Compare Register (PRMC0)

Index: 323H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 0 Compare Enable [0]	PRMCMP00	'0'
1	Programmable Range Monitor 0 Compare Enable [1]	PRMCMP01	'0'
2	Programmable Range Monitor 0 Compare Enable [2]	PRMCMP02	'0'
3	Programmable Range Monitor 0 Compare Enable [3]	PRMCMP03	'0'
4	Programmable Range Monitor 0 Compare Enable [4]	PRMCMP04	'0'
5	Programmable Range Monitor 0 Compare Enable [5]	PRMCMP05	'0'
6	Programmable Range Monitor 0 Compare Enable [6]	PRMCMP06	'0'
7	Programmable Range Monitor 0 Compare Enable [7]	PRMCMP07	'0'
8	Programmable Range Monitor 0 Compare Enable [8]	PRMCMP08	'0'
9	Programmable Range Monitor 0 Compare Enable [9]	PRMCMP09	'0'
10	Programmable Range Monitor 0 Compare Enable [10]	PRMCMP010	'0'
11	Programmable Range Monitor 0 Compare Enable [11]	PRMCMP011	'0'
12	Programmable Range Monitor 0 Compare Enable [12]	PRMCMP012	'0'
13	Programmable Range Monitor 0 Compare Enable [13]	PRMCMP013	'0'
14	Programmable Range Monitor 0 Compare Enable [14]	PRMCMP014	'0'
15	Programmable Range Monitor 0 Compare Enable [15]	PRMCMP015	'0'

Bit	Description
15:0	**Programmable Range Monitor 0 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.25 Programmable Range Monitor 1 Address Register (PRMA1)

Index: 324H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 1 Addresses [0]	PRMA10	'0'
1	Programmable Range Monitor 1 Addresses [1]	PRMA11	'0'
2	Programmable Range Monitor 1 Addresses [2]	PRMA12	'0'
3	Programmable Range Monitor 1 Addresses [3]	PRMA13	'0'
4	Programmable Range Monitor 1 Addresses [4]	PRMA14	'0'
5	Programmable Range Monitor 1 Addresses [5]	PRMA15	'0'
6	Programmable Range Monitor 1 Addresses [6]	PRMA16	'0'
7	Programmable Range Monitor 1 Addresses [7]	PRMA17	'0'
8	Programmable Range Monitor 1 Addresses [8]	PRMA18	'0'
9	Programmable Range Monitor 1 Addresses [9]	PRMA19	'0'
10	Programmable Range Monitor 1 Addresses [10]	PRMA110	'0'
11	Programmable Range Monitor 1 Addresses [11]	PRMA111	'0'
12	Programmable Range Monitor 1 Addresses [12]	PRMA112	'0'
13	Programmable Range Monitor 1 Addresses [13]	PRMA113	'0'
14	Programmable Range Monitor 1 Addresses [14]	PRMA114	'0'
15	Programmable Range Monitor 1 Addresses [15]	PRMA115	'0'

Bit	Description
15:0	**Programmable Range Monitor 1 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.26 Programmable Range Monitor 1 Compare Register (PRMC1)

Index: 325H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 1 Compare Enable [0]	PRMCMP10	'0'
1	Programmable Range Monitor 1 Compare Enable [1]	PRMCMP11	'0'
2	Programmable Range Monitor 1 Compare Enable [2]	PRMCMP12	'0'
3	Programmable Range Monitor 1 Compare Enable [3]	PRMCMP13	'0'
4	Programmable Range Monitor 1 Compare Enable [4]	PRMCMP14	'0'
5	Programmable Range Monitor 1 Compare Enable [5]	PRMCMP15	'0'
6	Programmable Range Monitor 1 Compare Enable [6]	PRMCMP16	'0'
7	Programmable Range Monitor 1 Compare Enable [7]	PRMCMP17	'0'
8	Programmable Range Monitor 1 Compare Enable [8]	PRMCMP18	'0'
9	Programmable Range Monitor 1 Compare Enable [9]	PRMCMP19	'0'
10	Programmable Range Monitor 1 Compare Enable [10]	PRMCMP110	'0'
11	Programmable Range Monitor 1 Compare Enable [11]	PRMCMP111	'0'
12	Programmable Range Monitor 1 Compare Enable [12]	PRMCMP112	'0'
13	Programmable Range Monitor 1 Compare Enable [13]	PRMCMP113	'0'
14	Programmable Range Monitor 1 Compare Enable [14]	PRMCMP114	'0'
15	Programmable Range Monitor 1 Compare Enable [15]	PRMCMP115	'0'

Bit	Description
15:0	**Programmable Range Monitor 1 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.27 Programmable Range Monitor 2 Address Register (PRMA2)

Index: 326H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 2 Addresses [0]	PRMA20	'0'
1	Programmable Range Monitor 2 Addresses [1]	PRMA21	'0'
2	Programmable Range Monitor 2 Addresses [2]	PRMA22	'0'
3	Programmable Range Monitor 2 Addresses [3]	PRMA23	'0'
4	Programmable Range Monitor 2 Addresses [4]	PRMA24	'0'
5	Programmable Range Monitor 2 Addresses [5]	PRMA25	'0'
6	Programmable Range Monitor 2 Addresses [6]	PRMA26	'0'
7	Programmable Range Monitor 2 Addresses [7]	PRMA27	'0'
8	Programmable Range Monitor 2 Addresses [8]	PRMA28	'0'
9	Programmable Range Monitor 2 Addresses [9]	PRMA29	'0'
10	Programmable Range Monitor 2 Addresses [10]	PRMA210	'0'
11	Programmable Range Monitor 2 Addresses [11]	PRMA211	'0'
12	Programmable Range Monitor 2 Addresses [12]	PRMA212	'0'
13	Programmable Range Monitor 2 Addresses [13]	PRMA213	'0'
14	Programmable Range Monitor 2 Addresses [14]	PRMA214	'0'
15	Programmable Range Monitor 2 Addresses [15]	PRMA215	'0'

Bit	Description
15:0	**Programmable Range Monitor 2 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.28 Programmable Range Monitor 2 Compare Register (PRMC2)

Index: 327H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 2 Compare Enable [0]	PRMCMP20	'0'
1	Programmable Range Monitor 2 Compare Enable [1]	PRMCMP21	'0'
2	Programmable Range Monitor 2 Compare Enable [2]	PRMCMP22	'0'
3	Programmable Range Monitor 2 Compare Enable [3]	PRMCMP23	'0'
4	Programmable Range Monitor 2 Compare Enable [4]	PRMCMP24	'0'
5	Programmable Range Monitor 2 Compare Enable [5]	PRMCMP25	'0'
6	Programmable Range Monitor 2 Compare Enable [6]	PRMCMP26	'0'
7	Programmable Range Monitor 2 Compare Enable [7]	PRMCMP27	'0'
8	Programmable Range Monitor 2 Compare Enable [8]	PRMCMP28	'0'
9	Programmable Range Monitor 2 Compare Enable [9]	PRMCMP29	'0'
10	Programmable Range Monitor 2 Compare Enable [10]	PRMCMP210	'0'
11	Programmable Range Monitor 2 Compare Enable [11]	PRMCMP211	'0'
12	Programmable Range Monitor 2 Compare Enable [12]	PRMCMP212	'0'
13	Programmable Range Monitor 2 Compare Enable [13]	PRMCMP213	'0'
14	Programmable Range Monitor 2 Compare Enable [14]	PRMCMP214	'0'
15	Programmable Range Monitor 2 Compare Enable [15]	PRMCMP215	'0'

Bit	Description
15:0	**Programmable Range Monitor 2 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.29 Programmable Range Monitor 3 Address Register (PRMA3)

Index: 328H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 3 Addresses [0]	PRMA30	'0'
1	Programmable Range Monitor 3 Addresses [1]	PRMA31	'0'
2	Programmable Range Monitor 3 Addresses [2]	PRMA32	'0'
3	Programmable Range Monitor 3 Addresses [3]	PRMA33	'0'
4	Programmable Range Monitor 3 Addresses [4]	PRMA34	'0'
5	Programmable Range Monitor 3 Addresses [5]	PRMA35	'0'
6	Programmable Range Monitor 3 Addresses [6]	PRMA36	'0'
7	Programmable Range Monitor 3 Addresses [7]	PRMA37	'0'
8	Programmable Range Monitor 3 Addresses [8]	PRMA38	'0'
9	Programmable Range Monitor 3 Addresses [9]	PRMA39	'0'
10	Programmable Range Monitor 3 Addresses [10]	PRMA310	'0'
11	Programmable Range Monitor 3 Addresses [11]	PRMA311	'0'
12	Programmable Range Monitor 3 Addresses [12]	PRMA312	'0'
13	Programmable Range Monitor 3 Addresses [13]	PRMA313	'0'
14	Programmable Range Monitor 3 Addresses [14]	PRMA314	'0'
15	Programmable Range Monitor 3 Addresses [15]	PRMA315	'0'

Bit	Description
15:0	**Programmable Range Monitor 3 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.30 Programmable Range Monitor 3 Compare Register (PRMC3)

Index: 329H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 3 Compare Enable [0]	PRMCMP30	'0'
1	Programmable Range Monitor 3 Compare Enable [1]	PRMCMP31	'0'
2	Programmable Range Monitor 3 Compare Enable [2]	PRMCMP32	'0'
3	Programmable Range Monitor 3 Compare Enable [3]	PRMCMP33	'0'
4	Programmable Range Monitor 3 Compare Enable [4]	PRMCMP34	'0'
5	Programmable Range Monitor 3 Compare Enable [5]	PRMCMP35	'0'
6	Programmable Range Monitor 3 Compare Enable [6]	PRMCMP36	'0'
7	Programmable Range Monitor 3 Compare Enable [7]	PRMCMP37	'0'
8	Programmable Range Monitor 3 Compare Enable [8]	PRMCMP38	'0'
9	Programmable Range Monitor 3 Compare Enable [9]	PRMCMP39	'0'
10	Programmable Range Monitor 3 Compare Enable [10]	PRMCMP310	'0'
11	Programmable Range Monitor 3 Compare Enable [11]	PRMCMP311	'0'
12	Programmable Range Monitor 3 Compare Enable [12]	PRMCMP312	'0'
13	Programmable Range Monitor 3 Compare Enable [13]	PRMCMP313	'0'
14	Programmable Range Monitor 3 Compare Enable [14]	PRMCMP314	'0'
15	Programmable Range Monitor 3 Compare Enable [15]	PRMCMP315	'0'

Bit	Description
15:0	**Programmable Range Monitor 3 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.31 Programmable Range Monitor 4 Address Register (PRMA4)

Index: 32AH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 4 Addresses [0]	PRMA40	'0'
1	Programmable Range Monitor 4 Addresses [1]	PRMA41	'0'
2	Programmable Range Monitor 4 Addresses [2]	PRMA42	'0'
3	Programmable Range Monitor 4 Addresses [3]	PRMA43	'0'
4	Programmable Range Monitor 4 Addresses [4]	PRMA44	'0'
5	Programmable Range Monitor 4 Addresses [5]	PRMA45	'0'
6	Programmable Range Monitor 4 Addresses [6]	PRMA46	'0'
7	Programmable Range Monitor 4 Addresses [7]	PRMA47	'0'
8	Programmable Range Monitor 4 Addresses [8]	PRMA48	'0'
9	Programmable Range Monitor 4 Addresses [9]	PRMA49	'0'
10	Programmable Range Monitor 4 Addresses [10]	PRMA410	'0'
11	Programmable Range Monitor 4 Addresses [11]	PRMA411	'0'
12	Programmable Range Monitor 4 Addresses [12]	PRMA412	'0'
13	Programmable Range Monitor 4 Addresses [13]	PRMA413	'0'
14	Programmable Range Monitor 4 Addresses [14]	PRMA414	'0'
15	Programmable Range Monitor 4 Addresses [15]	PRMA415	'0'

Bit	Description
15:0	**Programmable Range Monitor 4 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[19:4].

4.4.32 Programmable Range Monitor 4 Compare Register (PRMC4)

Index: 32BH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 4 Compare Enable [0]	PRMCMP40	'0'
1	Programmable Range Monitor 4 Compare Enable [1]	PRMCMP41	'0'
2	Programmable Range Monitor 4 Compare Enable [2]	PRMCMP42	'0'
3	Programmable Range Monitor 4 Compare Enable [3]	PRMCMP43	'0'
4	Programmable Range Monitor 4 Compare Enable [4]	PRMCMP44	'0'
5	Programmable Range Monitor 4 Compare Enable [5]	PRMCMP45	'0'
6	Programmable Range Monitor 4 Compare Enable [6]	PRMCMP46	'0'
7	Programmable Range Monitor 4 Compare Enable [7]	PRMCMP47	'0'
8	Programmable Range Monitor 4 Compare Enable [8]	PRMCMP48	'0'
9	Programmable Range Monitor 4 Compare Enable [9]	PRMCMP49	'0'
10	Programmable Range Monitor 4 Compare Enable [10]	PRMCMP410	'0'
11	Programmable Range Monitor 4 Compare Enable [11]	PRMCMP411	'0'
12	Programmable Range Monitor 4 Compare Enable [12]	PRMCMP412	'0'
13	Programmable Range Monitor 4 Compare Enable [13]	PRMCMP413	'0'
14	Programmable Range Monitor 4 Compare Enable [14]	PRMCMP414	'0'
15	Programmable Range Monitor 4 Compare Enable [15]	PRMCMP415	'0'

Bit	Description
15:0	**Programmable Range Monitor 4 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[19:4]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.33 Programmable Range Monitor 5 Address Register (PRMA5)

Index: 32CH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 5 Addresses [0]	PRMA20	'0'
1	Programmable Range Monitor 5 Addresses [1]	PRMA21	'0'
2	Programmable Range Monitor 5 Addresses [2]	PRMA22	'0'
3	Programmable Range Monitor 5 Addresses [3]	PRMA23	'0'
4	Programmable Range Monitor 5 Addresses [4]	PRMA24	'0'
5	Programmable Range Monitor 5 Addresses [5]	PRMA25	'0'
6	Programmable Range Monitor 5 Addresses [6]	PRMA26	'0'
7	Programmable Range Monitor 5 Addresses [7]	PRMA27	'0'
8	Programmable Range Monitor 5 Addresses [8]	PRMA28	'0'
9	Programmable Range Monitor 5 Addresses [9]	PRMA29	'0'
10	Programmable Range Monitor 5 Addresses [10]	PRMA210	'0'
11	Programmable Range Monitor 5 Addresses [11]	PRMA211	'0'
12	Programmable Range Monitor 5 Addresses [12]	PRMA212	'0'
13	Programmable Range Monitor 5 Addresses [13]	PRMA213	'0'
14	Programmable Range Monitor 5 Addresses [14]	PRMA214	'0'
15	Programmable Range Monitor 5 Addresses [15]	PRMA215	'0'

Bit	Description
15:0	**Programmable Range Monitor 5 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[19:4].

4.4.34 Programmable Range Monitor 5 Compare Register (PRMC5)

Index: 32DH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 5 Compare Enable [0]	PRMCMP50	'0'
1	Programmable Range Monitor 5 Compare Enable [1]	PRMCMP51	'0'
2	Programmable Range Monitor 5 Compare Enable [2]	PRMCMP52	'0'
3	Programmable Range Monitor 5 Compare Enable [3]	PRMCMP53	'0'
4	Programmable Range Monitor 5 Compare Enable [4]	PRMCMP54	'0'
5	Programmable Range Monitor 5 Compare Enable [5]	PRMCMP55	'0'
6	Programmable Range Monitor 5 Compare Enable [6]	PRMCMP56	'0'
7	Programmable Range Monitor 5 Compare Enable [7]	PRMCMP57	'0'
8	Programmable Range Monitor 5 Compare Enable [8]	PRMCMP58	'0'
9	Programmable Range Monitor 5 Compare Enable [9]	PRMCMP59	'0'
10	Programmable Range Monitor 5 Compare Enable [10]	PRMCMP510	'0'
11	Programmable Range Monitor 5 Compare Enable [11]	PRMCMP511	'0'
12	Programmable Range Monitor 5 Compare Enable [12]	PRMCMP512	'0'
13	Programmable Range Monitor 5 Compare Enable [13]	PRMCMP513	'0'
14	Programmable Range Monitor 5 Compare Enable [14]	PRMCMP514	'0'
15	Programmable Range Monitor 5 Compare Enable [15]	PRMCMP515	'0'

Bit	Description
15:0	**Programmable Range Monitor 5 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[19:4]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.35 Power Management Mode Register (PMM)

Index: 330H

Bit	Description	Name	Reset State
0	System Management Mode [0]	SM_MODE0	'0'
1	System Management Mode [1]	SM_MODE1	'0'
2	System Management Mode [2]	SM_MODE2	'0'
3	Resume	RESUME	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

2:0 **System Management Mode [2:0]:**

Bit [2:0]	Power Manangement State
0H	On
1H	Doze
2H	Sleep or Deep Sleep
3H	Suspend
All Others	Reserved

These bits are read and write. The system will enter the corresponding mode if a value of 0H-3H is written. A write of 4H-7H will have no effect on the power management mode.

3 **Resume:** When high, this bit indicates that the system has entered Suspend mode such that the previous system state must be restored. This bit should be written low upon resuming.

15:4 Reserved

4.4.36 On/Doze Mode Power Control Register (ONDZ-PC)

Index: 331H

Bit	Description	Name	Reset State
0	Power Control On/Doze Mode [0]	PCONDZ0	'1'
1	Power Control On/Doze Mode [1]	PCONDZ1	'1'
2	Power Control On/Doze Mode [2]	PCONDZ2	'1'
3	Power Control On/Doze Mode [3]	PCONDZ3	'0'
4	Power Control On/Doze Mode [4]	PCONDZ4	'0'
5	Power Control On/Doze Mode [5]	PCONDZ5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control On/Doze Mode [5:0]:** If any bit is high and On/Doze mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.37 Sleep Mode Power Control Register (SLP-PC)

Index: 332H

Bit	Description	Name	Reset State
0	Power Control Sleep Mode [0]	PCSLP0	'1'
1	Power Control Sleep Mode [1]	PCSLP1	'1'
2	Power Control Sleep Mode [2]	PCSLP2	'1'
3	Power Control Sleep Mode [3]	PCSLP3	'0'
4	Power Control Sleep Mode [4]	PCSLP4	'0'
5	Power Control Sleep Mode [5]	PCSLP5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control Sleep Mode [5:0]:** If any bit is high and Sleep mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.38 Suspend Mode Power Control Register (SPND-PC)

Index: 333H

Bit	Description	Name	Reset State
0	Power Control Suspend Mode [0]	PCSPND0	'1'
1	Power Control Suspend Mode [1]	PCSPND1	'1'
2	Power Control Suspend Mode [2]	PCSPND2	'1'
3	Power Control Suspend Mode [3]	PCSPND3	'0'
4	Power Control Suspend Mode [4]	PCSPND4	'0'
5	Power Control Suspend Mode [5]	PCSPND5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control Suspend Mode [5:0]:** If any bit is high and Suspend mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.39 Doze Mode Timer Register (DZMT)

Index: 335H

Bit	Description	Name	Reset State
0	Doze Mode Timer One's Digit [0]	DZTMR1SEL0	'0'
1	Doze Mode Timer One's Digit [1]	DZTMR1SEL1	'0'
2	Doze Mode Timer One's Digit [2]	DZTMR1SEL2	'0'
3	Doze Mode Timer One's Digit [3]	DZTMR1SEL3	'0'
4	Doze Mode Timer Ten's Digit [0]	DZTMR10SEL0	'0'
5	Doze Mode Timer Ten's Digit [1]	DZTMR10SEL1	'0'
6	Doze Mode Timer Ten's Digit [2]	DZTMR10SEL2	'0'
7	Doze Mode Timer Clock Prescalar	DZTMR_PRESCALAR	'0'
8	Enable Doze Mode Timer to be Reset by Primary Activity	DZTMR_RSTPAEN	'1'
9	Doze Mode Timer Enable	DZTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Doze Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Doze mode timer will be disabled.

Bit [3:0]	One's Value
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Doze Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Doze mode timer will be disabled.

Bit [3:0]	Ten's Value
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

7	**Doze Mode Timer Clock Prescalar:** '0' = 100 ms; '1' = 1 s. **NOTE:** If 100 ms is used, the accuracy is within ± 100 ms. If 1s is used, the accuracy is within ± 1s.
8	**Enable Doze Mode Timer to be Reset by Primary Activity:** '0' = disable; '1' = enable.
9	**Doze Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.40 Sleep Mode Timer Register (SLPMT)

Index: 336H

Bit	Description	Name	Reset State
0	Sleep Mode Timer One's Digit [0]	SLPTMR1SEL0	'0'
1	Sleep Mode Timer One's Digit [1]	SLPTMR1SEL1	'0'
2	Sleep Mode Timer One's Digit [2]	SLPTMR1SEL2	'0'
3	Sleep Mode Timer One's Digit [3]	SLPTMR1SEL3	'0'
4	Sleep Mode Timer Ten's Digit [0]	SLPTMR10SEL0	'0'
5	Sleep Mode Timer Ten's Digit [1]	SLPTMR10SEL1	'0'
6	Sleep Mode Timer Ten's Digit [2]	SLPTMR10SEL2	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Sleep Mode Timer Enable	SLPTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Sleep Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Sleep mode timer will be disabled.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

NOTE: The accuracy of the timer is within ± 1 min.

Bit	Description *(cont.)*
6:4	**Sleep Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Sleep mode timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

8:7	Reserved
9	**Sleep Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.41 Suspend Mode Timer Register (SPNDMT)

Index: 337H

Bit	Description	Name	Reset State
0	Suspend Mode Timer One's Digit [0]	SPDTMR1SEL0	'0'
1	Suspend Mode Timer One's Digit [1]	SPDTMR1SEL1	'0'
2	Suspend Mode Timer One's Digit [2]	SPDTMR1SEL2	'0'
3	Suspend Mode Timer One's Digit [3]	SPDTMR1SEL3	'0'
4	Suspend Mode Timer Ten's Digit [0]	SPDTMR10SEL0	'0'
5	Suspend Mode Timer Ten's Digit [1]	SPDTMR10SEL1	'0'
6	Suspend Mode Timer Ten's Digit [2]	SPDTMR10SEL2	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Suspend Mode Timer Enable	SPDTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Suspend Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Suspend mode timer will be disabled.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

NOTE: The accuracy of the timer is within ± 1 min.

Bit	Description *(cont.)*
6:4	**Suspend Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Suspend mode timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

NOTE: Tolerance is ± 3 minutes.

8:7	Reserved
9	**Suspend Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.42 Secondary Activity Timer Register (SAT)

Index: 338H

Bit	Description	Name	Reset State
0	Secondary Activity Timer One's Digit [0]	SATMR1SEL0	'0'
1	Secondary Activity Timer One's Digit [1]	SATMR1SEL1	'0'
2	Secondary Activity Timer One's Digit [2]	SATMR1SEL2	'0'
3	Secondary Activity Timer One's Digit [3]	SATMR1SEL3	'0'
4	Secondary Activity Timer Ten's Digit [0]	SATMR10SEL0	'0'
5	Secondary Activity Timer Ten's Digit [1]	SATMR10SEL1	'0'
6	Secondary Activity Timer Ten's Digit [2]	SATMR10SEL2	'0'
7	Secondary Activity Timer Clock Prescalar	SATMR_PRESCALAR	'0'
8	Reset Secondary Activity on SMI	RST_SA_ON_SMI	'0'
9	Secondary Activity Timer Enable	SATMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Secondary Activity Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the secondary activity timer will be disabled. The timer is used to extend the revive time due to a S/A source.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Secondary Activity Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the secondary activity timer will be disabled. The timer is used to extend the revive time due to a S/A source. **Bit [3:0]** — **Ten's Value** 0H — 0 1H — 1 2H — 2 3H — 3 4H — 4 5H — 5 6H — 6 7H — 7 All Others — Reserved
7	**Secondary Activity Timer Clock Prescalar:** '0' = 100 µs; '1' = 1 ms. **NOTE:** If the 100-µs option is used, the accuracy of the timer is within ± 100 µs. If the 1-ms option is used, the accuracy of the timer is within ±1 ms.
8	**Reset Secondary Activity on SMI:** Writing a '1' to this bit will initiate a single pulse which resets secondary activity on SMI.
9	**Secondary Activity Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.43 Power on Demand Primary Activity Timer Register (POD_PAT)

Index: 339H

Bit	Description	Name	Reset State
0	Primary Activity Timer One's Digit [0]	PATMR1SEL0	'0'
1	Primary Activity Timer One's Digit [1]	PATMR1SEL1	'0'
2	Primary Activity Timer One's Digit [2]	PATMR1SEL2	'0'
3	Primary Activity Timer One's Digit [3]	PATMR1SEL3	'0'
4	Primary Activity Timer Ten's Digit [0]	PATMR10SEL0	'0'
5	Primary Activity Timer Ten's Digit [1]	PATMR10SEL1	'0'
6	Primary Activity Timer Ten's Digit [2]	PATMR10SEL2	'0'
7	Primary Activity Timer Clock Prescalar	PATMR_PRESCALAR	'0'
8	Reserved		'0'
9	Primary Activity Timer Enable	PATMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Primary Activity Timer One's Digit [3:0]:** This timer is used to extend the time due to a P/A occurrence during which POD (Power on Demand) will be blocked. **NOTE:** This P/A will not affect the timers or power management modes.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Primary Activity Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the primary activity timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

7	**Primary Activity Timer Clock Prescalar:** '0' = 100 µs; '1' = 1 ms. **NOTE:** If the 100-µs option is used, the accuracy of the timer is within ± 100 µs. If the 1-ms option is used, the accuracy of the timer is within ±1 ms.
8	Reserved
9	**Primary Activity Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.44 General Purpose Control Register (GPC)

Index: 340H

Bit	Description	Name	Reset State
0	General Purpose I/O Data [0]	GPIODATA0	'0'
1	General Purpose I/O Data [1]	GPIODATA1	'0'
2	General Purpose I/O Data [2]	GPIODATA2	'0'
3	General Purpose I/O Data [3]	GPIODATA3	'0'
4	General Purpose I/O Data [4]	GPIODATA4	'0'
5	General Purpose I/O Data [5]	GPIODATA5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	General Purpose I/O Direction [0]	GPIODIR0	'0'
9	General Purpose I/O Direction [1]	GPIODIR1	'0'
10	General Purpose I/O Direction [2]	GPIODIR2	'0'
11	General Purpose I/O Direction [3]	GPIODIR3	'0'
12	General Purpose I/O Direction [4]	GPIODIR4	'0'
13	General Purpose I/O Direction [5]	GPIODIR5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**General Purpose I/O Data [5:0]:** When the corresponding GPIODIR for each bit is low, a read of the bit returns the state of the GPIO pin and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written.
7:6	Reserved
13:8	**General Purpose I/O Direction [5:0]:** When low, GPIO is an input pin; when high, GPIO is an output pin.
15:14	Reserved

4.4.45 General Purpose Counter/Timer Control Register (GP_CNTMRC)

Index: 341H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	GP Counter/Timer Clock Select	GPCT_CLKSEL	'0'
5	GP Counter/Timer Select [0]	GPCTSEL0	'0'
6	GP Counter/Timer Select [1]	GPCTSEL1	'0'
7	GP Counter/Timer Enable	GPCTEN	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	Reserved
4	**General Purpose Counter/Timer Clock Select:** When low, a 1-Hz clock will be used to feed into the general purpose counter/timer. When high, a 32-kHz clock will be used to feed into the general purpose counter/timer.
6:5	**General Purpose Counter/Timer Select [1:0]:** When either counter is enabled, GPIO3 will be enabled as the counter clock. When the 1-s timer is enabled, a 1-Hz clock will be enabled. When the 1-min. timer is enabled, a 1-min. clock will be enabled.
7	**General Purpose Counter/Timer Enable:** When high, the general purpose counter/timer will be enabled; when low it will be disabled.
15:8	Reserved

Bit [1:0]	GPCT_CLKSEL = 0	GPCT_CLKSEL = 1
'00'	16-bit counter	16-bit counter
'01'	24-bit counter	24-bit counter
'10'	1-second timer	31.25-µs timer
'11'	1-minute timer	1.875-ms timer

4.4.46 General Purpose Counter/Timer Current Value Register (GP_CNTMR_VAL)

Index: 342H

Bit	Description	Name	Reset State
0	General Purpose Counter/Timer [0]	GPCT0	'0'
1	General Purpose Counter/Timer [1]	GPCT1	'0'
2	General Purpose Counter/Timer [2]	GPCT2	'0'
3	General Purpose Counter/Timer [3]	GPCT3	'0'
4	General Purpose Counter/Timer [4]	GPCT4	'0'
5	General Purpose Counter/Timer [5]	GPCT5	'0'
6	General Purpose Counter/Timer [6]	GPCT6	'0'
7	General Purpose Counter/Timer [7]	GPCT7	'0'
8	General Purpose Counter/Timer [8]	GPCT8	'0'
9	General Purpose Counter/Timer [9]	GPCT9	'0'
10	General Purpose Counter/Timer [10]	GPCT10	'0'
11	General Purpose Counter/Timer [11]	GPCT11	'0'
12	General Purpose Counter/Timer [12]	GPCT12	'0'
13	General Purpose Counter/Timer [13]	GPCT13	'0'
14	General Purpose Counter/Timer [14]	GPCT14	'0'
15	General Purpose Counter/Timer [15]	GPCT15	'0'

Bit	Description
15:0	**General Purpose Counter/Timer [15:0]:** Reading this register returns the lower byte of the current value of the general purpose counter/timer. When the 24-bit counter is enabled, these bits represent counter bits [23:8]; otherwise they represent counter/timer bits [15:0]. Any write to this register will reset the entire counter/timer.

4.4.47 General Purpose Counter/Timer Compare Register (GP_CNTMR_CMP)

Index: 343H

Bit	Description	Name	Reset State
0	General Purpose Counter/Timer Compare [0]	GPTMRCMP0	'0'
1	General Purpose Counter/Timer Compare [1]	GPTMRCMP1	'0'
2	General Purpose Counter/Timer Compare [2]	GPTMRCMP2	'0'
3	General Purpose Counter/Timer Compare [3]	GPTMRCMP3	'0'
4	General Purpose Counter/Timer Compare [4]	GPTMRCMP4	'0'
5	General Purpose Counter/Timer Compare [5]	GPTMRCMP5	'0'
6	General Purpose Counter/Timer Compare [6]	GPTMRCMP6	'0'
7	General Purpose Counter/Timer Compare [7]	GPTMRCMP7	'0'
8	General Purpose Counter/Timer Compare [8]	GPTMRCMP8	'0'
9	General Purpose Counter/Timer Compare [9]	GPTMRCMP9	'0'
10	General Purpose Counter/Timer Compare [10]	GPTMRCMP10	'0'
11	General Purpose Counter/Timer Compare [11]	GPTMRCMP11	'0'
12	General Purpose Counter/Timer Compare [12]	GPTMRCMP12	'0'
13	General Purpose Counter/Timer Compare [13]	GPTMRCMP13	'0'
14	General Purpose Counter/Timer Compare [14]	GPTMRCMP14	'0'
15	General Purpose Counter/Timer Compare [15]	GPTMRCMP15	'0'

Bit	Description
15:0	**General Purpose Counter/Timer Compare [15:0]:** These bits represent the compare value at which the general purpose counter/timer will trigger an interrupt if the corresponding SMI is unmasked. If a 24-bit counter is enabled, these bits represent compare value bits [23:8].

4.4.48 Device Timer 0 Time-out Register (DTT0)

Index: 344H

Bit	Description	Name	Reset State
0	Device Timer 0 Time-out Select [0]	DEVTMR0SEL0	'0'
1	Device Timer 0 Time-out Select [1]	DEVTMR0SEL1	'0'
2	Device Timer 0 Time-out Select [2]	DEVTMR0SEL2	'0'
3	Device Timer 0 Time-out Select [3]	DEVTMR0SEL3	'0'
4	Device Timer 0 Time-out Prescalar [0]	DEVTMR0PRES0	'0'
5	Device Timer 0 Time-out Prescalar [1]	DEVTMR0PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 0 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 0 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.49 Device Timer 1 Time-out Register (DTT1)

Index: 345H

Bit	Description	Name	Reset State
0	Device Timer 1 Time-out Select [0]	DEVTMR1SEL0	'0'
1	Device Timer 1 Time-out Select [1]	DEVTMR1SEL1	'0'
2	Device Timer 1 Time-out Select [2]	DEVTMR1SEL2	'0'
3	Device Timer 1 Time-out Select [3]	DEVTMR1SEL3	'0'
4	Device Timer 1 Time-out Prescalar [0]	DEVTMR1PRES0	'0'
5	Device Timer 1 Time-out Prescalar [1]	DEVTMR1PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 1 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 1 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.50 Device Timer 2 Time-out Register (DTT2)

Index: 346H

Bit	Description	Name	Reset State
0	Device Timer 2 Time-out Select [0]	DEVTMR2SEL0	'0'
1	Device Timer 2 Time-out Select [1]	DEVTMR2SEL1	'0'
2	Device Timer 2 Time-out Select [2]	DEVTMR2SEL2	'0'
3	Device Timer 2 Time-out Select [3]	DEVTMR2SEL3	'0'
4	Device Timer 2 Time-out Prescalar [0]	DEVTMR2PRES0	'0'
5	Device Timer 2 Time-out Prescalar [1]	DEVTMR2PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 2 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 2 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.51 Device Timer 3 Time-out Register (DTT3)

Index: 347H

Bit	Description	Name	Reset State
0	Device Timer 3 Time-out Select [0]	DEVTMR3SEL0	'0'
1	Device Timer 3 Time-out Select [1]	DEVTMR3SEL1	'0'
2	Device Timer 3 Time-out Select [2]	DEVTMR3SEL2	'0'
3	Device Timer 3 Time-out Select [3]	DEVTMR3SEL3	'0'
4	Device Timer 3 Time-out Prescalar [0]	DEVTMR3PRES0	'0'
5	Device Timer 3 Time-out Prescalar [1]	DEVTMR3PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 3 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 3 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.52 Device Timer 4 Time-out Register (DTT4)

Index: 348H

Bit	Description	Name	Reset State
0	Device Timer 4 Time-out Select [0]	DEVTMR4SEL0	'0'
1	Device Timer 4 Time-out Select [1]	DEVTMR4SEL1	'0'
2	Device Timer 4 Time-out Select [2]	DEVTMR4SEL2	'0'
3	Device Timer 4 Time-out Select [3]	DEVTMR4SEL3	'0'
4	Device Timer 4 Time-out Prescalar [0]	DEVTMR4PRES0	'0'
5	Device Timer 4 Time-out Prescalar [1]	DEVTMR4PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 4 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 4 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.53 Device Timer 5 Time-out Register (DTT5)

Index: 349H

Bit	Description	Name	Reset State
0	Device Timer 5 Time-out Select [0]	DEVTMR5SEL0	'0'
1	Device Timer 5 Time-out Select [1]	DEVTMR5SEL1	'0'
2	Device Timer 5 Time-out Select [2]	DEVTMR5SEL2	'0'
3	Device Timer 5 Time-out Select [3]	DEVTMR5SEL3	'0'
4	Device Timer 5 Time-out Prescalar [0]	DEVTMR5PRES0	'0'
5	Device Timer 5 Time-out Prescalar [1]	DEVTMR5PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 5 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 5 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min.	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.54 Device Timer Time-out Source Register 1 (DTTS1)

Index: 34AH

Bit	Description	Name	Reset State
0	Video Activity Device Timer Select [0]	VD_TMRSEL0	'0'
1	Video Activity Device Timer Select [1]	VD_TMRSEL1	'0'
2	Video Activity Device Timer Select [2]	VD_TMRSEL2	'0'
3	Hard Drive 1 Activity Device Timer Select [0]	HD1_TMRSEL0	'0'
4	Hard Drive 1 Activity Device Timer Select [1]	HD1_TMRSEL1	'0'
5	Hard Drive 1 Activity Device Timer Select [2]	HD1_TMRSEL2	'0'
6	Hard Drive 2 Activity Device Timer Select [0]	HD2_TMRSEL0	'0'
7	Hard Drive 2 Activity Device Timer Select [1]	HD2_TMRSEL1	'0'
8	Hard Drive 2 Activity Device Timer Select [2]	HD2_TMRSEL2	'0'
9	Floppy Activity Device Timer Select [0]	FD_TMRSEL0	'0'
10	Floppy Activity Device Timer Select [1]	FD_TMRSEL1	'0'
11	Floppy Activity Device Timer Select [2]	FD_TMRSEL2	'0'
12	Keyboard Activity Device Timer Select [0]	KB_TMRSEL0	'0'
13	Keyboard Activity Device Timer Select [1]	KB_TMRSEL1	'0'
14	Keyboard Activity Device Timer Select [2]	KB_TMRSEL2	'0'
15	Reserved		'0'

Bit **Description**

2:0 **Video Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by video activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Hard Drive 1 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by hard drive 1 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Hard Drive 2 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by hard drive 2 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
11:9	**Floppy Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by floppy activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
14:12	**Keyboard Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by keyboard activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
15	Reserved

4.4.55 Device Timer Time-out Source Register 2 (DTTS2)

Index: 34BH

Bit	Description	Name	Reset State
0	Serial Port 1 Activity Device Timer Select [0]	SIO1_TMRSEL0	'0'
1	Serial Port 1 Activity Device Timer Select [1]	SIO1_TMRSEL1	'0'
2	Serial Port 1 Activity Device Timer Select [2]	SIO1_TMRSEL2	'0'
3	Serial Port 2 Activity Device Timer Select [0]	SIO2_TMRSEL0	'0'
4	Serial Port 2 Activity Device Timer Select [1]	SIO2_TMRSEL1	'0'
5	Serial Port 2 Activity Device Timer Select [2]	SIO2_TMRSEL2	'0'
6	Parallel Port Activity Device Timer Select [0]	PIO_TMRSEL0	'0'
7	Parallel Port Activity Device Timer Select [1]	PIO_TMRSEL1	'0'
8	Parallel Port Activity Device Timer Select [2]	PIO_TMRSEL2	'0'
9	Programmable Range 0 Activity Timer Select [0]	P0_TMRSEL0	'0'
10	Programmable Range 0 Activity Timer Select [1]	P0_TMRSEL1	'0'
11	Programmable Range 0 Activity Timer Select [2]	P0_TMRSEL2	'0'
12	Programmable Range 1 Activity Timer Select [0]	P1_TMRSEL0	'0'
13	Programmable Range 1 Activity Timer Select [1]	P1_TMRSEL1	'0'
14	Programmable Range 1 Activity Timer Select [2]	P1_TMRSEL2	'0'
15	Reserved		'0'

Bit **Description**

2:0 **Serial Port 1 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by serial port 1 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Serial Port 2 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by serial port 2 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Parallel Port Activity Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by parallel port activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
11:9	**Programmable Range 0 Activity Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 0 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
14:12	**Programmable Range 1 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 1 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
15	Reserved

4.4.56 Device Timer Time-out Source Register 3 (DTTS3)

Index: 34CH

Bit	Description	Name	Reset State
0	Programmable Range 2 Activity Timer Select [0]	P2_TMRSEL0	'0'
1	Programmable Range 2 Activity Timer Select [1]	P2_TMRSEL1	'0'
2	Programmable Range 2 Activity Timer Select [2]	P2_TMRSEL2	'0'
3	Programmable Range 3 Activity Timer Select [0]	P3_TMRSEL0	'0'
4	Programmable Range 3 Activity Timer Select [1]	P3_TMRSEL1	'0'
5	Programmable Range 3 Activity Timer Select [2]	P3_TMRSEL2	'0'
6	Programmable Range 4 Activity Timer Select [0]	P4_TMRSEL0	'0'
7	Programmable Range 4 Activity Timer Select [1]	P4_TMRSEL1	'0'
8	Programmable Range 4 Activity Timer Select [2]	P4_TMRSEL2	'0'
9	Programmable Range 5 Activity Timer Select [0]	P5_TMRSEL0	'0'
10	Programmable Range 5 Activity Timer Select [1]	P5_TMRSEL1	'0'
11	Programmable Range 5 Activity Timer Select [2]	P5_TMRSEL2	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

2:0 **Programmable Range 2 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 2 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Programmable Range 3 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 3 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Programmable Range 4 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 4 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
11:9	**Programmable Range 5 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 5 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
15:12	Reserved

4.4.57 Device Timer Time-out Source Register 4 (DTTS4)

Index: 34DH

Bit	Description	Name	Reset State
0	EXTACT0 Device Timer Select [0]	EXT0_TMRSEL0	'0'
1	EXTACT0 Device Timer Select [1]	EXT0_TMRSEL1	'0'
2	EXTACT0 Device Timer Select [2]	EXT0_TMRSEL2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**EXTACT0 Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by EXTACT0 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

15:3	Reserved

4.4.58 LED Indicator Control Register (LEDIC)

Index: 350H

Bit	Description	Name	Reset State
0	LED0 Flasher Enable	LED0FLSHEN	'0'
1	LED0 Flash Rate Selects [0]	FLSHRAT0	'0'
2	LED0 Flash Rate Selects [1]	FLSHRAT1	'0'
3	LED0 Flash Duration [0]	FLSHDUR0	'0'
4	LED0 Flash Duration [1]	FLSHDUR1	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	LED1 Flasher Enable	LED1FSH	'0'
9	LED1 Flash Rate Selects [0]	LED1RAT0	'0'
10	LED1 Flash Rate Selects [1]	LED1RAT1	'0'
11	LED1 Flash Duration [0]	LED1DUR0	'0'
12	LED1 Flash Duration [1]	LED1DUR1	'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

0 — **LED0 Flasher Enable:** '1' = enable; '0' = disable.

2:1 — **LED0 Flash Rate Selects [2:0]:** These bits control the flash rate of the LED0 flasher output while LED0FLSH is high.

NOTE: When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.

Bit [1:0]	LED Flash Rate
0H	0.5 Hz
1H	1 Hz
2H	2 Hz
3H	4 Hz

4:3 — **LED0 Flash Duration:** These bits control the duration of the flasher pulses while LED0FLSH is high.

Bit [1:0]	Flash Duration
0H	256 ms
1H	128 ms
2H	62.5 ms
3H	31.25 ms

NOTE: When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.

7:5 — Reserved

Bit	Description *(cont.)*
8	**LED1 Flasher Enable:** '1' = enable; '0' = disable.
10:9	**LED1 Flash Rate Selects [1:0]:** These bits control the flash rate of the suspend LED flasher output while LED1FLSH is high. **Bit [1:0]** — **LED Flash Rate** 0H — 0.5 Hz 1H — 1 Hz 2H — 2 Hz 3H — 4 Hz
12:11	**LED1 Flash Duration:** These bits control the duration of the suspend flasher pulses while LED1FLSH is high. **Bit [1:0]** — **Flash Duration** 0H — 256 ms 1H — 128 ms 2H — 62.5 ms 3H — 31.25 ms **NOTE:** When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.
15:13	Reserved

4.4.59 Leakage Control Register (LC)

Index: 351H

Bit	Description	Name	Reset State
0	Enable Input Leakage Control	EN_INPUT_LC	'0'
1	Enable Output Leakage Control	EN_OUTPUT_LC	'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Enable Input Leakage Control During 5-V Suspend:** '0' = disable; '1' = enable.
1	**Enable Output Leakage Control During 5-V Suspend:** '0' = disable; '1' = enable.
15:2	Reserved

In V1-LS, when the system enters the STR mode, all signals (except DRAM, PCx, GPIOx, and PM inputs) are leakage-controlled. Leakage control implies:

(i) Input: Isolated from external node; internal node is driven to inactive state.

(ii) Output: Tristated.

(iii) I/O: Output buffer is tristated while input buffer is isolated from external and internal nodes driven to inactive state.

A floating input will not cause leakage current to a leakage-controlled input buffer.

4.4.60 Pin Multiplexing Control Register (PINMUX)

Index: 352H

Bit	Description	Name	Reset State
0	GPIO0 Function [0]	GPIO0_FUNC0	'0'
1	GPIO0 Function [1]	GPIO0_FUNC1	'0'
2	GPIO1 Function [0]	GPIO1_FUNC0	'0'
3	GPIO1 Function [1]	GPIO1_FUNC1	'0'
4	GPIO2 Function [0]	GPIO2_FUNC0	'0'
5	GPIO2 Function [1]	GPIO2_FUNC1	'0'
6	GPIO3 Function [0]	GPIO3_FUNC0	'0'
7	GPIO3 Function [1]	GPIO3_FUNC1	'0'
8	GPIO4 Function [0]	GPIO4_FUNC0	'0'
9	GPIO4 Function [1]	GPIO4_FUNC1	'0'
10	GPIO5 Function [0]	GPIO5_FUNC0	'0'
11	GPIO5 Function [1]	GPIO5_FUNC1	'0'
12	Reserved		'0'
13	PC3 Function	PC3_FUNC	'0'
14	PC4 Function	PC4_FUNC	'0'
15	PC5 Function	PC5_FUNC	'0'

Bit **Description**

1:0 **GPIO0 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO0
'01'	LED0 output
'10'	FLOAT_REQ# input (Rev. BB and later silicon)
'11'	Reserved

3:2 **GPIO1 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO1
'01'	LED1 output
'10'	FLOAT_GNT# output (Rev. BB and later silicon)
'11'	Reserved

5:4 **GPIO2 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO2
'01'	DDMA_RETRY input
'10'	DPSLP_IRQPA input
'11'	Reserved

Bit	Description *(cont.)*	
7:6	**GPIO3 Function [1:0]:**	
	Bit [1:0]	**Function**
	'00'	GPIO3
	'01'	SUPPRESS_RESUME input
	'10'	Reserved
	'11'	Reserved
9:8	**GPIO4 Function [1:0]:**	
	Bit [1:0]	**Function**
	'00'	GPIO4
	'01'	Reserved
	'10'	SUSPA# input (Rev. BB and later silicon)
	'11'	Reserved
11:10	**GPIO5 Function [1:0]:**	
	Bit [1:0]	**Function**
	'00'	GPIO5
	'01'	Reserved
	'10'	THERM input active-high
	'11'	THERM input active-low
12	Reserved	
13	**PC3 Function:** '0' = PC3; '1' = LED0 output.	
14	**PC4 Function:** '0' = PC4; '1' = LED1 output.	
15	**PC5 Function:** '0' = PC5; '1' = Reserved	

4.4.61 Debounce Control Register (DBC)

Index: 353H

Bit	Description	Name	Reset State
0	SWTCH Debounce Select	SWTCH_DBSEL	'1'
1	WAKE0 Debounce Select	WAKE0_DBSEL	'1'
2	WAKE1 Debounce Select	WAKE1_DBSEL	'1'
3	RING Debounce Select	RING_DBSEL	'1'
4	EXTACT0 Debounce Select	EXT0_DBSEL	'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**SWTCH Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
1	**WAKE0 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
2	**WAKE1 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
3	**RING Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
4	**EXTACT0 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
15:5	Reserved

4.4.62 Edge Detect Control Register (EDC)

Index: 354H

Bit	Description	Name	Reset State
0	SWTCH Edge Detect [0]	SWTCHEGDT0	'0'
1	SWTCH Edge Detect [1]	SWTCHEGDT1	'1'
2	WAKE0 Edge Detect [0]	WAKE0EGDT0	'0'
3	WAKE0 Edge Detect [1]	WAKE0EGDT1	'1'
4	WAKE1 Edge Detect [0]	WAKE1EGDT0	'0'
5	WAKE1 Edge Detect [1]	WAKE1EGDT1	'1'
6	RING Edge Detect [0]	RINGEGDT0	'0'
7	RING Edge Detect [1]	RINGEGDT1	'1'
8	EXTACT0 Edge Detect [0]	EXTACT0EGDT0	'0'
9	EXTACT0 Edge Detect [1]	EXTACT0EGDT1	'1'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
1:0	**SWTCH Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description
3:2	**WAKE0 Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description
5:4	**WAKE1 Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description *(cont.)*
7:6	**RING Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Reserved

Bit	Description *(cont.)*
9:8	**EXTACT0 Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description *(cont.)*
15:10	Reserved

NOTE: Edge Detect Register selects the edge that is detected as toggling to trigger either a primary activity, secondary activity, SMI or Wakeup events.

4.5 Level-2 Cache Registers

4.5.1 Level-2 Cache Configuration Register (L2C)

Index: 400H

Bit	Description	Name	Reset State
0	L2 Cache Enable	L2EN	'0'
1	L2 Cache Size Select [0]	L2SIZE0	'1'
2	L2 Cache Size Select [1]	L2SIZE1	'0'
3	L2 Cache Size Select [2]	L2SIZE2	'0'
4	L2 Cache Type [0]	L2TYPE0	'0'
5	L2 Cache Type [1]	L2TYPE1	'0'
6	Reserved		'0'
7	Enable Pipelined Burst SRAM	EN_PIPE_SRAM	'0'
8	Select NALE Mode	SEL_NALE	'0'
9	Enable TAG Initialization	EN_TAG_INIT	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

0 — **L2 Cache Enable:** '0' = disable; '1' = enable.

3:1 — **L2 Cache Size Select:**

Bit [2:0]	L2 Cache Size
'000'	128 Kbytes
'001'	256 Kbytes
'010'	512 Kbytes
'011'	1 Mbyte
All others	Reserved

5:4 — **L2 Cache Type [1:0]:**

Bit [2:0]	L2 Cache Type
'00'	Standard asynchronous
'01'	Standard synchronous (both sync burst and pipelined burst)
'10'	Reserved
'11'	Reserved

6 — Reserved

7 — **Enable Pipelined Burst SRAM:** '0' = disable; '1' = enable. This bit is effective only if bit [5:4] = 01H.

Bit	Description *(cont.)*
8	**Select NALE Mode:** '0' = TAGCS#/NALE# pin is in TAGCS# mode. '1' = TAGCS#/NALE# pin is in NALE# mode.
9	**Enable TAG Initialization:** '0' = disable; '1' = enable.
15:10	Reserved

4.5.2 Level-2 Cache Timing Register (L2T)

Index: 401H

Bit	Description	Name	Reset State
0	L2 Cache Read Leadoff [0]	L2RDLDOF0	'0'
1	L2 Cache Read Leadoff [1]	L2RDLDOF1	'0'
2	L2 Cache Read Follow-on [0]	L2RDFLWON0	'0'
3	L2 Cache Read Follow-on [1]	L2RDFLWON1	'0'
4	L2 Cache Write Leadoff [0]	L2WRLDOF0	'0'
5	L2 Cache Write Leadoff [1]	L2WRLDOF1	'0'
6	L2 Cache Write Follow-on [0]	L2WRFLWON0	'0'
7	L2 Cache Write Follow-on [1]	L2WRFLWON1	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

1:0 **L2 Cache Read Leadoff:**

Bit [1:0]	Cycle Time
'00'	2T
'01'	3T
'10'	4T
'11'	Reserved

3:2 **L2 Cache Read Follow-on:**

Bit [1:0]	Cycle Time
'00'	1T
'01'	Reserved
'10'	Reserved
'11'	Reserved

5:4 **L2 Cache Write Leadoff:**

Bit [1:0]	Cycle Time
'00'	2T
'01'	3T
'10'	4T
'11'	Reserved

Bit	Description *(cont.)*
7:6	**L2 Cache Write Follow-on:** **Bit [1:0]** — **Cycle Time** '00' — 1T '01' — Reserved '10' — Reserved '11' — Reserved
15:8	Reserved

4.5.3 Level-2 Cache Miscellaneous Register (L2M)

Index: 402H

Bit	Description	Name	Reset State
0	Dead Clock Enable	DEAD_CLK_EN	'0'
1	Disable Invalidation of ROM Address	DIS_INVD_ROM_ ADDR	'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Advanced Synchronous Power Enhanced Cache Timing (ASPECT)	ASPECT	'0'
7	Disable Power Management on CE# only for 50-MHz Operation	DIS_CE_PM	'0'
8	Enable the Pipeline of Memory Read-Miss Cycle [0]	EN_PIPE_RDMISS0	'0'
9	Enable the Pipeline of Memory Read-Miss Cycle [1]	EN_PIPE_RDMISS1	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Dead Clock Enable:** When set to '0', there is no dead clock when there is a L2 read followed by a L2 write or vice versa. When '1', a dead clock will be inserted whenever there is a L2 read followed by a L2 write or vice versa.
1	**Disable Invalidation of ROM address:** '0' = enable; '1' = disable.
5:2	Reserved
6	**Advanced Synchronous Power Enhanced Cache Timing (ASPECT):** When enabled, clock to L2-cache will be turned off during bus idle condition. '0' = disable; '1' = enable.
7	**Disable Power Management on CE# only for 50-MHz Operation:** '0' = enable; '1' = disable.

Bit	Description *(cont.)*
9:8	**Enable the Pipeline of Memory Read-Miss Cycle [1:0]:** **Bit [1:0] — Mode** 'X0' (Rev. BB and later) — Disable Pipeline on Read-Miss Cycle '01' (Rev. BB and later) — Enable Pipeline on Read-Miss Cycle; 'NA' will be generated at the same time as the first BRDY#. '11' (Rev. BB and later) — Enable Pipeline on Read-Miss Cycle; 'NA' will be generated as soon as the internal read request is recognized.
15:10	Reserved

4.6 PCI Configuration Registers

NOTE: The following PCI registers are accessed through the PCI configuration space through I/O addresses 0CF8H and 0CFCH.

4.6.1 Vendor ID Register (VID)

Index: 00H

Bit	Description	Name	Reset State
0	Vendor ID Number [0]	VENDOR_ID0	'0'
1	Vendor ID Number [1]	VENDOR_ID1	'1'
2	Vendor ID Number [2]	VENDOR_ID2	'1'
3	Vendor ID Number [3]	VENDOR_ID3	'0'
4	Vendor ID Number [4]	VENDOR_ID4	'0'
5	Vendor ID Number [5]	VENDOR_ID5	'1'
6	Vendor ID Number [6]	VENDOR_ID6	'1'
7	Vendor ID Number [7]	VENDOR_ID7	'0'
8	Vendor ID Number [8]	VENDOR_ID8	'0'
9	Vendor ID Number [9]	VENDOR_ID9	'0'
10	Vendor ID Number [10]	VENDOR_ID10	'0'
11	Vendor ID Number [11]	VENDOR_ID11	'0'
12	Vendor ID Number [12]	VENDOR_ID12	'1'
13	Vendor ID Number [13]	VENDOR_ID13	'0'
14	Vendor ID Number [14]	VENDOR_ID14	'0'
15	Vendor ID Number [15]	VENDOR_ID15	'0'

Bit	Description
15:0	**Vendor ID Number [15:0]:** These bits are hardwired to 1066H.

4.6.2 Device ID Register (DID)

Index: 02H

Bit	Description	Name	Reset State
0	Device ID Number [0]	Device_ID0	'1'
1	Device ID Number [1]	Device_ID1	'0'
2	Device ID Number [2]	Device_ID2	'0'
3	Device ID Number [3]	Device_ID3	'0'
4	Device ID Number [4]	Device_ID4	'0'
5	Device ID Number [5]	Device_ID5	'0'
6	Device ID Number [6]	Device_ID6	'0'
7	Device ID Number [7]	Device_ID7	'0'
8	Device ID Number [8]	Device_ID8	'0'
9	Device ID Number [9]	Device_ID9	'0'
10	Device ID Number [10]	Device_ID10	'0'
11	Device ID Number [11]	Device_ID11	'0'
12	Device ID Number [12]	Device_ID12	'0'
13	Device ID Number [13]	Device_ID13	'0'
14	Device ID Number [14]	Device_ID14	'0'
15	Device ID Number [15]	Device_ID15	'0'

Bit	Description
15:0	**Device ID Number [15:0]:** These bits are hardwired. V1-LS = 0001H

4.6.3 Command Register (COMMD)

Index: 04H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Memory Space Enable	MEM_RESPOND	'1'
2	Reserved		'1'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Parity Error Response	PARERR_REP	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	Reserved
1	**Memory Space Enable:** When '0', PCI master access to main memory is disabled. When '1', PCI master access to main memory is enabled.
5:2	Reserved
6	**Parity Error Response:** When '1', V1-LS will assert PERR# when a PCI parity error is detected. When '0', V1-LS will not assert PERR# when a PCI parity error is detected.
15:7	Reserved

4.6.4 Status Register (STAT)

Index: 06H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	DEVSEL Timing [0]	DEVSEL_TIM0	'0'
10	DEVSEL Timing [1]	DEVSEL_TIM1	'1'
11	Reserved		'0'
12	Receive Target Abort	REC_TAG_ABRT	'0'
13	Receive Master Abort	REC_MST_ABRT	'0'
14	Reserved		'0'
15	Detect Parity Error	DET_PAR_ERR	'0'

Bit	Description
8:0	Reserved
10:9	**DEVSEL Timing:** These bits indicate the slowest time that V1-LS will return DEVSEL#. These bits are hardwired to 'slow' timing.
11	Reserved
12	**Receive Target Abort:** Reading a '1' indicates receiving a target abort condition. This bit can be reset by writing a '1'.
13	**Receive Master Abort:** Reading a '1' indicates receiving a master abort condition (does not include master abort generated from a special cycle). This bit can be reset by writing a '1'.
14	Reserved
15	**Detect Parity Error:** When V1-LS detects a PCI parity error, this bit will be set to '1'. This bit can be reset by writing a '1'.

4.6.5 Revision ID Register (RID)

Index: 08H

Bit	Description	Name	Reset State
0	Revision ID Number [0]	REVISION_ID0	'0'
1	Revision ID Number [1]	REVISION_ID1	'0'
2	Revision ID Number [2]	REVISION_ID2	'0'
3	Revision ID Number [3]	REVISION_ID3	'0'
4	Revision ID Number [4]	REVISION_ID4	'0'
5	Revision ID Number [5]	REVISION_ID5	'0'
6	Revision ID Number [6]	REVISION_ID6	'0'
7	Revision ID Number [7]	REVISION_ID7	'0'

Bit	Description
7:0	**Revision ID Number [7:0]:** These bits are hardwired.

Bit [3:0]	Revision ID
3H	AA
4H	BB
5H	CC

4.6.6 Class Register (CLASS)

Index: 09H

Bit	Description	Name	Reset State
0	Class Code [0]	CLASS_CODE0	'0'
1	Class Code [1]	CLASS_CODE1	'0'
2	Class Code [2]	CLASS_CODE2	'0'
3	Class Code [3]	CLASS_CODE3	'0'
4	Class Code [4]	CLASS_CODE4	'0'
5	Class Code [5]	CLASS_CODE5	'0'
6	Class Code [6]	CLASS_CODE6	'0'
7	Class Code [7]	CLASS_CODE7	'0'
8	Class Code [8]	CLASS_CODE8	'0'
9	Class Code [9]	CLASS_CODE9	'0'
10	Class Code [10]	CLASS_CODE10	'0'
11	Class Code [11]	CLASS_CODE11	'0'
12	Class Code [12]	CLASS_CODE12	'0'
13	Class Code [13]	CLASS_CODE13	'0'
14	Class Code [14]	CLASS_CODE14	'0'
15	Class Code [15]	CLASS_CODE15	'0'
16	Class Code [16]	CLASS_CODE16	'0'
17	Class Code [17]	CLASS_CODE17	'1'
18	Class Code [18]	CLASS_CODE18	'1'
19	Class Code [19]	CLASS_CODE19	'0'
20	Class Code [20]	CLASS_CODE20	'0'
21	Class Code [21]	CLASS_CODE21	'0'
22	Class Code [22]	CLASS_CODE22	'0'
23	Class Code [23]	CLASS_CODE23	'0'

Bit	Description
23:0	**Class Code [23:0]:** These bits are hardwired to 060000H.

4.6.7 Latency Timer Register (LTMR)

Index: 0DH

Bit	Description	Name	Reset State
0	Latency Timer [0]	LAT_TIM0	'0'
1	Latency Timer [1]	LAT_TIM1	'0'
2	Latency Timer [2]	LAT_TIM2	'0'
3	Latency Timer [3]	LAT_TIM3	'0'
4	Latency Timer [4]	LAT_TIM4	'0'
5	Latency Timer [5]	LAT_TIM5	'0'
6	Latency Timer [6]	LAT_TIM6	'0'
7	Latency Timer [7]	LAT_TIM7	'0'

Bit	Description
7:0	**Latency Timer [7:0]:** These bits are hardwired to 00H.

5. V1-LS ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5-1. Maximum Ratings

Condition	Maximum Rating
Ambient temperature	0^o - 70^o C
Storage temperature	-65^o to $+150^o$ C
Supply voltage to ground potential	3.135-V to 3.6-V (for 3-V design) 4.5-V to 5.5-V (for 5-V design)
Applied output voltage	-0.3 to V_{DD} + 0.3V
Applied input voltage	-0.3 to V_{DD} + 0.3V
Operating power dissipation	1 W

5.2 D.C. Characteristics 5.0 Volt

V_{DD} = 5-V ± 10% @ 50 MHz; T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{DD}	Power supply voltage	4.75	5.25	V	Normal operation
V_{IL}	Input low voltage (TTL)	-0.5	0.8	V	
V_{ILC}	Input low voltage (CMOS)	-0.5	0.3 * V_{DD}	V	
V_{ILP}	Input low voltage (PCI)	-0.5	0.8	V	
V_{IH}	Input high voltage (TTL)	2.2	V_{DD} + 0.5	V	
V_{IHC}	Input high voltage (CMOS)	0.7 * V_{DD}	V_{DD} + 0.5	V	
V_{IHP}	Input high voltage (PCI)	2.0	V_{DD} + 0.5	V	
V_{OH}	Output high voltage (TTL)	3.7		V	
V_{OHC}	Output high voltage (CMOS)	V_{DD} - 0.2		V	
V_{OHP}	Output high voltage (PCI)	2.4		V	I_{OUT} = -2 mA
V_{OL}	Output low voltage (TTL)		0.4	V	
V_{OLC}	Output low voltage (CMOS)		0.2	V	
V_{OLP}	Output low voltage (PCI)		0.55	V	I_{OUT} = 6 mA
I_{CC}	Power supply current		300	mA	
I_L	Input leakage current		1.0	µA	
I_{OZ}	Tristate leakage current		10.0	µA	
C_{IN}	Input capacitance	5.0	10.0	pF	
C_{OUT}	Output capacitance	5.0	10.0	pF	

5.3 D.C. Characteristics 3.3 Volt

V_{DD} = 3.3-V ± 10% @ 50 MHz; T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{DD}	Power supply voltage	3.135	3.6	V	Normal operation
V_{IL}	Input low voltage (TTL)	-0.3	0.8	V	
V_{ILC}	Input low voltage (CMOS)	-0.3	0.3 * V_{DD}	V	
V_{ILP}	Input low voltage (PCI)	-0.5	0.325 * V_{DD}	V	
V_{IH}	Input high voltage (TTL)	2.0	V_{DD} + 0.3	V	
V_{IHC}	Input high voltage (CMOS)	0.7 * V_{DD}	V_{DD} + 0.3	V	
V_{IHP}	Input high voltage (PCI)	0.475 * V_{DD}	V_{DD} + 0.5	V	
V_{OH}	Output high voltage (TTL)	2.4		V	
V_{OHC}	Output high voltage (CMOS)	V_{DD} - 0.2		V	
V_{OHP}	Output high voltage (PCI)	0.9 * V_{DD}		V	I_{OUT} = -500 µA
V_{OL}	Output low voltage (TTL)		0.4	V	
V_{OLC}	Output low voltage (CMOS)		0.2	V	
V_{OLP}	Output low voltage (PCI)		0.1 * V_{DD}	V	I_{OUT} = 1500 µA
I_{CC}	Power supply current		300	mA	
I_L	Input leakage current		1.0	µA	
I_{OZ}	Tristate leakage current		10.0	µA	
C_{IN}	Input capacitance	5.0	10.0	pF	
C_{OUT}	Output capacitance	5.0	10.0	pF	

5.4 A.C. Characteristics

Table 5-2. V1-LS AC Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes
PCI Timing					
t_{100a}	PCICLK to Signal Valid Delay - bussed signals	2	11	ns	1
t_{100b}	PCICLK to Signal Valid Delay - point to point	2	12	ns	1
t_{101}	Float to Active Delay	2		ns	1
t_{102}	Active to Float Delay		28	ns	1
t_{103a}	Input Set up Time to PCICLK - bussed signals	7		ns	
t_{103b}	Input Set up Time to PCICLK - point to point	12		ns	
t_{104}	Input Hold Time from PCICLK	0		ns	
CPU Timing					
t_{200h}	Hold Time: BE[7:0]#, D/C#, W/R#, CACHE#, A[31:3], LOCK#, ADS#, M/IO# to CPUCLK	1		ns	3
t_{200s}	Set Up time: BE[7:0]#, D/C#, W/R#, CACHE#, A[31:3], LOCK#, ADS#, M/IO# to CPUCLK		7	ns	3
t_{201h}	Hold Time: FERR#, SMIACT# to CPUCLK	1		ns	3
t_{201s}	Set Up Time: FERR#, SMIACT# to CPUCLK		6	ns	3
t_{202h}	Hold time: HLDA, HITM# to CPUCLK	1		ns	3
t_{202s}	Set Up Time: HLDA, HITM# to CPUCLK		8.0	ns	3
t_{203h}	Hold Time: D[63:0] to V2CLK	1.3		ns	3
t_{203s}	Set Up Time: D[63:0] to V2CLK		6	ns	3
t_{204}	CPUCLK to A[31:3], EADS# Valid Delay	2	8	ns	3
t_{205}	CPUCLK to INV, KEN#, NA#, WB/WT#, BRDY#, AHOLD, BOFF#, HOLD, A20M#, INTR, STPCLK#, INIT, NMI, SMI#, IGNNE# Valid Delay	2	9	ns	3
t_{206}	V2CLK to D[63:0] Valid Delay	2	11	ns	3
L2 Cache Timing					
t_{300}	CPUCLK to ADSC#, ADV# Valid Delay		11	ns	5

Table 5-2. V1-LS AC Timing Parameters *(cont.)*

Symbol	Parameter	Min	Max	Unit	Notes
t_{301}	CPUCLK to CWE[7:0]# Valid Delay		11	ns	2
t_{302}	CPUCLK to TAGD[7:0] Valid Delay	5	30	ns	4
t_{303}	CPUCLK to TAGWE# Valid Delay	2	13	ns	2
t_{304}	CPUCLK to COE# Valid Delay		9	ns	5
DRAM Timing					
t_{400}	CPUCLK to WE# Valid Delay		15	ns	6
t_{401}	CPUCLK to RAS#, CAS# Valid Delay (for both rising and falling edges)		10	ns	2
t_{402}	CPUCLK to MA Valid Delay		14	ns	6
t_{403}	V2CLK to MD Valid Delay (for both rising and falling edges)		14	ns	4
t_{404}	MD setup time to V2CLK		2	ns	4
t_{405}	V1-LS: BC[2:0], BD[7:0] output delay from V2CLK		9	ns	2
t_{406}	BD[7:0] setup time to V2CLK		3	ns	2
t_{407}	V2-LS: BD[7:0] output delay from V2CLK		9.5	ns	2
t_{408}	V2-LS: BD[7:0] setup time to V2CLK		5	ns	2
t_{409}	V1-LS: ADOE# output delay from PCICLK		8.5	ns	2

NOTES:

1) Minimum times are measured with 0 pF equivalent load; maximum times are measured with 50 pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
2) Measured with 15 pF equivalent load.
3) Measured with 20 pF equivalent load.
4) Measured with 25 pF equivalent load.
5) Measured with 35 pF equivalent load.
6) Measured with 60 pF equivalent load.

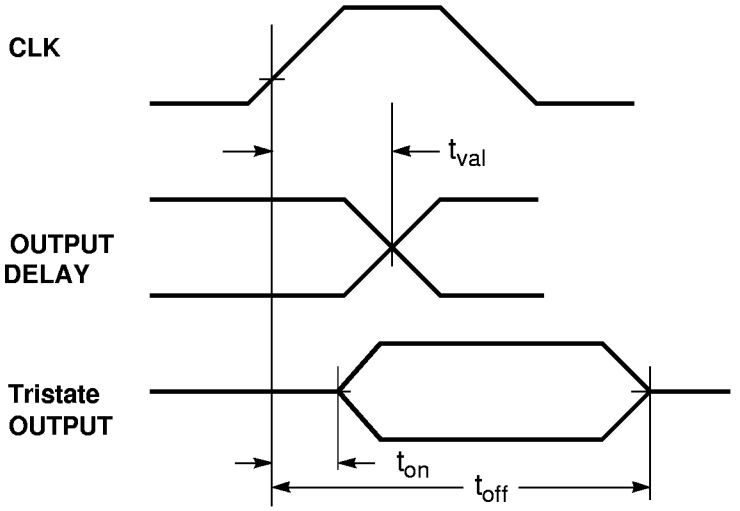


Figure 5-1. Output Timing Measurement Conditions

$t_{val} = t_{100a}, t_{100b}, t_{204}, t_{205}, t_{206}, t_{300} - t_{304}, t_{400} - t_{403}, t_{405}, t_{407}, t_{409}$

$t_{on} = t_{101}$

$t_{off} = t_{102}$

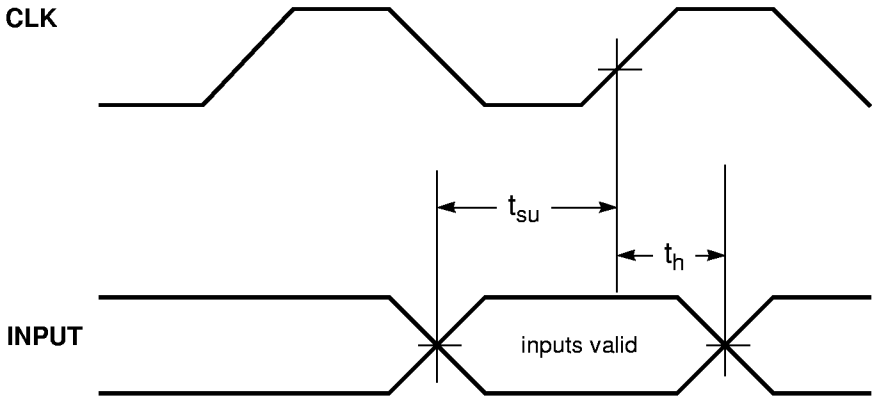


Figure 5-2. Input Timing Measurement Conditions

$t_{su} = t_{103a}, t_{103b}, t_{200s} - t_{203s}, t_{403}, t_{406}, t_{408}$

$t_h = t_{104}, t_{200h} - t_{203h}$

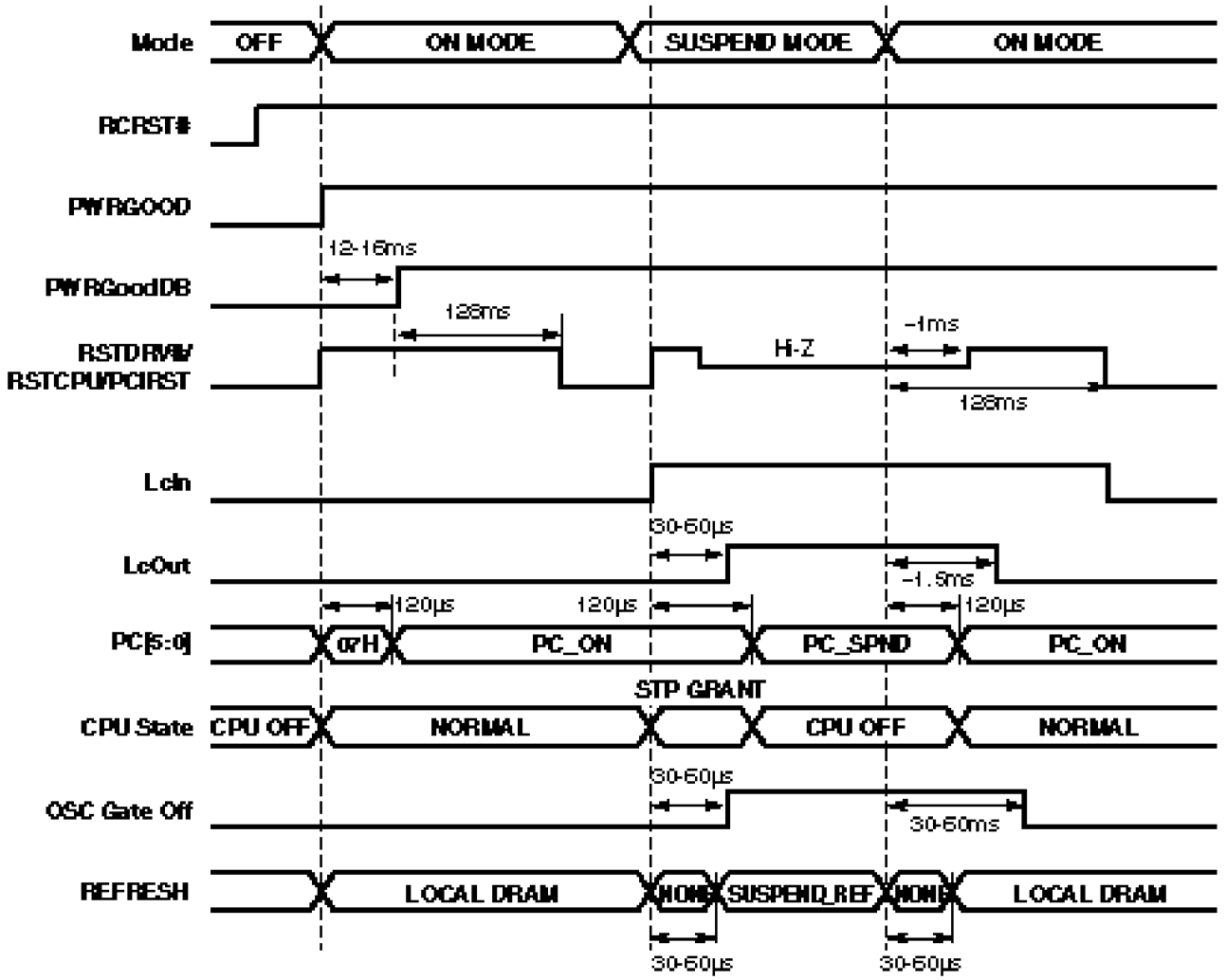


Figure 5-3. Power-On/5-V Suspend Timing Diagram

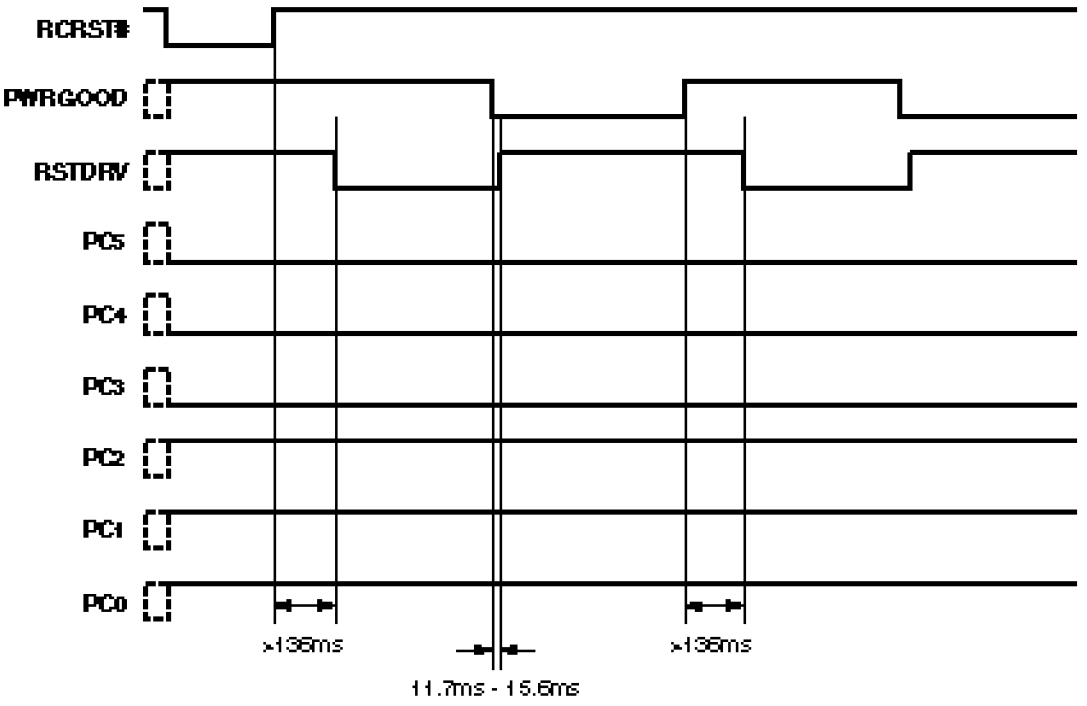


Figure 5-4. Reset Timing

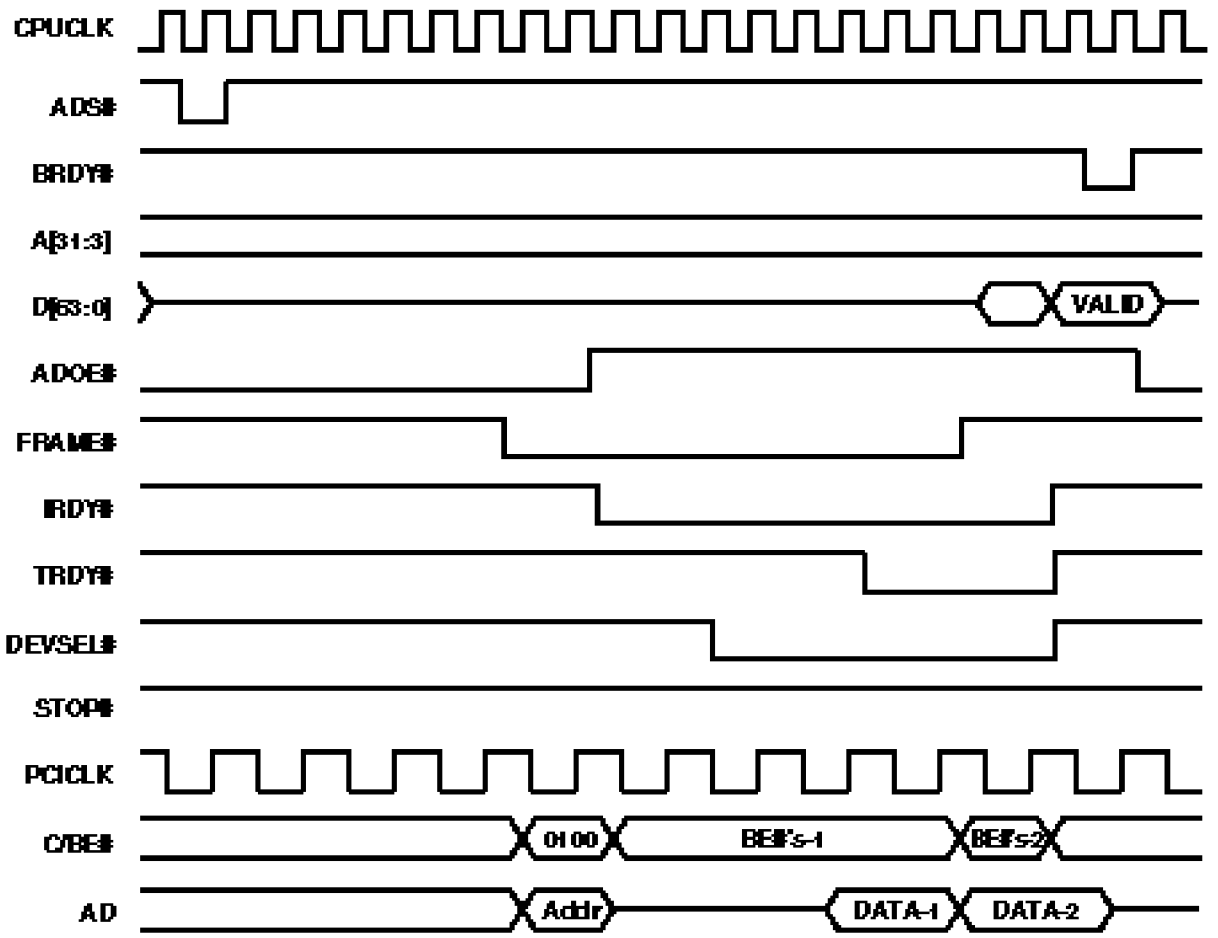


Figure 5-5. CPU-to-PCI Memory Burst Read Cycle

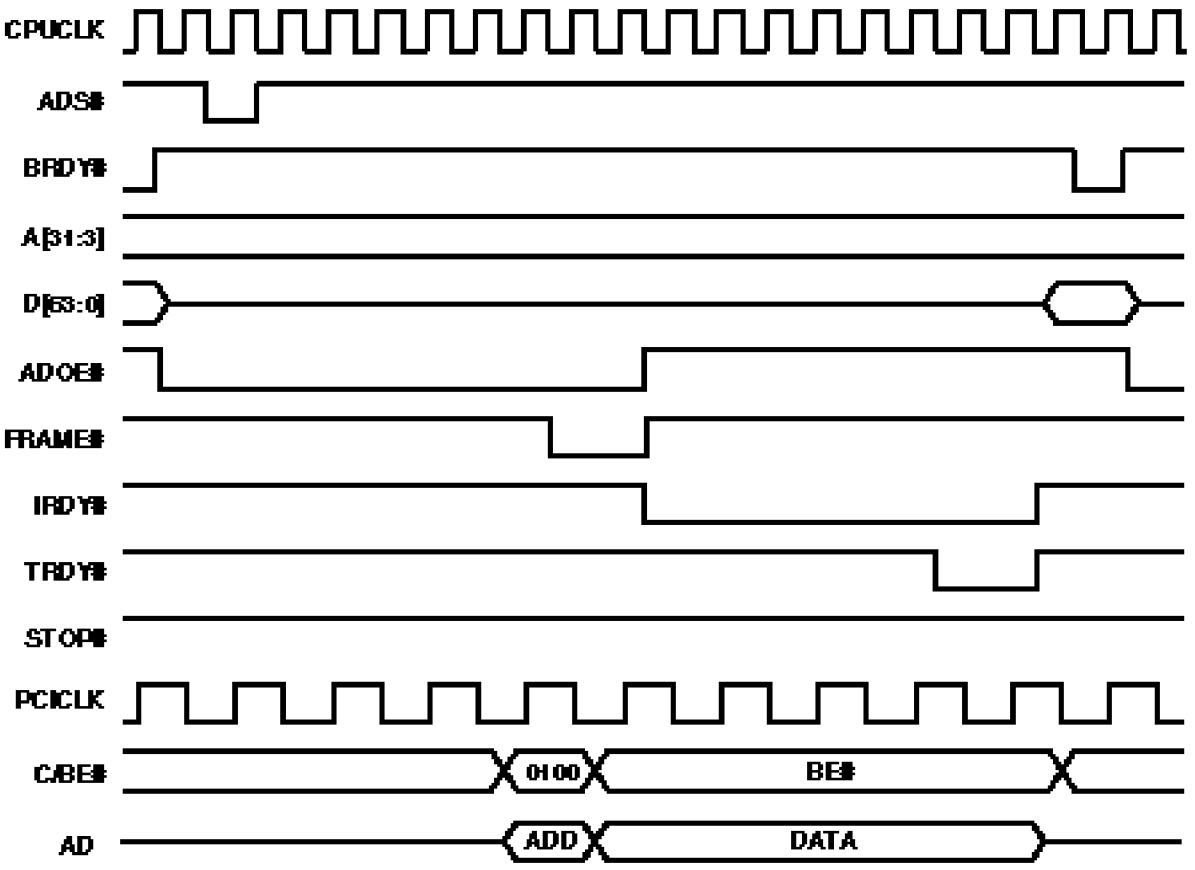


Figure 5-6. CPU-to-PCI Memory Read Cycle

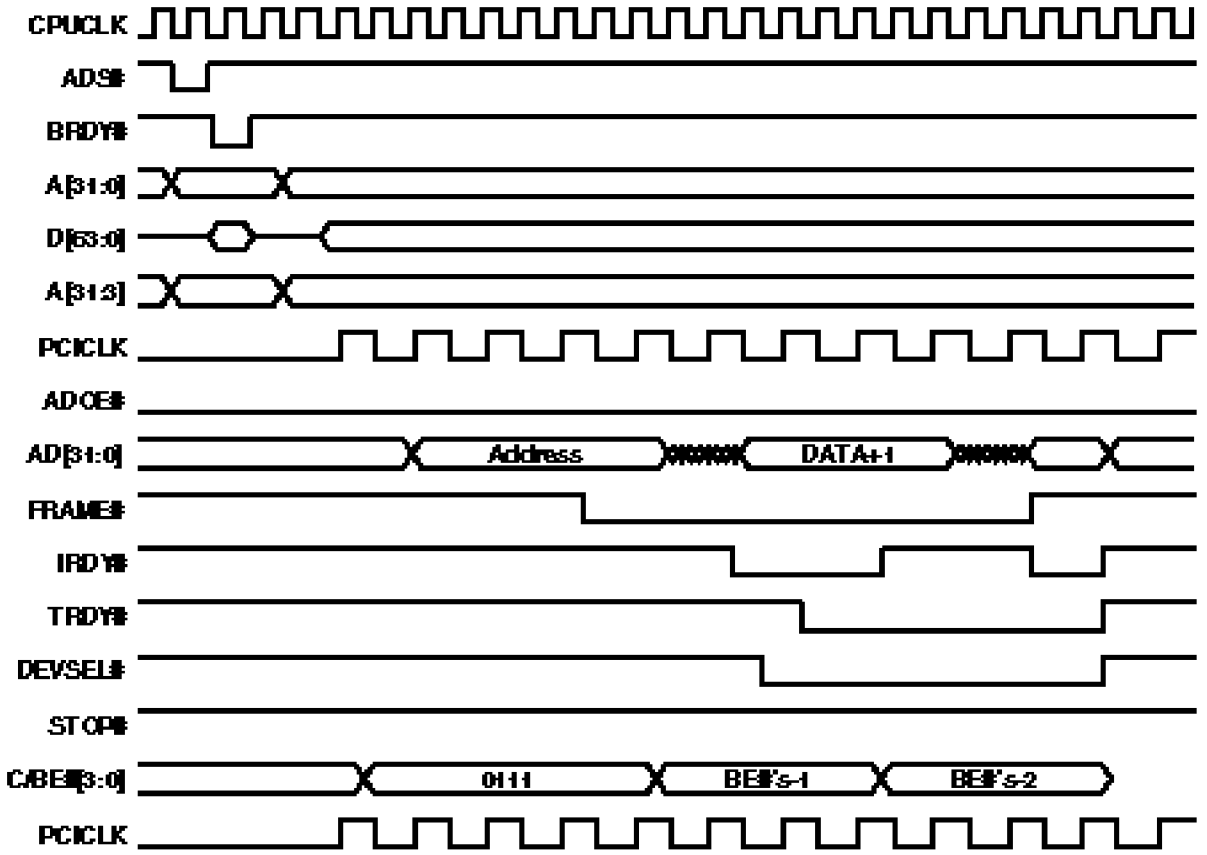


Figure 5-7. CPU-to-PCI Memory Write Cycle

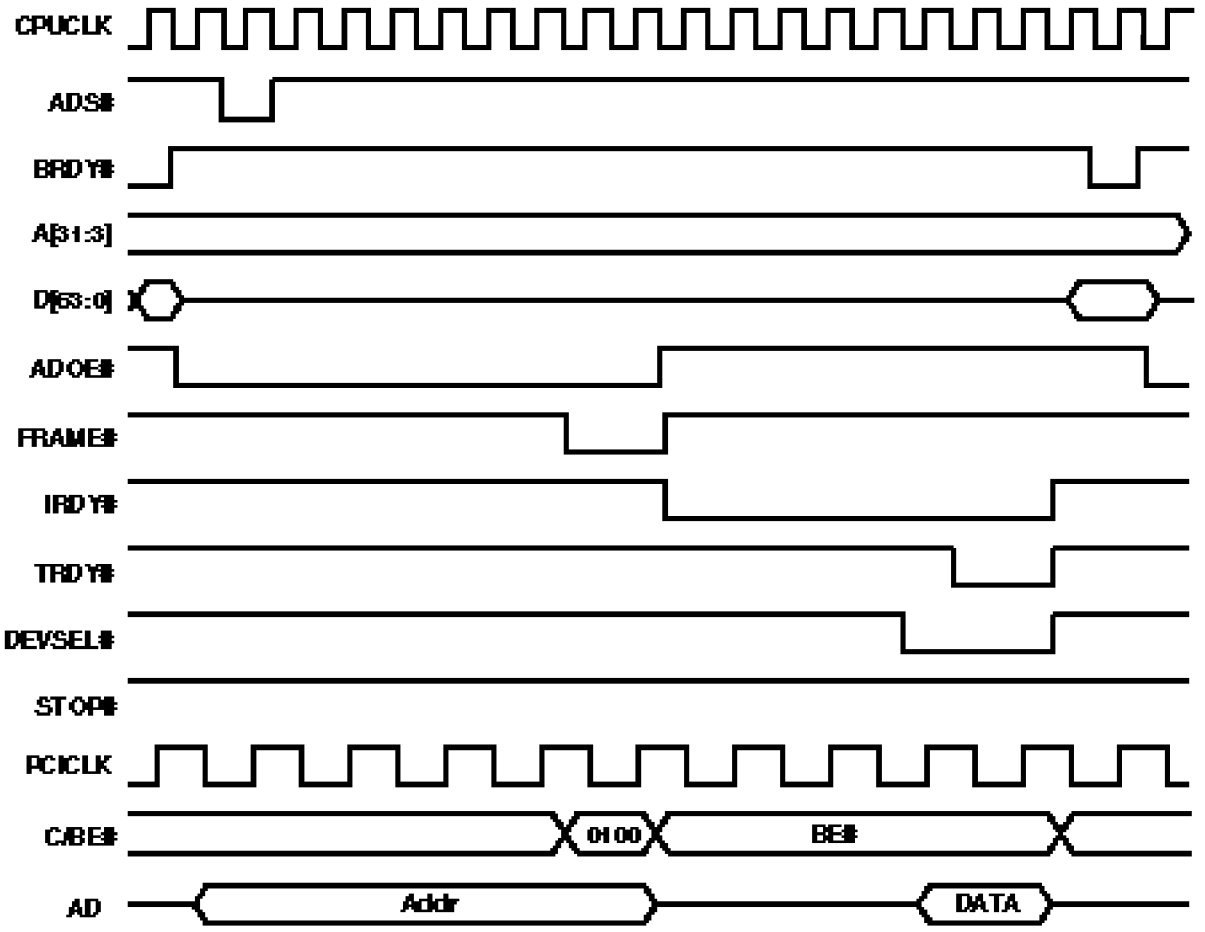


Figure 5-8. CPU-to-PCI I/O Read Cycle

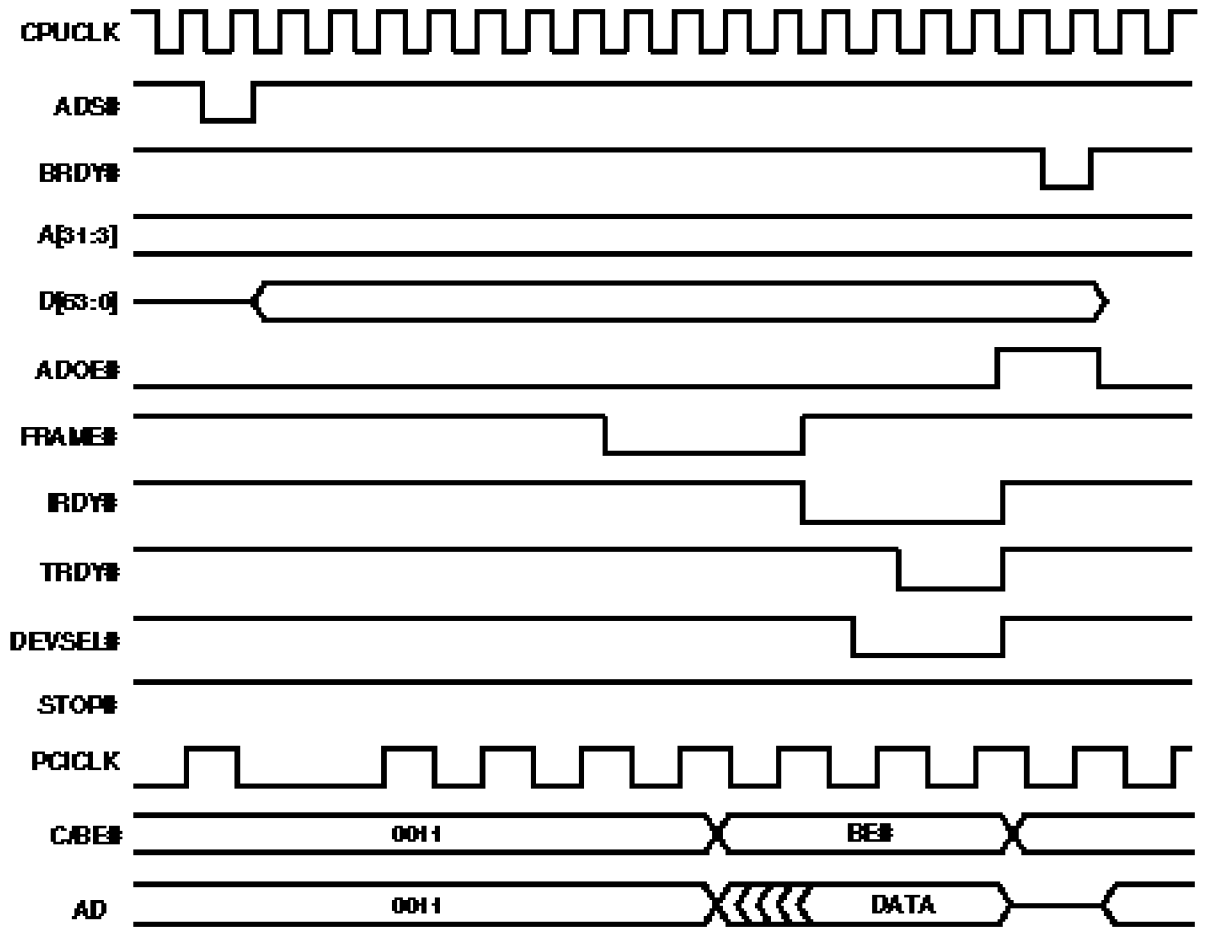


Figure 5-9. CPU-to-PCI I/O Write Cycle

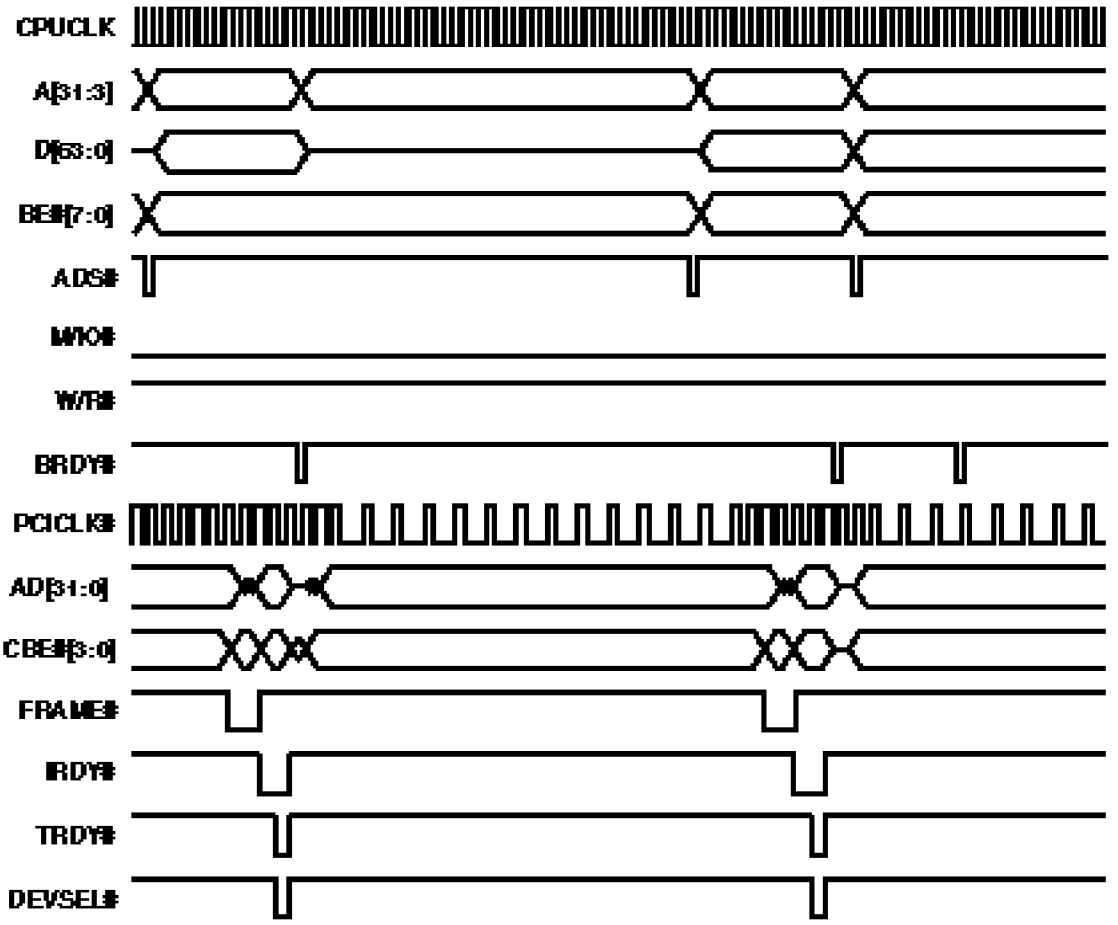


Figure 5-10. PicoPower PCICLK Control Scheme

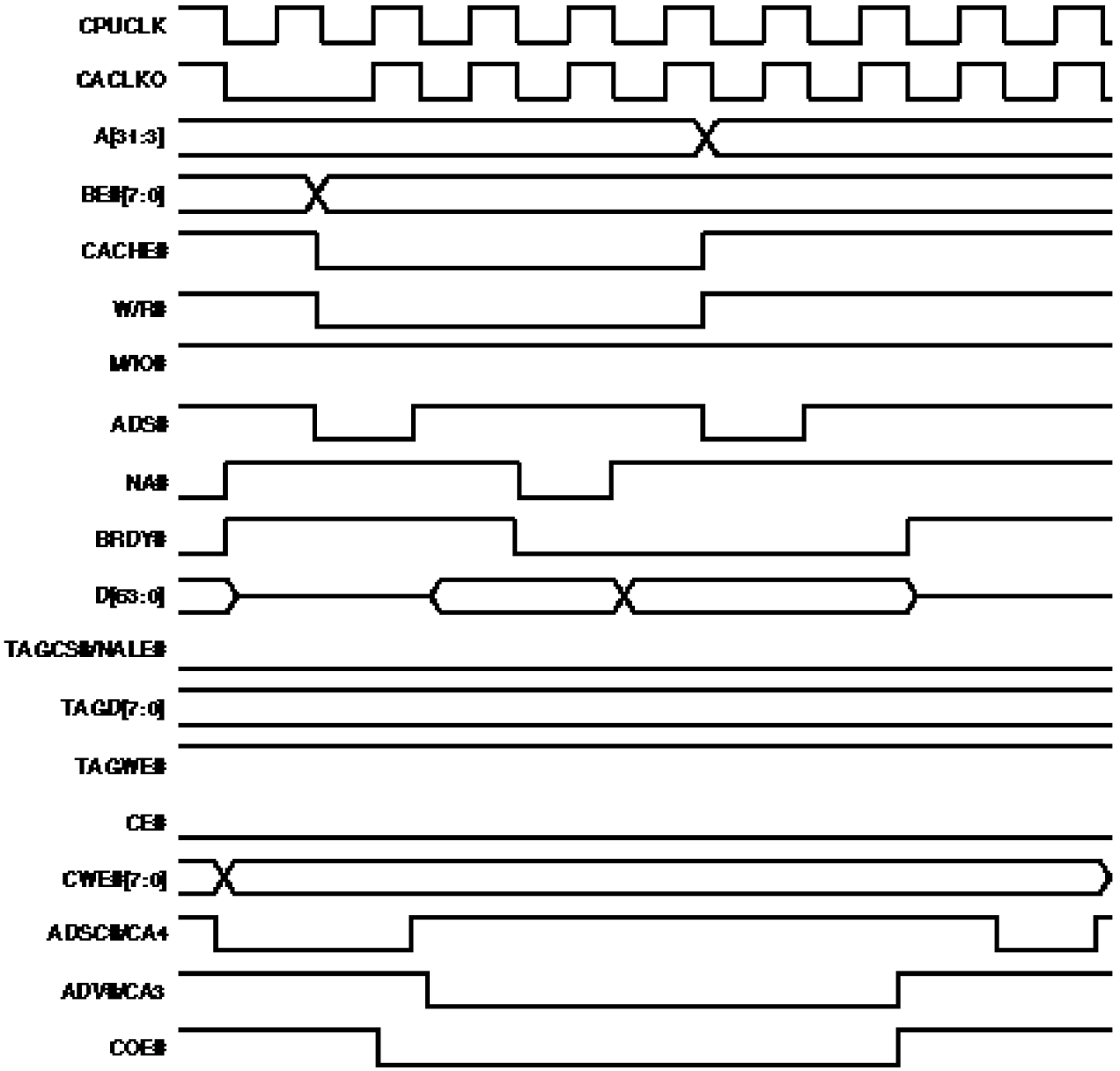


Figure 5-11. L2 Cache – Pipeline Synchronous, Single Read Hit

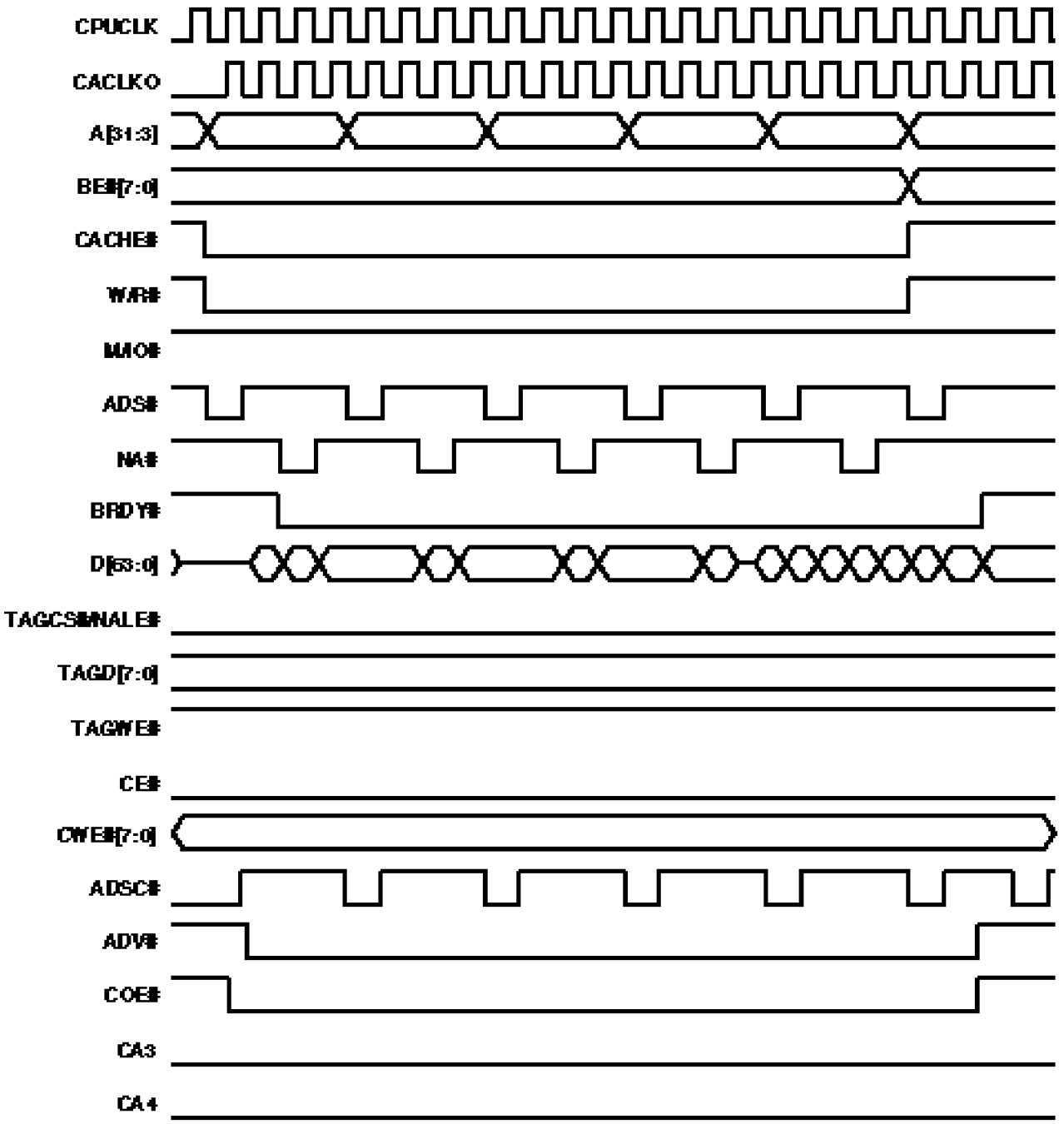


Figure 5-12. L2 Cache – Pipeline Synchronous, Multiple Read Hit

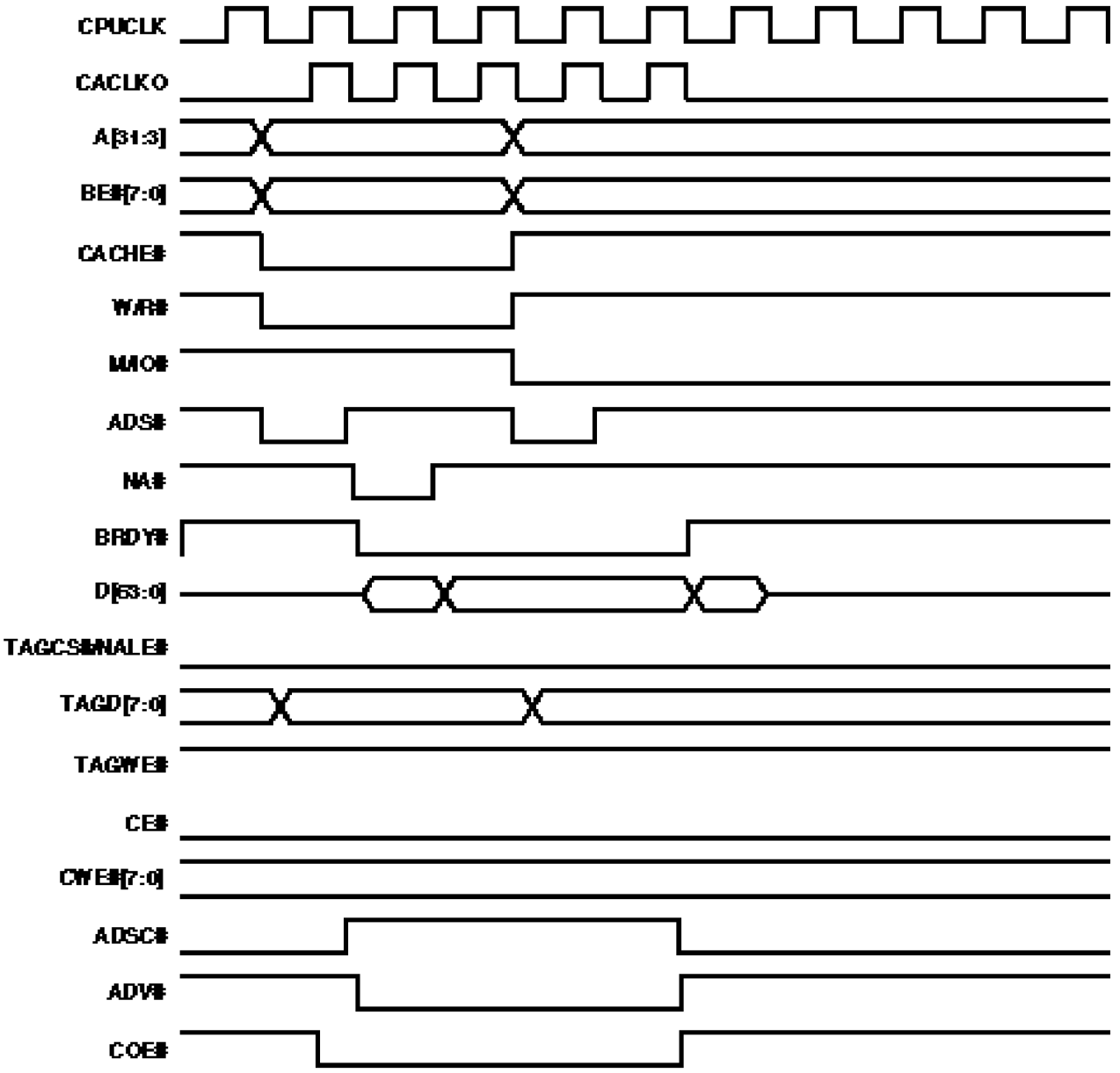


Figure 5-13. L2 Cache – Pipeline Synchronous Burst Read Hit

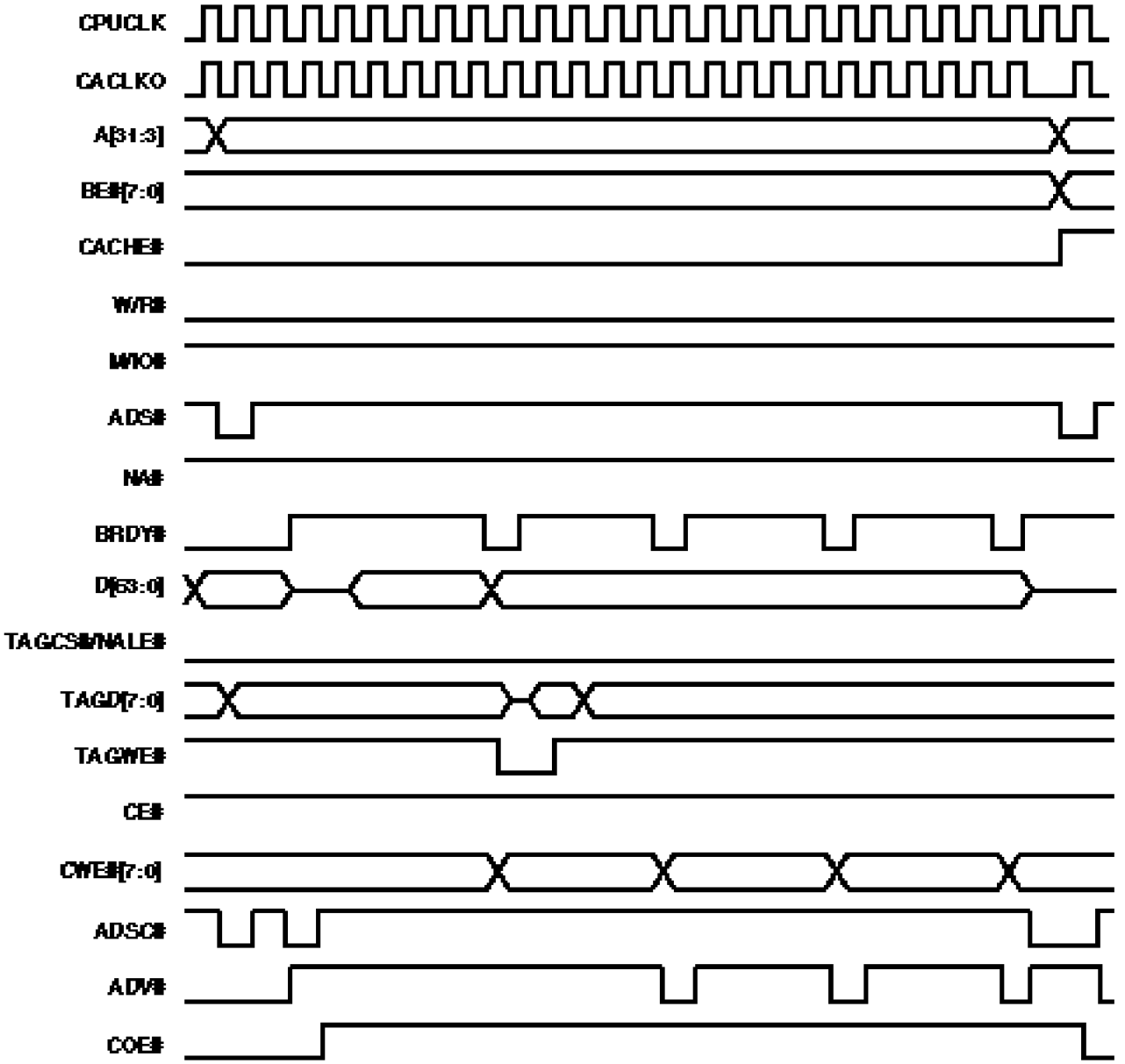


Figure 5-14. L2 Cache – Pipeline Synchronous Read Miss

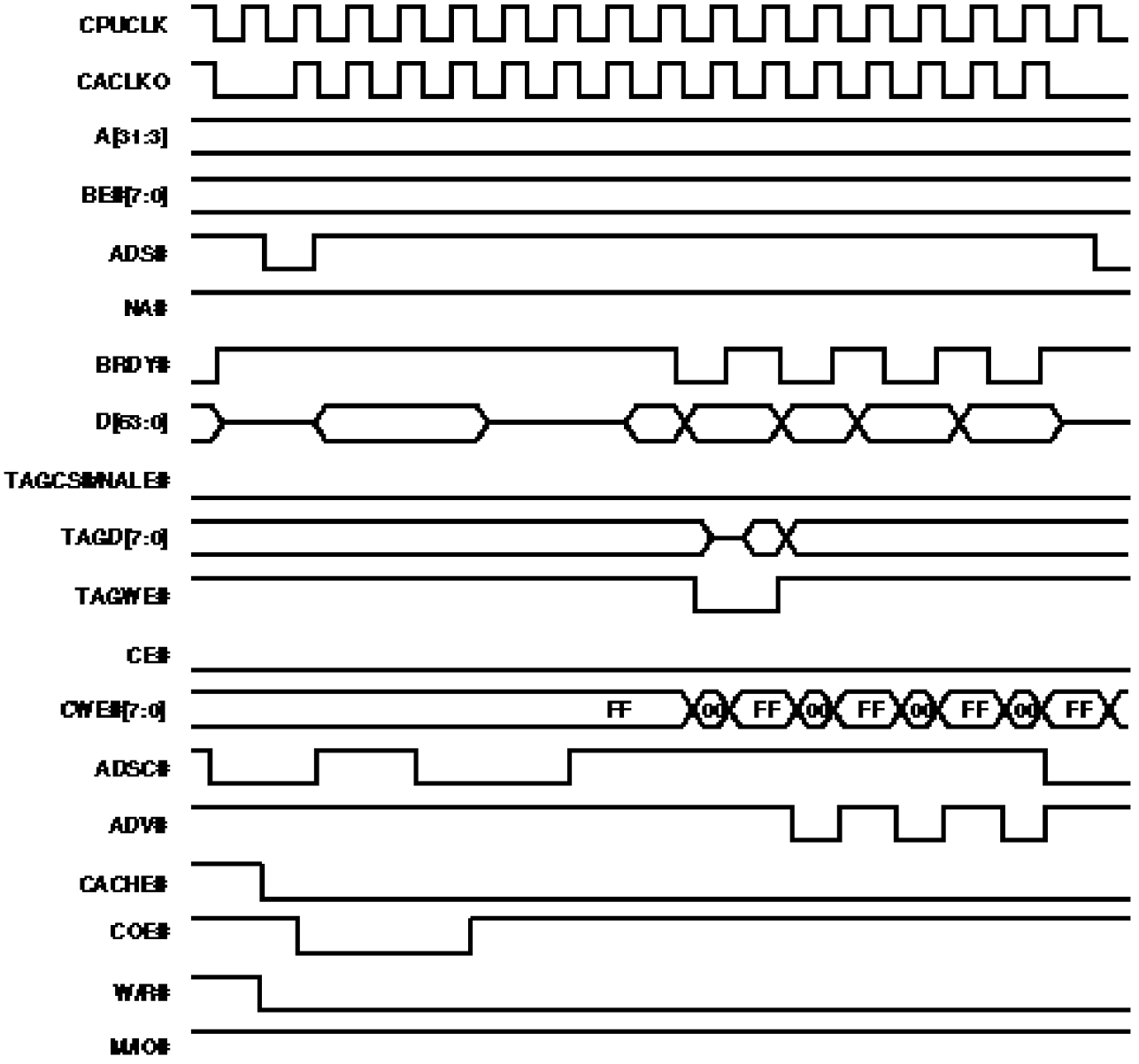


Figure 5-15. L2 Cache – Synchronous Burst Read Miss

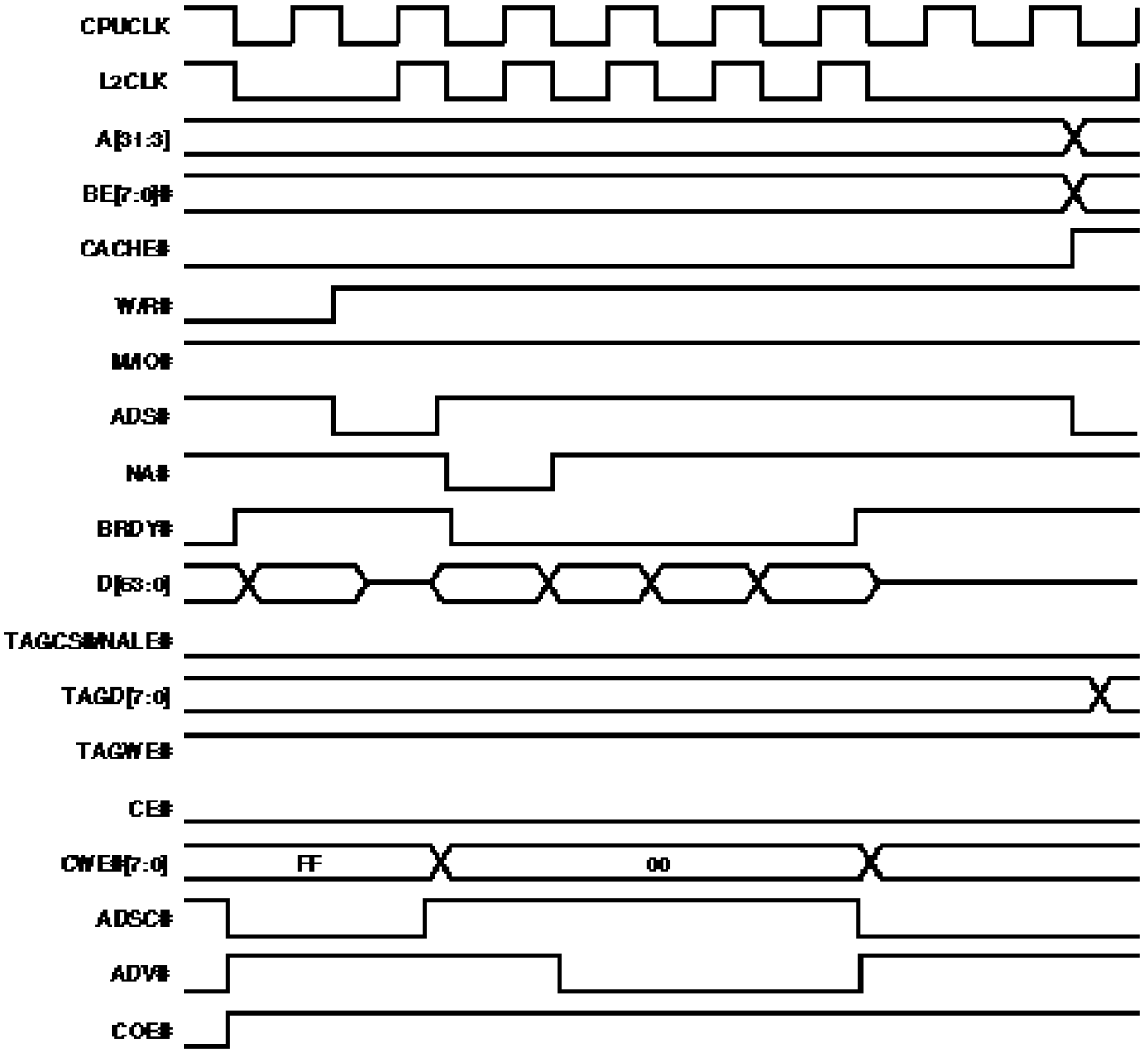


Figure 5-16. L2 Cache Write Burst Hit

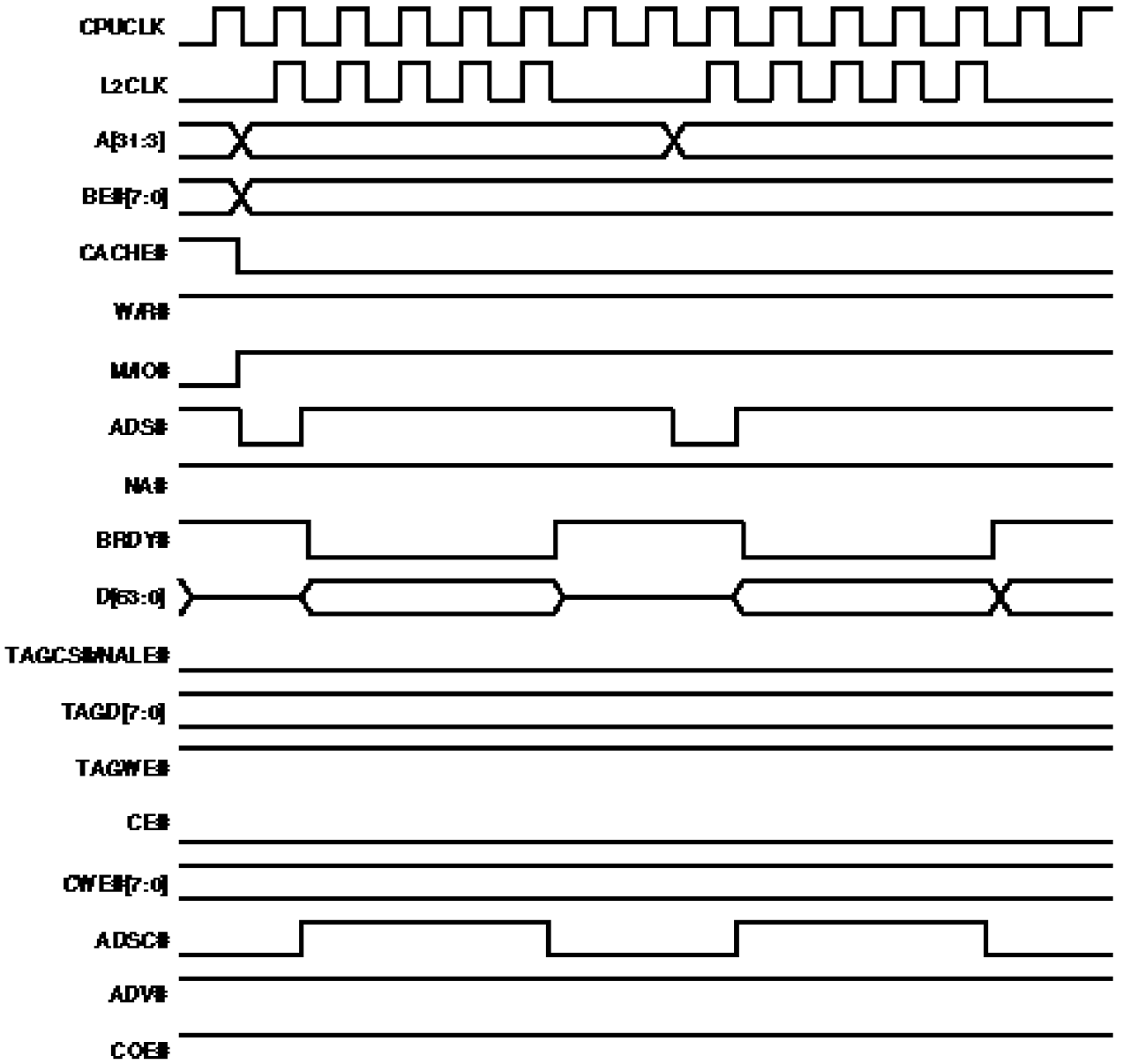


Figure 5-17. L2 Cache Write Burst Miss With Empty Write Buffer

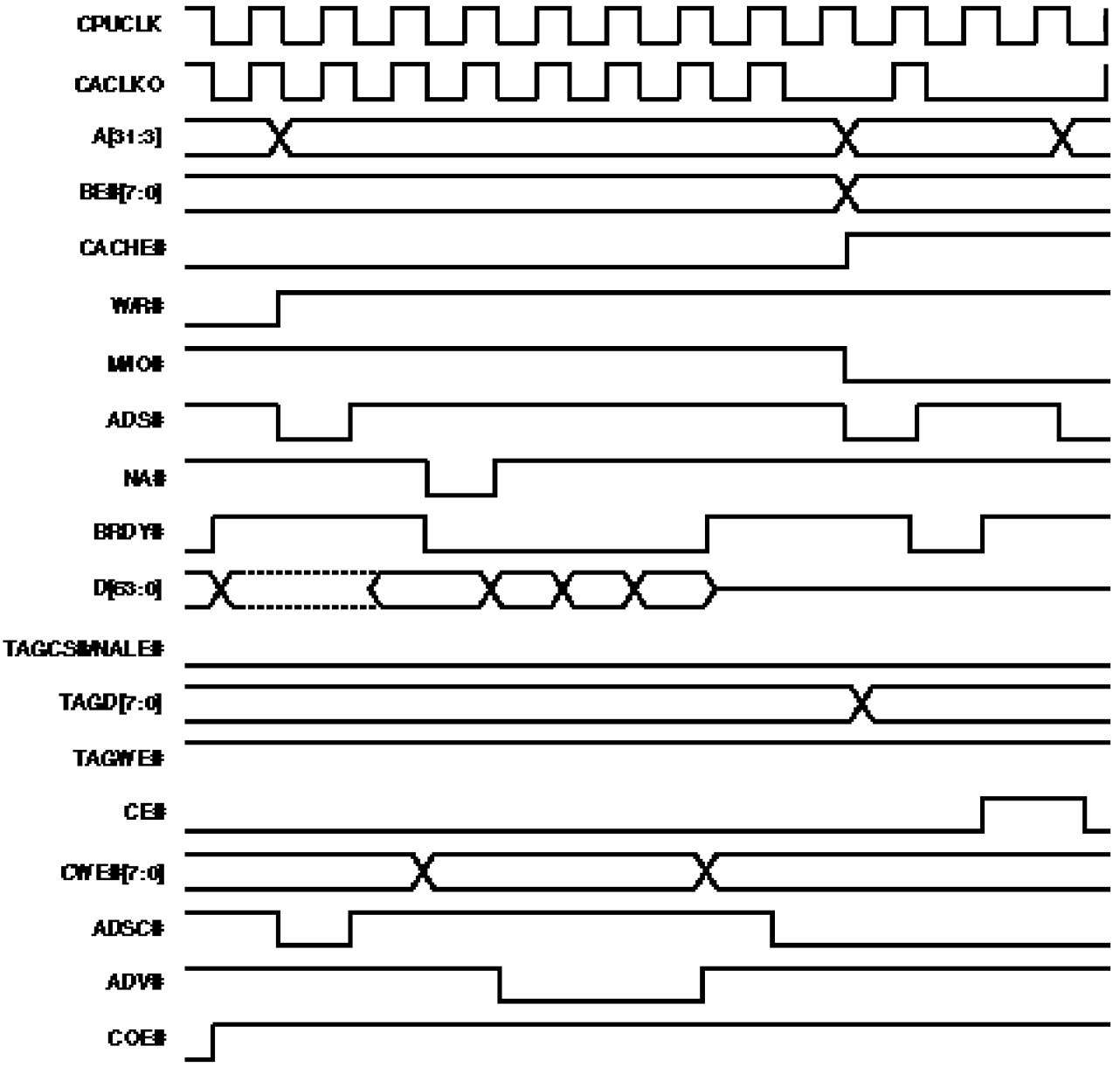


Figure 5-18. L2 Cache – Pipeline Synchronous, Write Burst Hit

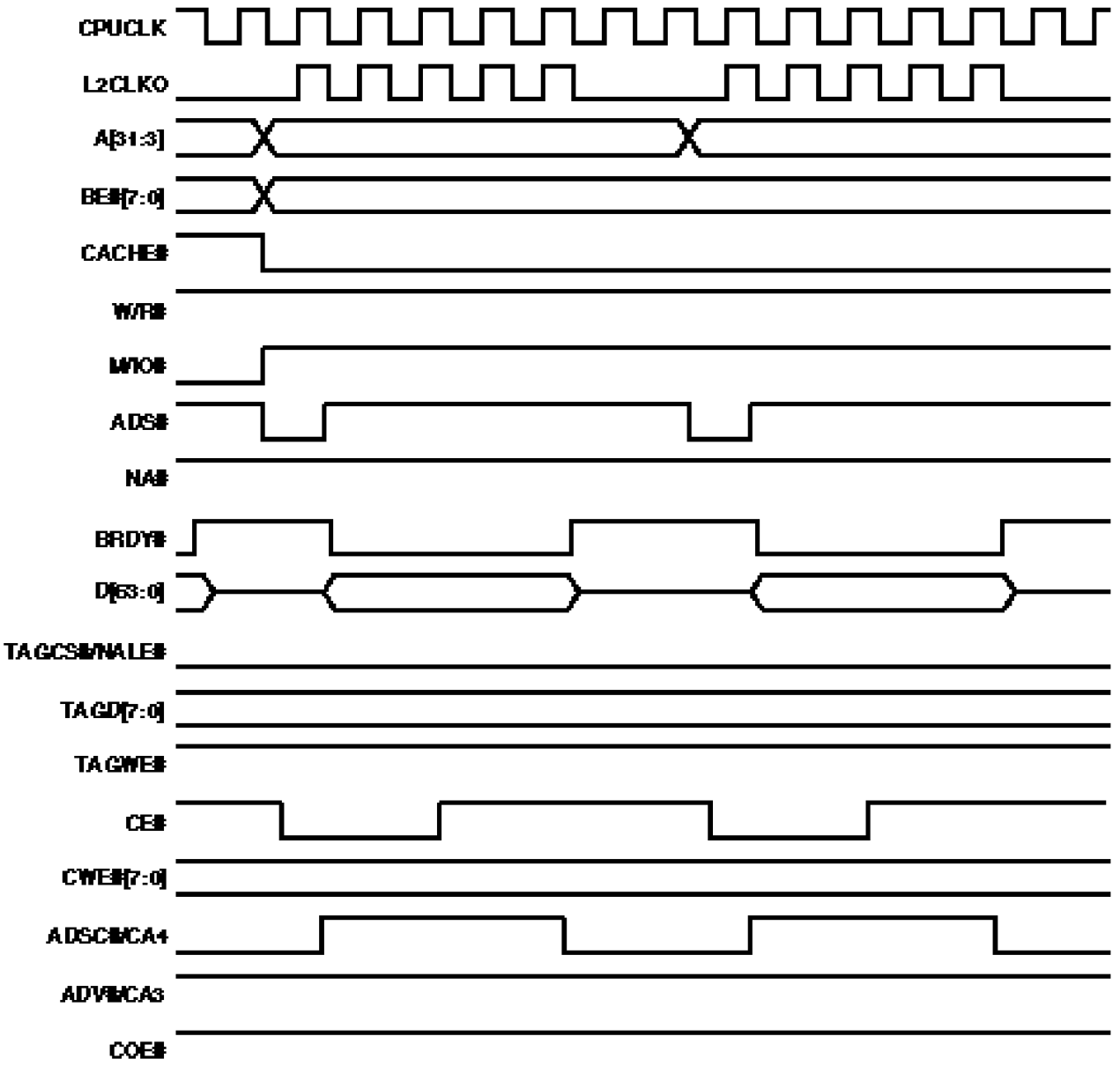


Figure 5-19. L2 Cache – Pipeline Synchronous, Burst Write Miss, Write Buffer Empty

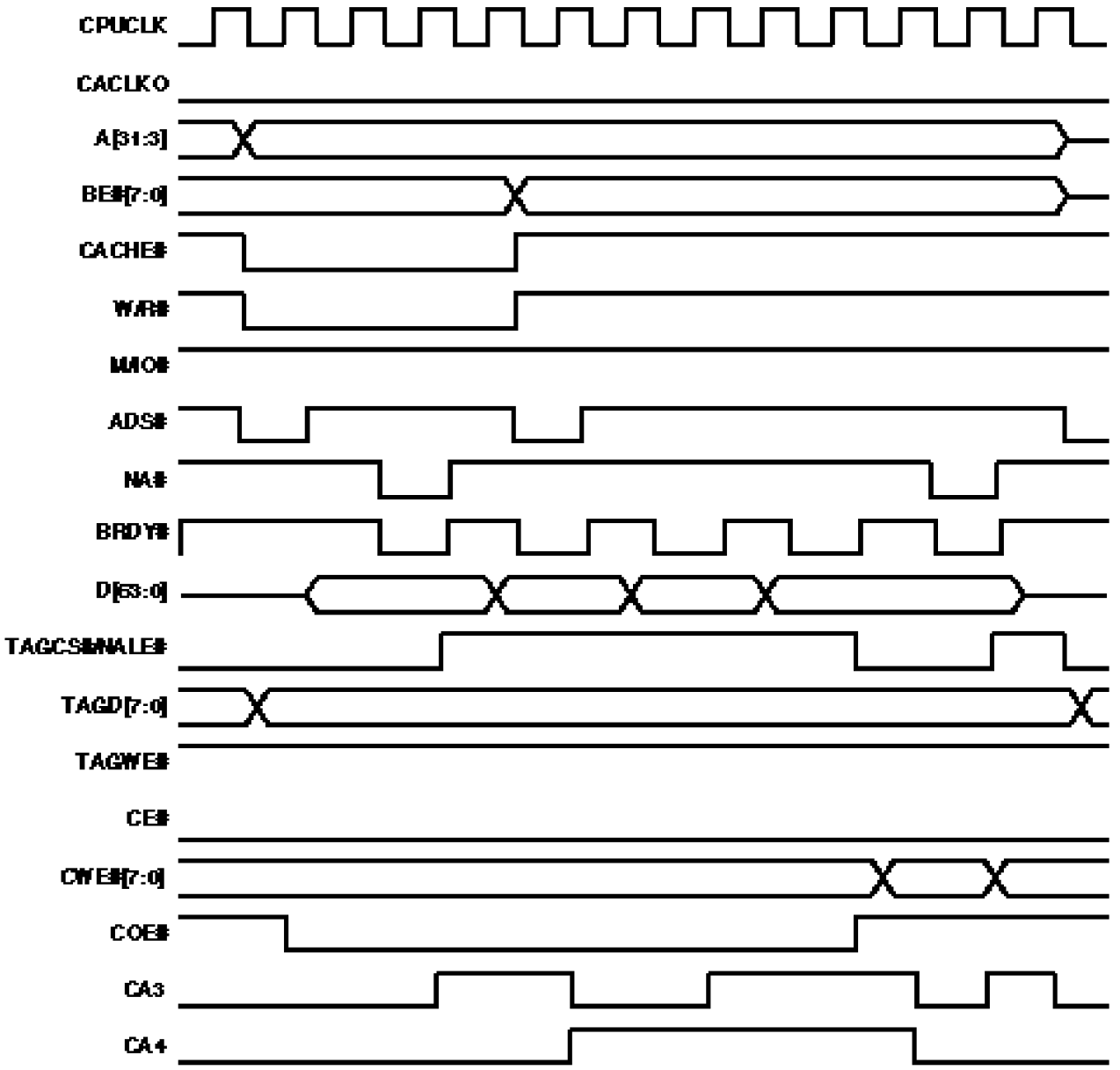


Figure 5-20. L2 Cache – Asynchronous, Burst Read 3-2-2-2 Hit

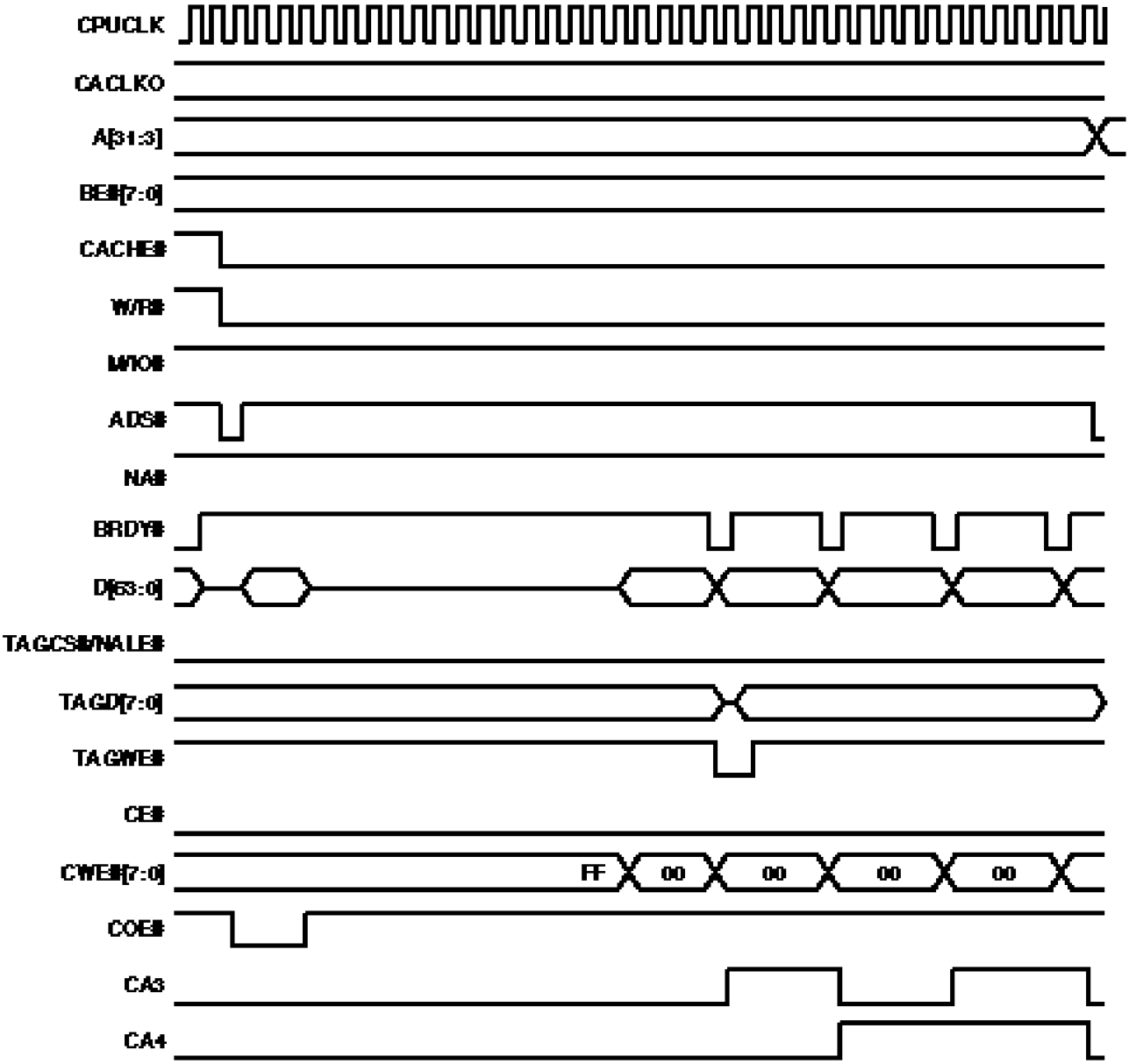


Figure 5-21. L2 Cache – Asynchronous, Burst Read Miss

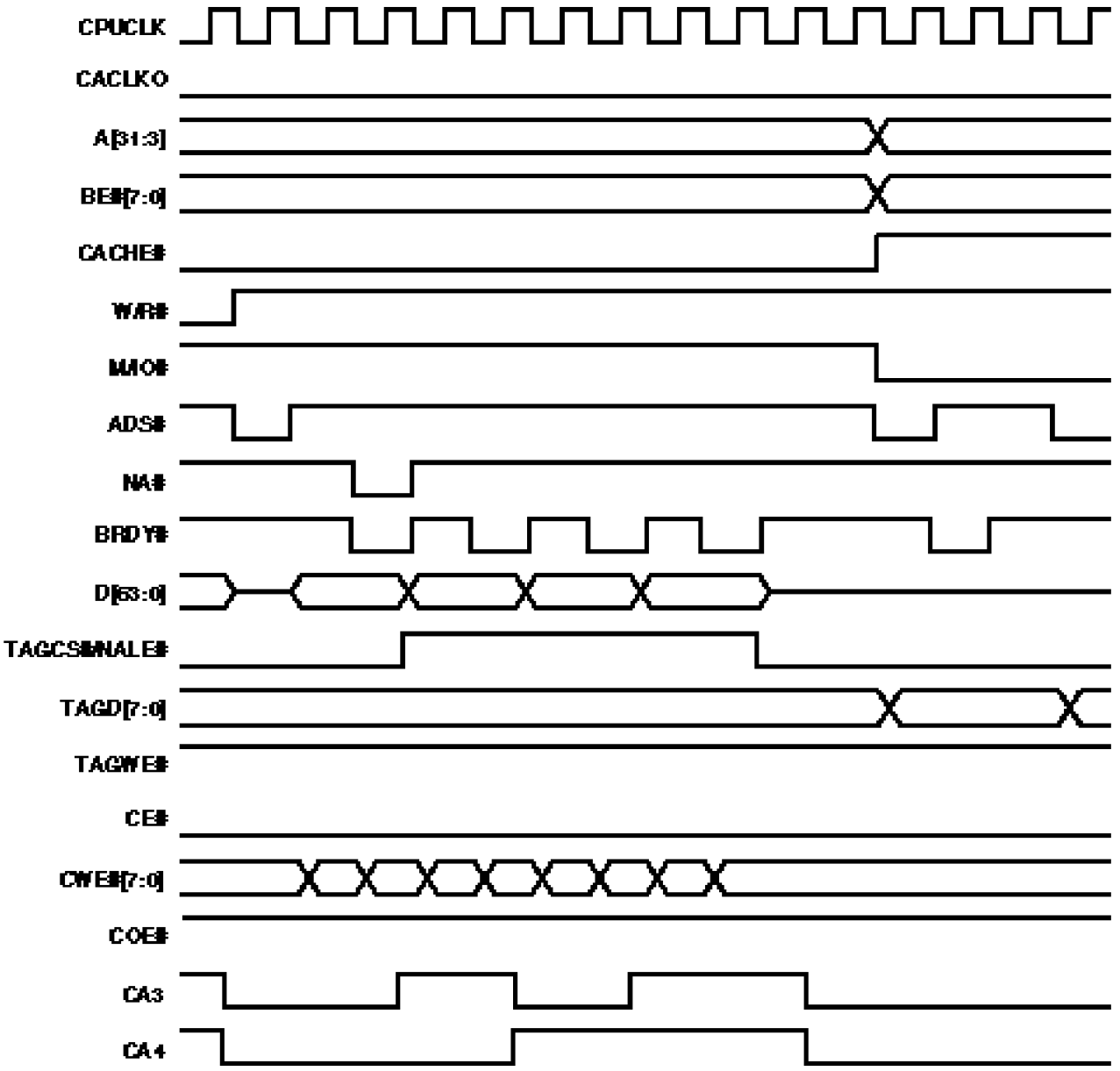


Figure 5-22. L2 Cache – Burst Write 3-2-2-2 Hit

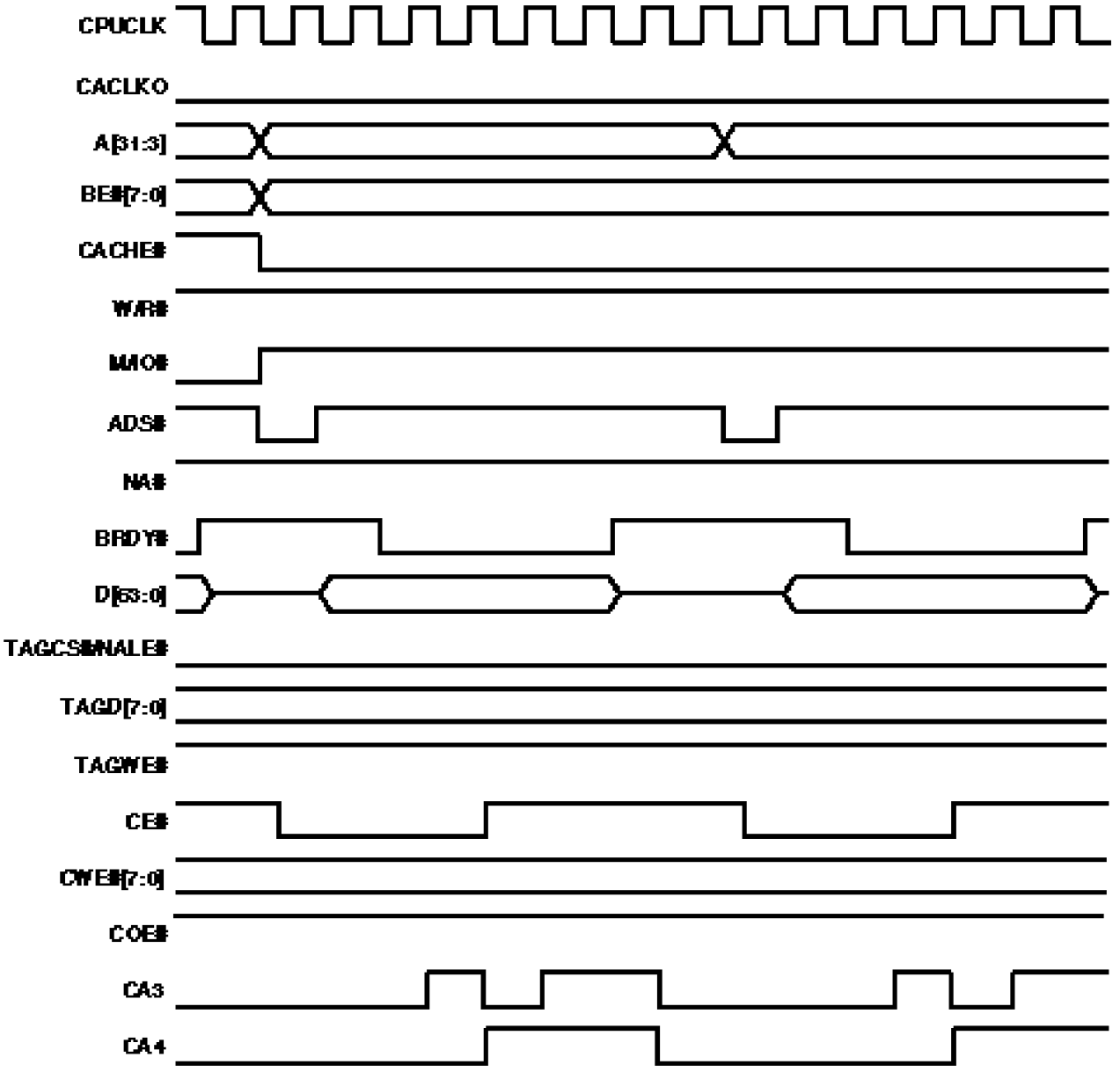


Figure 5-23. L2 Cache – Asynchronous, Burst Write Miss, Write Buffer Empty

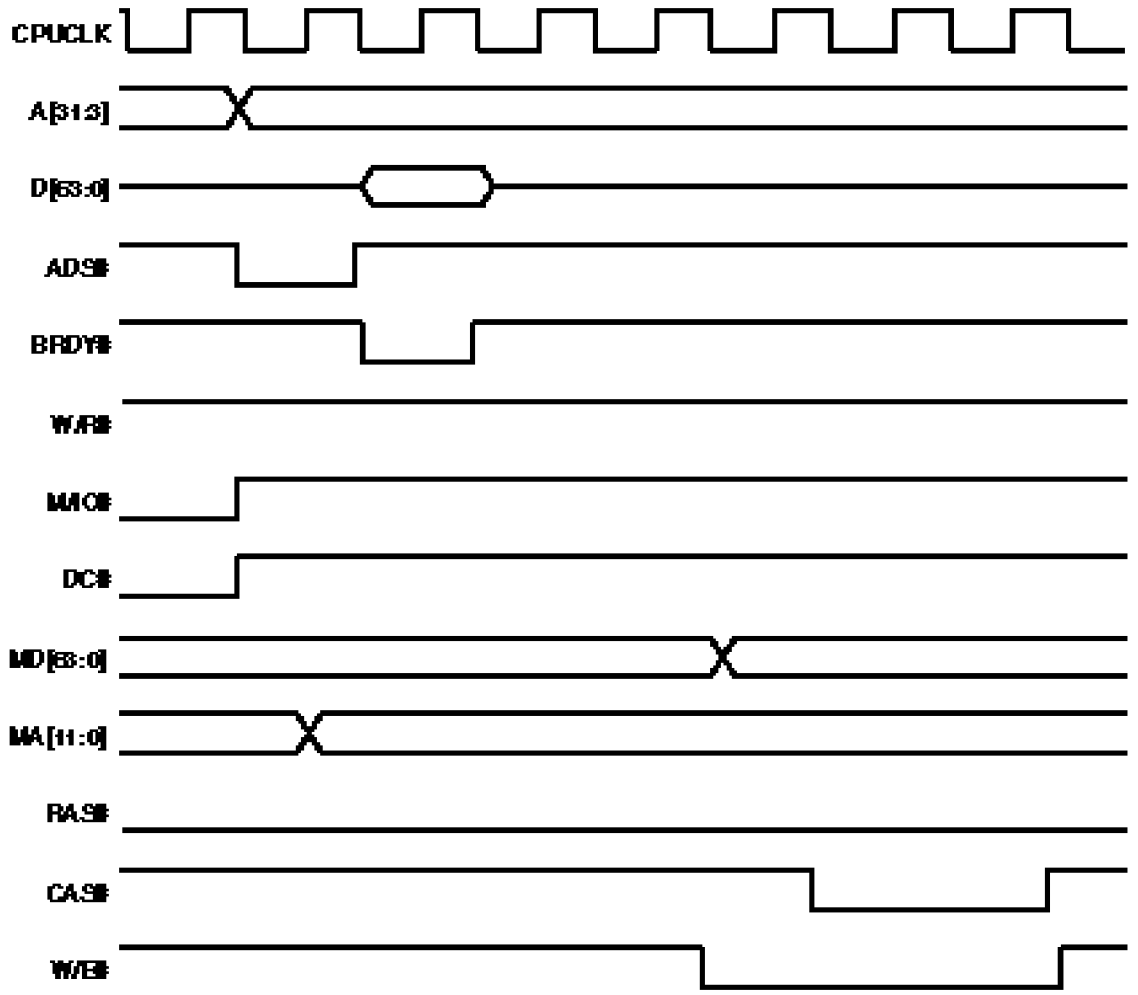


Figure 5-24. Fast Page Single Write – Page Hit

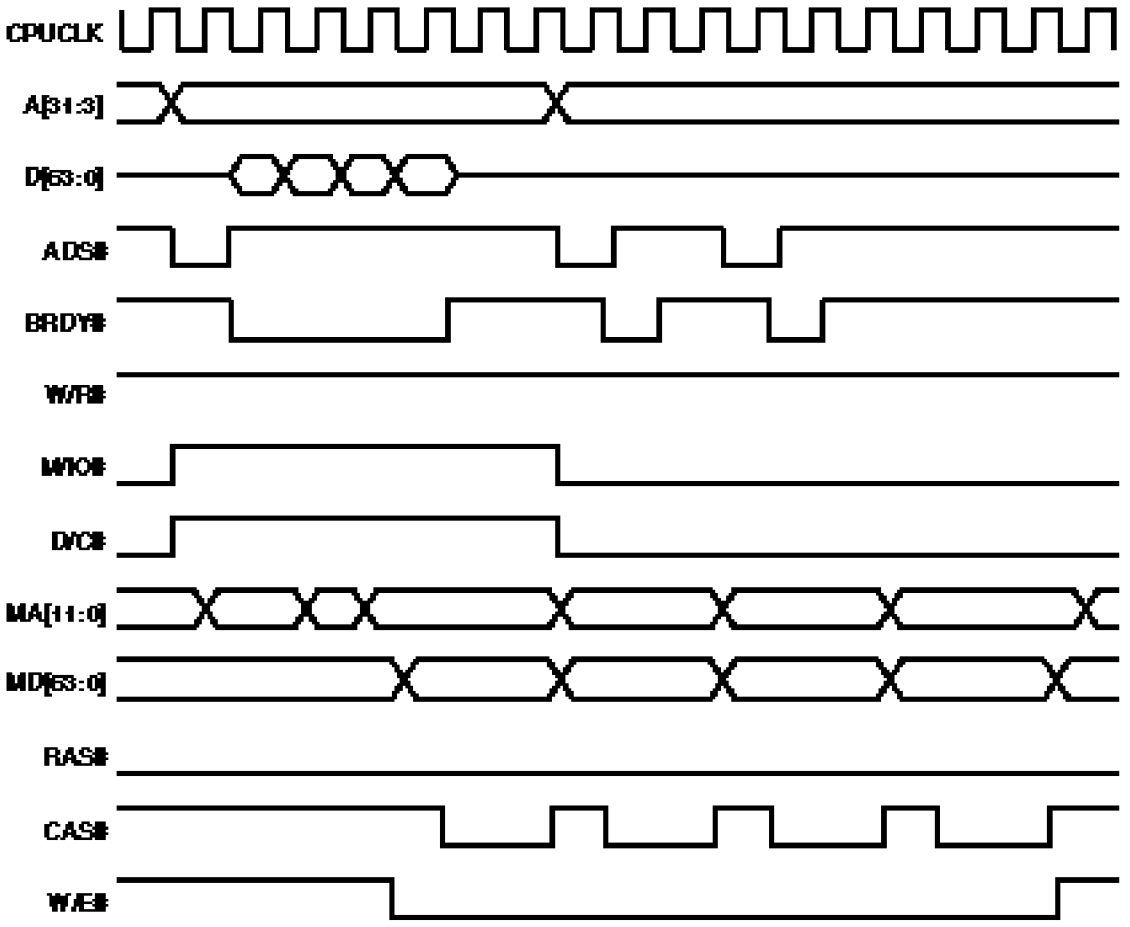


Figure 5-25. Fast Page Burst Write – Page Hit

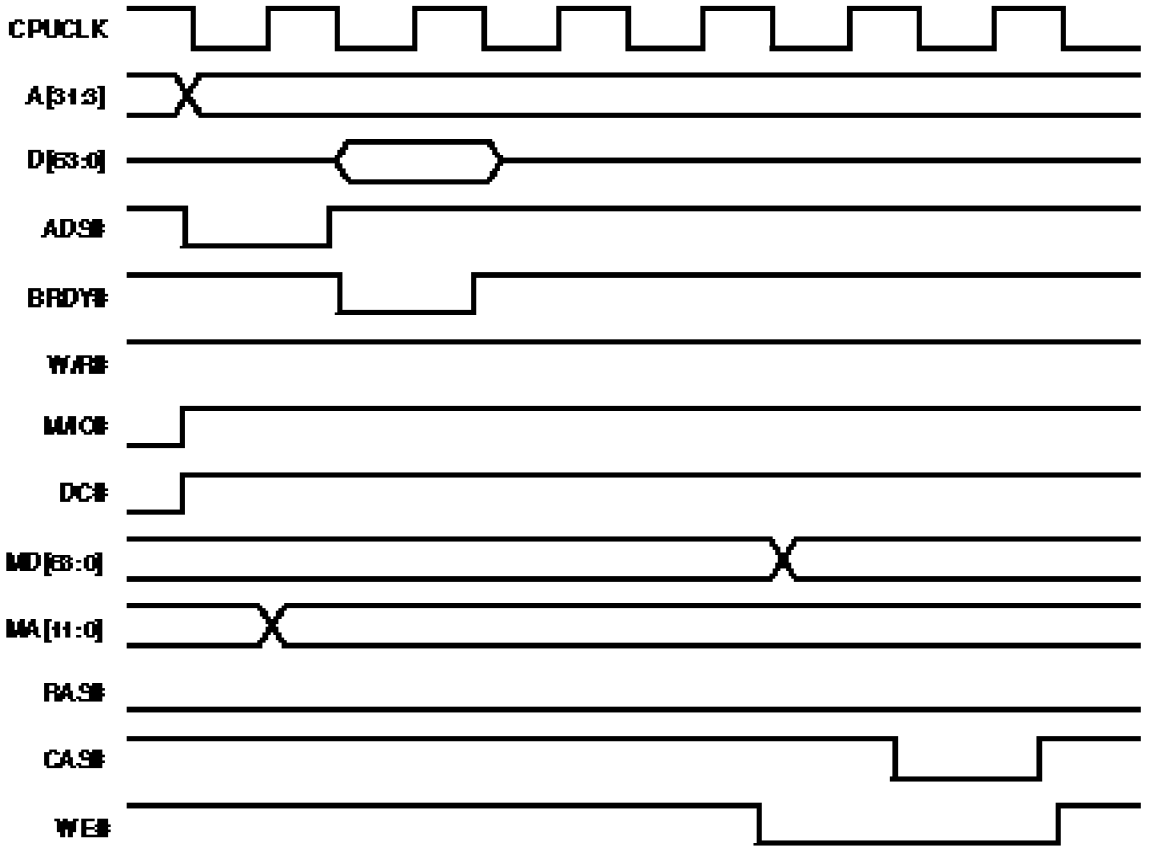


Figure 5-26. EDO Single Write – Page Hit

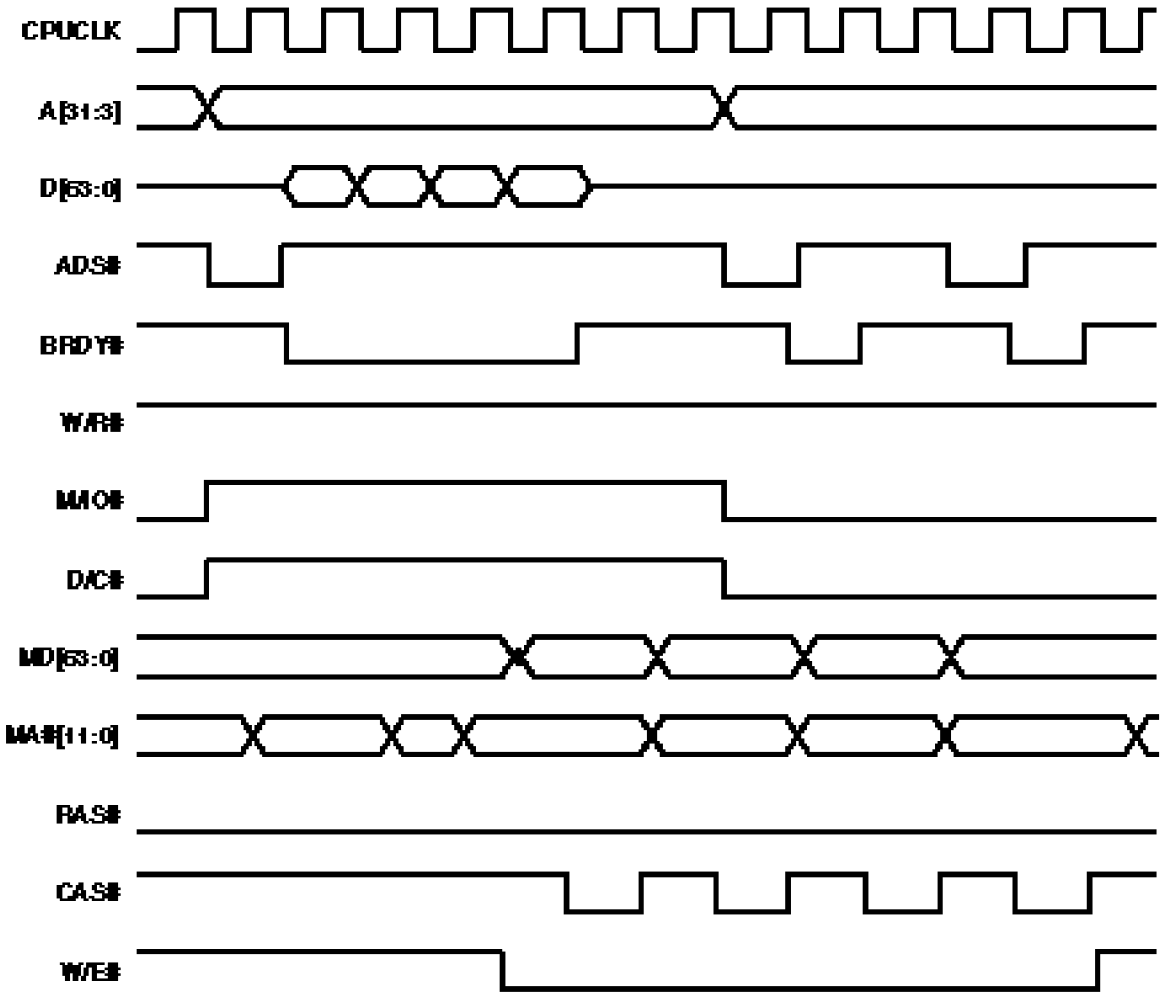


Figure 5-27. EDO Burst Write – Page Hit

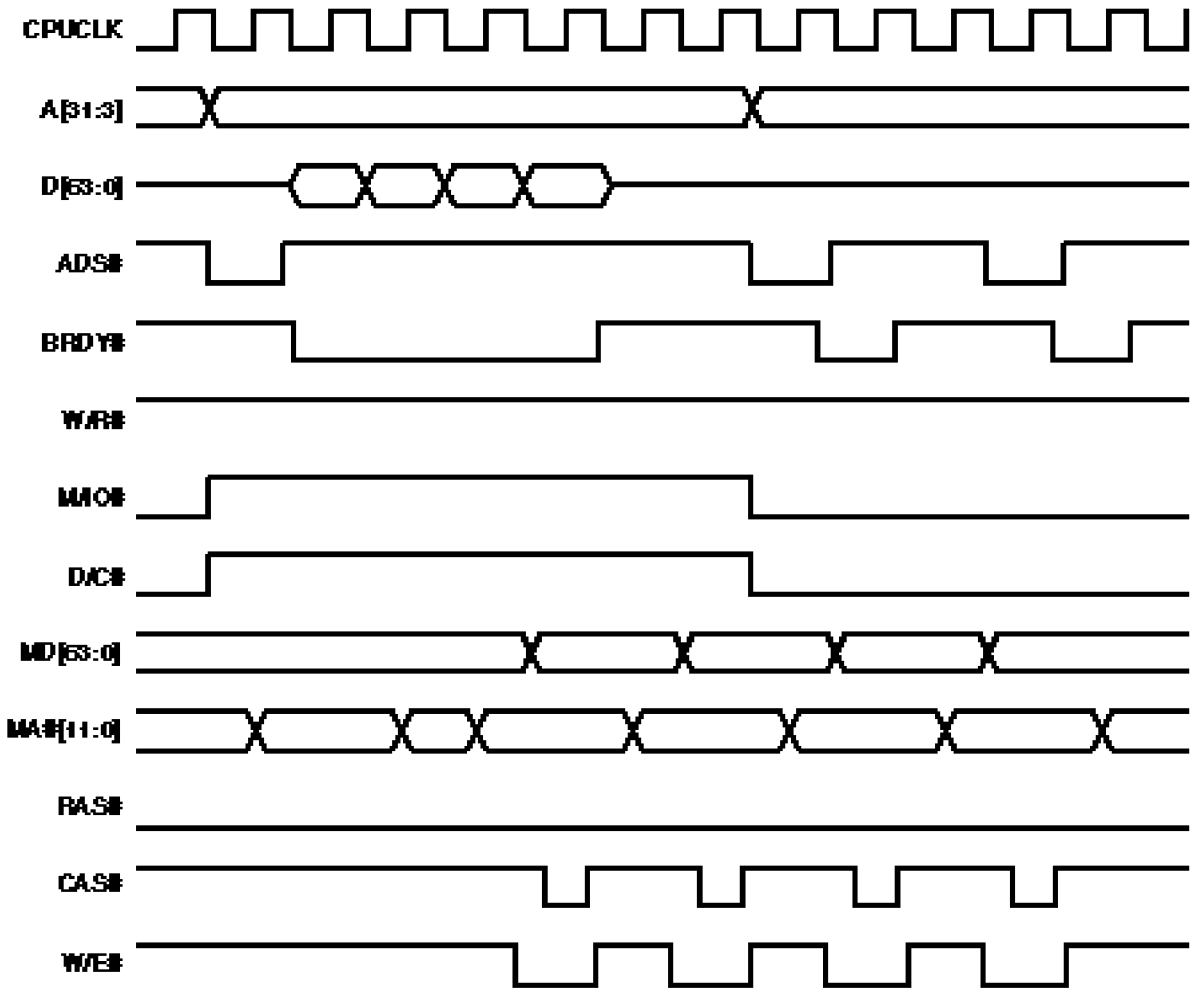


Figure 5-28. Burst EDO DRAM – Burst Write, Page Hit

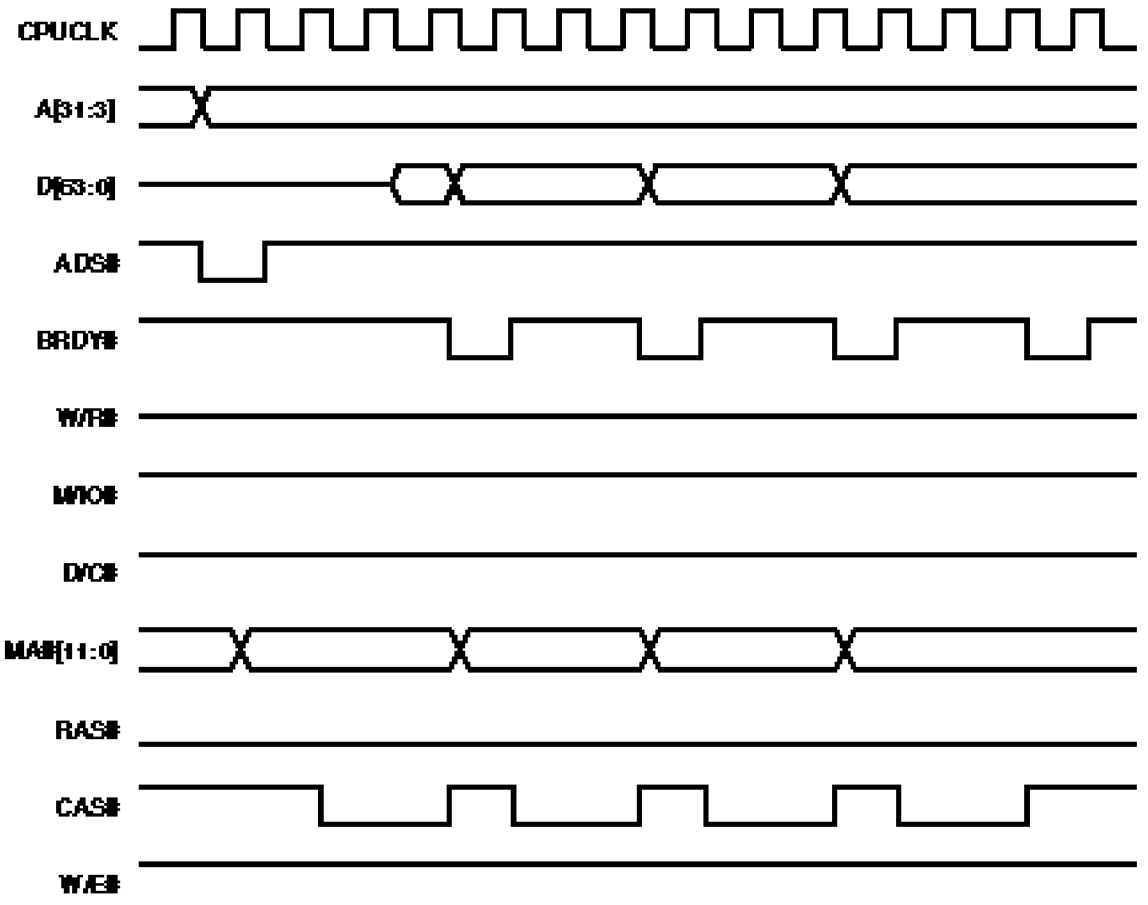


Figure 5-29. Fast Page Burst Read (5-3-3-3) – Page Hit (L2 cache disabled)

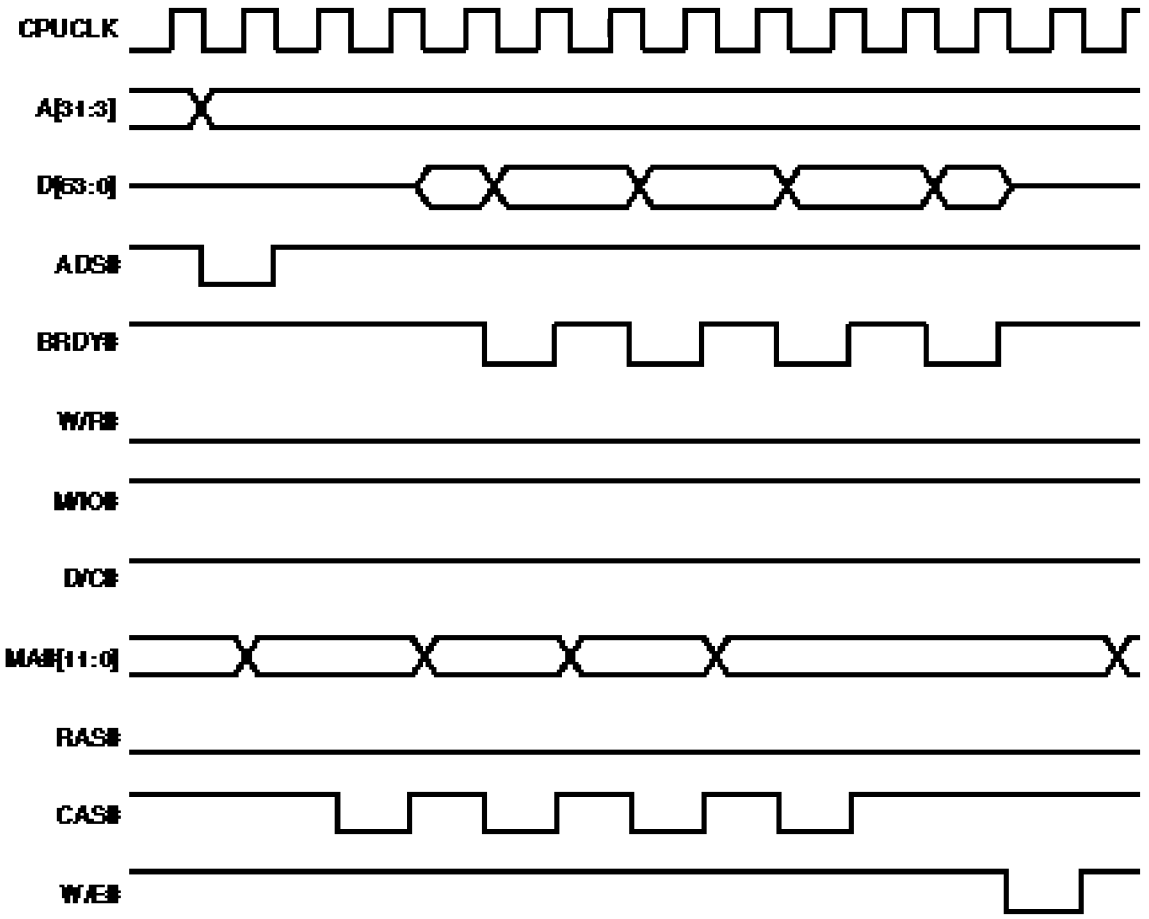


Figure 5-30. EDO Burst Read (5-2-2-2) – Page Hit (L2 cache disabled)

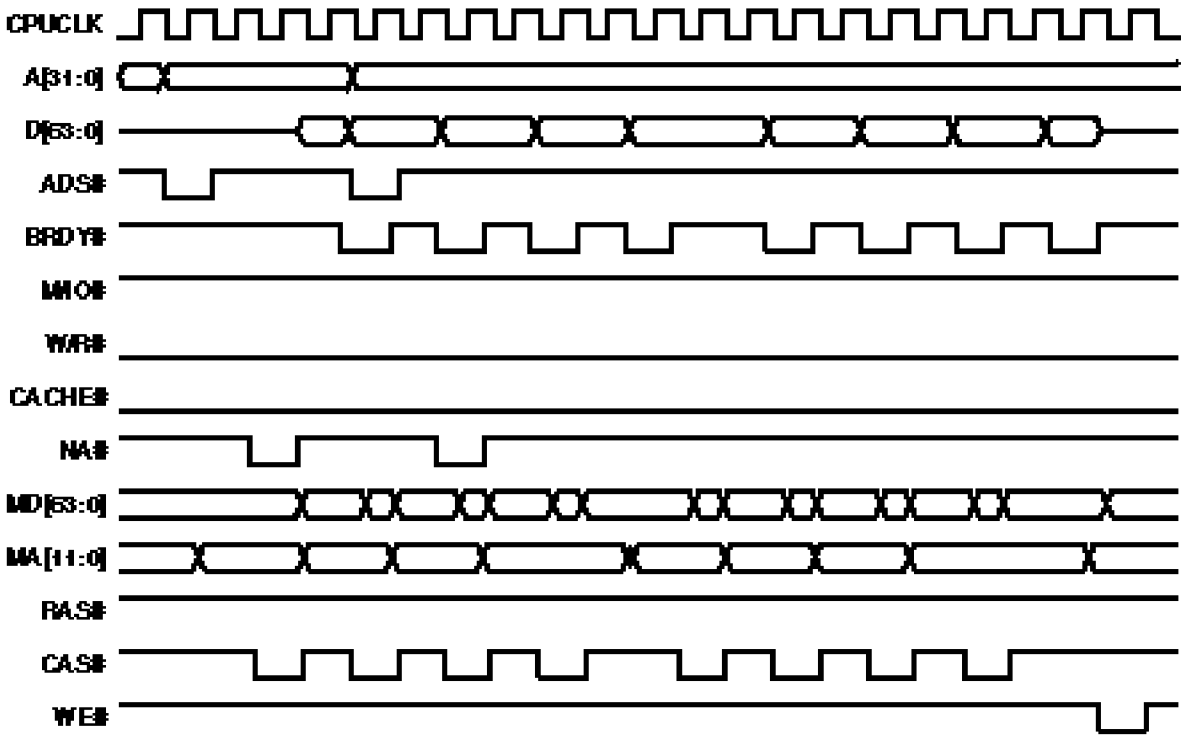


Figure 5-31. EDO Pipelined Burst Read (5-2-2-3-2-2-2)

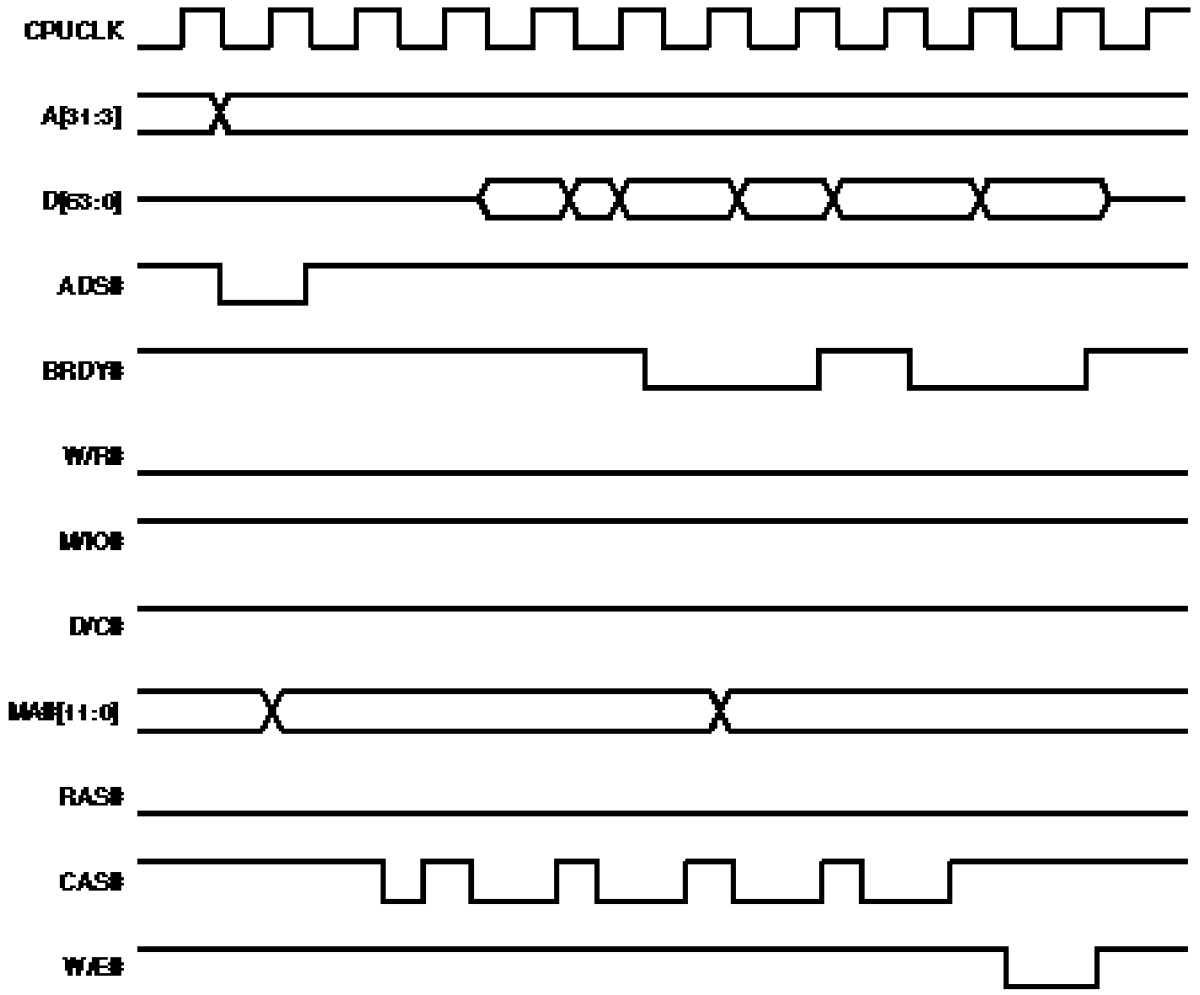


Figure 5-32. Burst EDO – Burst Read (6-1-2-1), Page Hit (L2 cache disabled)

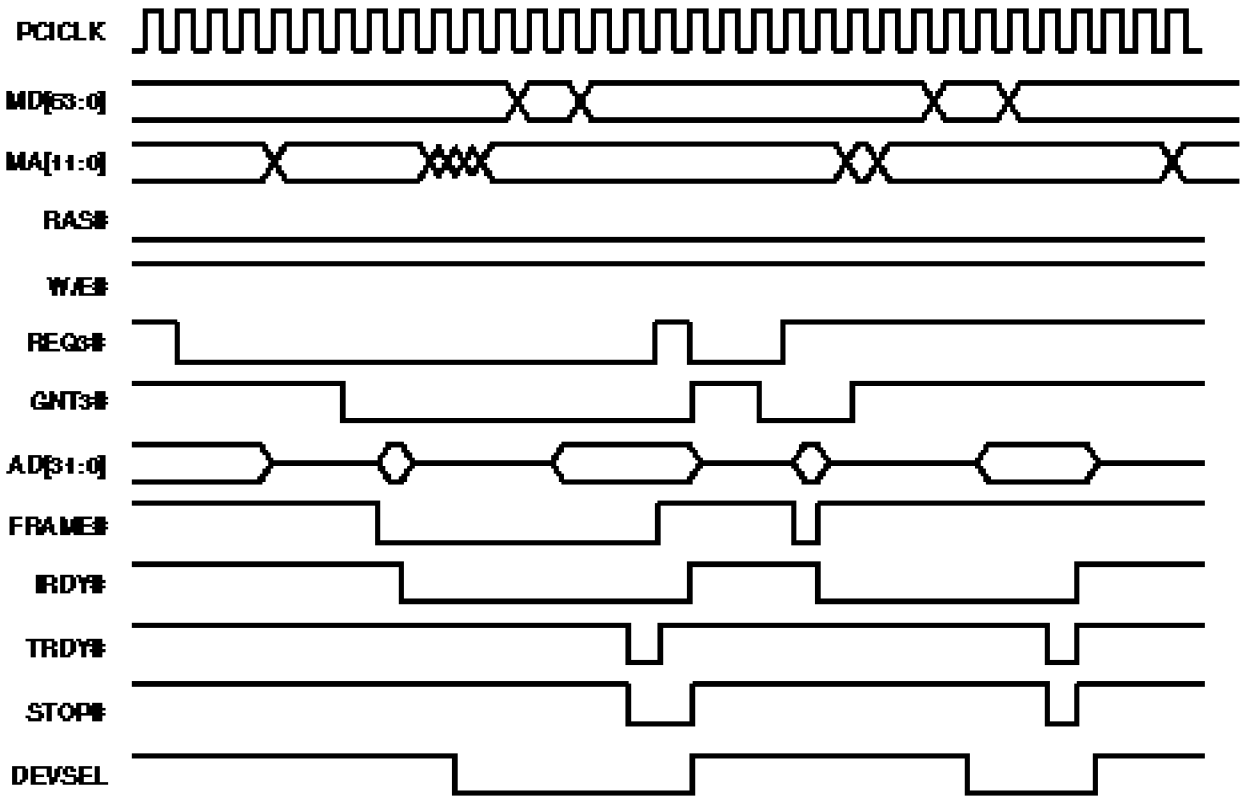


Figure 5-33. PCI Bus Master Read From 64-bit DRAM (no L1 cache hit)

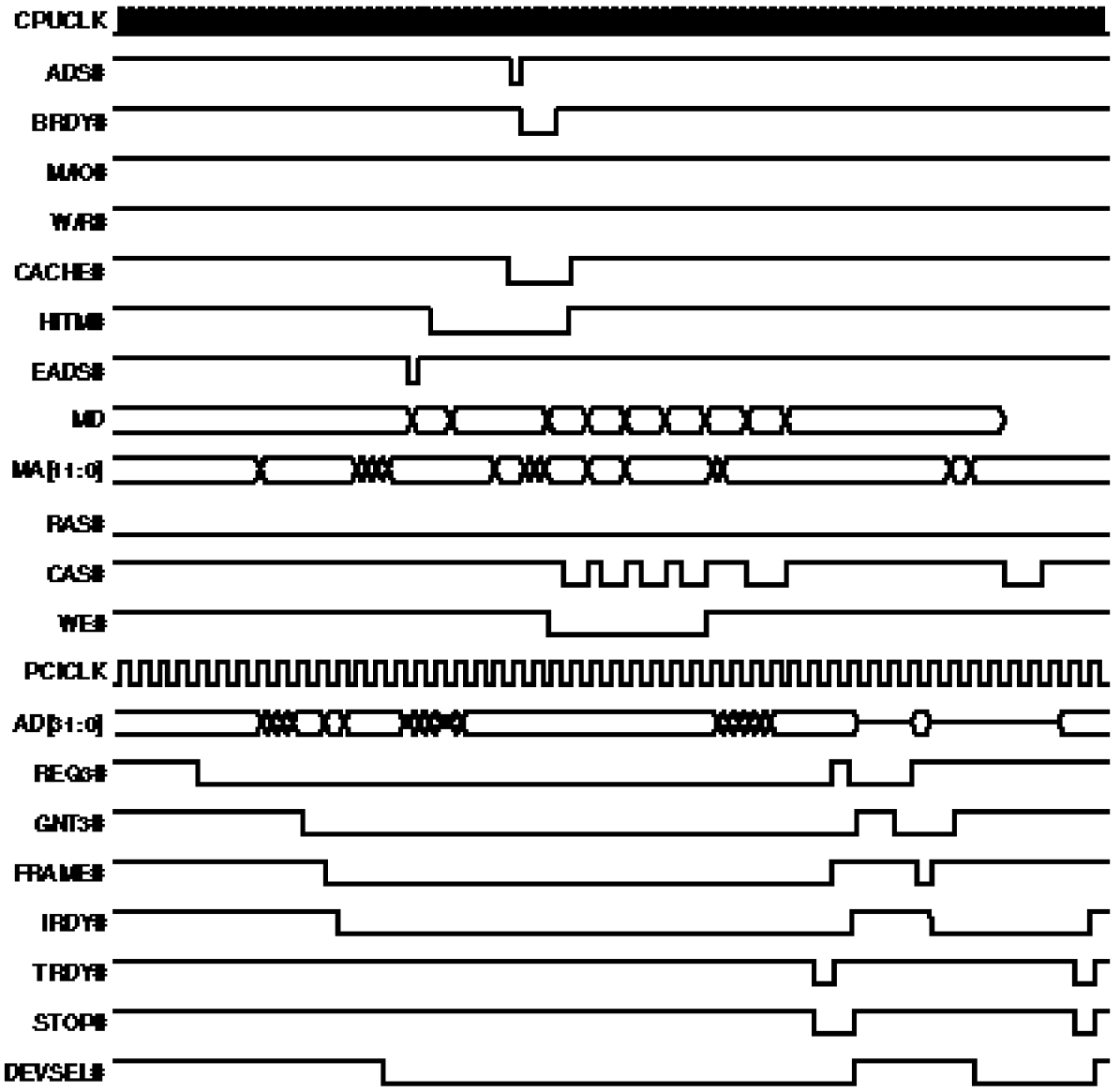


Figure 5-34. PCI Bus Master Read From 64-bit DRAM (L1 write-back)

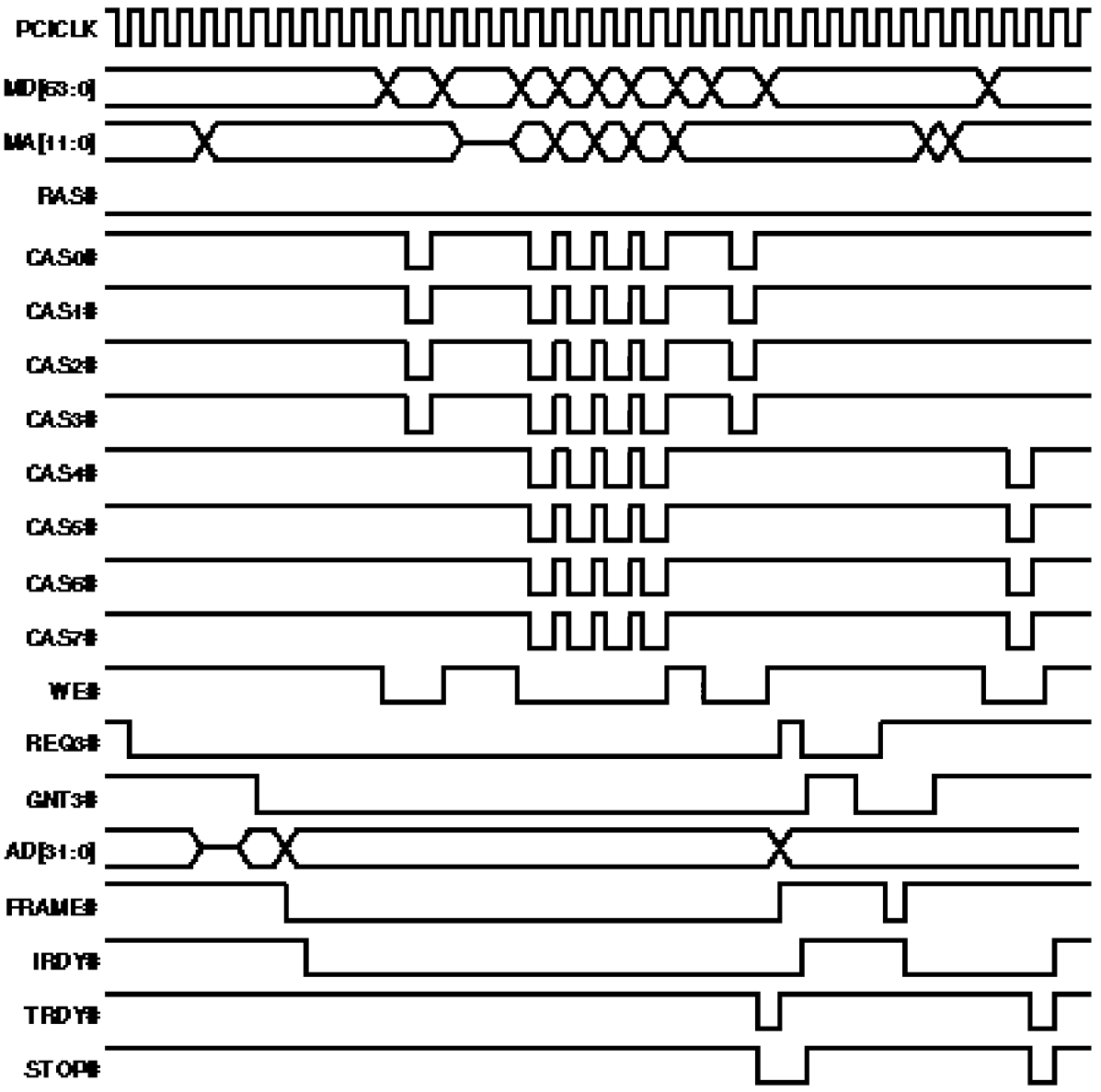


Figure 5-35. PCI Bus Master Write to 64-bit DRAM (L1 write-back)