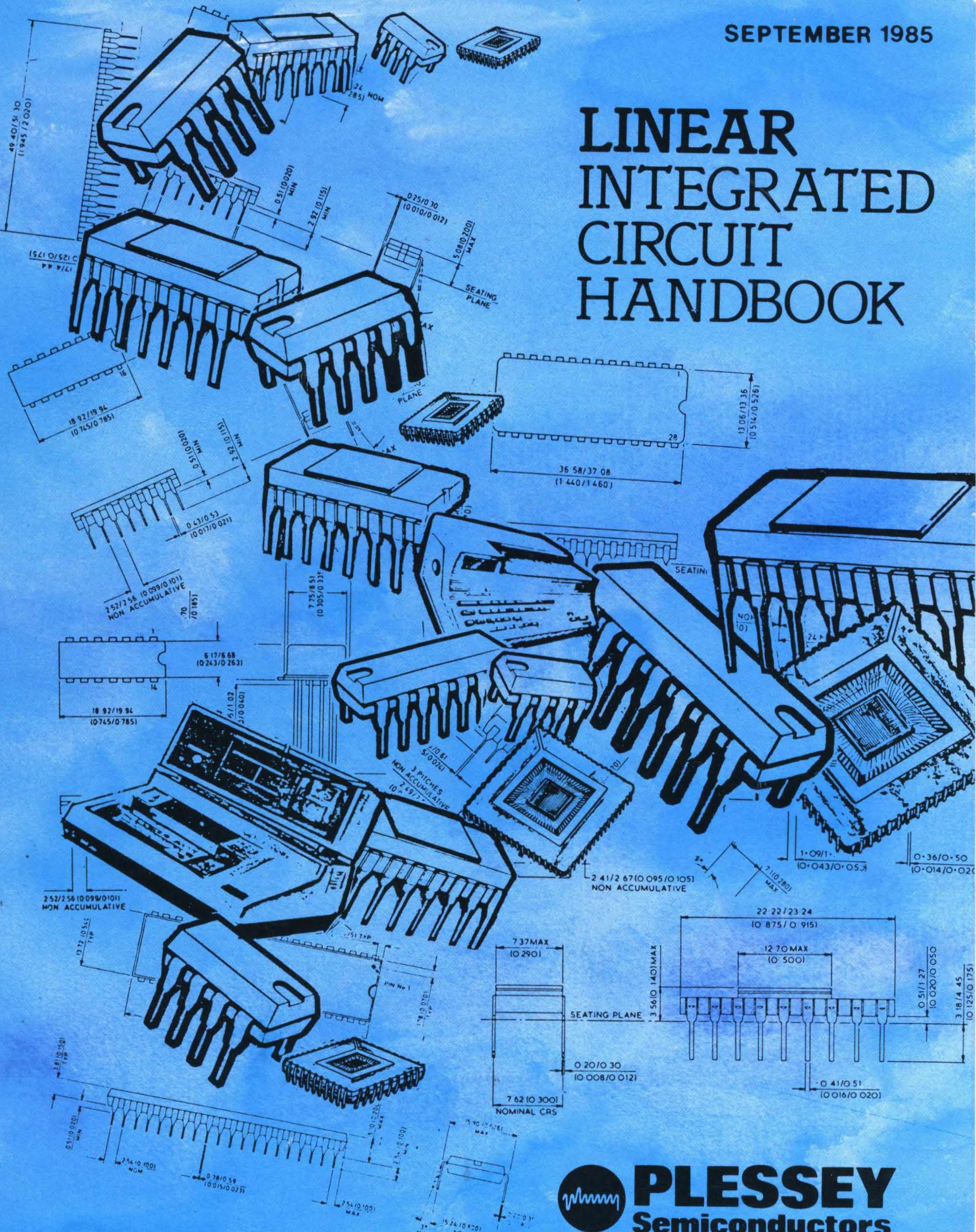
SEPTEMBER 1985

LINEAR INTEGRATED CIRCUIT HANDBOOK



PLESSEY
Semiconductors

LINEAR INTEGRATED CIRCUIT HANDBOOK

PLESSEY Semiconductors

Publication No. P.S. 1973 October 1985

Contents

Product index

Limiting wideband amplifiers

EXP products are new designs designated 'Experimental' but which are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to future availability. Please consult your local Plessey sales office for details of the current status.

Product list

The quality concept

In common with most semiconductor manufacturers, Plessey Semiconductors perform incoming piece parts check, in-line inspections and final electrical tests. However, quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes - followed by strict control and ongoing assessment to ensure that design requirements are still being met - that quality products will be produced.

In line with this philosophy, all designs conform to standard layout rules (evolved with performance and reliability in mind), all processes are thoroughly evaluated before introduction and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic system of evaluation, appraisals and checks is used on all products up to and including device packing for shipment. It is only at this stage that extra operations are performed for certain customers in terms of lot qualification or release procedure.

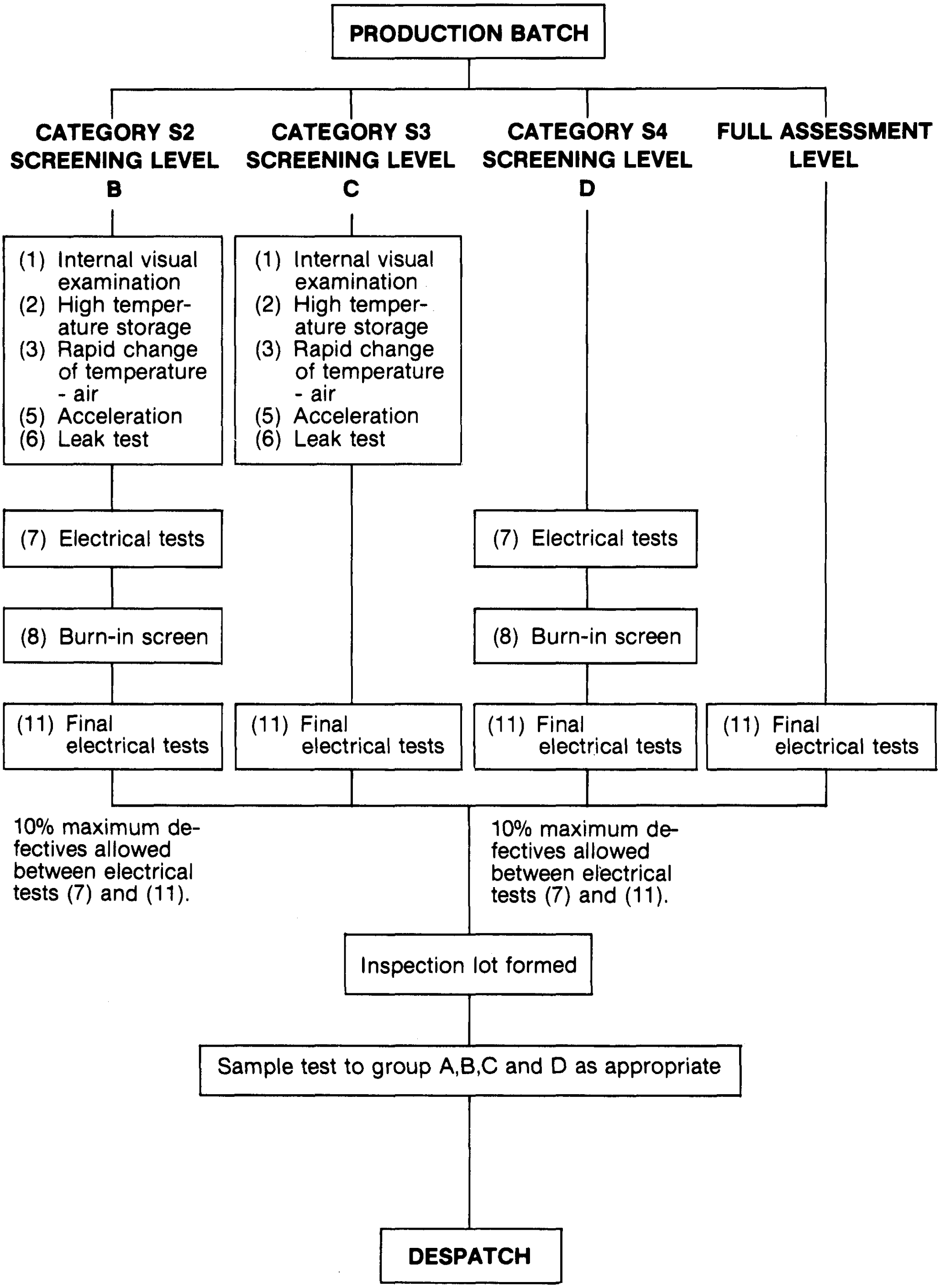
By working to common procedures for materials and processes for all types of customers advantages accrue to all users - the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved whilst the large scale user gains the benefits associated with basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals. **BS9300** and **BS9400** (BSI Approval No. 1053/M).

DEF-STAN 05-21 (Reg. No. 23H POD).

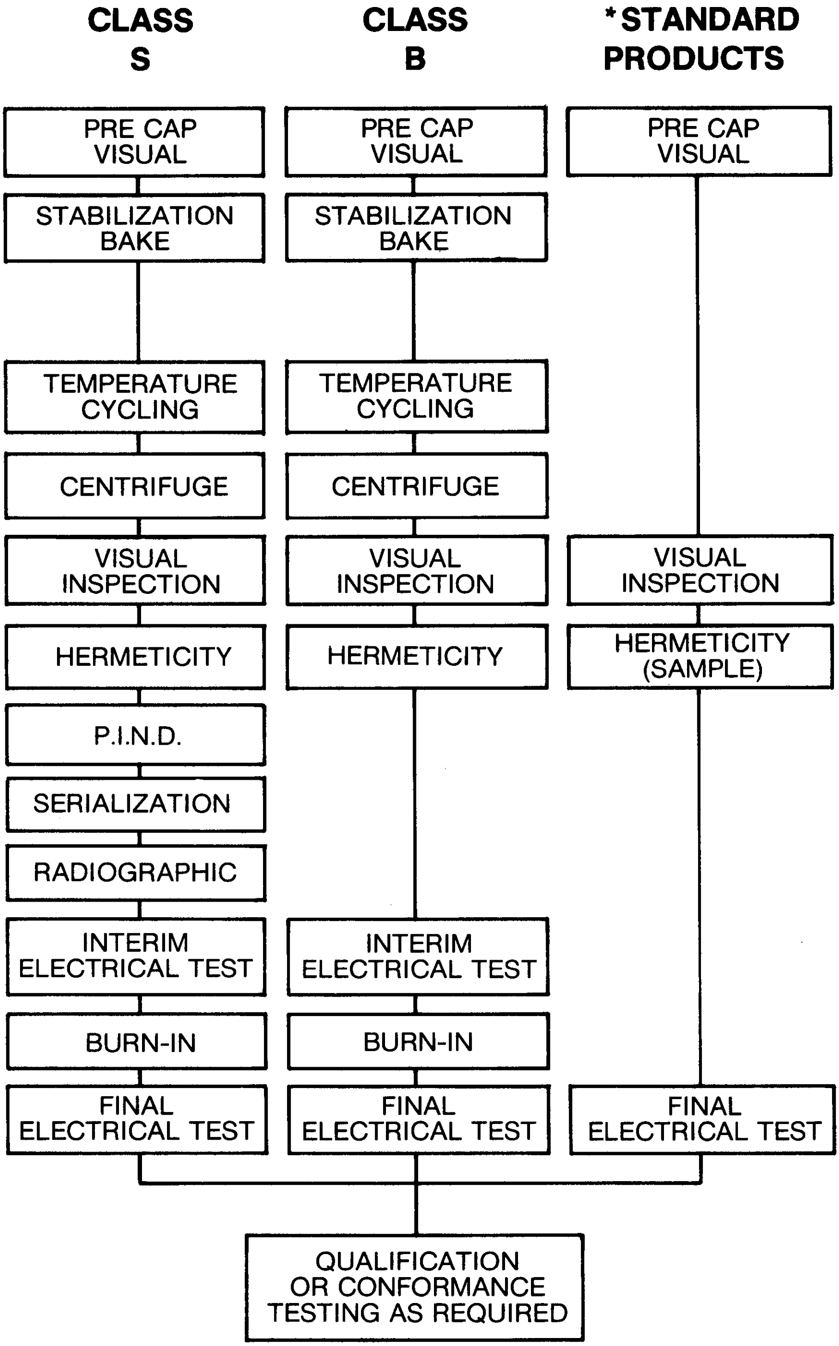
In addition a number of U.S., European and British customers manufacturing electronics for space have approved our facilities.

Screening to BS9400



Plessey Hi-Rel screening

The following Screening Procedures are available from Plessey Semiconductors.

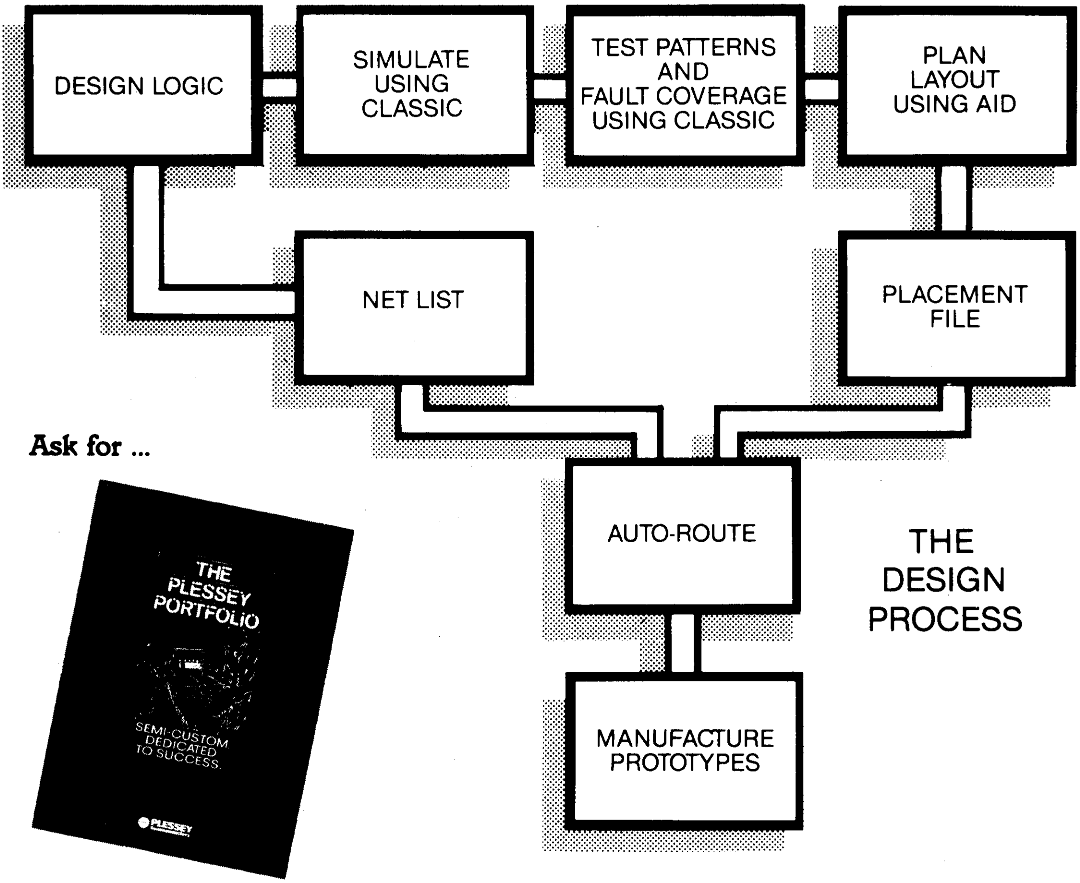


*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

Plessey Semiconductors' advanced work in the Semi-Custom field enables us to offer our customers the opportunity to develop their own high performance circuits using our CLASSIC software. Among the many advantages are:

• CLASSIC is cost effective and user friendly • Prototypes in as little as 3 weeks • Close coordination with customer throughout design and production process • State-of-the-art high performance produces • Up to 10044 gates available



THE DESIGN PROCESS

Ask for ...

Microgate-C (Si-Gate CMOS)

CLA 2000 SERIES

- Double layer metallisation
- 5 micron channel length
- Product family:
  CLA 21XX 840 Gates
  CLA 23XX 1400 Gates
  CLA 25XX 2400 Gates
- 7ns max. prop delay (2 input NAND fanout of 2 with 2mm track 0-70°C 4.5-5.5V)
- 14MHz system clock rate
- 30MHz toggle rate
- Fully auto-routed

CLA 3000 SERIES

- Double layer metallisation
- 4 micron channel length
- Product family:
  CLA 31XX 840 Gates
  CLA 33XX 1440 Gates
  CLA35XX 2400 Gates
  CLA 37XX 4200 Gates
  CLA 39XX 6000 Gates
- 5ns max. prop delay
- 20MHz system clock rate
- 50MHz toggle rate
- Fully auto-routed

CLA 5000 SERIES

- Double layer metallisation
- 2 micron channel length
- Product family:
  CLA 51XX 640 Gates
  CLA 52XX 1232 Gates
  CLA 53XX 2016 Gates
  CLA 54XX 3060 Gates
  CLA 55XX 4408 Gates
  CLA 56XX 5984 Gates
  CLA 58XX 8064 Gates
  CLA 59XX 10044 Gates
- 2.5ns max. prop delay
- 40MHz system clock rate
- 100MHz toggle rate
- Fully auto-routed

Plessey Megacell™

Now there's a VLSI design system available that's perfect for solving your Application Specific Integrated Circuit (ASIC) problems. It's **PLESSEY MEGACELL** - a complete set of advanced computer-aided engineering and design tools coupled with an advanced CMOS process for implementing VLSI integrated circuits in the system design environment.

PLESSEY MEGACELL redefines semicustom integrated circuit design. It allows system engineers to design complex circuits with a high level of confidence of first time success in silicon - thanks to one of the best simulation facilities available in the world. This greatly reduces time to market, eliminating the many prototyping iterations that are all too common now in VLSI design.

PLESSEY MEGACELL is just about as close as you can get to achieving hand-crafted results short of full custom itself. System engineers can directly create their designs using the advanced layout and routing tools provided - without the aid of integrated circuit designers. So none of the system designers' application expertise is ever lost in transition, while chips of the smallest size and lowest production cost are regularly achieved.

Supporting the **PLESSEY MEGACELL** design capability is one of the most advanced CMOS processes available. It uses a 2-micron geometry capable of providing performance comparable with advanced Schottky TTL, with clock speeds to 40MHz and toggle rates of 100MHz achievable. And Plessey has established a 200,000 square foot dedicated processing facility to guarantee the manufacturing capacity required by even the most aggressive volume considerations.

PLESSEY MEGACELL is truly the gateway to the future - custom VLSI performance, with confidence of first time success and fast time to market. And it's going to stay that way - with Plessey's commitment to add future capabilities for high-speed ECL processes, 1 micron and submicron CMOS processes, and advanced analog capabilities.

Thermal design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$$

where θ_{ja} is thermal resistance junction-to-ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$$T_j = T_{amb} + P_D (\theta_{ja})$$

T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

A device is to be used at an ambient temperature of +50° C. θ_{ja} for the DG14 package with a chip of approximately 1mm sq is 107° C/W. Assuming the datasheet for the device gives P_D = 330mW and T_j max = 175° C.

$$T_j = T_{amb} + P_D \theta_{ja}$$
$$= 50 + (0.33 \times 107)$$
$$= 85.31° C \text{ (typ.)}$$

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Thermal design (cont'd)

Example 2

A device with T_{amb} max. = +175° C is to be used at an ambient temperature of +150° C. Again, θ_{ja} = 107° C/W, P_D = 330mW and T_j max. = +175° C.

$$T_j = 150 + (0.33 \times 107)$$
$$= +185.3°C \text{ (typ.)}$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the device operated as in Example 2 would result in a junction temperature given by:

$$T_j = 150 + (0.33 \times 55)$$
$$= 168°C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Technical data

PLESSEY
Semiconductors

SL301L

400MHz DUAL NPN TRANSISTOR

The SL301L contains dual monolithic NPN transistors with close parameter matching and high f_T.

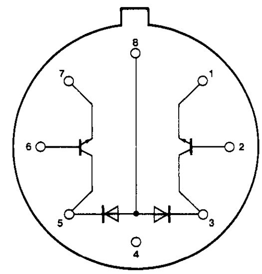


Fig.1 Pin connections

FEATURES

- Close V_{BE} Matching<3mV
- Close h_{fe} Matching>0.9
- Good Frequency Response>400MHz
- Good Thermal Tracking
- Wide Operating Current Range

APPLICATIONS

- Differential Amplifier to Very High Frequencies
- Comparators
- Current Sources
- Instrumentation

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Storage temperature -55°C to +175°C
Maximum junction temperature +175°C
Thermal resistance
Chip-to-case 265° C/W (see Note)
Chip-to-ambient 425° C/W

V_{CB} = 20V V_{EB} = 4.0V V_{CER} = 20V (see Fig.7)
V_{CE} = 12V V_{CI} = 25V I_C = 20mA

NOTE:
These figures are worst case, assuming all the power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50°C/watt.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Collector base breakdown	BV_{CBO}	20			V	I_C = 10μA
Collector emitter breakdown	BV_{CEO}	12			V	I_C = 10μA
Collector emitter breakdown	LV_{CEO}	12			V	I_C = 5mA
Emitter base leakage current	I_{EBO}			1	μA	V_{EB} = 4V
Emitter base leakage current	I_{EBO}			10	nA	V_{EB} = 2V
Collector isolation breakdown	BV_{CIO}	25			V	I_C = 10μA
Forward current transfer ratio	H_{FE}	40	70			V_{CE} = 5V, I_C = 100μA
		60	100			V_{CE} = 5V, I_C = 1mA
		50	80			V_{CE} = 5V, I_C = 10mA
Saturation voltage	$V_{CE}(SAT)$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
	$V_{BE}(SAT)$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
Collector base leakage current	I_{CBO}			10	nA	V_{CB} = 10V
Collector isolation leakage current	I_{CIO}			10	nA	V_{CI} = 10V
Collector capacitance	C_{OB}			2	pF	V_{CB} = 5V
Base capacitance	C_{IB}			4	pF	V_{BE} = 0V
Collector isolation capacitance	C_{CI}			6	pF	V_{CI} = +5V
Transition frequency	f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA, Freq = 100MHz
Matching						
H_{FE1}/H_{FE2}		0.9		1.1		V_{CE} = 5V, I_C = 100μA
		0.9		1.1		V_{CE} = 5V, I_C = 1mA
$\|V_{BE1} - V_{BE2}\|$	ΔV_{BE}		0.45	3	mV	V_{CE} = 5V, I_C = 100μA
			0.45	3	mV	V_{CE} = 5V, I_C = 1mA
Temperature coefficient of ΔV_{BE}			2	10	μV/°C	V_{CE} = 5V, I_C = 100μA

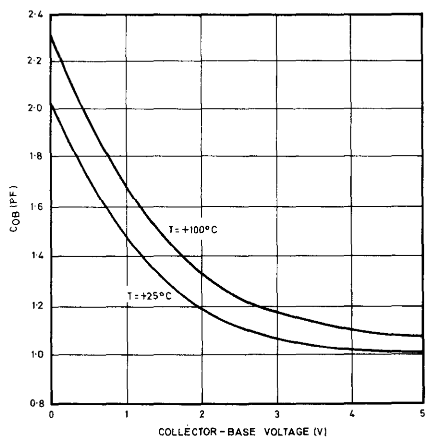


Fig. 2 Output capacitance (C_{ob}) v. voltage.

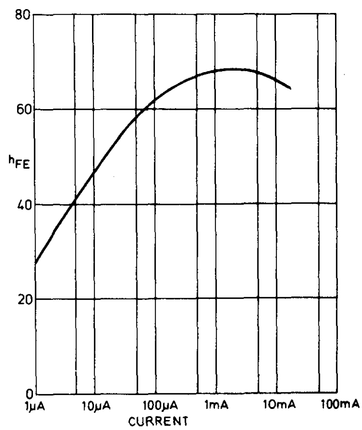


Fig. 3 Typical variation of h_{FE} with collector current

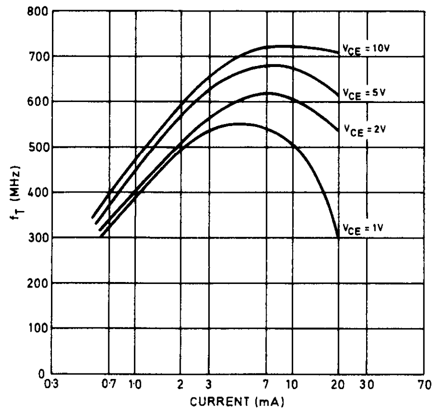


Fig.4 f_T v. collector current (f = 100MHz)

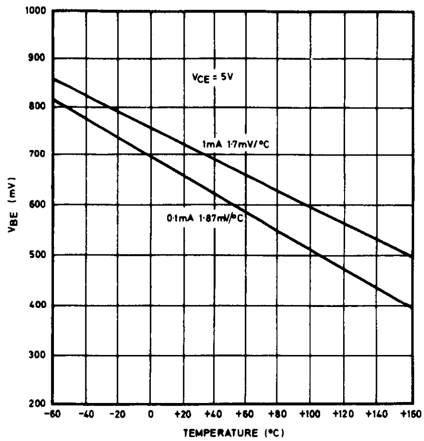


Fig. 5 V_{BE} v. temperature

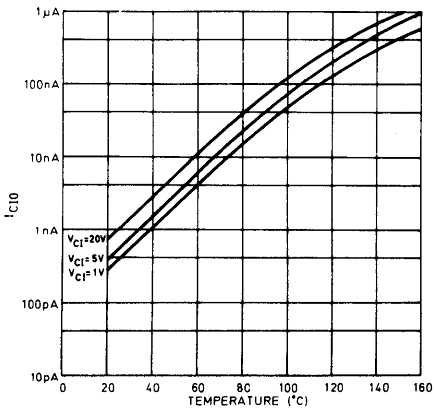


Fig. 6 Typical I_{CIO} v. temperature

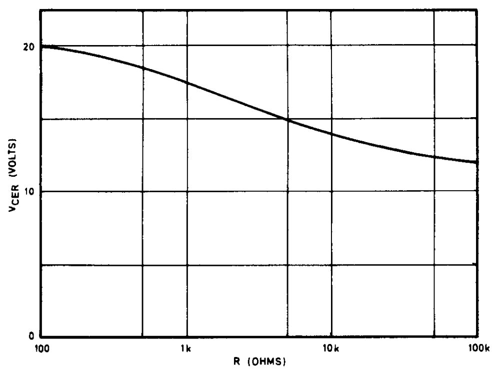


Fig. 7 Relationship between V_{CER} and R_{BE}

PLESSEY
Semiconductors

SL303L

400MHz TRIPLE NPN TRANSISTORS

The SL303 is a silicon monolithic integrated circuit comprising three separate transistors, two of which have closely matched parameters; the third transistor may be used as, for example, a tail transistor.

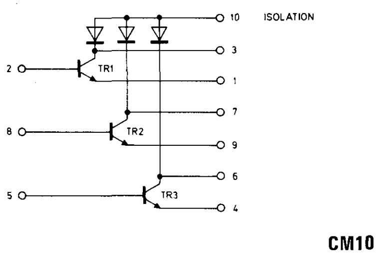


Fig. 1 Circuit diagram

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator

QUICK REFERENCE DATA

- Max voltage 12V to 20V
- Operating temperature range −55°C to +175°C

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	425° C/W (see Note)
Chip-to-case thermal resistance:	
TO-5 (CM)	265° C/W (see Note)
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see Figure 8)
V_{EBO}	4V
V_{CIO}	25V
I_{CM}	20mA

NOTE:
These figures are worst case, assuming all the power is dissipated in one transistor. If the power is equally shared between the three transistors, both thermal resistance figures can be reduced by 75° C/watt.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	20			V	$I_C = 10\mu A$
Collector emitter breakdown	BV_{CEO}	12			V	$I_C = 5mA$
Emitter base leakage current	I_{EBO}			1	μA	$V_{EB} = 4V$
Emitter base leakage current	I_{EBO}			10	nA	$V_{EB} = 2V$
Collector isolation breakdown	BV_{CIO}	25			V	$I_C = 10\mu A$
Forward current transfer ratio	H_{FE}	30	50			$V_{CE} = 5V, I_C = 10\mu A$
		40	70			$V_{CE} = 5V, I_C = 100\mu A$
		60	100			$V_{CE} = 5V, I_C = 1mA$
		50	80			$V_{CE} = 5V, I_C = 10mA$
Saturation voltage	$V_{CE}(SAT)$		0.36	0.6	V	$I_C = 10mA, I_B = 1mA$
	$V_{BE}(SAT)$	0.7	0.8	0.9	V	
Base emitter saturation voltage						$I_C = 10mA, I_B = 1mA$
Collector base leakage current	I_{CBO}			10	nA	$V_{CB} = 10V$
Collector isolation leakage current	I_{CIO}			10	nA	$V_{CI} = 10V$
Collector capacitance	C_{OB}			2	pF	$V_{CB} = 5V$
Base capacitance	C_{IB}			4	pF	$V_{BE} = 0V$
Collector isolation capacitance	C_{CIO}			6	pF	$V_{CI} = +5V$
Transition frequency	f_T	400	680		MHz	$V_{CE} = 5V, I_C = 5mA$
Matching						
TR1 & TR2 only						
H_{FE1}/H_{FE2}		0.9		1.1		$V_{CE} = 5V, I_C = 100\mu A$
		0.9		1.1		$V_{CE} = 5V, I_C = 1mA$
Input offset voltage	ΔV_{BE}			3	mV	$V_{CE} = 5V, I_C = 100\mu A$
				3	mV	$V_{CE} = 5V, I_C = 1mA$
Temperature coefficient of input offset voltage				10	$\mu V/°C$	$V_{CE} = 5V, I_C = 100\mu A$

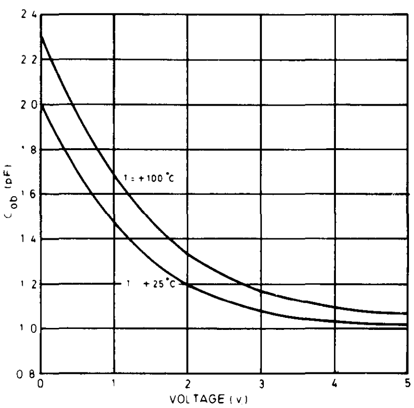


Fig. 2 Output capacitance (C_{ob}) v. voltage

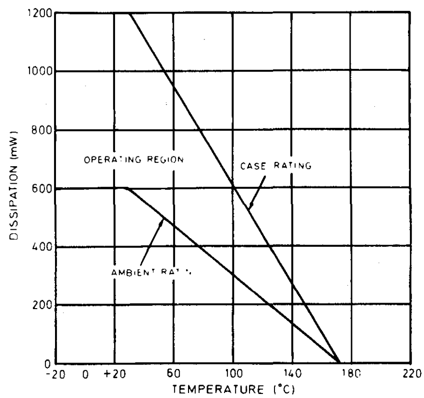


Fig. 3 Power dissipation derating curves (TO-5 package)

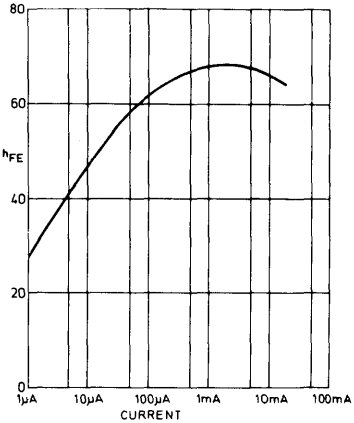


Fig. 4 Typical variation of h_{FE} with collector current

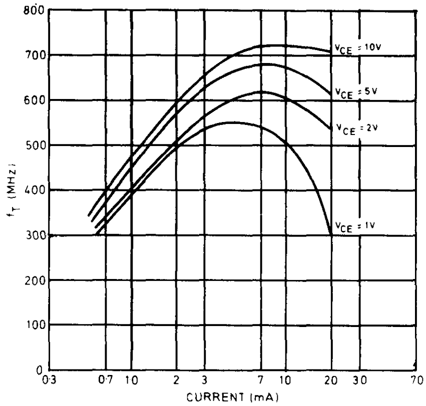


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. $f = 100$ MHz)

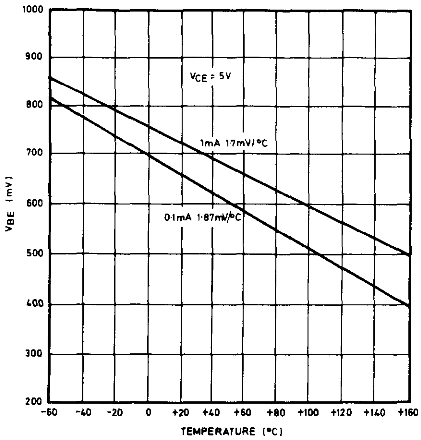


Fig. 6 V_{BE} v. temperature

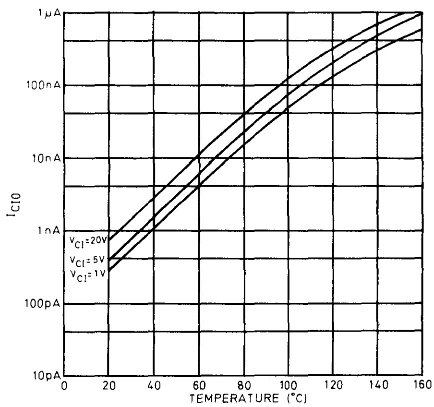


Fig. 7 Typical I_{CIO} v. temperature

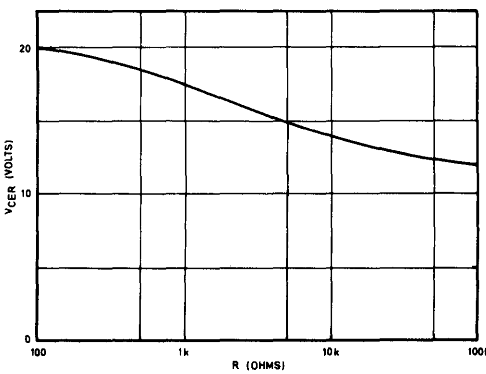


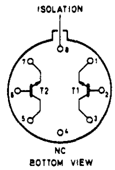
Fig.8 Relationship between V_{CER} and R_{BE}

PLESSEY
Semiconductors

SL360G & SL362C

HIGH PERFORMANCE NPN DUAL TRANSISTOR ARRAYS

The SL360G and SL362C are high performance NPN dual transistor arrays fabricated as monolithic silicon devices. They feature accurate parameter matching and close thermal tracking. They have high transition frequencies (typ. 2.2GHz) and low device capacitance. In addition the SL362C offers good noise performance (1.6dB noise figure at 60MHz).



CM8

Fig. 1 Pin connections

APPLICATIONS

- Instrumentation
- PCM Repeaters
- Analogue Signal Processing
- High Speed Switches – Digital and Analogue

FEATURES

- Accurate Parameter Matching.
- High f_T
- Low Noise (1.6dB at 60MHz SL362)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	Both	10	32		V	$I_C = 10\mu A$
Collector isolation breakdown	BV_{CIO}	Both	16	60		V	$I_C = 10\mu A$
Emitter base leakage	I_{EBO}	SL360/362			1	μA	$V_{EB} = 4V$
Emitter base leakage	I_{EBO}	SL360			1	nA	$V_{EB} = 2V$
Collector emitter breakdown	LV_{CEO}	All	7	14		V	$I_C = 5mA$
DC current gain	H_{FE}	SL360	30	65			$V_{CE} = 2V, I_E = 5mA$
		SL362	30	70			$V_{CE} = 2V, I_E = 1mA$
Transition frequency	f_T	SL360	1.6	2.2		GHz	$V_{CE} = 2.5V, I_E = 25mA$, f =200MHz
		SL362	1.4	2.0		GHz	$V_{CE} = 5V, I_F = 5mA$, f =200MHz
Input offset voltage	$V_{BE1} - V_{BE2}$	SL360		3	10	mV	$V_{CE} = 2V, I_E = 1mA$
		SL362		5		mV	$V_{CE} = 2V, I_E = 1mA$
Input offset current	H_{FE1}/H_{FE2}	Both	0.9	1.0	1.1		$V_{CE} = 2V, I_E = 5mA$
Saturation voltage	$V_{CE}(SAT)$	SL360		0.25	0.6	V	$I_E = 10mA, I_B = 1mA$
Noise figure	NF	SL362		1.6	2.0	dB	$I_E = 1mA, R_S = 200\Omega$, f =60MHz
Collector base capacitance	C_{OB}	SL360		0.5		pF	$V_{CB} = 0V$
		SL362		1.3		pF	$V_{CB} = 0V$
Collector isolation capacitance	C_{CI}	SL360		2.3		pF	$V_{CI} = 0V$
		SL362		3.8		pF	$V_{CI} = 0V$
Emitter base capacitance	C_{TE}	SL360		0.5		pF	$V_{BE} = 0V$
		SL362		2.1		pF	$V_{BE} = 0V$
Forward base emitter voltage	$V_{BE}(ON)$	SL360		0.72		V	$I_E = 1mA, V_{CE} = 2V$
Collector base leakage	I_{CBO}	SL360			1	nA	$V_{CB} = 10V$
Collector isolation leakage	I_{CIO}	SL360			1	nA	$V_{CI} = 10V$

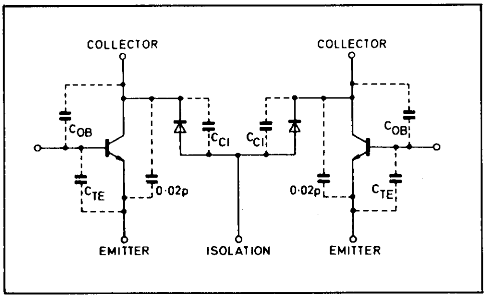


Fig.2 Equivalent circuit for SL360, SL362

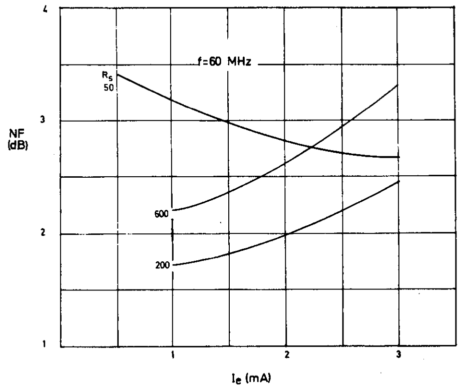


Fig. 3 Typical noise figure emitter current for SL362

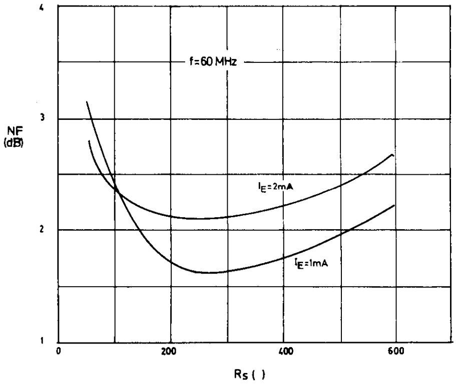


Fig. 4 Typical noise figure v source impedance for SL362

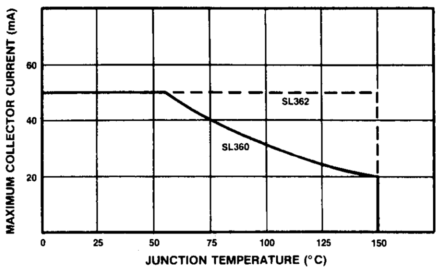


Fig.5 Max. continuous collector current vs junction temperature

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Electrical ratings

V_{CB} = 10V V_{EB} = 4V V_{CE} = 8V
V_{CI} = 16V I_C = 20mA (SL360); 50mA (SL362) (see Figure 5)

Thermal ratings

	CM8
Storage temperature	−55°C to +150°C
Operating junction temperature	150°C
Thermal resistance (see Note 2)	
Chip-to-case	265° C/W
Chip-to-ambient	425° C/W

These figures are worst case, assuming all power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50° C/watt.

PLESSEY
Semiconductors

SL521A, B & C

140MHz WIDEBAND LOG AMPLIFIER

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12 dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency.

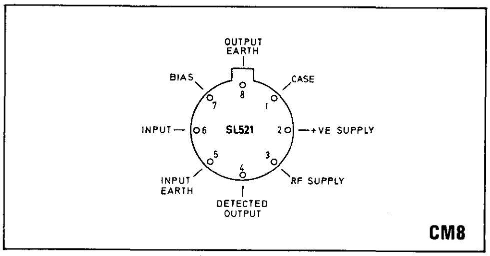


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS
(Non-simultaneous)

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

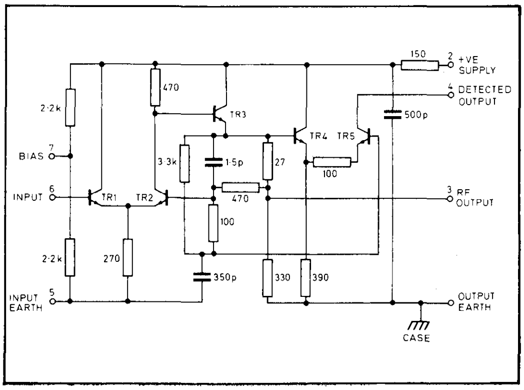


Fig. 2 SL521 Circuit diagram

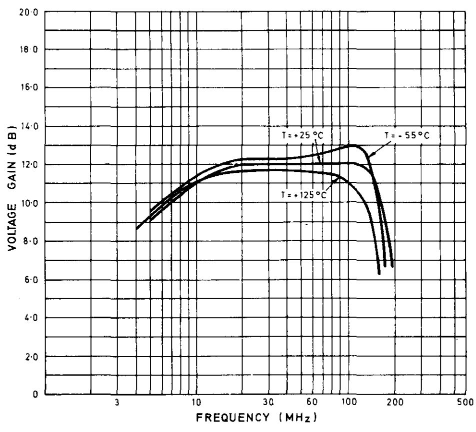


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain, f = 30MHz	A	11.5		12.5	dB	10 ohms source, 8pF load
	B	11.3		12.7	dB	
	C	11.0		13.0	dB	
Voltage gain, f = 60MHz	A	11.3		12.7	dB	
	B	11.0		13.0	dB	
	C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	A	150	170		MHz	10 ohms source, 8pF load
	B	140	170		MHz	
	C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	A B C		5	7	MHz	10 ohms source, 8pF load
Propagation delay	A B C		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	A	1.00		1.10	mA	f = 60MHz, 0.5V rms input
	B	0.95		1.15	mA	
	C	0.90		1.20	mA	
Variation of gain with supply voltage	A B C		0.7		db/V	
Variation of maximum rectified output current with supply voltage	A B C		25		%/V	
Maximum input signal before overload	ABC	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	A	12.5	15.0	18.0	mA	
	B	12.5	15.0	18.0	mA	
	C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

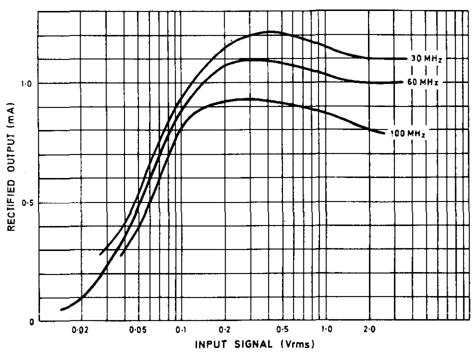


Fig. 4 Rectified output current v. input signal

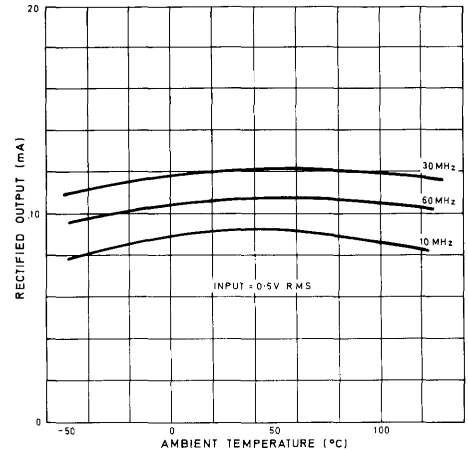


Fig. 5 Maximum rectified output current v. temperature

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

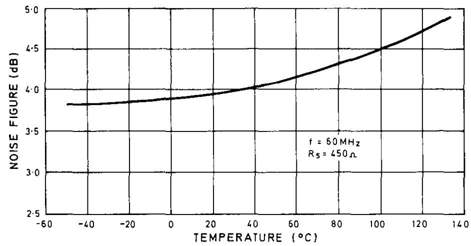


Fig. 6 Typical noise figure v. temperature

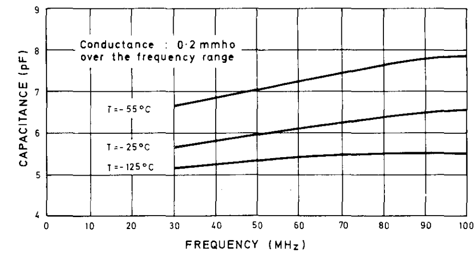


Fig. 7 Input admittance with open-circuit output

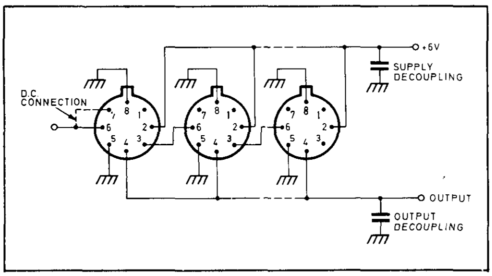


Fig. 8 Direct coupled amplifiers

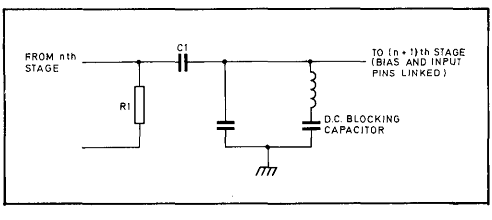


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos } (f = 10\text{MHz})$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \ (f = 10\text{MHz})$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

PLESSEY
Semiconductors

SL523B,C&HB

120MHz DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz. They are pin-compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers, internally connected in cascade. Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum output of 2.1mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier. RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1.8V RMS without damage.

The SL523HB is supplied in matched sets of eight devices. The gain at 60MHz of the devices in the set is matched to 0.75dB. In all other respects the device is identical to an SL523B. This selection enables very precise log strips to be produced. Supplied only to Plessey Level B screening including burn-in.

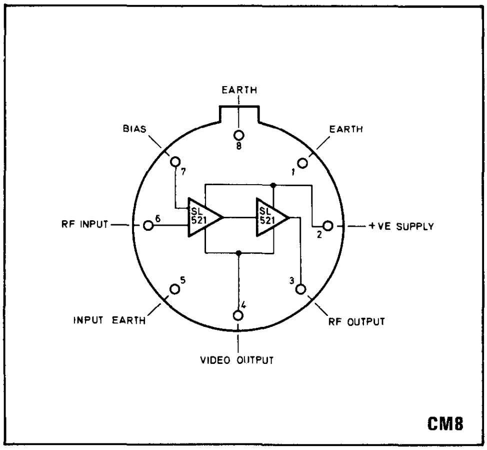


Fig. 1 Pin connections (view from beneath)

FEATURES

- Small Size/Weight
- Lower Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

QUICK REFERENCE DATA

Small Signal Voltage Gain	24dB
Detector Output Current	2.1mA
Noise Figure	4dB
Frequency Range	10 – 100MHz
Supply Voltage	+6V
Supply Current	30mA

ABSOLUTE MAXIMUM RATINGS

(Non simultaneous)

Storage temperature range	−55°C to + 175°C
Operating temperature range	−55°C to +125°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

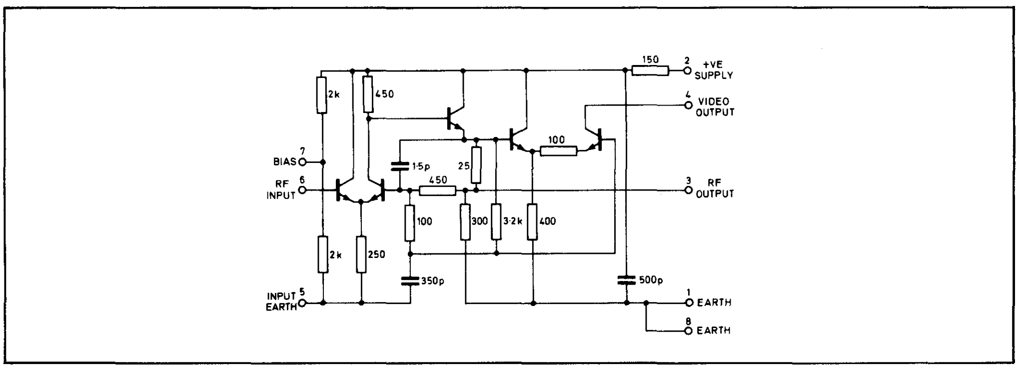


Fig. 2 Circuit diagram (one amplifier)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature 22°C ±2°C
Supply voltage +6V
DC connection between pins 6 and 7
Source impedance 10 Ω
Load impedance 8pF
Frequency 60MHz

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B H C	22.6 22	24 24	25.4 26	dB dB	Freq. = 30MHz
Small signal voltage gain	B H C	22 21.4	24 24	26 26.6	dB dB	Freq. = 60MHz
Gain variation (set of 8)	H		0.5	0.75	dB	Freq. = 60MHz
Upper cut off frequency	B C & H	120	150		MHz	
Lower cut-off frequency	B C & H		10	15	MHz	
Propagation delay	B C & H		4		ns	
Maximum rectified video output current	B H C	1.9 1.8	2.1 2.1	2.3 2.4	mA mA	V_{in} 0.5VRMS
Maximum input signal before overload	B C & H	1.8	1.9		VRMS	
Noise figure			4	5.25	dB	Source impedance 450 Ω
Supply current	B H C	25 23	30 30	36 38	mA mA	
Maximum RF output voltage	B C & H		1.2		Vp-p	

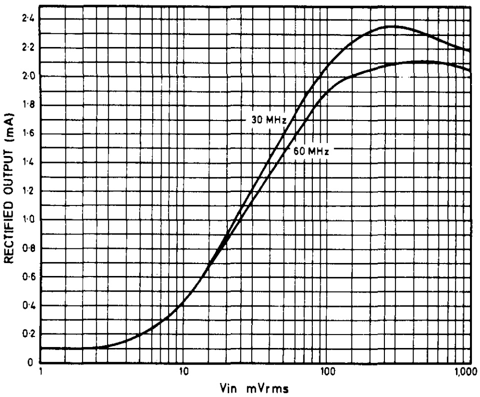


Fig. 3 Rectified output current v. input signal

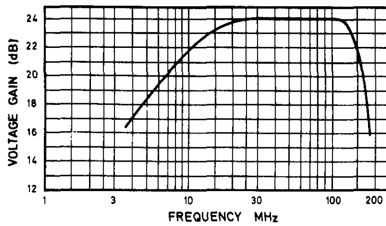
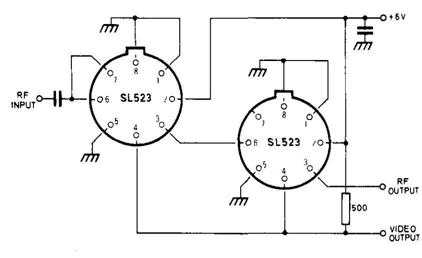


Fig. 4 Voltage gain v. frequency



Frequency range: 10 to 100MHz
Log.range: 45dB
RF small signal gain: 48dB
Video output: 2Vpeak

Fig. 5 Simple log.IF strip

OPERATING NOTES

The amplifier is designed to be directly coupled (see Fig. 5)

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The network chosen must give unity voltage gain at resonance to avoid distorting the log law. The typical value for input impedance is 500 ohms in parallel with 5pF and the output impedance is typically 30 ohms.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded. Minimum values for this capacitor are: 2 stages – 3nF, 3 or more stages – 30nF.

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line. The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig.6 will eliminate feed-back on the video line.

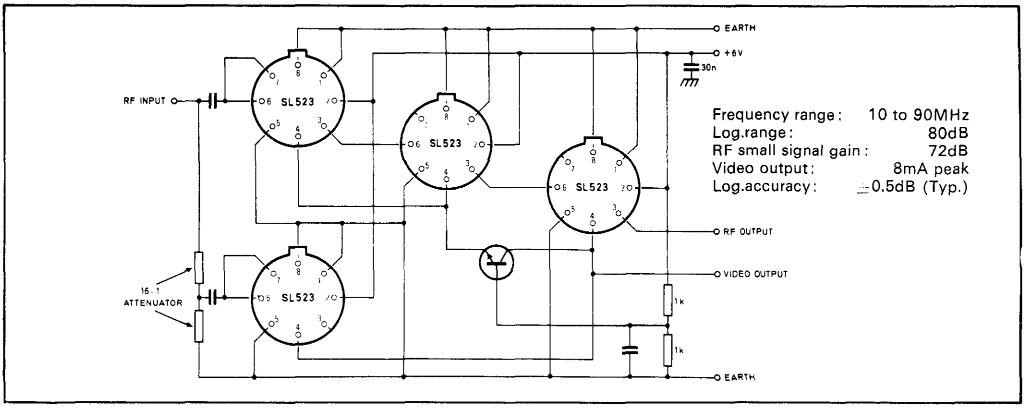


Fig. 6 Wide dynamic range log.IF strip

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wide-band logarithmic amplifier, described in RSRE Memo. No.3027 and shown in Fig. 7.
The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB. The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope.

Fig. 8 shows the dynamic range error curve and frequency response obtained. The stage gains of the SL523 devices used were as shown in Table 1.

Stages	f_o (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.123	
2	60	24.089	0.235
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v. output characteristic (Fig. 8a) is calibrated at 10dB/cm in the X axis and 1V/cm in the Y axis. 80dB of dynamic range was attained.

The error characteristic (Fig. 8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log. input v. output characteristic and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of ±0.5dB.

As a comparison, the log amplifier of Fig. 7 was constructed with randomly selected SL521Bs (two SL521Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig. 9a) with an accuracy of ±0.75dB (Fig. 9b).

Bandwidth curves are shown in Figs. 8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz. Using SL523Bs (Fig. 8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz. Fig. 9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum.

These tests show that the SL523 is a very successful dual-stage log.amplifier element and, since it is pin-compatible with the SL521, enables retrofit to be carried out in existing log.amplifiers. It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line.

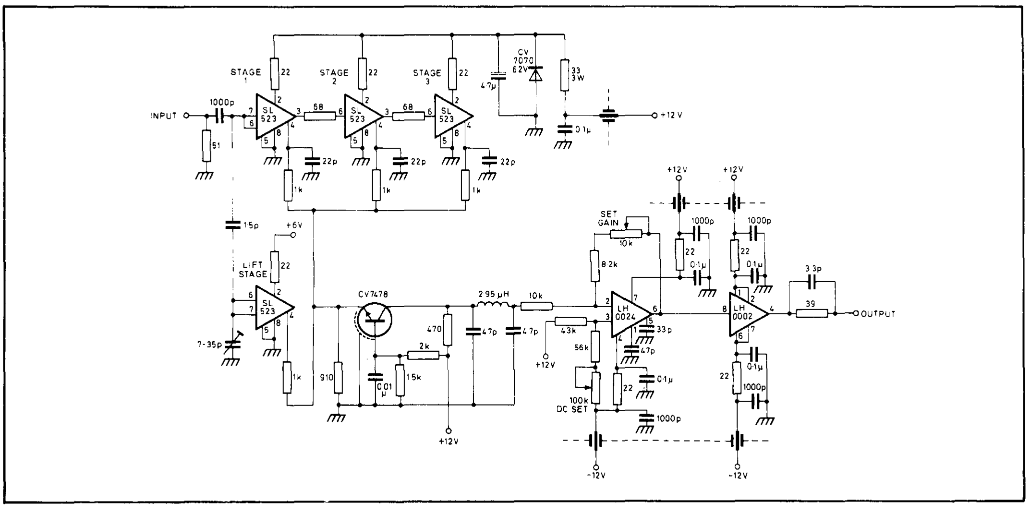


Fig. 7 Wideband logarithmic amplifier

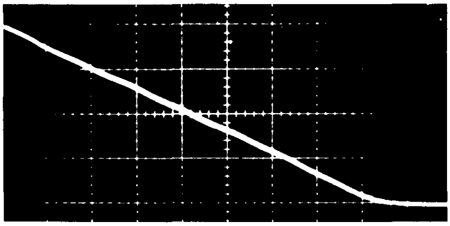


Fig. 8a Input/output

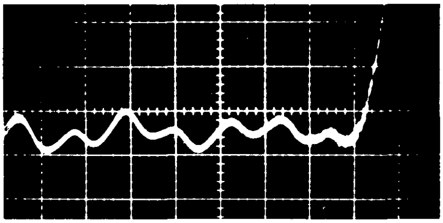


Fig. 8b Error curve

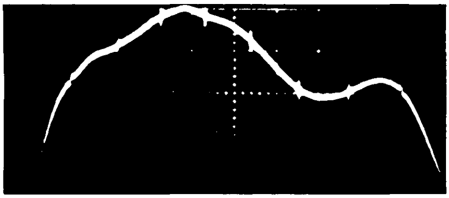


Fig. 8c Frequency response, detected output

Fig. 8 Characteristics of circuit shown in Fig. 7 using SL523Bs

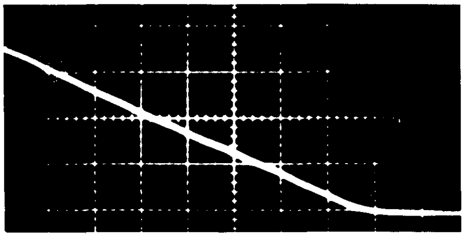


Fig.9a Input/output

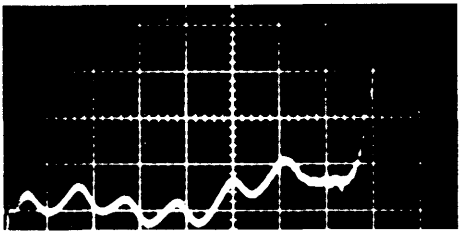


Fig. 9b Error curve

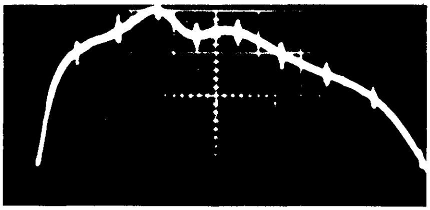


Fig. 9c Frequency response, detected output

Fig. 9 Characteristics of circuit shown in Fig. 7 using SL521Bs

PLESSEY
Semiconductors

SL531C

250MHz TRUE LOG IF AMPLIFIER

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

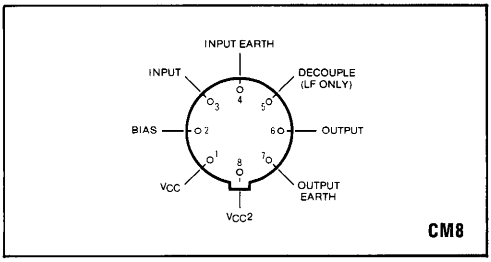


Fig. 1 Pin connections

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with:–

- Log Range 70 dB
- Centre frequencies 10 – 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15 volts
Storage temperature range	−55°C to + 150°C
Operating temperature range	−55°C to +125°C See operating notes
Max junction temperature	150°C
Junction — ambient thermal resistance	220°C/Watt
Junction — case thermal resistance	80°C/Watt

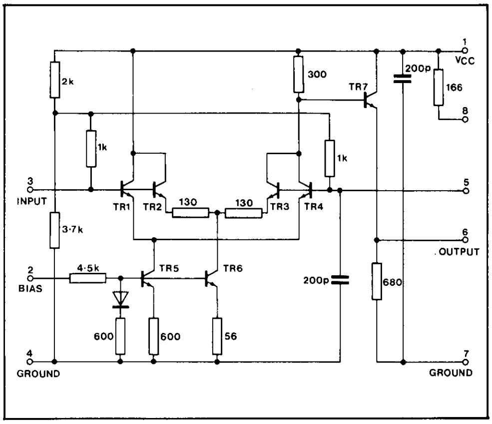


Fig. 2 Circuit diagram

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

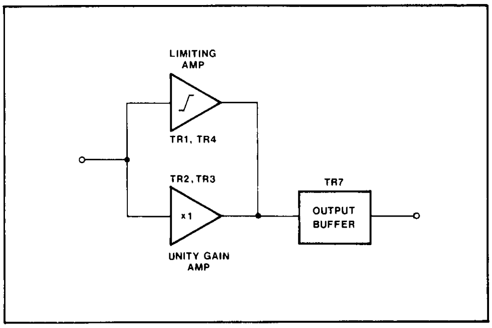


Fig. 3 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature 22± 2°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	Vin = −30 dBm
High level slope gain	−1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	−3dB w.r.t. ± 60 MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	-Vin = 30 dBm to + 10 dBm
Input impedance	2.5pf parallel with 1k				f = 10 - 200MHz
Output impedance	15Ω series with 25nh				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

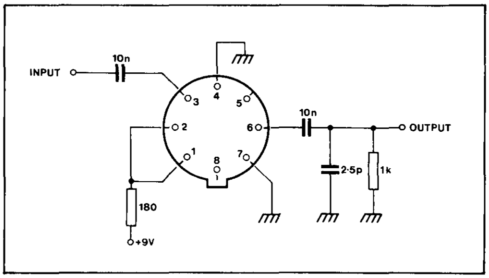


Fig. 4 Test circuit

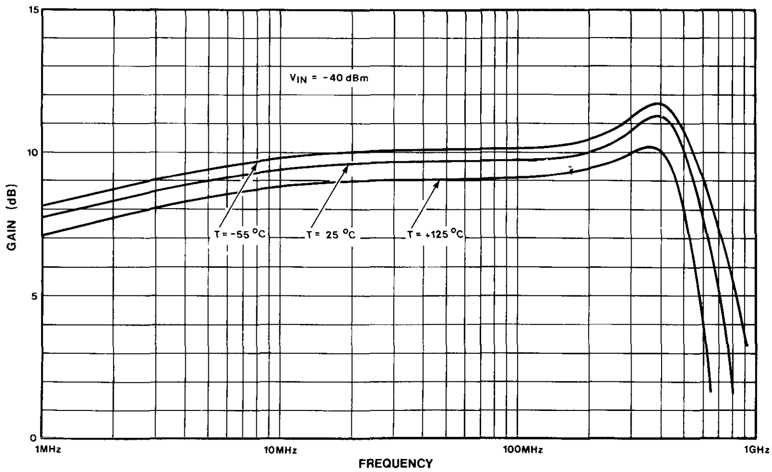


Fig. 5 Small signal frequency response

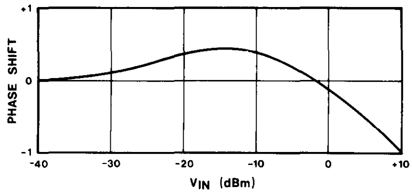


Fig. 6 Phase v. input

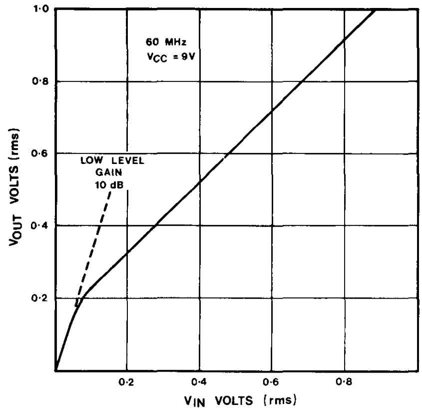


Fig. 7 Transfer characteristics linear plot

TYPICAL APPLICATION – 6 STAGE LOG STIP

Input log range 0dBm to −70dBm
Low level gain 60dB (−70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10 – 200MHz

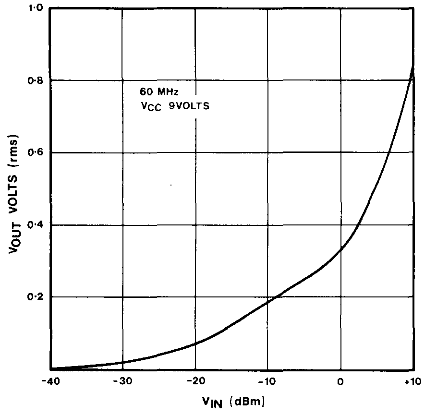


Fig. 8 Transfer characteristics logarithmic input scale

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip. The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient. If the ambient can be limited to + 100°C then the internal resistor can be used to reduce the external component count. Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer, the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

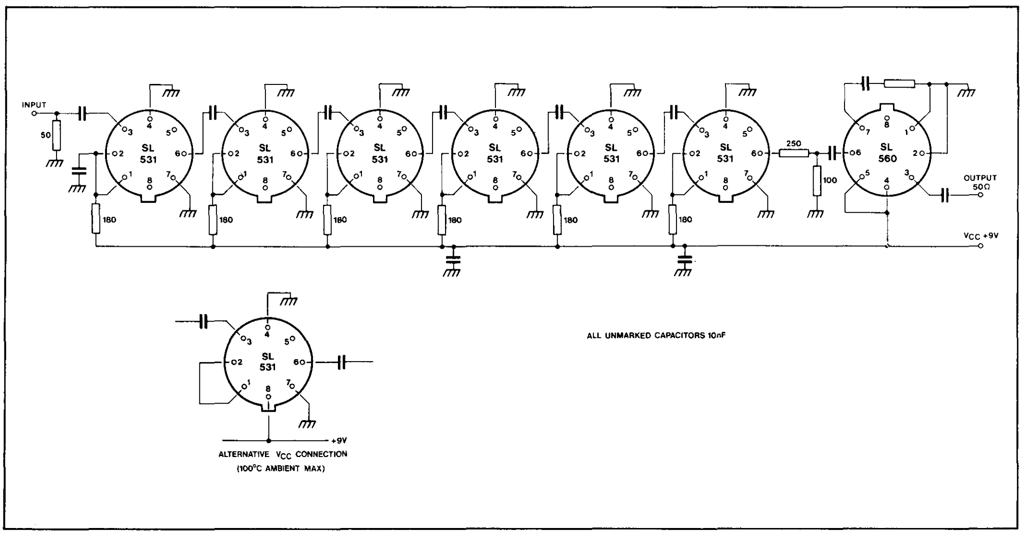


Fig. 9 Circuit diagram 6 stage strip

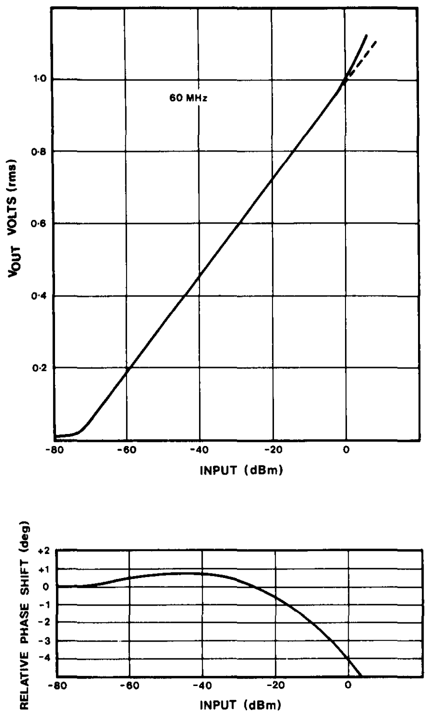


Fig. 10 Transfer function of log strip

PLESSEY
Semiconductors

SL532C

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wide band limiting IF strips. It offers a bandwidth of over 400MHz and very low phase shift with amplitude. The small signal gain is 12dB and the limited output is 1volt peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than 1° phase shift when overdriven by 12dB. The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

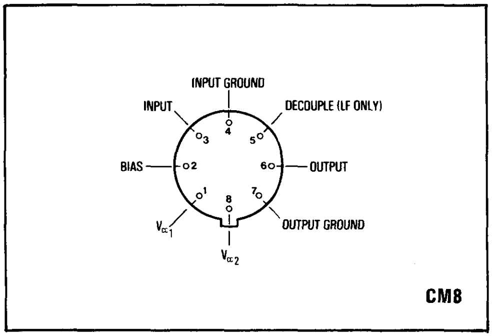


Fig.1 Pin connections

FEATURES

- Low Phase Shift v. Amplitude
- Wide Bandwidth
- Low External Component Count

APPLICATIONS

- Phase Recovery Strips in Radar and ECM Systems (e.g. Doppler)
- Limiting Amps for SAW Pulse Compression Systems
- Phase Monopulse Radars
- Phased Array Radars
- Low Noise Oscillators

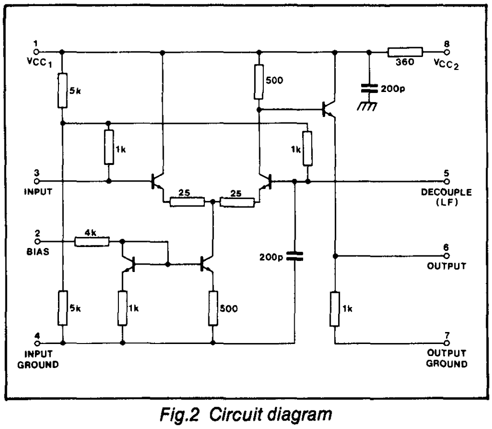


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature (Ambient) 25°C
Frequency 60MHz
$V_{CC} = +9V$
$R_L = 1k\Omega // 2.5pF$

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature (ambient) 25°C ± 2°C
Frequency 60MHz : R_L = 1kΩ / 5pF : V_{IN} = -30dBm
V_{CC} = +9.0V : R_S = 50Ω

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	12.8	14	dB	
Small signal voltage gain		12.5		dB	f = 150MHz
-1dB compression point		-10		dBm	
Limited output voltage	1.0	1.15	1.4	V p-p	V_{in} = +10dBm
Limited output voltage		1.10		V p-p	f = 150MHz
Upper cut off frequency	250			MHz	-3dB wrt 60MHz
Lower cut off frequency			10	MHz	May be extended by decoupling pin 5
Supply current	6	8.5	11	mA	No signal
Phase variation with signal level		±1	±3	Degrees	-30dBm to +10dBm
		±1.5		Degrees	-30dBm to 0dBm. f = 150MHz
Absolute phase shift		-34		Degrees	f = 100MHz
input to output		-43		Degrees	f = 150MHz
		-69		Degrees	f = 200MHz
Input impedance		1kΩ/2.5pF			
Output impedance		30Ω			
Noise figure		7		dB	400Ω source impedance. f = 60MHz
Gain variation with temperature		±1		dB	-40°C to +85°C
Phase variation with temperature		± 0.5		Degrees	-40°C to +85°C at any level between -30dBm to +10dBm
Limited output voltage variation with temperature		±0.05		V p-p	V_{in} = +10dBm -40°C to +85°C

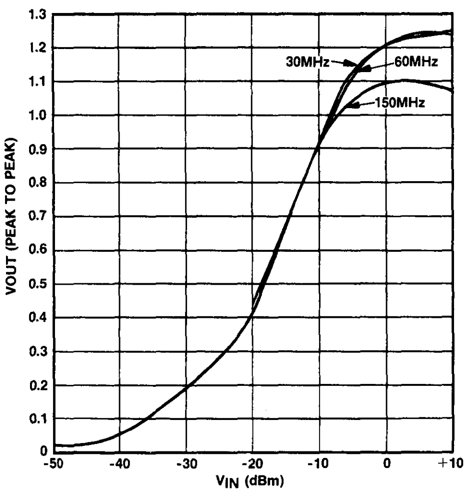


Fig.3 Transfer characteristic of a single stage

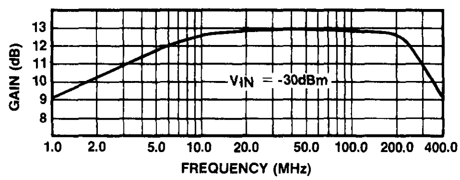


Fig.4 Gain/frequency curve of a typical device

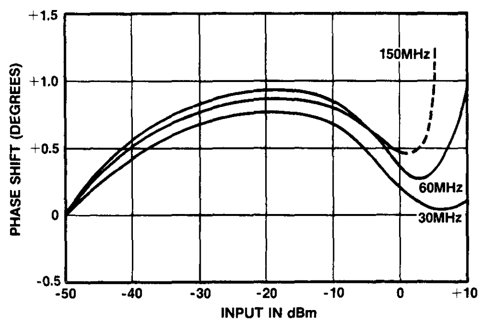
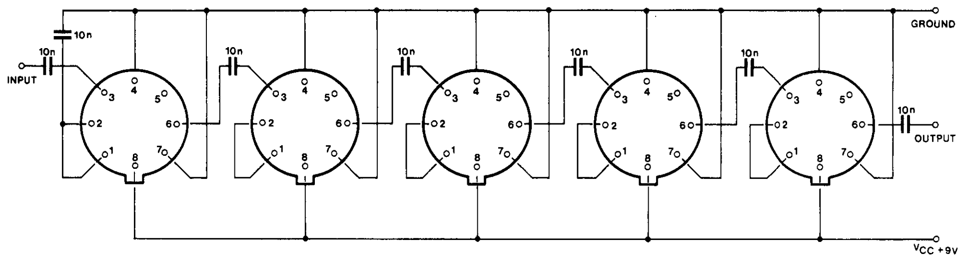


Fig.5 Phase change with input level

TYPICAL APPLICATION

Five stage strip

Input signal for full limiting	300μV rms -57dBm
Limited output	1V p-p
Phase shift (V_{IN} -57 → +10dBm)	±3° typ.



The recommended output buffer amplifier to drive 50Ω loads is the SL560C

Fig.6 Five stage IF strip

CIRCUIT DESCRIPTION

The SL532 uses a long-tailed pair limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15V
Storage temperature range	-55°C to +150°C
Operating temperature range	-55°C to +125°C

PLESSEY
Semiconductors

SL541B

HIGH SLEW RATE OPERATIONAL AMPLIFIER

The SL541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of ±5mV maximum and replaces the SL541C.

The SL541B is tested in two circuit applications (A and B).

FEATURES

- High Slew Rate: 175V/µs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B)
- Wide Bandwidth: DC to 100MHz at 10dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum
- Full Military Temperature Range (DIL Only)
  Package: 10 Lead TO-5
  14 Lead DIL Ceramic

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V+ to V−)		24V
Input voltage (Inv. I/P to non inv. I/P)		±9V
Storage temperature		−55°C to +175°C
Chip operating temperature		+175°C
Operating temperature:	TO-5:	−55°C to +85°C
	DIL:	−55°C to +125°C

Thermal resistances

Chip-to-ambient:	TO-5	220°C/W
	DIL	125°C/W
Chip-to-case:	TO-5	60°C/W
	DIL	40°C/W

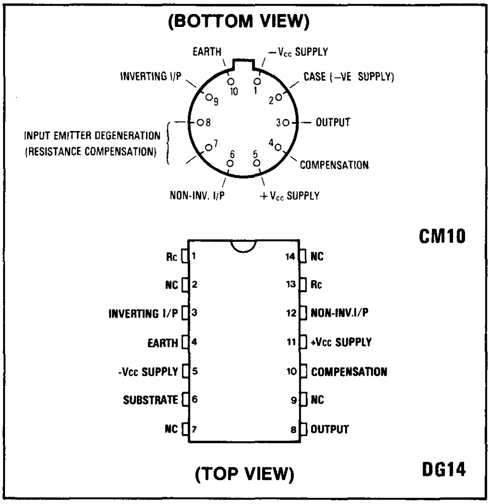


Fig. 1 Pin connections

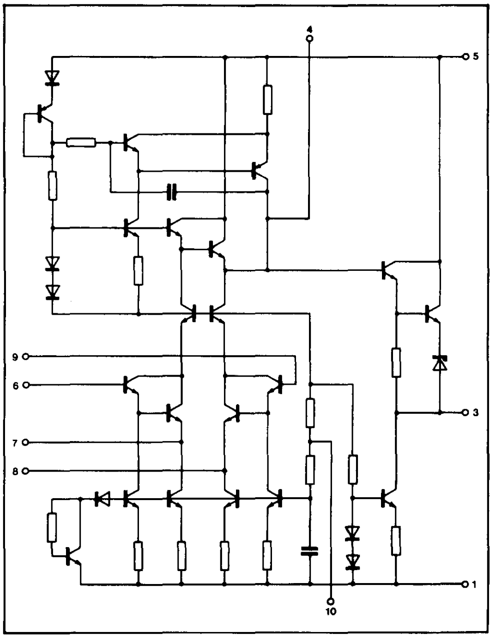


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C
R_C = 0Ω
Test circuits: see Fig.8

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	μA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
	B	60	71		dB	
Open loop temperature coefficient	A,B		-0.02		dB/° C	
Closed loop bandwidth (-3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/μs	X10 gain
Settling time to 1 %	A,B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5.7		V	
(-ve)	A		-1.9	-1.5	V	
(+ve)	B	2.5	3.0		V	
(-ve)	B		-3.0	-2.5	V	
Maximum output current	A,B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	Non-inverting modes
(-ve)	A	-1			V	
(+ve)	B			3	V	
(-ve)	B	-3			V	
Supply line rejection						
(+ve)	A,B	54	66		dB	
(-ve)	A,B	46	54		dB	
Input offset current	A,B			9.85	μA	
Common mode rejection	A,B	60.7			dB	
Input offset voltage drift	A		25		μV/° C	

ELECTRICAL CHARACTERISTICS (Typical)

Test conditions (unless otherwise stated):

T_{amb} = -55° C to +85° C (TO5)
T_{amb} = -55° C to +125° C (DIL only)
R_C = 0Ω, Test circuit B

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current			16	25	mA	
Input bias current				35	μA	
Input offset voltage	(+ve)			8	mV	
	(-ve)	-8			mV	
Maximum output current		3.5	6.5		mA	
Maximum input voltage	(+ve)			3	V	Non-inverting modes
	(-ve)	-3			V	
Supply line rejection	(+ve)	50			dB	
	(-ve)	42			dB	
Maximum output voltage	(+ve)	2.3			V	
	(-ve)			-2.5	V	
Common mode rejection		55			dB	
Input offset current				16	μA	
Output voltage drift			15		μV/° C	
Input bias current drift			60		nA/° C	
Output current drift			40		nA/° C	

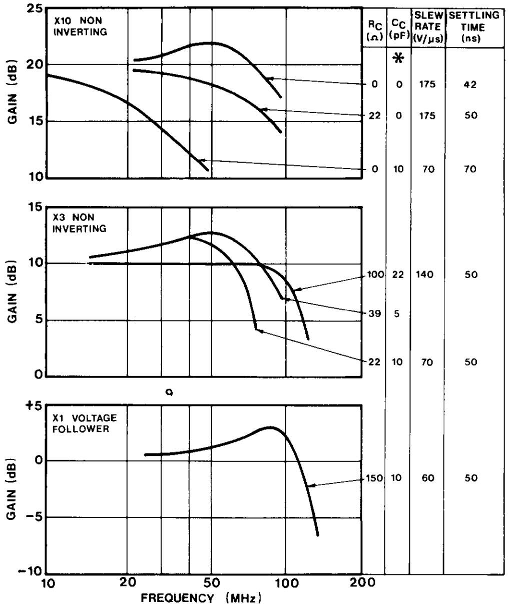


*Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ/10pF) * See operating note 2*

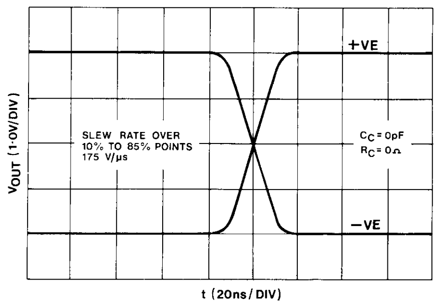


Fig.4 Slew rate - X10 non-inverting mode
Input square wave 0.4V p/p

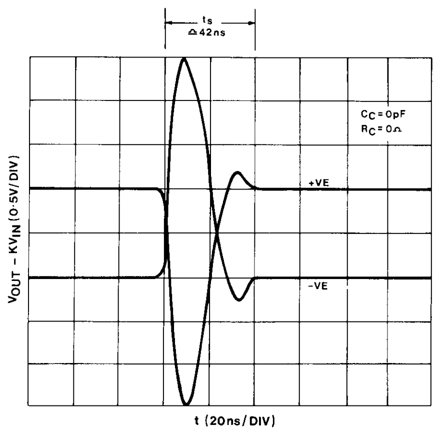


Fig.5 Settling time - X10 non-inverting mode

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (<1kΩ), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit (circuit B only).

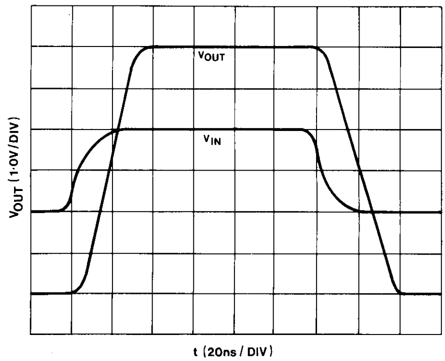


Fig.6 Output clipping levels - X10 non-inverting mode
Input moderately overdriven, so that output goes into clipping both sides

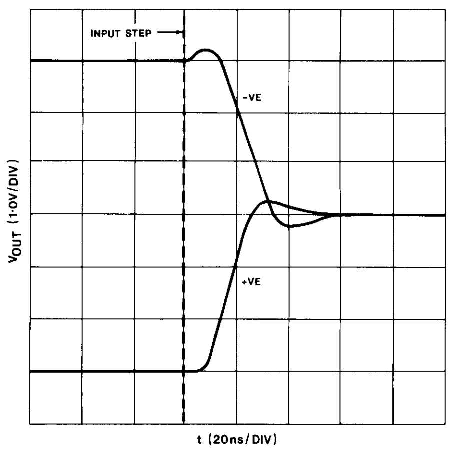


Fig.7 Output clippings levels - X10 non-inverting mode.
Output goes from clipping to zero volts. V_{in} = 3V peak step, offset +ve or -ve.

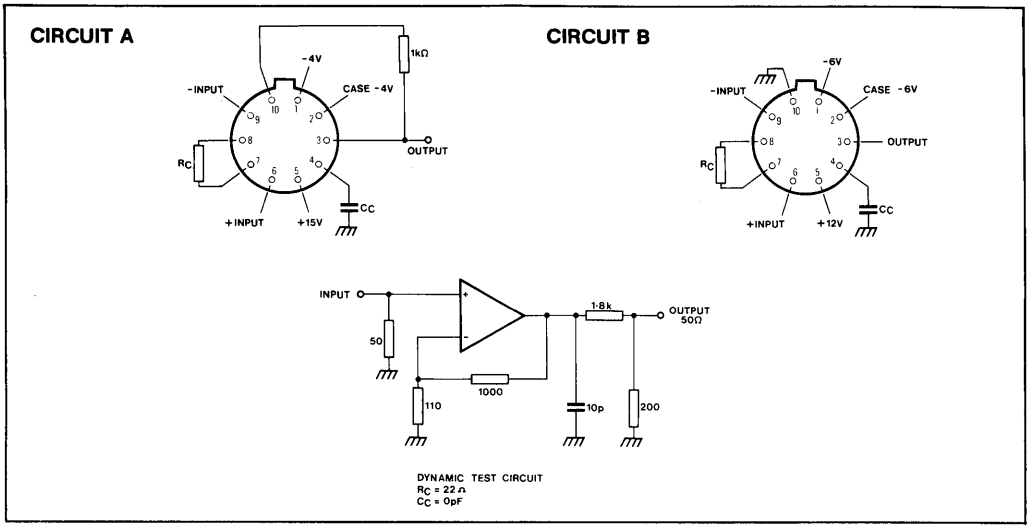


Fig. 8 Test circuits

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

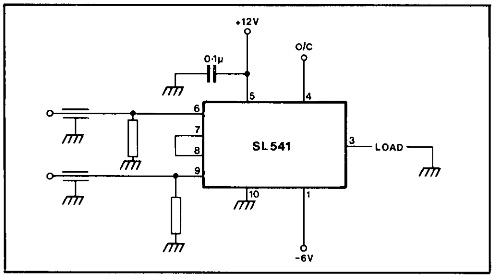


Fig. 9 Non-saturating sense amplifier (30V/µs for 5mV)
Note: the output may be caught at a pre-determined level. (TO-5 pin nos.)

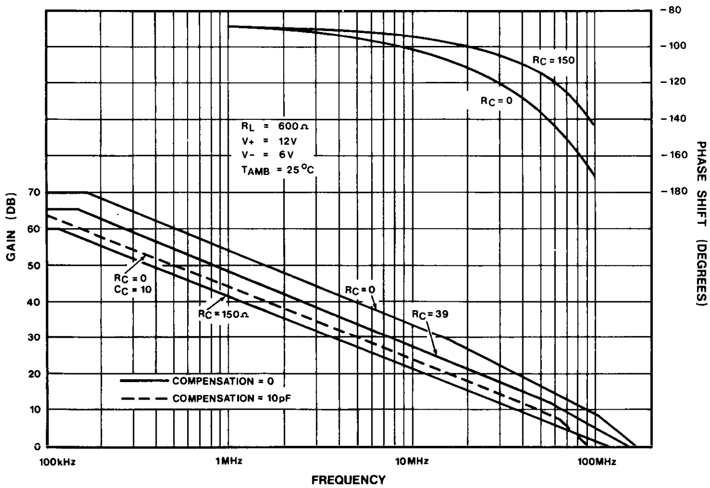


Fig.10 SL541B open loop gain and phase shift v. frequency

PLESSEY Semiconductors

SL550 D & G

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60MHz, the SL550G noise figure is 1.8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance load to be driven.

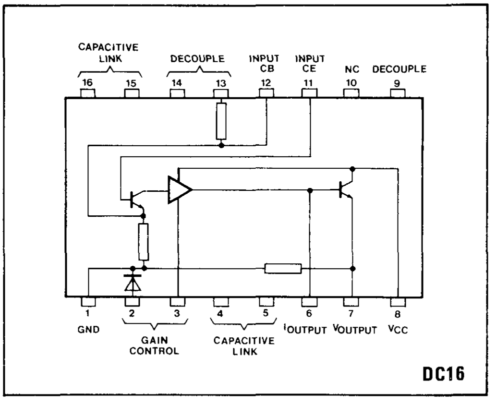


Fig. 1 Pin connections (top view)

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

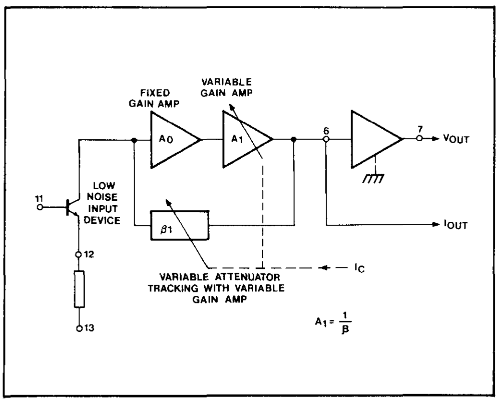


Fig. 2 Functional diagram

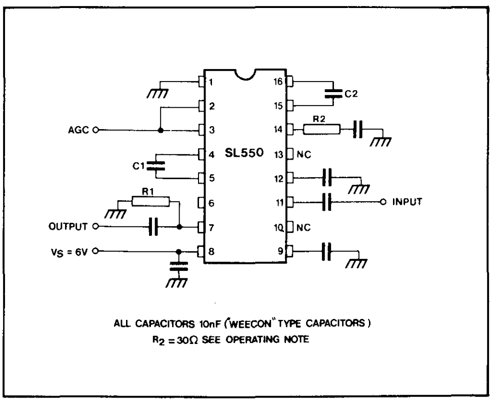


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
f = 30MHz, V_S = +6V, R_L = 200Ω, I_C = O, R_1 = 750Ω, T_{amb} = +25°C

Characteristic	Circuit	Value Min.	Typ.	Max.	Units	Conditions
Voltage gain	SL550G	39	42	44	dB	
	SL550D	35	40	45	dB	
Gain control characteristic	Both		See note 1			
Gain reduction at mid-point	SL550G		10		dB	I_C = 0.24mA
	SL550D		9		dB	I_C = 0.2mA
Max. gain reduction	SL550G	20	25		dB	I_C = 2.0mA
	SL550D		25		dB	I_C = 2.0mA
Noise figure	SL550G		2.0	2.7	dB	R_S = 200Ω
	SL550G		3.5		dB	R_S = 50Ω
	SL550D		3.0		dB	R_S = 200Ω
Output voltage	Both		0.15		Vrms	R_1 = ∞
	Both		0.3		Vrms	R_1 = 750Ω
Supply current	SL550G		11	13	mA	R_1 = ∞
	SL550G		15		mA	R_1 = 750Ω
	SL550D		11	20	mA	R_1 = ∞
Gain variation with supply voltage	Both		0.2		dB/V	V_S = 6 to 9V
Upper cut-off frequency (—3dB wrt 30MHz)	Both		125		MHz	
Gain variation with temperature (see note 2)	Both		±3		dB	T_{amb} = —55 to +125°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz.

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1 μA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range —55°C to +125°C (Figs. 6 and 7).

Low Input Impedance

A low input impedance (≃25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.

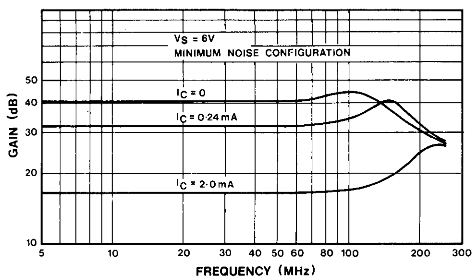


Fig. 4 Frequency response

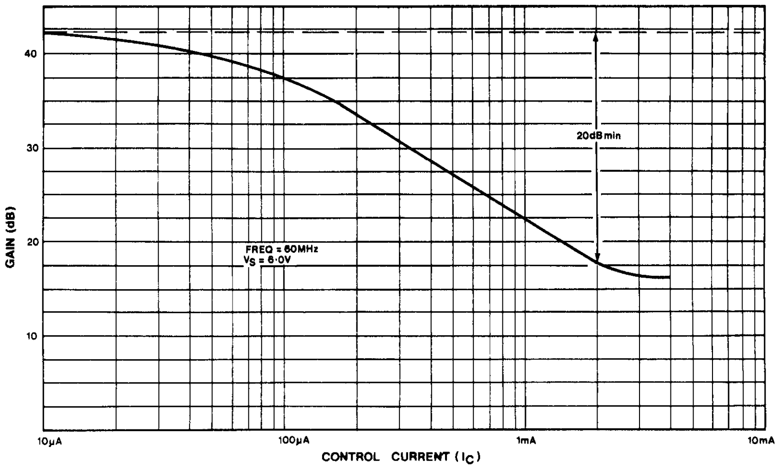


Fig. 5 Gain control characteristic

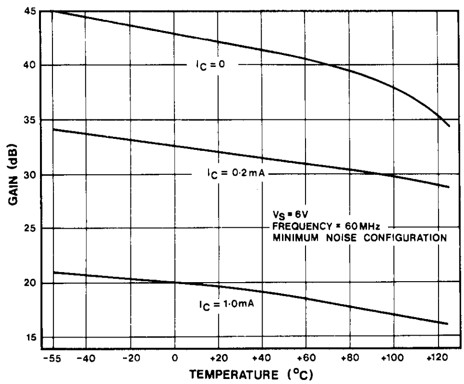


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration)

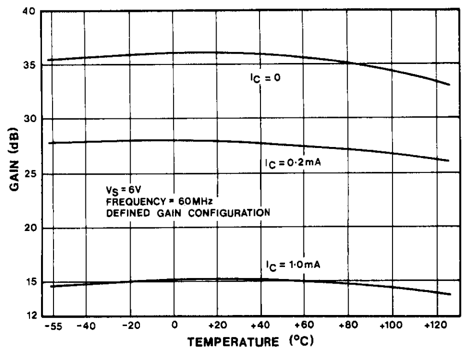


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes)

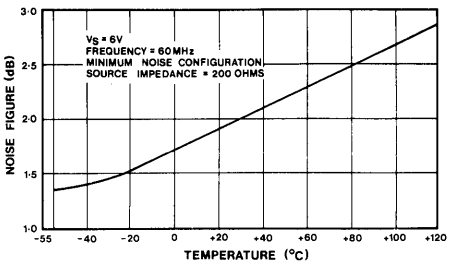


Fig. 8 Typical noise figure (SL550G)

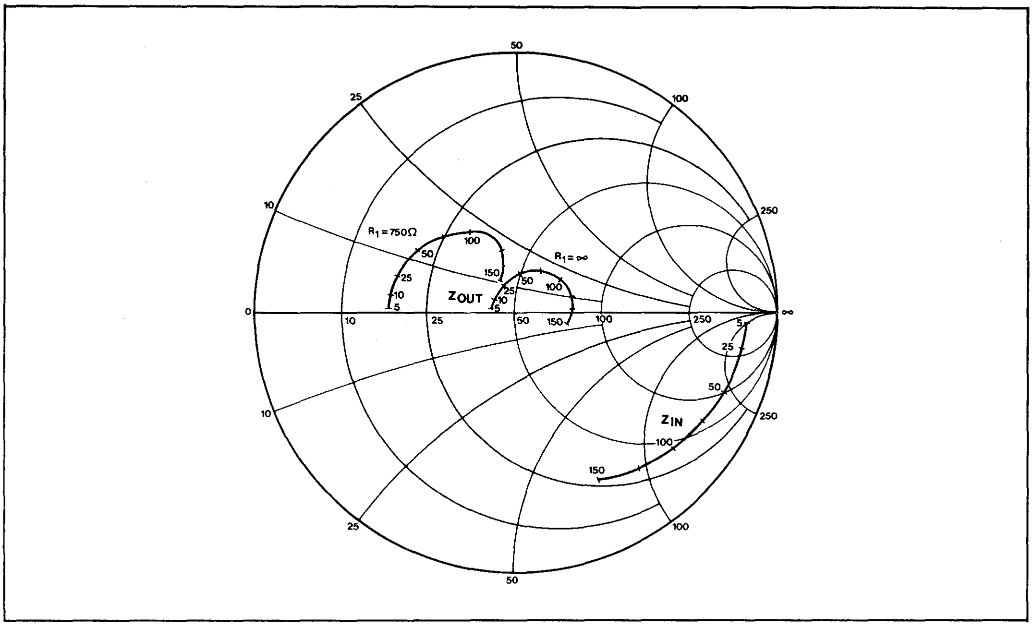


Fig. 9 Input and output impedances ($V_S = 6V$)

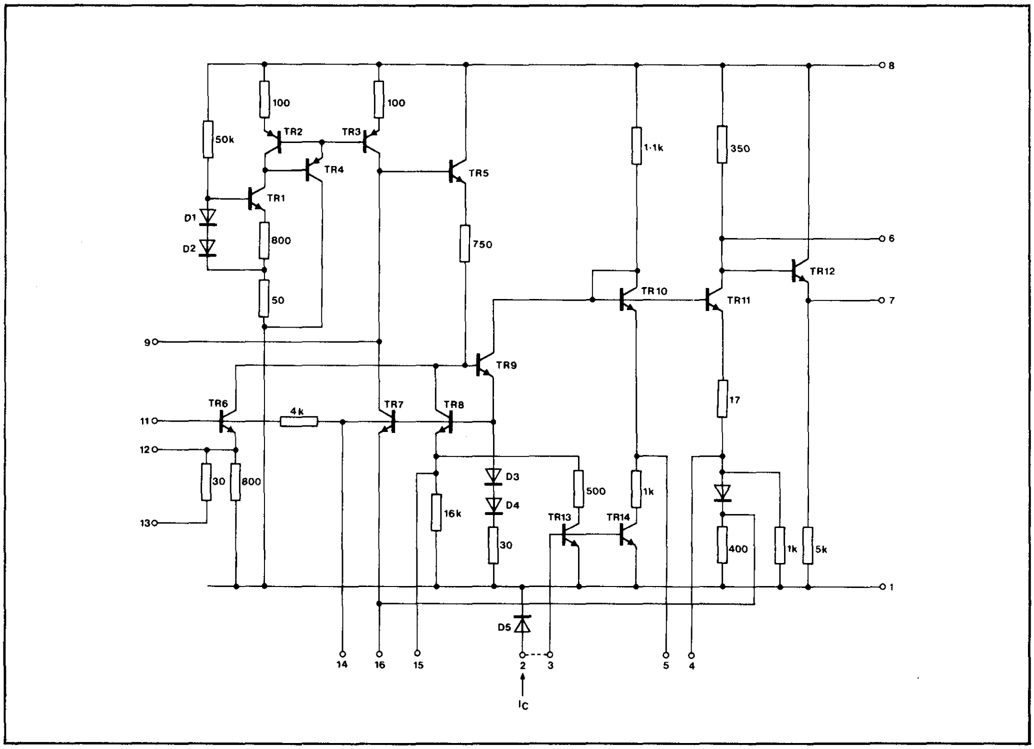


Fig. 10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

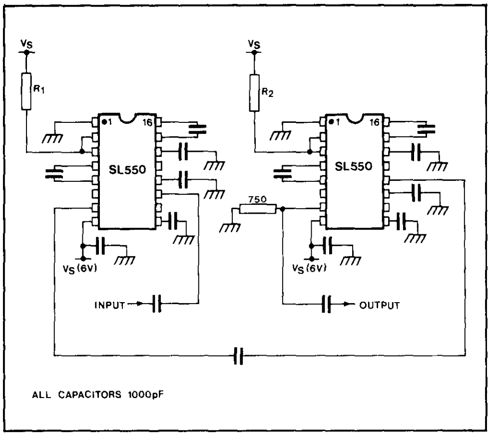


Fig. 11 A two-stage wide-band amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

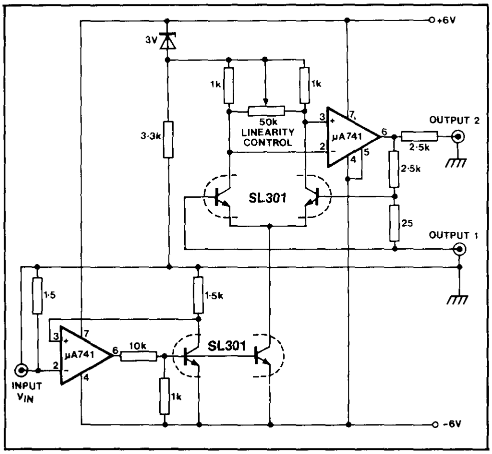


Fig. 12 Gain control linearising circuit

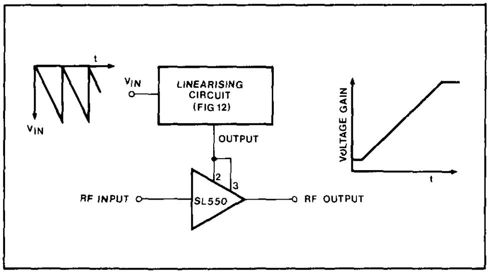


Fig. 13 Linear swept gain circuit

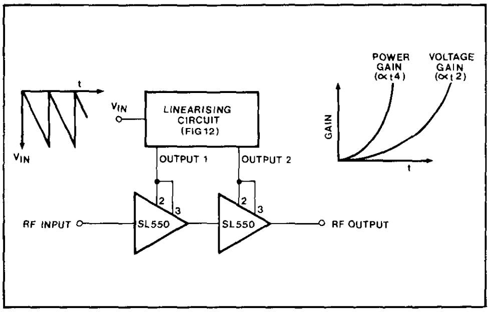
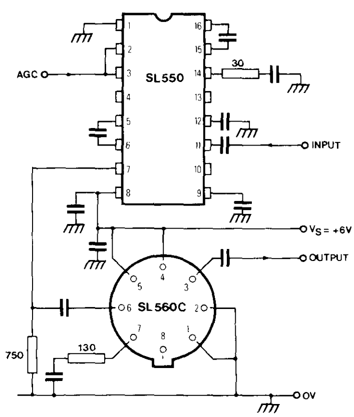


Fig. 14 Square law swept gain circuit



All Capacitors 10nF
Gain 46dB
Noise figure 2.0dB (RS = 200Ω)
Output power +5dBm (R1 = 50Ω)
Frequency response as SL550G
Dynamic range 70dB (1MHz bandwidth)

Fig. 15 Applications example of wide dynamic range: 50Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +150°C
Ambient operating temp.	—40°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V
Max. continuous AGC current pin 2	10mA
pin 3	1mA

PLESSEY
Semiconductors

SL560C

300 MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300 MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL 560C is a general-purpose low noise, high frequency gain block.

FEATURES
(Non-simultaneous)

- Gain up to 40 dB
- Noise Figure Less Than 2 dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range RF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

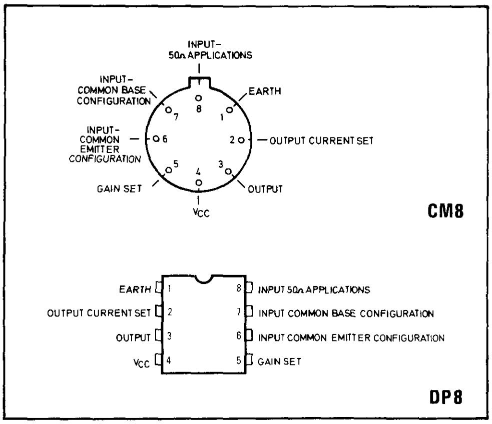


Fig. 1 Pin connections (viewed from beneath)

*ALSO AVAILABLE IN CHIP CARRIER

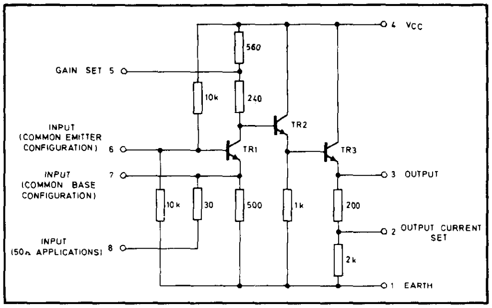


Fig. 2 SL560C circuit diagram

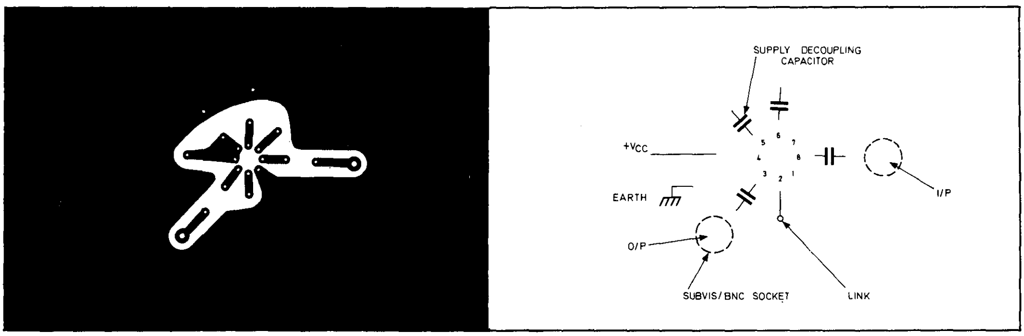


Fig. 3 PC layout for 50-Ω line driver (see Fig. 6)

*PLEASE ENQUIRE

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Frequency 30 MHz
Vcc 6V
$R_S = R_L = 50\Omega$
$T_A = 25°C$
Test Circuit: Fig. 6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10 MHz – 220 MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	Vcc = 6V } See Fig. 5
		+11		dBm	Vcc = 9V } See Fig. 5
Noise figure (common emitter)		1.8		dB	Rs = 200Ω
		3.5		dB	Rs = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17 ohms (for low noise operation) with a small physical size — giving a transition frequency, f_T, in excess of 1 GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2 dB noise figure (Rs = 200 Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75 MHz (see Figs. 8 and 9) or, using feedback, 14 dB with a bandwidth of 300 MHz (see Figs. 10 and 11).

Because the transistors used in the SL 560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is avaiable in the 'Broadband Amplifier Applications' booklet.

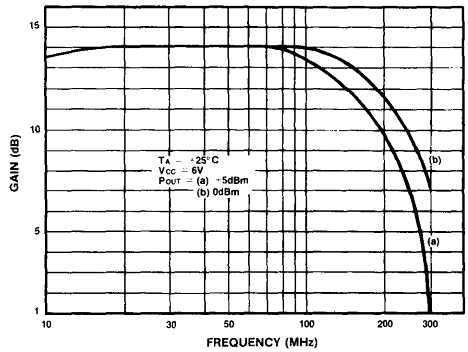


Fig. 4 Frequency response, small signal gain

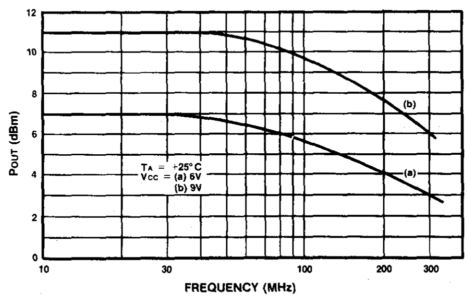
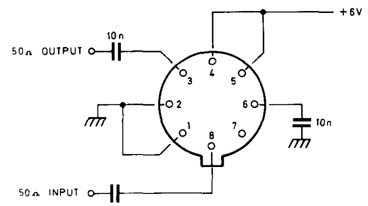


Fig. 5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression)

TYPICAL APPLICATIONS



Gain 14dB
Bandwidth 220 MHz (P_{out}=1mW, 50 Ω)
200 MHz (P_{out}=5mW, 50 Ω)
Input SWR 1.5:1

Fig. 6 50 Ω line driver. The response of this configuration is shown in Fig. 4.

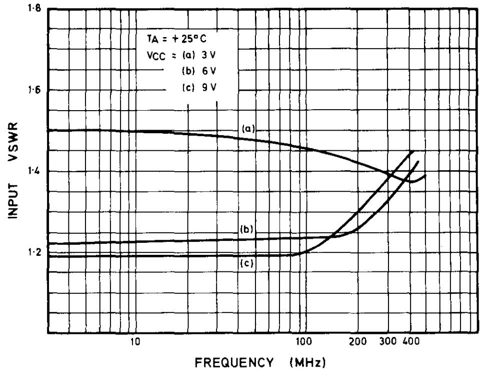
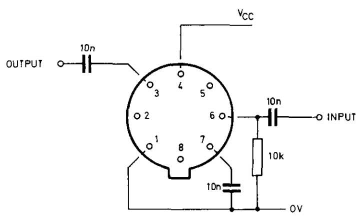


Fig. 7 Input standing wave ratio plot of circuit shown in Fig. 6



Voltage gain 32dB at 6V
35dB at 10V
Noise figure 1.8dB (RS=200 Ω)
Supply current 6mA at 6V
12mA at 10V
Bandwidth 75 MHz (see Fig. 9)

Fig. 8 Low noise preamplifier

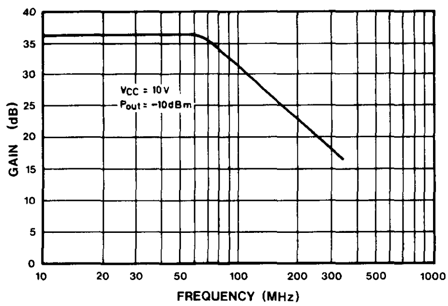
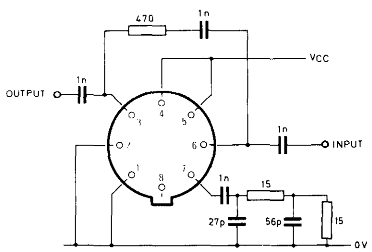


Fig. 9 Frequency response of circuit shown in Fig. 8



Gain 13dB at V_{CC}=9V
—1dB at 6 MHz and 300 MHz

Fig. 10 Wide bandwidth amplifier

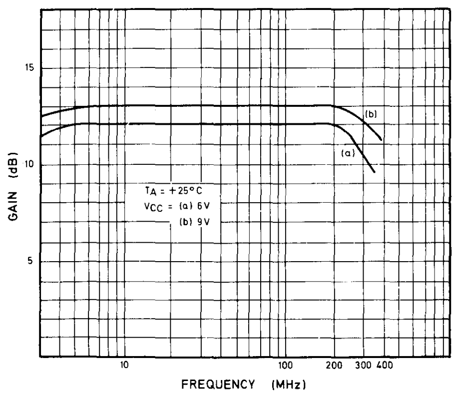


Fig. 11 Frequency response of circuit shown in Fig. 10

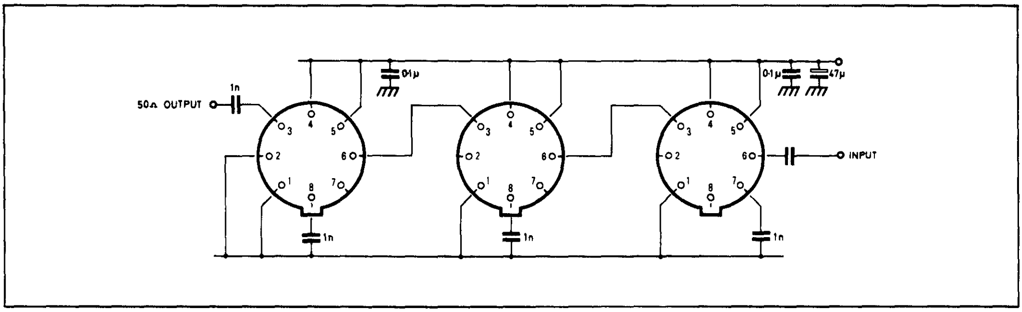


Fig. 12 Three-stage directly-coupled high gain low noise amplifier

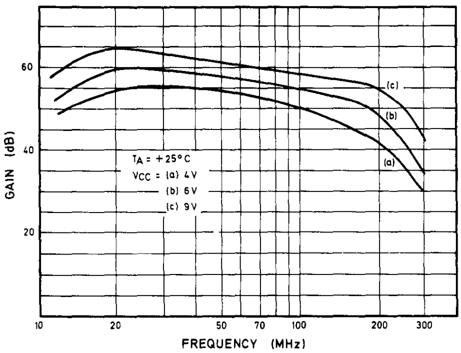
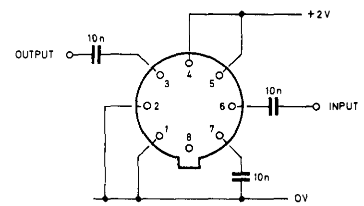


Fig. 13 Frequency response of circuit shown in Fig. 12



Gain 13dB
Power supply current 3mA
Bandwidth 125 MHz
Noise figure 2.5dB (RS=200 Ω)

Fig. 14 Low power consumption amplifier

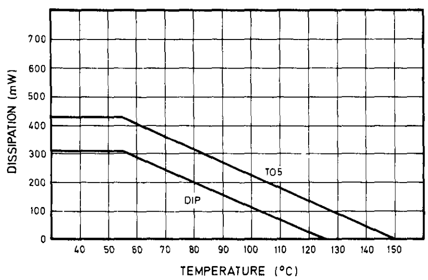


Fig. 15 Ambient operating temperature v. degrees centigrade

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	-55° C to 150° C (CM)
	-55° C to 125° C (DP)
Junction temperature	150° C (CM) 125° C (DP)
Thermal resistance	
Junction-case	60° C/W (CM)
Junction ambient	220° C/W (CM) 230° C/W (DP)
Maximum power dissipation	See Fig.15
Operating temperature range	−55°C to +125° C (CM) at 100mW
	−55°C to +100° C (DP) at 100mW

PLESSEY
Semiconductors

SL561B, SL561C

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/f noise. Noise performance is optimised for source impedances between 20Ω and 1kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.
The SL561B is only available in the TO-5 package.
The SL561C is only available in the Plastic package.

FEATURES

- High Gain — 60dB
- Low noise — 0.8nV/√Hz (Rs = 50Ω)
- Bandwidth — 6MHz
- Low Power Consumption — 10mW (V_{CC} = 5V)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

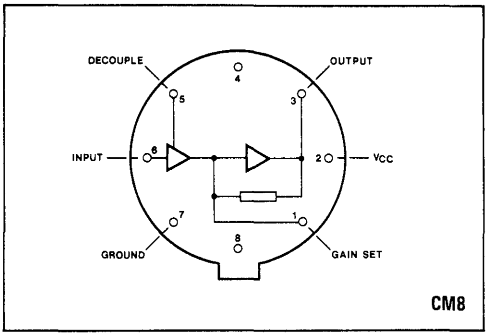


Fig.1 Pin connections (viewed from above) SL561B

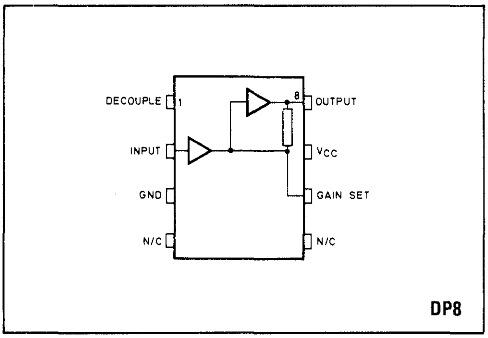


Fig.2 Pin connections (viewed from above) SL561C

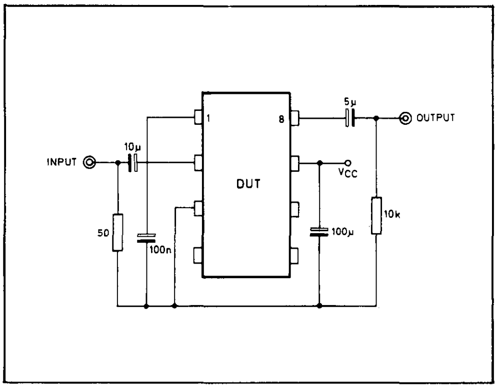


Fig.3 Test circuit

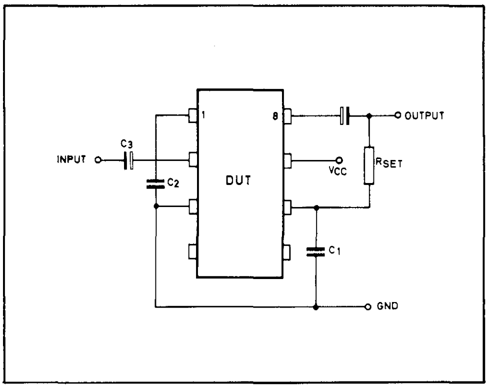


Fig.4 Typical application

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} 5V
Source impedance 50Ω
Load impedance 10kΩ
T_{amb} 25°C

SL561B

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 1 O/C
Equivalent input noise voltage		0.8	1.2	nV/√Hz	100Hz to 6MHz
Output voltage	2	3		V p-p	See note
Supply current		2.0	3.0	mA	
Output resistance		50		Ω	
Input resistance		3		kΩ	
Input capacitance		15		pF	
Upper cut-off frequency	5	6.5		MHz	V_{out} = 10mV p-p
		6.2		MHz	V_{out} = 1.5V p-p

SL561C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 O/C
Equivalent input noise voltage		0.8		nV/√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES (Pin numbers refer to DIL package)

Upper cut-off Frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig.5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/octave.

Low frequency response

The capacitors C_2 and C_3 (Fig.4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response either make C_2 less than 0.05 C_3 or make C_2 greater than 5 C_3.

Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV (see Fig.9).

Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7 From this the input noise voltage and current generators can be derived. They are:

$$e_n = 0.8\text{nV}/\sqrt{\text{Hz}}$$
$$i_n = 2.0\text{pA}/\sqrt{\text{Hz}}$$

Flicker or 1/f noise is not normally a problem, the knee frequency being typically below 100Hz.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature range	-55°C to +125°C
Operating temperature range DIL	-55°C to +100°C
Operating temperature range TO5	-55°C to +125°C

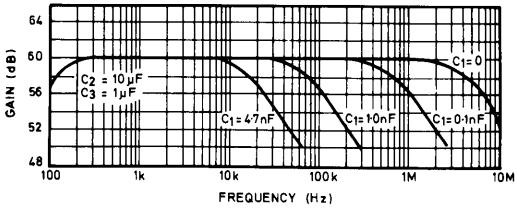


Fig.5 Gain v. frequency

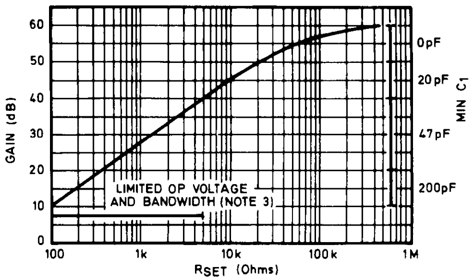


Fig.6 Gain v. Rset

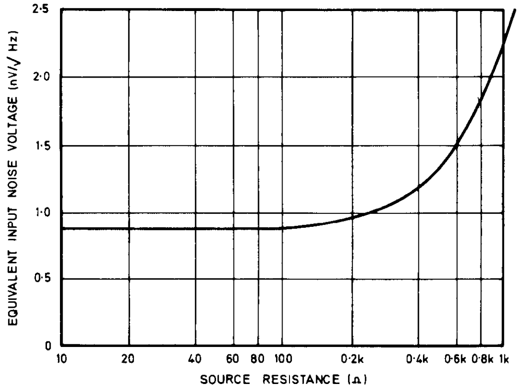


Fig.7 Noise v. source impedance

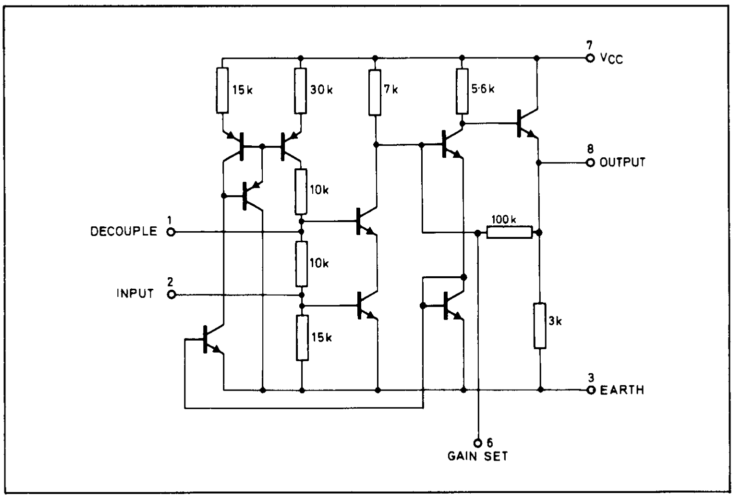


Fig.8 Circuit diagram

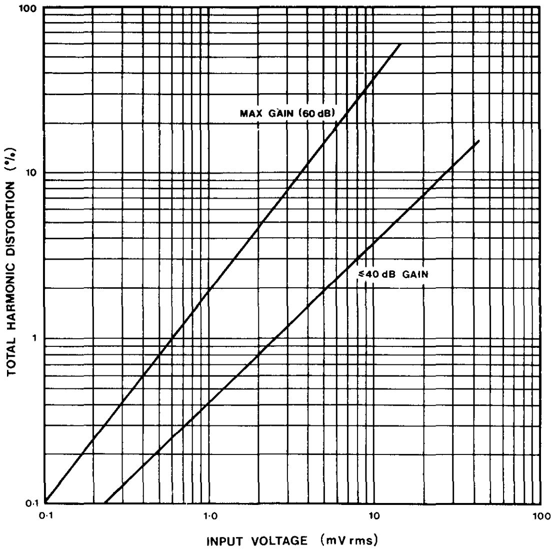


Fig.9 Harmonic distortion SL561 at 20kHz

PLESSEY Semiconductors

JUNE 1985
ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL562C

LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

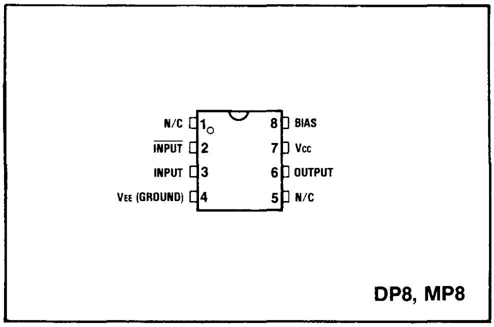


Fig.1 Pin connections - top view

FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- 741 Pin Compatibility
- Available In Small Outline

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Applications

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±10V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

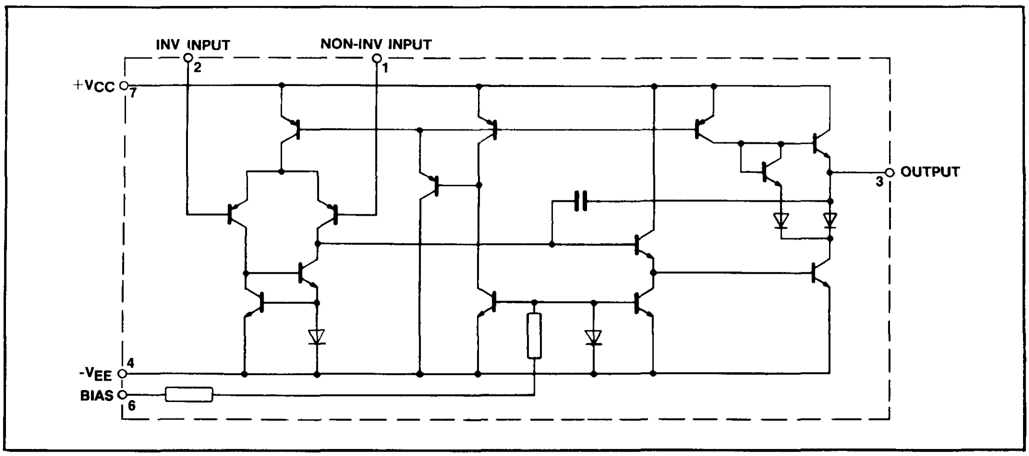


Fig.2 Circuit diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C
Operating mode A : Supply volts ±10V Bias set current 75μA
Operating mode B : Supply volts ±3.5V Bias set current 15μA
Operating mode C : Supply volts ±1.5V Bias set current 1μA

Characteristic	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S = 10kΩ
Input offset current		20	190			150			49	nA	
Input bias current		250	800			350			95	nA	
Input resistance	0.1	0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	μA	
Large signal voltage gain	74	95		74	90		74	90		dB	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	R_L = 4kΩ(A) R_L = 10kΩ(B) R_L = 4kΩ(C)
Supply voltage rejection ratio	74			85			85			dB	R_S = 10kΩ
Short circuit current	12		40				1	2.2		mA	T_{amb} = 0°C to +70°C
Gain bandwidth								50		kHz	Gain = 20dB
product		3.5			1					MHz	
Slew rate		1.5			0.5			0.02		V/μs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	f_O = 1kHz
Input noise current		1.6			1.6			1.0		pA√Hz	f = 1kHz

OPERATING NOTES

Bias set current

The amplifier is programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02V/μs
	(I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

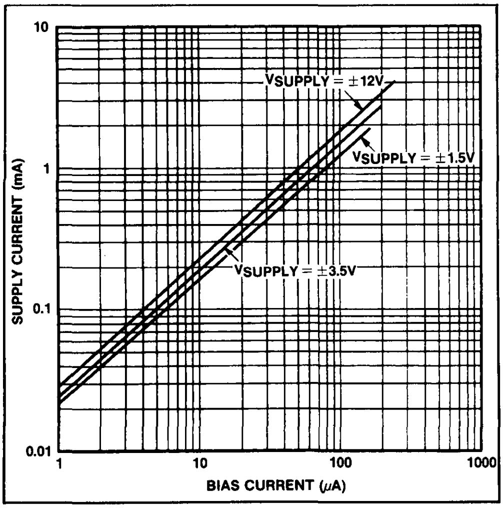


Fig.3 Supply current v. bias set current.

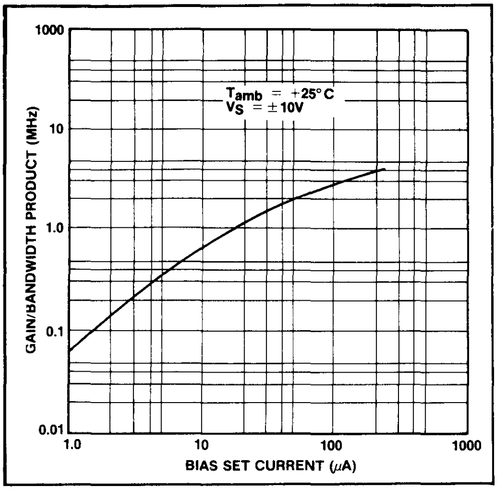


Fig.4 Gain bandwidth product v. ISET

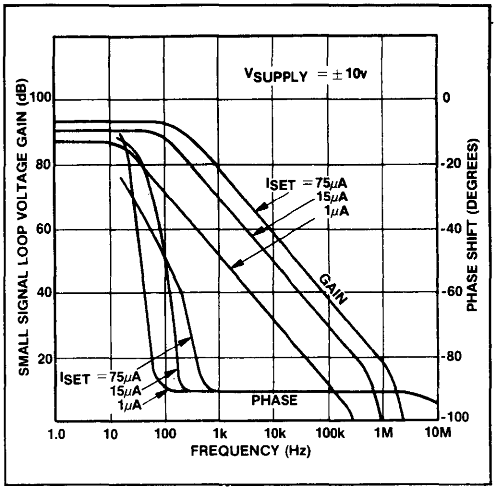


Fig. 5 Typical frequency response

APPLICATION EXAMPLE

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the Plessey low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

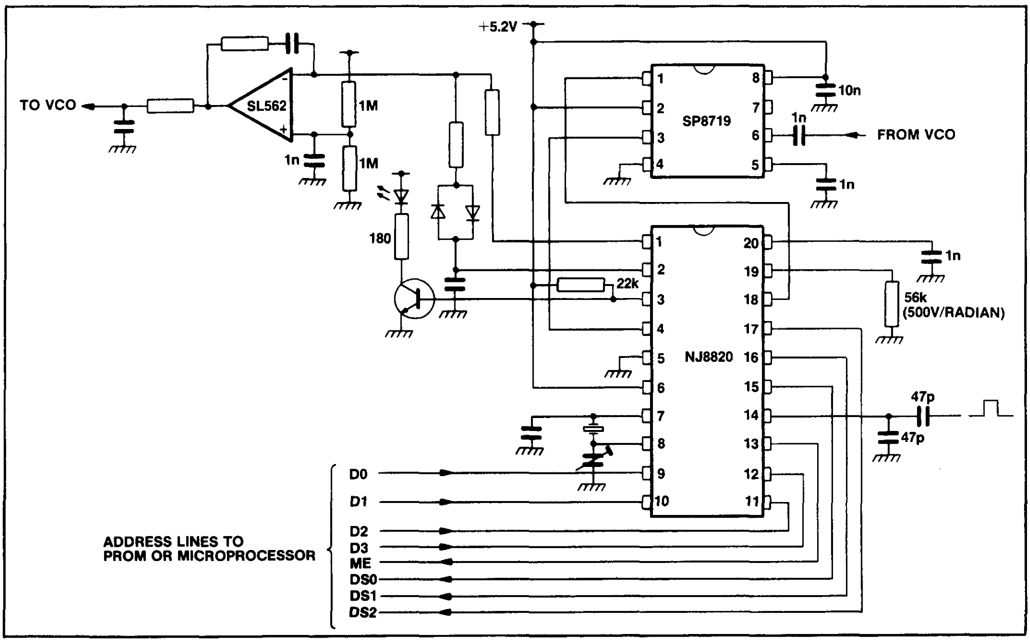


Fig.6 Application example.

PLESSEY Semiconductors

SL565C

1GHz WIDEBAND AMPLIFIER

The SL565 is a low cost wide bandwidth amplifier featuring differential inputs and outputs and useful performance to 1GHz. Typical applications are in wideband amplifiers, instrumentation, ECM and communications.

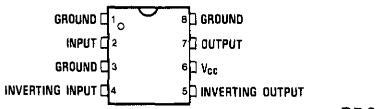


Fig.1 Pin connections - top view

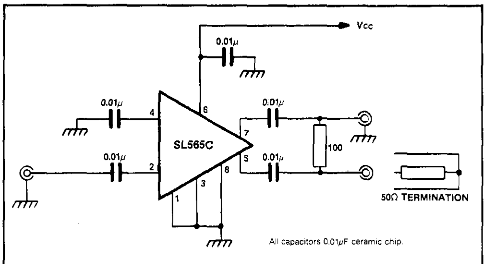


Fig.2 Test circuit

FEATURES

- Low Cost
- Wide Bandwidth: 1GHz
- High Gain: 22dB
- Differential Input and Output
- +5V Supply
- High Reverse Isolation

ABSOLUTE MAXIMUM RATINGS

Supply voltage, Vcc +8V
Storage temperature -55°C to +125°C
Operating temperature -30°C to +85°C
Chip temperature +150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

V_{CC} = 5.0V T_{amb} = +25°C. Test circuit Fig.2 except for differential gain measurements.

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply voltage	4.75	5.0	5.5	V	
Supply current		50	70	mA	
Differential gain S_{21}		16		dB	10-900MHz
		21		dB	1GHz
		16		dB	1.3GHz
Single ended gain	8	10	12		100MHz
	13	15	17		500MHz
	8	10	12		1GHz
1dB gain compression		-19		dBm	Input power at 500MHz
Noise figure		13		dB	50Ω source
3rd order input intercept point		-3.5		dBm	50MHz
		-7		dBm	200MHz
		-9.5		dBm	500MHz
2nd order input intercept point		+3.0		dBm	500 and 400MHz inputs
Reverse isolation pins 7 to 4		70		dB	f = 50MHz
		60		dB	f = 50-100MHz
		20		dB	f = 500MHz
		20		dB	f = 1GHz
Reverse isolation pins 5 to 4		75		dB	f = 100MHz
		30		dB	f = 1GHz
Maximum output		600		mV p-p	f < 500MHz
		300		mV p-p	f = 500MHz to 1GHz
Maximum output power		-3		dBm	1GHz
for 1dB compression		-2		dBm	500MHz

OPERATING NOTES

The SL565 is a general purpose wideband gain block, suitable for many applications. The frequency response and input impedance plots are shown in Figs. 3 and 4 respectively.

Like all wideband high frequency circuits, the SL565 should be used with short leads to its associated components, and a ground plane printed circuit board layout is recommended. There are advantages in using the top surface of the PCB as the ground plane with cage jacks e.g. Cambion 450-3750-01-06-00 or similar sockets for each device pin, as then chip capacitors can be installed with minimum lead lengths on top of the board. Resistors should be miniature carbon composition types (metal oxide and carbon film types often have an appreciable parasitic inductance).

The high reverse isolation makes the SL565 ideal for driving High Speed Divider integrated circuits in both frequency counters and synthesisers, and Fig. 5 shows a typical application in a 100MHz to 1000MHz ÷10 prescaler for a frequency counter. This prescaler operates with inputs as low as 70mV rms over the whole frequency range of the device.

Other applications for the SL565 include oscillators using SAW devices as frequency determining elements, where the wide bandwidth of the SL565 enables high frequency oscillators to be produced at minimum cost.

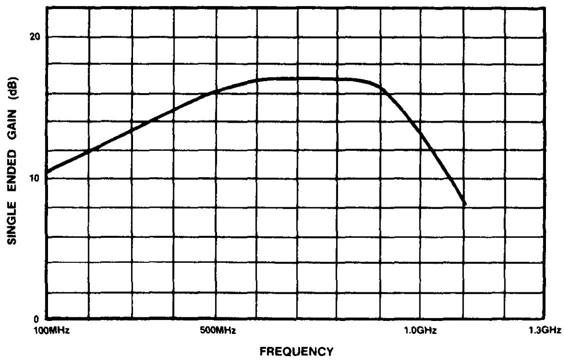


Fig.3 Typical frequency response, SL565C

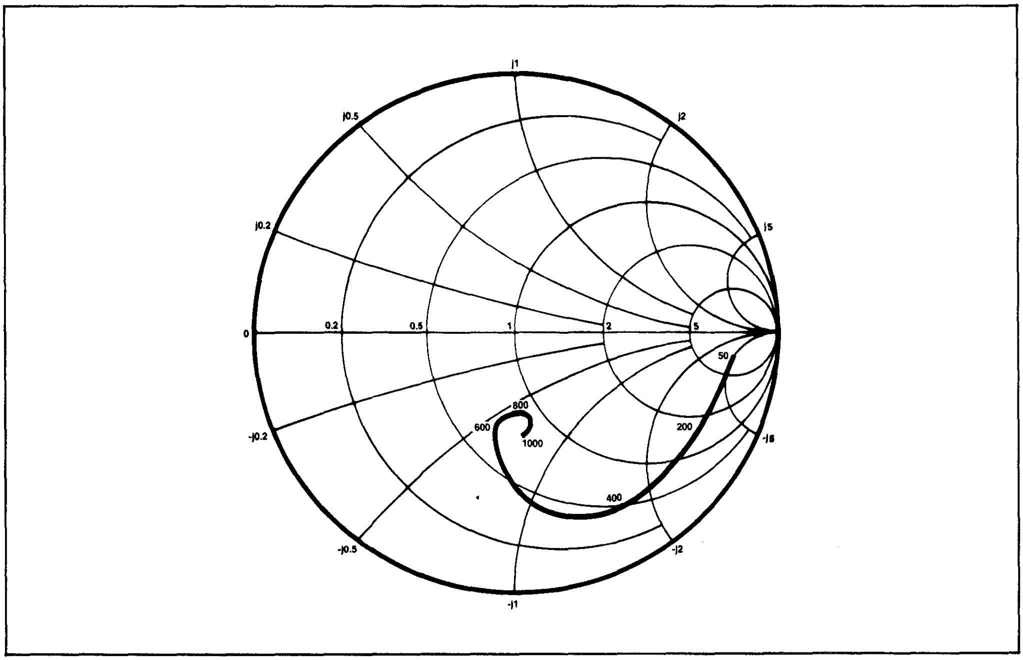


Fig.4 Single-ended input impedance of SL565C, normalised to 50Ω. V_{CC} = 5V, T_{amb} = 25°C, load = 50Ω, frequencies in MHz.

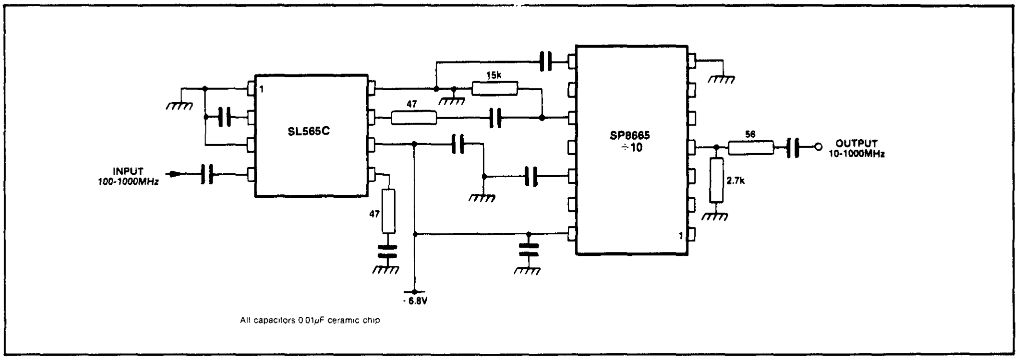


Fig.5 1GHz prescaler

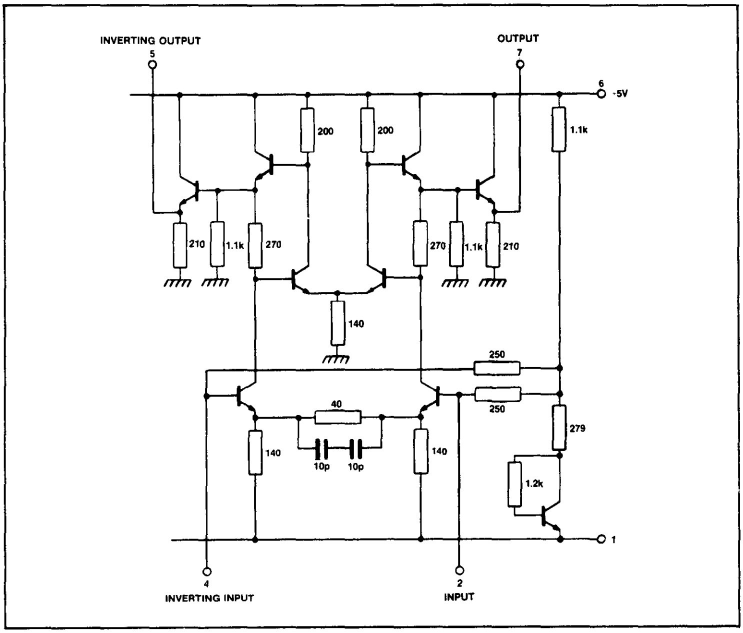


Fig.6 SL565C circuit diagram

PLESSEY
Semiconductors

SL952

1GHz LIMITING WIDEBAND AMPLIFIER

The SL952 amplifier has been designed to drive prescalers. It features a differential output to reduce local oscillator radiation, and a differential input.

The device operates from a single 5V supply with a minimal number of external components and is encapsulated in a 14 lead DIL package. Typical applications are in instrumentation and communications.

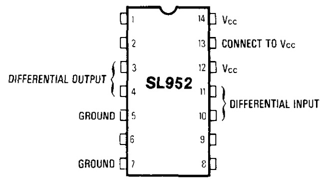


Fig. 1 Pin connections

FEATURES

- Low Cost
- High Gain
- Minimal External Component Count
- Good Limiting Characteristics
- 1GHz Response
- 5V Supply

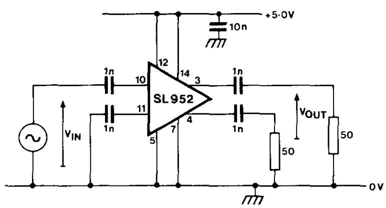


Fig. 2 Test circuit

ABSOLUTE MAXIMUM RATINGS

Vcc +10V
Ambient temperature 0°C to +65°C
Storage temperature −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5.0V
T_{AMB} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.00	5.50	V	
Supply current		70	90	mA	
DC output level		3.2		V	
Output offset		100	600	mV	
Maximum differential output swing	600			mVp-p	950MHz
Differential voltage gain	30	35		dB	100MHz
Differential voltage gain	30	35		dB	500MHz
Differential voltage gain	15	26		dB	950MHz

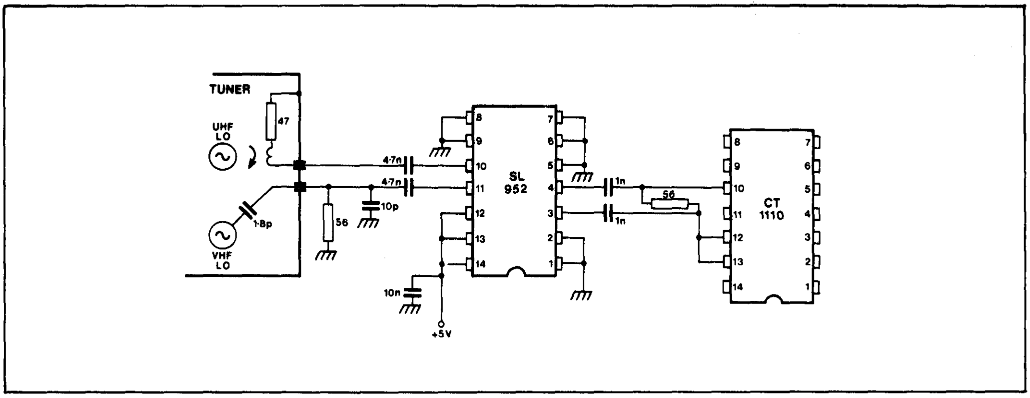


Fig. 3 Typical application for TV frequency synthesis

PLESSEY
Semiconductors

SL610C, SL611C & SL612C

RF/IF AMPLIFIERS

The SL610C, SL611C and SL612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15 MHz to 120 MHz according to type.

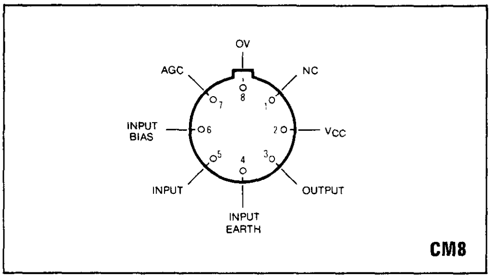


Fig. 1 Pin connections (bottom view)

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

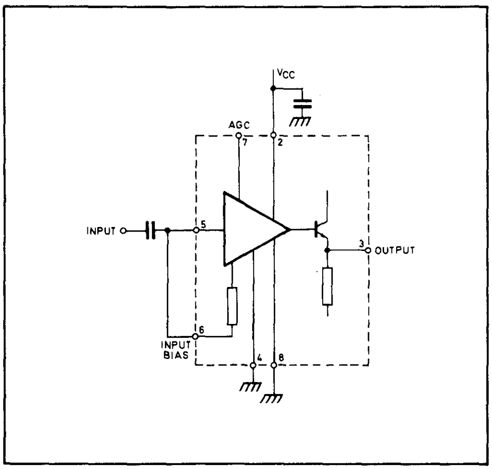


Fig. 2 Block diagram

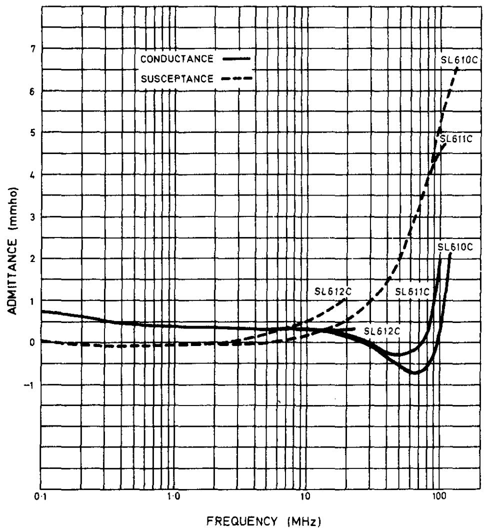


Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL610C 30MHz
SL611C 30MHz
SL612C 1.75MHz

Characteristic	Circuit	Value Min.	Typ.	Max.	Units	Conditions
Supply current	SL610C		15	20	mA	
	SL611C		15	20	mA	No signal, pin 3 open circuit
	SL612C		3.3	5	mA	
Voltage gain	SL610C	18	20	22	dB	Rs = 50Ω
	SL611C	24	26	28	dB	RL = 22°C
	SL612C	32	34	36	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL610C	85	120		MHz	
	SL611C	50	80		MHz	
	SL612C	10	15		MHz	
Max.output signal (max.AGC)			1.0		V rms	RL = 150Ω (SL610C/611C)
						RL = 1.2kΩ (SL612C)
Max.input signal (max.AGC)			250		mV rms	
AGC range	SL610C	40	50		dB	
	SL611C	40	50		dB	Pin 7 0V to 5.1V
	SL612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL610C, SL611C only) and is shown in Fig. 3. If the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

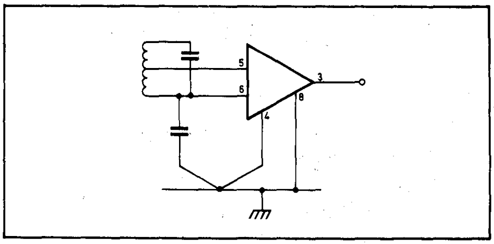


Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

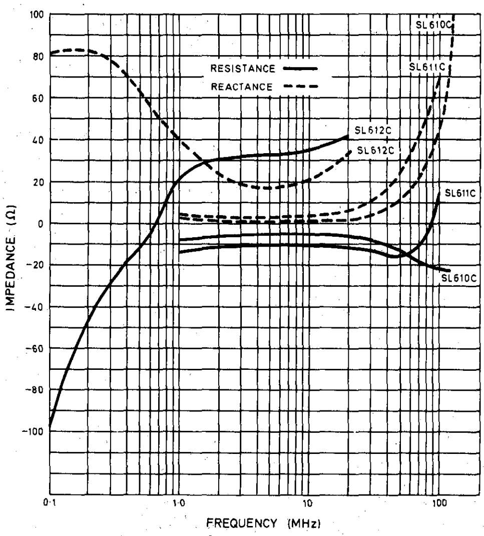


Fig. 5 Typical output impedance with s/c input (G22)

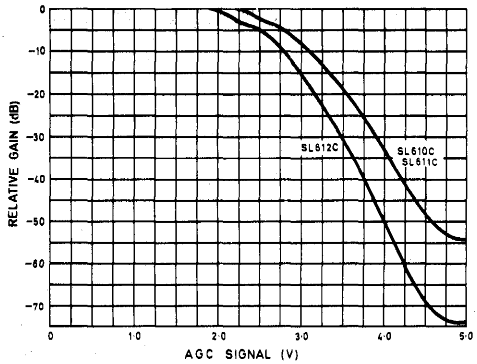


Fig. 6 AGC characteristics (typical)

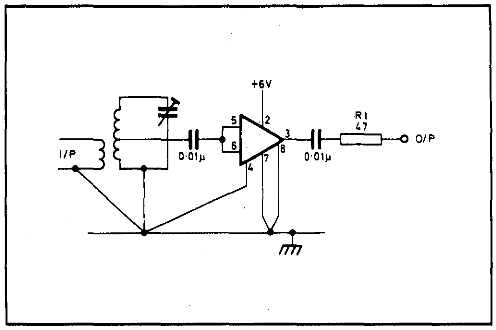


Fig. 7 RF preamplifier

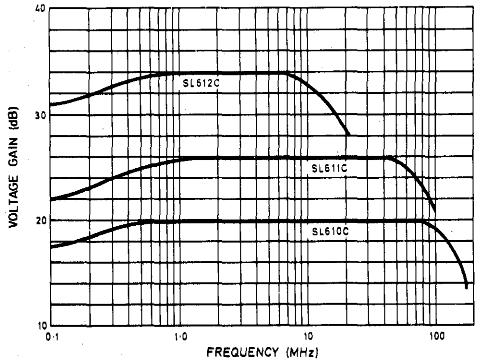


Fig. 8 Typical voltage gain (R_S=50 Ω)

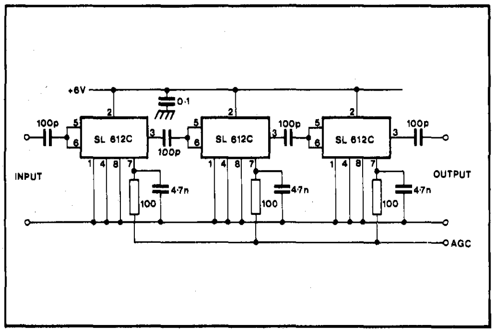


Fig. 9 IF amplifier using SL612

PLESSEY
Semiconductors

SL621C

AGC GENERATOR

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

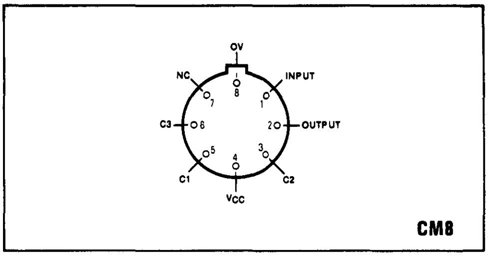


Fig. 1 Pin connections (bottom view)

FEATURES

- All Time Constants Set Externally
- Easy Interfacing
- Compatible with SL610/611/612

APPLICATIONS

- SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply voltage: 6V
- Supply current: 3mA

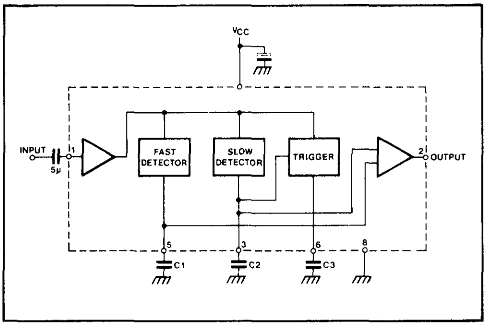


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature: −30°C to +85°C
Test frequency: 1kHz
Test circuit as Fig. 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.1	4.3	mA	No signal
Cut-off frequency (−3dB)		6		kHz	
Input for 2.2V DC output	3	7	11	mVrms	
Input for 4.6V DC output	9	11	16	mVrms	
Maximum output voltage	5.1			V	
AC ripple on output		12	20	mV pk-pk	1kHz, output open circuit
Input resistance	350	500	700	Ω	
Output resistance		70	230	Ω	
'Fast' rise time t_1		20	55	ms	0 to 50% full output
'Fast' decay time t_2	150	200	330	ms	100% to 36% full output
'Slow' rise time t_3	150	200	300	ms	Time to output transistion point
Hold collapse time t_4	65	100	150	ms	90% to 10% full output
Hold time t_5	0.75	1.0	1.25	s	

APPLICATION NOTES

The SL621C consists of an input AF amplifier coupled to a DC output amplifier by means of two detectors having short and long rise and fall times respectively. The time constants of these detectors are set externally by capacitors on pins 5 (C_1) and 3 (C_2).

The detected audio signal at the input will rapidly establish an AGC level via the 'fast' detector time in t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is more sensitive.

Input signals greater than approximately 4mV rms will actuate a trigger circuit whose output pulses provide a discharge current for C_2.

By this means the voltage on C_2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C_2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C_3. When the trigger pulses cease, C_3 discharges and after t_5 C_2 is discharged rapidly (in time t_4) and so full receiver gain is restored. The hold time, t_5 is approximately one second with $C_3 = 100\mu F$. If signals reappear during t_5, then C_3 will recharge and normal operation will continue. The C_3 recharge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for $C_1 = 50\mu F$ and $C_2 = C_3 = 100\mu F$. These time constants may be altered by varying the appropriate capacitors. C_1 controls t_1, t_2; C_2 controls t_3, t_4; C_3 controls t_5.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500µF so that it is not affected by the current surge resulting from a sudden input on pin 1.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output should not exceed 15000pF or the impulse suppression will suffer.

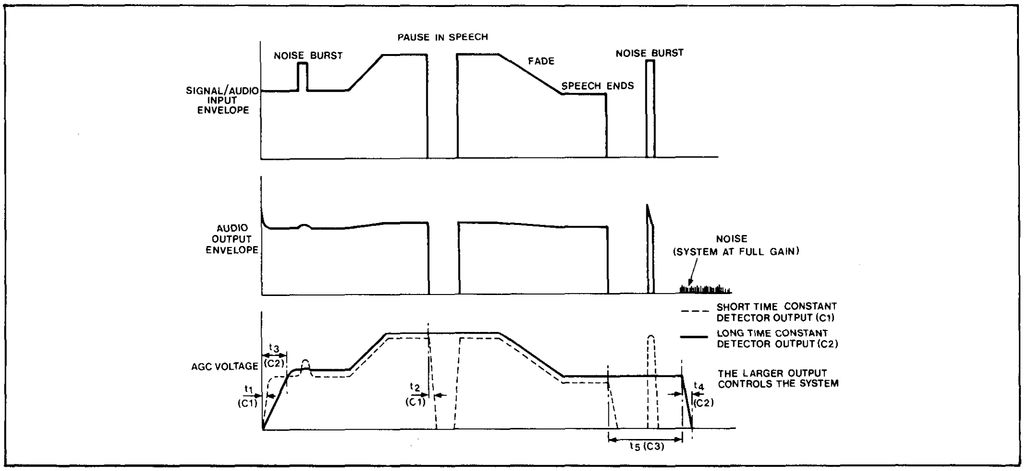


Fig. 3 Dynamic response of a system controlled by SL621C AGC generator

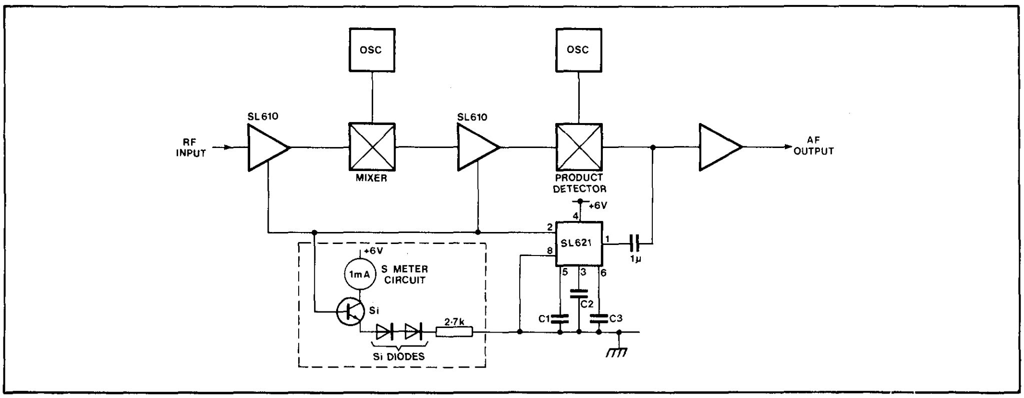


Fig. 4 SL621C used to control SSB receiver

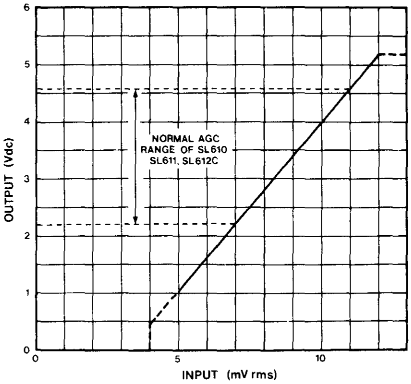


Fig. 5 Transfer characteristic of SL621C (typical)

Under some conditions,overload of the AGC output may occur in a receiver. Possible solutions are shown in Figs.6 and 7.

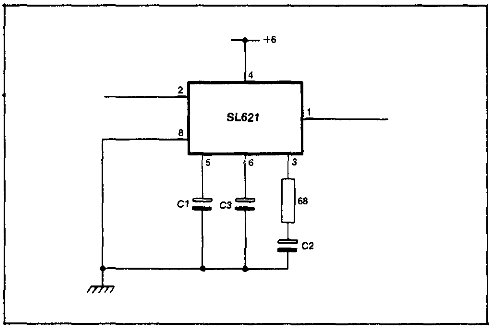


Fig.6

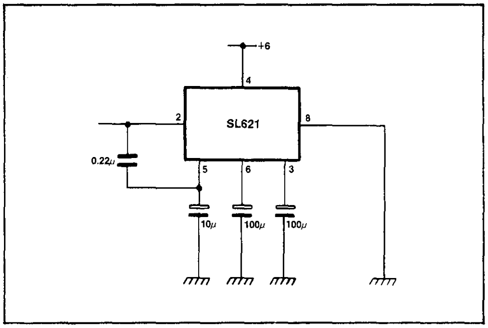


Fig.7

PLESSEY
Semiconductors

SL623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5dB range for a 90dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies.

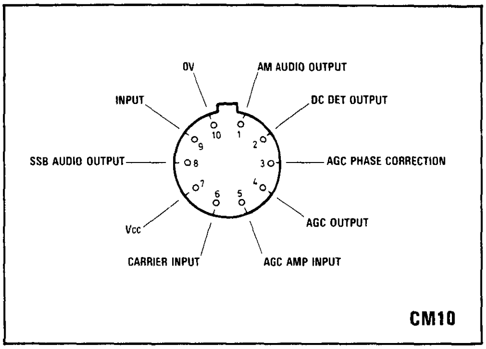


Fig. 1 Pin connections (bottom view)

FEATURES

- Negligible Distortion
- Easy Interfacing
- Fast Response Time

APPLICATIONS

- AM SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Maximum Frequency: 30MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

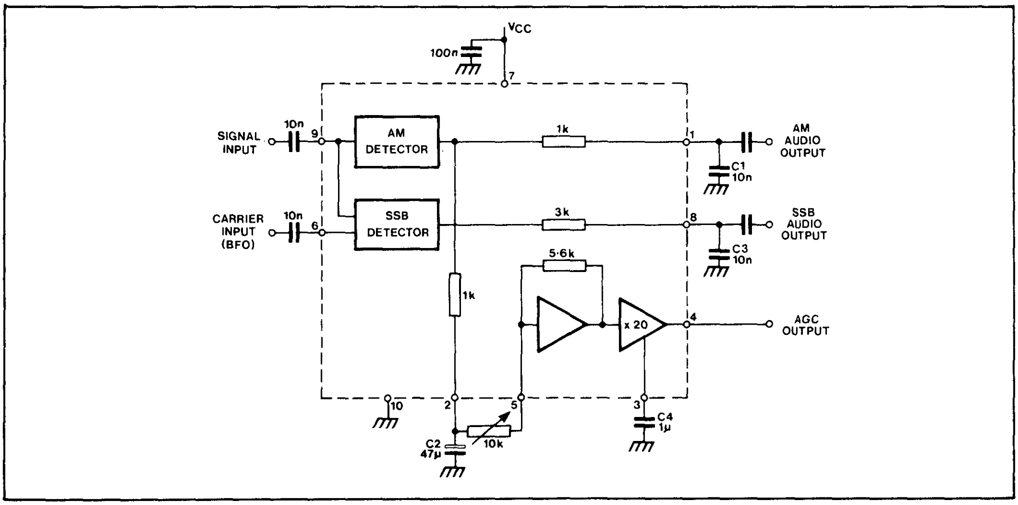


Fig. 2 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature = −30°C to +85°C
Test circuit as Fig. 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11	mA	No signal, Pin 4 open
Input impedance		800		Ω	Pins 6, 9
SSB audio output	22	30	47	mVrms	Signal input 20mV rms @ 1.748 MHz. Ref. signal input 100mV @ 1.750 MHz
AM audio output	43	55	67	mV rms	Signal input 125mV rms @ 1.75MHz modulated to 80% at 1kHz
AGC range (Note 1)			6	dB	Initial signal input 125mV rms at 1.75MHz modulated to 80% at 1kHz. Output set to 2.0V with 10kΩ potentiometer between Pins 2 & 5.

NOTES
1. The AGC range is the change in input level to increase AGC output voltage from 2.0V to 4.6V

APPLICATION NOTES

AGC Generator

Pin 3, the AGC amplifier phase correction point should be decoupled to ground by a 1 microfarad capacitor (C4), keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

The AGC output (Pin 4) will drive at least two SL610/11/12 amplifiers. The SL623AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623 will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to Pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs – no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

PLESSEY
Semiconductors

SL640C & SL641C

DOUBLE BALANCED MODULATORS

The SL640C and SL641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL641 has a single output designed as a current drive to a tuned circuit.

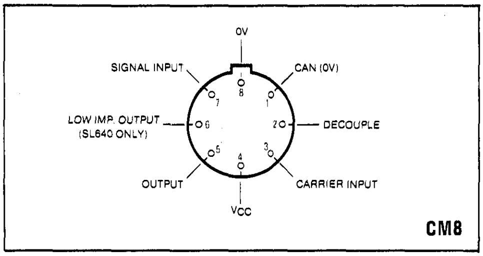


Fig. 1 Pin connections (bottom view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

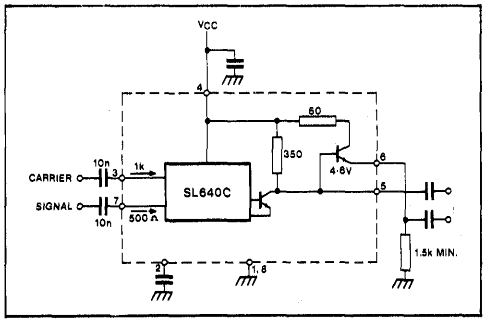


Fig. 2 Block diagram (SL640C)

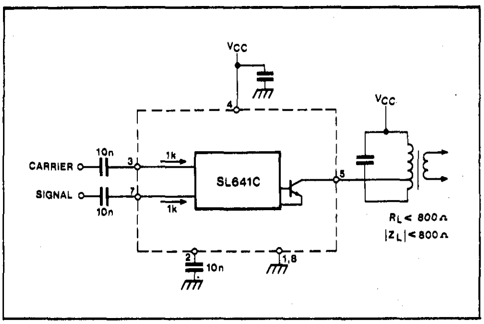


Fig. 3 Block diagram (SL641C)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current	SL640C		12	17	mA	
	SL641C		10	13	mA	
Conversion gain	SL640C	−3	0	+3	dB	
Conversion transconductance	SL641C	1.75	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL640C		500		Ω	
	SL641C		1		kΩ	
Maximum input voltage	SL640C		210		mV rms	
	SL641C		250		mV rms	
Signal leak	SL640C		−30	−18	dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL640C		−30	−20	dB	
Signal leak	SL641C		−18	−12	dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL640C		−45	−35	dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL641C		−45	−30	dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 3.75MHz

APPLICATION NOTES

The SL640C and SL641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

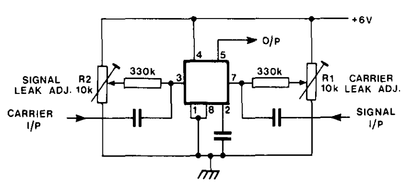


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

PLESSEY
Semiconductors

SL1521A & C

300MHz WIDEBAND AMPLIFIERS

The SL1521A and C are wideband amplifiers intended for use in successive detection logarithmic IF strips operating at centre frequencies of up to 200MHz. It is a plug in replacement for the SL521 series of RF amplifiers. The mid-band voltage gain of the SL1521 is typically 12dB. The SL1521A and C differ mainly in the tolerance of voltage gain.

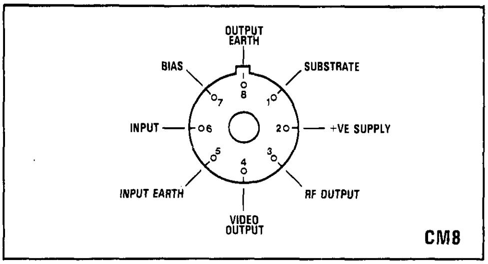


Fig.1 Pin connections

APPLICATIONS

- Radar IF Strips
- Wideband Amplification

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Operating temperature	−55°C to +125°C
Maximum chip operating temperature	150°C
Chip to ambient thermal resistance	250°C/W

Test circuits: see Fig.8

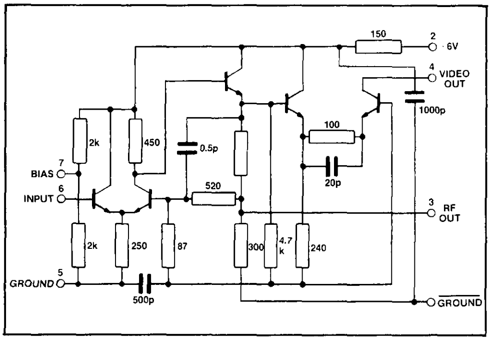


Fig.2 Circuit diagram

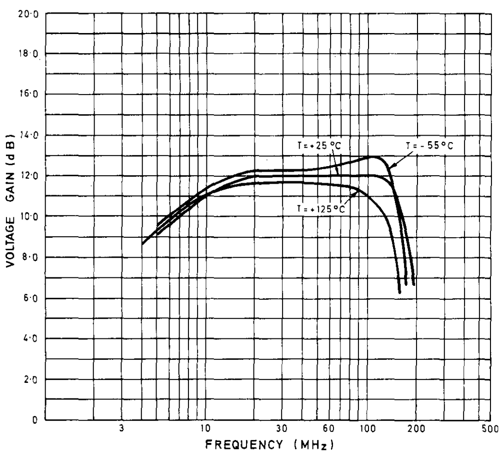


Fig.3 Voltage gain v. frequency

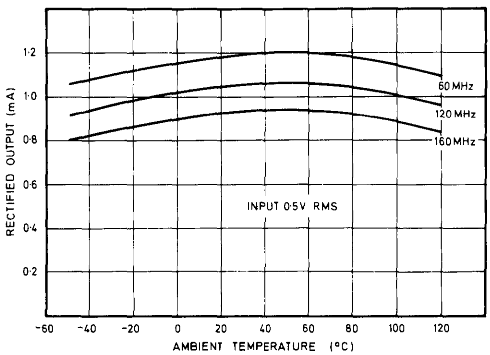


Fig.4 Maximum rectified output current v. temperature

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +5.2V
DC connection between input and bias pins.

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain, f =120MHz	SL1521A	11.5		12.5	dB	3mV rms input
	SL1521C	10.8		13.1	dB	50 ohms source
Voltage gain, f =160MHz	SL1521A	11.2		12.8	dB	8pF load + 500Ω
	SL1521C	10.6		13.4	dB	
Upper cut-off frequency	SL1521A	315	350		MHz	50 ohms source
	SL1521C	300	350		MHz	
Lower cut-off frequency	All types		6	10	MHz	50 ohms source
Propagation delay	All types		0.6		ns	
						f = 120MHz
Maximum rectified video output	SL1521A	0.95		1.05	mA	0.5V rms input
current	SL1521C	0.90		1.20	mA	8pF load, 500 ohms in parallel
Variation of gain with supply voltage	All types		1.0		dB/V	
Variation of maximum rectified output current with supply voltage	All types		30		%/V	
Maximum input signal before overload	All types		1.5		V rms	See note below
Noise figure			3	4.5	dB	f = 120MHz, source
Supply current	All types	10.0	15.0	20.0	mA	resistance optimised
Maximum RF output voltage	All types	1.0			V p-p	f = 120MHz

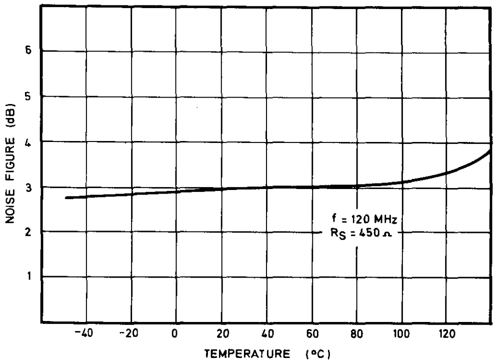


Fig.5 Typical noise figure v. temperature

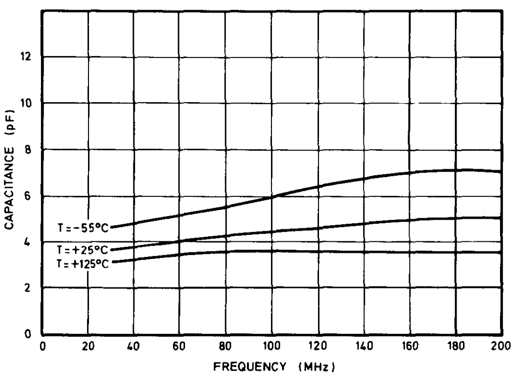


Fig.6 Input admittance with open-circuit output

Operating Notes

The amplifiers are intended for use directly coupled, as shown in Fig.7.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

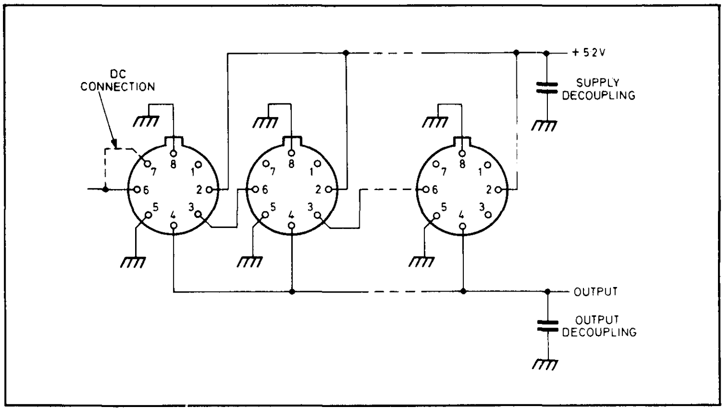


Fig.7 Direct coupled amplifier

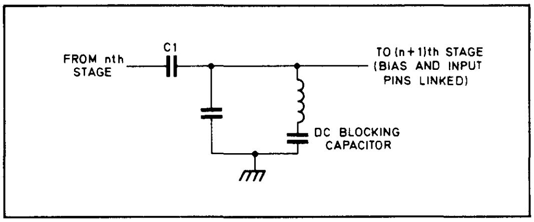


Fig.8 Suitable interstage tuned circuit

PLESSEY
Semiconductors

SL1523C

300MHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL1523C consists of two SL1521's in series, and is intended to reduce the package count and improve the packing density in logarithmic strips at frequencies up to 200 MHz.

Absolute Maximum Ratings
(Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	—55°C to +175°C
Operating temperature	—55°C to +125°C
Chip operating temperature:	150°C
Chip-to-ambient thermal resistance	300°C/W
Chip-to-case thermal resistance	95° C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+ 9V

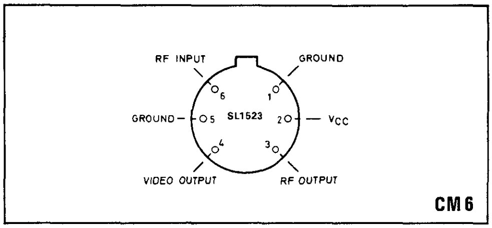


Fig. 1 Pin connections (bottom view)

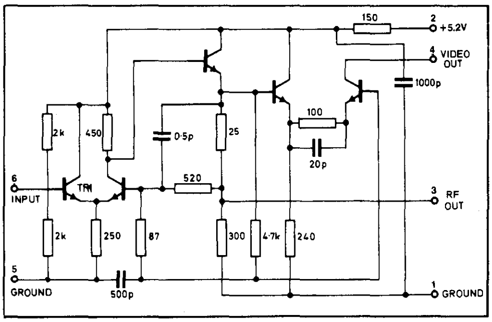


Fig. 2 SL1523 circuit diagram (each amp)

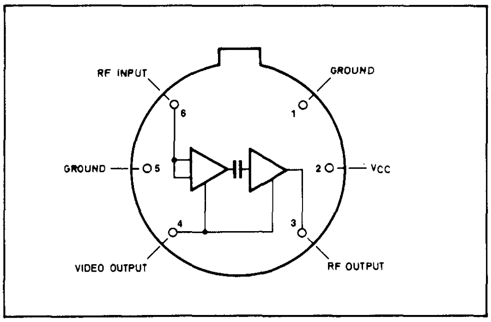


Fig. 3 SL1523 block diagram

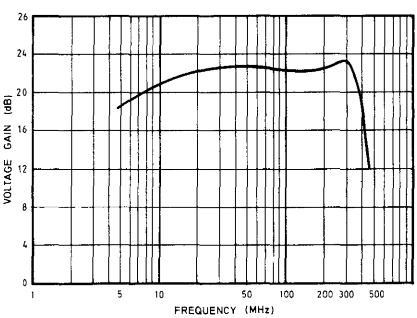


Fig. 4 Voltage gain v. frequency

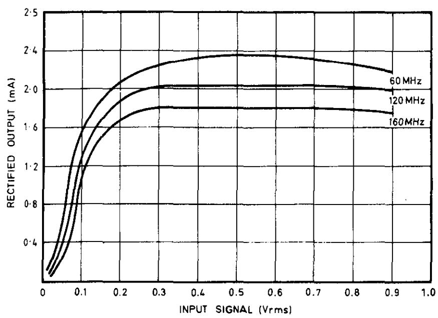


Fig. 5 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Temperature = 22°C ± 2°C
Supply voltage = + 5.2V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	21		27	dB	f = 120MHz, 3mV rms input, 50Ω source 4pF load + 50Ω
Voltage gain	20		27	dB	f = 160MHz, 3mV rms input, 50Ω source 4pF load + 500Ω
Upper cut-off frequency	300	325		MHz	50Ω source
Lower cut-off frequency		8	10	MHz	50Ω source
Propagation delay		1.2		ns	
Maximum rectified video output current	1.6		2.0	mA	f = 120MHz, 0.5V rms input, 4pF load
Variation of gain with supply voltage		2.0		dB/V	
Variation of maximum rectified output current with supply voltage		30		%/V	
Maximum input signal before overload		1.5		V rms	See note below
Noise figure		3		dB	f = 120MHz, source resistance optimised
Supply current	20	30	40	mA	
Maximum RF output voltage	1.0			V p-p	f = 120MHz

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction of TR1 on peaks.

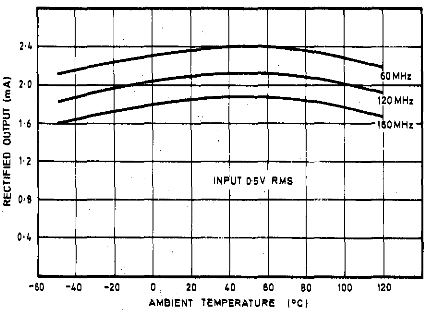


Fig. 6 Maximum rectified output current v. temperature

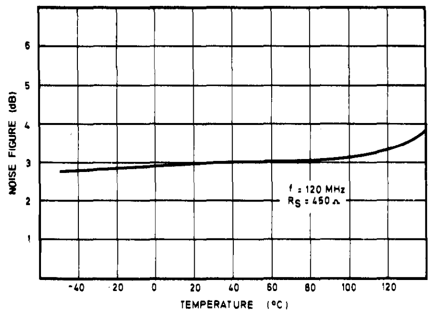


Fig. 7 Typical noise figure v. temperature

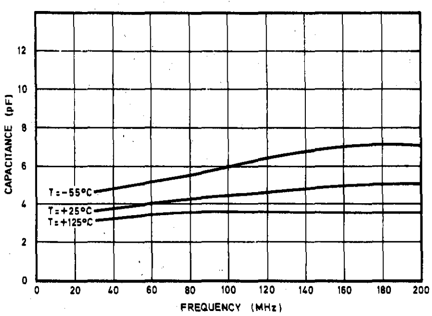


Fig. 8 Input admittance with open circuit output

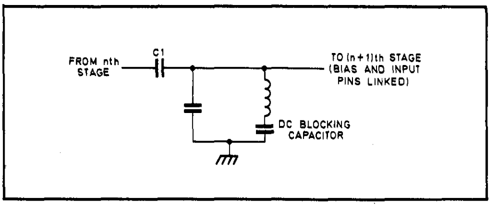


Fig. 9 Suitable interstage tuned circuit

PLESSEY
Semiconductors

SL1613C

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613C is a bipolar monolithic integrated circuit wideband amplifier intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL1613C is typically 12dB.

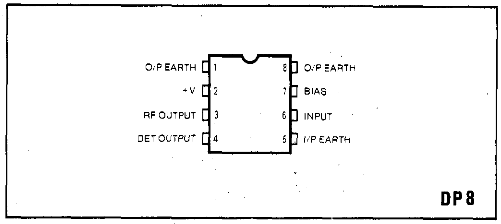


Fig. 1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +125°C
Operating temperature range	−30°C to +85°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Field Strength Meters

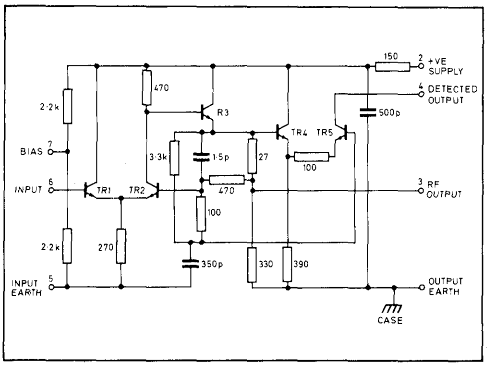


Fig. 2 Circuit diagram

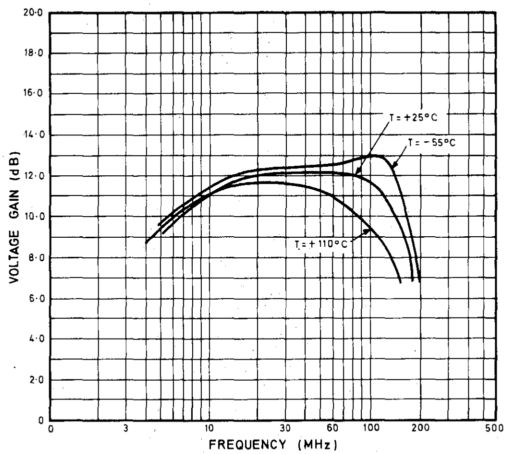


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	f=30MHz, R_s=10Ω, C_L=8pF
Upper cut-off frequency (Fig. 3)		150		MHz	R_S=10Ω, C_L=8pF
Lower cut-off frequency (Fig. 3)		5		MHz	R_S=10Ω, C_L=8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.8	1	1.3	mA	f=60MHz, V_{in}=500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		% / V	
Maximum input signal before overload		1.9		V rms	See Note 1
Noise figure (Fig. 6)		4.5		dB	f=60MHz, R_s=450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15	20	mA	

Note 1. Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction of TR1 on peak.

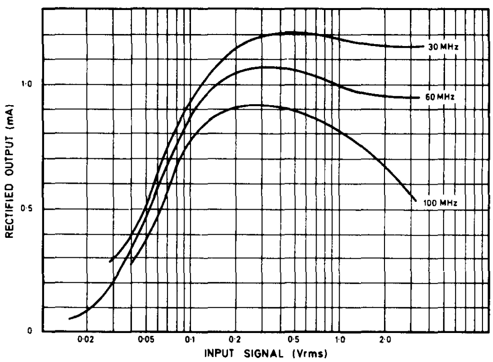


Fig. 4 Rectified output current v. input signal

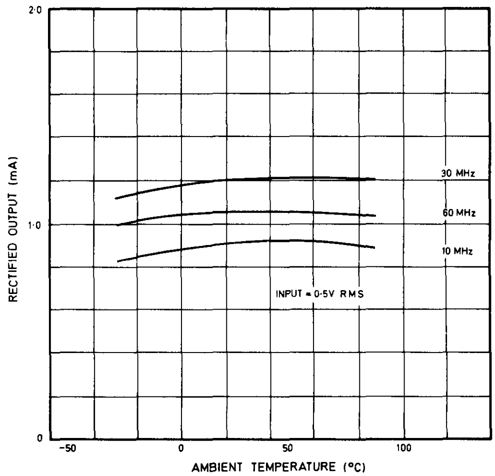


Fig. 5 Maximum rectified output current v. temperature

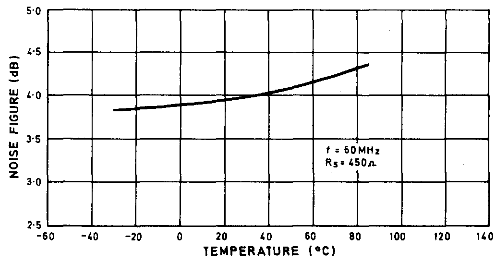


Fig. 6 Typical noise figure v. temperature

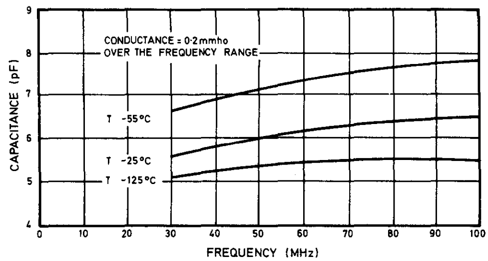


Fig. 7 Input admittance with open circuit output

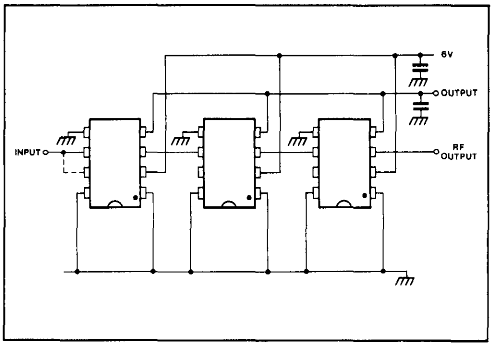


Fig. 8 Direct coupled amplifiers

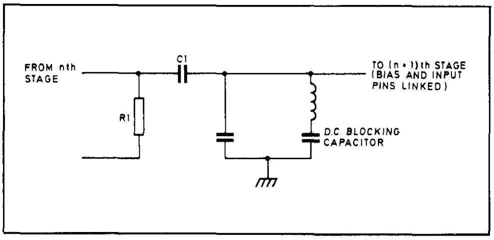


Fig. 9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nf	10nF	3nF	1nF

The 500pF supply decoupling capacitor has a resistance of, typically, 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (See Absolute Maximum Ratings).

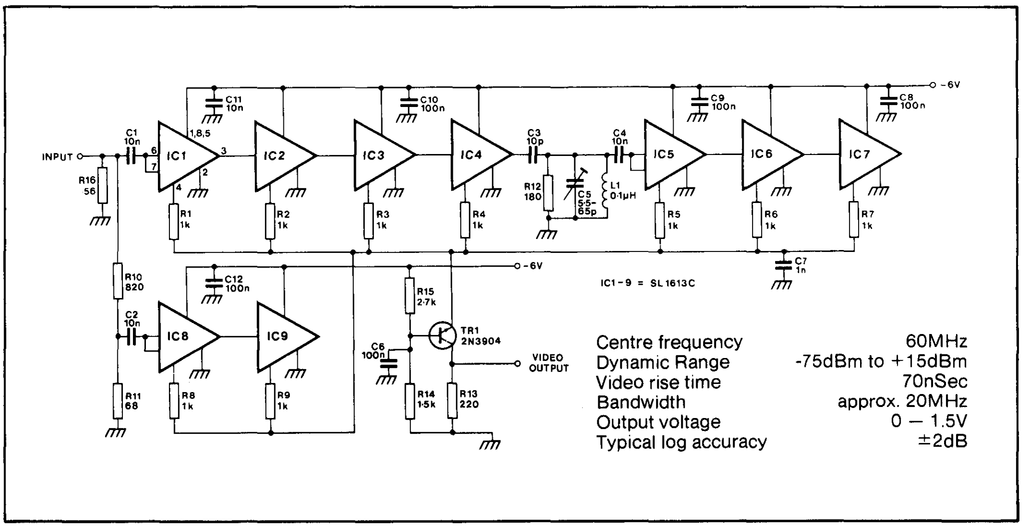


Fig. 10 Circuit diagram of low cost strip

PLESSEY
Semiconductors

SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.

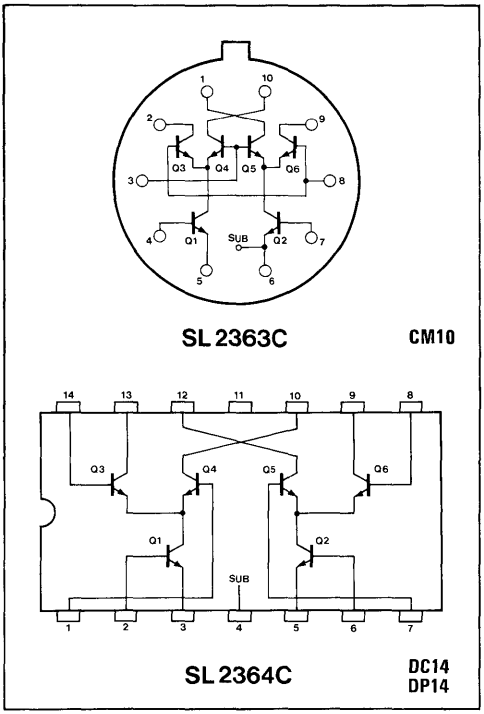


Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	20	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

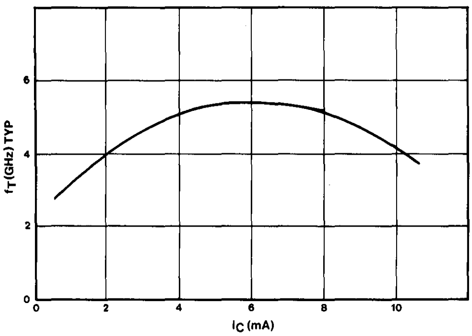


Fig. 2 Collector current

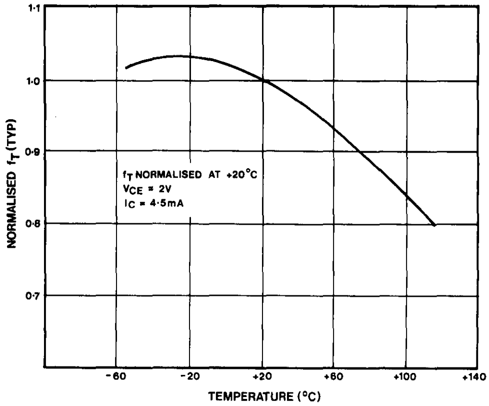


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature	−55°C to +150°C
Maximum junction temperature	+150°C

Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, I_C (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

PLESSEY Semiconductors

AUGUST 1985
PRELIMINARY INFORMATION

SL2521 EXP

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm 1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

FEATURES

- 1.3GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperature Stabilised
- Full Military Temperature Range/Surface Mountable

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

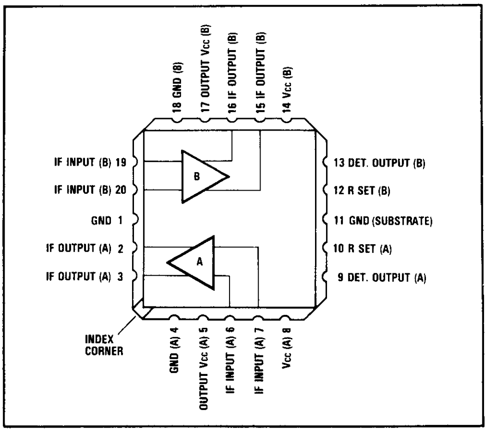


Fig.1 Pin connections - top view

FUTURE DEVELOPMENTS

It is the intention of Plessey Semiconductors Ltd. to offer the SL2521 EXP fully guaranteed over the temperature range -55°C to +125°C, with a second variant guaranteed over -30°C to +85°C.

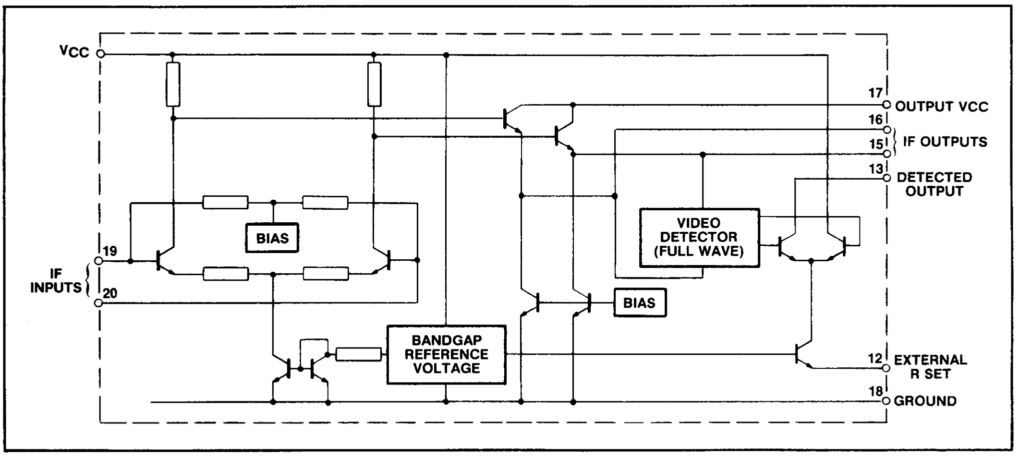


Fig.2 Circuit diagram (single stage B only)

DESCRIPTION

Logarithmic and limiting amplifiers are used extensively in radar and EW equipment, where phase performance and narrow pulse handling capability are essential, coupled with log accuracy (linearity) and wide dynamic range.

The video output is useable up to 600MHz and offers excellent temperature tracking. Due to the compact design, fast rise and fall times can be achieved and the IC does not suffer from 'pulse stretching' as with many discrete hybrid log modules.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 6V R_S = 50Ω R_L = 1kΩ; For single stage

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
Small signal gain	9.5	10	10.5	dB	f = 300MHz : T_{amb} = 25°C
IF upper cut-off frequency		1.3		GHz	-3dB wrt 200MHz
Detected output (bandwidth)		600			50% output current wrt 200MHz
Lower cut-off frequency		30		MHz	
Temperature variation detected output		±5		%	-55°C to +125°C
Temperature variation of IF gain		±0.2		dB	-55°C to +125°C
Ripple in band		±0.25		dB	100 to 400MHz
Supply current		40		mA	

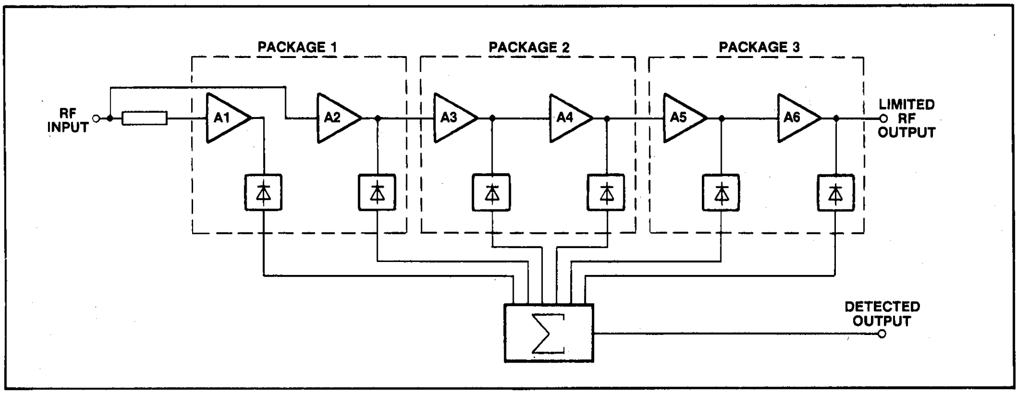


Fig.3 Schematic diagram showing configuration of SD amplifier

LOGARITHMIC LINEARITY/ACCURACY

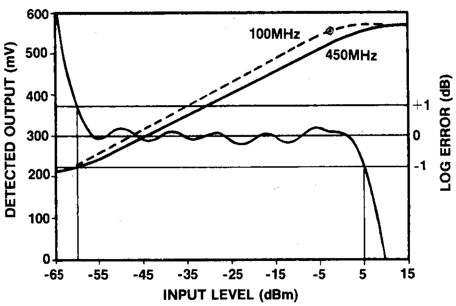


Fig.4 Detected output and logarithmic linearity at 450MHz. Detected output at 100MHz also imposed (6-stage strip)

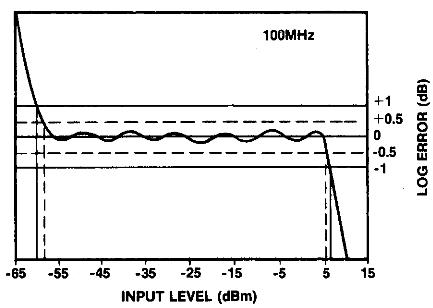


Fig.5 Logarithmic linearity at 100MHz showing greater than 62dB of dynamic range with accuracy of ±0.5dB (6-stage strip)

TYPICAL CHARACTERISTICS FOR 6-STAGE STRIP (as shown in Fig.3)

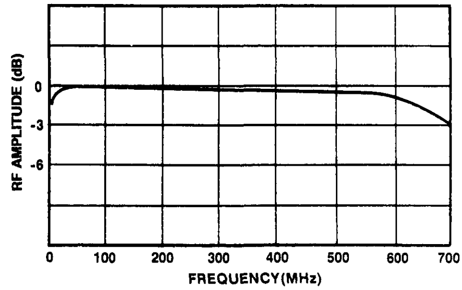


Fig.6 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

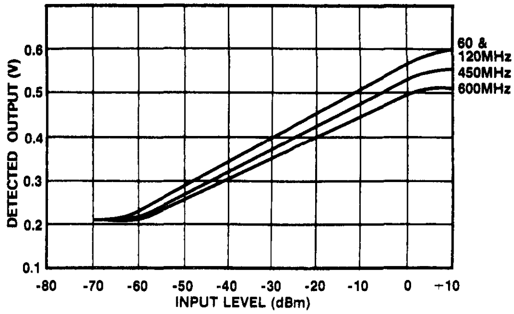


Fig.9 Video output v. CW input at 60, 120, 450 and 600MHz at 25° C

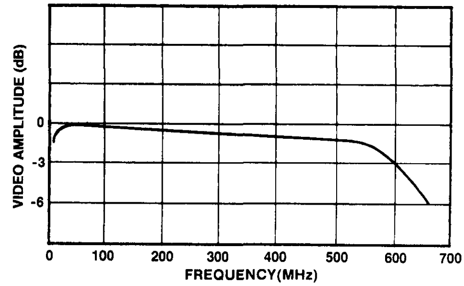


Fig.7 Video bandwidth

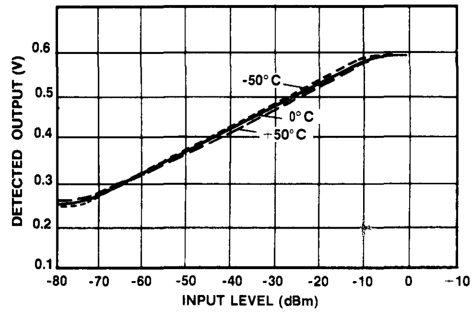


Fig.10 Video output v. temperature at 450MHz

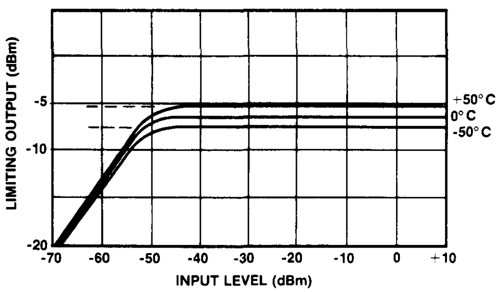


Fig.8 IF limiting v. temperature with CW input at 450MHz

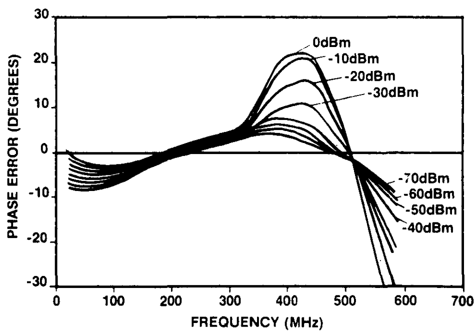


Fig.11 Departure from linear phase of a 6-stage SD log strip

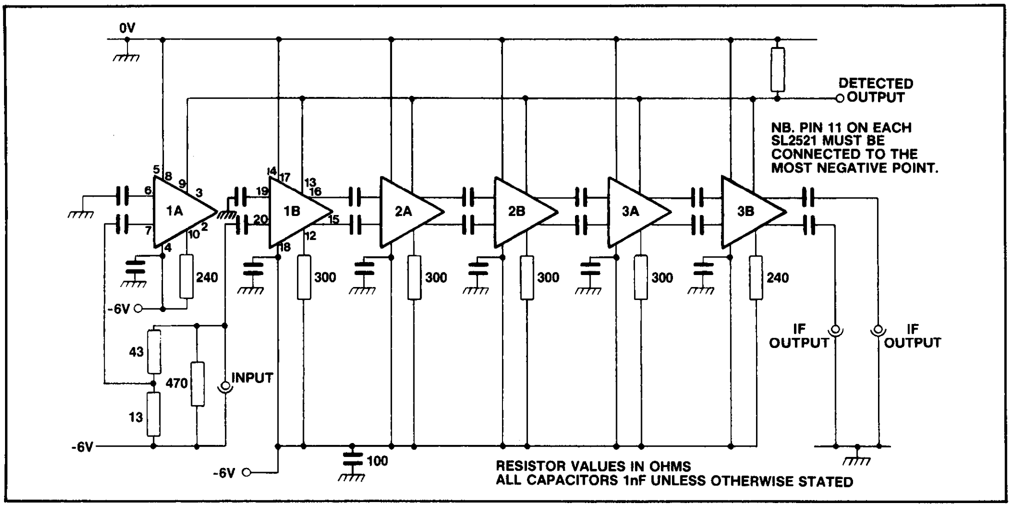


Fig.12 Circuit diagram for 6-stage log strip (results shown in Figs. 4 to 11 were achieved with this circuit)

PLESSEY
Semiconductors

SL3046C

GENERAL PURPOSE NPN TRANSISTOR ARRAY

The SL3046C is a monolithic array of five general purpose transistors arranged as a differential pair and three isolated transistors.

FEATURES

- 5 General Purpose Monolithic Transistors
- Good Thermal Tracking
- Wide Operating Current Range
- Suitable for Operation from DC to VHF
- Low Noise Performance 3.5dB at 1kHz

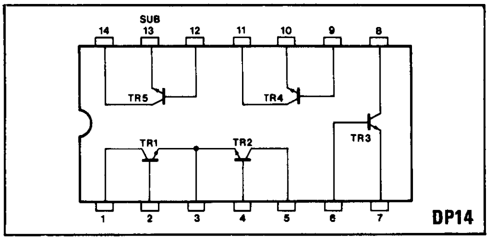


Fig. 1 Pin connections

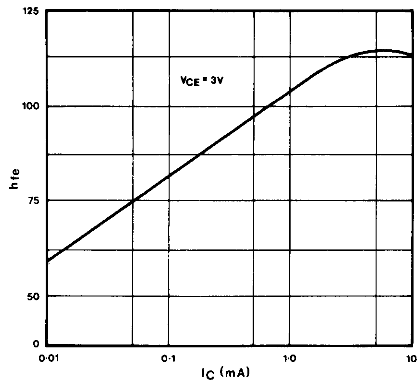


Fig. 2 Typical small signal current gain (common emitter vs. collector current)

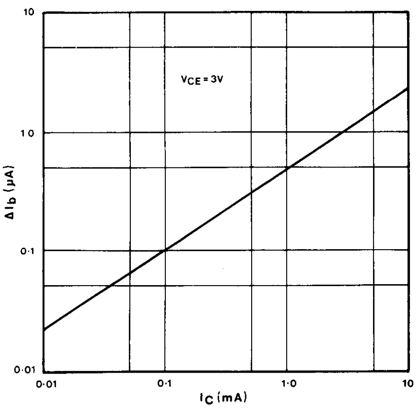


Fig. 3 Base current matching vs. collector current

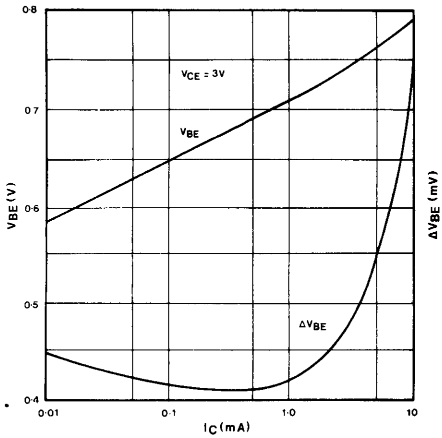


Fig. 4 Typical base emitter voltage and base emitter volt matching vs. collector current

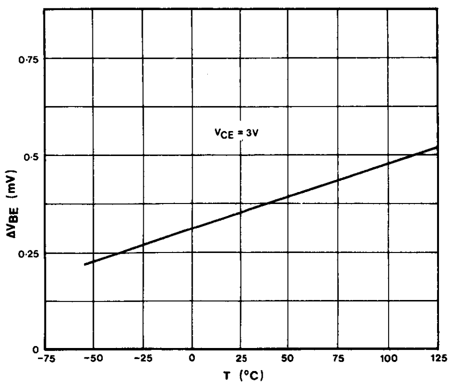


Fig. 5 Typical base emitter volt matching vs. chip temperature

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Static characteristics						
Emitter base leakage	I_{EBO}		0.1	1	μA	V_{EB} = 6V
Collector emitter breakdown	LV_{CEO}	15	20		V	I_C = 1mA
Collector-base breakdown	BV_{CBO}	20	50		V	I_C = 10μA
Collector-subtrate breakdown	BV_{CIO}	20	70		V	I_C = 10μA
Collector cut off current	I_{CEO}			0.5	μA	V_{CE} = 10V, I_B = 0
	I_{CBO}			40	nA	V_{CB} = 10V, I_B = 0
Base emitter voltage	$V_{BE}(ON)$		0.71		V	V_{CE} = 3V, I_C = 1mA
Collector-emitter saturation	$V_{CE}(SAT)$		0.23		V	I_B = 1mA, I_C = 10mA
Static forward current-transistor ratio	H_{FE}		120			V_{CE} = 3V, I_C = 10mA
		40	100			V_{CE} = 3V, I_C = 1mA
			50			V_{CE} = 3V, I_C = 10μA
Input offset current differential pair	I_{IO}		0.2	2	μA	V_{CE} = 3V, I_C = 1mA
Input offset voltage differential pair	ΔV_{BE1}		0.35	5	mV	V_{CE} = 3V, I_C = 1mA
Input offset voltage isolated transistors	ΔV_{BE2}		0.45	5	mV	V_{CE} = 3V, I_C = 1mA
Temperature coefficient of input offset voltage	$\frac{\partial \Delta V_{BE}}{\partial T}$		2		μV°C	V_{CE} = 3V, I_C = 1mA
Temperature coefficient of base emitter voltage	$\frac{\partial V_{BE}(ON)}{\partial T}$		-1.8		mV/°C	V_{CE} = 3V, I_C = 1mA
Dynamic characteristics						
Wideband noise figure	NF		3.25		dB	f = 10Hz to 10kHz V_{CE} = 3V, I_C = 100μA Source resistance = 1kΩ
Forward transfer admittance	Y_{fe}		31-j1.5		mmho	
Input admittance	Y_{ie}		0.3-j0.04		mmho	f = 1MHz
Output admittance	Y_{oe}		0.001 +j0.03		mmho	V_{CE} = 3V, I_C = 1mA
Reverse transfer admittance	Y_{re}		0.000-j0.003		mmho	
Forward current transfer ratio	h_{fe}		110			
Short circuit input impedance	h_{ie}		3.5		kΩ	
Open circuit output admittance	h_{oe}		15.6		μmho	f = 1kHz
Open circuit reverse voltage transfer ratio	h_{re}		1.8x10^{-4}			V_{CE} = 3V, I_C = 1mA
Gain bandwidth product	f_T	300	500		MHz	V_{CE} = 3V, I_C = 3mA
Emitter base capacitance	C_{EB}		1.2		pF	V_{EB} = 3V, I_E = 0
Collector base capacitance	C_{OB}		0.65		pF	V_{CB} = 3V, I_C = 0
Collector substrate capacitance	C_{CI}		2.55		pF	V_{CS} = 3V, I_C = 0

NOTE 1. Typical values are for design guidance only

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified performance may be impaired.

All electrical ratings apply to individual transistors; thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

Chip-to-ambient thermal resistance	175°C/W (DP14)
Storage temperature	−55°C to +125°C (DP14)
Junction operating temperature	+125°C (DP14)

V_{CBO} = 20V V_{EBO} = 6V I_C = 15mA I_B = 10mA
V_{CEO} = 15V V_{CIO} = 20V I_E = 15mA

PLESSEY
Semiconductors

SL3127C

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127C is a monolithic array of five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.6dB. The SL3127C is pin compatible with the CA3127.

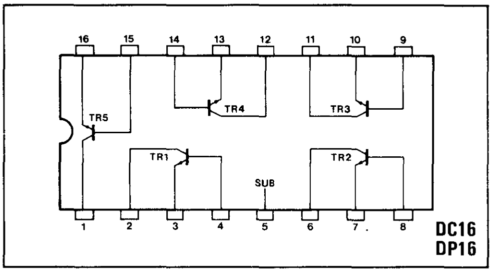


Fig.1 Pin connections SL3127

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.6dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

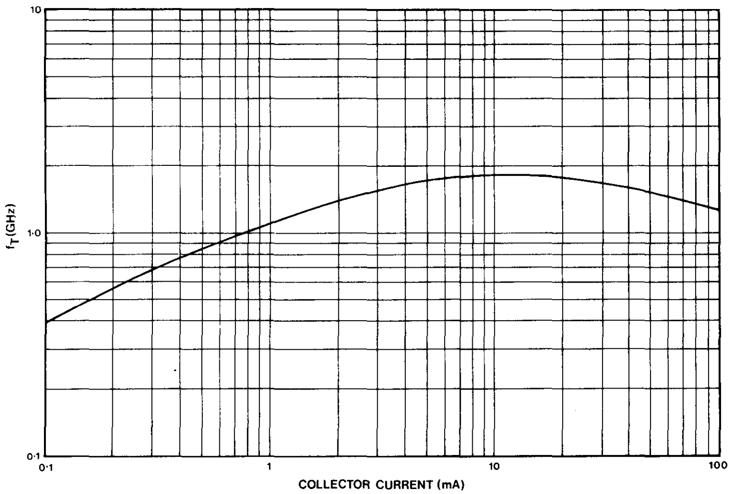


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}=2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22° C ± 2° C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10μA, I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA, I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10μA, I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10μA, I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector emitter saturation voltage	$V_{CE}(SAT)$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	μA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE}(SAT)$		0.95		V	I_C = 10mA, I_B = 1mA
Base emitter voltage difference, all transistors	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V, I_C = 1mA
Input offset current	ΔI_B		0.2	3	μA	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/°C	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V, I_C = 1mA
Static forward current ratio	H_{FE}	35	95			V_{CE} = 6V, I_C = 5mA
		35	100			V_{CE} = 6V, I_C = 0.1mA
		40	100			V_{CE} = 6V, I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Wideband noise figure	NF		3.6		dB	f = 60MHz } V_{CC} = 6V, I_C = 2mA, R_S = 200Ω
Knee of 1/f noise curve			1		kHz	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):—

Package Type	DC16	DP16
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

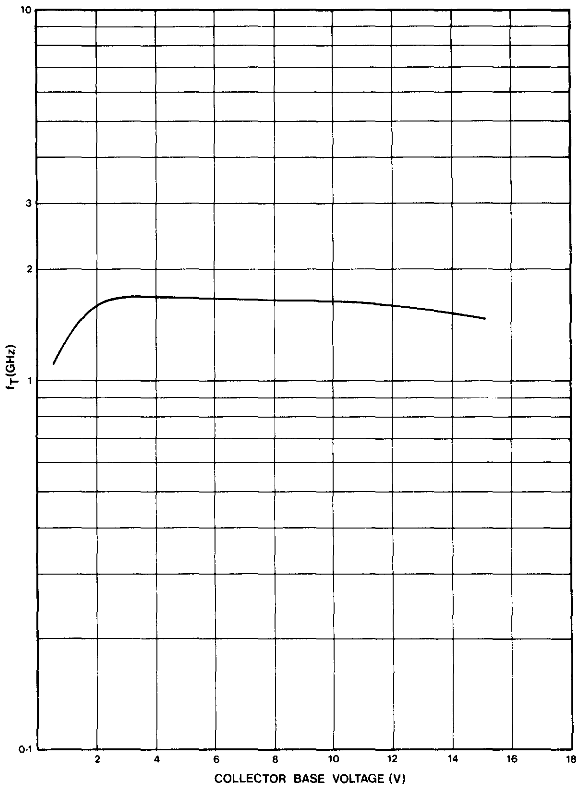


Fig.3 Transition frequency (f_T) v. collector base voltage
(I_C = 5mA, Frequency = 200MHz)

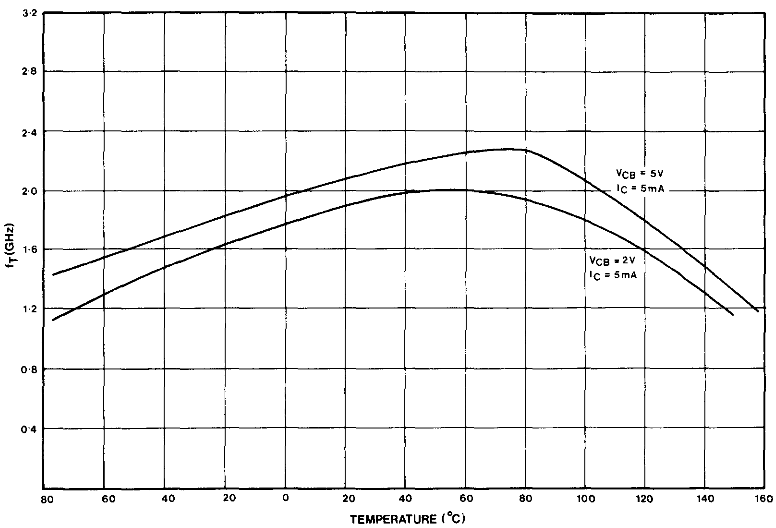


Fig.4 Variation of transition frequency (f_T) with temperature

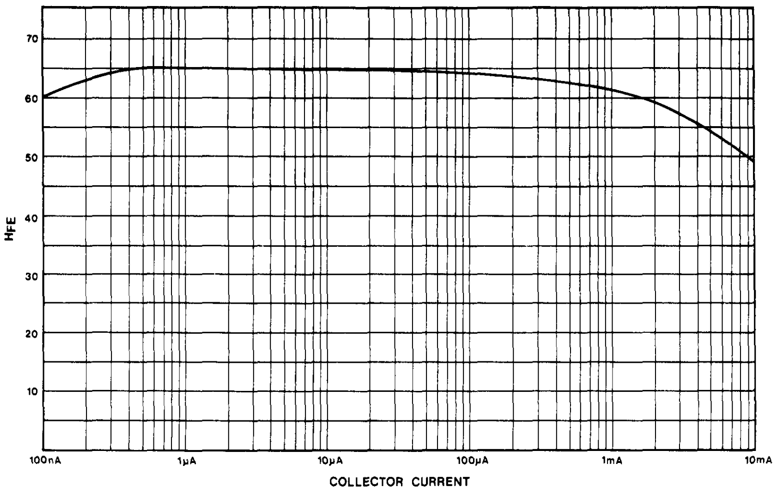


Fig.5 DC current gain v. collector current

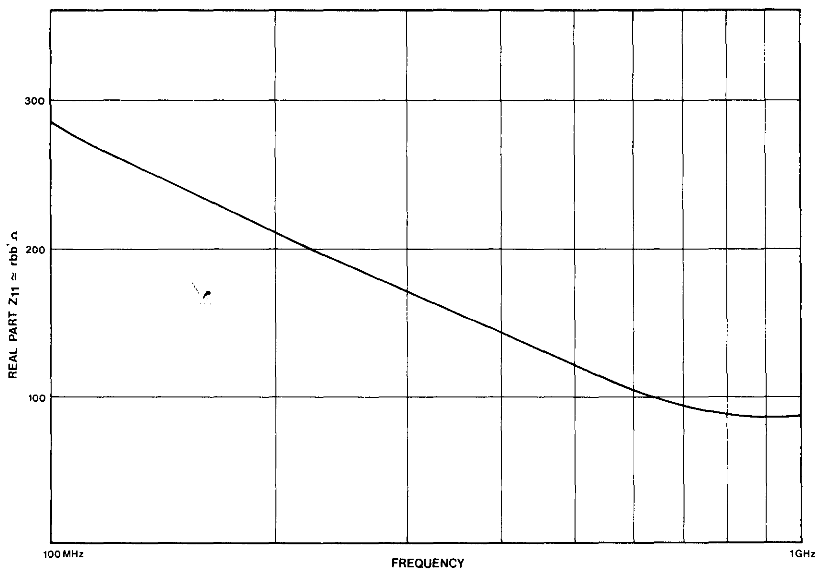


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r_{bb'}$)

PLESSEY
Semiconductors

SL3145C,E

1.2GHz HIGH FREQUENCY NPN TRANSISTOR ARRAYS

The SL3145C is a monolithic array of five high frequency low current NPN transistors. The SL3145C consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_{T}s of 1.6GHz and wideband noise figures of 3.0dB. The device is pin compatible with the SL3045C. The SL3145E has guaranteed C_{CB} and f_T figures.

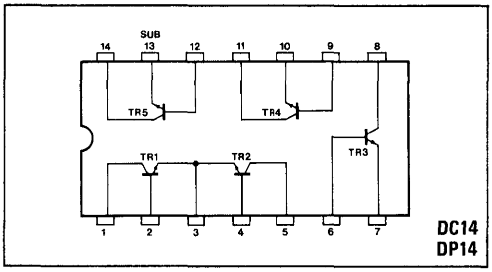


Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

Ordering information	
SL3145C-DC	Ceramic/Metal
SL3145C-DP	Plastic
SL3145E-DP	Plastic

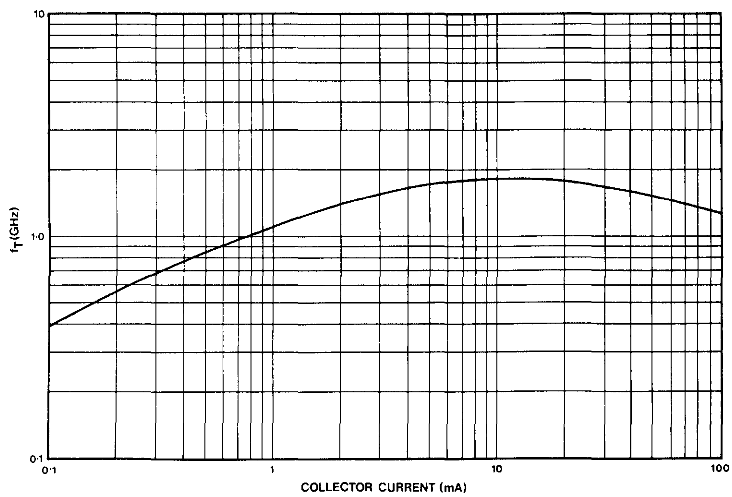


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	$I_C = 10\mu A, I_E = 0$
Collector emitter breakdown	LV_{CEO}	15	18		V	$I_C = 1mA, I_B = 0$
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	$I_C = 10\mu A, I_R = I_E = 0$
Base to isolation breakdown	BV_{BIO}	10	20		V	$I_B = 10\mu A, I_C = I_E = 0$
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	$V_{CE} = 6V, I_C = 1mA$
Collector emitter saturation voltage	$V_{CE}(SAT)$		0.26	0.5	V	$I_C = 10mA, I_B = 1mA$
Emitter base leakage current	I_{EBO}		0.1	1	μA	$V_{EB} = 4V$
Base emitter saturation voltage	$V_{BE}(SAT)$		0.95		V	$I_C = 10mA, I_B = 1mA$
Base emitter voltage difference, all transistors except TR1,TR2	ΔV_{BE}		0.45	5	mV	$V_{CE} = 6V, I_C = 1mA$
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	$V_{CE} = 6V, I_C = 1mA$
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	μA	$V_{CE} = 6V, I_C = 1mA$
Input offset current TR1, TR2	ΔI_B		0.2	2	μA	$V_{CE} = 6V, I_C = 1mA$
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/°C	
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	$V_{CE} = 6V, I_C = 1mA$
Static forward current ratio	H_{FE}	40	100			$V_{CE} = 6V, I_C = 1mA$
Collector base leakage	I_{CBO}		0.3		nA	$V_{CB} = 16V$
Collector isolation leakage	I_{CIO}		0.6		nA	$V_{CI} = 20V$
Base isolation leakage	I_{BIO}		100		nA	$V_{BI} = 5V$
Emitter base capacitance	C_{EB}		0.4		pF	$V_{EB} = 0V$
Collector base capacitance						
SL3145C	C_{CB}		0.4		pF	$V_{CB} = 0V$
SL3145E			0.4	1.1	pF	$V_{CB} = 0V$
Collector isolation capacitance	C_{CI}		0.8		pF	$V_{CI} = 0V$
Dynamic characteristics						
Transition frequency						
SL3145C	f_T		1.6		GHz	$V_{CE} = 6V, I_C = 5mA$
SL3145E		1.2			GHz	$V_{CE} = 6V, I_C = 10mA$
Wideband noise frequency	NF		3.0		dB	$V_{CE} = 2V, R_S = 1k\Omega$, $I_C = 100\mu A, f = 60MHz$
Knee of 1/f noise curve			1		kHz	$V_{CE} = 6V, R_S = 200\Omega$, $I_C = 2mA$

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):—

Package Type	DC14	DP14
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

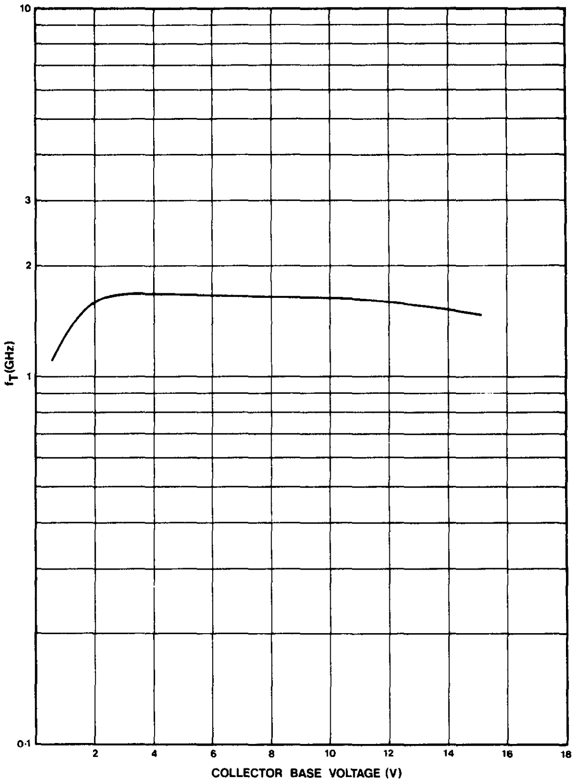


Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, frequency = 200MHz)

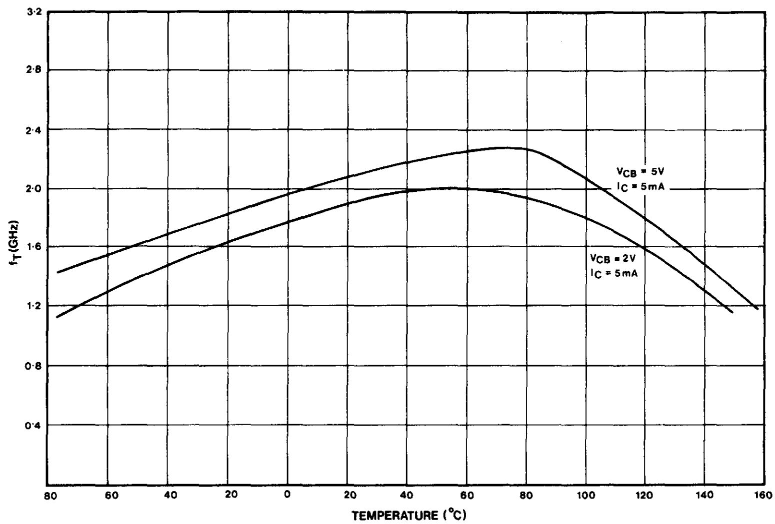


Fig.4 Variation of transition frequency (f_T) with temperature

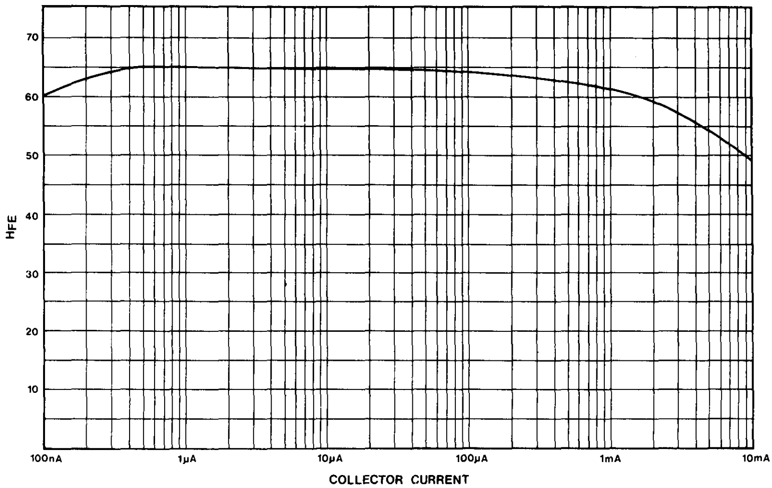


Fig.5 DC current gain v. collector curent

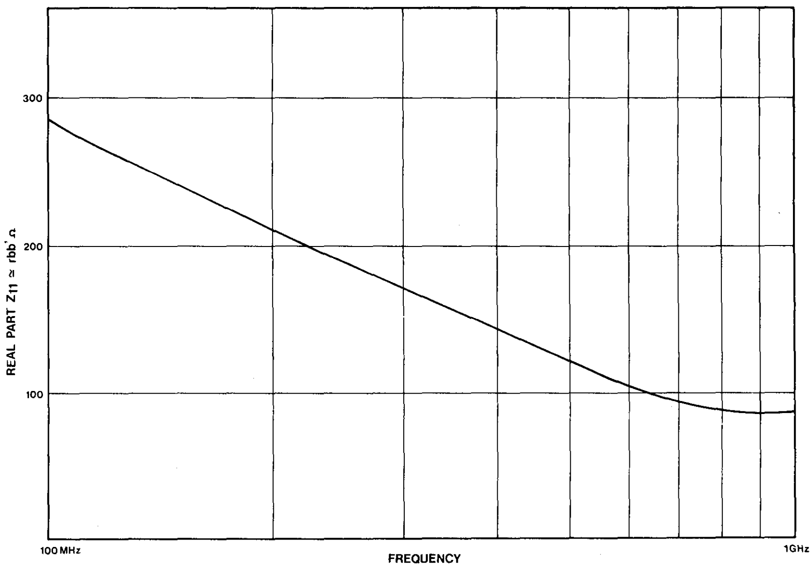


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r66'$)

PLESSEY
Semiconductors

SL6270C

GAIN CONTROLLED PREAMPLIFIER

The SL6270C is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

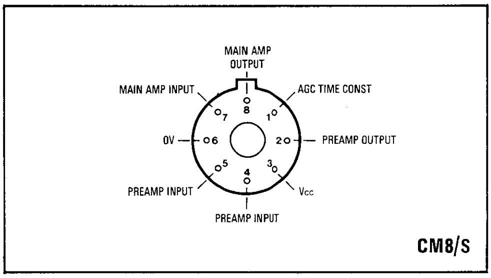


Fig. 1 Pin connections, SL6270C – CM (bottom view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

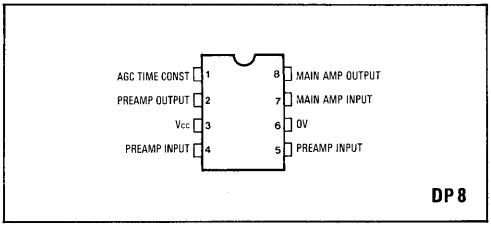


Fig. 2 Pin connections, SL6270C – DP (top view)

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: –55°C to +125°C

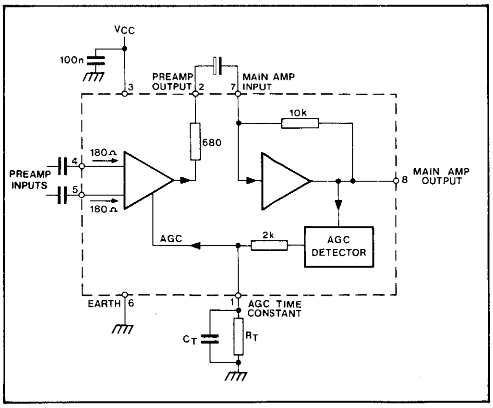
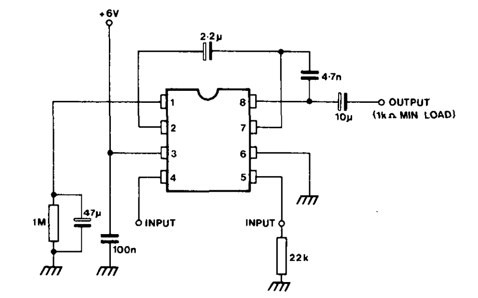


Fig. 3 SL6270C block diagram

ELECTRICAL CHARACTERISTICS

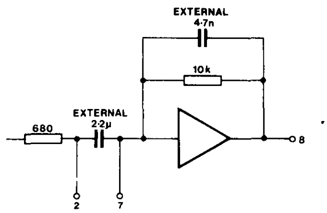
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: –30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72µV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		µV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig. 4 SL6270C test and application circuit



$$\text{Voltage gain} = \frac{10k\Omega}{680\Omega}$$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2µF = 300Hz

Fig. 5 SL6270C frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270C may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270C is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a –3dB point at 300Hz, corresponding to 2.2µF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270C has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and decay times

Normally the SL6270C is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig. 4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

Attack time = 0.4ms/µF

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

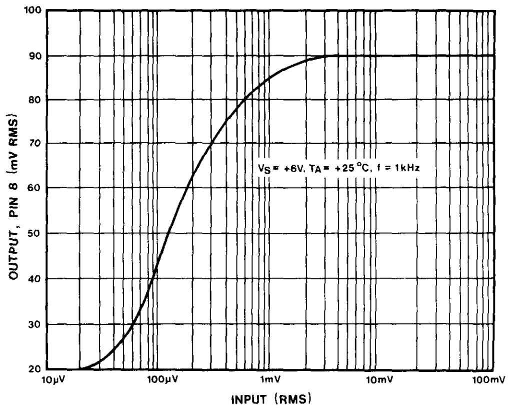


Fig. 6 Voltage gain (single ended input) (typical)

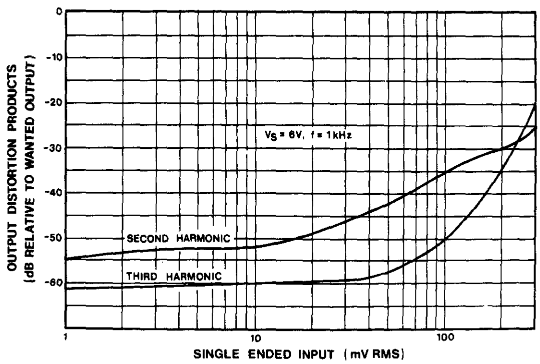


Fig. 7 Overload characteristics (typical)

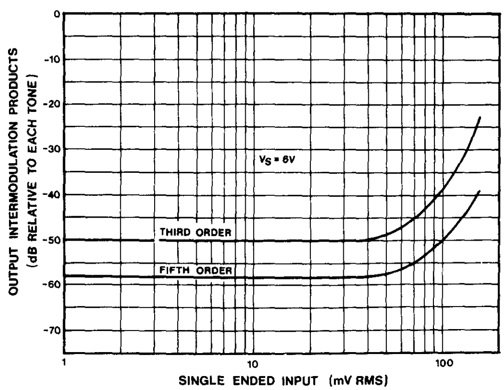


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

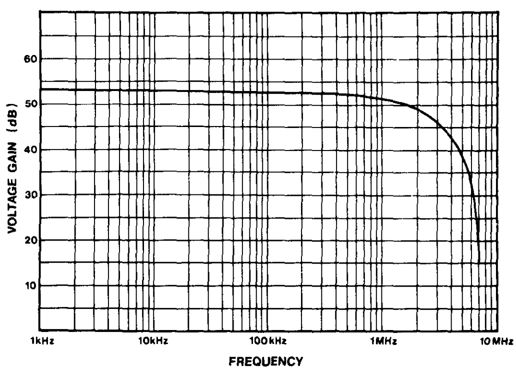


Fig. 9 Open loop frequency response (typical)

PLESSEY
Semiconductors

SL6310C

SWITCHABLE AUDIO AMPLIFIER

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply: 400mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: –55°C to +125°C

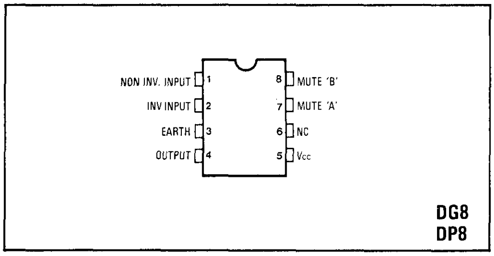


Fig.1 Pin connections SL6310C - (top view)

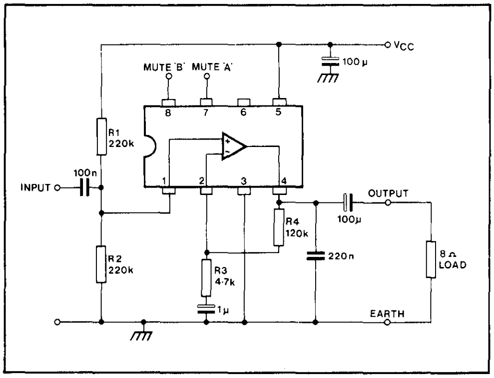


Fig.2 SL6310C test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 9V
Ambient temperature: –30°C to +85°C
Mute facility: Pins 7 and 8 open circuit frequency = 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 100k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs≤10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	Vcc = 4.5V
		10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs≤10k
Output power	400	500		mW	R_L = 8Ω
THD		0.4	3	%	P_{OUT} = 400mW, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

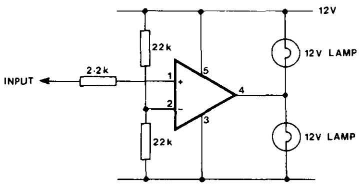


Fig.3 SL6310 lamp driver

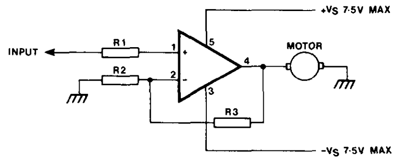


Fig.4 SL6310C servo amplifier

OPERATING NOTES

Mute facility

The SL6310C has two mute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310C is muted.

Mute control 'B', pin 8, is left open circuit or connected to a voltage less than 1 volt for normal operation: a voltage greater than 2.5V on pin 8 mutes the device. The input resistance at pin 8 is around 100kΩ and is suitable for interfacing with CMOS.

Only one mute control pin may be used at any time; the unused pin must be left open circuit.

Audio amplifier

As the SL6310C is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig. 2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

The output and power supply decoupling capacitors have to carry currents of several hundred milliamps and should be rated accordingly.

Applications include hand-held radio equipment, hi-fi headphone amplifiers and line drivers.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310C offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring a high output current.

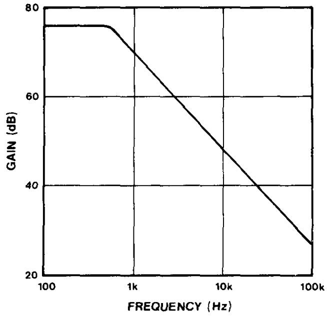


Fig.5 Gain v. frequency

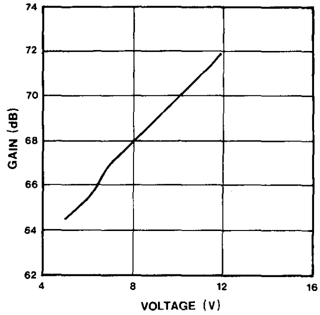


Fig.6 Gain v. supply voltage

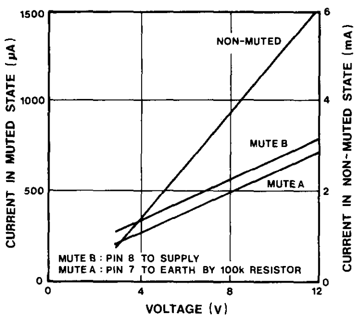


Fig.7 Supply current v. supply voltage

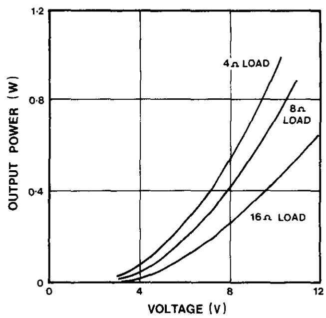


Fig.8 Output power v. supply voltage at 5 % (max) distortion

PLESSEY
Semiconductors

SL6440C

HIGH LEVEL MIXER

The SL6440 is a double balanced mixer intended for use in radio systems up to 150MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (bias) and V_{CC}. When biased for a supply current of 50mA the SL6440 offers a 3rd order intermodulation intercept point of typically +30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where diode ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

The SL6440C (in a 16-lead DIL plastic package) is specified for operation from -30° C to +85° C.

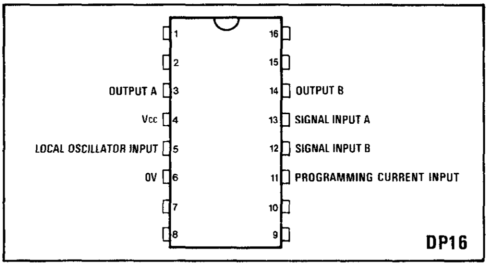


Fig.1 Pin connections - top view

FEATURES

- +30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance

APPLICATIONS

- Mixers in Radio Transceivers
- Phase Comparators
- Modulators

ABSOLUTE MAXIMUM RATINGS

Supply voltage and output pins: 15V
(Derate above 25° C: 8mW/° C)
Storage temperature range: -65° C to +150° C
Programming current into pin 11: 50mA

PACKAGE THERMAL DATA

Thermal resistance: Junction-Ambient: 125° C/W
Junction-Case: 40° C/W
Time constant: *Junction-Ambient: 1.9 mins.*
Max. chip temperature: 150° C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{CC}1$ = 12V; $V_{CC}2$ = 10V; I_p = 25mA; -30°C to +85°C (SL6440C)
Local oscillator input level = 0dBm; Test circuit Fig. 2.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
3rd order input intercept point		+30		dBm	
Third order intermodulation distortion		-60		dB	Two 0dBm input
Second order intermodulation distortion		-75		dB	Signals
1dB compression point		15		dBm	$V_{CC}1$ = 15V $V_{CC}2$ = 12V
		12		dBm	$V_{CC}1$ = 12V $V_{CC}2$ = 10V
Noise figure		11		dB	Fig.8 test circuit
Conversion gain		-1		dB	50Ω load Fig.2
Carrier leak to signal input	-40			dB	Test circuit Fig.8
Level of carrier at IF output		-25		dBm	See applications information
Supply current		7		mA	I_p = 0
Supply current (total from $V_{CC}1$ & $V_{CC}2$)		60		mA	
Local oscillator input	100	250	500	mVrms	I_p = 35mA
Local oscillator input impedance		1.5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

NOTE Supply current in Pin 3 is equal to that in Pin 14 and is equal to I_p See over. $V_{pin11} \approx 3\ V_{be} \approx 2.1V$

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_p pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply Vcc1 through a load.

The choice of Vcc1 is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than Vcc2 the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum Vcc1 = (I_p x RL) + Vs + Vcc2
where I_p = programmed current
RL = DC load resistance
Vs = max signal swing at output
if the signal swing is not known:
minimum Vcc1 = 2 (I_p x RL) + Vcc2

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply (Vcc2) for the oscillator buffer (pin 4).

The current (I_p) programmed into pin 11 can be supplied via a resistor from Vcc1 or from a current source.

The conversion gain is equal to

$$GdB = 20 \text{ Log } \frac{RL\ I_p}{56.6\ I_p + 0.0785} \text{ for single-ended output}$$

$$GdB = 20 \text{ Log } \frac{2\ RL\ I_p}{56.6\ I_p + 0.0785} \text{ for differential output}$$

Device dissipation is calculated using the formula

mW diss = 2 I_p Vo + V_p I_p + Vcc2 Diss
where Vo = voltage on pin 3 or pin 14
V_p = voltage on pin 11
I_p = programming current (mA)
Vcc2 Diss = dissipation obtained from graph(Fig.5)

As an example Fig. 7 shows typical dissipations assuming Vcc1 and Vo are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig. 4 shows the intermodulation performance against I_p. The curves are independent of Vcc1 and Vcc2 but if Vcc1 becomes too low the output signal swing cannot be accommodated, and if Vcc2 becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

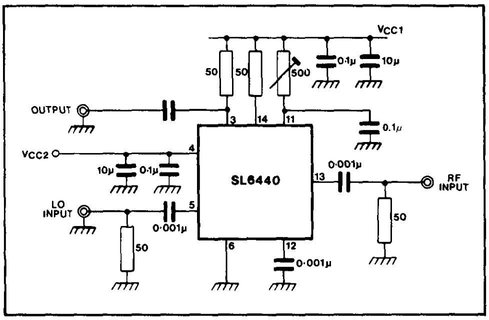


Fig.2 Typical application and test circuit

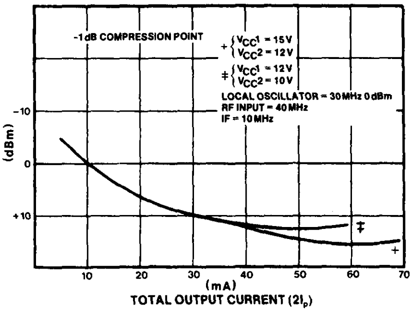


Fig.3 Compression point v. total output current

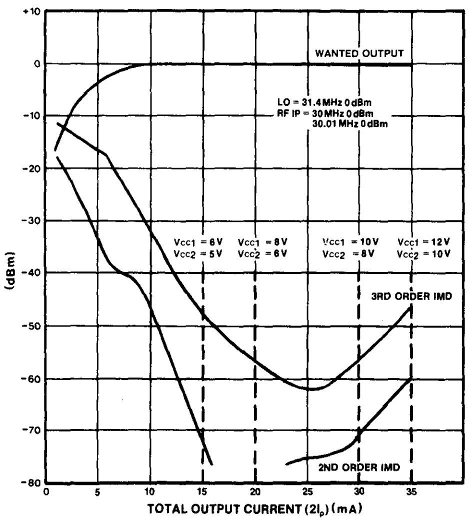


Fig.4 Intermodulation v. programming current

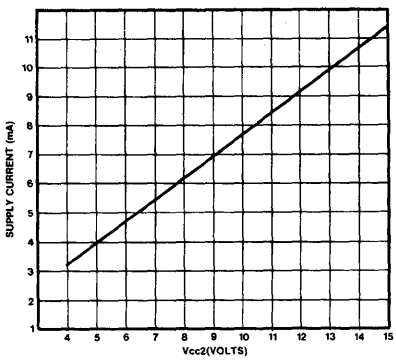


Fig.5 Supply current v. Vcc2 (I_p = 0)

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11.

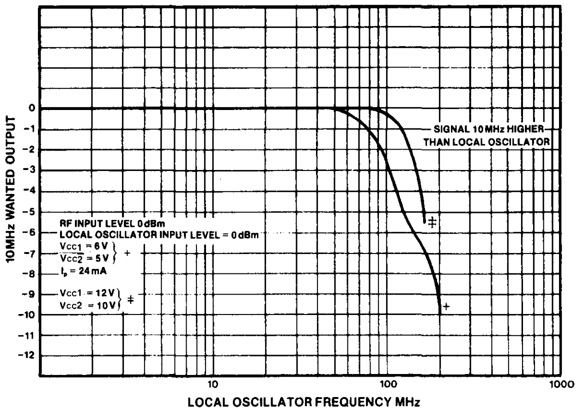


Fig.6 Frequency response at constant output IF

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single-ended and I_p is supplied from V_{CC1} via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for V_{CC1}.

Fig. 8 shows an application with balanced input, for improved carrier leak, and balanced output for increased conversion gain. A lower V_{CC1} giving lower device dissipation can be used with this arrangement.

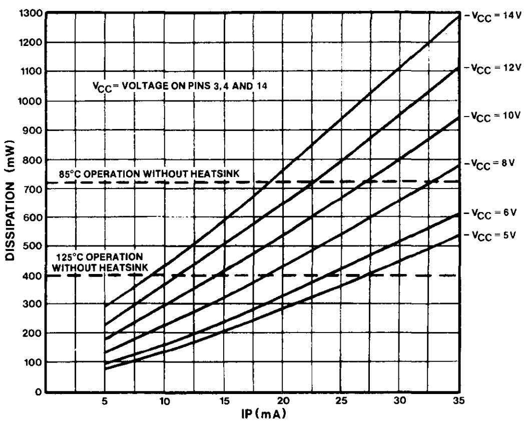


Fig.7 Device dissipation v. I_p

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data. If using transformer on input, decide on ratio from noise considerations.
2. Decide on output configuration and value of conversion gain required.
3. Decide on value of I_p and V_{CC2} using intermodulation and compression point graphs.
4. Using values of conversion gain, V_{CC2}, load and I_p already chosen, decide on value of V_{CC1}.
5. Calculate device dissipation and decide whether heatsink is required from maximum operating temperature considerations.

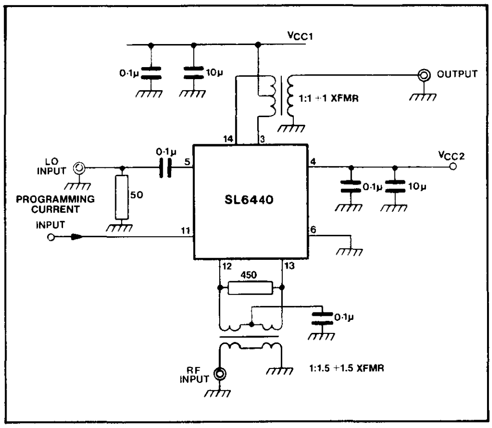


Fig.8 Typical application circuit for highest performance

PLESSEY Semiconductors

SL6601C

LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

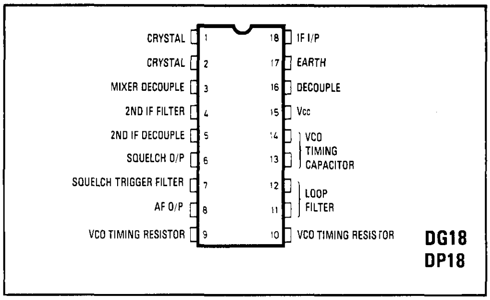


Fig.1 Pin connections - top view

FEATURES

- High Sensitivity: 2µV Typical
- Low Power: 2·3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

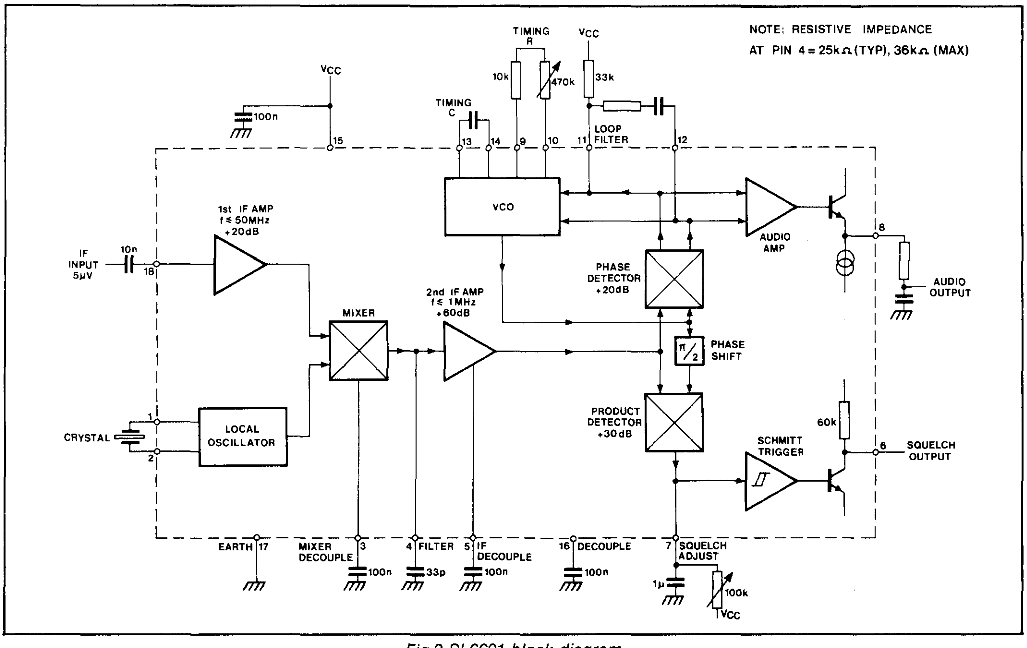


Fig.2 SL6601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage Vcc : 7V
Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation
Ambient temperature: -30° C to +85° C; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		μV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100μV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20μV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3μV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		μV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	390pF timing capacitor } No input
Grade 3	105		120	kHz	390pF timing capacitor } No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor according to the formula $(\frac{f}{35})$pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz (or uncoded)
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and V_{CC} to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choise of f_n, the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio f_m/f_n highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_e f_n}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error
f_n - loop natural frequency
Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for Φ_e should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of f_n should be chosen and the process repeated.

With f_n and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_oK_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_oK_D}$$

K_oK_D is $0.3f_o$, where f_o is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor: t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t_2 \times 20 \times 10^3}{t_1}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. $C_{calc} = 238pF$, use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'rounded up' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional $(R_{ext})^{-1/2}$ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let $f_n = 6$kHz and $D = 0.5$

Then from the graph

$$\frac{\Phi_e f_n}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \quad \frac{\Phi_e f_n}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set $f_n = 7.5\text{kHz}$

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_e f_n}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_oK_D}{(2\pi f_n)^2}$$

$K_oK_D = 0.3f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu s$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_oK_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu s$$

$$t_1 = 22.5\mu s$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4k\Omega \text{ (use 3.9k)}$$

Actual loop parameters can now be recalculated

$t_1 = 20\mu s \quad t_2 = 3.9\mu s$

$$2\pi f_n = \frac{(K_oK_D)}{(t_1 \times t_2} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} = 7.97\text{kHz}$$

$$D = f_n(t_2 + \frac{1}{K_oK_D}) = \underline{0.515}$$

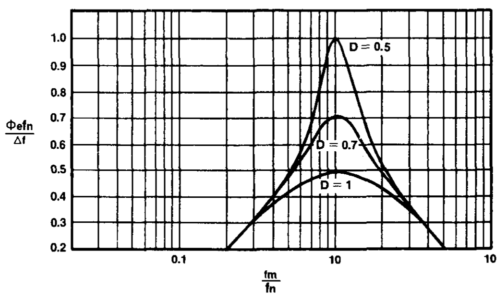


Fig.3 Damping factor

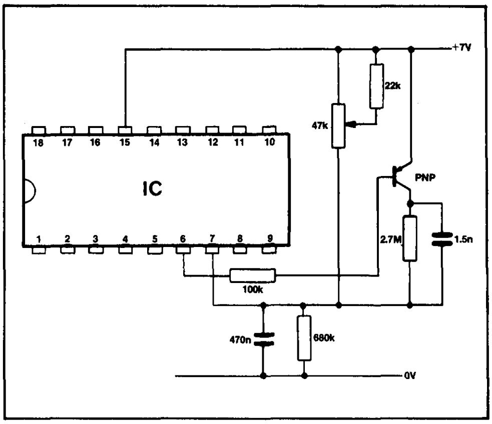


Fig.4 Using an external PNP in the squelch circuit

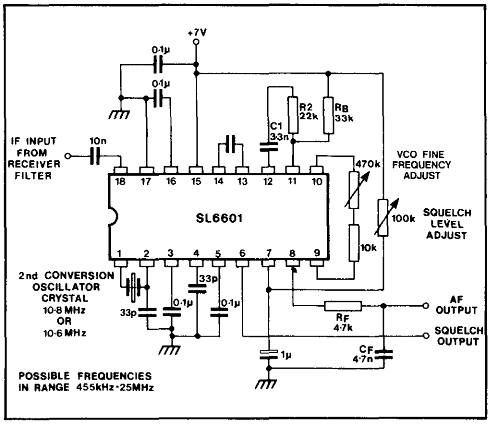


Fig.5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

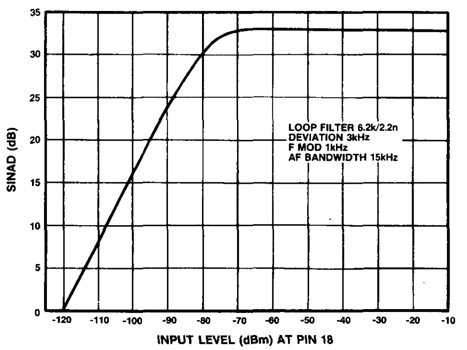


Fig.6 Typical SINAD
(signal + noise + distortion/noise + distortion)

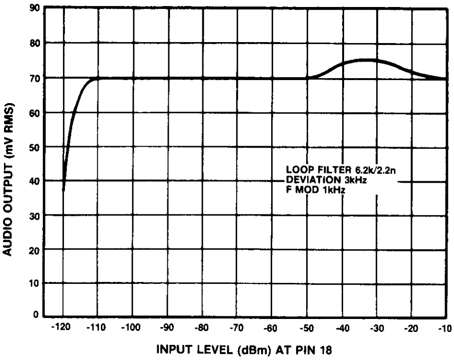


Fig.7 Typical recovered audio v. input level (3kHz deviation)

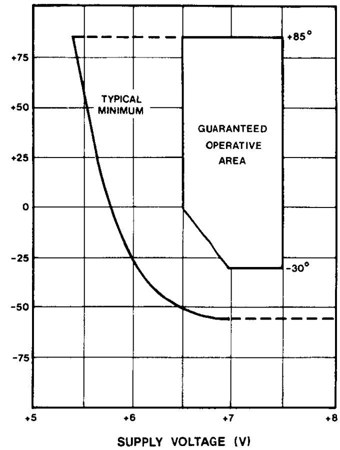


Fig.8 Supply voltage v. temperature

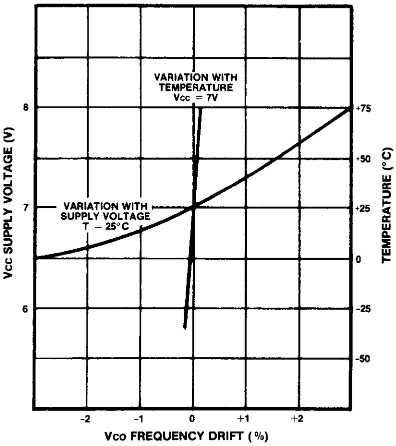


Fig.9 Typical VCO characteristics

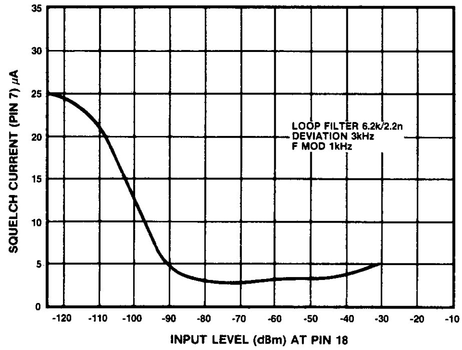


Fig.10 Typical squelch current v. input level

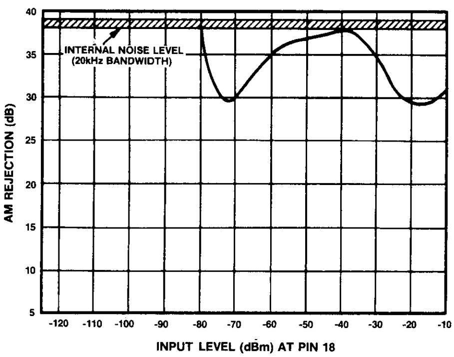


Fig.11 Typical AM rejection

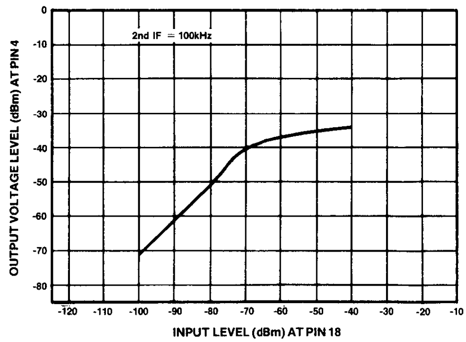


Fig.12 Typical conversion gain (to pin 4)

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55°C to +125°C (DP package)
	-55°C to +150°C (DG)
Operating temperature (see Electrical Characteristics)	-55°C to +125°C
Input voltage	1V RMS at pin 18

PLESSEY Semiconductors

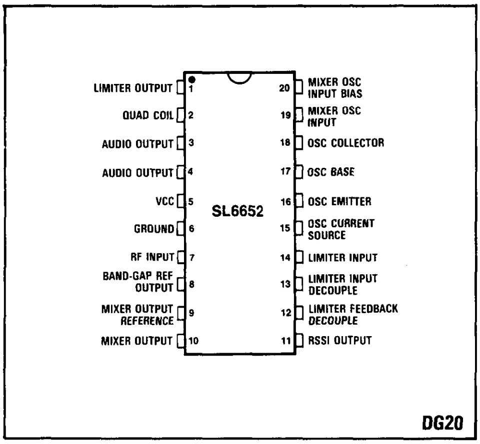
ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL6652

LOW POWER IF/AF CIRCUIT FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.



FEATURES

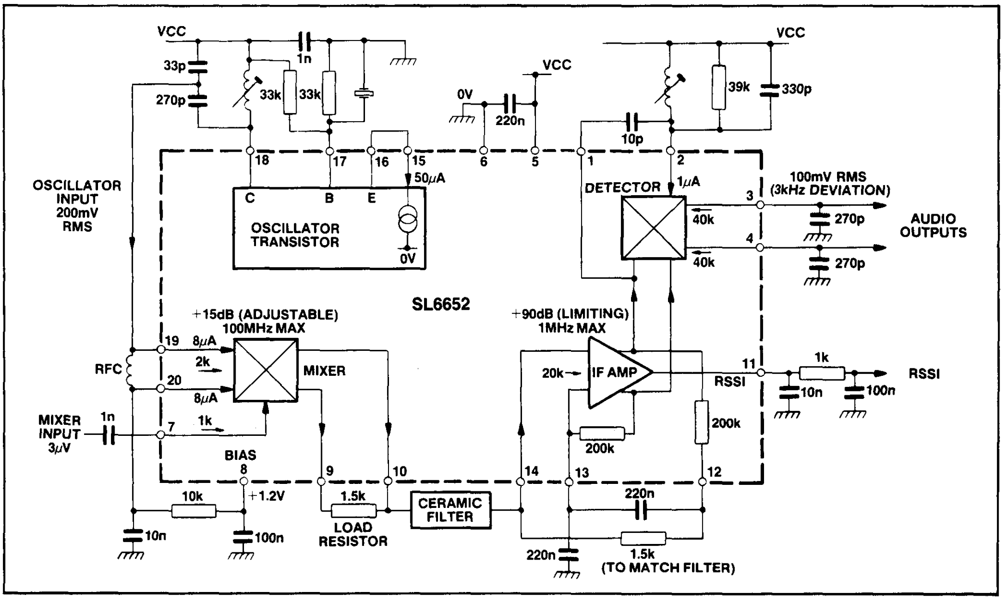
- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB



ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25°C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	5mV into pin 14
THD		0.5	5	%	5mV into pin 14
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output(T_{amb} = +25°C)					
Output current			20	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20°C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

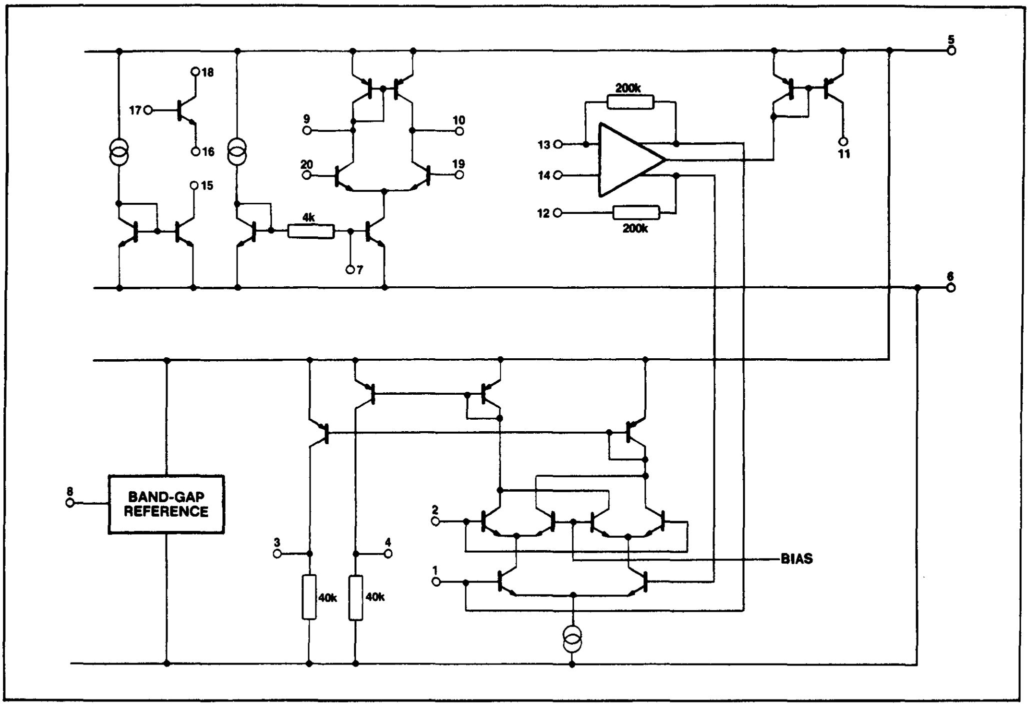


Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

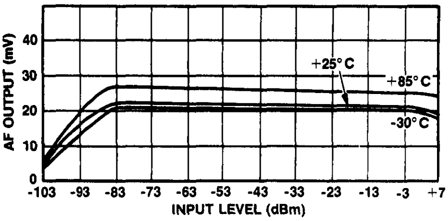


Fig.4 Audio output vs input and temperature at 2.5V

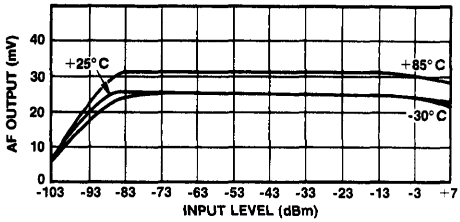


Fig.5 Audio output vs input and temperature at 5.0V

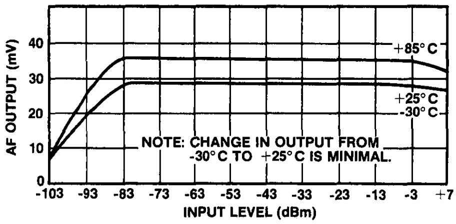


Fig.6 Audio output vs input and temperature at +7.5V

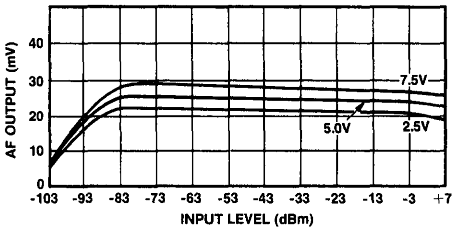


Fig.7 Audio output vs input and supply voltage at +25°C

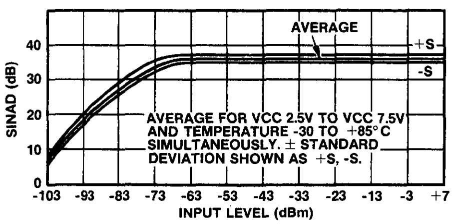


Fig.8 SINAD and input level

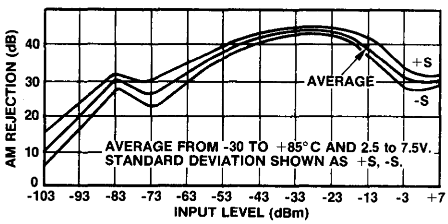


Fig.9 AM rejection and input level

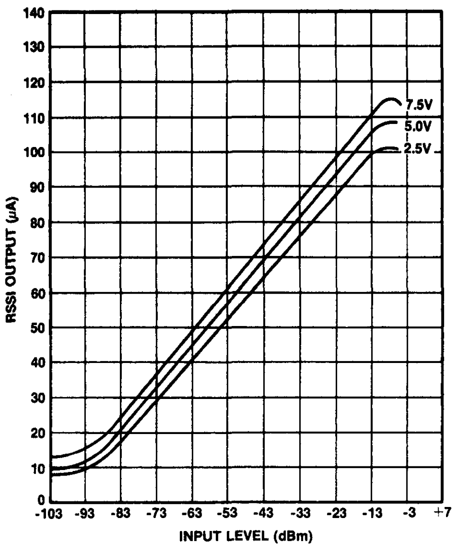


Fig.10 RSSI output vs input and supply voltage
(T_{amb} = 20° C)

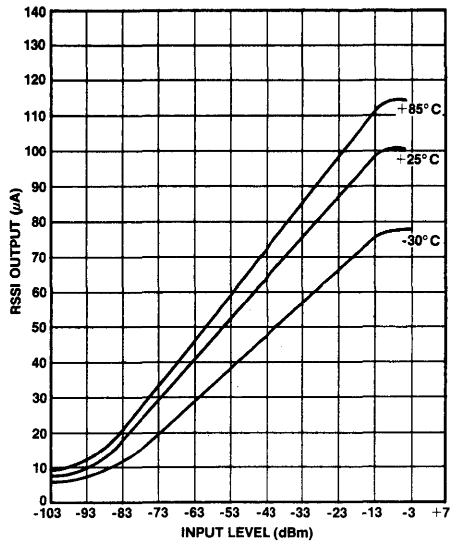


Fig.11 RSSI output vs input level and temperature
(V_{CC} = 2.5V)

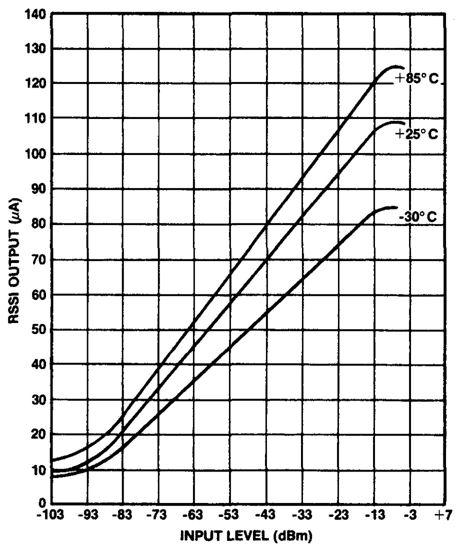


Fig.12 RSSI output vs input level and temperature
(V_{CC} = 5V)

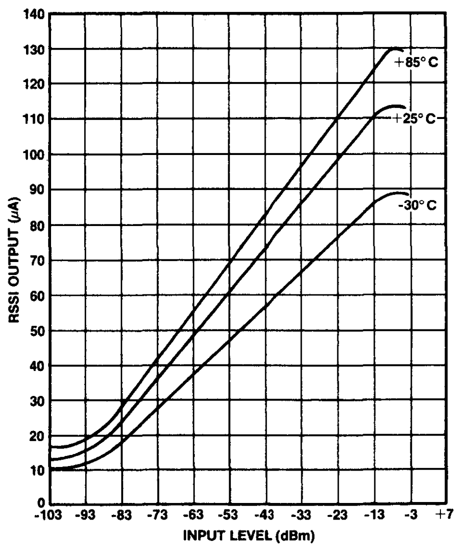


Fig.13 RSSI output vs input level and temperature
(V_{CC} = 7.5V)

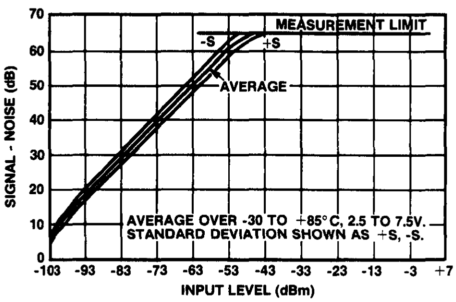


Fig.14 Signal + noise to noise ratio vs input level

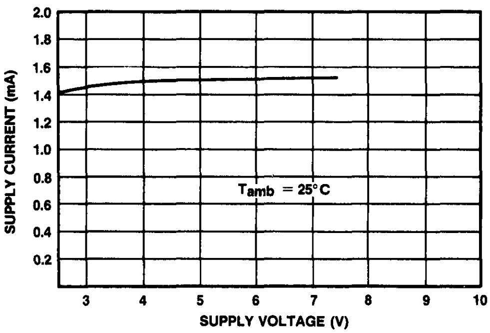


Fig.15 Supply current vs supply voltage

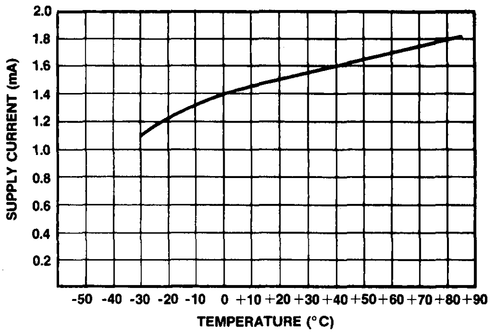


Fig.16 Supply current vs temperature (V_{CC} = 5V)

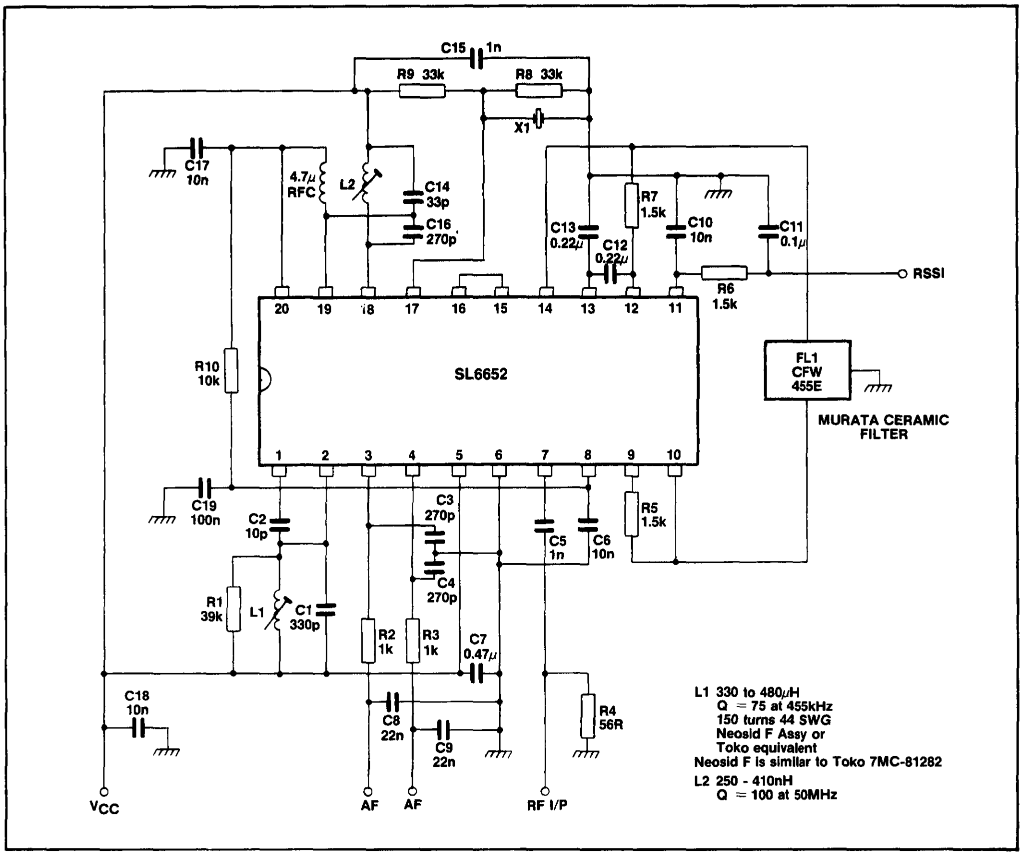


Fig.17 Circuit diagram of SL6652 demonstration board

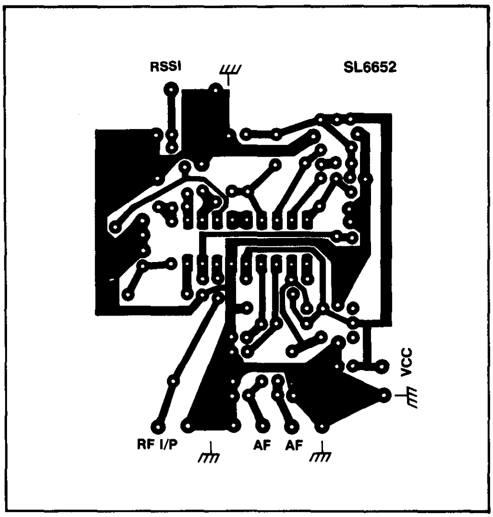


Fig.18 PCB mask of demonstration board (1:1)

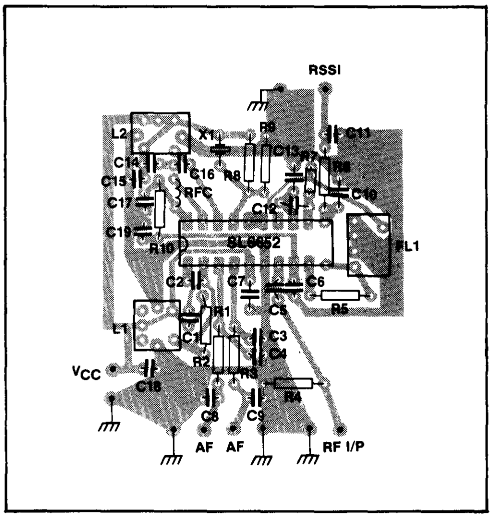


Fig.19 Component overlay of demonstration board (1:1)

PLESSEY Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL6653

LOW POWER IF/AF CIRCUIT FOR FM RECEIVERS

The SL6653 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V

The SL6653 affords maximum flexibility in design and use. It is supplied in a dual-in-line hermetic package.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation

QUICK REFERENCE DATA

- Supply voltage 2.5V to 7.5V
- Sensitivity 3µV

APPLICATIONS

- Mobile Radio Telephones
- Cordless Telephones

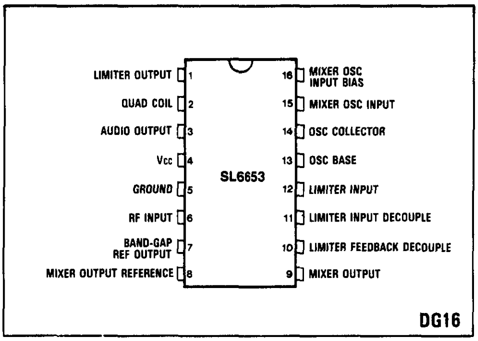


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

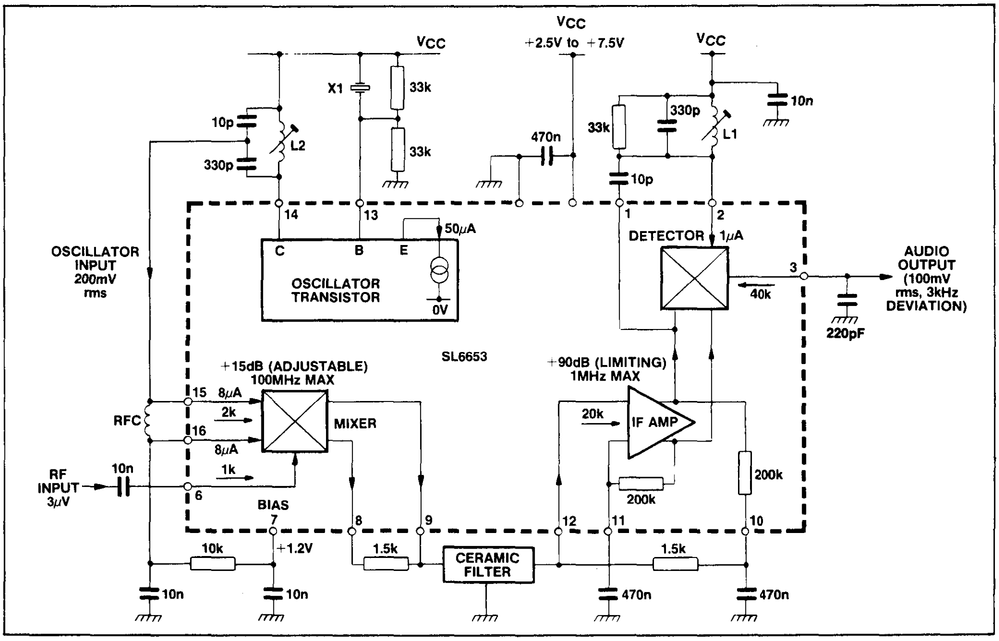


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, Mod.Freq. = 1kHz, Deviation = 2.5kHz, Quadrature Circuit Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		30		dB	RF input < 500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25°C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	
Ultimate S/N ratio		60		dB	10mV into pin 12
THD		0.5	5	%	
Output impedance		40		kohm	

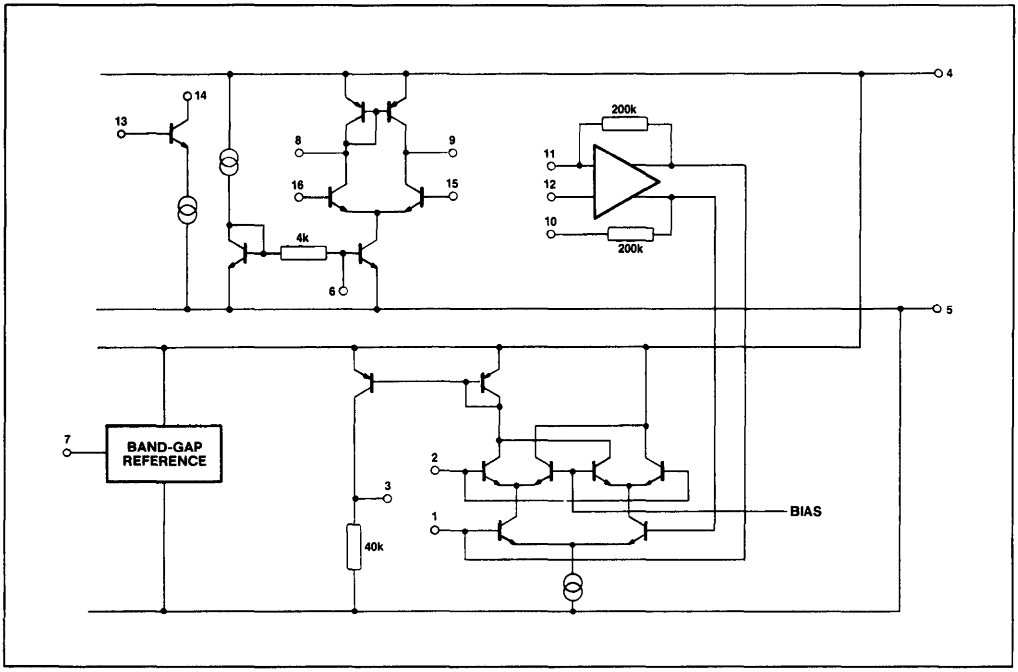


Fig.3 Simplified internal schematic

GENERAL DESCRIPTION

The SL6653 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- A transistor for use as an oscillator
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of a transistor and a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

Supply voltage

The SL6653 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

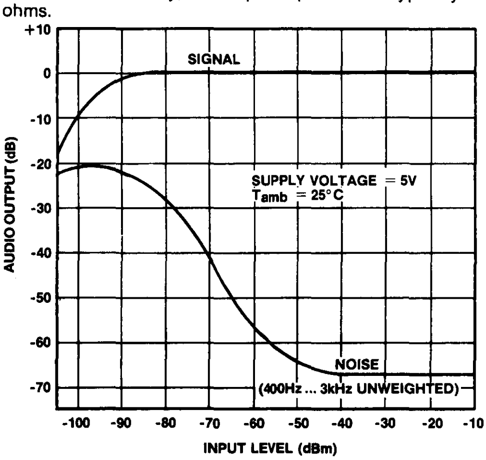


Fig.4 Audio and noise outputs vs input level

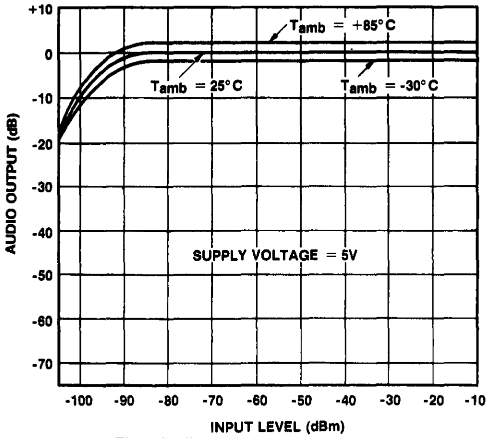


Fig.5 Audio output vs temperature

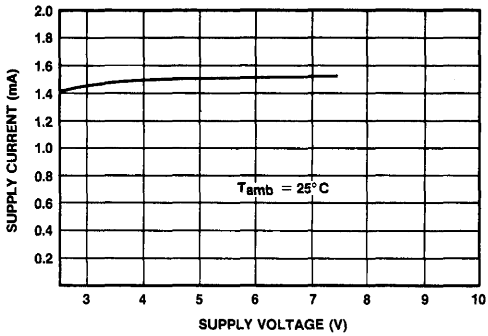


Fig.6 Supply current vs supply voltage

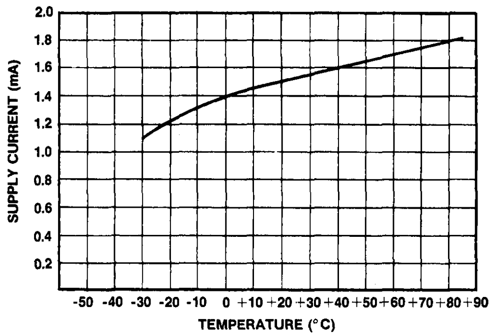


Fig.7 Supply current vs temperature

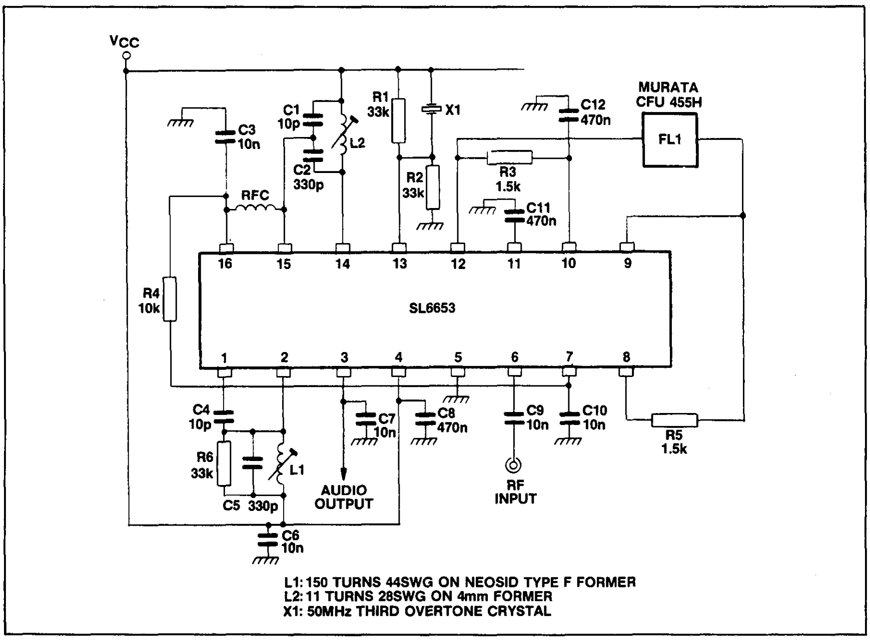


Fig.8 Circuit diagram of SL6653 demonstration board

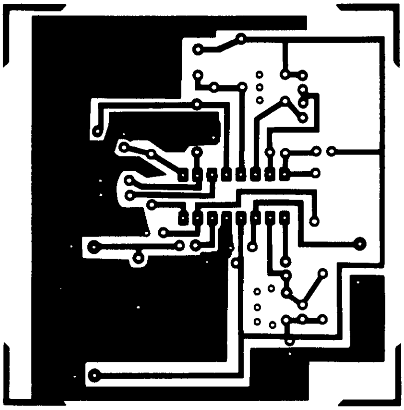


Fig.9 PCB mask of demonstration board (1:1)

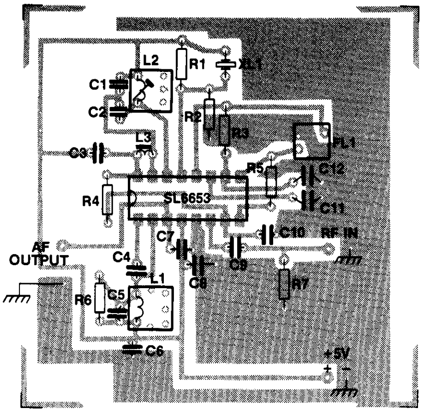


Fig.10 Component overlay of demonstration board (1:1)

PLESSEY
Semiconductors

SL6691C

MONOLITHIC CIRCUIT FOR PAGING RECEIVERS

The SL6691C is an IF system for paging receivers, consisting of a limiting IF amplifier, quadrature demodulator, voltage regulator and audio tone amplifier with Schmitt trigger.

The voltage regulator requires an external PNP transistor as the series pass transistor. The frequency response of the tone audio amplifier is externally defined.

The SL6691C operates over the temperature range -30° C to +85° C.

FEATURES

- Very Low Standby Current
- Fast Turn-on
- Wide Dynamic Range
- Minimum External Components

APPLICATIONS

- Pagers
- Portable FM Broadcast Receivers

ABSOLUTE MAXIMUM RATINGS

Storage temperature - 65°C to + 150°C
Supply voltage 6V

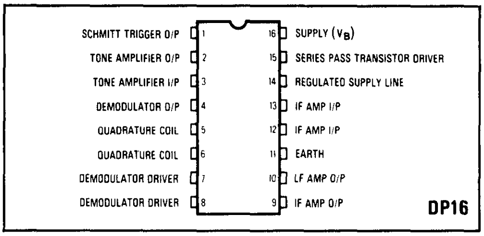


Fig.1 Pin connections (top view)

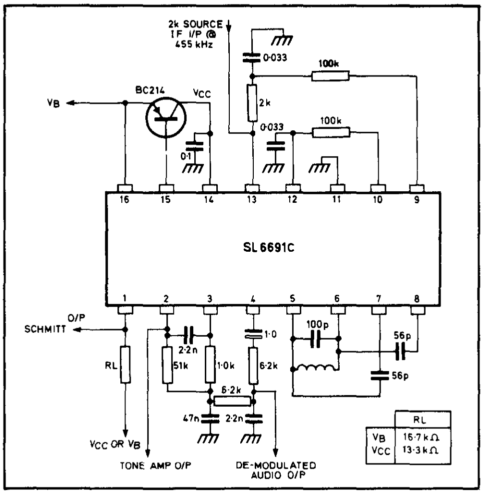


Fig.2 SL6691C test circuit

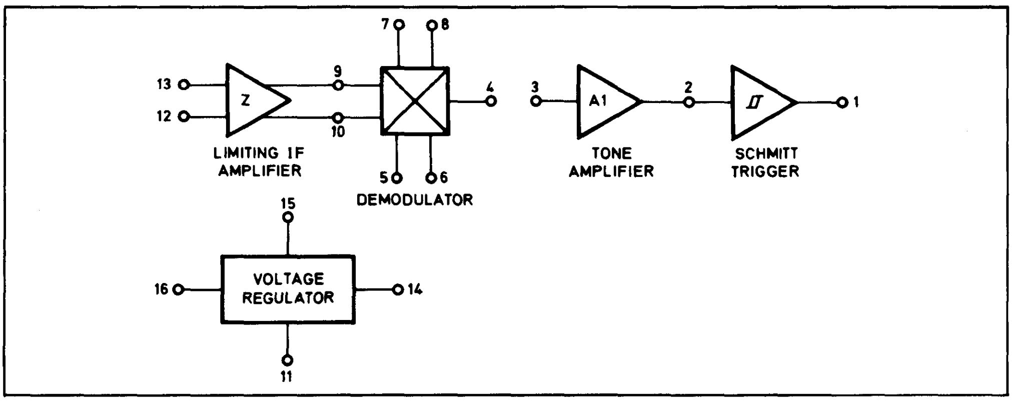


Fig.3 SL6691C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature	-30°C to +85°C
Supply voltage (V_C)	2.5V
IF frequency	455kHz (nominal)
Modulation frequency	500Hz
Deviation	±4.5kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Quiescent current		1.0	1.4	mA	$V_B = 3V$ Pins 2 and 3 S/C Pins 1 and 4 O/C
Switch on time		12	18	ms	Note 1
Voltage regulator					
Regulated voltage	1.9		2.1	V	$V_B > 2.2V$
Supply line rejection		40		dB	$V_B > 2.2V$ 200mV p-p square wave @ 500 Hz injected
Current sink capability pin 15	100			μA	
IF amplifier					
Input impedance		20//2		kΩ//pF	
Output impedance		2		kΩ	
Dynamic range		100		dB	
Output voltage swing		600		mV p-p	
Amplifier gain		90		dB	
Sensitivity	20	16		μV rms	Audio 20dB S+N/N ratio
AM rejection		40		dB	100μV rms I/P @ 30% AM modulation
Amplifier 3dB bandwidth		1.5		MHz	
Demodulator					
Audio output	8	15		mV rms	Quadrature element L-C tuned circuit: Q = 30
Distortion, THD		1.5	3	%	
Output impedance		1	3	kΩ	
Signal-to-noise ratio		40		dB	100μV rms I/P 3kHz audio bandwidth
Tone amplifier					
Open loop gain		54		dB	
Peak output current		20		μA	
Schmitt trigger					
Mark space ratio		45/55	38/62		20μV rms I/P

NOTES

1. The 'Switch On' time is the time to the zero crossing point of the centre of the first occurrence of a 30/70 or 70/30 mark space wave on the output of the Schmitt trigger after the supply voltage has been switched on. Conditions: $V_B = 2V$, Tone filter connected (See Fig.2), IF input = 100μV rms, Modulation 500 Hz @ 2 kHz deviation.

CIRCUIT DESCRIPTION

IF Amplifier and Detector

The IF amplifier consists of five identical differential amplifier/emitter follower stages with outputs at the fourth (pins 9 and 10) and fifth (pins 7 and 8) stages. The outputs from the fourth stage are used when the lowest turn-on time is required. Coupling to the quadrature network of the detector is via external capacitors; otherwise the design is conventional. The audio output is taken from pin 4 and filtered externally.

Tone (Audio) Amplifier

The tone amplifier is a simple inverting audio amplifier with voltage gain determined by the ratio of feedback resistor to input resistor. The frequency response can readily be controlled by suitable selection of feedback components.

Schmitt Trigger

The Schmitt trigger has an open collector output stage which saturates when the input at pin 2 is high. A 20μV rms input is sufficient.

NOMINAL DC PIN VOLTAGES(DP16)

Function	Pin	Voltage
Supply	16	Battery voltage
Series pass transistor driver	15	Battery voltage –0.7V
Regulated supply line	14	2V
Earth	11	0V
IF amp I/P	13	1V
IF amp I/P	12	1V
IF amp O/P	10	1V
IF amp O/P	9	1V
Demodulator O/P	4	1V
Quadrature coil	6	1V
Quadrature coil	5	1V
Tone amplifier I/P	3	1.4V
Schmitt trigger O/P	1	0V or pin 16 or pin 14
Tone amplifier O/P	2	1.4V
Demodulator driver	7	1V
Demodulator driver	8	1V

PLESSEY Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL6700A

IF AMPLIFIER AND AM DETECTOR

The SL6700A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable. This device is characterised for operation from -55°C to +125°C.

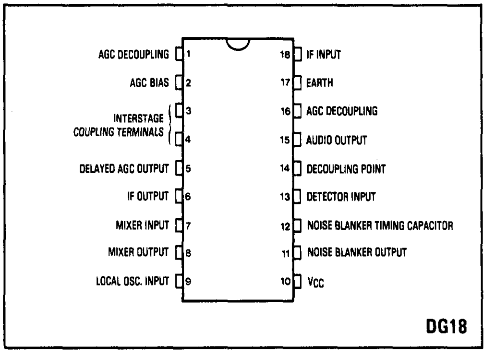


Fig.1 Pin connections (top view)

FEATURES

- High Sensitivity: 10μV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

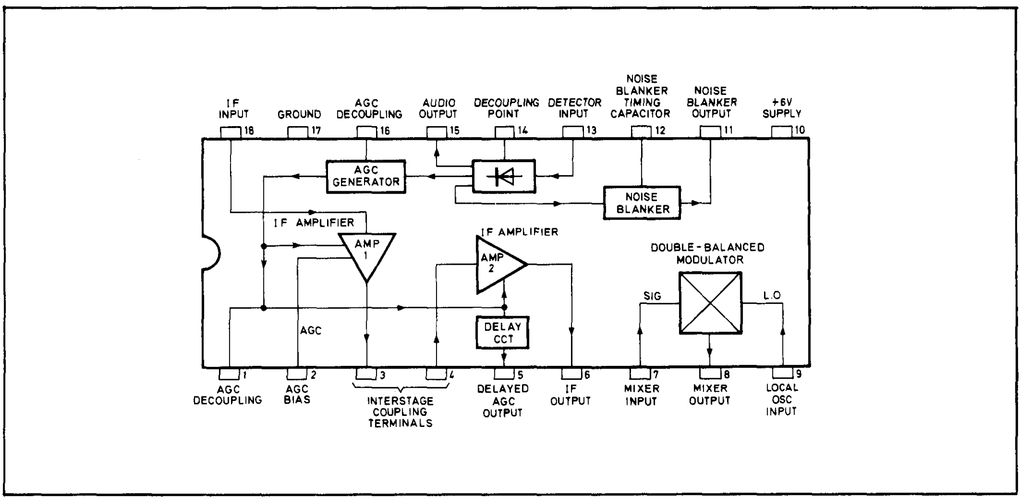


Fig.2 SL6700A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} -55°C to +125°C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	1mV input 30% modulation
Sensitivity	10	5		μV	10dB S + N/N ratio, 30%
Audio output level change		6	10	dB	10μV to 50mV input 80%
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	4.0			V	Logic 1
			0.3	V	Logic 0
Noise blank duration	300	400	500	μs	C pin 12 = 30nF,R pin 12-11 = 18k
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (L.O.)	3	5	8	kΩ	
Mixer L.O. injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 30μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

The mixer may also be used as a product detector. Further application information is available on request in Application Note AN1001.

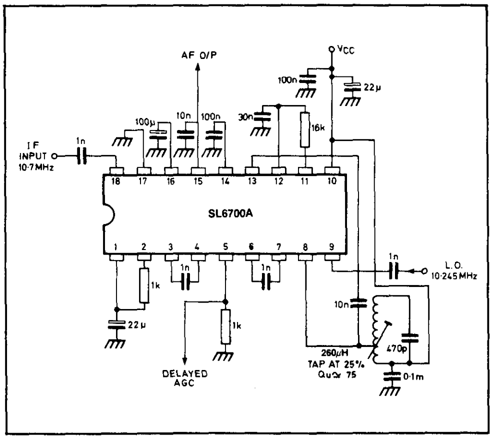


Fig.3 SL6700A AM double conversion receiver with noise blanker

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

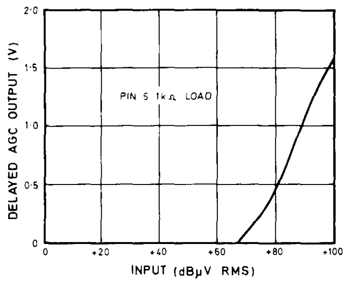


Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

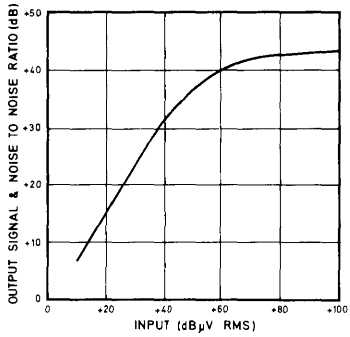


Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

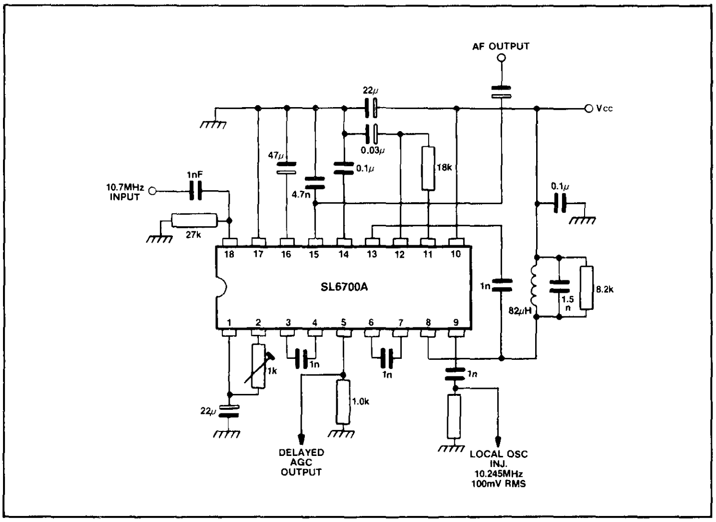


Fig.6 Test circuit

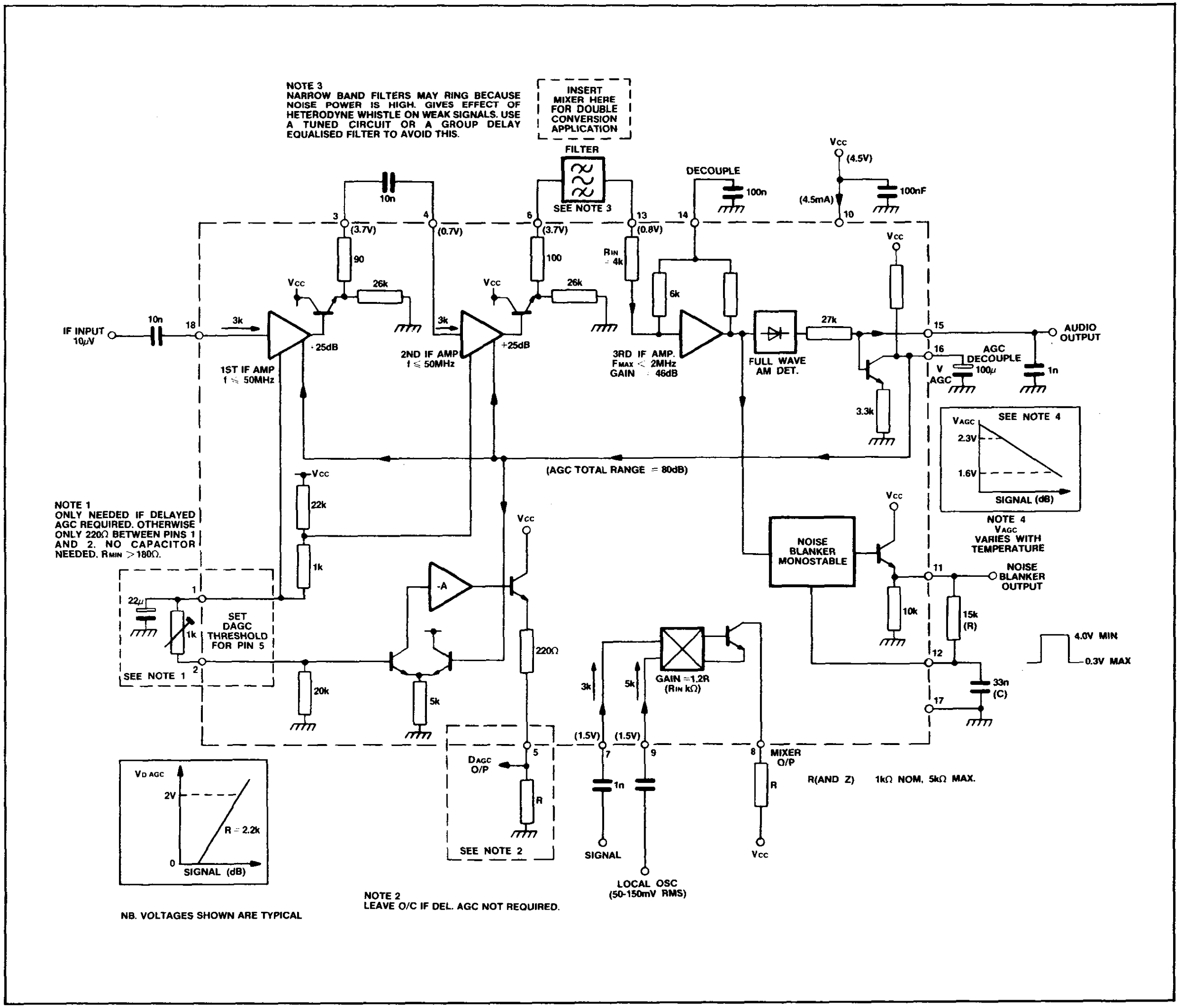


Fig.7 SL6700A Typical application circuit showing interfacing

PLESSEY
Semiconductors

SL6700C

IF AMPLIFIER AND AM DETECTOR

The SL6700C is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700C will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable.

FEATURES

- High Sensitivity: 10μV minimum
- Low Power: 8mA Typical at 6V
- Linear Detector

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

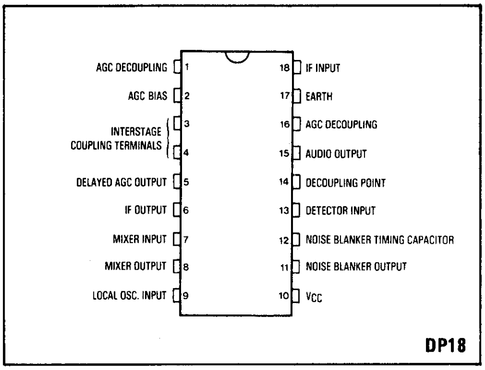


Fig. 1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 7.5V
Storage temperature: —55°C to +125°C

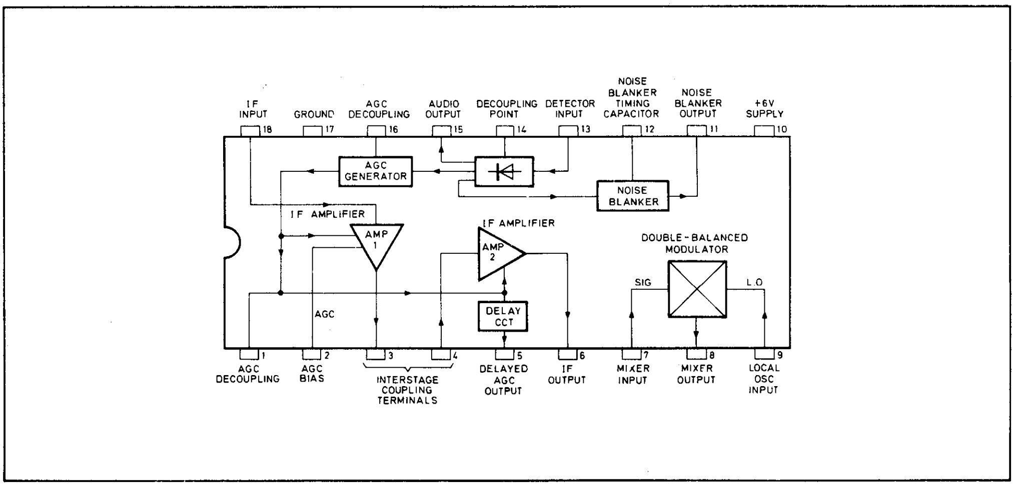


Fig. 2 SL6700C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 4.5V
T_{Amb} -30°C to +85°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		4.5	6	mA	
S/N ratio		40		dB	1mV input 80% mod @ 1kHz
TH distortion		1	5	%	1mV input 80% mod @ 1kHz
Sensitivity	10	5		μV	10dB S + n/N ratio, 30% mod 1kHz
Audio output level change		6	10	dB	10μV to 50mV input 80% mod 1kHz
AGC threshold		5		μV	
AGC range		80		dB	
AF output level		25		mV rms	30 % modulation 1kHz
Delayed AGC threshold		10		mV rms	80 % modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	40	50		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM 1kHz
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	2.7			V	Logic 1
			0.6	V	Logic 0
Noise blank duration		300		μs	C pin 12 = 30nF
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (signal)	2	3	5	kΩ	
Mixer Z_{in} (LO)	3	5	8	kΩ	
Mixer LO injection	20	50	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, 1kHz modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 300μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700C and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available in Application Note AN1001.

TYPICAL DC PIN VOLTAGES
(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

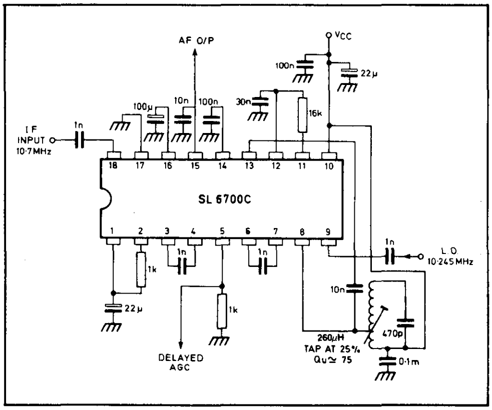


Fig. 3 SL6700C AM double conversion receiver with noise blanker

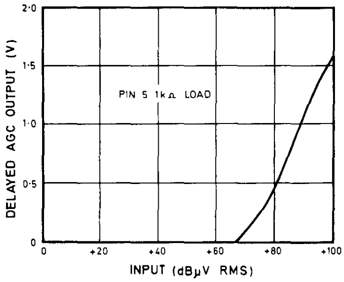


Fig. 4 Typical delayed AGC output variation with input signal (f=10.7MHz, 30% modulation)

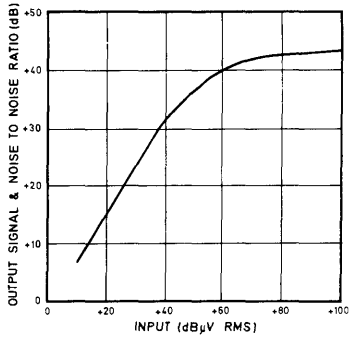


Fig. 5 Typical signal to noise ratio (S+N/N) with input signal (f=10.7MHz, 30% modulation)

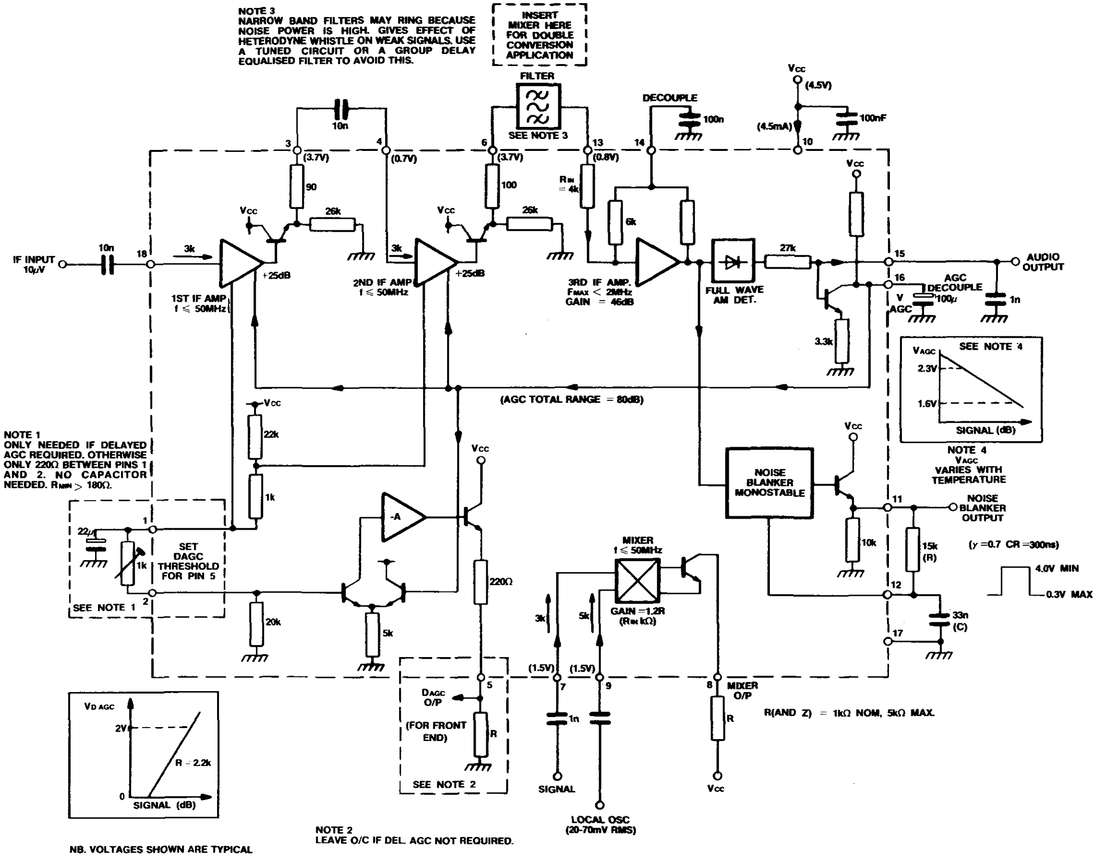


Fig.6 SL6700C Typical application circuit showing interfacing

PLESSEY
Semiconductors

TAB1042

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1042 is an advanced bipolar integrated circuit containing four separate programmable operational amplifiers. The four amplifiers are programmed by current into a common bias pin which determines the main characteristics of each amplifier, supply current, frequency response and slew rate.

For example, with a suitable choice of bias current, the TAB1042 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1042 is especially suitable for use in active filter applications.

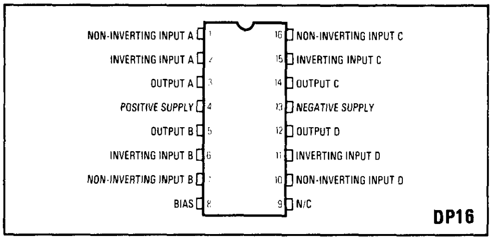


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Low Noise

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

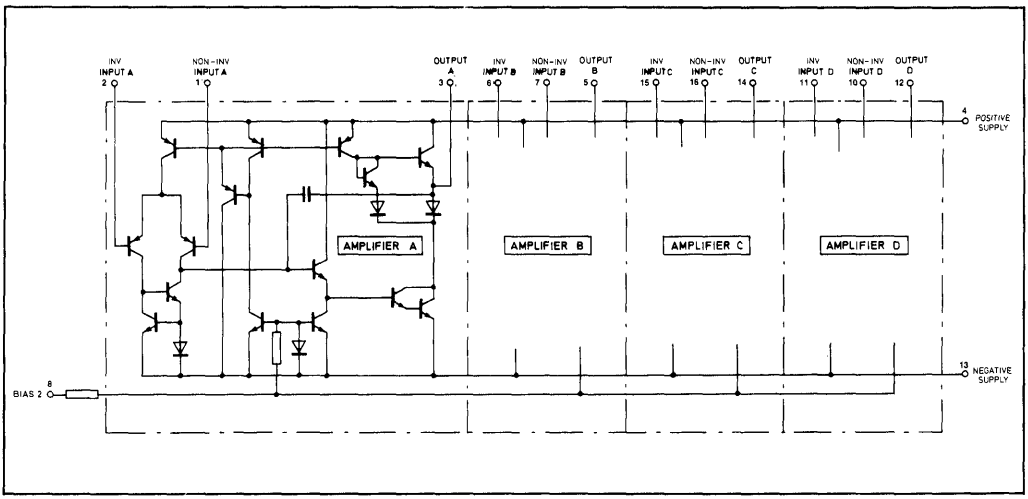


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 25°C
Operating mode A: Supply volts ±12V Bias set current 75μA
Operating mode B: Supply volts ±12V Bias set current 1μA
Operating mode C: Supply volts ±1.5V Bias set current 1μA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current (each amplifier)	1000	1600	2200		42		20	40	60	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A) RL = 100kΩ(B) RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL = 4kΩ(A) RL = 100kΩ(B) RL = 4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Gain bandwidth product					50			50		kHz	Gain = 20dB
		3.5								MHz	
Slew rate		1.5			0.02			0.02		V/μs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	fo = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	fo = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each amplifier)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

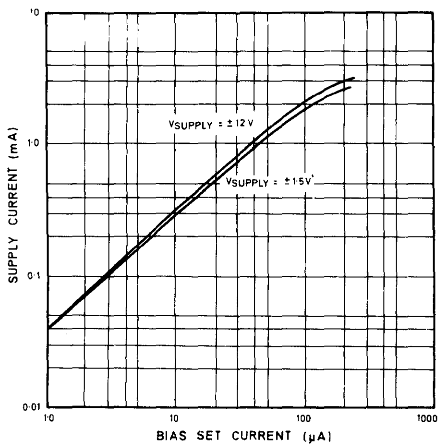


Fig.3 Supply current (each amplifier) v. bias set current

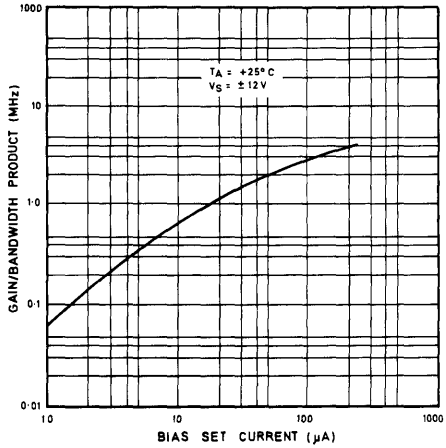


Fig. 4 Gain bandwidth product v. ISET

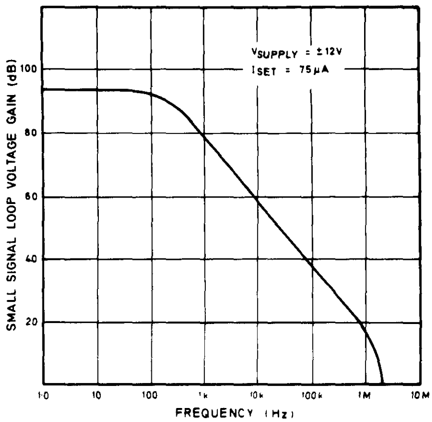


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage	-55°C to +125°C
Power dissipation	800mW at 25°C
	Derate at 7mW/°C above 25°C
Operating temperature range	-40°C to +85°C

PLESSEY
Semiconductors

TAB 1043

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1043 is an advanced bipolar integrated circuit containing four separate operational amplifiers. The amplifiers are programmed by current into the appropriate bias pin. Pin 8 (Bias 2) programmes amplifiers B, C and D and pin 16 (Bias 1) programmes amplifier A.

For example, with a suitable choice of bias current, the TAB1043 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1043 is especially suitable for use in active filter applications.

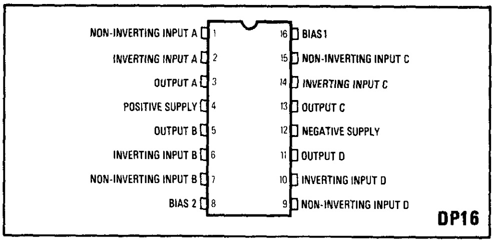


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Very Low Noise

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

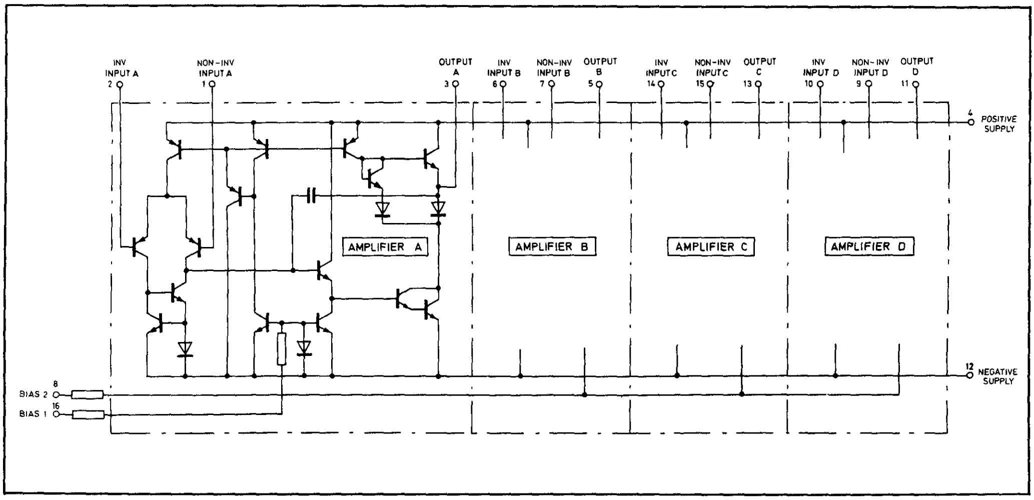


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A: Supply volts ±12V Bias set current 75µA
Operating mode B: Supply volts ±12V Bias set current 1µA
Operating mode C: Supply volts ±1.5V Bias set current 1µA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current (each amplifier)	1000	1600	2200		42		20	40	60	µA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Gain bandwidth product					50			50		kHz	Gain = 20dB
		3.5								MHz	
Slew rate		1.5			0.02			0.02		V/µs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	fo = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	fo = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each amplifier)	I_{SET} x 25µA
Slew rate	I_{SET} x 0.02 V/µs (I_{SET} in µA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10µA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

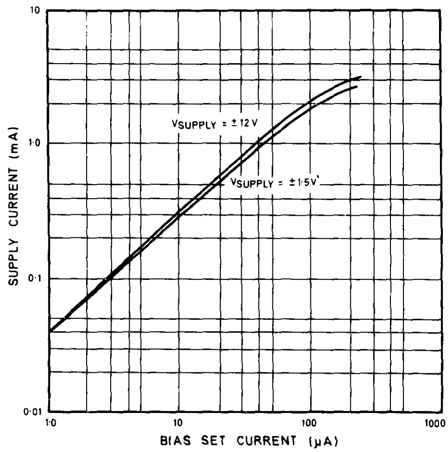


Fig.3 Supply current (each amplifier) v. bias set current

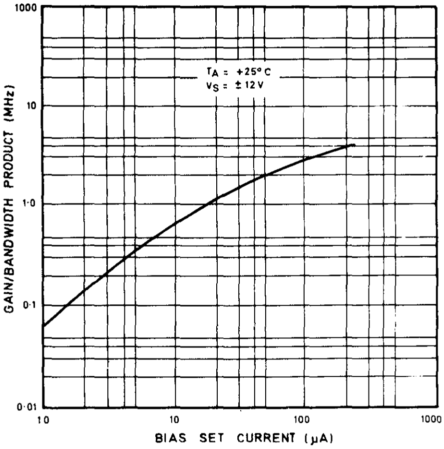


Fig. 4 Gain bandwidth product v. ISET

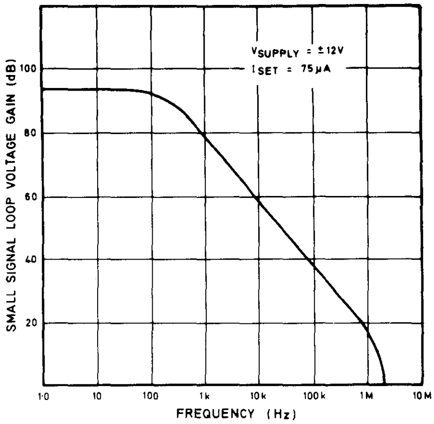
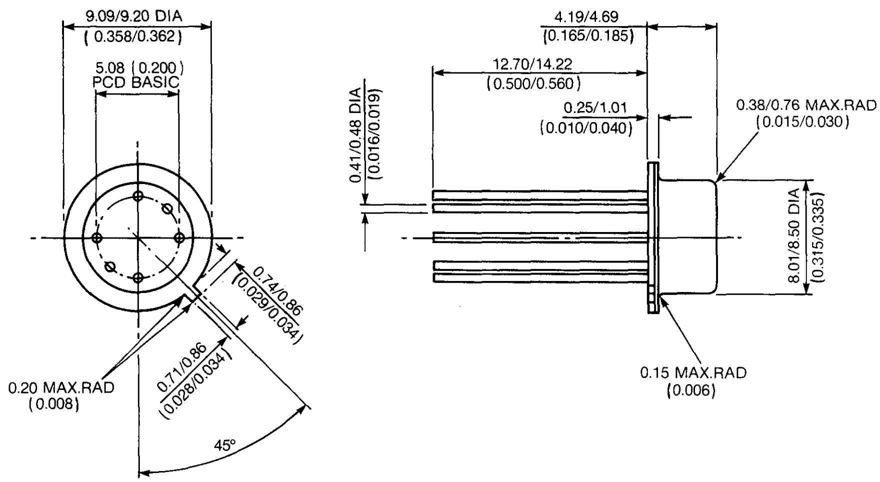


Fig. 5 Typical frequency response

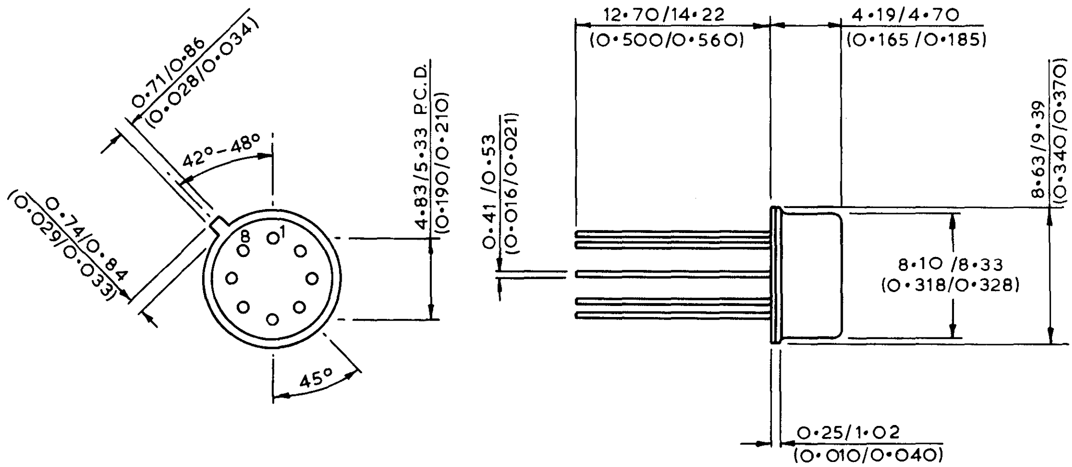
ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55°C to +125°C
Power dissipation	800mW at 25°C Derate at 7mW/°C above 25°C
Operating temperature range	-40°C to +85°C

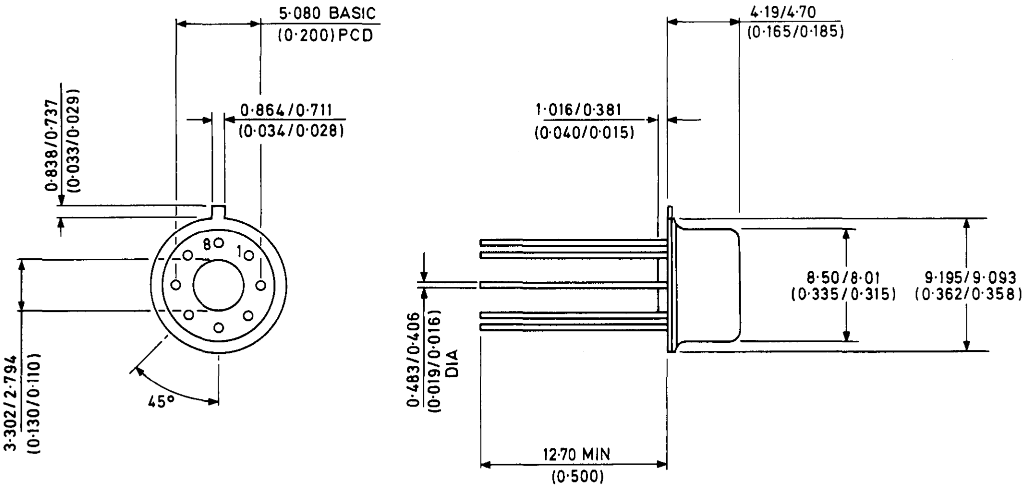
Package Outlines



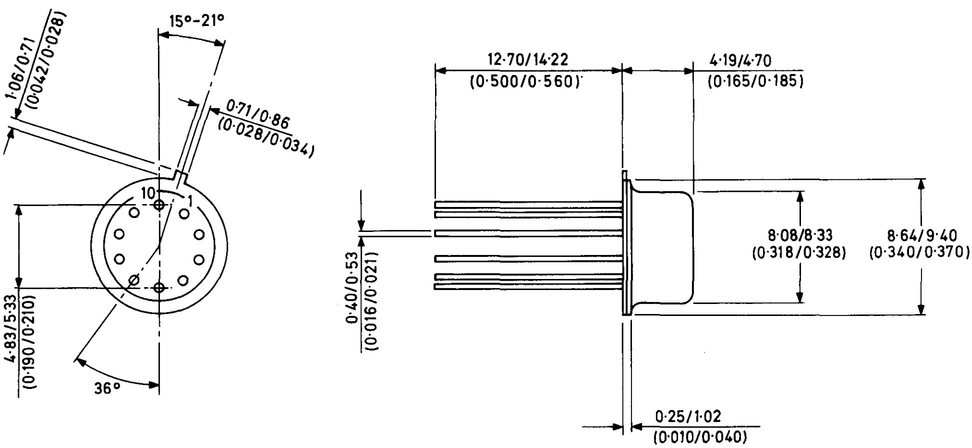
6 LEAD TO-5 - CM6



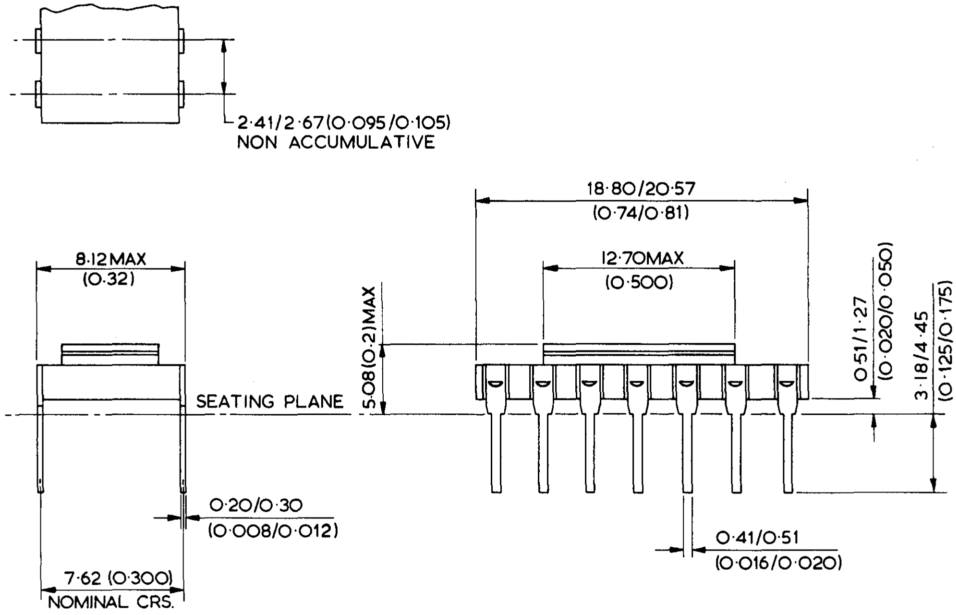
8 LEAD TO-5 (5.08 mm PCD) - CM8



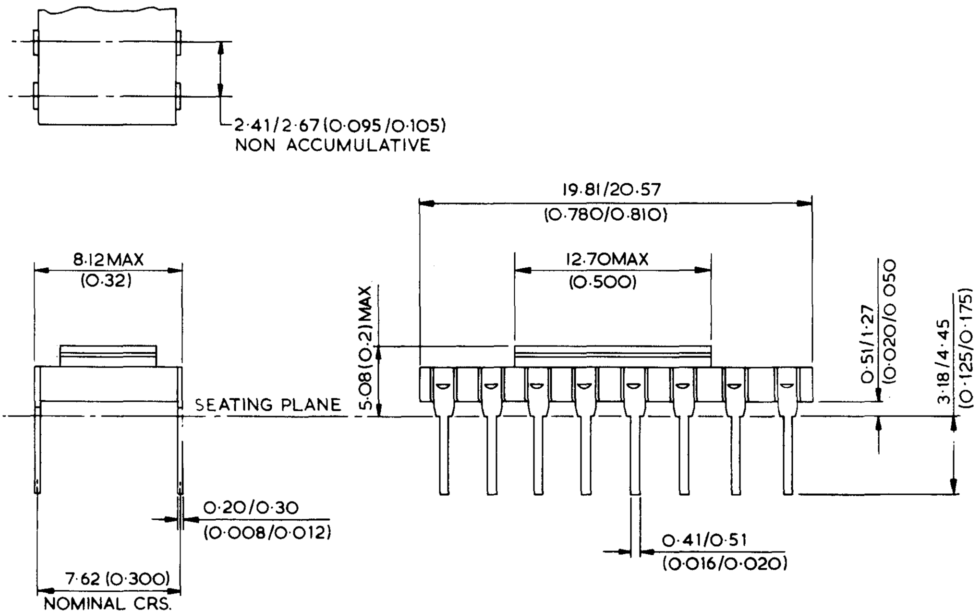
8 LEAD TO-5 (5.08 mm PCD) WITH STANDOFF - CM8/S
N.B. FOR SL1521 ONLY, PCD IS 5.84 BASIC (0.23)



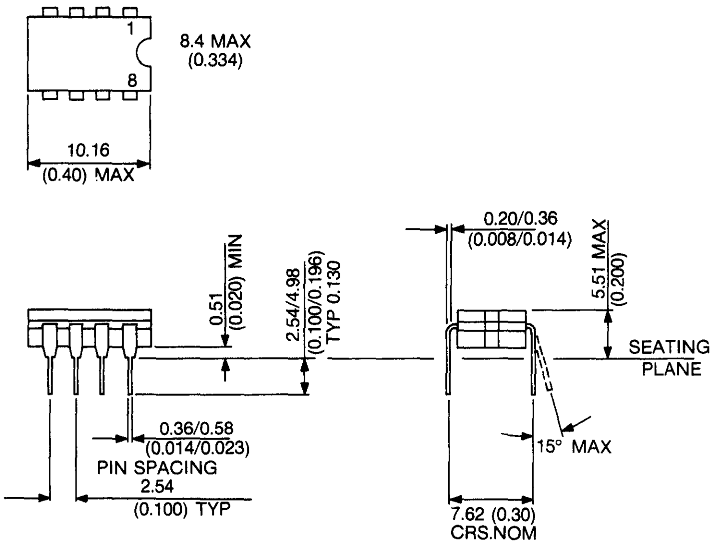
10 LEAD TO-5 - CM10



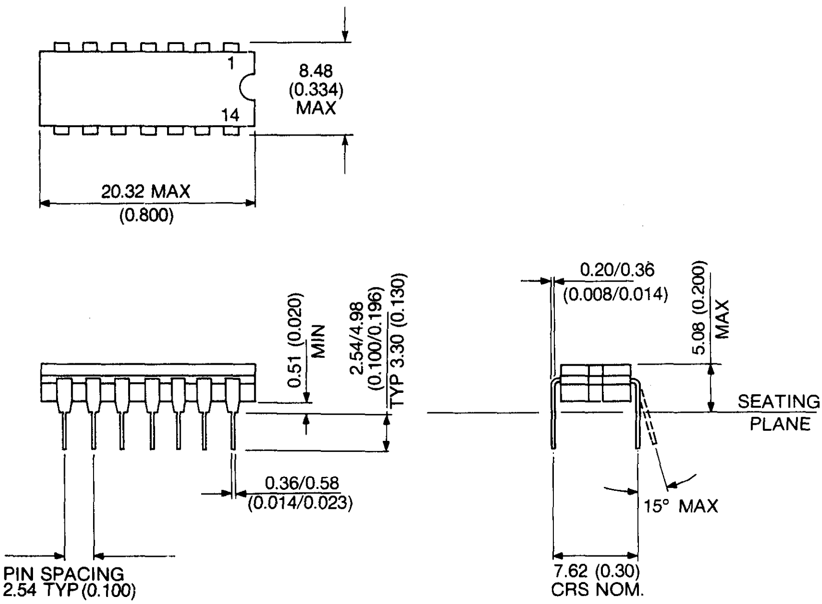
14 LEAD DILMON - DC14



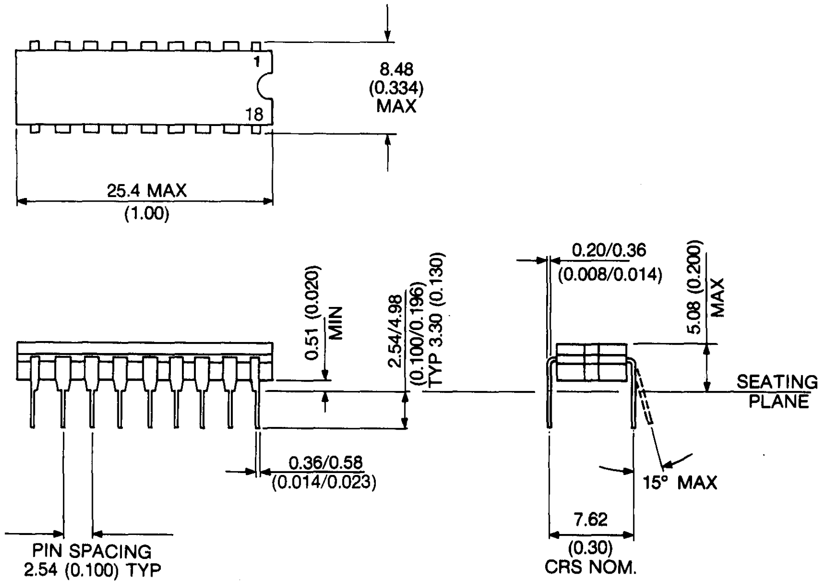
16 LEAD DILMON - DC16



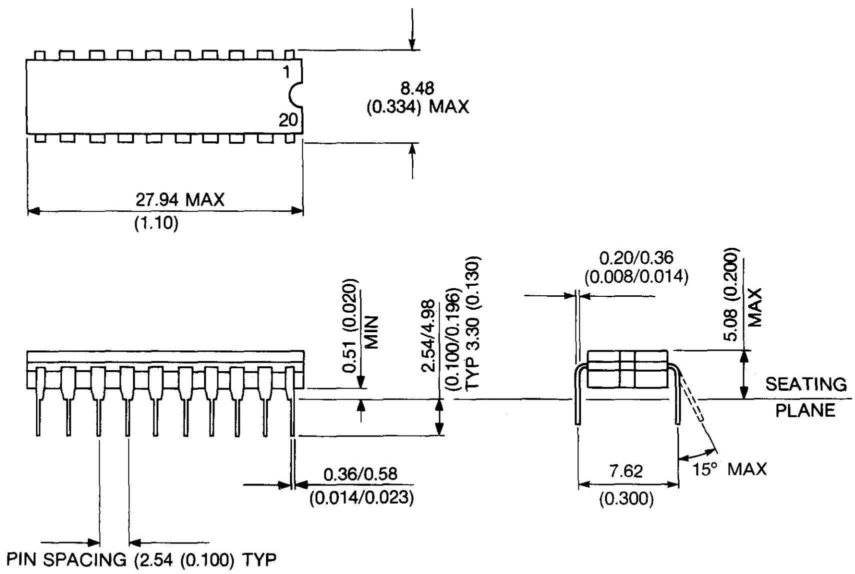
8 LEAD CERAMIC DIL
CERDIP - DG8



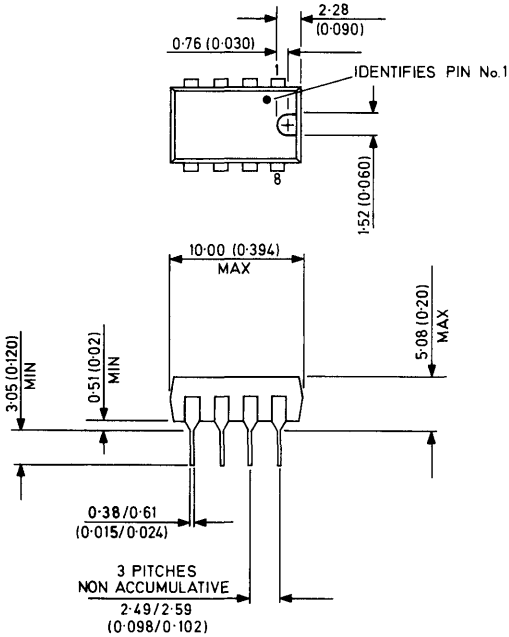
14 LEAD CERAMIC DIL
CERDIP - DG14

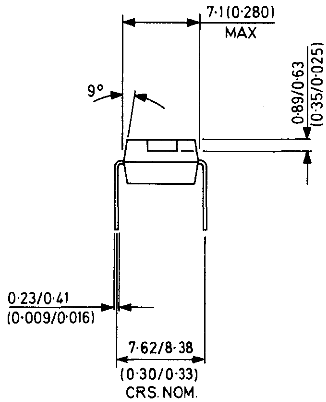


18 LEAD CERAMIC DIL
CERDIP - DG18

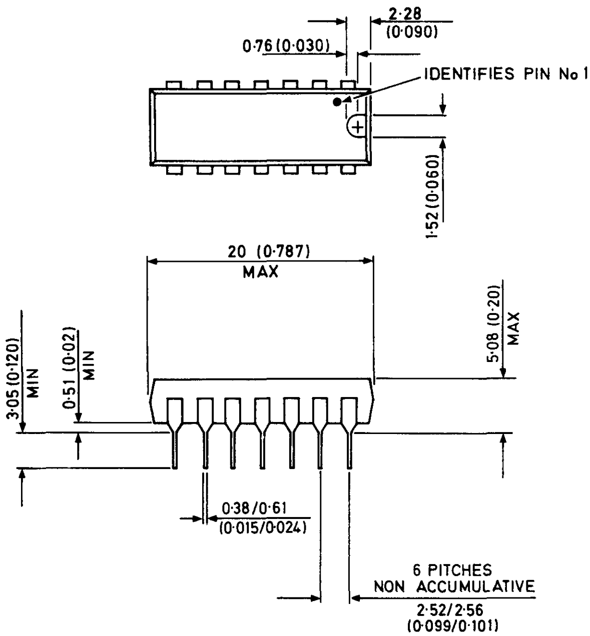


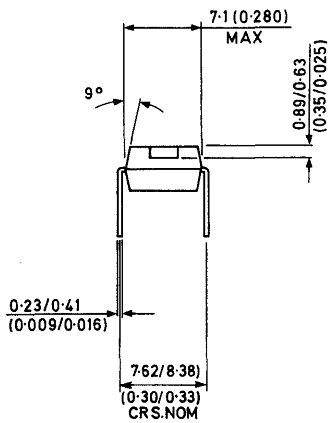
20 LEAD CERAMIC DIL
CERDIP - DG20



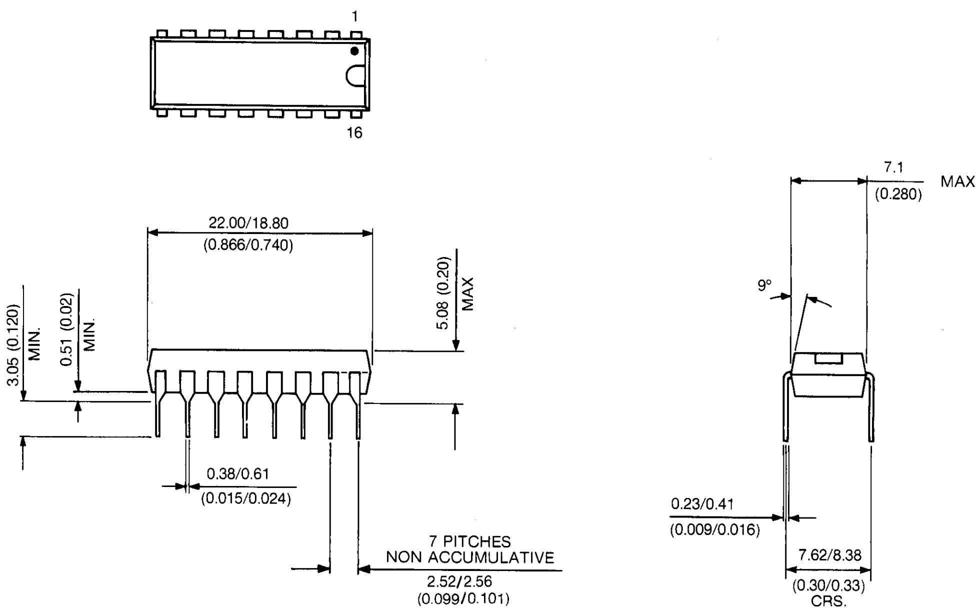


8-LEAD PLASTIC DIL - DP8

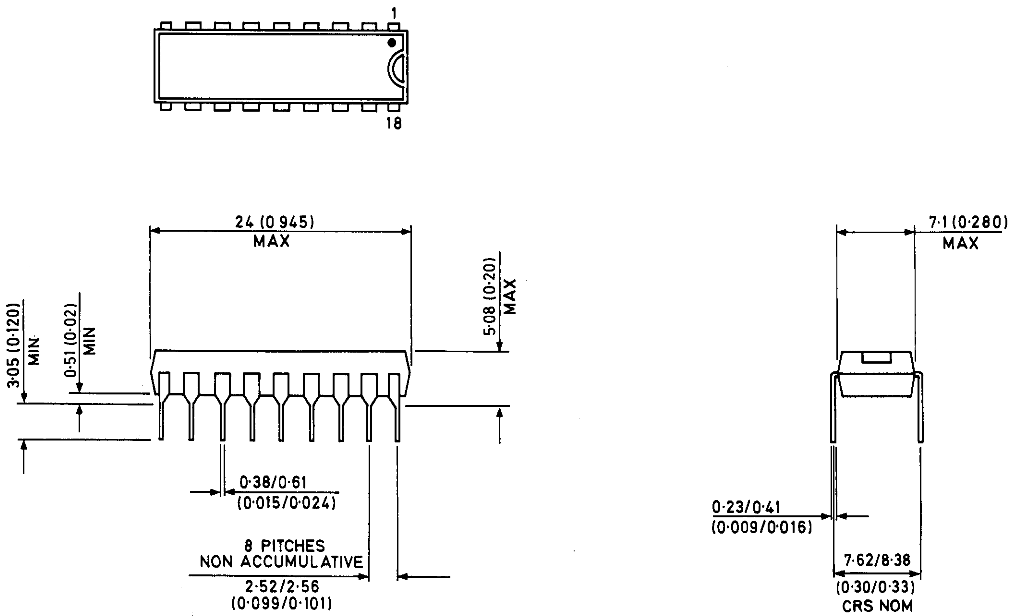




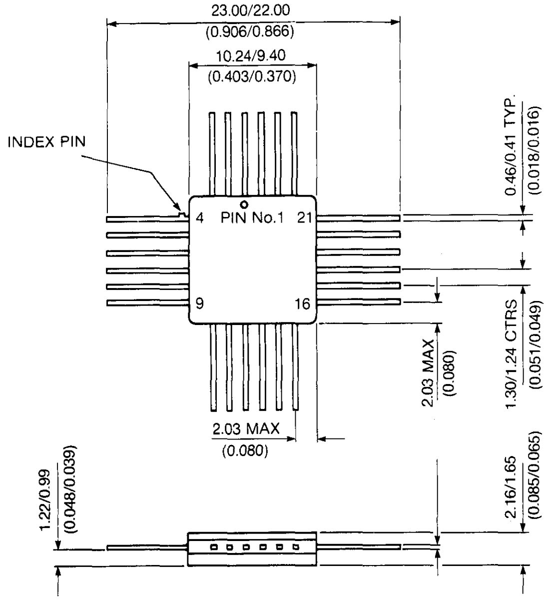
14-LEAD PLASTIC DIL - DP14



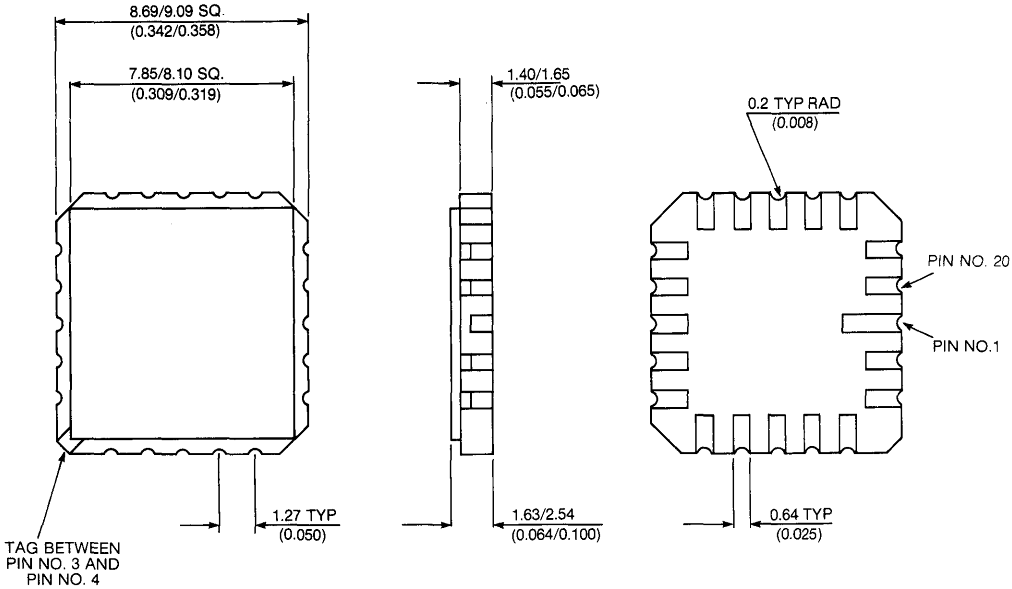
16-LEAD PLASTIC DIL - DP16



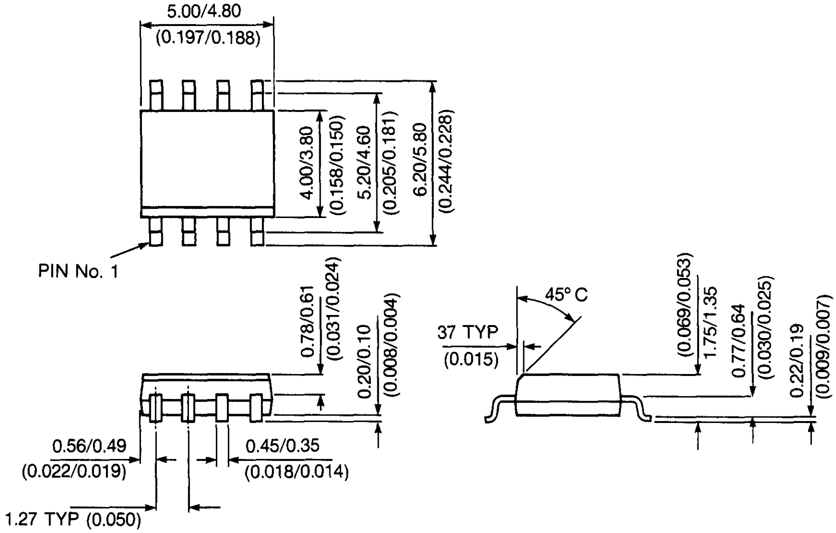
18 LEAD PLASTIC DIL - DP18



24 LEAD FLATPACK - GG24



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



SO-8 LEAD PLASTIC DIL PACKAGE - MP8

Ordering information

Ordering information

Plessey Semiconductors integrated circuits are allocated type numbers which take the following general form

WW XXXX Y/ZZ

where **WW** is a two-letter code identifying the product group and/or technology, **XXXX** is a three or four numeral code uniquely specifying the particular device, **Y** is a single letter which denotes the precise electrical or thermal specification for certain devices and **ZZ** is a two-letter code defining the package style. Digits **WW**, **XXXX** and **Y** must always be used when ordering; digits **ZZ** need only be used where a device is offered in more than one package style. For example, the **SL532C** is offered in **CM** (TO-5) and **LC** (hermetic chip carrier) packages so the full ordering number for this device in TO-5 package would be **SL523C/CM.**

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

A Pin-Grid Array
C Cylindrical
D Dual-in-Line (DIL)
F Flat Pack (leads on two sides)
G Flat Pack (leads on four sides)
Q Quad-in-Line

M Miniature (for Small Outline)
L Leadless Chip Carrier
H Leaded Chip Carrier
} Not yet designated by Pro-Electron

SECOND LETTER (indicates material)

C Metal-Ceramic (Metal Sealed)
G Glass-Ceramic (Glass Sealed)
M Metal
P Plastic
E Epoxy

Note: Gull-winged Quad Cerpac is a Flat Pack with leads on 4 sides hence it will be represented by GG.

Please Note:

Leadless Chip Carriers

LC Metal-Ceramic 3 Layer (Metal Sealed)
LG Glass-Sealed Ceramic
LE Epoxy-Sealed 1 Layer
LP Plastic

Leaded Chip Carriers

Where supplied without lead forming, flat pack rules apply. Where leads are bent under to form footprints equivalent to leadless chip carriers then use H.

e.g. **HG** Glass-Sealed Ceramic Leaded Chip Carrier (J Leaded Quad Cerpac)
HP Plastic Leaded Chip Carrier

Note: The above information refers generally to all Plessey Semiconductors integrated circuit products and does not necessarily apply to devices contained in this handbook.

Plessey Semiconductors World Wide

Sales offices

BELGIUM, NETHERLANDS, LUXEMBOURG	Plessey Semiconductors, Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100
FRANCE	Plessey Semiconductors, Z.A de Courtaboeuf, Rue du Quebec, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Tx: 692858F
ITALY	Plessey Trading SpA, Corso Garibaldi 70, 20121 Milan. Tel: 6596081 Tx: 331347
NORTH AMERICA	Plessey Semiconductors, 3 Whatney, Irvine, California 92718, USA. Tel: 714 951 5212 Twx: 701464 **See separate North American listings**
UNITED KINGDOM	Plessey Semiconductors Ltd., Cheney Manor, Swindon, Wiltshire SN2 2QW. Tel: (0793) 36251 Tx: 449637
WEST GERMANY, AUSTRIA, SWITZERLAND	Plessey GmbH, Altheimer Eck 10, 8000 Munchen 2, West Germany. Tel: 089 23 62-0 Tx: 0522197

Agents

ARGENTINA	Electroimpex SA, Guatemala 5991, (1425) Buenos Aires. Tel: 771-3773/722-9573
AUSTRALIA	Plessey Australia Pty Ltd., P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: 120384
EASTERN EUROPE	Plessey plc., Vicarage Lane, Ilford, Essex, England. Tel: 01 478 3040 Tx: 23166
GREECE	Plessey Company Ltd., Hadjigianni Mexi 2, Athens. Tel: 21 724 3000 Tx: 219251
	Mammeas, Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR
INDIA	Semiconductors Ltd., 809 Raheja Centre, Nariman Point, Bombay 400 021. Tel: 233999 Tx: 011-5414 CITO IN
	Semiconductors Ltd., Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739
	Semiconductors Ltd., 513, Ashoka Estate, 24, Barakhamba Road, Nf w Delhi — 110001. Tel: 44879 Tx: 31 3369
JAPAN	Cornes & Company Ltd., Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874
	Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496
HONG KONG	YES Products Ltd., Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444241-6 Tx: 36590
KOREA	Young O Ind Co. Ltd., Yeoevido, P.O. Box 149, Seoul. Tel: 782 1707 Tx: K25701
NEW ZEALAND	Plessey (NZ) Ltd., Te Pai Place, Henderson, Auckland 8. Tel: 8364189 Tx: NZ2851
SCANDINAVIA	
Denmark	Scansupply, Nannasgade 18-20, DK-2200 Copenhagen. Tel: 45 1 83 50 90 Tx: 19037
Finland	Oy Ferrado AB, P.O.Box 54, Valimontie 1, SF-00380 Helsinki 38. Tel: 90 55 00 02 Tx: 122214
Norway	Skandinavisk Elektronikk A/S, Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx: 71963
Sweden	Micronet AB, Odengatan 16, 114 24 Stockholm. Tel: 08/15 0230-31 Tx: 14725
SINGAPORE	Plessey Singapore Private Ltd., 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013
SOUTH AFRICA	Plessey South Africa Ltd., Forum Building, Struben Street, P.O.Box 2416, Pretoria 0001, Transvaal. Tel: (012) 3234511 Tx: 320277
SPAIN	JR Trading, Apartado de Correos 8432, Madrid 8. Tel: 248 12 18/248 38 82 Tx: 42701
TAIWAN	Artistex International Inc., Express Trade Building 3rd Floor, 56 Nanking Road East, Section 4 Taipei 105, (P.O.Box 59253, Taipei 105) Taiwan, Republic of China. Tel: 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446
THAILAND	Plessey Thailand, Rama Mansion 47, Sukhumvit Soi 12, Bangkok 11. Tel: 2526621 Tx: CHAVALIT TH2747
TURKEY	Turkelek Elektronic Co. Ltd., Hatay Sokak 8, Ankara. Tel: 90-41-25 21 09, 90-41-18 94 83 Tx: 42120
	Turkelek Elektronic Co. Ltd., Kemeralti Caddesi, Tophane Ishani 406, Istanbul. Tel: 90-1-143 12 68, 90-1-143 40 46 Tx: 22036
	Plessey M.M.E.R., Paris Caddesi 76/4, Kavaklidere, Ankara. Tel: 263820 Tx: 42061

Distributors

AUSTRIA	DAHMS Elektronik Ges. mbH, Wiener Str. 287, A-8051 Graz Tel: 0316/64030 Tx: 31099
BELGIUM	Master Chips, 4 St. Lazarus Laan, 1030 Brussels. Tel: 02 219 58 62 Tx: 62500
FRANCE	Mateleco, 66,Bd Augustin Dumont, 92240 Malakoff, Paris. Tel: 657 70 55 Mateleco Rhône-Alpes, 2 Rue Emile Zola, 38130 Echirolles. Tel: (76) 40 38 33 Tx: 980837 ICC, 78, Chemin Lanusse, Boîte postale n° 2147, 31200 Toulouse. Tel: (61) 26-14-10 Tx: 520897 F ICC, Z.A. du Haut Vigneau, Rue de la Source, 33170 Gradignan. Tel: (56) 31-17-17 Tx: 541539 F ICC, 9 bis, rue du Bas Champflour, 63019 Clermont Ferrand. Tel: (73) 91-70-77 Tx: 990928 F ICC, Z.A. Artizanord II, Lot 600 - bâtiment 19, Traverse de l'Oasis, 13015 Marseille. Tel: (91)-03-12-12 Tx: 441313 F
INDIA	Semiconductors Ltd., 809 Reheja Centre, Nariman Point, Bombay 400 021. Tel: 233999 Tx: 011 5415 CITO IN
ITALY	Melchioni, Via P. Colletta 39, 20135 Milan. Tel: 5794 Tx: 320321 Eurelettronica, Via Mascheroni 19, 20145 Milan. Tel: 498 18 51 Tx: 332102 Eurelettronica, Via Bertoloni 27, Rome. Tel: 875394 Tx: 610358
NETHERLANDS	Heynen B.V., Postbus 10, 6590 AA Gennep. Tel: 8851-99111 Tx: 37282
NEW ZEALAND	Professional Electronics Ltd., P.O.Box 31-143, Auckland. Tel: 493 029 Tx: 21084
SWITZERLAND	Aumann & Co. AG, Forrlibuckstrasse 150, CH-8037 Zurich. Tel: 01/443300 Tx: 822966
UNITED KINGDOM	Celdis Ltd., 37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171 Tx: 848370 Gothic Crellon Ltd., 380 Bath Road, Slough, Berkshire SL1 6JE. Tel: 06286 4300 Tx: 847571 Quarndon Electronics Ltd., Slack Lane, Derby DE3 3ED. Tel: 0332 32651 Tx: 37163 Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958 United Components Ltd., Victory Electronics Division, Unit 7, Crown Way, West Drayton, Middlesex UB7 8PS Tel: 01-573 6622 Tx: 8952920
WEST GERMANY	AS Electronic Vertriebs GmbH, Elisabethenstrasse 35, 6380 Bad Homburg Tel: 06172/2 90 28-29 Tx: 410868 Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708 Nordelektronik GmbH, Carl-Zeiss-Str. 6, 2085 Quickborn. Tel: 04106/72072 Tx: 214299

Iorth America

PLESSEY SALES REPRESENTATIVES:

ABAMA:	Huntsville	(205) 837-7363	E.M.A.
IIZONA:	Phoenix	(602) 252-0897	Chaparral Electronics
ıLIFORNIA:	San Diego	(619) 450-1754	CERCO
	Sacramento	(916) 442-2558	Ross Marketing Associates
	Santa Clara	(408) 998-8111	Ross Marketing Associates
	Tustin	(714) 731-9206	S.C. Cubed
	Thousand Oaks	(805) 496-7307	S.C. Cubed
ORIDA:	Almonte Springs	(305) 339-3855	Lawrence Associates
	Boca Raton	(305) 368-7373	Lawrence Associates
	Clearwater	(813) 584-8110	Lawrence Associates
	Melbourne	(305) 724-8294	Lawrence Associates
:ORGIA:	Atlanta	(404) 448-1215	E.M.A.
DIANA:	Fort Wayne	(219) 637-5548	Corrao Marsh
	Carmel	(317) 843-0739	Corrao Marsh
.INOIS:	Arlington Heights	(312) 956-1000	Micro Sales Inc.
WA:	Cedar Rapids	(319) 377-4666	Lorenz Sales Inc.
.NSAS:	Overland Park	(913) 541-8431	Kebco, Inc.
	Wichita	(316) 733-1301	Kebco, Inc.
\RYLAND:	Owings Mills	(301) 356-9500	Walker-Houck
\SSACHUSETTS:	Framingham	(617) 875-3266	Stone Components
CHIGAN:	Southfield	(313) 559-5363	Fred Gehrke & Associates
NNESOTA:	Bloomington	(612) 884-8291	Electronics Sales Agency
SSOURI:	St. Louis	(314) 576-4111	Kebco, Inc.
:BRASKA:	Lincoln	(402) 475-4660	Lorenz Sales Inc.
:VADA:	Reno	(702) 322-8299	Ross Marketing Associates
)UTH NEW JERSEY:	Marlton	(609) 428-2440	B.G.R. Associates
)RTH NEW JERSEY:	Hicksville	(516) 681-8746	Lorac Sales
:W YORK:	Hicksville	(516) 681-8746	Lorac Sales
	Skanaeteles	(315) 685-5731	Robtron Inc.
)RTH CAROLINA:	Raleigh	(919) 847-8800	E.M.A.
)UTH CAROLINA:	Greenville	(803) 233-4637	E.M.A.
IIO:	Cincinnati	(513) 729-1969	Stegman Blaine
	Vanadalia	(513) 890-7975	Stegman Blaine
	Westlake	(216) 871-0520	Stegman Blaine
IEGON:	Portland	(503) 620-8320	Crown Electronics
XAS:	Richardson	(214) 234-8438	Bonser-Phihower (B-F Sales)
\SHINGTON:	Bellevue	(206) 643-8100	Crown Electronic Sales Inc.
	Greenacres	(519) 624-4410	Crown Electronic Sales Inc.
SCONSIN:	Brookfield	(414) 781-1171	Micro Sales Inc.
	Menomonee Falls	(414) 251-0151	Micro Sales Inc.
.NADA EASTERN:	Rexdale	(416) 674-1330	Bestec Electronics Ltd.
	Montreal	(514) 484-2923	Eli Manis Inc.
.NADA WESTERN:	Burnaby	(604) 291-8866	R.A.E. Industrial Electronics

PLESSEY DISTRIBUTORS

LIFORNIA:	Irvine	(714) 951-5212	Plessy Solid State
NADA:	Mississauga	(416) 624-8300	G.E.C. Canada Ltd.

PLESSEY REGIONAL SALES OFFICES

Region
Veterans Memorial Hwy.
ral Islip, NY 11722
705922 PLESNY
582-8070
REDKO

New England District
132 Central Street, #212
Foxborough, MA 02035
(617) 543-3855
JOHN BEARCE

Southeast Region
499 Crane Roost Blvd. #235
Altamonte Springs, FL 32701
TLX 705185 PLESGA UD
(305) 339-6191
FRANK ABREU

Dixie District
1229 Johnson Terry Rd. #203
Marietta, GA 33067
(404) 973-8793
DON PAPESH

Chesapeake District
1932 Arlington Blvd. #217
Charlottsville, VA 22903
(804) 296-7229
AL REICHL

Midwest Region
1919 S. Highland Ave. #120C
Lombard, IL 60148
TLX 705186
(312) 953-1484
JON HILL

ral District
LBJ Freeway, #900
s, TX 75243
ink 821379
690-4930
BURDIN

Plains District Sales
1523 Towne Drive
Ellisville, MO 63011
(314) 527-4100
DOUG SCHMIESKORS

West Region
3 Whatney
Irvine, CA 92714
TWX 910-595-1930
TLX 701464 PLESSY
(714) 951-5212
LARRY FRANKFURT
Distribution Manager

Ohio Valley District
1717 E. 116th Street, #210
Carmel, Indiana 46032
(317) 843-0561
HARLAN WOODMANSEE

Northwest District
4633 Old Ironside Dr. #250
Santa Clara, CA 95054
TLX 705187
(408) 986-8911
STEVE BOLARIS

Southwest District
3 Whatney
Irvine, CA 92714
TWX 910-595-1930
TLX 701464 PLESSY
(714) 951-5212
DAN WOLFE

ıde U.S.A. Refer to PLESSY U.K. (0793) 36251