PCI 9656 Blue Book Revision 0.90 Corrections

This document details several corrections to the PCI 9656 Blue Book, revision 0.90. Please review these corrections before proceeding with your design.

1. Toggling IDDQEN# At Power On Time

> When using the PCI 9656AA, PCI 9656AB, PCI 9656AC, or PCI 9656AD, external logic is required on the IDDQEN# pin to configure the PCI buffers for proper operation. The requirement for this logic is not included in the Blue Book.

The IDDQEN# pin of the *PCI 9656AA, PCI 9656AB, PCI 9656AC, and PCI 9656AD* PLX part is a multiplexed pin with three functions:

1. It is used to identify main power present status for the $D3_{cold}$ function of Power Management.

2. It is used as an IDDQ enable to put the chip's output buffers into a quiescent state.

3. It is used to set a switch in the chip's PCI buffers for proper 3.3V and 5V operation.

The first two IDDQEN# functions are detailed in the Blue Book.

This third IDDQEN# function is *not* covered in the Blue Book.

The following details this third function of the IDDQEN# pin.

Please note that any designs using this silicon will need to include the IDDQEN# toggling logic detailed in this document.

PCI Buffer Voltage Selection

For the PCI buffers of the silicon to determine the PCI Bus voltage environment, the IDDQEN# input pin needs to transition from logic low (0) to logic high (1) after the chip powers up. As a result of this transition, a voltage comparator will latch the V_{io} voltage and configure a switch in the chip's PCI buffers for proper 3.3V and 5V signaling operation.

The specific requirements for this transition are as follows:

1. In order to guarantee that the chip's PCI buffers are stable, the transition must start after the chip receives full power.

2. In order to guarantee that the 3.3V and/or 5V tolerant circuitry is configured properly prior to driving any PCI signals, the transition must complete prior to the de-assertion of the chip's PCI RST# pin.

This transition should occur as quickly as possible. There is no slew rate requirement.

After the transition is complete, the IDDQEN# signal is free to be used for its other two functions as detailed in the Blue Book.

Two possible external logic implementations are illustrated in Figures 1 and 2. Figure 1 is an implementation that may be used in any design, and must be used for all designs that require the PCI Power Management $D3_{cold}$ support function. Figure 2 is an optional implementation for CompactPCI Hot Swap designs.

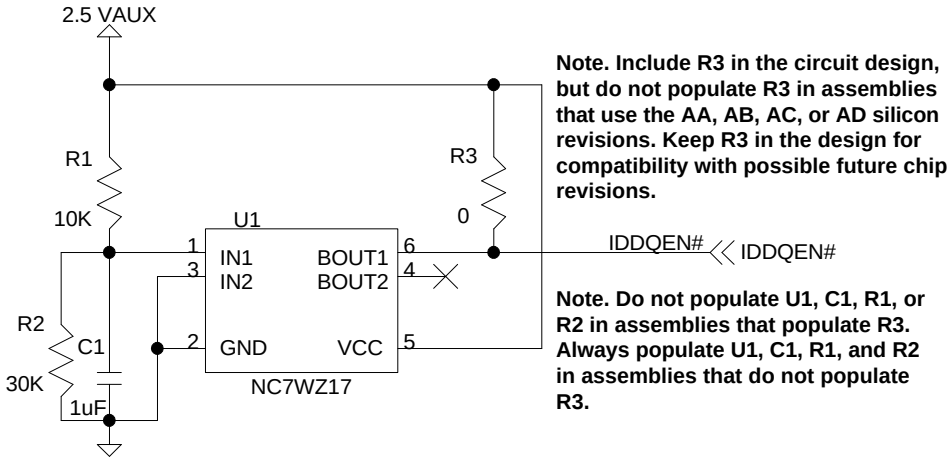

Figure #1. IDDQEN# transition logic at Boot Up. (PC-type PCI Implementations)

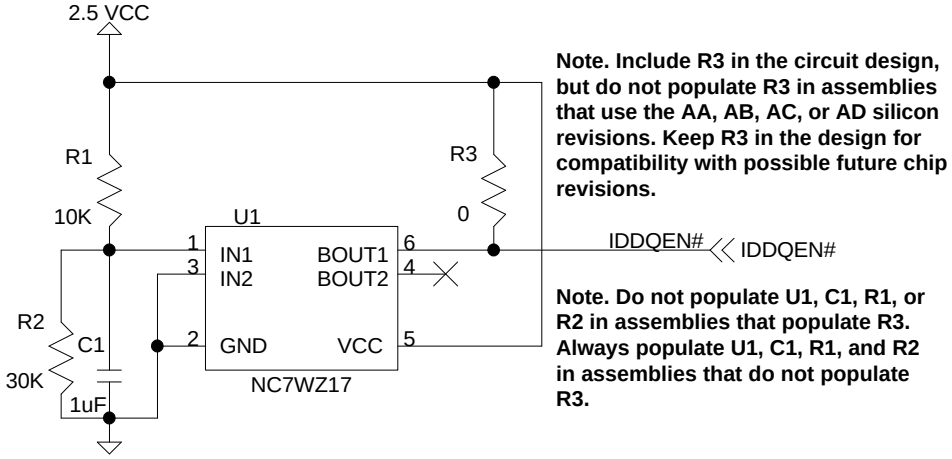

Figure #2. IDDQEN# transition logic at Boot Up. (CompactPCI Hot Swap Implementations)

2. USERi Pull-Up/Pull-Down At Power Up Time

When using the PCI 9656, an external pull-up or pull-down resistor is required on the USERi pin to configure the chip for the desired PCI bus behavior during chip initialization. A pull-up resistor configures the chip to issue PCI Retries during initialization [high = retry], and a pull-down resistor configures the chip to do nothing on the PCI bus during initialization. This is true for the PCI 9656AC and PCI 9656AD. The description in the Blue Book regarding this is incorrect for these chip revisions. It is not true for the PCI 9656AA or PCI 9656AB.

The following text replaces sections 2.4.1.2 and 4.4.1.2 of the Blue Book.

2.4.1.2/4.4.1.2 Local Initialization

As stated in *PCI r2.*2, Section 3.5.1.1:

"If the target is accessed during initialization-time, it is allowed to do any of the following:

1. Ignore the request (except if it is a boot device). This results in a Master Abort.

2. Claim the access and hold in wait sates until it can complete the request, not to exceed the end of initialization-time.

3. Claim the access and terminate with [PCI] Retry."

The PCI 9656 supports Option 1 (*Initially Not Respond*), and Option 3 (*Initially Retry*), above. For CompactPCI Hot Swap live insertion systems, the preferred method for the silicon is usually not to respond to PCI Configuration accesses during initialization. For legacy systems, Retries are usually preferred for compatibility reasons. However, it is ultimately the designer's choice of which option to use.

The PCI 9656 determines the option to use as follows:

The USERi pin is sampled at the rising edge RST# to determine the selected PCI Bus response mode during local initialization. If USERi is low (through an external 1K ohm pull-down resistor), the PCI 9656 does not respond to PCI activity until the device's Local Bus initialization is complete. This results in a Master Abort (the preferred method for CompactPCI Hot Swap systems). If USERi is high (through an external 1K—4.7K ohm pull-up resistor), the PCI 9656 responds to PCI accesses with PCI Retry cycles until the device's Local Bus initialization is complete. Local Bus initialization is complete when the Local Init Status bit is set (LMISC1[2]=1).

The LMISC1[2] bit can be programmed in one of three ways:

1. By a Local Bus master writing a 1 directly to LMISC1[2].

2. By the serial EEPROM specifying a value of 1 for LMISC1[2] during a serial EEPROM load.

3. If a Local Bus Master is not present and either a serial EEPROM is not present or a blank serial EEPROM is present, the PCI 9656 reverts to its power on/reset default register values and sets this bit. (Refer to Table 2-18 on page 2-9.)

During run time, USERi can be used as a general purpose input as described in the Tables 12-10, 12-11, and 12-12, for the M, C, and J mode Local Bus pins.

Refer to Section 9, "CompactPCI Hot Swap" for specifics on using this feature in *PICMG 2.1, R2.0* systems.

3. EEDI/EEDO Pull-Up When Local Processor Present But EEPROM Not Present

When using the PCI 9656, if initialization is to be performed by a Local Bus master and no serial EEPROM is present, the EEDI/EEDO pin must *not* be pulled down. This is true for all versions of the PCI 9656: PCI 9656AA, PCI 9656AB, PCI 9656AC, and PCI 9656AD. The description in the Blue Book regarding this is vague.

Tables 2-18 and 4-18 of the Blue Book make no mention of a pull-up or pull-down resistor on the EEDI/EEDO pin when a Local Processor is present but an EEPROM is not present. The correct requirement is that the EEDI/EEDO pin must be either be left floating or pulled up with a 1K-ohm or greater value resistor when an EEPROM is not present. In any case, the pin must *not* be pulled down.

The following shows the corrected entry of Tables 2-18 and 4-18:

Table 2-18/4-18. Serial EEPROM Guidelines

Local Processor	Serial EEPROM	System Boot Condition
		...
Present	None	The Local Processor programs the PCI 9656 registers, then sets the Local Init Status bit (LMISC1[2] = 1). A 1K ohm or greater pull-up resistor on EEDI/EEDO is recommended, but not required. The EEDI/EEDO pin already has an internal pull-up (ref. Table 12-1). ***Note:*** *Some systems may avoid configuring devices that do not complete configuration accesses within 2^{25} PCI clocks after RST# has been de-asserted. In addition, some systems may hang if Direct Slave reads and writes are immediately retried. The value of the Direct Slave Retry Delay Clocks (LBRD0[31:28]) may resolve the hang by delaying assertion of the STOP# signal by the PCI 9656.*
		...

4. Updated Electrical Specifications

The following table updates the Electrical Specifications for the PCI 9656AA, PCI 9656AB, PCI 9656AC, and PCI 9656AD. Changes from the Blue Book are underlined.

Table 13-5. Electrical Characteristics Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}[1]	Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12.0 mA	2.4	-	V
V_{OL}[1]	Output Low Voltage		I_{OL} = 12.0 mA	-	0.4	V
V_{OH}[2]	Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0 mA	2.4	-	V
V_{OL}[2]	Output Low Voltage		I_{OL} = 24.0 mA	-	0.4	V
V_{IH}	Input High Level	-	-	2.0	5.5	V
V_{IL}	Input Low Level	-	-	-0.5	0.8	V
V_{OH3}	PCI 3.3V Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -500 µA	0.9 V_{DD}	-	V
V_{OL3}	PCI 3.3V Output Low Voltage		I_{OL} = 1500 µA	-	0.1 V_{DD}	V
V_{IH3}	PCI 3.3V Input High Level	-	-	0.5 V_{DD}	V_{DD}+0.5	V
V_{IL3}	PCI 3.3V Input Low Level	-	-	-0.5	0.3 V_{DD}	V
I_{II}	Input Leakage Current	V_{SS} = V_{IN} = V_{DD}, V_{DD} = Max		-10	+10	µA
I_{LPC}[3]	DC Current Per Pin During Pre-charge	V_P = 0.8 to 1.2V		-	1.0	mA
I_{OZ}	Three-State Output Leakage Current	V_{DD} = Max		-10	+10	µA
I_{DD}[4] (I/O Ring)	Power Supply Current for I/O Ring	I/O Ring V_{DD} = 3.6V, PCLK = 66MHz, LCLK = 66MHz		-	95	mA
I_{DD} (Core)	Power Supply Current for Core	Core V_{DD} = 2.63V, PCLK = 66MHz, LCLK = 66MHz		-	185	mA
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max, V_{IN} = GND or V_{CC}		-	50	µA

Notes:
1. For 12 mA I/O or output cells (Local Bus side).
2. For 24 mA I/O or output cells (Local Bus side).
3. I_{LPC} is the DC current flowing from VDD to Ground during pre-charge, as both PMOS and NMOS devices remain on during pre-charge. It is not the leakage current flowing into or out of the pin under pre-charge.
4. 40 Local Bus side I/Os switching simultaneously and 76 PCI side I/Os switching simultaneously.

5. PCI Arbiter Enable/Disable

When using the PCI 9656, the configuration register bit that is used to enable or disable the PCI 9656's PCI Arbiter can only be written by the EEPROM or a Local Bus master. A PCI master cannot be write this bit. This is true for all versions of the PCI 9656: PCI 9656AA, PCI 9656AB, PCI 9656AC, and PCI 9656AD. The description in the Blue Book regarding this is incorrect.

Register 11-57 of the Blue Book incorrectly states that the PCI Arbiter Enable bit (PCIARB[0]) can be written by a PCI master. In fact, a PCI master cannot write the PCI Arbiter Enable bit.

The following shows the corrected entry of Register 11-57:

Register 11-57. (PCIARB; PCI:100h, LOC:1A0h) PCI Arbiter Control

Bit	Description	Read	Write	Value after Reset
0	**PCI Arbiter Enable.** Value of 0 indicates the PCI arbiter is disabled and REQ0# and GNT0# are used by the PCI 9656 to acquire PCI Bus use. Value of 1 indicates the PCI arbiter is enabled.	Yes	Local/ Serial EEPROM	0
...				

6. PCI BAR's 4 & 5 Unused

For Direct Slave data transfers, the PCI 9656 supports mapping two PCI address spaces to the Local Bus using PCI Base Address Registers (BAR's) 2 and 3. The Blue Book PCI Configuration Register table regarding this is potentially confusing.

Table 11-2 of the Blue Book could be interpreted to indicate that the PCI 9656 supports mapping four PCI address spaces to the Local Bus for Direct Slave data transfers. The PCI 9656 in fact only supports mapping two PCI address spaces.

The following shows the corrected entries of Table 11-2.

Table 11-2. PCI Configuration Registers

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9656 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI/ Local Writeable	Serial EEPROM Writeable
...				
20h	20h	PCI Base Address 4; unused	Y	N
24h	24h	PCI Base Address 5; unused	Y	N
...				

7. Big Endian/Little Endian/Byte Lane Mode

The Blue Book descriptions of Big Endian and Little Endian conversion are potentially confusing.

PCI 9656 Big Endian and Little Endian conversion are detailed in Blue Book sections 2.3 and 4.3. The following tables provide further clarification by detailing precisely PCI 9656 signal mappings between the PCI bus and the Local Bus during Big Endian and Little Endian conversion.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	C Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD0	1-LD0	1-LD0	1-LD24	1-LD8	1-LD0
AD33	AD1	1-LD1	1-LD1	1-LD1	1-LD25	1-LD9	1-LD1
AD34	AD2	1-LD2	1-LD2	1-LD2	1-LD26	1-LD10	1-LD2
AD35	AD3	1-LD3	1-LD3	1-LD3	1-LD27	1-LD11	1-LD3
AD36	AD4	1-LD4	1-LD4	1-LD4	1-LD28	1-LD12	1-LD4
AD37	AD5	1-LD5	1-LD5	1-LD5	1-LD29	1-LD13	1-LD5
AD38	AD6	1-LD6	1-LD6	1-LD6	1-LD30	1-LD14	1-LD6
AD39	AD7	1-LD7	1-LD7	1-LD7	1-LD31	1-LD15	1-LD7
AD40	AD8	1-LD8	1-LD8	2-LD0	1-LD16	1-LD0	2-LD0
AD41	AD9	1-LD9	1-LD9	2-LD1	1-LD17	1-LD1	2-LD1
AD42	AD10	1-LD10	1-LD10	2-LD2	1-LD18	1-LD2	2-LD2
AD43	AD11	1-LD11	1-LD11	2-LD3	1-LD19	1-LD3	2-LD3
AD44	AD12	1-LD12	1-LD12	2-LD4	1-LD20	1-LD4	2-LD4
AD45	AD13	1-LD13	1-LD13	2-LD5	1-LD21	1-LD5	2-LD5
AD46	AD14	1-LD14	1-LD14	2-LD6	1-LD22	1-LD6	2-LD6
AD47	AD15	1-LD15	1-LD15	2-LD7	1-LD23	1-LD7	2-LD7
AD48	AD16	1-LD16	2-LD0	3-LD0	1-LD8	2-LD8	3-LD0
AD48	AD17	1-LD17	2-LD1	3-LD1	1-LD9	2-LD9	3-LD1
AD50	AD18	1-LD18	2-LD2	3-LD2	1-LD10	2-LD10	3-LD2
AD51	AD19	1-LD19	2-LD3	3-LD3	1-LD11	2-LD11	3-LD3
AD52	AD20	1-LD20	2-LD4	3-LD4	1-LD12	2-LD12	3-LD4
AD53	AD21	1-LD21	2-LD5	3-LD5	1-LD13	2-LD13	3-LD5
AD54	AD22	1-LD22	2-LD6	3-LD6	1-LD14	2-LD14	3-LD6
AD55	AD23	1-LD23	2-LD7	3-LD7	1-LD15	2-LD15	3-LD7
AD56	AD24	1-LD24	2-LD8	4-LD0	1-LD0	2-LD0	4-LD0
AD57	AD25	1-LD25	2-LD9	4-LD1	1-LD1	2-LD1	4-LD1
AD58	AD26	1-LD26	2-LD10	4-LD2	1-LD2	2-LD2	4-LD2
AD59	AD27	1-LD27	2-LD11	4-LD3	1-LD3	2-LD3	4-LD3
AD60	AD28	1-LD28	2-LD12	4-LD4	1-LD4	2-LD4	4-LD4
AD61	AD29	1-LD29	2-LD13	4-LD5	1-LD5	2-LD5	4-LD5
AD62	AD30	1-LD30	2-LD14	4-LD6	1-LD6	2-LD6	4-LD6
AD63	AD31	1-LD31	2-LD15	4-LD7	1-LD7	2-LD7	4-LD7

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD5" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD5 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD5 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	C Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD0	1-LD16	1-LD24	1-LD24	1-LD24	1-LD24
AD33	AD1	1-LD1	1-LD17	1-LD25	1-LD25	1-LD25	1-LD25
AD34	AD2	1-LD2	1-LD18	1-LD26	1-LD26	1-LD26	1-LD26
AD35	AD3	1-LD3	1-LD19	1-LD27	1-LD27	1-LD27	1-LD27
AD36	AD4	1-LD4	1-LD20	1-LD28	1-LD28	1-LD28	1-LD28
AD37	AD5	1-LD5	1-LD21	1-LD29	1-LD29	1-LD29	1-LD29
AD38	AD6	1-LD6	1-LD22	1-LD30	1-LD30	1-LD30	1-LD30
AD39	AD7	1-LD7	1-LD23	1-LD31	1-LD31	1-LD31	1-LD31
AD40	AD8	1-LD8	1-LD24	2-LD24	1-LD16	1-LD16	2-LD24
AD41	AD9	1-LD9	1-LD25	2-LD25	1-LD17	1-LD17	2-LD25
AD42	AD10	1-LD10	1-LD26	2-LD26	1-LD18	1-LD18	2-LD26
AD43	AD11	1-LD11	1-LD27	2-LD27	1-LD19	1-LD19	2-LD27
AD44	AD12	1-LD12	1-LD28	2-LD28	1-LD20	1-LD20	2-LD28
AD45	AD13	1-LD13	1-LD29	2-LD29	1-LD21	1-LD21	2-LD29
AD46	AD14	1-LD14	1-LD30	2-LD30	1-LD22	1-LD22	2-LD30
AD47	AD15	1-LD15	1-LD31	2-LD31	1-LD23	1-LD23	2-LD31
AD48	AD16	1-LD16	2-LD16	3-LD24	1-LD8	2-LD24	3-LD24
AD48	AD17	1-LD17	2-LD17	3-LD25	1-LD9	2-LD25	3-LD25
AD50	AD18	1-LD18	2-LD18	3-LD26	1-LD10	2-LD26	3-LD26
AD51	AD19	1-LD19	2-LD19	3-LD27	1-LD11	2-LD27	3-LD27
AD52	AD20	1-LD20	2-LD20	3-LD28	1-LD12	2-LD28	3-LD28
AD53	AD21	1-LD21	2-LD21	3-LD29	1-LD13	2-LD29	3-LD29
AD54	AD22	1-LD22	2-LD22	3-LD30	1-LD14	2-LD30	3-LD30
AD55	AD23	1-LD23	2-LD23	3-LD31	1-LD15	2-LD31	3-LD31
AD56	AD24	1-LD24	2-LD24	4-LD24	1-LD0	2-LD16	4-LD24
AD57	AD25	1-LD25	2-LD25	4-LD25	1-LD1	2-LD17	4-LD25
AD58	AD26	1-LD26	2-LD26	4-LD26	1-LD2	2-LD18	4-LD26
AD59	AD27	1-LD27	2-LD27	4-LD27	1-LD3	2-LD19	4-LD27
AD60	AD28	1-LD28	2-LD28	4-LD28	1-LD4	2-LD20	4-LD28
AD61	AD29	1-LD29	2-LD29	4-LD29	1-LD5	2-LD21	4-LD29
AD62	AD30	1-LD30	2-LD30	4-LD30	1-LD6	2-LD22	4-LD30
AD63	AD31	1-LD31	2-LD31	4-LD31	1-LD7	2-LD23	4-LD31

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD21" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD21 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD21 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	J Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LAD0	1-LAD0	1-LAD0	1-LAD24	1-LAD8	1-LAD0
AD33	AD1	1-LAD1	1-LAD1	1-LAD1	1-LAD25	1-LAD9	1-LAD1
AD34	AD2	1-LAD2	1-LAD2	1-LAD2	1-LAD26	1-LAD10	1-LAD2
AD35	AD3	1-LAD3	1-LAD3	1-LAD3	1-LAD27	1-LAD11	1-LAD3
AD36	AD4	1-LAD4	1-LAD4	1-LAD4	1-LAD28	1-LAD12	1-LAD4
AD37	AD5	1-LAD5	1-LAD5	1-LAD5	1-LAD29	1-LAD13	1-LAD5
AD38	AD6	1-LAD6	1-LAD6	1-LAD6	1-LAD30	1-LAD14	1-LAD6
AD39	AD7	1-LAD7	1-LAD7	1-LAD7	1-LAD31	1-LAD15	1-LAD7
AD40	AD8	1-LAD8	1-LAD8	2-LAD0	1-LAD16	1-LAD0	2-LAD0
AD41	AD9	1-LAD9	1-LAD9	2-LAD1	1-LAD17	1-LAD1	2-LAD1
AD42	AD10	1-LAD10	1-LAD10	2-LAD2	1-LAD18	1-LAD2	2-LAD2
AD43	AD11	1-LAD11	1-LAD11	2-LAD3	1-LAD19	1-LAD3	2-LAD3
AD44	AD12	1-LAD12	1-LAD12	2-LAD4	1-LAD20	1-LAD4	2-LAD4
AD45	AD13	1-LAD13	1-LAD13	2-LAD5	1-LAD21	1-LAD5	2-LAD5
AD46	AD14	1-LAD14	1-LAD14	2-LAD6	1-LAD22	1-LAD6	2-LAD6
AD47	AD15	1-LAD15	1-LAD15	2-LAD7	1-LAD23	1-LAD7	2-LAD7
AD48	AD16	1-LAD16	2-LAD0	3-LAD0	1-LAD8	2-LAD8	3-LAD0
AD48	AD17	1-LAD17	2-LAD1	3-LAD1	1-LAD9	2-LAD9	3-LAD1
AD50	AD18	1-LAD18	2-LAD2	3-LAD2	1-LAD10	2-LAD10	3-LAD2
AD51	AD19	1-LAD19	2-LAD3	3-LAD3	1-LAD11	2-LAD11	3-LAD3
AD52	AD20	1-LAD20	2-LAD4	3-LAD4	1-LAD12	2-LAD12	3-LAD4
AD53	AD21	1-LAD21	2-LAD5	3-LAD5	1-LAD13	2-LAD13	3-LAD5
AD54	AD22	1-LAD22	2-LAD6	3-LAD6	1-LAD14	2-LAD14	3-LAD6
AD55	AD23	1-LAD23	2-LAD7	3-LAD7	1-LAD15	2-LAD15	3-LAD7
AD56	AD24	1-LAD24	2-LAD8	4-LAD0	1-LAD0	2-LAD0	4-LAD0
AD57	AD25	1-LAD25	2-LAD9	4-LAD1	1-LAD1	2-LAD1	4-LAD1
AD58	AD26	1-LAD26	2-LAD10	4-LAD2	1-LAD2	2-LAD2	4-LAD2
AD59	AD27	1-LAD27	2-LAD11	4-LAD3	1-LAD3	2-LAD3	4-LAD3
AD60	AD28	1-LAD28	2-LAD12	4-LAD4	1-LAD4	2-LAD4	4-LAD4
AD61	AD29	1-LAD29	2-LAD13	4-LAD5	1-LAD5	2-LAD5	4-LAD5
AD62	AD30	1-LAD30	2-LAD14	4-LAD6	1-LAD6	2-LAD6	4-LAD6
AD63	AD31	1-LAD31	2-LAD15	4-LAD7	1-LAD7	2-LAD7	4-LAD7

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LAD5" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LAD5 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LAD5 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	J Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LAD0	1-LAD16	1-LAD24	1-LAD24	1-LAD24	1-LAD24
AD33	AD1	1-LAD1	1-LAD17	1-LAD25	1-LAD25	1-LAD25	1-LAD25
AD34	AD2	1-LAD2	1-LAD18	1-LAD26	1-LAD26	1-LAD26	1-LAD26
AD35	AD3	1-LAD3	1-LAD19	1-LAD27	1-LAD27	1-LAD27	1-LAD27
AD36	AD4	1-LAD4	1-LAD20	1-LAD28	1-LAD28	1-LAD28	1-LAD28
AD37	AD5	1-LAD5	1-LAD21	1-LAD29	1-LAD29	1-LAD29	1-LAD29
AD38	AD6	1-LAD6	1-LAD22	1-LAD30	1-LAD30	1-LAD30	1-LAD30
AD39	AD7	1-LAD7	1-LAD23	1-LAD31	1-LAD31	1-LAD31	1-LAD31
AD40	AD8	1-LAD8	1-LAD24	2-LAD24	1-LAD16	1-LAD16	2-LAD24
AD41	AD9	1-LAD9	1-LAD25	2-LAD25	1-LAD17	1-LAD17	2-LAD25
AD42	AD10	1-LAD10	1-LAD26	2-LAD26	1-LAD18	1-LAD18	2-LAD26
AD43	AD11	1-LAD11	1-LAD27	2-LAD27	1-LAD19	1-LAD19	2-LAD27
AD44	AD12	1-LAD12	1-LAD28	2-LAD28	1-LAD20	1-LAD20	2-LAD28
AD45	AD13	1-LAD13	1-LAD29	2-LAD29	1-LAD21	1-LAD21	2-LAD29
AD46	AD14	1-LAD14	1-LAD30	2-LAD30	1-LAD22	1-LAD22	2-LAD30
AD47	AD15	1-LAD15	1-LAD31	2-LAD31	1-LAD23	1-LAD23	2-LAD31
AD48	AD16	1-LAD16	2-LAD16	3-LAD24	1-LAD8	2-LAD24	3-LAD24
AD48	AD17	1-LAD17	2-LAD17	3-LAD25	1-LAD9	2-LAD25	3-LAD25
AD50	AD18	1-LAD18	2-LAD18	3-LAD26	1-LAD10	2-LAD26	3-LAD26
AD51	AD19	1-LAD19	2-LAD19	3-LAD27	1-LAD11	2-LAD27	3-LAD27
AD52	AD20	1-LAD20	2-LAD20	3-LAD28	1-LAD12	2-LAD28	3-LAD28
AD53	AD21	1-LAD21	2-LAD21	3-LAD29	1-LAD13	2-LAD29	3-LAD29
AD54	AD22	1-LAD22	2-LAD22	3-LAD30	1-LAD14	2-LAD30	3-LAD30
AD55	AD23	1-LAD23	2-LAD23	3-LAD31	1-LAD15	2-LAD31	3-LAD31
AD56	AD24	1-LAD24	2-LAD24	4-LAD24	1-LAD0	2-LAD16	4-LAD24
AD57	AD25	1-LAD25	2-LAD25	4-LAD25	1-LAD1	2-LAD17	4-LAD25
AD58	AD26	1-LAD26	2-LAD26	4-LAD26	1-LAD2	2-LAD18	4-LAD26
AD59	AD27	1-LAD27	2-LAD27	4-LAD27	1-LAD3	2-LAD19	4-LAD27
AD60	AD28	1-LAD28	2-LAD28	4-LAD28	1-LAD4	2-LAD20	4-LAD28
AD61	AD29	1-LAD29	2-LAD29	4-LAD29	1-LAD5	2-LAD21	4-LAD29
AD62	AD30	1-LAD30	2-LAD30	4-LAD30	1-LAD6	2-LAD22	4-LAD30
AD63	AD31	1-LAD31	2-LAD31	4-LAD31	1-LAD7	2-LAD23	4-LAD31

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LAD21" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LAD21 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LAD21 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	M Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD31	1-LD31	1-LD31	1-LD7	1-LD23	1-LD31
AD33	AD1	1-LD30	1-LD30	1-LD30	1-LD6	1-LD22	1-LD30
AD34	AD2	1-LD29	1-LD29	1-LD29	1-LD5	1-LD21	1-LD29
AD35	AD3	1-LD28	1-LD28	1-LD28	1-LD4	1-LD20	1-LD28
AD36	AD4	1-LD27	1-LD27	1-LD27	1-LD3	1-LD19	1-LD27
AD37	AD5	1-LD26	1-LD26	1-LD26	1-LD2	1-LD18	1-LD26
AD38	AD6	1-LD25	1-LD25	1-LD25	1-LD1	1-LD17	1-LD25
AD39	AD7	1-LD24	1-LD24	1-LD24	1-LD0	1-LD16	1-LD24
AD40	AD8	1-LD23	1-LD23	2-LD31	1-LD15	1-LD31	2-LD31
AD41	AD9	1-LD22	1-LD22	2-LD30	1-LD14	1-LD30	2-LD30
AD42	AD10	1-LD21	1-LD21	2-LD29	1-LD13	1-LD29	2-LD29
AD43	AD11	1-LD20	1-LD20	2-LD28	1-LD12	1-LD28	2-LD28
AD44	AD12	1-LD19	1-LD19	2-LD27	1-LD11	1-LD27	2-LD27
AD45	AD13	1-LD18	1-LD18	2-LD26	1-LD10	1-LD26	2-LD26
AD46	AD14	1-LD17	1-LD17	2-LD25	1-LD9	1-LD25	2-LD25
AD47	AD15	1-LD16	1-LD16	2-LD24	1-LD8	1-LD24	2-LD24
AD48	AD16	1-LD15	2-LD31	3-LD31	1-LD23	2-LD23	3-LD31
AD48	AD17	1-LD14	2-LD30	3-LD30	1-LD22	2-LD22	3-LD30
AD50	AD18	1-LD13	2-LD29	3-LD29	1-LD21	2-LD21	3-LD29
AD51	AD19	1-LD12	2-LD28	3-LD28	1-LD20	2-LD20	3-LD28
AD52	AD20	1-LD11	2-LD27	3-LD27	1-LD19	2-LD19	3-LD27
AD53	AD21	1-LD10	2-LD26	3-LD26	1-LD18	2-LD18	3-LD26
AD54	AD22	1-LD9	2-LD25	3-LD25	1-LD17	2-LD17	3-LD25
AD55	AD23	1-LD8	2-LD24	3-LD24	1-LD16	2-LD16	3-LD24
AD56	AD24	1-LD7	2-LD23	4-LD31	1-LD31	2-LD31	4-LD31
AD57	AD25	1-LD6	2-LD22	4-LD30	1-LD30	2-LD30	4-LD30
AD58	AD26	1-LD5	2-LD21	4-LD29	1-LD29	2-LD29	4-LD29
AD59	AD27	1-LD4	2-LD20	4-LD28	1-LD28	2-LD28	4-LD28
AD60	AD28	1-LD3	2-LD19	4-LD27	1-LD27	2-LD27	4-LD27
AD61	AD29	1-LD2	2-LD18	4-LD26	1-LD26	2-LD26	4-LD26
AD62	AD30	1-LD1	2-LD17	4-LD25	1-LD25	2-LD25	4-LD25
AD63	AD31	1-LD0	2-LD16	4-LD24	1-LD24	2-LD24	4-LD24

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD26" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD26 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD26 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	M Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD31	1-LD15	1-LD7	1-LD7	1-LD7	1-LD7
AD33	AD1	1-LD30	1-LD14	1-LD6	1-LD6	1-LD6	1-LD6
AD34	AD2	1-LD29	1-LD13	1-LD5	1-LD5	1-LD5	1-LD5
AD35	AD3	1-LD28	1-LD12	1-LD4	1-LD4	1-LD4	1-LD4
AD36	AD4	1-LD27	1-LD11	1-LD3	1-LD3	1-LD3	1-LD3
AD37	AD5	1-LD26	1-LD10	1-LD2	1-LD2	1-LD2	1-LD2
AD38	AD6	1-LD25	1-LD9	1-LD1	1-LD1	1-LD1	1-LD1
AD39	AD7	1-LD24	1-LD8	1-LD0	1-LD0	1-LD0	1-LD0
AD40	AD8	1-LD23	1-LD7	2-LD7	1-LD15	1-LD15	2-LD7
AD41	AD9	1-LD22	1-LD6	2-LD6	1-LD14	1-LD14	2-LD6
AD42	AD10	1-LD21	1-LD5	2-LD5	1-LD13	1-LD13	2-LD5
AD43	AD11	1-LD20	1-LD4	2-LD4	1-LD12	1-LD12	2-LD4
AD44	AD12	1-LD19	1-LD3	2-LD3	1-LD11	1-LD11	2-LD3
AD45	AD13	1-LD18	1-LD2	2-LD2	1-LD10	1-LD10	2-LD2
AD46	AD14	1-LD17	1-LD1	2-LD1	1-LD9	1-LD9	2-LD1
AD47	AD15	1-LD16	1-LD0	2-LD0	1-LD8	1-LD8	2-LD0
AD48	AD16	1-LD15	2-LD15	3-LD7	1-LD23	2-LD7	3-LD7
AD48	AD17	1-LD14	2-LD14	3-LD6	1-LD22	2-LD6	3-LD6
AD50	AD18	1-LD13	2-LD13	3-LD5	1-LD21	2-LD5	3-LD5
AD51	AD19	1-LD12	2-LD12	3-LD4	1-LD20	2-LD4	3-LD4
AD52	AD20	1-LD11	2-LD11	3-LD3	1-LD19	2-LD3	3-LD3
AD53	AD21	1-LD10	2-LD10	3-LD2	1-LD18	2-LD2	3-LD2
AD54	AD22	1-LD9	2-LD9	3-LD1	1-LD17	2-LD1	3-LD1
AD55	AD23	1-LD8	2-LD8	3-LD0	1-LD16	2-LD0	3-LD0
AD56	AD24	1-LD7	2-LD7	4-LD7	1-LD31	2-LD15	4-LD7
AD57	AD25	1-LD6	2-LD6	4-LD6	1-LD30	2-LD14	4-LD6
AD58	AD26	1-LD5	2-LD5	4-LD5	1-LD29	2-LD13	4-LD5
AD59	AD27	1-LD4	2-LD4	4-LD4	1-LD28	2-LD12	4-LD4
AD60	AD28	1-LD3	2-LD3	4-LD3	1-LD27	2-LD11	4-LD3
AD61	AD29	1-LD2	2-LD2	4-LD2	1-LD26	2-LD10	4-LD2
AD62	AD30	1-LD1	2-LD1	4-LD1	1-LD25	2-LD9	4-LD1
AD63	AD31	1-LD0	2-LD0	4-LD0	1-LD24	2-LD8	4-LD0

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD10" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD10 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD10 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

8. Local Bus Pause Timer Count Must Be Even (MARBR[8] = 0)

The Blue Book includes a description of the Local Bus Pause Timer in the MARBR register (Register Description 11-40). For the PCI 9656AD, the Local Bus Pause Timer count must be even (MARBR[8] = 0). This restriction is not included in the Blue Book description. For the PCI 9656AA, PCI 9656AB, and PCI 9656AC, this count may be odd or even (MARBR[8] = 0 or 1).

The PCI 9656 includes a Local Bus Pause Timer (MARBR[15:8]) for specifying how long to stay off of the Local Bus between transfers to/from the Local Bus during DMA. For the PCI 9656AD, this count must be even (MARBR[8] = 0). Note that this counter is 0 after reset, so the only time this correction is of concern is if the Local Bus Pause Timer count is ever changed from its reset value.

For the PCI 9656AA, PCI 9656AB, and PCI 9656AC, this count may be odd or even (MARBR[8] = 0 or 1).

9. ALE Output Delay Timing For Any Local Bus Clock Rate

The Blue Book includes tables 13-3 and 13-4 that show the ALE output delay timing to the Processor/Local Bus clock for clock rates of 33MHz and 66MHz, respectively. It does not show the output delay timing for other clock rates.

The following table shows the PCI 9656AD ALE output delay timing for any Processor/Local Bus clock rate. It replaces Figures 13-3 and 13-4 in the Blue Book. LC_{HIGH} is the time in ns that the Processor/Local Bus clock is high.

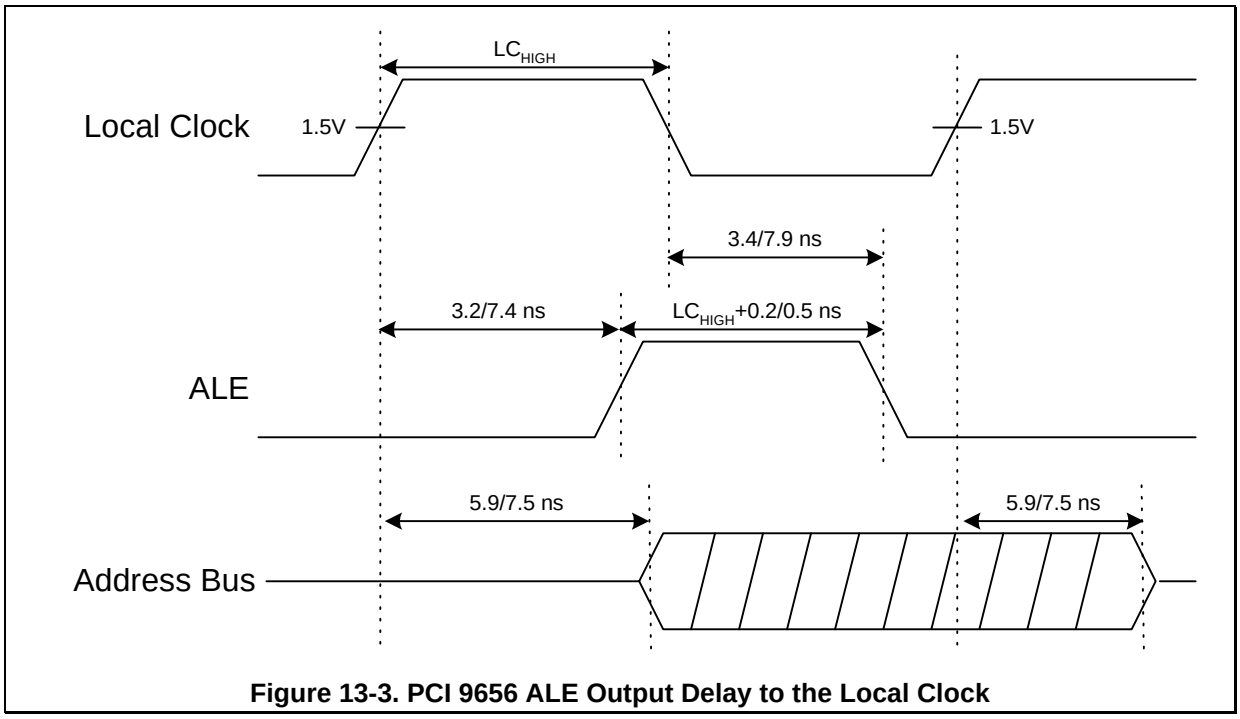

Figure 13-3. PCI 9656 ALE Output Delay to the Local Clock